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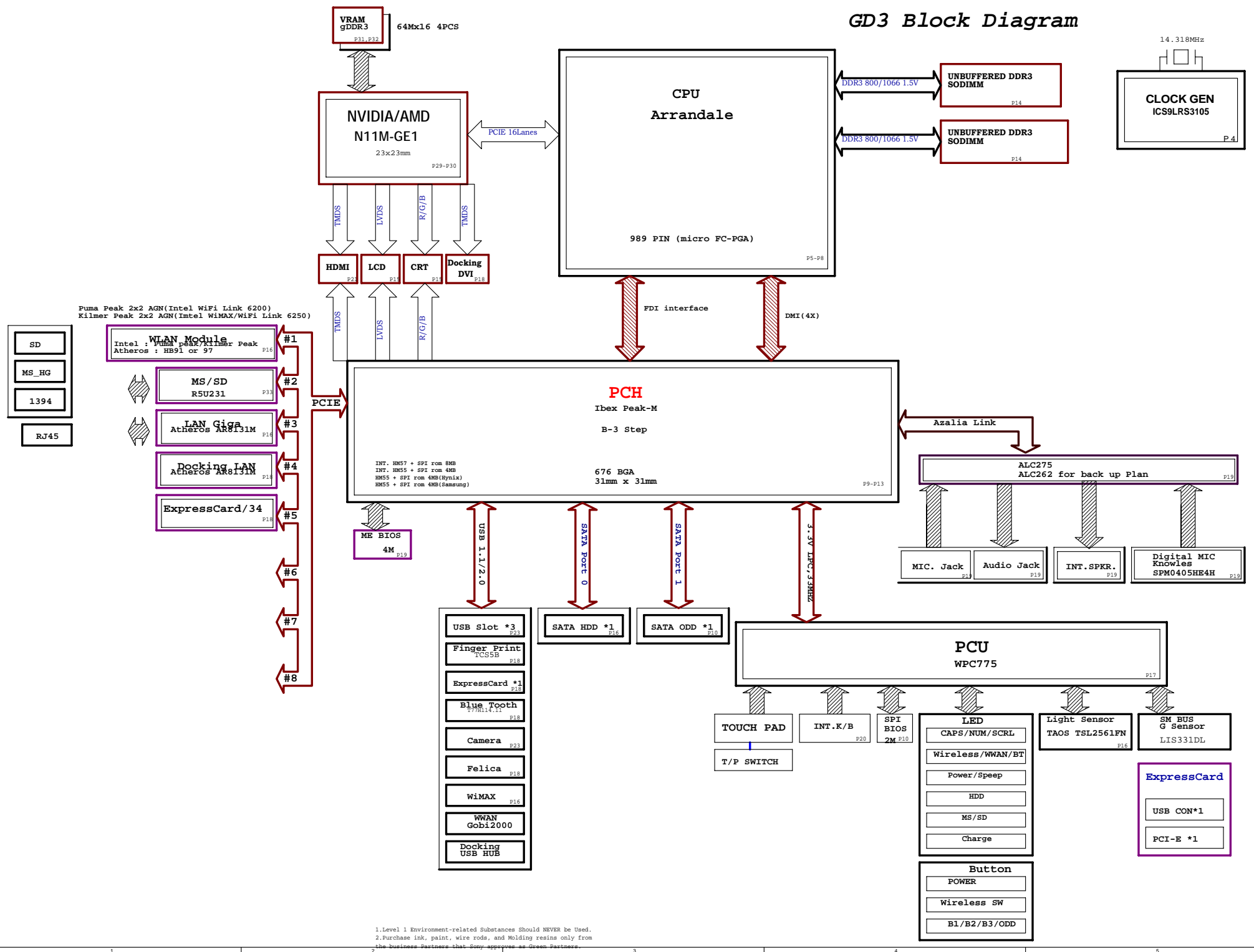


**QUANTA
COMPUTER**

Title: **Page List**

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GD3 Block Diagram




1. Level 1 Environment-related Substances Should NEVER be Used.
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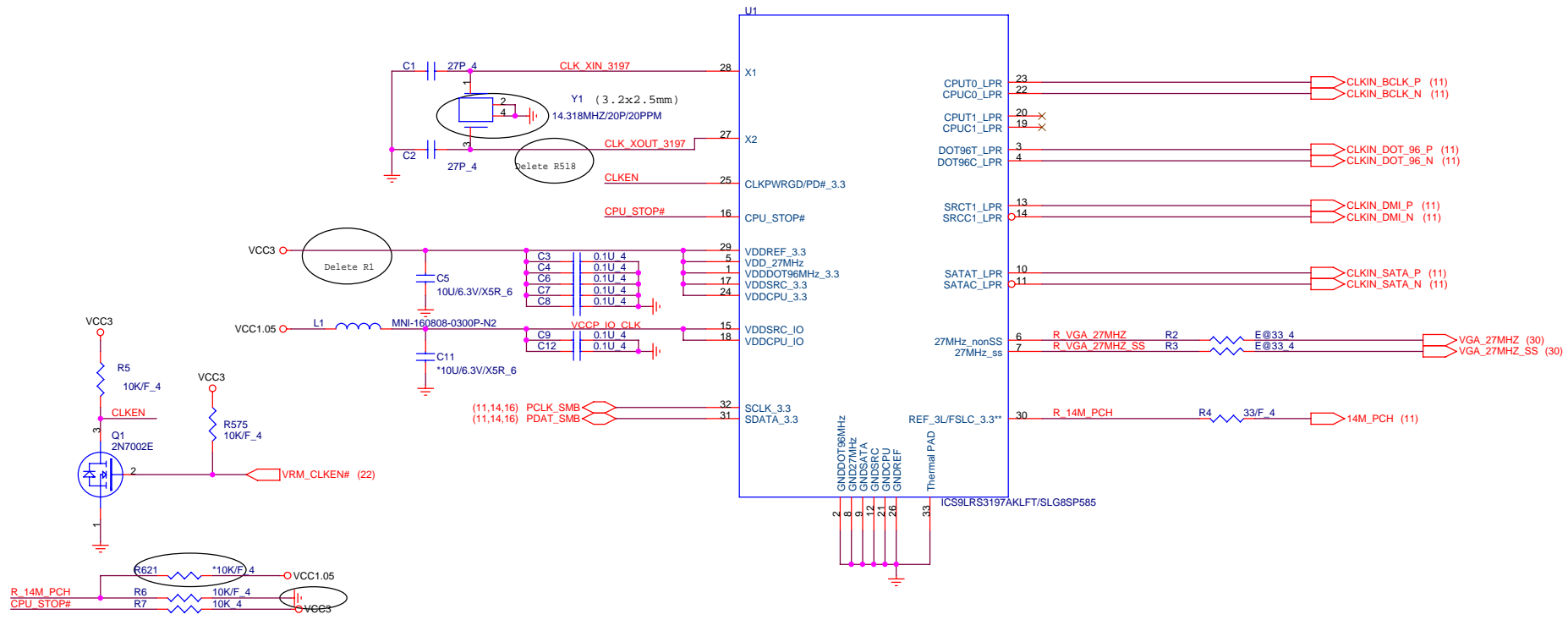
DVT change list

0708:
 -P4 Delete R518 0 ohm.
 -P4 Delete R1
 -P4 Y1 change pin assignment.
 -P4 Add R621
 -P4 R6 change PU to PD and mount 10K.
 -P5 Add Q67 2N7002.(For GFX PROCHOT)
 -P5 U2.AN15 add GFX_PROHOT Net.(For GFX_PROCHOT)
 -P9 R567 no mount(Driver from EC)
 -P10 R152 change from 33 to SBK160808T-121Y-N.(For EMI)
 -P10 C156 mount 22PF.(For EMI)
 -P10 R133 change from 4.7K to 51 ohm
 -P10 Swap U54 pin2 & pin5.
 -P10 Add R619 2.37K/F.
 -P10 R126 change from 4.7K to 2.37K/F
 -P11 Add R622 10K(For PCIE_REQ_WLAN)
 -P11 RP8 mount for Ext. only
 -P11 Add Q66 2N7002(For PCIE_REQ_WLAN)
 -P11 Add Y3 25MHz for Int. only.
 -P11 Add R179 1M (For Int. only).
 -P11 Add C168,C169 6.8PF (For Int. only)
 -P11 R584 mount 0 ohm(for N11 only)
 -P11 D1 change to SW1010CPT.(For 3VPCU leakage)
 -P11 Add R624 10k for N11 SKU only.
 -P11 R186 mount 10k.(For Int. only)
 -P13 Delete R218,R220 0 ohm.(save cost)
 -P13 Delete R215 0_25.(save cost)
 -P13 Mount C214,C188 1uF.
 -P14 Swap SMDDR_VREF_DQ0 & SMDDR_VREF_DQ1
 -P14 R227,R232 mount 470 ohm.
 -P15 L12,L13,L14 change to BK1608H680.
 -P15 CON4 pin assignment reverse.(ME request)
 -P17 Add R620 2.2K
 -P17 R314 value change from 39K to 100K.
 -P17 Delete D55
 -P17 Add Q65 PDTA124EU.
 -P17 D58 mount
 -P17 Add R623 100K .(For EC idle mode save power)
 -P17 D9,D10,D12,D13,D14,D15,D16,D17, D18,D19 change from SW1010CPT to RB501V-40.
 -P17 Add D59 RB501V-40.(For SCI# leakage current)
 -P18 R330 change Pull-up from RVCC3 to VCC3.
 -P19 CON44 change to "掀蓋式".
 -P19 CON17 pin assignment reverse.
 -P19 R588 change from 37.2K/F to 36K/F.(For ODD current limit)
 -P19 CON10 change footprint.(add Lock pin)
 -P20 Q48 change footprint to "SOT23_213-3_3-2"
 -P20 Q57 change from PDTCL44EU to 2N7002E.
 -P20 R573 change from 5.2K to 3.01K.
 -P21 CON32 change pin assignment.
 -P22 PC23,PC24 no mount.
 -P22 Add PR311 68 ohm.(for Prochot# in IMVP6.5)
 -P22 PC19 & PC25 modify net
 -P23 Delete PG1,PG2
 -P23 PR93 change net from"+VCC_CFXCORE-1" to "+VGA_CORE"
 -P23 PC59 1000P delete (For VCC3 timing)
 -P23 PC61 1000P delete (For VCC5 timing)
 -P24 PR280 change to 820K(For VCC1.5 timing)
 -P24 PC212 change to 2200P(For VCC1.5 timing)
 -P24 PR119 change to 0 ohm
 -P24 PC94 no mount
 -P24 Add PD40 RB501V-40.(for N11 powerr off time)
 -P24 Delete PG16.
 -P24 Delete PG13,PG14
 -P24 PR214 no mount
 -P25 Delete PG7,PG8
 -P26 PR178 change from 7.5K/F to 6.04K/F.(VGA OCP)
 -P26 Add PR312 10K ohm.(For GFX PROCHOT)
 -P26 Add PR313 0 ohm.(For GFX PROCHOT)
 -P26 Add PD39 RB501V-40.
 -P26 Delete PG9,PG10
 -P26 PC141 change to E0.1UF (Ext. only)(+VGA_CORE timing)
 -P26 PR202 change to 47K(For +VGA_CORE timing)
 -P26 VID For External VGA_CORE circuit modify
 -P28 Delete PG11
 -P28 PC225 change to 0.1UF.(For VCC1.8 timing)
 -P30 R4045 change from GND to VCC3
 -P30 R4047 change from VCC3 to GND
 -P30 Add R4108 Pull-high,(PU-ES sample,PD QS sample)
 -P31 CON32 reverse pin assignment
 -P33 C322,C323 change from 27PF to 22PF.

0804
 -P5 Add Q68,R628,R630,R629,R633 for DRAMRST#
 -P5 R22 change power from 1.5VSUS to VCC1.5_CPU
 -P7 C108,C110 change height to lower.
 -P7 VDDQ power change to VCC1.5_CPU
 -P10 Y2 change footprint
 -P12 U4.C38 change to BT_PRSH#
 -P12 U4.AA4 change to CRIT_TEMP_REP#
 -P12 U4.F1 change to DRAMRST_CNTRL_PCH.
 -P12 R577 change from GND to RVCC3
 -P13 C178 change from 1U to 10uF.(For CRT wave noise)
 -P15 Delete L15.(save cost)
 -P17 R615 mount 0 ohm
 -P17 U18.106 change to CRIT_TEMP_REP#.
 -P17 Add R625 100K.(For RSMRST# abnormal shutdown)
 -P17 D11 change to SW1010CPT
 -P17 Add R626,R627 0 ohm.
 -P18 Add C752,C753 1000P.(For EMI)
 -P19 U30.9 delete net.
 -P19 C392 change to 10UF.(reduce ripple)
 -P19 CON44.14 change to GND
 -P19 CON44.42 change to HDA_BCLK0
 -P19 CON44.44 change to GND
 -P24 Add Pq74,PR314,PD41,PC242,PR315,PR316,PQ75
 -P29 L4001 change to PBV160808T-221Y-N(220,2A).
 -P33 CON8 change footprint.
 -P33 R298 change from 68 to 22 ohm

0805
 -P5 Add C756 470PF.
 -P5 R22 change value from 1.1K/F to 1.5K/F(For S3 power)
 -P5 R23 change value from 3K/F to 750/F.(For S3)
 -P5 Add U64,C755,R634. (For S3 power)
 -P5 U2.F6 change to DRAMRST_CPU#
 -P7 C688 mount 330UF(Reduce ripple)
 -P8 U2.J17 U2.H17 delete net "DDR_VREF_DQ0""DDR_VREF_DQ1"
 -P10 Delete R583
 -P10 R152 change from 0603 to 0402
 -P13 Add C754 0.01uF(Reduce ripple)
 -P13 L6,L7 change to TDK MKG1608B10NJ
 -P13 C190 change from 0.1U to 1uF.
 -P14 Delete U7.(thermal don't use)
 -P14 Delete R228,R230,R231,R233
 -P14 CON1.1 CON2.2 change net to "SMDDR_VREF_DQ0"
 -P15 R241,R242 change to 33 ohm.
 -P15 R237,R238 change to 4.7K
 -P15 delete L10,L11
 -P15 Add R631 100K.
 -P15 Add F17.
 -P16 Delete F10
 -P17 R321 no mount
 -P17 Add 5V_RESET net
 -P17 U63.6 add DRAMRST_CNTRL net
 -P17 Add R632 10K
 -P17 U22.1 add net"5V_RESET#"
 -P18 P373,C374,C375 mount 10P.
 -P18 CON15 change to Foxconn,(EMI solution)
 -P18 Add D60
 -P20 U57 change input voltage from VCC5 to 5VPCU.
 -P22 PR1 change to 2.2/F_6
 -P23 PQ10,PQ13 change to AON7406.(Reduce ripple)
 -P23 Add PU16,PR317,PR318,PR319,PD42,PC243,PC244,PC245
 -P24 PU4.11 add net "VCC1.5_CPU_VCC105_PWRGD"
 -P24 PR120 delete
 -P24 PR124 value change to 8.06K/F
 -P24 Add PU17,PR320,PC246,PR321,PR323,PC247,PR322,PR324
 -P24 Add PR110,PQ30
 -P24 Add PQ77
 -P24 Delete PR120,PR130
 -P24 PR314 change to 100K/F
 -P24 PC242 change to 2200PF.
 -P24 Add PQ74 NTMS4935
 -P24 Add PQ75 2N7002E
 -P24 Add PR316 220_6 ohm
 -P28 PR137 mount 24.9K/F
 -P28 PR141 mount 470K/NTC/THINKING_4
 -P29 Delete R4002

 QUANTA COMPUTER		Change List	
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CPU Frequency Select Table

FSLC	CPU MHz	SRC MHz	REF MHz	USB MHz	DOT MHz
0 (default)	133.33	100.00	14.318	48.00	96.00
1	100.00				

Table 2: pin 6, 7 Configuration

B1b4	B1b3	B1b2	B1b1	Pin 6 MHz	Pin 7 MHz	Spread %	Comment
0	0	0	0	N/A	N/A	N/A	N/A
0	0	0	1	N/A	N/A	N/A	N/A
0	0	1	0	27MHz_nonSS	27MHz_SS	-0.5%	
0	0	1	1	27MHz_nonSS	27MHz_SS	-1%	
0	1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
0	1	0	1	27MHz_nonSS	27MHz_SS	-2%	
0	1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
0	1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	
1	0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
1	0	0	1	27MHz_nonSS	27MHz_SS	+0.5%	
1	0	1	0	27MHz_nonSS	27MHz_SS	+0.75%	
1	0	1	1	N/A	N/A	N/A	N/A
1	1	0	0	N/A	N/A	N/A	N/A
1	1	0	1	N/A	N/A	N/A	N/A
1	1	1	0	N/A	N/A	N/A	N/A
1	1	1	1	N/A	N/A	N/A	N/A

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	56 pin TSSOP
0	0	0	1	64 pin TSSOP
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	72 pin QFN
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	32 pin QFN
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 3: IO Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

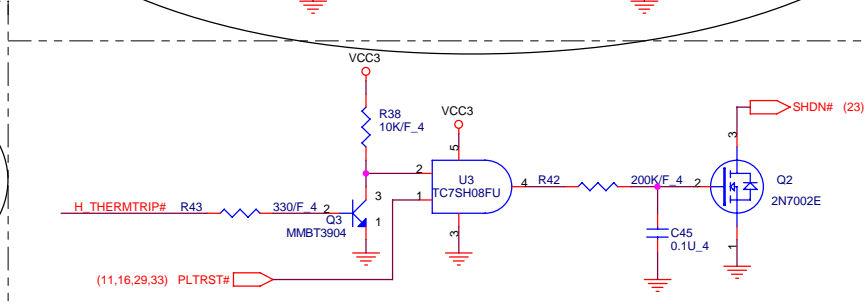
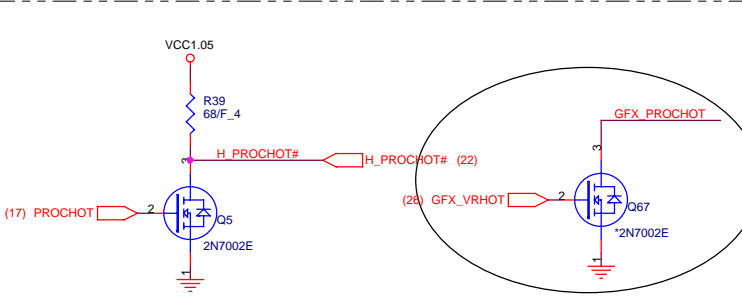
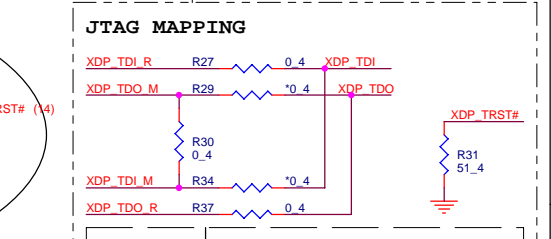
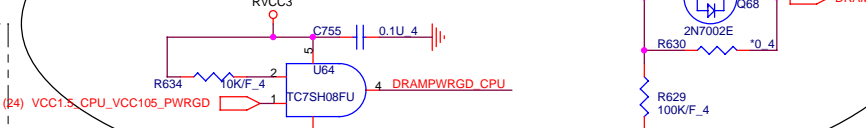
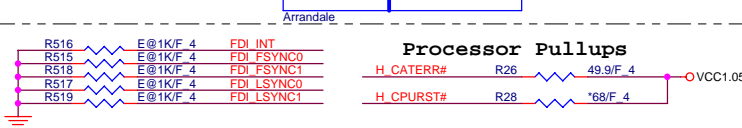
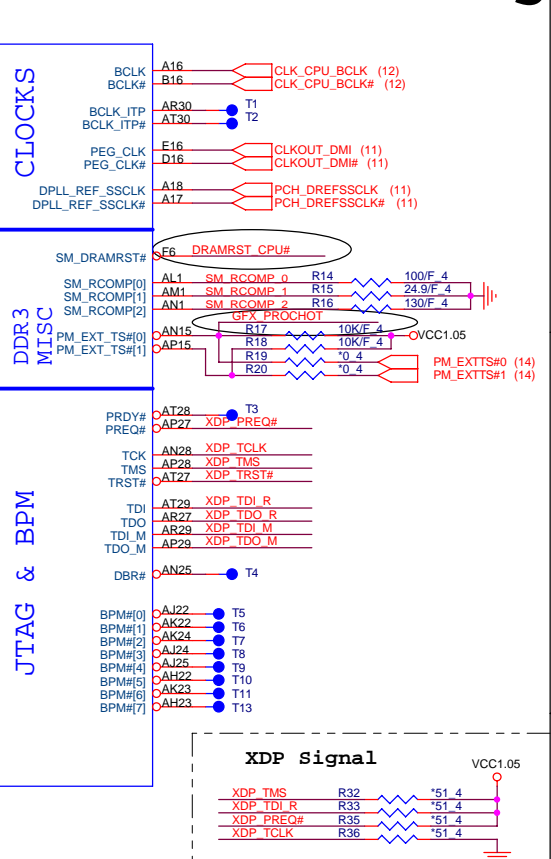
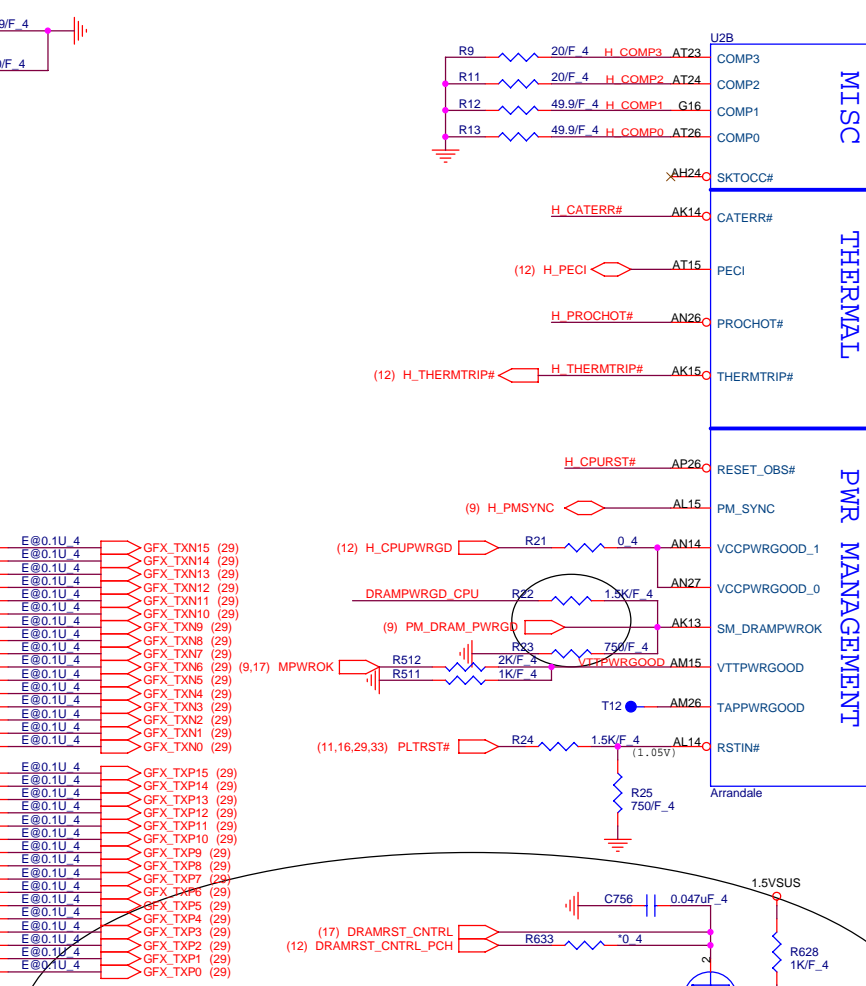
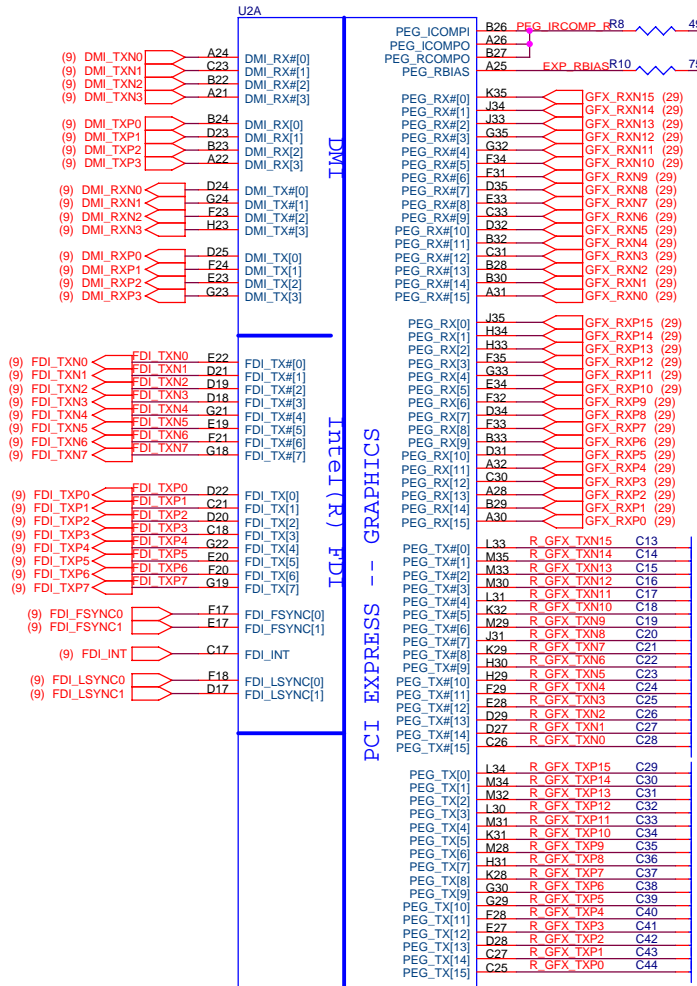
QUANTA COMPUTER

Title: **CLOCK GENERATOR**

Size: Document Number: **GD3 Main Board** Rev 1A

Date: Tuesday, September 01, 2009 Sheet 4 of 33

1. Level 1 Environment-related Substances should NEVER be Used.
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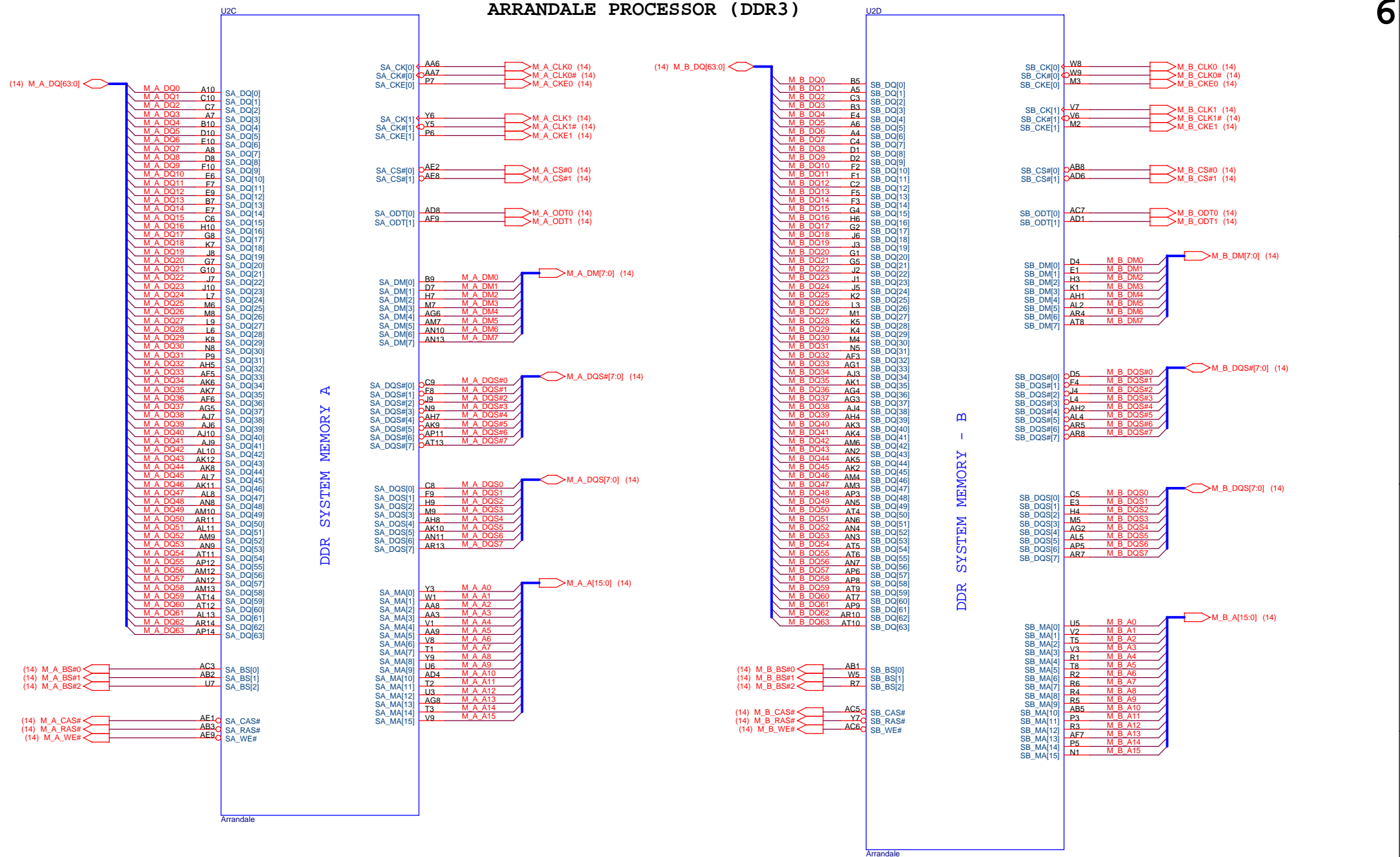
Scan Chain (Default)	STUFF -> R27, R30, R37 NO STUFF -> R29, R34
CPU Only	STUFF -> R27, R29 NO STUFF -> R30,
GMCH Only	R34, R37 STUFF -> R34, R37 NO STUFF -> R27, R29, R30



Title: **PROCESSOR 1/4(HOST&PCI)**

Size: Custom Document Number: **GD3 Main Board** Rev: 2A

ARRANDALE PROCESSOR (DDR3)



QUANTA COMPUTER

Title: **PROCESSOR 2/4(DDR)**

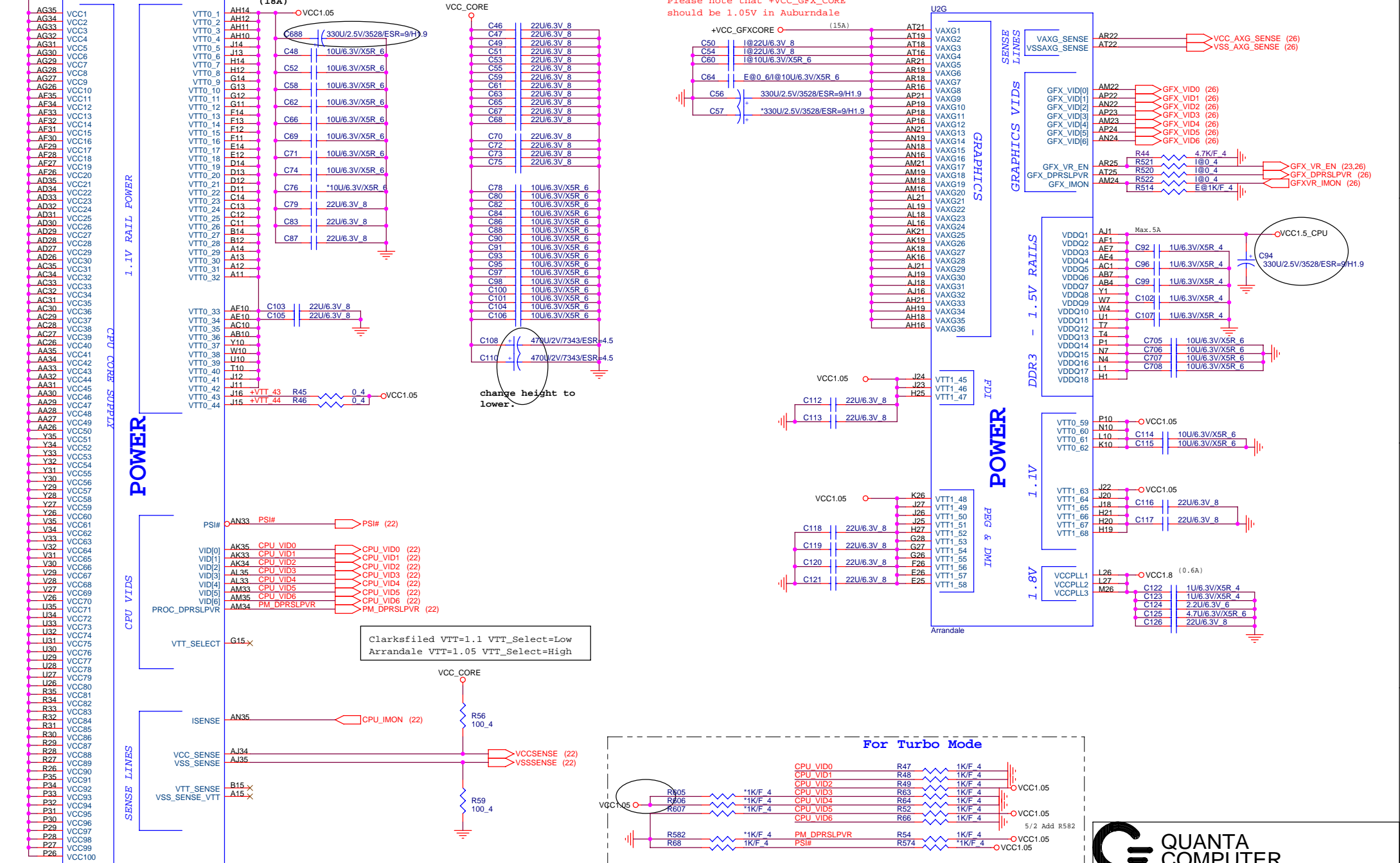
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Custom	GD3 Main Board	1A

Date: Monday, August 31, 2009 Sheet 6 of 33

1. Level 1 Environment-related Substances Should NEVER be Used.
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ARRANDALE PROCESSOR (GRAPHICS POWER)

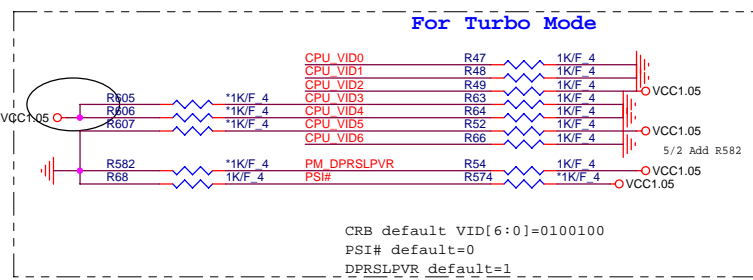
CPU:
ARRANDALE 1.05V



Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

change height to lower.

Clarksfiled VTT=1.1 VTT_Select=Low
Arrandale VTT=1.05 VTT_Select=High



CRB default VID[6:0]=0100100
PSI# default=0
DPRSLPVR default=1



Title: **PROCESSOR 3/4(POWER)**

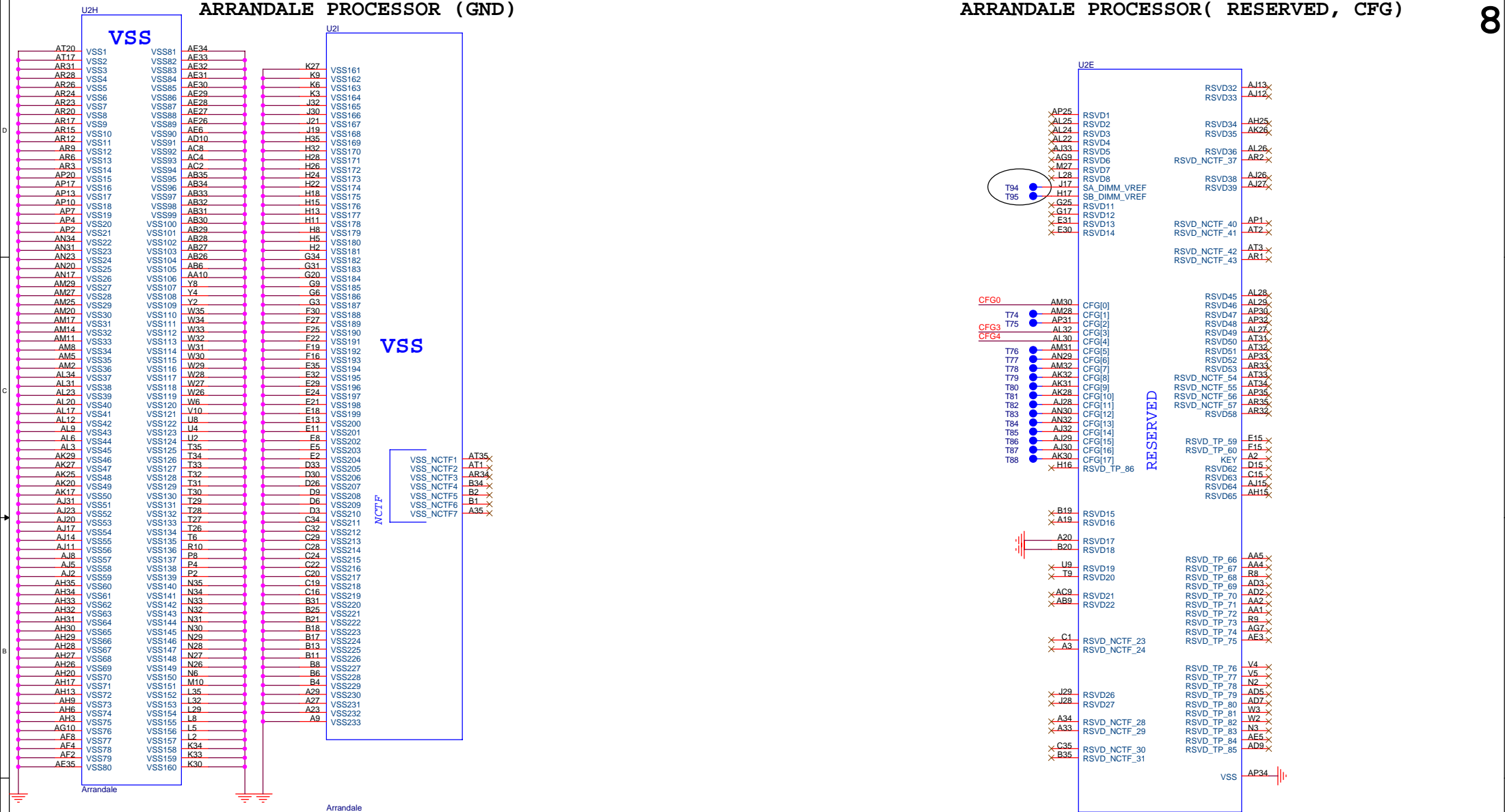
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ARRANDALE PROCESSOR (GND)

ARRANDALE PROCESSOR (RESERVED, CFG)



CFG0 R73 3.01K 4

Not applicable for Clarksfield Processor

PCI-Epress Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enabled

CFG3 R74 3.01K 4

PCI-Epress Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display port device is connected to the Embedded Display port
------	--

CFG4

R75 3.01K 4

QUANTA COMPUTER

Title: PROCESSOR 4/4(GND)

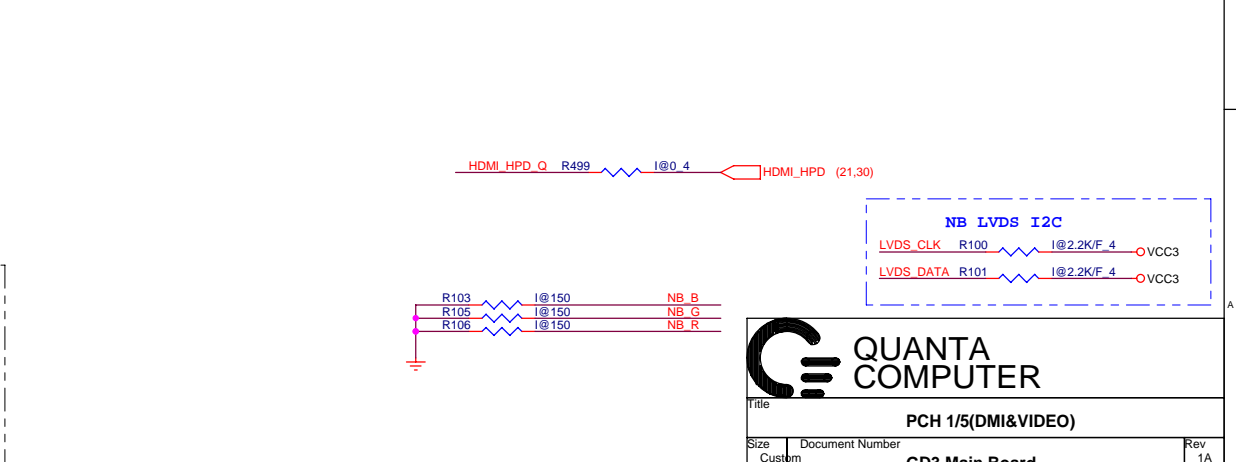
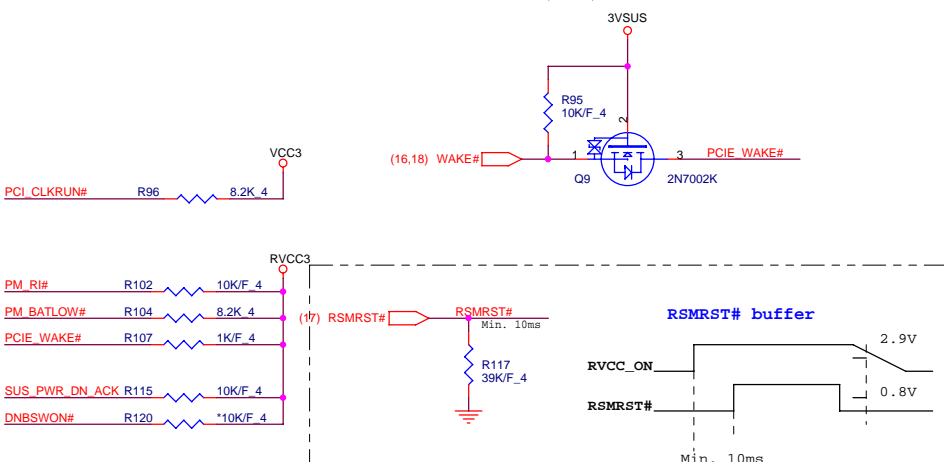
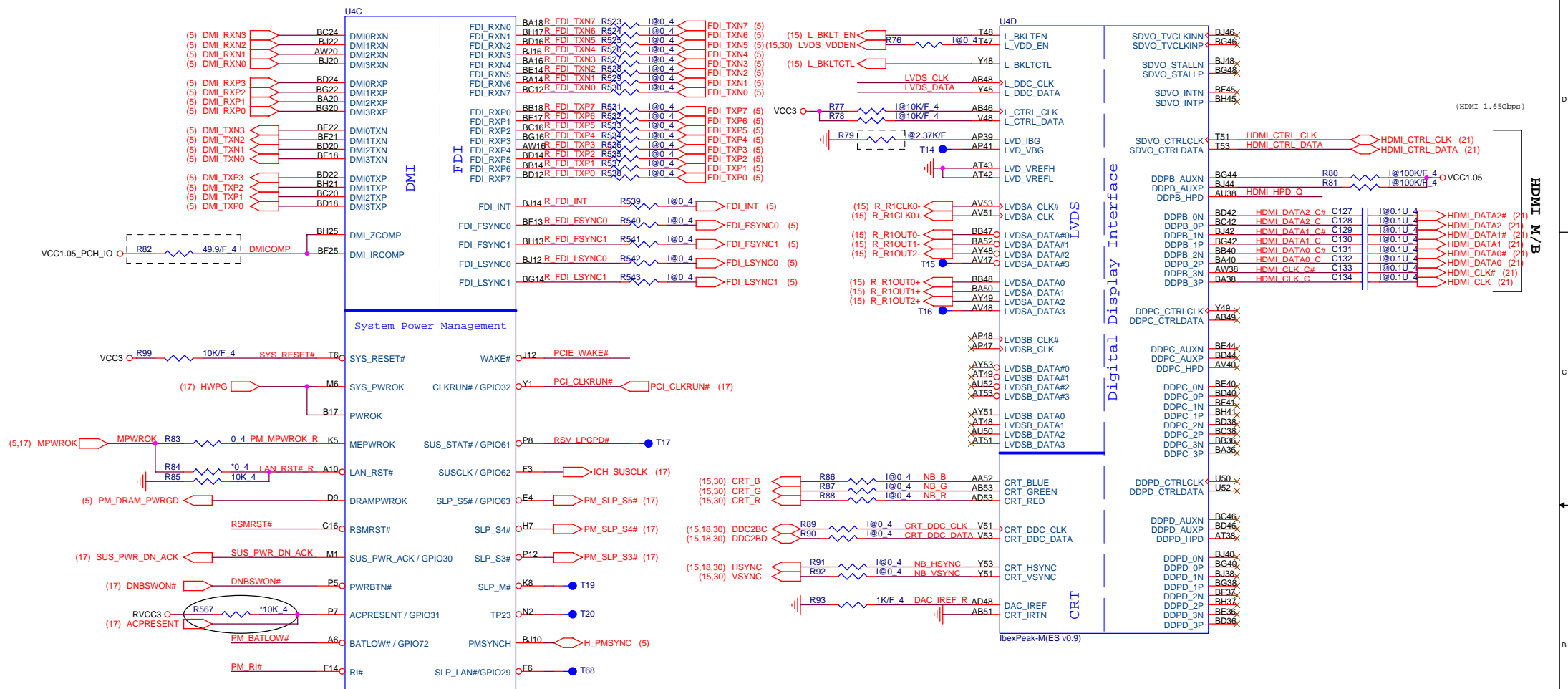
Size	Document Number	Rev
Custm	GD3 Main Board	1A

Date: Saturday, August 29, 2009 Sheet 8 of 33

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IBEX PEAK-M (DMI, FDI, GPIO)

IBEX PEAK-M (LVDS, DDI)



QUANTA COMPUTER

Title: PCH 1/5(DMI&VIDEO)

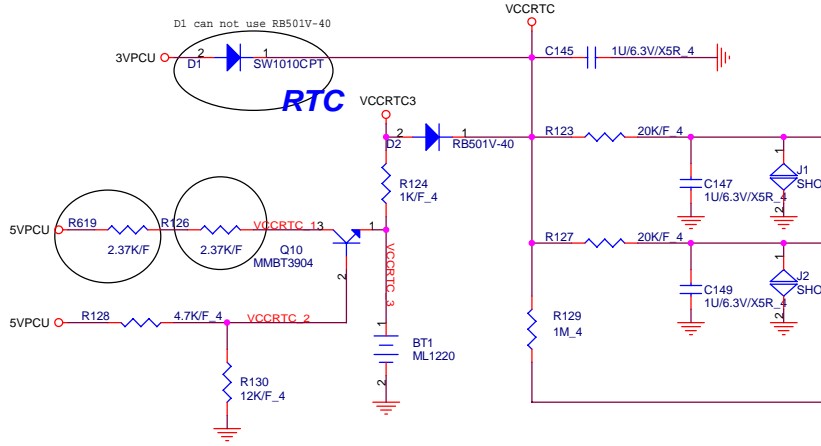
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Document Number: **GD3 Main Board**

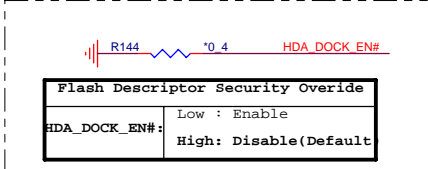
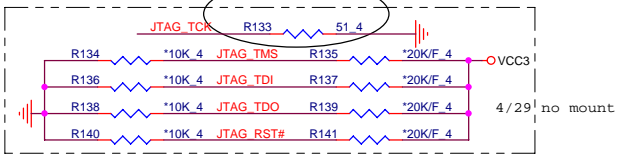
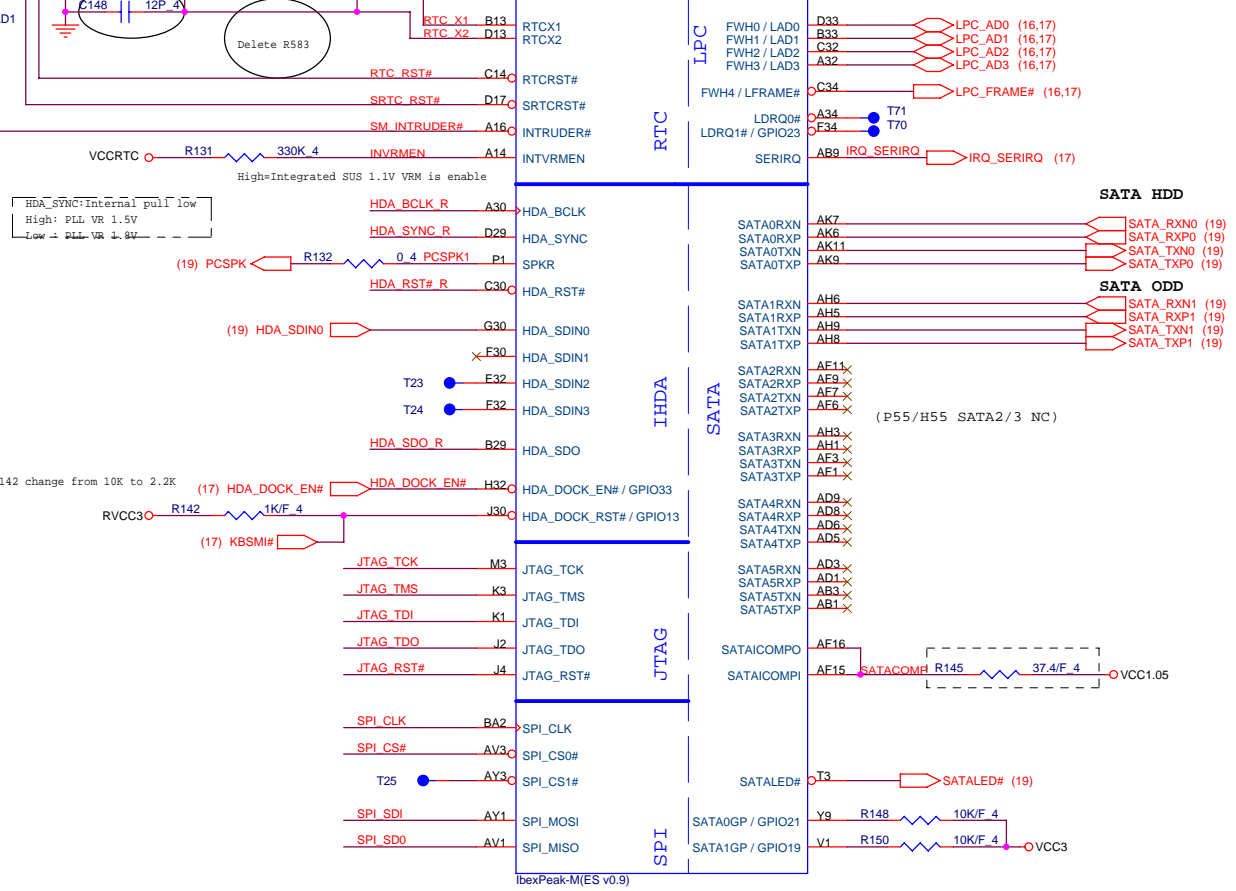
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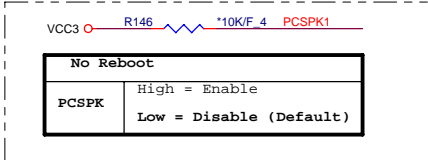
Rev: 1A



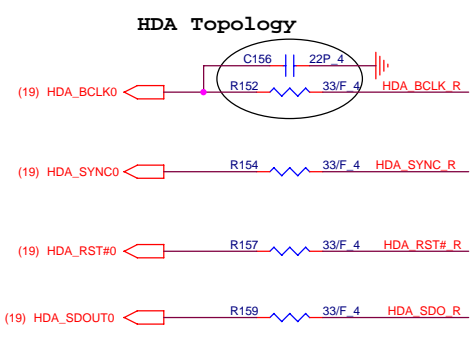
IBEX PEAK-M (HDA, JTAG, SATA) GREENPEAK



Flash Descriptor Security Override	
HDA_DOCK_EN#:	Low : Enable High: Disable(Default)



No Reboot	
PCSPK	High = Enable Low = Disable (Default)



HDA_SYNC
Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.

HDA_SDO
Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.

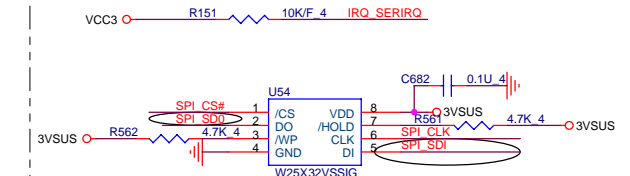
HDA_SDO
Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.

INVRMEN
High = Enable
High (1) = Integrated VRM is enabled
Low (0) = Integrated VRM is disabled

SPI_SDI Intel Anti-Theft Technology
High = Enable
Low = Disable (Default)

4/30 R142 change from 10K to 2.2K

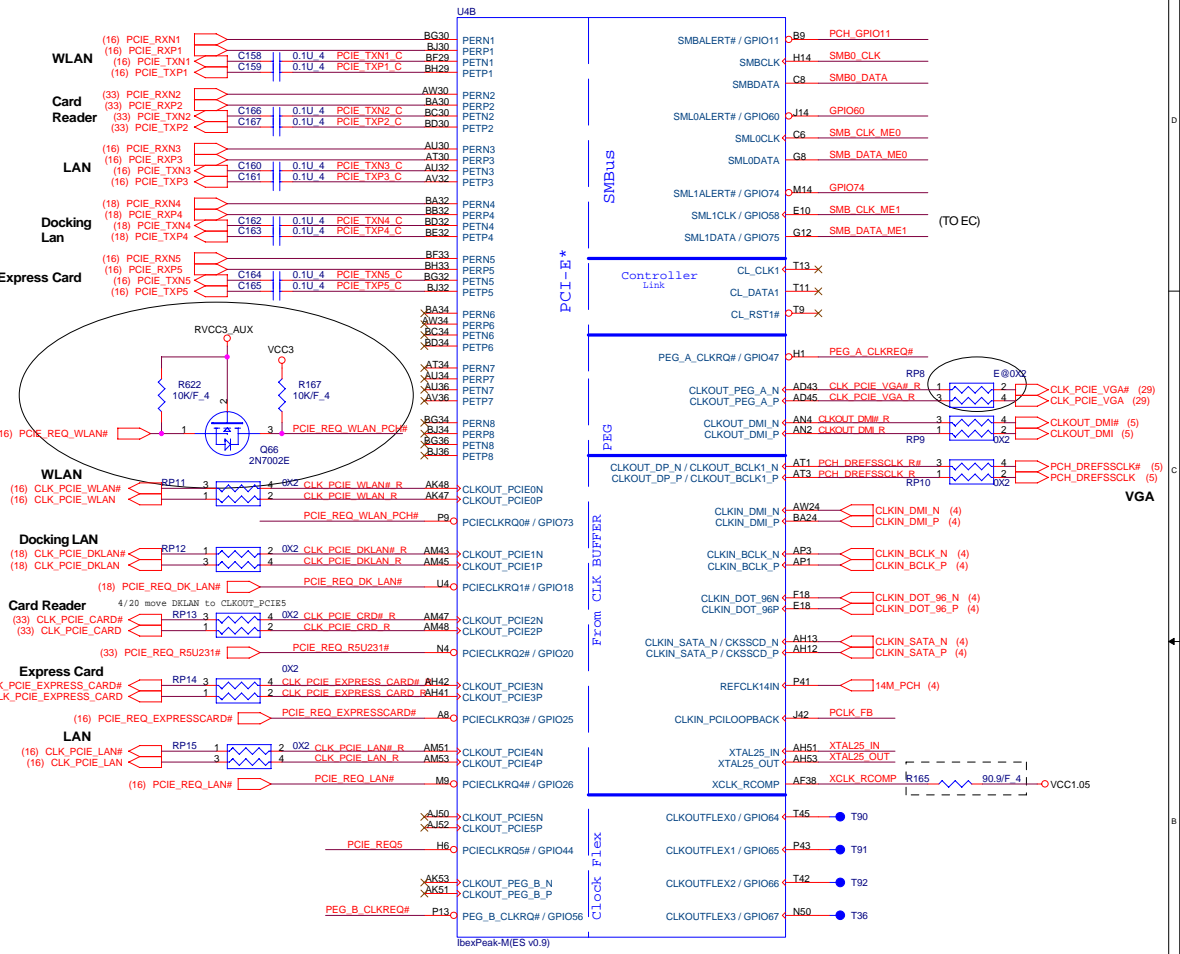
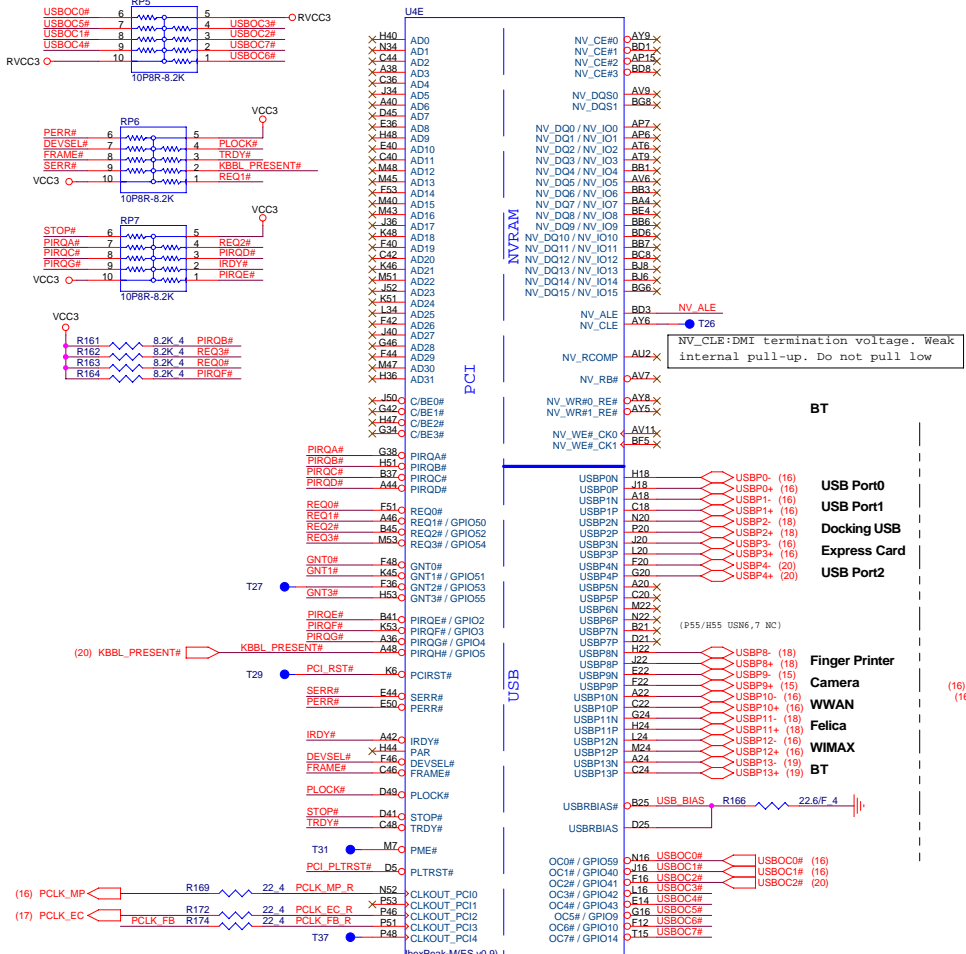
HDA_SYNC: Internal pull low
High: PLL VR 1.5V
Low: PLL VR 1.8V



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IBEX PEAK-M (PCI,USB,NVRAM)

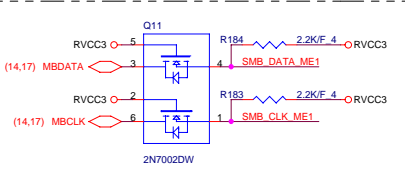
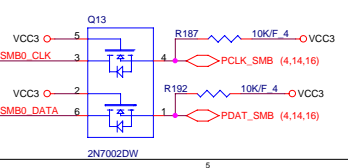
IBEX PEAK-M (PCI-E,SMBUS,CLK)



GNT2#/GPIO53 :
 High : Internal pull-up
 Low : Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops)

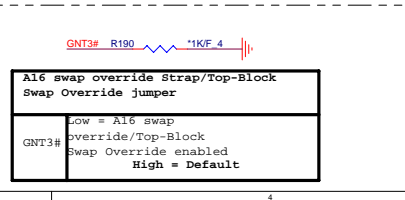
SM BUS for C0 (CLOCK/DRAM)

PCLK_SMB/PDAT_SMB	Address
SO-DIMM0	1010 000X A0h
SO-DIMM1	1010 010X A4h
IC'SPLRS105 Express Card	1101 0010 D2h



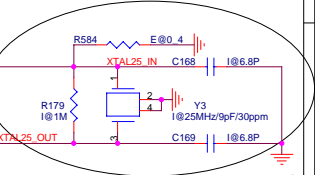
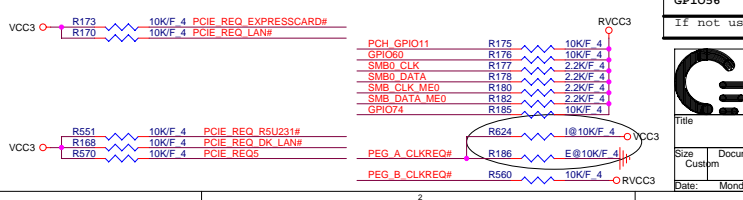
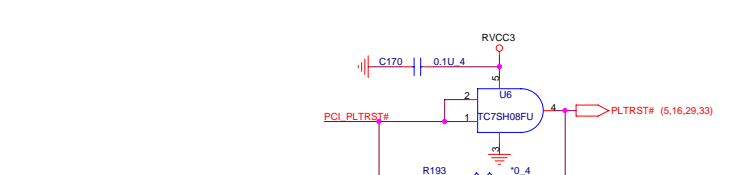
Anti-Theft Technology

NV_ALE	High = Enable
NV_CLE	Low = Disable



Boot BIOS Strap

GNT0#	GNT1#	Boot BIOS Location
0	0	* LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



GPIO56
 If not used, 8.2-k Ω to 10-k Ω pull-up to +V3.3A

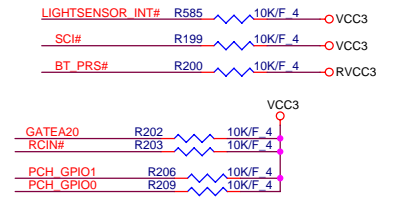
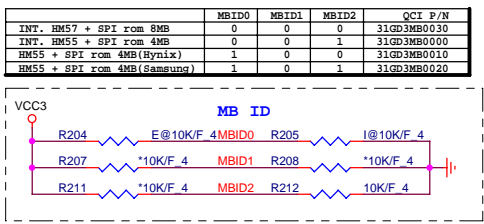
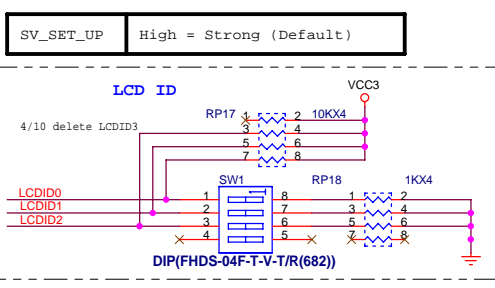
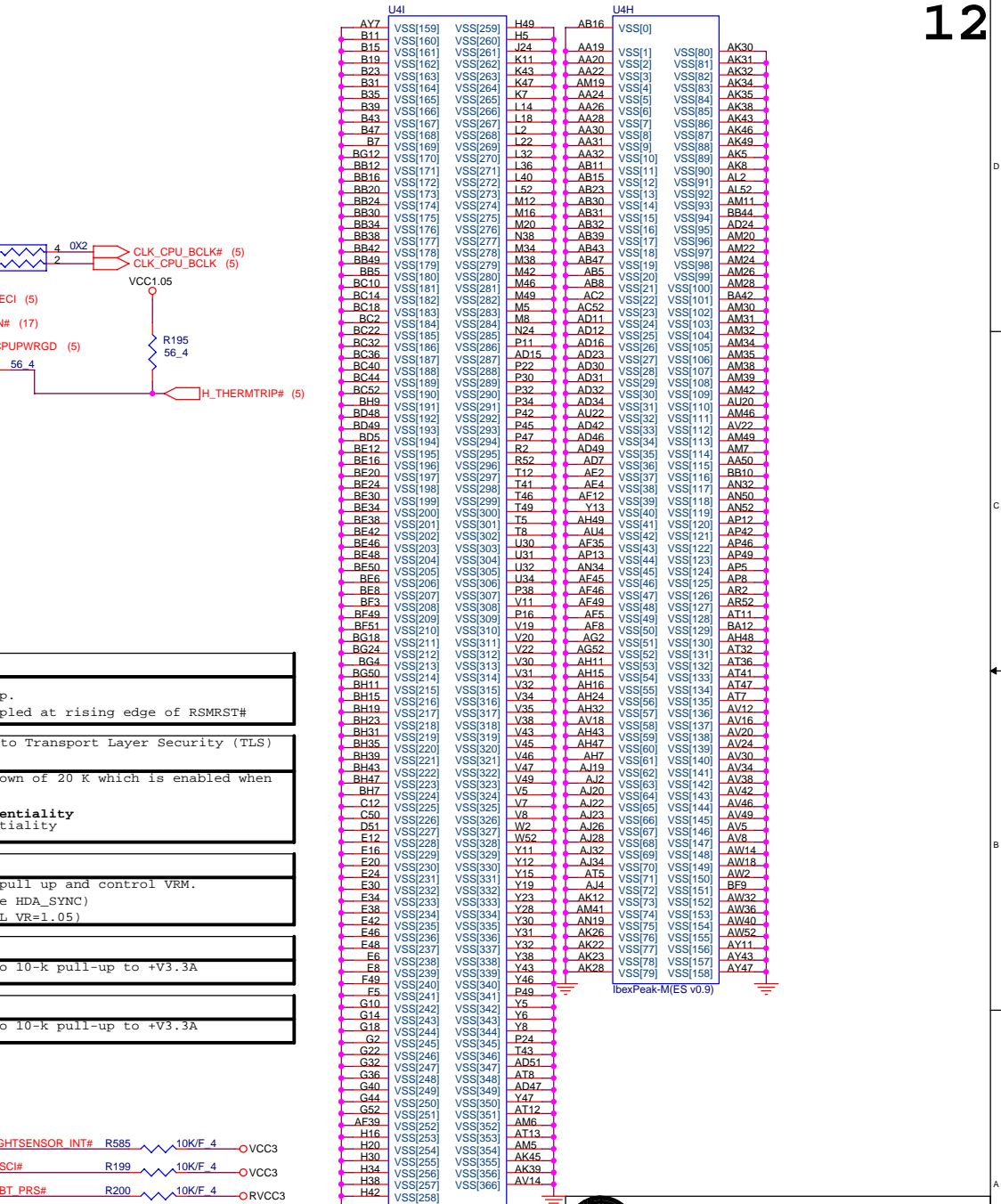
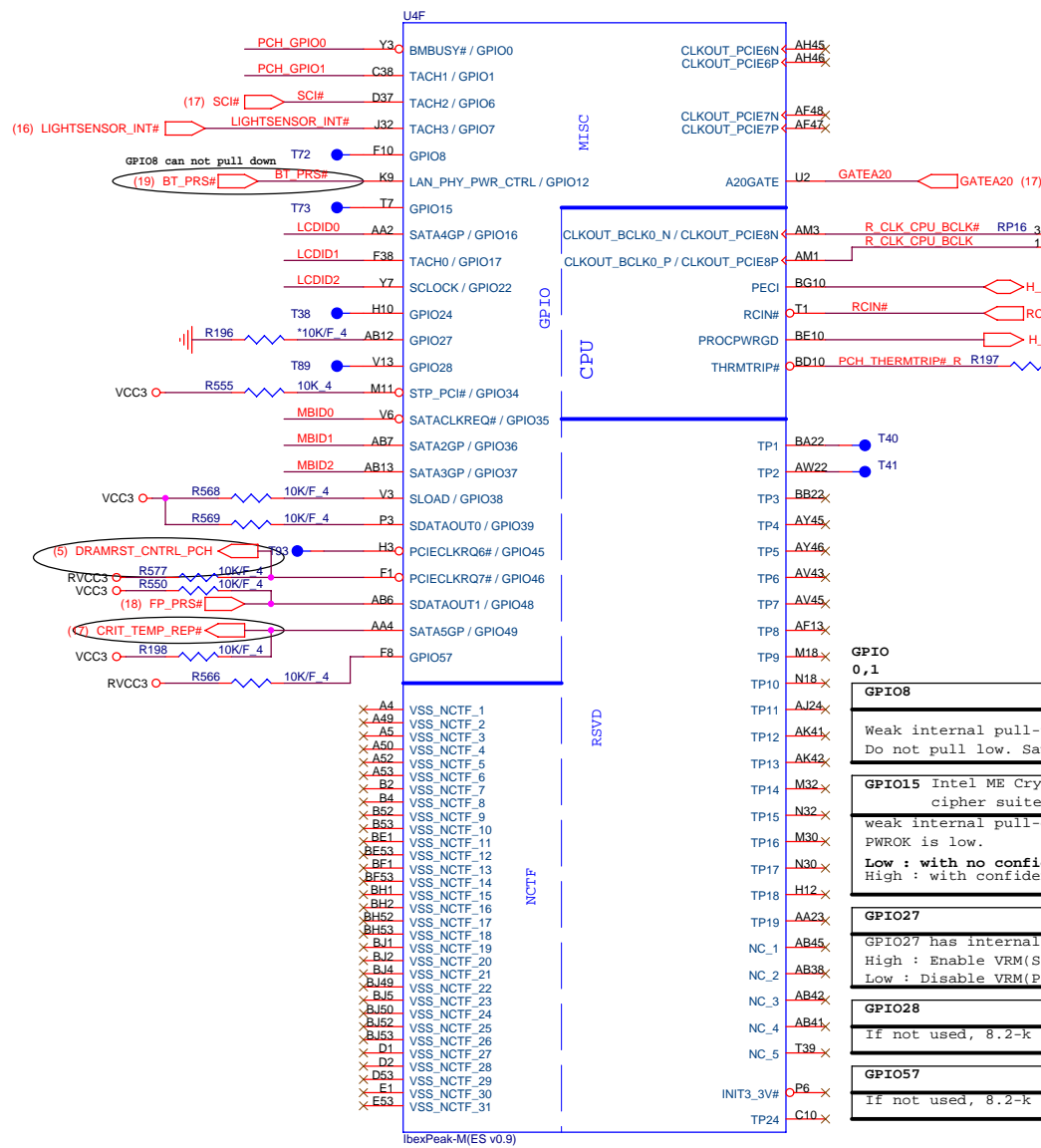
QUANTA COMPUTER

PCH 3/5(PCI)


GD3 Main Board

Size Custom Document Number
 Date: Monday, August 31, 2009 Sheet 11 of 33

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



QUANTA COMPUTER

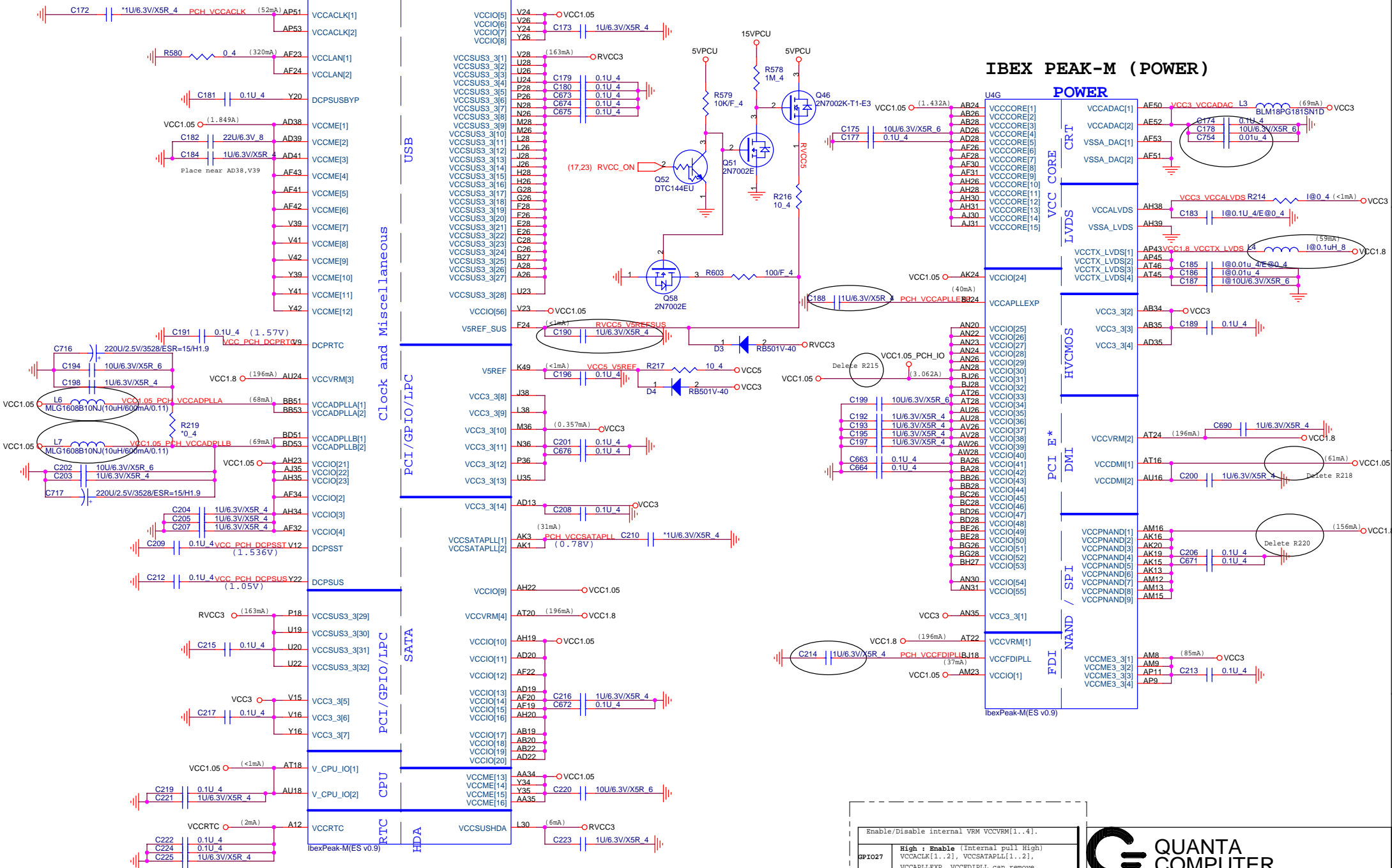
Title: **PCH 4/5(GPIO)**

Size: Custom Document Number: **GD3 Main Board** Rev: 1A

Date: Tuesday, September 01, 2009 Sheet: 12 of 33

POWER

IBEX PEAK-M (POWER)



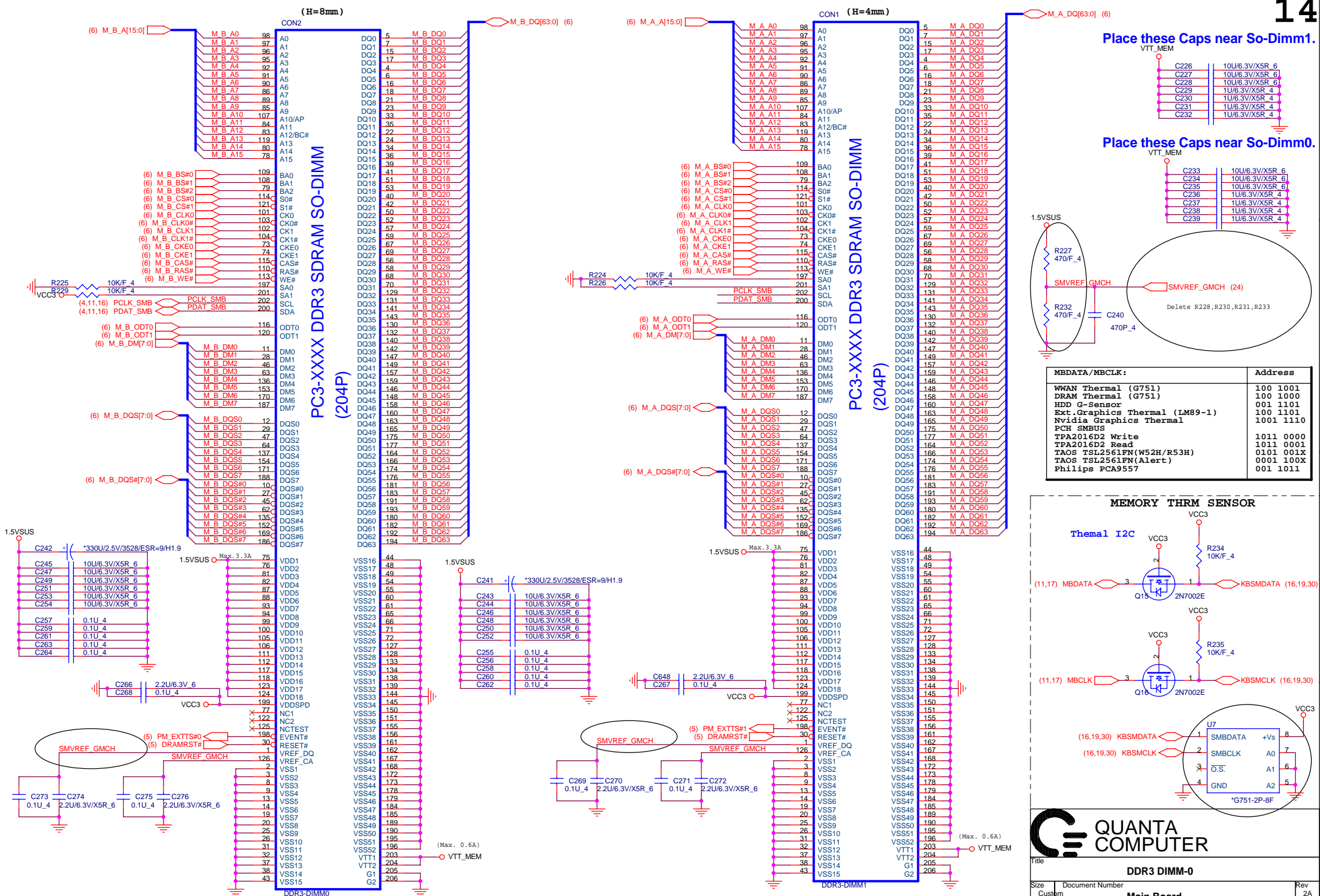
Enable/Disable internal VRM VCCVRM[1..4].	
GPIO27	High : Enable (Internal pull High) VCCACLK[1..2], VCCSATAPLL[1..2], VCCAPLLEXP, VCCFDIPLL can remove Low : Disable
Strapping VCC1.5 or VCC1.8	
HDA_SYNC	High : VCC1.5 Low : VCC1.8 (Internal pull Low)

QUANTA COMPUTER

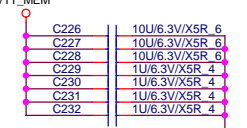
Title: **PCH 5/5(POWER)**

Size: Document Number: **GD3 Main Board** Rev: 2A

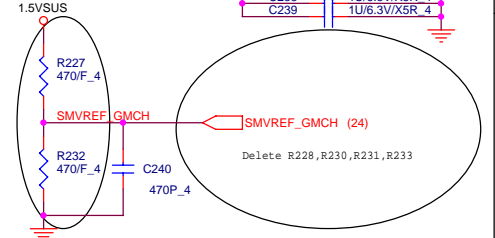
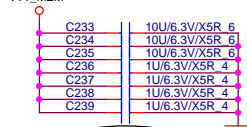
Date: Tuesday, September 01, 2009 Sheet: 13 of 33



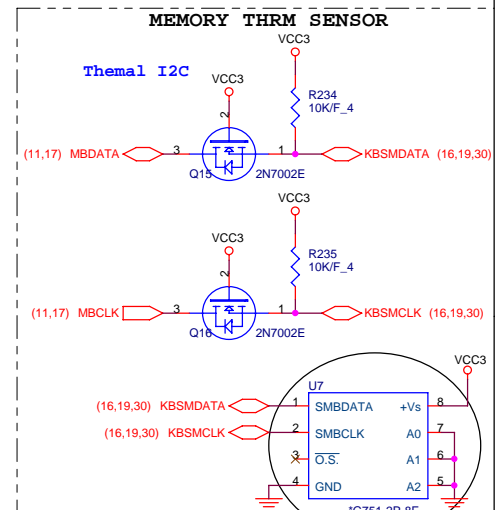
Place these Caps near So-Dimm1.



Place these Caps near So-Dimm0.



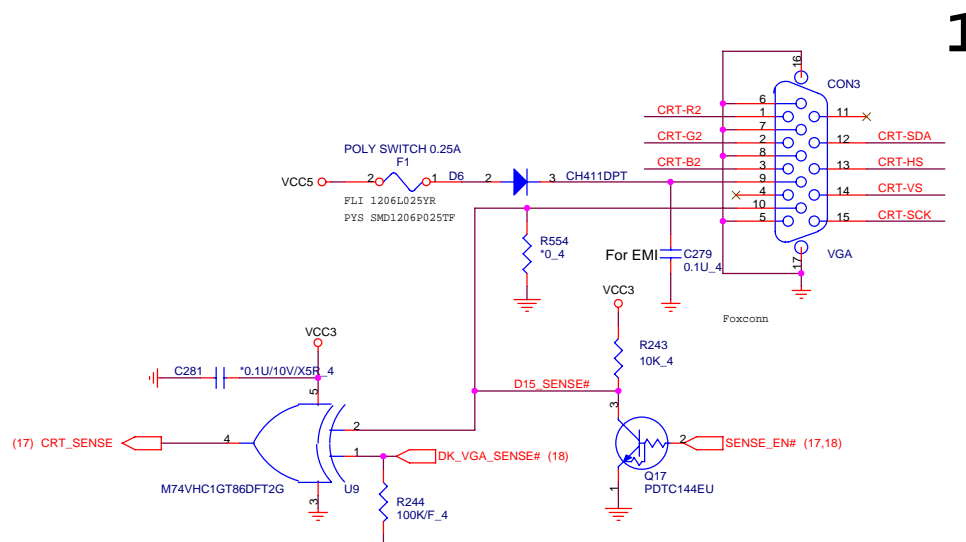
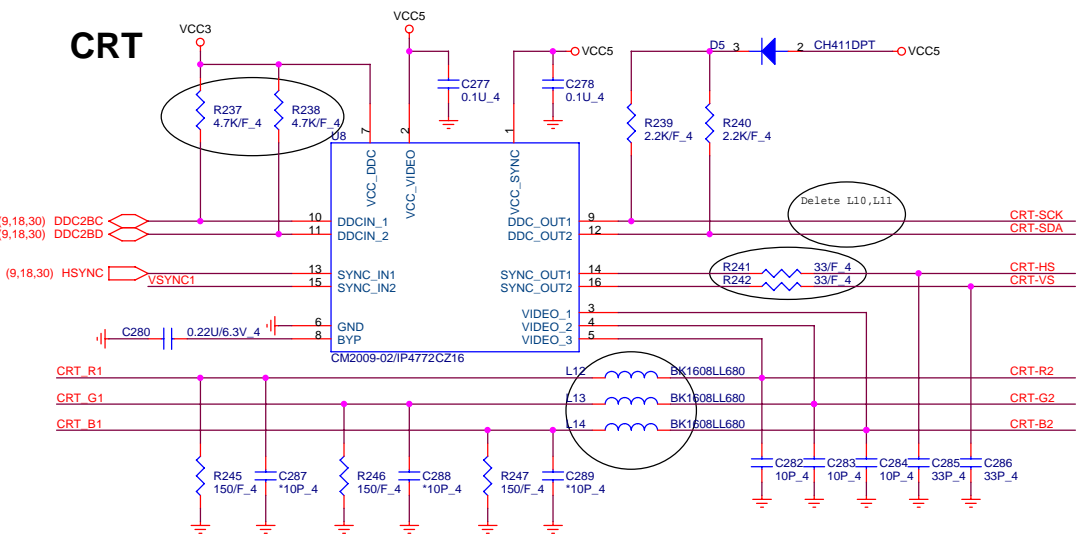
MBDATA/MBCLK:	Address
Wwan Thermal (G751)	100 1001
DRAM Thermal (G751)	100 1000
HDD G-sensor	001 1101
Ext.Graphics Thermal (LM89-1)	100 1101
Nvidia Graphics Thermal	1001 1110
PCH SMBUS	
TPA2016D2 Write	1011 0000
*TPA2016D2 Read	1011 0001
TAOS tsl2561FN(W52H/R53H)	0101 001X
TAOS TSL2561FN(alert)	0001 100X
Philips PCA9557	001 1011



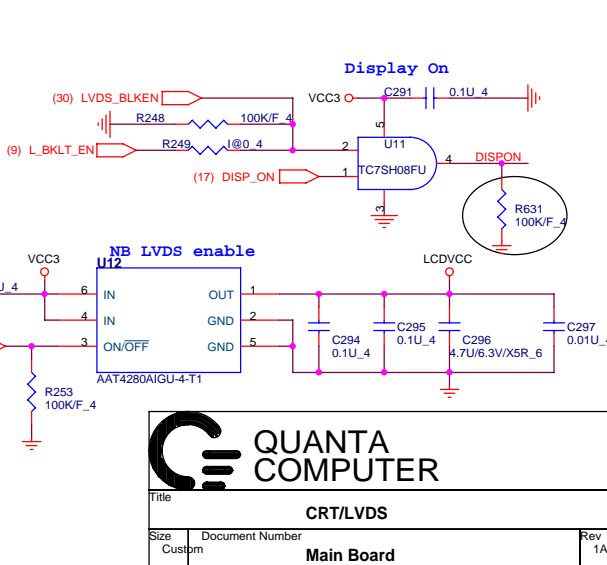
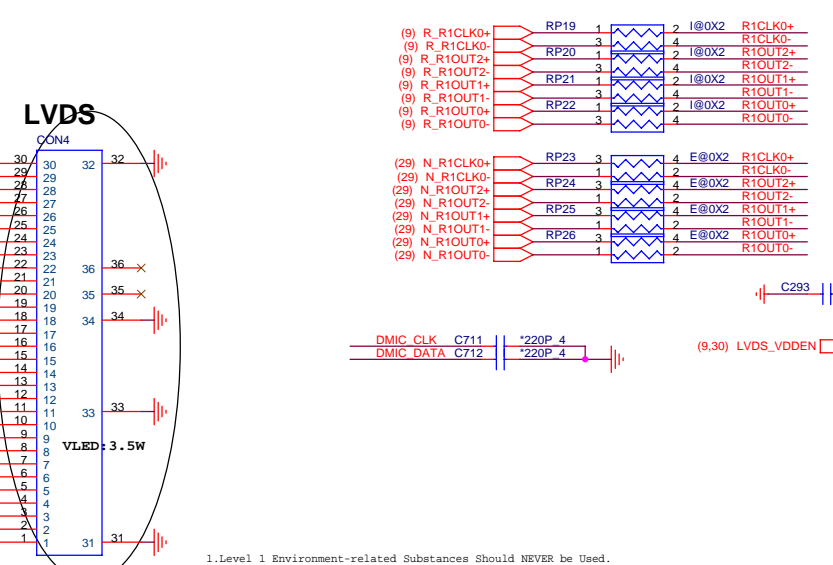
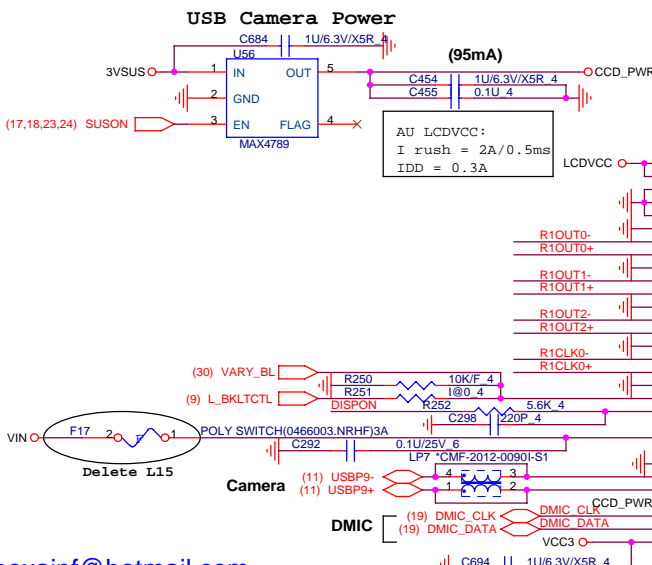
DDR3 DIMM-0
Main Board

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

CRT



	SENSE_EN#	DK_VGA_SENSE#	D15_SENSE#	Docking_Insert#	CRT_SENSE
Without Docking					
MB CRT no Plug	L	L	H	H	L
MB CRT Plug in	L	L	H => L	H	L => H
MB CRT plug out	L	L	L => H	H	H => L
With Docking					
All no Plug	L	L	H	L	L
MB CRT Plug in	L	L	H => L	L	L => H
MB CRT plug out	L	L	L => H	L	H => L
DOCK DVI Plug in	L	H => L	H	L	H => L
DOCK DVI Plug out	L	L => H	H	L	L => H
DOCK CRT Plug	L	H => L	H	L	H => L
DOCK CRT/DVI Plug	L	L => H	H	L	L => H



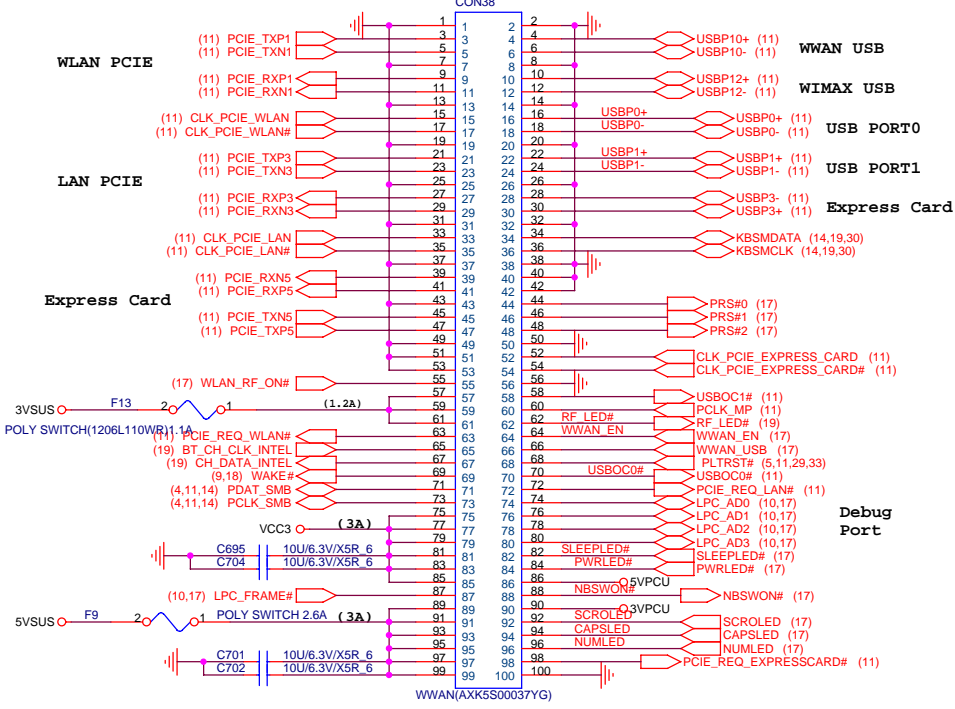
QUANTA COMPUTER

Title: CRT/LVDS

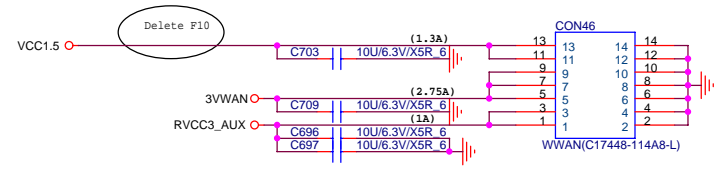
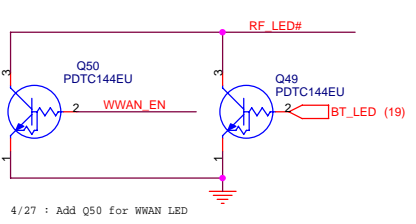
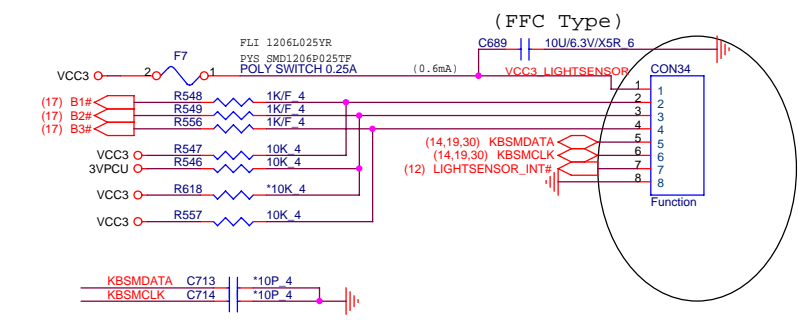
Size: Custom | Document Number: Main Board | Rev: 1A

Date: Thursday, September 03, 2009 | Sheet: 15 of 33

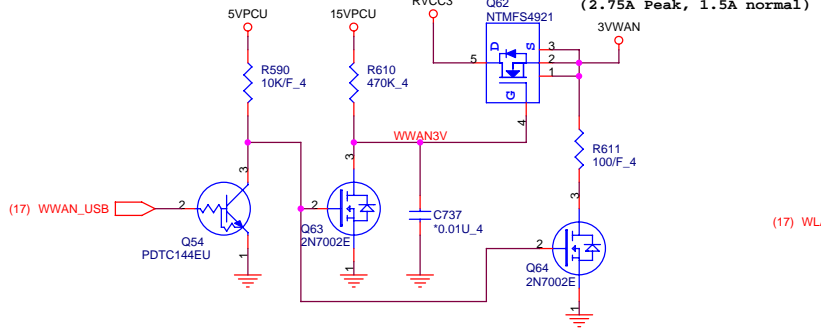
LAN Board BTB



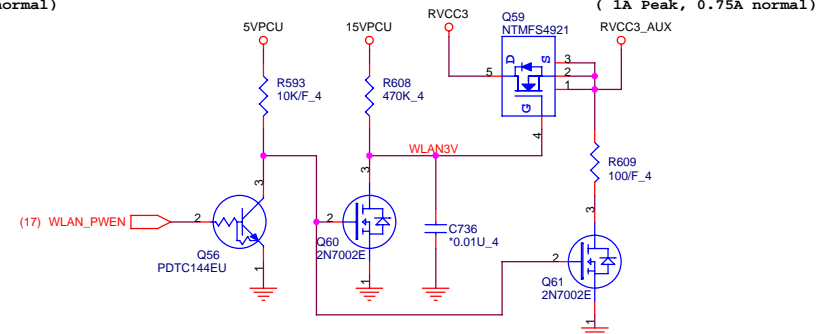
M/B to Function Board



WWAN Power



WLAN Power



QUANTA COMPUTER

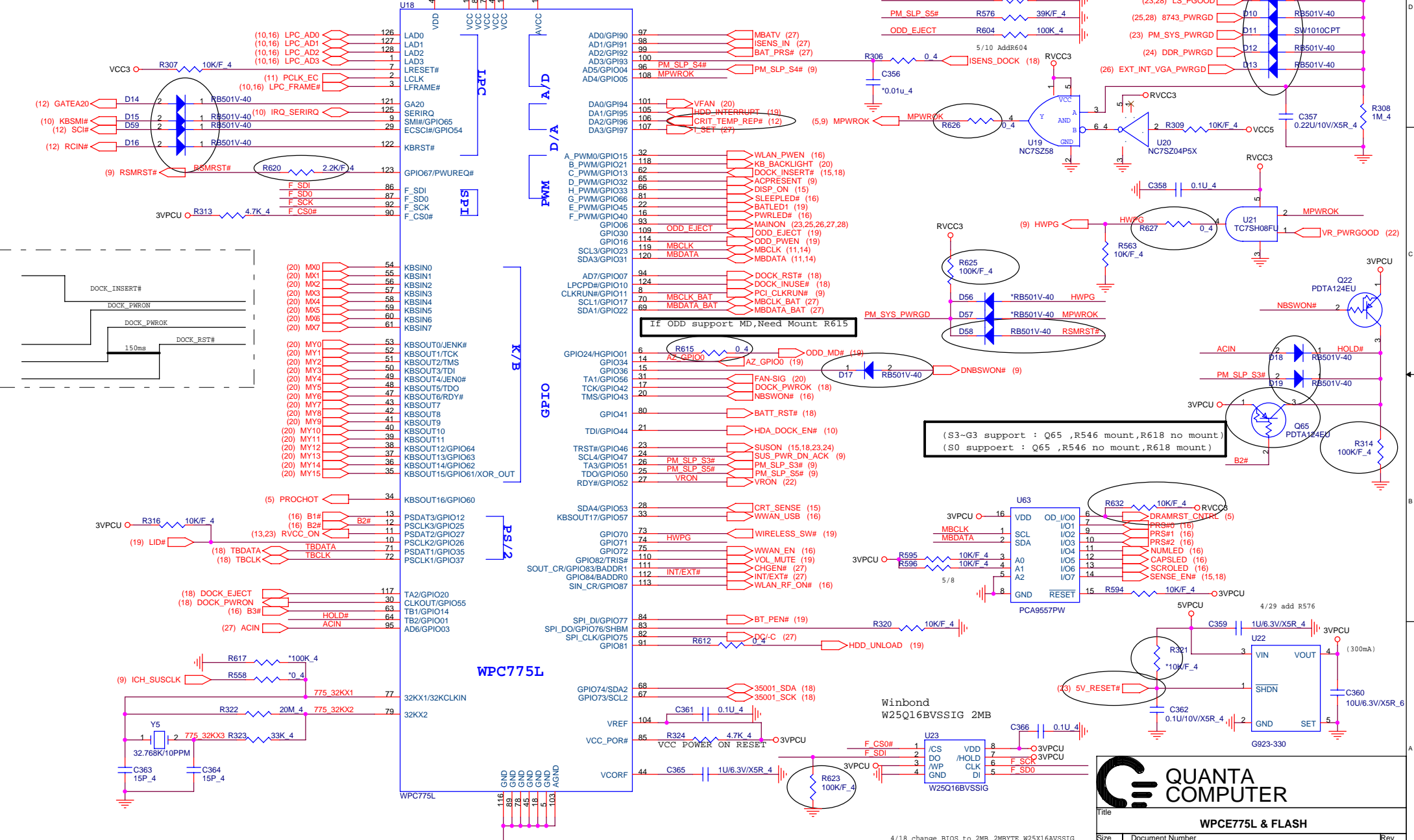
Title: LAN Board/ Function Board

Size: Document Number: Main Board Rev 1A

Date: Thursday, September 03, 2009 Sheet 16 of 33

I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
0 1	XOR-TRFEE TEST	

SHMB: SHMB(If = 0 Enable share host BIOS memory)
 DOCK_RST# : BADDR0
 T#: BADDR1



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4/18 change BIOS to 2MB 2MBYTE W25K16AVSSIG AKE382PON01

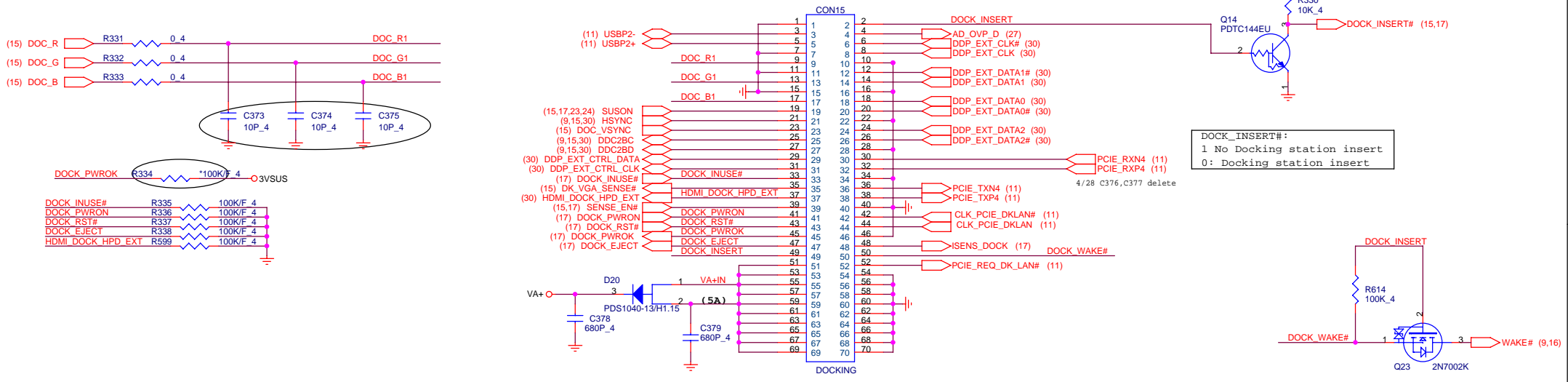
QUANTA COMPUTER

Title: **WPCE775L & FLASH**

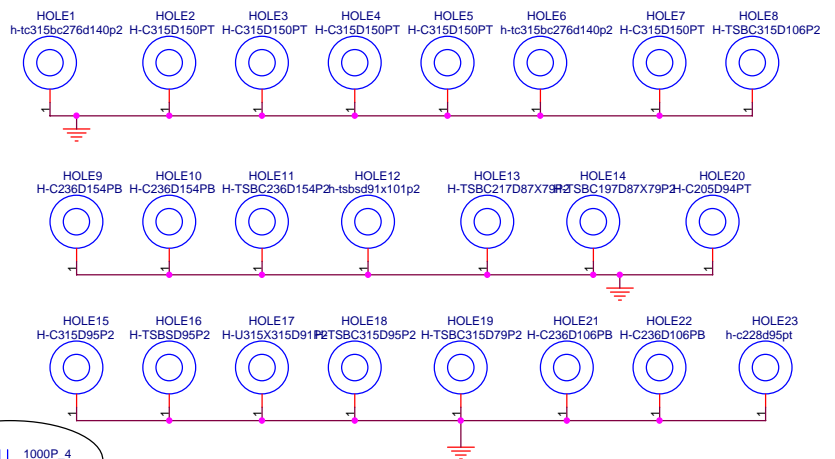
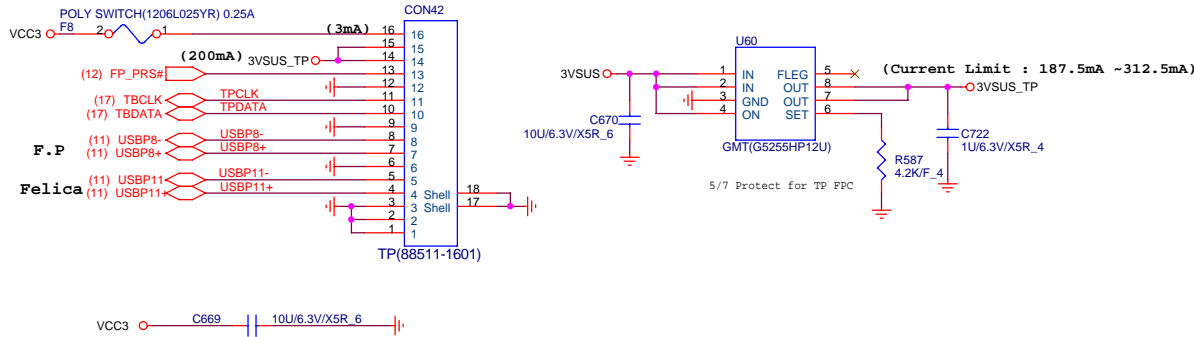
Size: Document Number: **Main Board** Rev: 2A

Date: Wednesday, September 02, 2009 Sheet 17 of 33

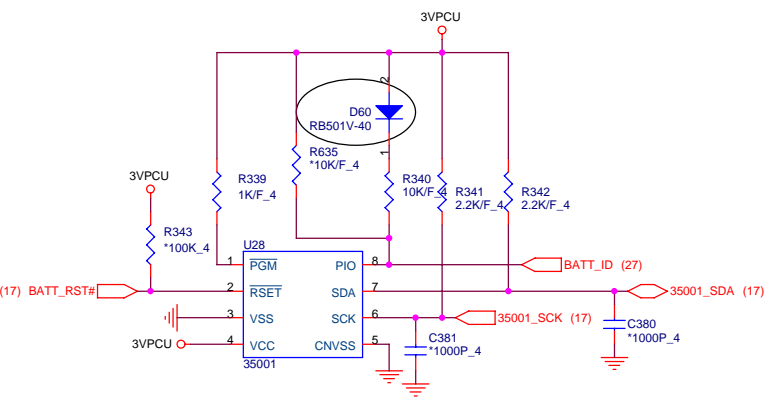
Docking



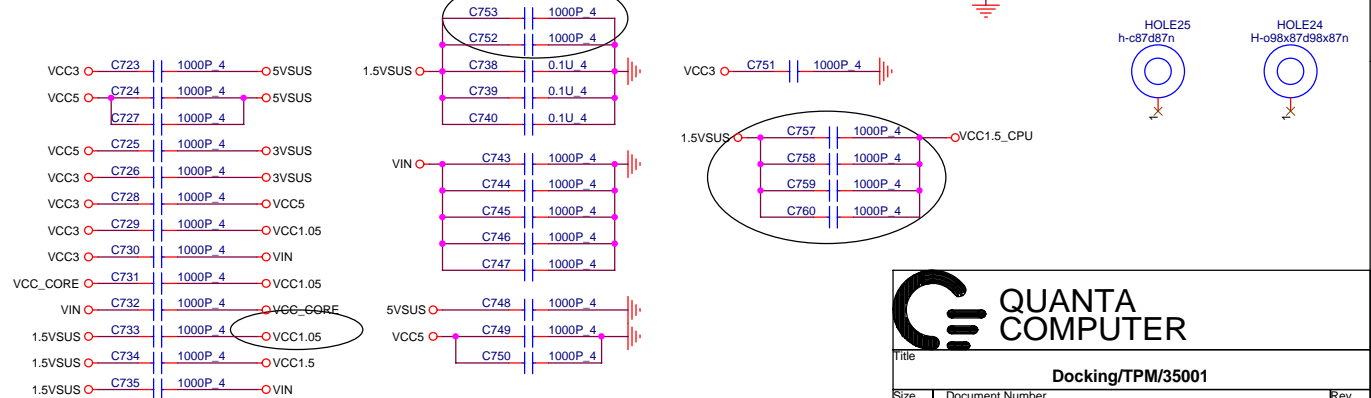
T/P to M/B (FPC)



35001



EMI



QUANTA COMPUTER

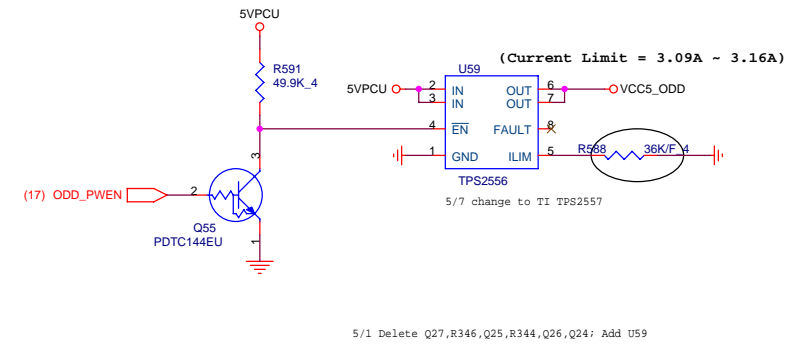
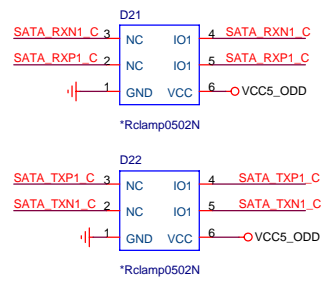
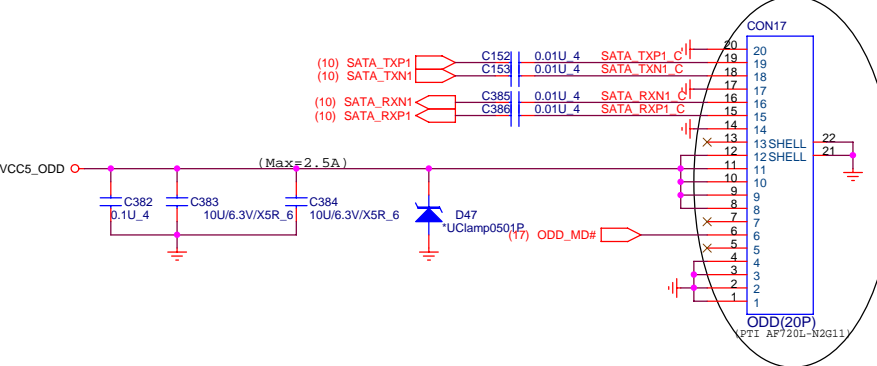
Title: **Docking/TPM/35001**

Size: Document Number: **Main Board** Rev: 2A

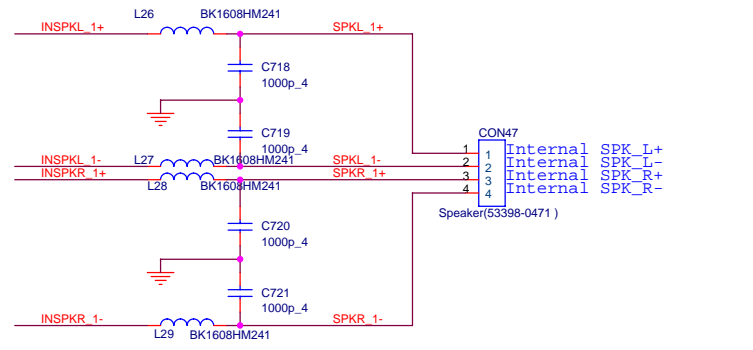
Date: Thursday, September 03, 2009 Sheet 18 of 33

1. Level 1 Environment-related Substances should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

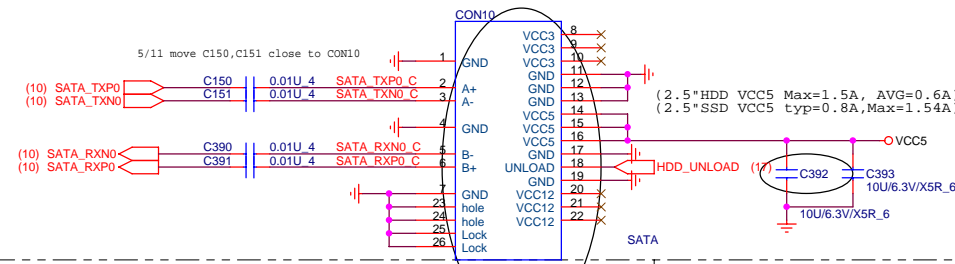
ODD CONNECTOR (FPC 20pin)



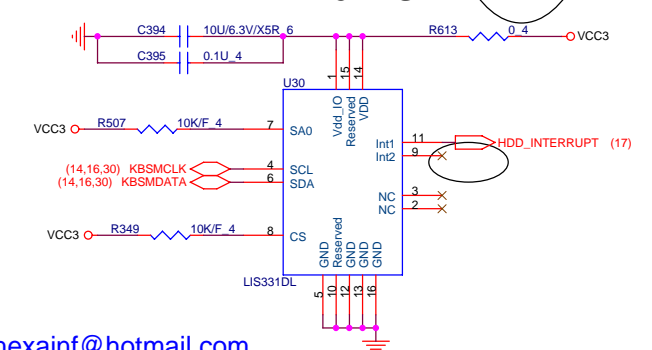
SPEAKER CONNECTOR



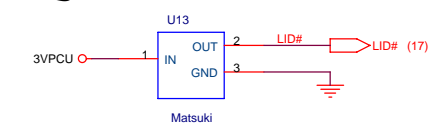
HDD CONNECTOR



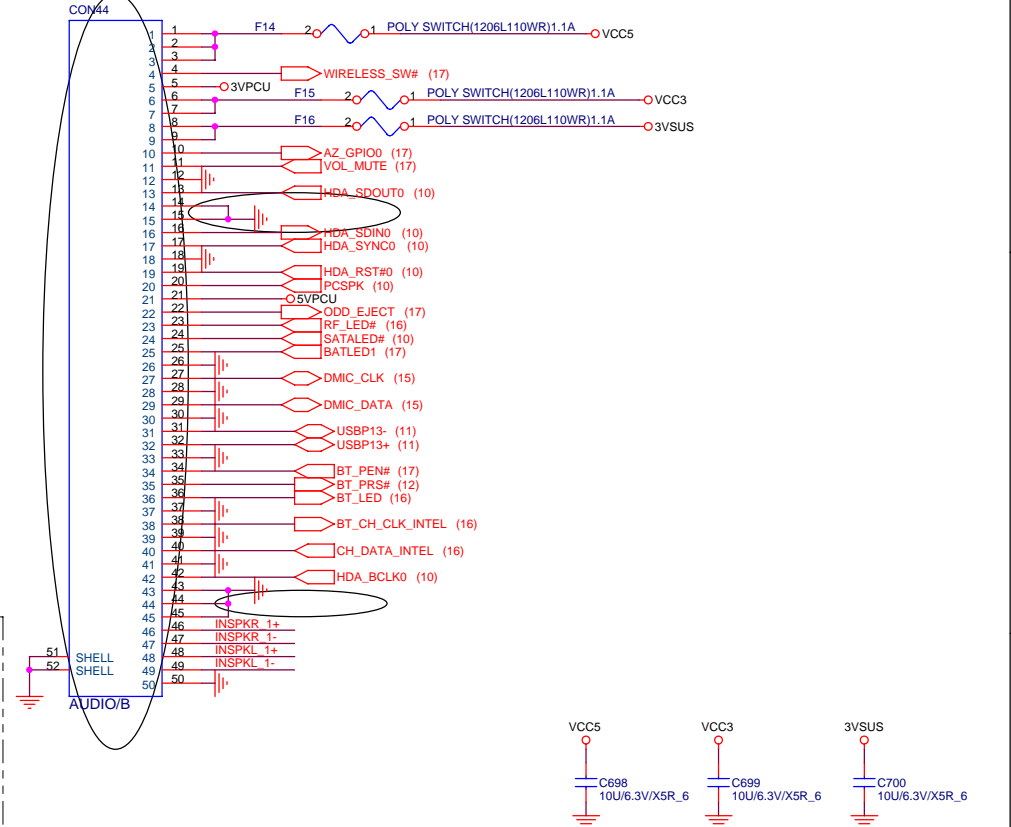
HDD PROTECT



Magnetic Lid Switch



Audio Board



1.Level 1 Environment-related Substances Should NEVER be Used.
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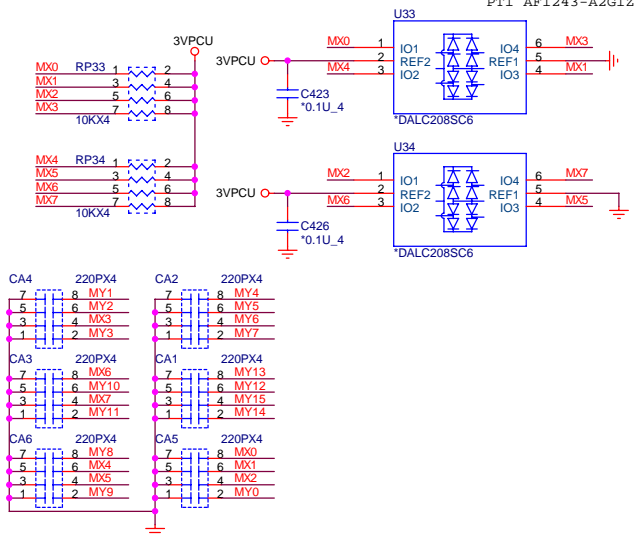
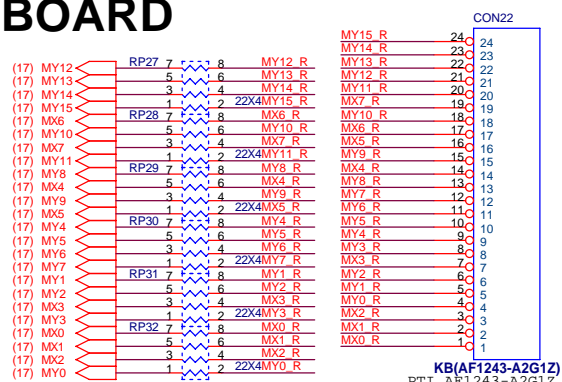
QUANTA COMPUTER

Title: **HDD/ODD/SSD**

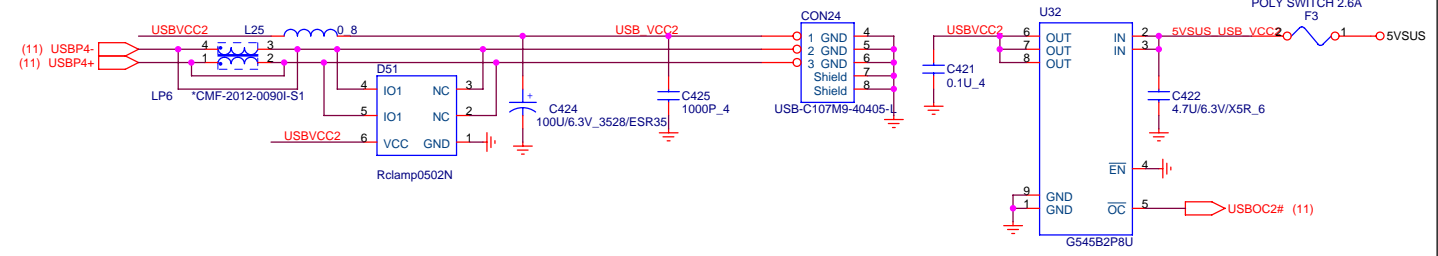
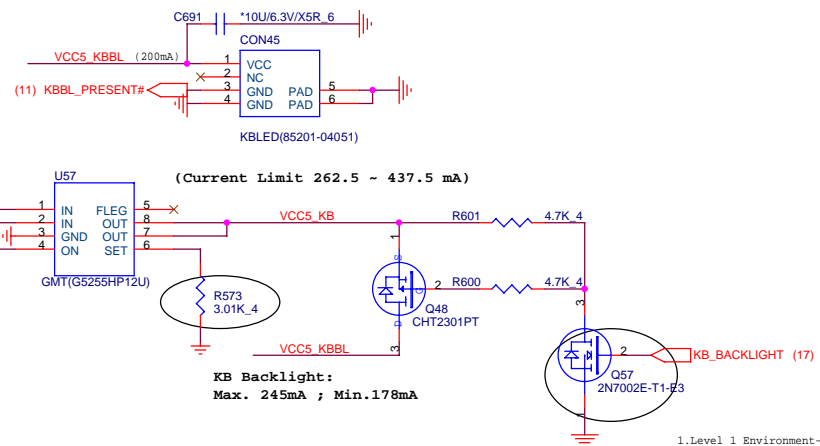
Size: Document Number: **Main Board** Rev: 2A

Date: Friday, September 04, 2009 Sheet: 19 of 33

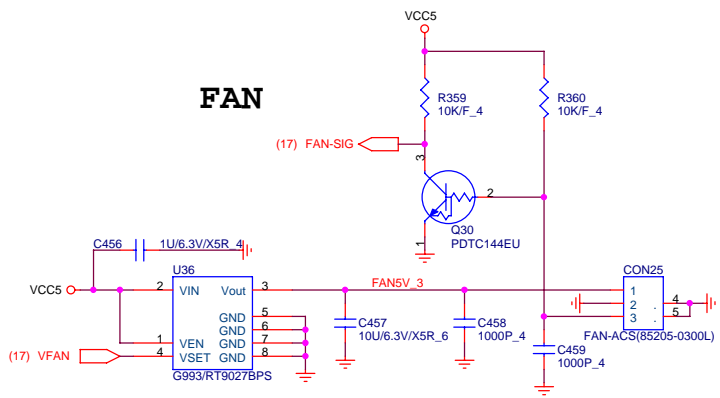
KEYBOARD



KB BACKLIGHT



FAN



1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

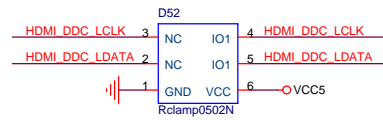
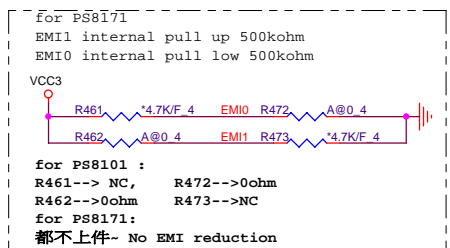
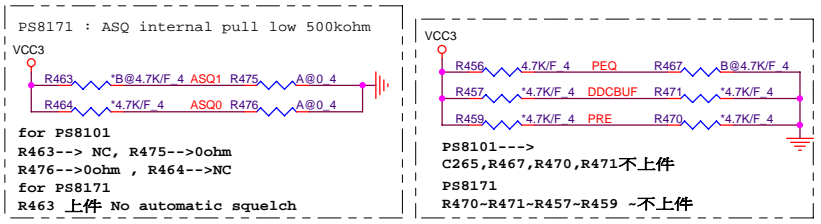
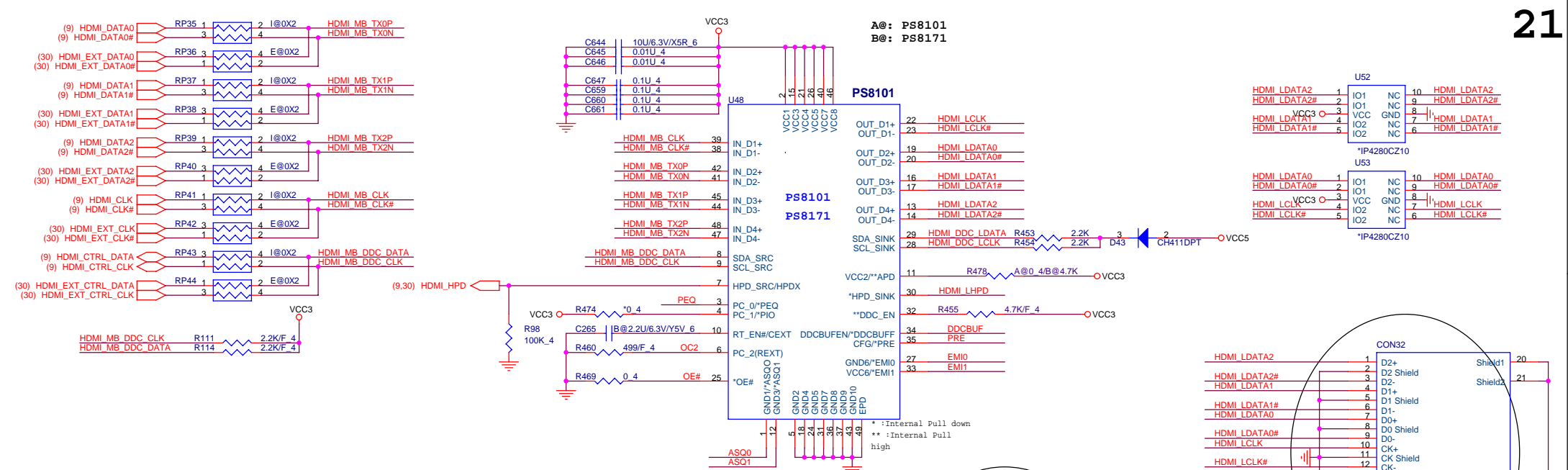
Title: **KB/USB/FAN**

Size: **Main Board**

Date: Monday, August 31, 2009

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Rev 2A



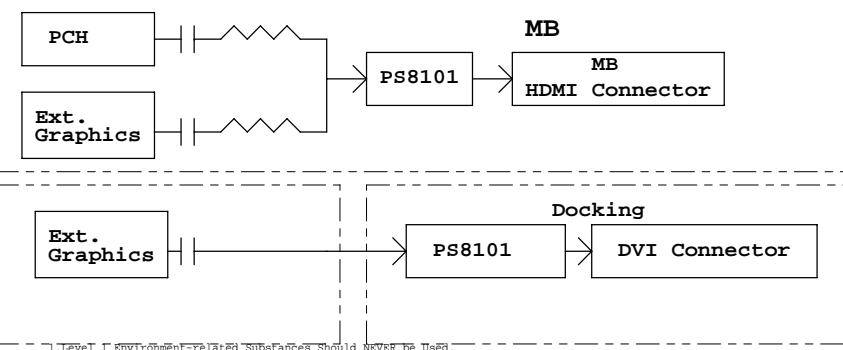
EMIO	EMI1	EMI reduction and filter setting
L	L	
L	H	※ no EMI reduction
H	L	
MID	MID	

PIN34	LEVEL	Description
DDCBUF	HIGH	Active DDC buffer enable;Setting 1
	MID	Active DDC buffer enable;Setting 2
	LOW	※ No DDC active buffer,passive DDC level shifting

PC1	PC0	EQUALIZATION
0	0	8dB
0	1	※ 4dB
1	0	12dB
1	1	0dB

PIN3	LEVEL	EQ
PEQ	HIGH	7dB
	MID	※ 2dB
	LOW	4dB

PIN35	LEVEL	dB
PRE	HIGH	1.2dB
	MID	2dB
	LOW	※ 0dB

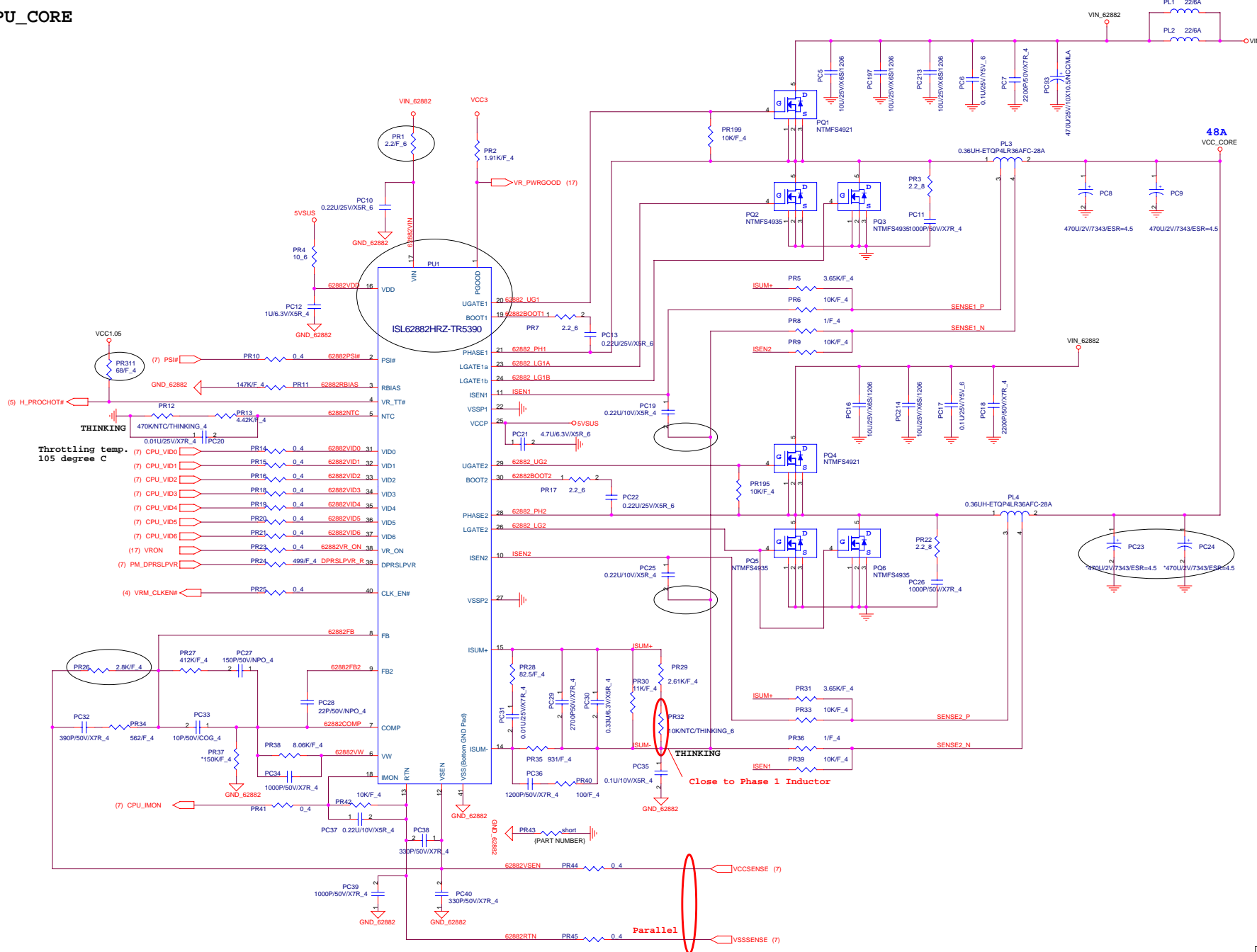


PIN11	LEVEL	Description
APD	HIGH	Automatic power down enable
	MID	
	LOW	Automatic power down disable

PIN1	LEVEL	Automatic Squelch
ASQ[1,0]	HL	※ No automatic squelch
	LL	Level=100mVpp,default timer
	LH	Level=150mVpp,default timer
	HH	Level=200mVpp,default timer
	ML	Level=120mVpp,extended timer
	MH	Level=100mVpp,extended timer
	LM	Level=80mVpp,extended timer
	HM	Reserved
	MM	Reserved

**QUANTA
COMPUTER**

Size	Document Number	Rev
	GD3 Main Board	2A

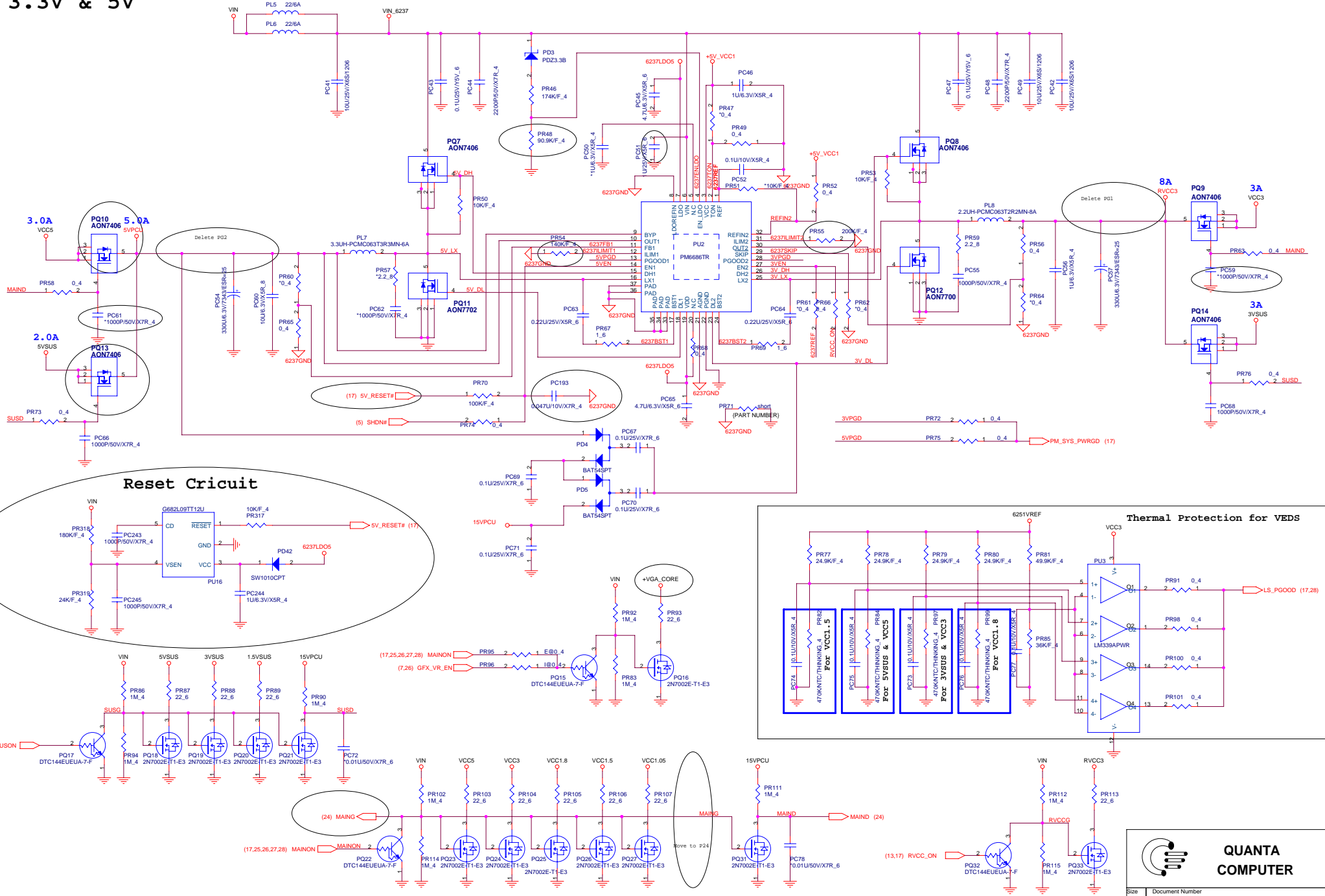


QUANTA COMPUTER

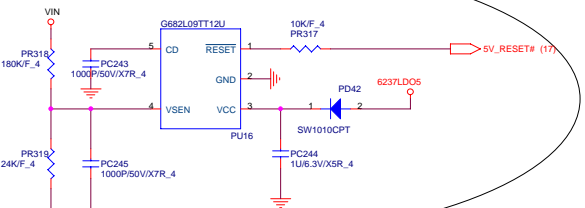
Size	Document Number	Rev
	GD3 Main Board	2A
Date:	Wednesday, September 02, 2009	Sheet 22 of 33

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Welding resins only from the business Partners that Sony approves as Green Partners.

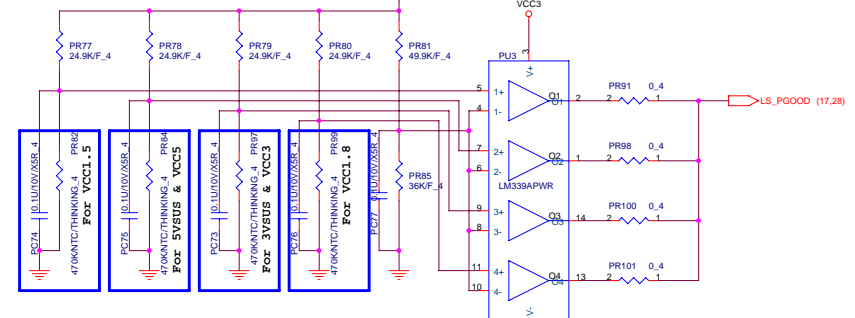
3.3V & 5V



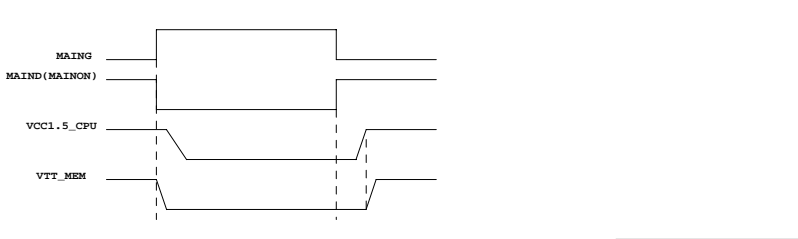
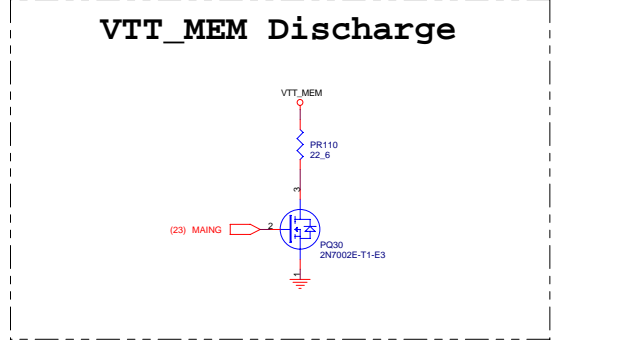
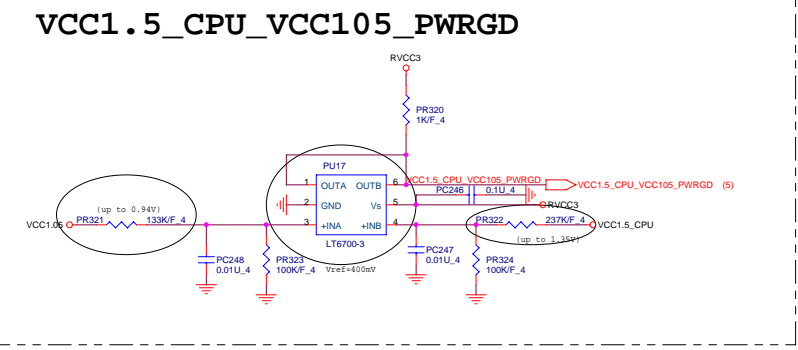
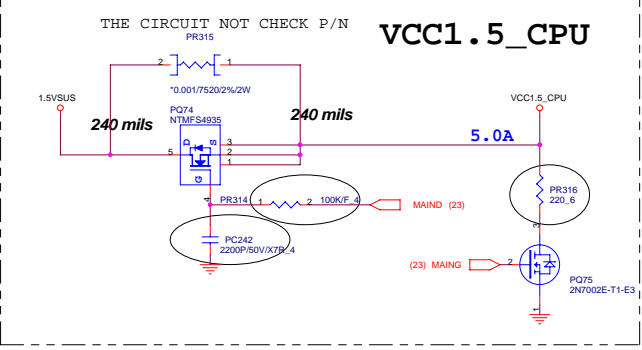
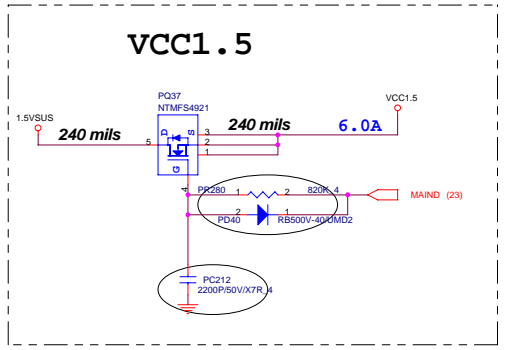
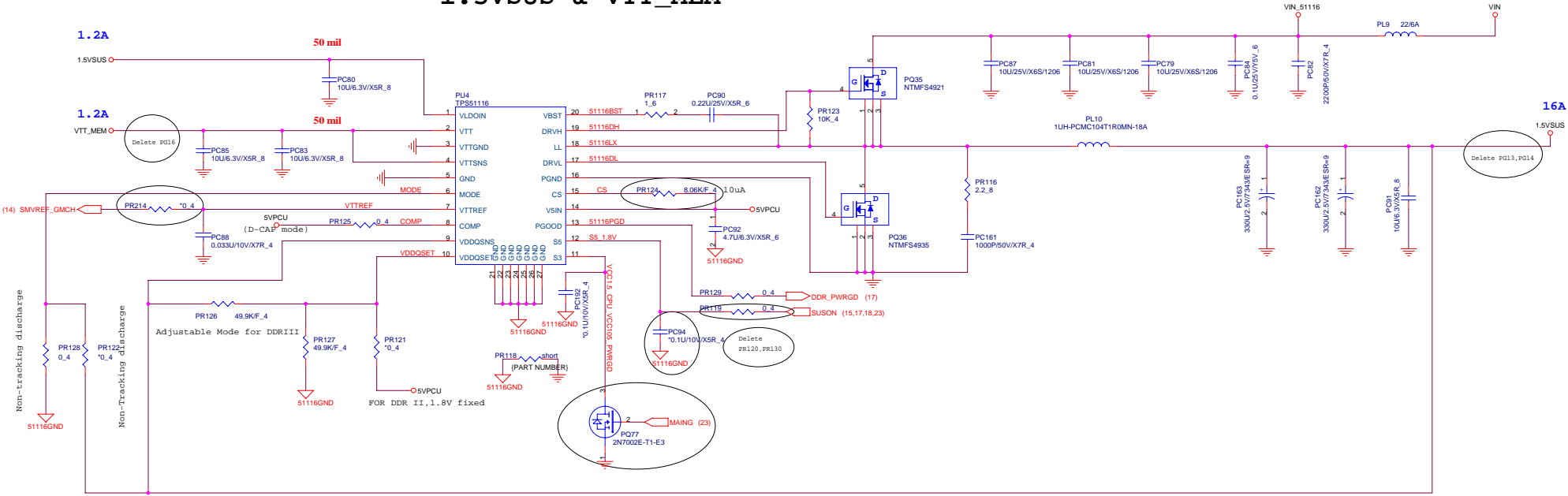
Reset Circuit



Thermal Protection for VEDS



1.5VSUS & VTT_MEM



MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

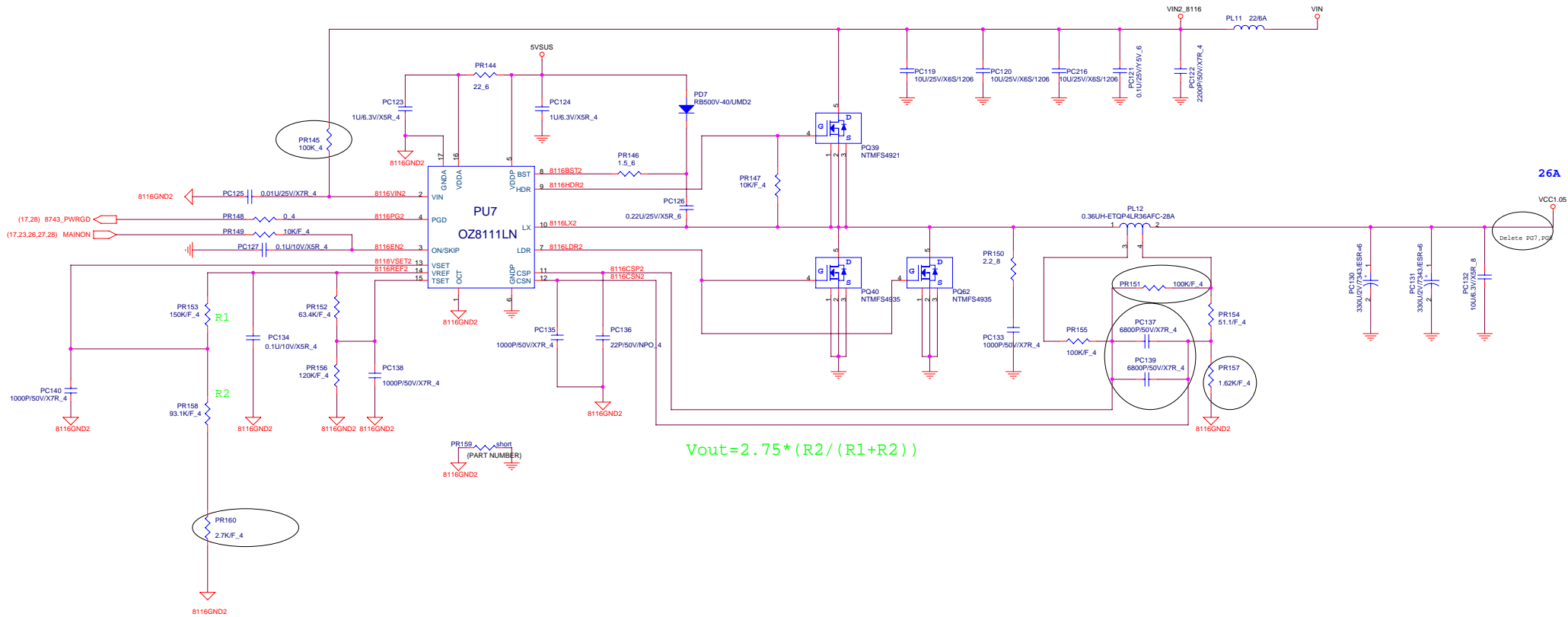
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 Fixed	VDDQSN5/2	DDR
5V	1.8 Fixed	VDDQSN5/2	DDR2
FB-Resistor	Adjustable	VDDQSN5/2	1.5V<VDDQ<3V

VTT = VTTREF = VDDQSN5/2 = 0.9V

STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

**QUANTA
COMPUTER**

Size	Document Number	Rev
GD3 Main Board		2A
1.Level 1 Environment-related Substances Should NEVER be Used. 2.Purchase ink, paints, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners. Date: Wednesday, September 02, 2009 Sheet 24 of 33		



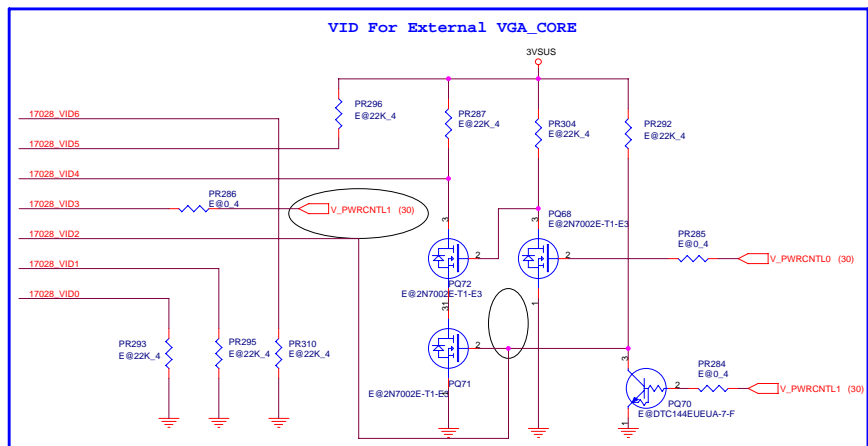
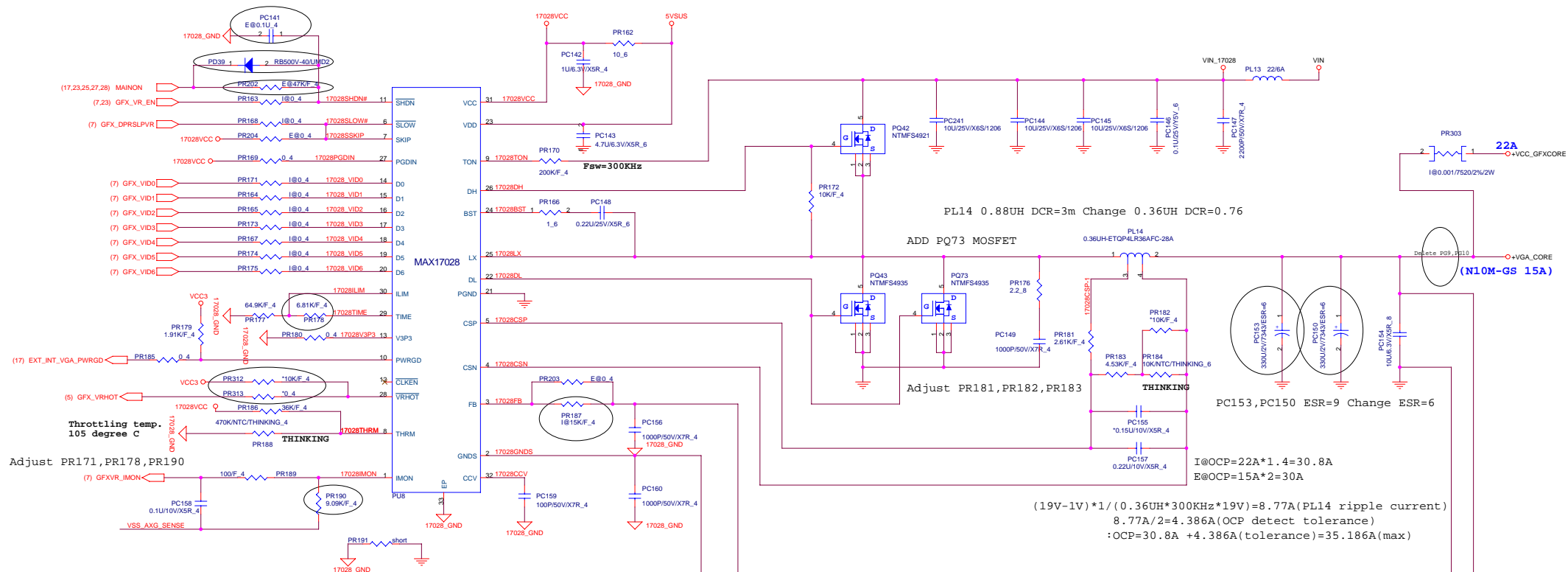
$V_{out} = 2.75 * (R2 / (R1 + R2))$

(Ext. Graphice Plaes NDI
RQ41, PR161)

VTT_SEL	VCC1.05-1
High	1.05V
Low	1.10V

**QUANTA
COMPUTER**

Size	Document Number	Rev
	GD3 Main Board	1A
1.Level 1 Environment-related Substances Should NEVER be Used. 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners. Date: Friday, September 04, 2009 Sheet 25 of 33		



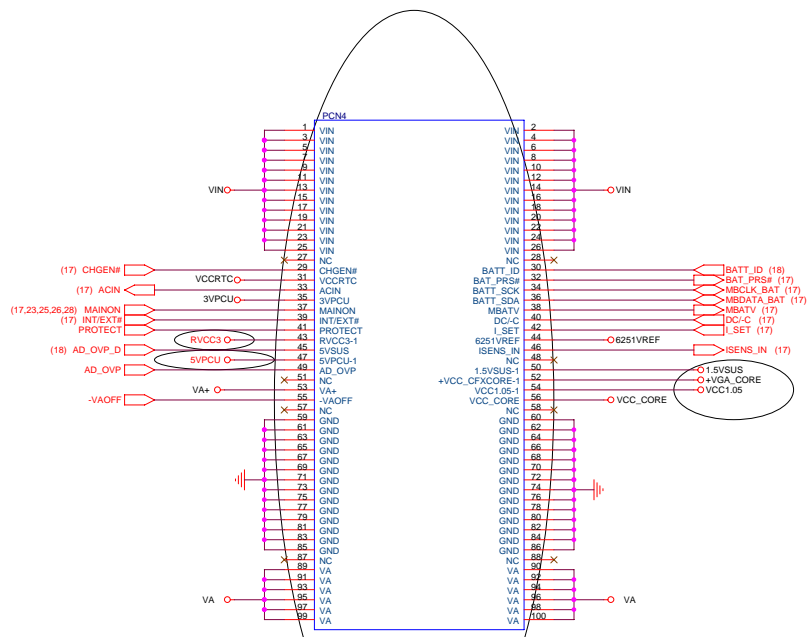
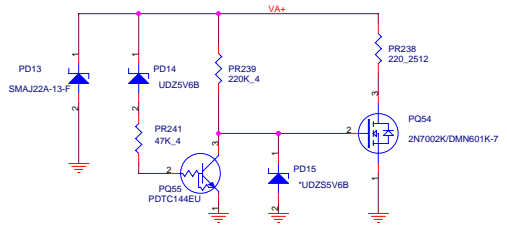
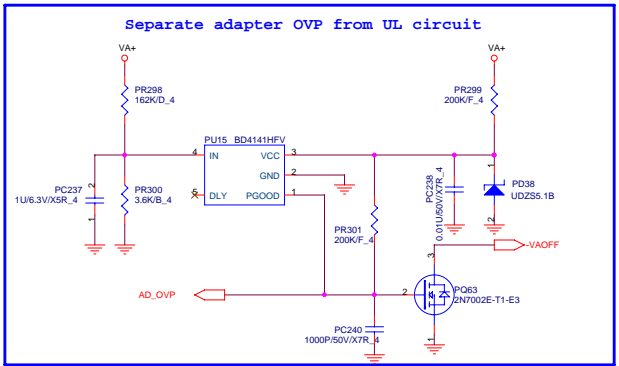
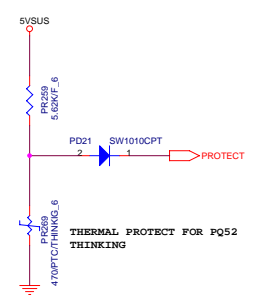
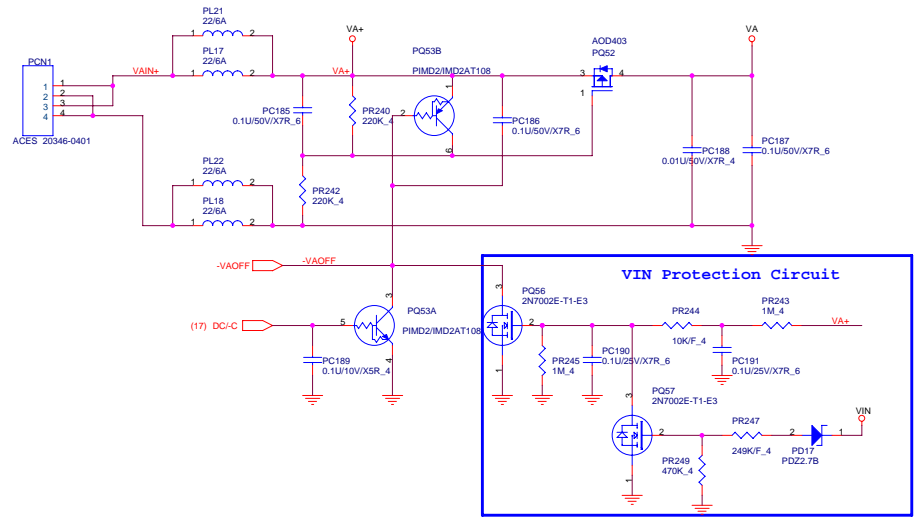
External VGA_CORE voltage setting:

V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0100100	1.05V
0	1	0110100	0.85V
1	0	0111000	0.8V

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COMPUTER**

Size: Document Number: **GD3 Main Board** Rev: 2A

1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners. Date: Friday, September 04, 2009 Sheet: 26 of 33



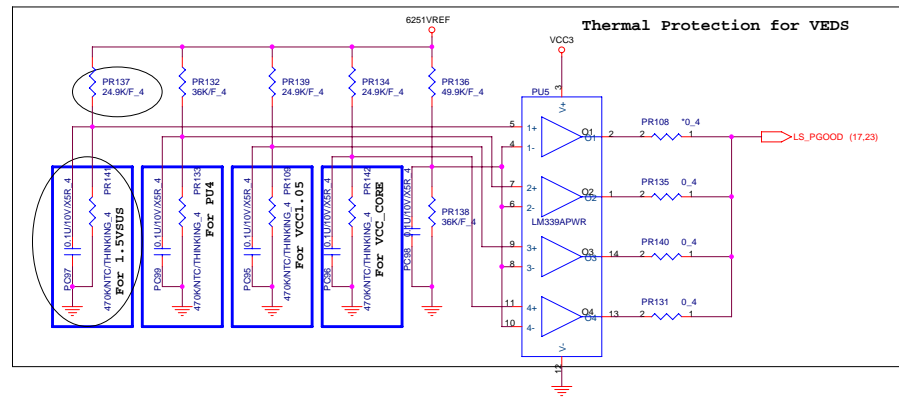
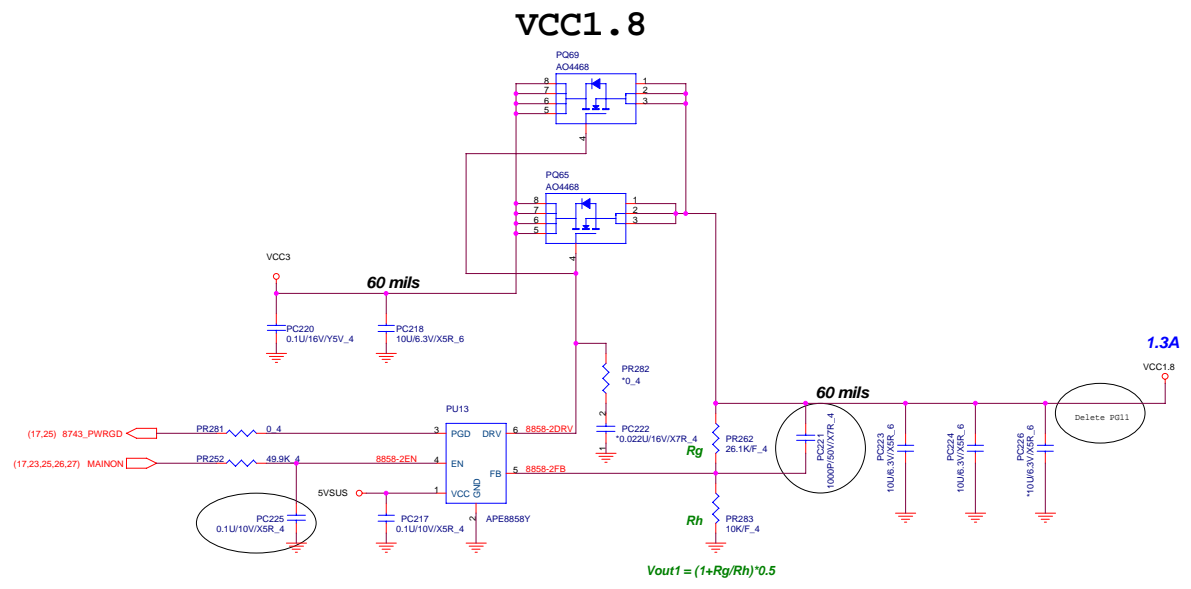
QUANTA COMPUTER

Size: Document Number
GD3 MB

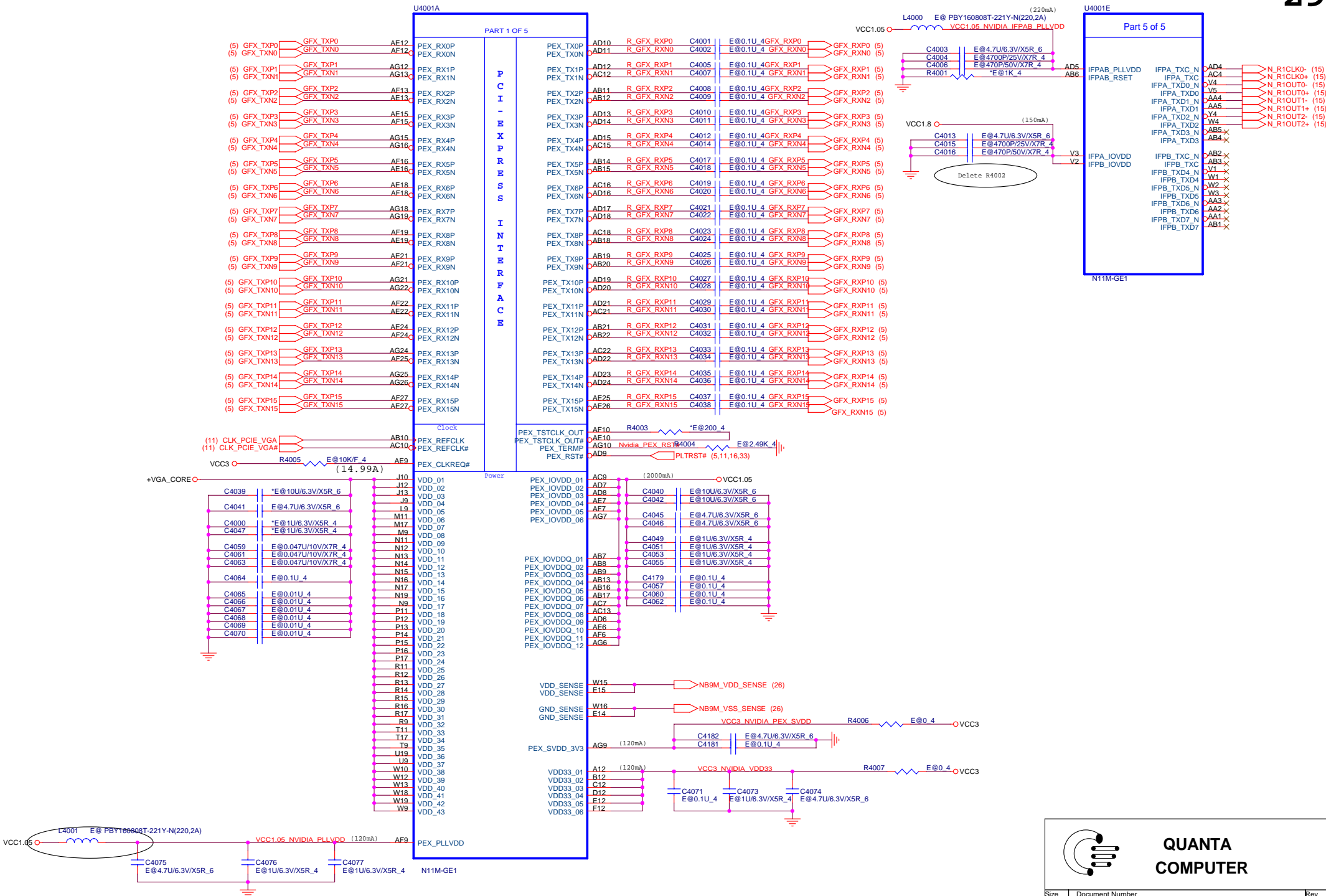
Rev: 1A

Date: Wednesday, September 02, 2009 Sheet 27 of 33

1. Level 1 Environment-related Substances should NEVER be Used.
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Date: Monday, August 31, 2009 Sheet 29 of 33

nVidia VGA_CORE voltage setting:

V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0101000	1.0V
0	1	0110100	0.85V
1	0	0111000	0.8V

Logical Strap Bit Mapping

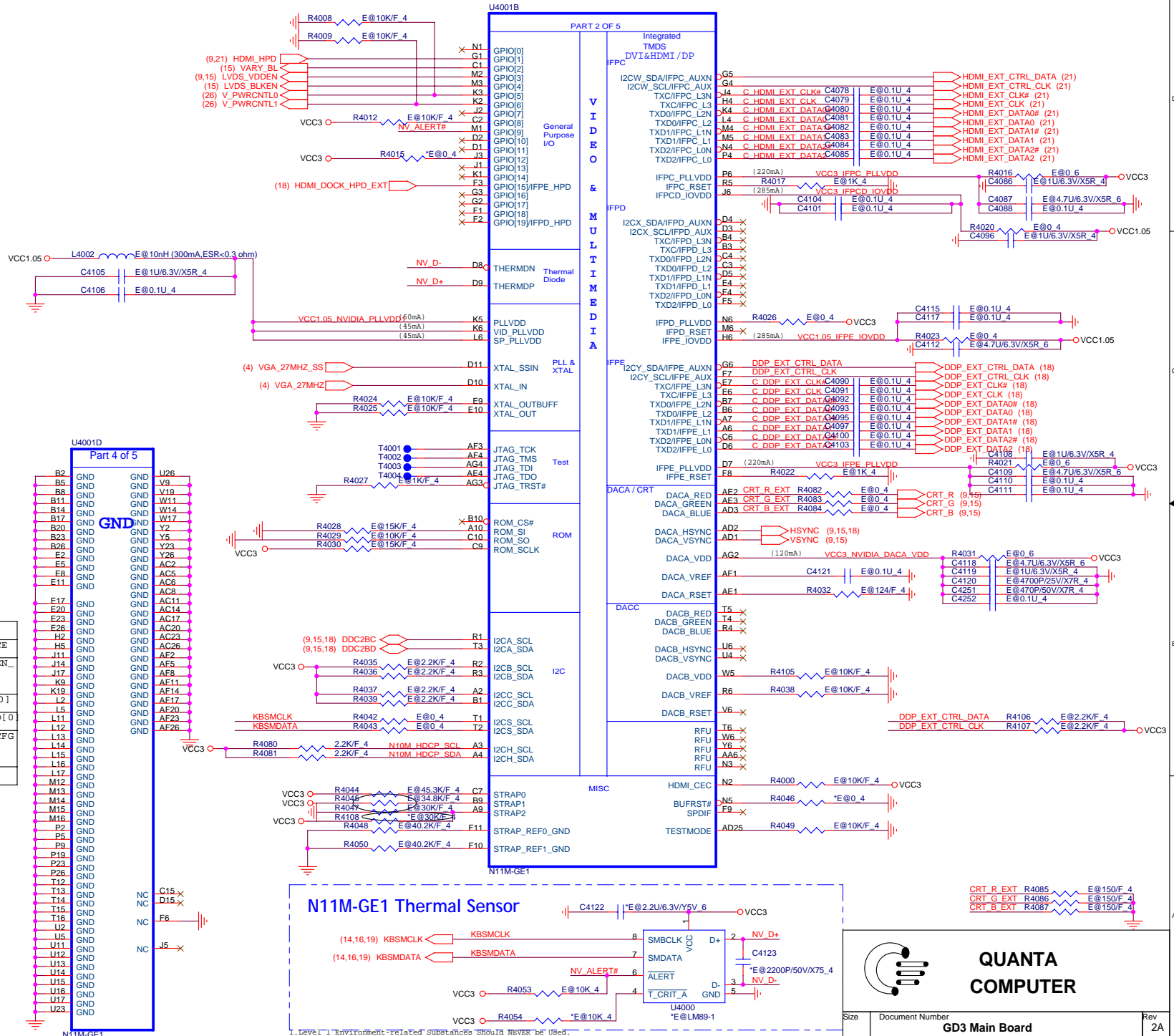
Resistor Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Strap Bit Define

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

VRAM Strap:ROM_SI ; RAMCFG[x]

VRAM Capacity	VRAM Vender	ID	R4028
DDR3 64Mx16	Samsung	0011	PD20K
	Hynix	0010	PD15K



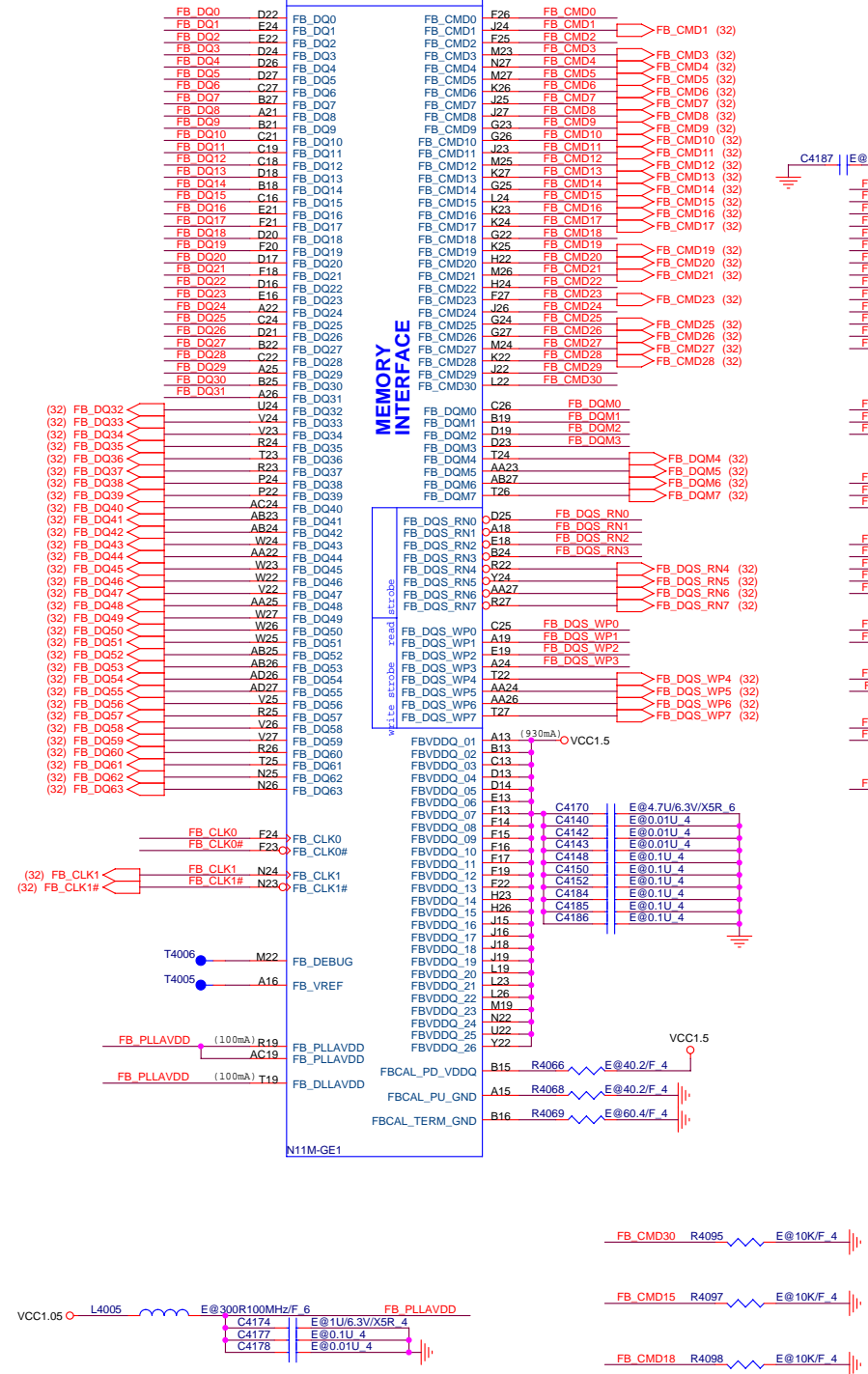
**QUANTA
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Date: Wednesday, September 02, 2009	Sheet 30 of 33

1. Level 1 Environment-Related substances should NEVER be used.
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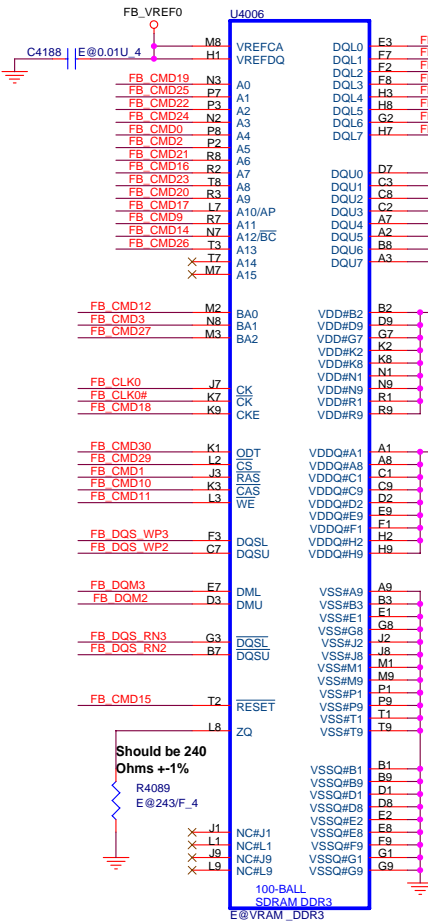
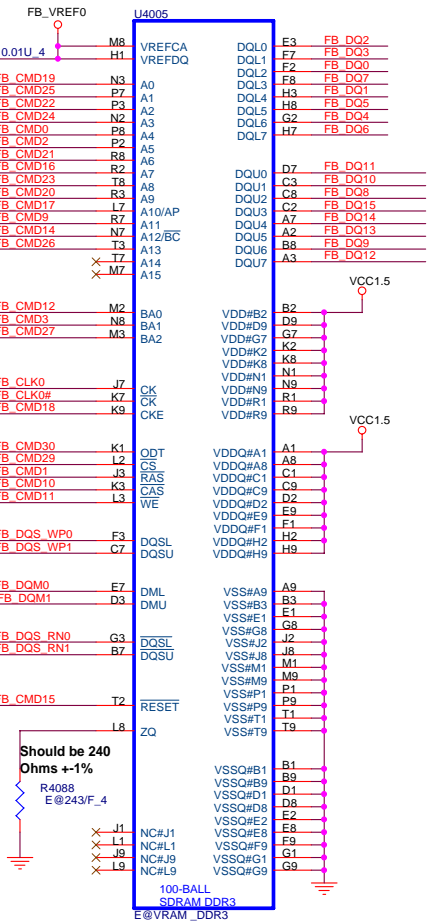
Down Side VRAM TOP/BOT

U4001C Part 3 of 5



TOP

BOT



Place near U4005

Place near U4006

Place near VRAM side

QUANTA COMPUTER

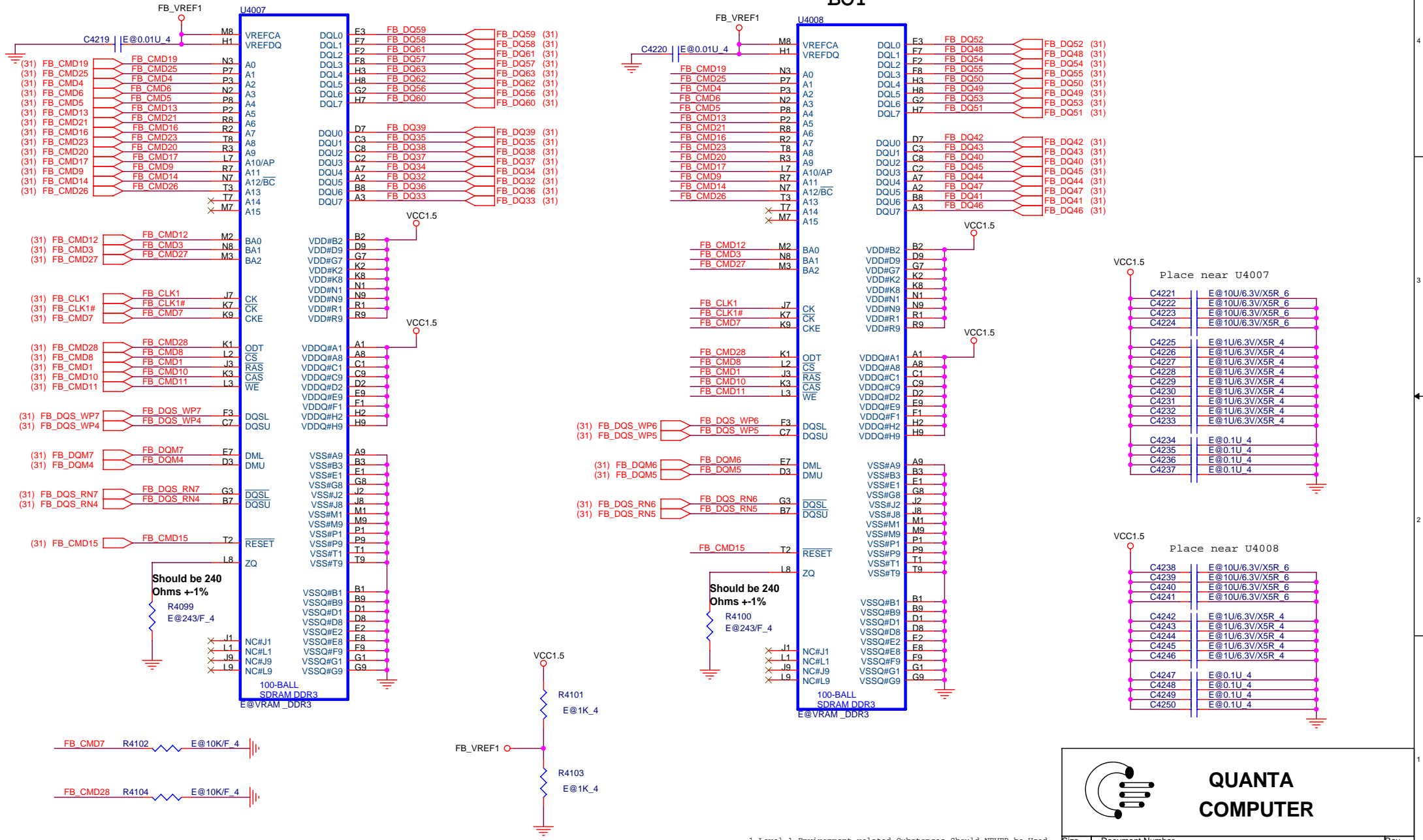
Size: Document Number: Rev: 1A


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Up Side VRAM TOP/BOT

TOP

BOT

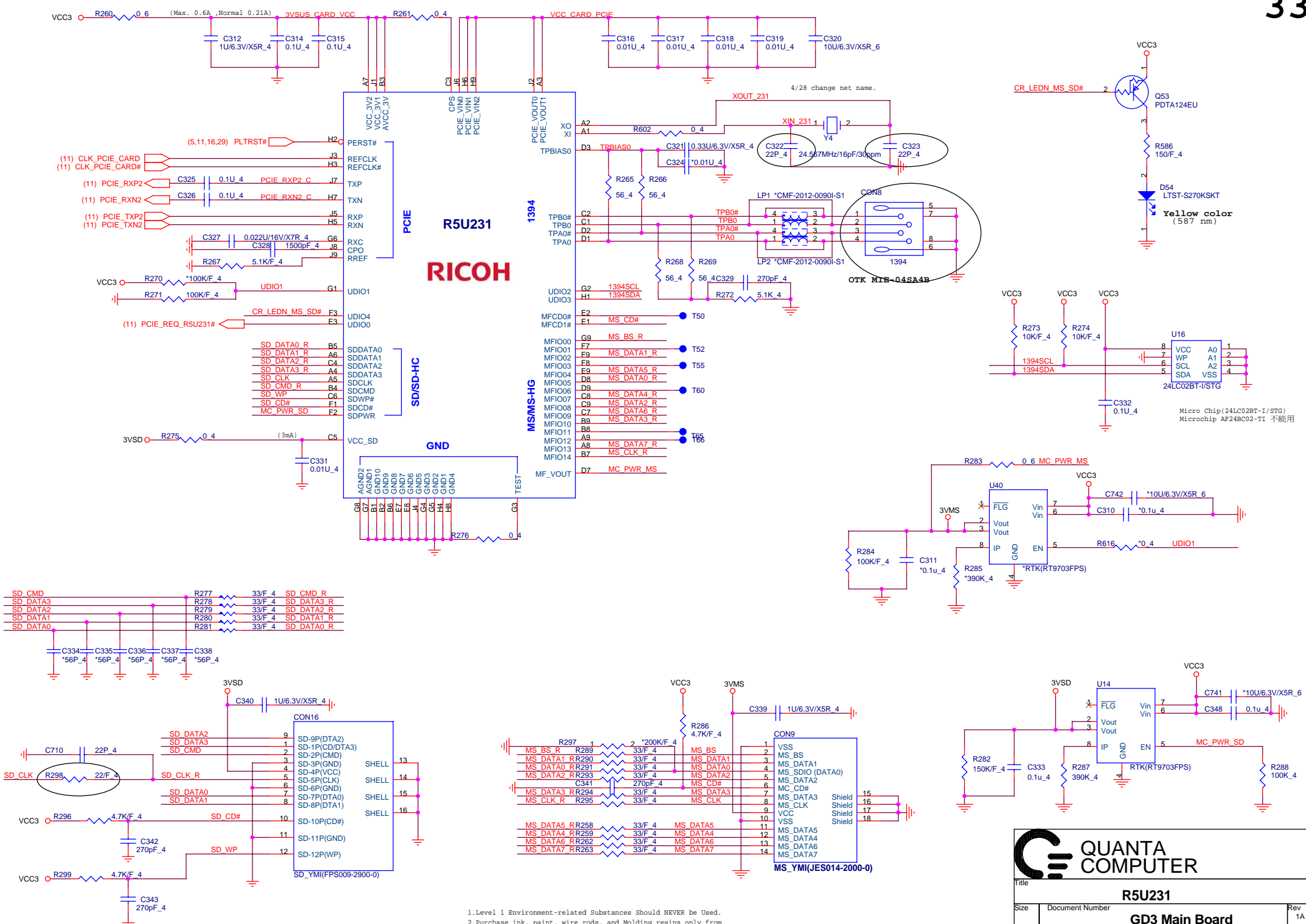




**QUANTA
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Date:	Monday, August 31, 2009	Sheet 32 of 33

1.Level 1 Environment-related Substances Should NEVER be Used.
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QUANTA COMPUTER

Title: **R5U231**

Size: **GD3 Main Board**

Date: Friday, September 04, 2009

Sheet: 33 of 33

Rev: 1A

1. Level 1 Environment-related Substances should NEVER be Used.
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