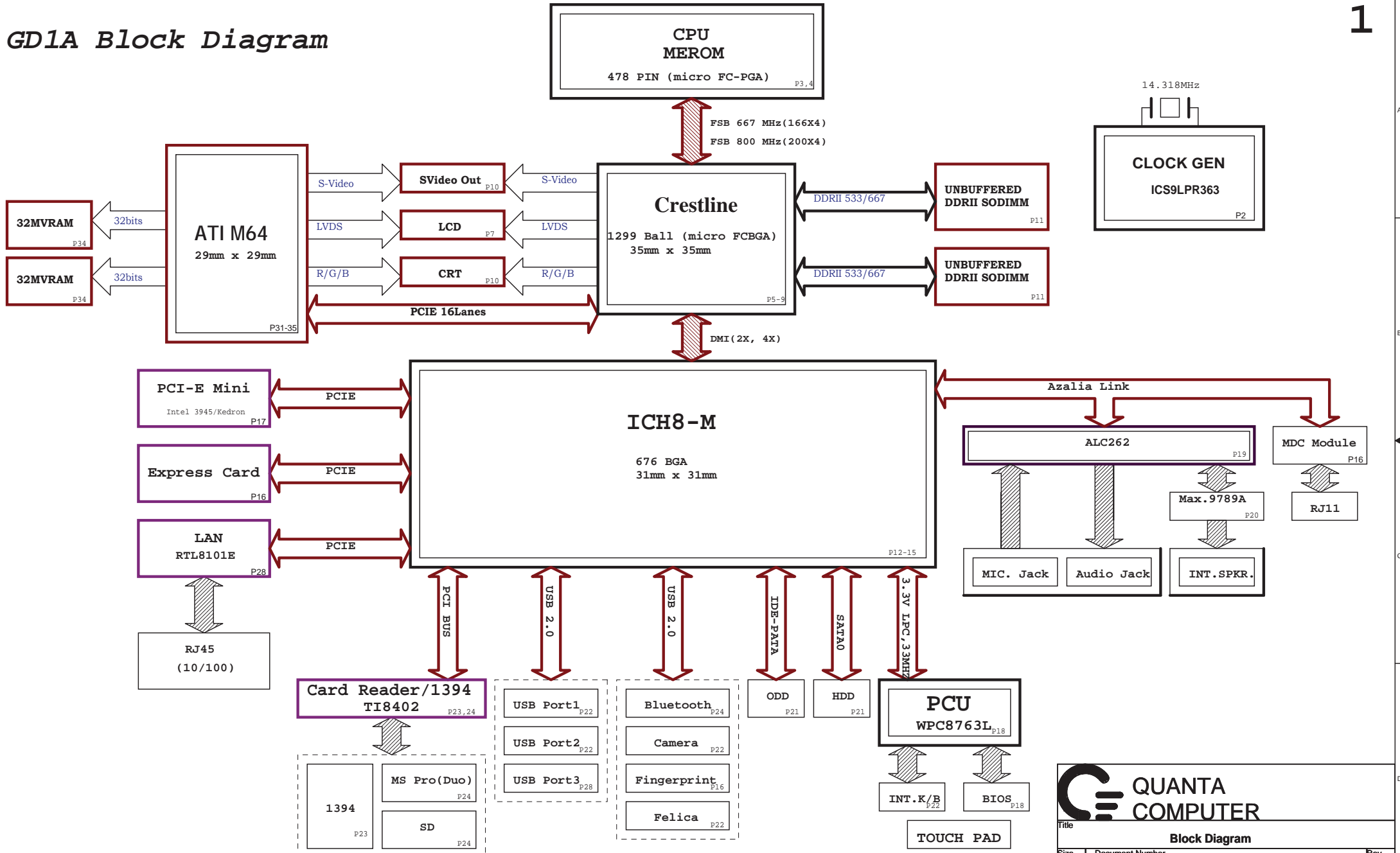
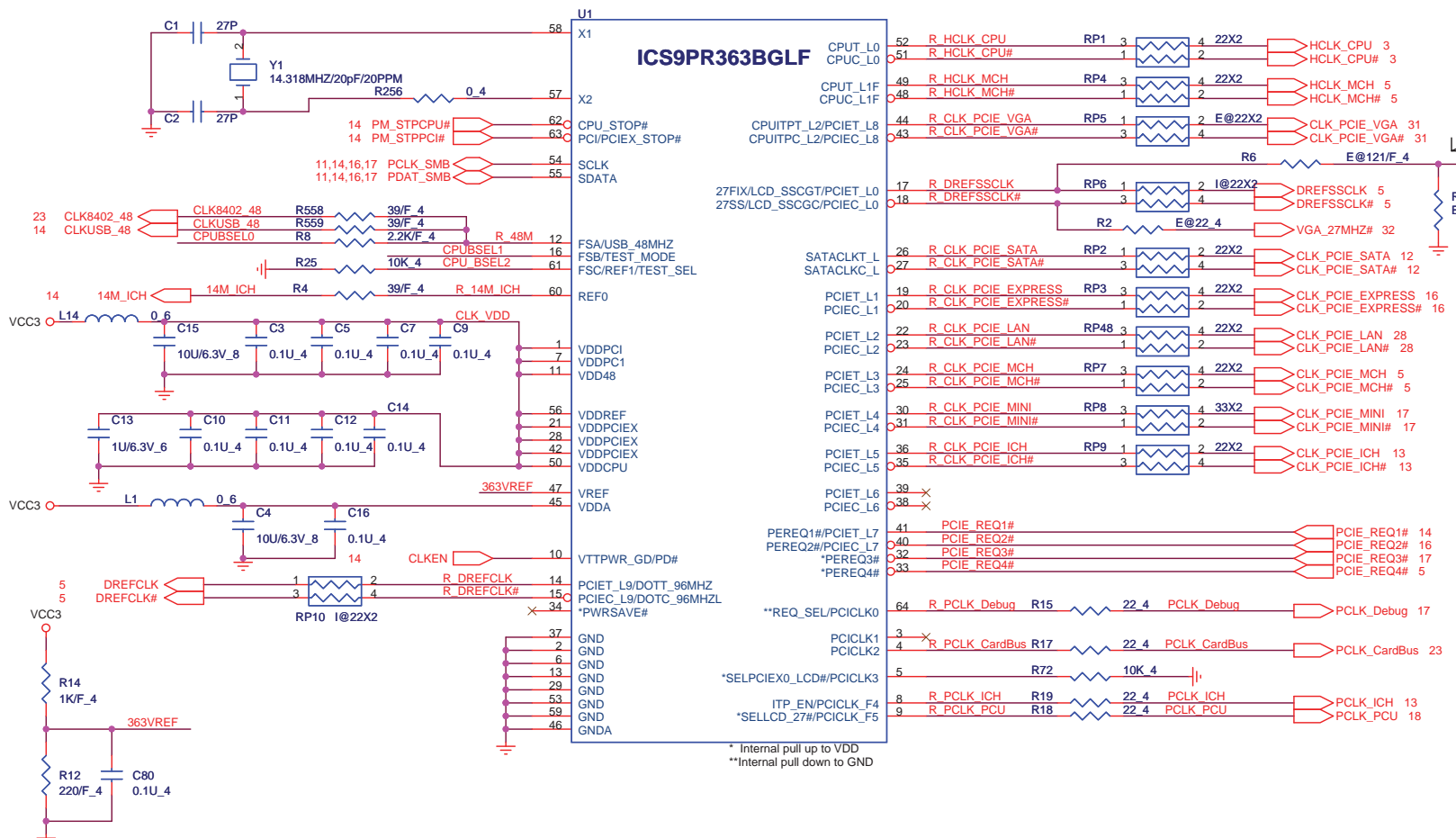


GD1A Block Diagram



1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

		QUANTA COMPUTER	
		Block Diagram	
Title	Document Number	Rev 2A	
Size B	GD1A Main Board		Date: Monday, July 23, 2007
Date:	Monday, July 23, 2007	Sheet 1 of 35	Rev 2A



Check level M64=1.2V; M72/74=1.8V

Signal		965GM	965PM
VGA_27MHZ	R6	NI	121
VGA_27MHZ#	R7	NI	71.5
CLK_PCIE_VGA	RP5	NI	22X2
DREFSSCLK	RP6	22X2	NI
DREFCLK	RP10	22X2	NI

PIN 5 R72	PIN 9 R24	PIN 14/15	PIN 17/18
LO (10K)	LO (10K) HI (NC)	PCIEX9 DOT96	27MHZ LCD
HI (NC)	LO (10K) HI (NC)	PCIEX9 DOT96	PCIEX0 PCIEX0

ITP_EN(PIN8)
 LOW : PIN43/44 SRC
 HIGH : PIN43,44 CPUTIP

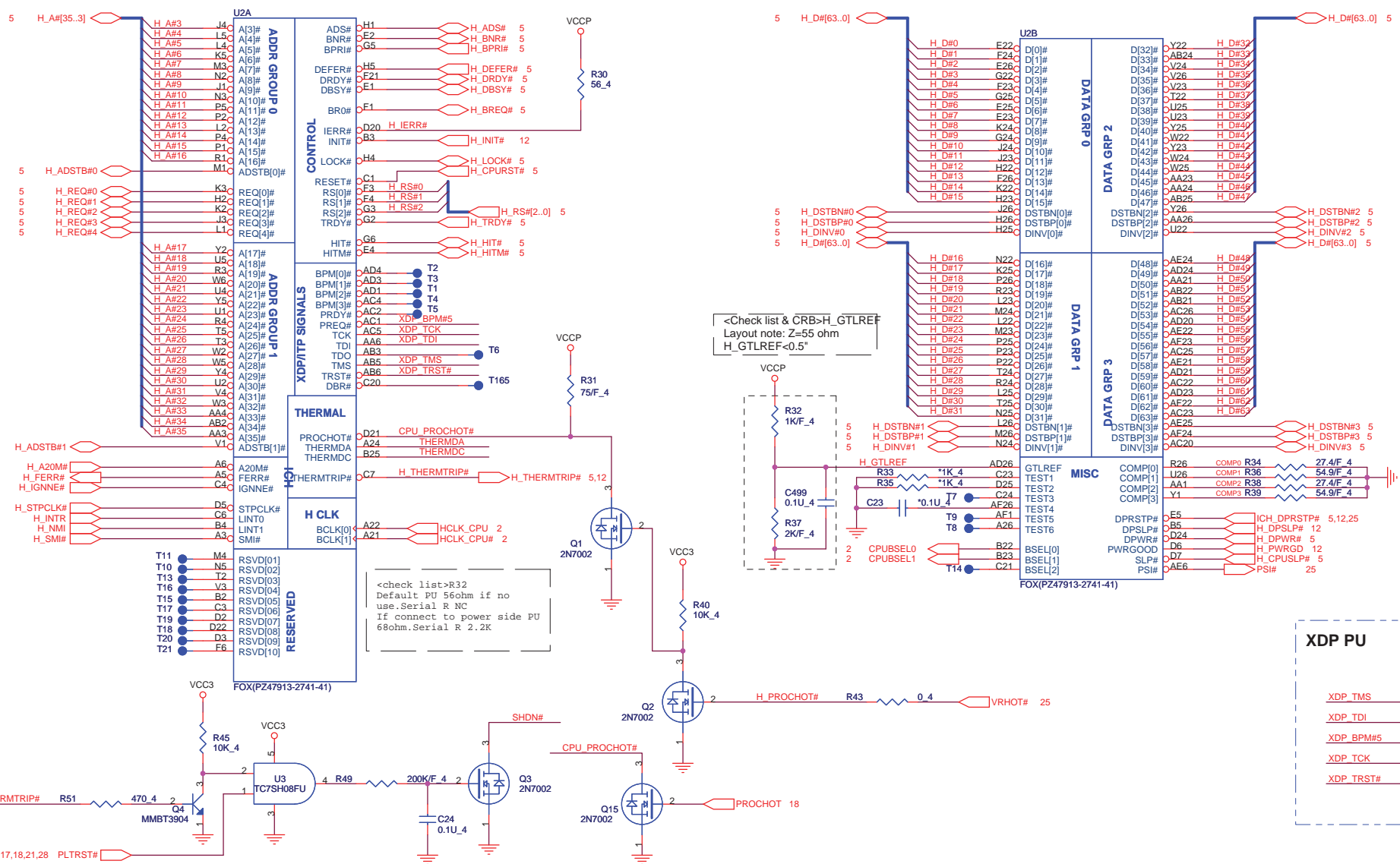
PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB ¹	DOT ¹	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

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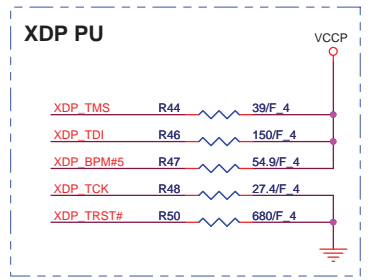
Title: **CLOCK GENERATOR**
 Size B Document Number: **GD1A Main Board** Rev 2A
 Date: Monday, July 23, 2007 Sheet 2 of 35



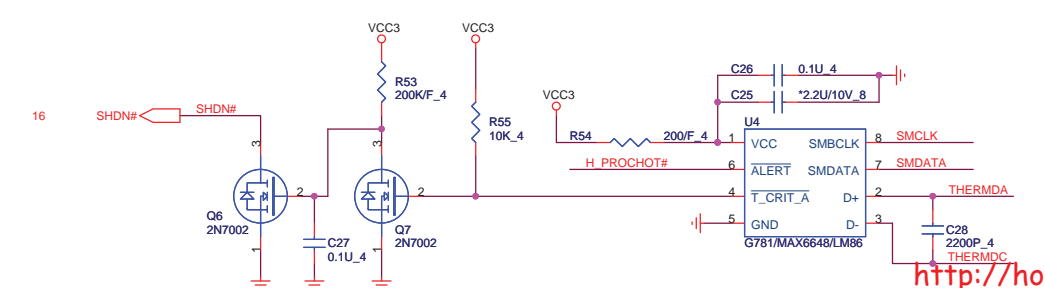
Layout note:
 Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".
 Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".

<Check list & CRB>H_GTLREF
 Layout note: Zo=55 ohm
 H_GTLREF<0.5"

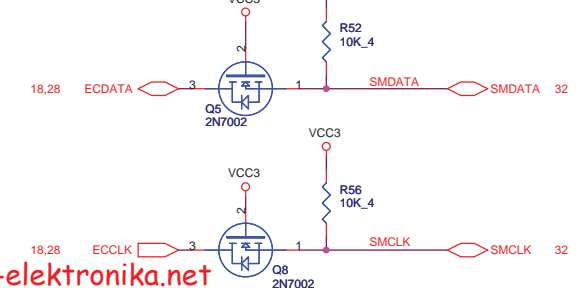
<check list>R32
 Default PU 56ohm if no use.Serial R NC
 If connect to power side PU 68ohm.Serial R 2.2K



Thermal Sensor



Thermal SMBUS



<http://hobi-elektronika.net>

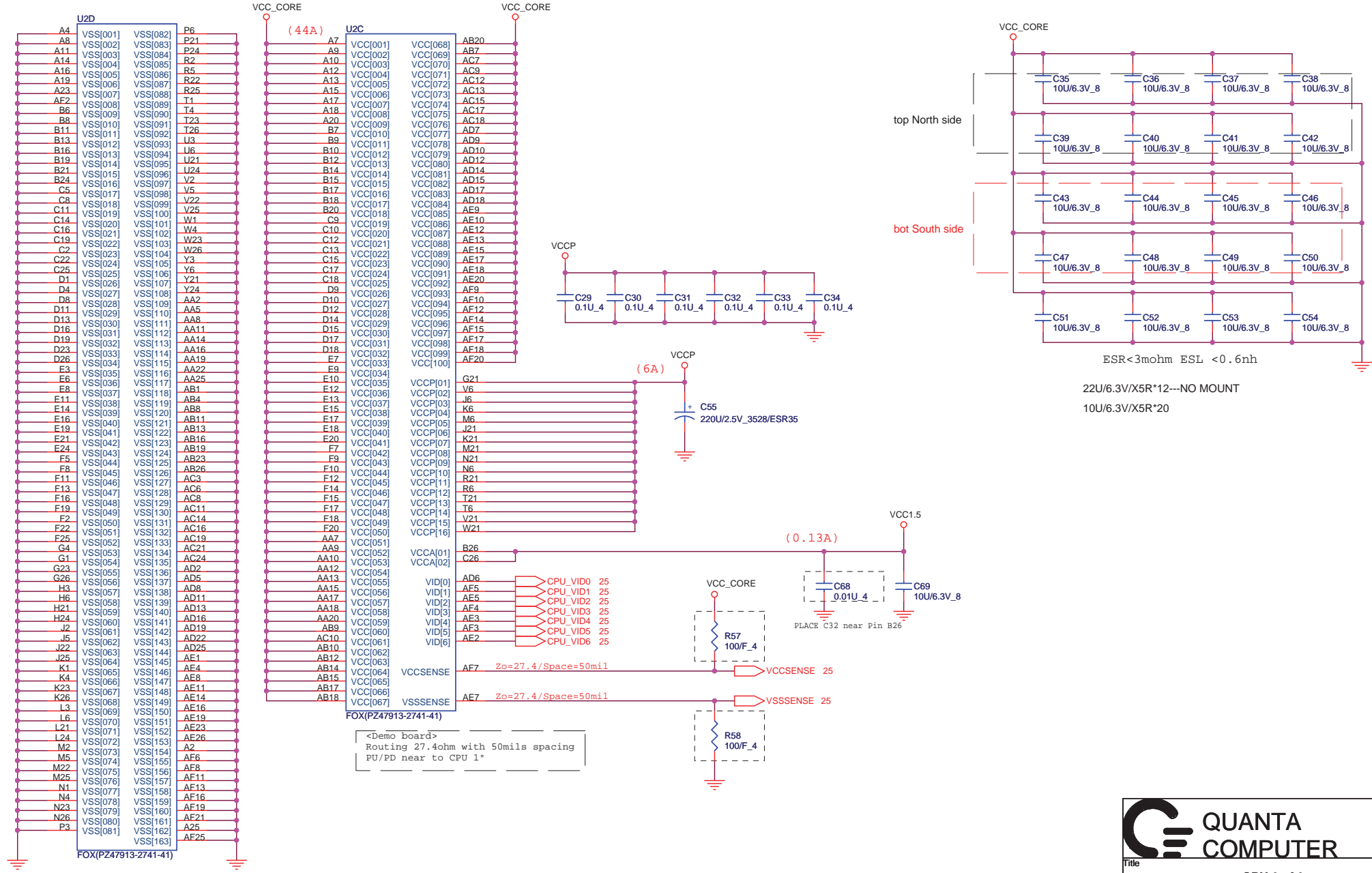
1.Level 1 Environment-related Substances should NEVER be Used.
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QUANTA COMPUTER

Title: **CPU1 of 2**

Size: Document Number **GD1A Main Board** Rev 2A

Date: Monday, July 23, 2007 Sheet 3 of 35



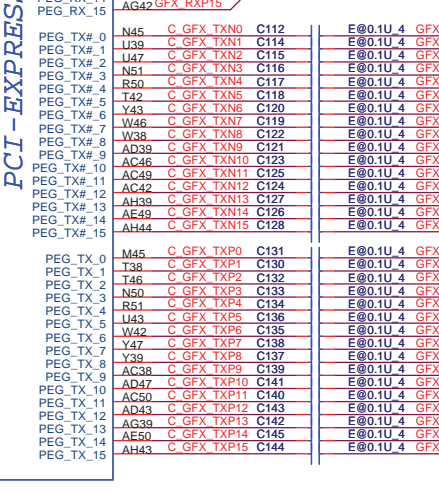
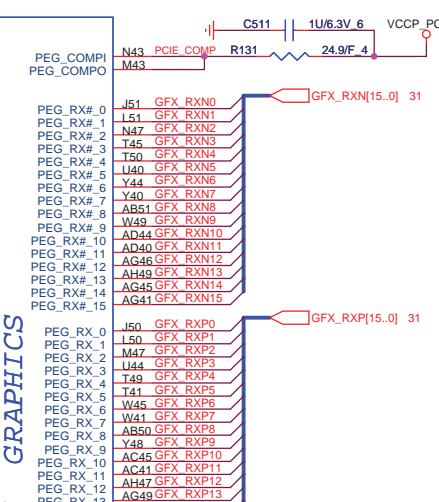
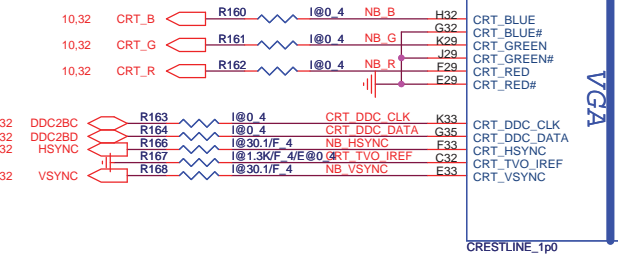
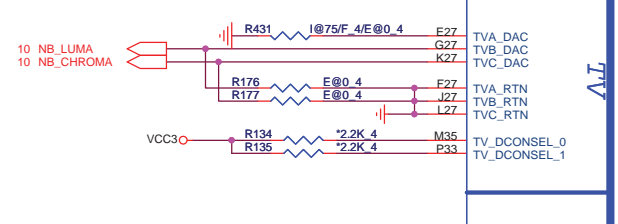
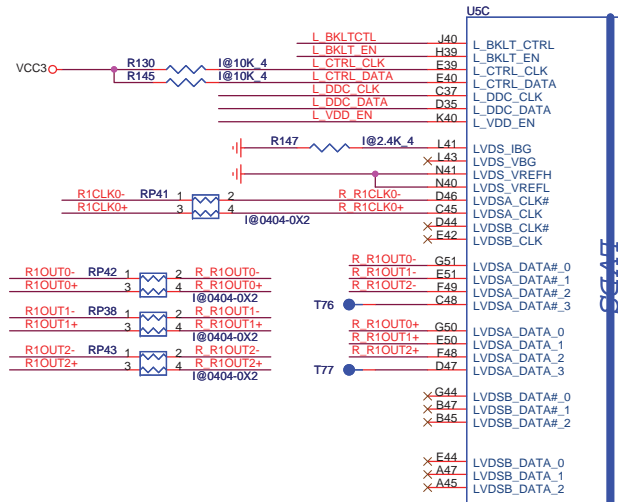
QUANTA COMPUTER

Title: CPU 2 of 2

Size B Document Number: GD1A Main Board Rev 2A

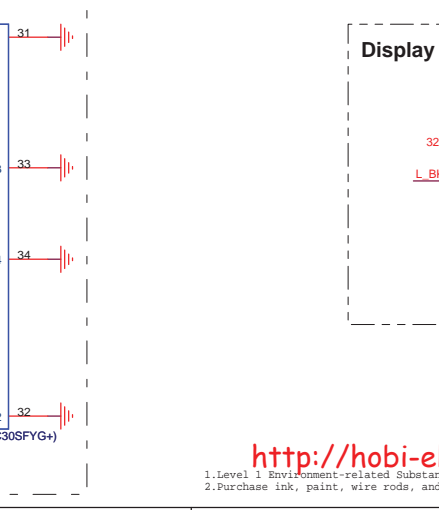
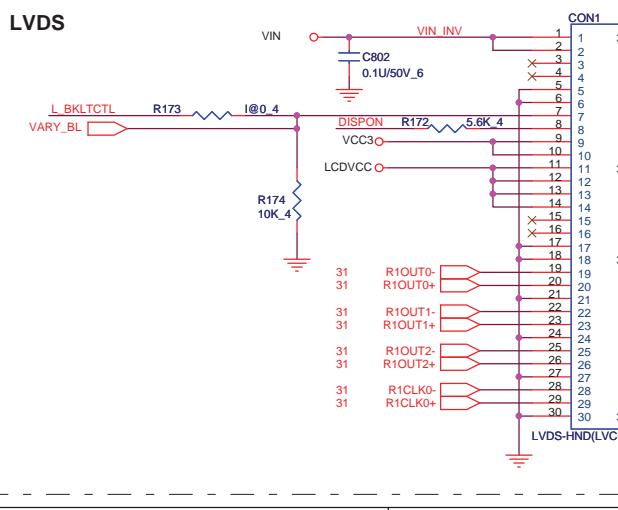
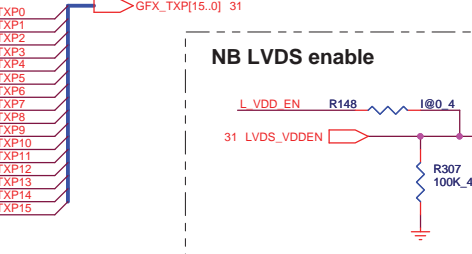
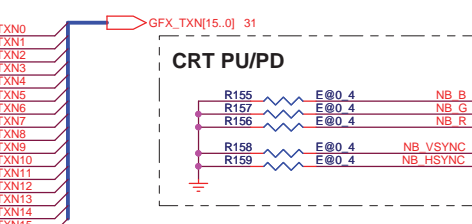
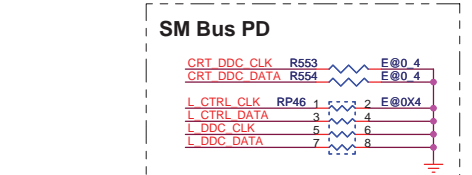
Date: Monday, July 23, 2007 Sheet 4 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Signal

Signal	GM965	PM965
NB_VSYNC	R158 NI	0_4
NB_B	R155 150_4	0_4
NB_G	R157 150_4	0_4
NB_R	R156 150_4	0_4
L_IBG	R147 2.4K_4	NI
LVDS	RP38 RP41-RP43 0X2	NI
L_BKLT_EN	R170 0_4	NI
L_CTRL_CLK	R130 10K	NI
L_CTRL_DATA	RP46 NI	0X4
LVDS_VDDEN	R146 0_4	NI
DDC2BC	R163 0_4	NI
DDC2BD	R164 0_4	NI
CRT_TVO_IREF	R167 1.3K_4	0
L_DDC_CLK	RP46 NI	0X4
L_DDC_DATA	RP46 NI	0X4
BRIGHT	R173 0_4	NI
	R175 NI	0_4



QUANTA COMPUTER

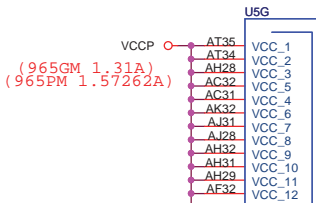
Title: **GMCH DMI VEDIO 3 of 5**

Size: Document Number **GD1A Main Board** Rev 2A

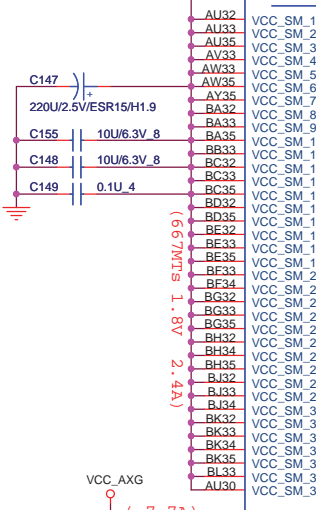
Date: Monday, July 23, 2007 Sheet 7 of 35

<http://hobi-elektronika.net>

1.Level 1 Environment-related Substances Should NEVER be Used.
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POWER

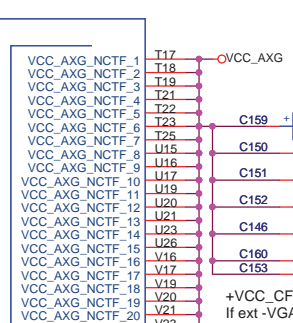


VCC SM

VCC CORE

VCC GFX

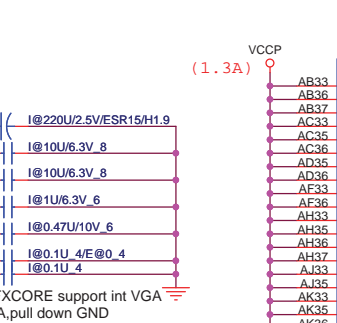
VCC SM LF



VCC AXG

VCC GFX NCTF

VCC SM LF

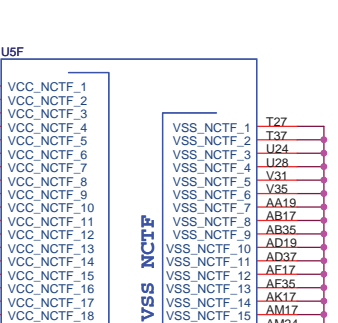


VCC AXG

VCC AXM

VCC AXM NCTF

VCC AXM LF

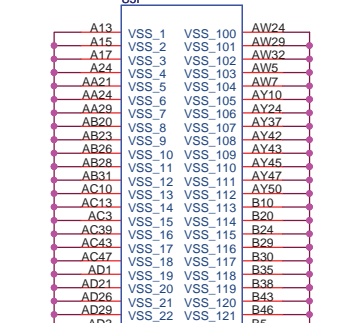


VCC NCTF

VCC SCB

VCC AXM

VCC AXM NCTF

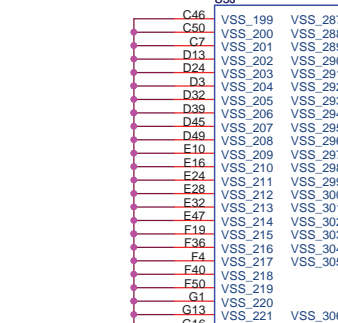


VSS NCTF

VSS SCB

VCC AXM

VCC AXM NCTF

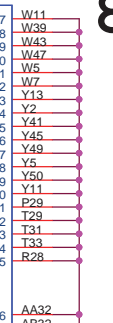


VSS

VSS SCB

VCC AXM

VCC AXM NCTF

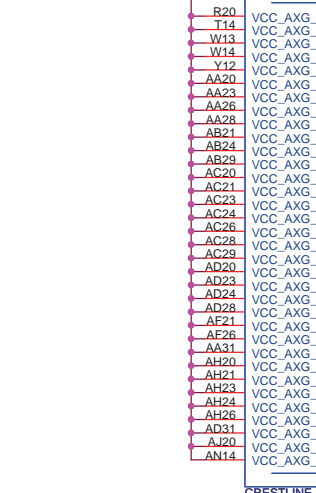


VSS

VSS SCB

VCC AXM

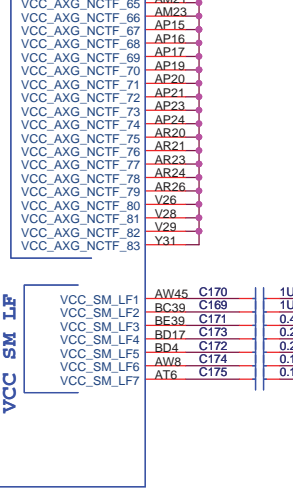
VCC AXM NCTF



VCC AXG

VCC AXM

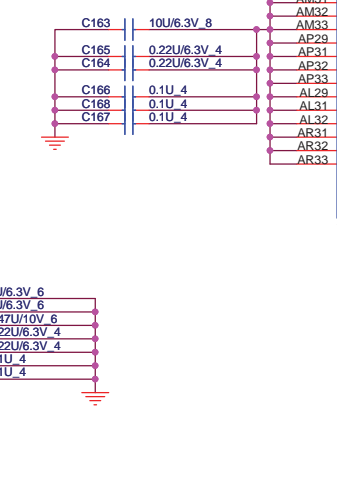
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VCC AXG

VCC AXM

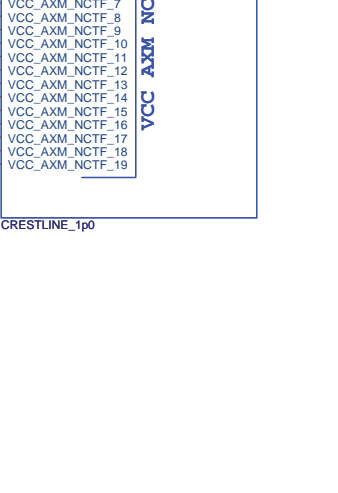
VCC AXM NCTF



VCC AXG

VCC AXM

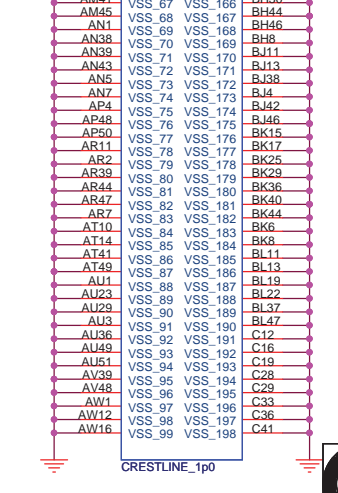
VCC AXM NCTF



VCC AXG

VCC AXM

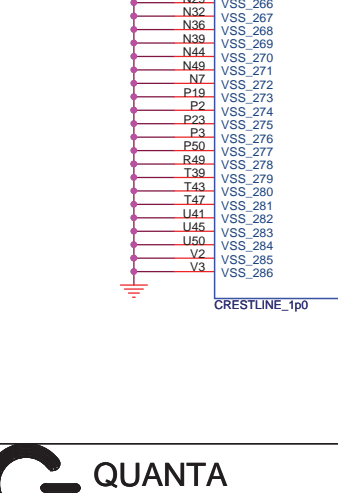
VCC AXM NCTF



VCC AXG

VCC AXM

VCC AXM NCTF



VCC AXG

VCC AXM

VCC AXM NCTF



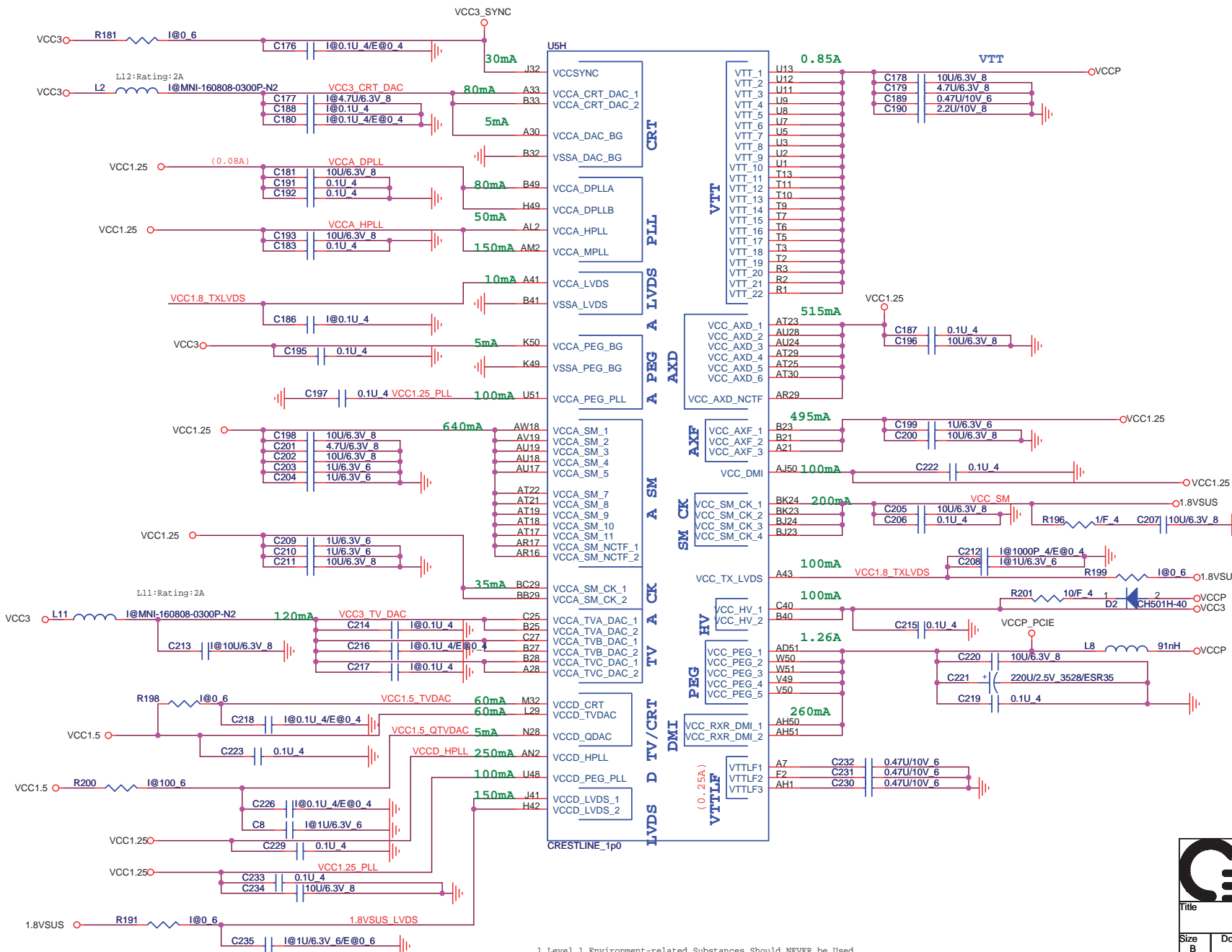
VCC AXG

VCC AXM

VCC AXM NCTF

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1. Level 1 Environment-related Substances Should NEVER be Used.
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Signal		965GM	965PM
VCCA_TV_DAC	L12	v	x
	C244	v	x
	C245	v	x
	C246	v	x
	C248	v	x
	R193	x	v
VCC1.5_TVDAC	L14	v	x
	C250	v	x
	C247	v	x
	R195	x	v
VCC1.5_QTVDAC	L17	v	x
	C257	v	x
	C258	v	x
	R197	x	v

Signal		965GM	965PM
VCCA_DAC_BG	L8	v	x
	C214	v	x
	R181	x	v
VCCSYNC	R177	v	x
	C201	v	x
	C202	v	x
	R178	x	v
	L7	v	x
VCC3_CRT_DAC	C203	v	x
	C211	v	x
	C211	x	v
	R179	x	v
VCCD_LVDS	R198	v	x
	C265	v	x
	C264	v	x
	R199	x	v
	C264	x	v
VCCA_LVDS	R183	0_4	NC
	C208	0.01u_4	NC
	C209	0.1u_4	NC
	R184	NC	0_4
	C208	NC	0_4
VCC_TX_LVDS	R192	v	x
	C240	v	x
	C238	v	x
	C238	v	x
	R191	x	v

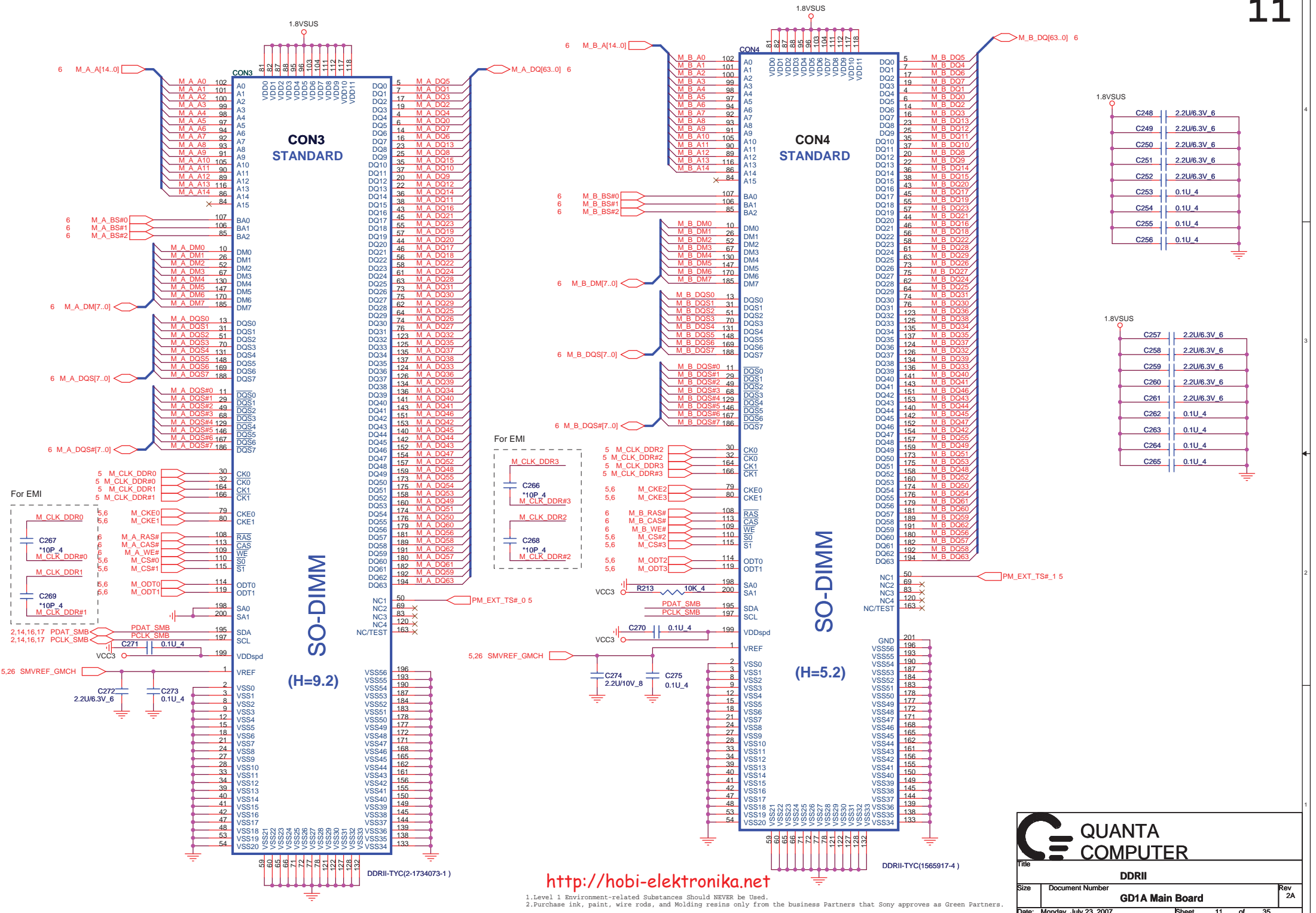
1.Level 1 Environment-related Substances Should NEVER be Used.
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**QUANTA
COMPUTER**

Title: **GMCH Power 25 of 5**

Size B Document Number: **GD1A Main Board** Rev 2A

Date: Monday, July 23, 2007 Sheet 9 of 35



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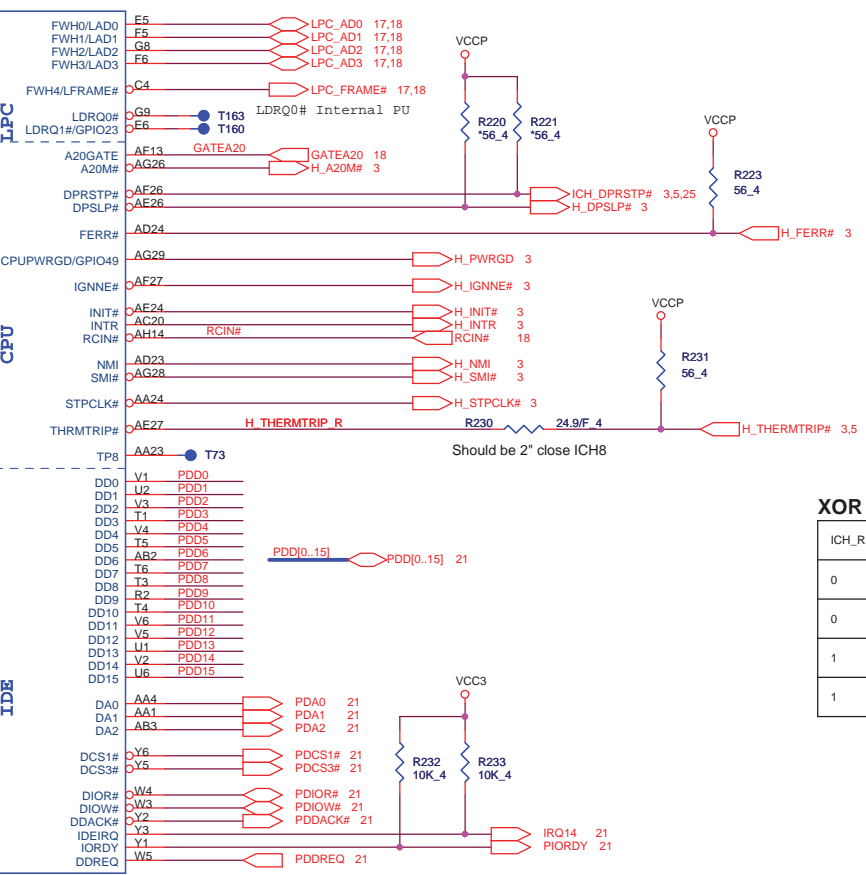
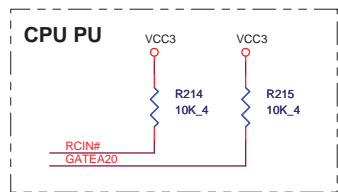
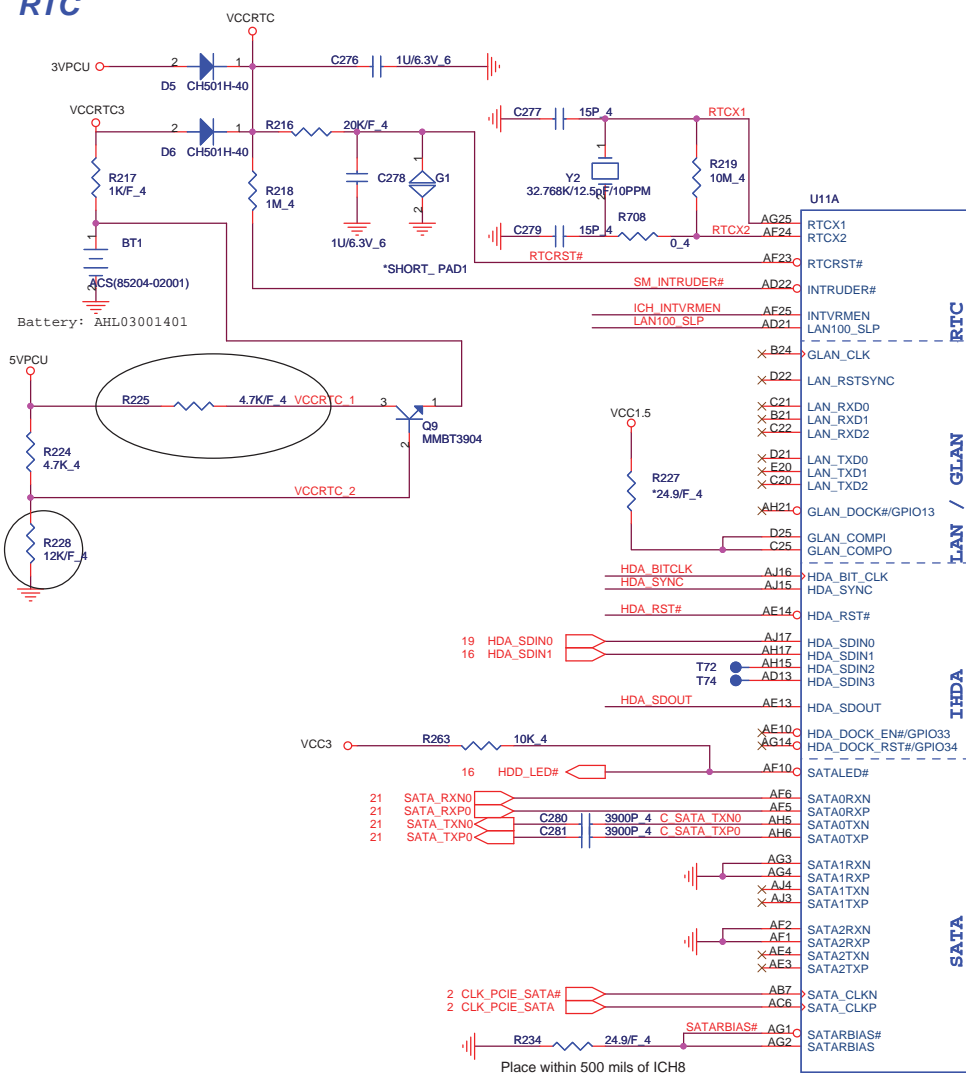
1.Level 1 Environment-related Substances should NEVER be Used.
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QUANTA COMPUTER

Title: **DDRII**

Size: Document Number: **GD1A Main Board** Rev: **2A**

Date: **Monday, July 23, 2007** Sheet: **11** of **35**



XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

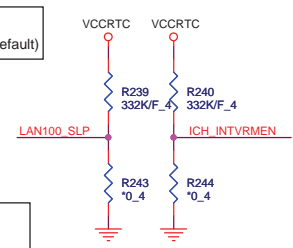
ICH8 strap

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

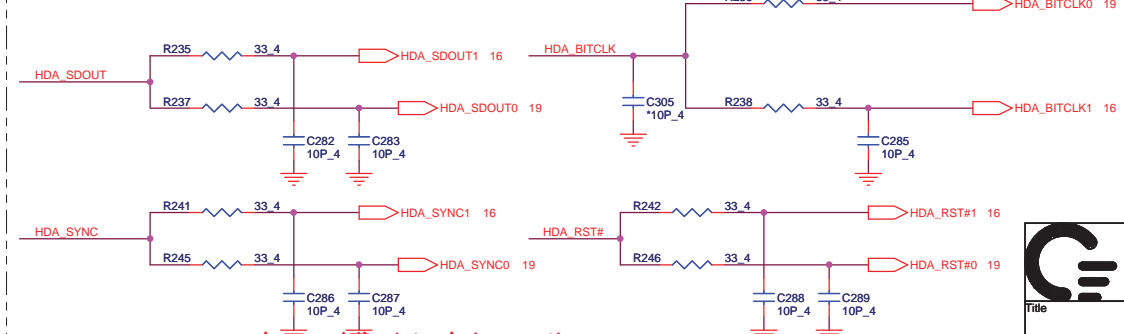
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

ICH_INTVRMEN	Low = Disable High = Enable(Default)
--------------	---

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)



HD Audio to Codec and Modem



<http://hobi-elektronika.net>

QUANTA COMPUTER

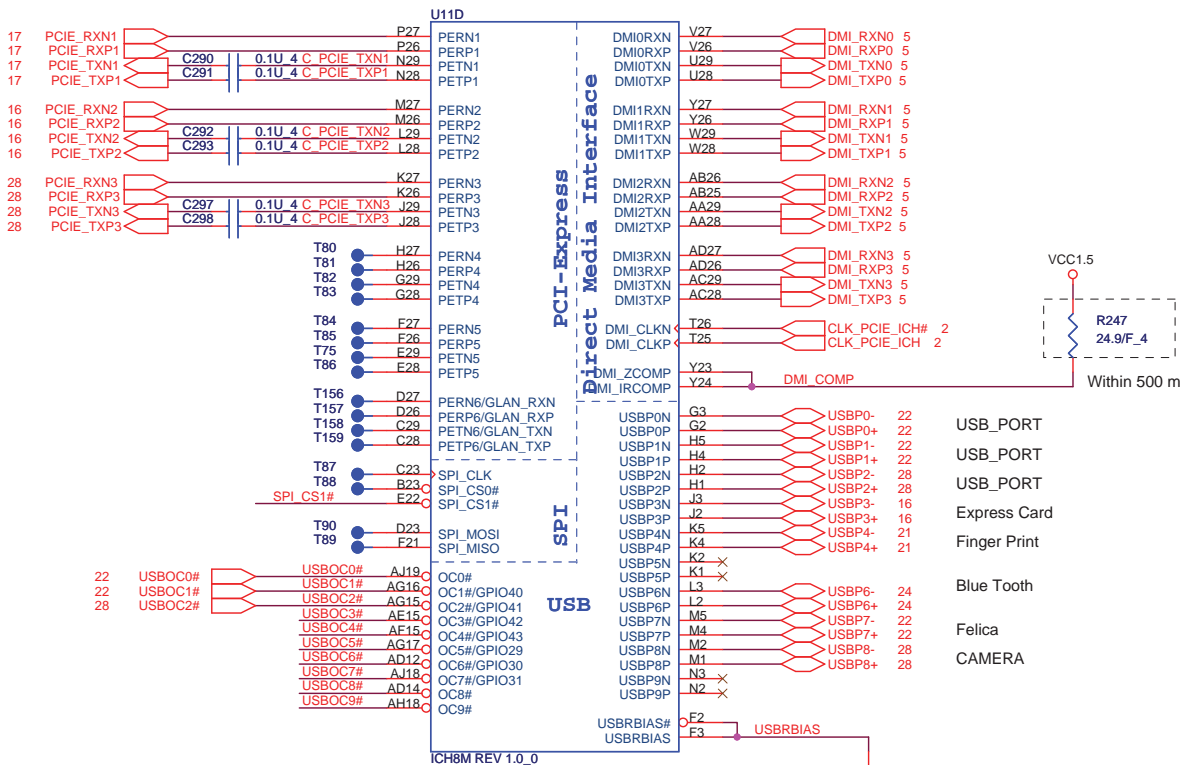
Title: ICH8-M HOST 1 of 4

Size	Document Number	Rev
	GD1A Main Board	3A

Date: Monday, July 23, 2007 Sheet 12 of 35

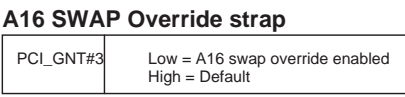
1.Level 1 Environment-related Substances Should NEVER be Used.
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WireLess Lan
Express card
10/100 Lan



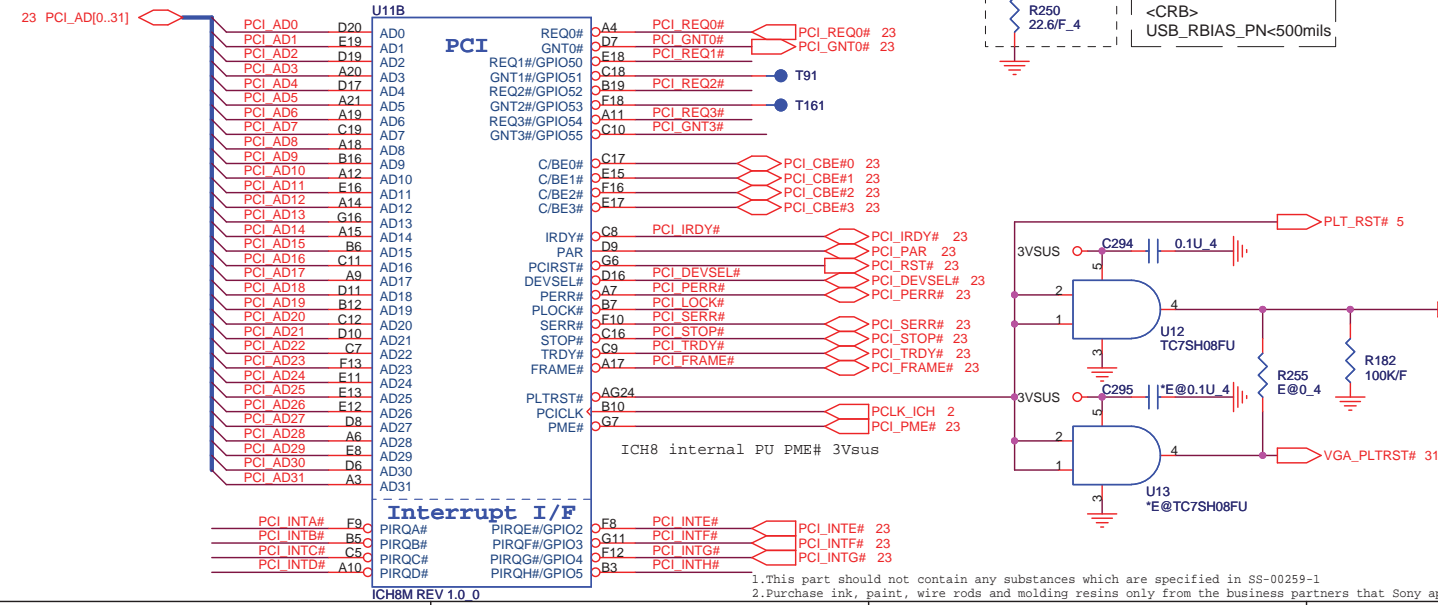
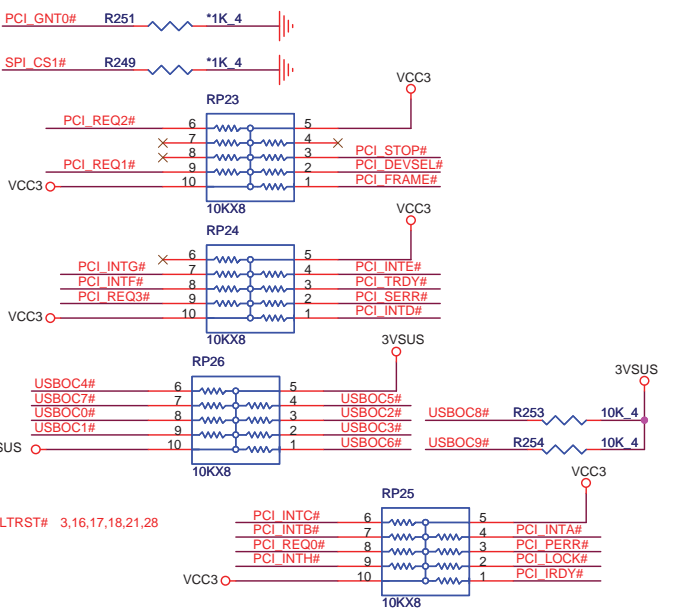
PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
T18402	AD23	REQ0# / GNT0#	PIRQ E/F/G



ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)



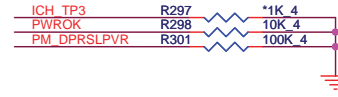
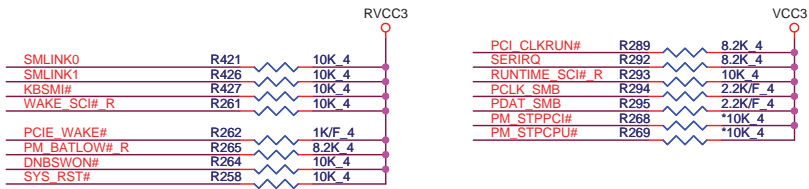
QUANTA COMPUTER

Title: **ICH8-M PCIE 2 of 4**

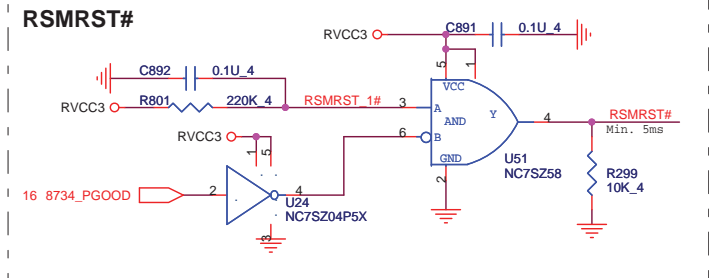
Size B Document Number: **GD1A Main Board** Rev 2A

Date: Monday, July 23, 2007 Sheet 13 of 35

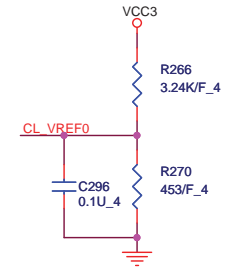
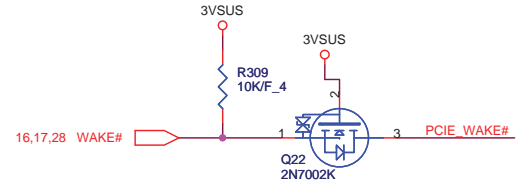
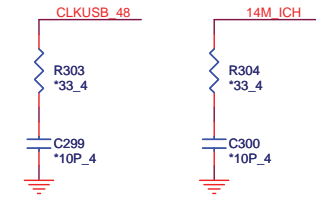
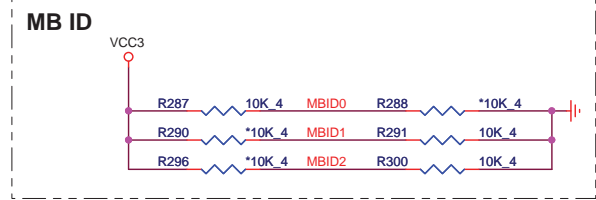
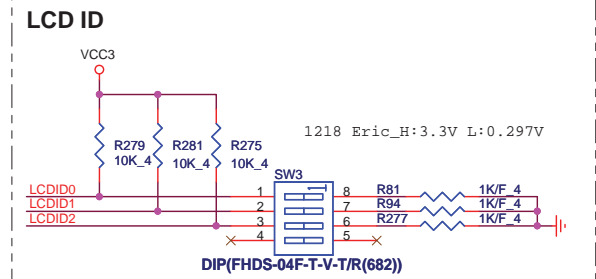
1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



RSMRST# must be after RVCC3 10 ms



LCDID	Panel Type
X001	AUO -QD14TL0206
X010	CPT -CLAA141WB02A
X011	CPT -CLAA141WB05A



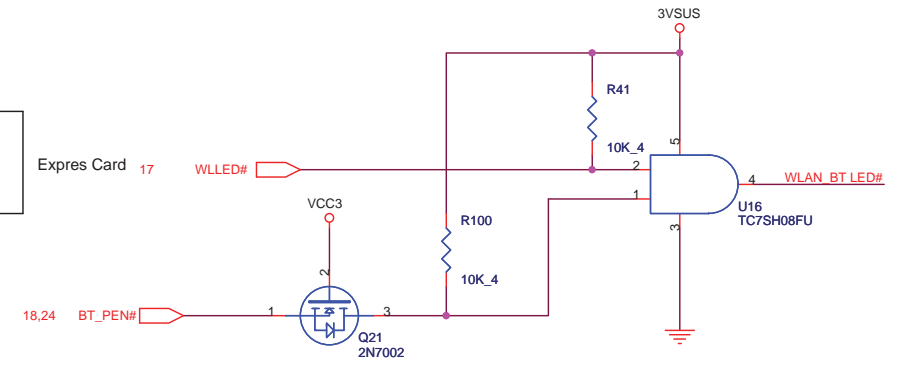
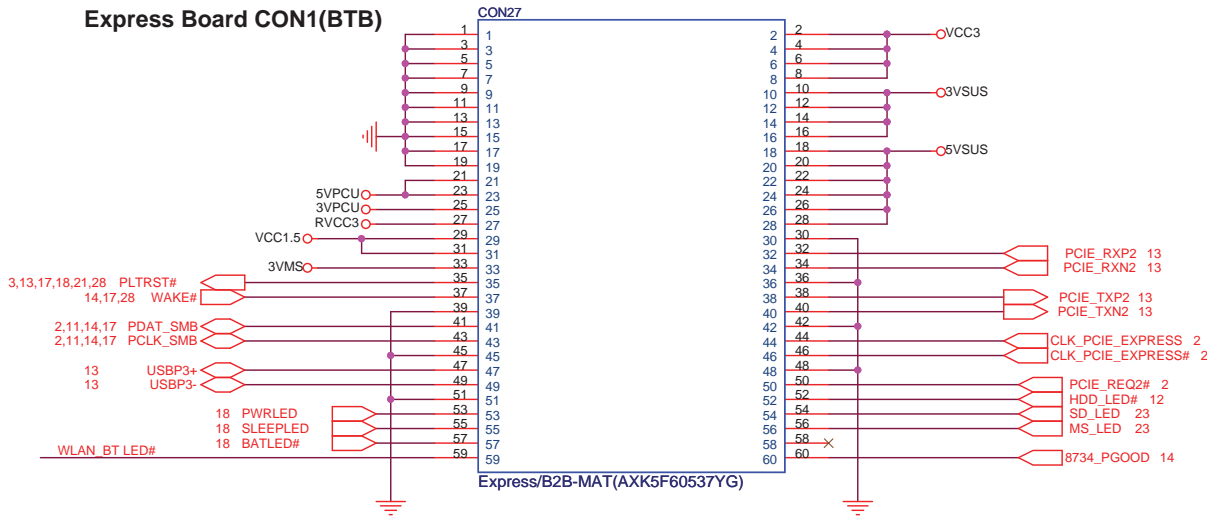
1.Level 1 Environment-related Substances Should NEVER be Used.
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QUANTA COMPUTER

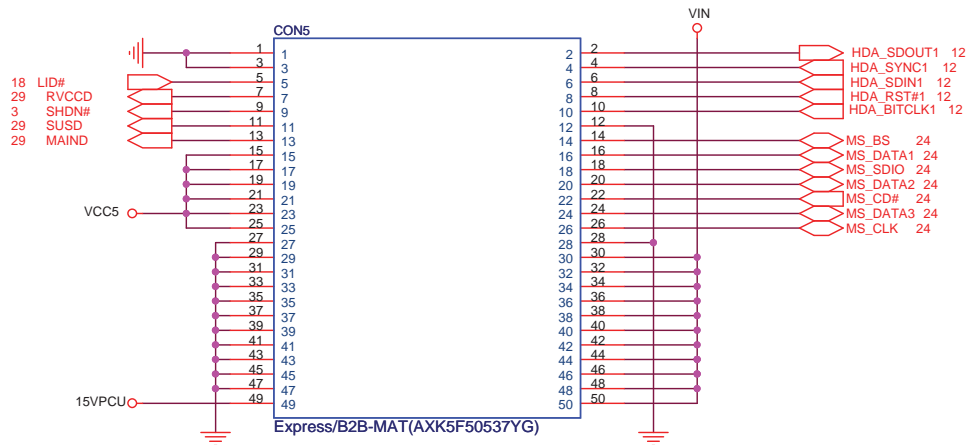
Title: ICH8-M GPIO 3 of 4

Size B	Document Number	Rev 2A
GD1A Main Board		
Date: Monday, July 23, 2007	Sheet 14	of 35

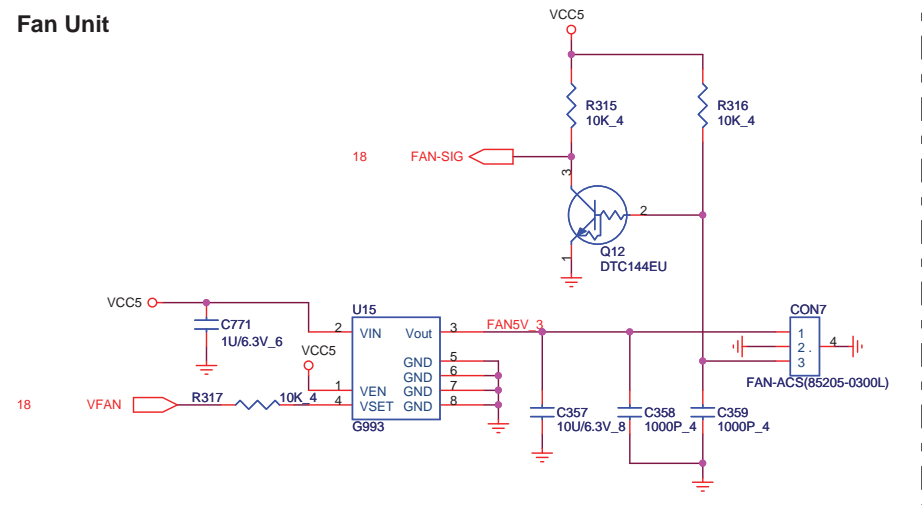
Express Board CON1(BTB)



Express Board CON2(BTB)



Fan Unit

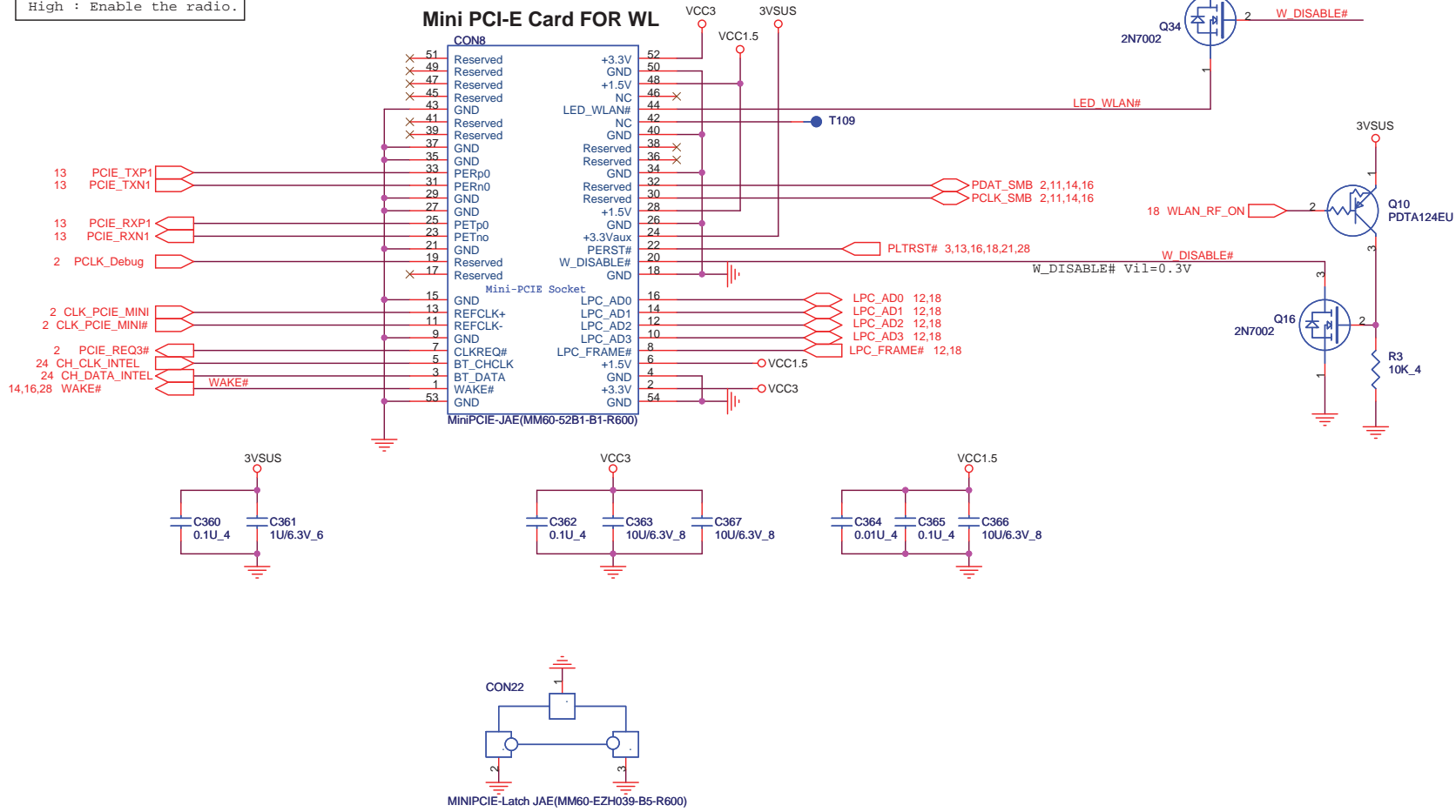


Title			Express Card		
Size	Document Number				Rev
B	GD1A Main Board				2A
Date:	Monday, July 23, 2007	Sheet	16	of	35

1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

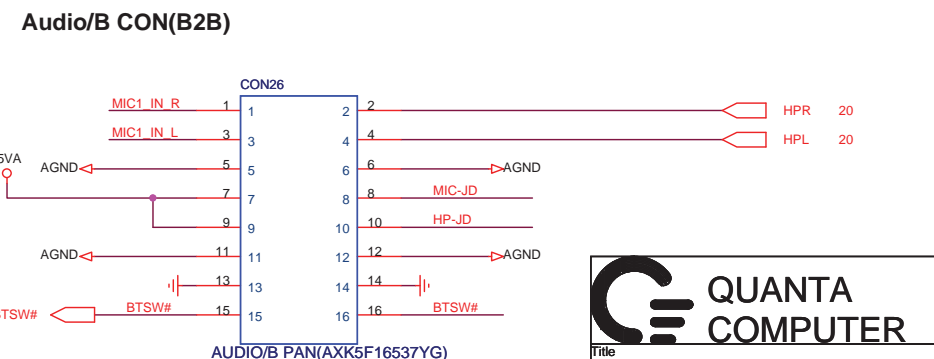
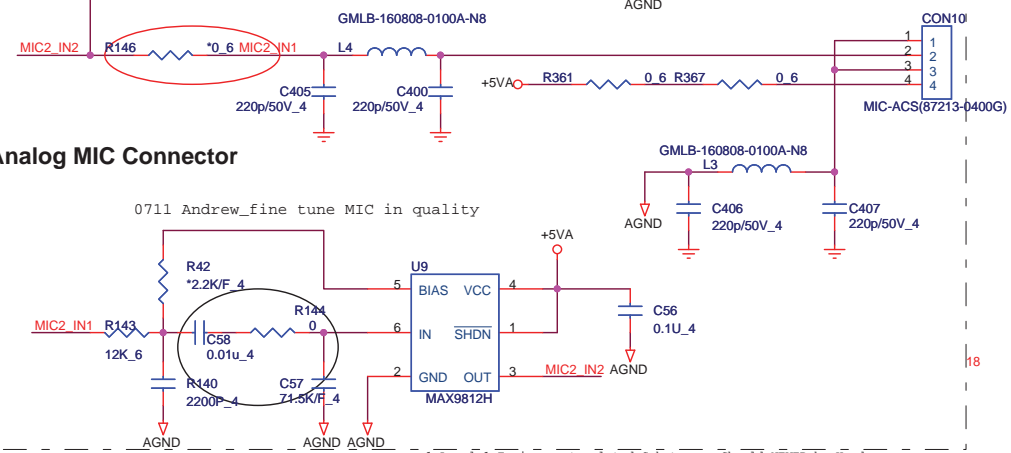
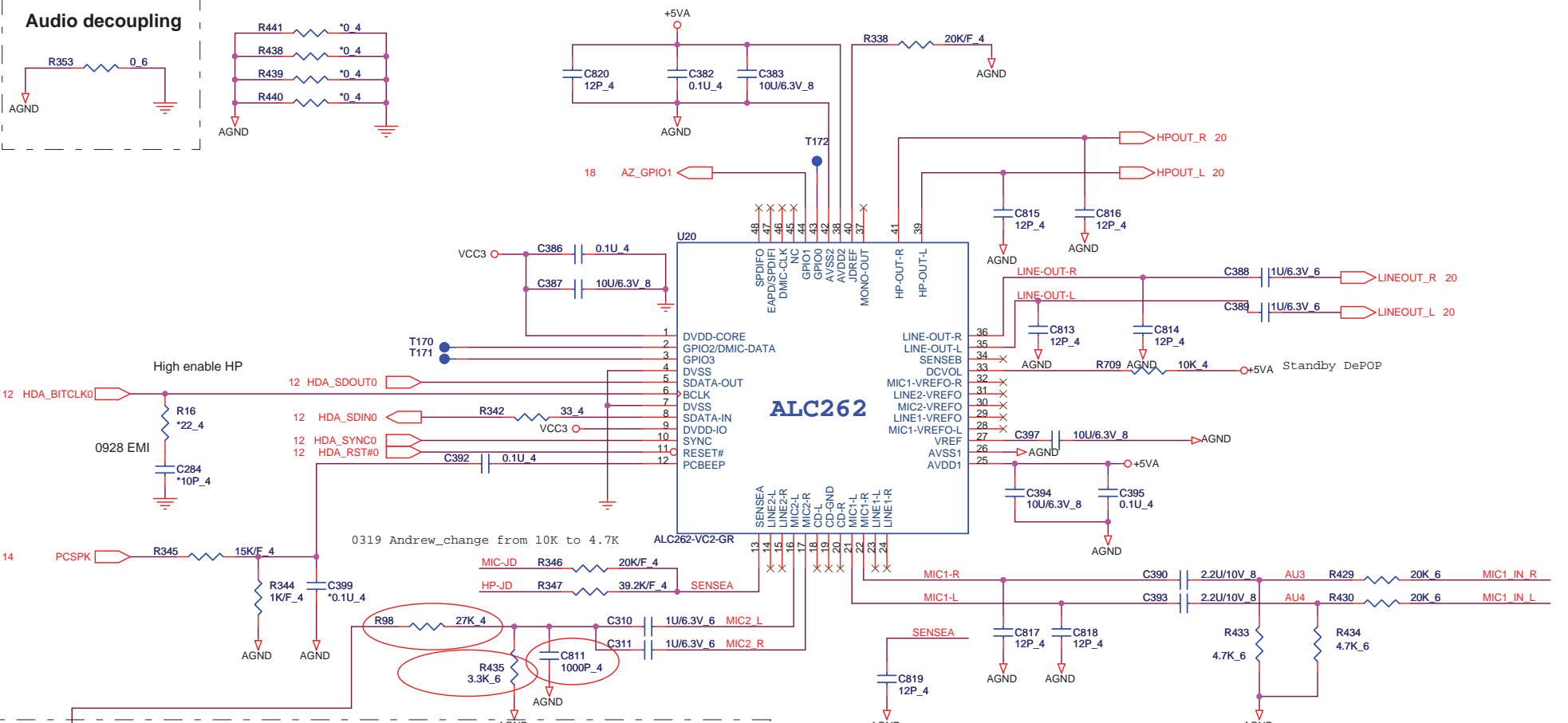
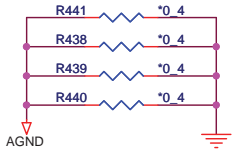
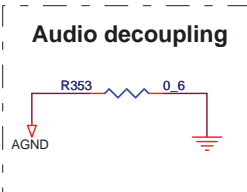
LED_GP :LED WLEN LINK
 Output Current : 7mA
 Blink rate : 1 flash per every 3 sec.

WLSW:
 Low : disable the radio.
 High : Enable the radio.



1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER		
Title MINIPCI-E / MDC		
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007 Sheet 17 of 35		

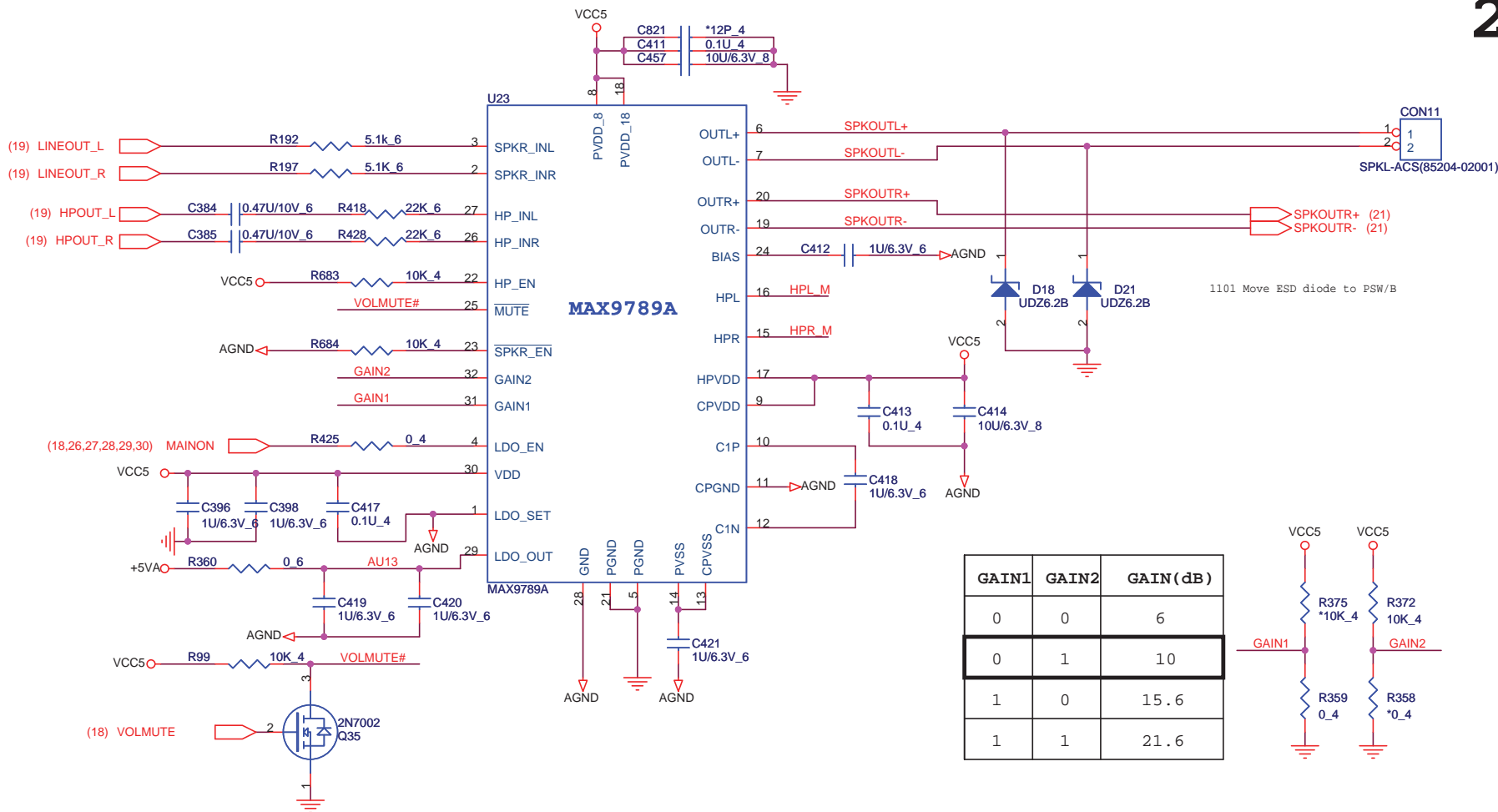


1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

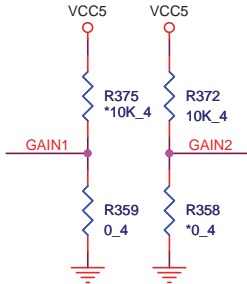
QUANTA COMPUTER

Title: **Audio ALC268**

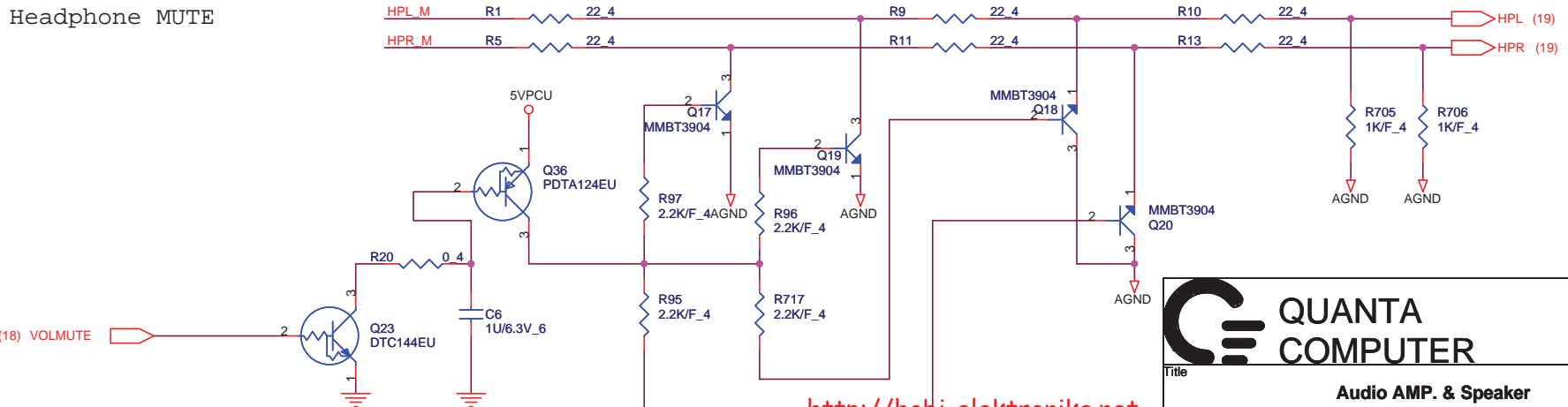
Size: Custom	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet: 19 of 35	



GAIN1	GAIN2	GAIN (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



Headphone MUTE



1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

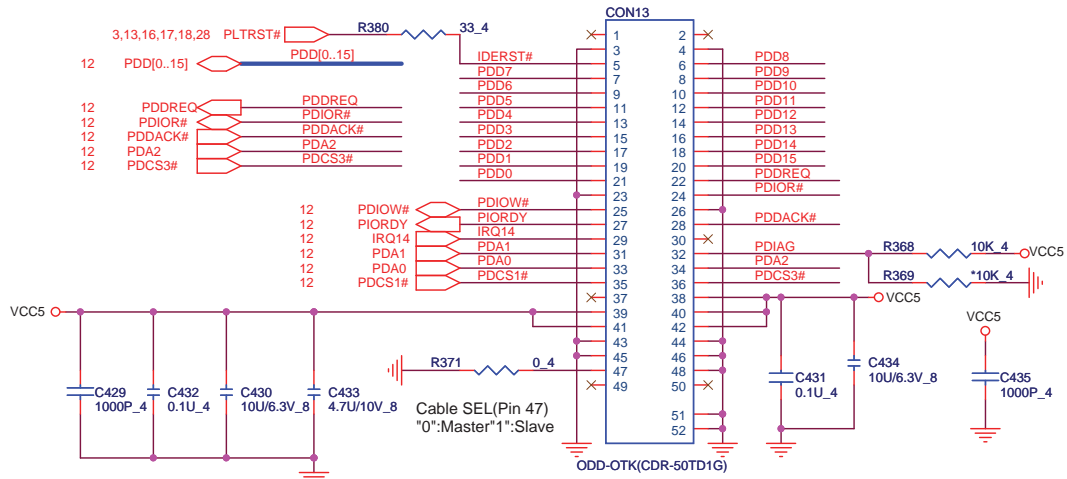
<http://hobi-elektronika.net>

**QUANTA
COMPUTER**

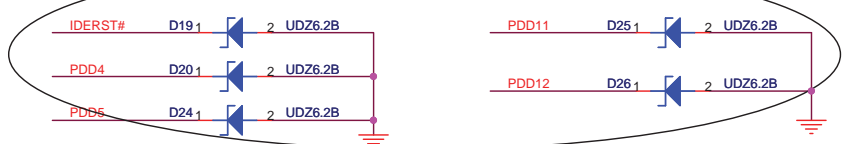
Title: **Audio AMP. & Speaker**

Size: Custom	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007		Sheet 20 of 35

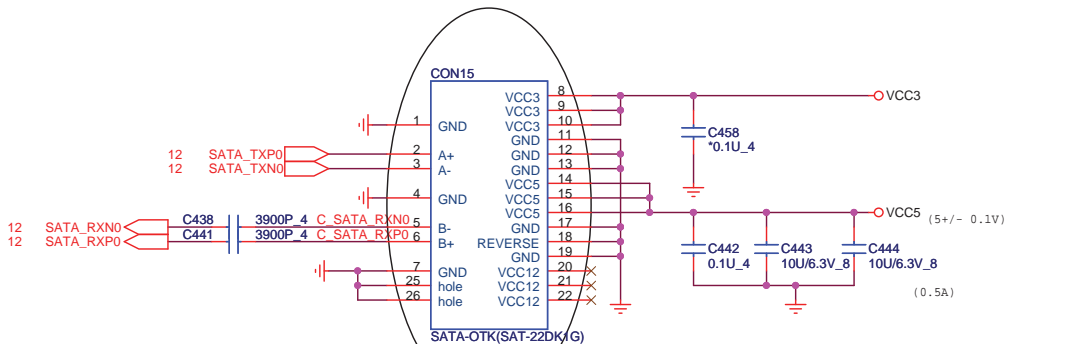
ODD CONNECTOR



0618 Eric_add ESD diode for ODD ESD issue

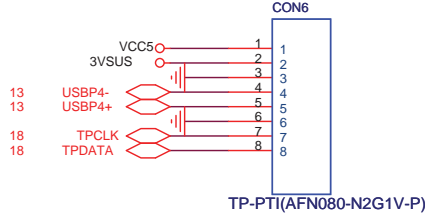


HDD CONNECTOR

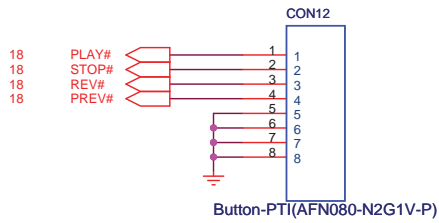


0611 Eric_modify HDD FP for SMT shift issue

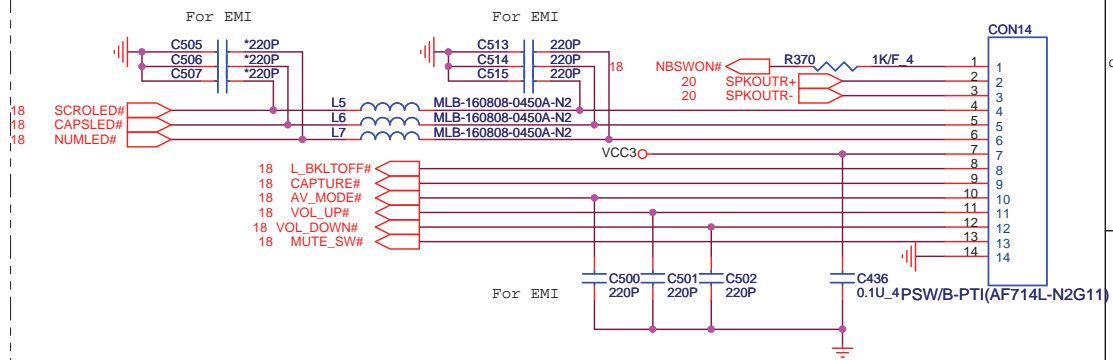
TouchPAD Board CON(FPC)



Button CON(FFC)



PSW Board CON(Inverse FFC)



1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

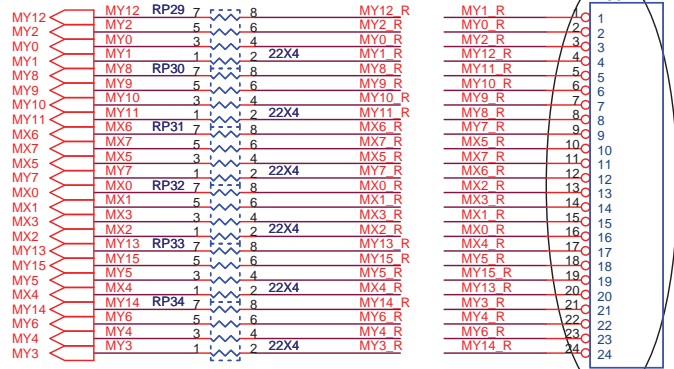
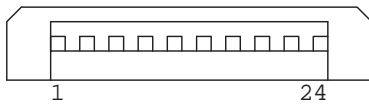
**QUANTA
COMPUTER**

Title: **HDD/ODD/PSW/BUT/TP**

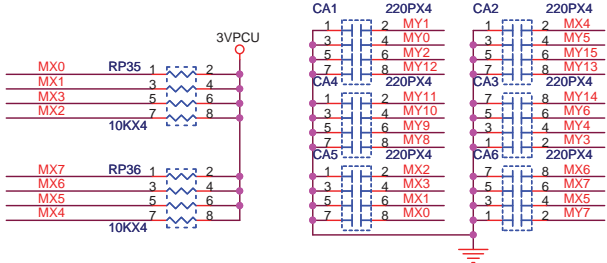
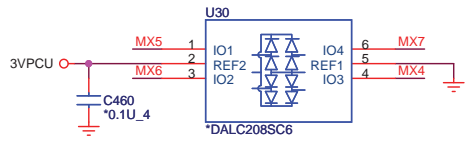
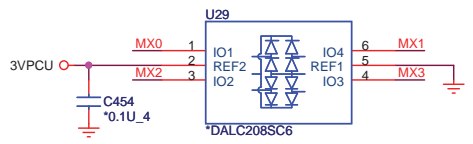
Size: B Document Number: **GD1A Main Board** Rev: 3A

Date: Monday, July 23, 2007 Sheet: 21 of 35

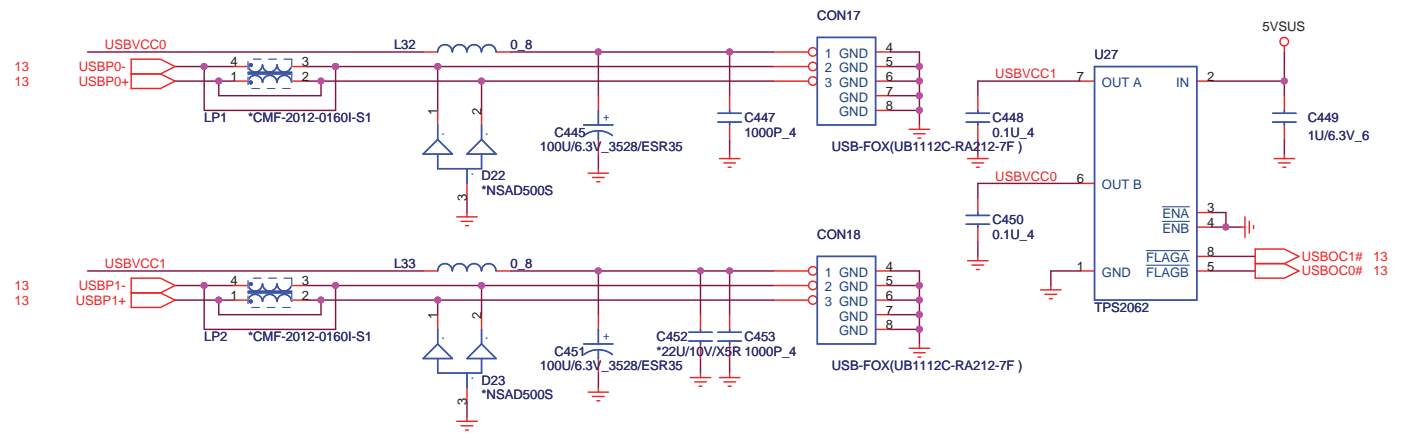
Keyboard



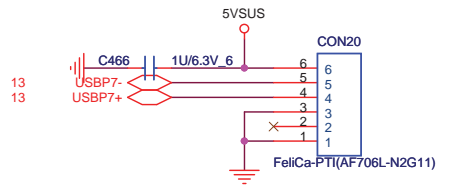
0711 Eric_modify FP for 2nd IR



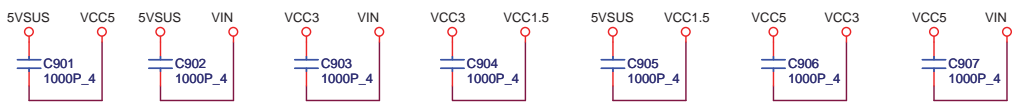
USB Port x 2



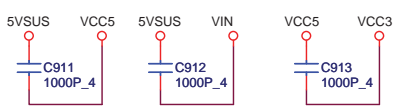
Felica



ODD

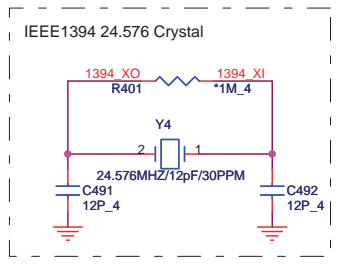
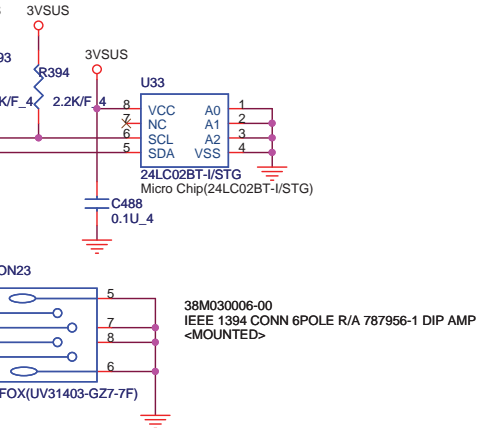
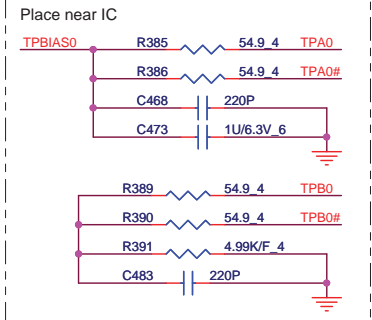
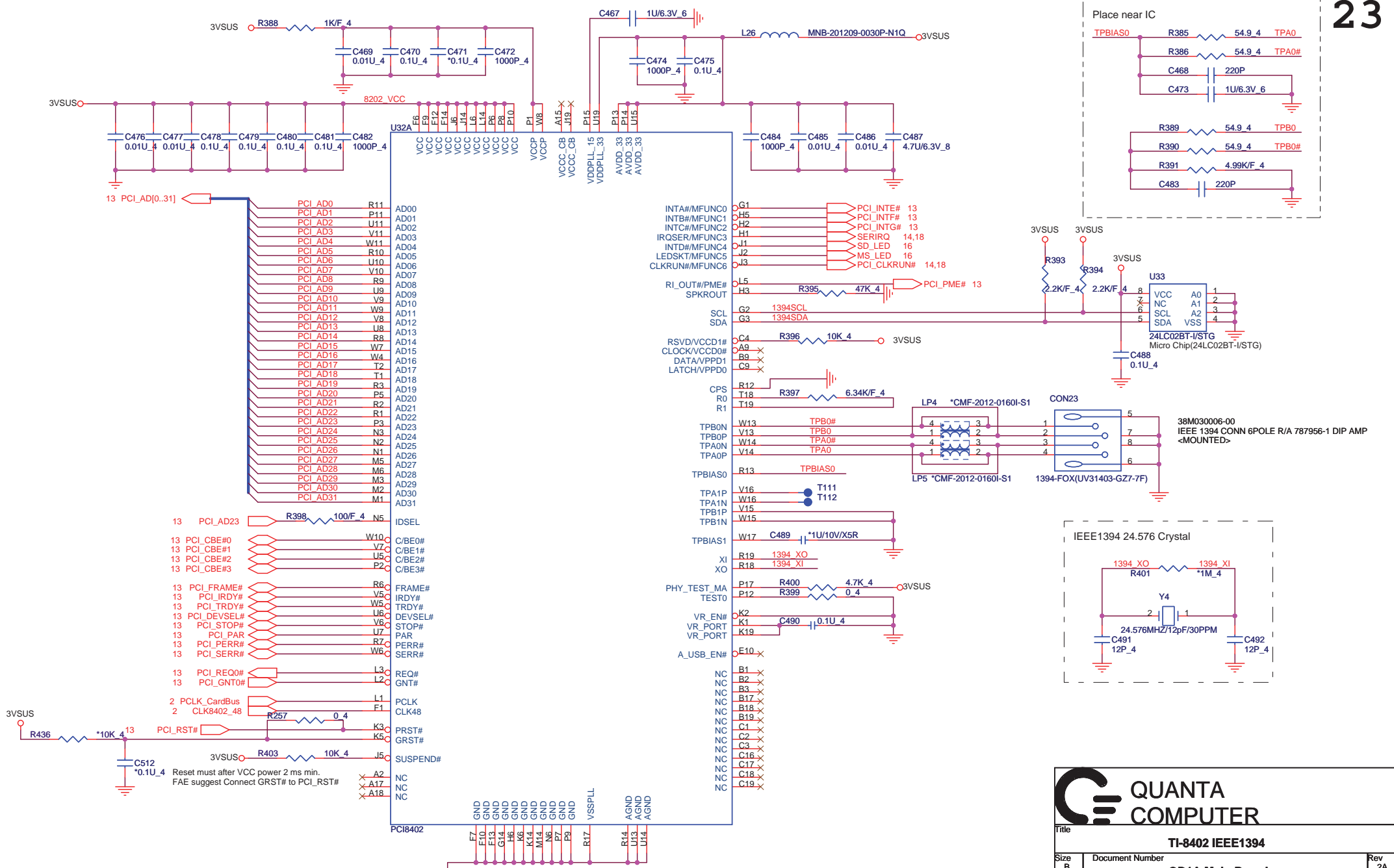


PCI Bus



1.Level 1 Environment-related Substances Should NEVER be Used. 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER logo and title block containing: Title: K/B ,USB Device; Document Number: GD1A Main Board; Rev: 3A; Date: Monday, July 23, 2007; Sheet: 22 of 35.



QUANTA COMPUTER

Title: **TI-8402 IEEE1394**

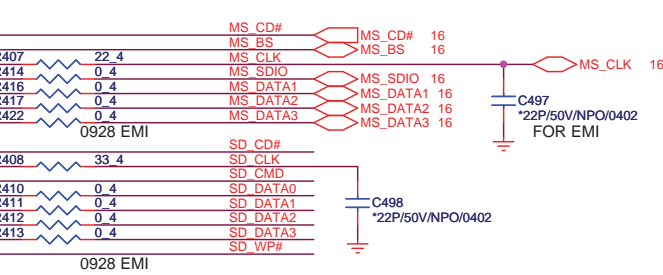
Size B Document Number: **GD1A Main Board** Rev 2A

Date: Monday, July 23, 2007 Sheet 23 of 35

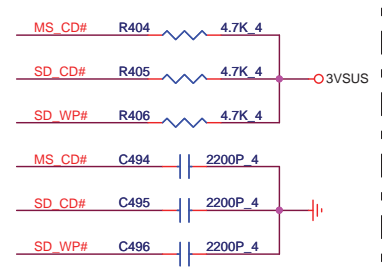
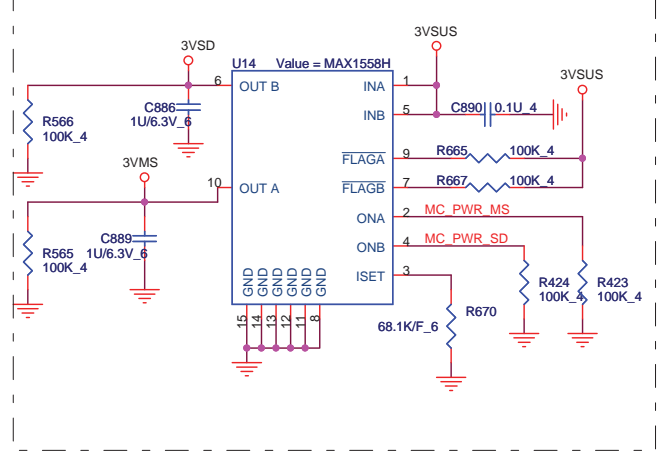
1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

P19	D3/CAD0	MS_CD#	A8	MS_CD#	MS_CD#	16
N18	D4/CAD1	MS_BS/SD_CMD/xD_WE#	E8	MS_BS	MS_BS	16
N17	D11/CAD2	MS_CLK/SD_CLK/xD_ELPW#	A7	MS_CLK	MS_CLK	16
M15	D5/CAD3	MS_SDIO/SD_DAT0/xD_D0	B7	R414	0.4	
N19	D12/CAD4	MS_DATA1/SD_DAT1/xD_D1	C7	R416	0.4	
M18	D6/CAD5	MS_DATA2/SD_DAT2/xD_D2	A6	R417	0.4	
M17	D13/CAD6	MS_DATA3/SD_DAT3/xD_D3	B6	R422	0.4	
L19	D7/CAD7					
L18	D15/CAD8	SD_CD#	E9	SD_CD#	SD_CD#	
L15	A10/CAD9	SD_CLK/xD_RE#	A4	R408	33.4	
K18	CE2#/CAD10	SD_CMD/xD_ALE#	C5			
K17	OE#/CAD11	SD_DAT0/xD_D4	C6	R410	0.4	
K15	A11/CAD12	SD_DAT1/xD_D5	A5	R411	0.4	
J18	IORD#/CAD13	SD_DAT2/xD_D6	B5	R412	0.4	
J15	A9/CAD14	SD_DAT3/xD_D7	E6	R413	0.4	
J17	IOWR#/CAD15	SD_WP#	E7			
H19	A17/CAD16	SM_CD#	B8			
F15	A24/CAD17	xD_CLE	B4			
E17	A7/CAD18					
D19	A25/CAD19					
A16	A6/CAD20	XD_CD#/xD_PHYS_WP#	A3			
F14	A5/CAD21					
B15	A4/CAD22	SC_CD#	E3			
B14	A3/CAD23	SC_CLK	E2			
A14	A2/CAD24	SC_DATA	E1			
C13	A1/CAD25	SC_FCB	E0			
B13	A0/CAD26	SC_OC#	G5			
C11	D0/CAD27	SC_PWR_CTRL	D1			
F11	D8/CAD28	SC_RFU	F5			
A10	D1/CAD29	SC_RST	G6			
C10	D9/CAD30	SC_VCC_5V				
D10	D10/CAD31					
L17	CE1#/CCBE0#	MC_PWR_CTRL_0	C8	MC_PWR_MS		
H18	A8/CCBE1#	MC_PWR_CTRL_1	F8	MC_PWR_SD		
E18	A12/CCBE2#					
E13	REG#/CCBE3#					
F18	A16/CLK	MS/SD:	D2	High Active PWR CTL		
A11	WP/CLKRUN#		D3			
C15	RESET/CRST#		D17			
H14	A13/CPAR		D18			
E19	A23/CFRAME#		E5			
F17	A15/CRDY#		N14			
G15	A22/CTRDY#		P18			
G18	A20/CSTOP#		T3			
F19	A21/CDEVSEL#		T17			
C14	CREQ/INPACK#		U1			
G17	WE#/CGNT#		U2			
G19	A14/CPERR#		U3			
C12	WAIT#/CSERR#		U12			
E12	READY/CINT#		U16			
A12	BVD1/STSCHG#		U17			
B12	BVD2/CAUDIO		U18			
H15	A19/CBLOCK#		V1			
			V2			
			V3			
			V4			
N15	CD1#/CCD1#		V12			
B11	CD2#/CCD2#		V17			
A13	VS1#/CVS1		V18			
B16	VS2#/CVS2		V19			
B10	D2		W2			
M19	D14		W3			
H17	A18		W12			
			W18			

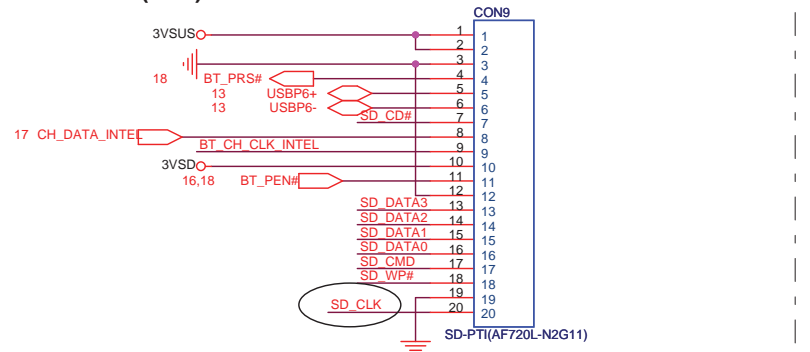
PCI8402



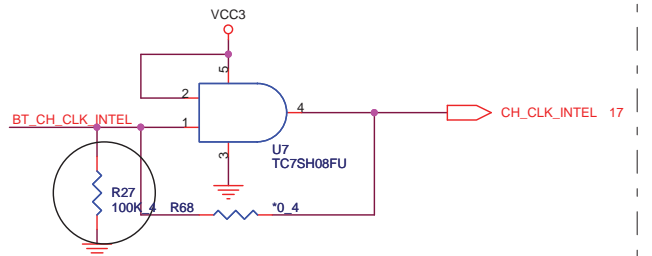
SD & MS Power Switch



SD CON(FPC)



0711 Eric_Delete R432, fixture of KB will damage it

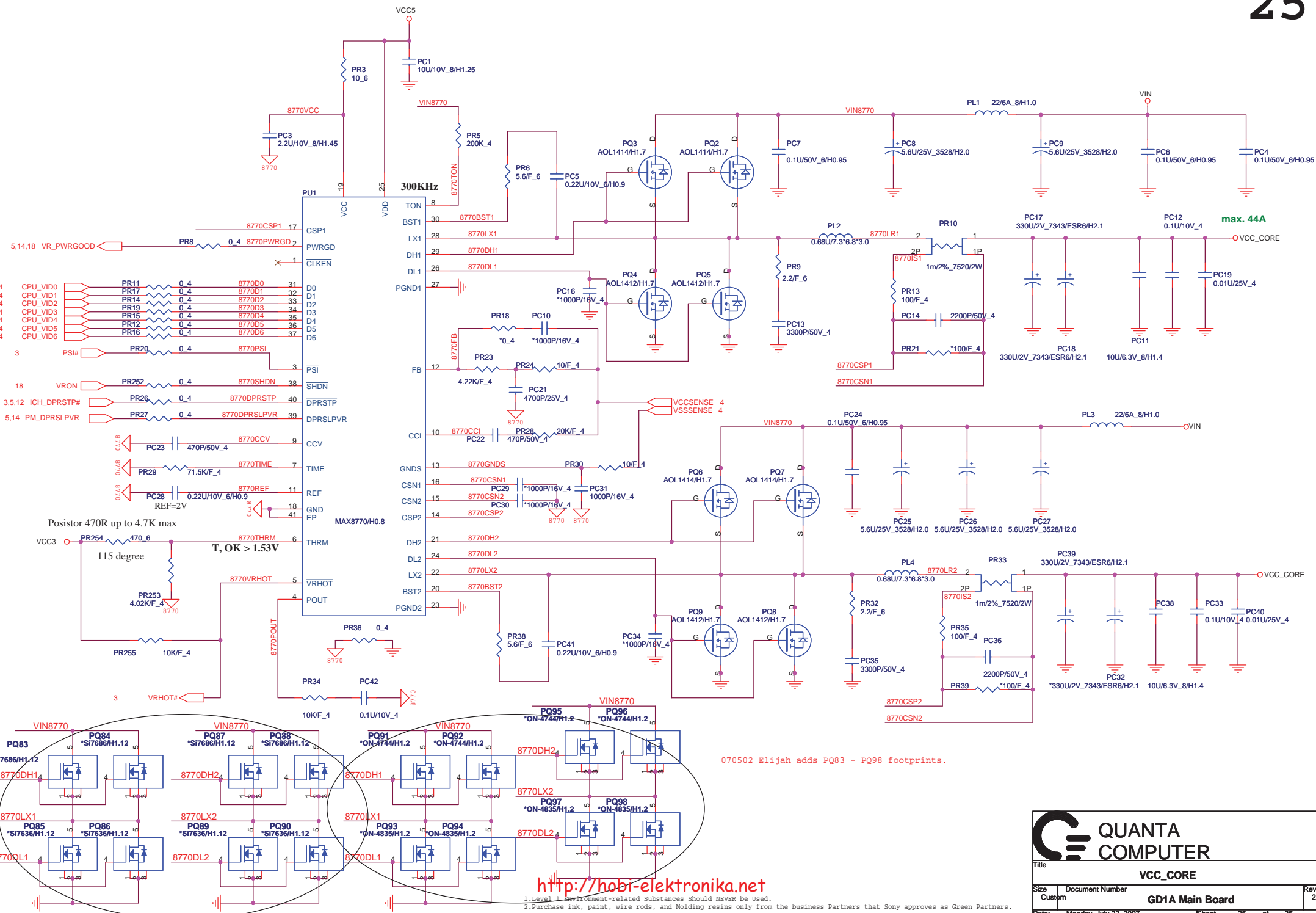


0611 Eric_install R27 for WL disconnecting issue



Title			TI-8402 MS & SD
Size	Document Number	Rev	
B		3A	
Date: Monday, July 23, 2007			Sheet 24 of 35

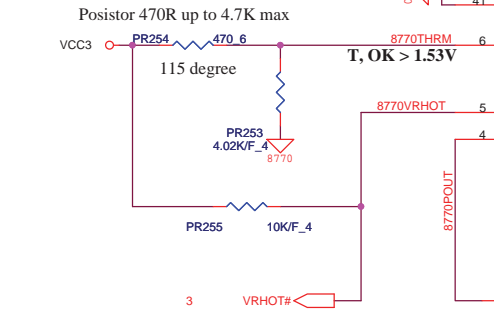
1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



- 4 CPU_VID0 PR11 0.4 8770D0 31
- 4 CPU_VID1 PR17 0.4 8770D1 32
- 4 CPU_VID2 PR14 0.4 8770D2 33
- 4 CPU_VID3 PR19 0.4 8770D3 34
- 4 CPU_VID4 PR15 0.4 8770D4 35
- 4 CPU_VID5 PR12 0.4 8770D5 36
- 4 CPU_VID6 PR16 0.4 8770D6 37

- 3 PSIF# PR20 0.4 8770PSI 3
- 18 VRON PR252 0.4 8770SHDN 38
- 3,5,12 ICH_DPRSTP# PR26 0.4 8770DPRSTP 40
- 5,14 PM_DPRSLPVR PR27 0.4 8770DPRSLPVR 39

- 0.4,8 PC23 470P/50V_4 8770CCV 9
- 0.4,8 PR29 71.5K/F_4 8770TIME 7
- 0.4,8 PC28 0.22U/10V_6/H0.9 8770REF 11
- 0.4,8 REF=2V 18
- 0.4,8 GND EP 41



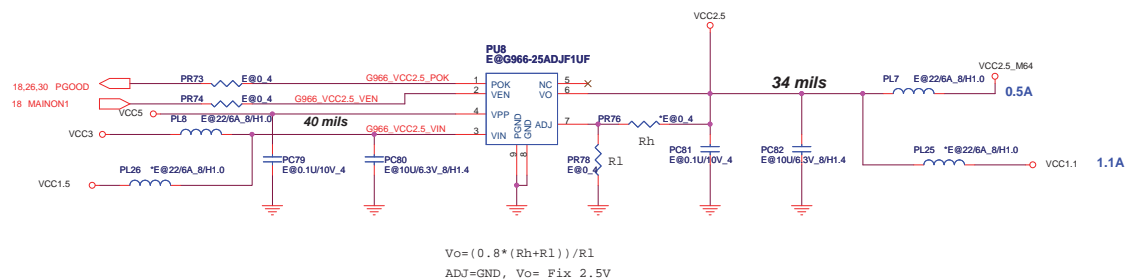
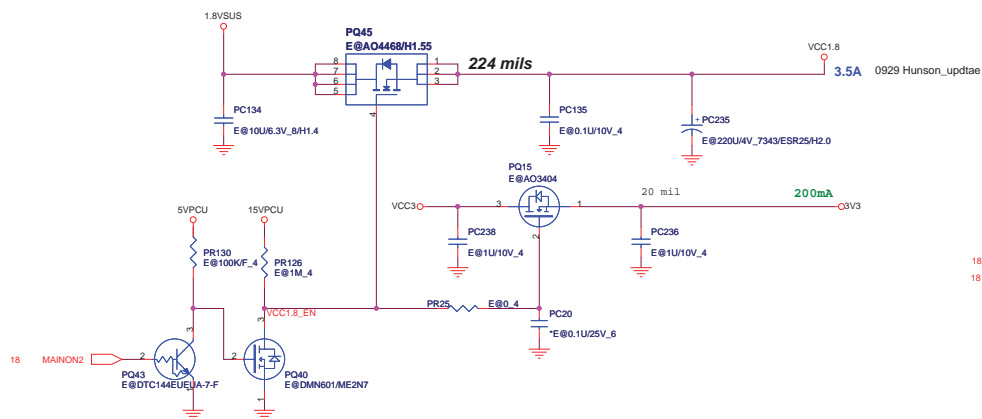
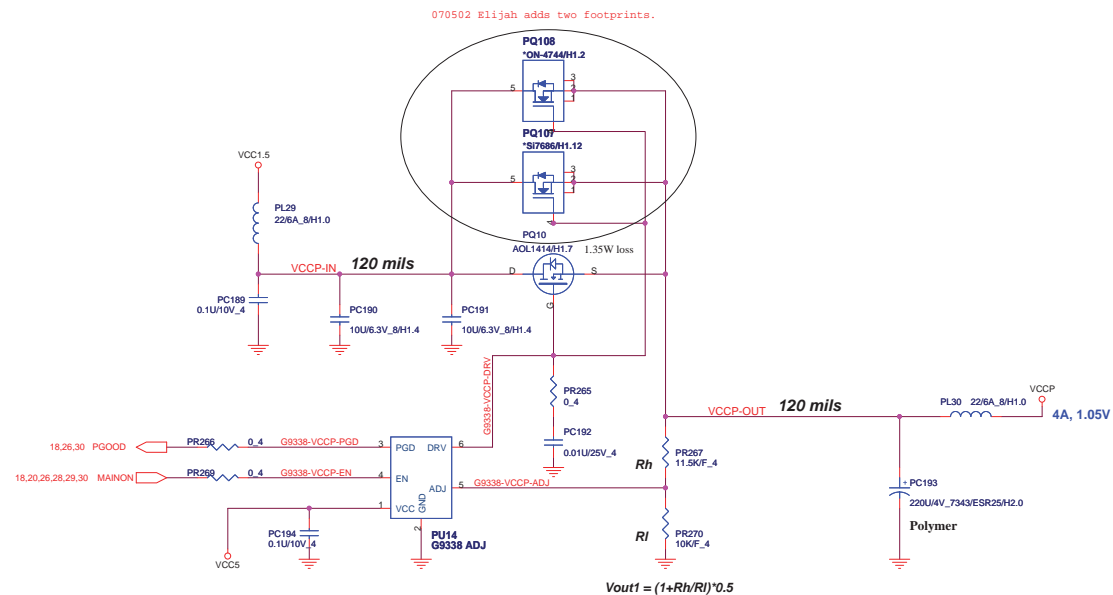
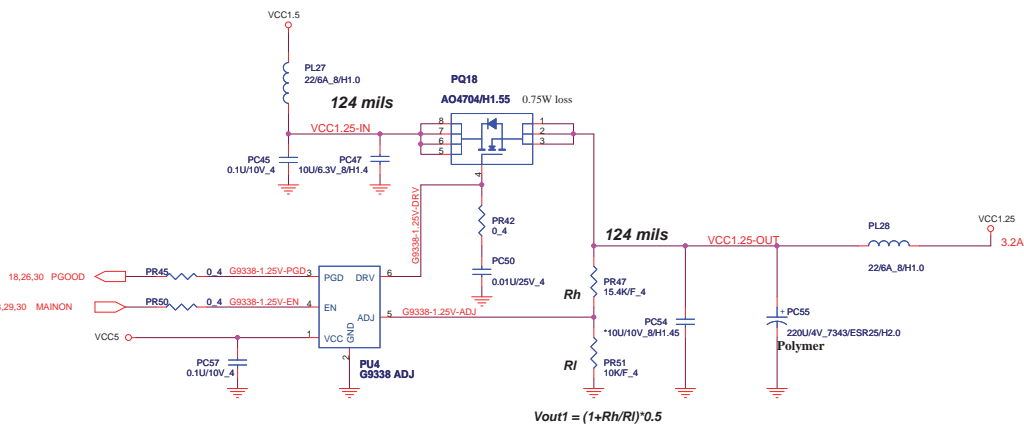
<http://hobi-elektronika.net>

1. Level 1 environment-related Substances should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Welding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

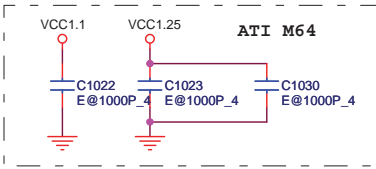
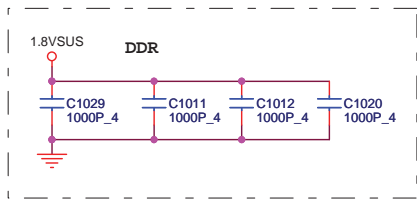
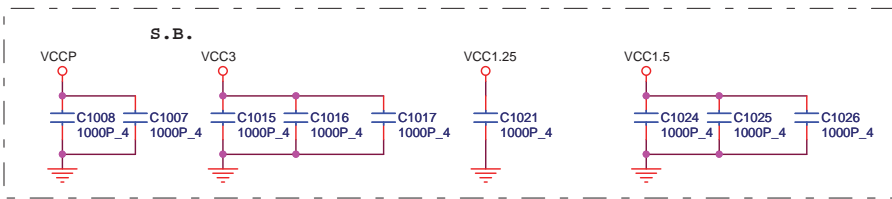
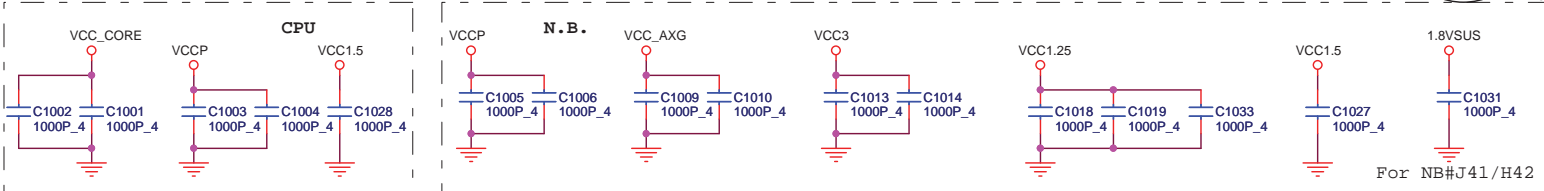
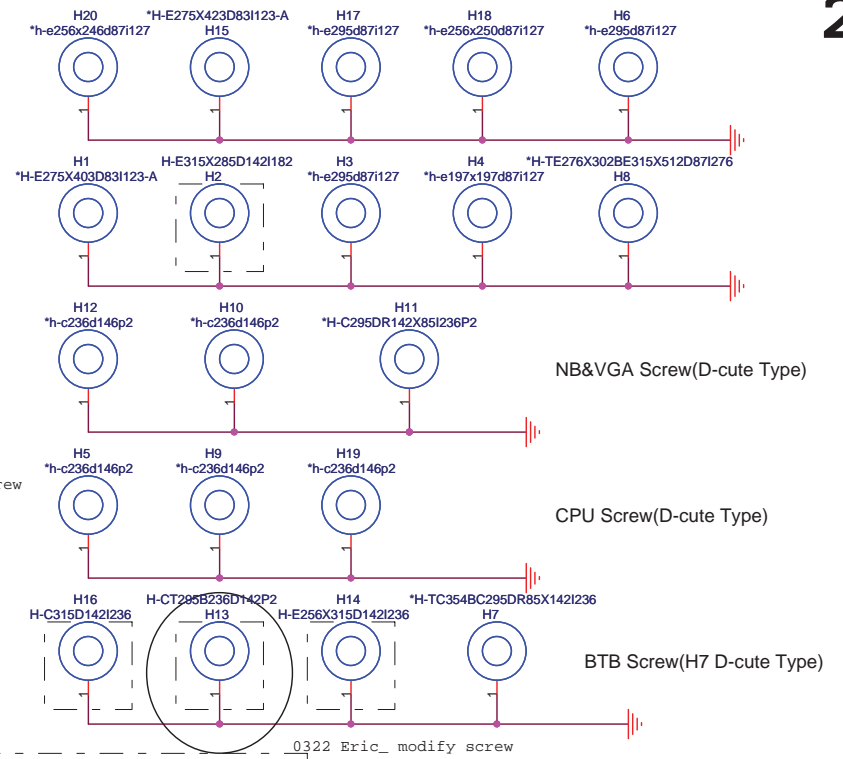
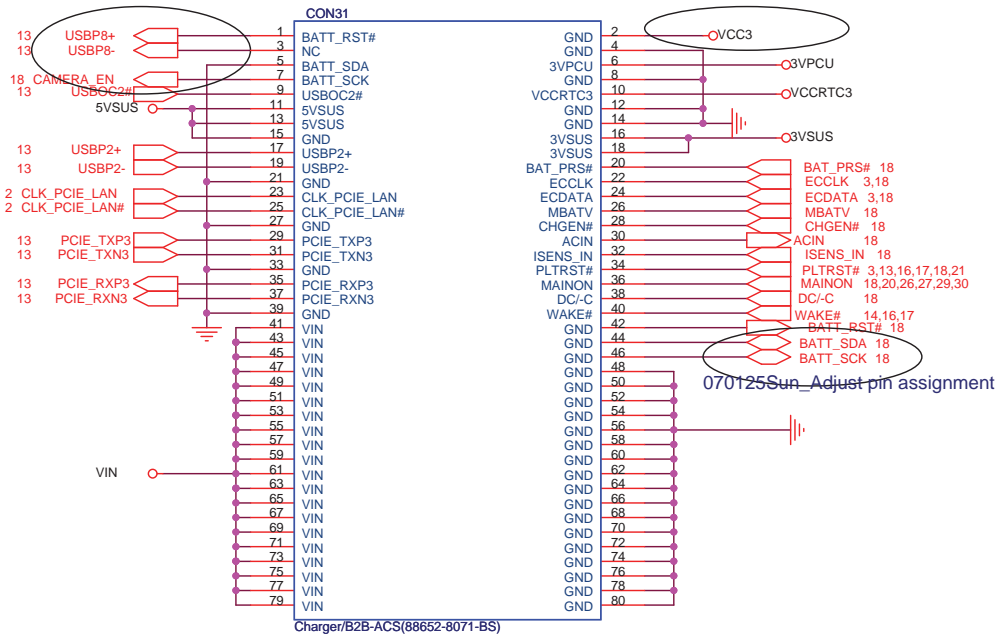
Title: **VCC_CORE**

Size: Custom	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet: 25 of 35	



070125Sun_Adjust pin assignment

070125Sun_Adjust pin assignment



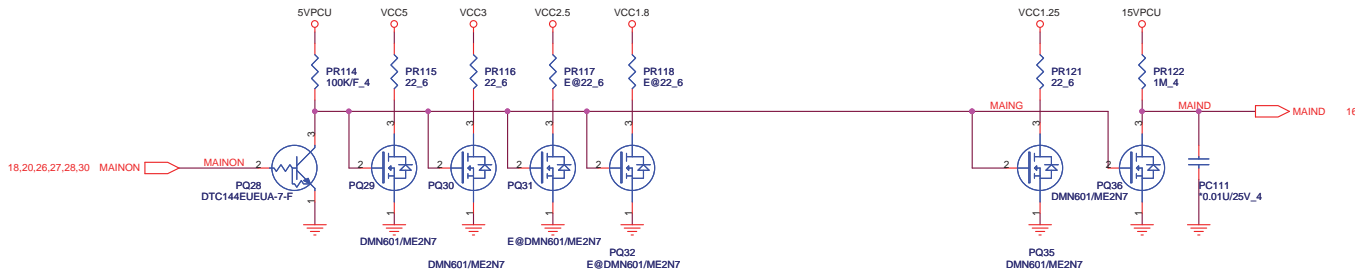
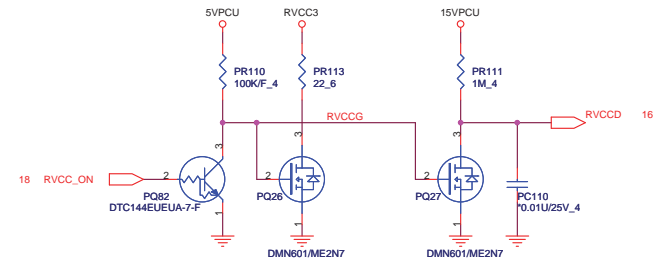
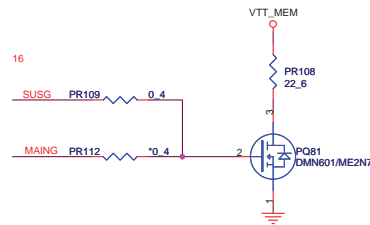
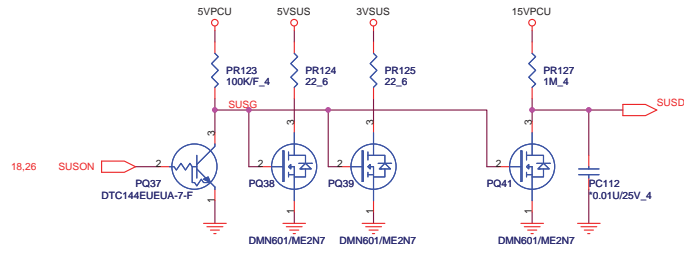
QUANTA COMPUTER

Title: **Power Charger & LAN CON**

Size B	Document Number	Rev 2A
GD1A Main Board		

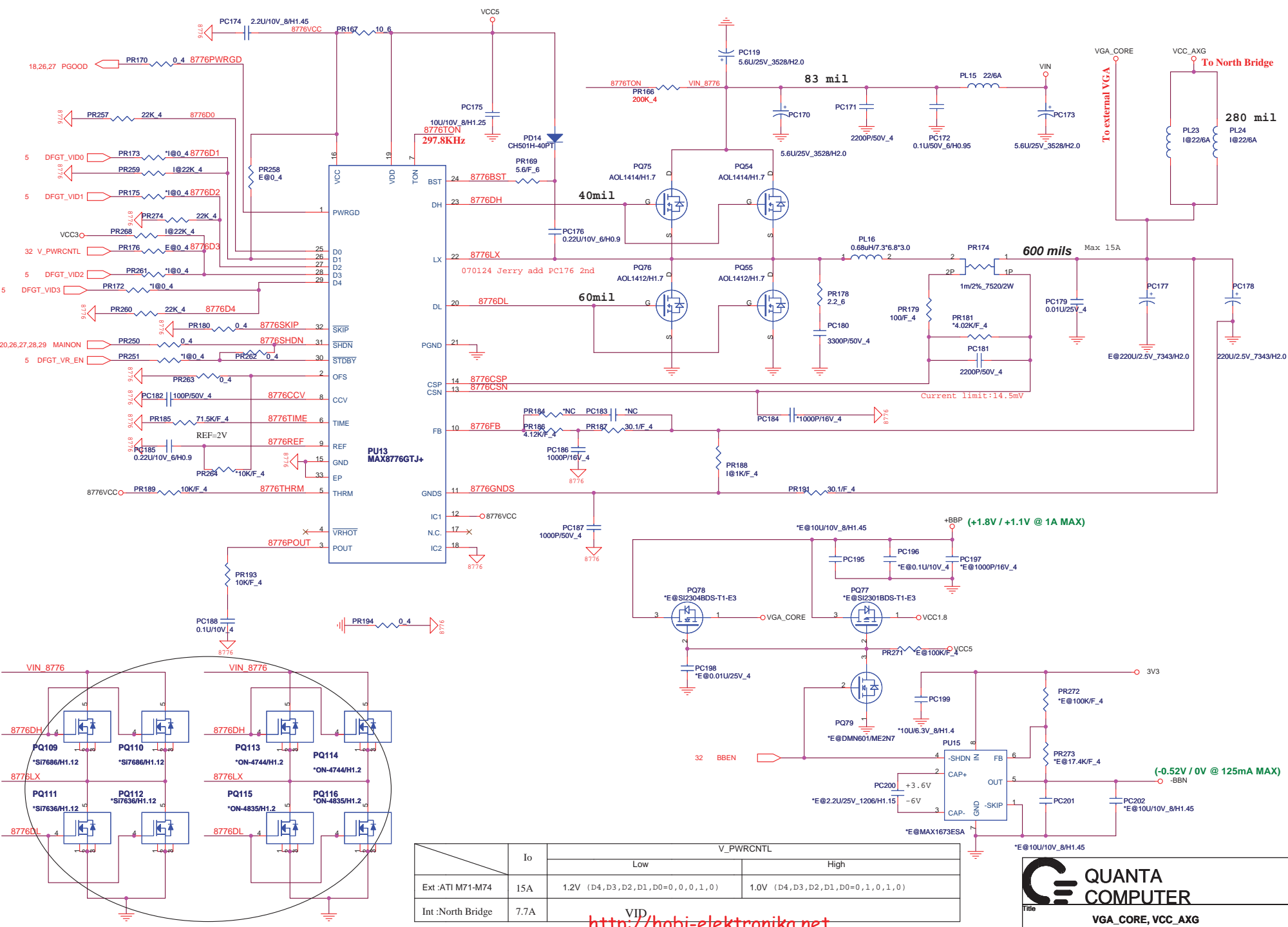
Date: Monday, July 23, 2007 Sheet 28 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



1.Level 1 Environment-related Substances should NEVER be Used.
 2.Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER	
Title Discharge, SUSG, RVCCD, MAIND	
Size Custom	Document Number GD1A Main Board
Date: Monday, July 23, 2007	Rev 2A
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070502 Elijah adds PQ109 - PQ116 footprints.

	I _o	V_PWRCNTL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4,D3,D2,D1,D0=0,0,0,1,0)	1.0V (D4,D3,D2,D1,D0=0,1,0,1,0)
Int :North Bridge	7.7A		

<http://hobi-elektronika.net>

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QUANTA COMPUTER

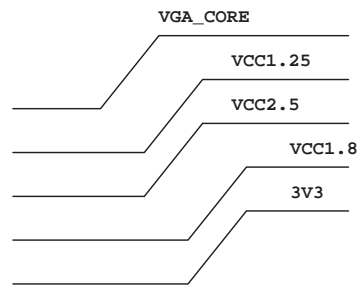
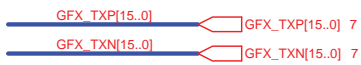
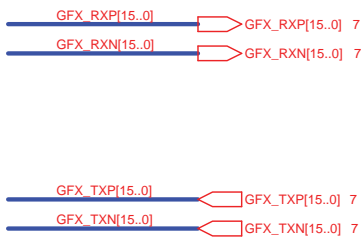
Title: **VGA_CORE, VCC_AXG**

Size: Document Number: **GD1A Main Board** Rev 2A

Date: Monday, July 23, 2007 Sheet 30 of 35

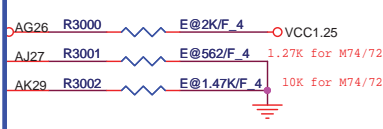
U3001A PART 1 OF 7

GFX_TXP0	AK33	PCIE_RX0P	PCIE_TX0P	AG31	C GFX_RXP0	C3000	E@0.1U_4	GFX_RXP0
GFX_TXN0	AJ33	PCIE_RX0N	PCIE_TX0N	AG30	C GFX_RXN0	C3001	E@0.1U_4	GFX_RXN0
GFX_TXP1	AJ35	PCIE_RX1P	PCIE_TX1P	AF31	C GFX_RXP1	C3002	E@0.1U_4	GFX_RXP1
GFX_TXN1	AJ34	PCIE_RX1N	PCIE_TX1N	AF30	C GFX_RXN1	C3003	E@0.1U_4	GFX_RXN1
GFX_TXP2	AH35	PCIE_RX2P	PCIE_TX2P	AF28	C GFX_RXP2	C3004	E@0.1U_4	GFX_RXP2
GFX_TXN2	AH34	PCIE_RX2N	PCIE_TX2N	AF27	C GFX_RXN2	C3005	E@0.1U_4	GFX_RXN2
GFX_TXP3	AG35	PCIE_RX3P	PCIE_TX3P	AD31	C GFX_RXP3	C3006	E@0.1U_4	GFX_RXP3
GFX_TXN3	AG34	PCIE_RX3N	PCIE_TX3N	AD30	C GFX_RXN3	C3007	E@0.1U_4	GFX_RXN3
GFX_TXP4	AF33	PCIE_RX4P	PCIE_TX4P	AD28	C GFX_RXP4	C3008	E@0.1U_4	GFX_RXP4
GFX_TXN4	AE33	PCIE_RX4N	PCIE_TX4N	AD27	C GFX_RXN4	C3009	E@0.1U_4	GFX_RXN4
GFX_TXP5	AE35	PCIE_RX5P	PCIE_TX5P	AB31	C GFX_RXP5	C3010	E@0.1U_4	GFX_RXP5
GFX_TXN5	AE34	PCIE_RX5N	PCIE_TX5N	AB30	C GFX_RXN5	C3011	E@0.1U_4	GFX_RXN5
GFX_TXP6	AD35	PCIE_RX6P	PCIE_TX6P	AB28	C GFX_RXP6	C3012	E@0.1U_4	GFX_RXP6
GFX_TXN6	AD34	PCIE_RX6N	PCIE_TX6N	AB27	C GFX_RXN6	C3013	E@0.1U_4	GFX_RXN6
GFX_TXP7	AC35	PCIE_RX7P	PCIE_TX7P	AA31	C GFX_RXP7	C3014	E@0.1U_4	GFX_RXP7
GFX_TXN7	AC34	PCIE_RX7N	PCIE_TX7N	AA30	C GFX_RXN7	C3015	E@0.1U_4	GFX_RXN7
GFX_TXP8	AB33	PCIE_RX8P	PCIE_TX8P	AA28	C GFX_RXP8	C3016	E@0.1U_4	GFX_RXP8
GFX_TXN8	AA33	PCIE_RX8N	PCIE_TX8N	AA27	C GFX_RXN8	C3017	E@0.1U_4	GFX_RXN8
GFX_TXP9	AA35	PCIE_RX9P	PCIE_TX9P	W31	C GFX_RXP9	C3018	E@0.1U_4	GFX_RXP9
GFX_TXN9	AA34	PCIE_RX9N	PCIE_TX9N	W30	C GFX_RXN9	C3019	E@0.1U_4	GFX_RXN9
GFX_TXP10	Y35	PCIE_RX10P	PCIE_TX10P	W28	C GFX_RXP10	C3020	E@0.1U_4	GFX_RXP10
GFX_TXN10	Y34	PCIE_RX10N	PCIE_TX10N	W27	C GFX_RXN10	C3021	E@0.1U_4	GFX_RXN10
GFX_TXP11	W35	PCIE_RX11P	PCIE_TX11P	V31	C GFX_RXP11	C3022	E@0.1U_4	GFX_RXP11
GFX_TXN11	W34	PCIE_RX11N	PCIE_TX11N	V30	C GFX_RXN11	C3023	E@0.1U_4	GFX_RXN11
GFX_TXP12	V33	PCIE_RX12P	PCIE_TX12P	V28	C GFX_RXP12	C3024	E@0.1U_4	GFX_RXP12
GFX_TXN12	U33	PCIE_RX12N	PCIE_TX12N	V27	C GFX_RXN12	C3025	E@0.1U_4	GFX_RXN12
GFX_TXP13	U35	PCIE_RX13P	PCIE_TX13P	U31	C GFX_RXP13	C3026	E@0.1U_4	GFX_RXP13
GFX_TXN13	U34	PCIE_RX13N	PCIE_TX13N	U30	C GFX_RXN13	C3027	E@0.1U_4	GFX_RXN13
GFX_TXP14	T35	PCIE_RX14P	PCIE_TX14P	U28	C GFX_RXP14	C3028	E@0.1U_4	GFX_RXP14
GFX_TXN14	T34	PCIE_RX14N	PCIE_TX14N	U27	C GFX_RXN14	C3029	E@0.1U_4	GFX_RXN14
GFX_TXP15	R35	PCIE_RX15P	PCIE_TX15P	R31	C GFX_RXP15	C3030	E@0.1U_4	GFX_RXP15
GFX_TXN15	R34	PCIE_RX15N	PCIE_TX15N	R30	C GFX_RXN15	C3031	E@0.1U_4	GFX_RXN15



Clock		Calibration	
PCIE_REFCLKP	PCIE_REFCLKN	PCIE_CALRN	PCIE_CALRP
RSVD_1	RSVD_2	PCIE_CALI	
PERSTB			

E@ATI-M64-M

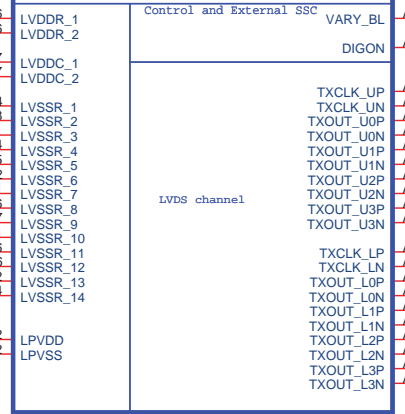


1.8V for M74/72

1.8V for M74/72

1.8V for M74/72

U3001G PART 7 OF 7



E@ATI-M64-M

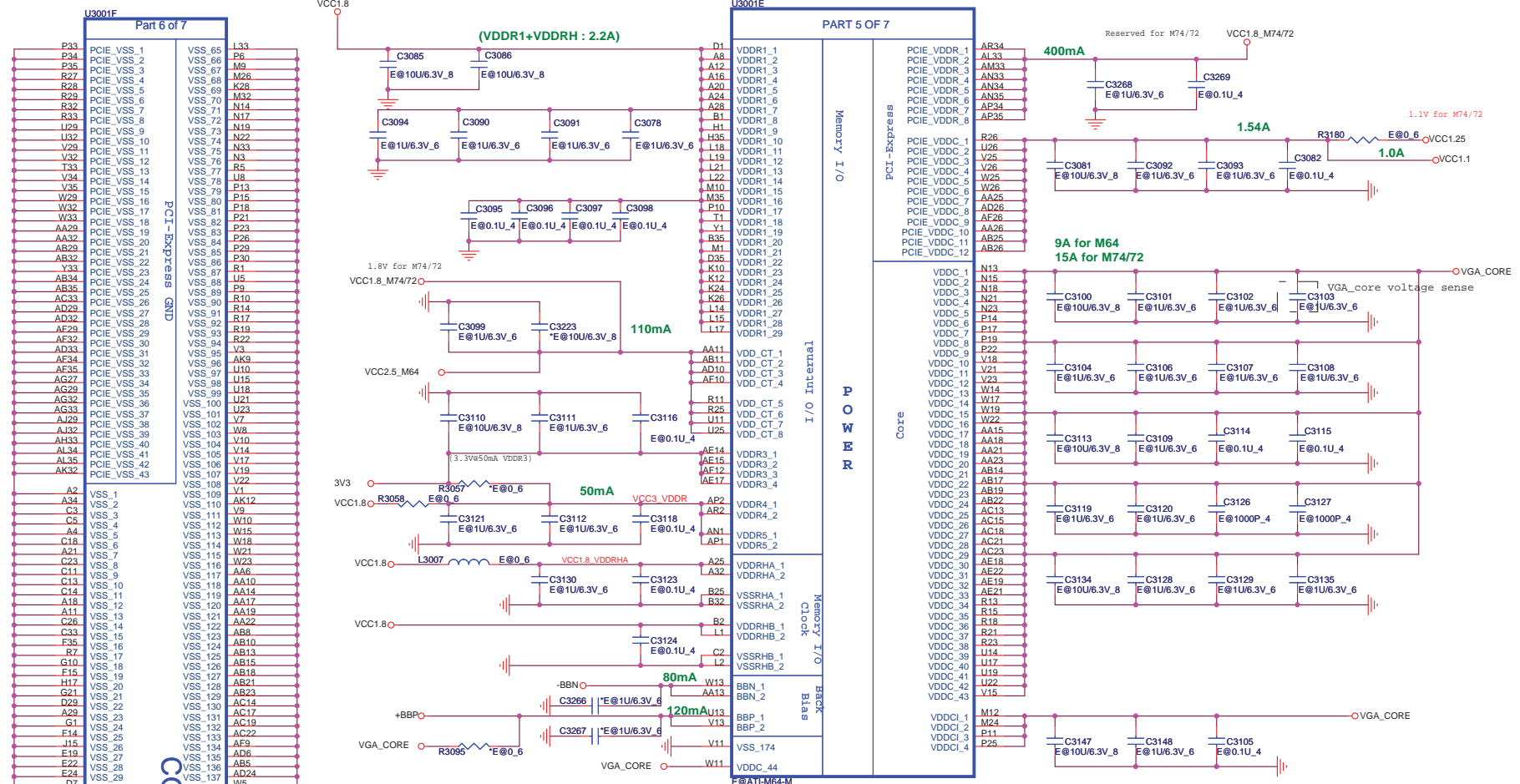


1st LVDS CH



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CORE GND

POWER Regulator	M64/M71	Ra11	M72/M74	Ra11
VDDC+VDDCI	1.0-1.2V	VGA_CORE	0.95-1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+TPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VDD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72

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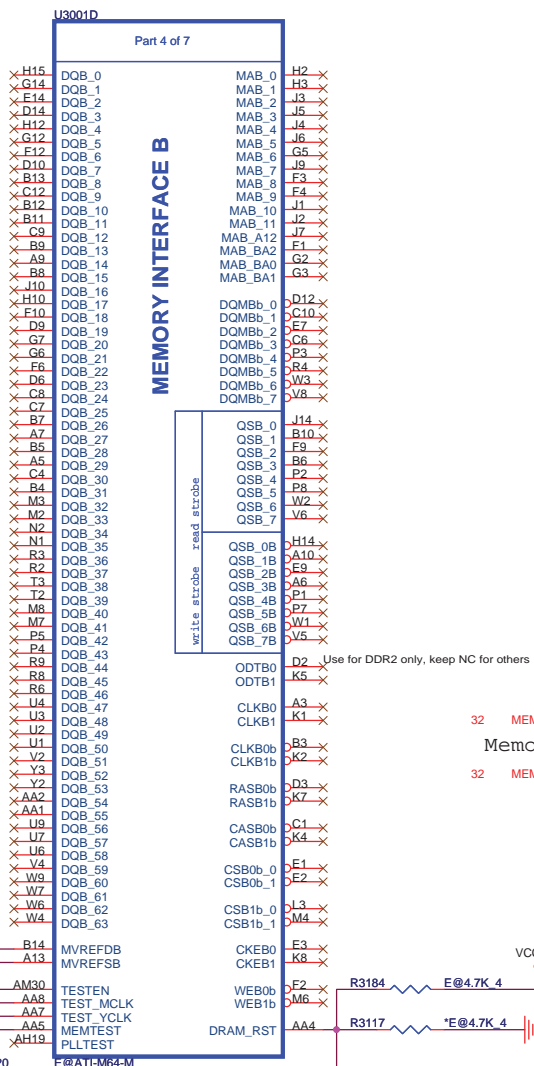
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QUANTA COMPUTER

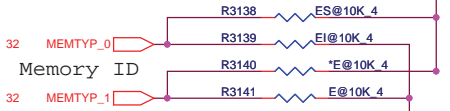
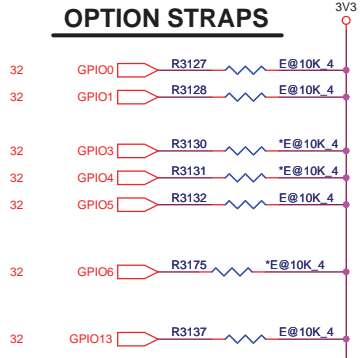
File: **ATI M64M POWER**

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Channel B



OPTION STRAPS



M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3140	R3141	R3138	R3139	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3(G) : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - Hynix GDDR3: 2M x 32 bits x 4 banks
1	1	10K	NC	10K	NC	11 - SAMSUNG GDDR3(I) : 2M x 32 bits x 4 banks



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