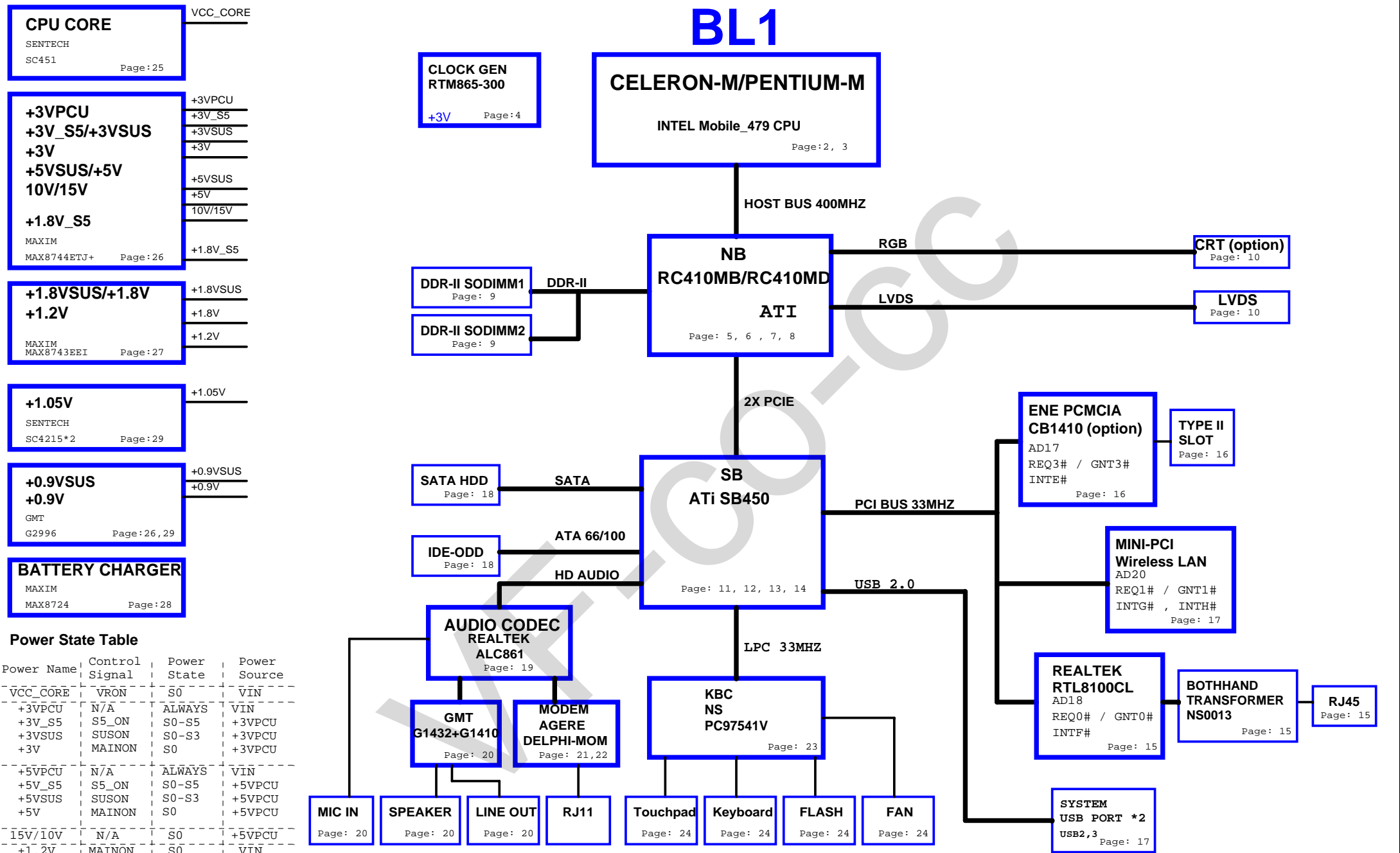
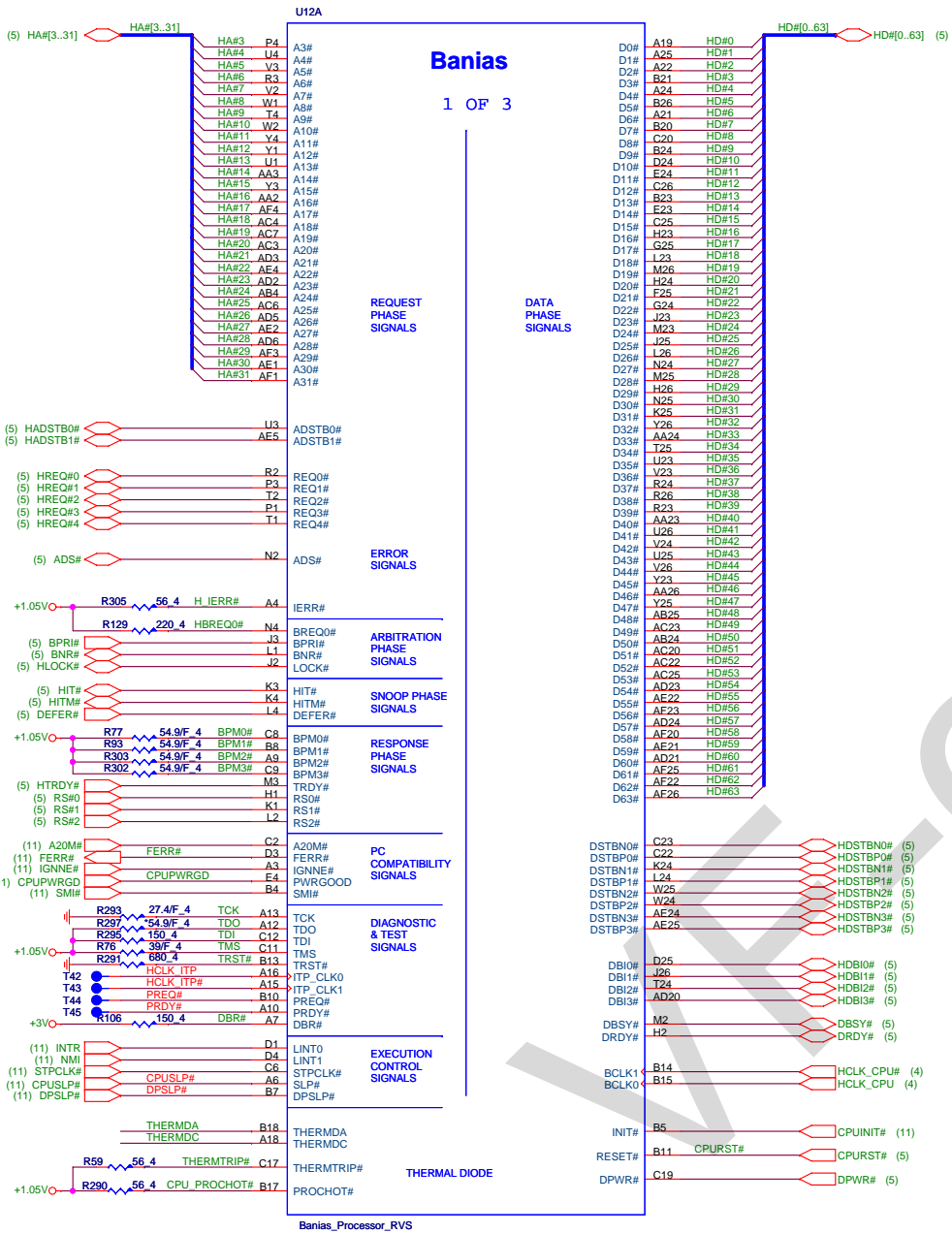


# BL1



**Power State Table**

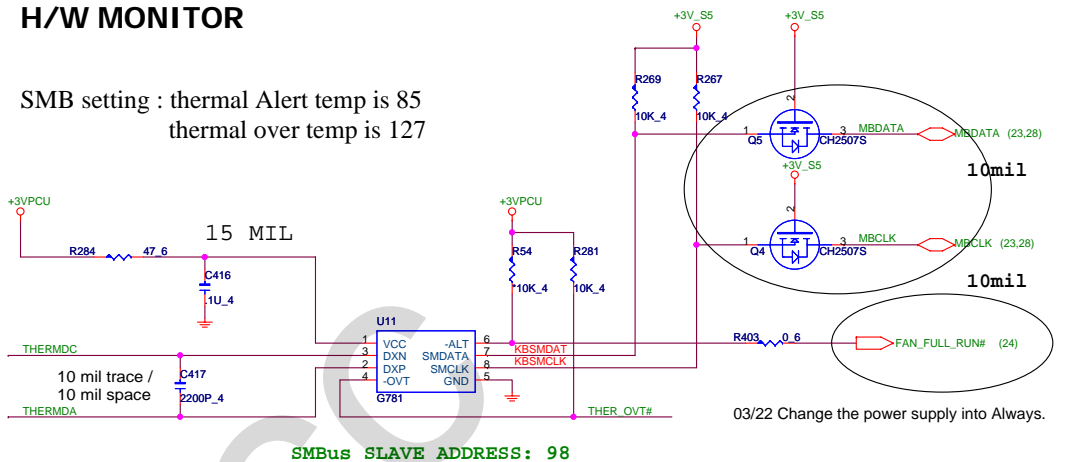
Power Name	Control Signal	Power State	Power Source
VCC_CORE	VRON	S0	VIN
+3VPCU	N/A	ALWAYS	VIN
+3V_S5	S5_ON	S0-S5	+3VPCU
+3VSUS	SUSON	S0-S3	+3VPCU
+3V	MAINON	S0	+3VPCU
+5VPCU	N/A	ALWAYS	VIN
+5V_S5	S5_ON	S0-S5	+5VPCU
+5VSUS	SUSON	S0-S3	+5VPCU
+5V	MAINON	S0	+5VPCU
15V/10V	N/A	S0	+5VPCU
+1.2V	MAINON	S0	VIN
+1.05V	MAINON	S0	+1.8VSUS
+0.9V	MAINON	S0	+1.8VSUS
+1.8V_S5	S5_ON	S0-S5	+3VPCU
+1.8VSUS	SUSON	S0-S3	VIN
+1.8V	MAINON	S0	+1.8VSUS



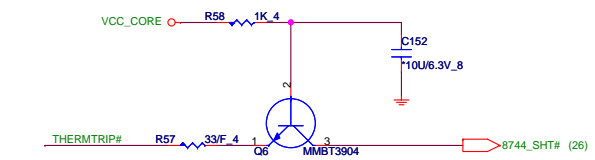
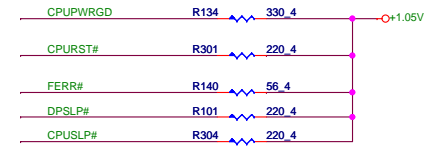
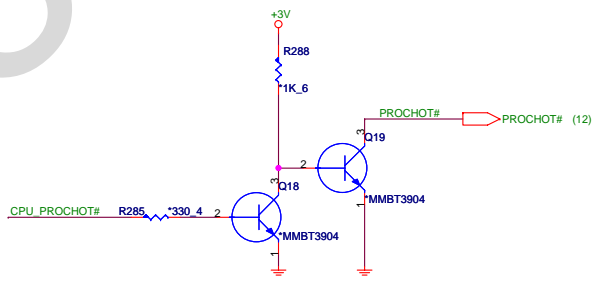
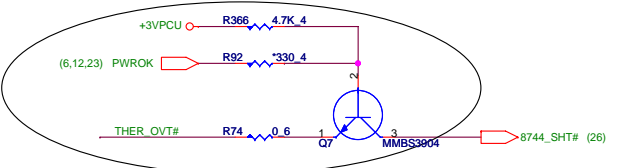
# CPU

## H/W MONITOR

SMB setting : thermal Alert temp is 85  
thermal over temp is 127

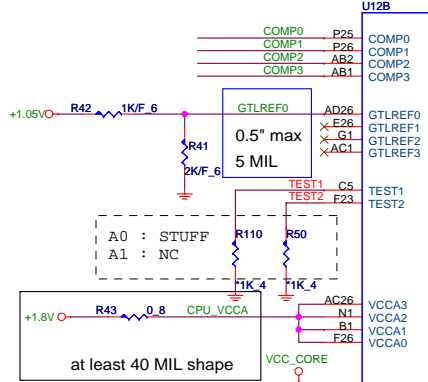
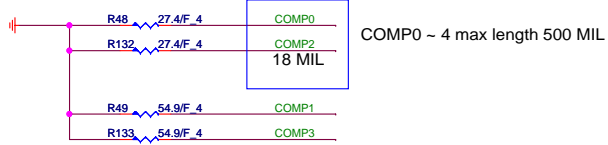


	-OVT	-ALT
CPU	127	
Ambient		85

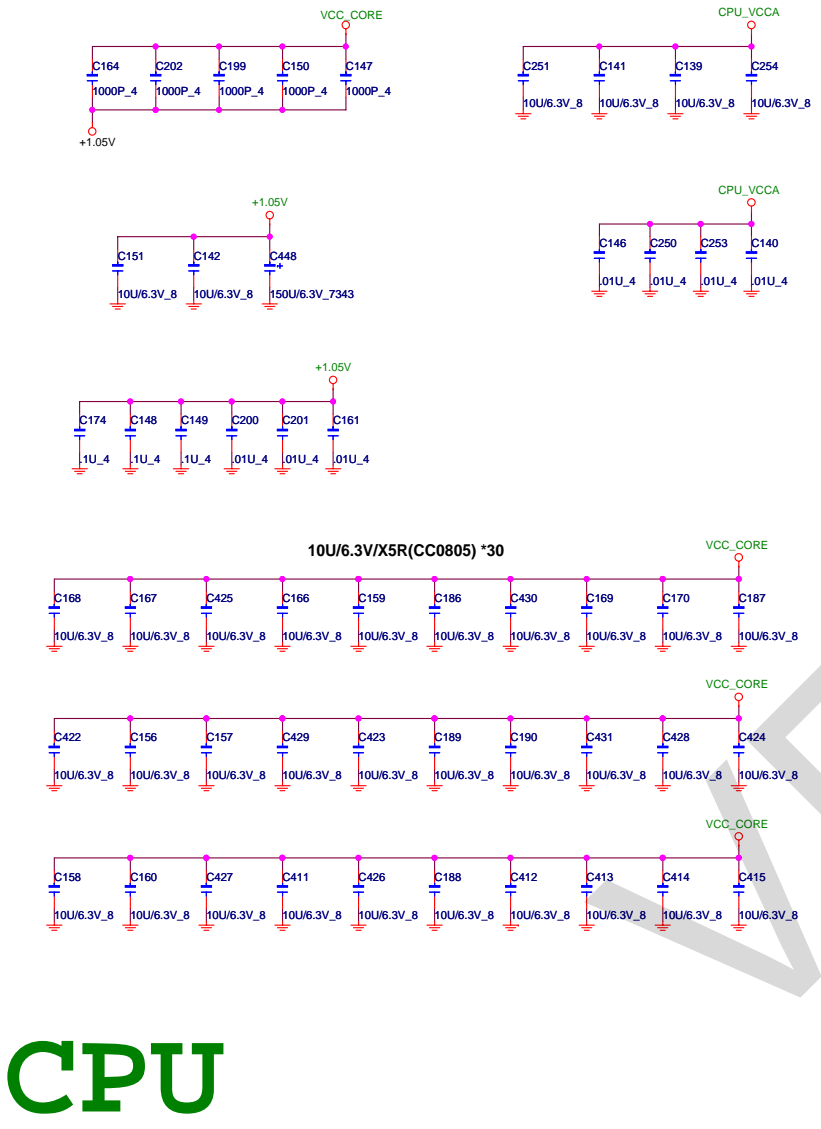
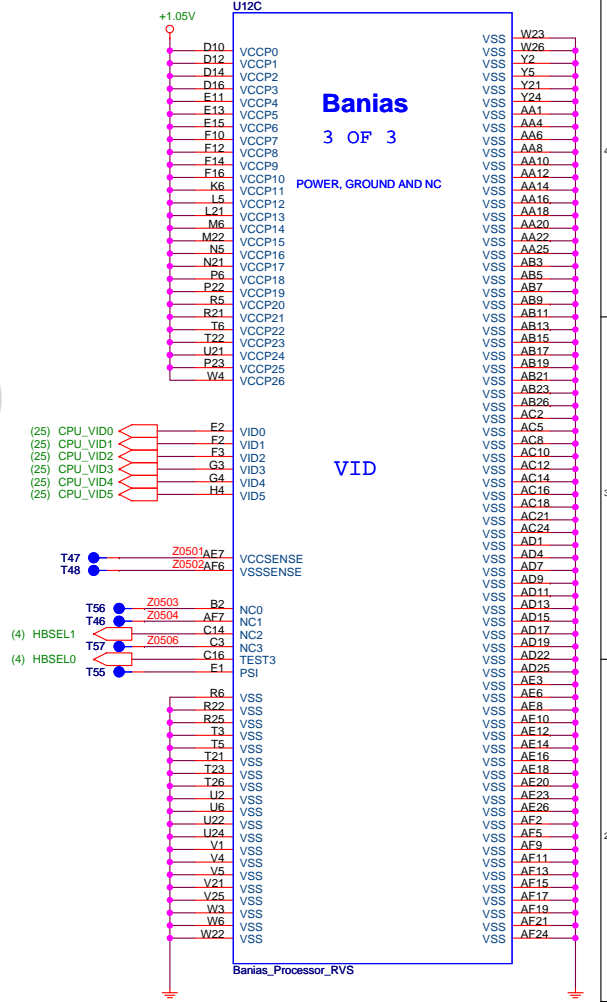


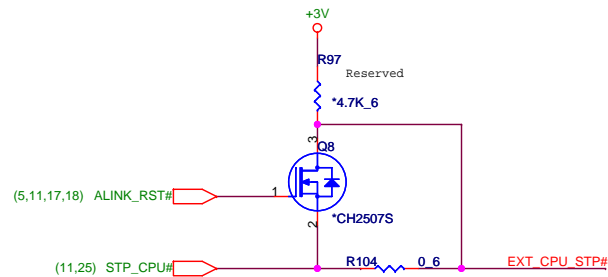
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CPU ( HOST BUS )-1</b>	2A
Date:	Monday, April 03, 2006	Sheet 2 of 30

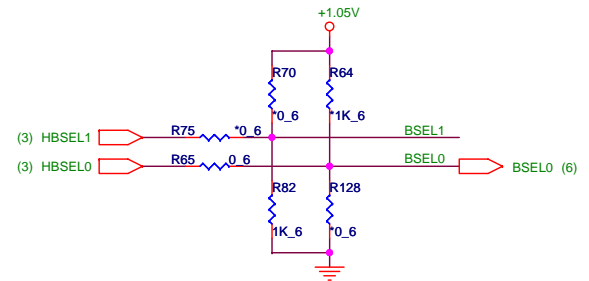
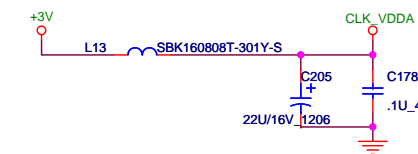
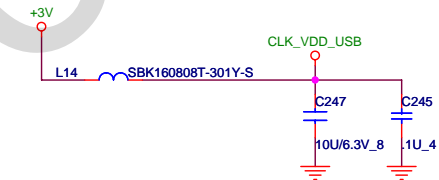
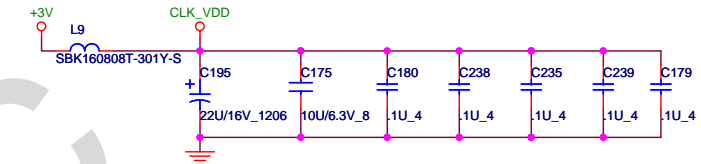
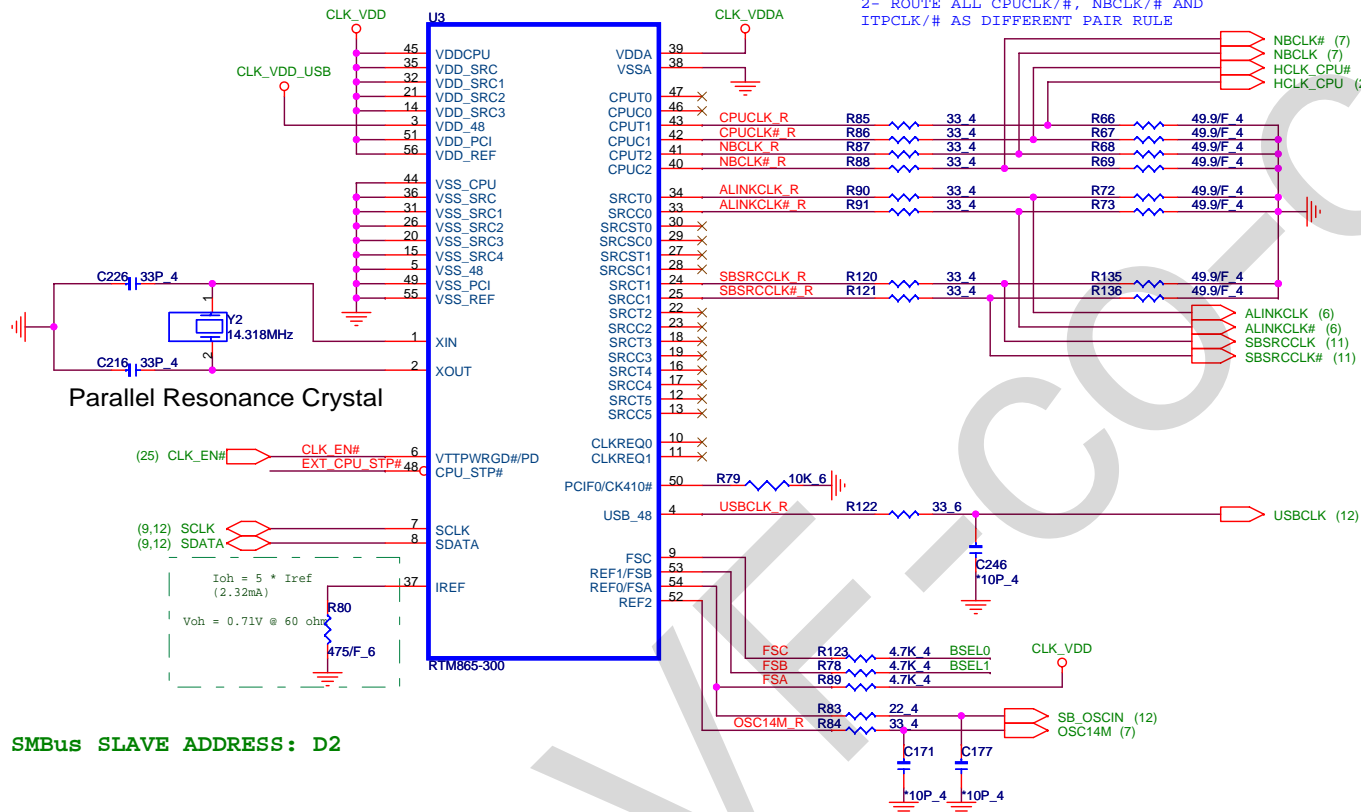


COMP0	P25	COMP0	A2
COMP1	P26	COMP1	A5
COMP2	AB2	COMP2	A8
COMP3	AB1	COMP3	A11
			A14
			A17
			A20
			A23
			A26
			B3
			B6
			B9
			B12
			B16
			B19
			B22
			B25
			M22
			M6
			VCCP4
			C7
			C10
			C13
			C15
			C18
			C21
			C24
			D2
			D7
			D9
			D11
			D13
			D15
			D17
			D19
			D21
			D23
			D26
			E3
			E6
			E8
			E10
			E12
			E14
			E16
			E18
			E20
			E22
			E25
			F1
			F4
			F7
			F9
			F11
			F13
			F15
			F17
			F19
			F21
			F24
			G2
			G6
			G22
			G23
			G26
			H3
			H5
			H21
			H25
			J1
			J4
			J6
			J22
			J24
			K2
			K5
			K21
			K23
			K26
			L3
			L6
			L22
			L25
			M1
			M4
			M5
			M21
			M24
			N3
			N6
			N22
			N23
			N26
			P2
			P5
			P21
			P24
			R1
			R4





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CLK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCCLK/# AS DIFFERENT PAIR RULE



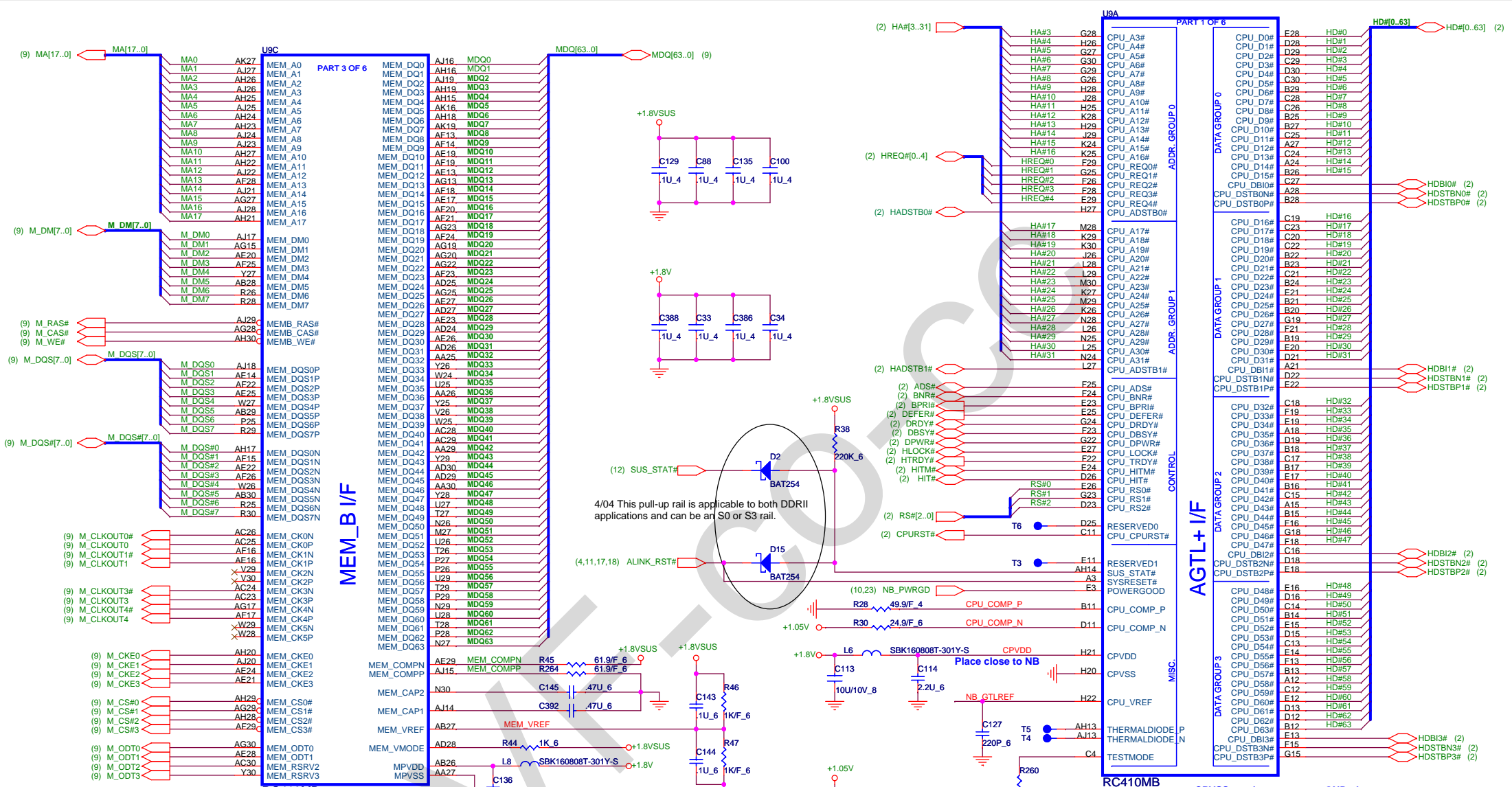
BSEL1	BSEL0	Frequency
0	0	133 MHz
0	1	100 MHz

SMBus SLAVE ADDRESS: D2

CK410 FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Rsvd

# CLK

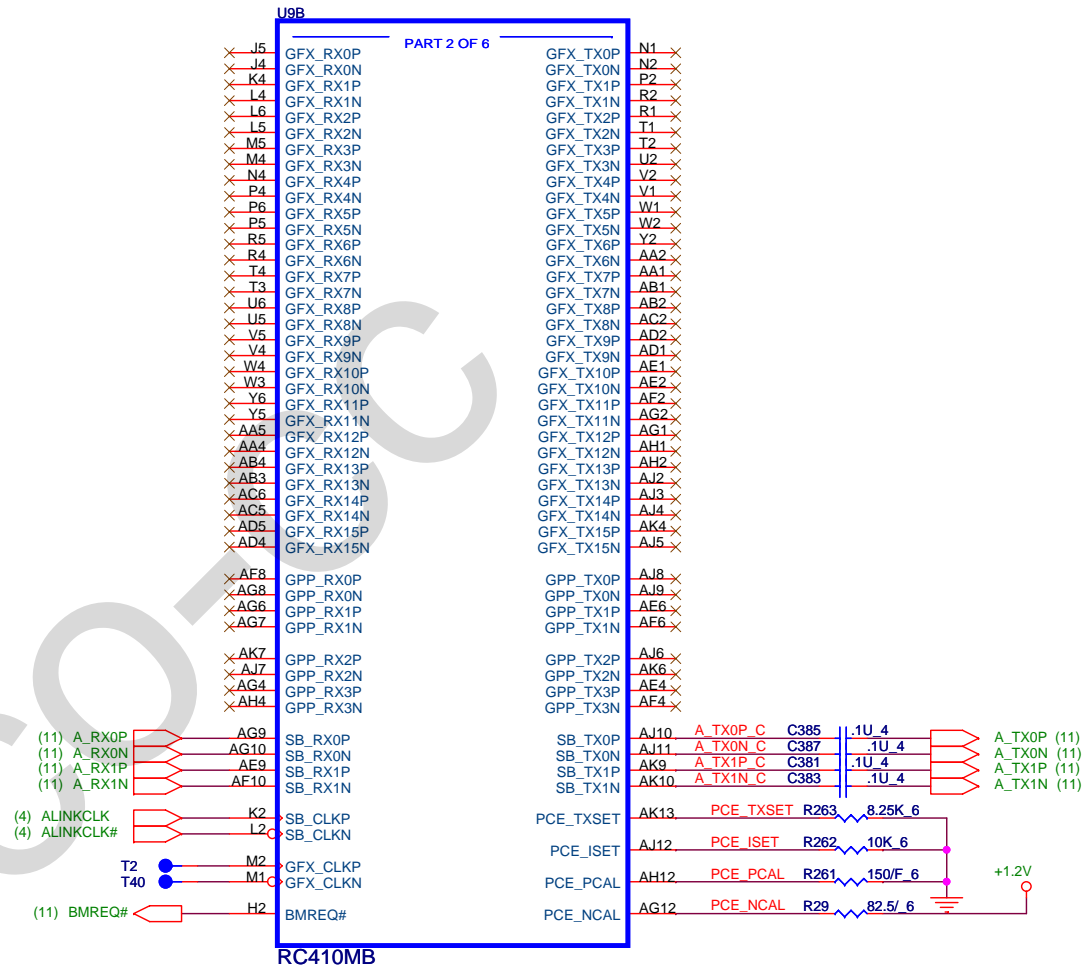
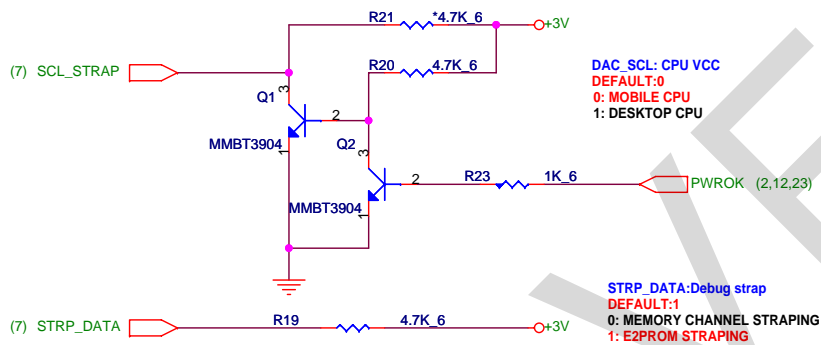
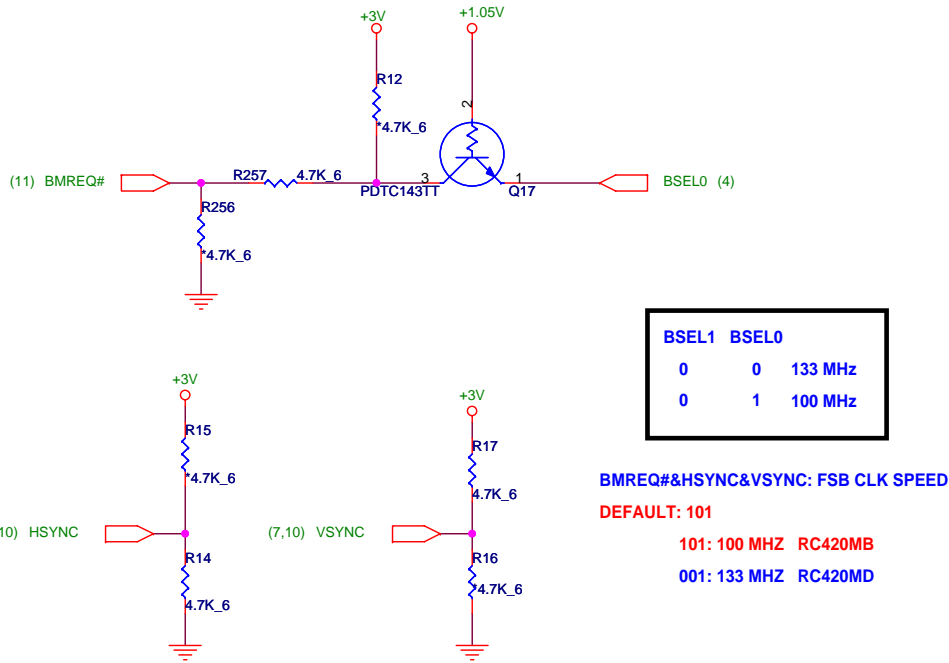


MEM\_B I/F  
RC410MB  
MPVSS need to connect to GND plane immediately through a dedicated VIA

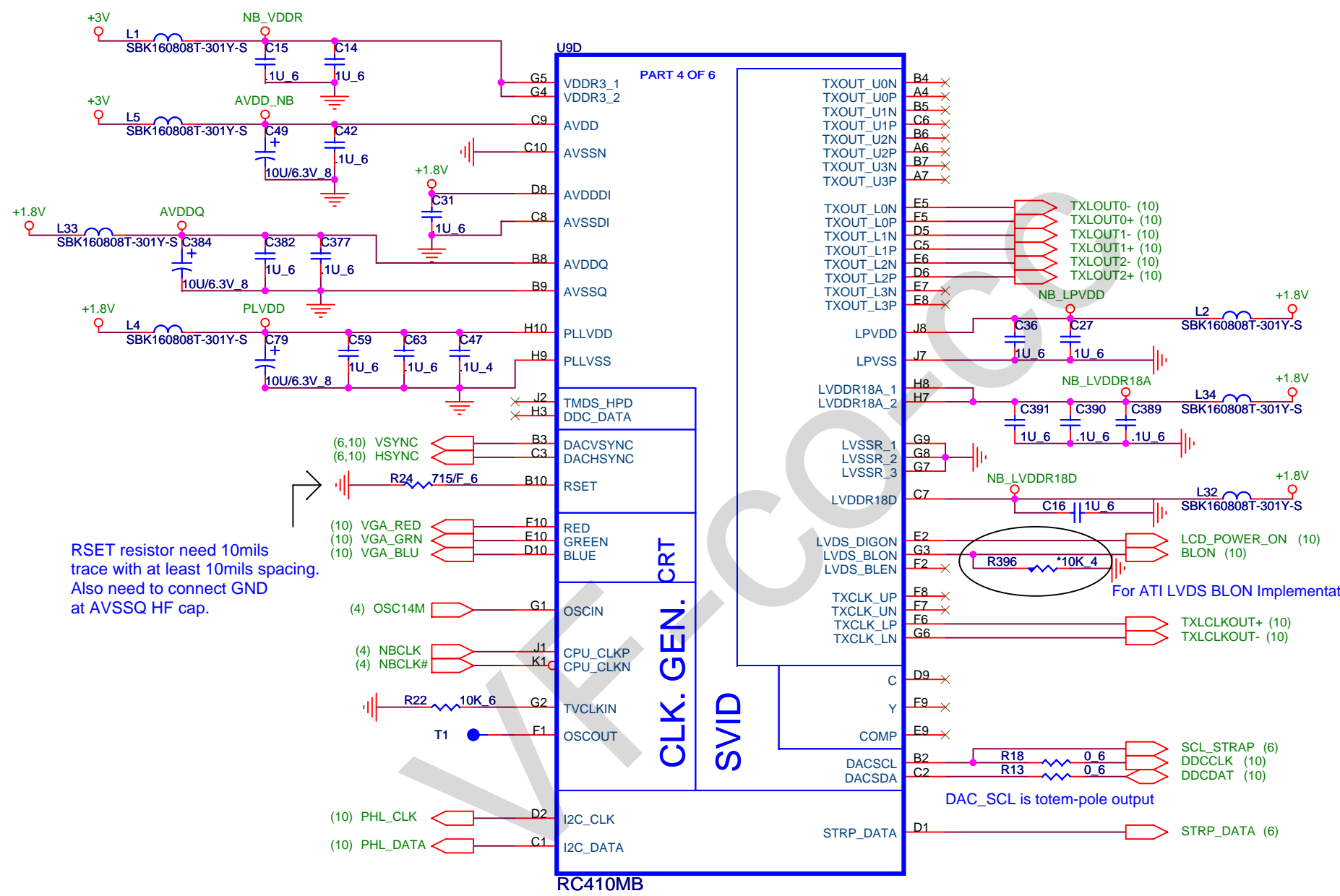
AGTL+ I/F  
RC410MB  
CPVSS need to connect to GND plane immediately through a dedicated VIA

		PROJECT : BL1 Quanta Computer Inc.
Size	Document Number	Rev
	RC410MB-AGTL+ I/F	3A
Date:	Friday, April 28, 2006	Sheet 5 of 30

# NB strapping




**PROJECT : BL1**  
**Quanta Computer Inc.**



RSET resistor need 10mils trace with at least 10mils spacing. Also need to connect GND at AVSSQ HF cap.

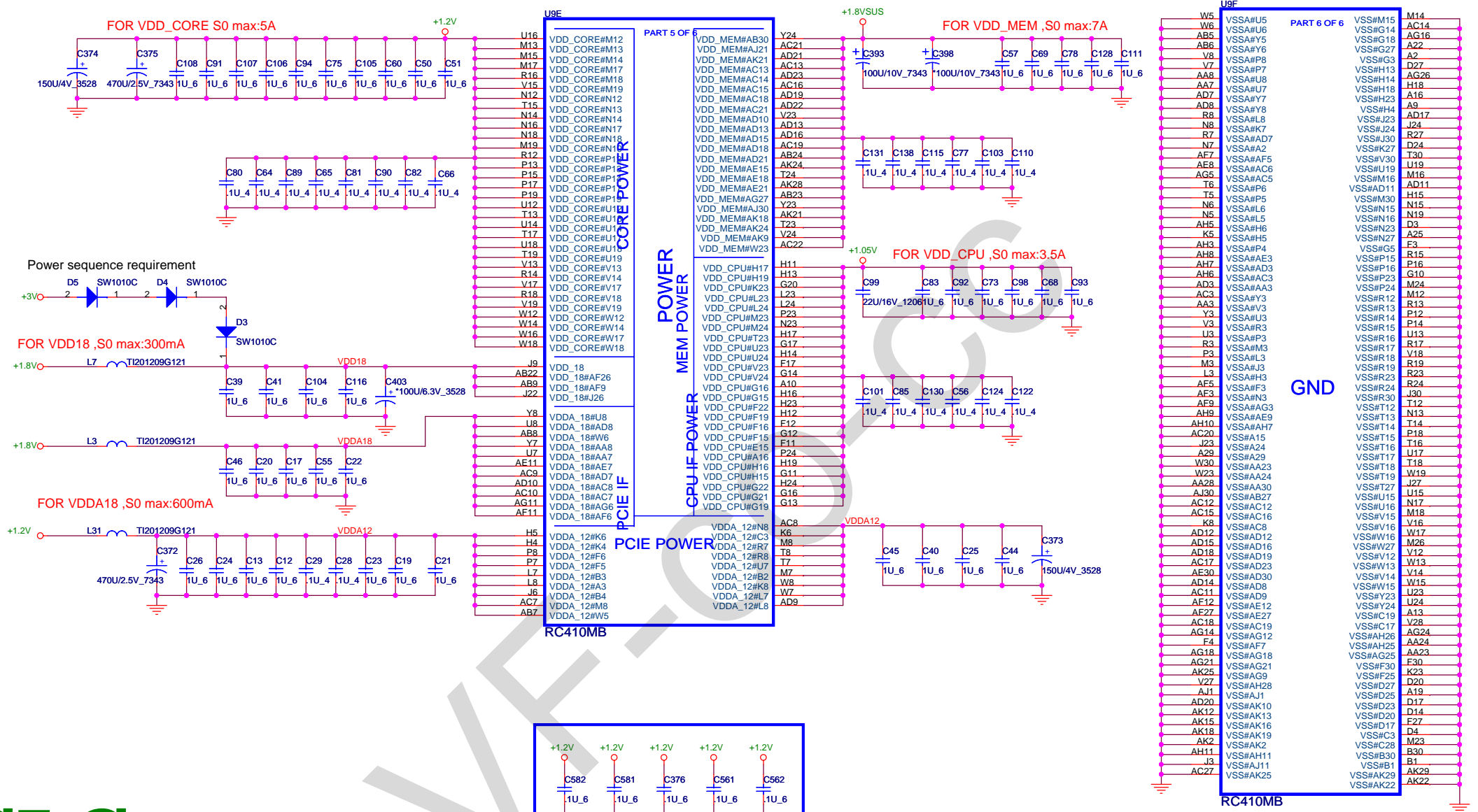
For ATI LVDS BLON Implementation Details

DAC\_SCL is totem-pole output



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-VIDEO &amp; CLKGEN</b>	2A
Date:	Friday, May 05, 2006	Sheet 7 of 30



5

4

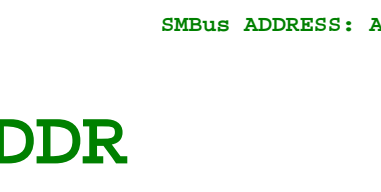
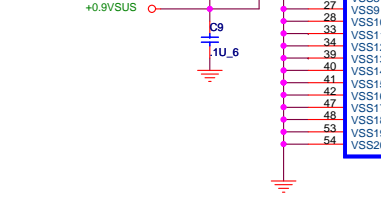
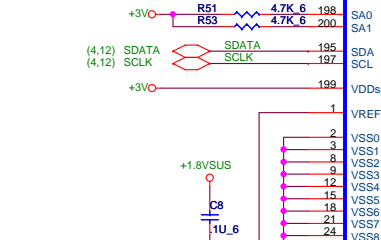
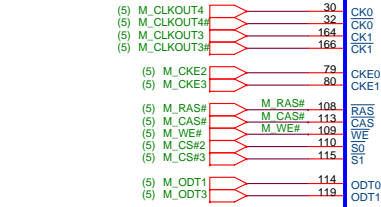
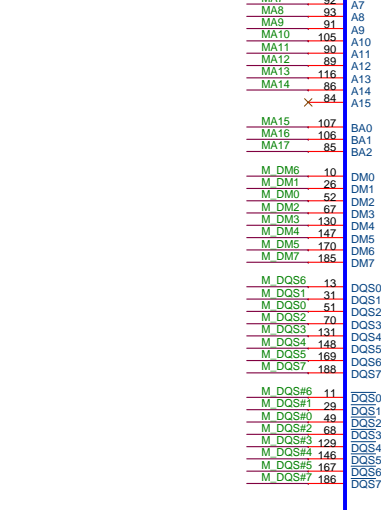
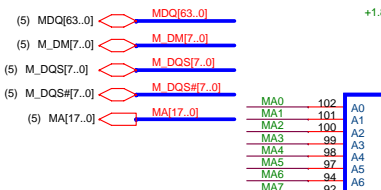
3

2

**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-POWER</b>	1A
Date:	Thursday, April 06, 2006	Sheet 8 of 30

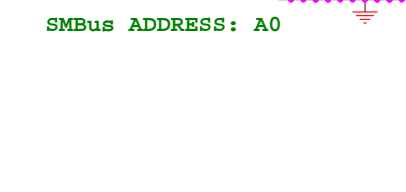
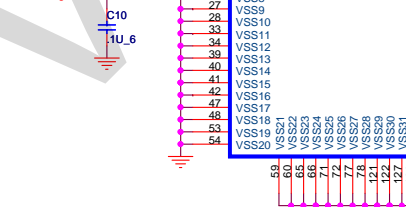
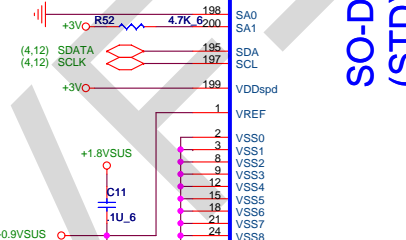
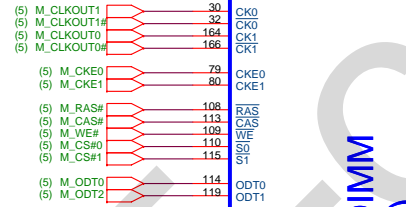
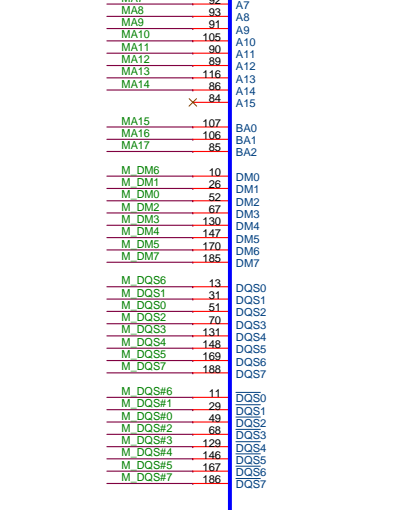
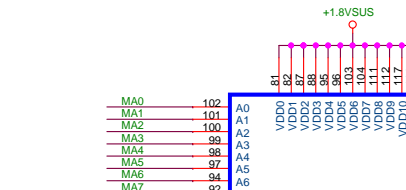




SO-DIMM  
(STD)

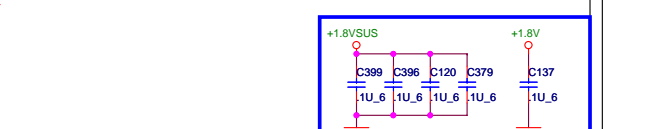
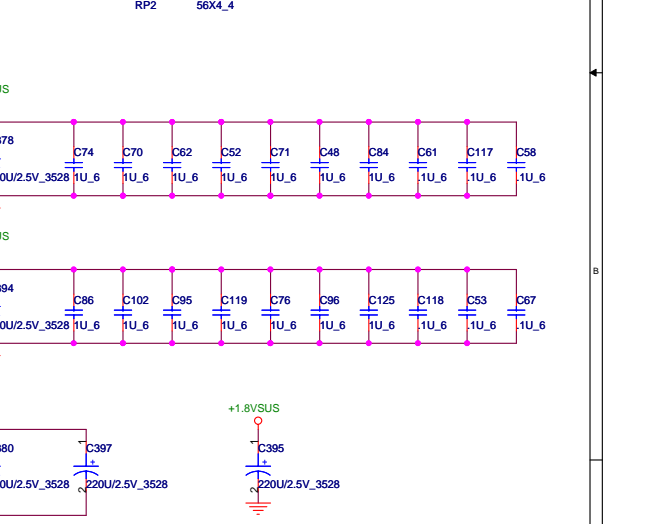
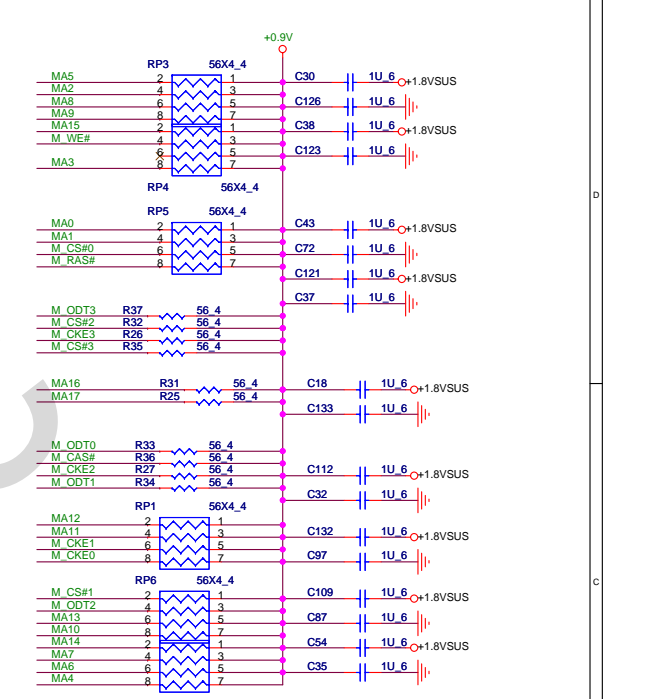
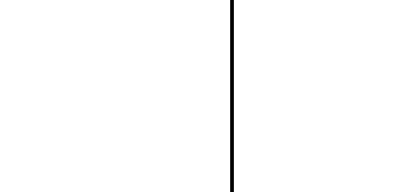
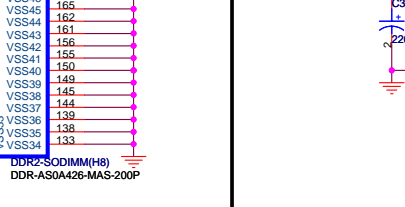
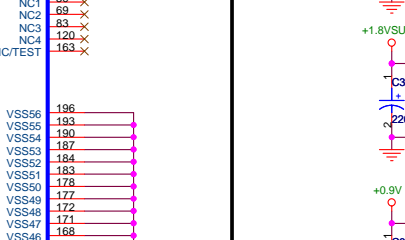
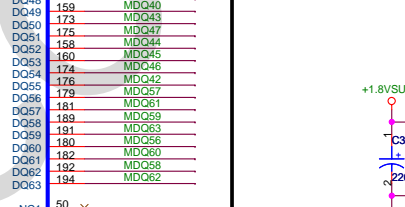
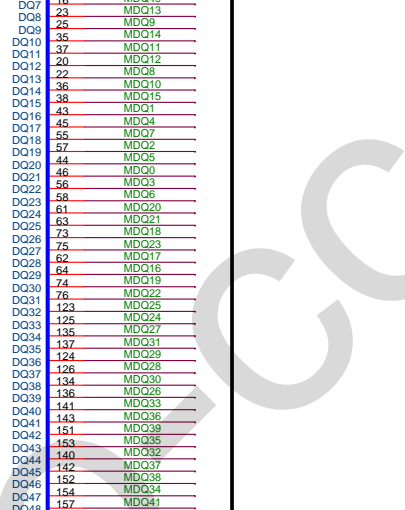
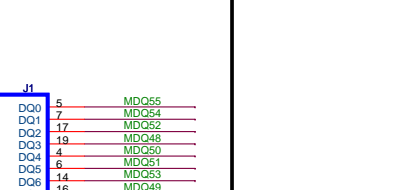
AMP-DDR-SODIMM-200P

DDR



SO-DIMM  
(STD)

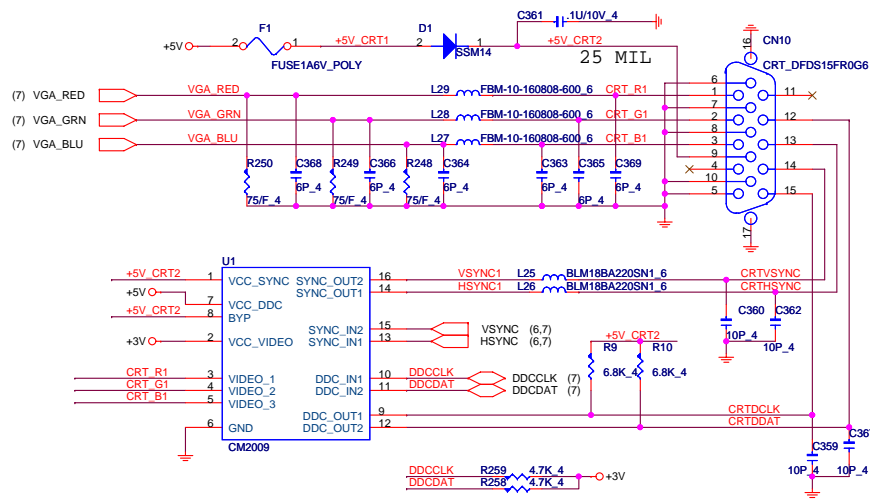
DDR-A0A426-MA5-200P



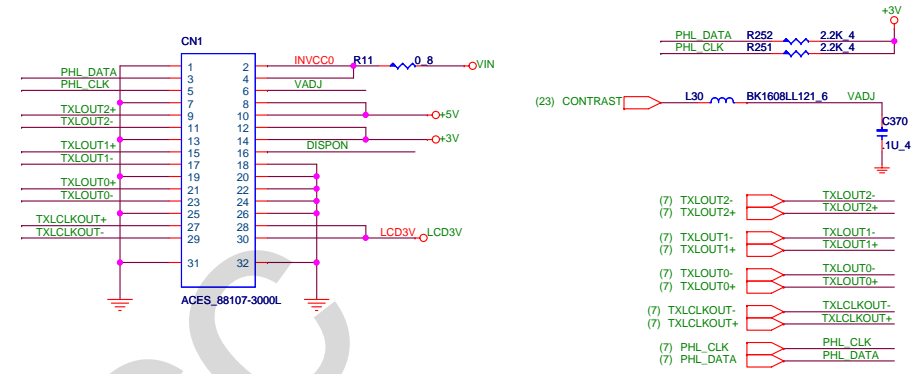
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR2 SO-DIMM</b>	1A
Date:	Saturday, May 06, 2006	Sheet 9 of 30

# CRT PORT

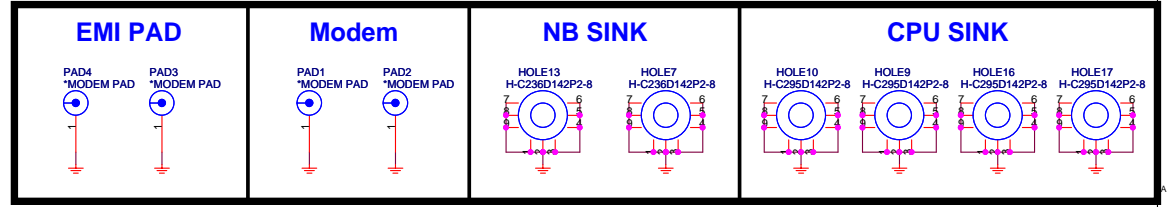
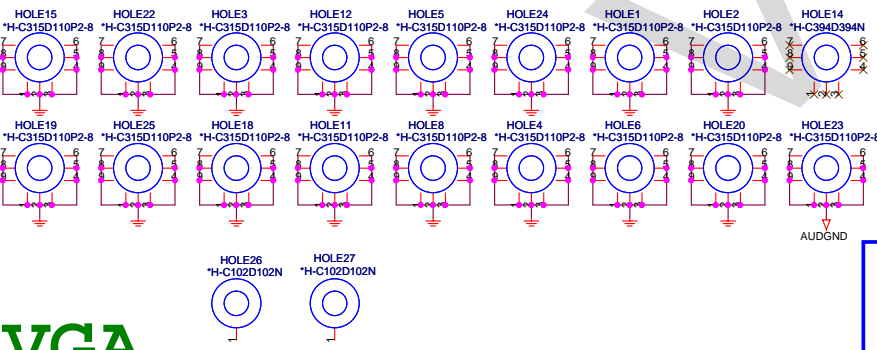
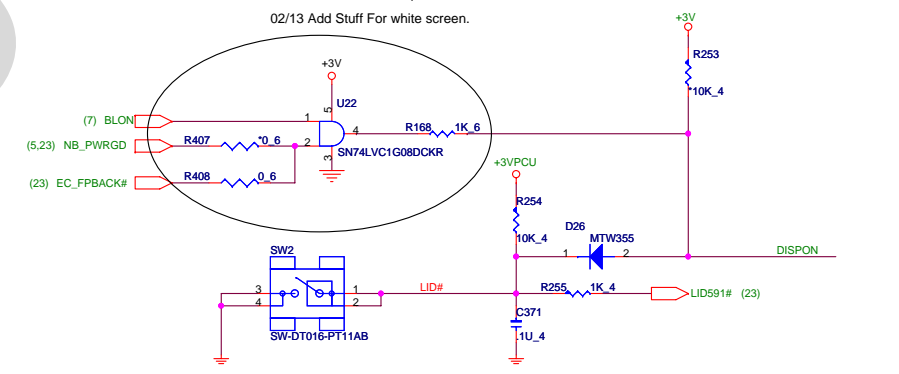


# LCD Connector



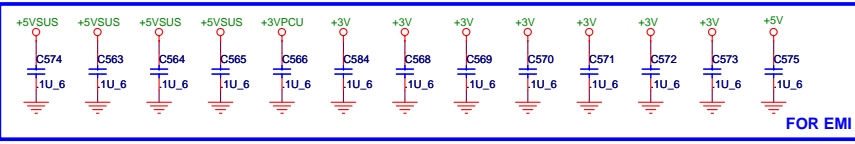
# Lid Switch

05/05 Add Resistor 1Kohm on Buffer output.  
 04/28 The Solve Boot up white line on LG LCD issue.  
 02/13 Add Stuff For white screen.



VGA

3/31 Add EMI Solution

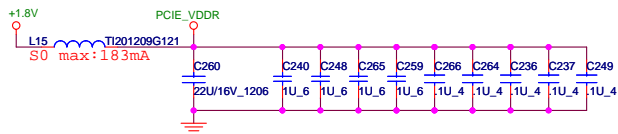
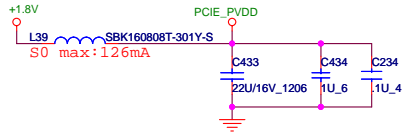
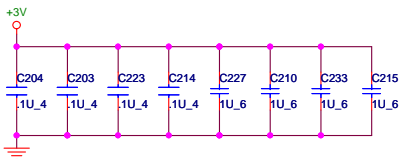


**PROJECT : BL1**  
**Quanta Computer Inc.**

Size: Document Number  
**VGA Ports, LID, & HOLES**

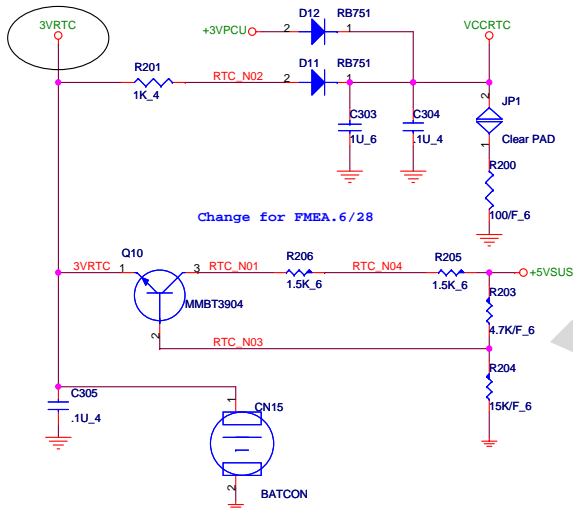
Date: Wednesday, May 10, 2006 Sheet 10 of 30

Rev 3B

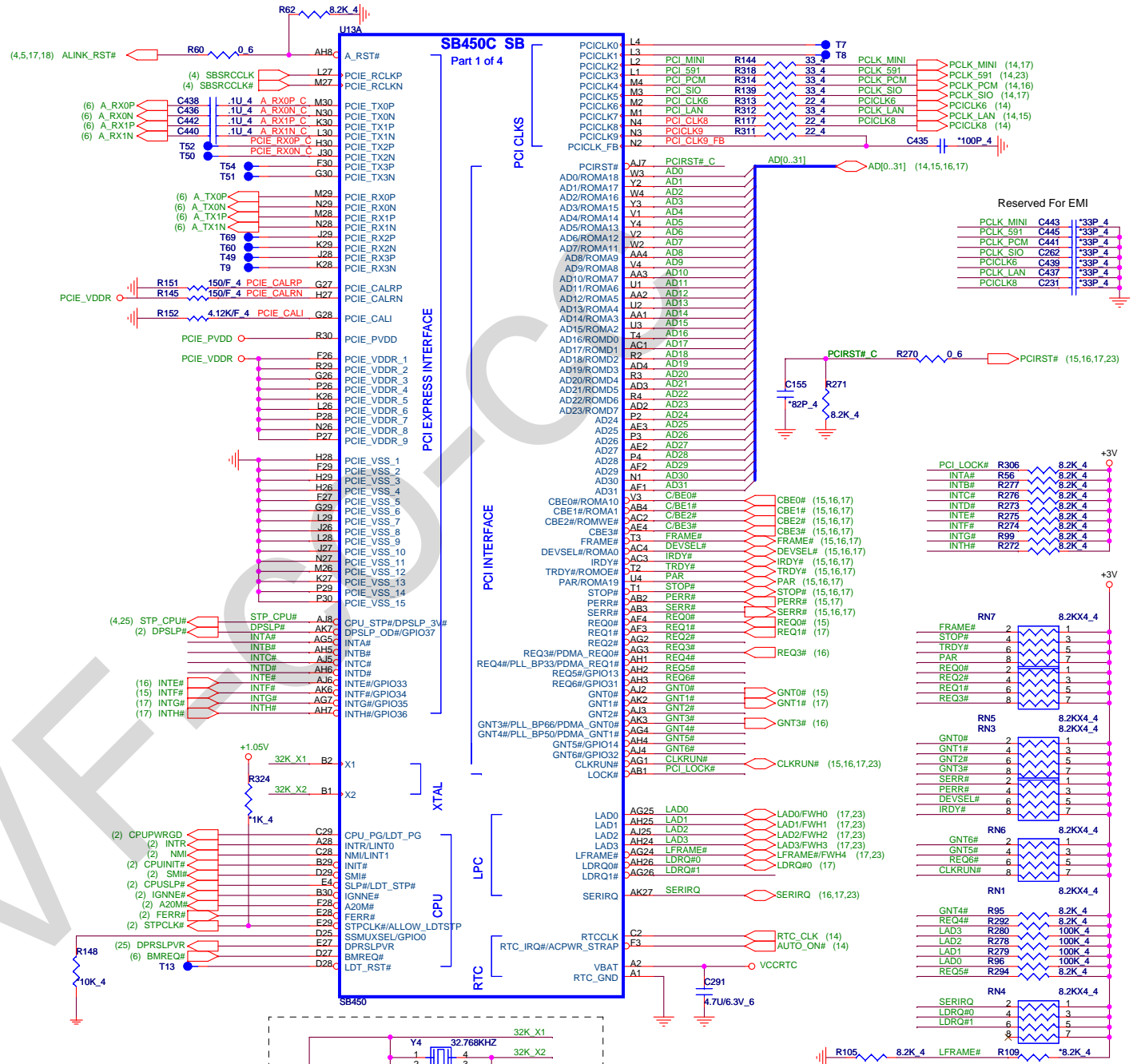


**RTC**

4/2 Battery should be connected directly - not through a UL resistor, and not through a diode.



**CLG**



Reserved For EMI

PCCLK_MINI	C443	*33P_4
PCCLK_S91	C445	*33P_4
PCCLK_PCM	C441	*33P_4
PCCLK_SIO	C262	*33P_4
PCICLK6	C439	*33P_4
PCCLK_LAN	C437	*33P_4
PCICLK8	C231	*33P_4

PCI_LOCK#	R306	8.2K_4
INTA#	R56	8.2K_4
INTB#	R277	8.2K_4
INTC#	R276	8.2K_4
INTD#	R273	8.2K_4
INTE#	R275	8.2K_4
INTF#	R274	8.2K_4
INTG#	R99	8.2K_4
INTH#	R272	8.2K_4

FRAME#	RN7	8.2KX4_4
STOP#	2	1
TRDY#	6	5
PAR	8	7
REQ0#	2	1
REQ2#	4	3
REQ1#	6	5
REQ3#	8	7

GNT0#	RN5	8.2KX4_4
RN3	2	1
GNT1#	4	3
GNT2#	6	5
GNT3#	8	7
SERR#	2	1
PERR#	4	3
DEVSEL#	6	5
IRDY#	8	7

GNT6#	RN6	8.2KX4_4
GNT5#	4	3
REQ6#	6	5
CLKRUN#	8	7

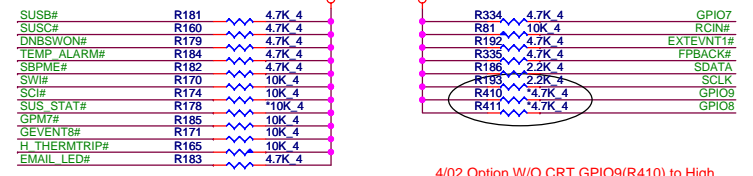
GNT4#	RN1	8.2KX4_4
REQ4#	2	1
LAD3	R280	100K_4
LAD2	R278	100K_4
LAD1	R279	100K_4
LAD0	R96	100K_4
REQ5#	R284	8.2K_4

SERIRQ	RN4	8.2KX4_4
LDRQ#0	4	3
LDRQ#1	6	5
CLKRUN#	8	7

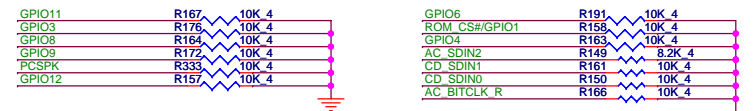
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Customer	SB450C PCIE/PC/CPU/LPC/IF	1A
Date:	Friday, May 05, 2006	Sheet 11 of 30

**PU/PD**

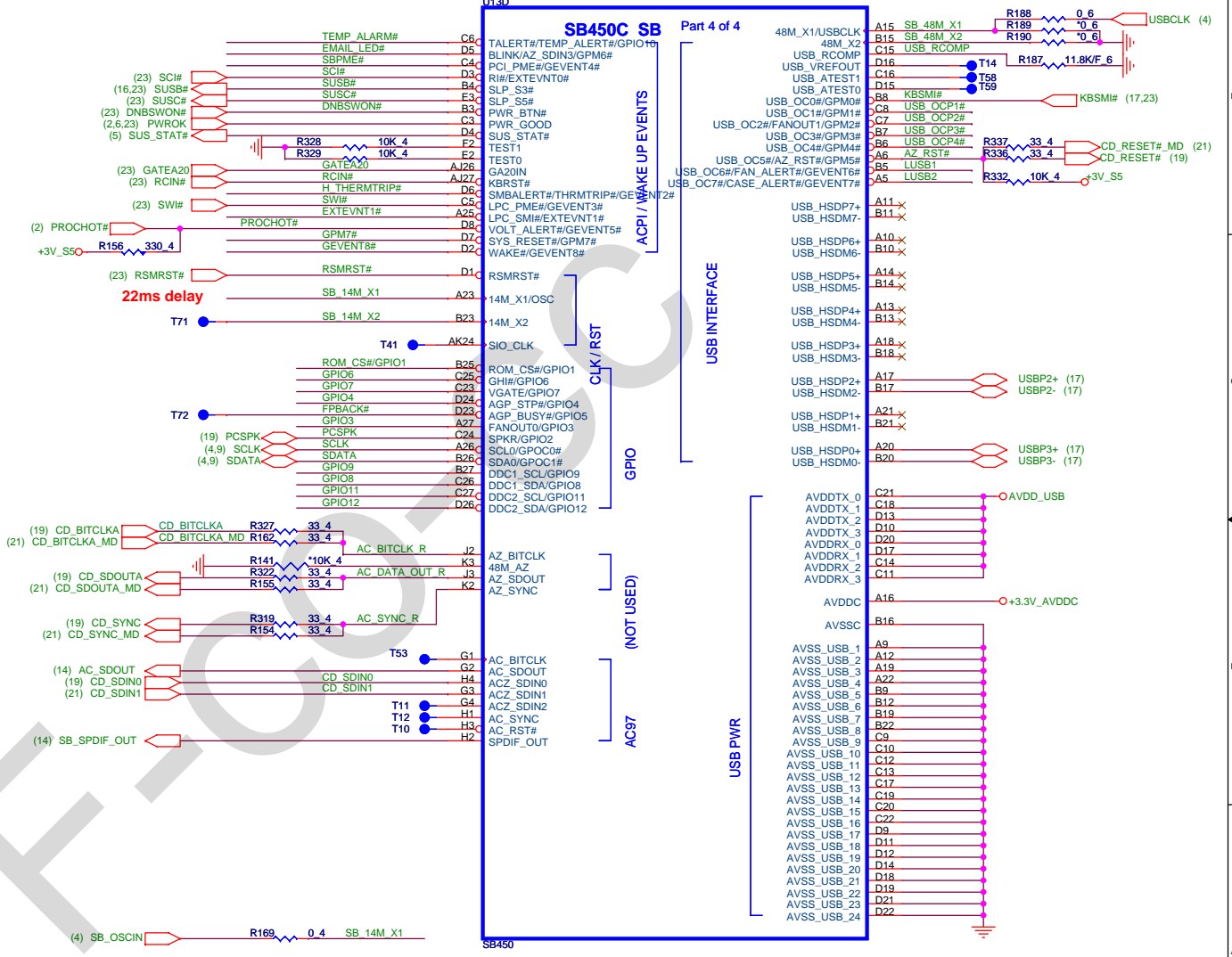
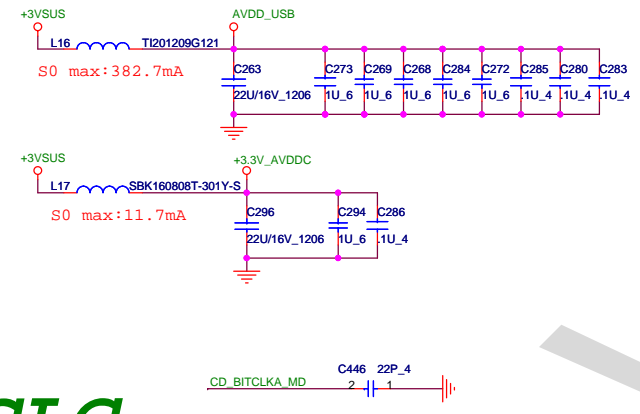
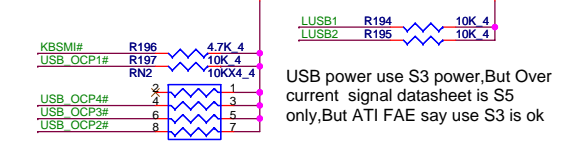


4/02 Option W/O CRT GPIO9(R410) to High.  
4/02 Option(Normal) CRT GPIO9(R172) to Low.



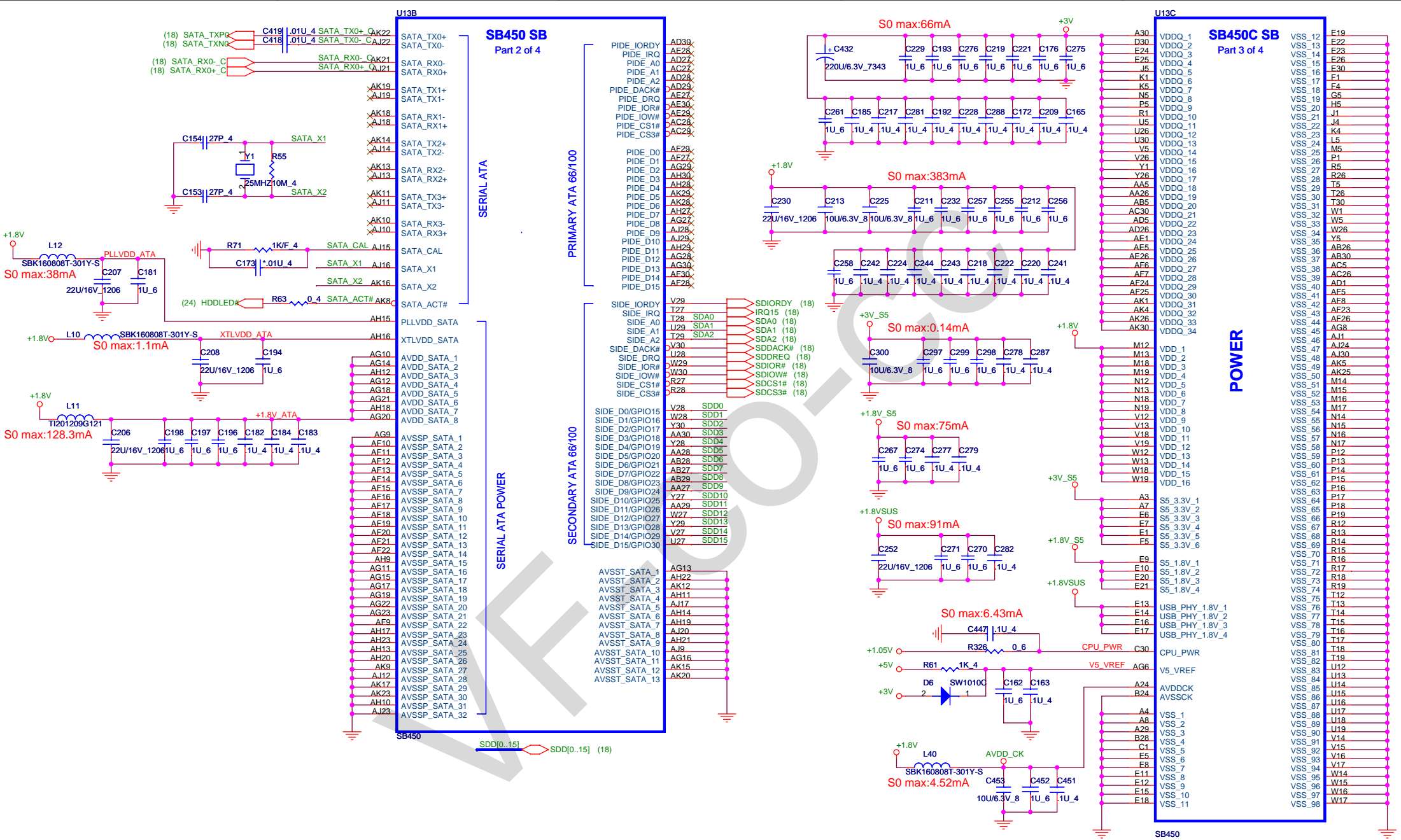
	GPIO9 PIN	GPIO8 PIN
CRT	LOW	
W/O CRT	HIGH	
Modem		LOW
W/O Modem		HIGH

**USB power**



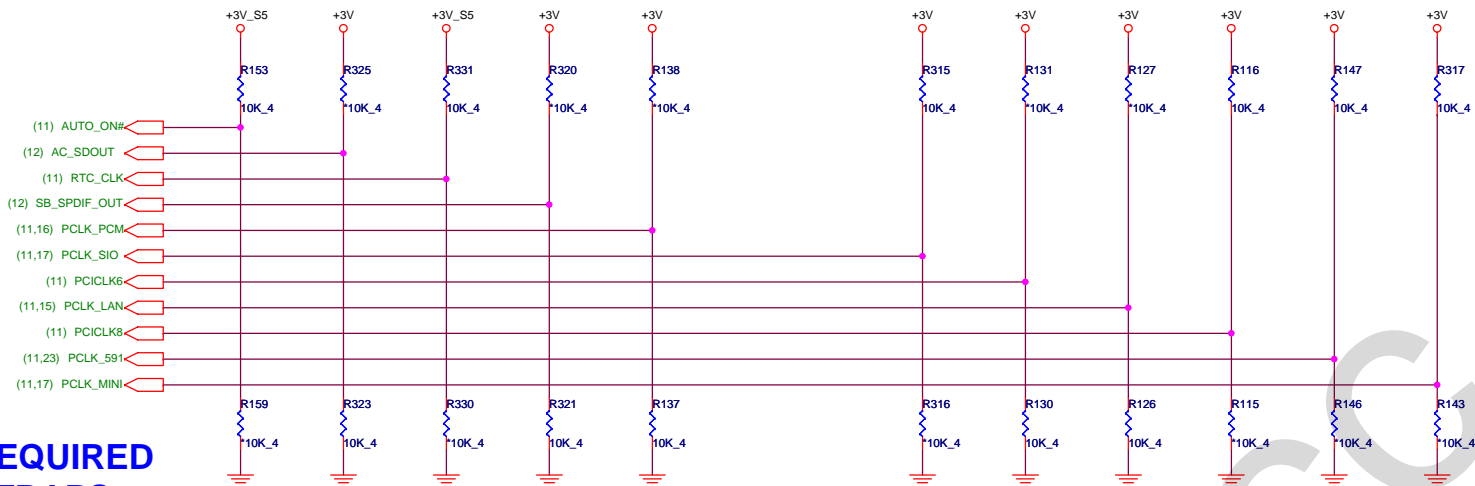
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>SB450C ACPI/GPIO/USB/AC97</b>	3A
Date:	Monday, May 08, 2006	Sheet 12 of 30



**PROJECT : BL1**  
**Quanta Computer Inc.**

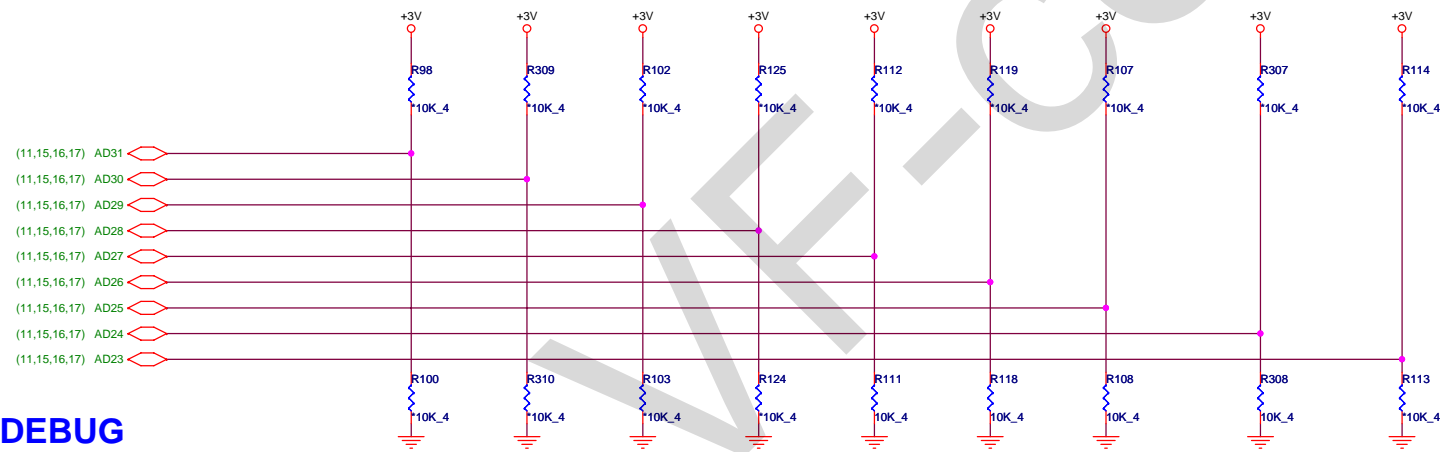
Size	Document Number	Rev
Custom	<b>SB450C HDD/POWER/DECOUPLING</b>	1A
Date:	Monday, May 08, 2006	Sheet 13 of 30



## REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI*
<b>PULL HIGH</b>	MANUAL PWR ON <b>DEFAULT</b>	USE DEBUG STRAPS	INTERNAL RTC <b>DEFAULT</b>	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE	CPU I/F = K8	H,H = PCI(X BUS) ROM L,H = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE <b>DEFAULT</b>	48MHz Crystal Pad <b>DEFAULT</b>
<b>PULL LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS <b>DEFAULT</b>	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz <b>DEFAULT</b>	48MHz use External Clock <b>DEFAULT</b>	14MHz XTAL MODE	CPU I/F = P4 <b>DEFAULT</b>	L,H = LPC ROM II (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz OSC/Clock Buffer

\*This strap is only required if the strap on PCICLK4 is configured for External Clock.



## DEBUG STRAPS

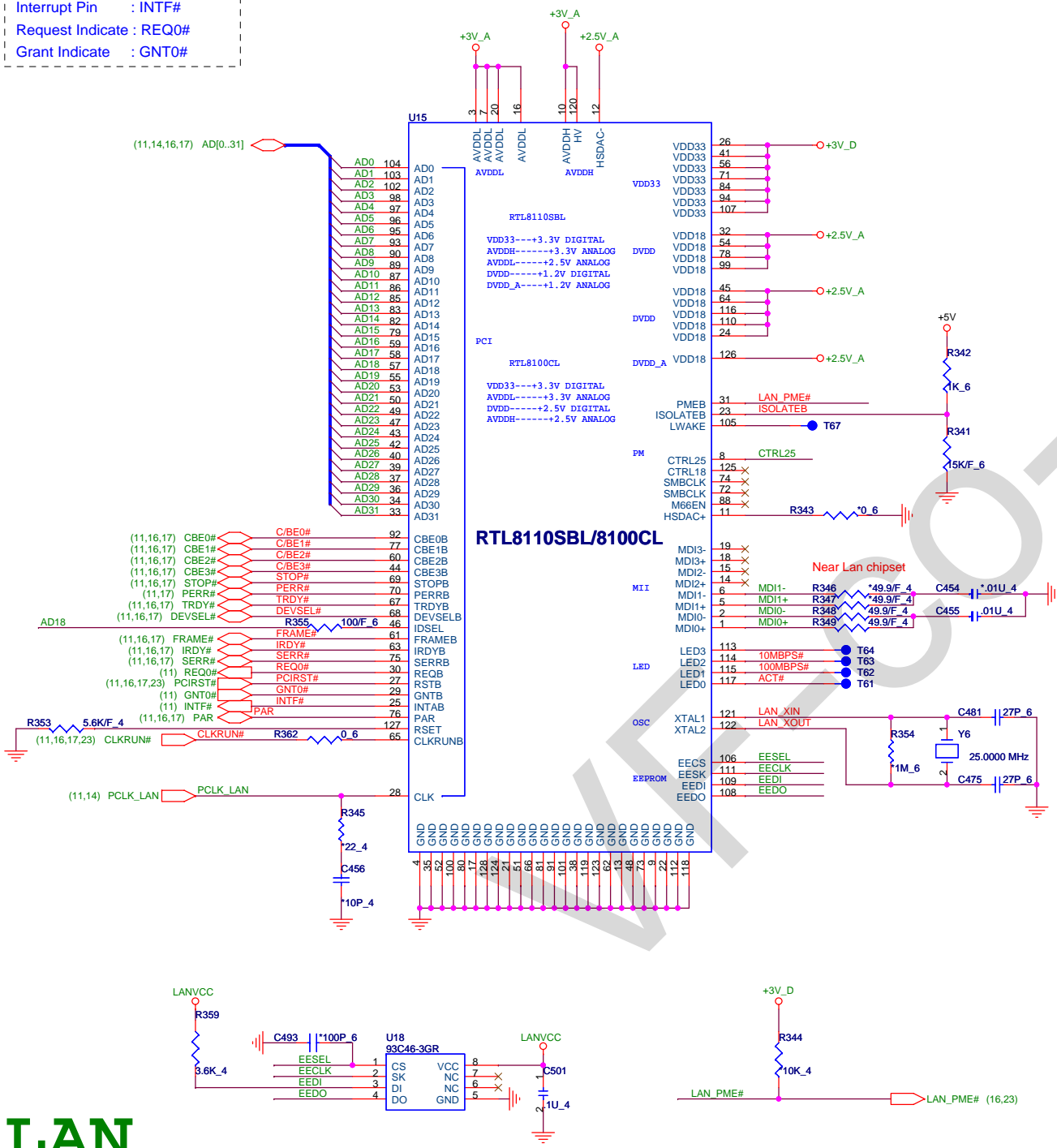
	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET <b>DEFAULT</b>	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
<b>PULL LOW</b>	USE SHORT RESET					USE PCI PLL <b>DEFAULT</b>	USE ACPI BCLK <b>DEFAULT</b>	USE IDE PLL <b>DEFAULT</b>	USE DEFAULT PCIE STRAPS <b>DEFAULT</b>	



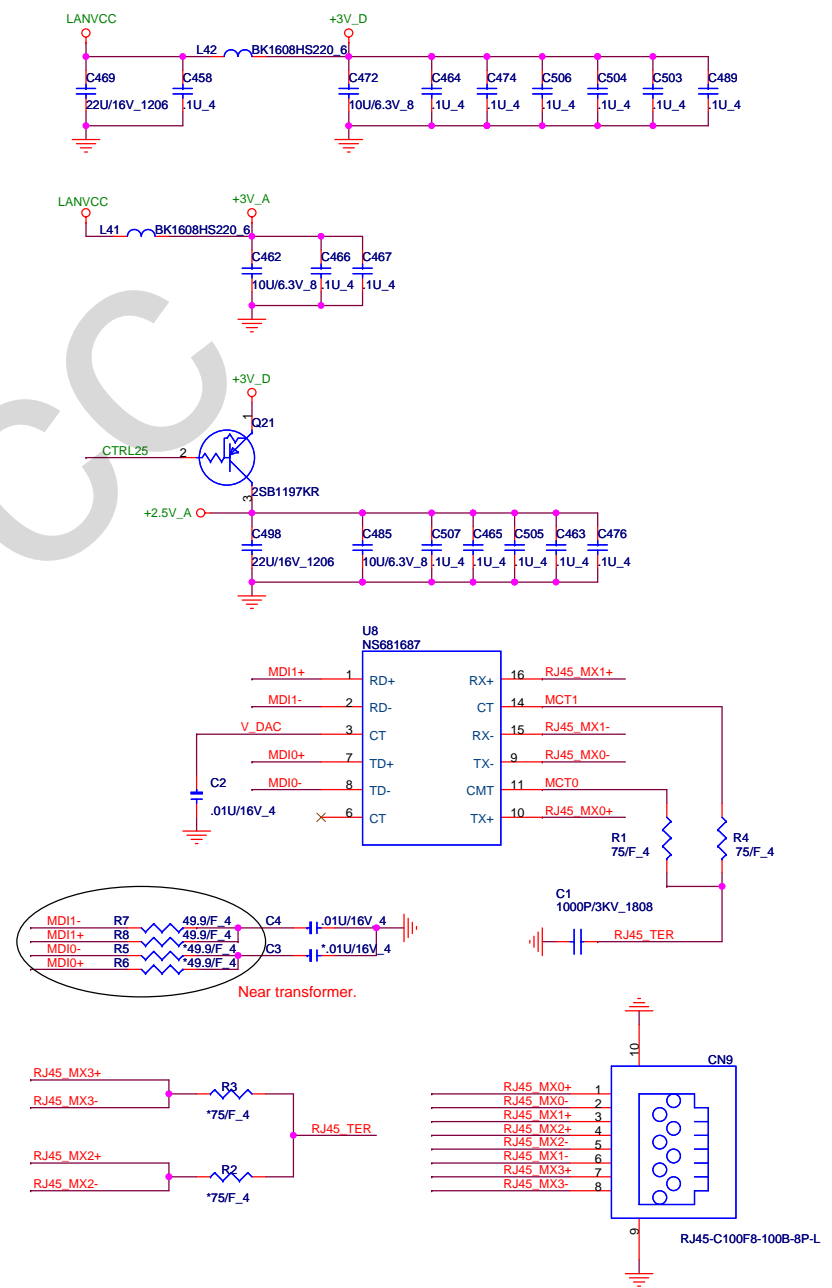
PROJECT : BL1  
**Quanta Computer Inc.**

Size Custom	Document Number SB450C STRAPS	Rev 1A
Date: Monday, April 03, 2006	Sheet 14 of 30	

ID Select : AD18  
 Interrupt Pin : INTF#  
 Request Indicate : REQ0#  
 Grant Indicate : GNT0#



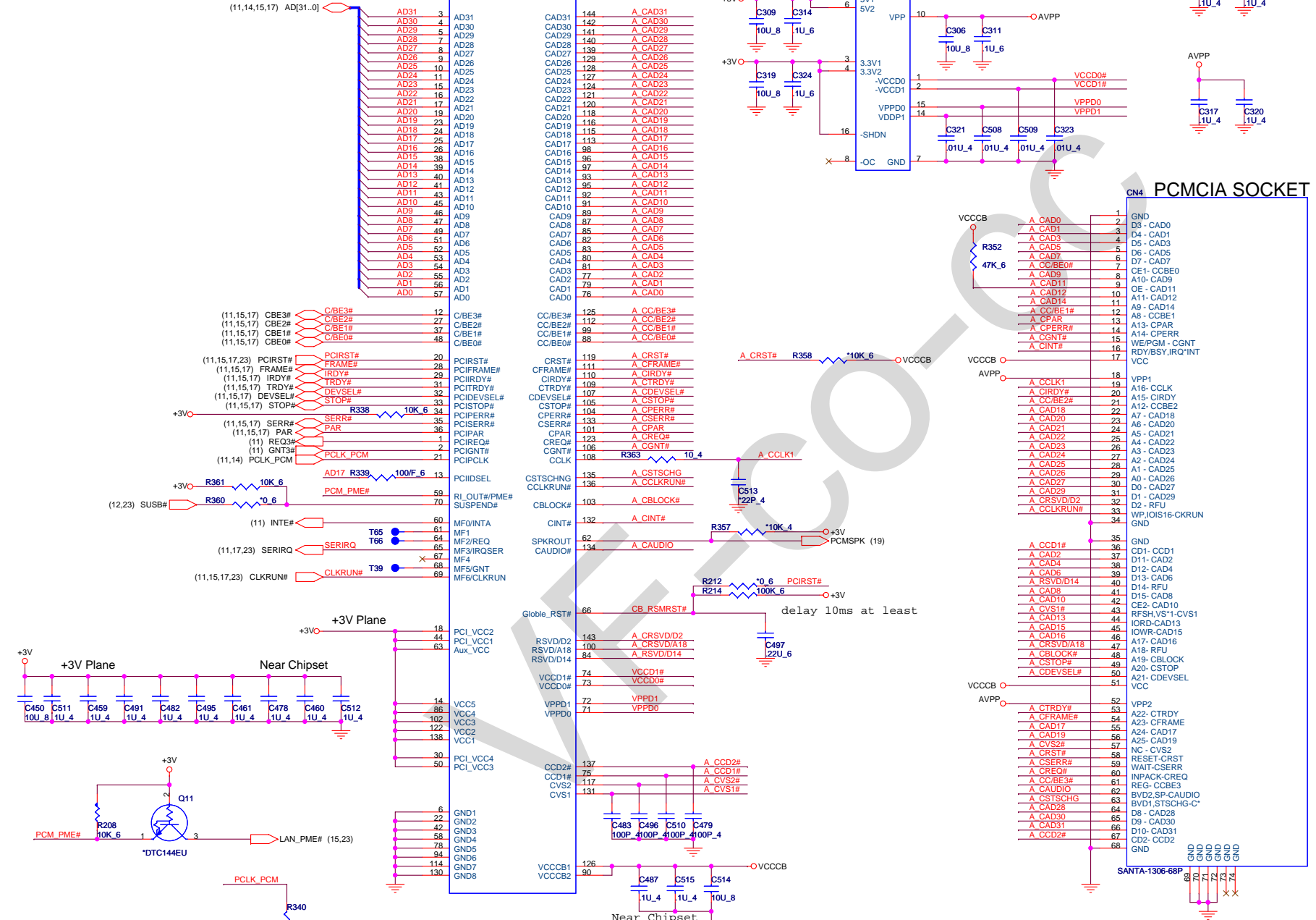
**LAN**



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>LAN RTL8110SBL/8100CL</b>	1A
Date:	Saturday, May 06, 2006	Sheet 15 of 30

ID Select : AD17  
 Interrupt Pin : INTE#  
 Request Indicate : REQ3#  
 Grant Indicate : GNT3#



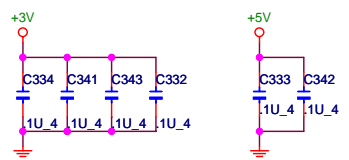
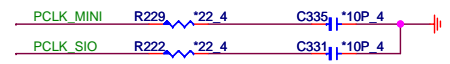
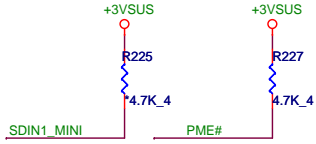
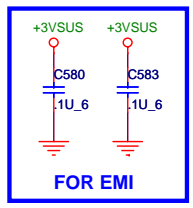
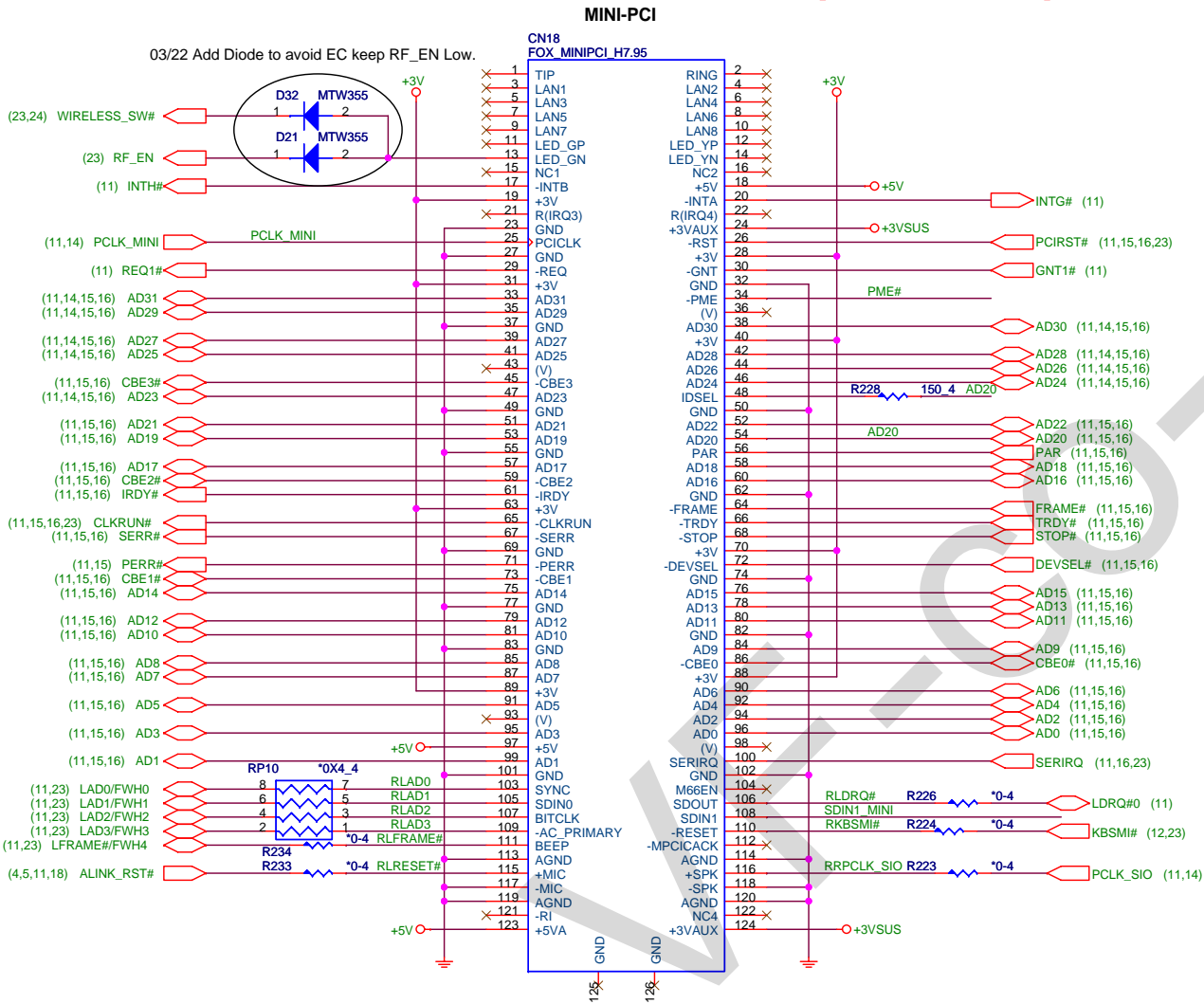
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size Document Number  
**PCMCIA(CB1410)-OPTION**

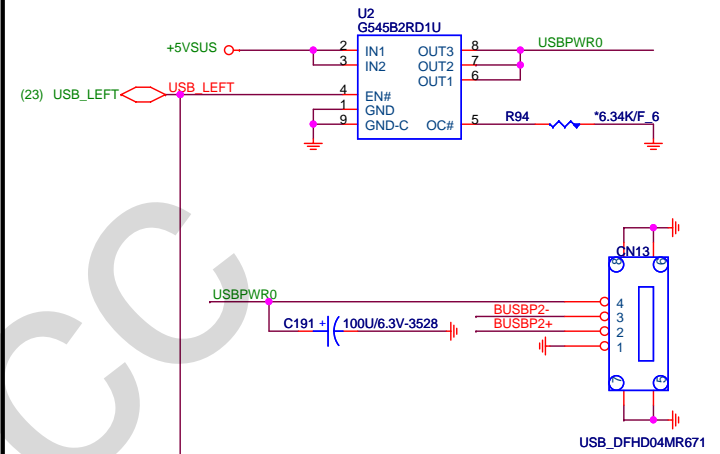
Date: Friday, April 28, 2006 Sheet 16 of 30 Rev 1A



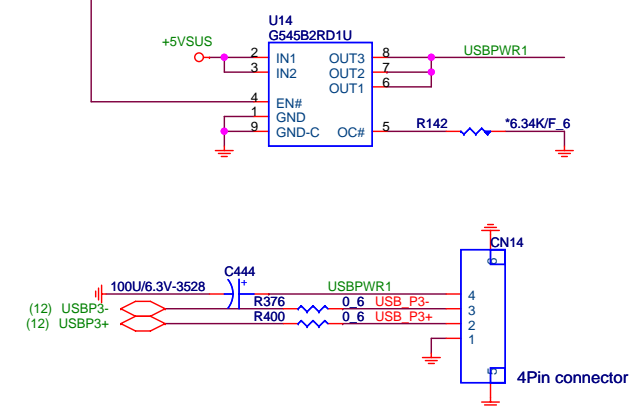
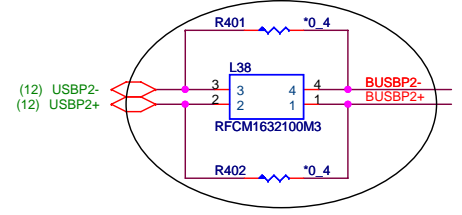
ID Select : AD20  
 Interrupt Pin : INTG# , INTH#  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#



# USB



02/24 Add 0ohm jumper

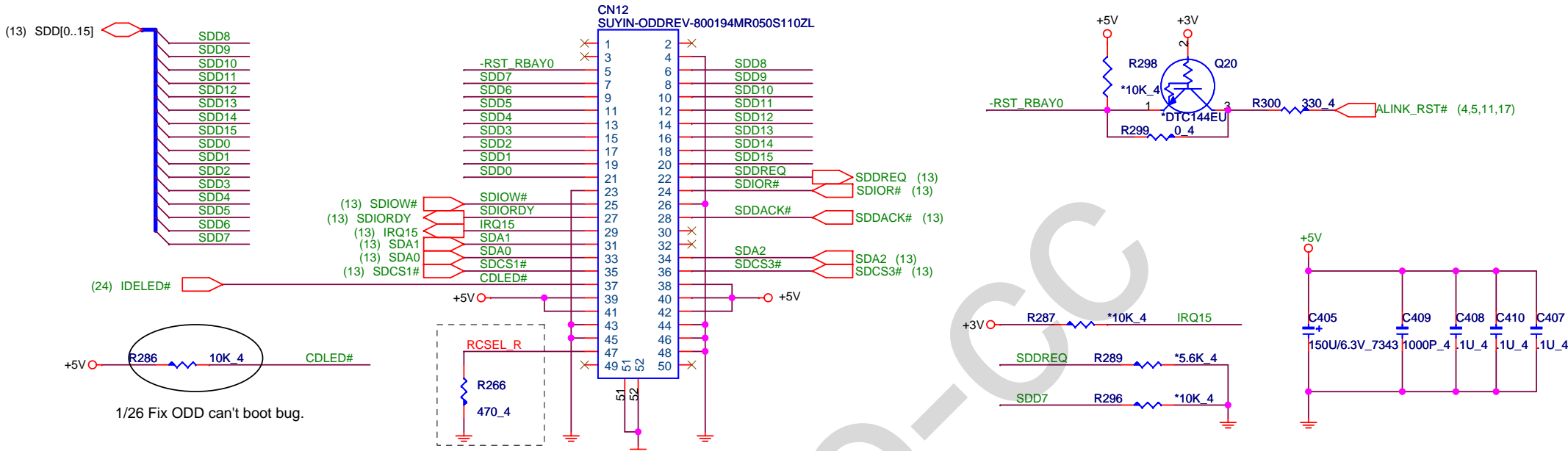


04/28 Del Reserved the Second USB Port.

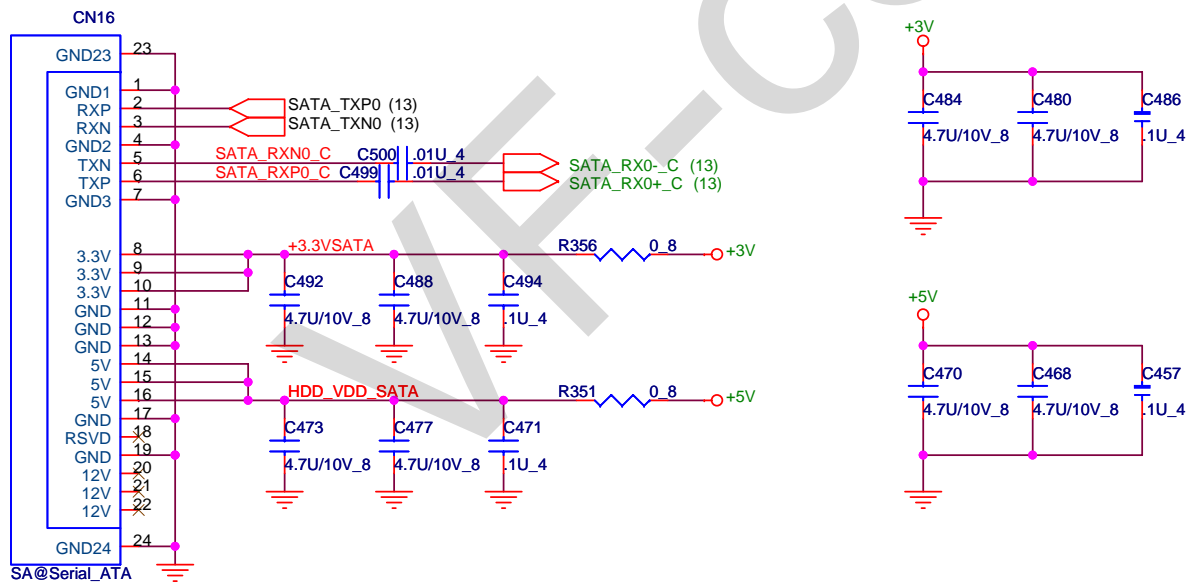


PROJECT : BL1  
 Quanta Computer Inc.

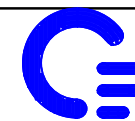
# ODD CONN



# SATA HDD CONN



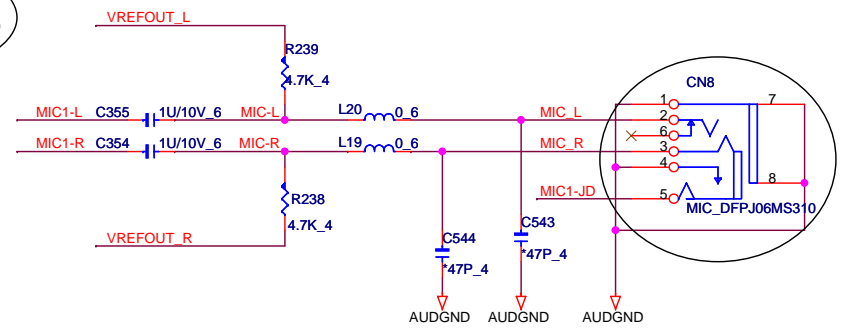
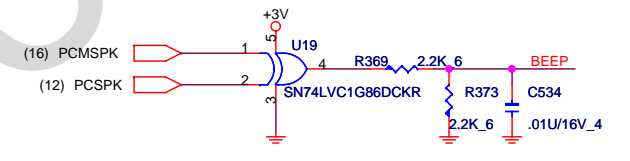
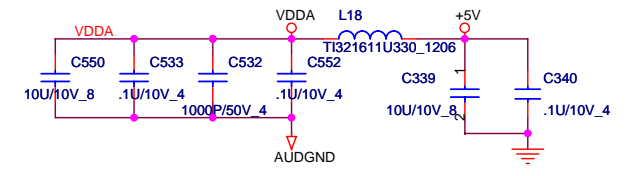
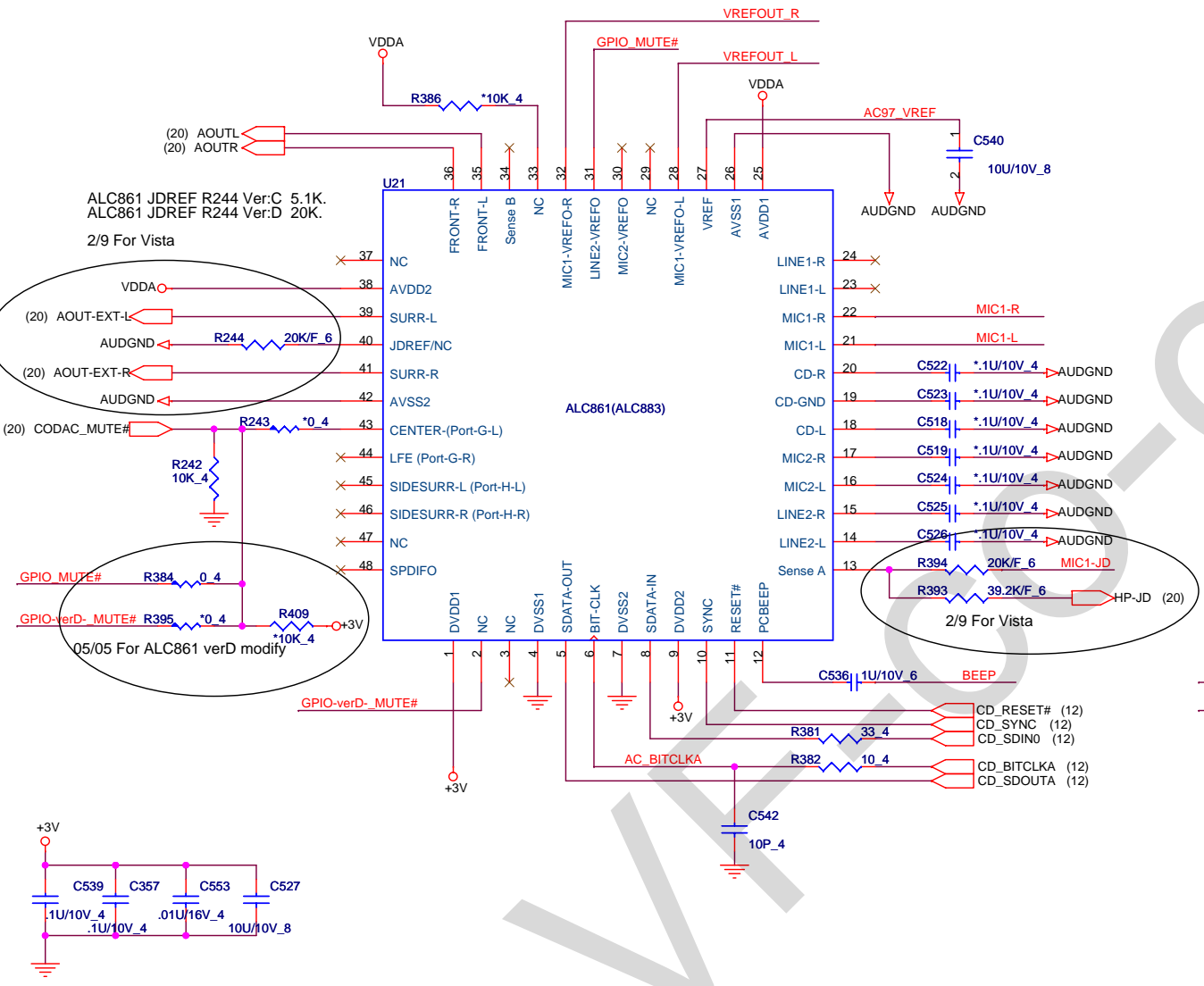
**IDE**



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>HDD &amp; CDROM</b>	2A
Date:	Monday, May 08, 2006	Sheet 18 of 30

ADO



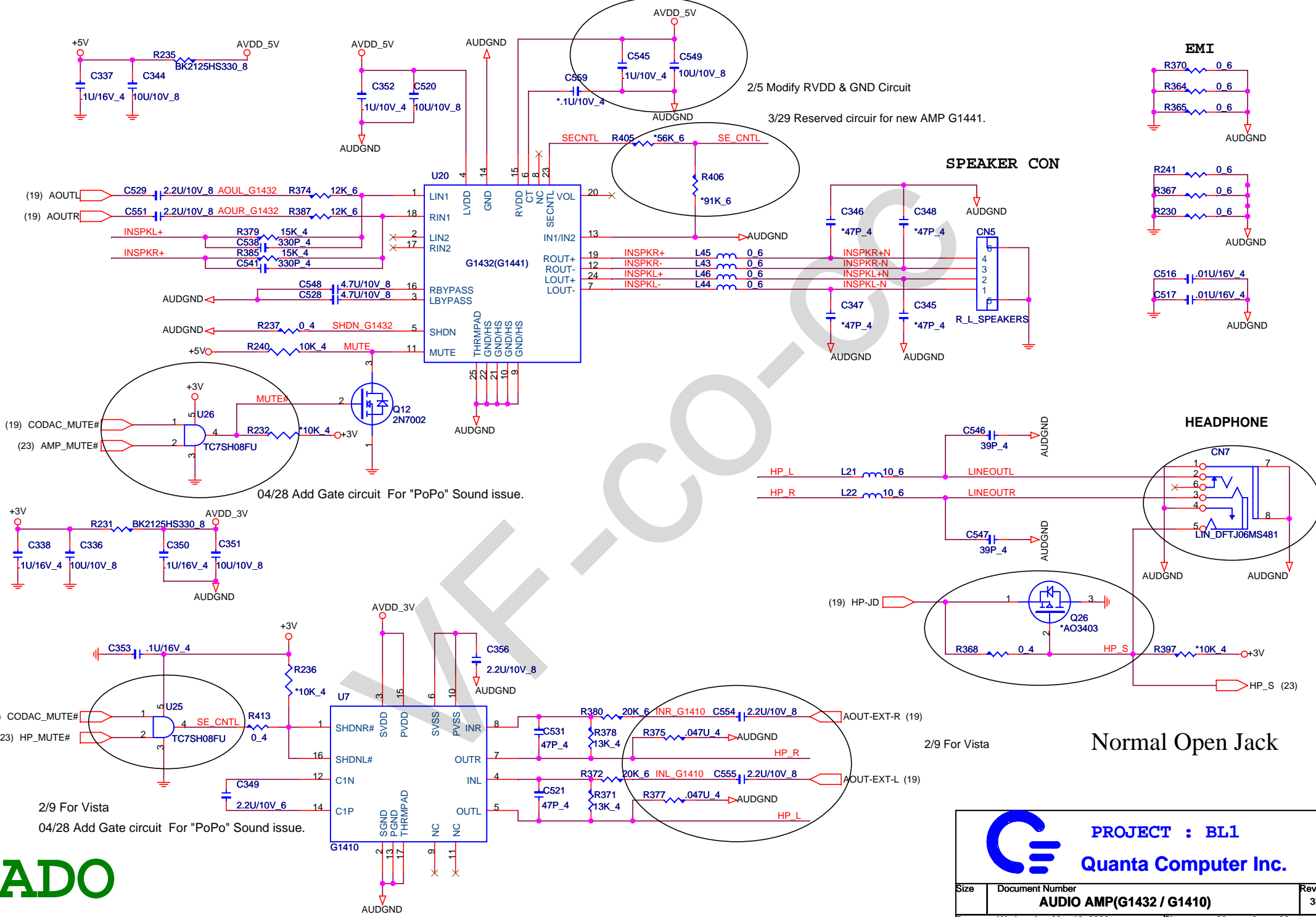
Normal Open Jack




PROJECT : BL1  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>REALTEK ALC861</b>	2A

Date: Friday, May 05, 2006 Sheet 19 of 30



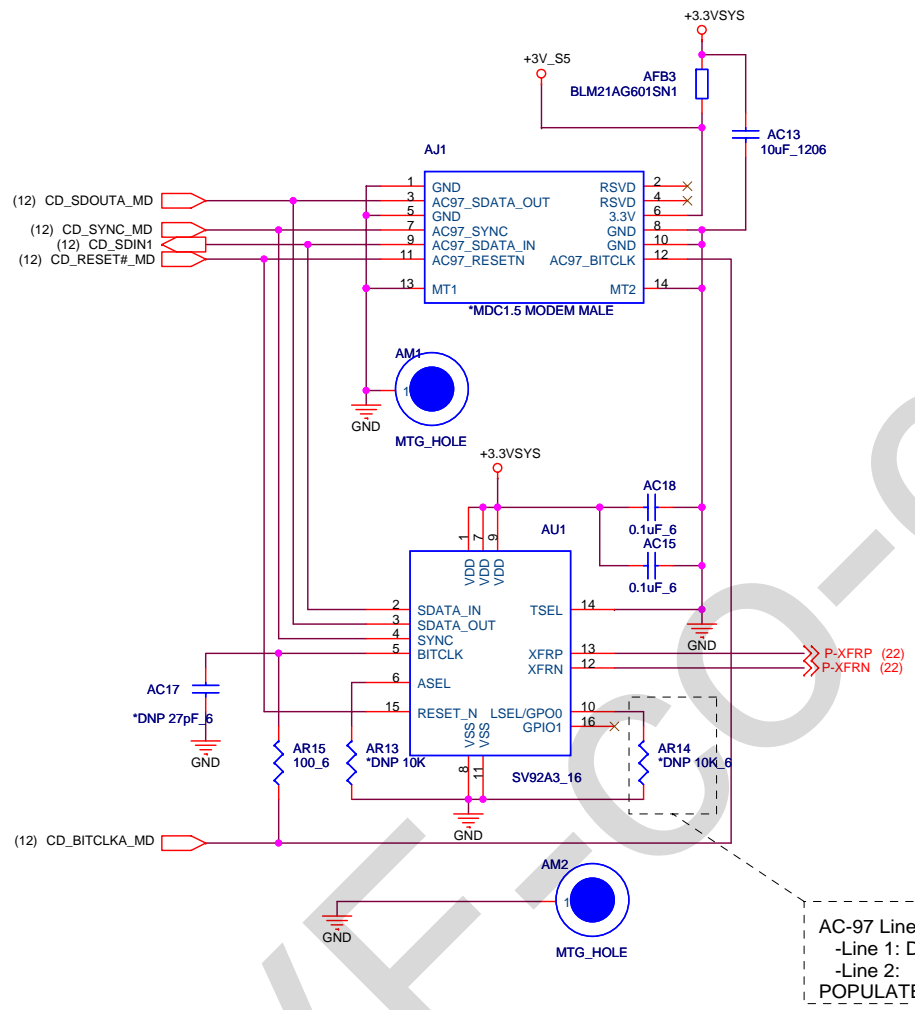
**ADO**



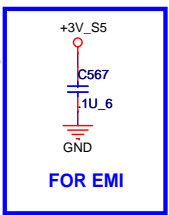
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AUDIO AMP(G1432 / G1410)</b>	<b>3B</b>
Date:	Wednesday, May 10, 2006	Sheet 20 of 30

**MDM**



AC-97 Line Select:  
 -Line 1: DNP R14  
 -Line 2:  
 POPULATE R14



**Agere Systems**  
 Holmdel NJ

**Design Engineer: C. Russo**

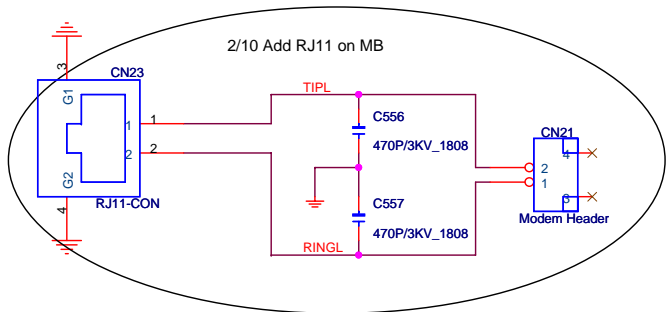
**agere systems**

Title: **DELPHI SV92A3 MDC 1.5 Reference Design**

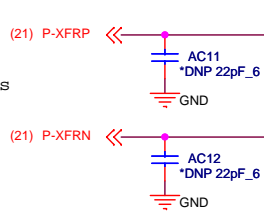
Size: B	Document Number: <b>DIGITAL INTERFACE</b>	Rev: 1A
Date: Friday, April 28, 2006	Sheet: 21	of 30

Agere Systems Proprietary  
 DRAFT COPY - FOR REVIEW ONLY  
 SUBJECT TO CHANGE





Locate C11, C12 as close to digital device as possible.

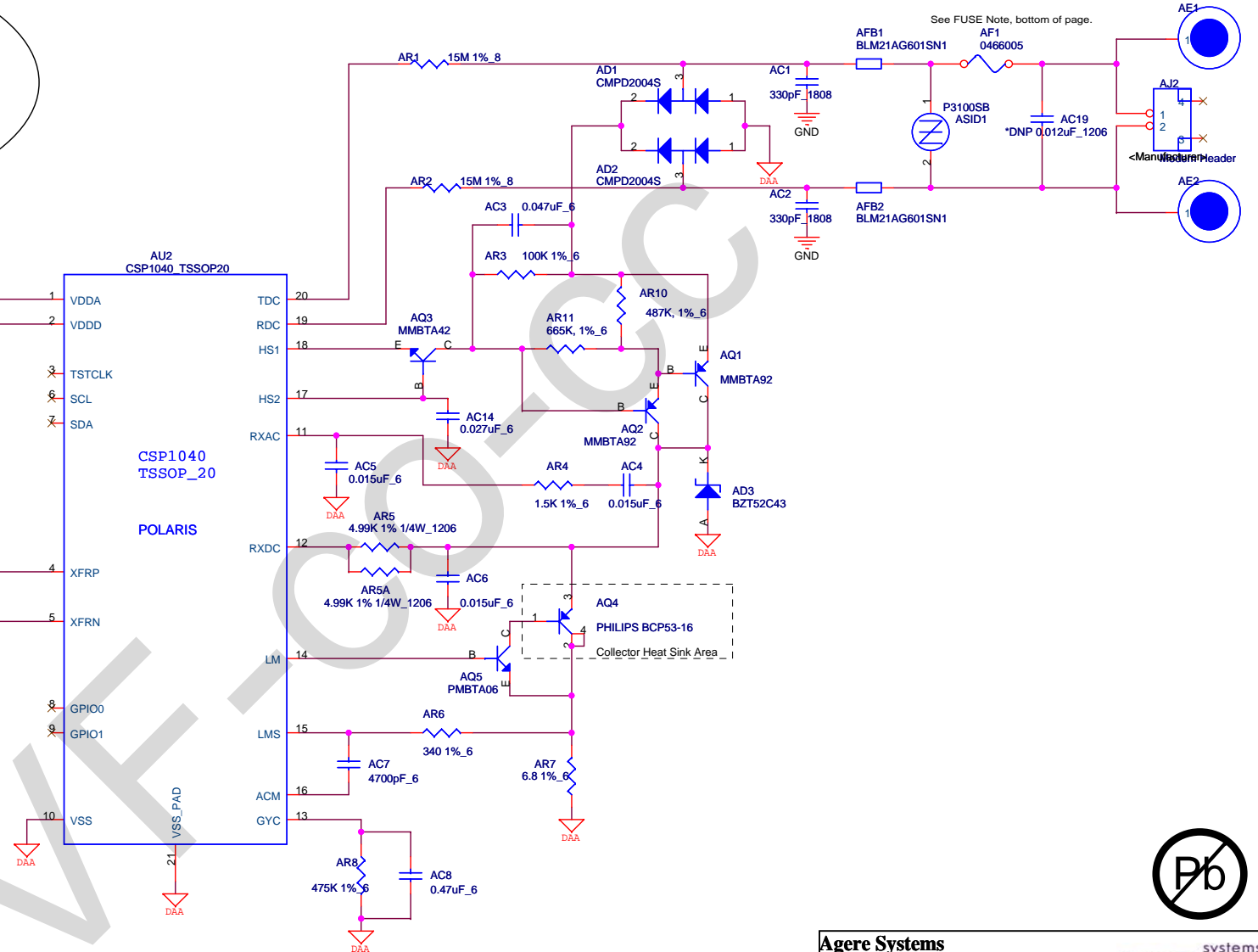


# MDM

## FUSE Note:

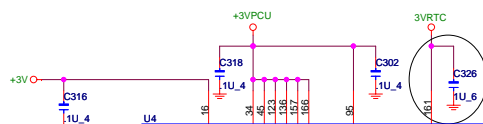
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



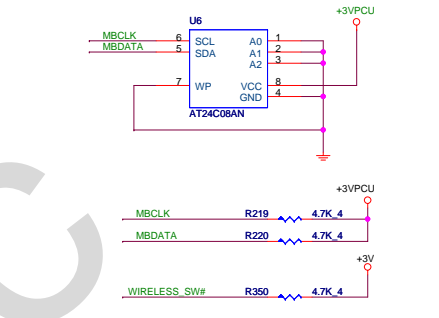
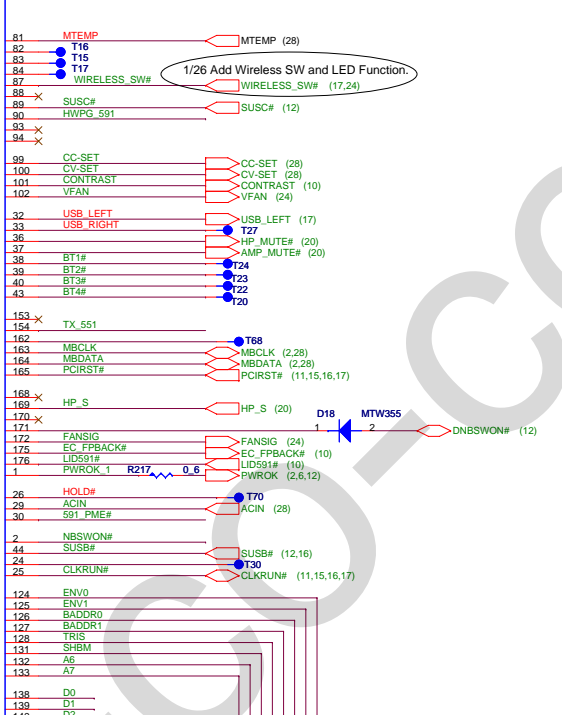
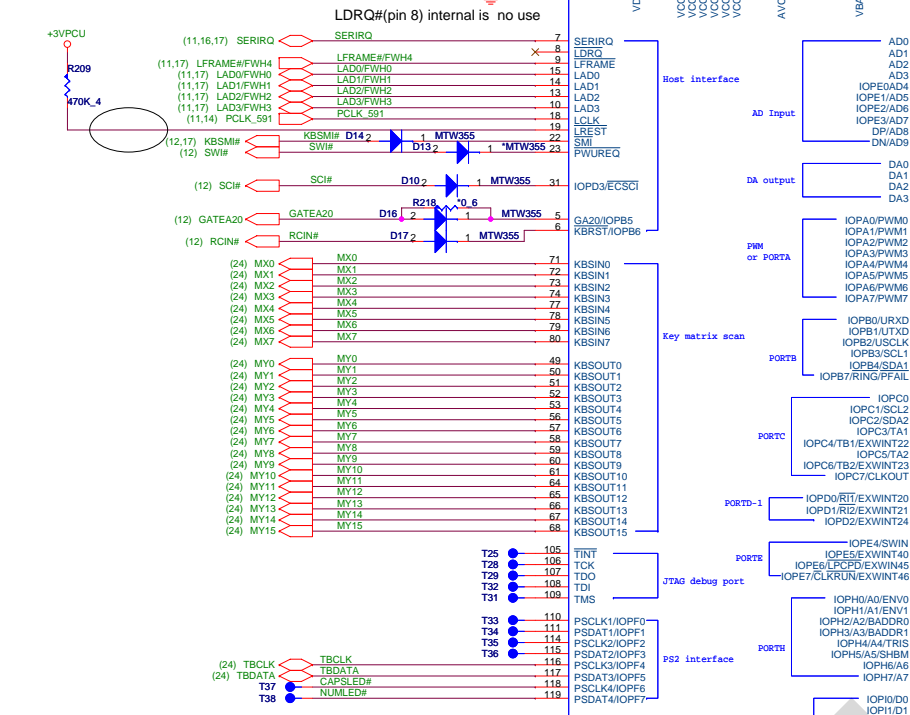
<b>Agere Systems</b> Holmdel NJ		
Design Engineer: <b>R. Trevino</b>		
Title <b>DELPHI SV92A3 MDC 1.5 Reference Design</b>		
Size B	Document Number <b>CSP1040 DAA</b>	Rev 2A
Date:	Saturday, May 06, 2006	Sheet 22 of 30

Agere Systems Proprietary  
 DRAFT COPY - FOR REVIEW ONLY  
 SUBJECT TO CHANGE

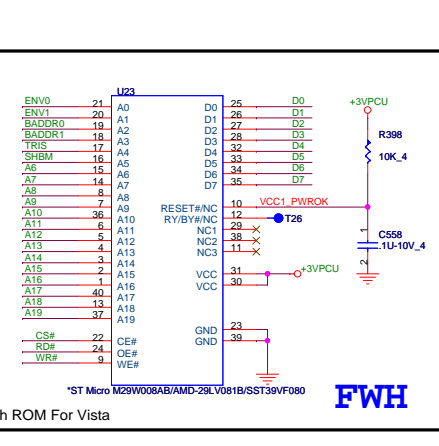
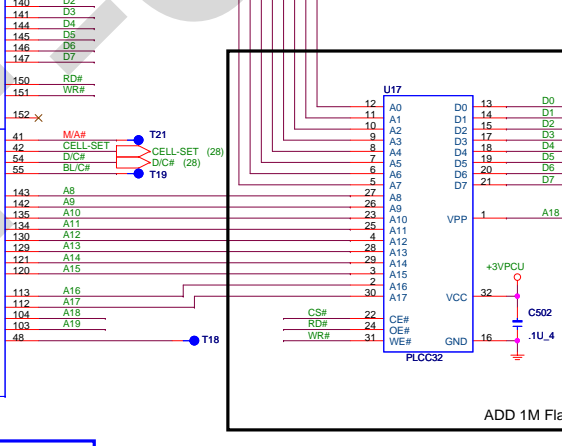
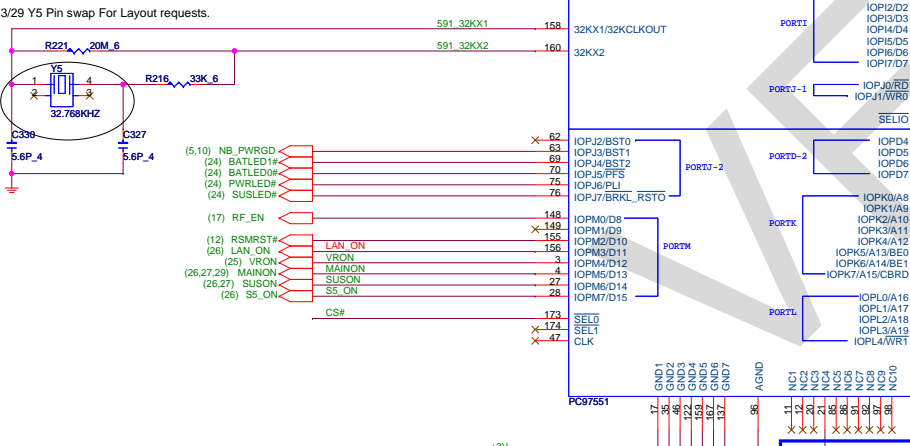
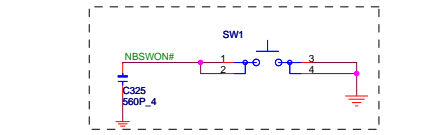
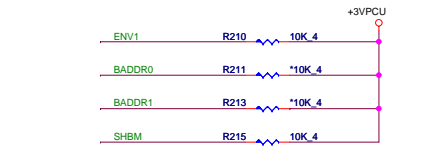


SRBM=1: Enable shared memory with host BIOS

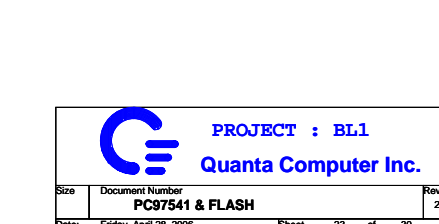
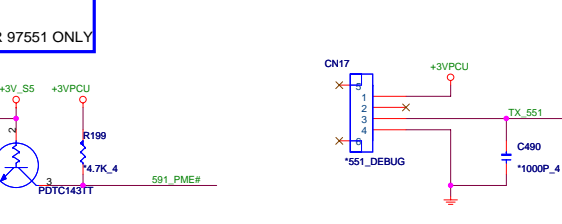
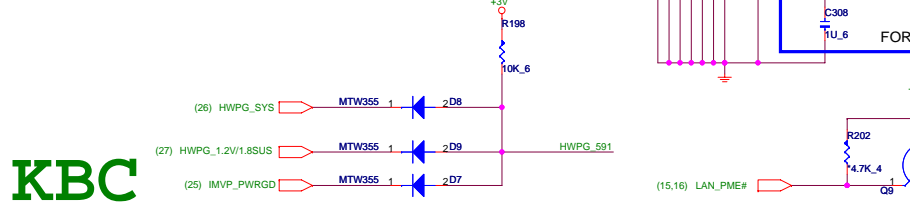
BADDR1-0	Index	Data
0 0	3F	3F
0 1	4E	4F
1 0	[HC]PCBAH, [HC]PCBAL	[HC]PCBAH, [HC]PCBAL+1
1 1	Reserved	



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

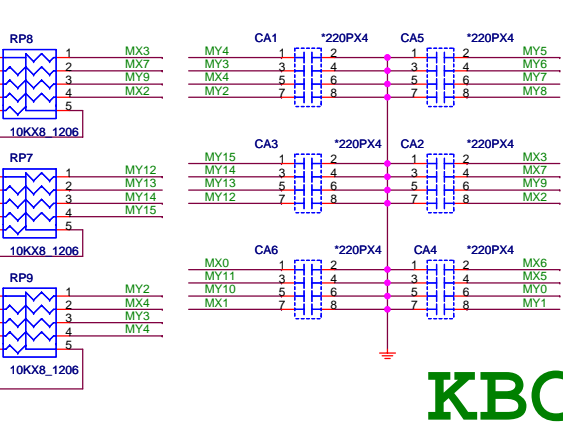
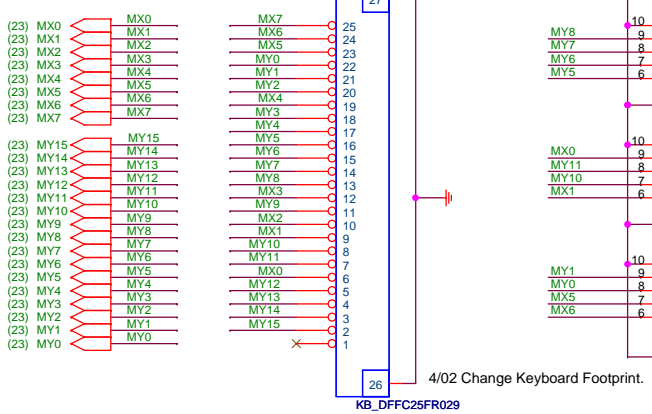


\*ST Micro M29W008AB/AMD-29LV081B/ST939VF080  
ADD 1M Flash ROM For Vista



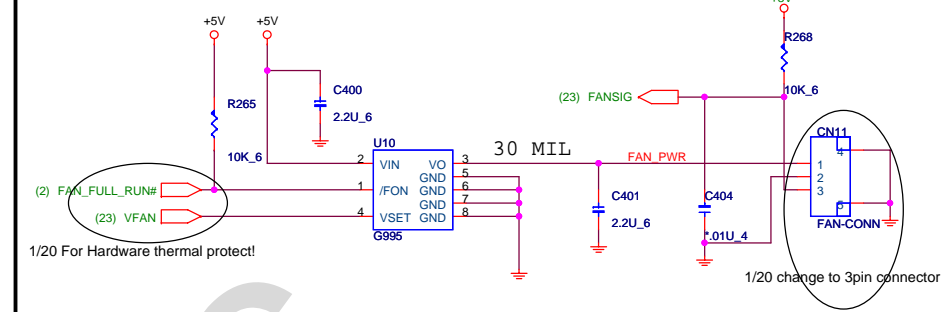
**PROJECT : BL1**  
**Quanta Computer Inc.**

**INT K/B**



**KBC**

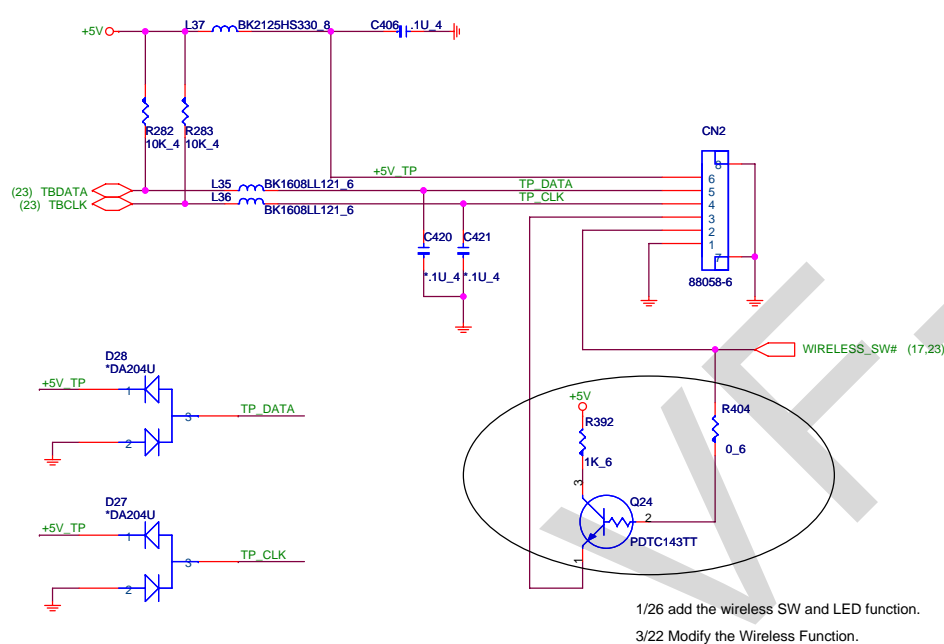
**FAN CONTROL**



**THM**

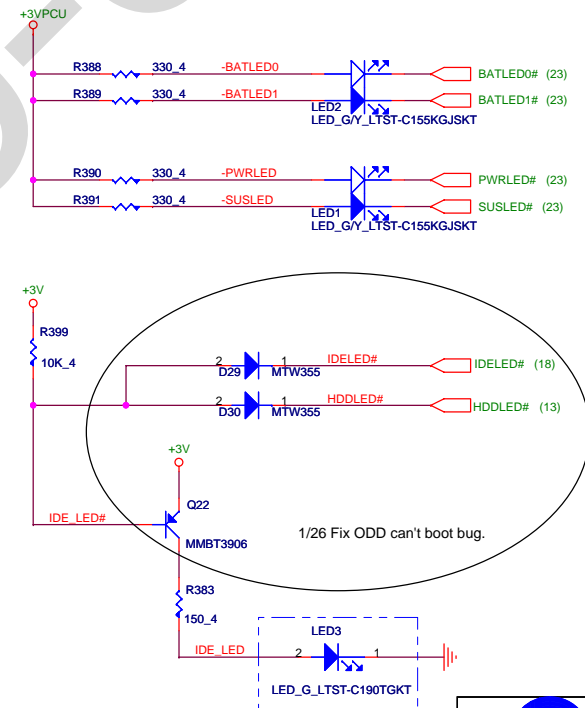
**TOUCH PAD**

20 MIL



**TPD**

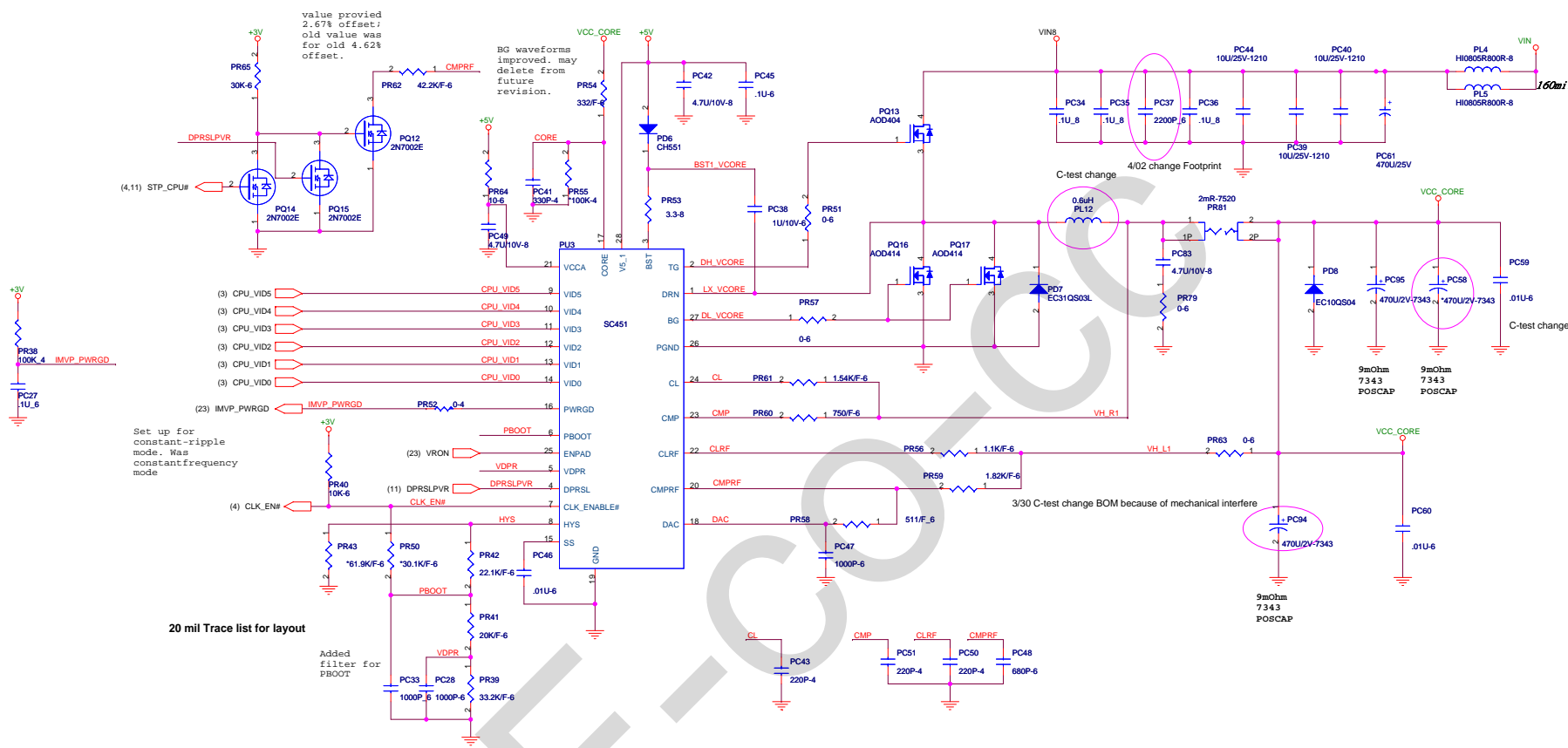
**ON BOARD LED**



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>T/P,FAN,SWITCH,LED,K/B</b>	3A
Date:	Friday, May 05, 2006	Sheet 24 of 30





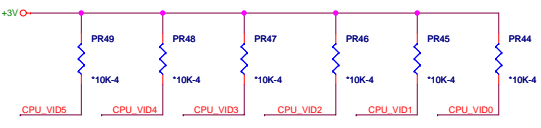
V I D							Vaore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	1	0	1	1	1	1.340	
0	1	1	1	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	1	0	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	

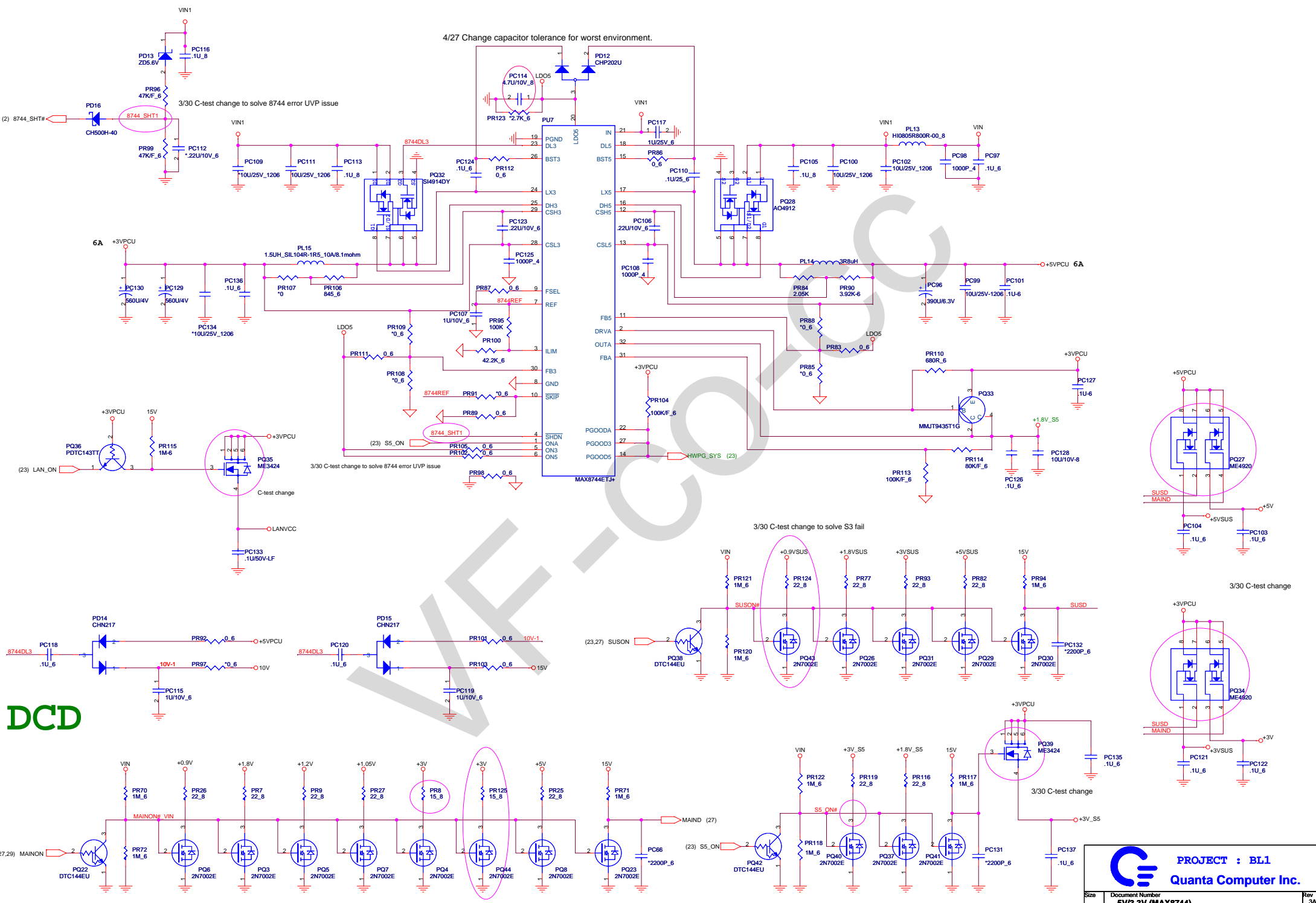
100 mil Trace list for layout

- DH\_VCORE
- LX\_VCORE
- DL\_VCORE
- DH\_VCORE2
- LX\_VCORE2
- DL\_VCORE2

30 mil Trace list for layout


- SC1476
- pin 4
- pin 5
- pin 7
- pin 25
- pin 30



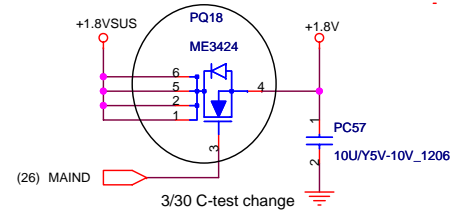
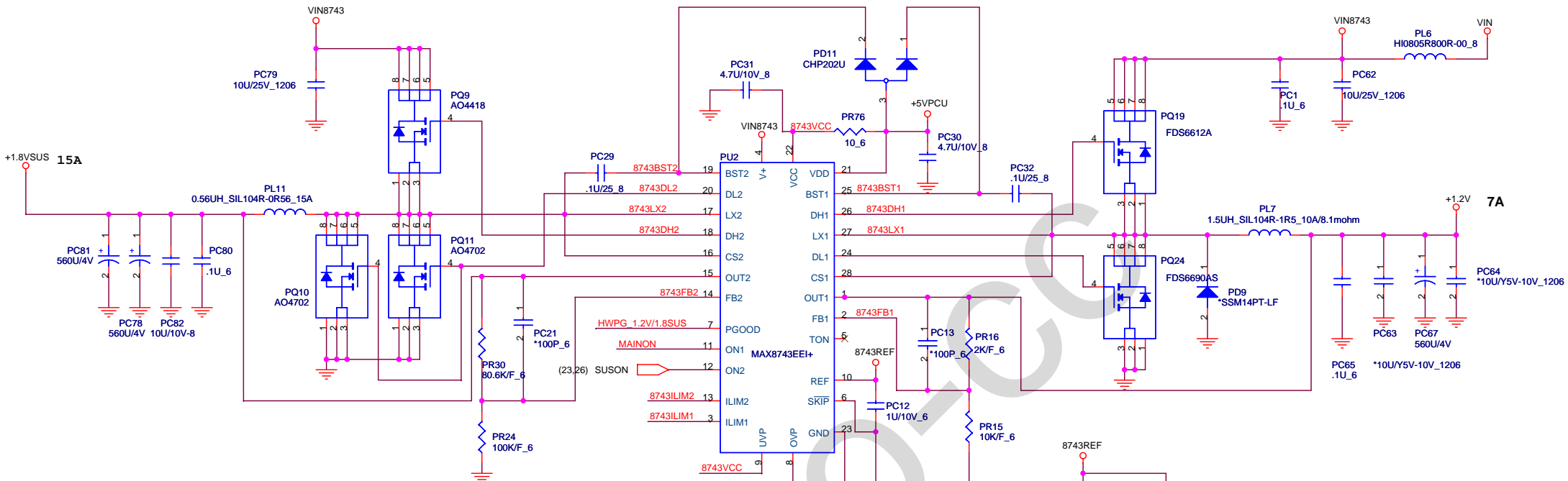


# DCD

3/30 C-test change to speed up +3V discharge time

 <b>PROJECT : BL1</b> <b>Quanta Computer Inc.</b>		Size	Rev
		Document Number	3A
<b>5V/3.3V (MAX8744)</b>		Date:	Tuesday, May 09, 2006
Sheet 26 of 30			

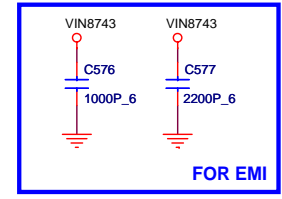
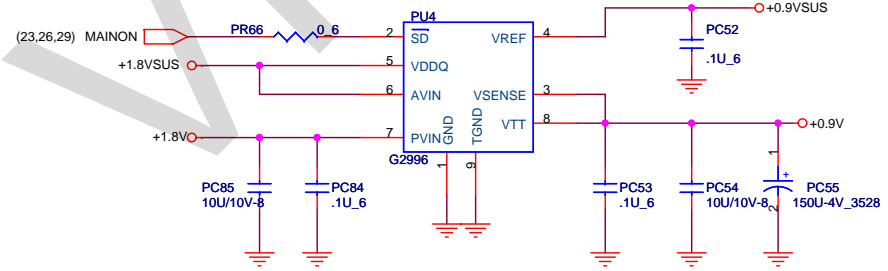
+1.8VSUS 15A



(23) HWPG\_1.2V/1.8SUS

AO4704 Rds on = 13mOhm  
 ILOAD \* Rds on \* 10 = ILIM  
 ILIM2 = 1.235V Current limit 9.5A  
 ILIM1 = 0.91V Current limit 7A

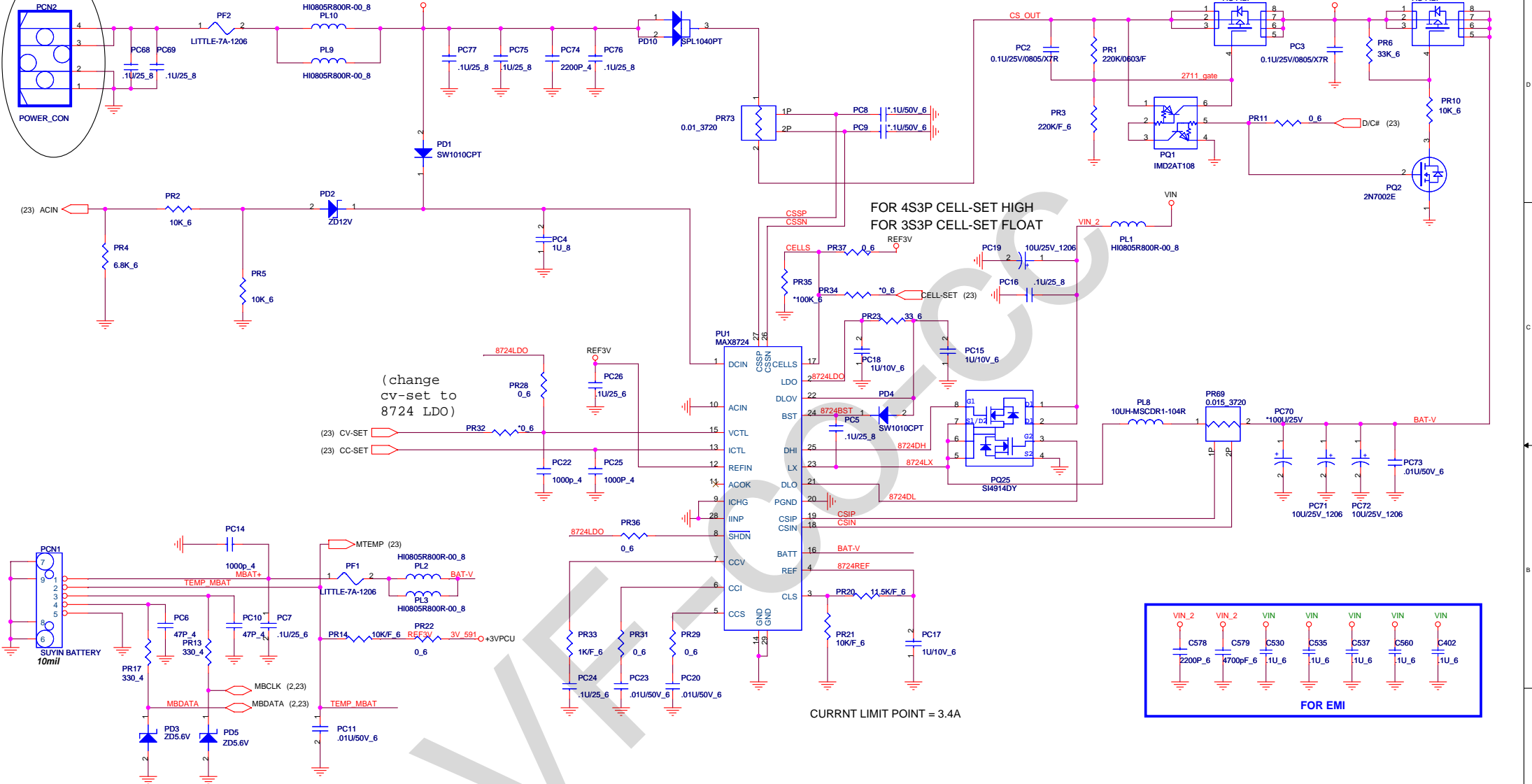
DCD



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>+1.8/1.2V / VTT</b>	1A
Date:	Friday, April 28, 2006	Sheet 27 of 30

2/10 Modify Pin define

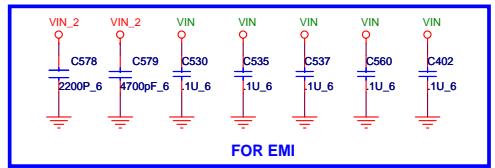


# DCD

SMBus SLAVE ADDRESS: 16

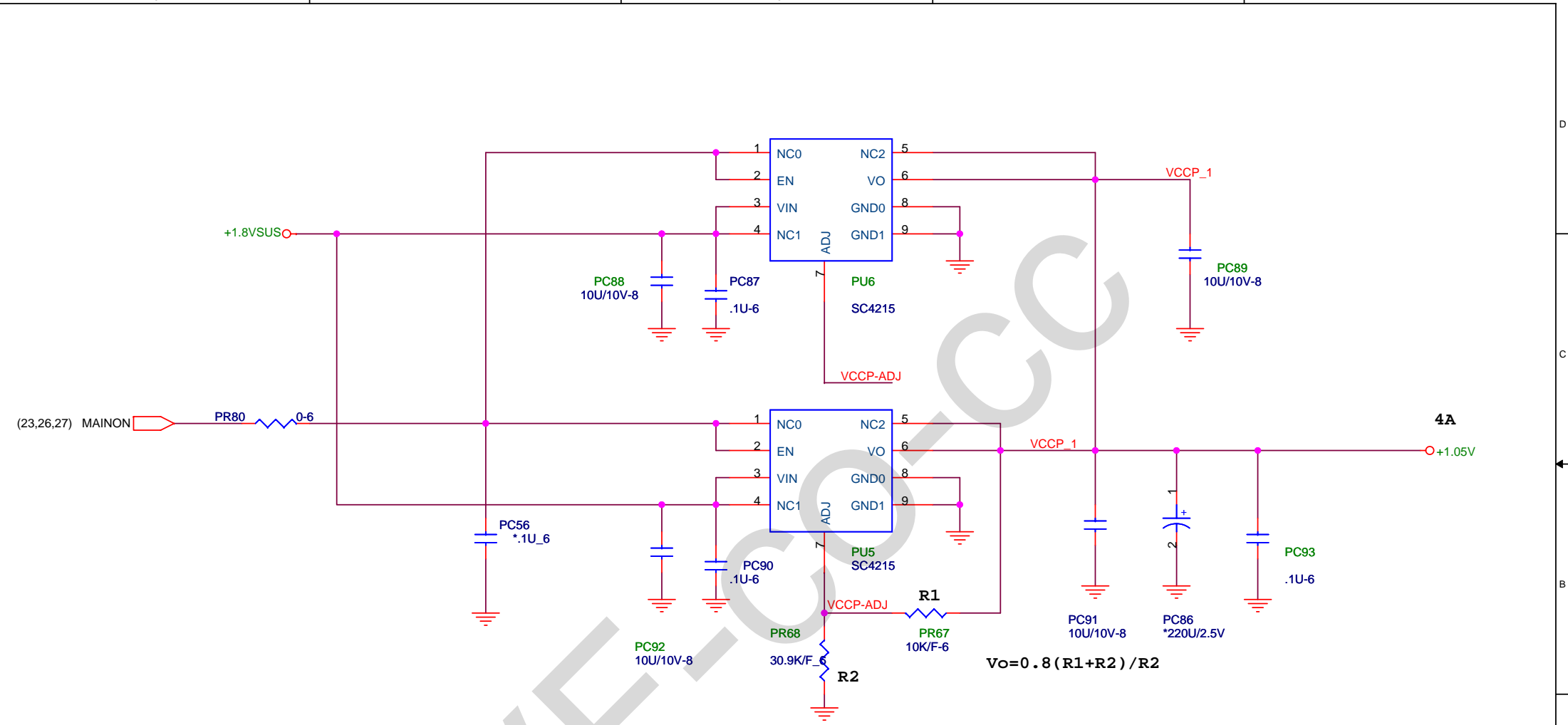
FOR 4S3P CELL-SET HIGH  
FOR 3S3P CELL-SET FLOAT

CURRNT LIMIT POINT = 3.4A




**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	BATTERY CHARGER	2A
Date:	Friday, April 28, 2006	Sheet 28 of 30



DCD

VFW

		PROJECT : BL1	
		Quanta Computer Inc.	
Size	Document Number		Rev
	<b>+1.05V</b>		1A
Date:	Friday, April 28, 2006	Sheet	29 of 30