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Suzhou_UL

CPU : Intel Penryn
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

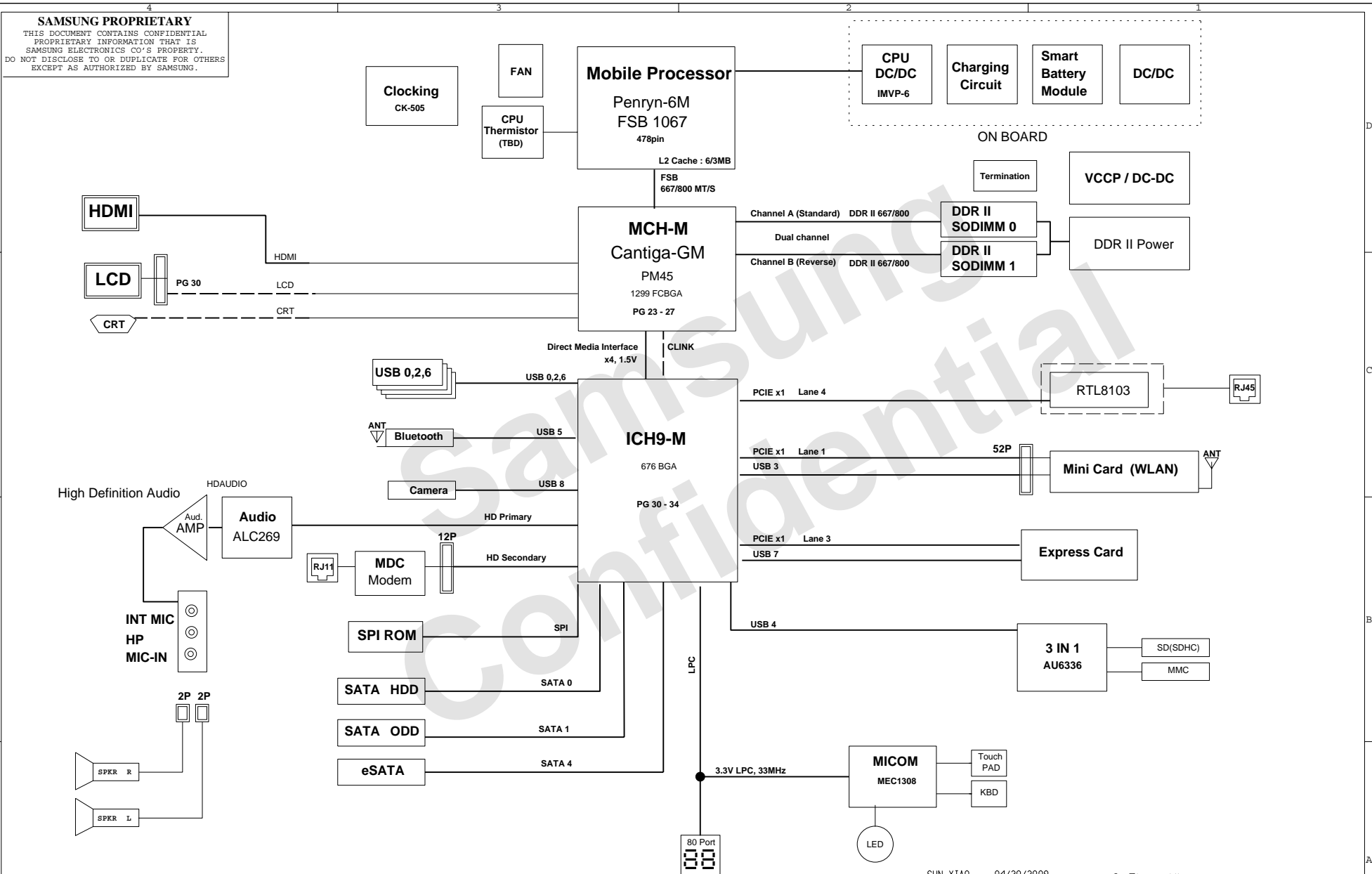
Model Name : Suzhou_UL_DDR3
 PCB Code : GCE BA41-01213A
 : NAN BA41-01212A
 : HAN BA41-01214A

Dev. Step : P R
 Revision : 1.0
 T.R. Date : 2009.09.12

DESIGN	CHECK	APPROVAL

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0	COVER		PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	1	OF 51

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DESIGN	SUN XIAO,	04/30/2009	TITLE	Suzhou_UL
CHECK	WU SHIJIANG,	04/30/2009	DATE	Suzhou_UL
APPROVAL	WU SHIJIANG,	PR	REV	1.0
MODULE CODE	BC LEE,	REV	1.0	November 25, 2009 15:50:02 PM
			LAST EDIT	November 25, 2009 15:50:02 PM

SAMSUNG
 ELECTRONICS
 PART NO. BA41-01213A
 REV. 2
 BA41-01213A

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHC1) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Panel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

(This table will be update.)

REVISION HISTORY

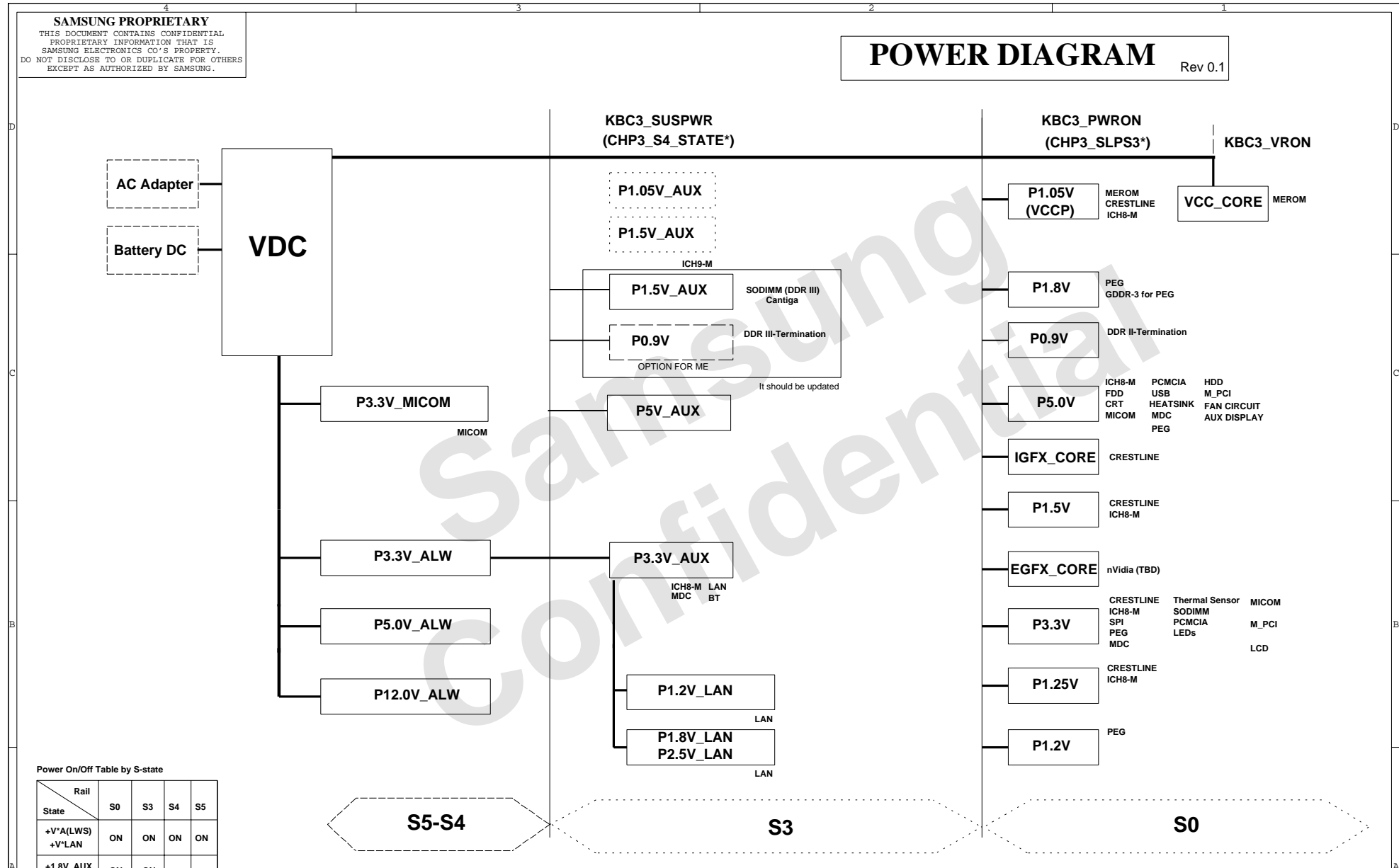
See rev notes for more information.

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		BCAFDINFO	PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	3	OF 51

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POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

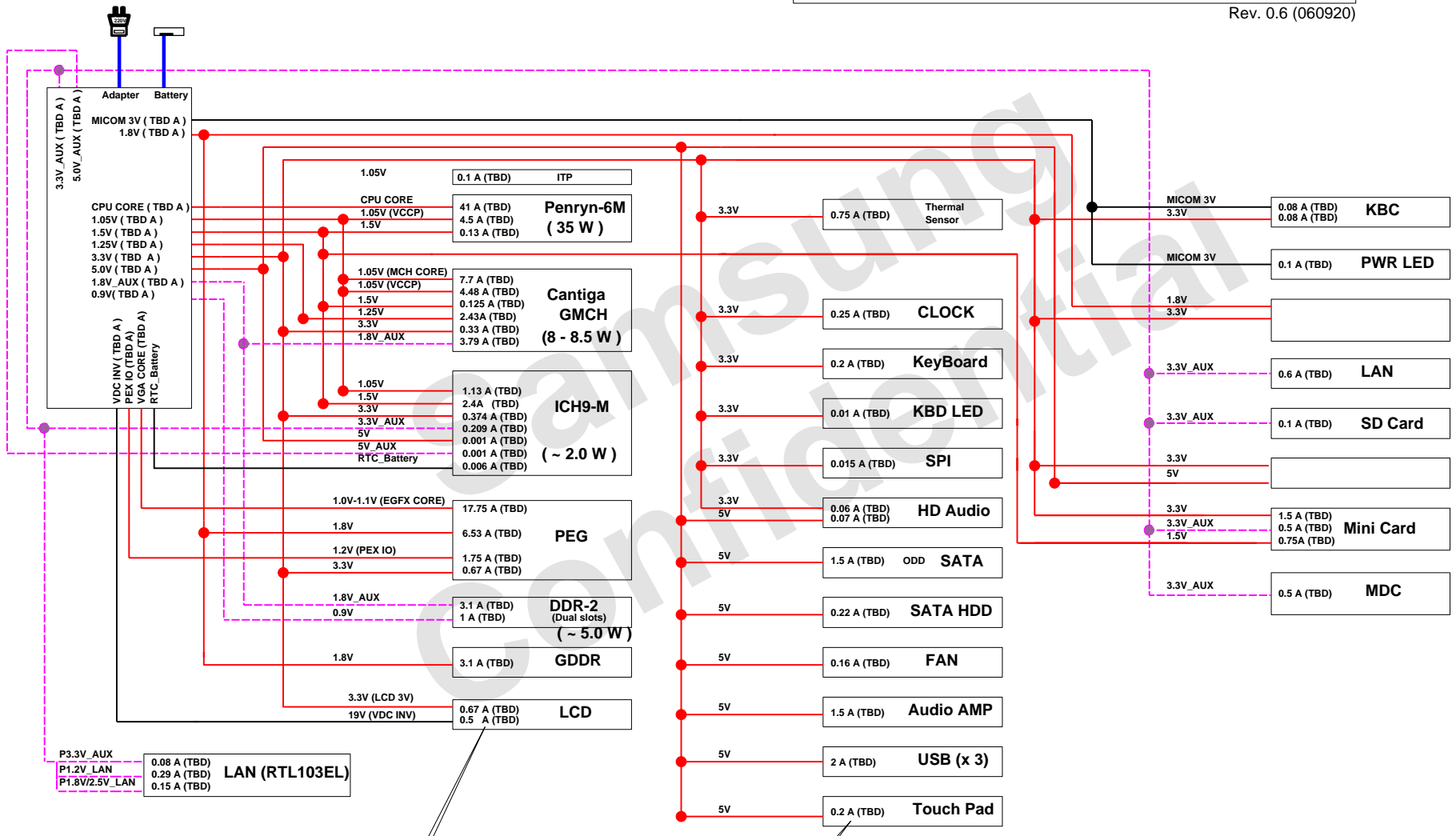
Rail	S0	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	---	---
+V*AUX	ON	ON	---	---
+V	ON	---	---	---
+V* (CORE)	ON	---	---	---

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		POWER DIAGRAM	PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	4	OF 51

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	POWER RAILS	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	5	OF 51

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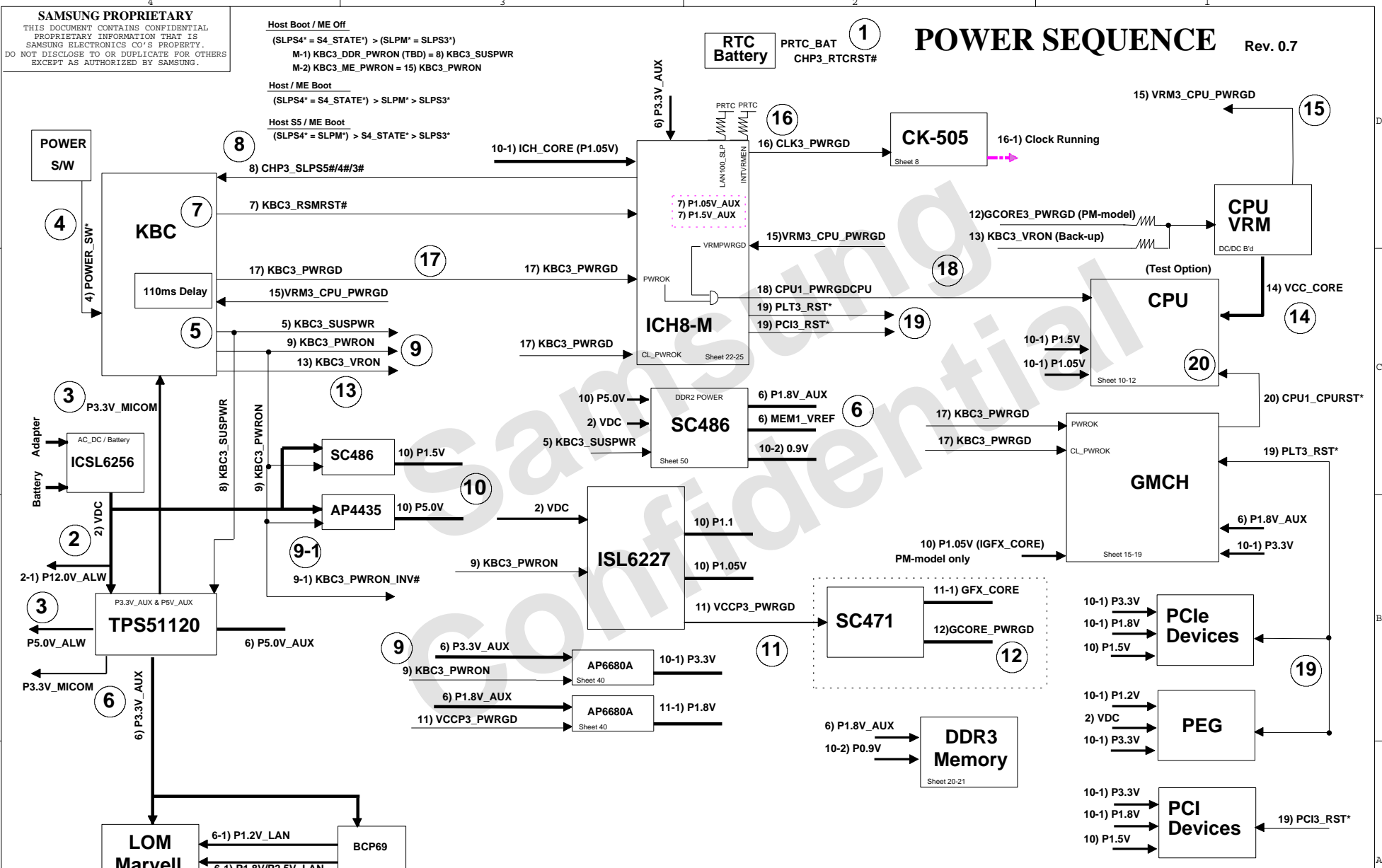
Host Boot / ME Off
 (SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
 M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
 M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
 (SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
 (SLPS4* = SLPM*) > S4_STATE* > SLPS3*

POWER SEQUENCE

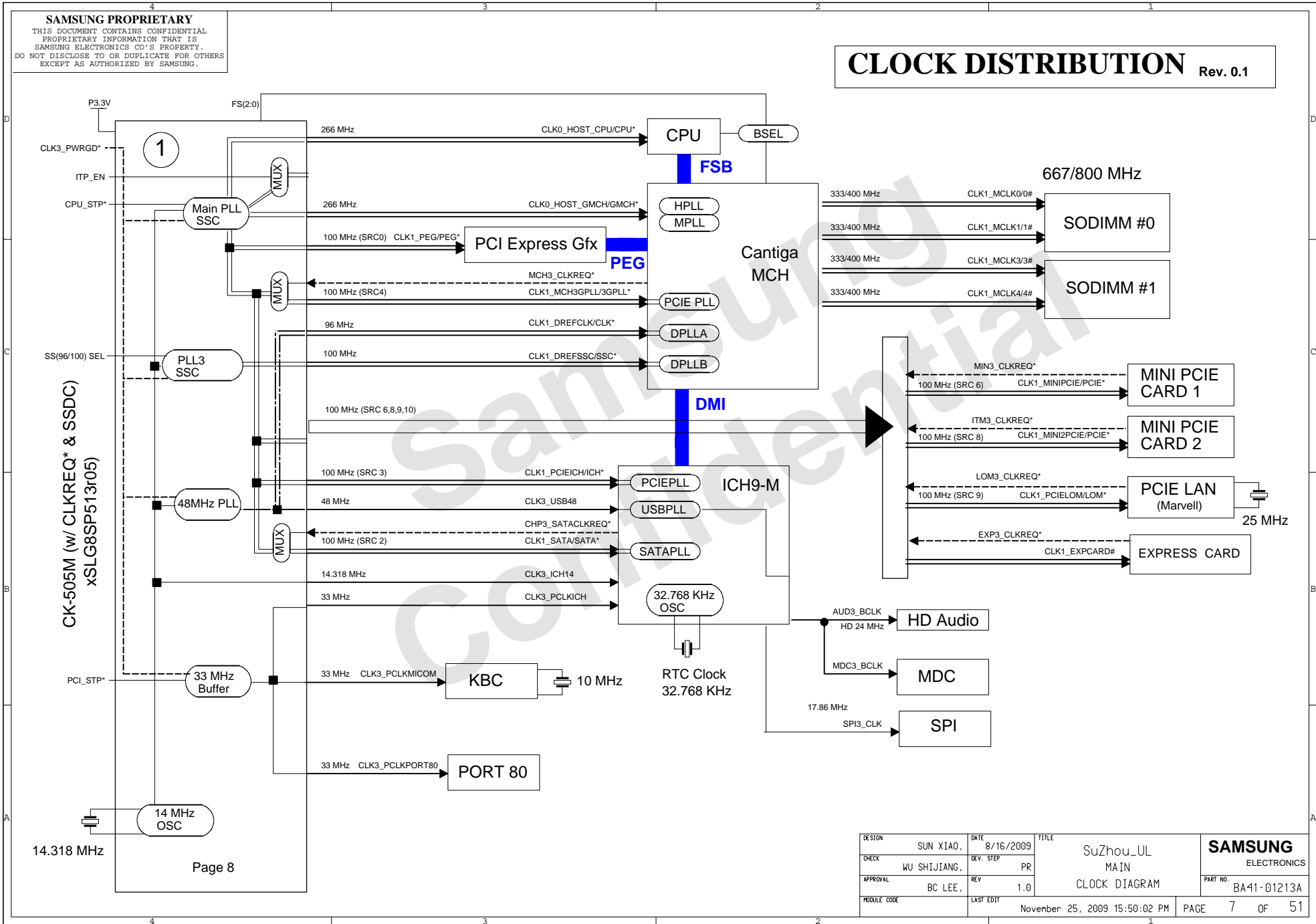
Rev. 0.7



DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	POWER SEQUENCE	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	6	OF 51

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CLOCK DISTRIBUTION Rev. 0.1

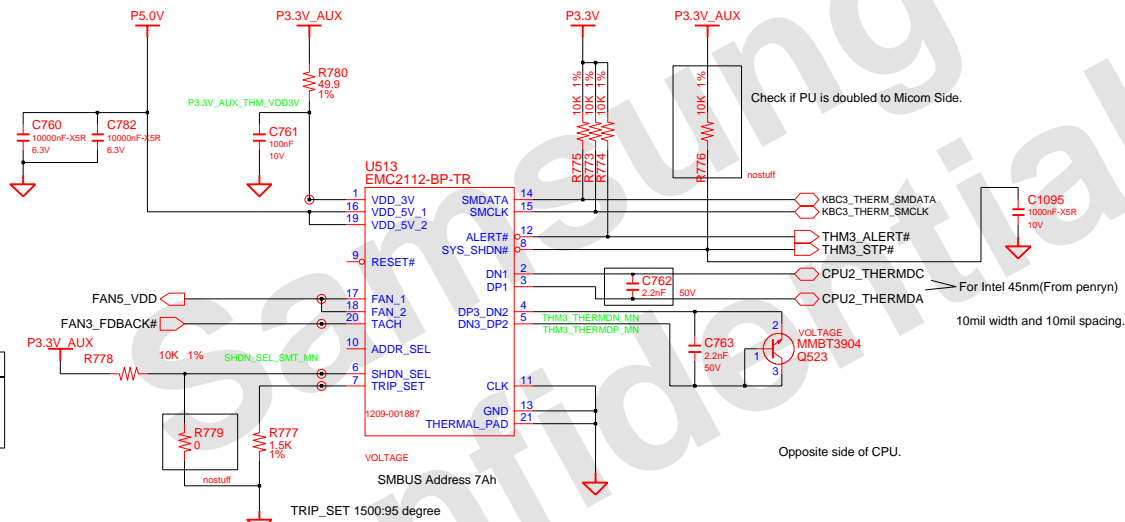


CK-505M (w/ CLKREQ* & SSDC)
xSLG8SP513r05

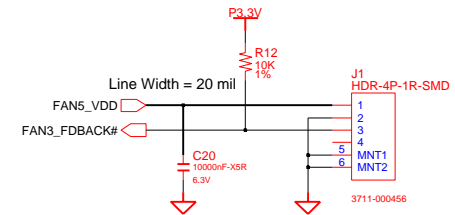
DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	CLOCK DIAGRAM	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	7	OF 51

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THERMAL SENSOR & FAN CONTROL

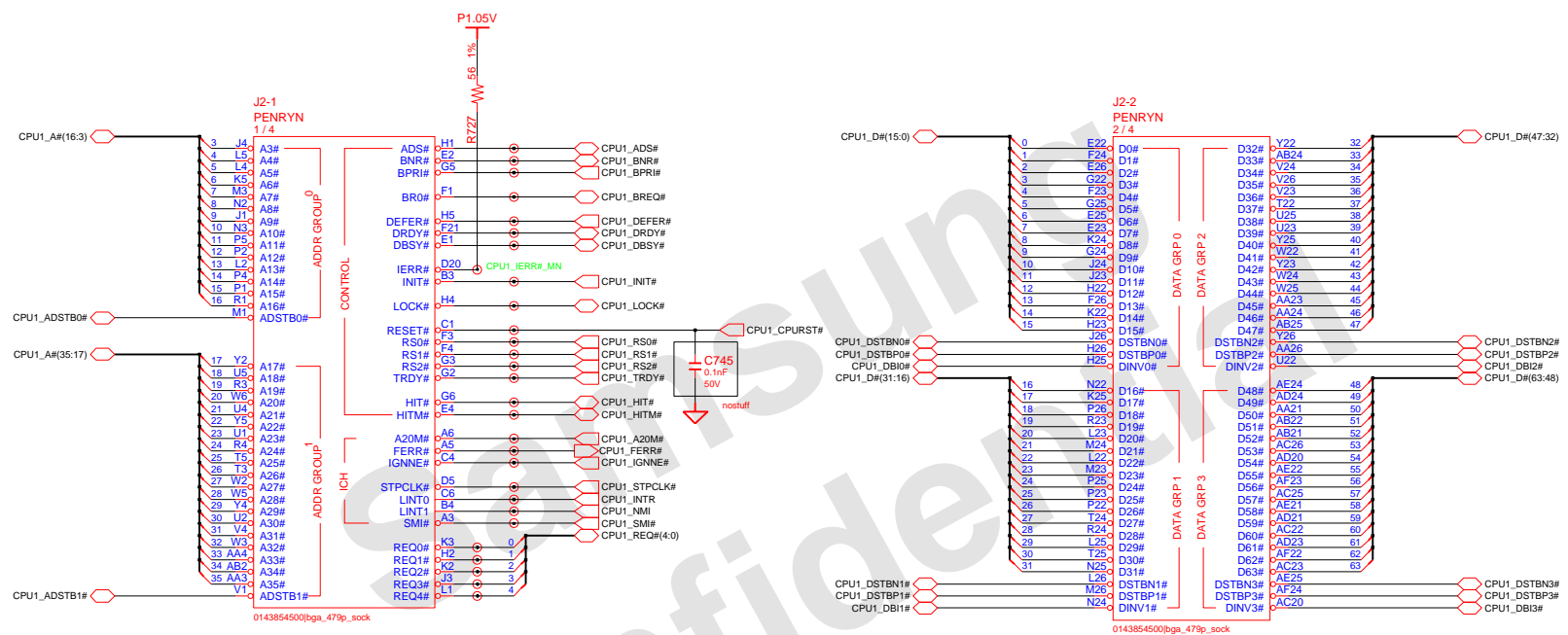


SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

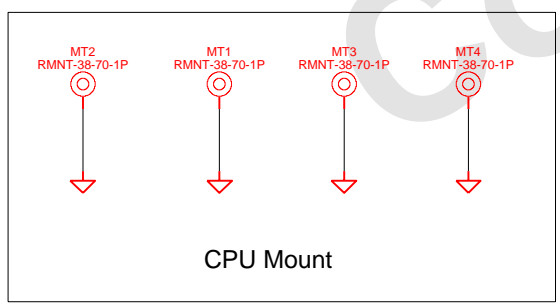


DESIGN	SUN XIAO,	DATE	6/17/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	Thermal Sensor EMC2102	PART NO.	
APPROVAL	BC LEE,	REV	1.0			BA41-01213A
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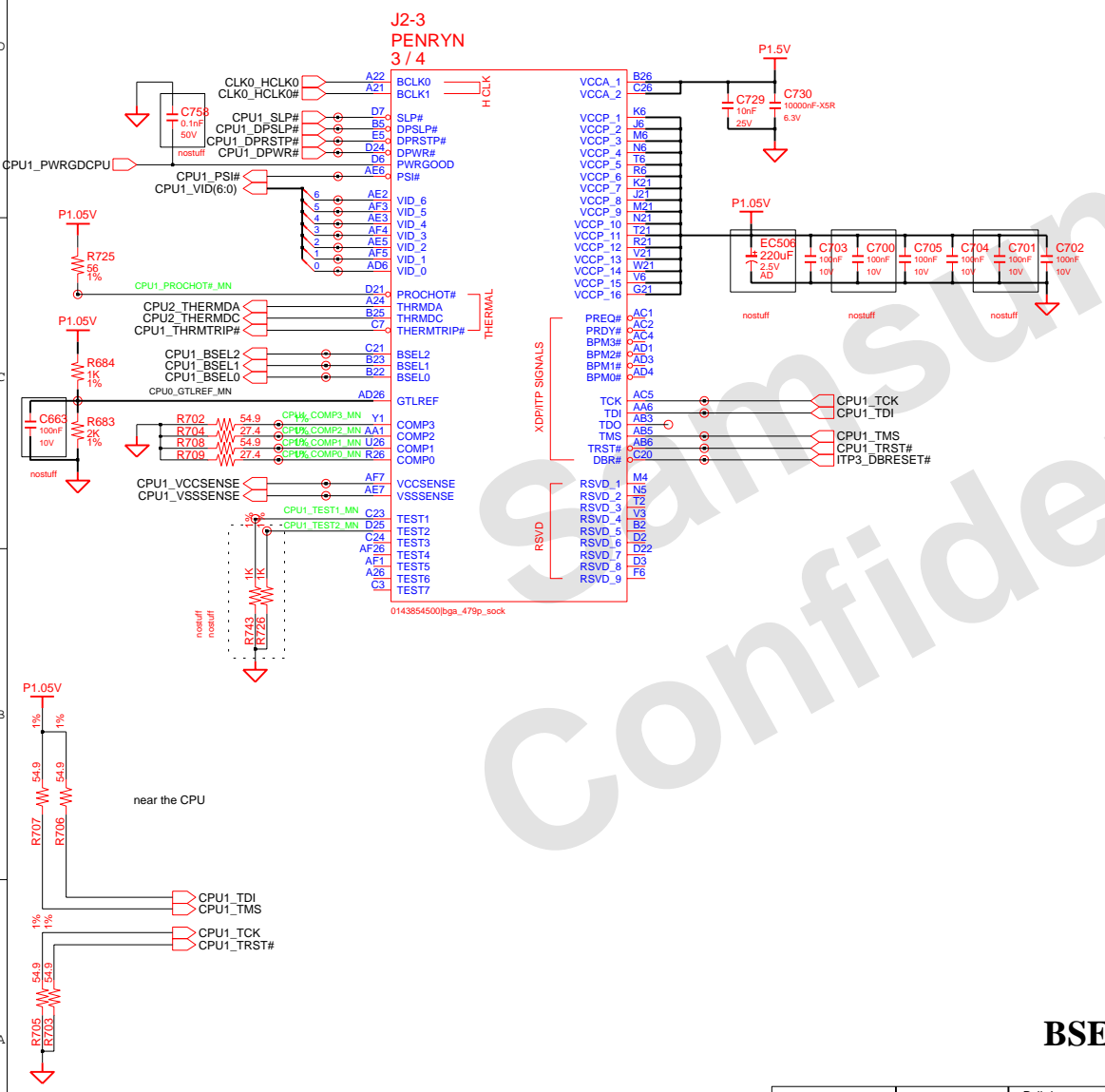


CPU Socket: 3704-001153



DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	CPU		
APPROVAL	BC LEE,	REV	1.0	PENRYN (1/3)	PART NO.	BA41-01213A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	9	OF 51

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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 1 0 0 0 0 0	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 1	1.1000 V	1 0 0 0 1 1 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 1 0	1.0875 V	1 0 0 0 1 1 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 1	1.0750 V	1 0 0 0 1 1 1	0.5750 V	1 1 1 0 1 0 0	0.0625 V
0 1 0 0 1 0 0	1.0625 V	1 0 0 0 1 1 1	0.5625 V	1 1 1 0 1 0 1	0.0500 V
0 1 0 0 1 0 1	1.0500 V	1 0 0 0 1 1 1	0.5500 V	1 1 1 0 1 1 0	0.0375 V
0 1 0 0 1 1 0	1.0375 V	1 0 0 0 1 1 1	0.5375 V	1 1 1 0 1 1 1	0.0250 V
0 1 0 0 1 1 1	1.0250 V	1 0 0 0 1 1 1	0.5250 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5000 V	1 1 1 1 0 1 0	0.0000 V
		1 0 0 0 1 1 1	0.5000 V	1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=50ohm trace. Minimize coupling of any switching signals to this net.

COMP0.2(COMP1.3) should be connected with Zo=27.4ohm(50ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSense at the end of the line. Route the VCC/VSSense as a Zo=50ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

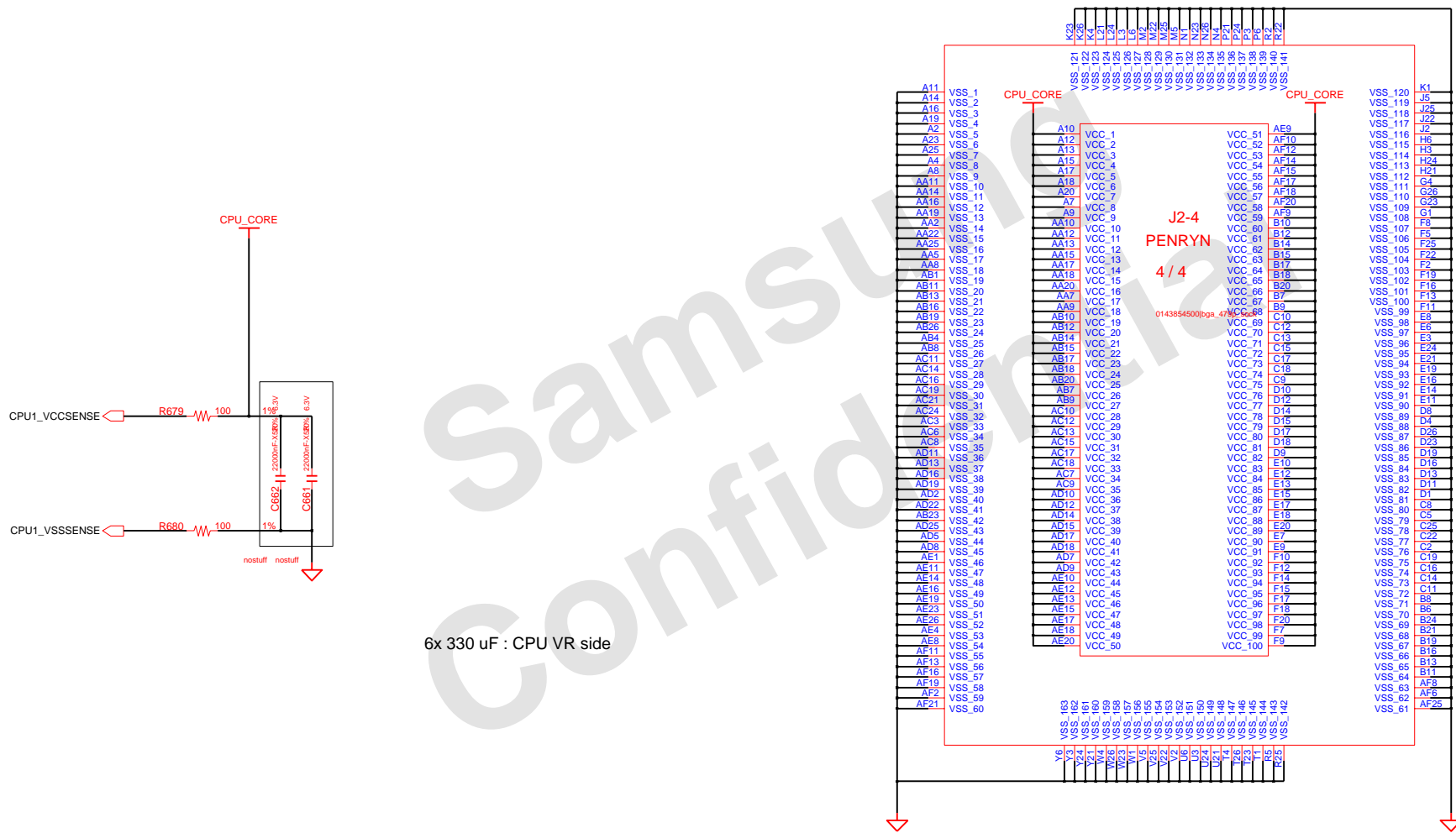
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

BSEL

FSB 1067 MHz		Pull-down
FSB 800 MHz		BSEL0, BSEL1, BSEL2
		BSEL0, BSEL2

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	REV. STEP	PR		CPU	
APPROVAL	BC LEE,	REV	1.0		PENRYN (2/3)	PART NO. BA41-01213A
MODULE CODE	undef ined	LAST EDIT	November 25, 2009 15:50:02 PM			PAGE 10 OF 51

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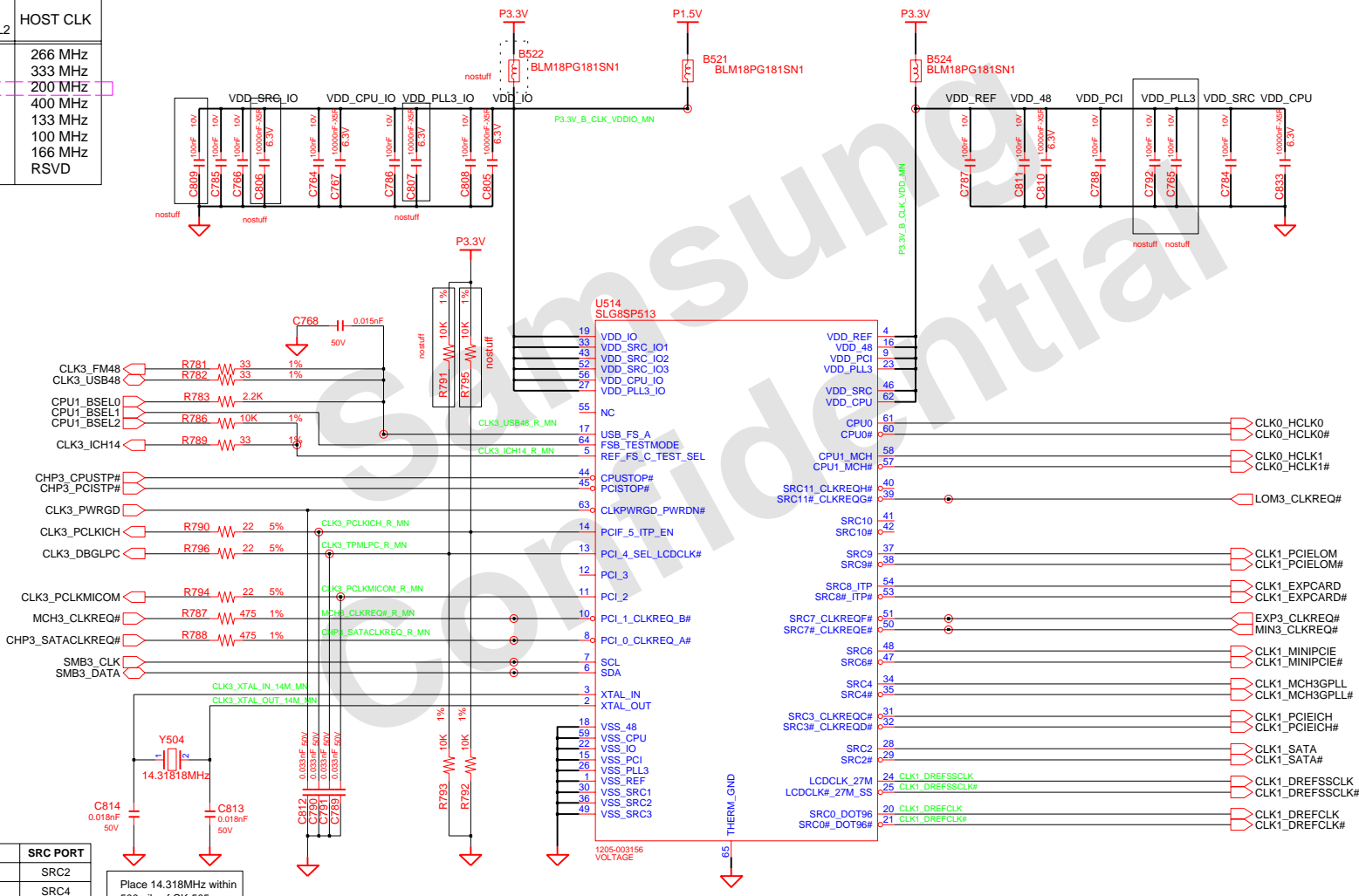
6x 330 uF : CPU VR side

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		CPU	
APPROVAL	BC LEE,	REV	1.0		PENRYN (3/3)	PART NO. BA41-01213A
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CK505M

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

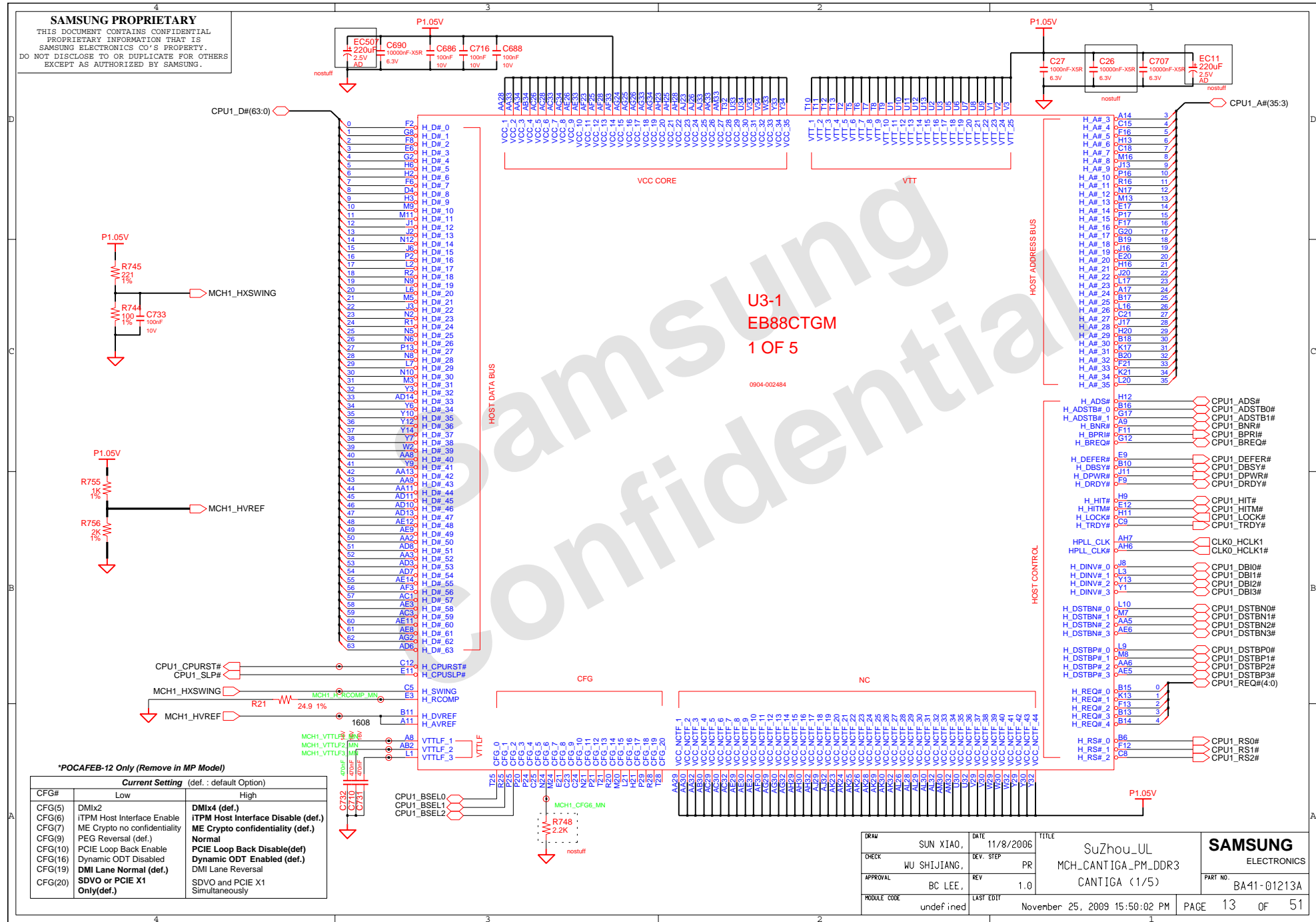
Place 14.318MHz within 500mils of CK-505

This part is 64pin QFN package.

IDT: 1205-003159
 SL: 1205-003533

DRAW	SUN XIAO,	DATE	8/12/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	Main_Clock_Circuit		
APPROVAL	BC LEE,	REV	1.0	CK_Clock_505M		
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	12 OF 51	

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U3-1
 EB88CTGM
 1 OF 5

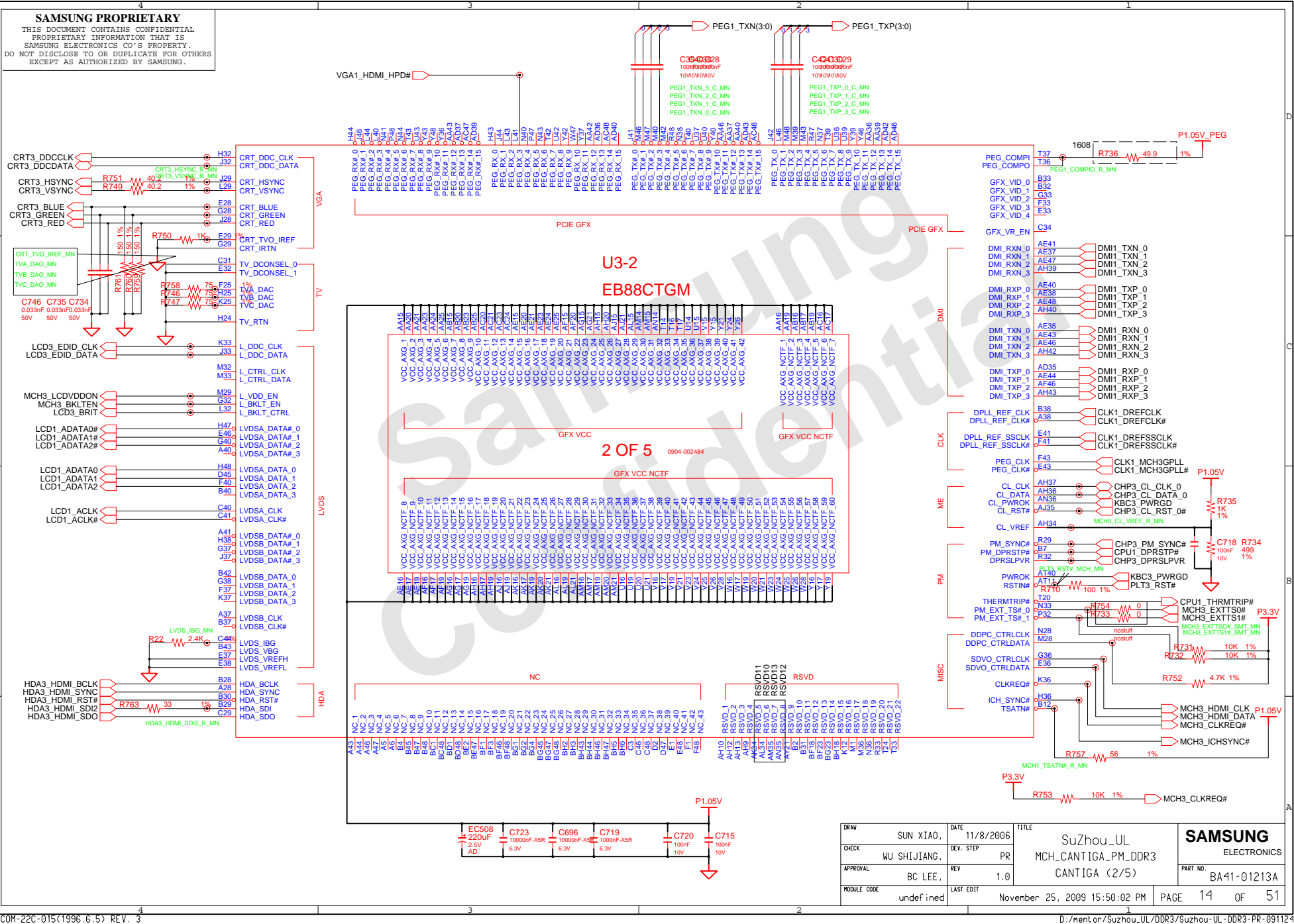
0904-002484

***POCAFEB-12 Only (Remove in MP Model)**

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	iTPM Host Interface Enable	iTPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

DRAW: SUN XIAO, DATE: 11/8/2006 CHECK: WU SHUIJIANG, DEV. STEP: PR APPROVAL: BC LEE, REV: 1.0 MODULE CODE: undefined, LAST EDIT: November 25, 2009 15:50:02 PM	TITLE: SuZhou_UL MCH_CANTIGA_PM_DDR3 CANTIGA (1/5)	SAMSUNG ELECTRONICS PART NO.: BA41-01213A
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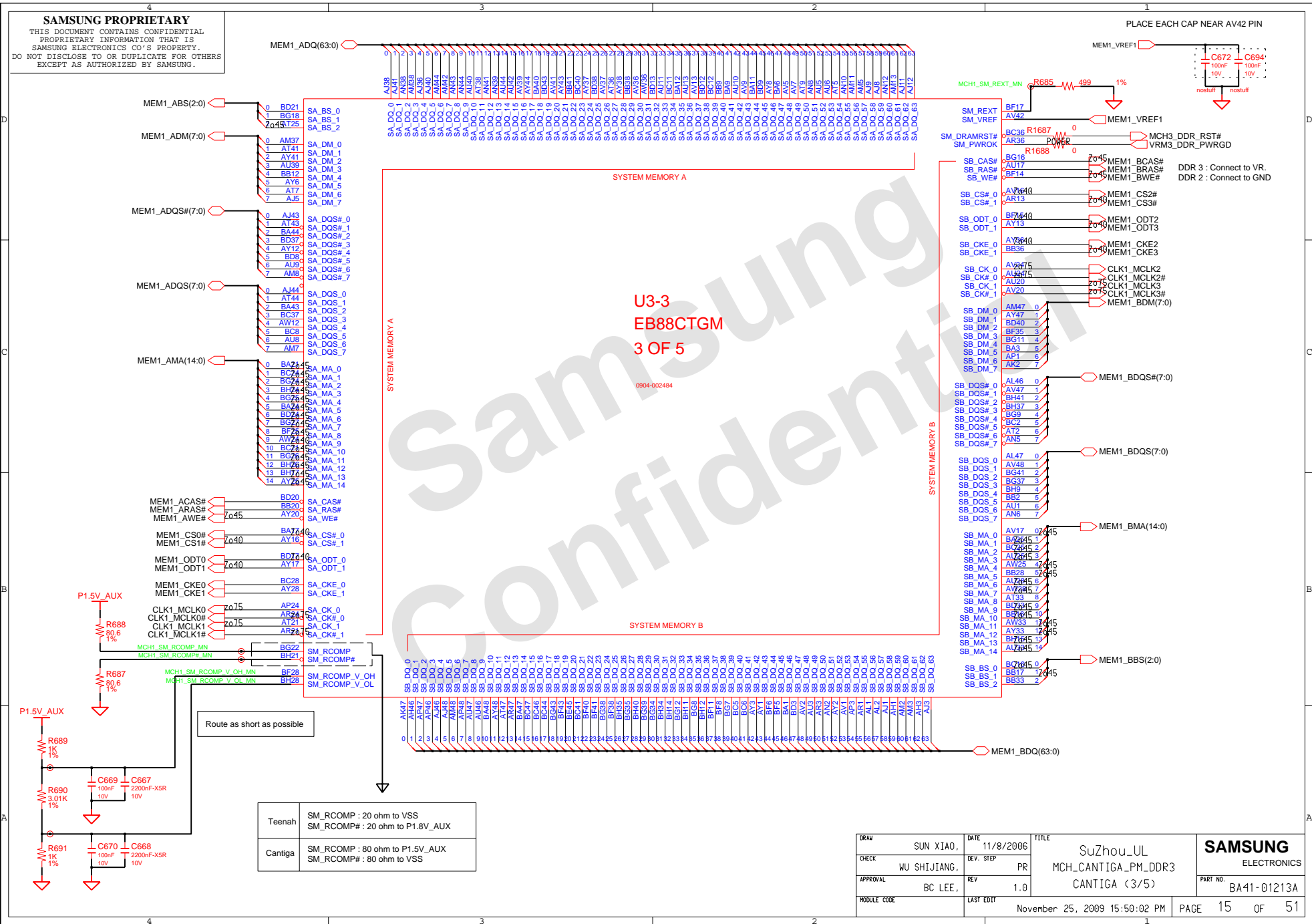
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DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHUIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3	CANTIGA (2/5)	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE	undef ined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	14	OF 51

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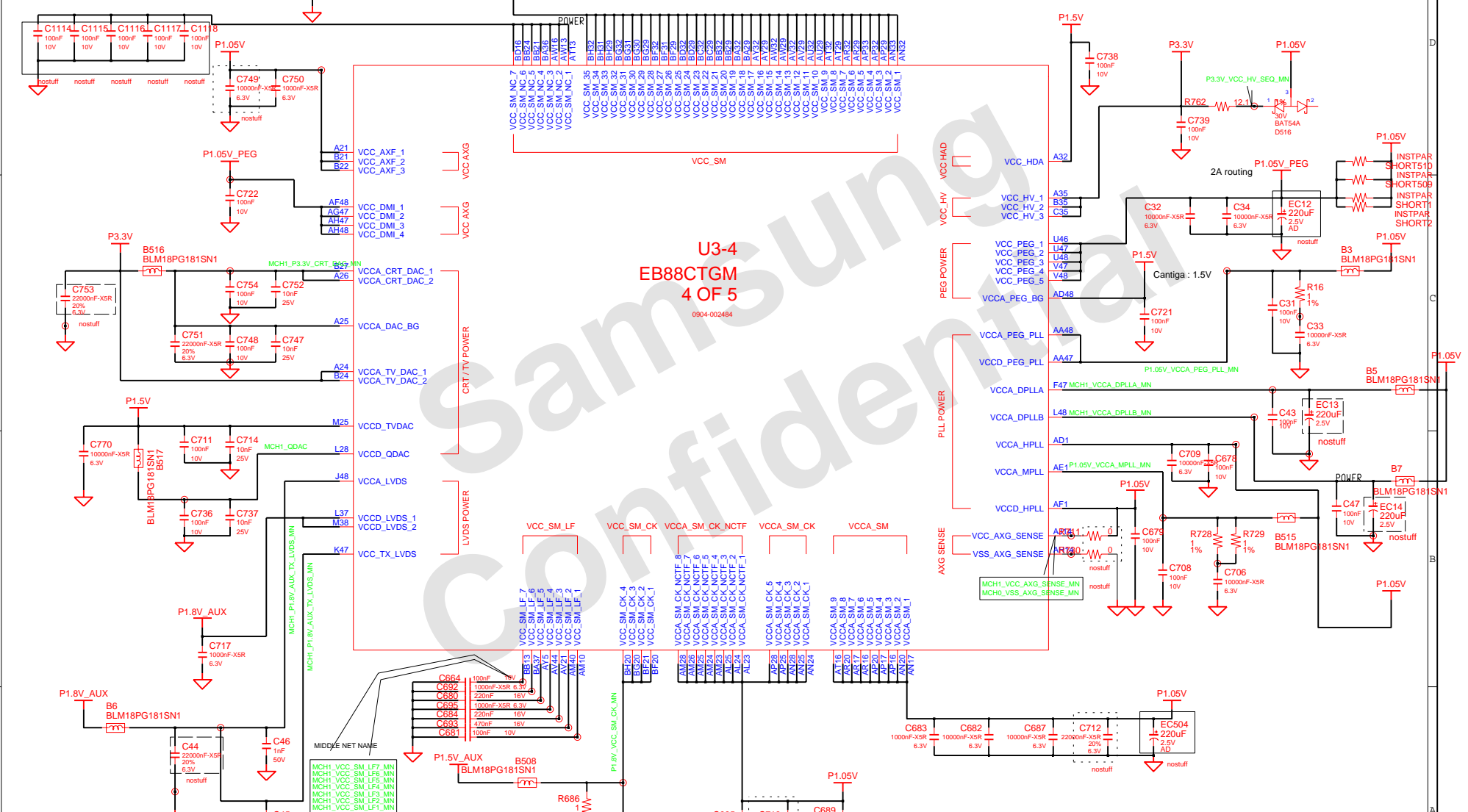
PLACE EACH CAP NEAR AV42 PIN



Teenah	SM_RCAMP : 20 ohm to VSS SM_RCAMP# : 20 ohm to P1.8V_AUX
Cantiga	SM_RCAMP : 80 ohm to P1.5V_AUX SM_RCAMP# : 80 ohm to VSS

DATE	SUN XIAO, 11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG, PR	DEV. STEP	MCH_CANTIGA_PM_DDR3	
APPROVAL	BC LEE, REV 1.0	REV	CANTIGA (3/5)	PART NO. BA41-01213A
MODULE CODE	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE 15	OF 51

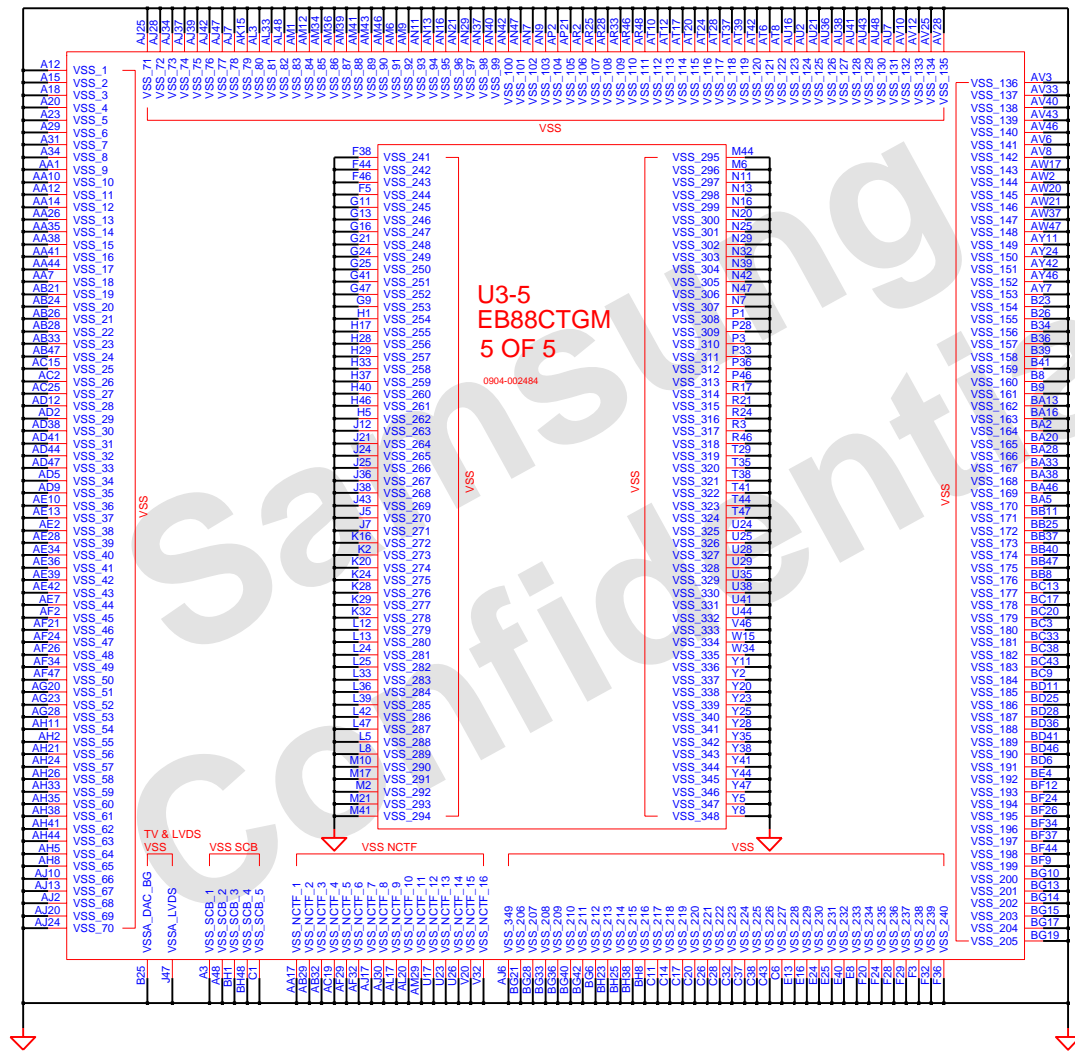
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**U3-4
 EB88CTGM
 4 OF 5**
 0904-002484

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3	CANTIGA (4/5)	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			PAGE 16 OF 51

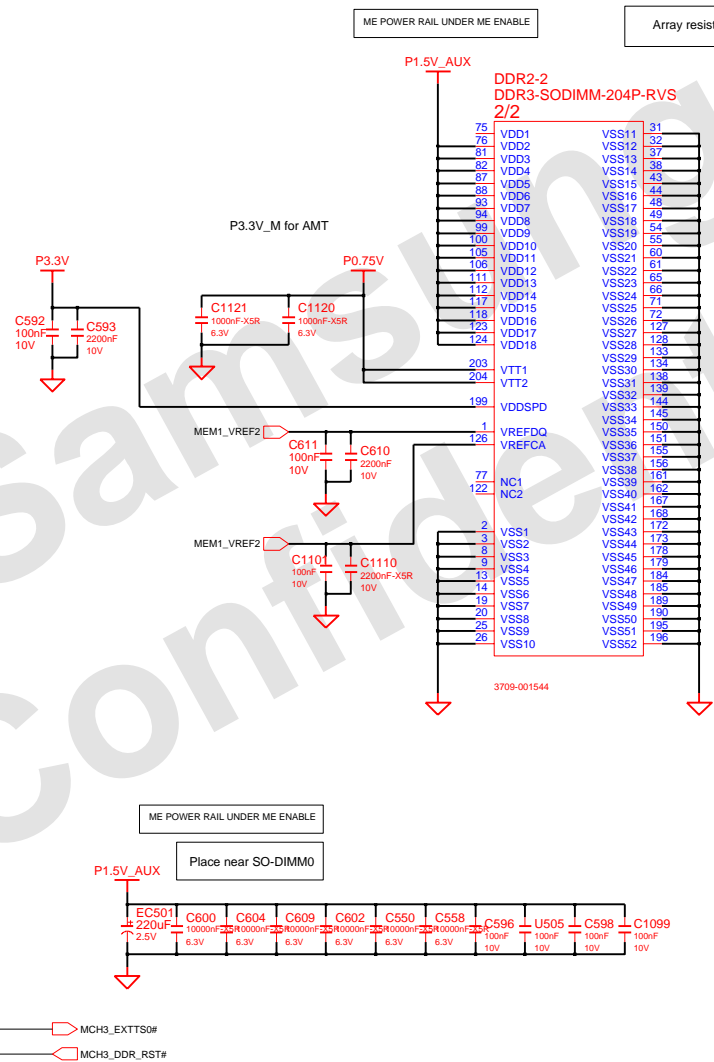
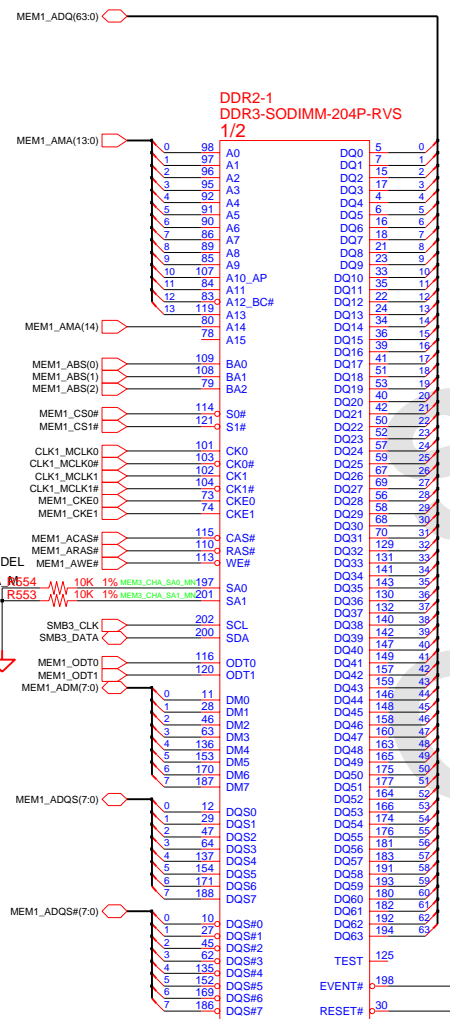
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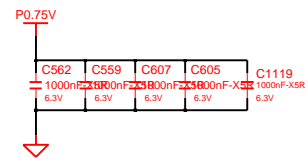
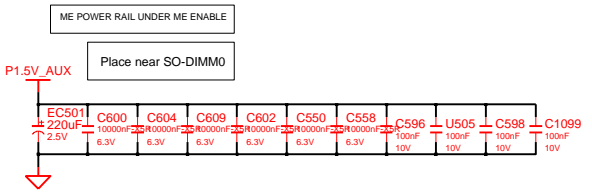
DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3	CANTIGA (5/5)	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	17	OF 51

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DDR SO-DIMM #0



Array resistors & Single resistors used to improve layout & routing.

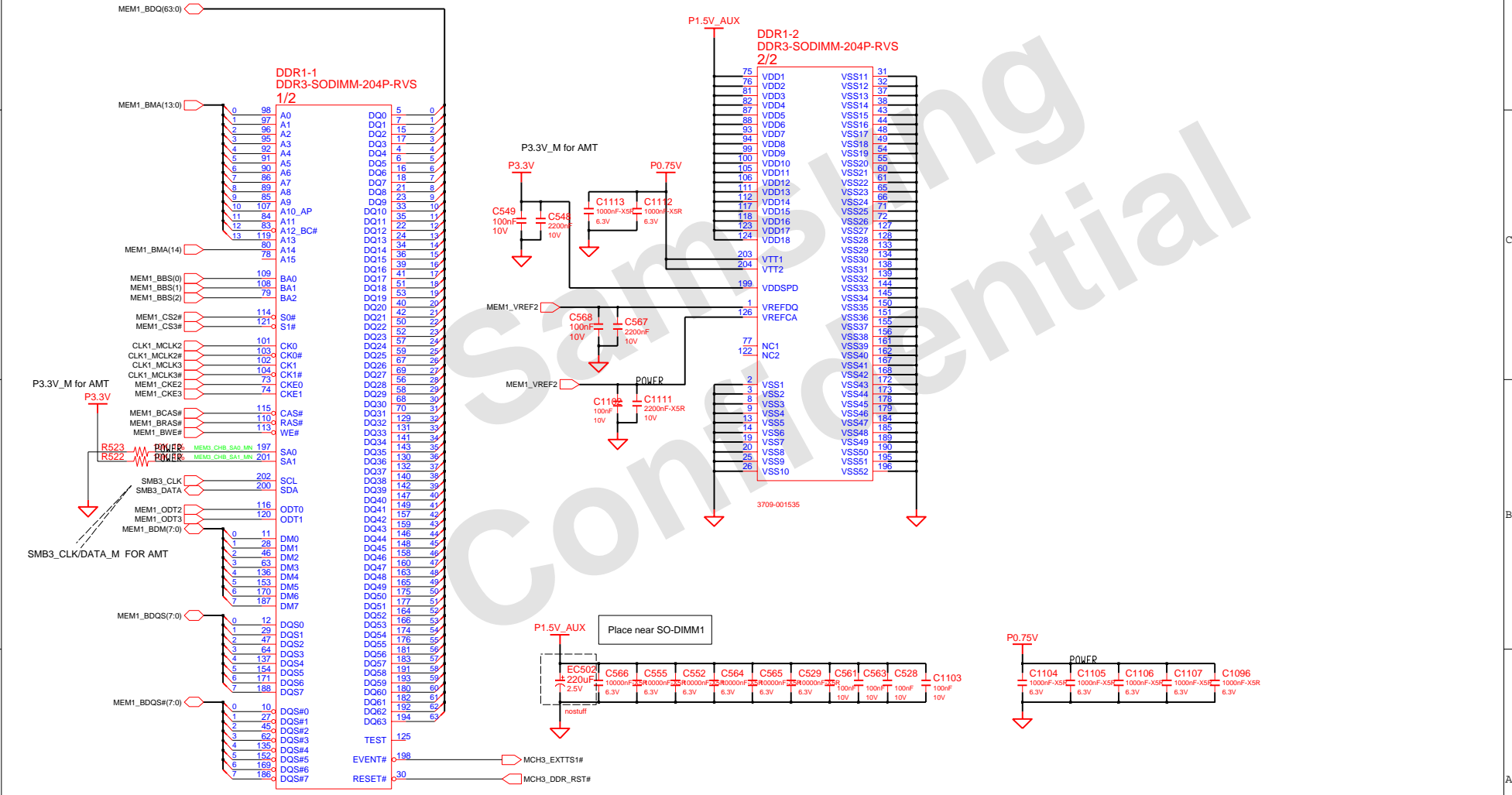


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CHECK	WU SHIJIANG,	DEV. STEP	PR	SODIMM_REV	PART NO.	
APPROVAL	BC LEE,	REV	1.0	DDR3 CH A	BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	18 OF 51	

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DDR SO-DIMM #1

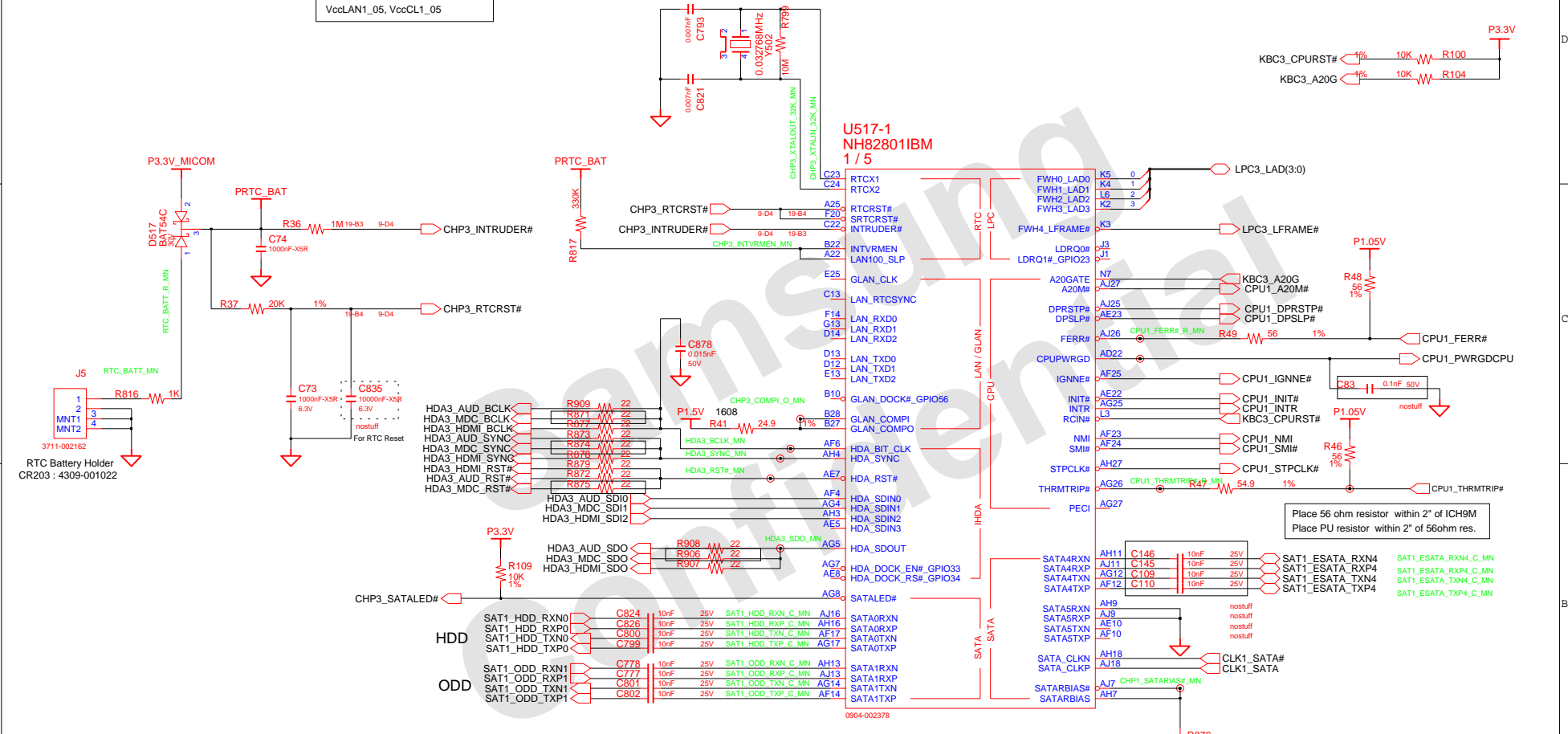
Array resistors & Single resistors used to improve layout & routing.



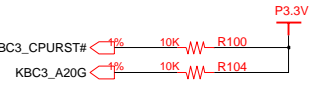
DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	SODIMM_REV	PART NO.	
APPROVAL	BC LEE,	REV	1.0	DDR3 CH B	BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	19 OF 51	

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Internal VR Strap
 INTVRMEN Pull up
 VccSus1_05, VccSus1_5, VccCL1_5
 VccLAN1_05, VccCL1_05



SATA Cap. Place ment :
 Distance b/w the ICH9-M & cap on the "P" signal should be identical
 distance b/w the ICH9-M & cap on the "N" signal same pair.

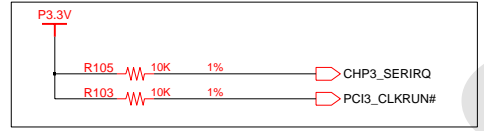


Place 56 ohm resistor within 2" of ICH9M
 Place PU resistor within 2" of 56ohm res.

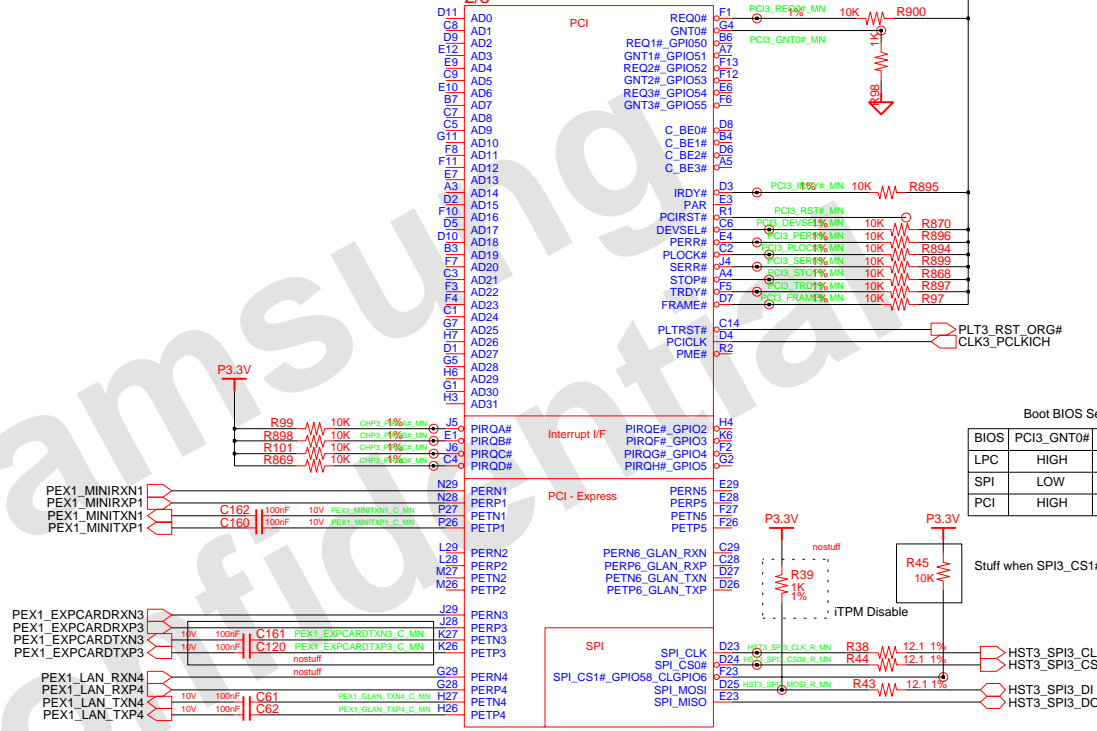
DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		ICH9M_B	
APPROVAL	BC LEE,	REV	1.0		ICH9-M (1/5)	PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			PAGE 20 OF 51

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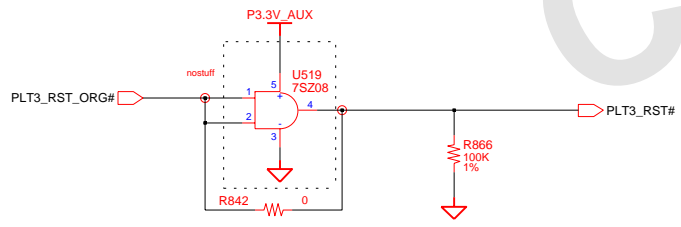
**U517-2
 NH82801IBM
 2/5**



LPC option : These are used with LPC

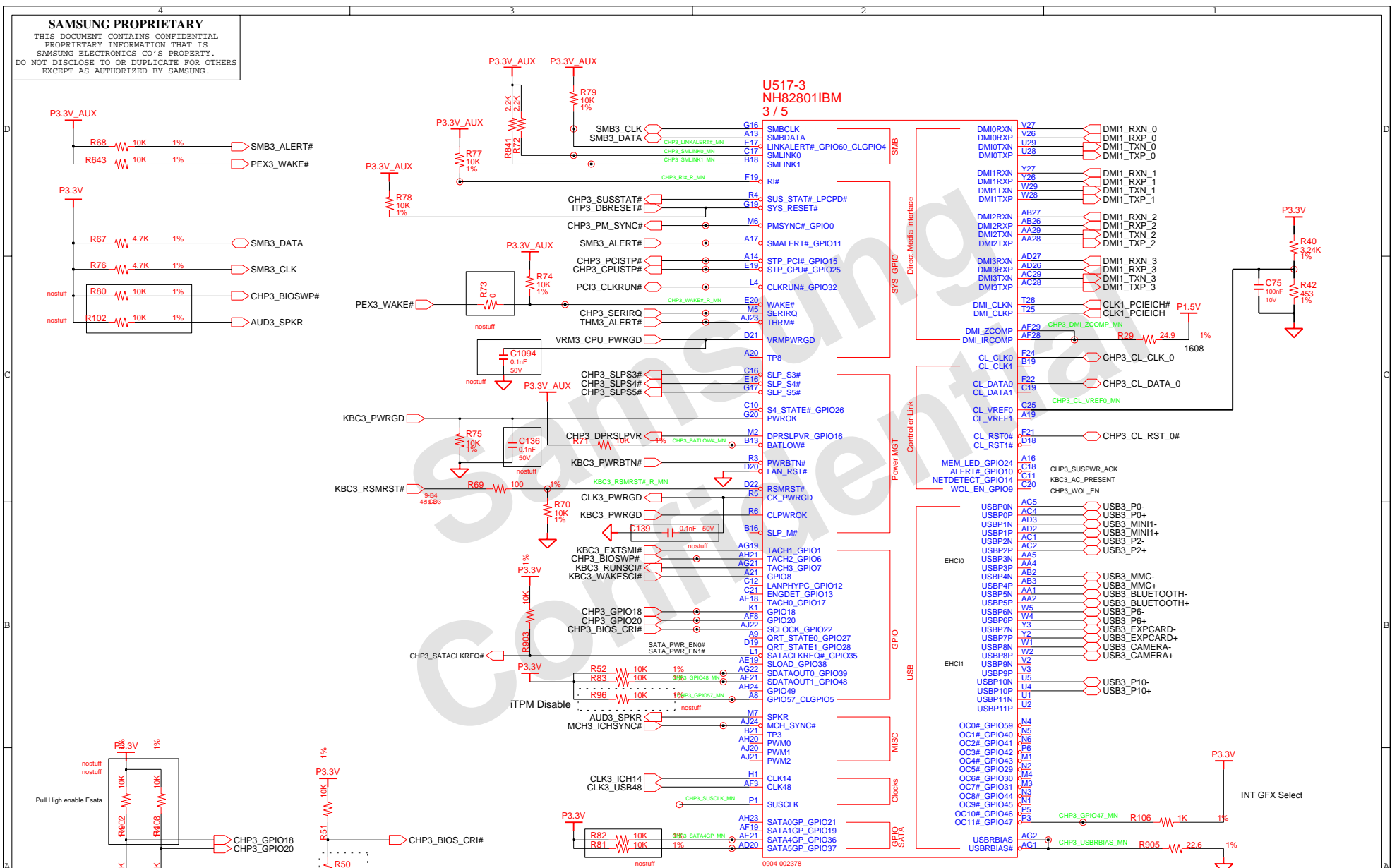


AC caps : PCIe need to be within 250mils of the driver
 Resistor for Test : Place Stuffing Option to minimize stubs



DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		ICH_9M_B	
APPROVAL	BC LEE,	REV	1.0		ICH9-M (2/5)	PART NO. BA41-01213A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM			PAGE 21 OF 51

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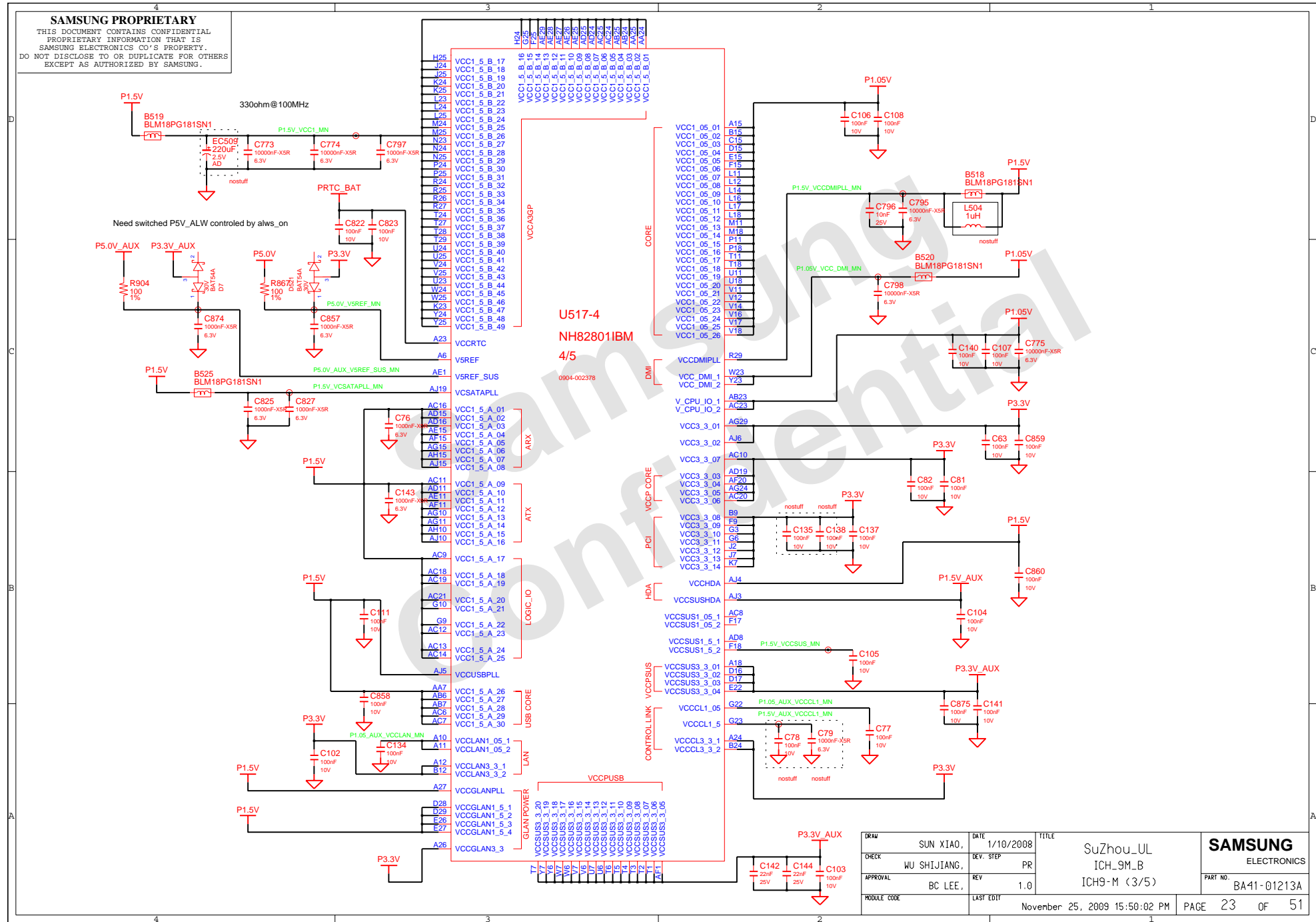


**U517-3
NH82801IBM
3/5**

DRWN	SUN XIAO,	DATE	1/10/2008	TITLE	SuZhou_UL
CHECK	WU SHIJIANG,	DEV. STEP	PR		ICH_9M_B
APPROVAL	BC LEE,	REV	1.0		ICH9-M (3/5)
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM		

<p>SAMSUNG ELECTRONICS</p>	PART NO.	BA41-01213A
	PAGE	22 OF 51

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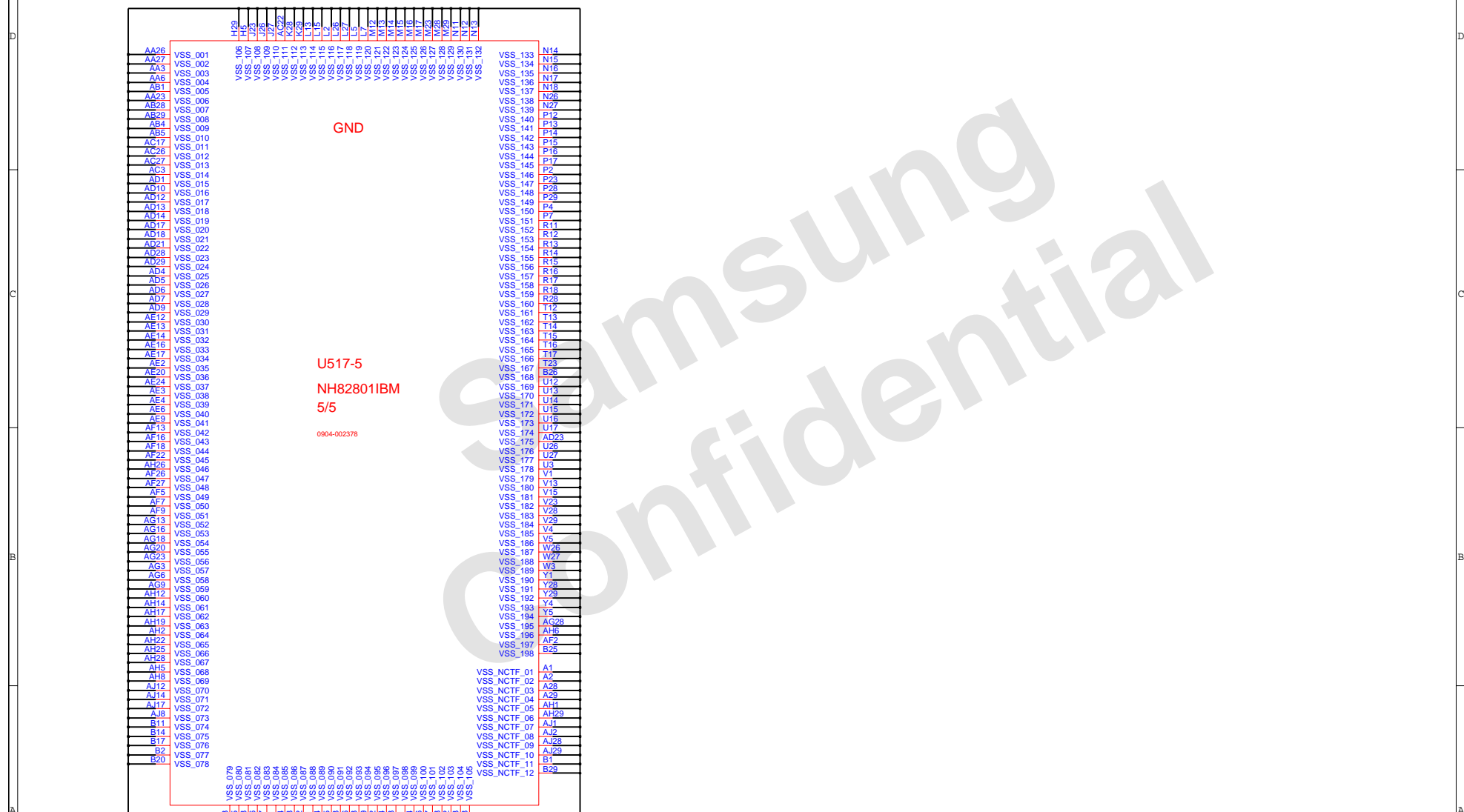


U517-4
NH82801BM
 4/5
 0904-002378

DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	SuZhou_UL
CHECK	WU SHIJIANG,	DEV. STEP	PR	ICH_9M_B	
APPROVAL	BC LEE,	REV	1.0	ICH9-M (3/5)	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	23 OF 51

SAMSUNG
 ELECTRONICS
 PART NO. BA41-01213A

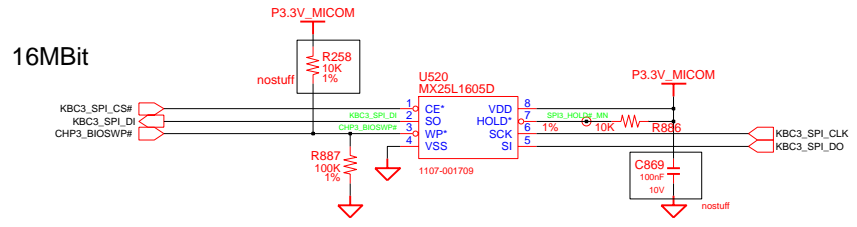
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DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		ICH_9M_B	
APPROVAL	BC LEE,	REV	1.0		ICH9-M (5/5)	PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	24	OF 51

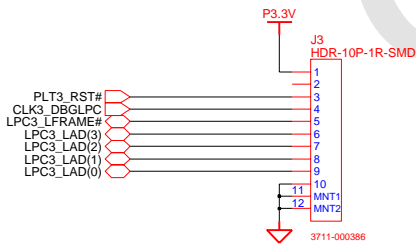
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SPI_BIOS_ROM

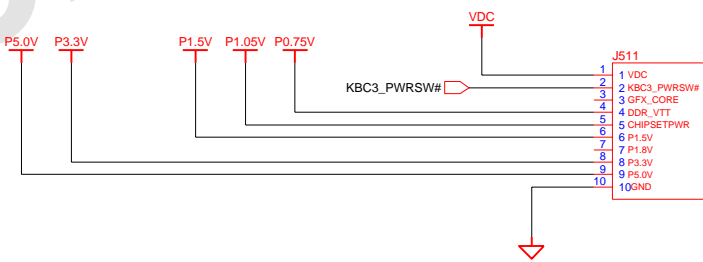


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM HW	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT.	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	RESET CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTERNATE REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	89	ENABLE NMI
54	SET KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 1
5A	DISPLAY PRESS. SETUP	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



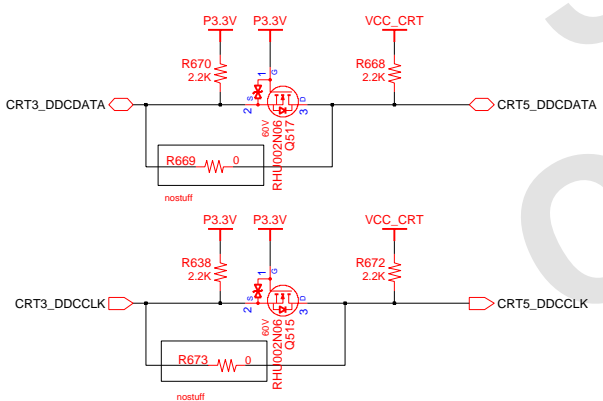
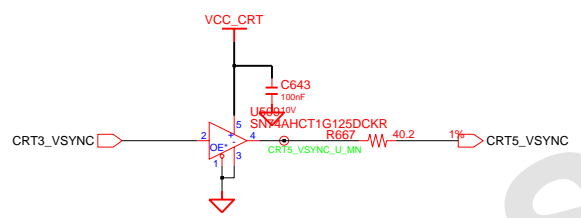
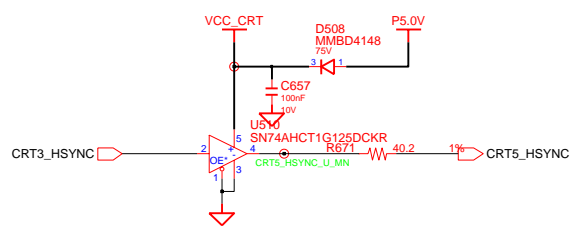
ICT PORT



DRAW	SUN XIAO,	DATE	8/12/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	SPI_BIOS_ROM	PART NO.	
APPROVAL	BC LEE,	REV	1.0	SPI_BIOS_ROM	BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			

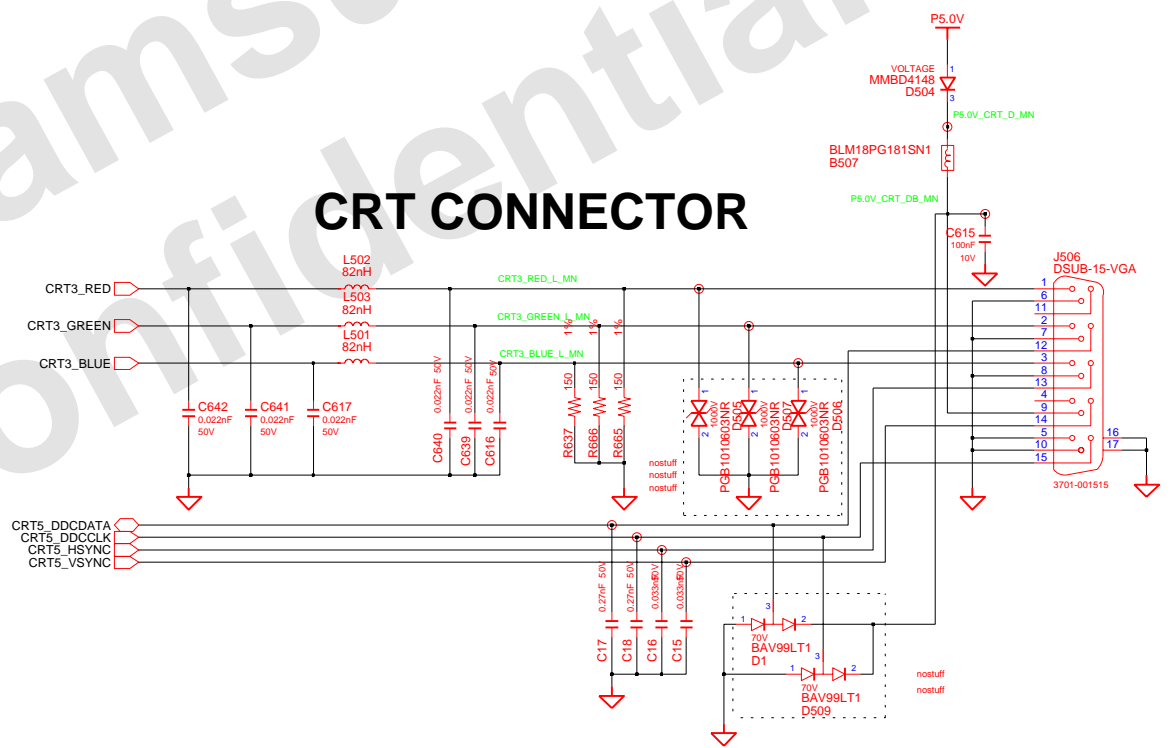
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CRT



Check "CRT3_DDCCLK/DATA" Voltage Level
 2N06 Can be replaced with SM6K2

CRT CONNECTOR



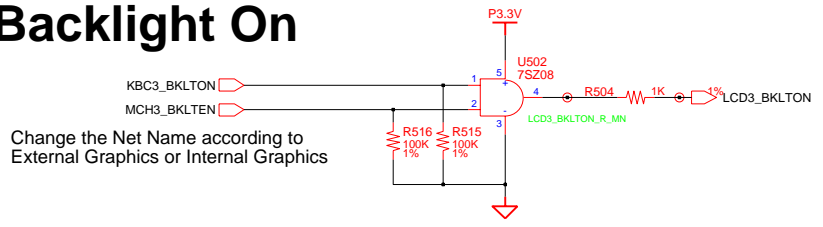
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CHECK	WU SHIJIANG,	DEV. STEP	PR	GRAPHICS_IF	PART NO.	
APPROVAL	BC LEE,	REV	1.0	CRT	BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	26	OF 51

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LVDS

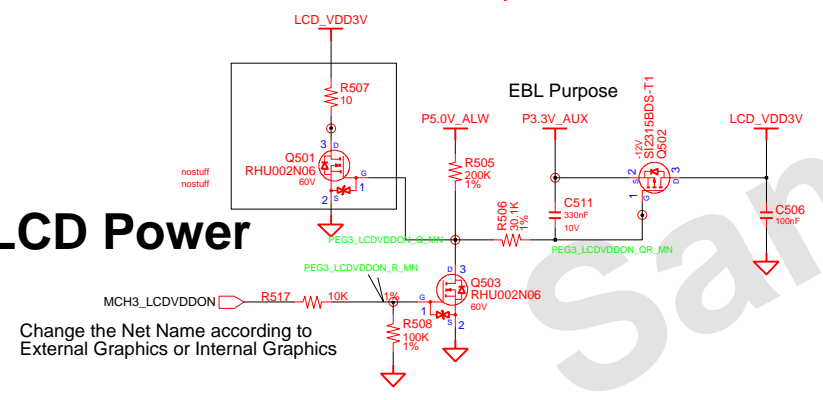
1Ch. LCD Connector

Backlight On



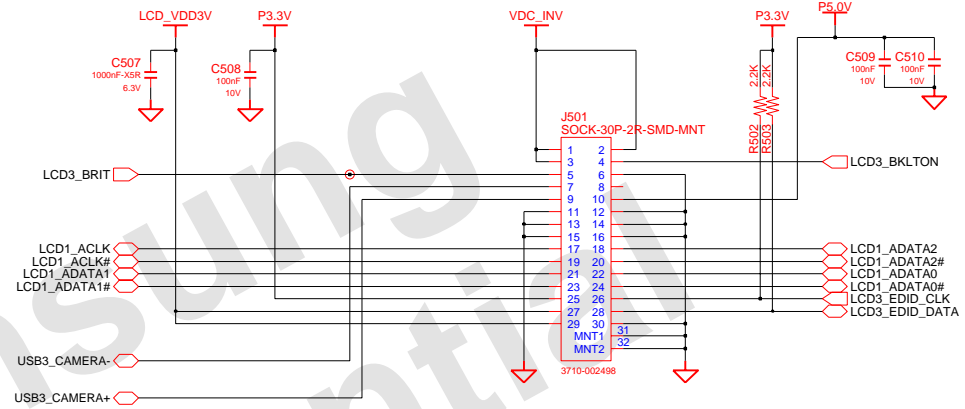
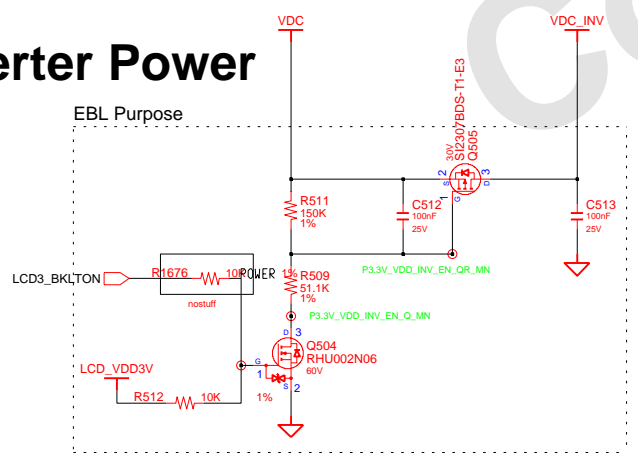
Change the Net Name according to
 External Graphics or Internal Graphics

LCD Power



Change the Net Name according to
 External Graphics or Internal Graphics

Inverter Power



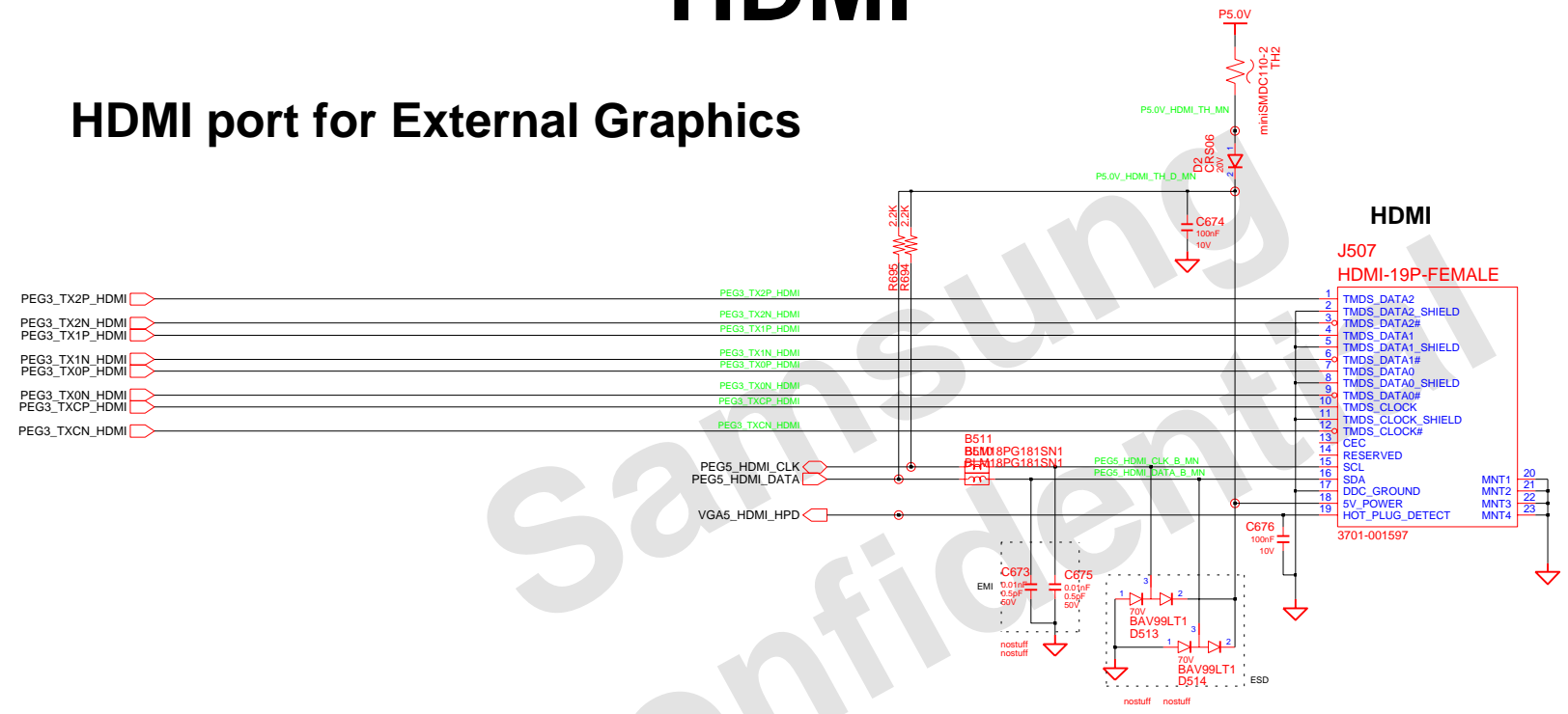
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DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	GRAPHICS_IF		
APPROVAL	BC LEE,	REV	1.0	LVDS		PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			PAGE 27 OF 51

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HDMI

HDMI port for External Graphics

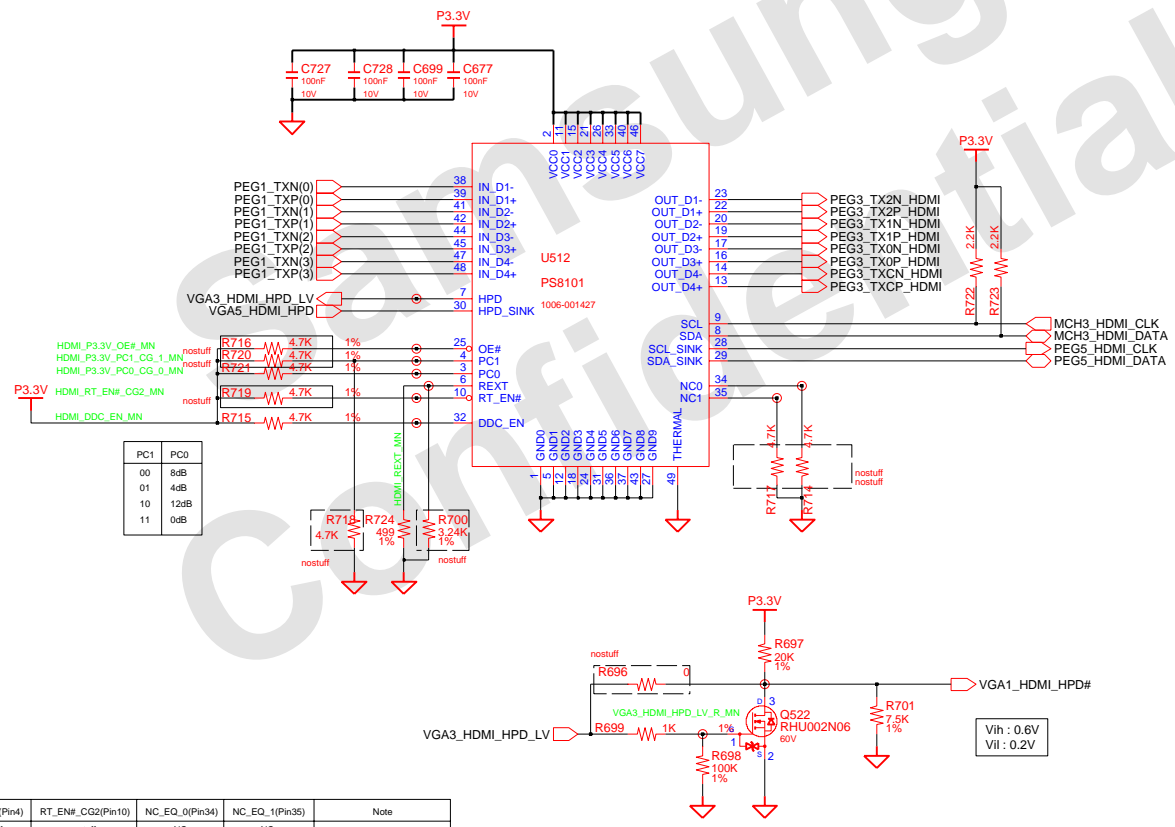


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DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	GRAPHICS_IF		
APPROVAL	BC LEE,	REV	1.0	HDMI	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	28	OF 51

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HDMI Level Shifter for Int. Graphic only



EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

Internal Default Value

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB

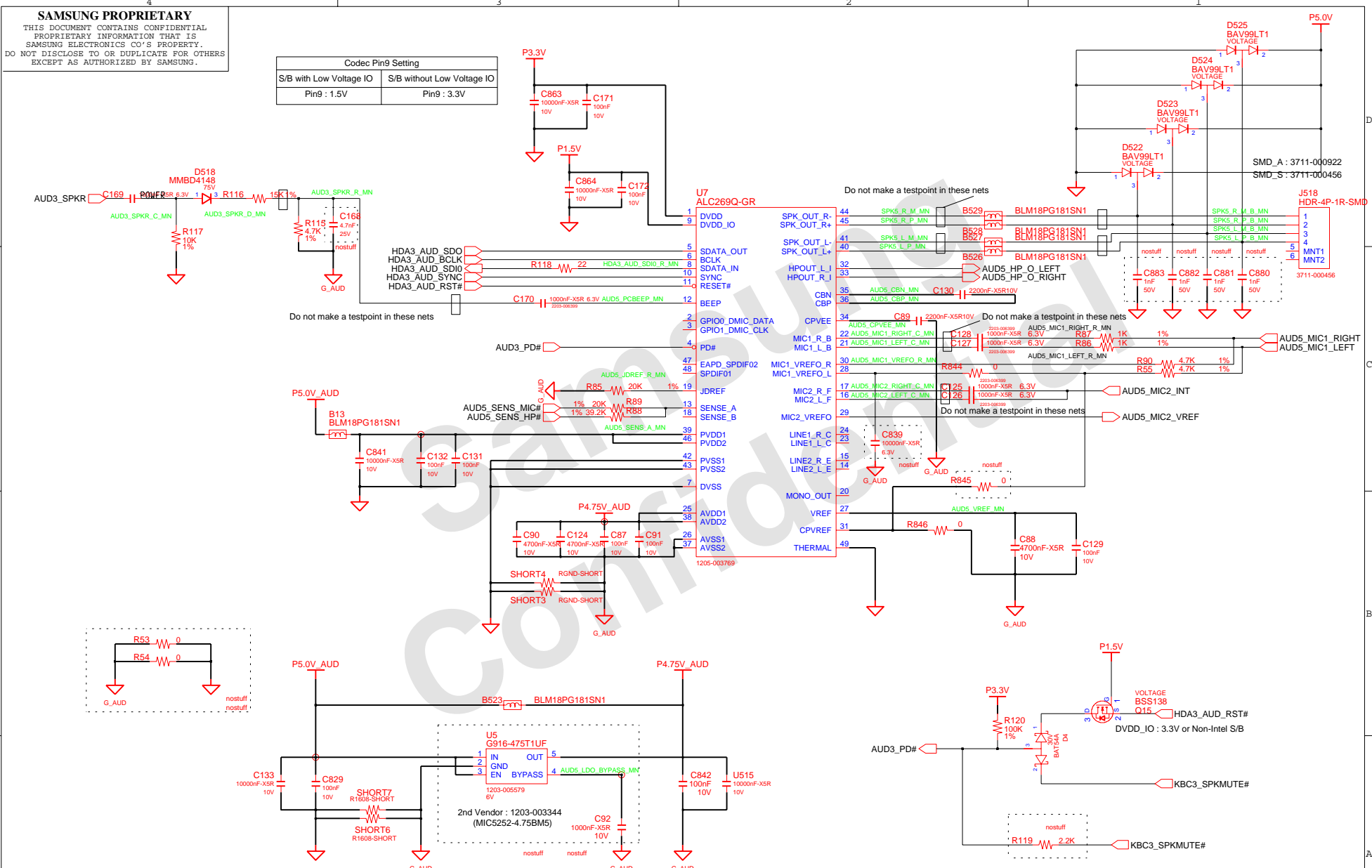
PC1	PC0
00	9dB
01	4dB
10	12dB
11	0dB

HDMI Level Shifter	REXT(Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC	
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PUPD exist CGs nostuff is 450mV swing

DESIGN	SUN XIAO,	DATE	9/14/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	HDMI LEVEL SHIFTER		PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	29	OF 51

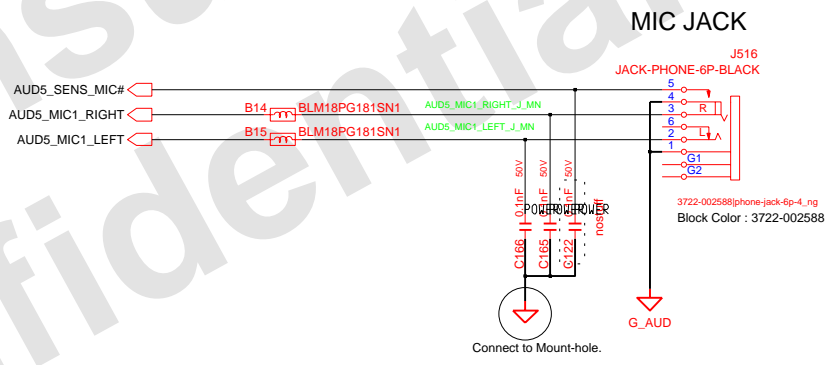
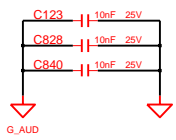
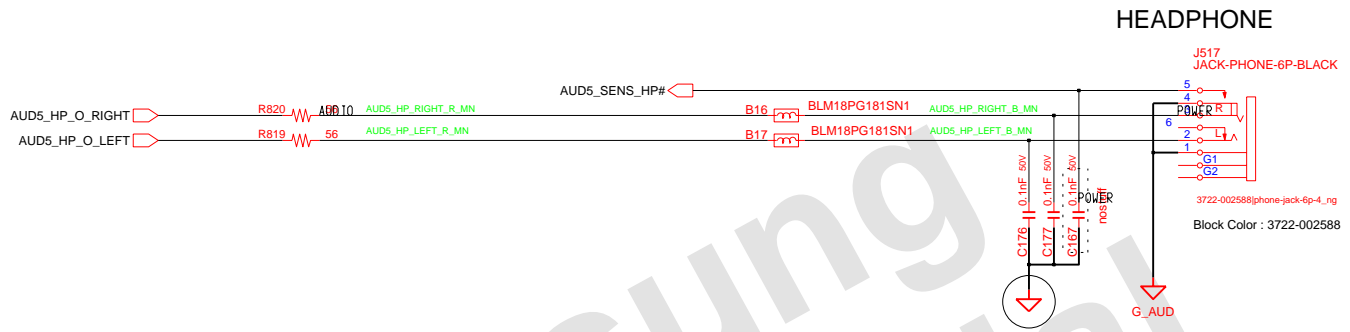
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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



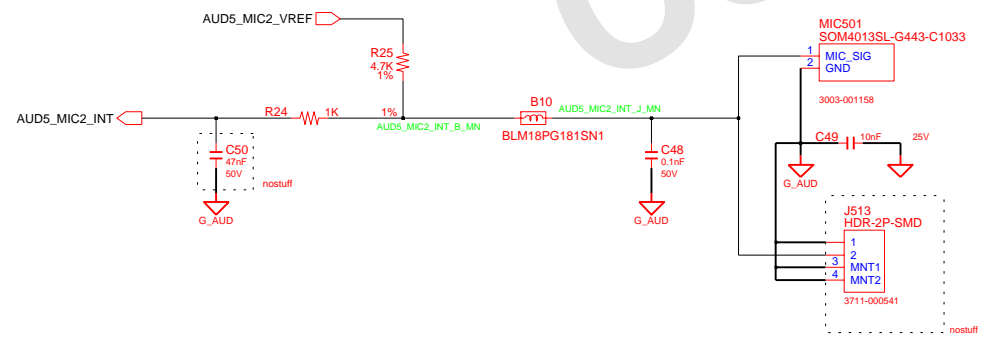
DESIGN	SUN XIAO,	DATE	3/13/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS PART NO. BA41-01213A
CHECK	WU SHIJIANG,	DEV. STEP	PR		HDA_ALC269_GR	
APPROVAL	BC LEE,	REV	1.0		AUDIO CODEC	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			

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Analog mono Mic Ass'y : Place inside Audio Analog Plane

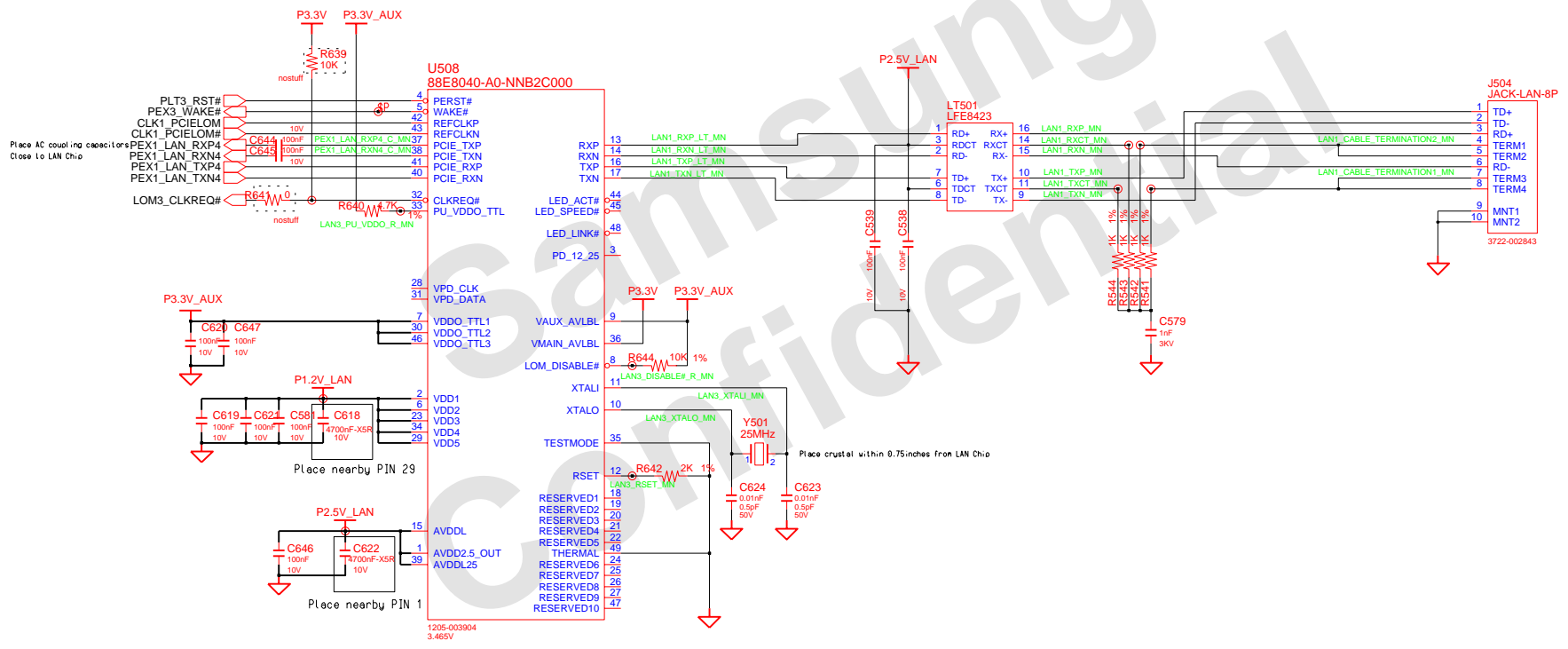
SMD MIC



DESIGN	SUN XIAO,	DATE	3/13/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	HDA_ALC269_GR	PART NO.	
APPROVAL	BC LEE,	REV	1.0	AUDIO INPUT/OUTPUT	BA41-01213A	PAGE 31 OF 51
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			

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MARVELL 88E8040

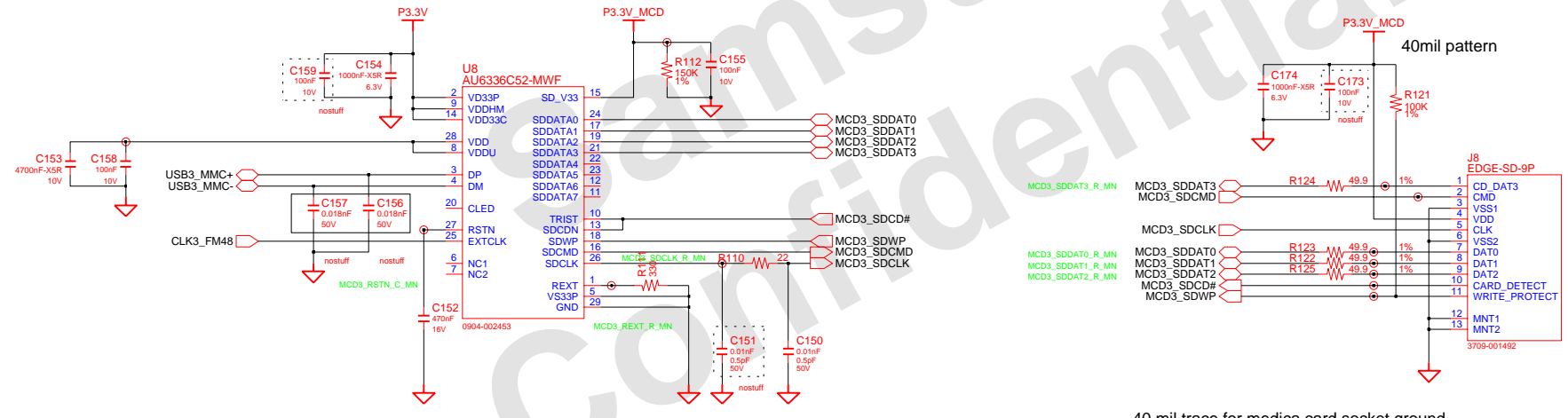


DESIGN	SUN XIAO,	DATE	3/17/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	32	OF 51

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3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches

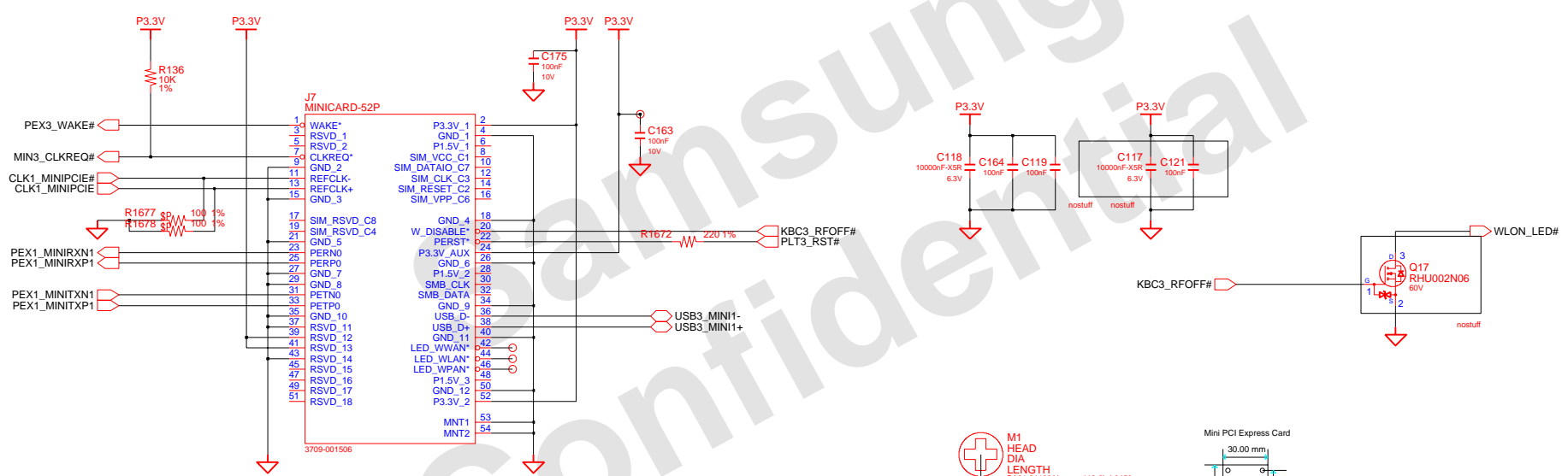


40 mil trace for medica card socket ground

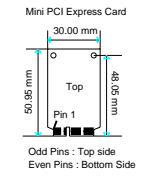
DESIGN	SUN XIAO,	DATE	4/29/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			PAGE 33 OF 51

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WLAN, 7mm



To fix Shirley Peak EMI issue
 Place it at the old rubber area

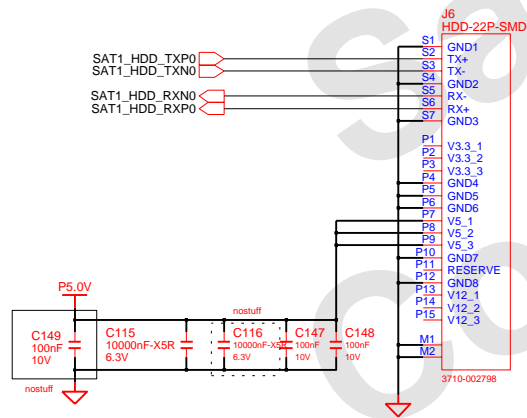


DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJANG,	DEV. STEP	PR	MINI_PCIE_CONN	PART NO.	
APPROVAL	BC LEE,	REV	1.0		BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	34	OF 51

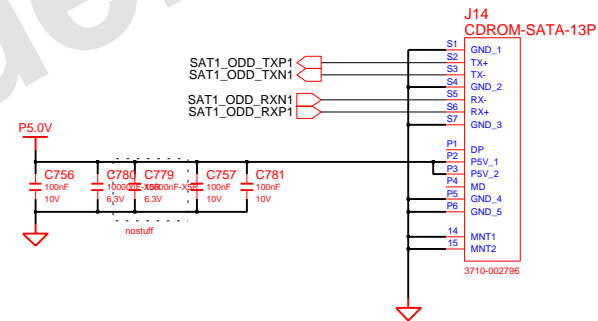
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SATA I/F CONN

SATA HDD CONN



SATA ODD CONN

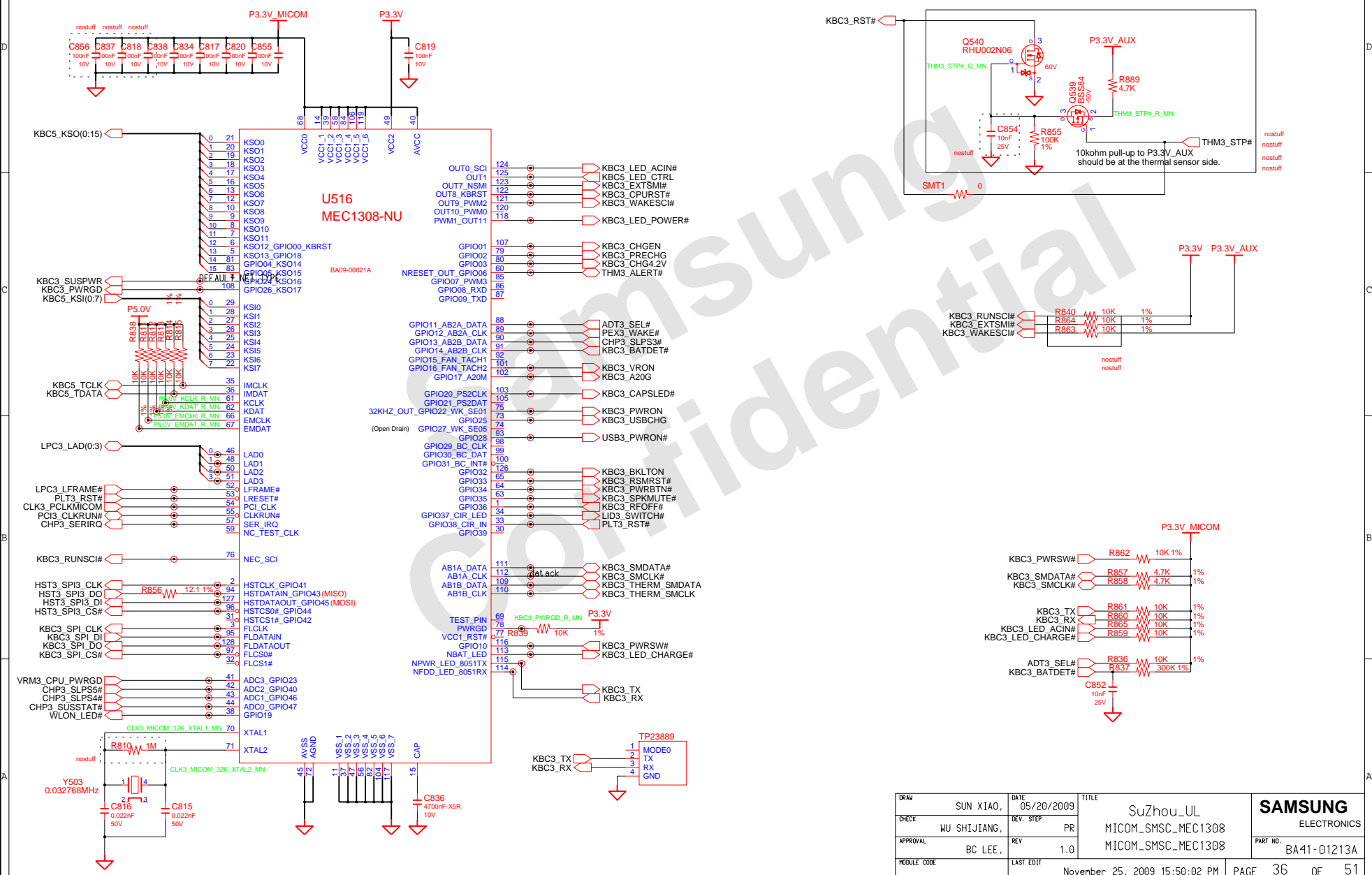


DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	SATA_DEVICES	PART NO.	
APPROVAL	BC LEE,	REV	1.0		BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	35	OF 51

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MAIN BOARD (MICOM)

MICOM POWER RESET

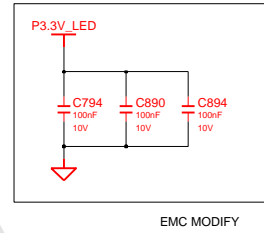
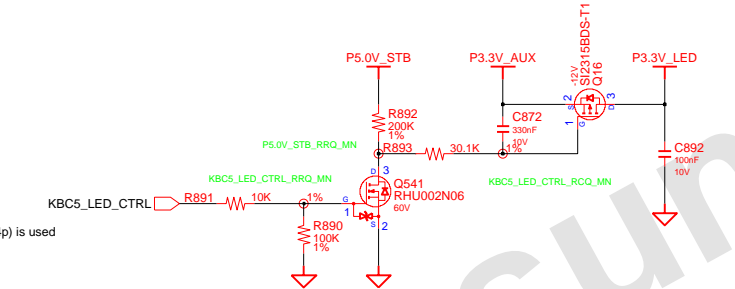
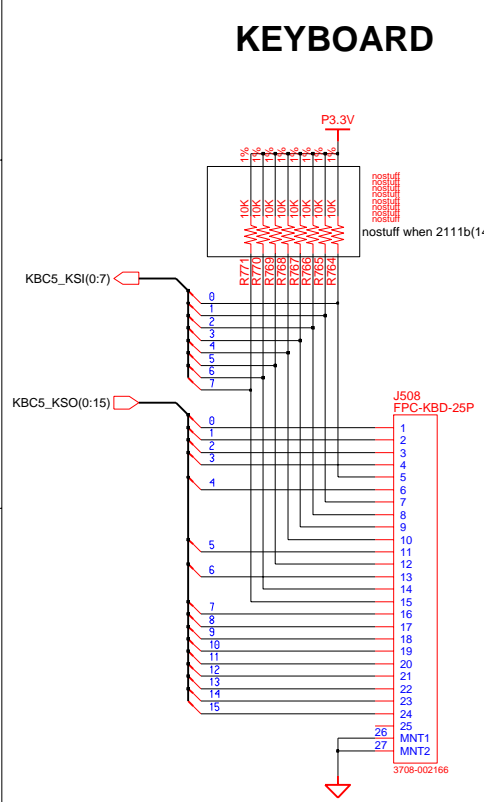


DRAWN	SUN XIAO,	DATE	05/20/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MICOM_SMSC_MEC1308	PART NO.	
APPROVAL	BC LEE,	REV	1.0	MICOM_SMSC_MEC1308	BA41-01213A	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	36	OF 51

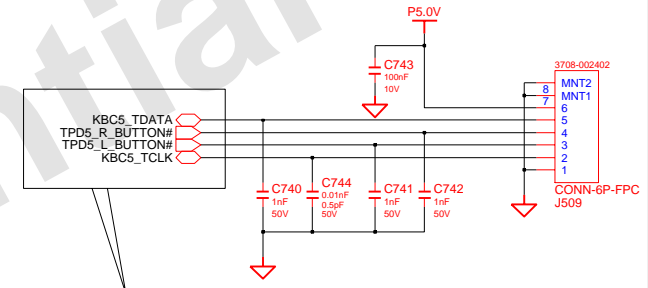
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Micom Glue Logic

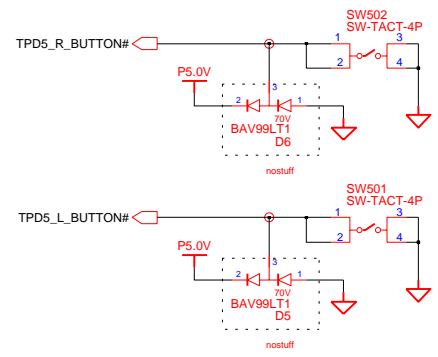
KEYBOARD



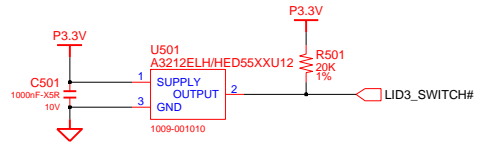
TOUCHPAD



Confirm that there are PU on Touch PAD module side & micom.



LID_SWITCH



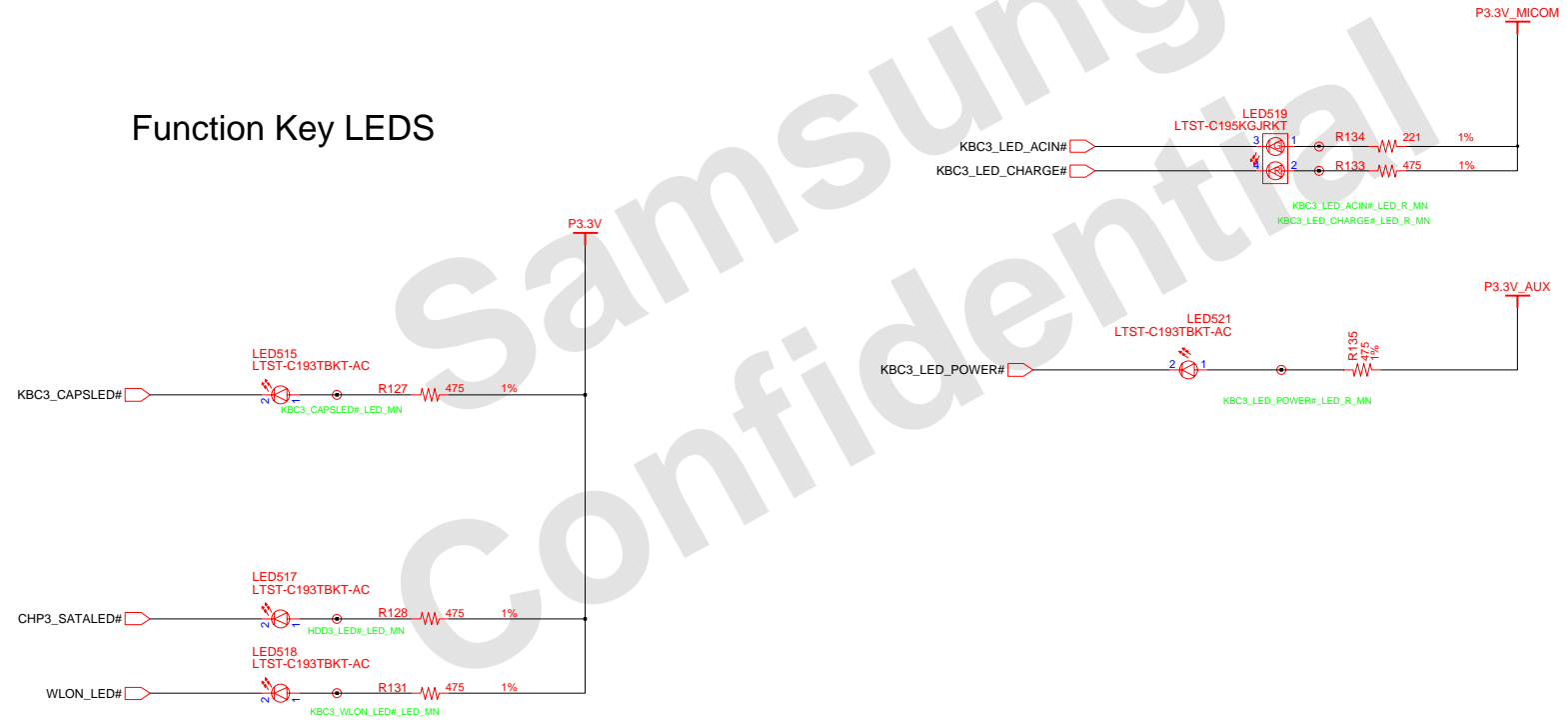
P3.3V_LED_LED1_MN	R802	475	1%	LED505	LTST-C193TBKT-AC
P3.3V_LED_LED2_MN	R797	475	1%	LED504	LTST-C193TBKT-AC
P3.3V_LED_LED3_MN	R880	475	1%	LED510	LTST-C193TBKT-AC
P3.3V_LED_LED4_MN	R888	475	1%	LED511	LTST-C193TBKT-AC
P3.3V_LED_LED5_MN	R129	475	1%	LED516	LTST-C193TBKT-AC
P3.3V_LED_LED6_MN	R126	475	1%	LED514	LTST-C193TBKT-AC
P3.3V_LED_LED7_MN	R922	475	1%	LED523	LTST-C193TBKT-AC
P3.3V_LED_LED8_MN	R910	475	1%	LED512	LTST-C193TBKT-AC
P3.3V_LED_LED9_MN	R854	475	1%	LED509	LTST-C193TBKT-AC
P3.3V_LED_LED10_MN	R809	475	1%	LED50Z	LTST-C193TBKT-AC
P3.3V_LED_LED11_MN	R800	475	1%	LED503	LTST-C193TBKT-AC
P3.3V_LED_LED12_MN	R801	475	1%	LED504	LTST-C193TBKT-AC
P3.3V_LED_LED13_MN	R920	475	1%	LED520	LTST-C193TBKT-AC
P3.3V_LED_LED14_MN	R921	475	1%	LED522	LTST-C193TBKT-AC
P3.3V_LED_LED15_MN	R798	475	1%	LED502	LTST-C193TBKT-AC
P3.3V_LED_LED16_MN	R919	475	1%	LED513	LTST-C193TBKT-AC
P3.3V_LED_LED28_MN	R818	475	1%	LED508	LTST-C193TBKT-AC
P3.3V_LED_LED29_MN	R803	475	1%	LED506	LTST-C193TBKT-AC
	R1679	475	1%	LED524	LTST-C193TBKT-AC
	R1680	475	1%	LED525	LTST-C193TBKT-AC

DESIGN	SUN XIAO,	DATE	6/27/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	37	OF 51

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LED SWITCH LOGIC

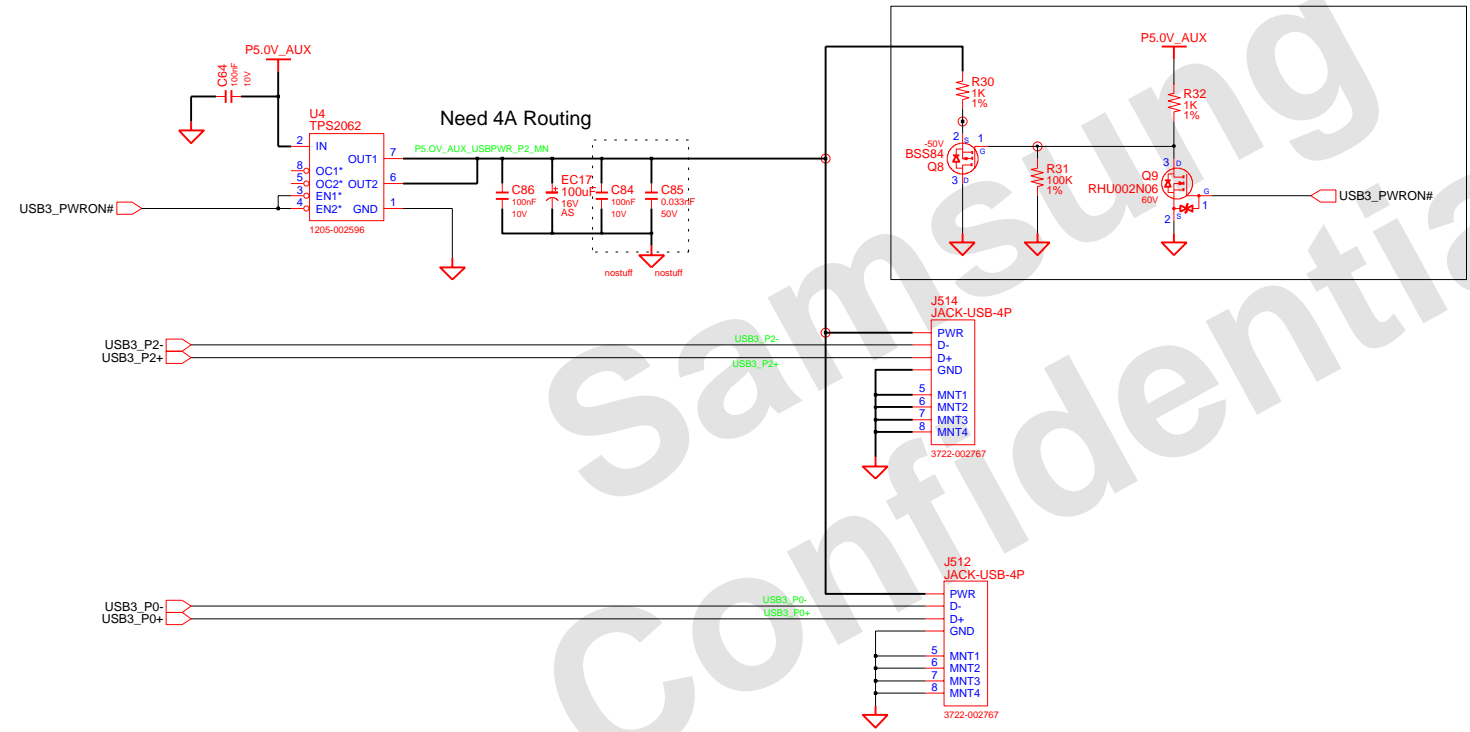
Function Key LEDs



DRAWN	SUN XIAO,	DATE	8/12/2006	TITLE	Suzhou_UL	SAMSUNG ELECTRONICS	
CHECK	WU SHUJANG,	REV. STEP	PR	LED_Switch			
APPROVAL	BC LEE,	REV	1.0	LED_Switch		PART NO.	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			BA41-01213A	
						PAGE	38
						OF	51

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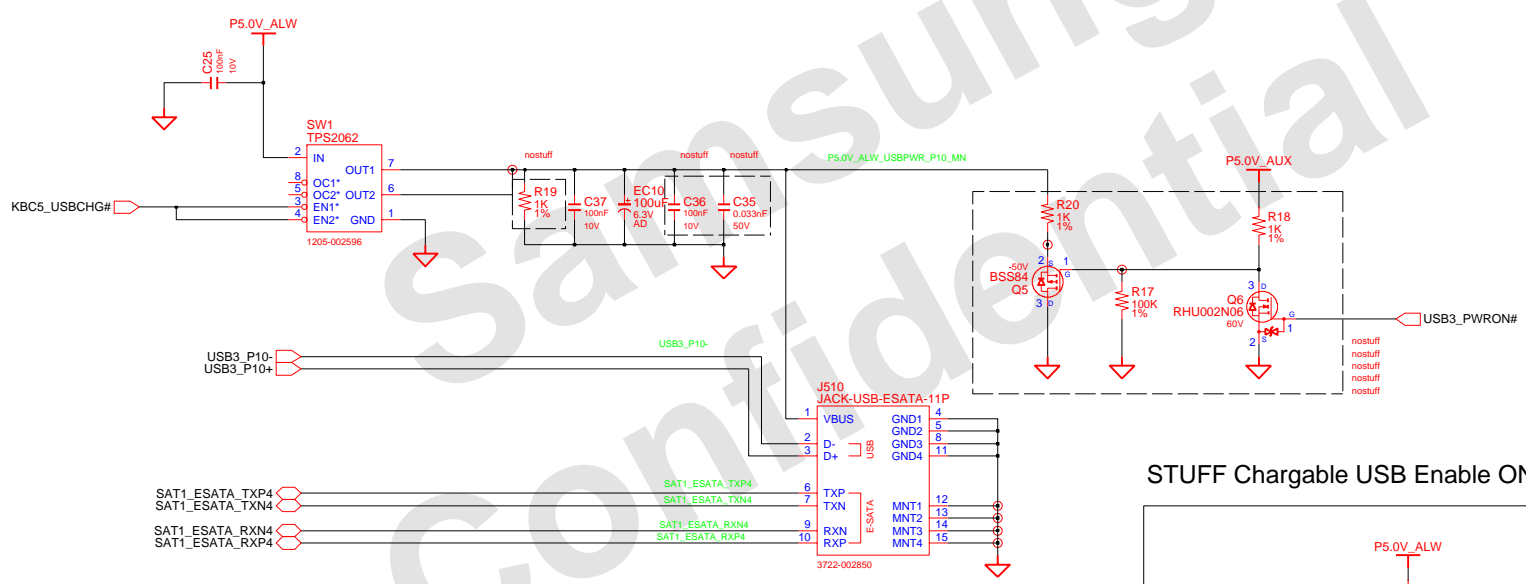
1/2 PORT USB CONNECTOR



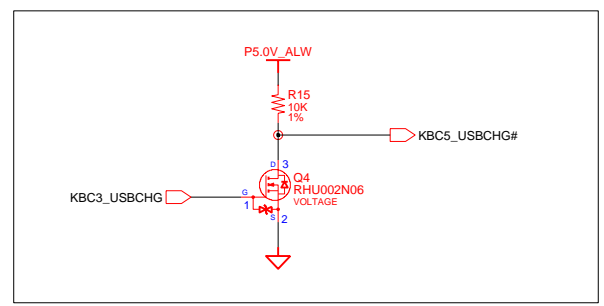
DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_UL USB_CONN	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	39	OF 51

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eSATA



STUFF Chargeable USB Enable ONLY



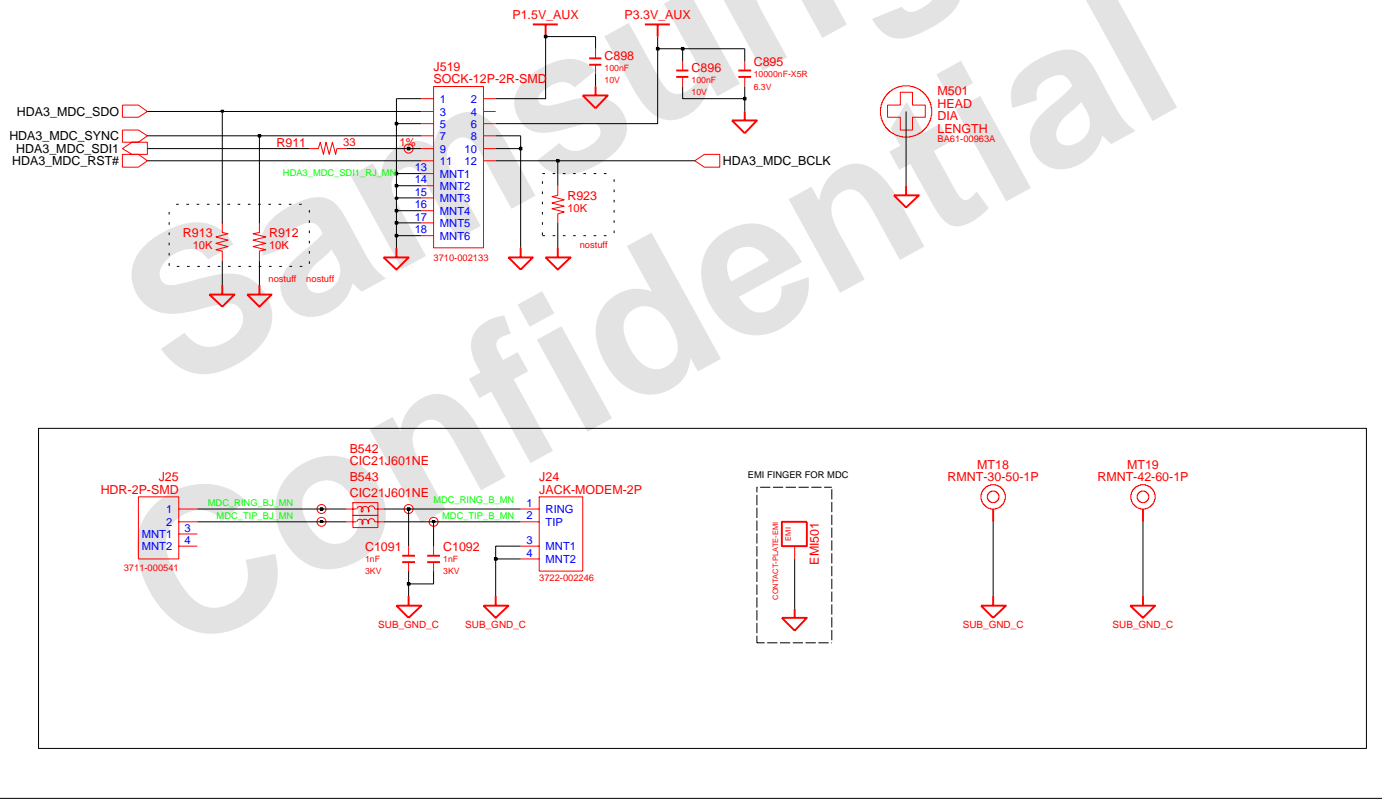
nostuff
 nostuff
 nostuff
 nostuff
 nostuff
 nostuff
 nostuff

DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	ESATA		PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	40	OF 51

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MDC

MDC Connector

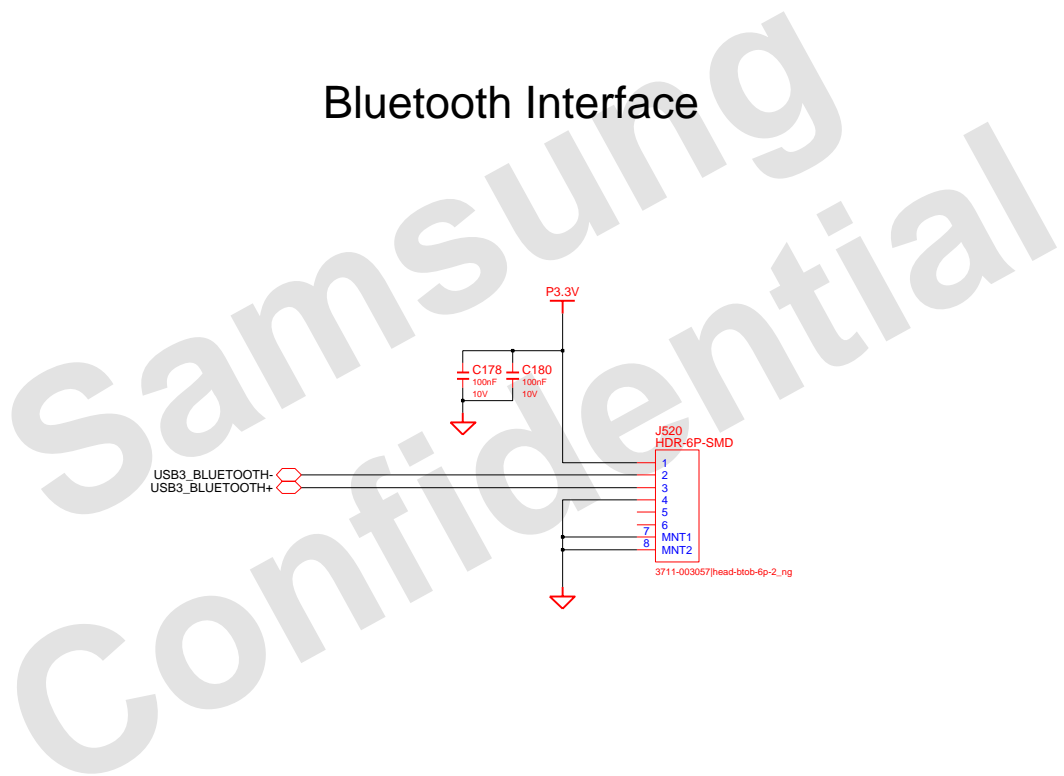


Factory Option

DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		HDA_MODEM	PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	41	OF 51

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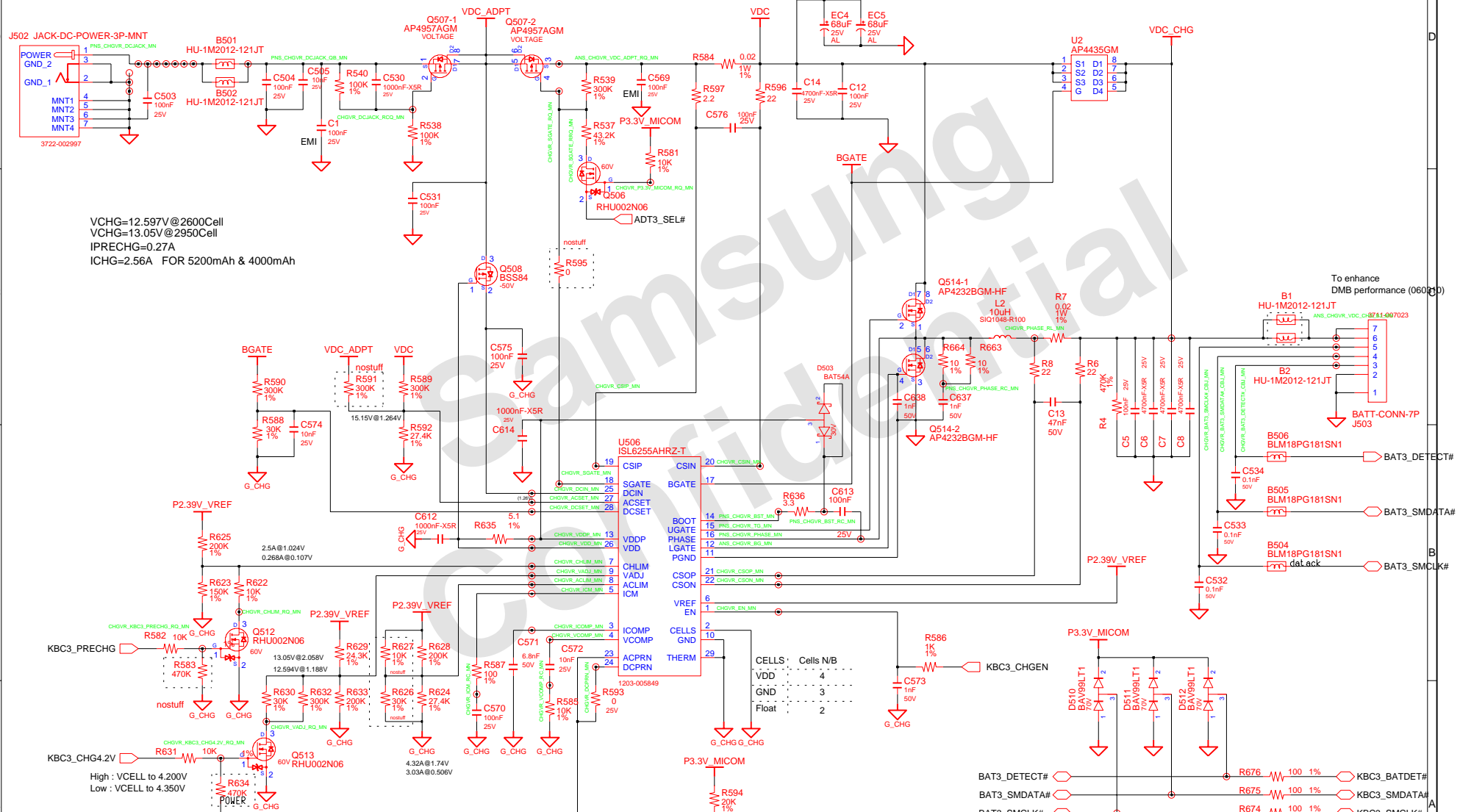
Bluetooth Interface



DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_UL USB_DEVICES	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0		PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	42	OF 51

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CHARGER & POWER MANAGEMENT



VCHG=12.597V@2600Cell
VCHG=13.05V@2950Cell
IPRECHG=0.27A
ICHG=2.56A FOR 5200mAh & 4000mAh

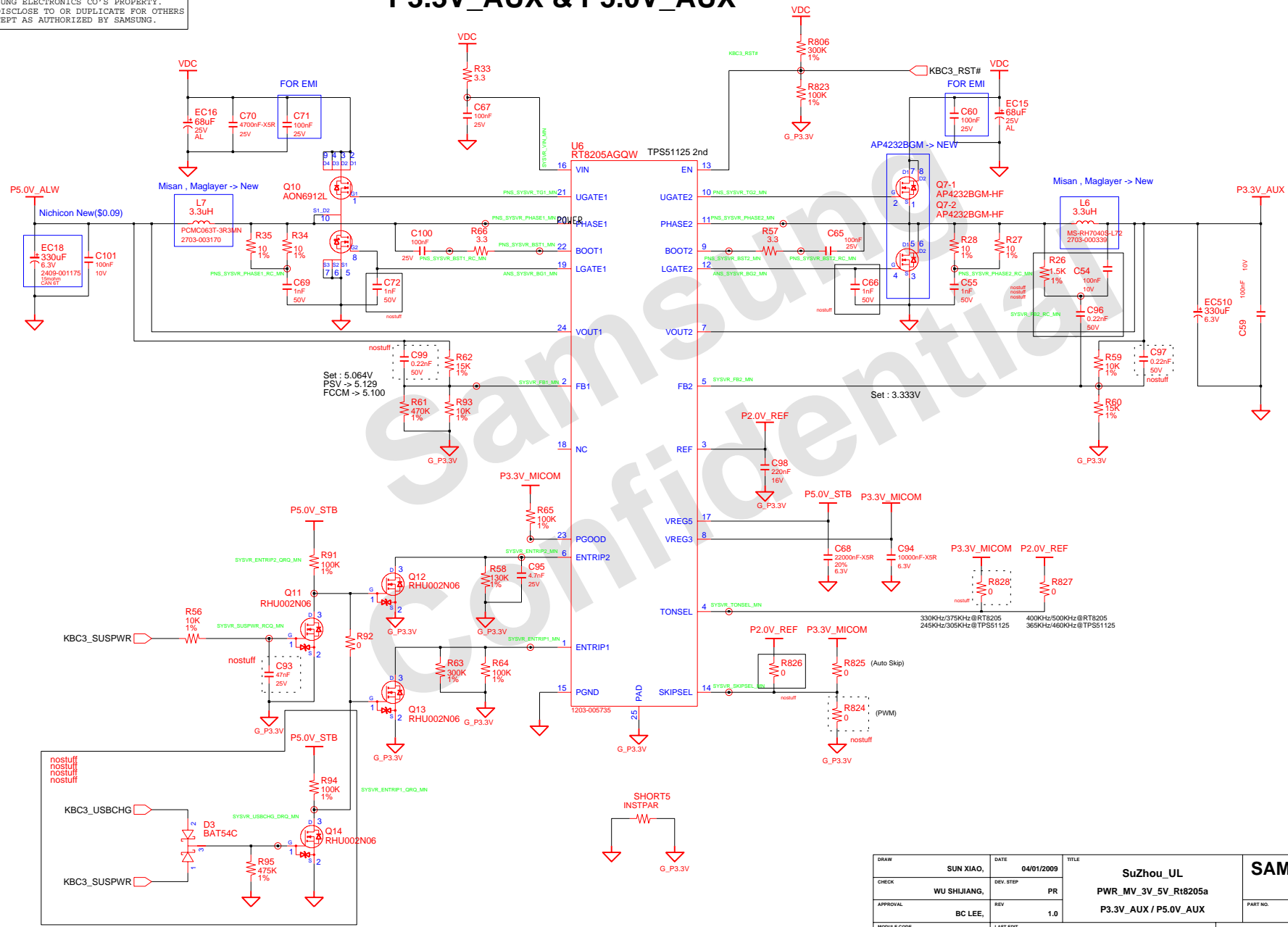
To enhance
DMB performance (06031)

Adapter configuration				
60W / 3.03A / 96%		90W / 4.32A / 91.2%		
Value	SEC Code	Value	SEC Code	
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30K	2007-008275

DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	Suzhou_UL	SAMSUNG
CHECK	WU SHUJIANG,	DEV. STEP	PR		PWR_MV_Charger_Isl6256a	ELECTRONICS
APPROVAL	BC LEE,	REV	1.0		CHARGER (ISL6256A)	PART NO.
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM			BA41-01213A
						PAGE 43 OF 51

P3.3V_AUX & P5.0V_AUX

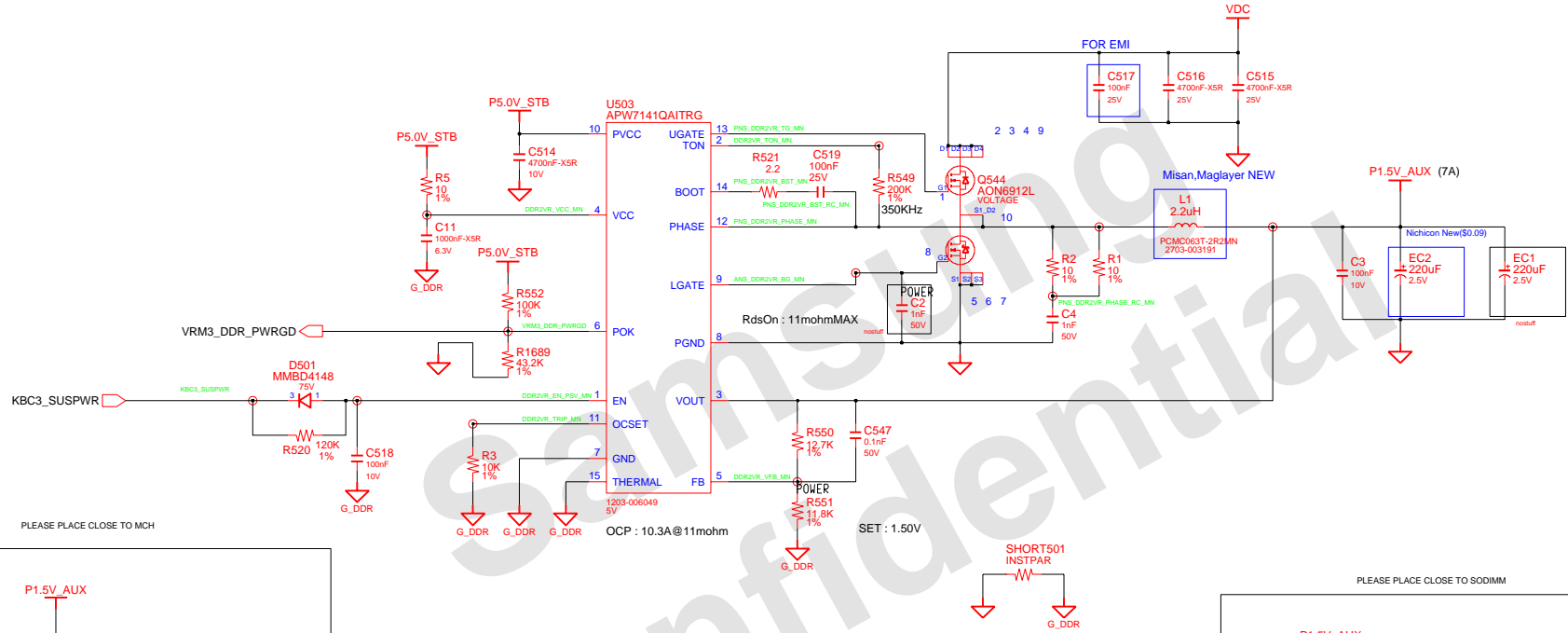
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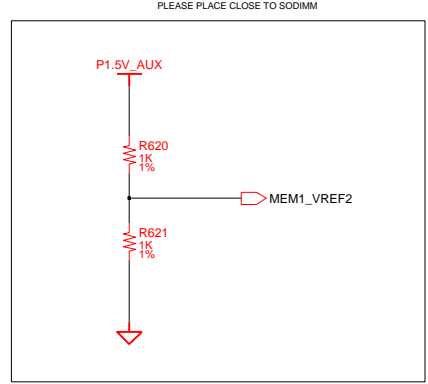
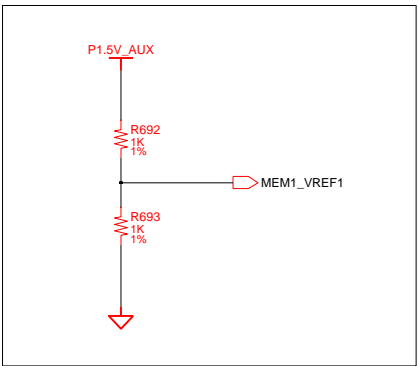
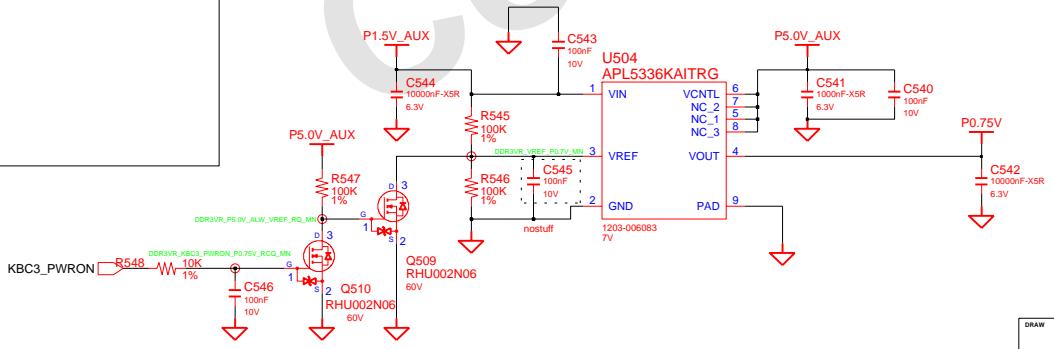
DRAW	SUN XIAO,	DATE	04/01/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	DEV. STEP	PR	PWR_MV_3V_5V_Rt8205a		
APPROVAL	BC LEE,	REV	1.0	P3.3V_AUX / P5.0V_AUX		PART NO.
MODULE CODE	undefined	LAST EDIT		November 25, 2009 15:50:02 PM	PAGE	44 OF 51

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DDR3 Power



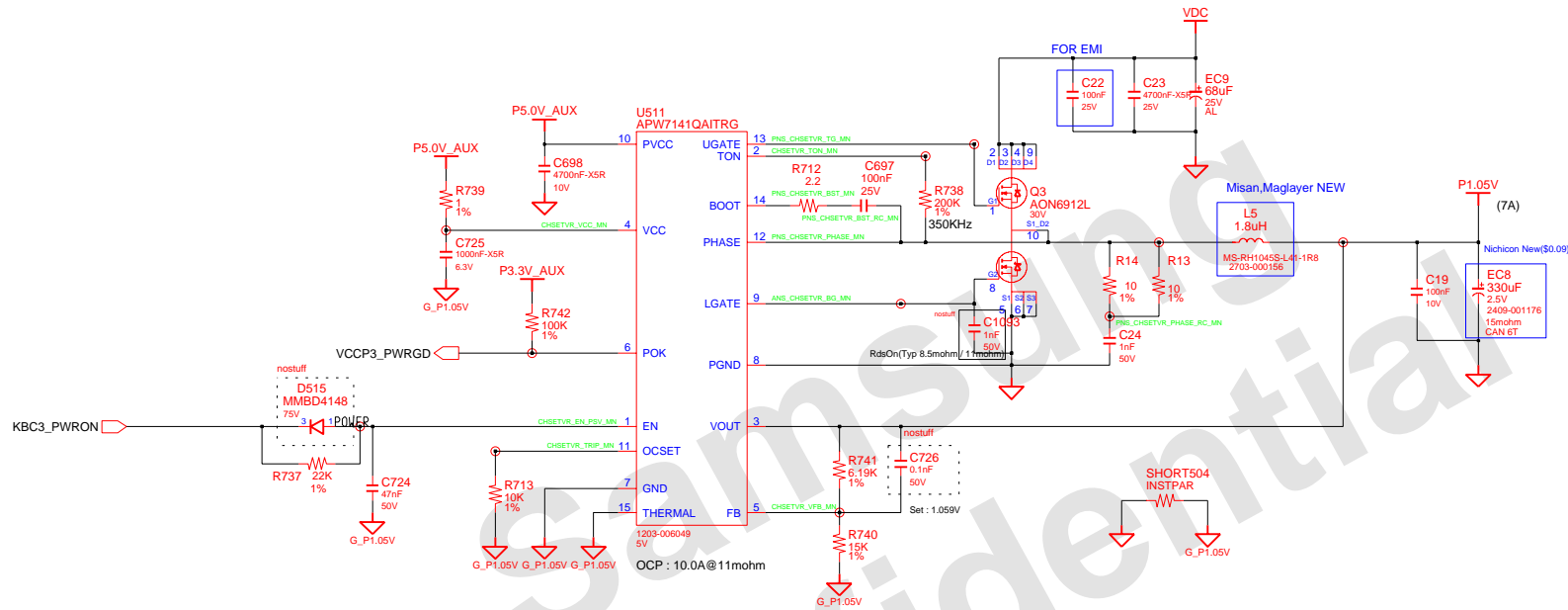
DDR3 VTT(0.75V)



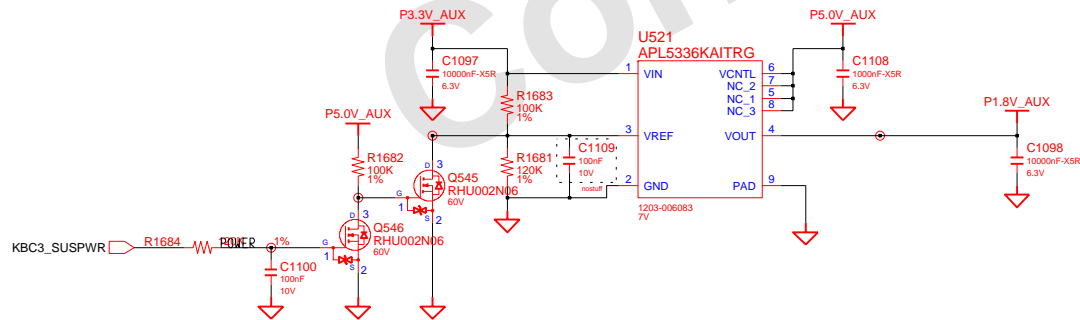
DRAW	SUN XIAO,	DATE	03/13/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	REV. STEP	PR	PWR_MV_Memory_Rt8207	PART NO.	
APPROVAL	BC LEE,	REV	1.0	DDR3 POWER (P1.5V_AUX)	BA41-01213A	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	45	OF 51

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CHIPSET POWER (P1.05V)



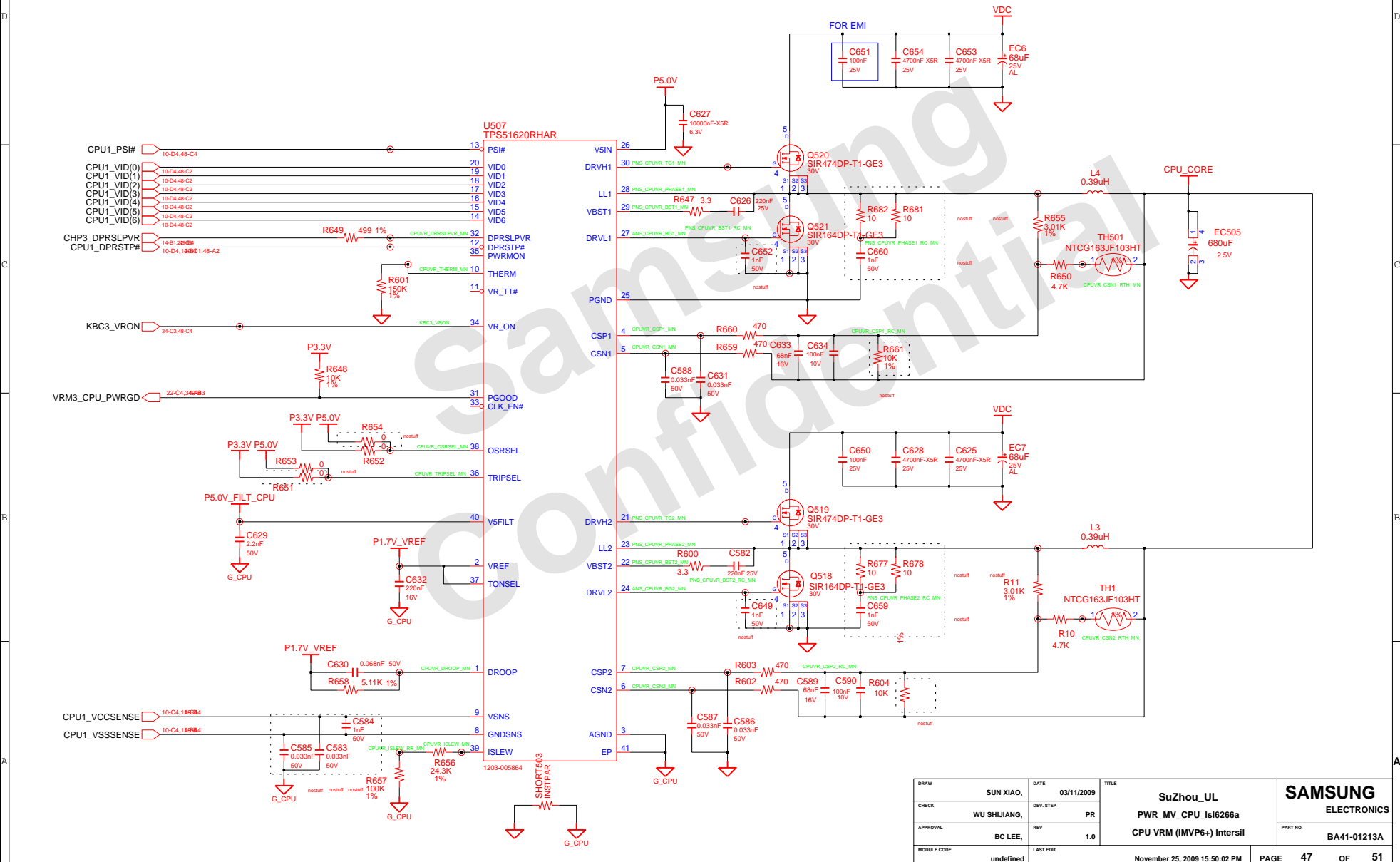
P1.8V_AUX(LDO)



DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	Suzhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	DEV. STEP	PR	PWR_MV_Cantiga	PART NO.	
APPROVAL	BC LEE,	REV	1.0	Chipset Power (P1.05V_M,P1.2V)	BA41-01213A	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	46	OF 51

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CPU VRM [TI IMVP6+]

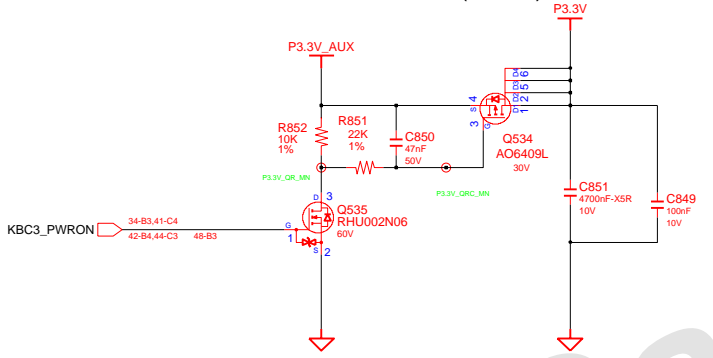


DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_UL	
CHECK	WU SHUJIANG,	DEV. STEP	PR	PWR_MV_CPU_Isi6266a		SAMSUNG ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	CPU VRM (IMVP6+) Intersil		PART NO. BA41-01213A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	47	OF 51

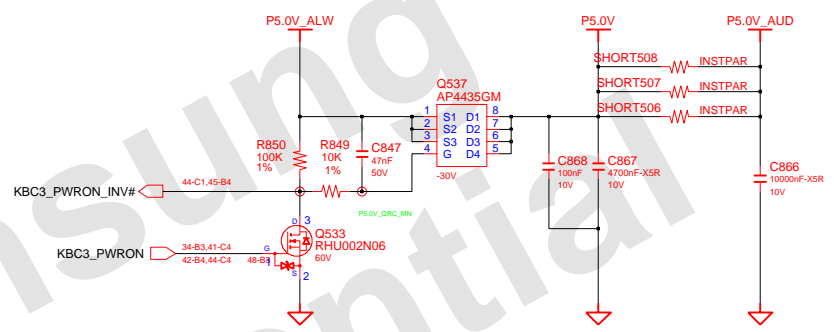
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Switched Power

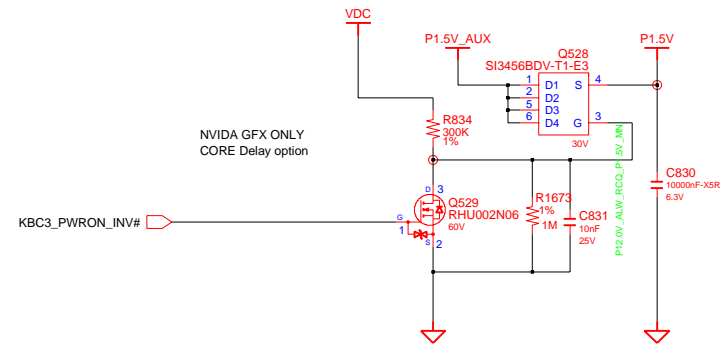
Switched Power On (P3.3V)



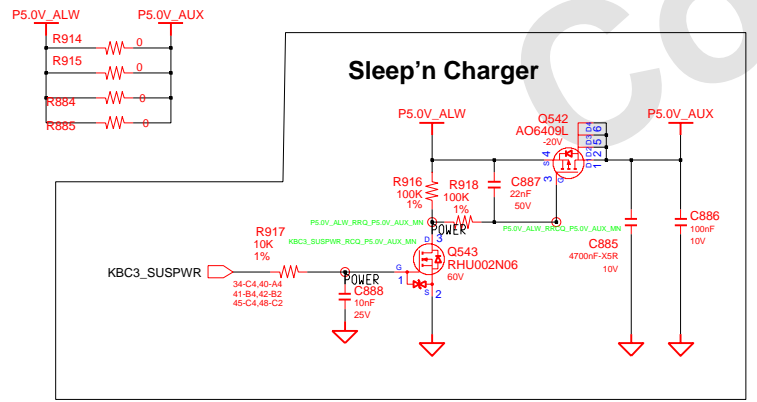
Switched Power On (P5.0V)



Switched Power On (P1.5V)



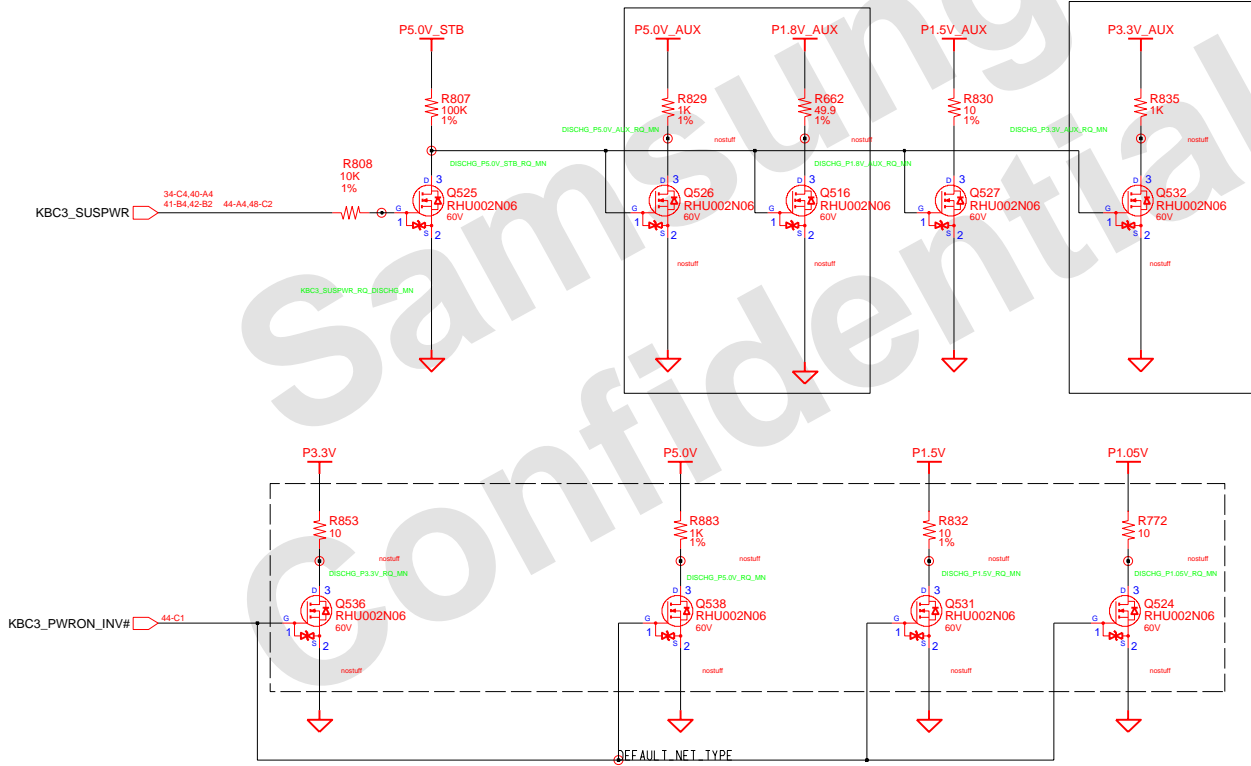
Sleep'n Charger



DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	REV. STEP	PR	PWR_MV_Switched	PART NO.	
APPROVAL	BC LEE,	REV	1.0	SWITCHED POWER	BA41-01213A	
MODULE CODE		LAST EDIT		November 25, 2009 15:50:02 PM	PAGE	48 OF 51

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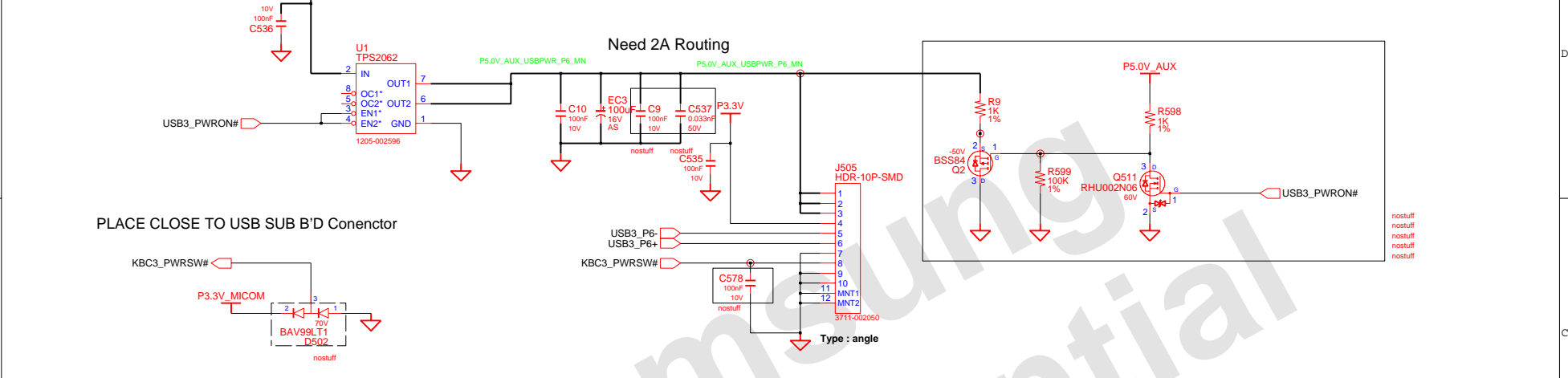
POWER DISCHARGER



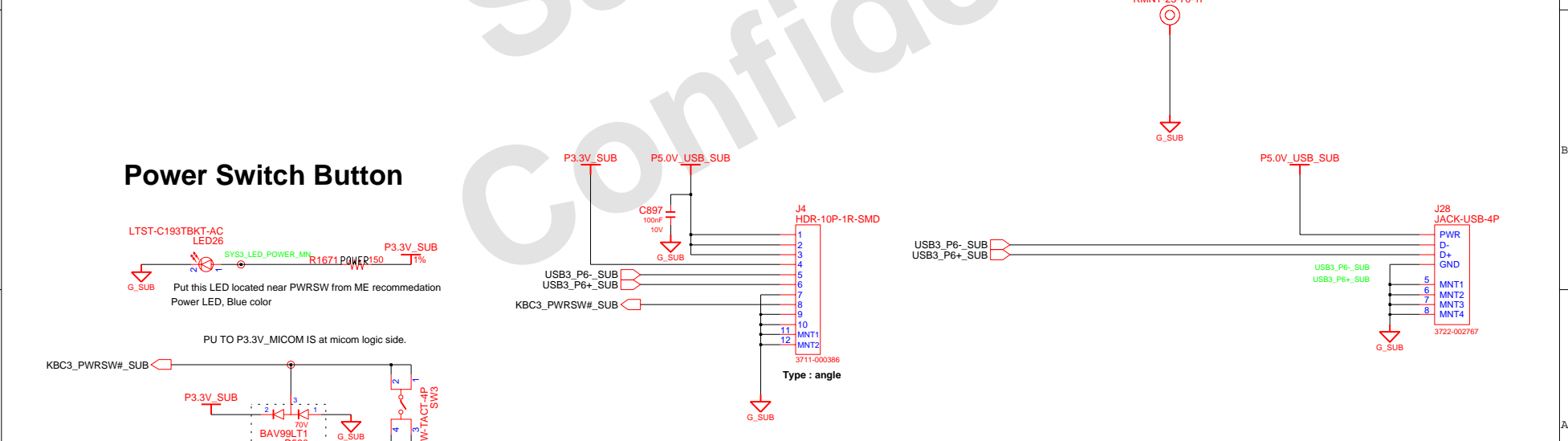
DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHUIJANG,	DEV. STEP	PR	PWR_MV_DisCharger	PART NO.	
APPROVAL	BC LEE,	REV	1.0	DISCHARGING LOGIC	BA41-01213A	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	49	OF 51

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Main Borad

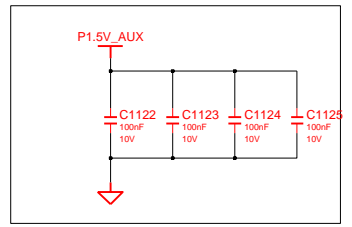
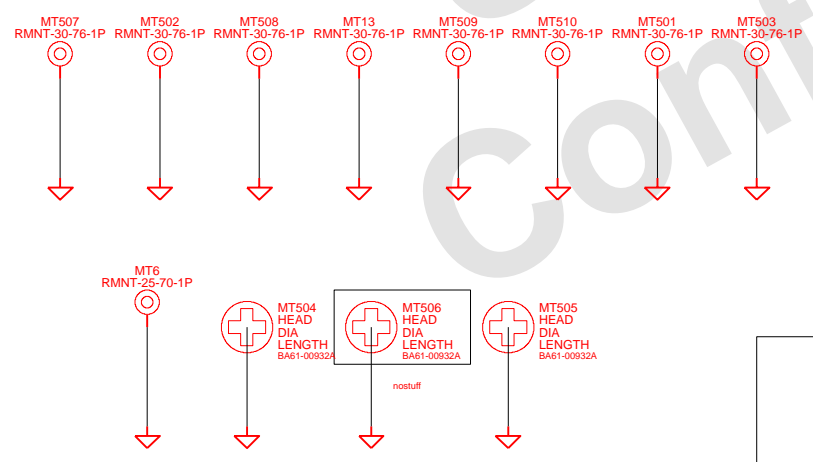
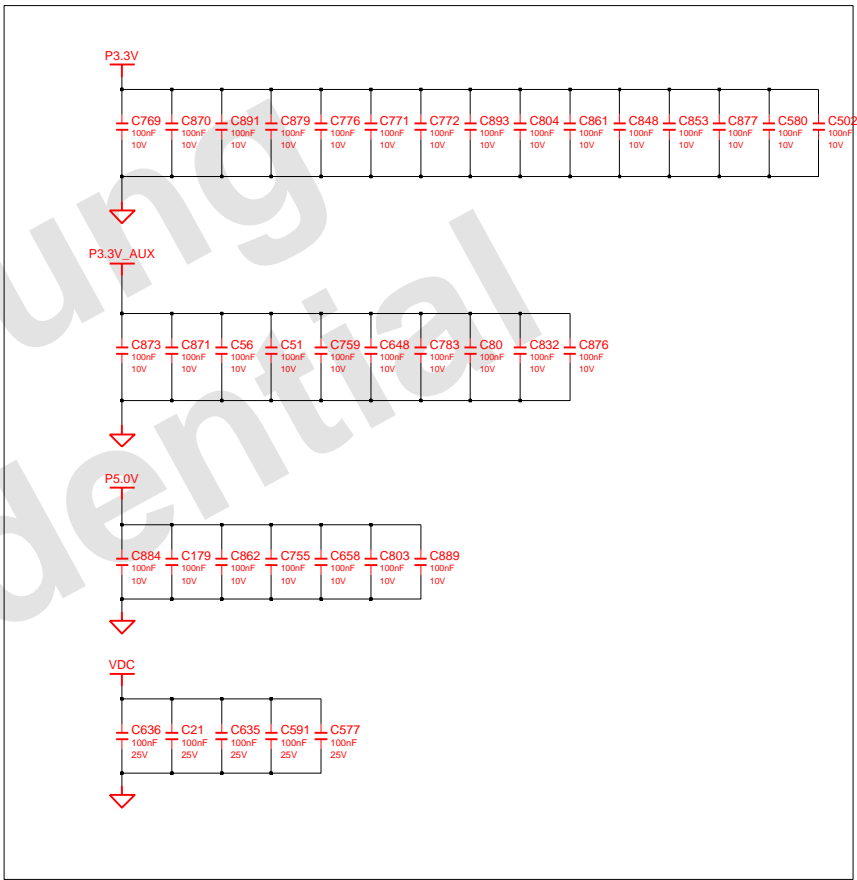
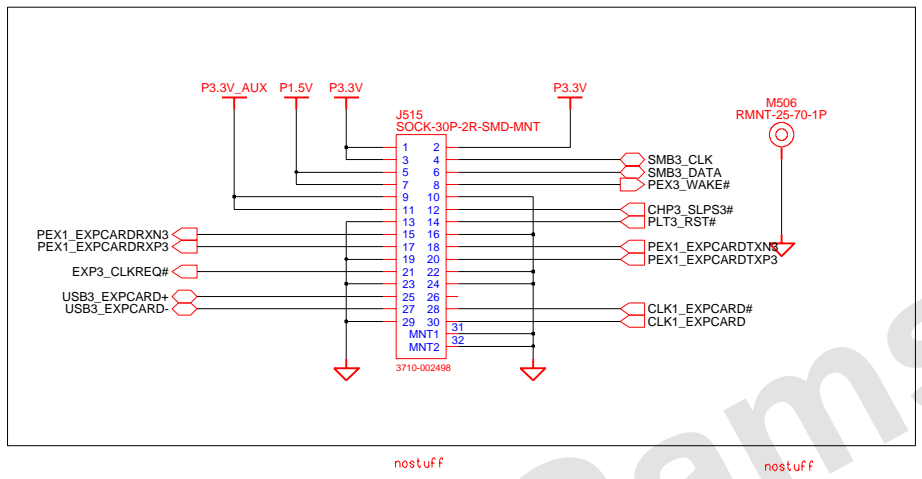


SUB Borad



DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	SUB BOARD	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	50	OF 51

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EMC MODIFY

EMC MODIFY

DESIGN	SUN XIAO,	DATE	9/9/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	BC LEE,	REV	1.0	EXPRESS CARD	BA41-01213A	PAGE 51 OF 51
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			