

R63 INTEL SYSTEM DIAGRAM

+3V/+5V S5
PG.36
+1.05V
PG.37
CPU Core
PG.40-41
DDR3L
PG.38
Charge
PG.35
Dis-Charge
PG.39
+VGACORE
PG.42
+1.5 VGA
PG.43
+1.0V/+1.8/ +3 VGA
PG.44

SODIMM1
Max. 4GB
PG.12

1600MT/s
DDR3 L
Channel A

SODIMM2
Max. 4GB
PG.13

1600MT/s
DDR3 L
Channel B

INTEL Haswell
Processor : Dual / Quad Core
Power : 37 / 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)

PG.2-5

AMD
Mars / SUN XT
29mm X 29mm
TDP 35W / 25W

PG.14-20

VRAM
128Mx16x8,128bit
PG.21-22

HDD PG.33

SATA0

ODD PG.33

SATA1

INTEL PCH Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)

PG.6-11

RTD 2136 S/R
DP to LVDS Converter
PAGE 23

LVDS

PG.25

HDMI

PG.26

CRT

PG.25

PCI-E x 1

LAN
RTL8166EH
10/100
PG.30

LANE2

LANE1

WLAN
BT COMBO
PG.34

USB 2.0
PORT10

PCI-E x 1

Accelerometer
PG.34

LANE3

Card Reader
RTS5237
PG.27

SMBUS

KBC
EnE KB3940QF A1
PG.31

LPC

KB PG.32

TP PG.32

ROM PG.31

FAN PG.32

USB 3.0

USB3.0 Ports X2
PG.29

Webcam
PG.25

USB 2.0

PORT1, 2

PORT4

USB2.0 Ports
PG.29

PORT0, 1

AUDIO CODEC
ALC 3227
PG.28

Speaker
PG.28

HP/MIC
PG.29

Analog MIC
PG.29

Stackup

TOP


GND

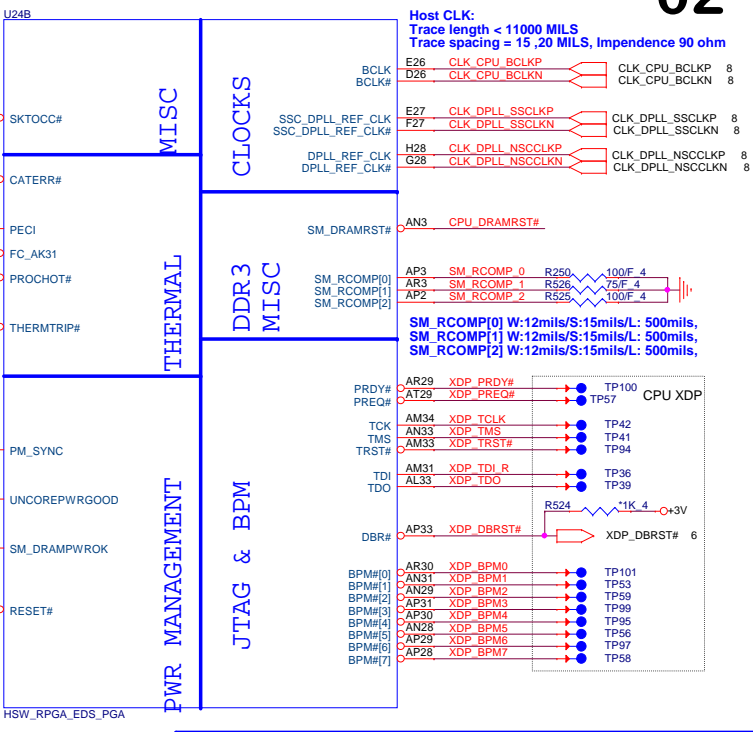
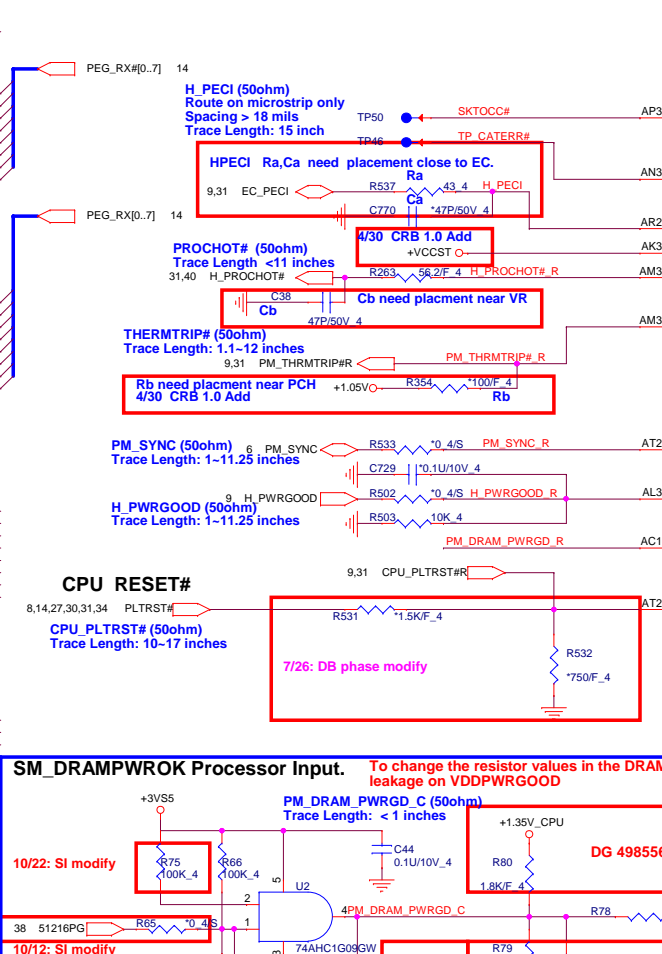
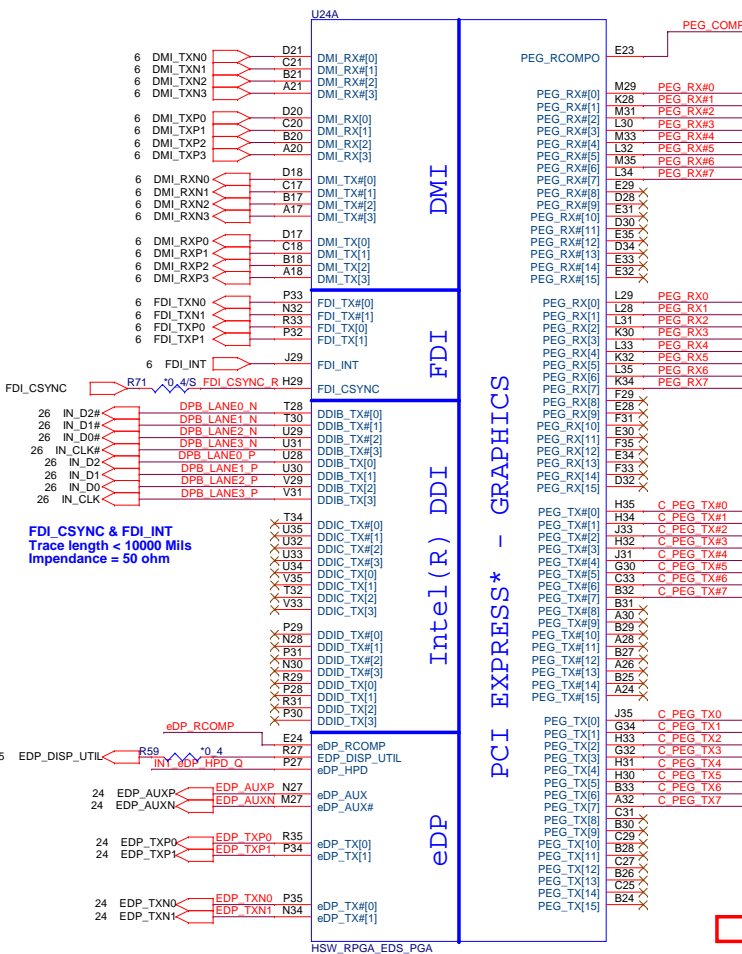
IN1

IN2

VCC

BOT

	PROJECT : R63 Quanta Computer Inc.		Rev 1A
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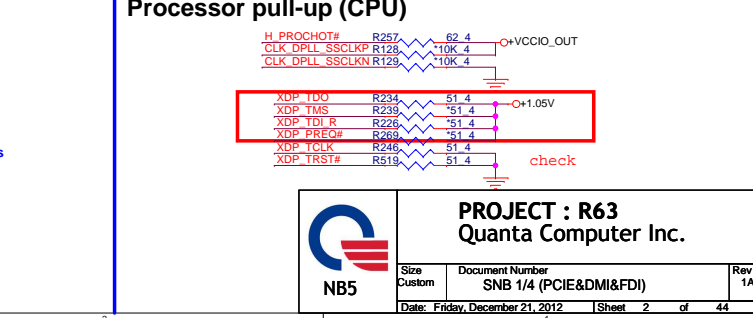
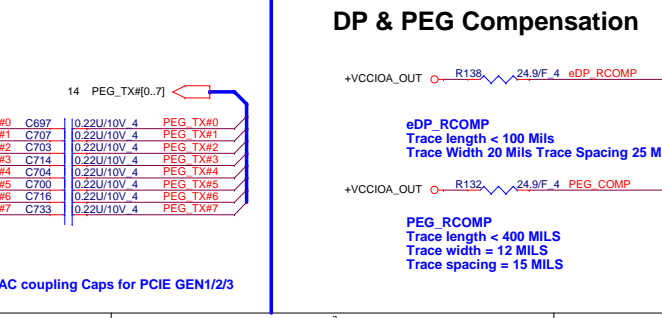
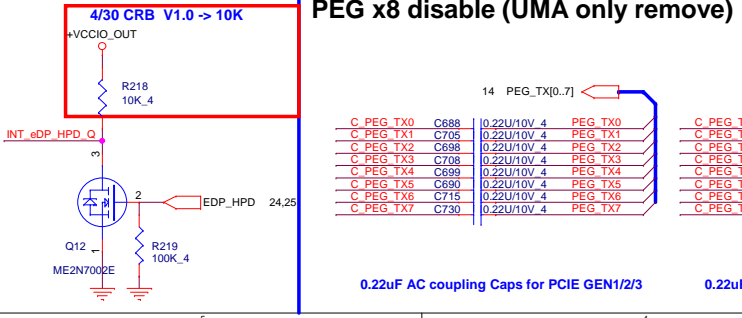
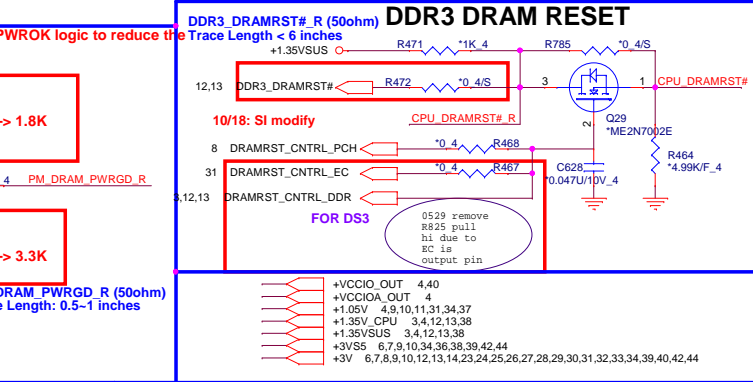
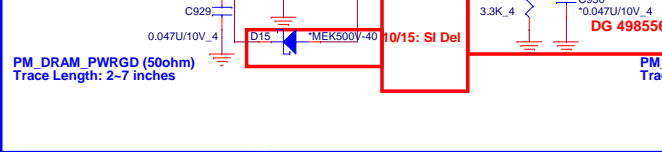
Host CLK:
Trace length < 11000 MILS
Trace spacing = 15_20 MILS, Impedence 90 ohm

- E26 CLK CPU BCLKP
- D26 CLK CPU BCLKN
- E27 CLK DPPLL SSCLKP
- F27 CLK DPPLL SSCLKN
- H28 CLK DPPLL NSCLKP
- G28 CLK DPPLL NSCLKN

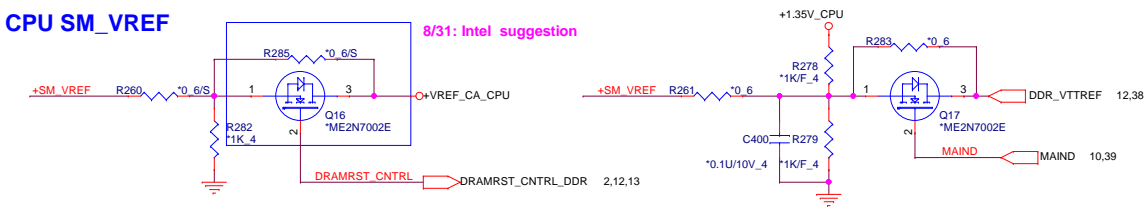
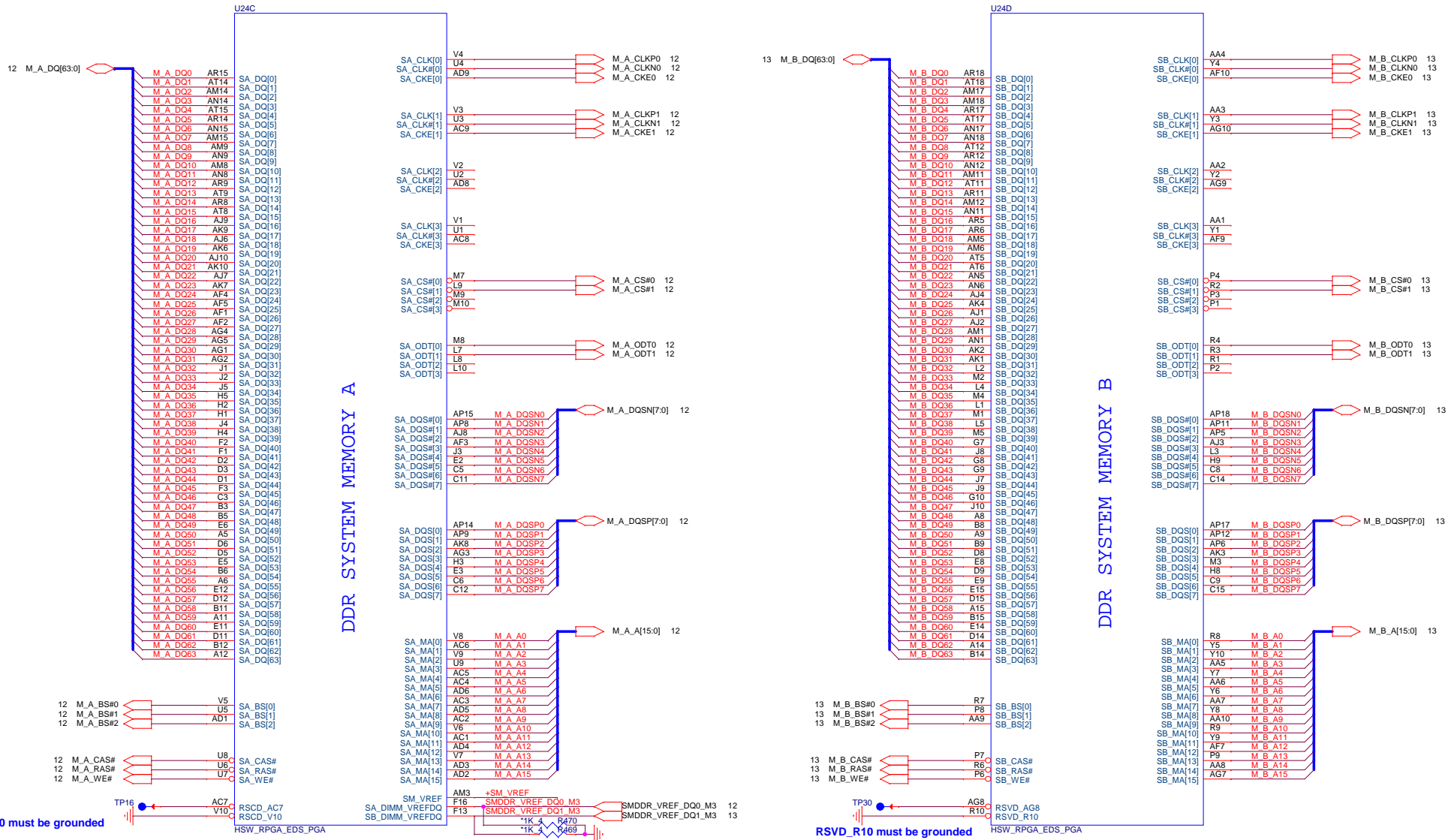
SM_RCMP0[W:12mils/S:15mils/L: 500mils,
SM_RCMP1[W:12mils/S:15mils/L: 500mils,
SM_RCMP2[W:12mils/S:15mils/L: 500mils,

CPU XDP

- TP100
- TP57
- TP42
- TP41
- TP94
- TP36
- TP39
- TP101
- TP53
- TP59
- TP99
- TP95
- TP56
- TP97
- TP58



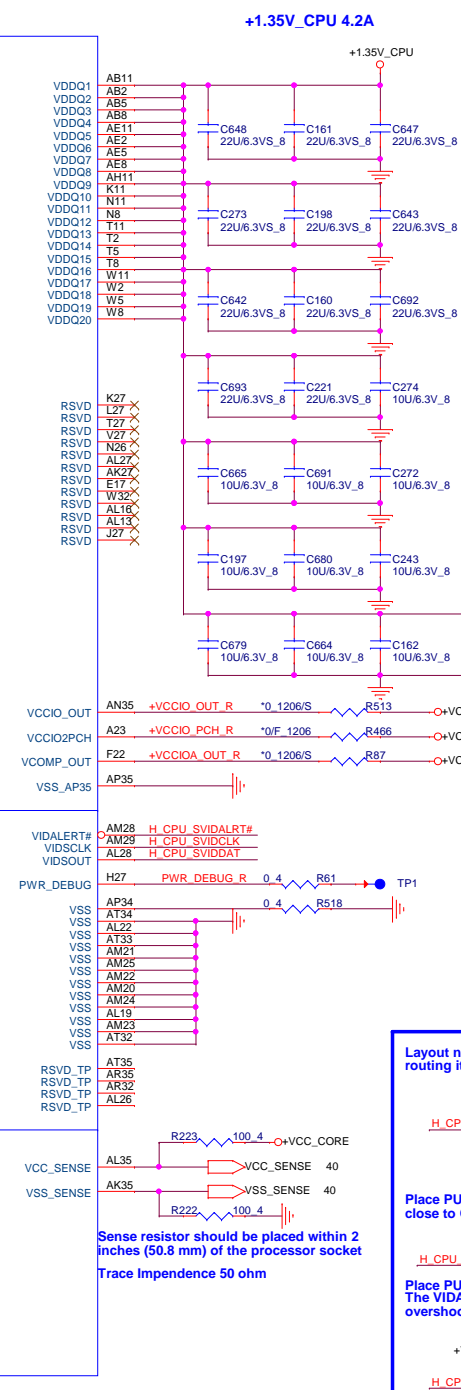
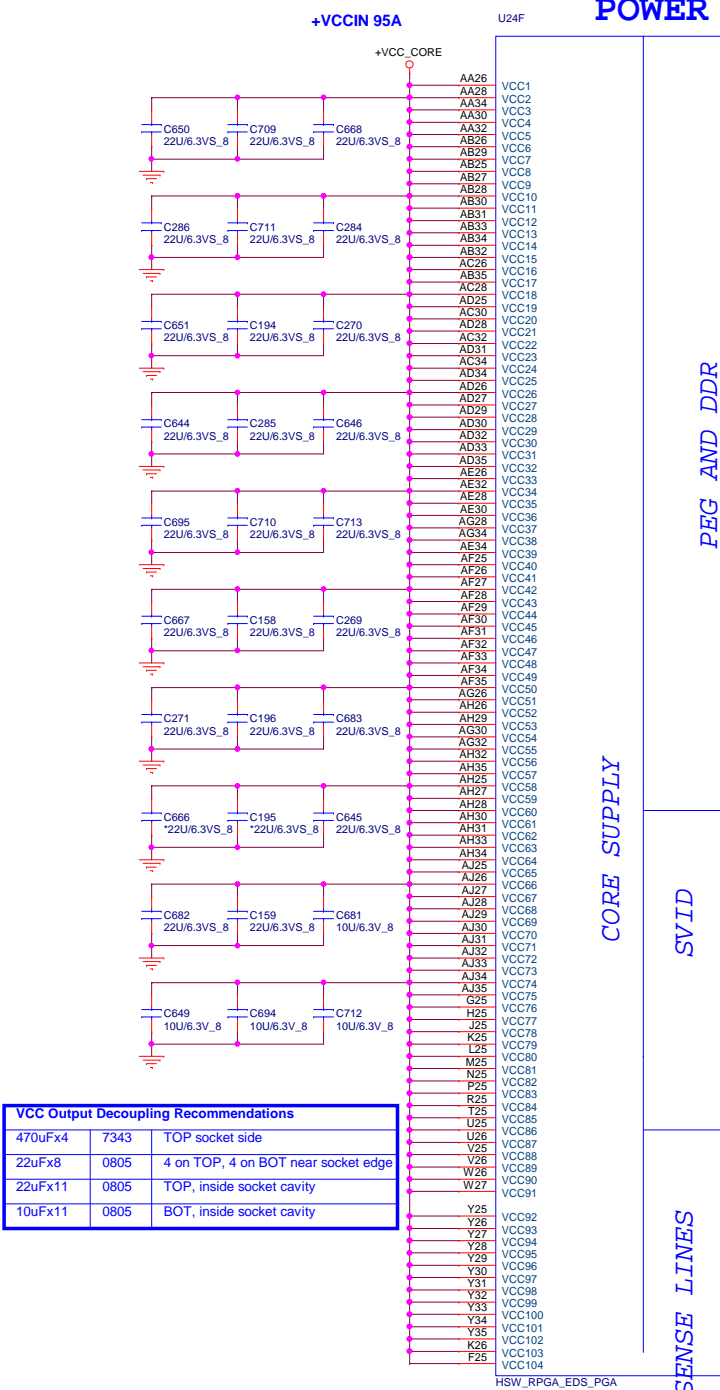
Haswell Processor (DDR3)



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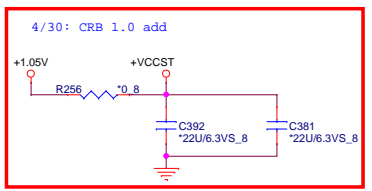
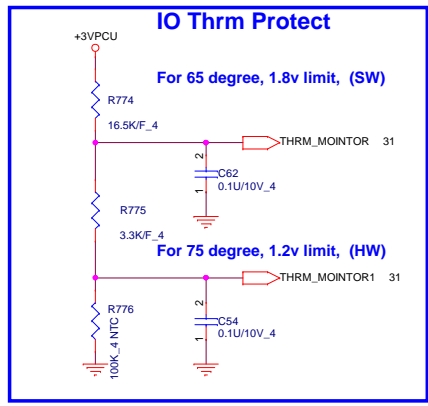
Haswell Processor (POWER)



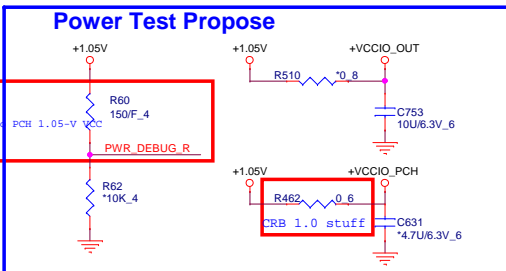
VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

- +VCCIO_OUT 2
- +VCCIO_OUT 2,40
- +VCCIO_PCH 10
- +1.5V 6,7,8,10,28,34,38,44
- +1.35V_CPU 2,3,12,13,38
- +1.05V 2,9,10,11,31,34,37
- +VCC_CORE 40,41
- +VCCST 2
- +1.35VSUS 2,3,12,13,38

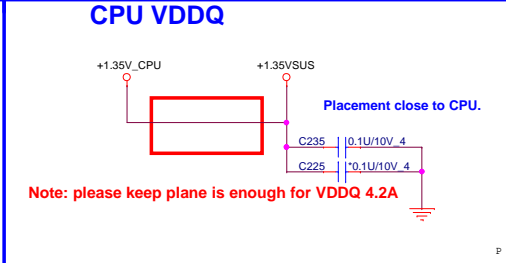
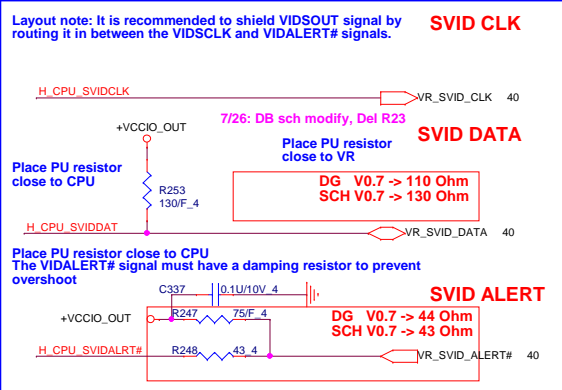


4/30: DG 498550
Haswell PWR_DEBUG requires a 150-ohm pull-up resistor to Core when routed to XDP



VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

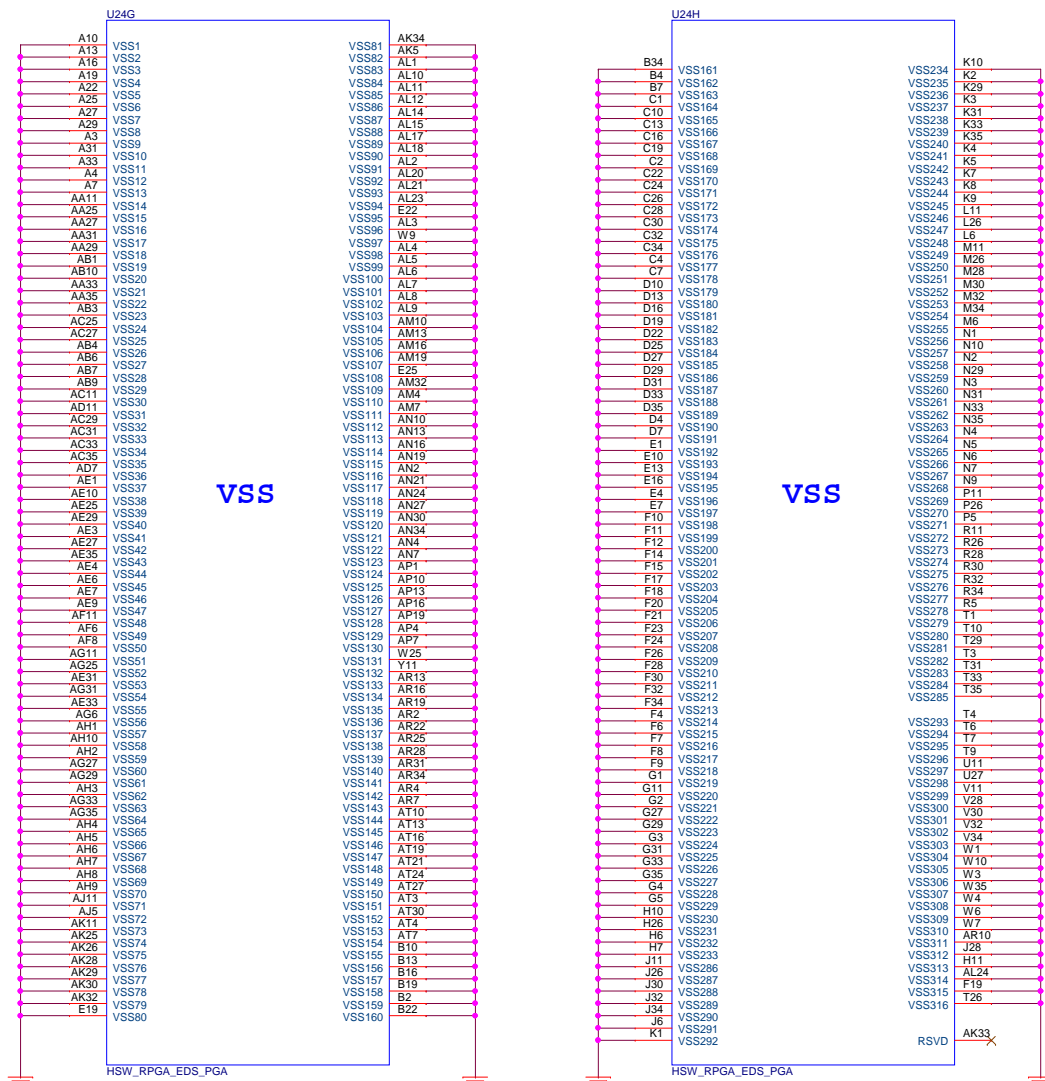


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NBS

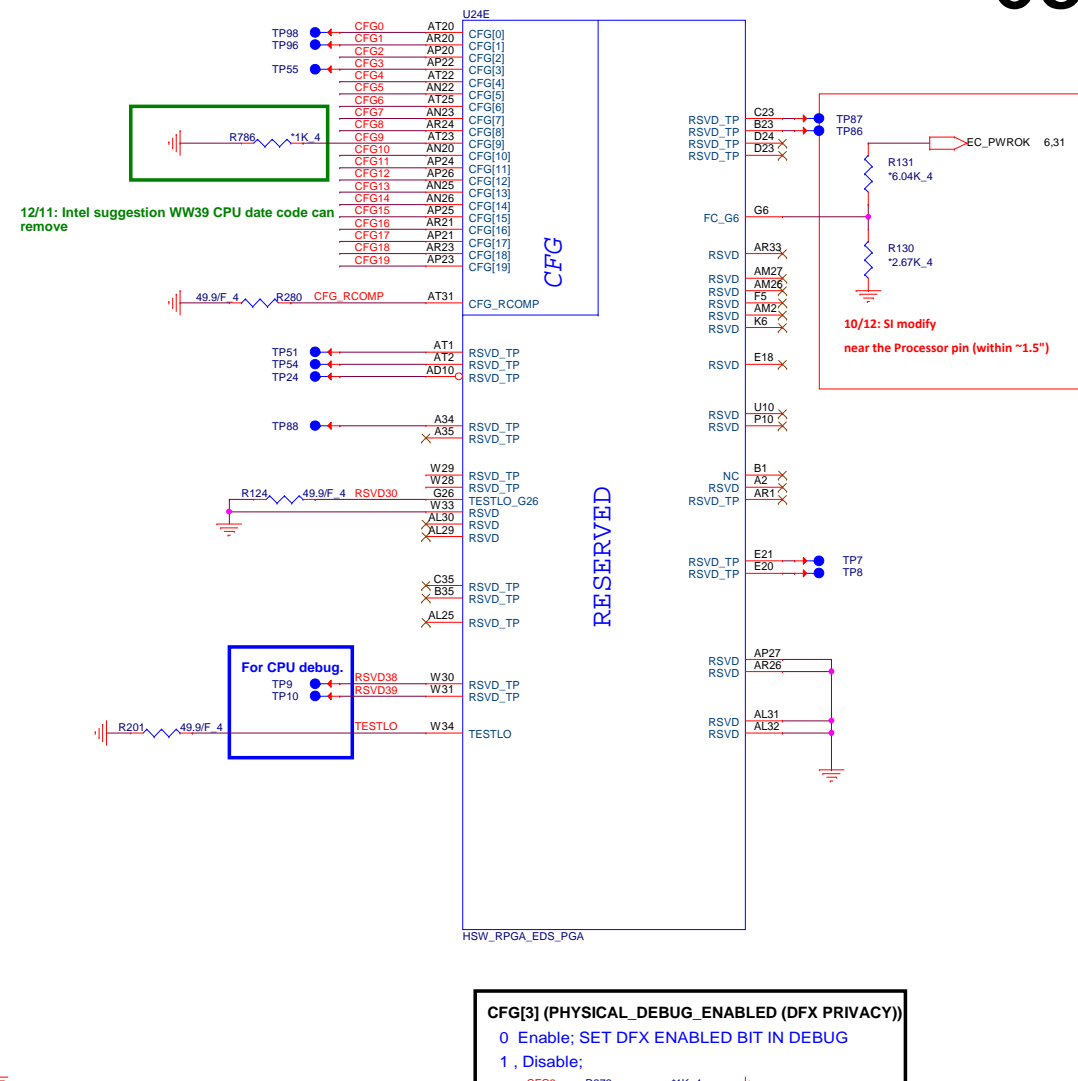
Size	Document Number	Rev
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Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)

05



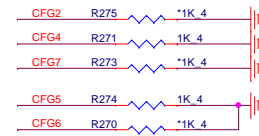
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))
 0 Enable; SET DFX_ENABLED BIT IN DEBUG
 1, Disable;

CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

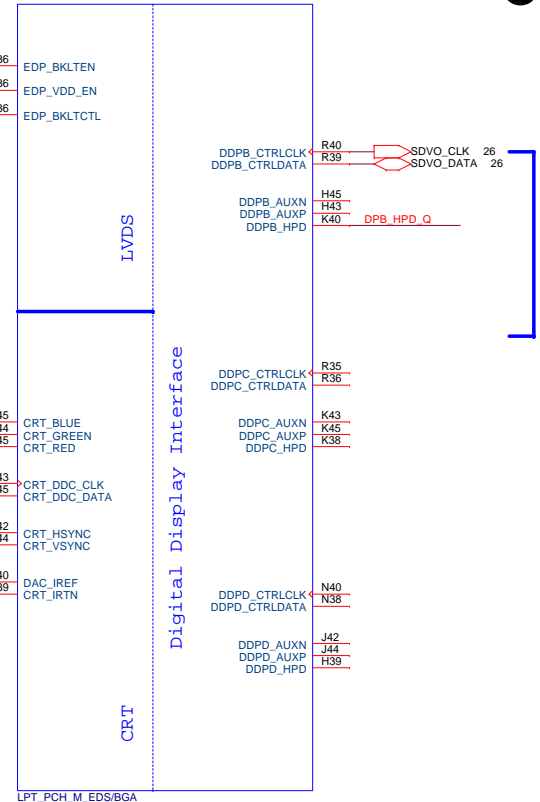
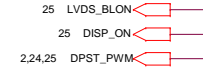
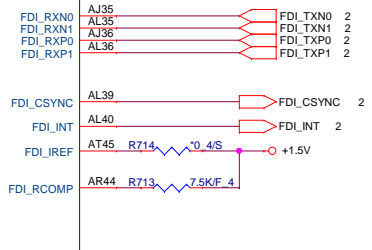
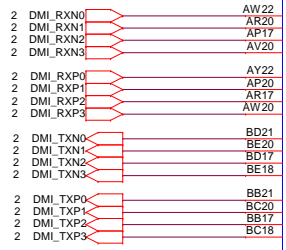


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U33C

U33D



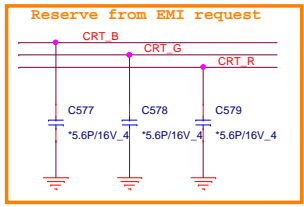
INT - HDMI

Digital Display Interface

PD Res place close to PCH
PCH to Res routing 37.5 ohm Impedance.
Res to connector filter routing 50ohm Impedance.

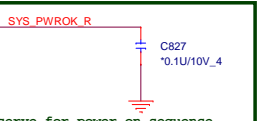
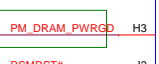
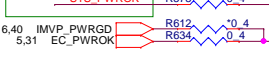
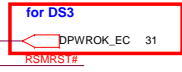
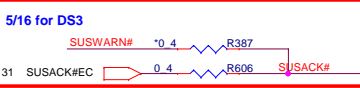
DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm

DAC_IREF (50ohm)
Trace length = 500 MILLS
Trace spacing = 30 MILLS



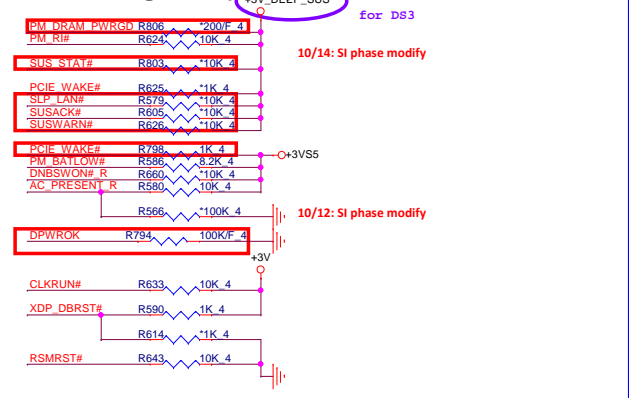
- +3V_DEEP_SUS 7,8,9,10,39
- +3V_RTC 7,10,11
- +1.05V 2,4,9,10,11,31,34,37
- +3VPCU 4,7,9,11,25,31,32,34,35,36
- +3VS5 2,7,9,10,34,36,38,39,42,44
- +3V 2,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
- +5V 7,23,26,28,29,32,33,34,39

System Power Management

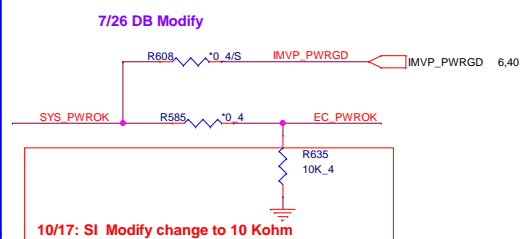


Reserve for power on sequence

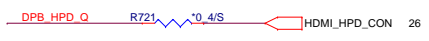
PCH Pull-high/low(CLG)



System PWR_OK(CLG)



INT HDMI Detect Function



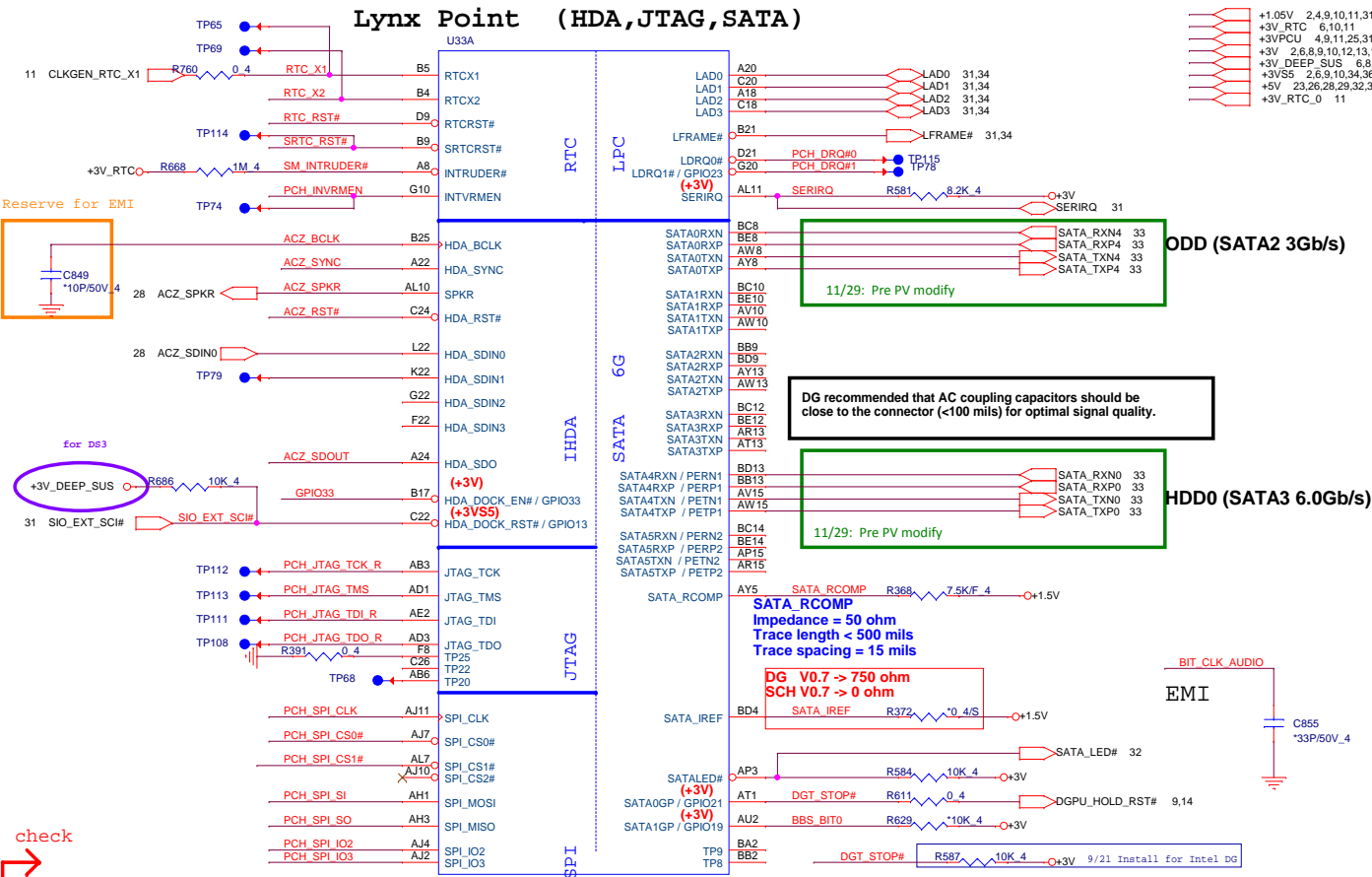
On Die DSW VR Enable
High = Enable (Default)
Low = Disable



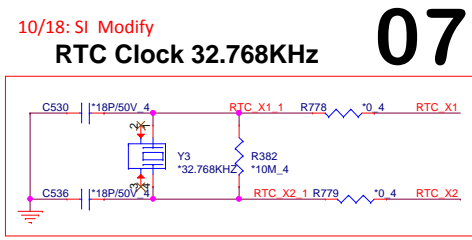
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Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)	Rev 1A
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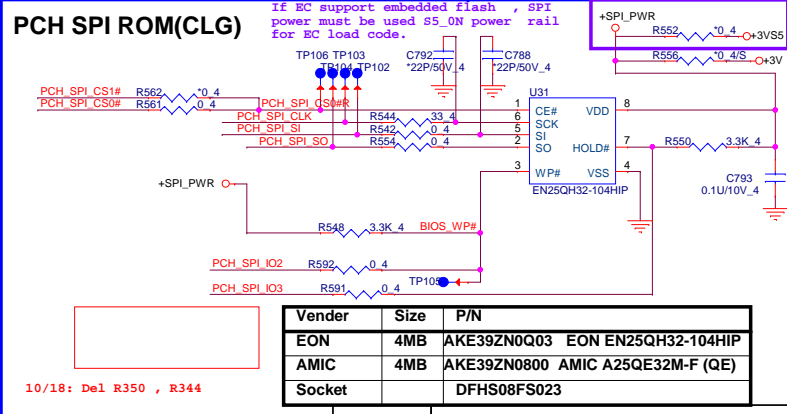
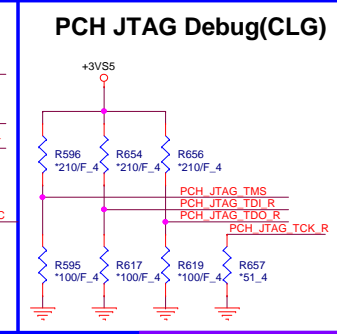
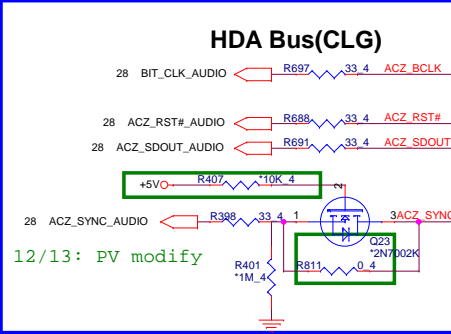
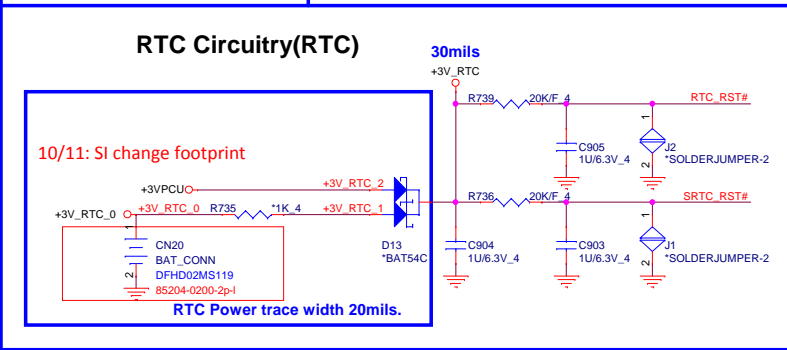
Lynx Point (HDA, JTAG, SATA)



- +1.05V 2,4,9,10,11,31,34,37
- +3V_RTC 6,10,11
- +3VPCU 4,9,11,25,31,32,34,35,36
- +3V 2,6,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
- +3V_DEEP_SUS 6,8,9,10,39
- +3VSS 2,6,9,10,34,36,38,39,42,44
- +5V 23,26,28,29,32,33,34,39
- +3V_RTC_0 11



07



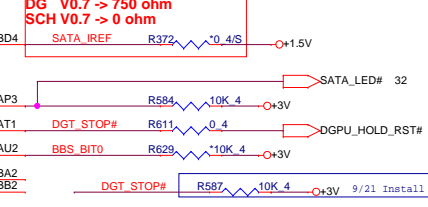
Vender	Size	P/N
AMIC	4MB	AKE392N0Q03 EON EN25QH32-104HIP
AMIC	4MB	AKE392N0800 AMIC A25QE32M-F (QE)
Socket		DFHS08F5023

11/29: Pre PV modify

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

11/29: Pre PV modify

SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R569 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R563 *1K 4 PCL_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R389 *330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Intelposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R680 *0.4 2 +3V 10/18: SI Modify
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R613 *1K 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R390 *1K 4 BBS_BIT1 8
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R684 *1K 4 ACZ_SYNC 12/13: PV modify
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overriden	GPIO33_E R693 *1K 4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internal PU	R621 *1K 4 BT_OFF# 9,34
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R571 *1K 4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R374 *1K 4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	R564 *1K 4 PCH_SUSCLK 6,31

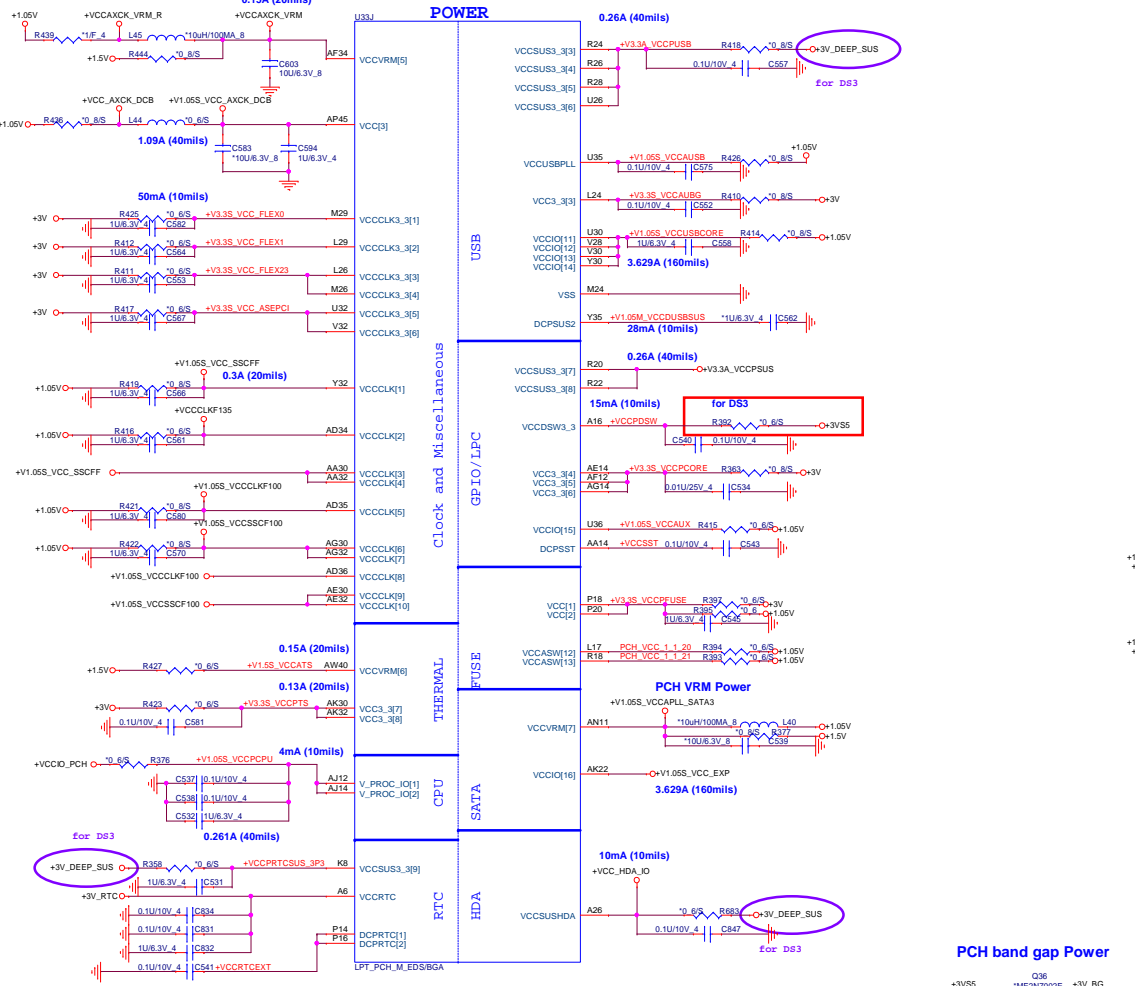
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NBS

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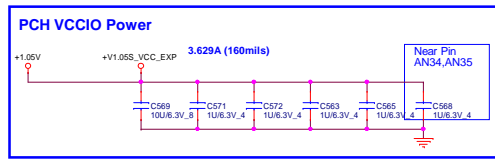
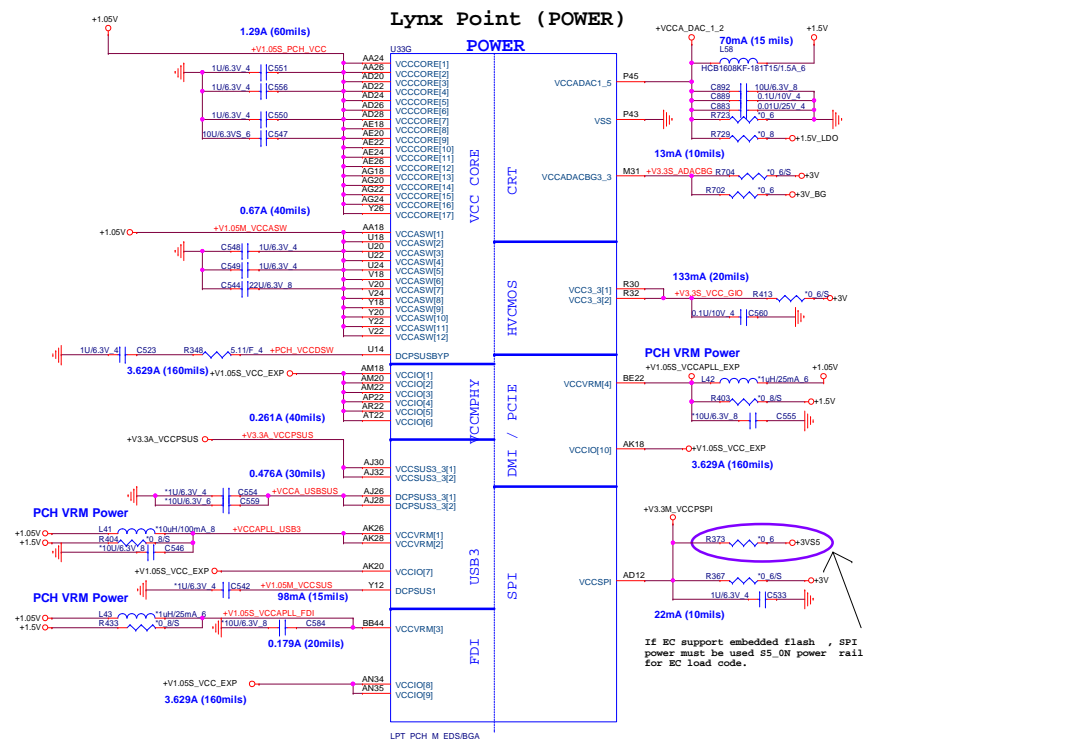
Lynx Point (POWER)



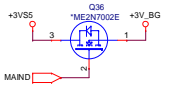
+3V 2.6,7,8,9,11,12,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
 +3V_DEEP_SUS 6,7,8,9,39
 +3VSS 23,29,30,34,36,37,38,39,40,41,42,43,44
 +5V 7,23,26,28,29,32,33,34,39

+VCCIO_PCH 4
 +1.05V 2,4,9,11,31,34,37
 +1.5V 6,7,8,29,34,38,44
 +3VSS 2,6,7,8,34,36,38,39,42,44

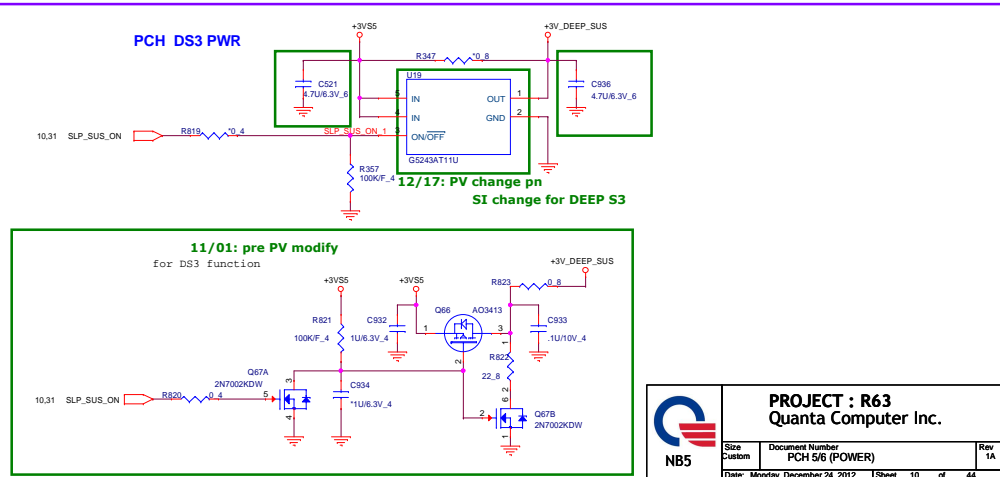
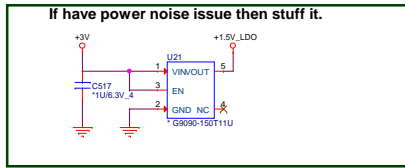
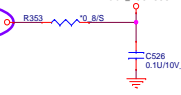
Lynx Point (POWER)



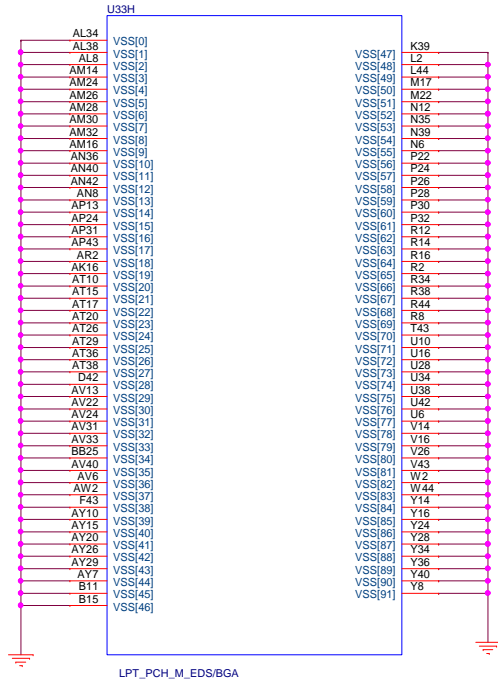
PCH band gap Power



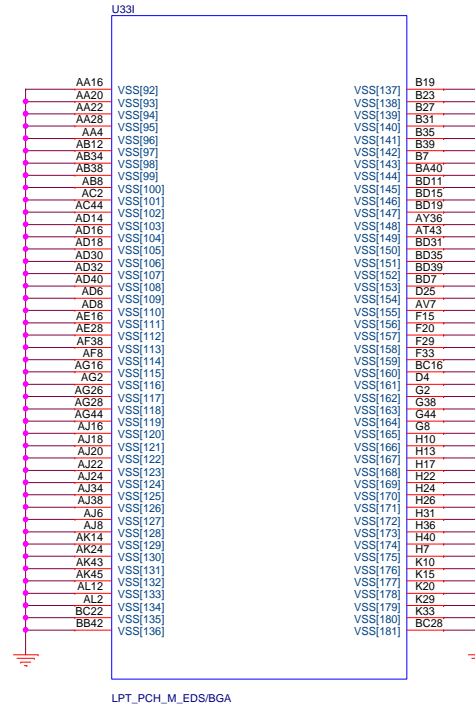
PCH VCCSUS



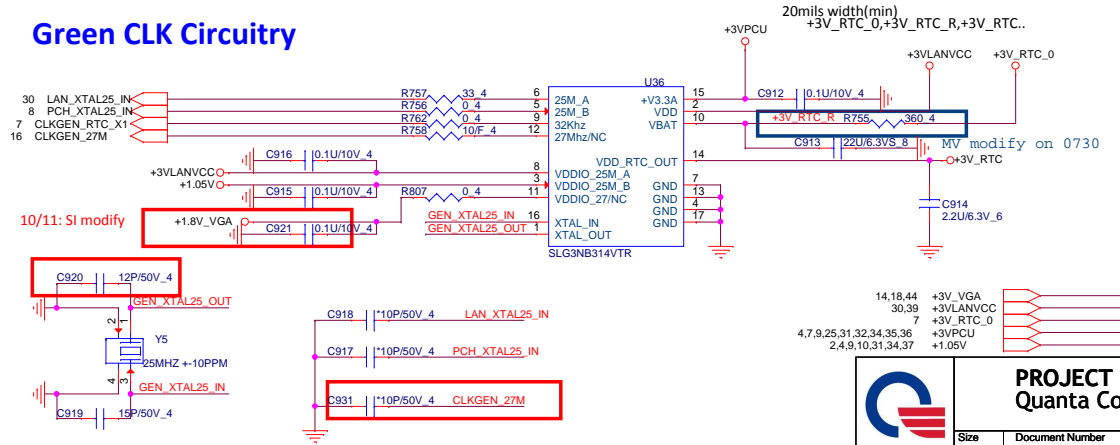
Lynx Point (GND)



Lynx Point (GND)

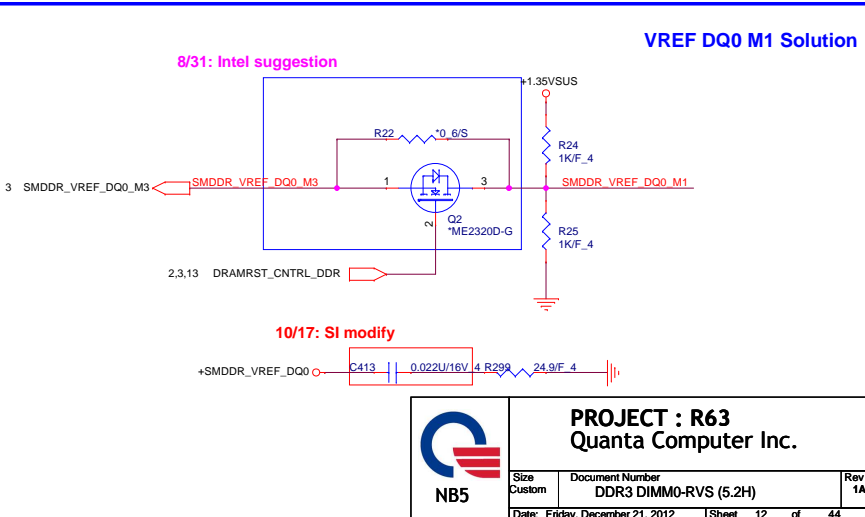
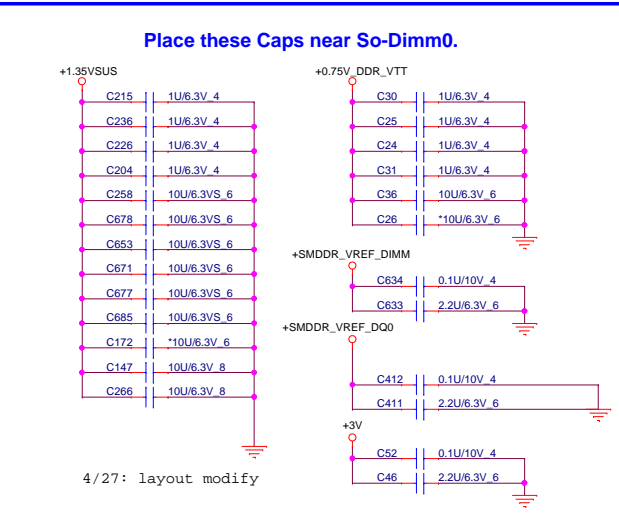
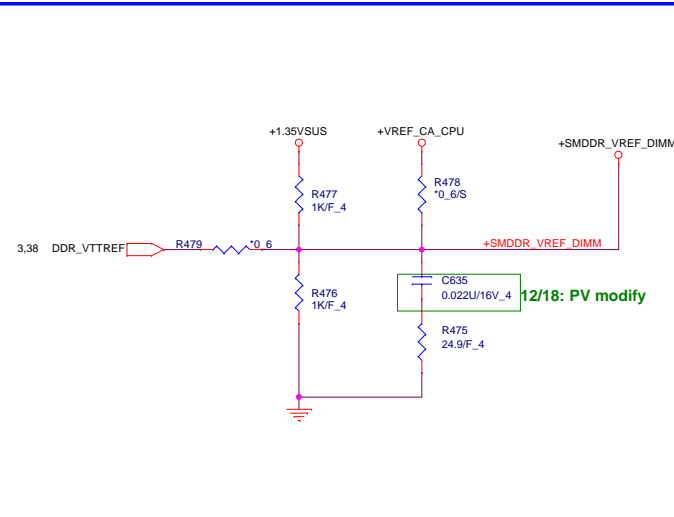
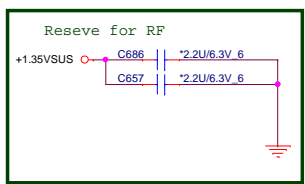
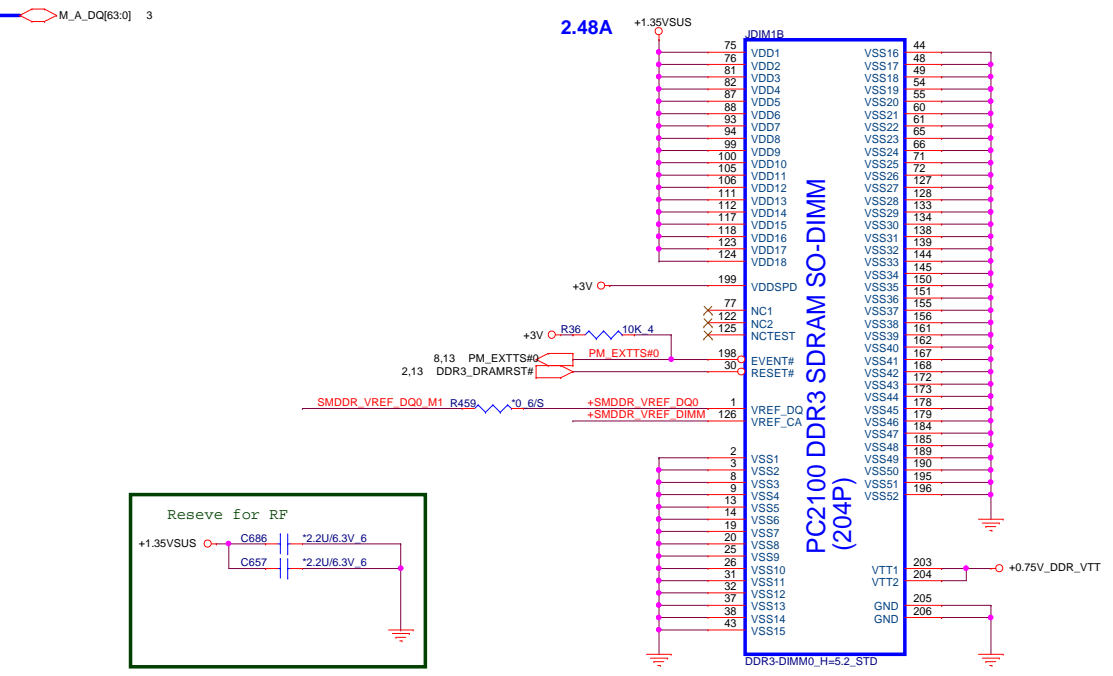
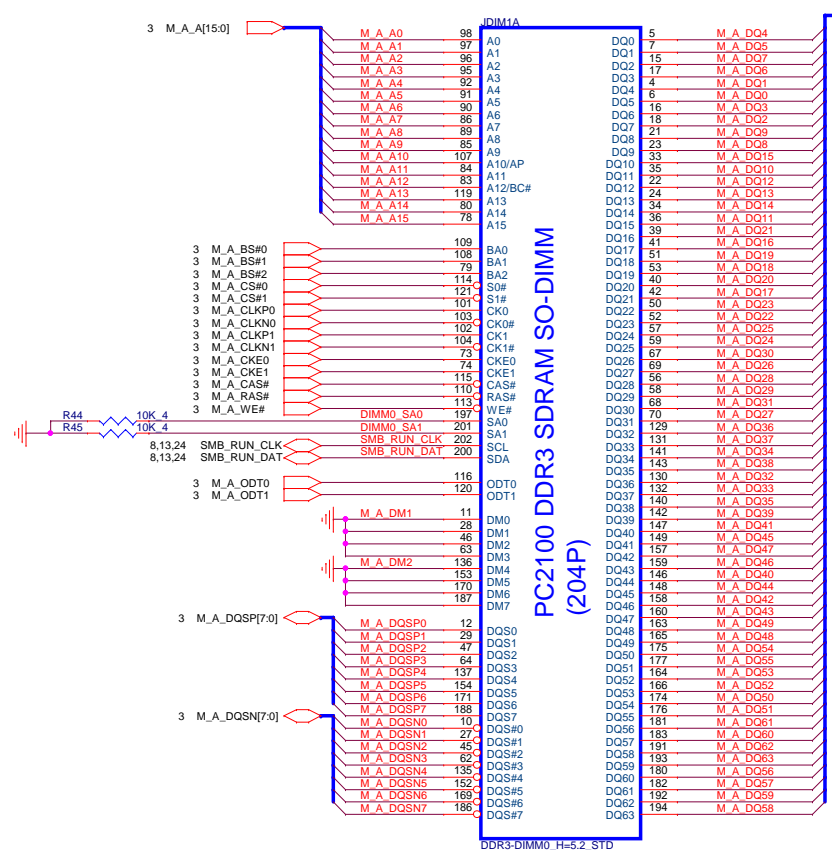


Green CLK Circuitry

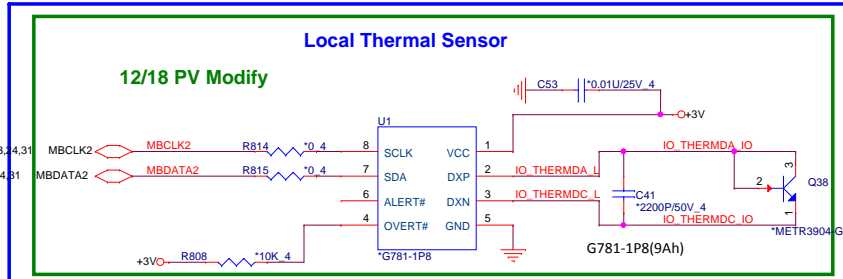
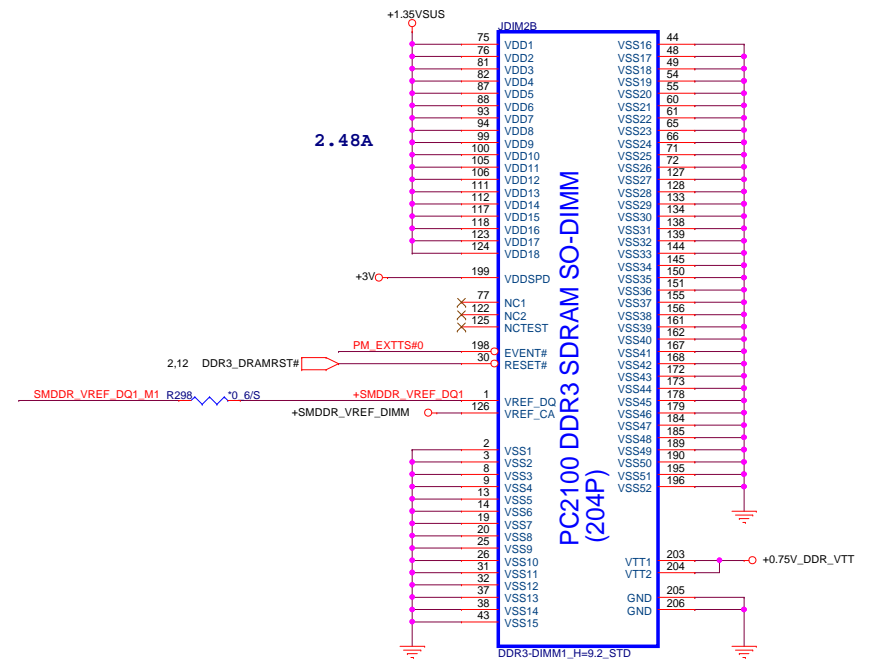
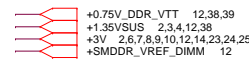
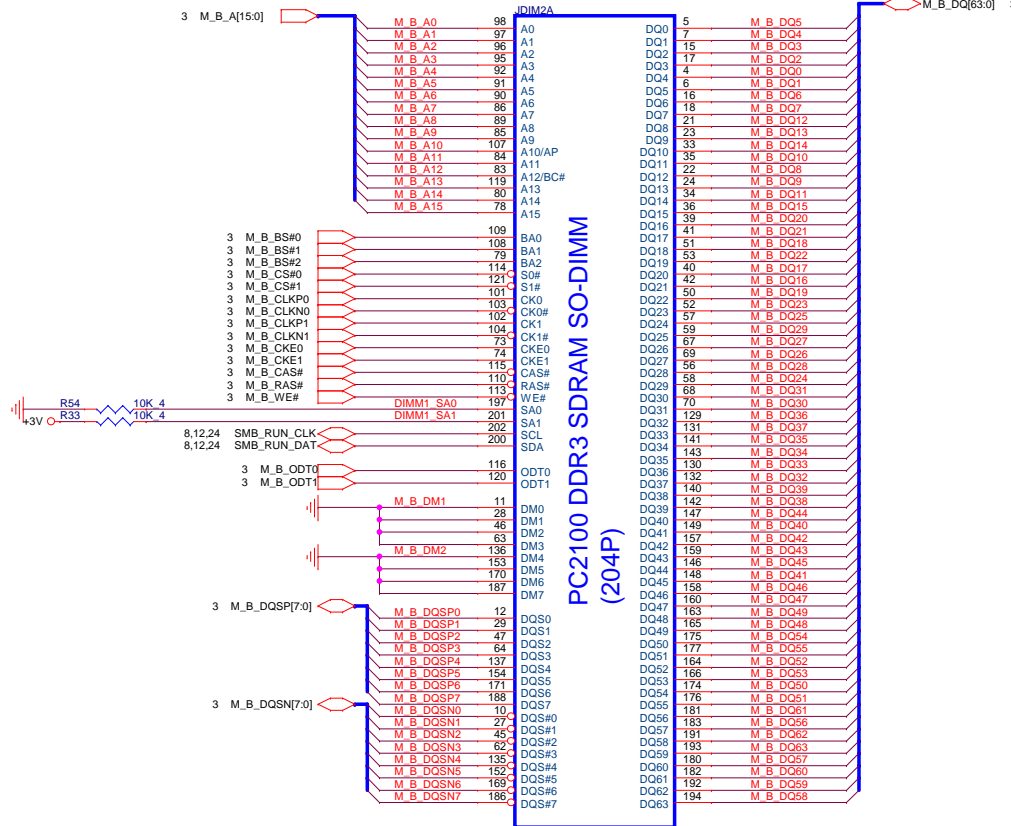


	U36 P/N
UMA	AL3NB244000
DIS	AL000314000

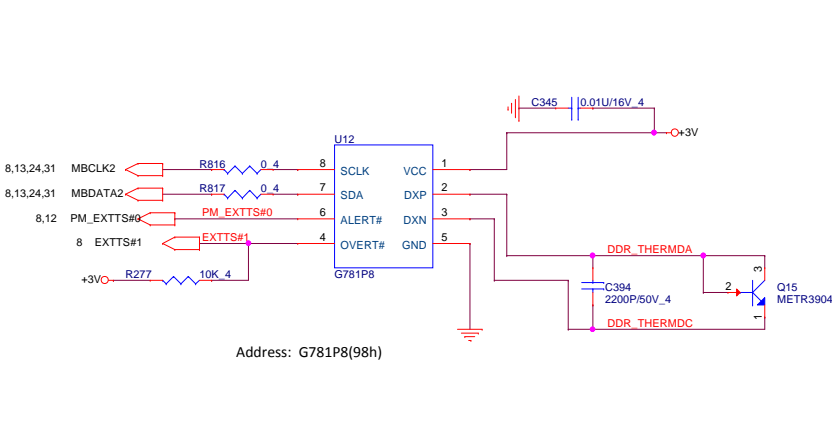
	PROJECT : R63 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number PCH 6/6 (GND)	
		Sheet 11 of 44	



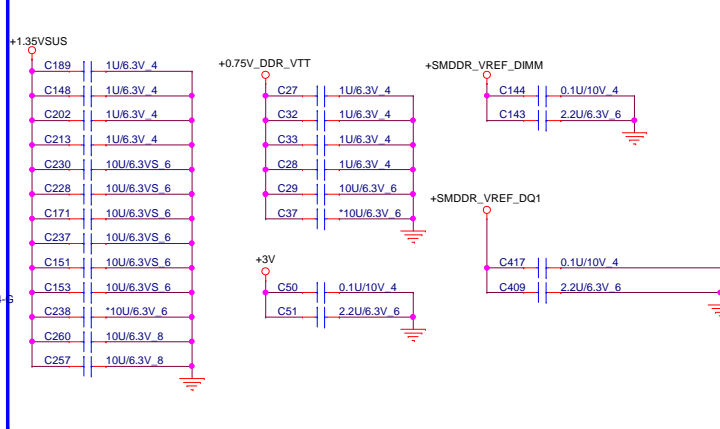
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	Quanta Computer Inc.		
	Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	
Date: Friday, December 21, 2012		Sheet 12 of 44	



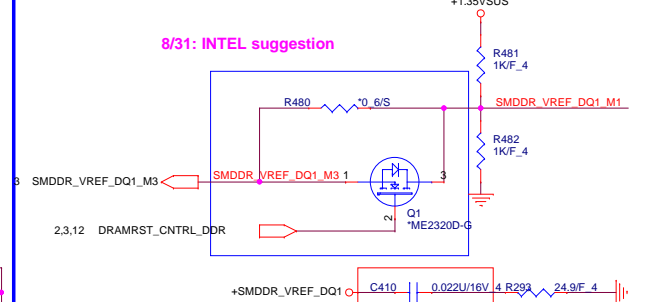
DDR Thermal Sensor



Place these Caps near So-Dimm1.



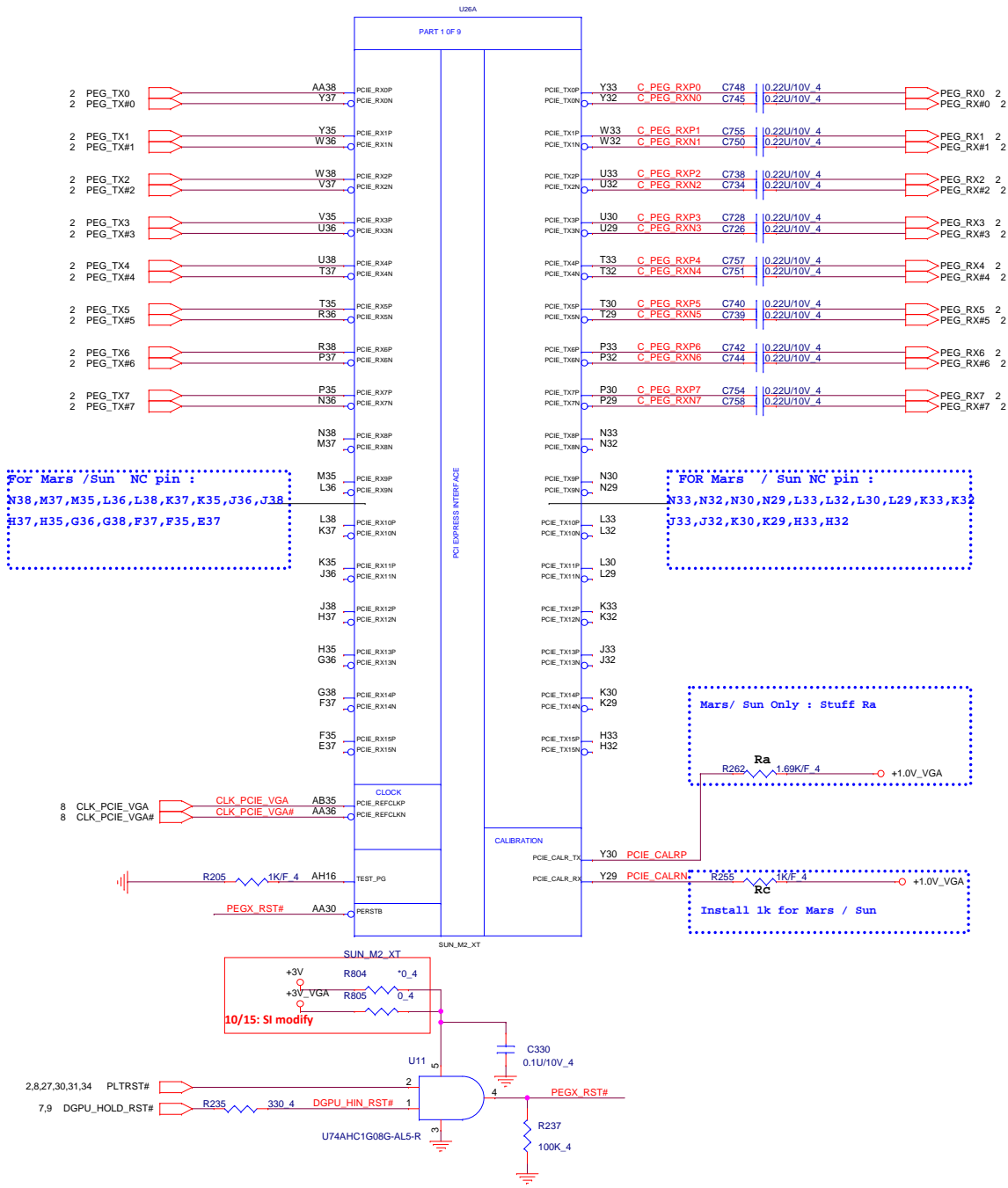
VREF DQ1 M1 Solution



PROJECT : R63
Quanta Computer Inc.

NB5

Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 1A
Date: Friday, December 21, 2012	Sheet 13 of 44	



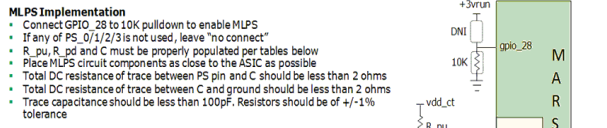
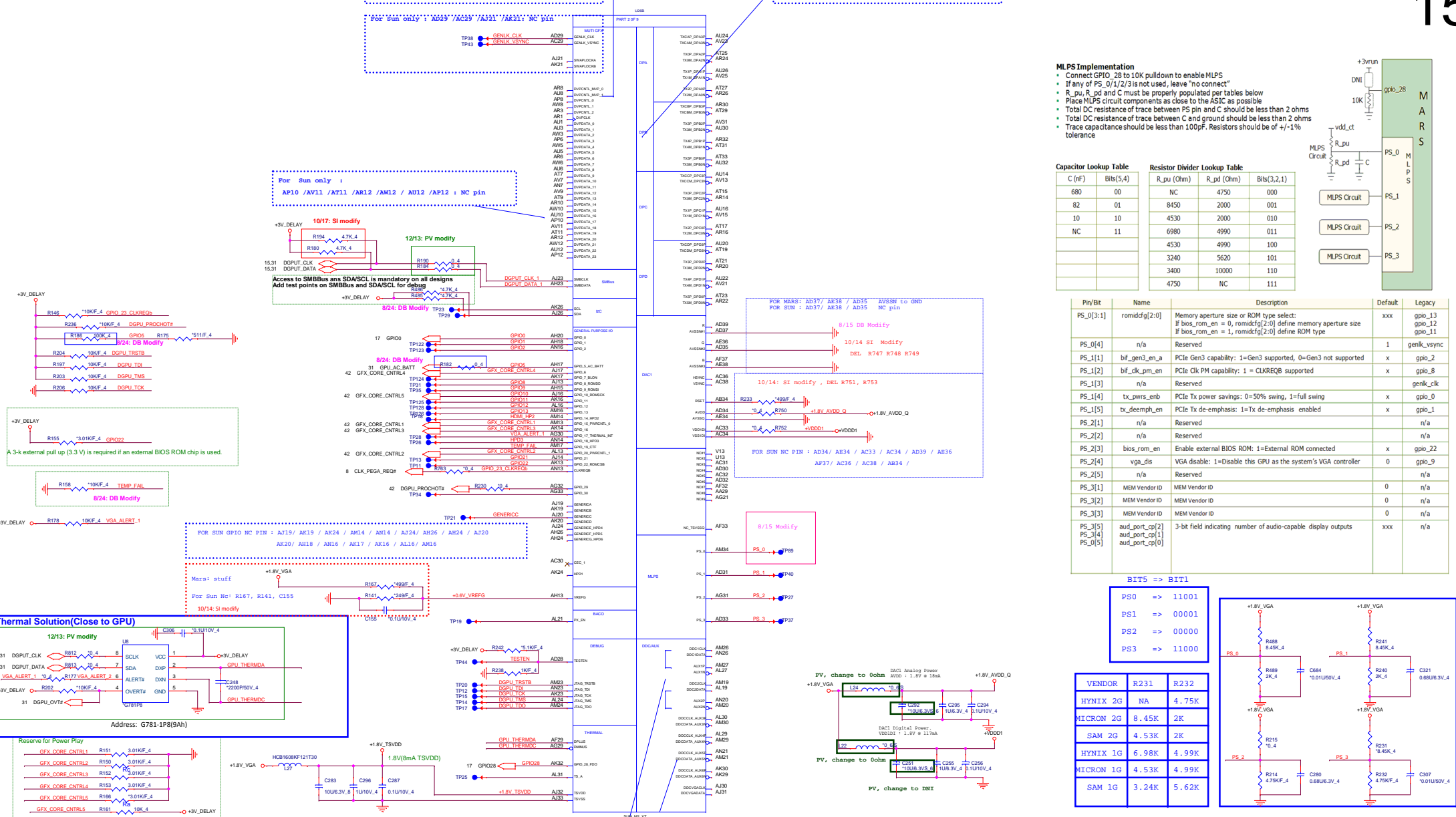
2,6,7,8,9,10,12,13,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
16,18,19,44 +1.0V_VGA

	PROJECT : R63 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number THAMES_PCIE_Interface	

For Mars / Sun : AR1/AR6/AR3/AR8/AU8 : NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only : AP10 /AV11 /AT11 /AR12 /AM12 / AU12 /AP12 : NC pin



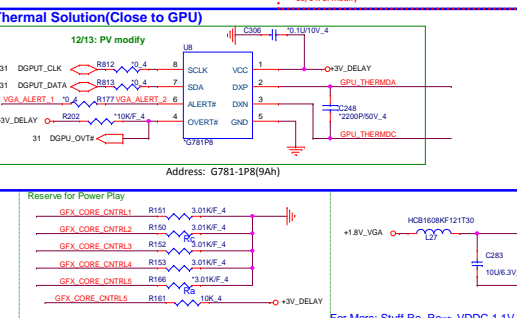
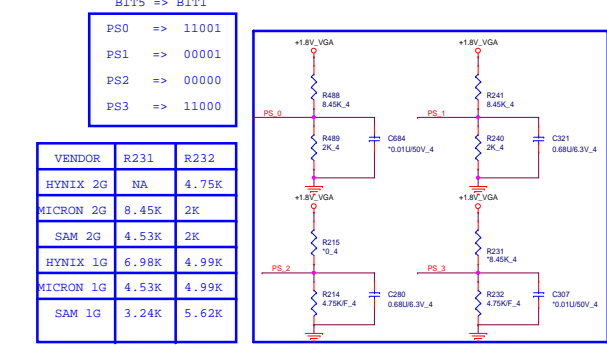
Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

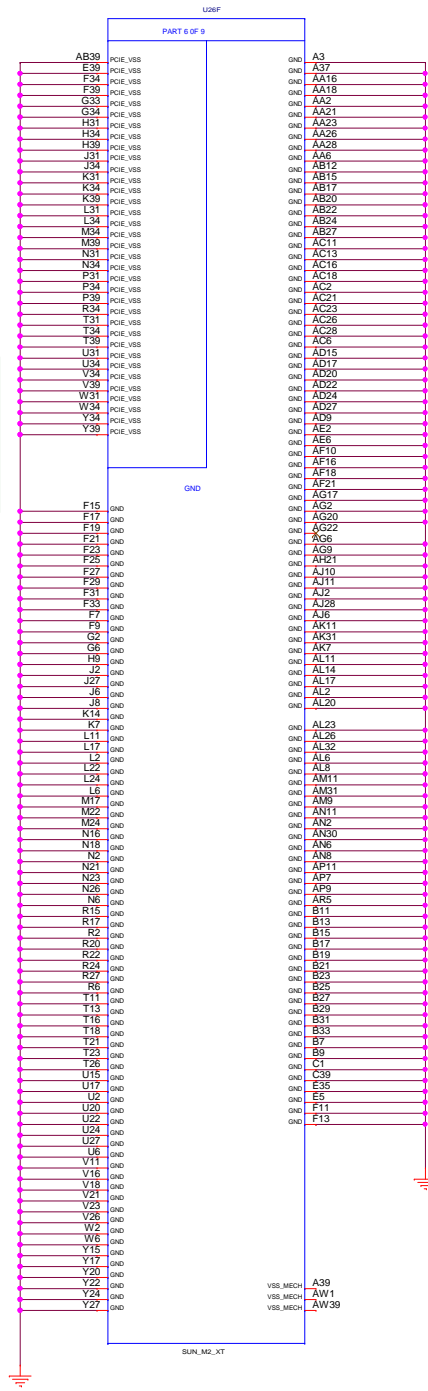
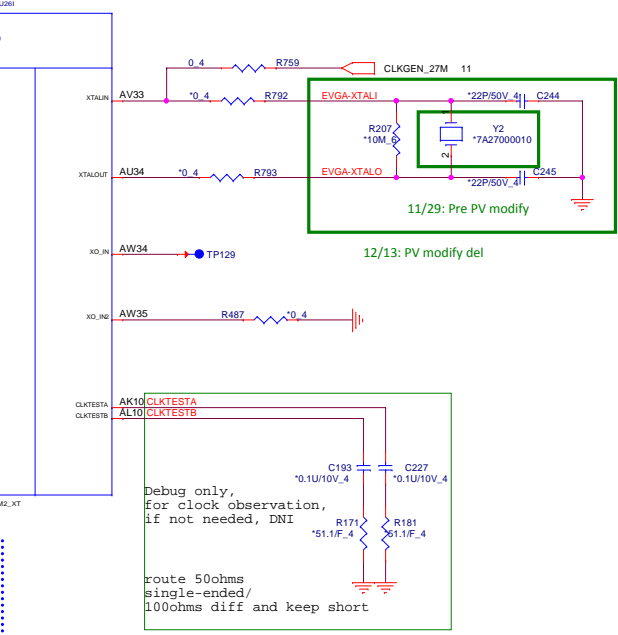
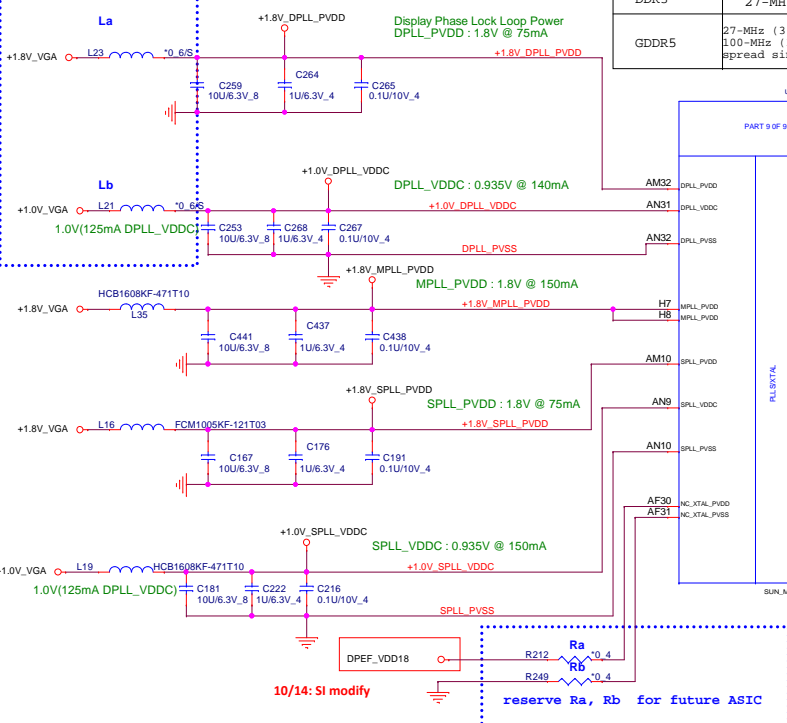
R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcf[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcf[2:0] define memory aperture size If bios_rom_en = 1, romidcf[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[2]	bf_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[3]	bf_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ supported	x	gpio_8
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved	n/a	n/a
PS_2[2]	n/a	Reserved	n/a	n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved	n/a	n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[0]	aud_port_cp[0]			

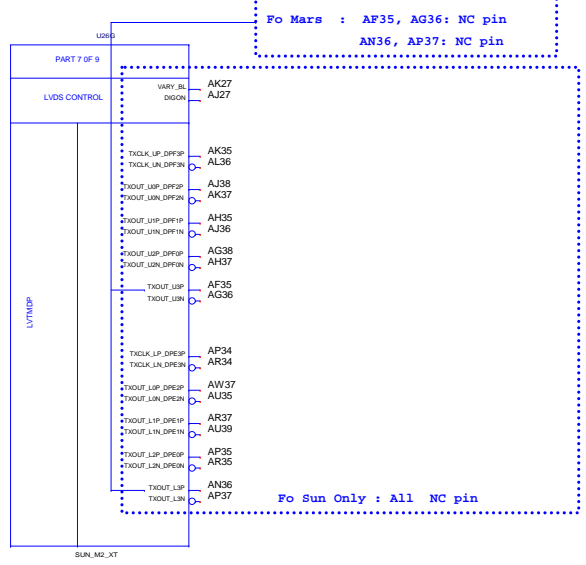


For Mars/ Sun
Change La, Lb
Bead to 0 ohm

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

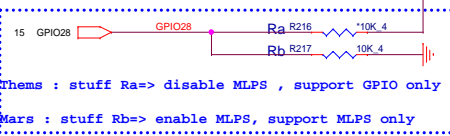


AG22 is nc pin



CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 80% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (STD) 101 - 1Mbit M25P10A (STD) 102 - 1Mbit M25P10A (STD) 103 - 2Mbit M25P30 (STD) 104 - 2Mbit M25P30 (STD) 105 - 2Mbit M25P30 (STD) 106 - 4Mbit M25P40 (Chingis) 107 - 4Mbit M25P40 (Chingis) 108 - 8Mbit M25P80 (Chingis) 109 - 8Mbit M25P80 (Chingis) 110 - 16Mbit M25P160 (Chingis) 111 - 16Mbit M25P160 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dangle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO6 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[3] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

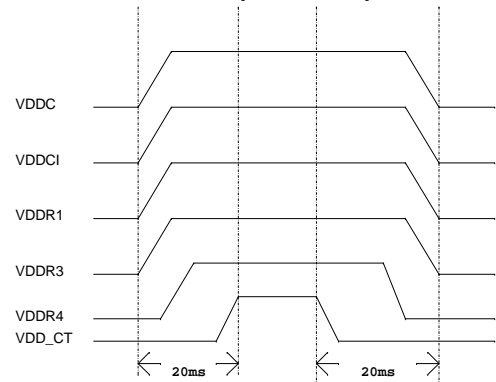


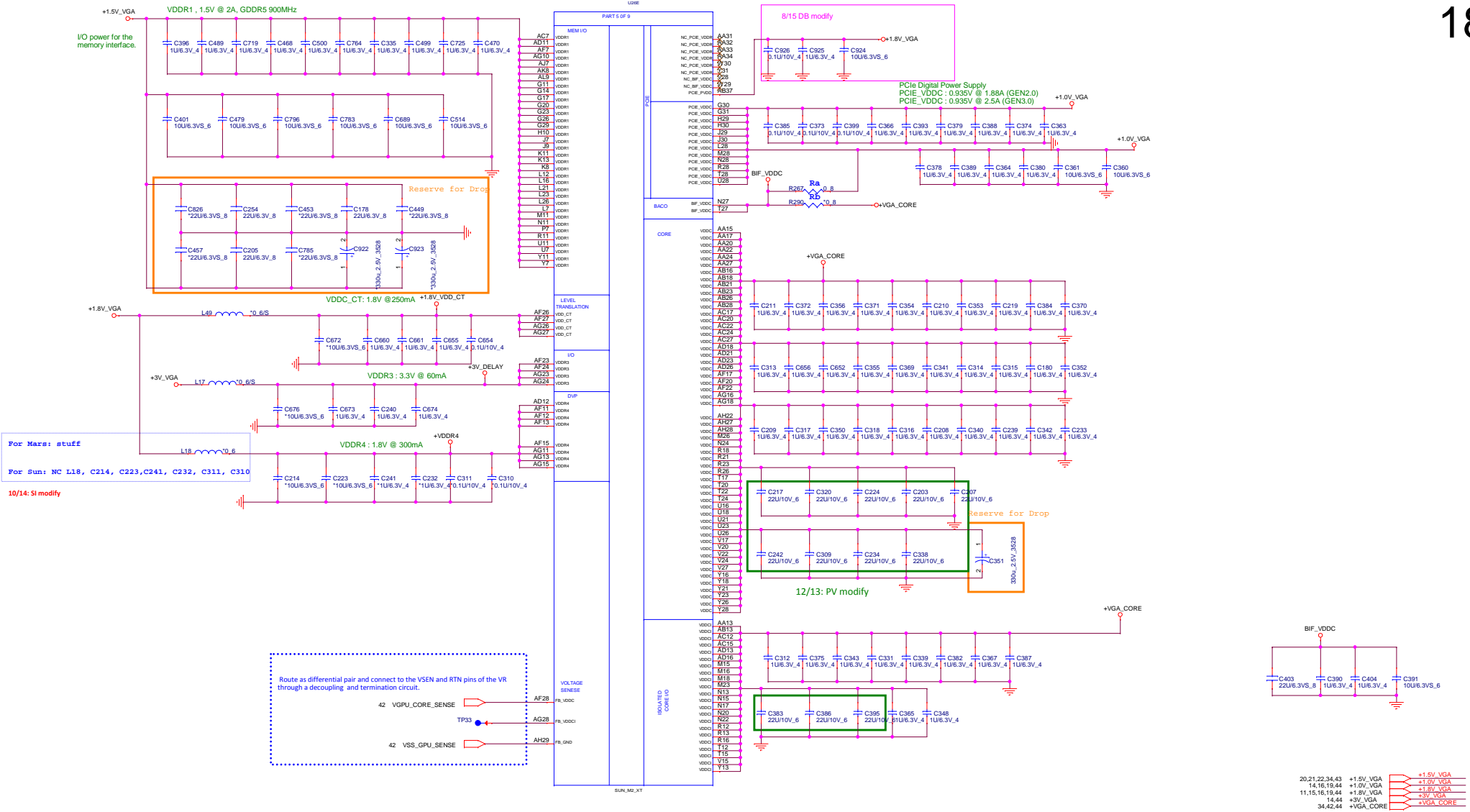
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+1.5V_VGA
0	512M	1	0	0	+3.3V_Delay
0	1G	1	0	1	+3.3V_Delay
0	2G	1	1	0	+1.8V_VGA
0	4G	1	1	1	+1.8V_VGA

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence

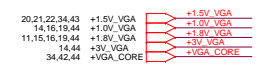


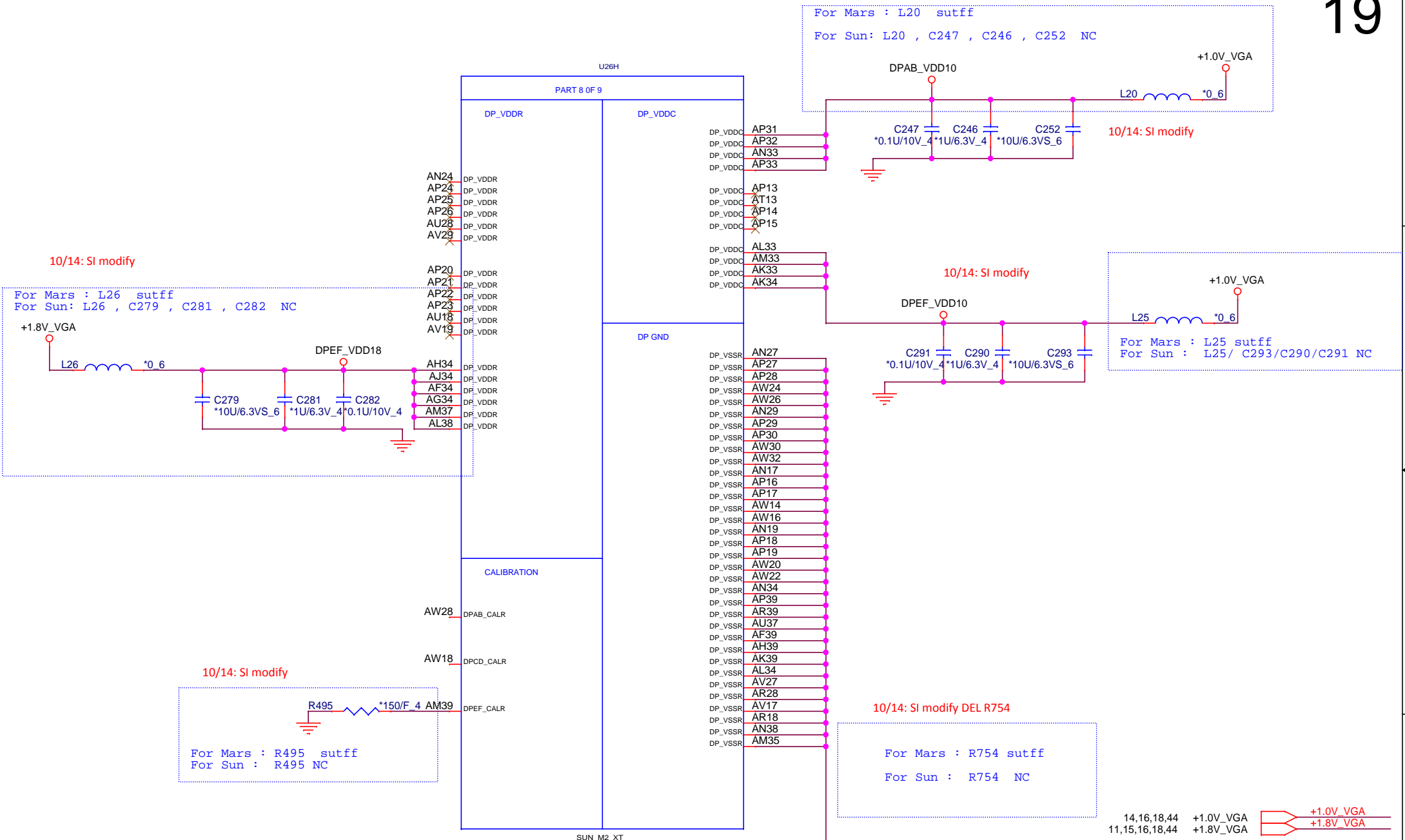


Support BACO Mode

- Notel. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

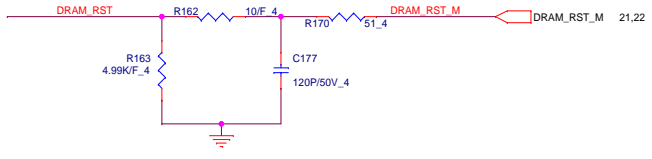
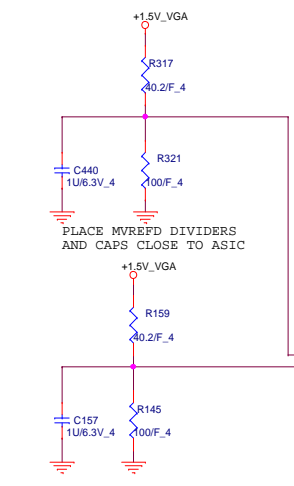
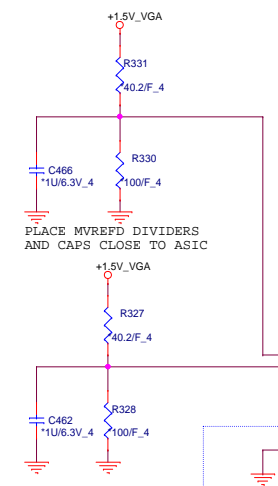
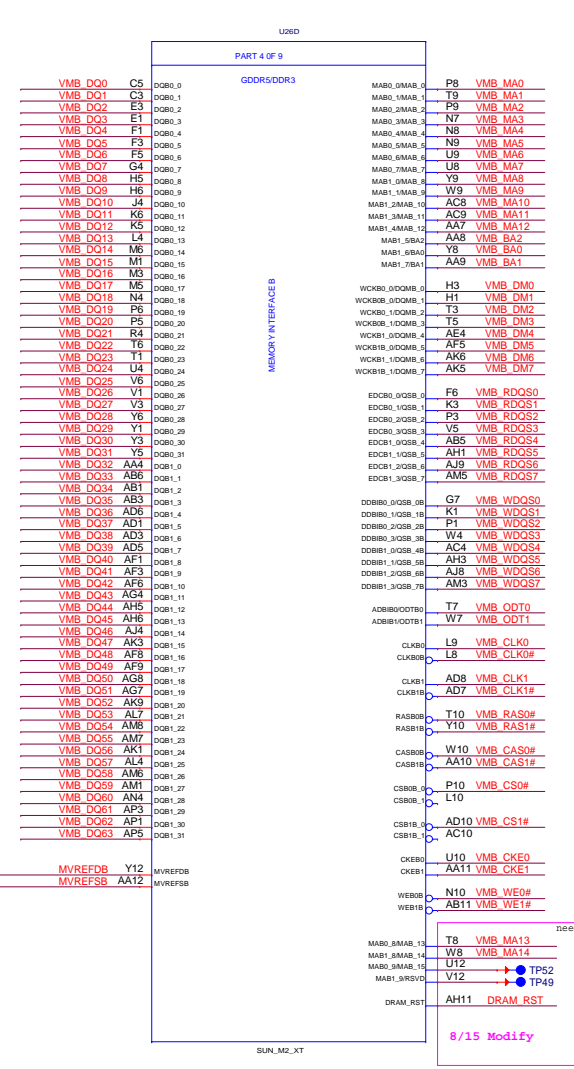
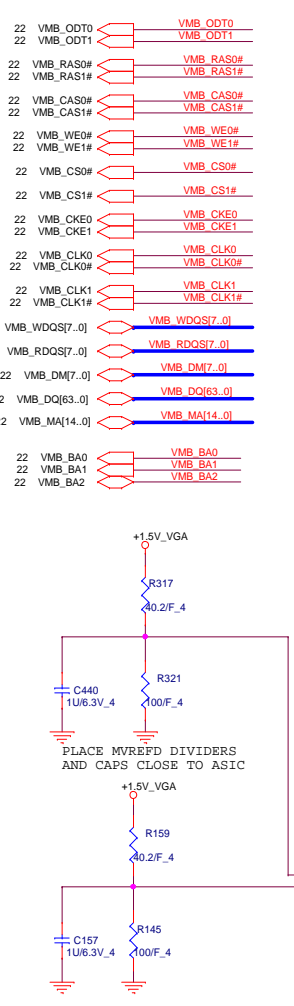
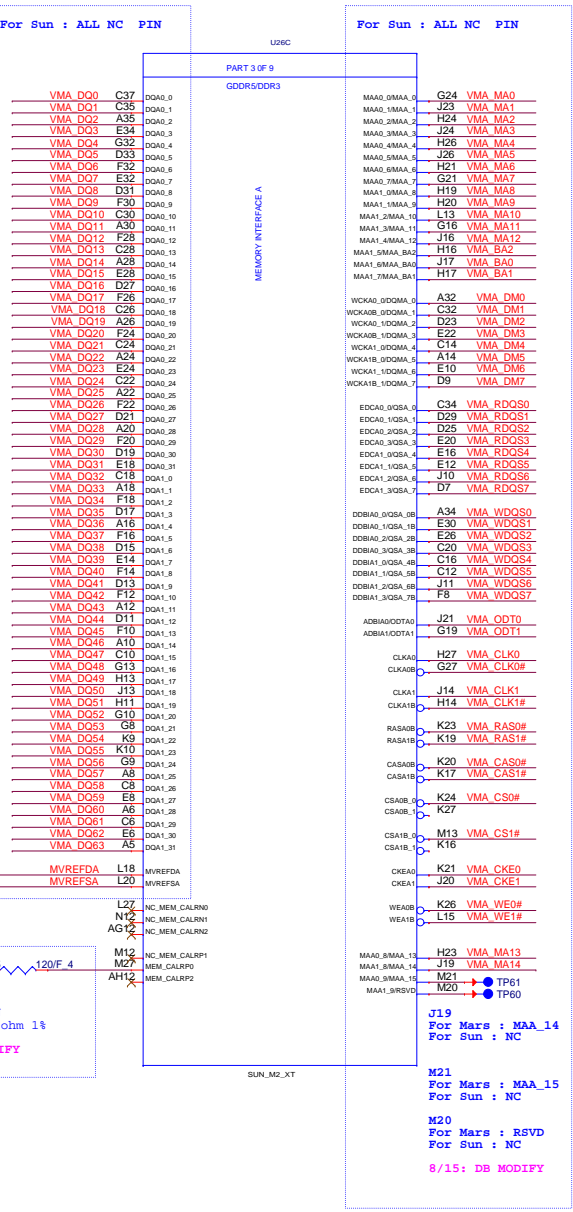
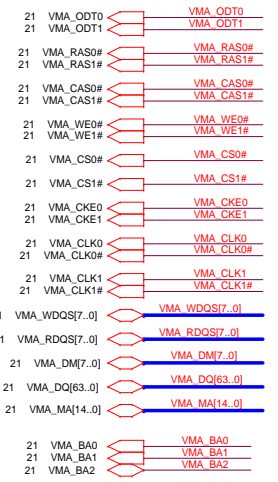
PX_EN = 0, for Normal Operation
 PX_EN = 1, for BACO MODE



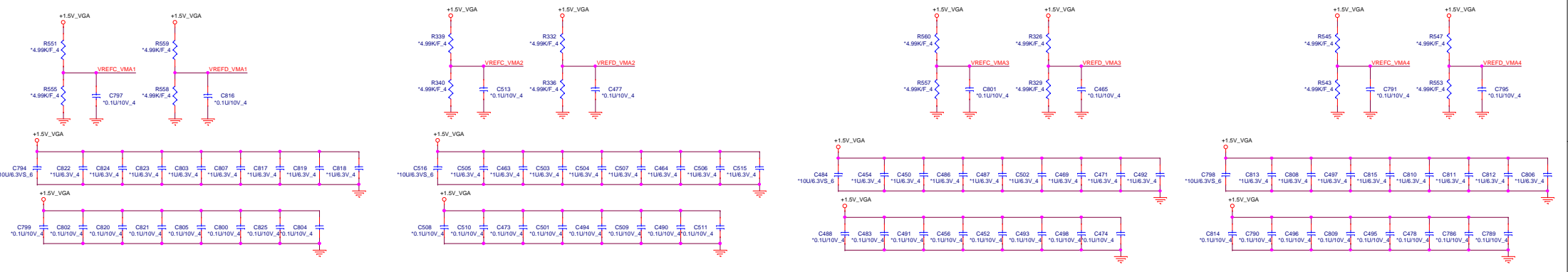
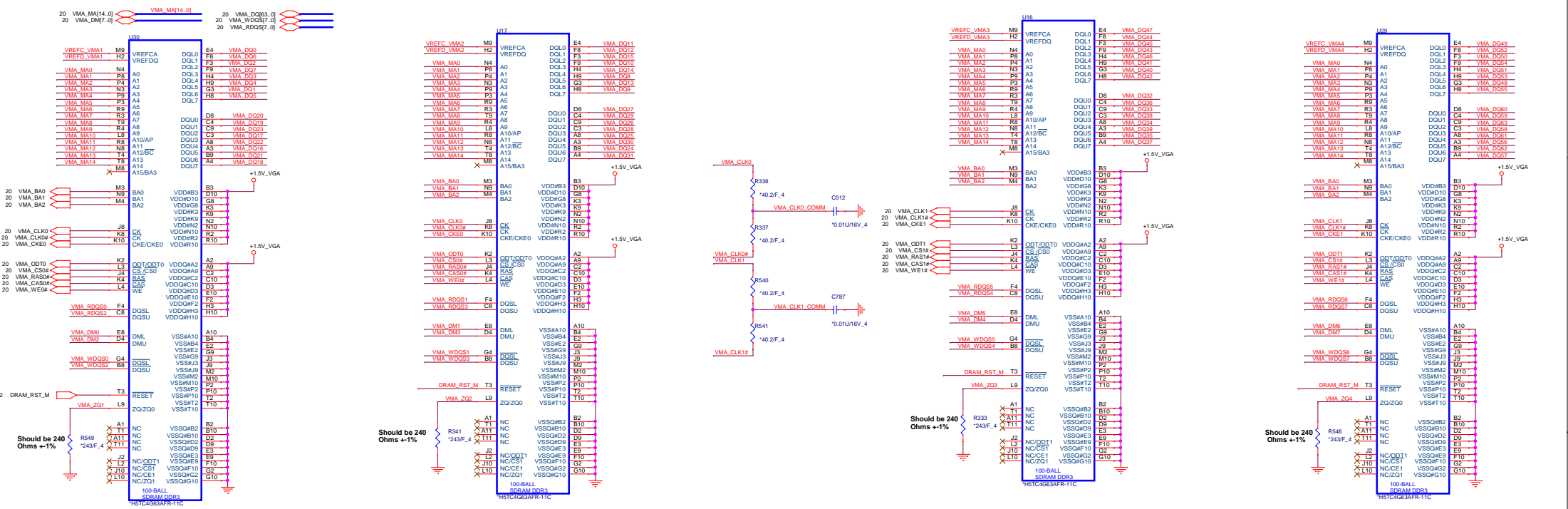


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Quanta Computer Inc.

Size Custom	Document Number THAMES_DP Powers	Rev 1A
Date: Friday, December 21, 2012	Sheet 19 of 44	



CHANNEL A: 256MB/512MB DDR3

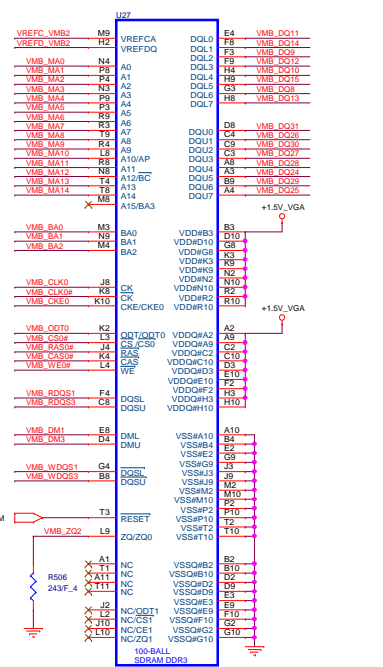


PROJECT : R63
Quanta Computer Inc.

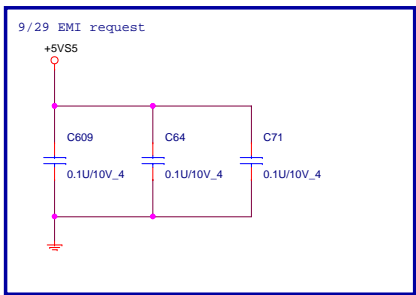
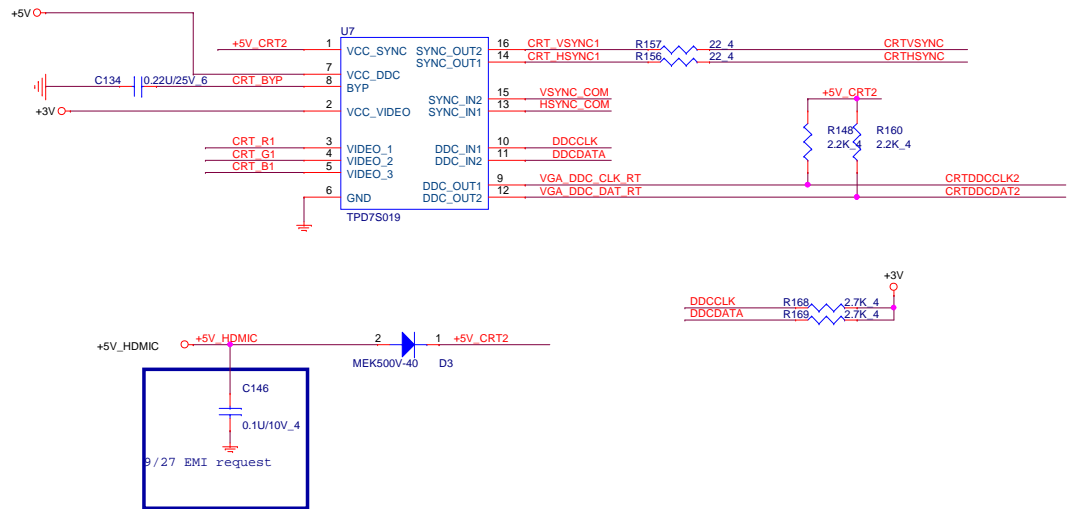
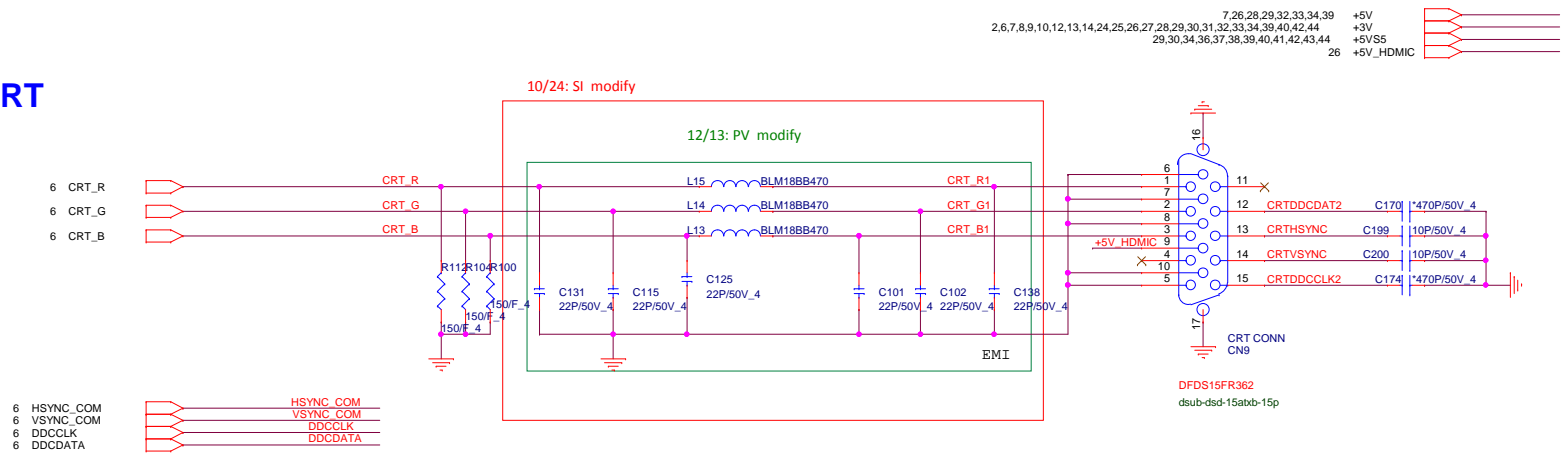
Size Custom Document Number VRAM-A (DDR3 BGA96) Rev 3A
Date: Friday, December 21, 2012 Sheet 21 of 44

18.20.22.34.43 +1.5V_VGA

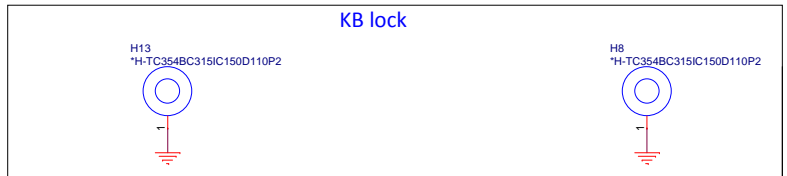
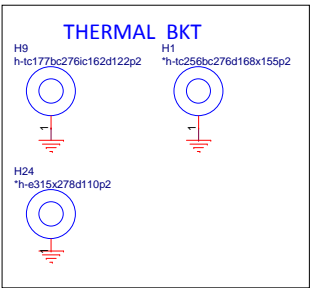
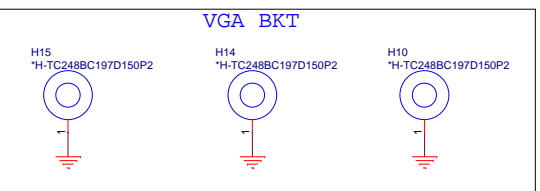
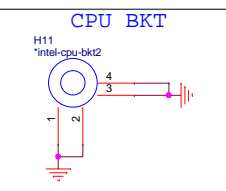
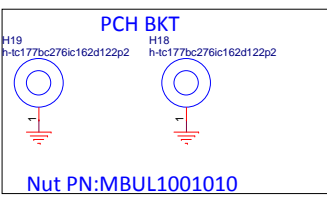
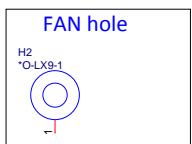
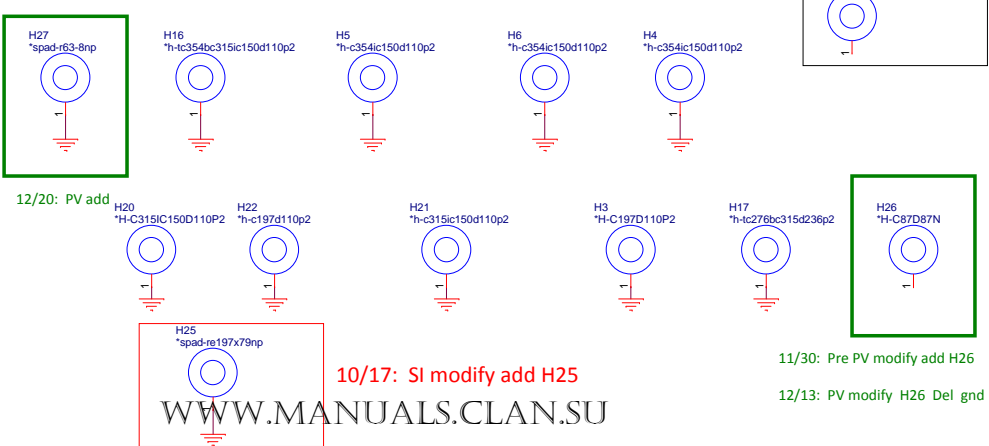
CHANNEL B: 256MB/512MB DDR3



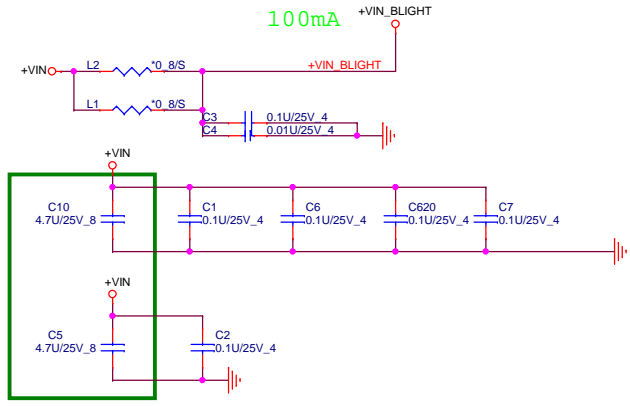
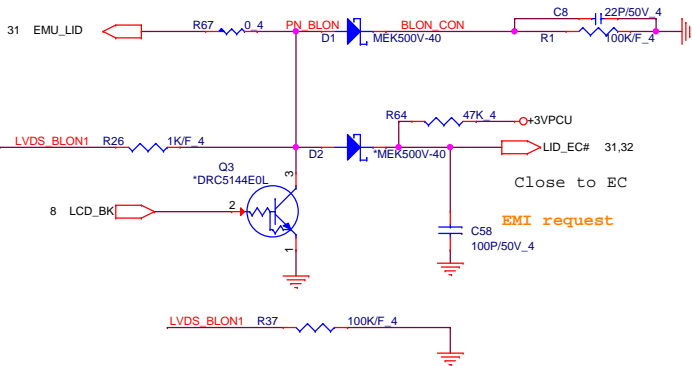
CRT PORT



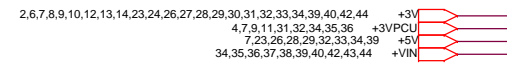
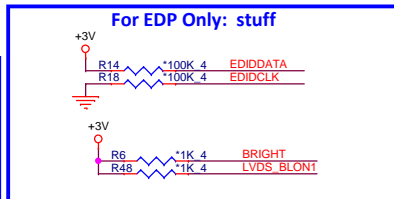
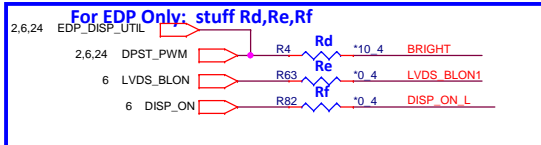
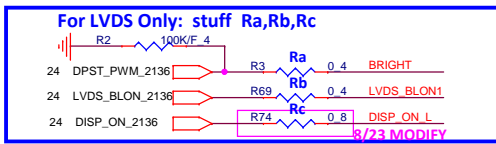
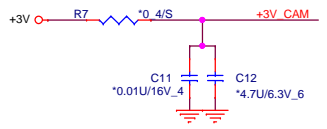
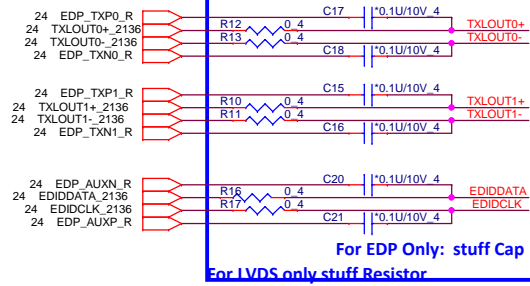
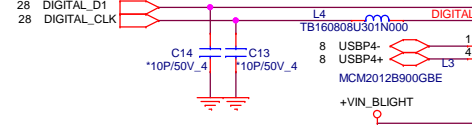
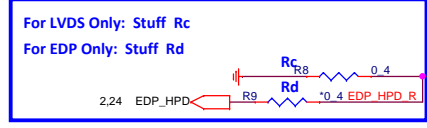
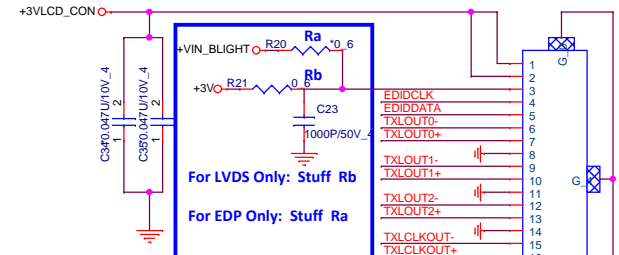
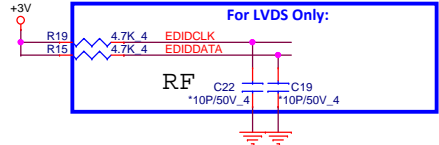
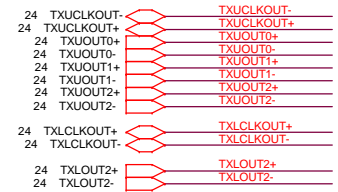
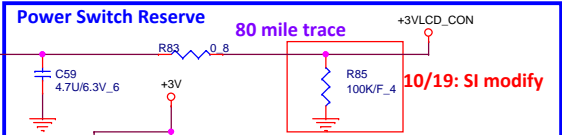
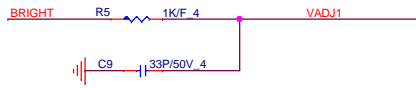
HOLE



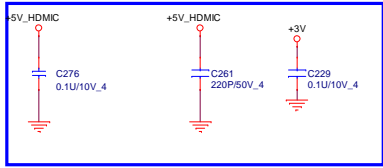
LID Switch



12/17: PV modify pn for 0.85 height



EMI request

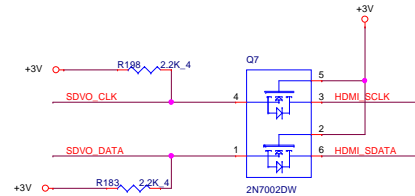


close to HDMI conn

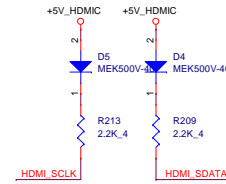
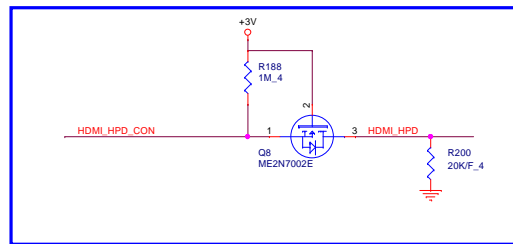
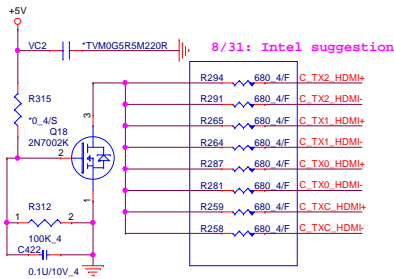
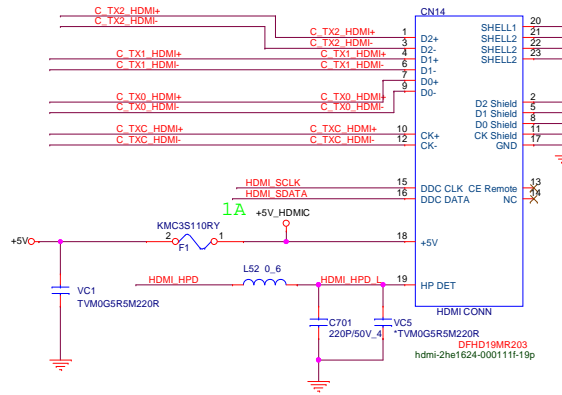
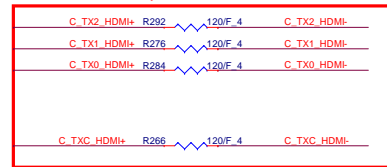
2	IN_CLK#	IN_CLK#	C346	0.1U/10V_4	C TXC_HDMI-
2	IN_CLK	IN_CLK	C347	0.1U/10V_4	C TXC_HDMI+
2	IN_D0#	IN_D0#	C397	0.1U/10V_4	C TX0_HDMI-
2	IN_D0	IN_D0	C402	0.1U/10V_4	C TX0_HDMI+
2	IN_D1#	IN_D1#	C357	0.1U/10V_4	C TX1_HDMI-
2	IN_D1	IN_D1	C358	0.1U/10V_4	C TX1_HDMI+
2	IN_D2#	IN_D2#	C405	0.1U/10V_4	C TX2_HDMI-
2	IN_D2	IN_D2	C408	0.1U/10V_4	C TX2_HDMI+

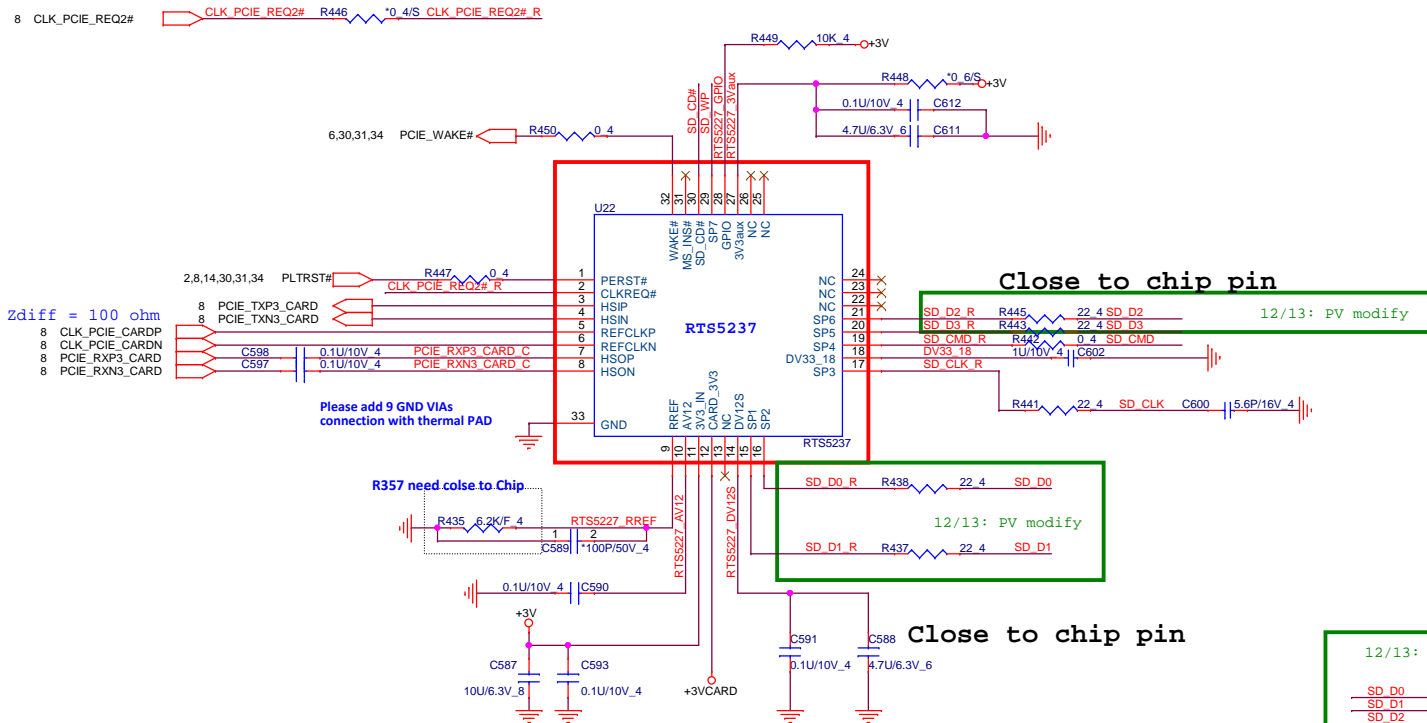


Close to HDMI Connector



10/14: SI for EMI request





SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin

Zdiff = 100 ohm
 8 CLK_PCIE_CARDP
 8 CLK_PCIE_CARDN
 8 PCIE_RXP3_CARD
 8 PCIE_RXN3_CARD

Close to chip pin
 SD D2 R R445 22 4 SD D2
 SD D3 R R443 22 4 SD D3
 SD CMD R R442 0 4 SD CMD
 DV33 18 1U/10V_4 C602
 SD CLK R R441 22 4 SD CLK C600 5.6P/16V_4

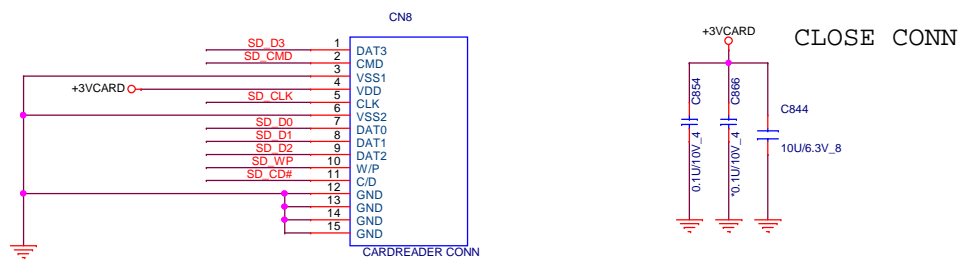
Close to chip pin
 SD D0 R R438 22 4 SD D0
 SD D1 R R437 22 4 SD D1

Close to chip pin

12/13: PV modify
 SD D0 C596 5.6P/16V_4
 SD D1 C586 5.6P/16V_4
 SD D2 C610 5.6P/16V_4
 SD D3 C605 5.6P/16V_4

8/21 DB Modify
 RTS5227_AV12 R784 0 4/S RTS5227_DV12S

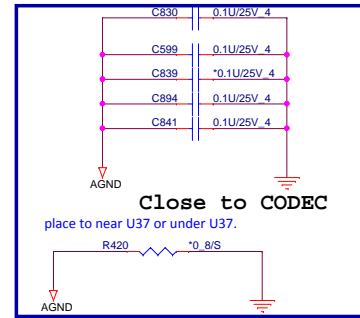
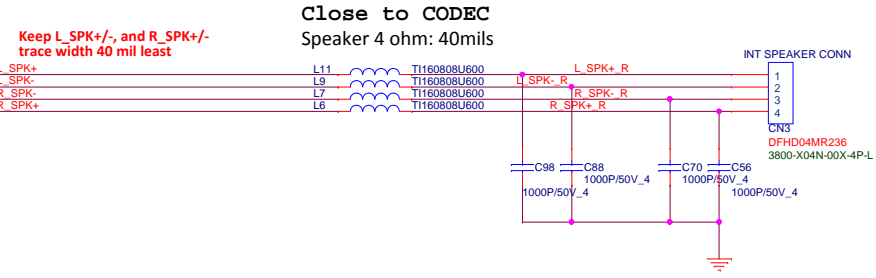
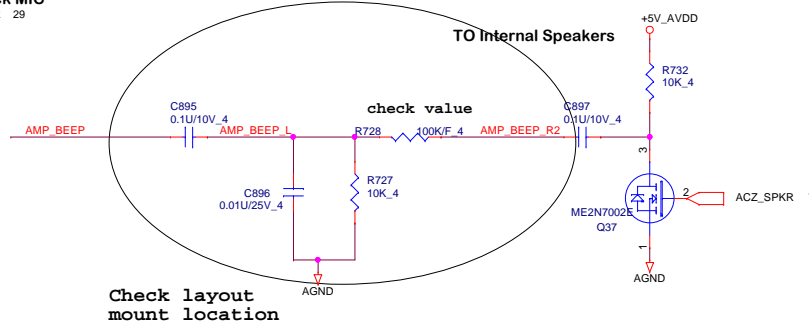
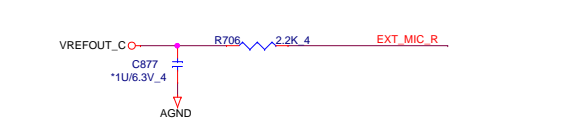
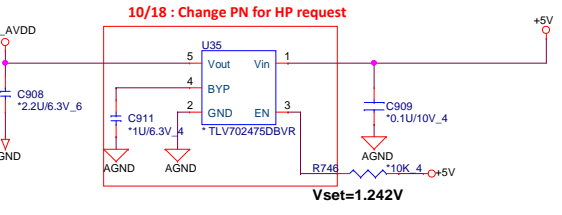
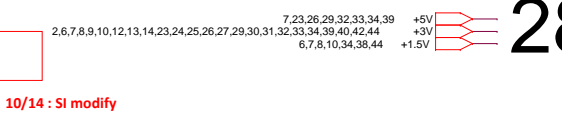
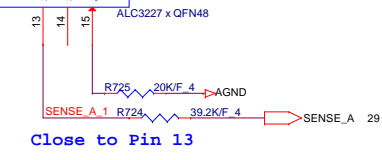
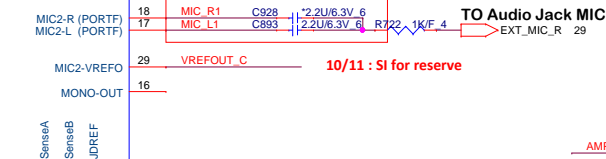
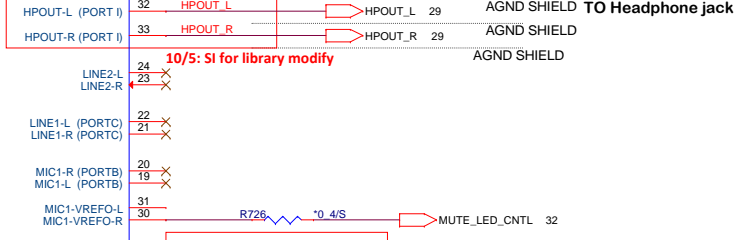
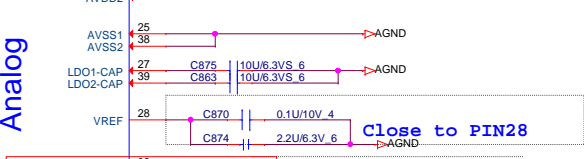
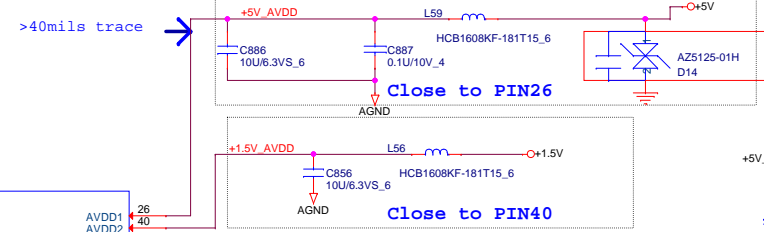
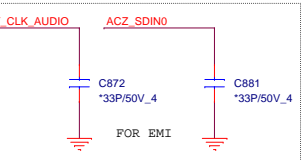
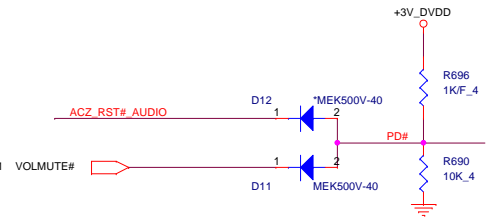
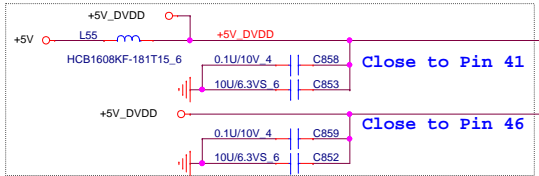
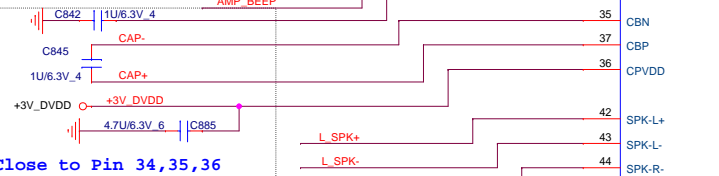
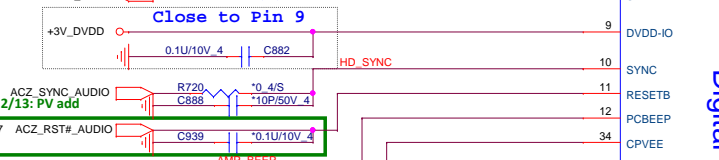
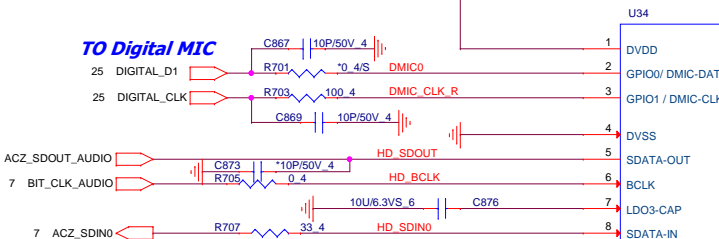
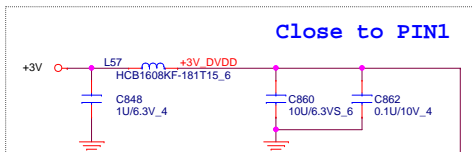
SD / MMC
 CARD READER

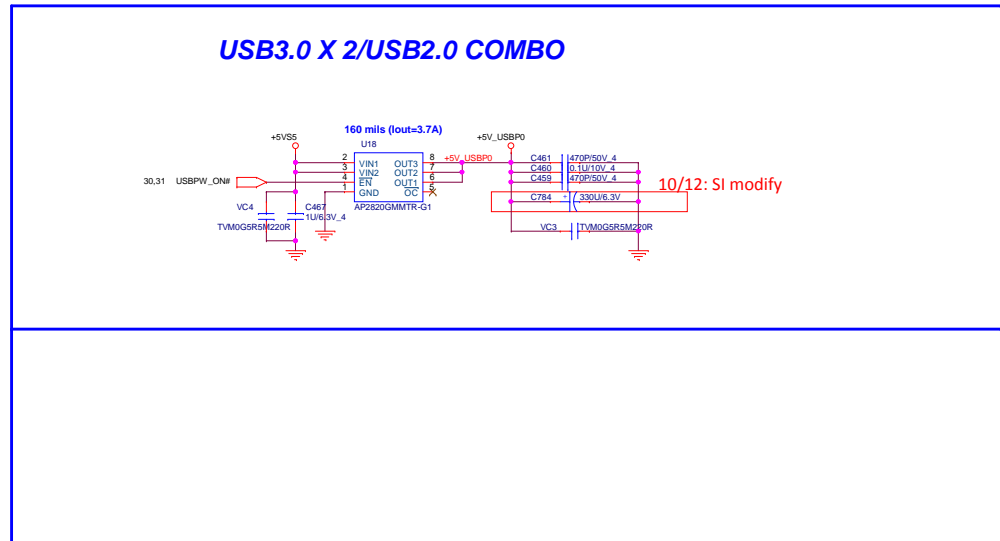
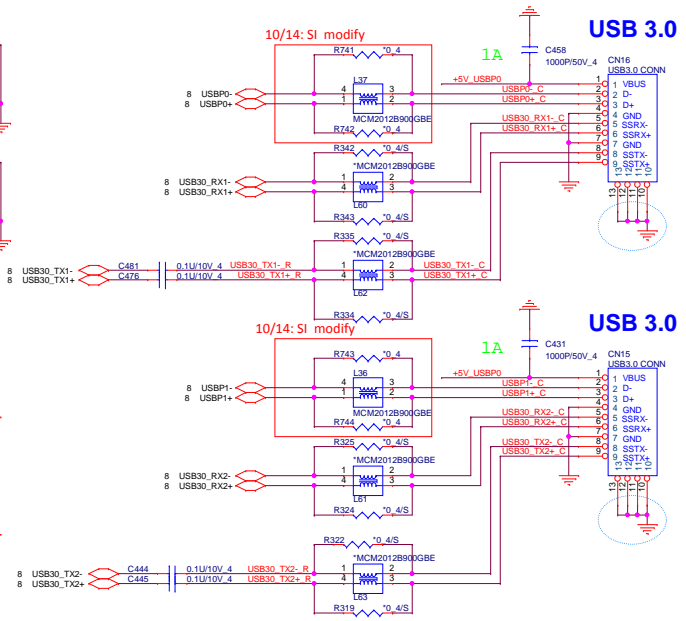
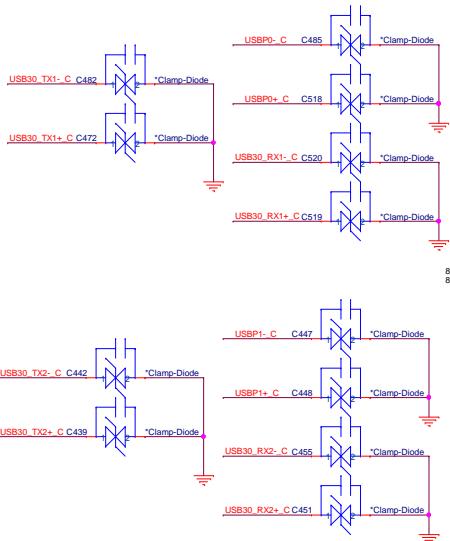


Change footprint to
 sdcard-psdbtc-09glbs1nn4h3-11p

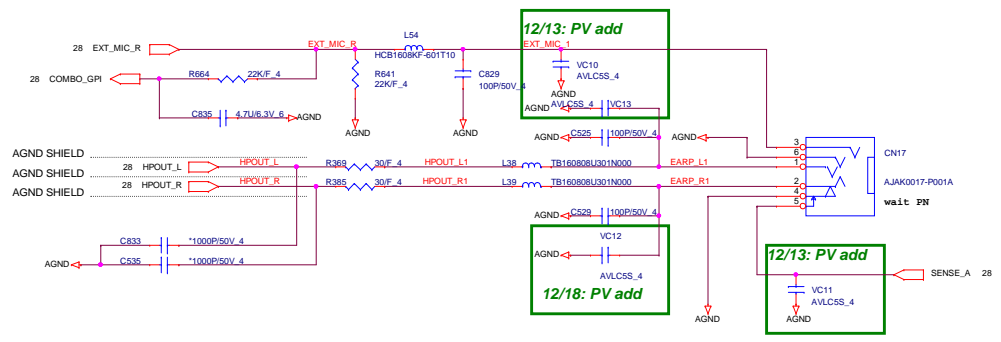
2,6,7,8,9,10,12,13,14,23,24,25,26,28,29,30,31,32,33,34,39,40,42,44 +3VS5
 +3V
 +3VCARD

	PROJECT : R63 Quanta Computer Inc.	
	Size Custom	Document Number RTS5229 & CR SOCKET
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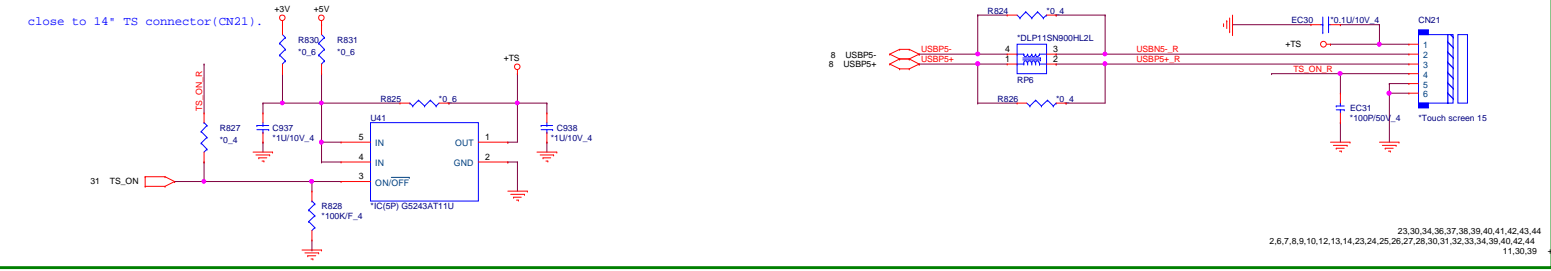


COMBO JACK

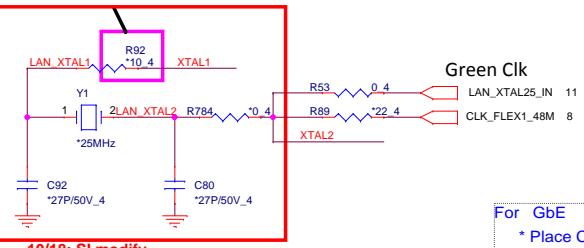


12/11: PV add

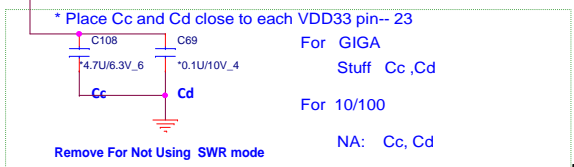
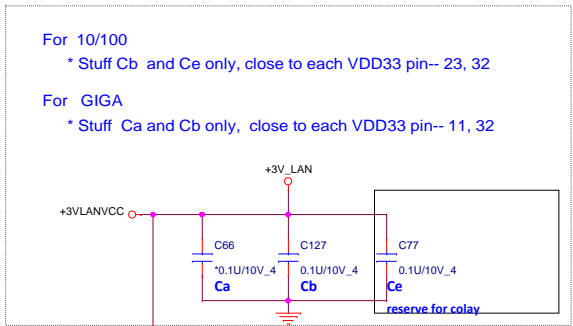
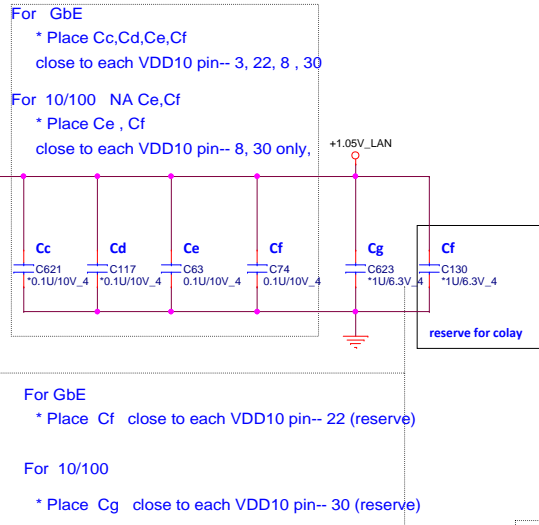
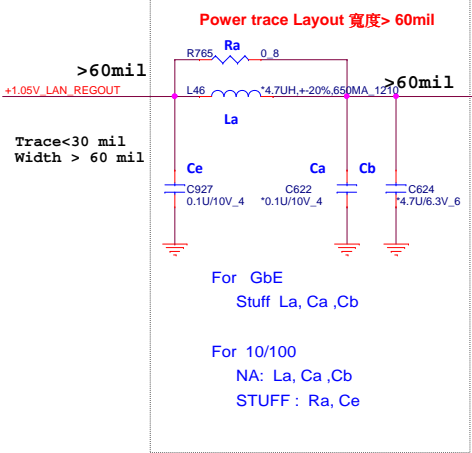
Touch Screen Connector



For EMI 0 ~ 22 ohm

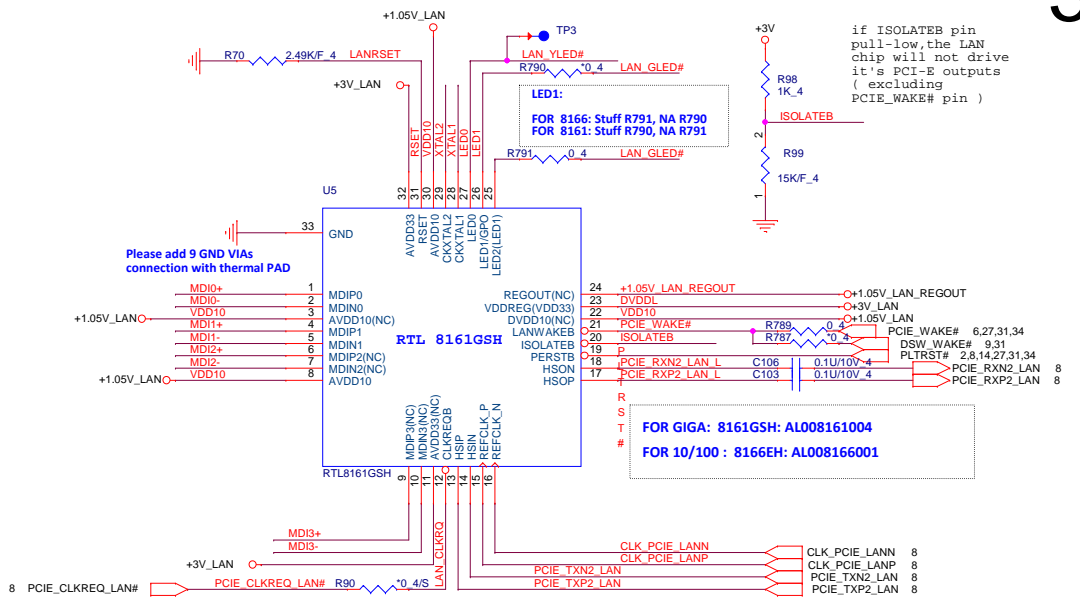
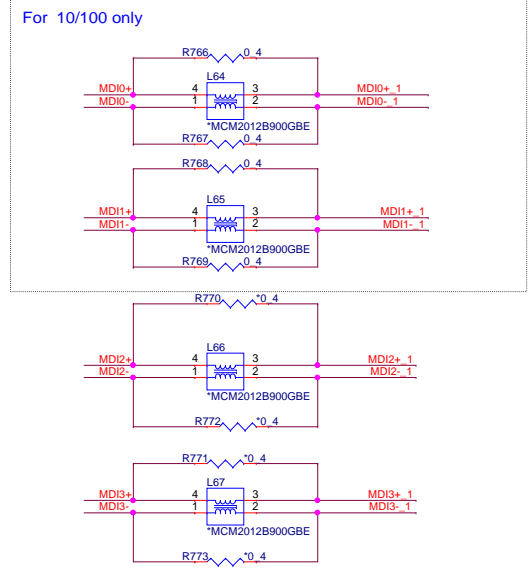


10/18: SI modify

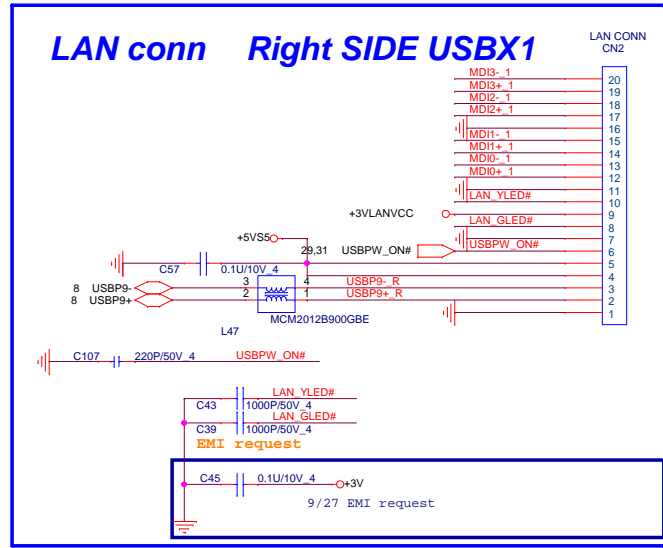


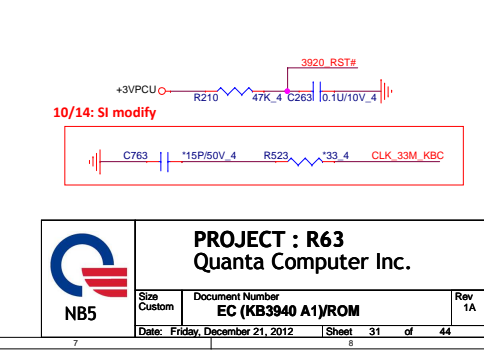
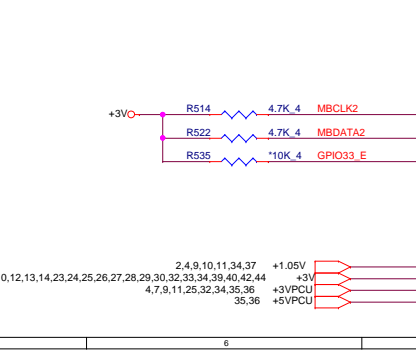
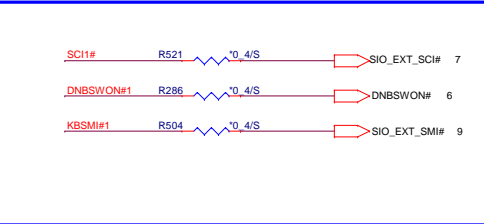
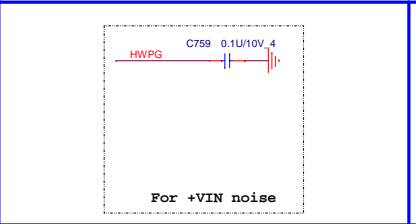
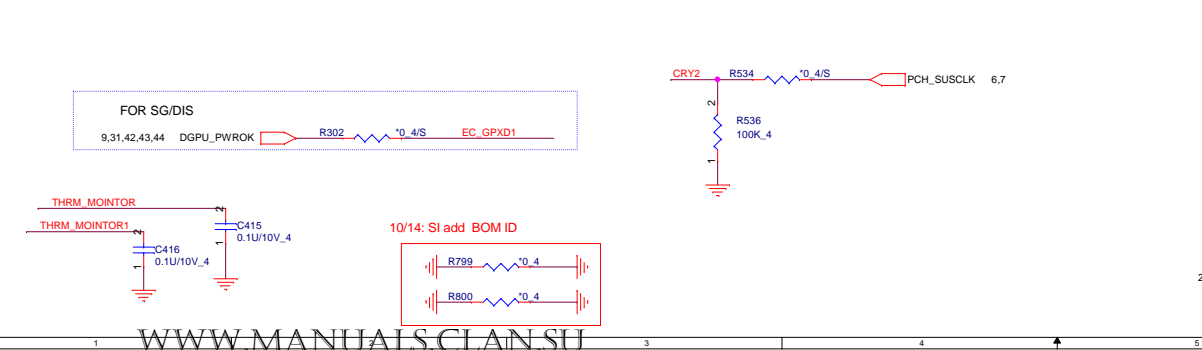
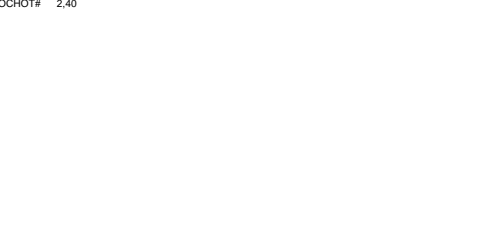
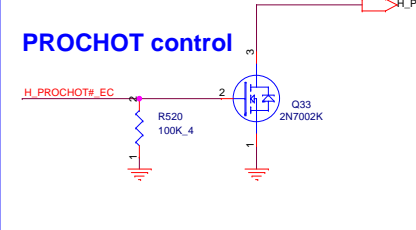
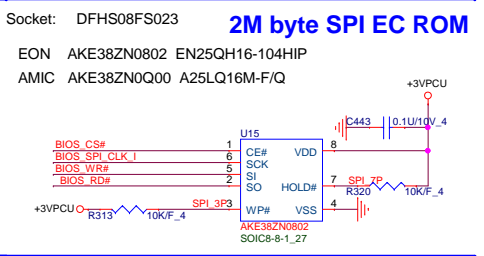
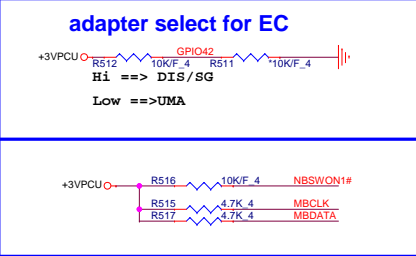
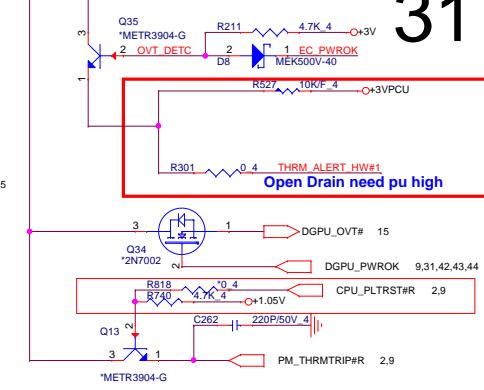
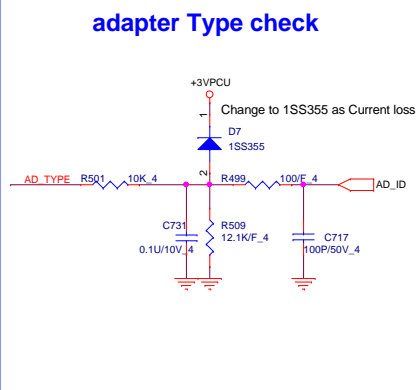
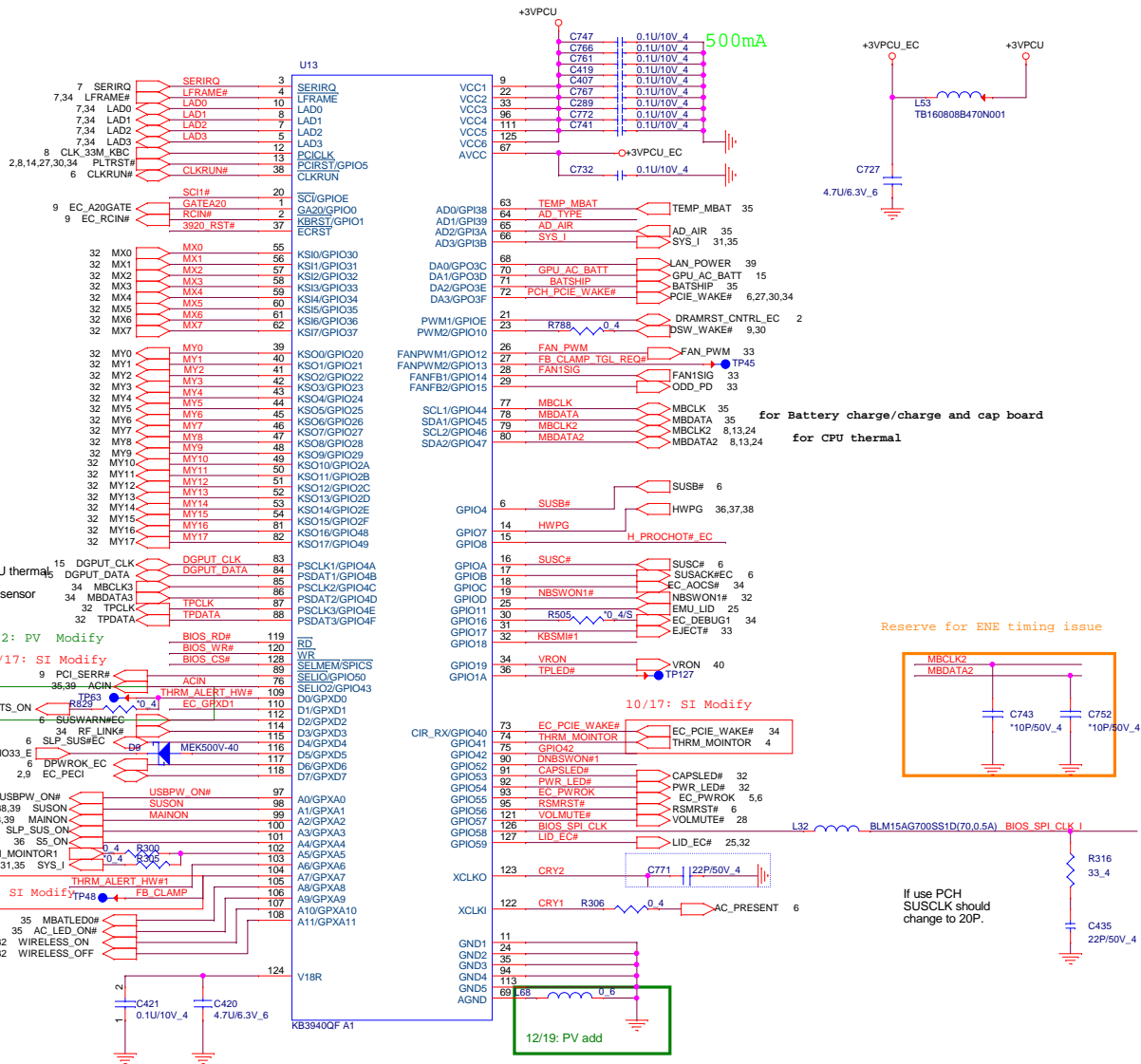
For GIGA
 BOT:GST5009B LF,DB0Z06LAN00
 FCE :NS892407 ,DB0LL1LAN00

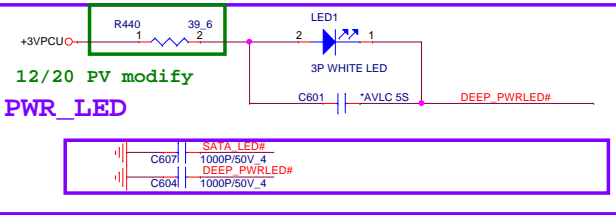
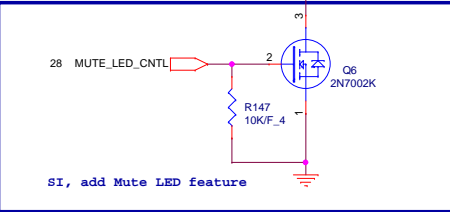
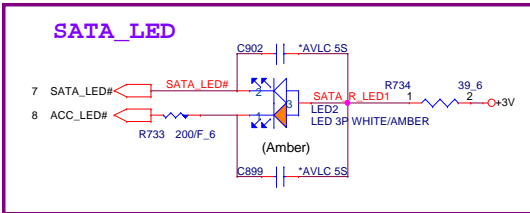
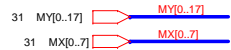
For 10/100
 BOT:TST1284R LF DB0EL5LAN00
 FCE :NS892408 ,DB0EF7LAN01



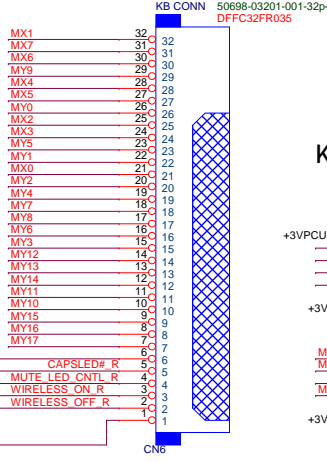
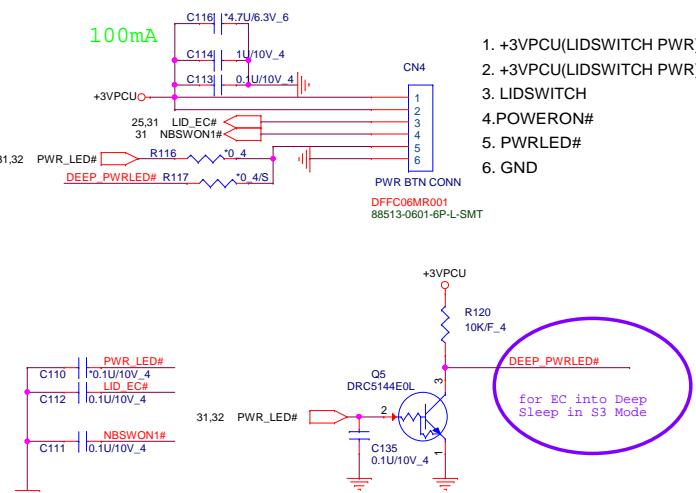
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCI_WAKE# pin)



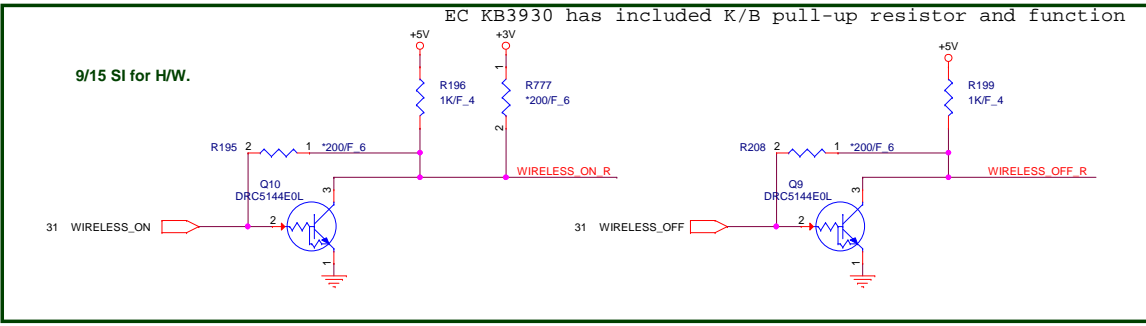
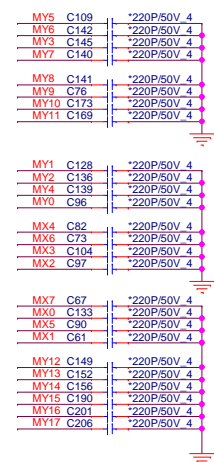
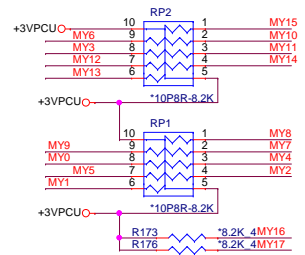




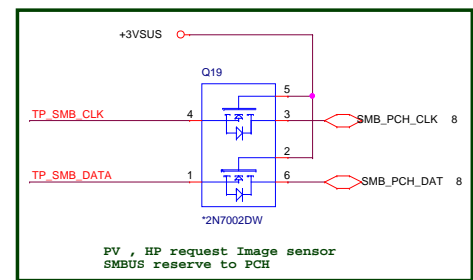
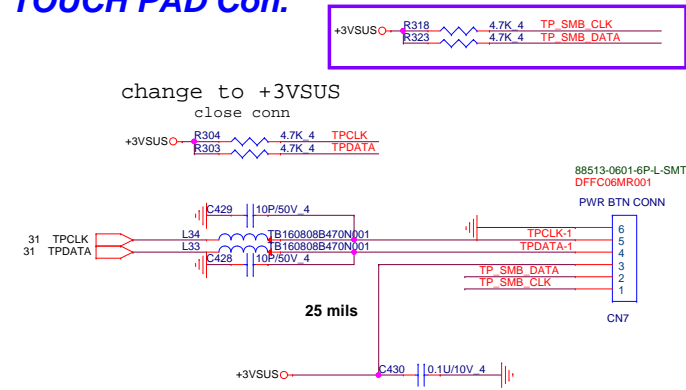
POWER BOTTON CONNECT



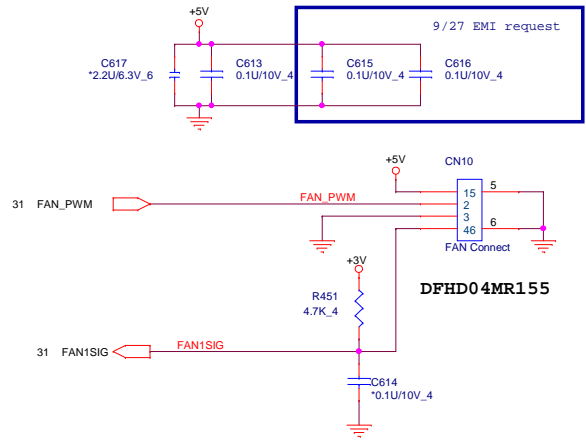
KEYBOARD PULL-UP



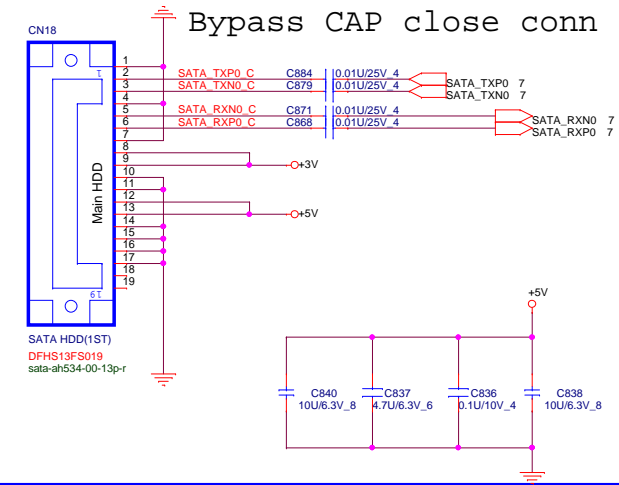
TOUCH PAD Con.



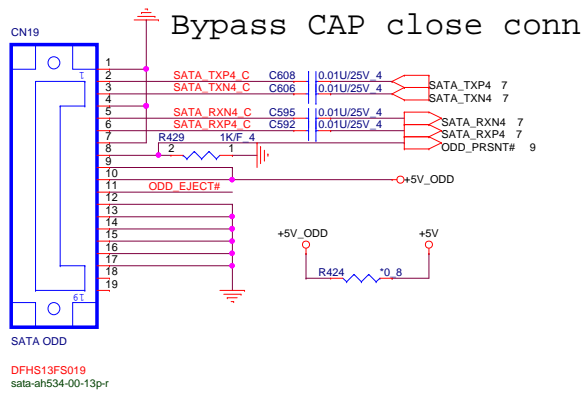
CPU FAN



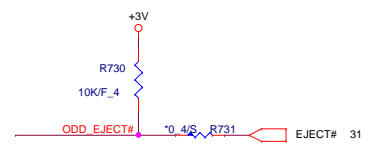
SATA HDD CONNECTOR



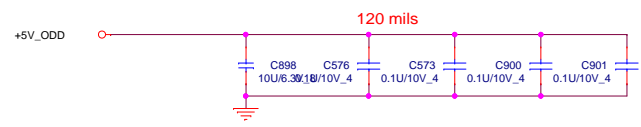
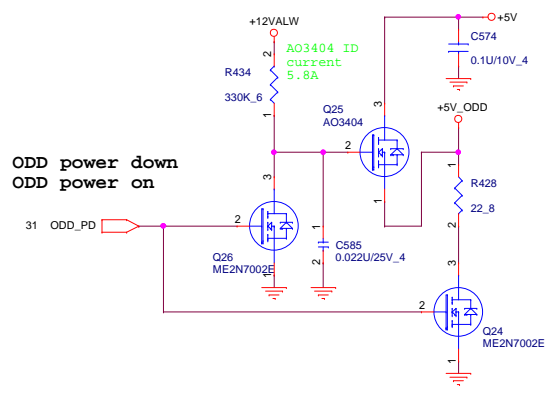
SATA ODD CONNECTOR



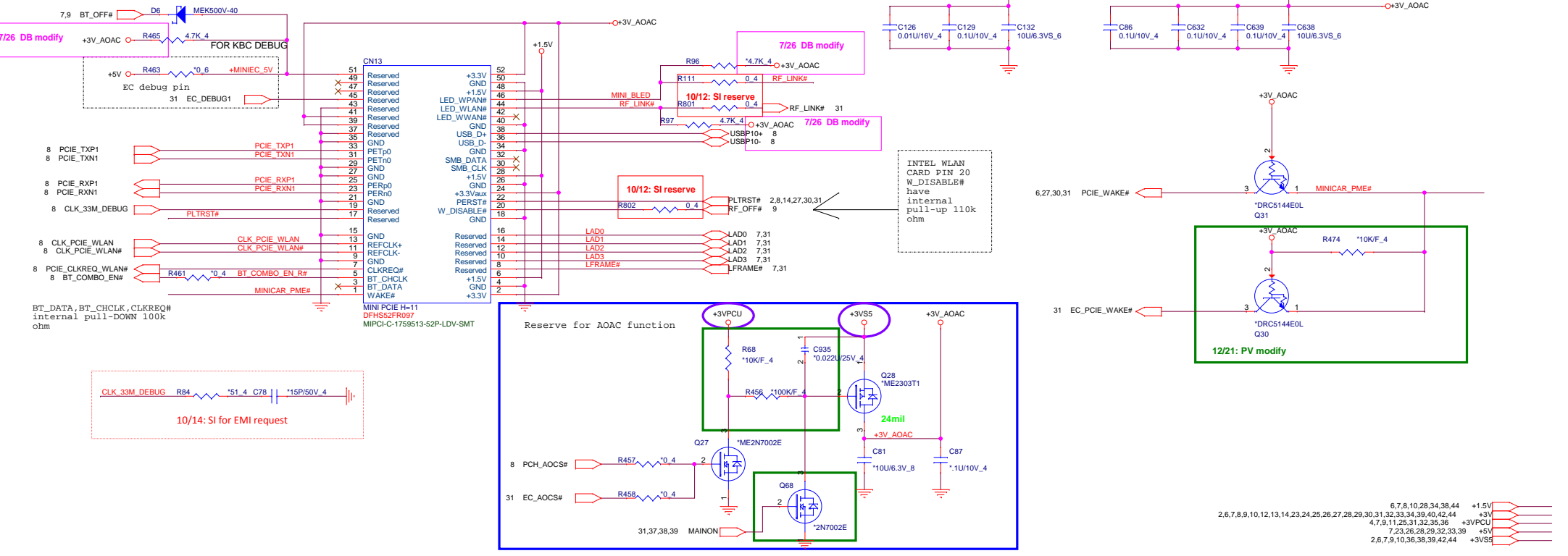
follow INTEL DG change eject PU to +3V.



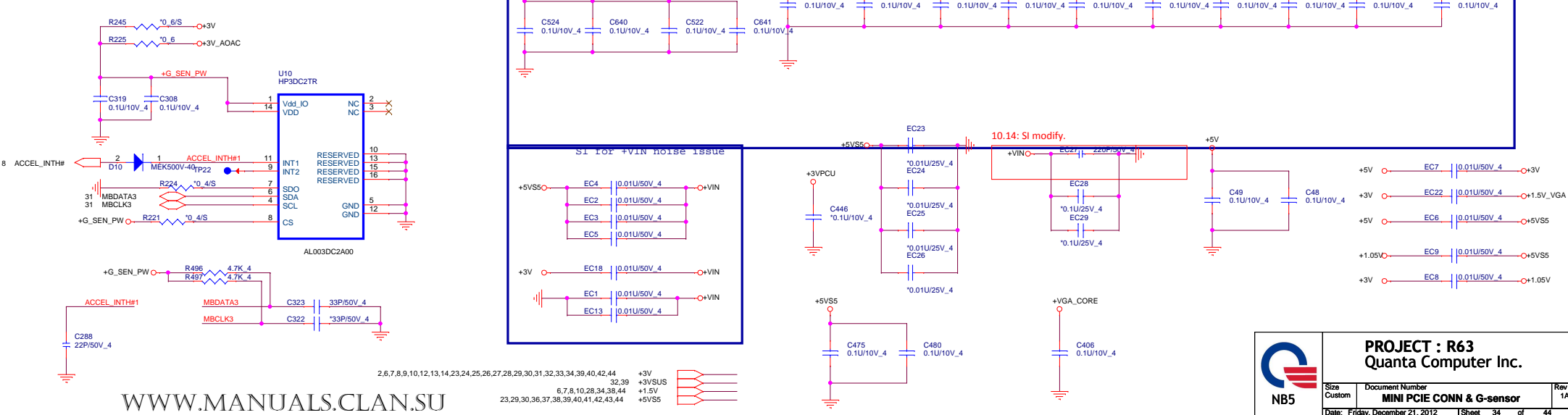
High : ODD power down
Low : ODD power on



Mini PCI-E Card 1 WLAN



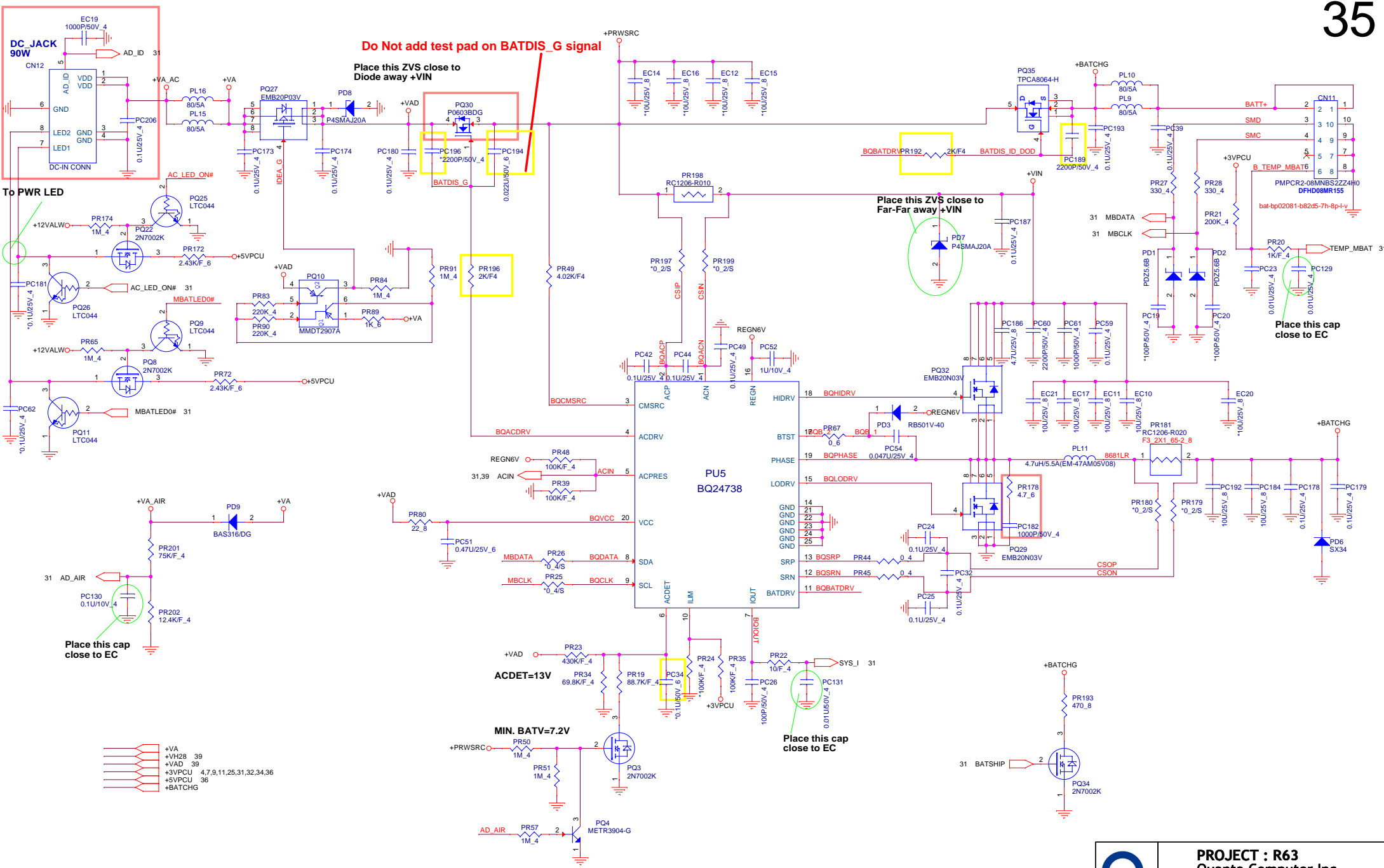
Accelerometer Sensor



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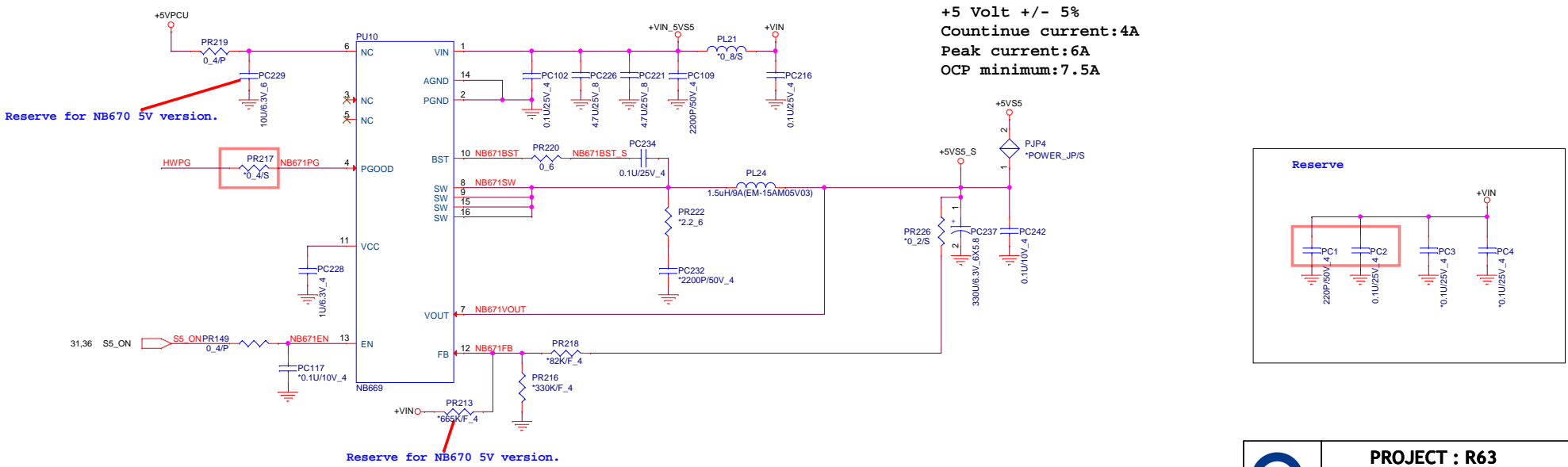
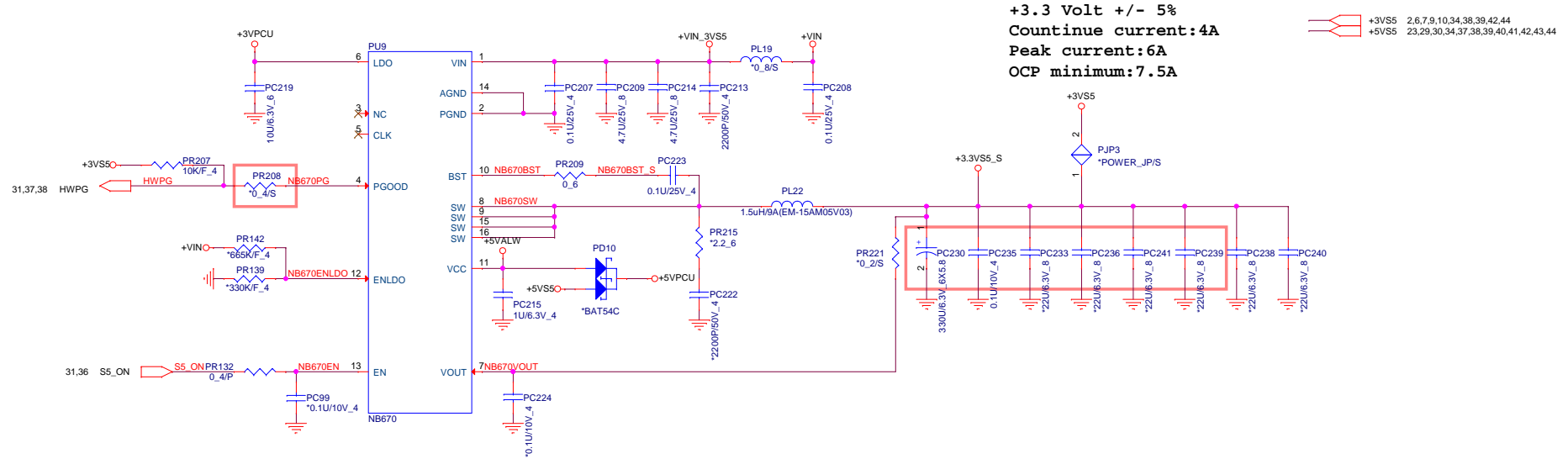
Size Custom Document Number **MINI PCI-E CONN & G-sensor** Rev 1A

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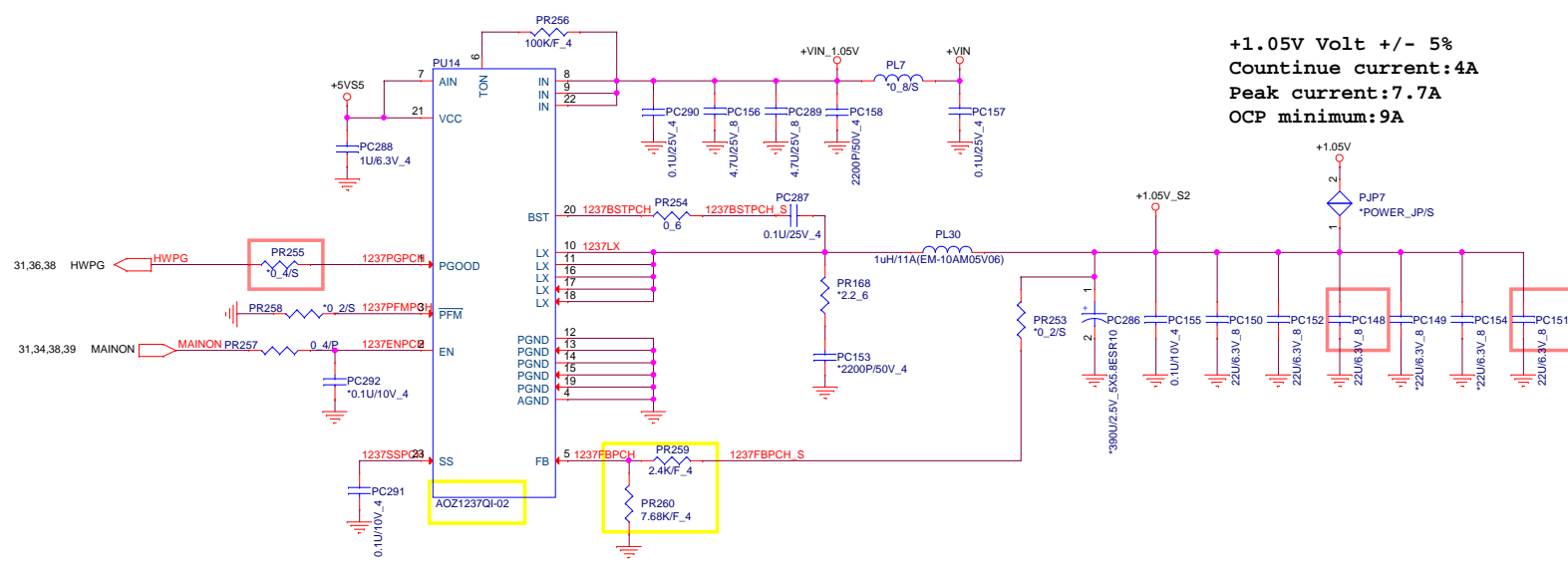


- +VA
- +VH28 39
- +VAD 39
- +3VPCU 4,7,9,11,25,31,32,34,36
- +5VPCU 36
- +BATV
- +BATSHIP

		PROJECT : R63 Quanta Computer Inc.	




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	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8243A)	
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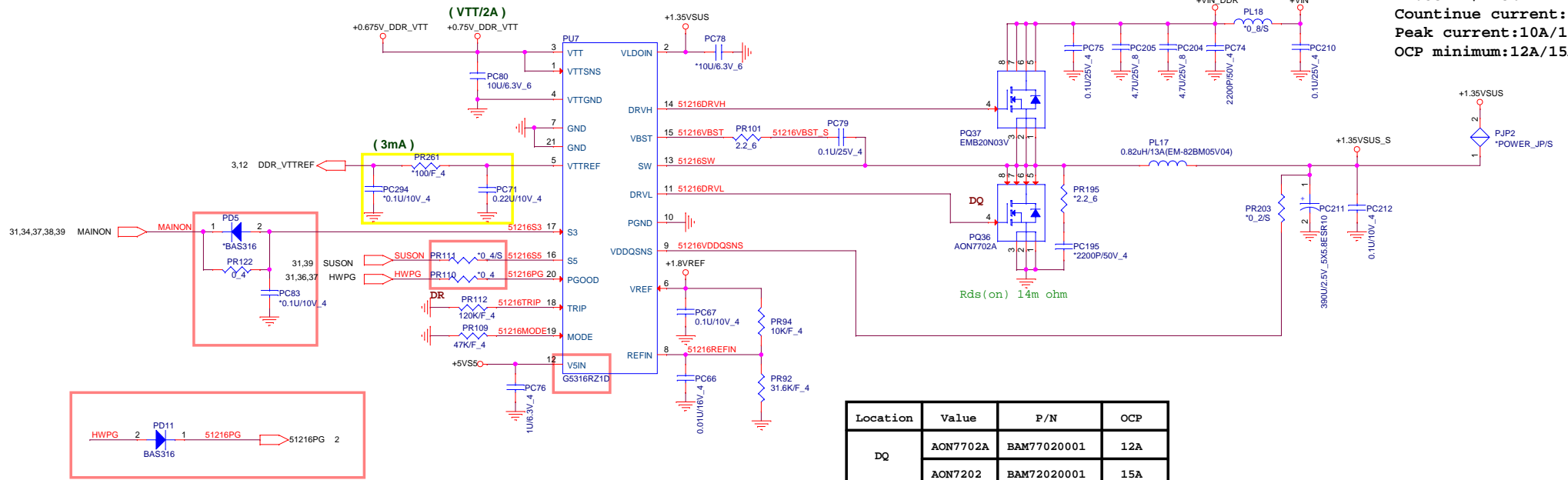
+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A

➔ +1.05V 2,4,9,10,11,31,34

	PROJECT : R63 Quanta Computer Inc.		
	Size Custom	Document Number 1.05V(RT8228BZ)	Rev 1A
	Date: Friday, December 21, 2012	Sheet 37 of 44	

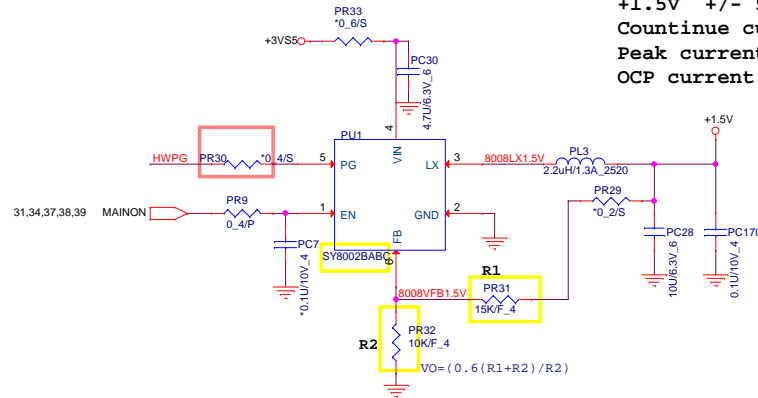
+1.35VSUS 2,3,4,12,13
+1.5V 6,7,8,10,28,34,44

+1.35V +/- 5%
Countinue current:6A/8A
Peak current:10A/12A
OCP minimum:12A/15A

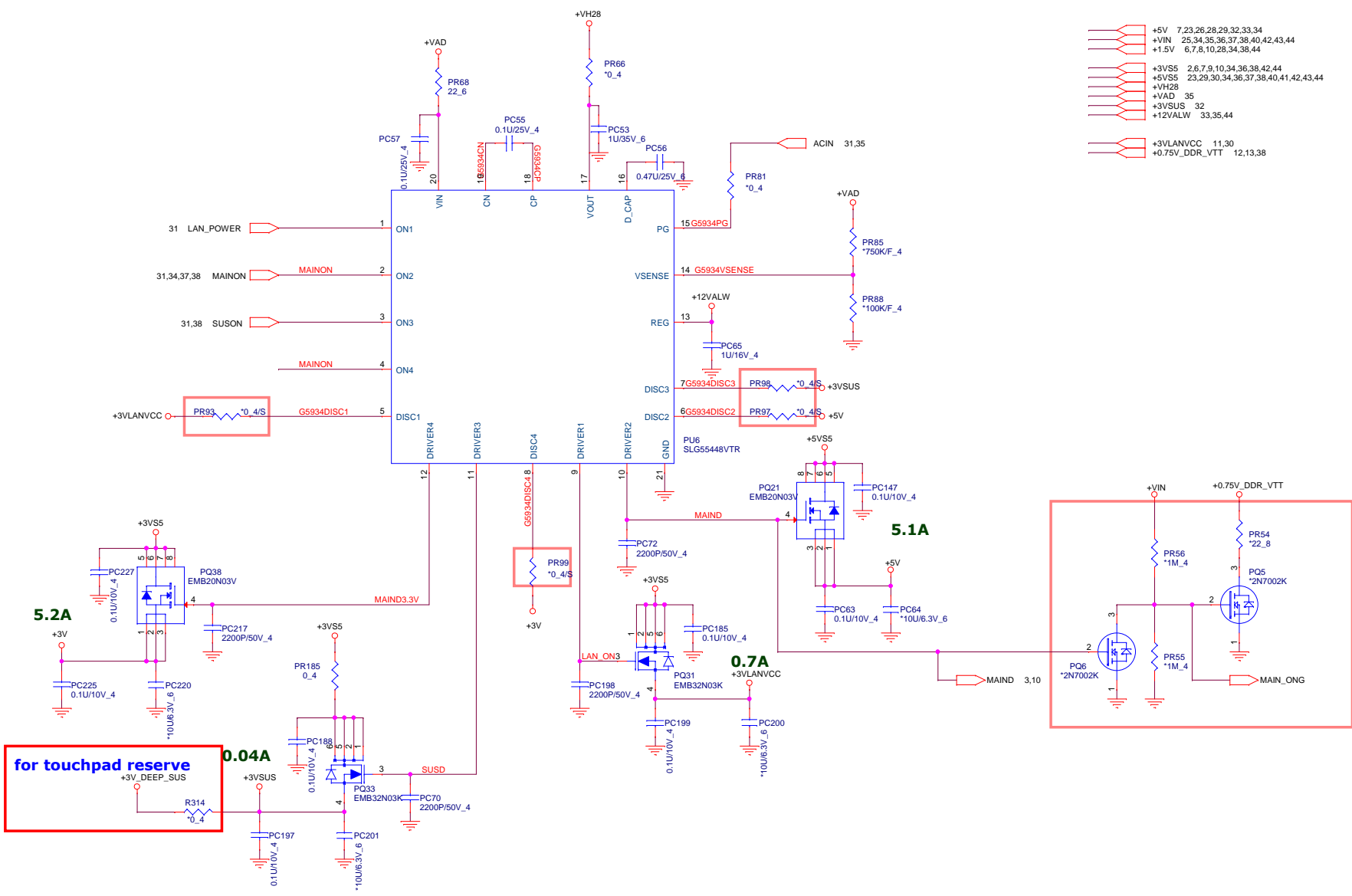


Location	Value	P/N	OCP
DQ	AON7702A	BAM77020001	12A
	AON7202	BAM72020001	15A
DR	120K	CS41202FB17	12A
	76.8K	CS37682FB00	15A

+1.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
OCP current:1.2A



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	Quanta Computer Inc.		
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- +5V 7,23,26,28,29,32,33,34
- +VIN 25,34,35,36,37,38,40,42,43,44
- +1.5V 6,7,8,10,28,34,38,44
- +3VS5 2,6,7,9,10,34,36,38,42,44
- +5VS5 23,29,30,34,36,37,38,40,41,42,43,44
- +VH2B
- +VAD 35
- +3VSUS 32
- +12VALW 33,35,44
- +3VLANVCC 11,30
- +0.75V_DDR_VTT 12,13,38

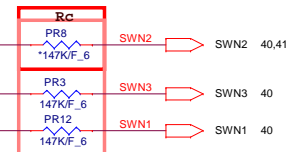
for touchpad reserve

	PROJECT : R63		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number Dis-charge IC (G5934)	
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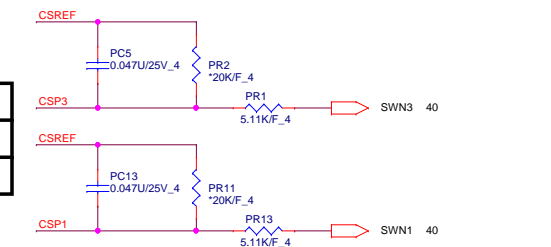
CPU	Re	PR18
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

PUT COLSE TO VCORE Phase 1 Inductor

Dummy Rc For 2 phase



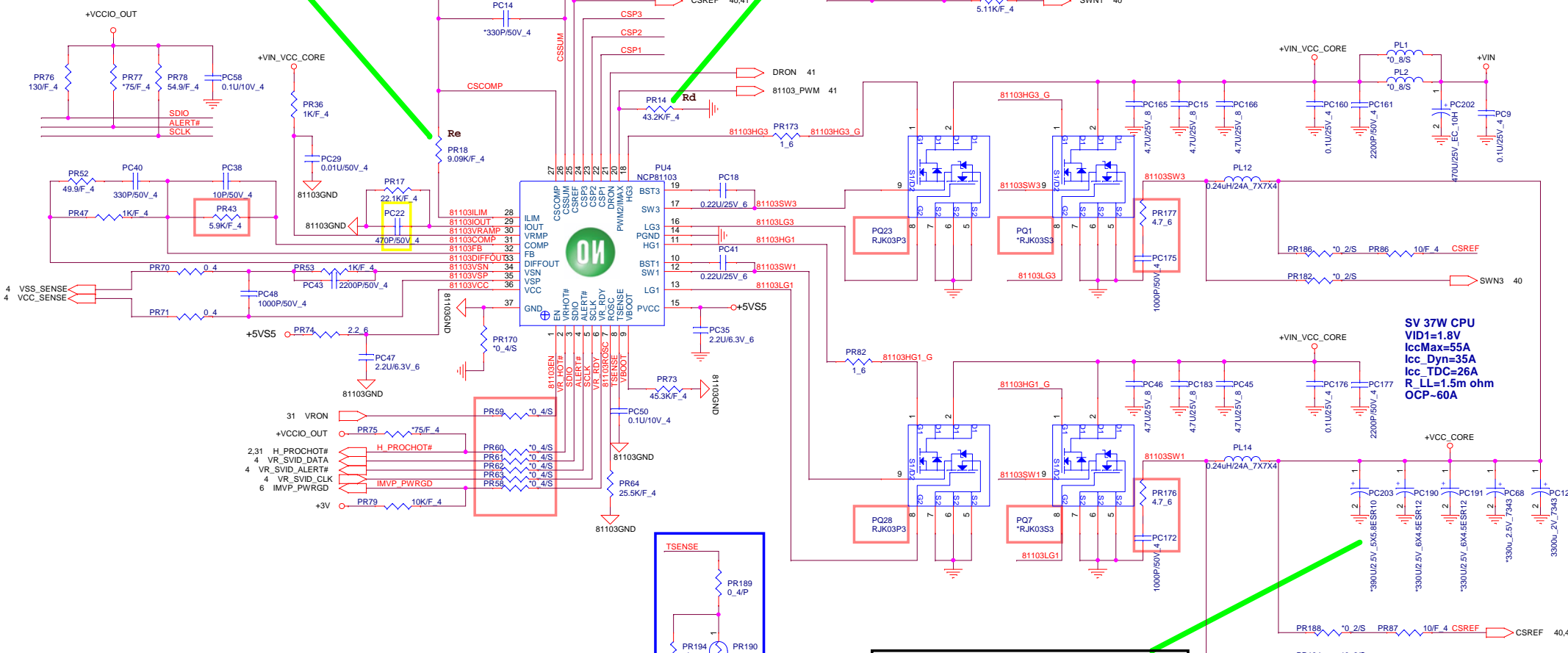
Dummy Ra and Ca For 2 phase



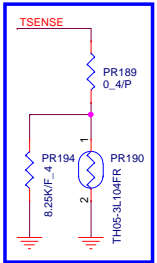
POP Rb for 2 phase



CPU	Rd	PR14
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16



SV 37W CPU
 VID1=1.8V
 IccMax=55A
 Icc_Dyn=35A
 Icc_TDC=26A
 R_LL=1.5m ohm
 OCP=60A



PUT COLSE TO VCORE HOT SPOT

For 37W CPU ; PC128 Placed 330uF_9 mohm
 For 47W CPU ; PC128 Placed 560uF_4.5 mohm

CPU	Ra	Ca	Rb	Rc	Rd	Re	
37W	Dummy	Dummy	POP	Dummy	CS34322FB00	CS29092FB27	CH733RY8802
47W	POP	POP	Dummy	POP	CS36652FB16	CS31472FB14	CH756RM8802

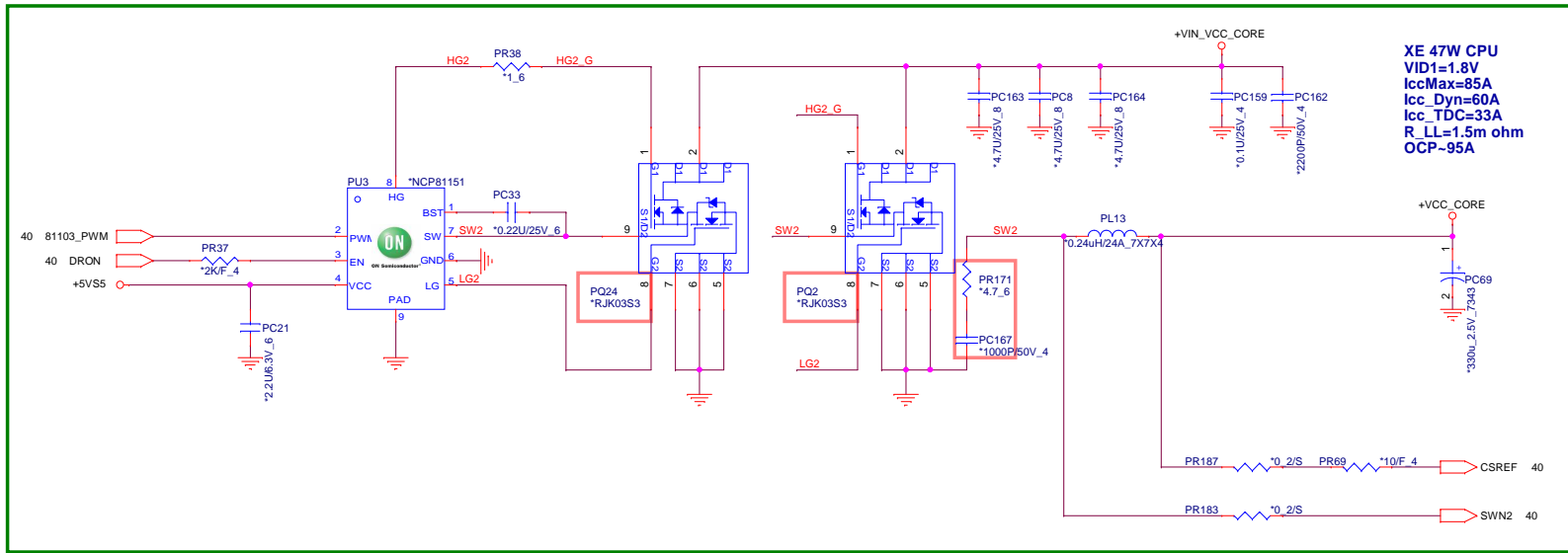
R63 Location	PR10	PC6	PR4	PR8	PR14	PR18	PC128

CPU	PC128
37W	CH733RY8802
47W	CH756RM8802



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For 37W CPU
 Dummy these components

+VCC_CORE 4,40

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GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE	Default
0	1	0	1.0V	Default
1	0	0	0.9V	
1	0	1	0.875V	

Default

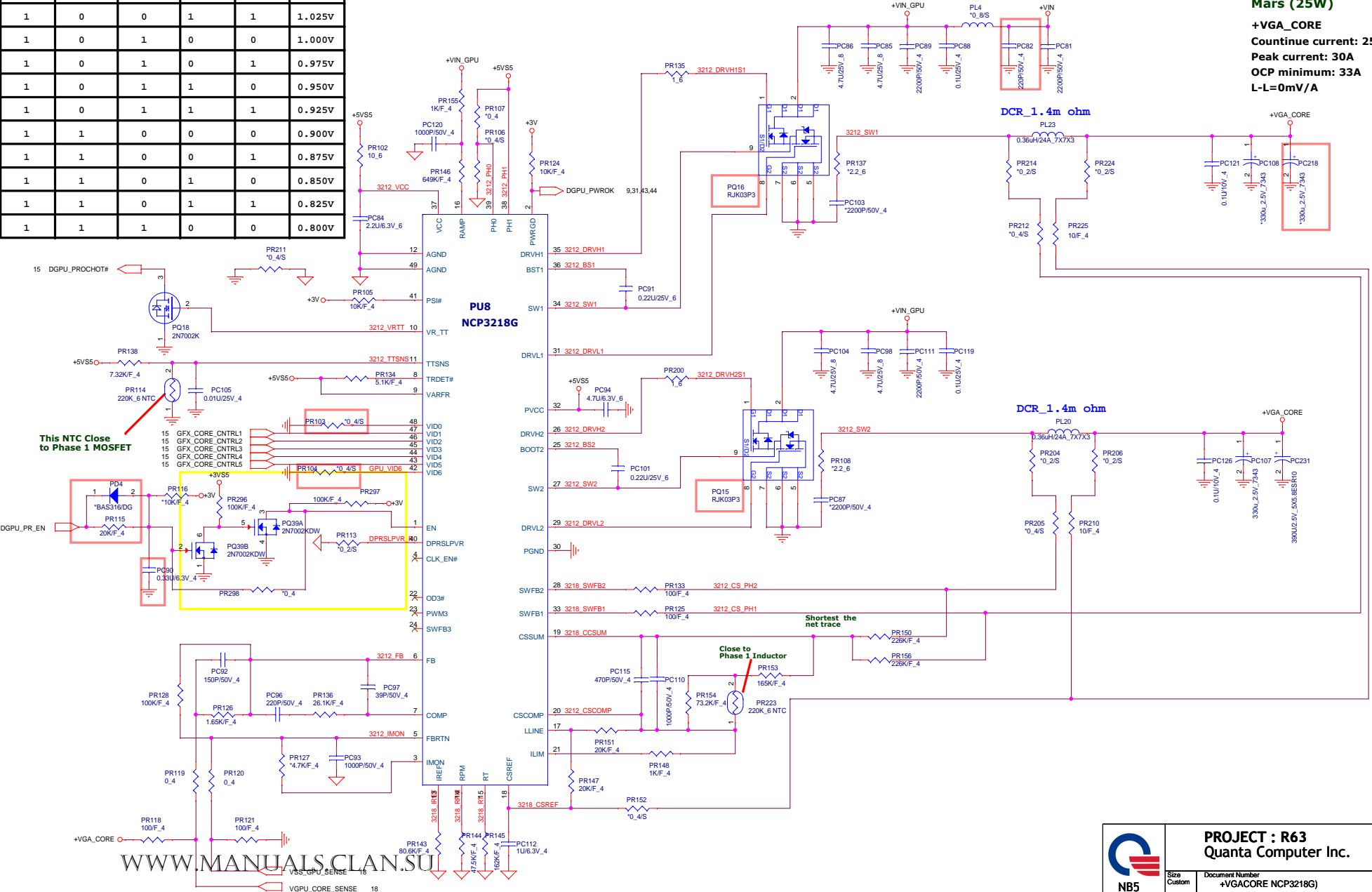
GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	Default
0	1	1	1	1	1.125V	Default
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	

Default

Mars (25W)

+VGA_CORE
 Continuum current: 25A
 Peak current: 30A
 OCP minimum: 33A
 L-L=0mV/A

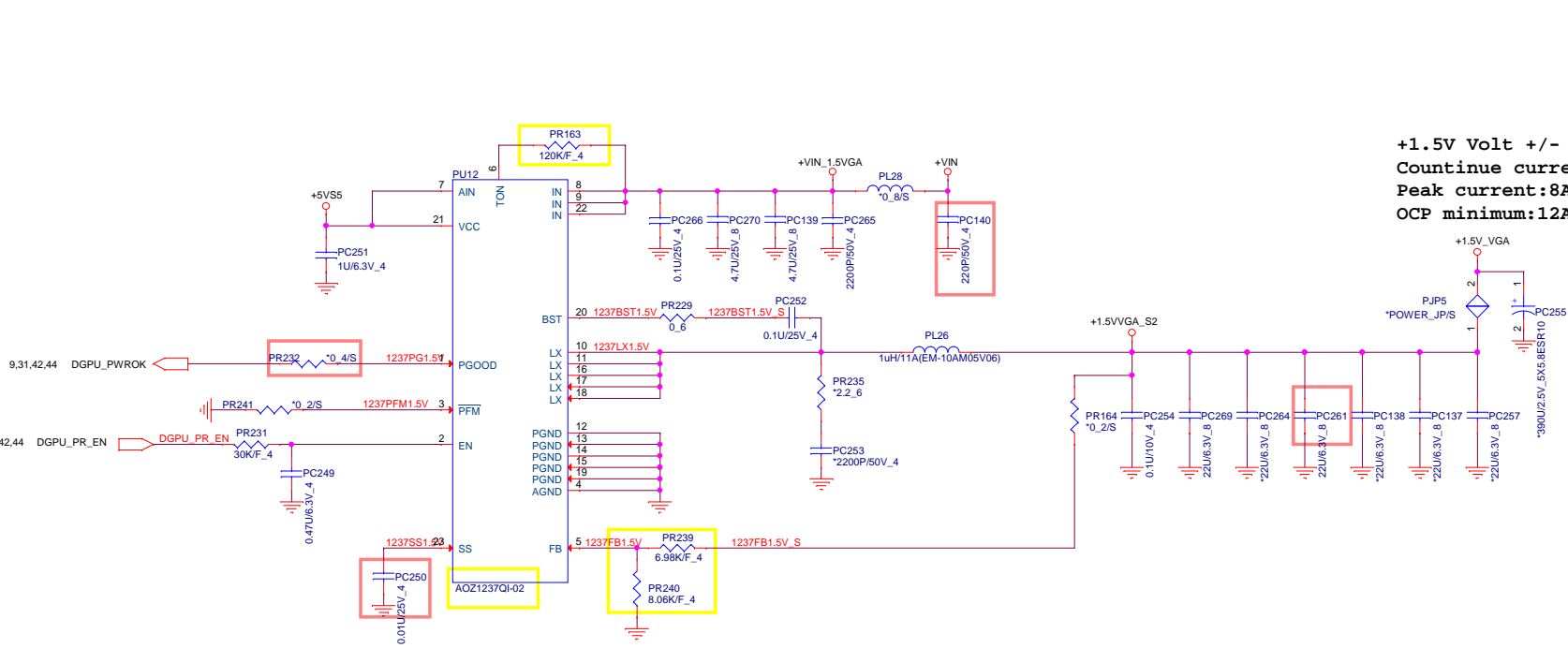


This NTC Close to Phase 1 MOSFET


Shortest the net trace

Close to Phase 1 Inductor

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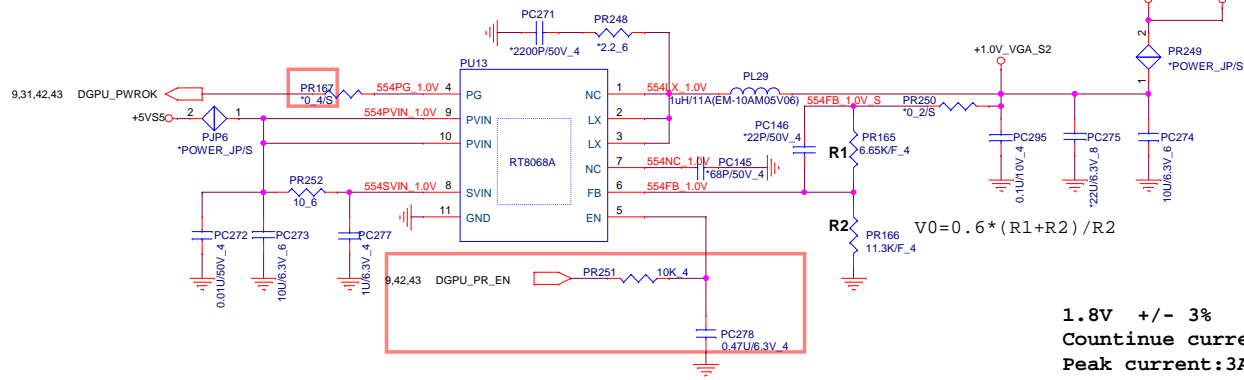


+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

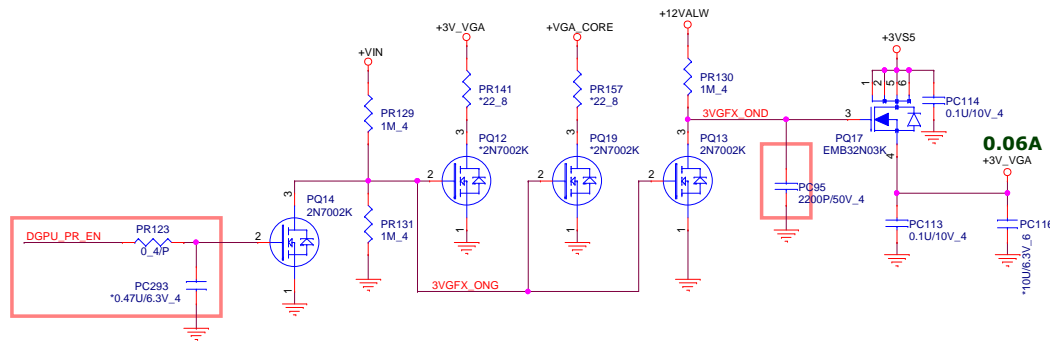
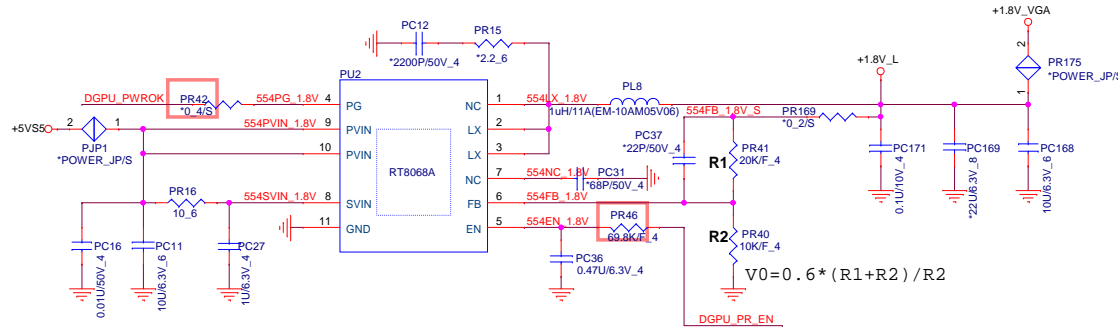
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VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

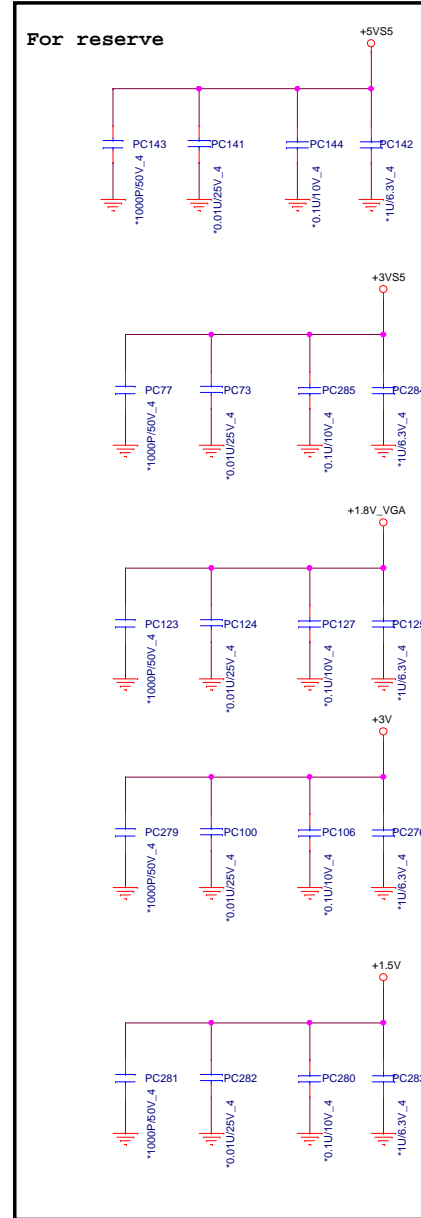
+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



+1.8V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



- +1.8V_VGA 11,15,16,18,19
- +1.0V_VGA 14,16,18,19
- +3V_VGA 14,18



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