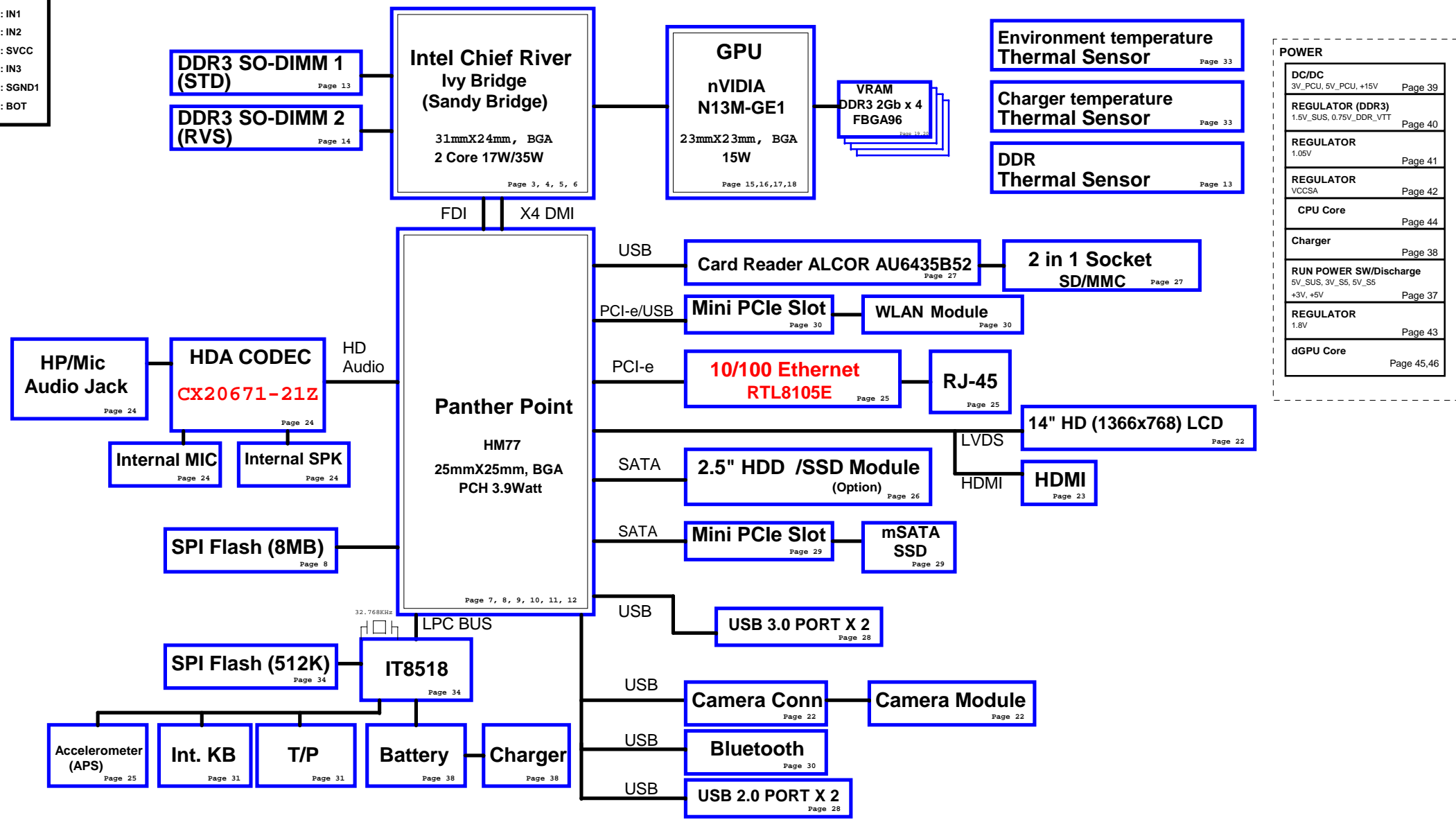


LZ8 14" Block Diagram -- Intel Chief River ULV

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



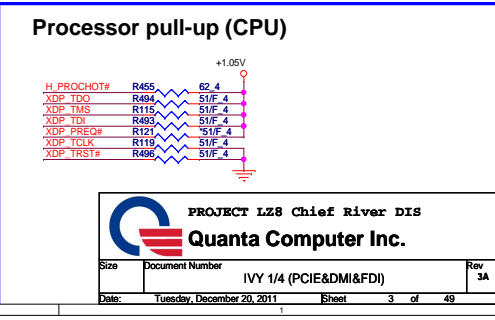
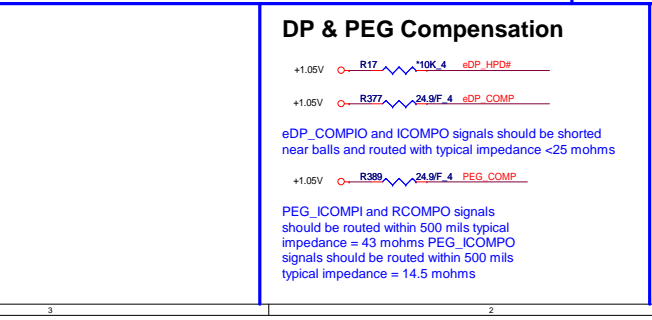
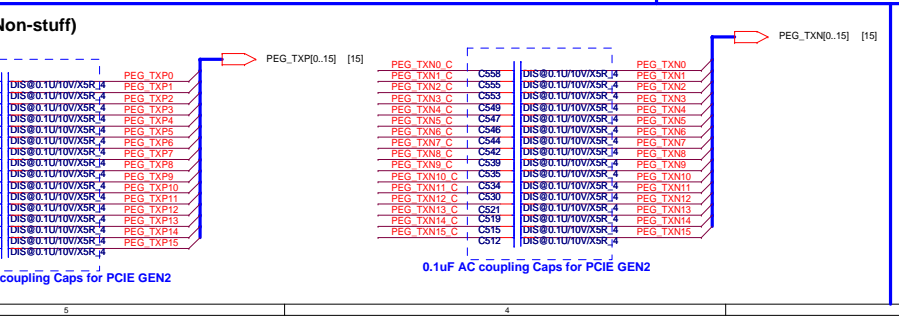
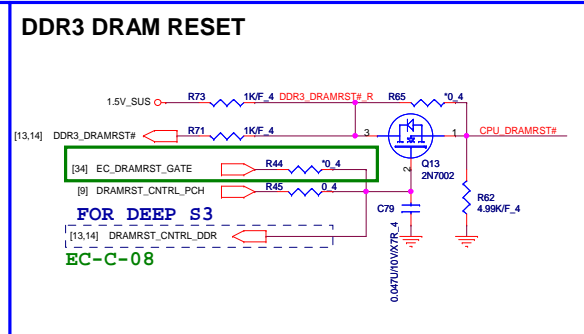
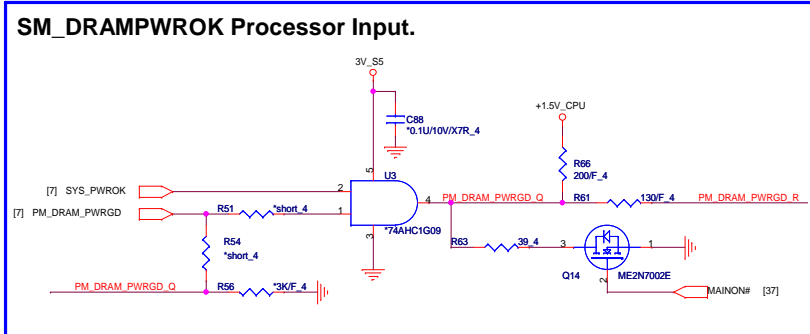
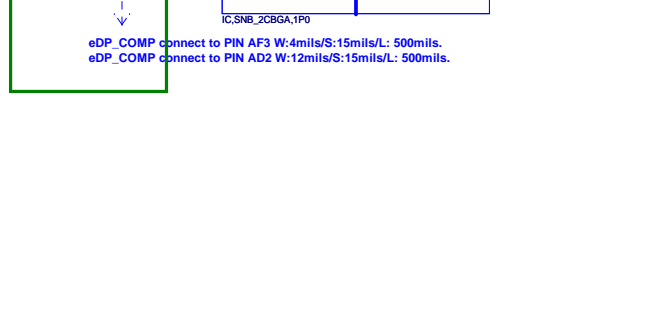
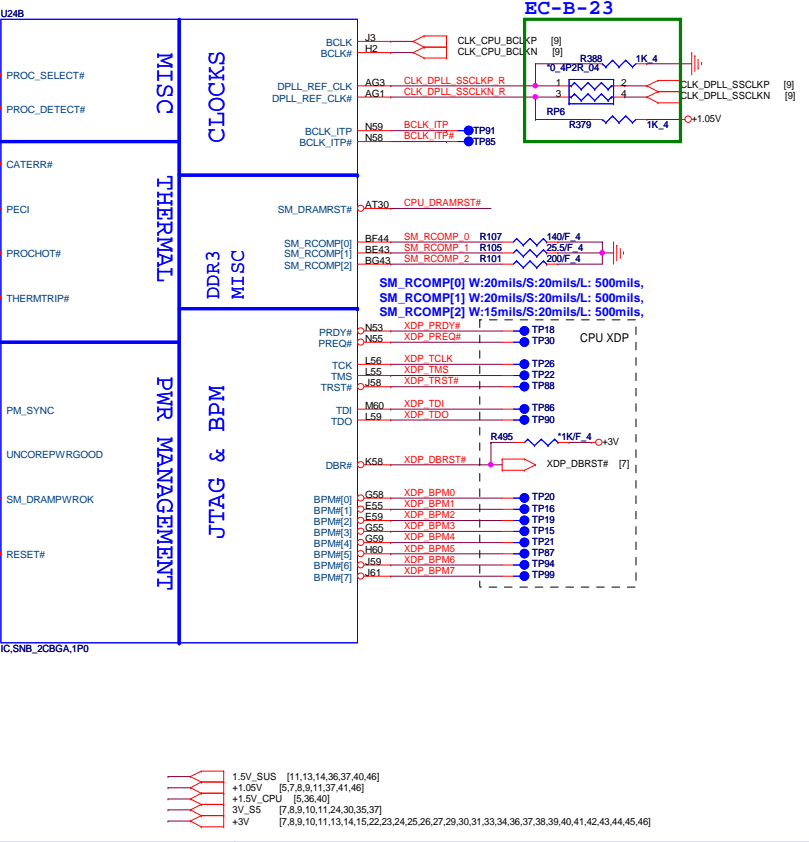
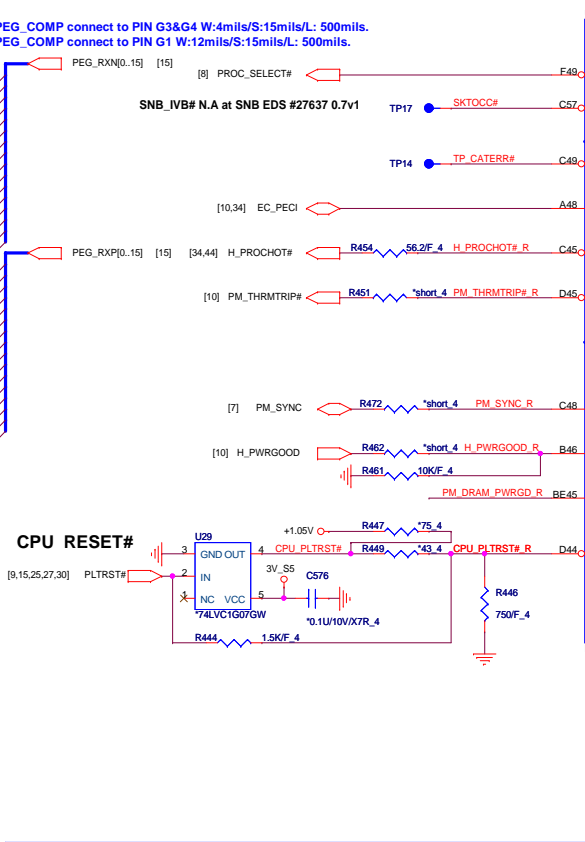
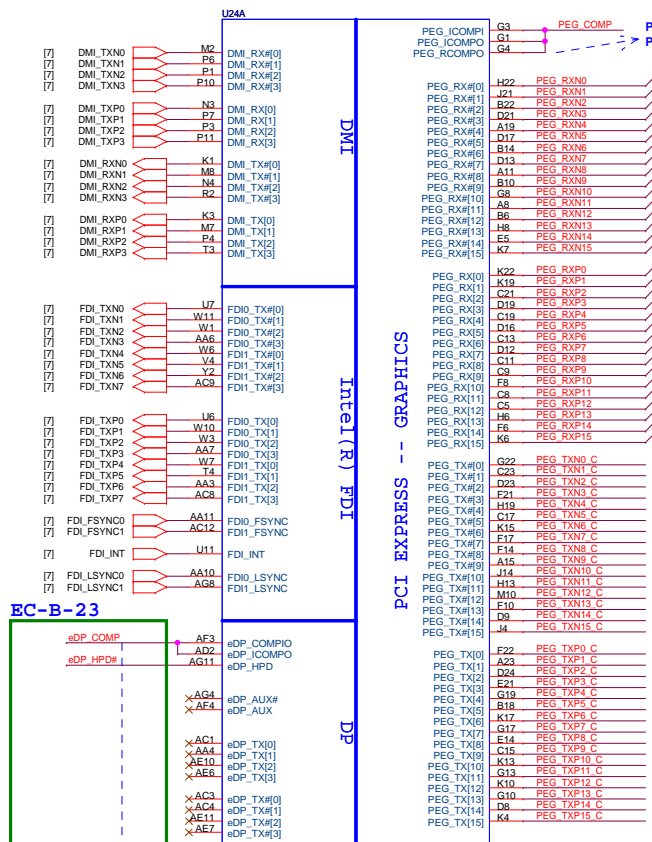
POWER	
DC/DC	3V_PCU, 5V_PCU, +15V Page 39
REGULATOR (DDR3)	1.5V_SUS, 0.75V_DDR_VTT Page 40
REGULATOR	1.05V Page 41
REGULATOR	VCCSA Page 42
CPU Core	Page 44
Charger	Page 38
RUN POWER SW/Discharge	5V_SUS, 3V_S5, 5V_S5 +3V, +5V Page 37
REGULATOR	1.8V Page 43
dGPU Core	Page 45,46

Table of Contents

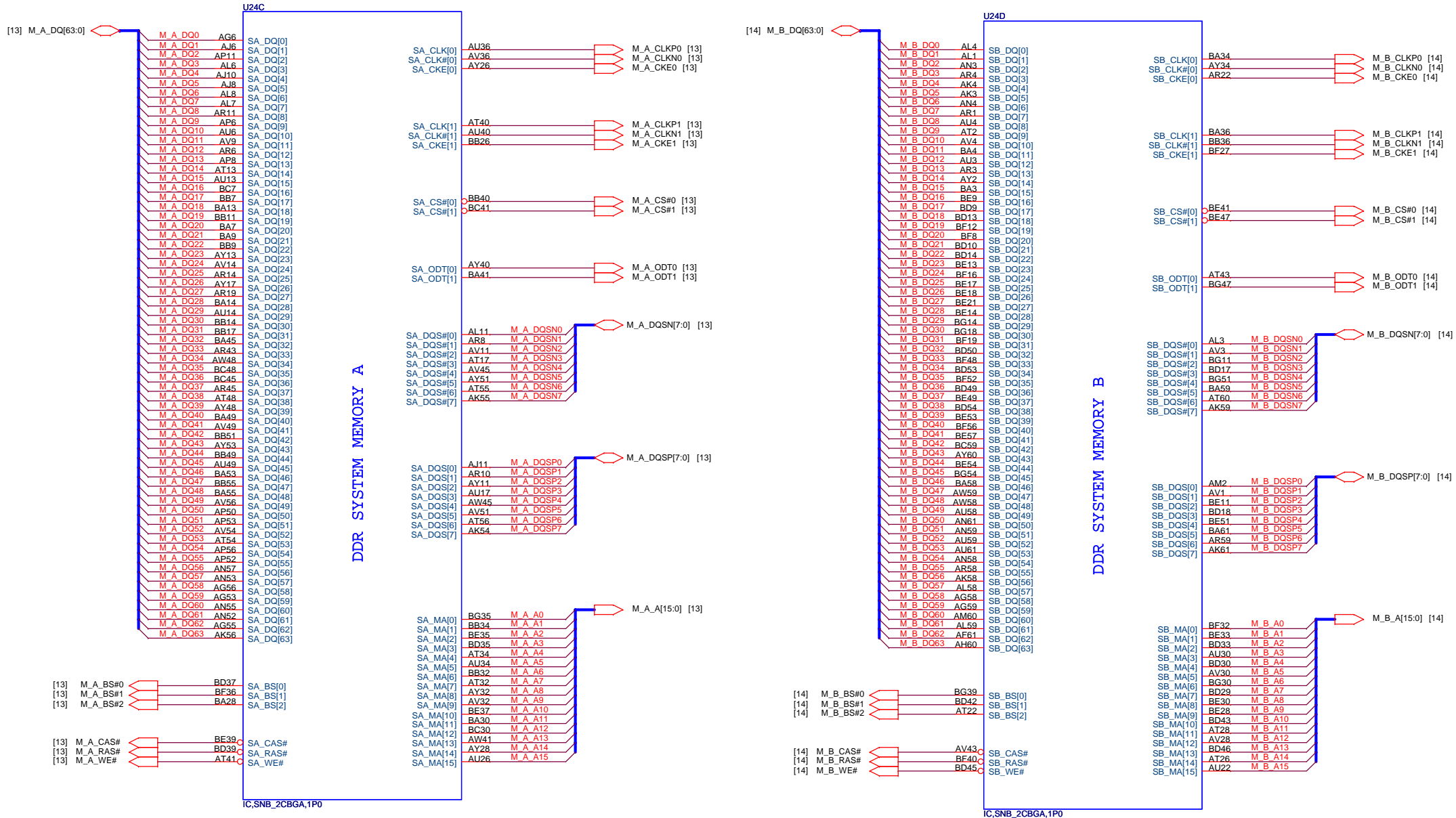
PAGE	DESCRIPTION
01	BLOCK DIAGRAM
02	FRONT PAGE
03-06	IVY/Sandy Bridge
07-12	Panther/Cougar Point-PCH
13-14	DDR3 SO-DIMM
15-18	N13M
19-20	N13M VRAM
21	PS8622 LVDS converter
22	LCD/CAMERA
23	HDMI CONN
24	Audio Codec CX20672
25	LAN[RTL8105E]
26	SATA
27	Card Reader-AU6435B52-GDL
28	USB2.0 X2/USB3.0 X2
29	MINI Card (SSD)
30	WLAN/BT
31	KB/TP/LID
32	USB2.0--Audio Jack conn
33	FAN/Thermal
34	KBC IT8518
35	SW/LED
36	Screw Hole/EMI/ESD
37	Discharge
38	CHARGER (bq24725A)
39	3V/5V (TPS51123ARGER)
40	DDR3/0.75V (TPS51216)
41	1.05V_PCH(RT8240B)
42	VCCSA (RT8241A)
43	1.8V(TPS54318)
44	CPU(ISL95831)IMVP2+1
45	DGPU CORE(TPS51728)
46	GPU
47	
48	
49	
50	
51	

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,36,38,39,40,41,42,44,45	MAIN POWER		S0-S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0-S5
3VPCU	+3.3V	7,8,22,23,25,30,31,34,35,36,37,38,39,43,45	IT8518/19 POWER	3V5V_EN	S0-S5
5VPCU	+5V	22,36,37,39,40,41,42,43,44,45,46	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
15V	+15V	22,37,39,40,46	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	25,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,24,28,32,37	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	3,7,8,9,10,11,30,35,37,45	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0-S3
1.5V_SUS	+1.5V	3,11,13,14,36,37,40,46	DDR3 SODIMM POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	13,14,37,40	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,22,23,24,26,31,33,36,37,38	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,21,22,23,24,25,26,27,29,30,31,33,34,35,36,37,38,39,40,41,42,43,44,45,46	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX		5,36,44	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,37,42	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,37,43	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,21,36,37,41,46	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,36,44	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	22	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	38	MAIN BATTERY	CHG_PBATT	S0-S5
+1.5V_CPU	+1.5V	3,5,36	DDR3 1.5V Rails	PS_S3CNTRL	S0

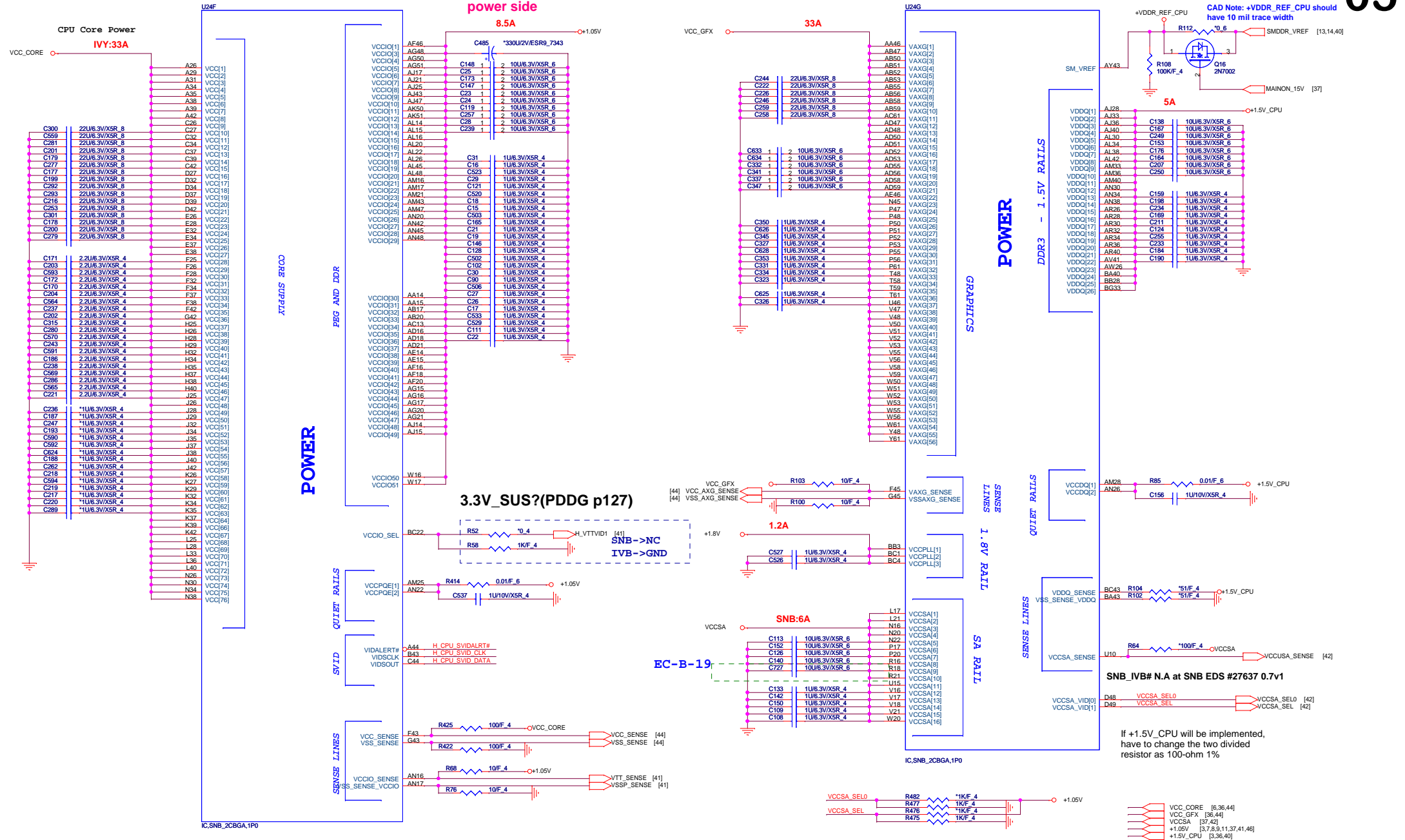


Ivy/Sandy Bridge Processor (DDR3)



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	IVY 2/4 (DDR3 I/F)	Rev
	Custom		1A
Date:	Tuesday, December 20, 2011	Sheet	4 of 49



POWER

POWER

GRAPHICS

DDR3 - 1.5V RAILS

1.8V RAIL

SA RAIL

OUTLET RAILS

SENSE LINES

3.3V_SUS?(PDDG p127)

EC-B-19

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

SVID CLK



SVID DATA

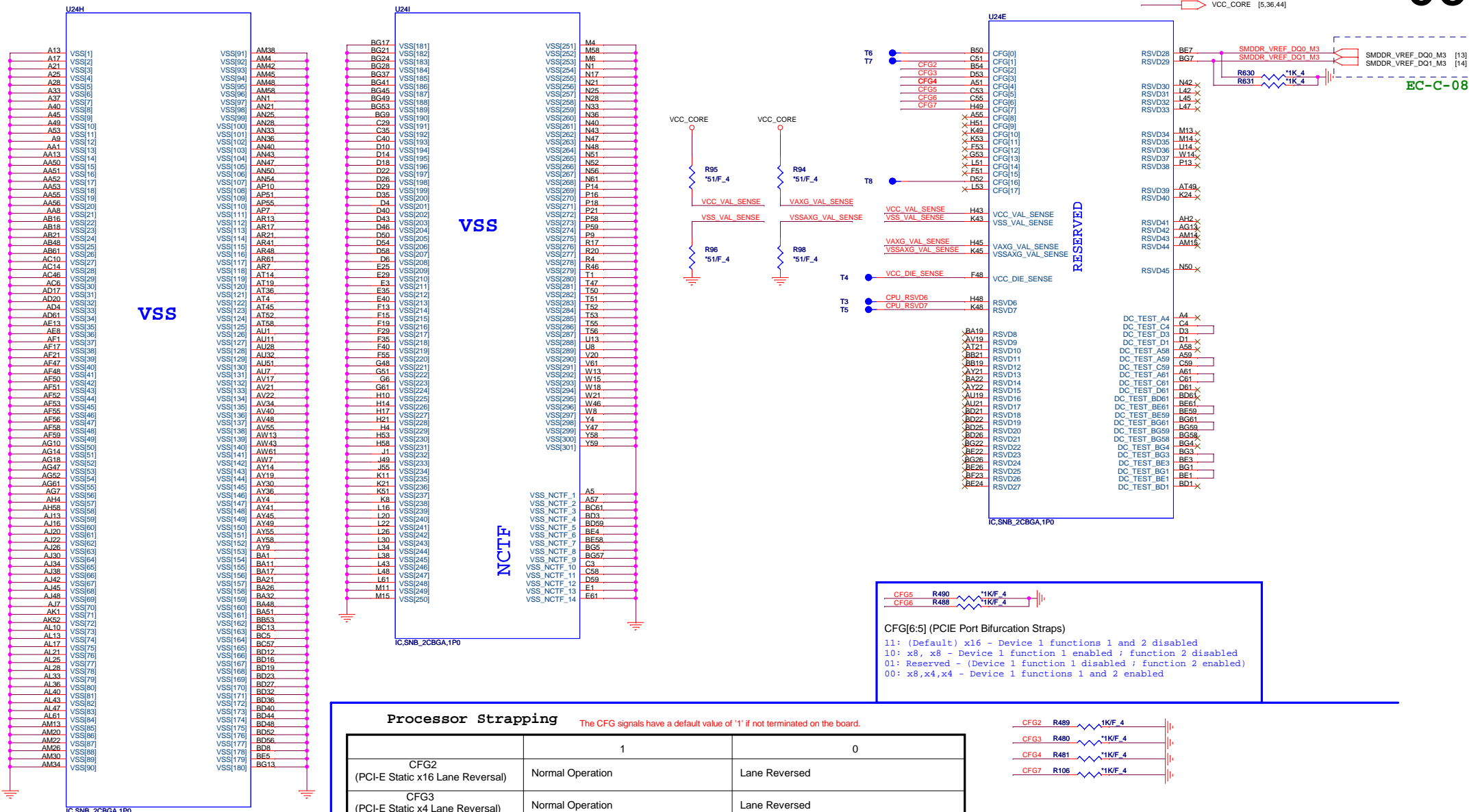


SVID ALERT



PROJECT IZ8 Chief River DIS
Quanta Computer Inc.

Size: _____ Document Number: SNB 3/4 (POWER) Rev: 1A
 Date: Tuesday, December 20, 2011 Sheet: 5 of 49



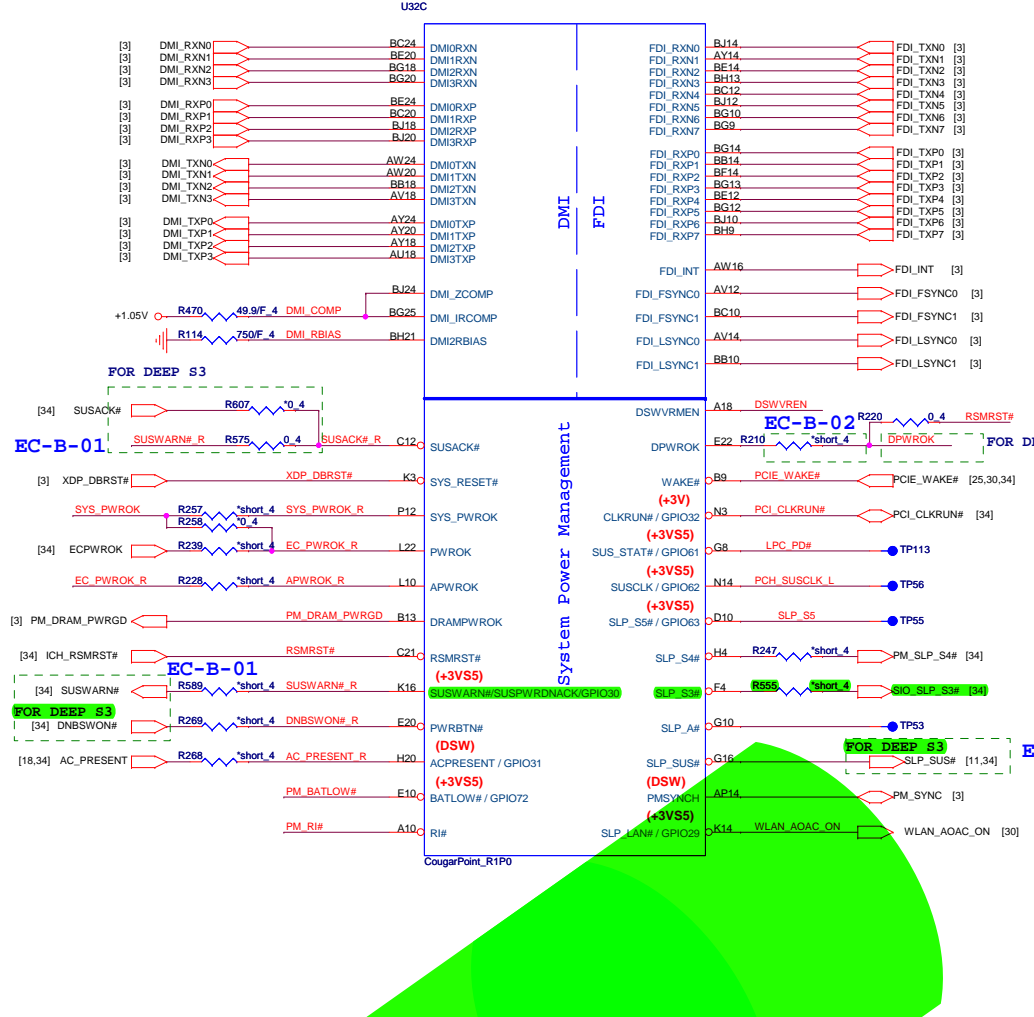
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

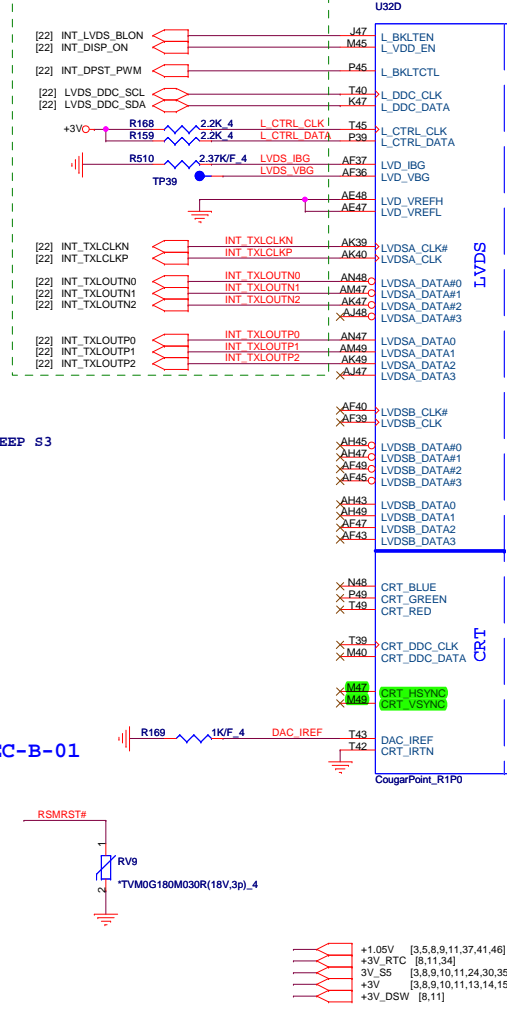
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

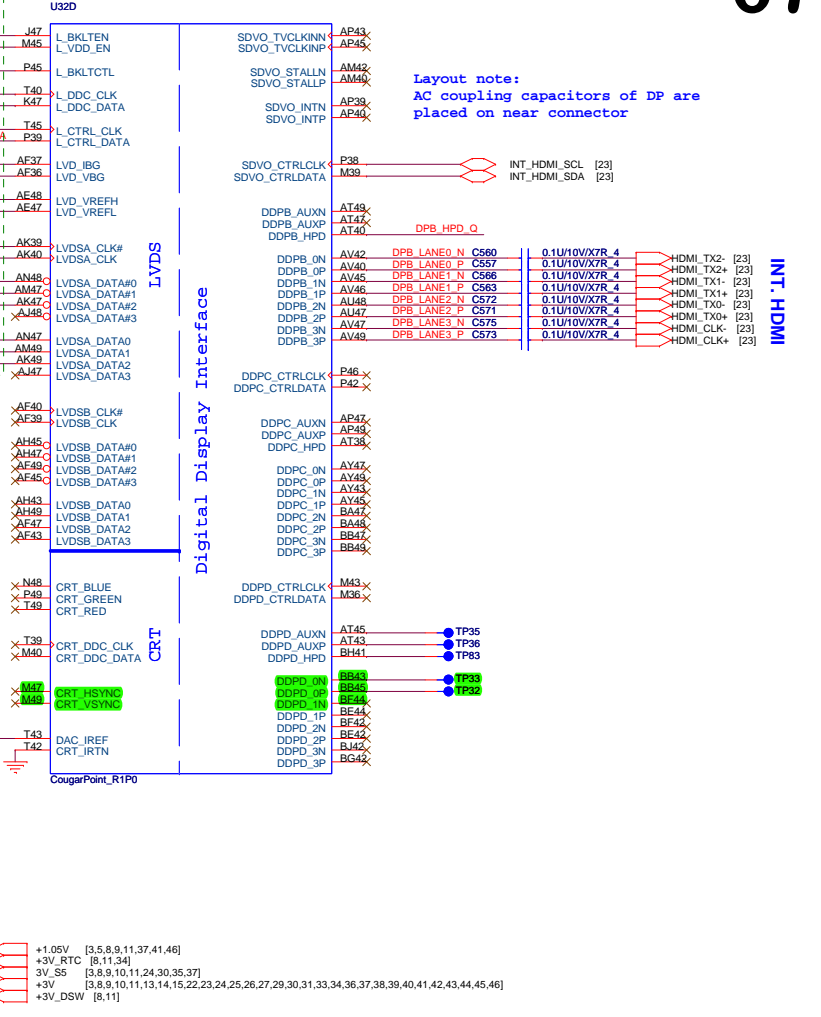
Panther/Cougar Point (DMI, FDI, PM)



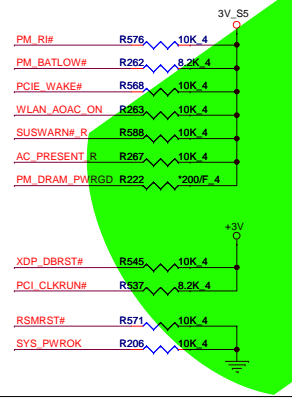
EC-B-23



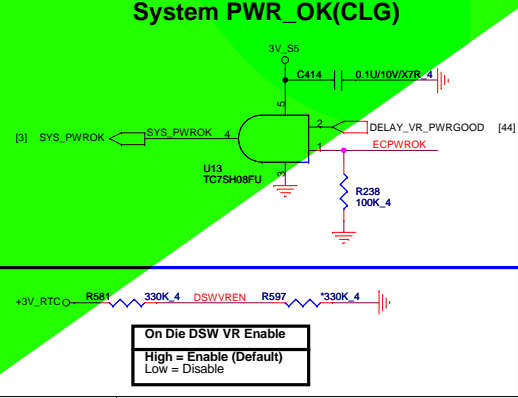
Panther/Cougar Point (LVDS, DDI)



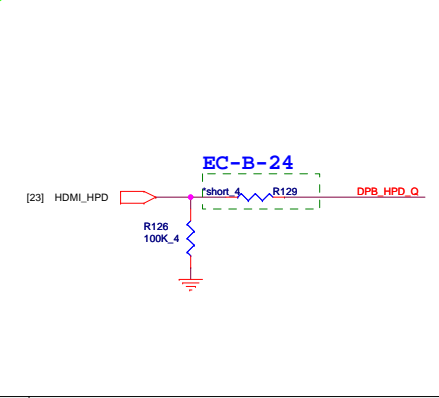
PCH Pull-high/low (CLG)



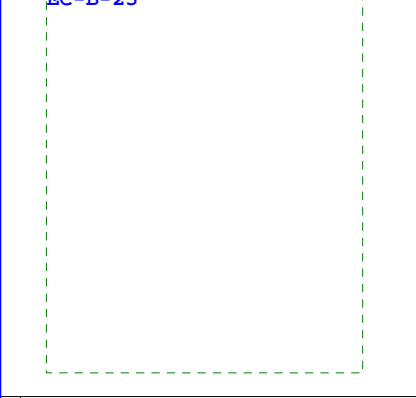
System PWR_OK (CLG)



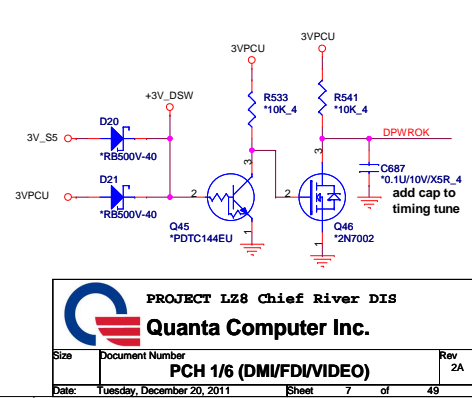
INT HDMI DETECT



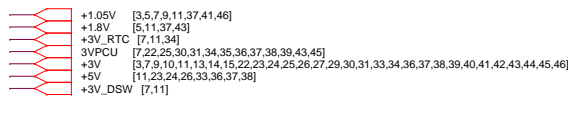
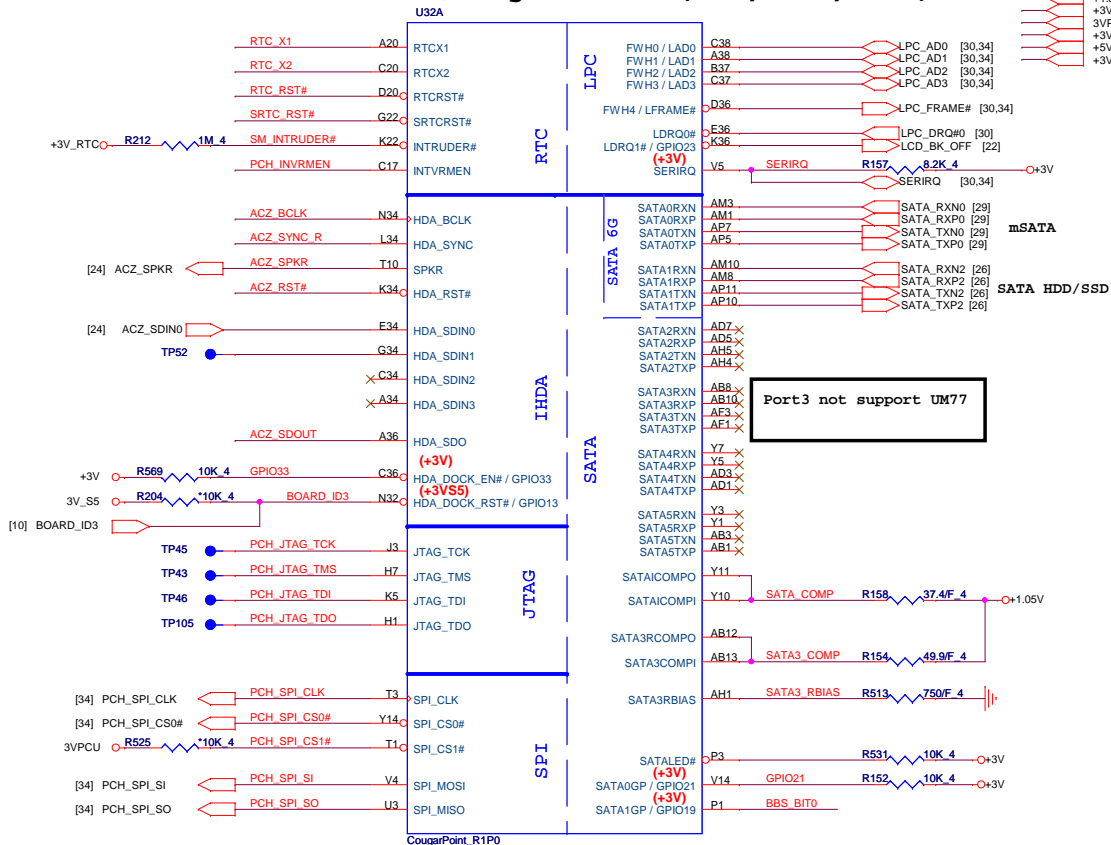
LVDS for HM76



DPWROK FOR DSW (DEEP S3)

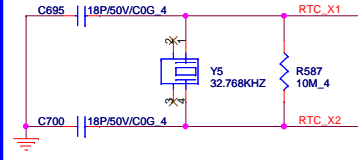


Panther/Cougar Point (HDA, JTAG, SATA)

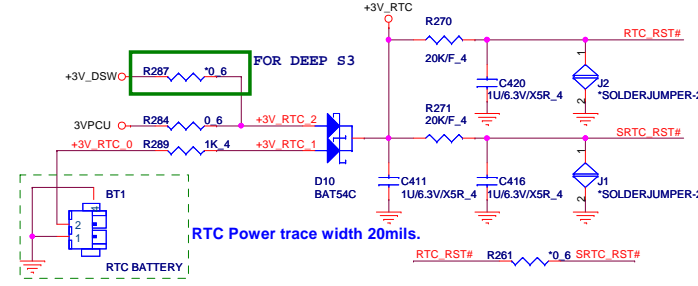


RTC Clock 32.768KHZ

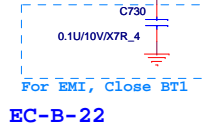
08



RTC Circuitry(RTC)



Port3 not support UM77

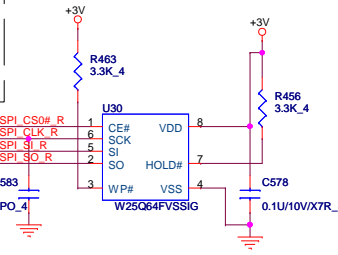
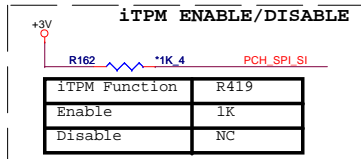


EC-B-25

W25Q64CVSSIG: AKE3EFP0N04
 MX25L6406EM2I-12G: AKE3NFP0Z00
 EN25Q64-104HIP: AKE3EFPN0Q00

PCH Dual SPL

64Mbit (8M Byte), SPI

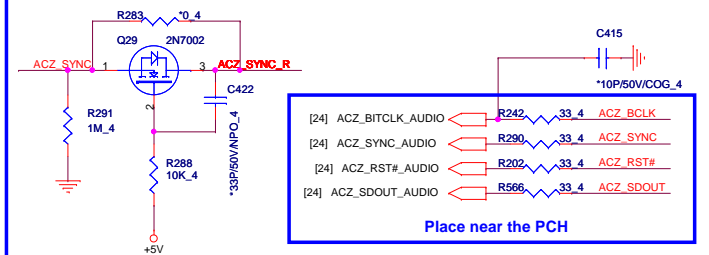


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	Different from Calpella	No reboot mode setting	PWROK 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R180 *1K_4 +3V									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R578 *1K_4 R561 *10K_4 +3V									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R564 330K_4 +3V_RTC									
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDO R567 *1K_4 3V_S5									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>0</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>1</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	R530 *1K_4 R592 *1K_4 BBS_BIT0 BBS_BIT1 [9]
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19	Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK										
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
DF_TV5	DMI Termination voltage	PWROK	weak pull-down 20kohm	[3] PROC_SELECT# R500 2.2K_4 +1.8V R501 1K_4 DF_TV5 [10]									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R203 1K_4 ACZ_SYNC_R									
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable	[10] HOST_ALERT#1_R HOST_ALERT#1 R R554 1K_4 +3V_S5									
GPIO28	Different from Calpella	On-die PLL Voltage Regulator	0 = Disable 1 = Enable (Default)	R195 *1K_4 PLL_ODVR_EN [10]									
DSWVREN		0: disable 1: enable											

if default boot destination is SPI,
no external pull-up/-down resistors on the board are necessary

HDA Bus(CLG)

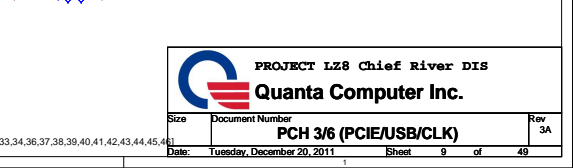
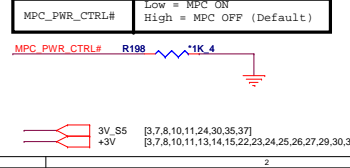
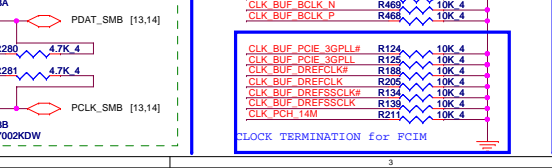
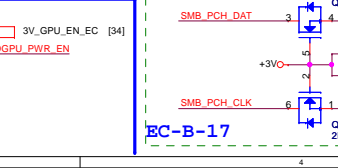
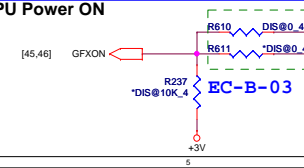
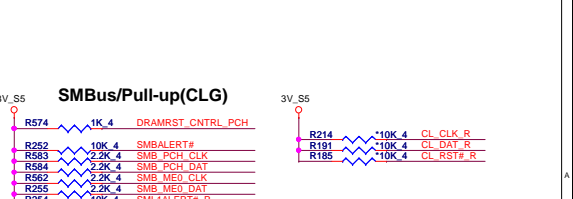
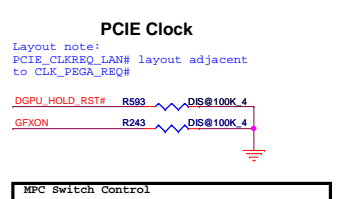
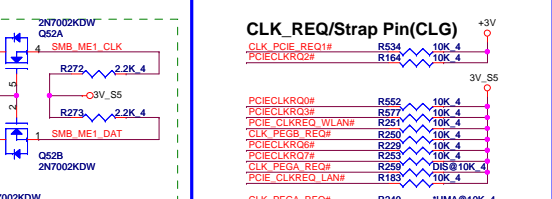
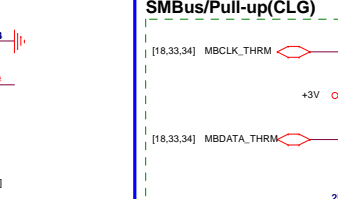
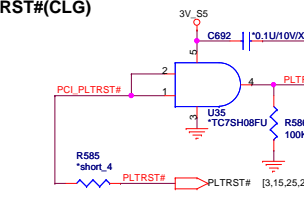
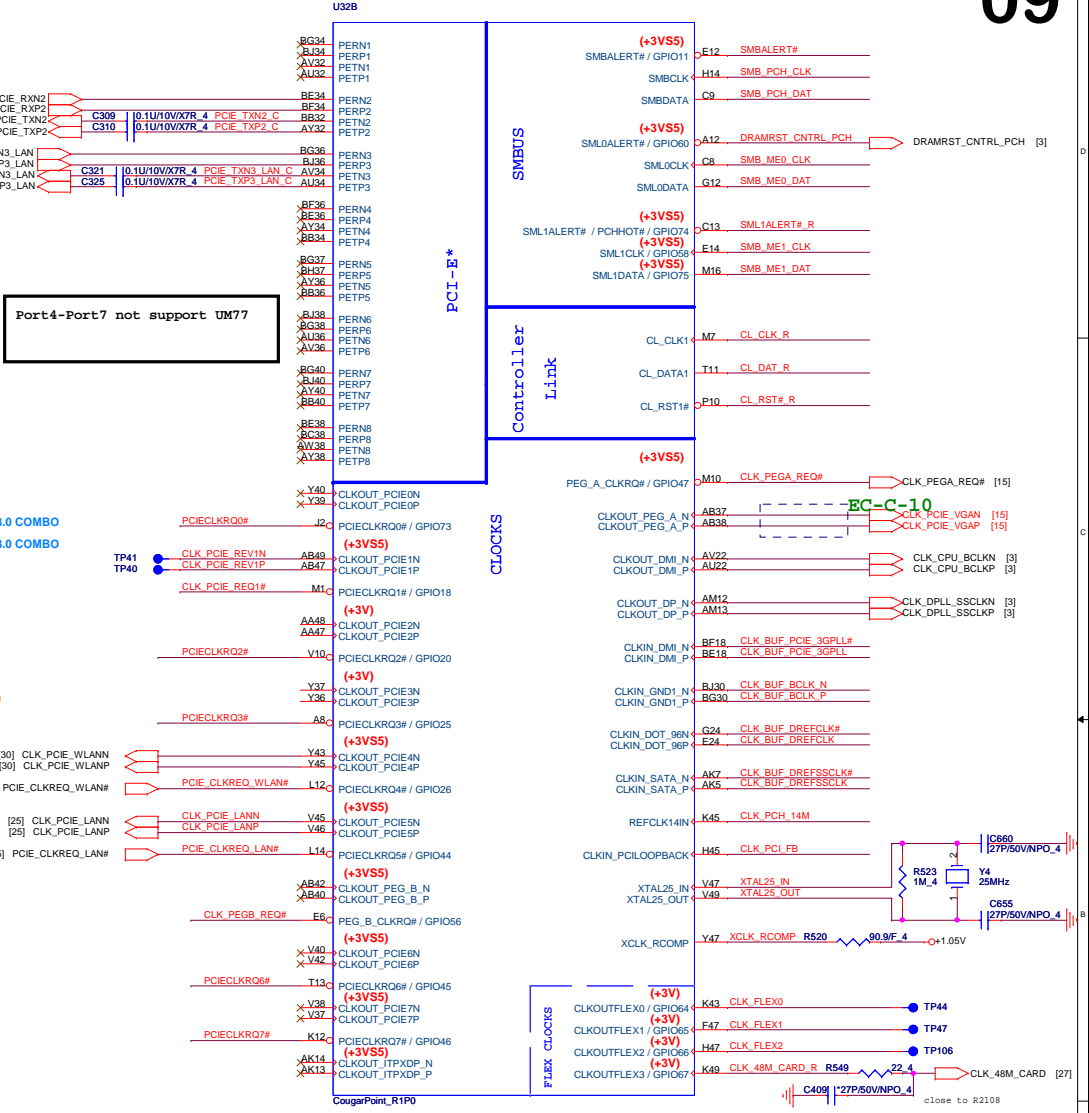
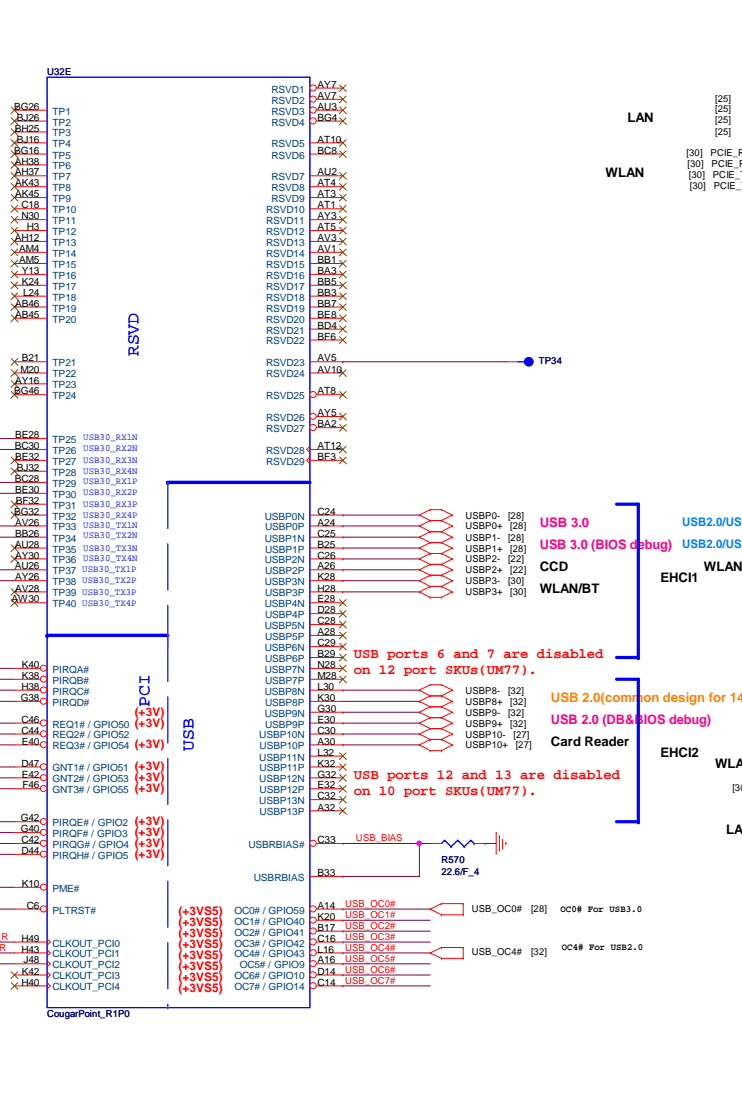
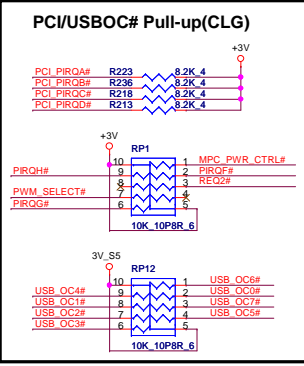


PROJECT L28 Chief River DIS

Quanta Computer Inc.

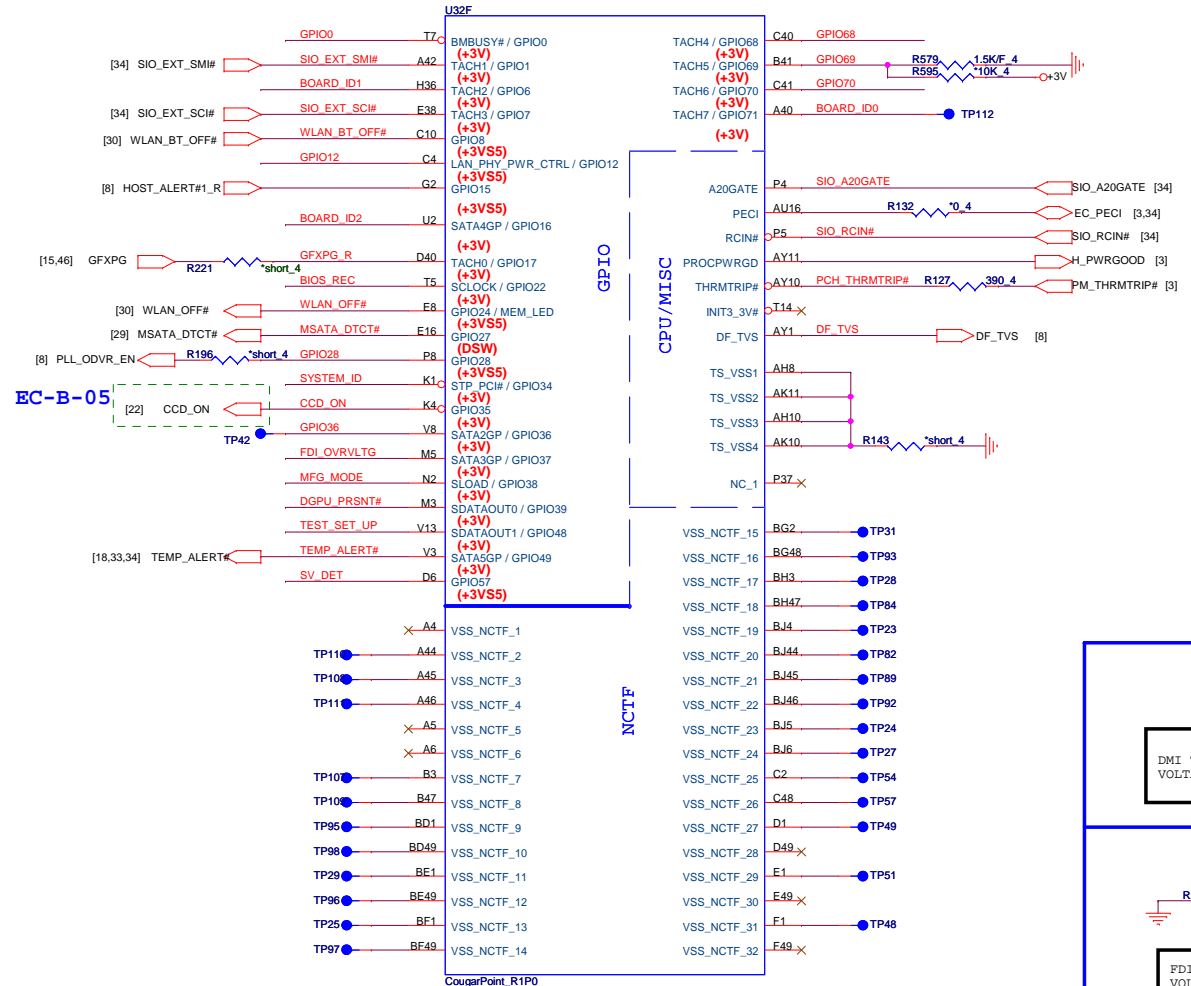
Size: Document Number: **PCH 2/6 (SATA/HDA/SPI)** Rev 1A

Date: Tuesday, December 20, 2011 Sheet 8 of 49

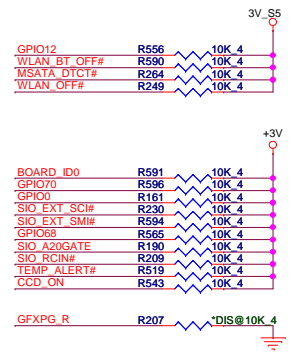


Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)

3V_S5 [3,7,8,9,11,24,30,35,37]
+3V [3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]



GPIO Pull-up/Pull-down(CLG)

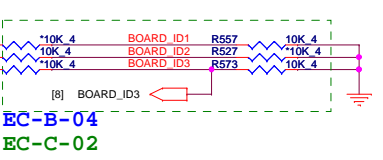
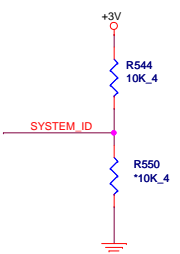


3V_S5 [3,7,8,9,11,24,30,35,37]
+3V [3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

	SYSTEM_ID
L27	0
L28	1



DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SV_SET_UP

High = Strong (Default)

FDI TERMINATION VOLTAGE OVERRIDE

LOW = Tx, Rx terminated to same voltage

TEST SET_UP

High = Strong (Default)

MFG-TEST

MFG MODE

	Optimus	UMA
Stuff	R547	R546
No Stuff	R546	R547

BIOS RECOVERY

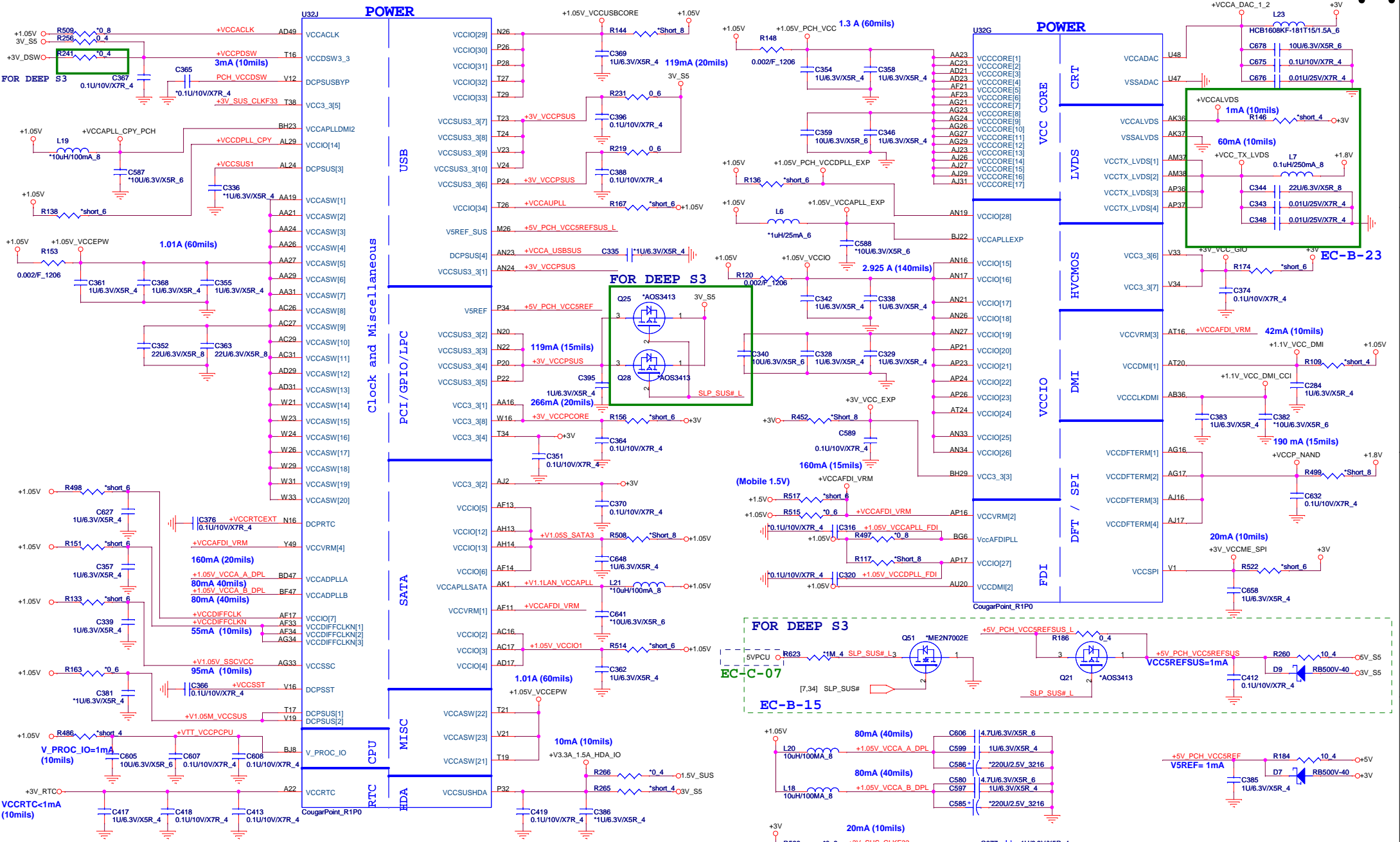
High = Disable (Default)
Low = Enable

BIOS REC

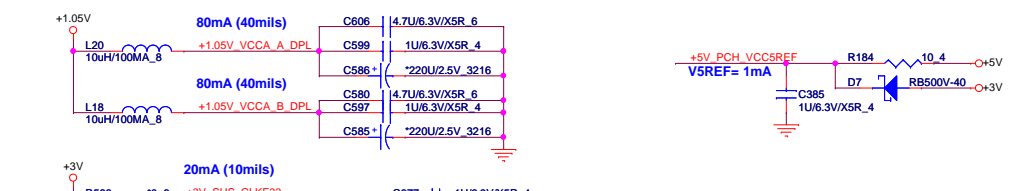
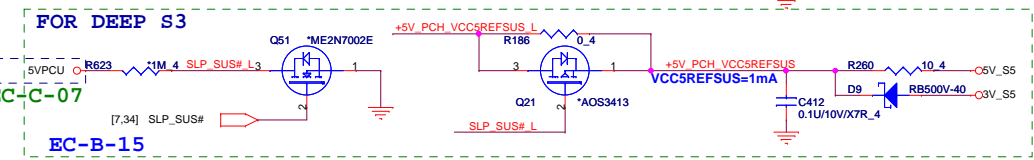
High = Disable (Default)
Low = Enable

Panther/Cougar Point-M (POWER)

Panther/COUGAR POINT (POWER)



5VPCU	[22,36,37,39,40,41,42,43,44,45,46]
+3V_RTC	[7,8,34]
3V_S5	[3,7,8,9,10,24,30,35,37]
+3V	[3,7,8,9,10,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
5V_S5	[28,32,37]
+5V	[8,23,24,26,33,36,37,38]
+1.05V	[3,5,7,8,9,37,41,46]
1.5V_SUS	[3,13,14,36,37,40,46]
+1.8V	[5,8,37,43]
+3V_DSW	[7,8]



PROJECT L28 Chief River DIS

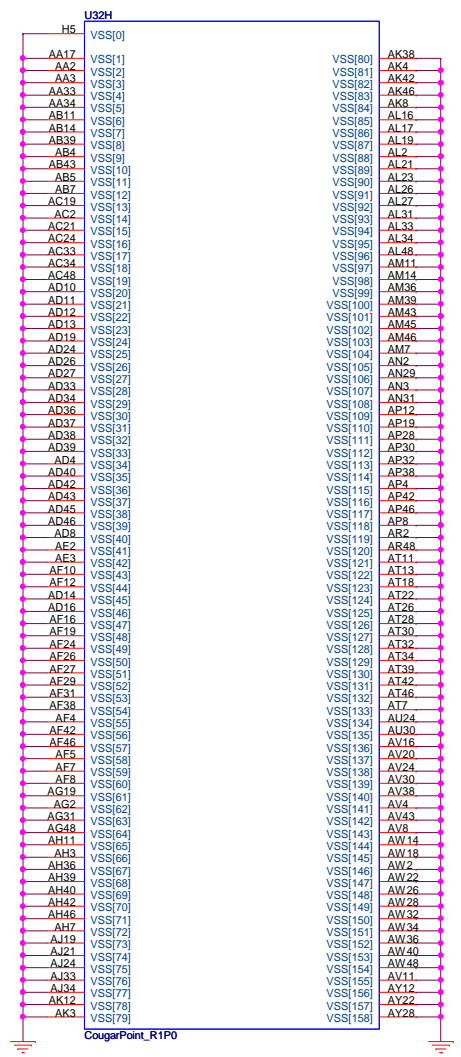
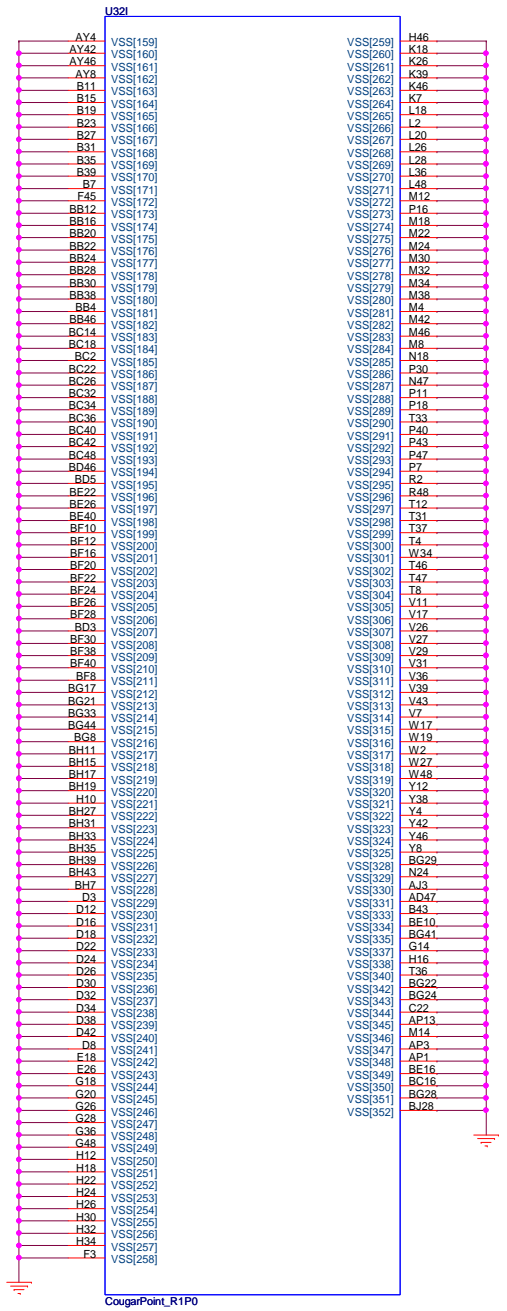
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 5/6 (POWER)	3A

Date: Tuesday, December 20, 2011 Sheet 11 of 49

Panther/Cougar Point-M (GND)

Panther/Cougar Point-M (GND)



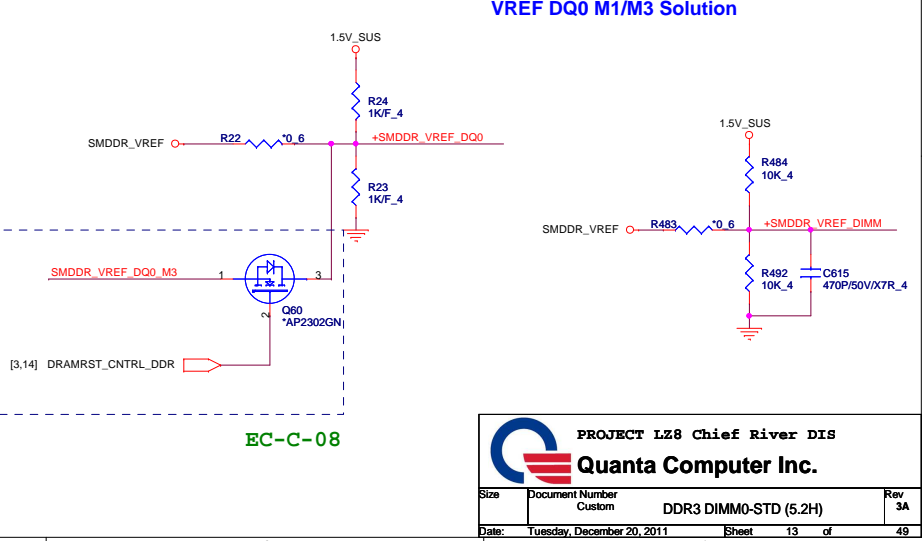
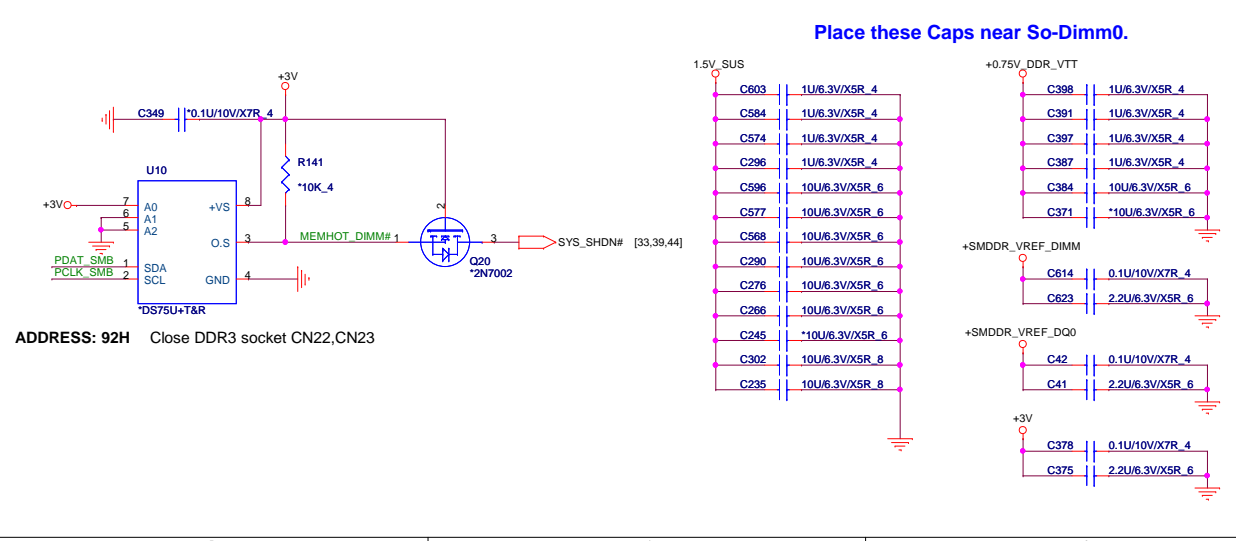
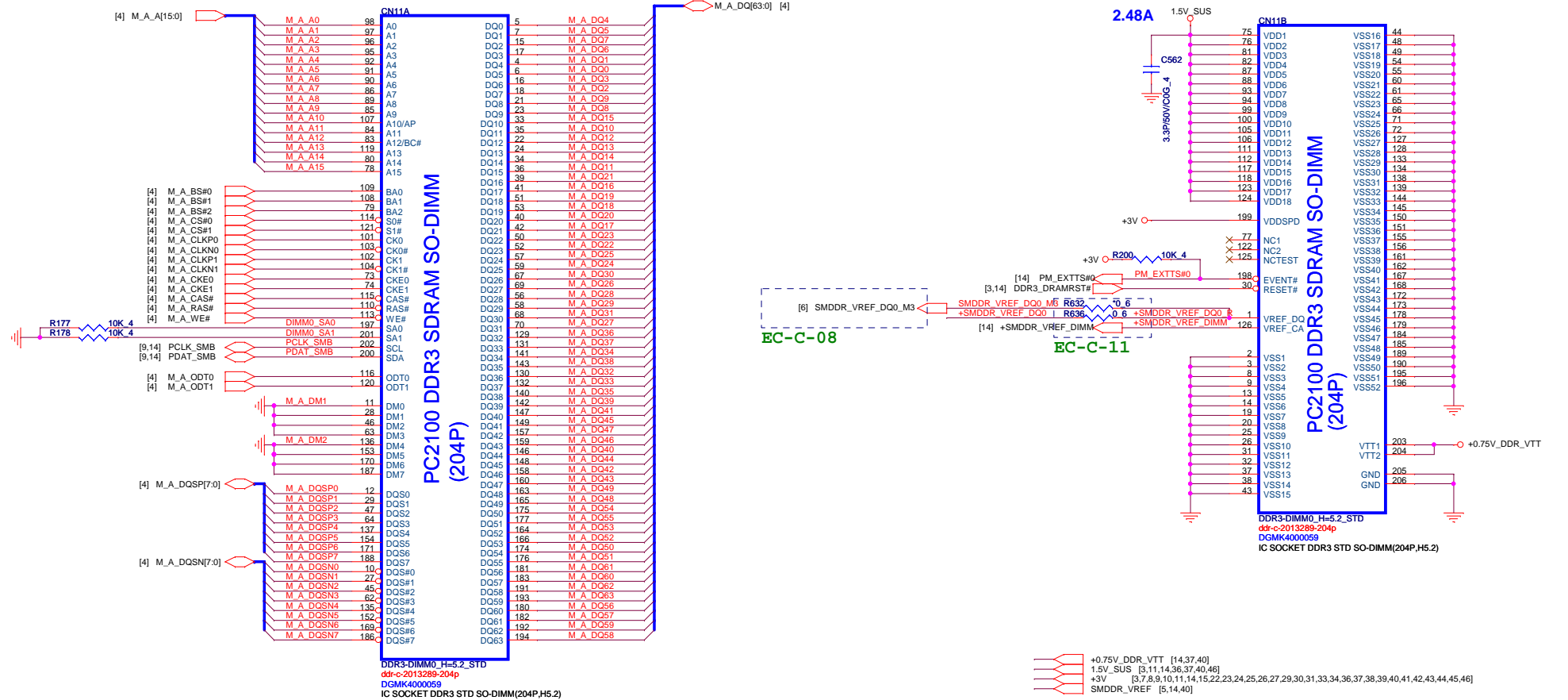
PROJECT LZ8 Chief River DIS

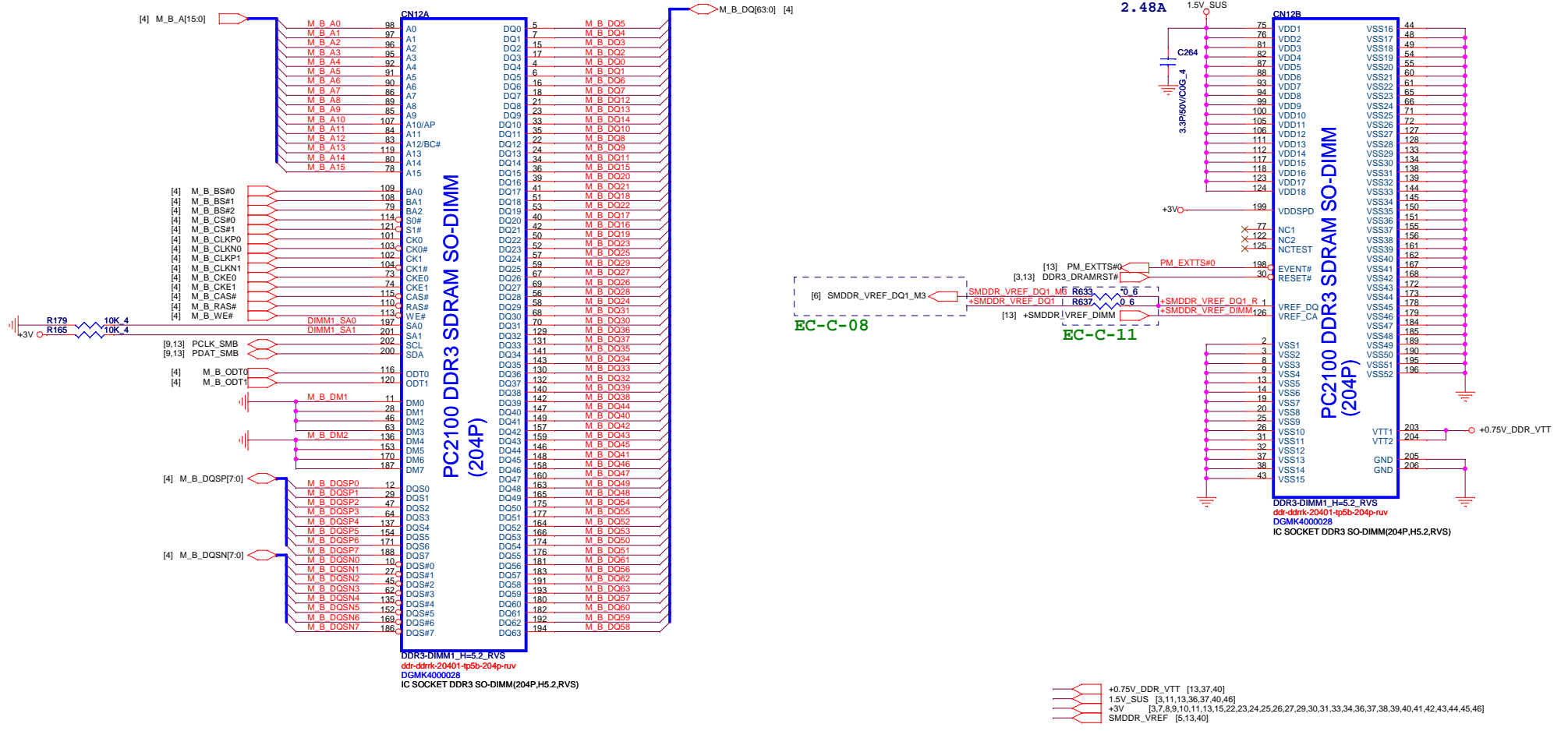
Quanta Computer Inc.

Size: Document Number: Rev 1A

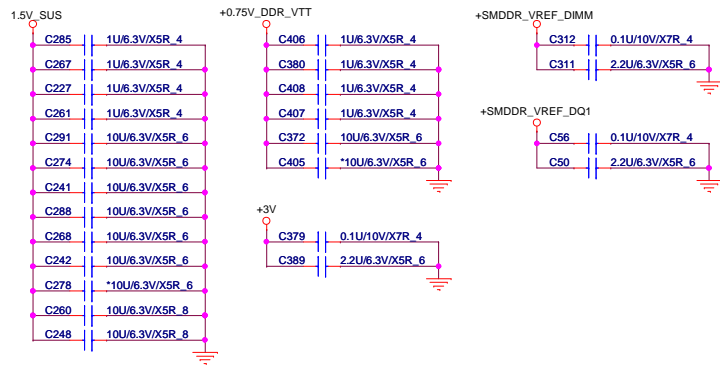
PCH 6/6 (GND)

Date: Friday, November 11, 2011 Sheet 12 of 49

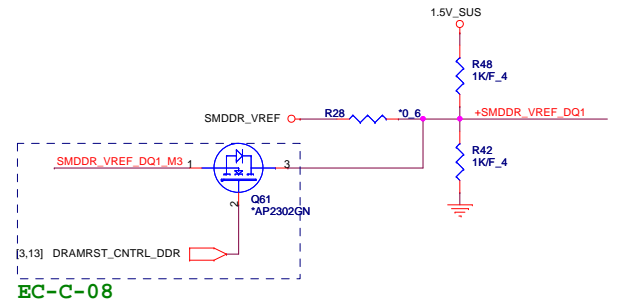




Place these Caps near So-Dimm1.



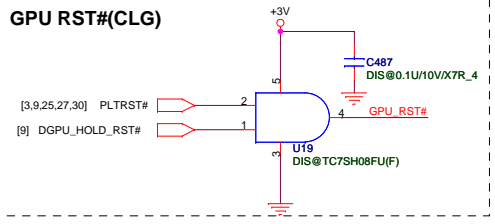
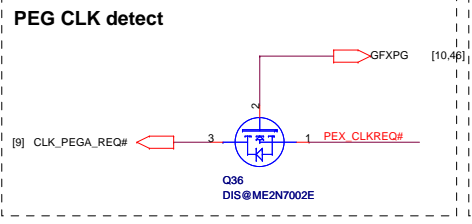
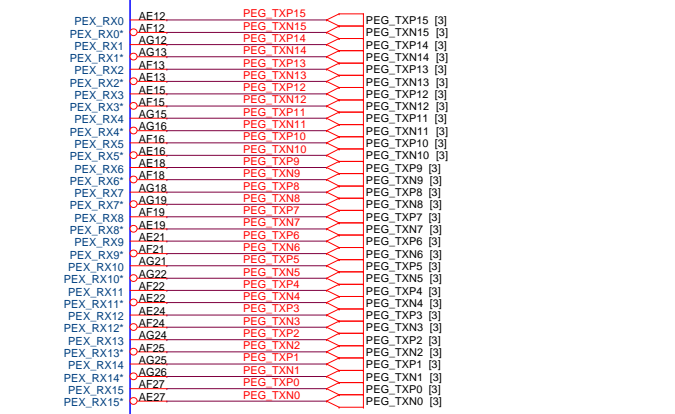
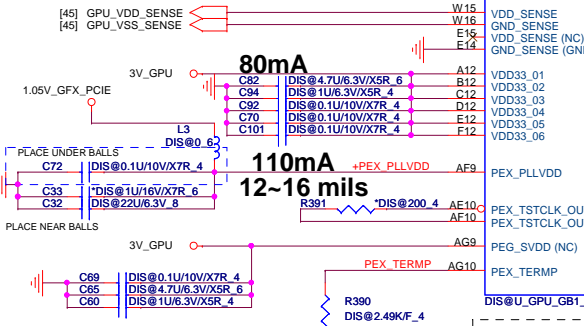
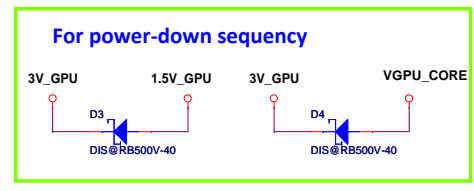
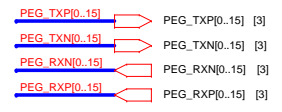
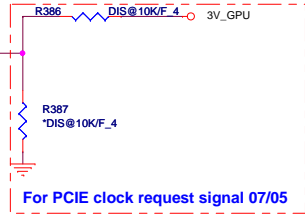
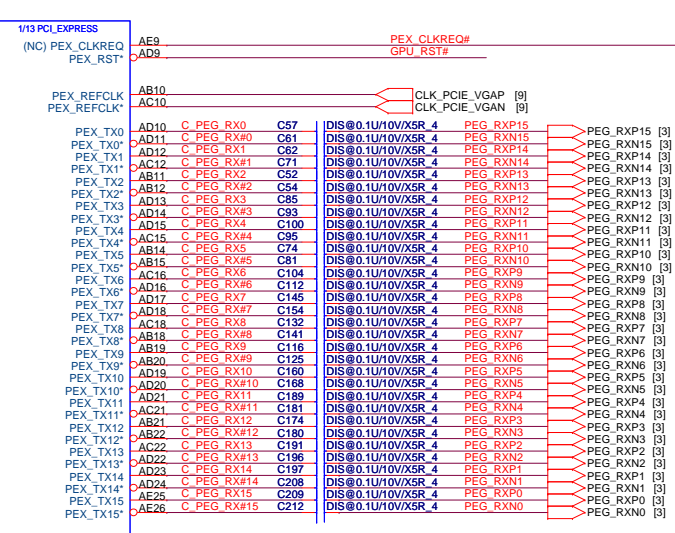
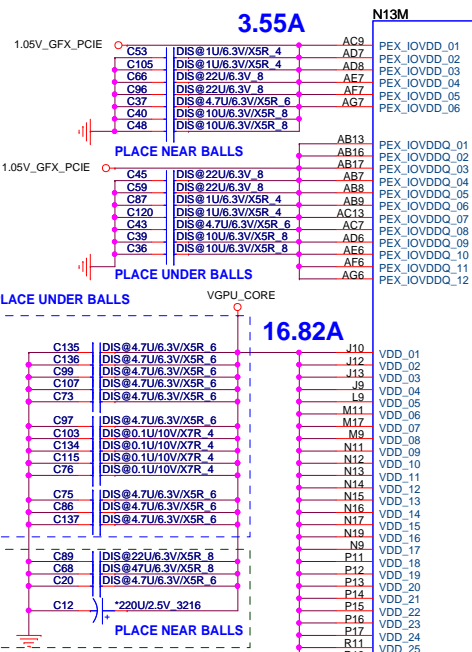
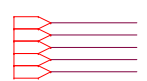
VREF DQ1 M1/M3 Solution



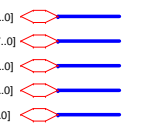
U23A

[3,7,8,9,10,11,13,14,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

[16,17,46] 1.05V_GFX_PCIE
[17,18,46] 3V_GPU
[16,19,46] 1.5V_GPU
+3V
[45] VGPU_CORE



[15,17,46] 1.05V_GFX_PCIE
[15,19,20,46] 1.5V_GPU

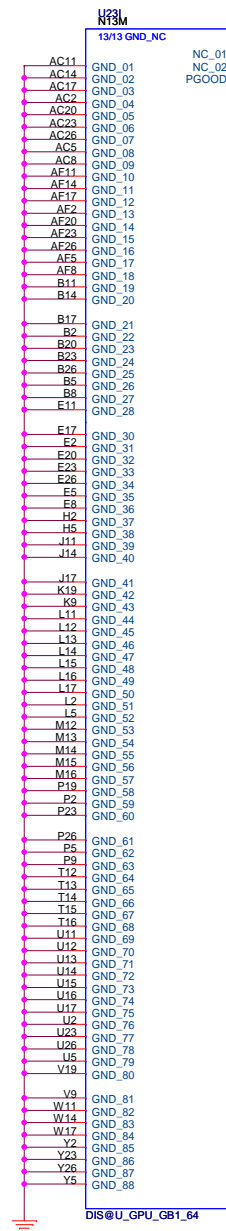
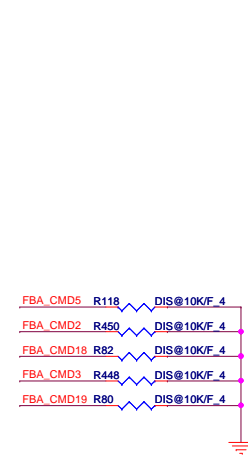
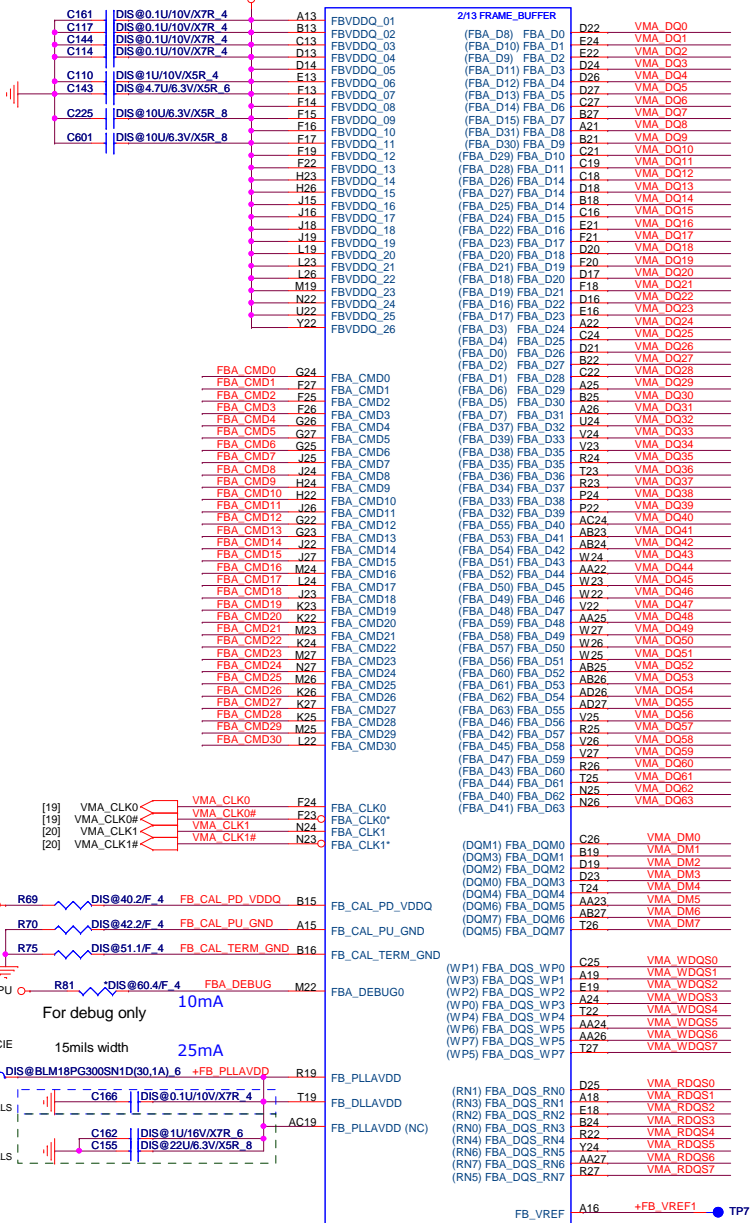


2.63A

1.5V_GPU

U23B
N13M

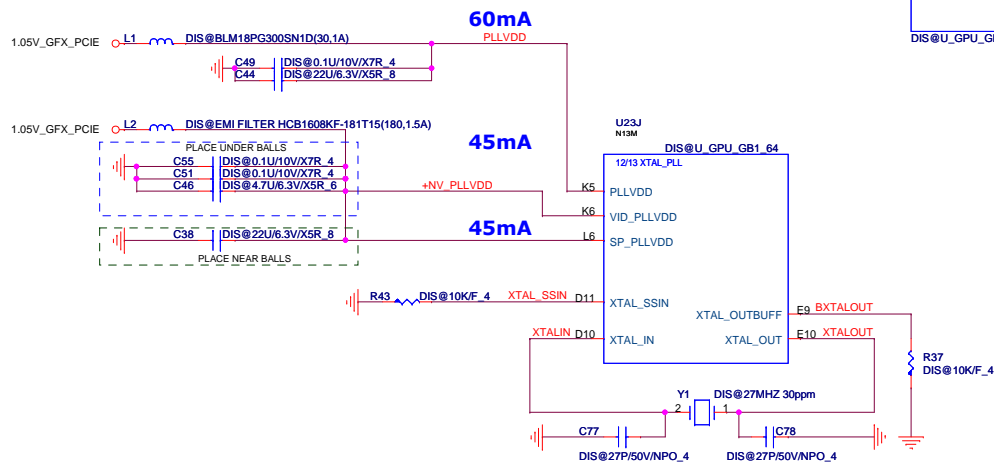
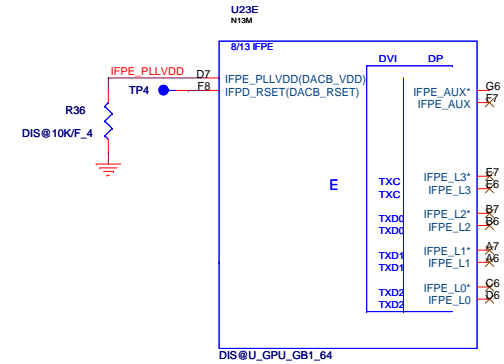
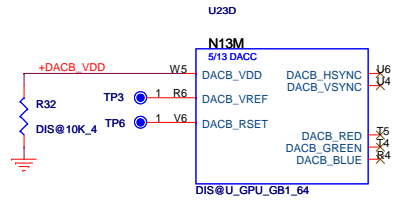
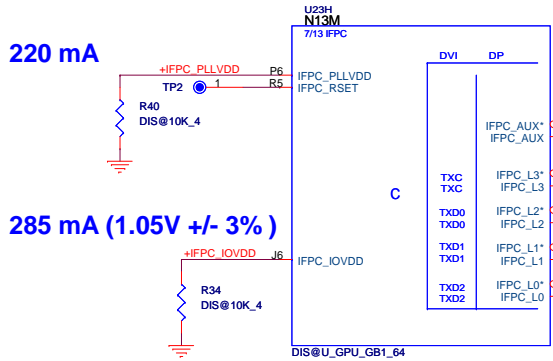
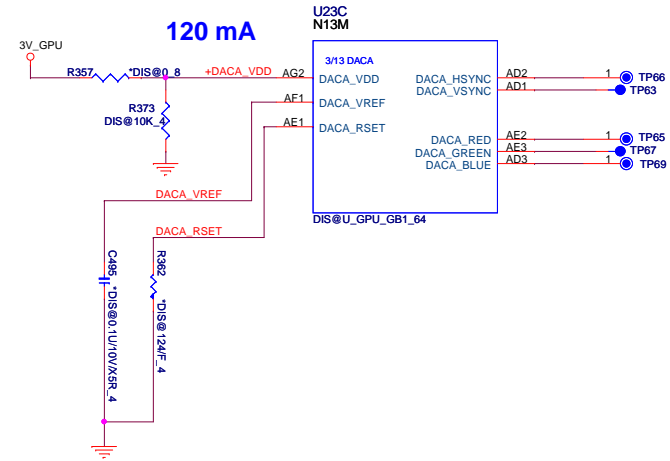
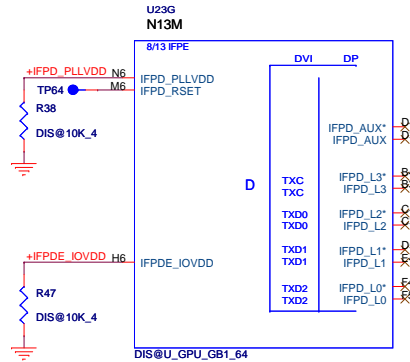
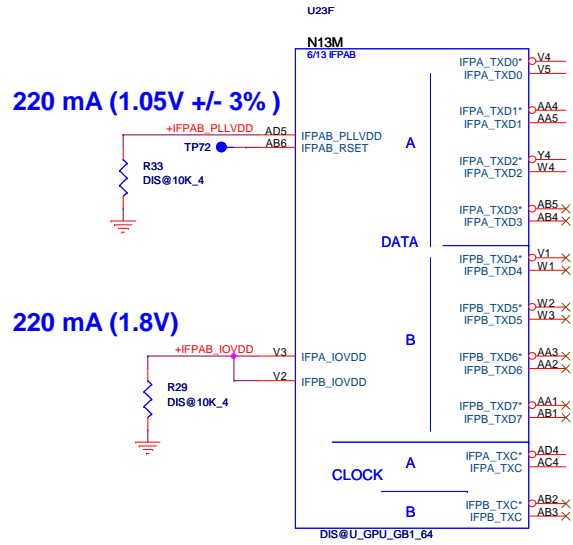
2/13 FRAME_BUFFER



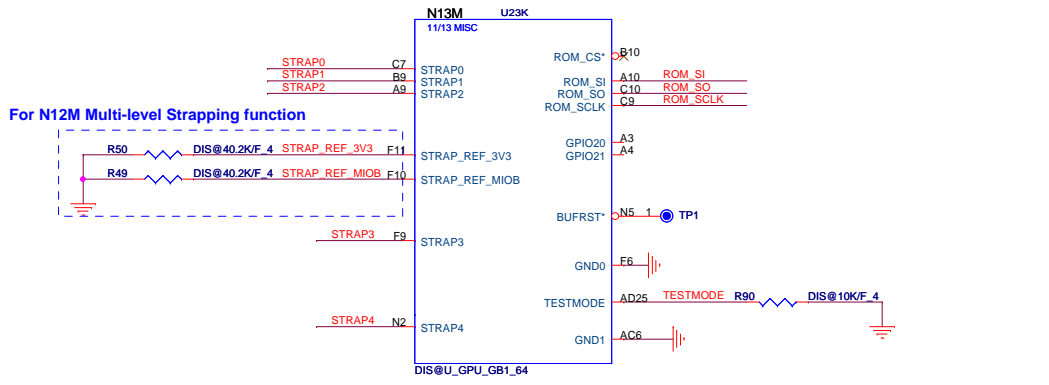
DIS@U_GPU_GB1_64

DIS@U_GPU_GB1_64

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.
Size: Custom Document Number: N13M(MEMORY I/F & GND) 2/5 Rev 1A
Date: Tuesday, December 20, 2011 Sheet 16 of 49

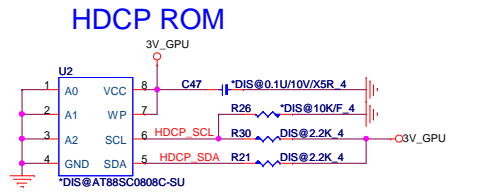
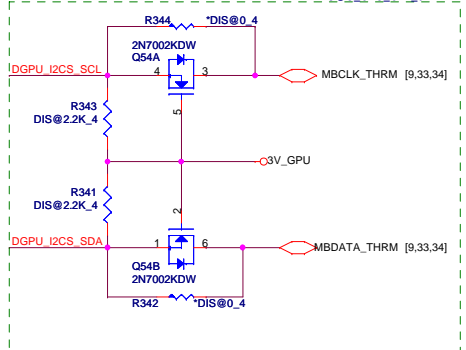
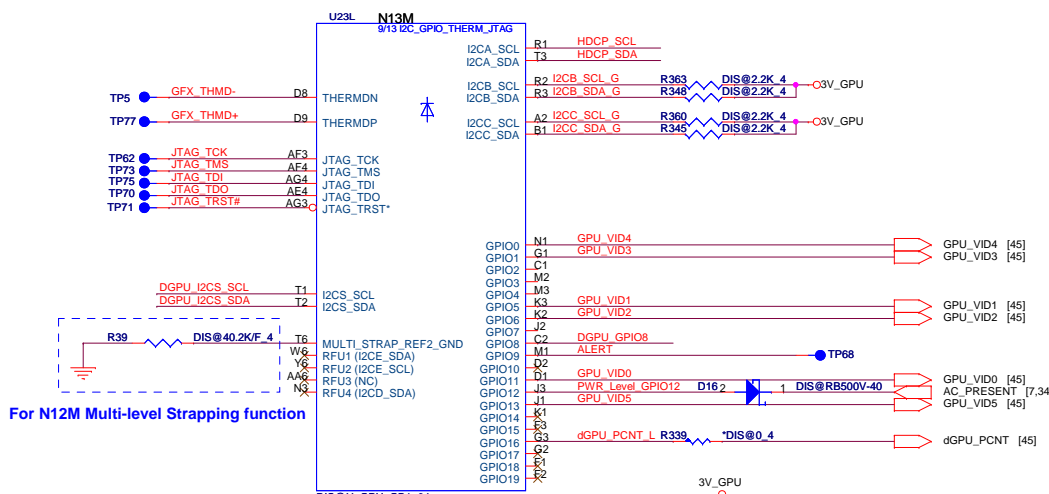


STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS Install it when not connected to Spread spectrum device



9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors, routing.



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

nV FAE suggest that the device ID for N13M-GE1 is 0x1058

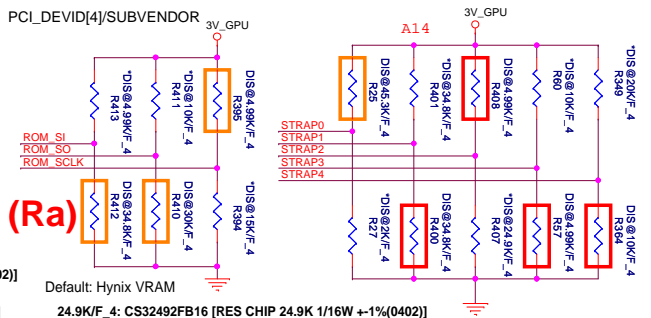
[15,17,46] 3V_GPU

Logical Strap Bit Mapping

Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

N13M-GE1

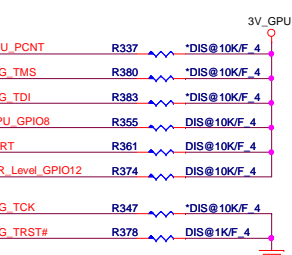
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
 10K/F 4: CS31002FB24 [RES CHIP 10K 1/16W +1% (0402)]
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
 30K/F 4: CS33002FB13 [RES CHIP 30K 1/16W +1% (0402)]
 34.8K/F 4: CS33482FB22 [RES CHIP 34.8K 1/16W +1% (0402)]
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N13M-GE1	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001

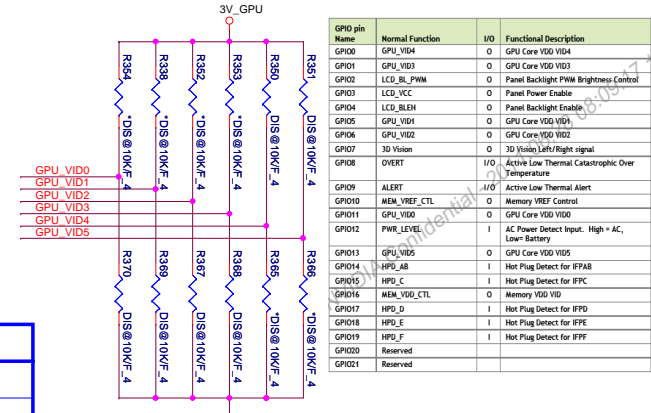
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001		Reserved		
0010		Reserved		
0011		Reserved		
0101		Reserved		
0110		Reserved		
0111	DDR3 128Mx16x4, 64bit, 1GB,900MHz DDR3 128Mx16x4, 64bit, 1GB,900MHz	Hynix Samsung	H5TQ2G63BFR-11C K4W2G1646C-HC11	PD 34.8K/F PD 45.3K/F



NVDD Table

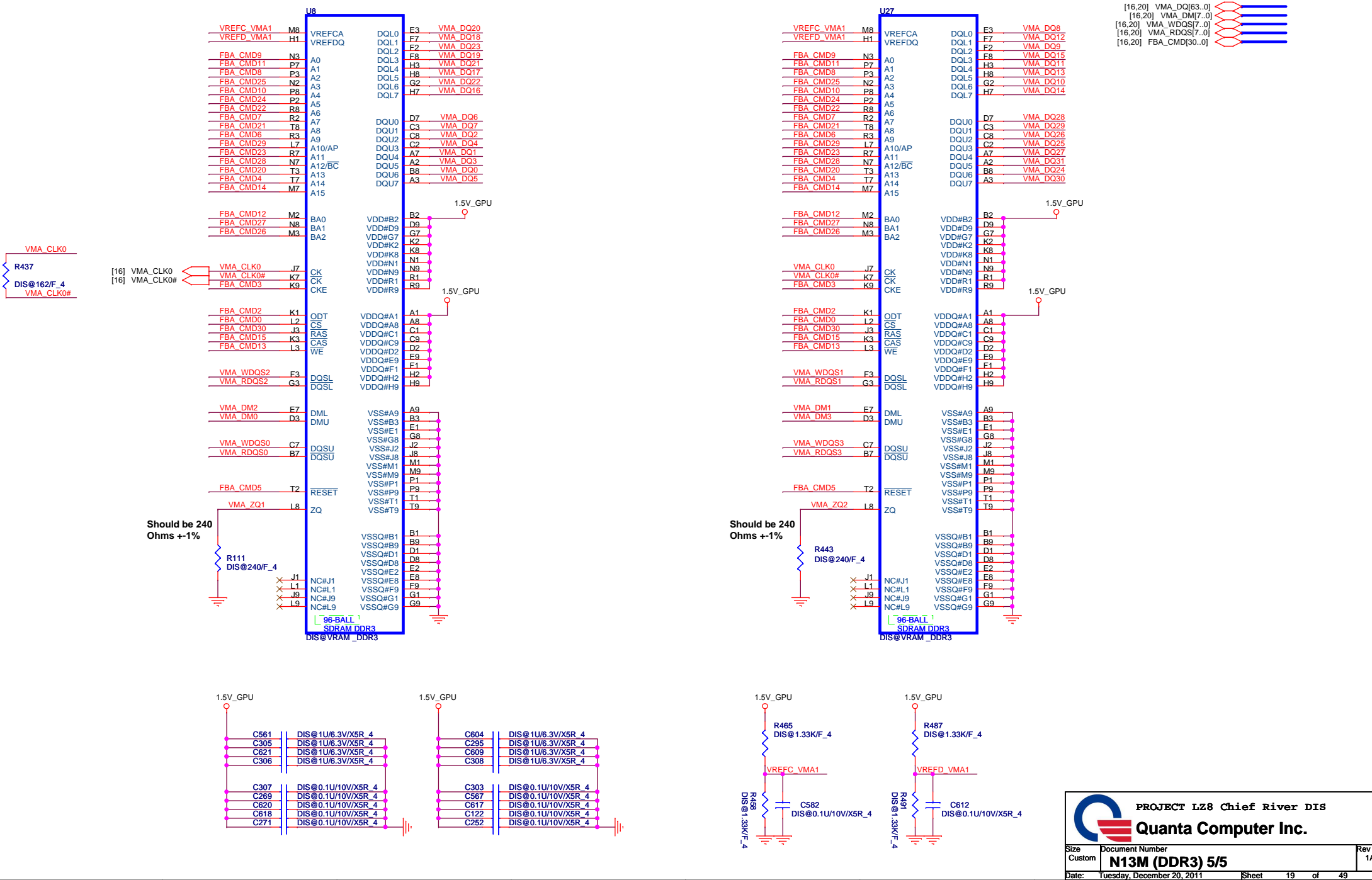
N13M-GE1 (GF119)	NVDD (0.875V)
GPU_VID0	0 (R370)
GPU_VID1	0 (R369)
GPU_VID2	0 (R367)
GPU_VID3	0 (R368)
GPU_VID4	1 (R350)
GPU_VID5	1 (R351)



GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	0	GPU Core VDD VID4
GPIO1	GPU_VID3	0	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	0	Panel Power Enable
GPIO4	LCD_BL_EN	0	Panel Backlight Enable
GPIO5	GPU_VID1	0	GPU Core VDD VID1
GPIO6	GPU_VID2	0	GPU Core VDD VID2
GPIO7	3D Vision	0	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	0	Memory VREF Control
GPIO11	GPU_VID0	0	GPU Core VDD VID0
GPIO12	PWR_LEVEL	1	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	0	GPU Core VDD VID5
GPIO14	HPU_AB	1	Hot Plug Detect for HPA
GPIO15	HPU_C	1	Hot Plug Detect for HPC
GPIO16	MEM_VDD_CTL	0	Memory VDD VID
GPIO17	HPU_D	1	Hot Plug Detect for HPD
GPIO18	HPU_E	1	Hot Plug Detect for HPE
GPIO19	HPU_F	1	Hot Plug Detect for HFF
GPIO20	Reserved		
GPIO21	Reserved		

CHANNEL A: 1024MB DDR3

[15,16,20,46] 1.5V_GPU



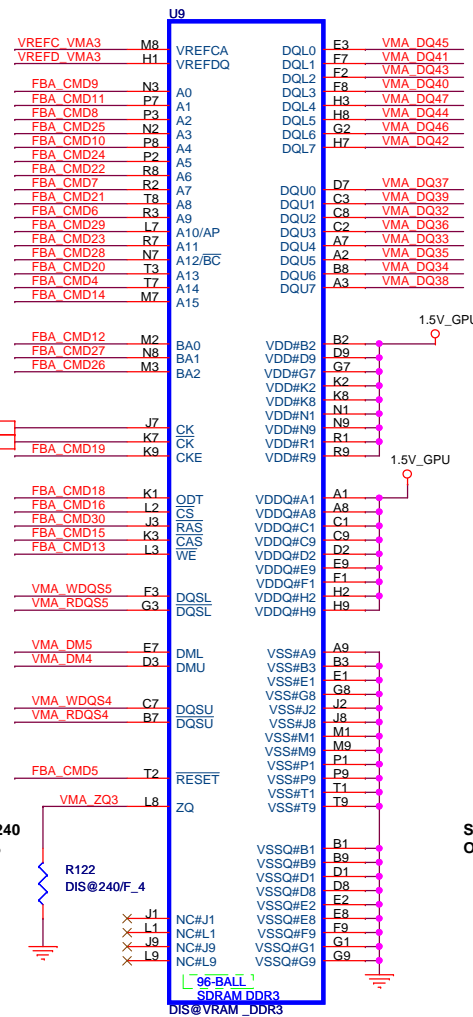
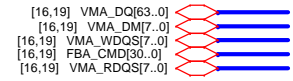
PROJECT Lz8 Chief River DIS
Quanta Computer Inc.

Size Custom Document Number **N13M (DDR3) 5/5** Rev 1A

Date: Tuesday, December 20, 2011 Sheet 19 of 49

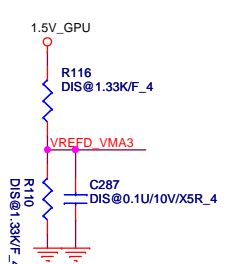
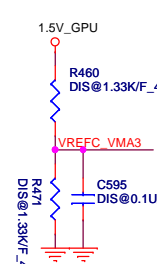
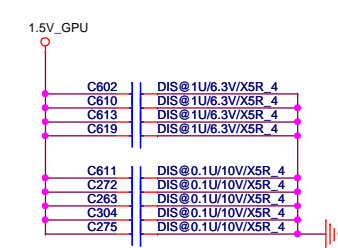
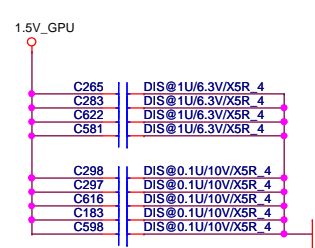
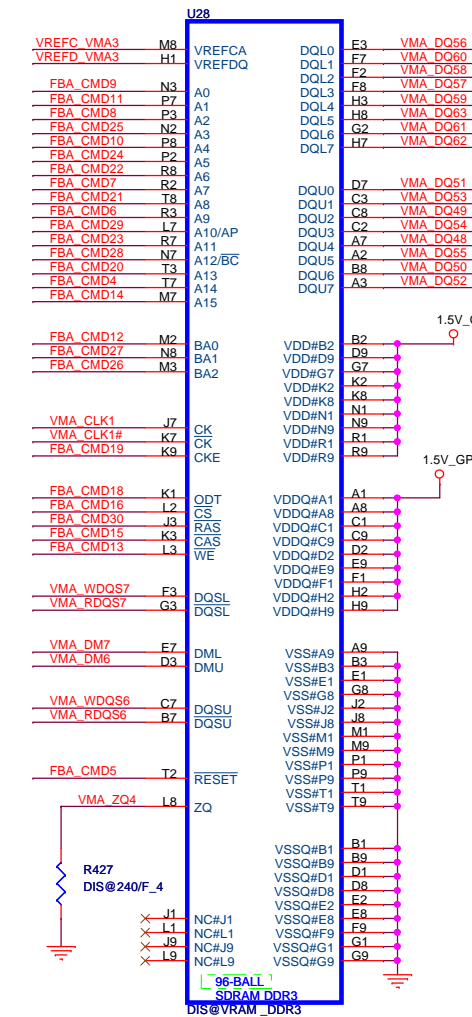
CHANNEL A: 1024MB DDR3

[15,16,19,46] 1.5V_GPU



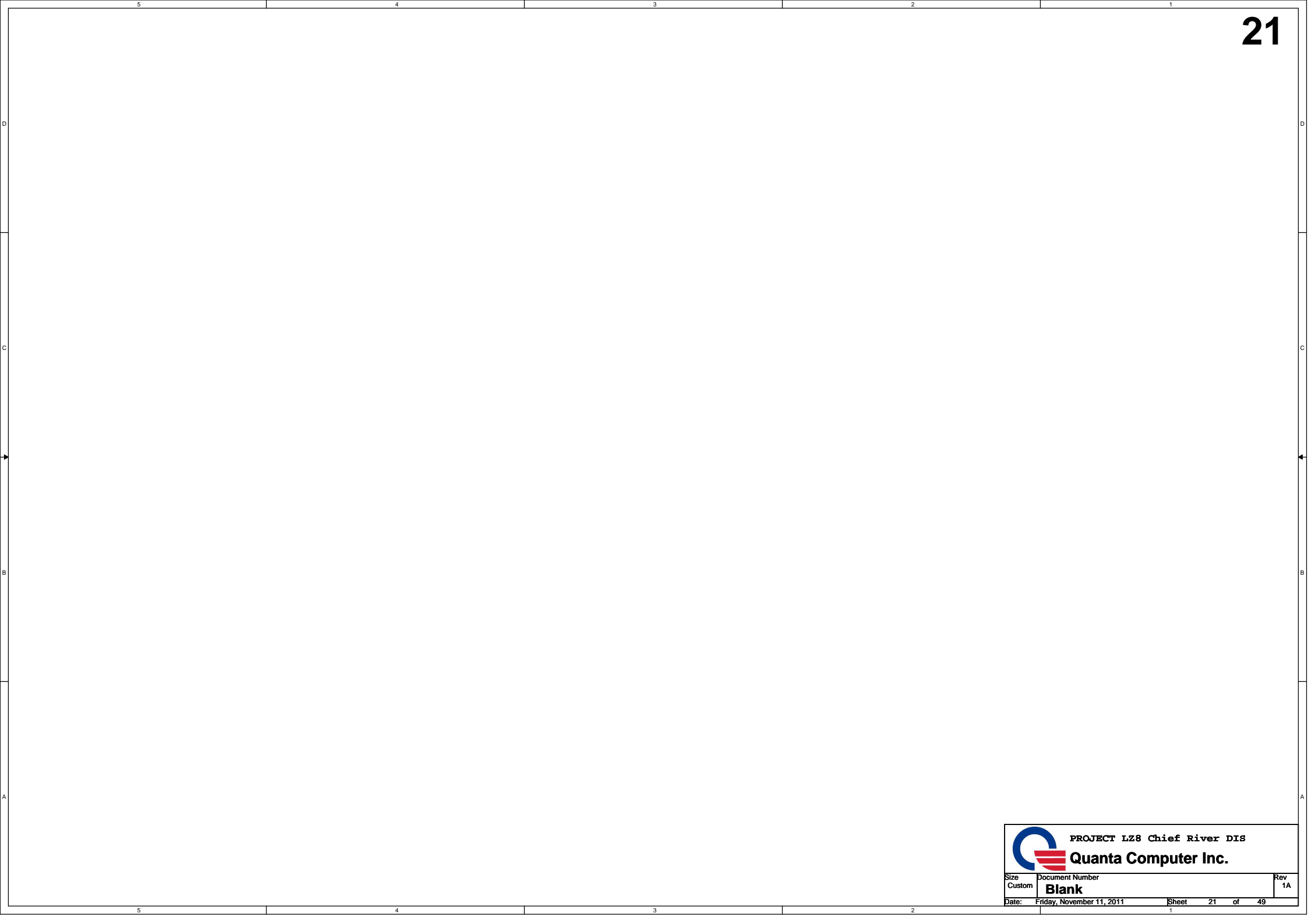
Should be 240 Ohms +/-1%


Should be 240 Ohms +/-1%



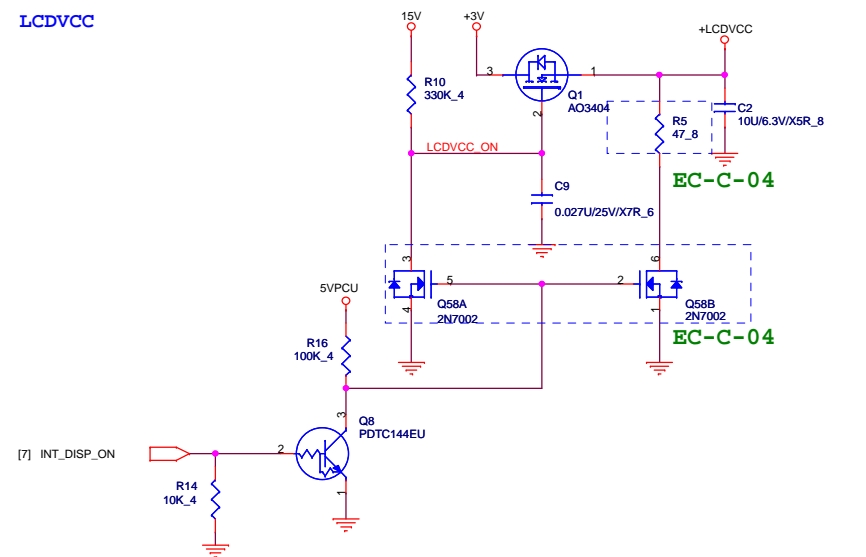
PROJECT Lz8 Chief River DIS
Quanta Computer Inc.

Size Custom Document Number **N13M (DDR3) 6/6** Rev 1A
 Date: Tuesday, December 20, 2011 Sheet 20 of 49

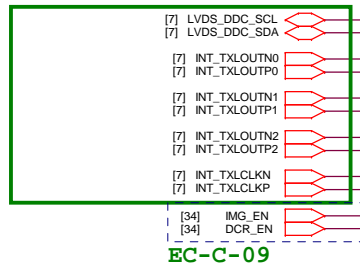


	PROJECT LZ8 Chief River DIS		
	Quanta Computer Inc.		
Size Custom	Document Number Blank	Date: Friday, November 11, 2011	Rev 1A
		Sheet 21 of 49	1

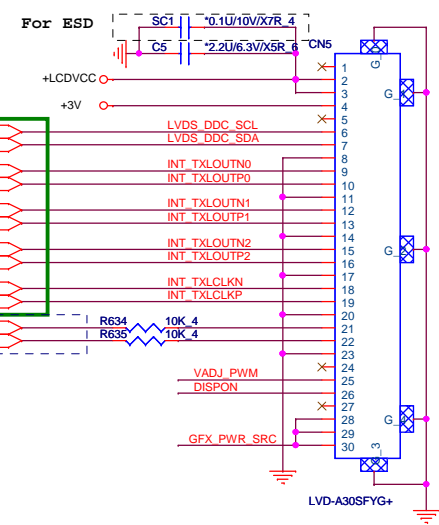
+3V	[3,7,8,9,10,11,13,14,15,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
3VPCU	[7,8,25,30,31,34,35,36,37,38,39,43,45]
15V	[37,39,40,46]
VIN	[36,38,39,40,41,42,44,45]
5VPCU	[11,36,37,39,40,41,42,43,44,45,46]



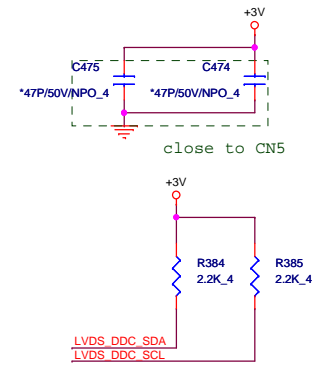
EC-B-22



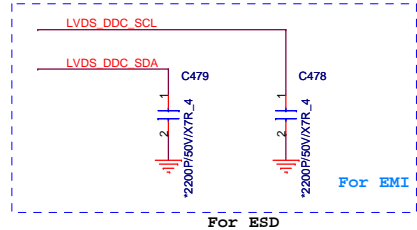
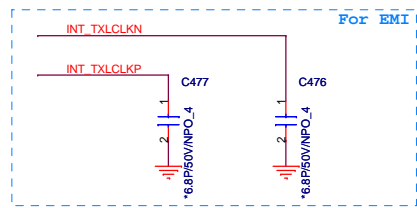
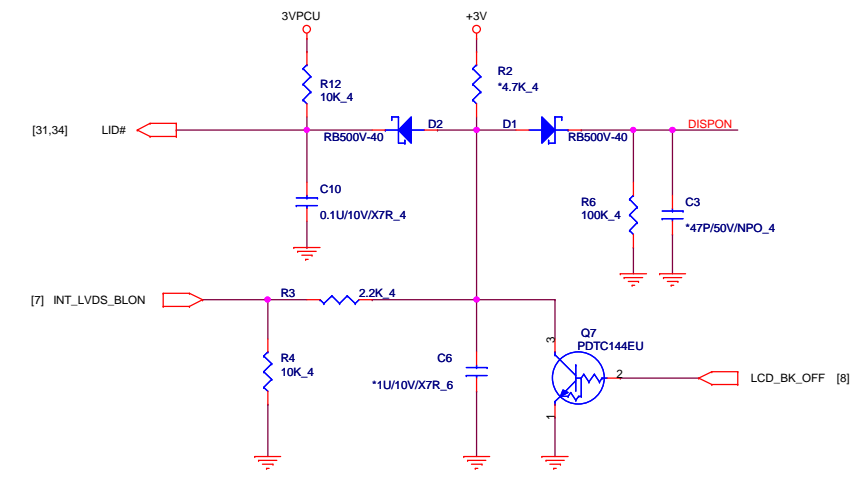
EC-C-09



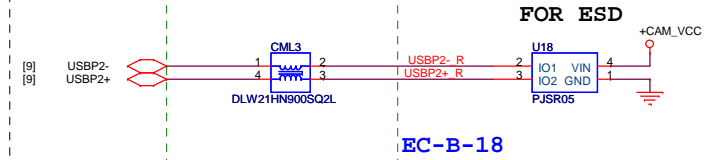
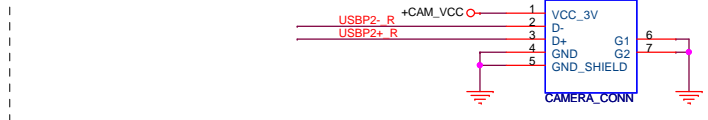
LVDS (14")
(1024x600,
1366x768)



Back light

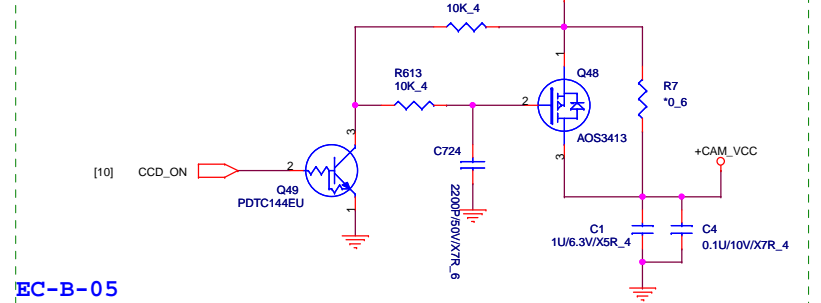


CAMERA CONN

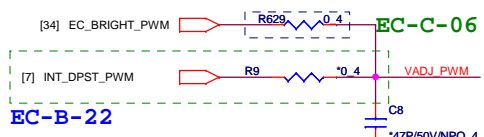
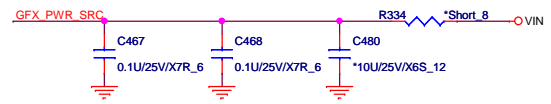


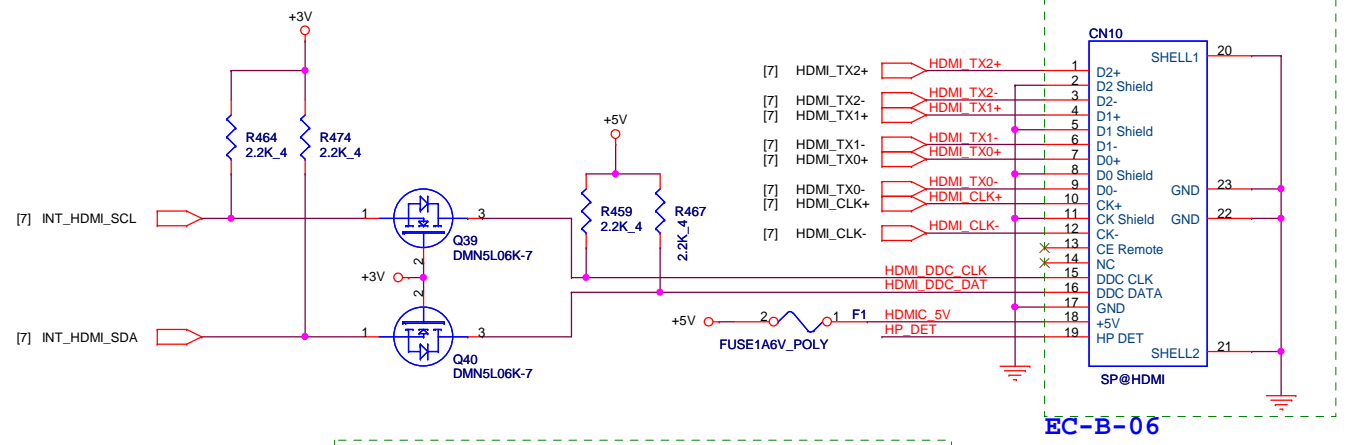
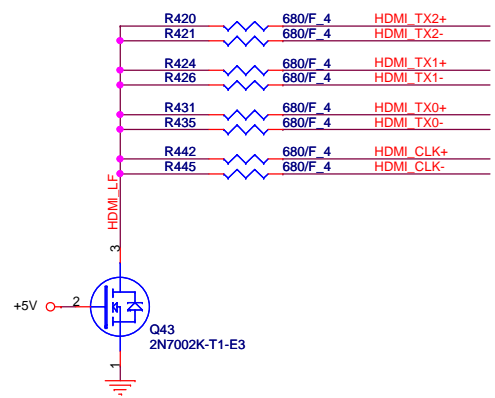
EC-B-18

CAMERA VCC Control

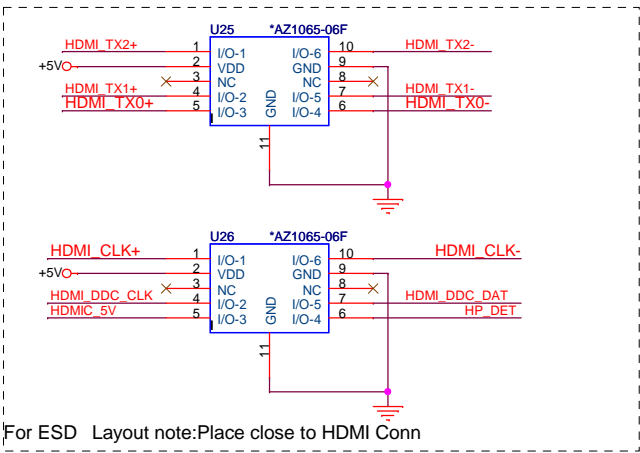


EC-B-05



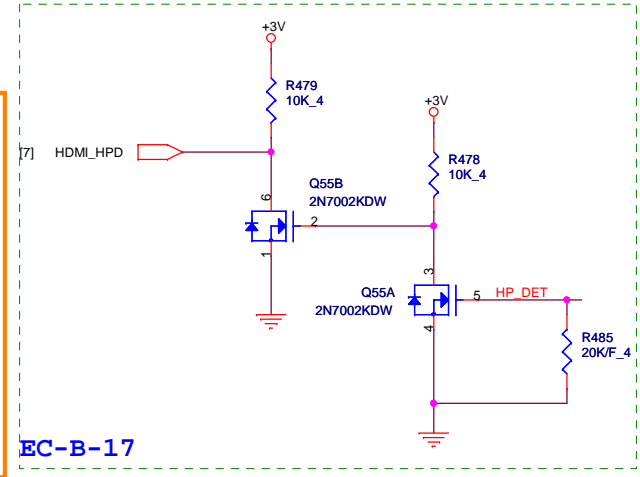
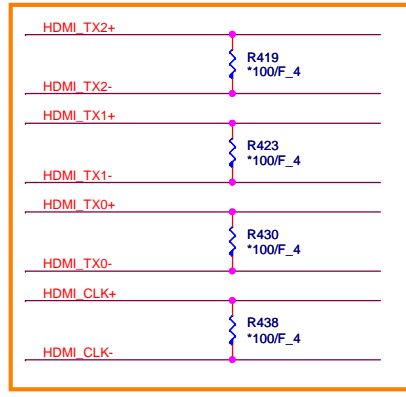


EC-B-06

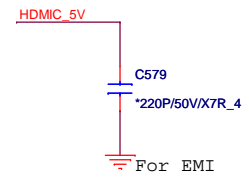


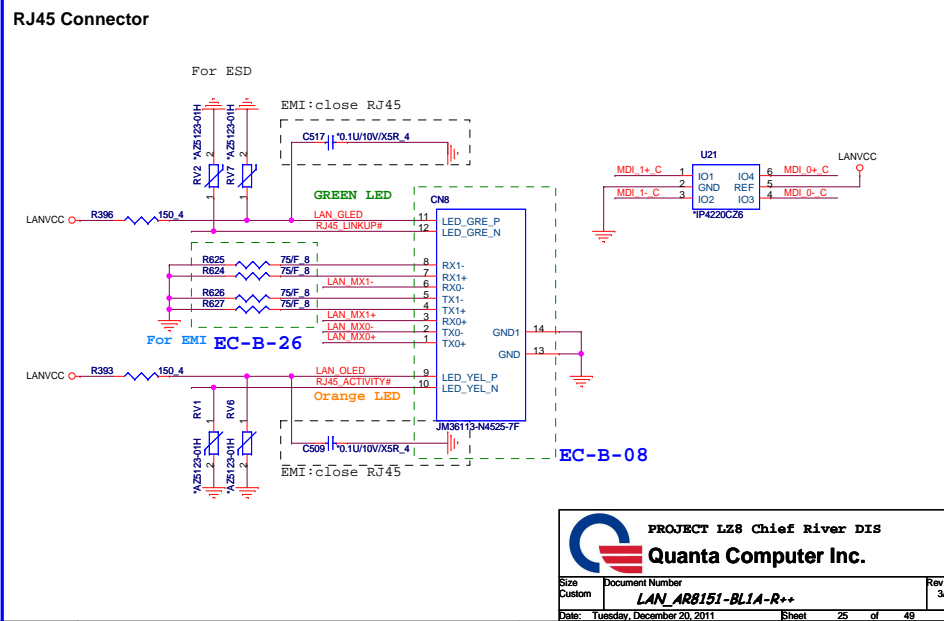
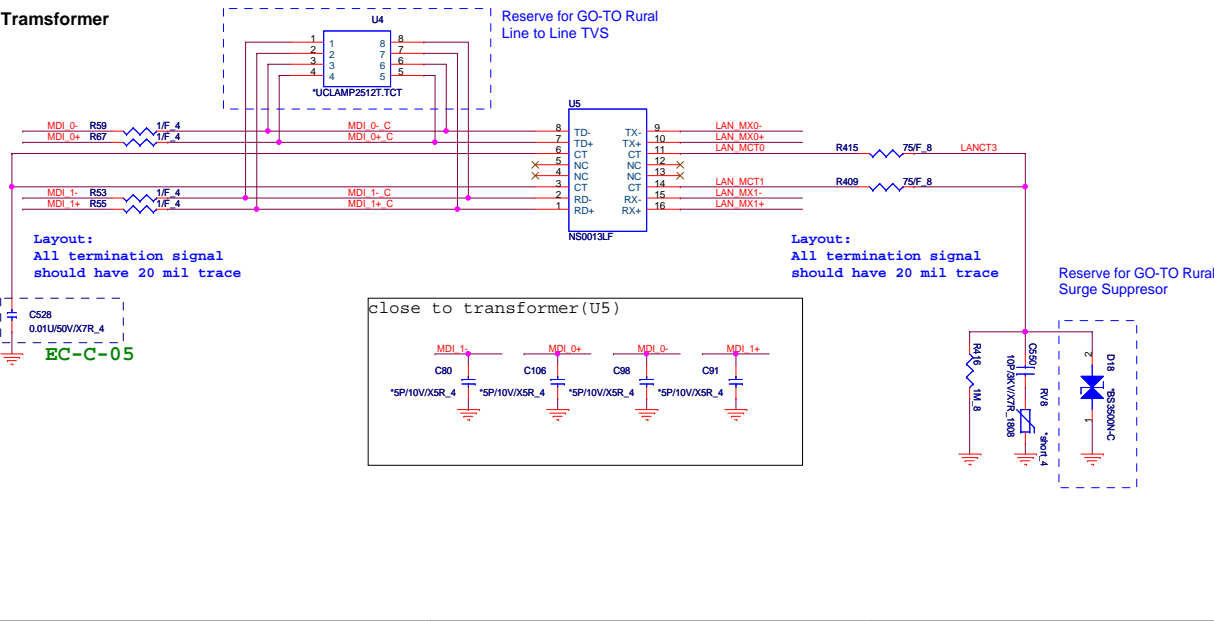
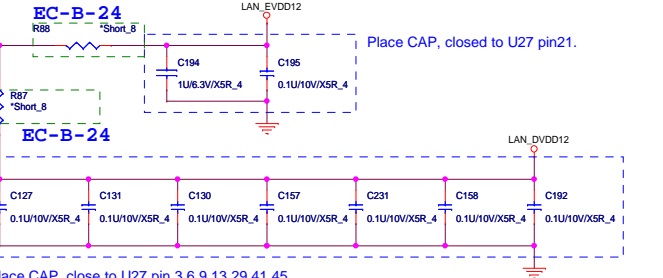
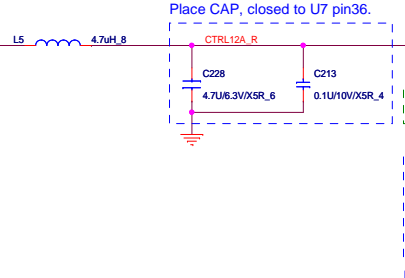
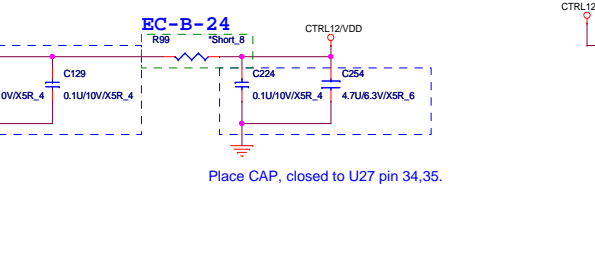
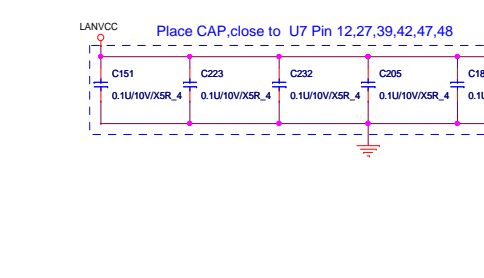
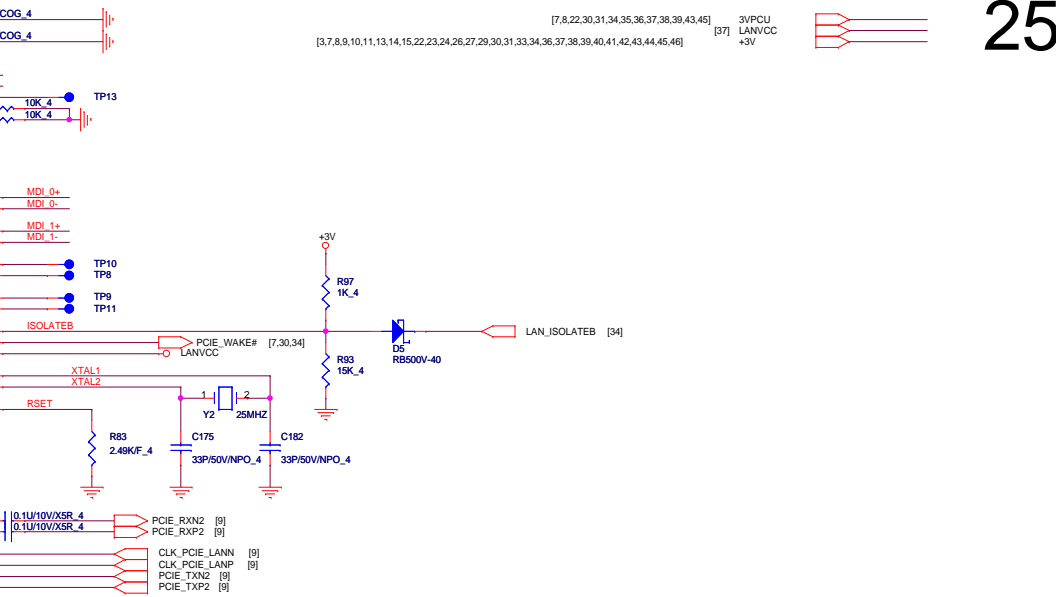
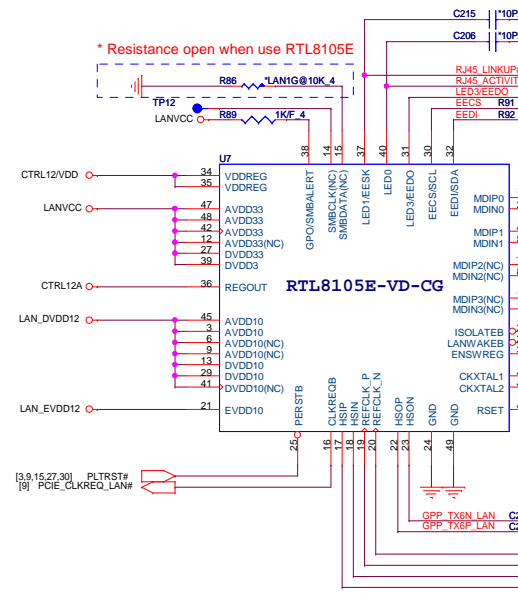
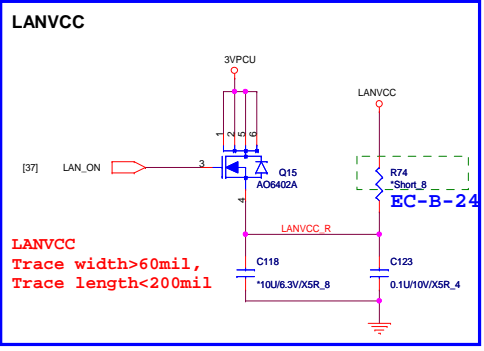
For ESD Layout note: Place close to HDMI Conn

EMI reserve for HDMI

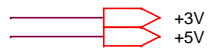


EC-B-17

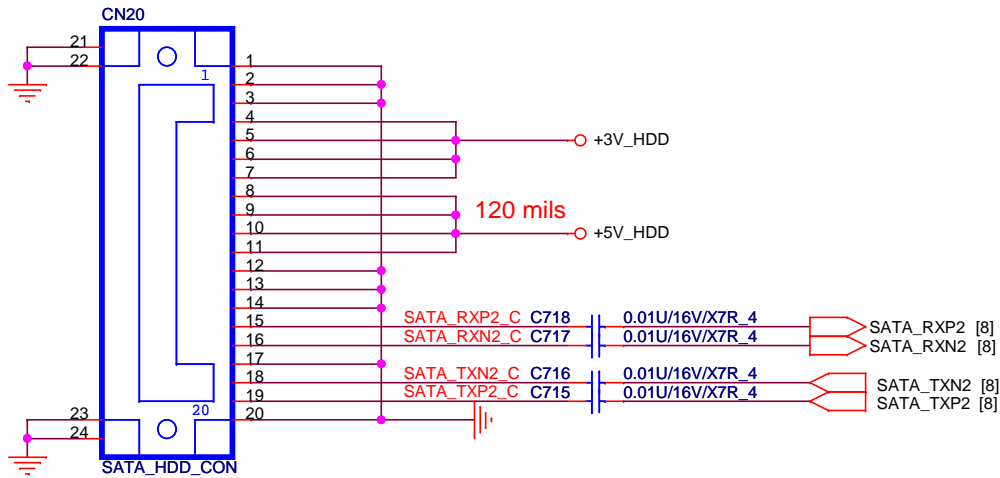




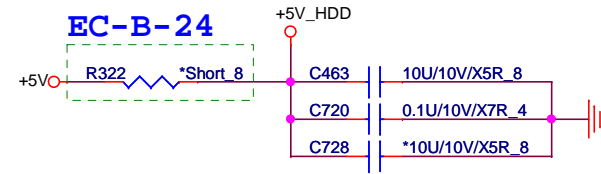
PLACE SATA AC COUPLING CAPS CLOSE TO Connector



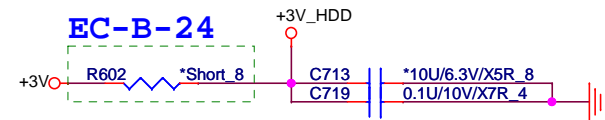
[3,7,8,9,10,11,13,14,15,22,23,24,25,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
[8,11,23,24,33,36,37,38]




DC Current rating: 2 A (MAX)



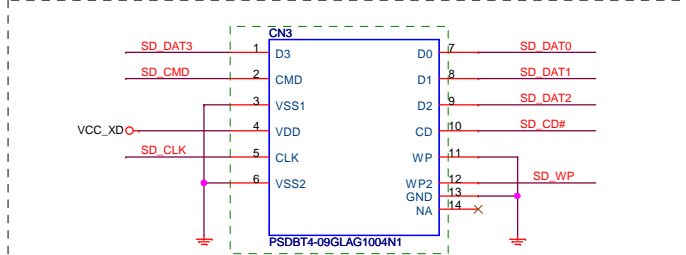
DC Current rating: 3 A (MAX)



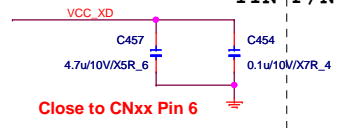
		PROJECT LZ8 Chief River DIS	
		Quanta Computer Inc.	
Size	Document Number		Rev
	SATA		1A
Date:	Tuesday, December 20, 2011	Sheet	26 of 49

R277	0	Normal mode
	1	Saving mode

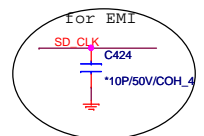
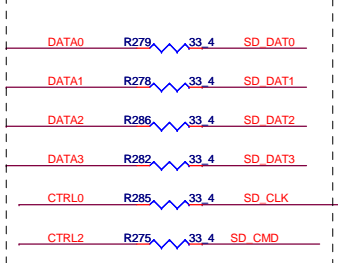
2 IN 1 CARD READER (SD/MMC)



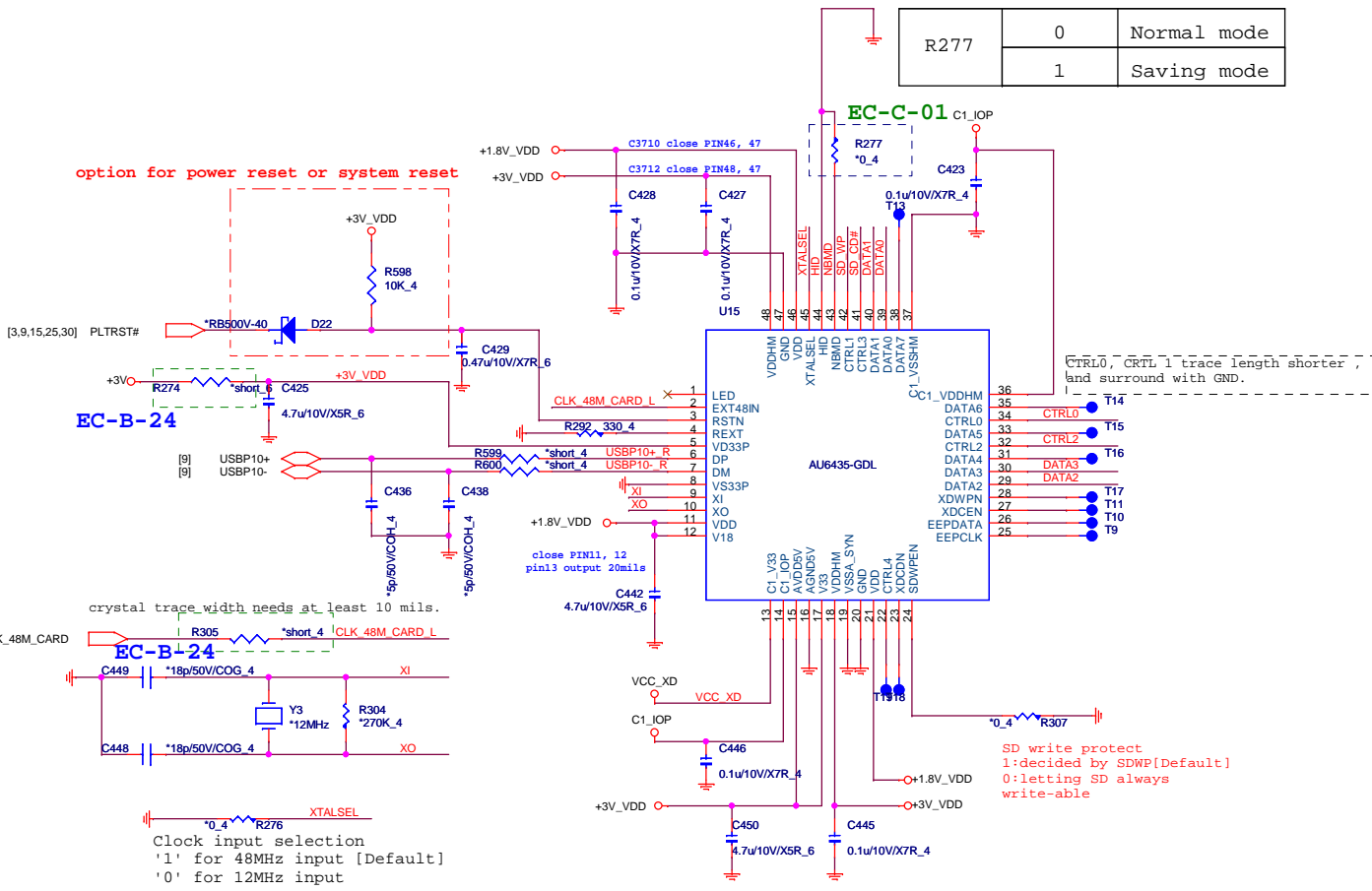
EC-B-21
 QCI P/N : DFHD14MS009
 TTN P/N : PSDBT4-09GLAG1004N1



Main	DFHD14MS009
Second	



SD write protect
 1:decided by SDWP[Default]
 0:letting SD always write-able



option for power reset or system reset

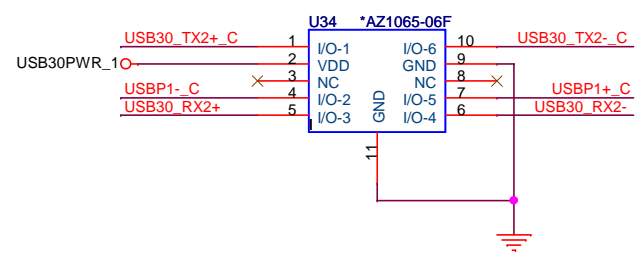
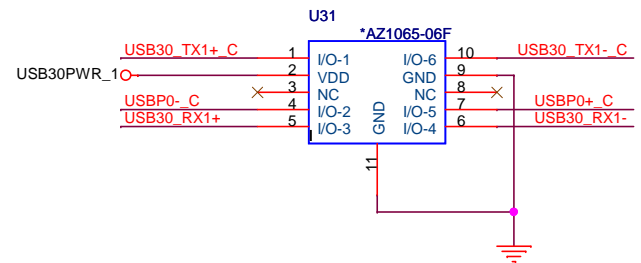
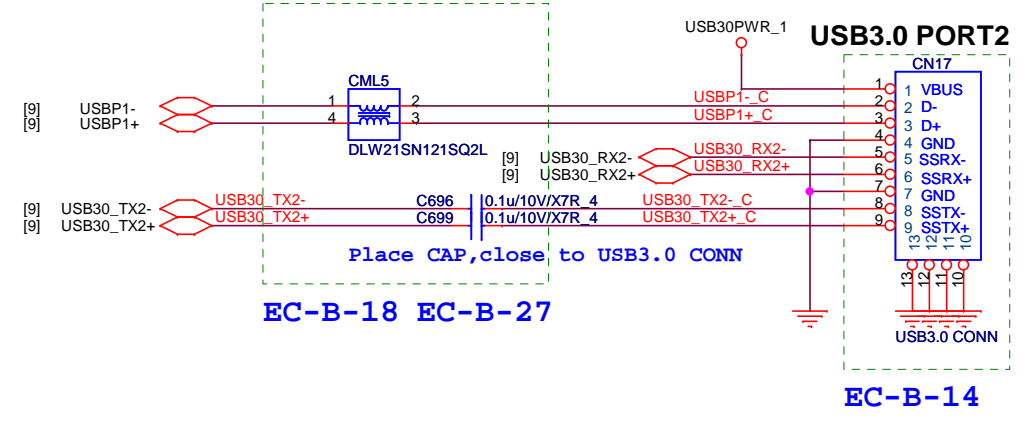
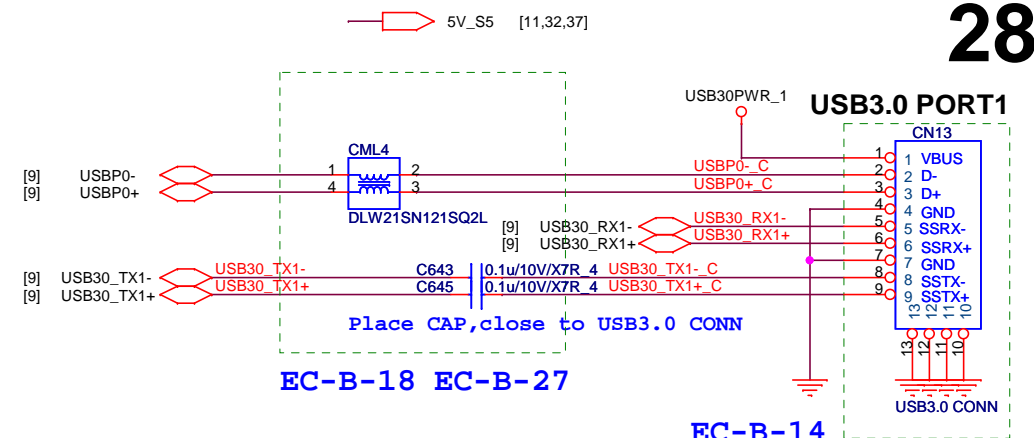
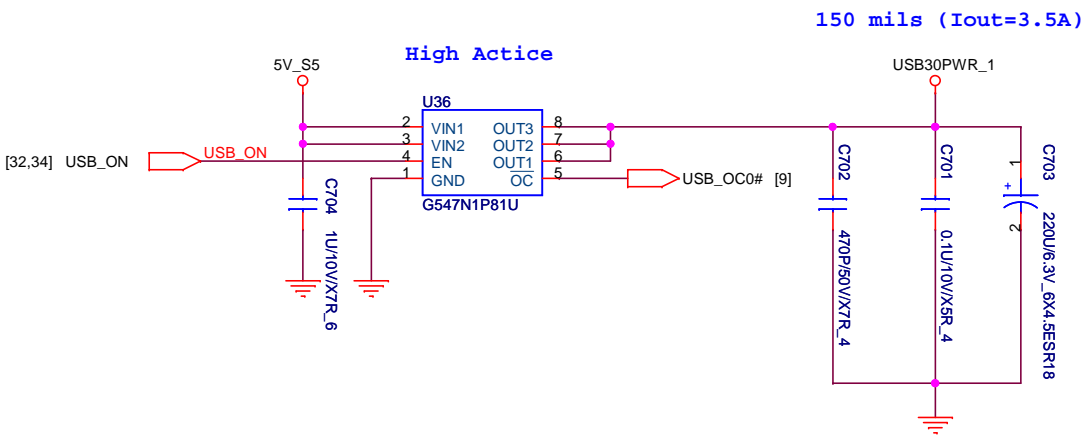
EC-B-24

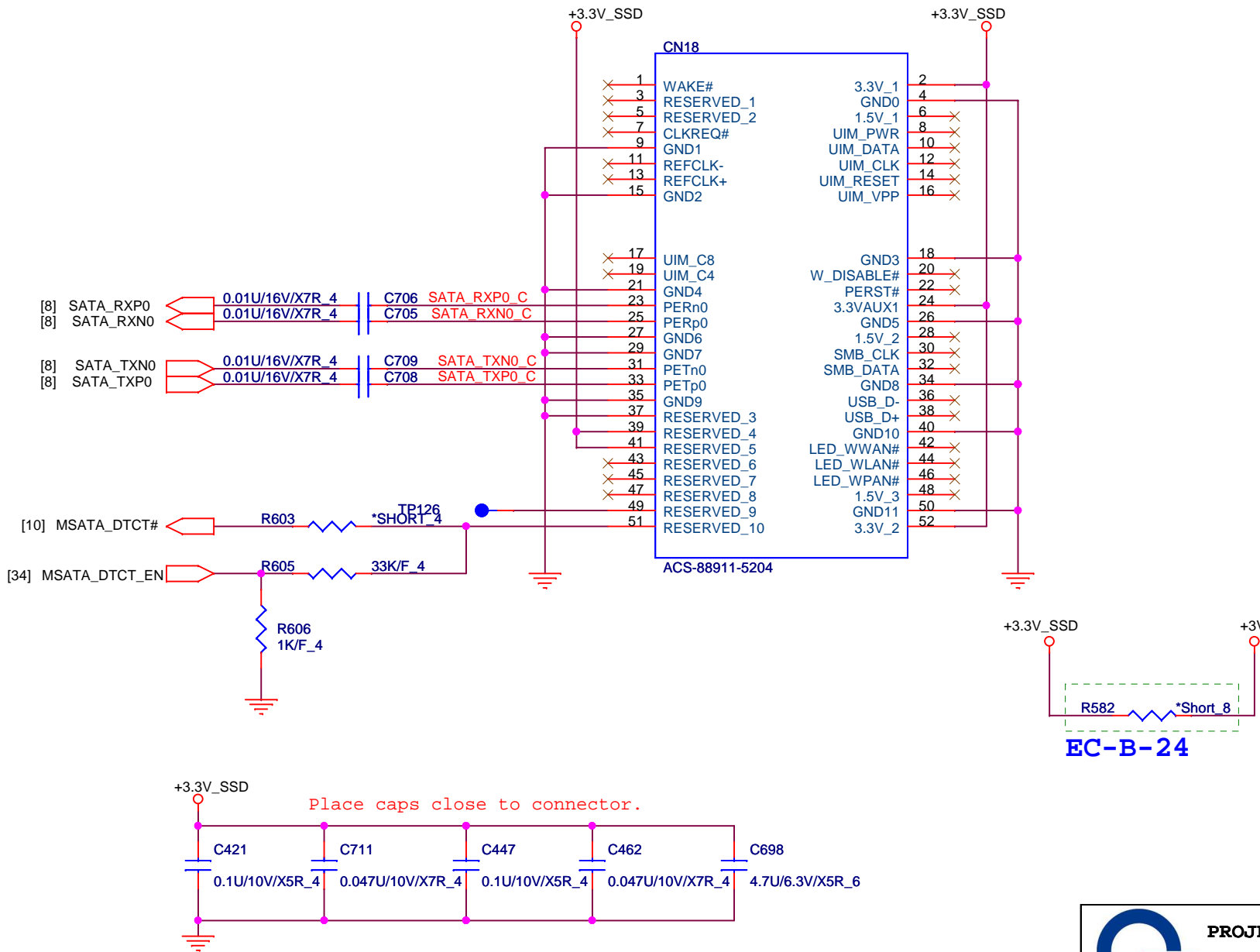
EC-B-24


XTALSEL
 Clock input selection
 '1' for 48MHz input [Default]
 '0' for 12MHz input

CTRL0, CTRL1 trace length shorter,
 and surround with GND.

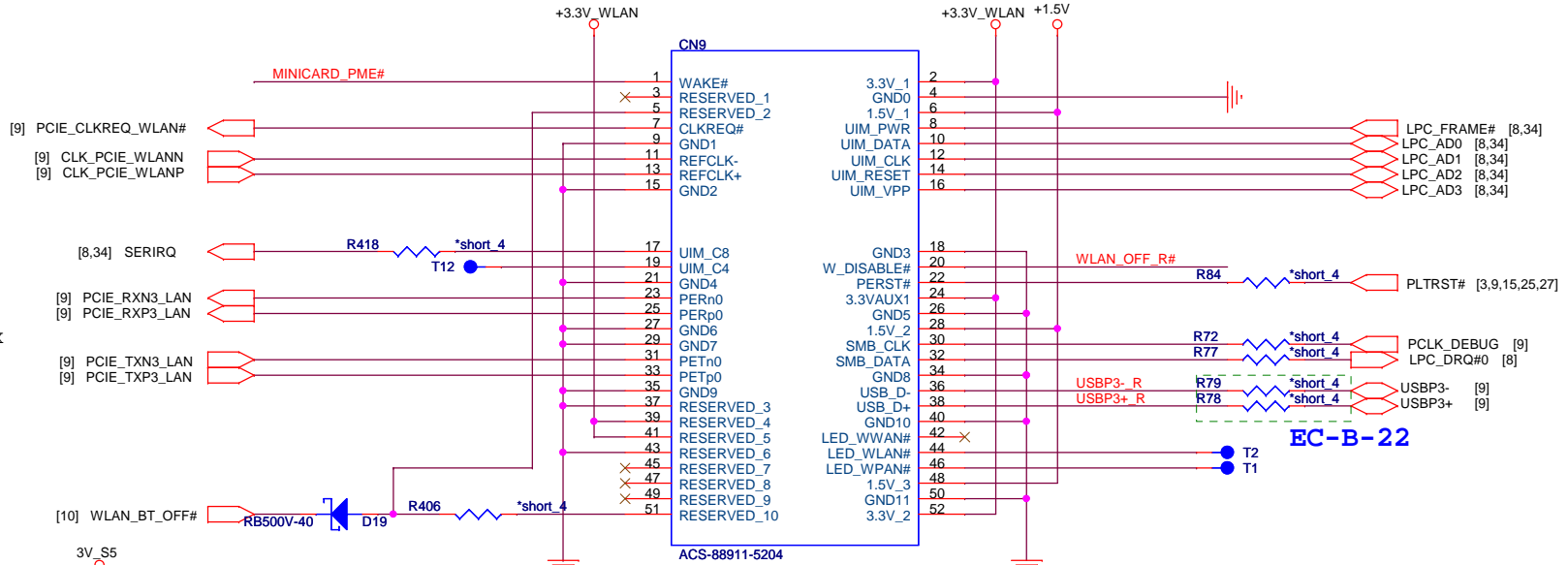
crystal trace width needs at least 10 mils.



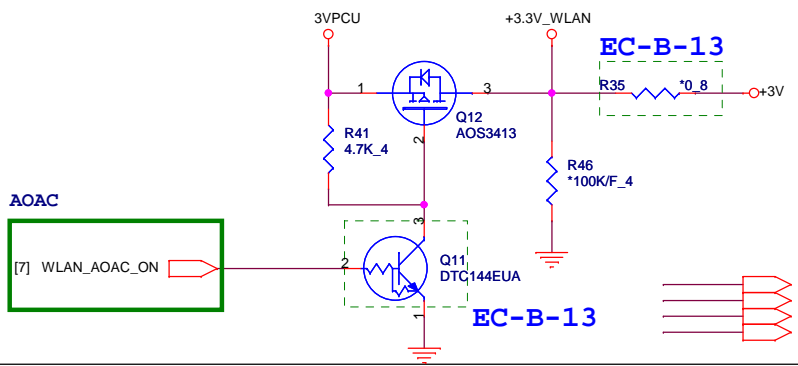
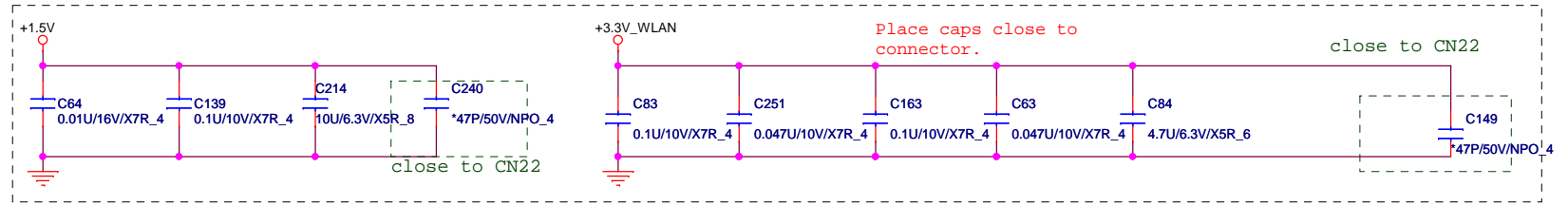
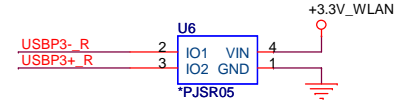
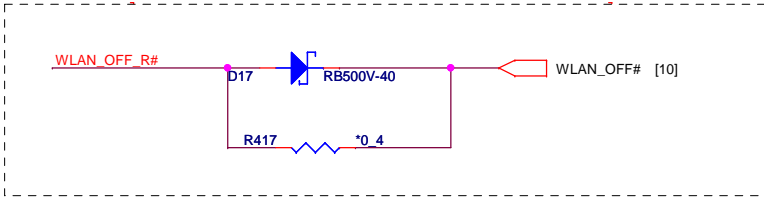
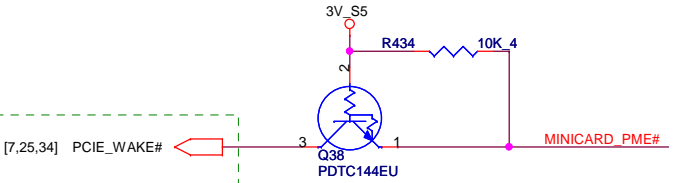


 PROJECT LZ8 Chief River DIS Quanta Computer Inc.		Size	Document Number	Rev
		Custom	MINI Card (SSD)	1A
Date:	Tuesday, December 20, 2011	Sheet	29	of 49

MiniCard WLAN connector



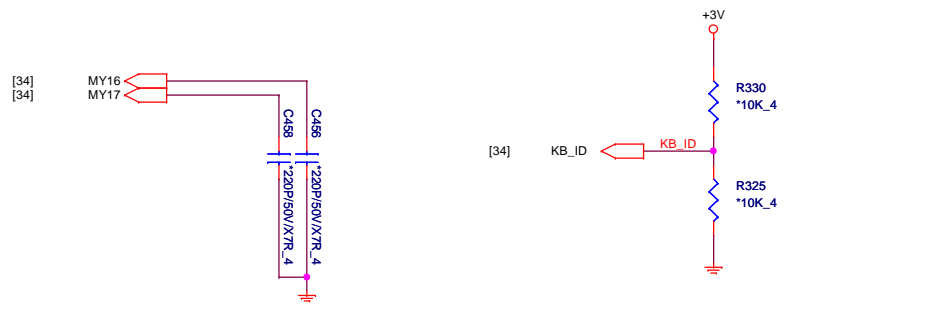
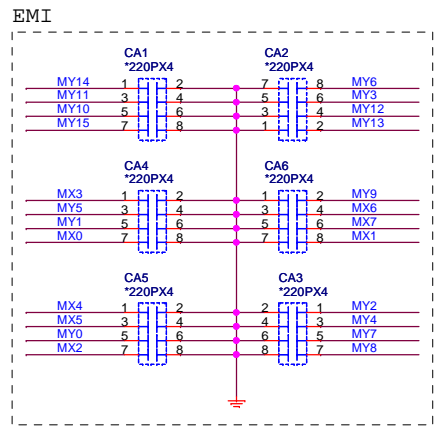
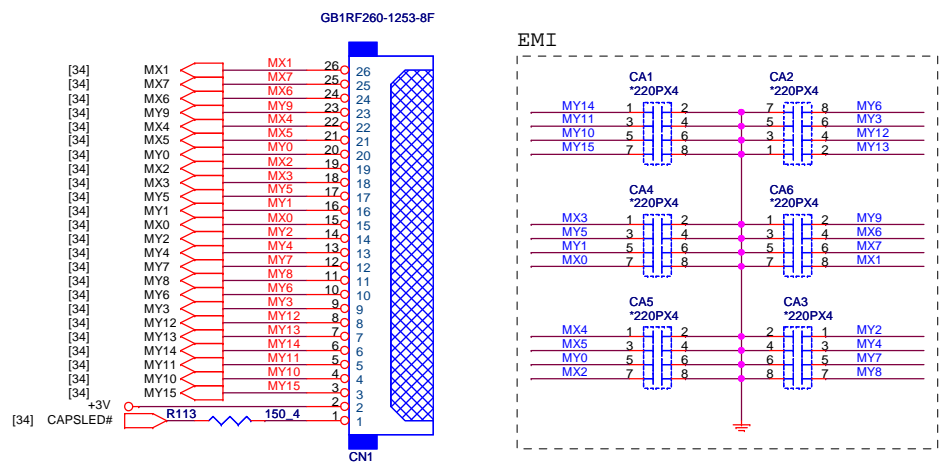
PCI-Express TX and RX direct to connector



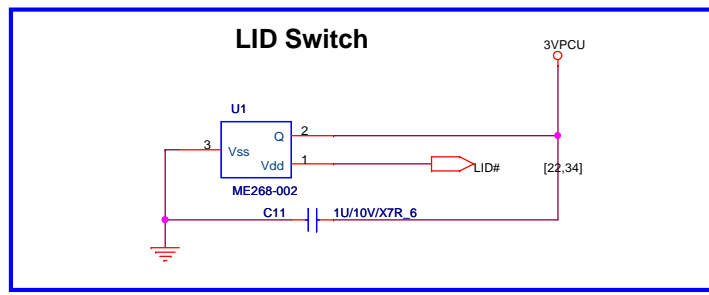
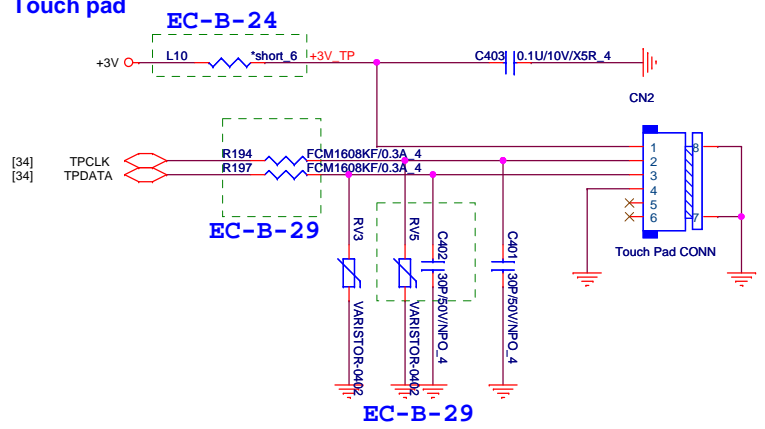
- 3VPCU [7, 8, 22, 25, 31, 34, 35, 36, 37, 38, 39, 43, 45]
- +3V [3, 7, 8, 9, 10, 11, 13, 14, 15, 22, 23, 24, 25, 26, 27, 29, 31, 33, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46]
- +1.5V [11, 40]
- 3V_S5 [3, 7, 8, 9, 10, 11, 24, 35, 37]

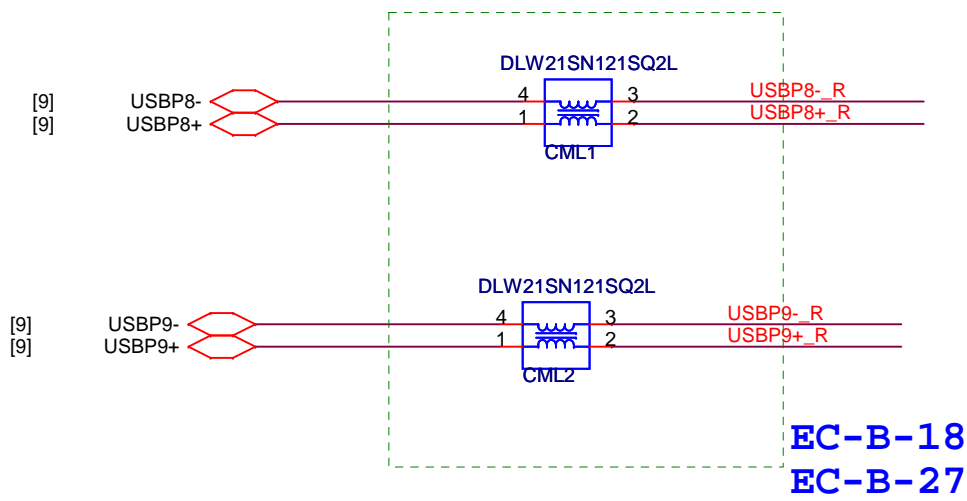
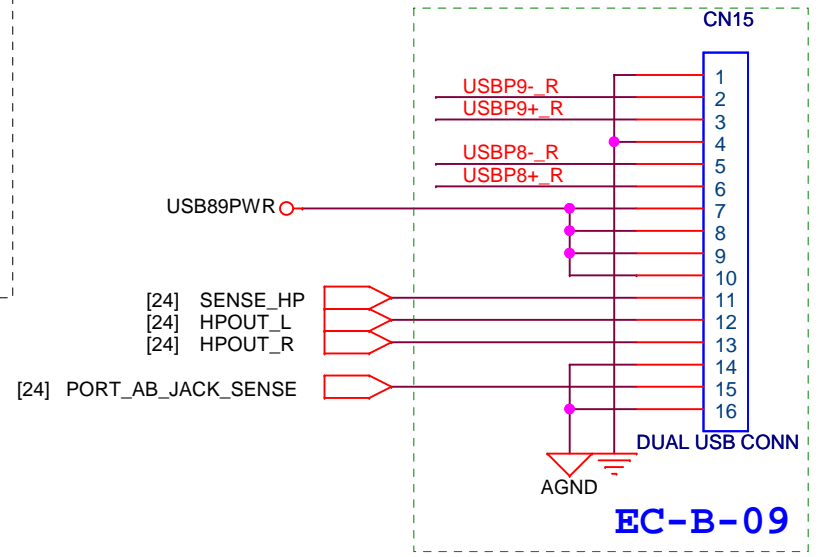
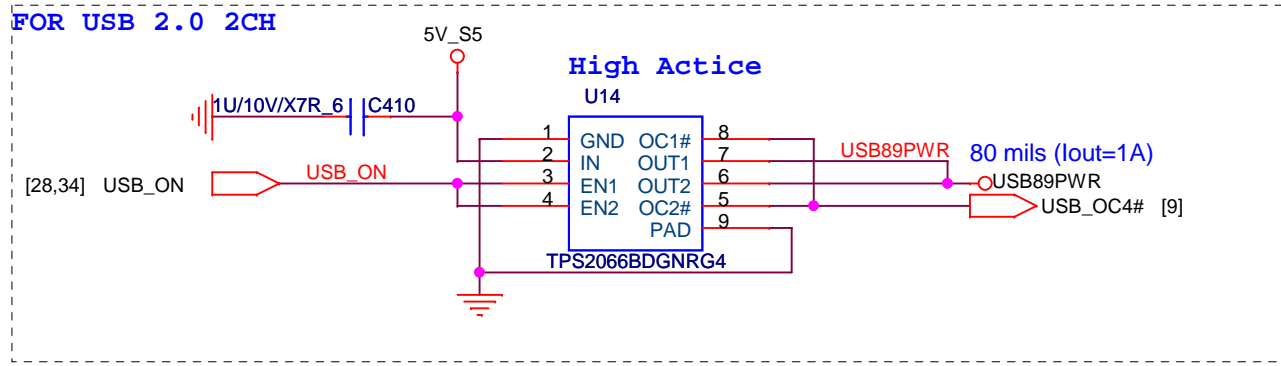
KEYBOARD

+3V [3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,33,34,36,37,38,39,40,41,42,43,44,45,46]



Touch pad





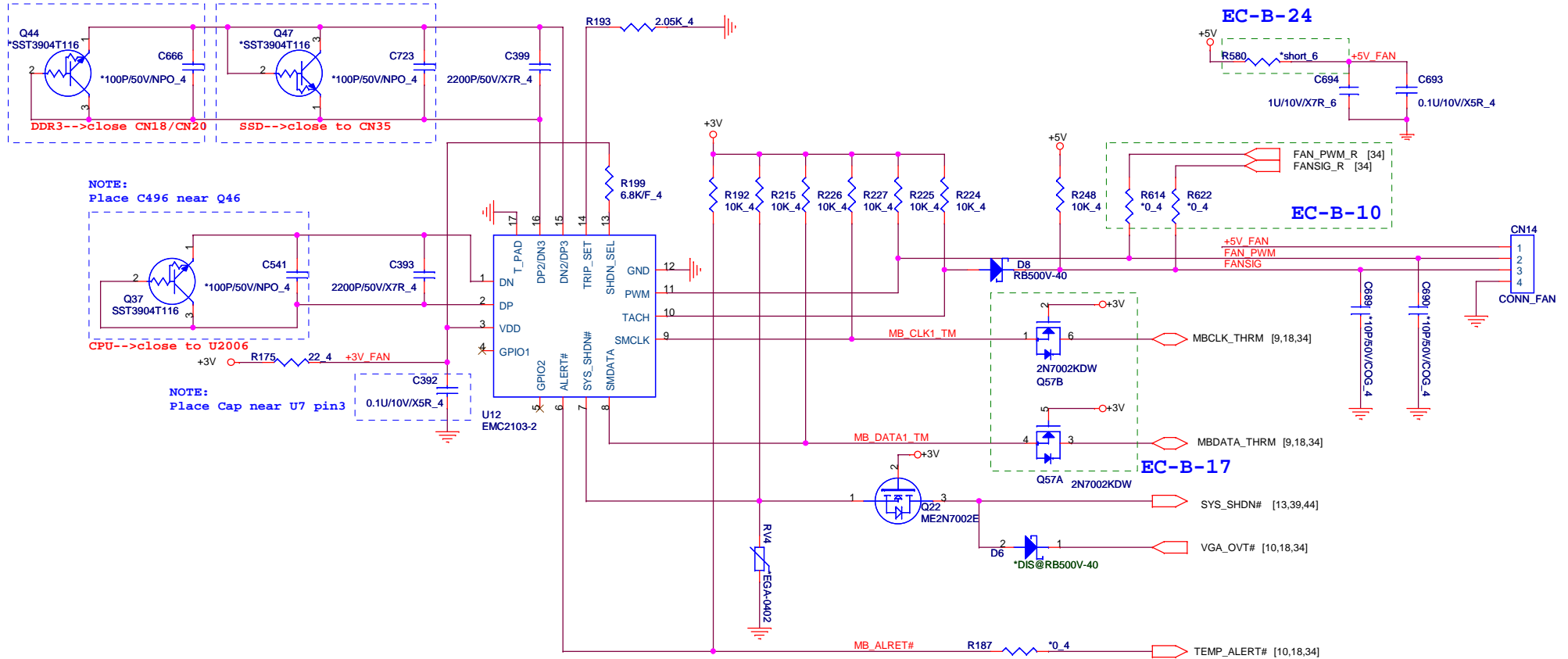
PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	USB2.0--Audio Jack Conn	3A
Date:	Tuesday, December 20, 2011	Sheet 32 of 49


NOTE:
Place C587 near Q47

NOTE:
Place C588 near Q50

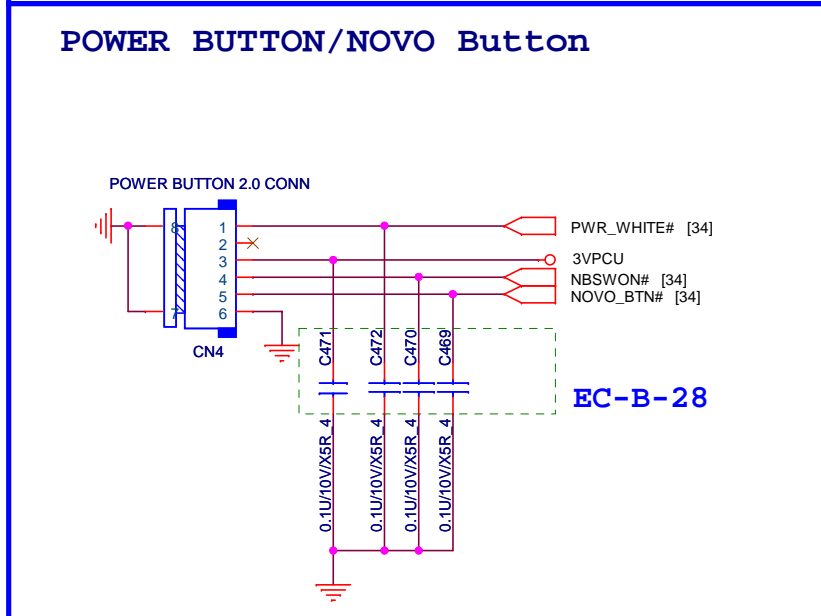
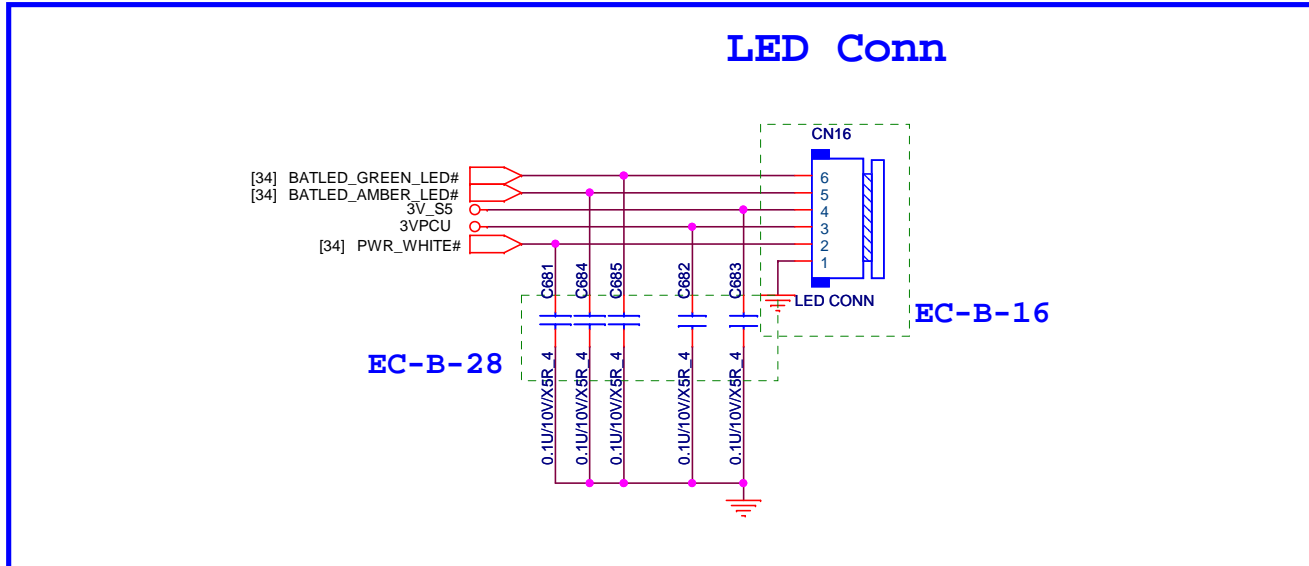


NOTE:
Place C496 near Q46

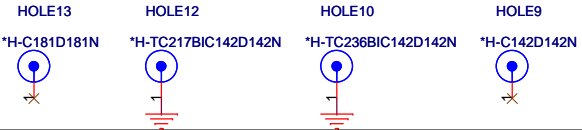
NOTE:
Place Cap near U7 pin3

 PROJECT LZ8 Chief River DIS Quanta Computer Inc.		
Size	Document Number	Rev
	FAN/Thermal	2A
Date:	Tuesday, December 20, 2011	Sheet 33 of 49

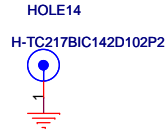
3VPCU [7,8,22,25,30,31,34,36,37,38,39,43,45]
 3V_S5 [3,7,8,9,10,11,24,30,37]



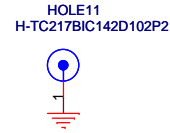
Hole for CPU support



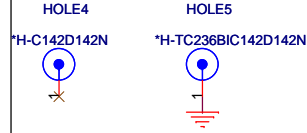
MiniCard WWAN



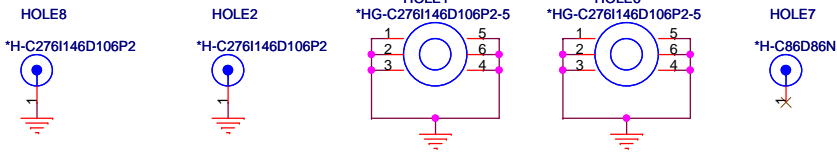
MiniCard WLAN



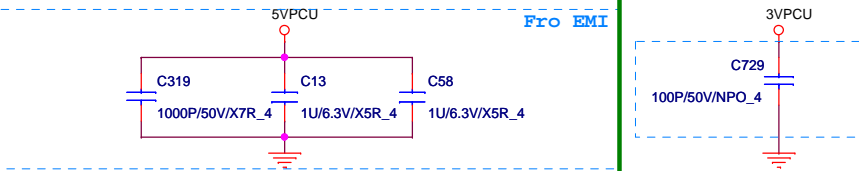
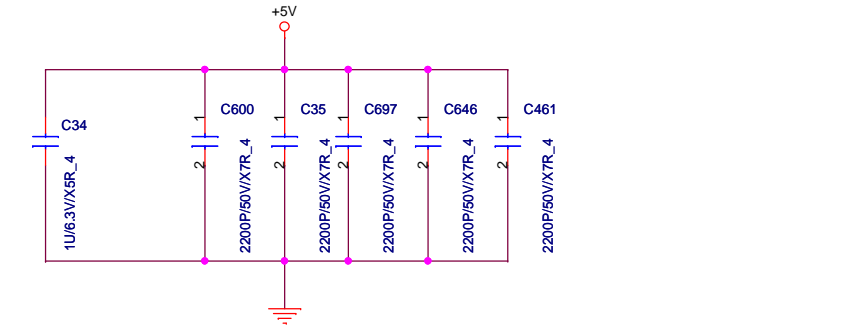
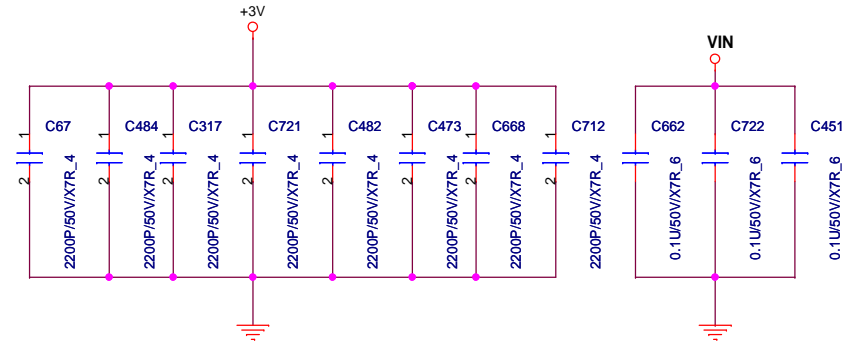
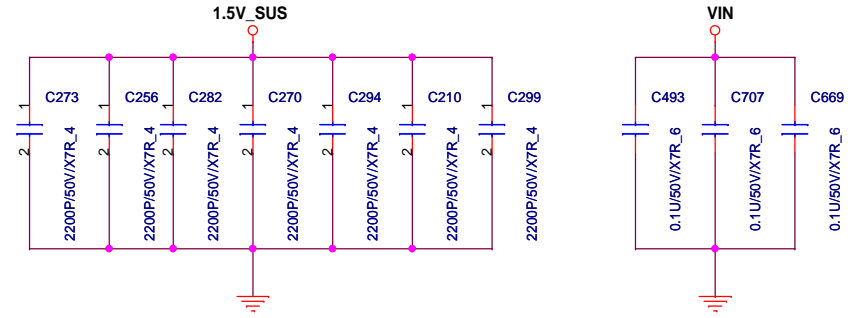
Hole for GPU support



Boundary Hole

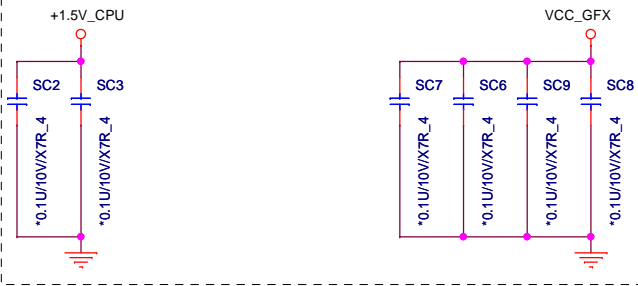


EMI

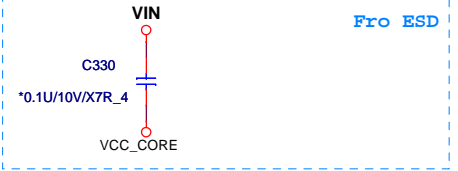


3VPCU [7,8,22,25,30,31,34,35,37,38,39,43,45]

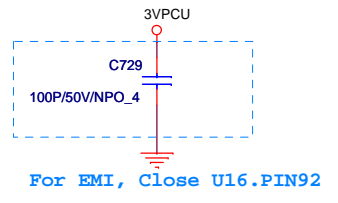
Fro ESD



Fro ESD



Fro EMI



EC-B-22

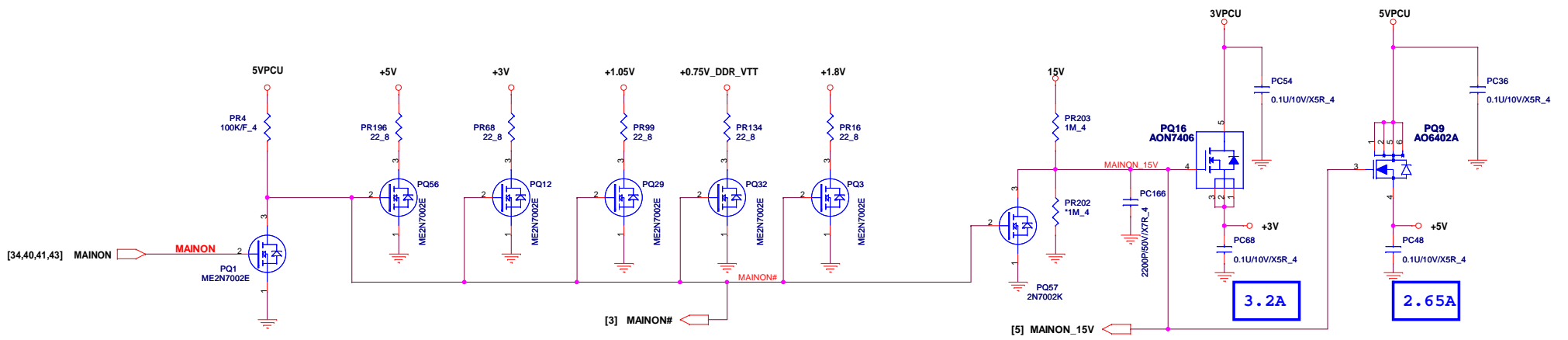
For EMI, Close U16.PIN92

+1.5V_CPU	[3,5,40]
3VPCU	[7,8,22,25,30,31,34,35,37,38,39,43,45]
VCC_GFX	[5,44]
+3V	[3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,37,38,39,40,41,42,43,44,45,46]
+5V	[8,11,23,24,26,33,37,38]
1.5V_SUS	[3,11,13,14,37,40,46]
5VPCU	[11,22,37,39,40,41,42,43,44,45,46]
VIN	[22,38,39,40,41,42,44,45]
VCC_CORE	[5,6,44]
+1.05V	[3,5,7,8,9,11,37,41,46]

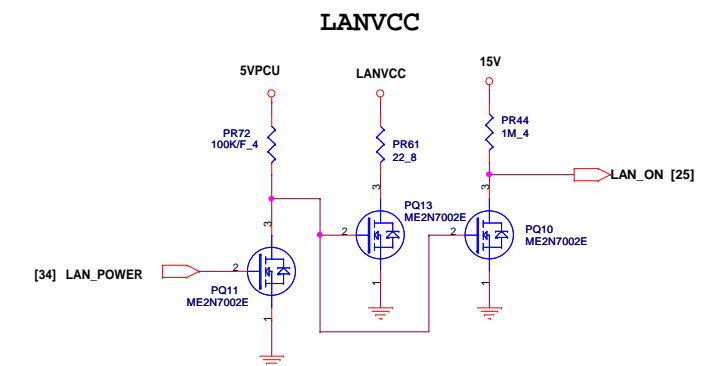
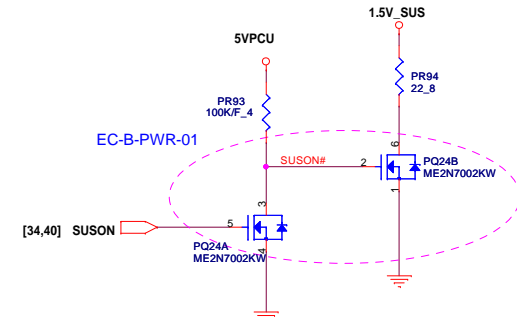
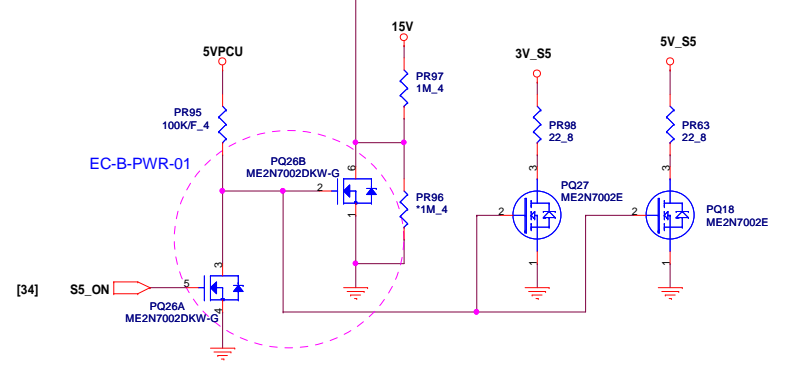
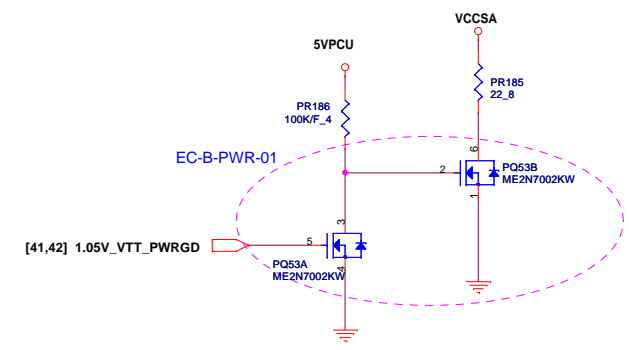
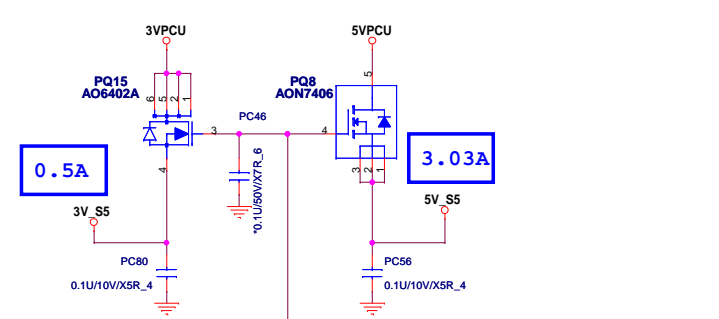
PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

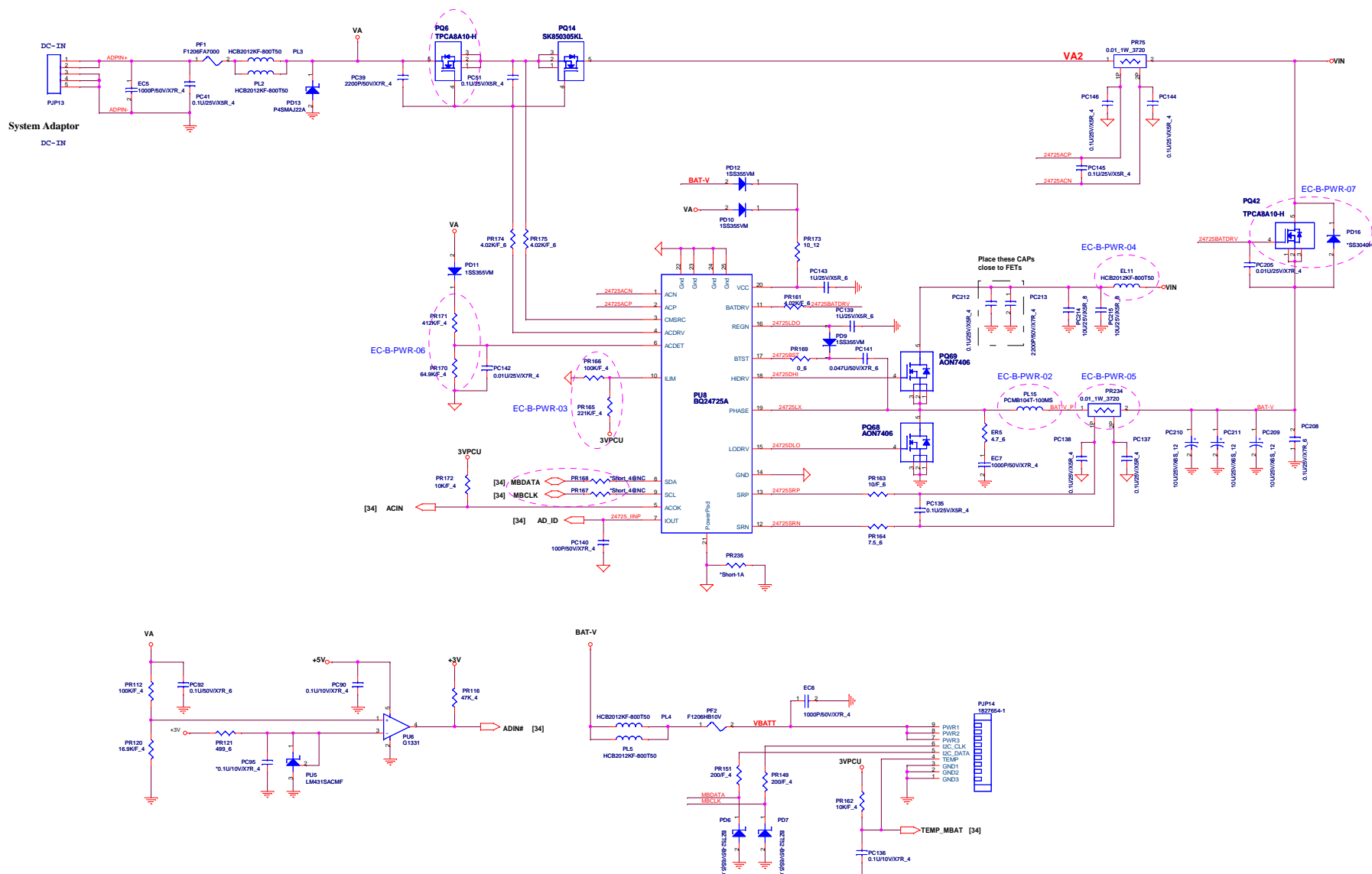
Size: Document Number: **Screw Hole/EMI** Rev: 1A

Date: Tuesday, December 20, 2011 Sheet: 36 of 49



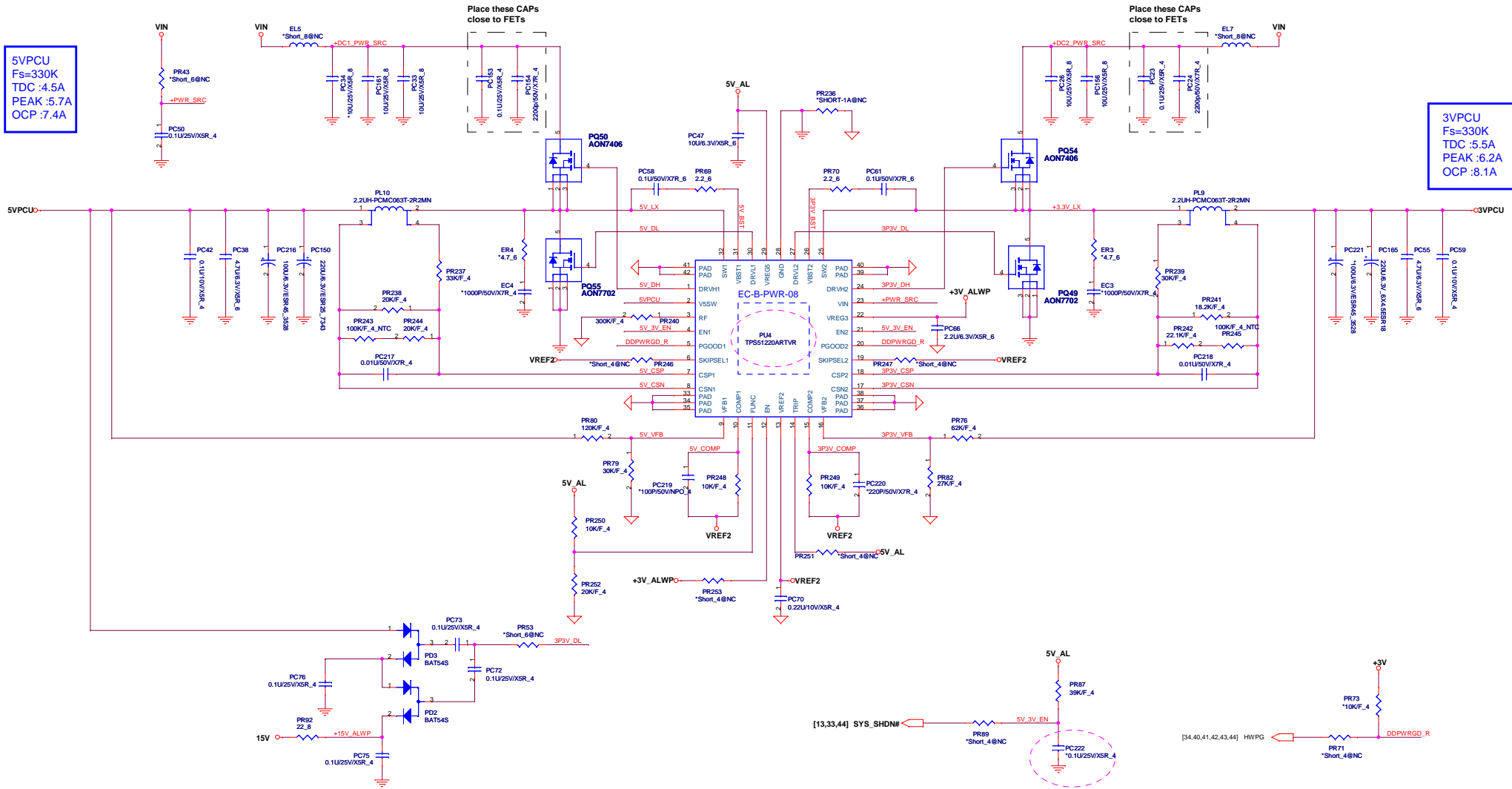
3V_S5, 5V_S5

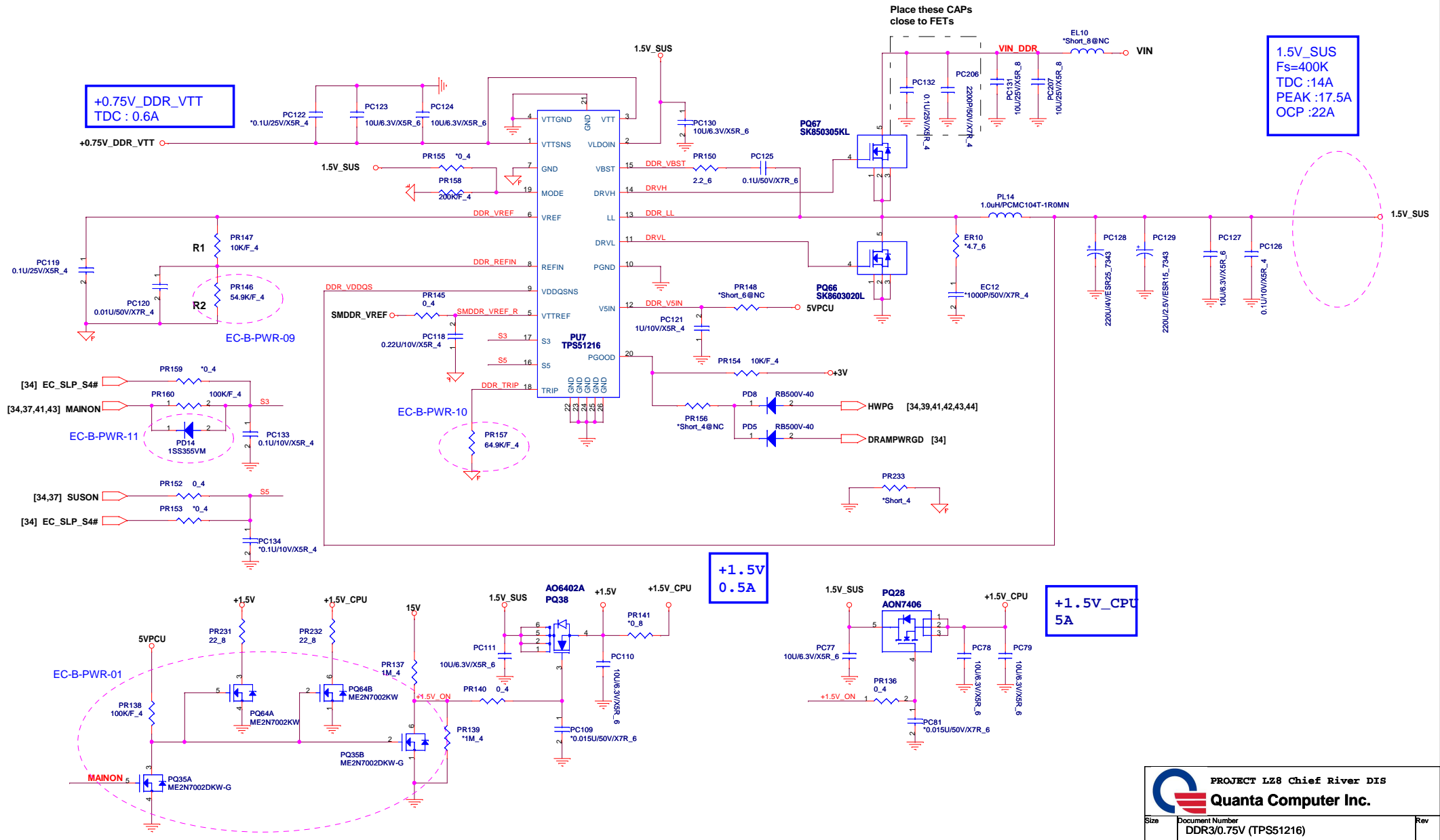




5VPCU
Fs=330K
TDC :4.5A
PEAK :5.7A
OCP :7.4A

3VPCU
Fs=330K
TDC :5.5A
PEAK :6.2A
OCP :8.1A



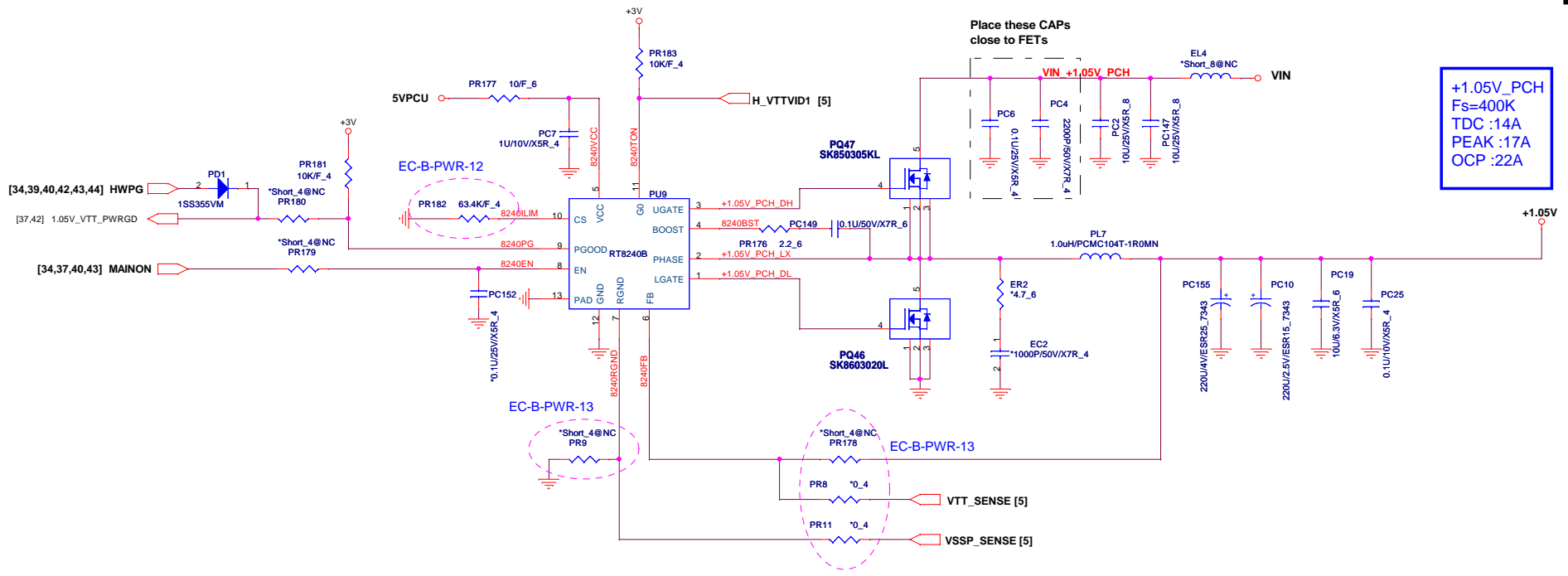


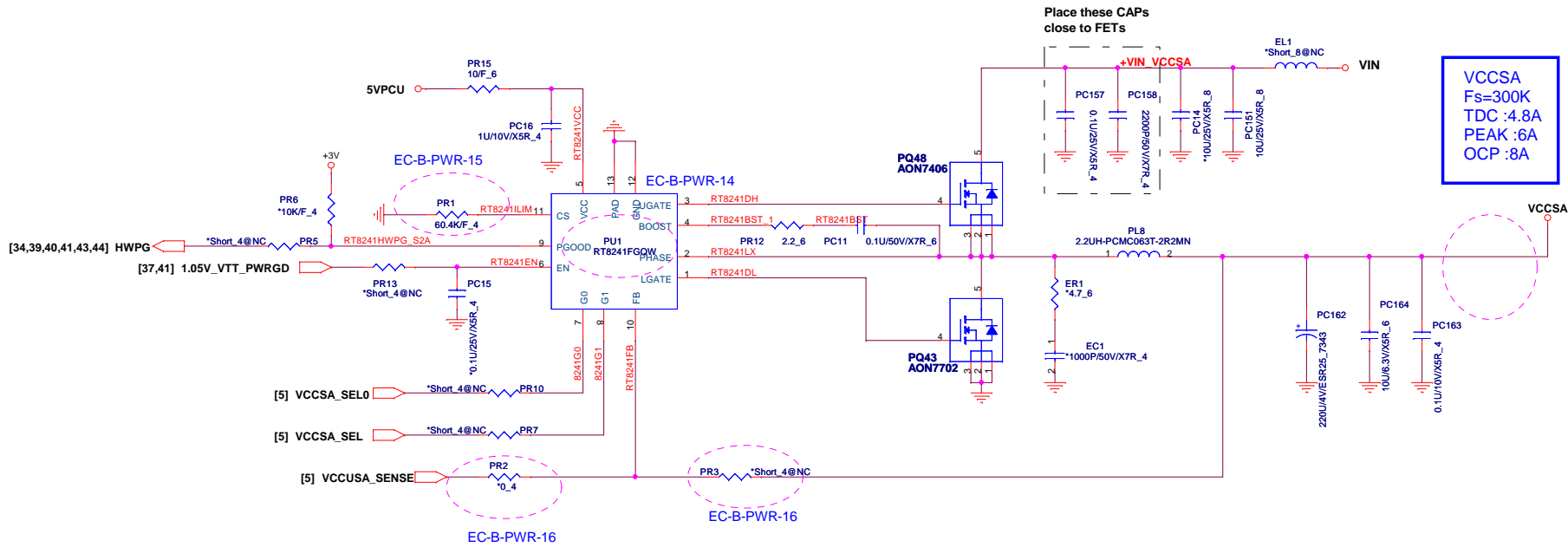
+0.75V_DDR_VTT
TDC : 0.6A

1.5V_SUS
Fs=400K
TDC :14A
PEAK :17.5A
OCP :22A

+1.5V
0.5A

+1.5V_CPU
5A

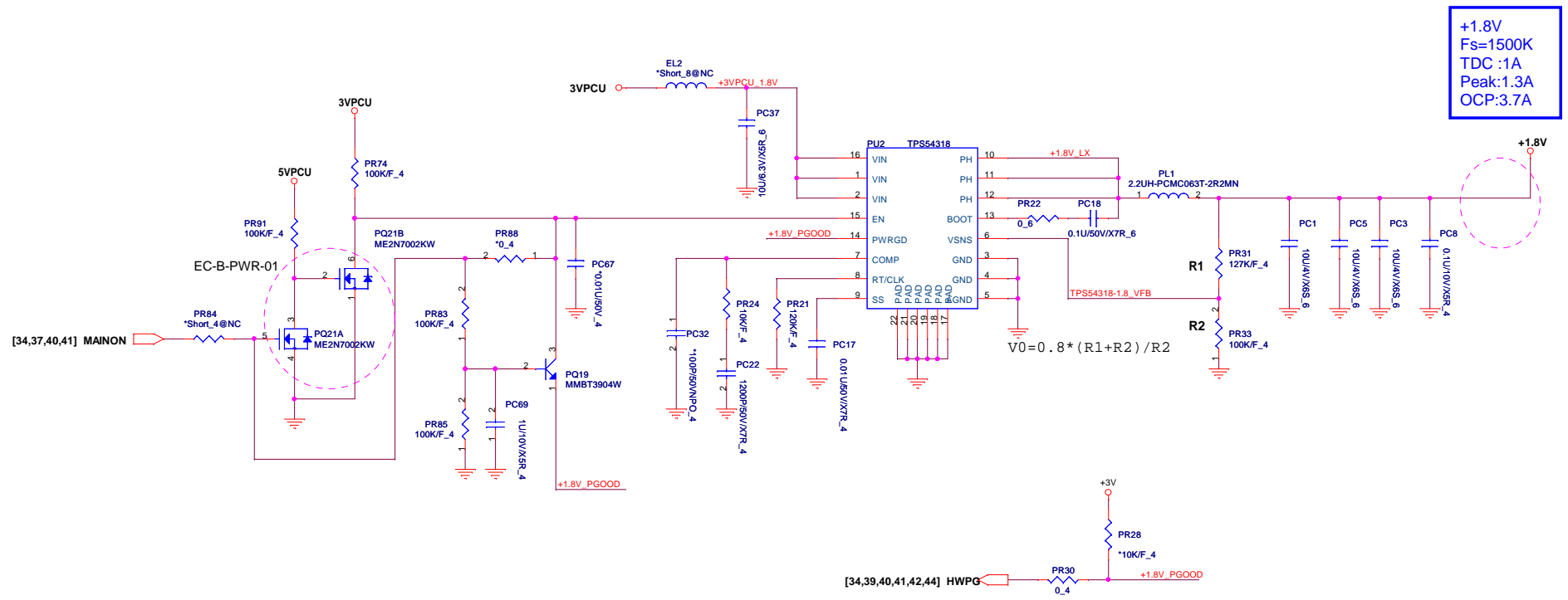




VCCSA
 Fs=300K
 TDC :4.8A
 PEAK :6A
 OCP :8A

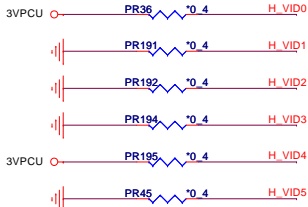
G0	G1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

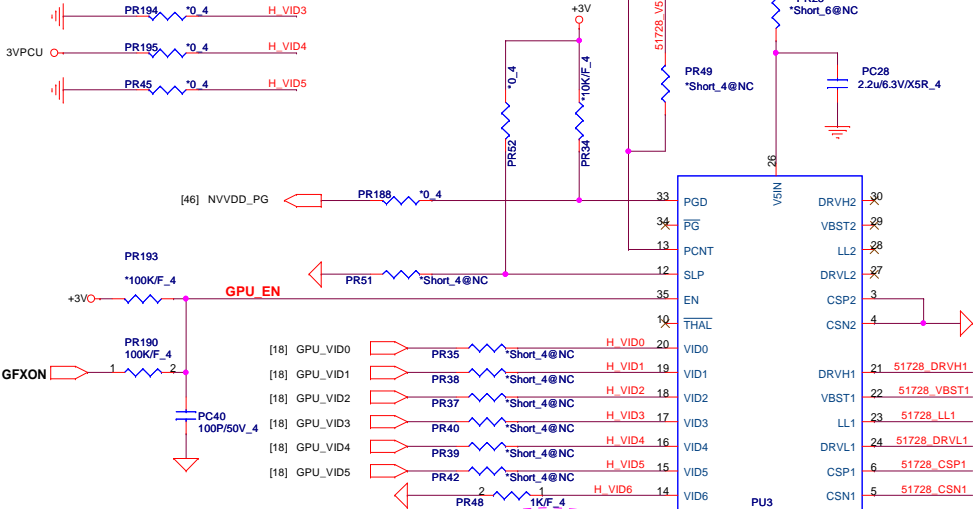


+1.8V
 Fs=1500K
 TDC :1A
 Peak:1.3A
 OCP:3.7A

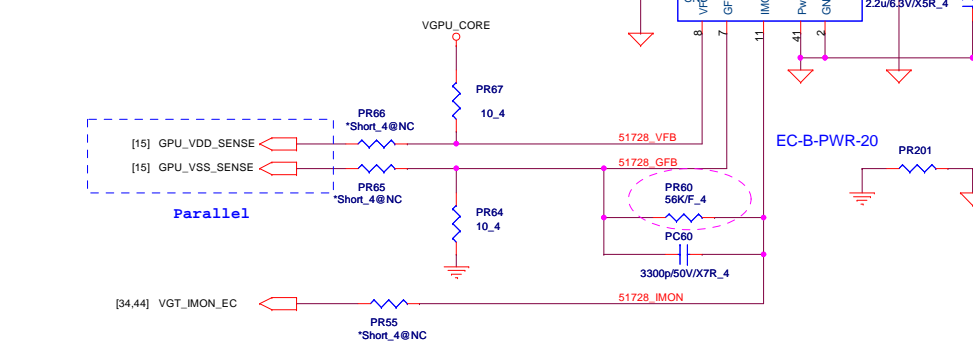
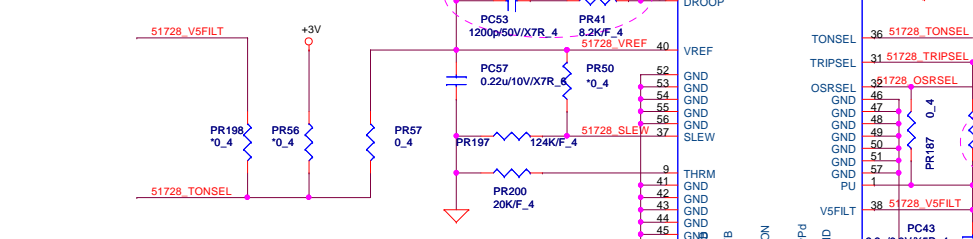
VID 1.2875V



[18] dGPU_PCNT



EC-B-PWR-22



EC-B-PWR-20

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

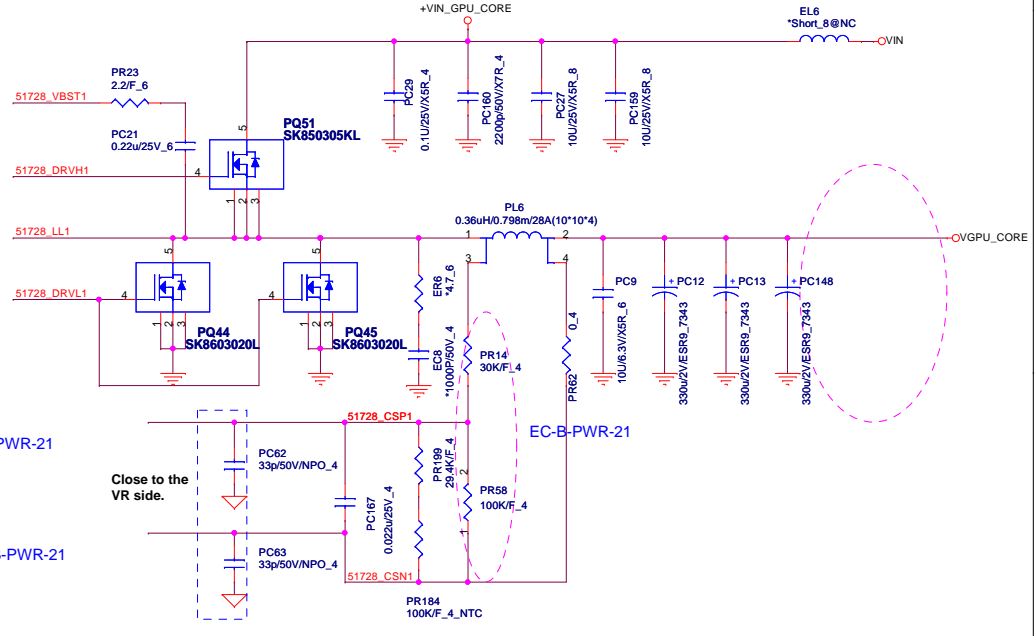
EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

EC-B-PWR-21

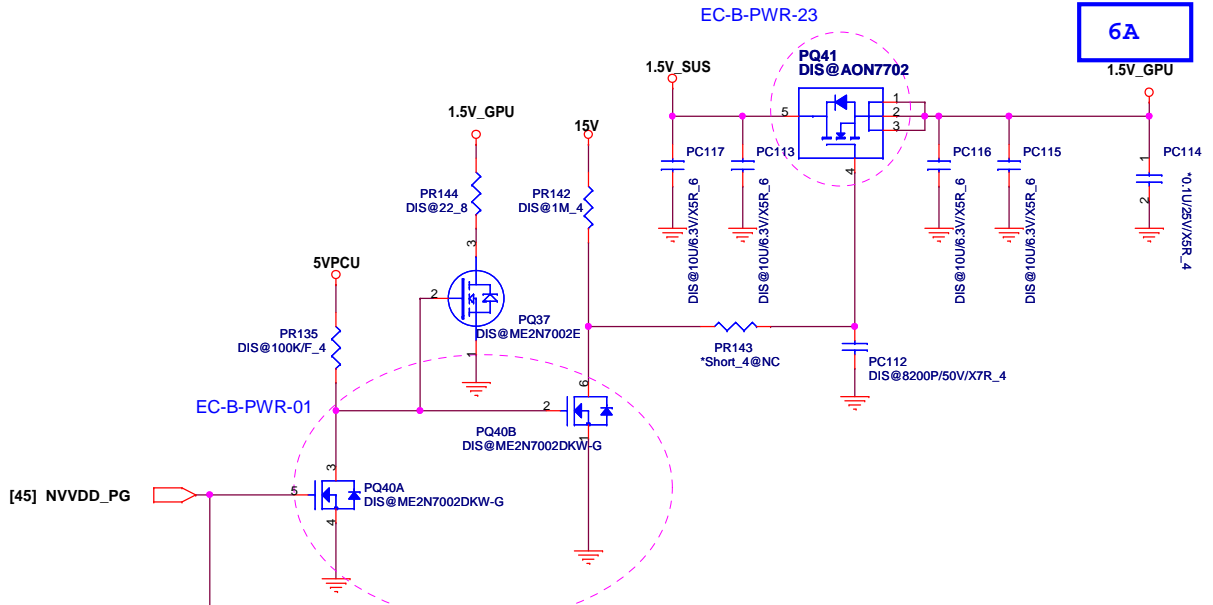
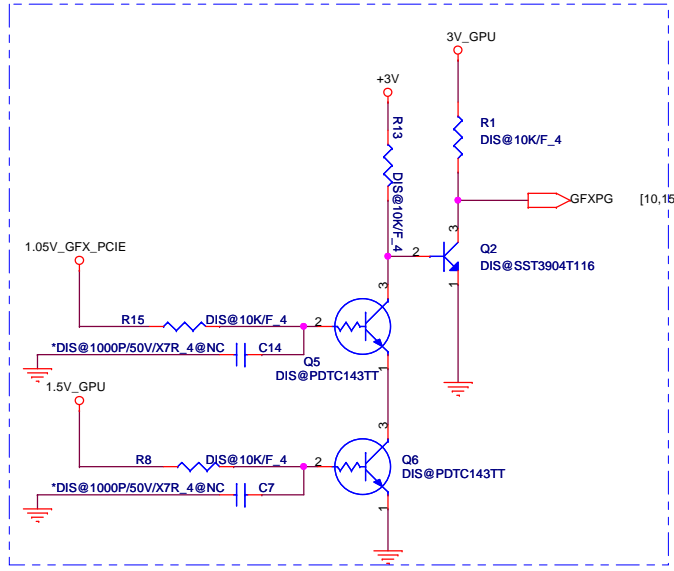


VGPU_CORE
 Fs=300k Hz
 TDC:20A
 Peak:25A
 OCP:33A
 Loadline=0mV/A

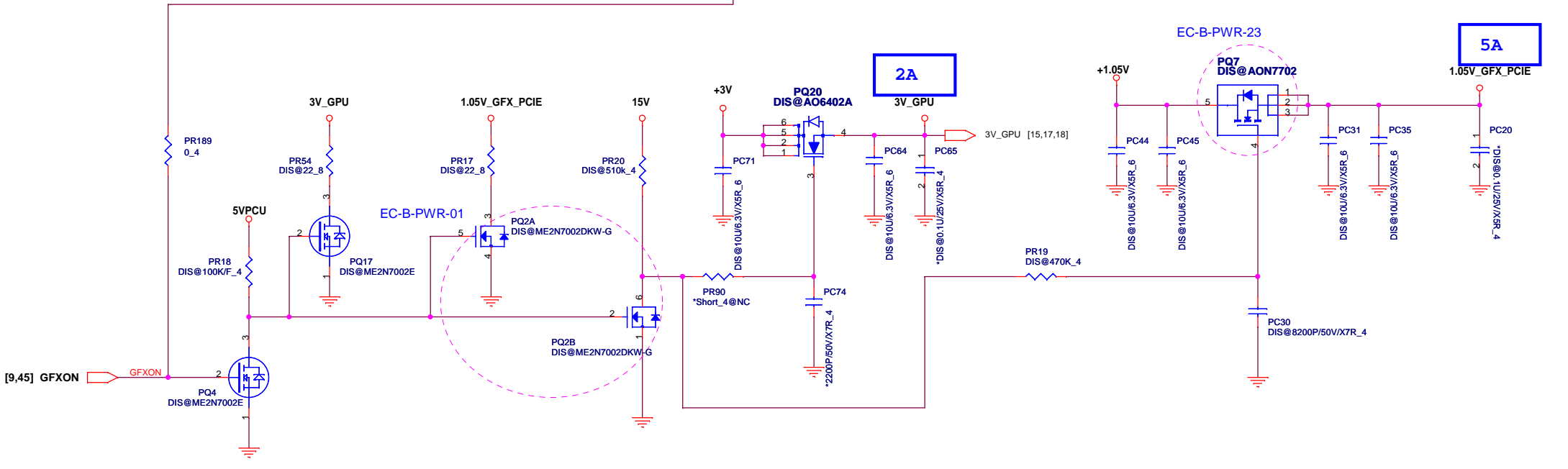
Close to the VR side.

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	DGPU Core (TPS51728)	1A
Date:	Tuesday, December 20, 2011	Sheet 45 of 49



6A



2A

5A

EC N	PG	DA A/mm/dd	PA R	DE C
EC-B-01	7,11,34	11/10/13	Add R607,R608,R621 and no ASM	Add DEEP S3 function
EC-B-02	7	11/10/13	R210	R210 chnage to short pad
EC-B-03	9	11/10/13	R610 no ASM,R611 ASM, R	For DGPU power enable sequence
EC-B-04	10	11/10/13	R573 no ASM,R572 ASM	Change Board ID for SIV stage
EC-B-05	10,22	11/10/13	Q49,R613,C724,R612,Q48 add and ASM	Change CCD control by PCH GPIO35
EC-B-06	23	11/10/13	CN10	Change CN10 to correct footprint
EC-B-07	24	11/10/13	R	Change Audio detect schematic
EC-B-08	25	11/10/13	CN8	Change CN8 to correct footprint
EC-B-09	32	11/10/13	CN15	Change CN25 Pin define
EC-B-10	33	11/10/13	Add R614,R622 no ASM	Add EC detect Fan speed schematic
EC-B-11	34	11/10/13	DEL R321	Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-B-12	34	11/10/13	R298 no ASM	EC can output CLOCK by itself
EC-B-13	30	11/10/13	R35 no ASM,Q11ASM	input AOAC function
EC-B-14	28	11/10/13	CN13,CN17	Change CN13,CN17 to correct footprint
EC-B-15	28	11/10/13	add Q51,R623 no ASM	Add DEEP S3 function
EC-B-16	35	11/10/13	CN16	Change CN16 footprint for ME request
EC-B-17	9,18,22 23,33	11/10/14	Q30,Q31,Q26,Q27,Q34,Q35,Q3,Q4, Q41,Q42,Q23,Q24 DEL Add Q52,Q53,Q54,Q55,Q56,Q57 and ASM	Change MOS to Dual MOS
EC-B-18	21	11/10/19	Add Q58	For PS8622 flash ROM by EC ROM
EC-B-19	05	11/10/19	Add C727	Add a 10UF CAP for INTEL suggestion
EC-B-20	21	11/10/19	L14,L15,L16	Change footprint to 0603
EC-B-21	27	11/10/20	CN3	Change footprint for ME request
EC-B-22	36	11/10/24	Add C729,C730,C731	For EMI request
EC-B-23	3,7,11	11/10/24		Change LVDS singal by PCH provide
EC-B-24	7,24,25 26,27,29 30,31,33	11/10/24	R602,R322,R274,R305,R582,R580, L10,R129,R88,R87,R99,R79,R78, L22,L24	Change to short PAD
EC-B-25	8	11/10/24	BT1	Change BT1 footprint
EC-B-26	25	11/10/24	CN8	CN8 PIN4,5,7,8 connect to GND
EC-B-27	11,15	11/10/24	CML1,CML2,CML4,CML5 ASM R505,R502,R560,R563,R232,R233 R234,R235,C486,C488,C490,C497	for EMI request
EC-B-28	35	11/10/25	C472, C471, C470,C469,C681, C682 C683, C684,C685 ASM 0.1U	for EMI request
EC-B-29	35	11/10/25	RV5,C402 ASM 30P R194,R197 change to Bead	for EMI request
EC-B-30	35	11/10/26	C460 ASM 22P	for EMI request

EC	PG	D A/mm/dd	PA	DE
EC-B-PWR-01	37, 40, 43, 46	11/10/31	PQ26, PQ24, PQ53, PQ35, PQ64, PQ21, PQ2, PQ40	Change to dual 2N7002
EC-B-PWR-02	38	11/10/31	PL15	Change PL15 to 10u H, size 10*10
EC-B-PWR-03	38	11/10/31	PR165, PR166	Change charger ILIM resistors
EC-B-PWR-04	38	11/10/31	RL11	Add EL11
EC-B-PWR-05	38	11/10/31	PR234	Change Charger resistor
EC-B-PWR-06	38	11/10/31	PR170, PR171	Change charger ACDET res
EC-B-PWR-07	38	11/10/31	PQ42	Change MOSFET with Schottky
EC-B-PWR-08	39	11/10/31	PU4 and so on	Change 3V/5V IC and schematic
EC-B-PWR-09	40	11/10/31	PR146	Change voltage setting resistor
EC-B-PWR-10	40	11/10/31	PR157	Change 1.5V_SUS OCP resistor
EC-B-PWR-11	40	11/10/31	PD14	Add PD14 to improve sequence
EC-B-PWR-12	41	11/10/31	PR182	Change 1.05V OCP resistor
EC-B-PWR-13	41	11/10/31	PR8, PR9, PR11, PR178	Improve 1.05V feedback
EC-B-PWR-14	42	11/10/31	EU1	Change VCCSA IC to AL008241003
EC-B-PWR-15	42	11/10/31	PR1	Change VCCSA OCP resistor
EC-B-PWR-16	42	11/10/31	PR2, PR3	Improve VCCSA feedback
EC-B-PWR-17	44	11/10/31	PR216	Change GFXcore OCP resistor
EC-B-PWR-18	44	11/10/31	PR125	Change VCC_core IMON resistor
EC-B-PWR-19	44	11/10/31	PC89, PR114, PR105	Change VCC_core OCP and Loadline
EC-B-PWR-20	45	11/10/31	PR60	Change DGPU IMON resistor
EC-B-PWR-21	45	11/10/31	PR26, PR27, PR14, PR58	Change DGPU OCP resistors
EC-B-PWR-22	45	11/10/31	PC52, PC53, PR41	Improve function
EC-B-PWR-23	46	11/10/31	PQ7, PQ41	Improve function