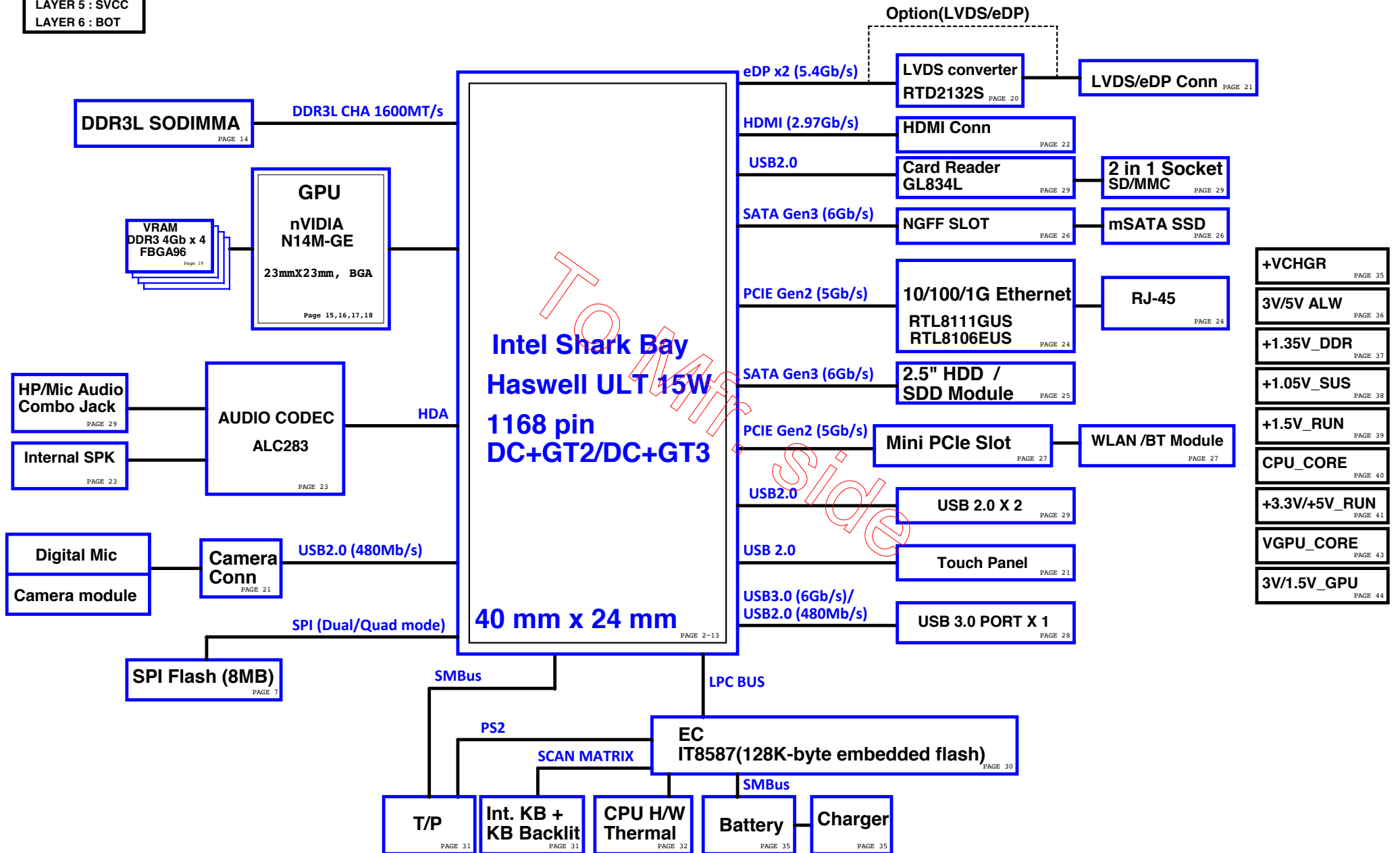
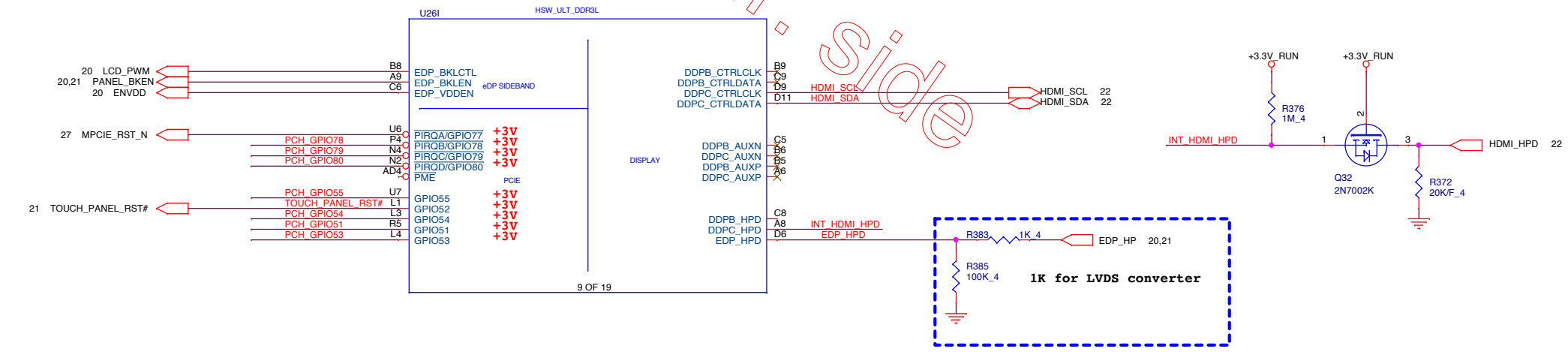
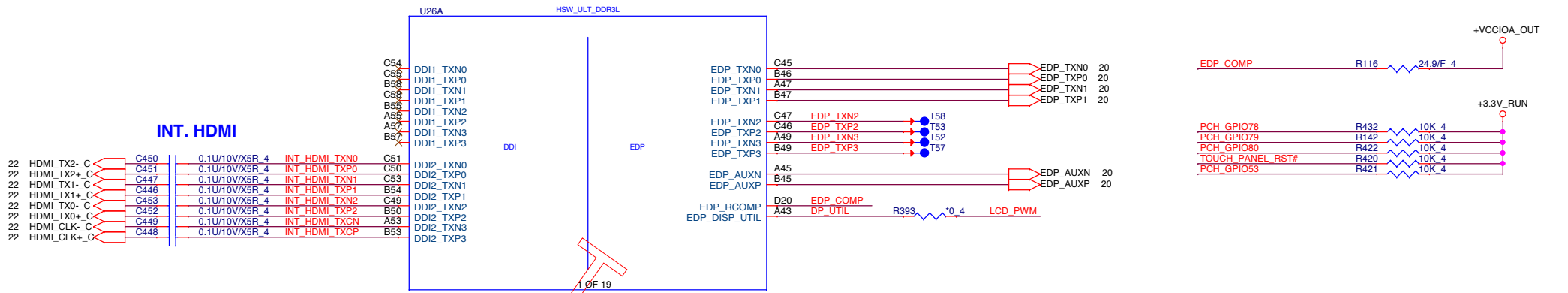


LAYER 1 : TOP  
 LAYER 2 : SGND  
 LAYER 3 : IN1  
 LAYER 4 : IN2  
 LAYER 5 : SVCC  
 LAYER 6 : BOT

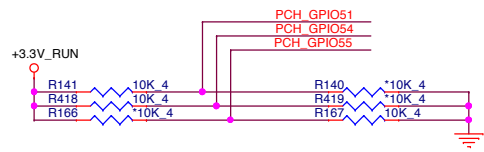
# ST6/6A 14" OPTIMUS INTEL SHARK BAY ULT ONE CHIP PLATFORM



### Haswell ULT (DISPLAY)



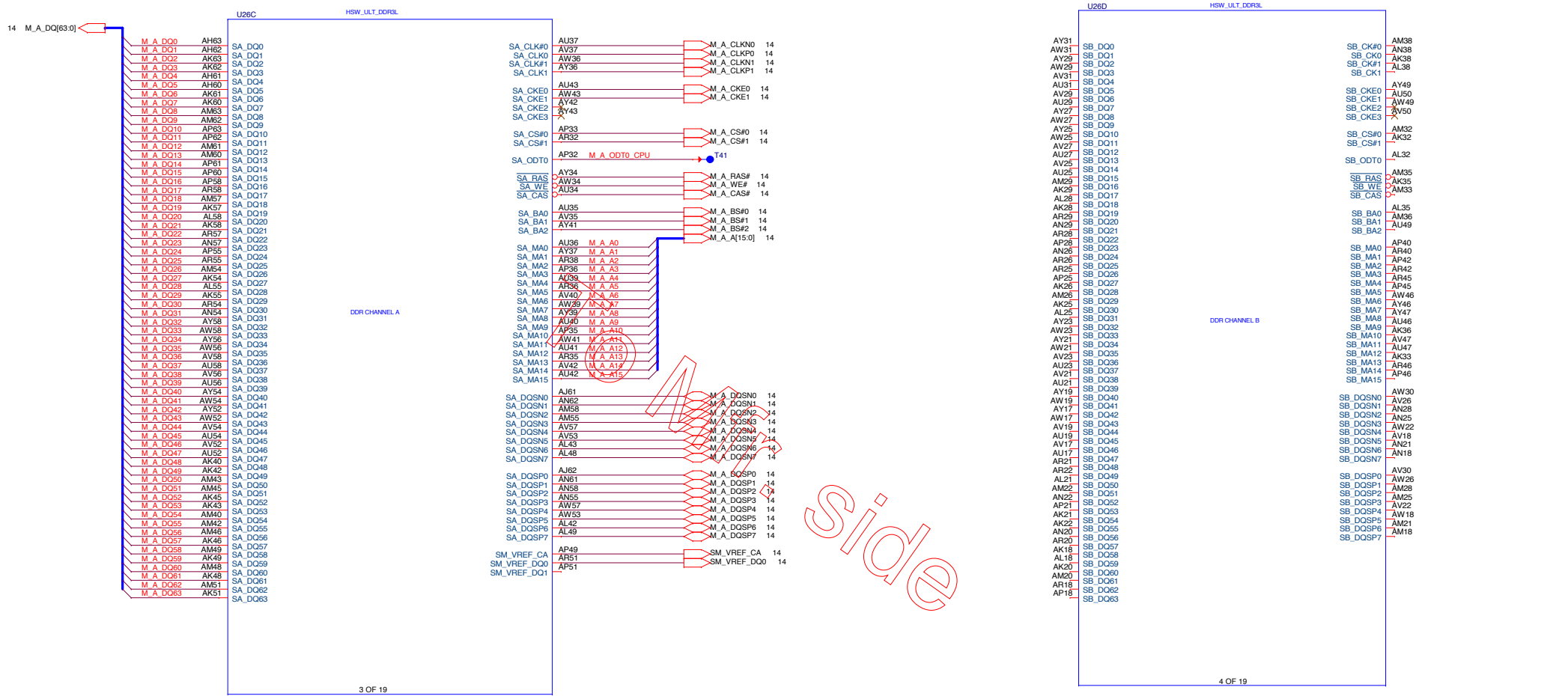
Board ID	GPIO51	GPIO54	GPIO55
SDV	1	1	1
SIV	1	1	0
SIT			
SVT			



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Haswell ULT (DDR3L)



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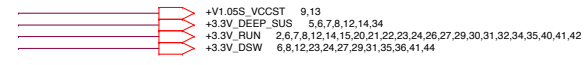
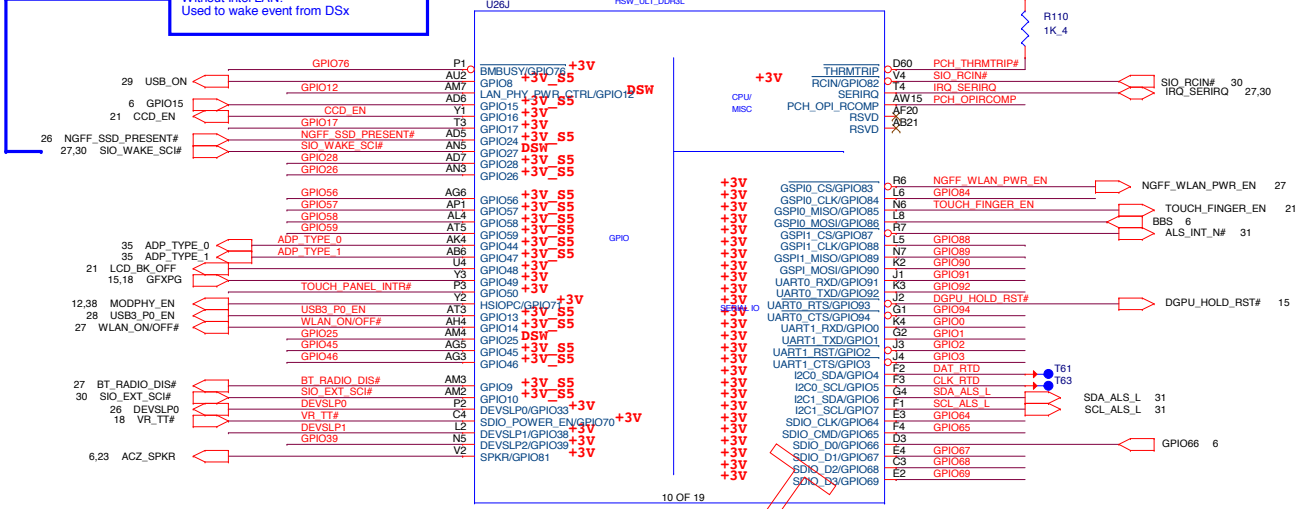
**PROJECT : ST6A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Haswell ULT 2/12</b>	1A
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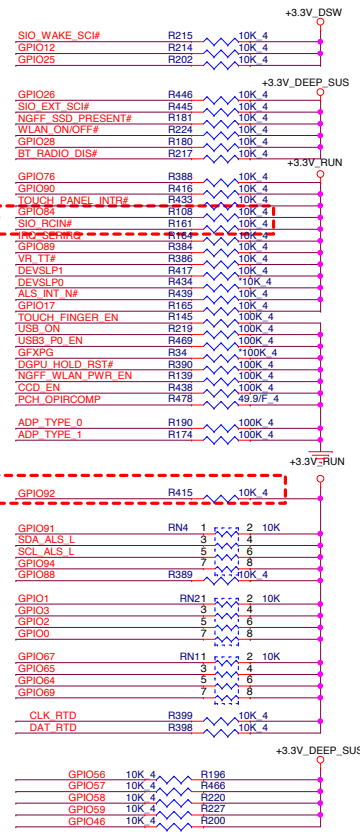
# Hasswell ULT (GPIO, LPIO, MISC)

## GPIO27

With Intel LAN:  
Connect to LANWAKE# pin on the LAN  
Without Intel LAN:  
Used to wake event from DsX



## GPIO Pull-up/Pull-down (CLG)



DGPU SELECT	GPIO39
UMA	1
DIS	0



Model ID	GPIO45
S14	0
S15	1



VRAM Freq.	GPIO68
1G	1
900M	0

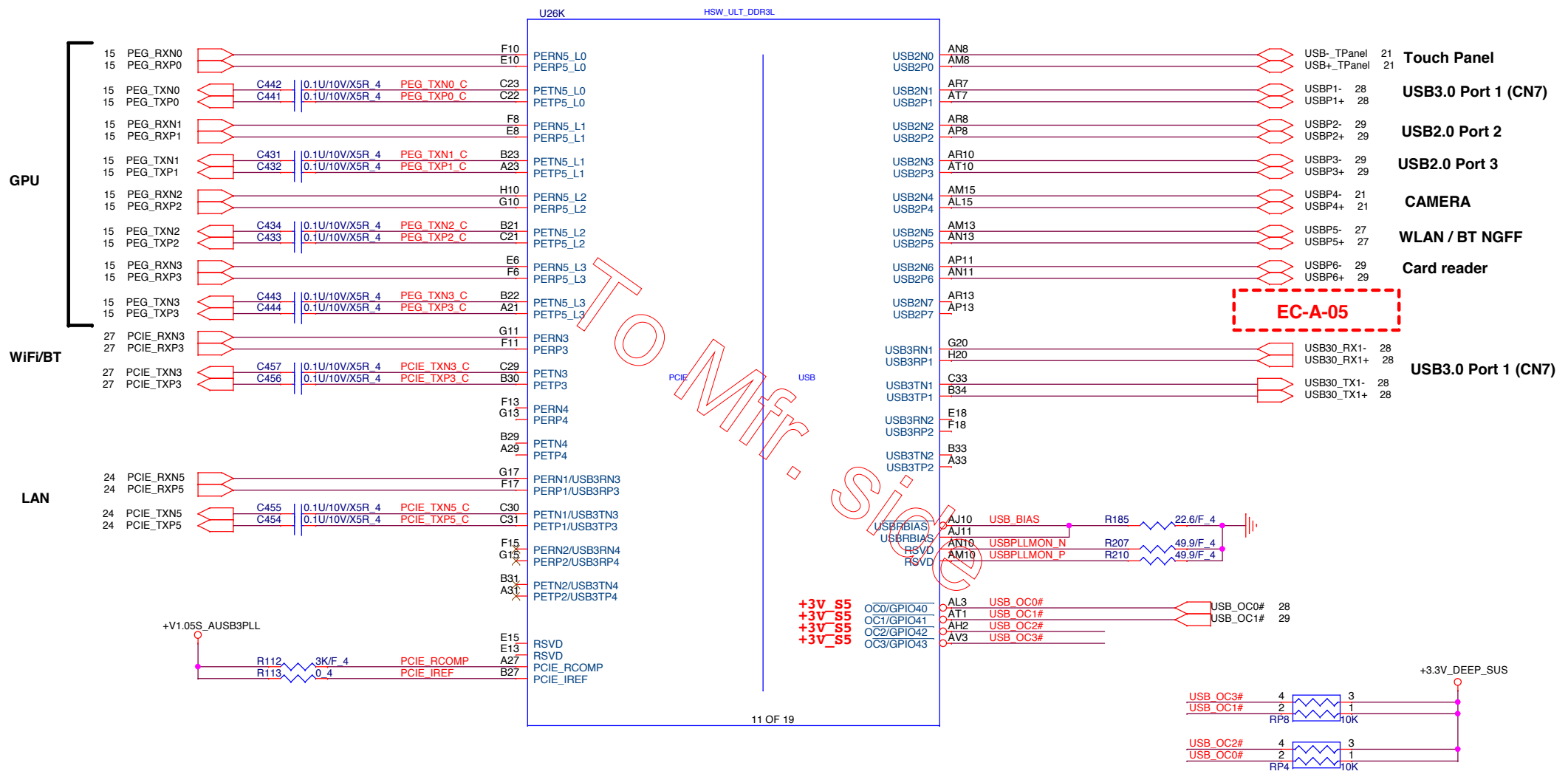


HW board ID to distinguish VRAM 900MHz & 1GHz

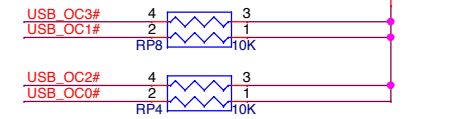
**PROJECT : ST6A**  
**Quanta Computer Inc.**

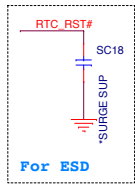
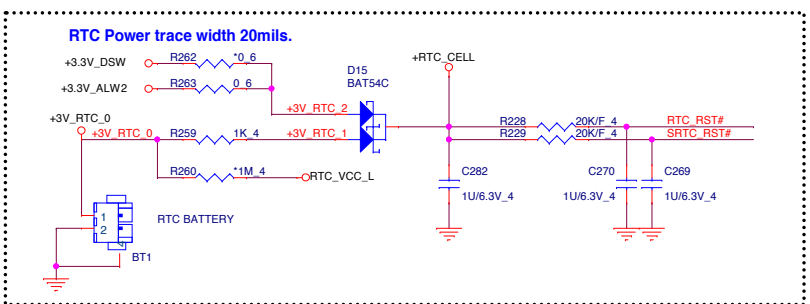
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# Haswell ULT (PCIE,USB)

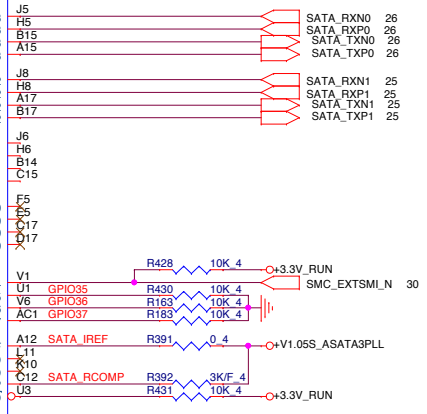
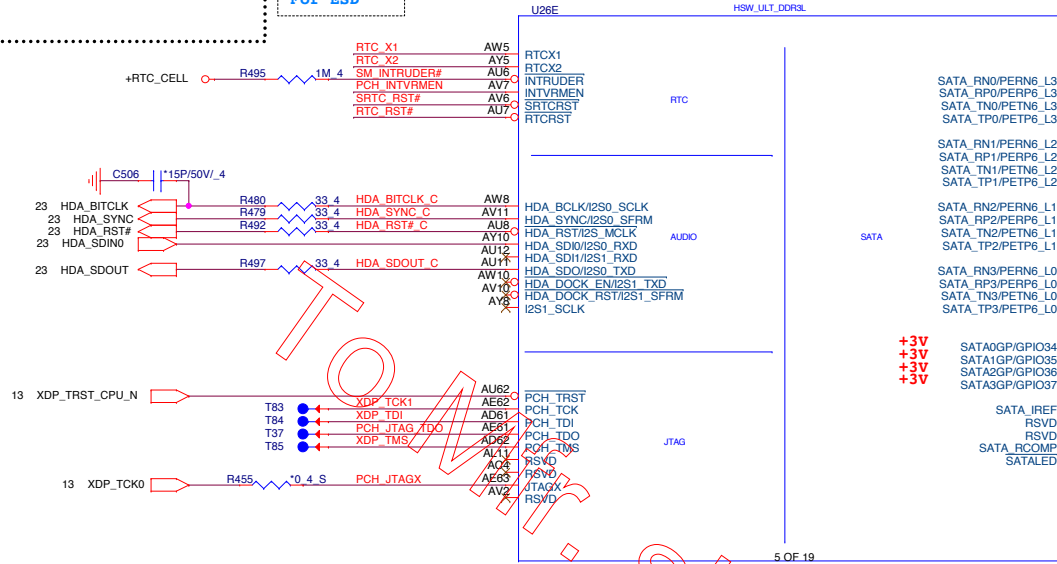
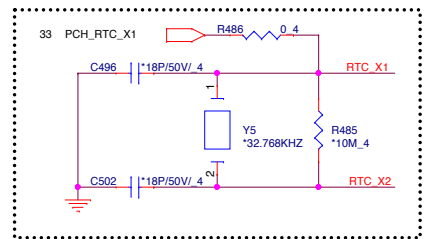


EC-A-05



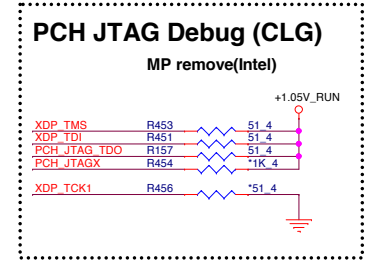


### Haswell ULT (RTC, HDA, JTAG, SATA)



### PCH Strap Table

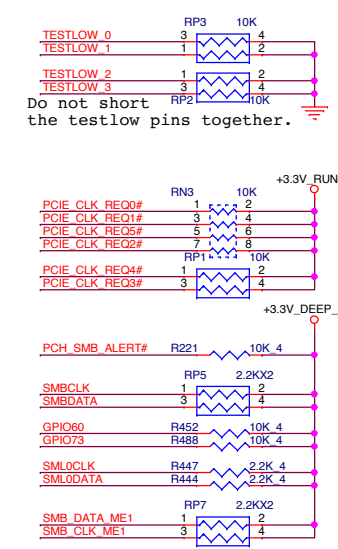
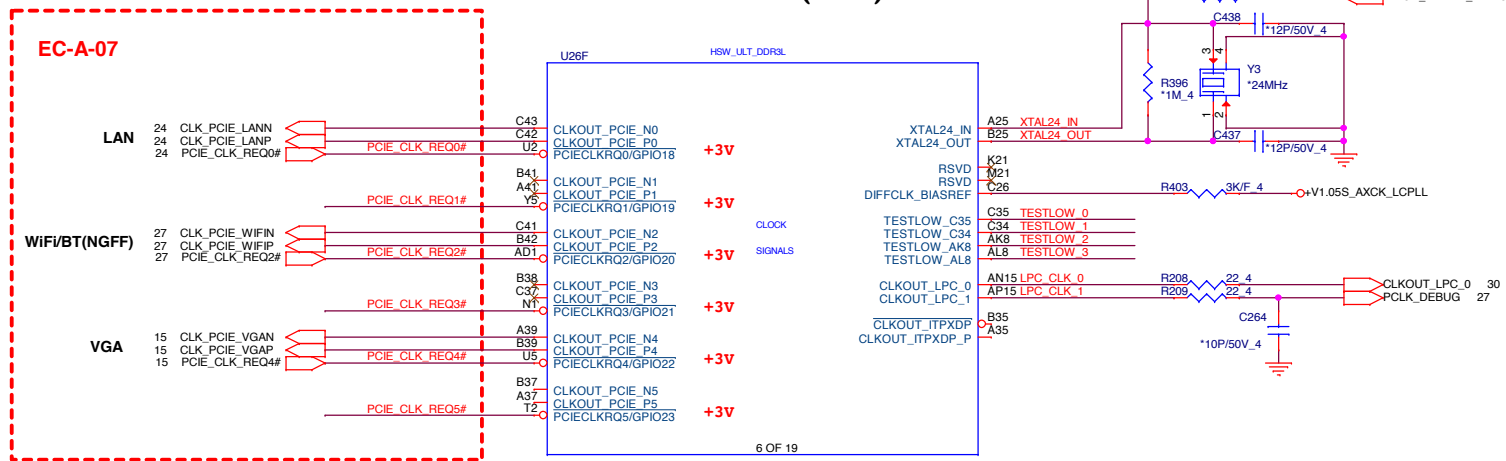
Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN → R429 → *1K → ACZ_SPKR 4,23
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	30 ME_WR# → R491 → *1K → HDA_SDOUT C
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	<b>Should be always pull-up</b>	+RTC_CELL → R493 → 330K → PCH_INTRVREN → R481 → *330K →
GPIO66	Top-Block Swap override		<b>0 = Default disable (iPD 20K)</b> 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO → R394 → *1K → GPIO66 4 R404 → *1K →
GPIO86	BBS(Boot BIOS Strap Bit)		<b>0 = Default SPI (iPD 20K)</b> 1 = LPC	+3.3V_RUN → R106 → *1K → BBS 4 R105 → *1K →
GPIO15	TLS(Transport layer security)		<b>0 = Default enable w/o confidentiality(iPD 20K)</b> 1 = Default enable with confidentiality	+3.3V_DEEP_SUS → R182 → *10K → GPIO15 4
DSWVREN	Deep Sx well on die DSW VR enable		<b>1=Should be always pull-up</b>	+RTC_CELL → R483 → 330K → DSWVRMEN 8



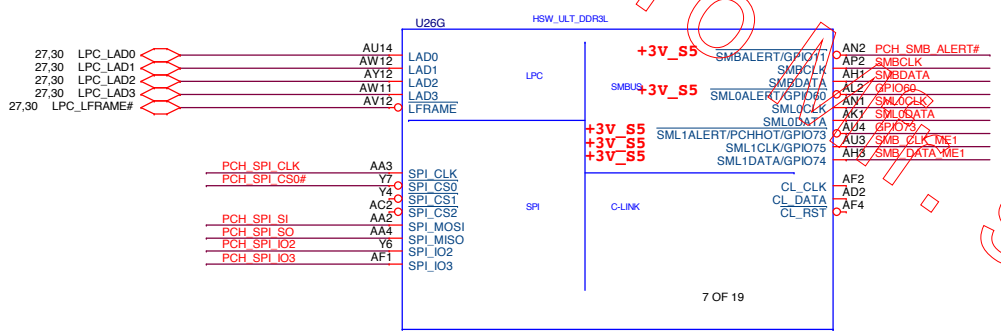
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**Quanta Computer Inc.**

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	<b>Haswell ULT 5/12</b>	1A
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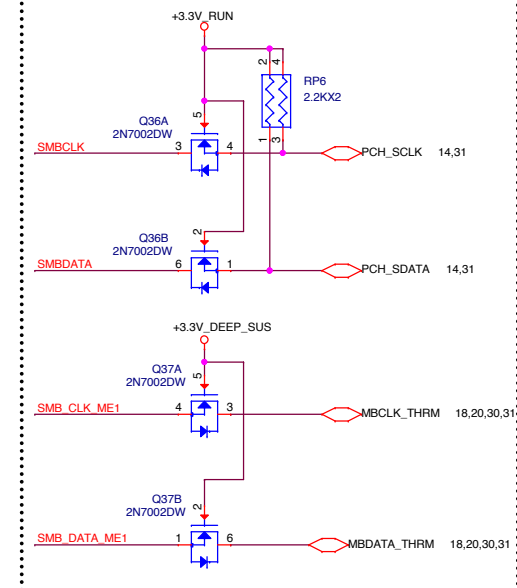
### Haswell ULT (CLK)



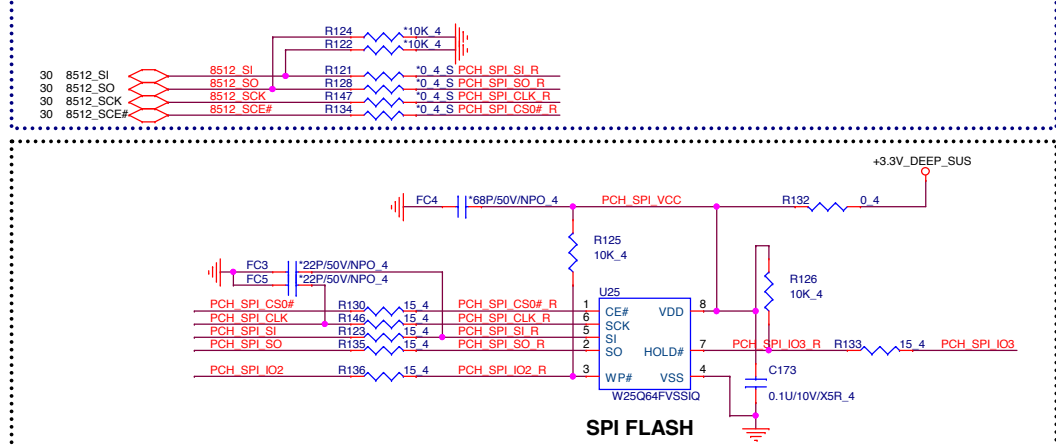
### Haswell ULT (LPC/SPI/SMB/CLINK)



### SMBus/Pull-up(CLG)

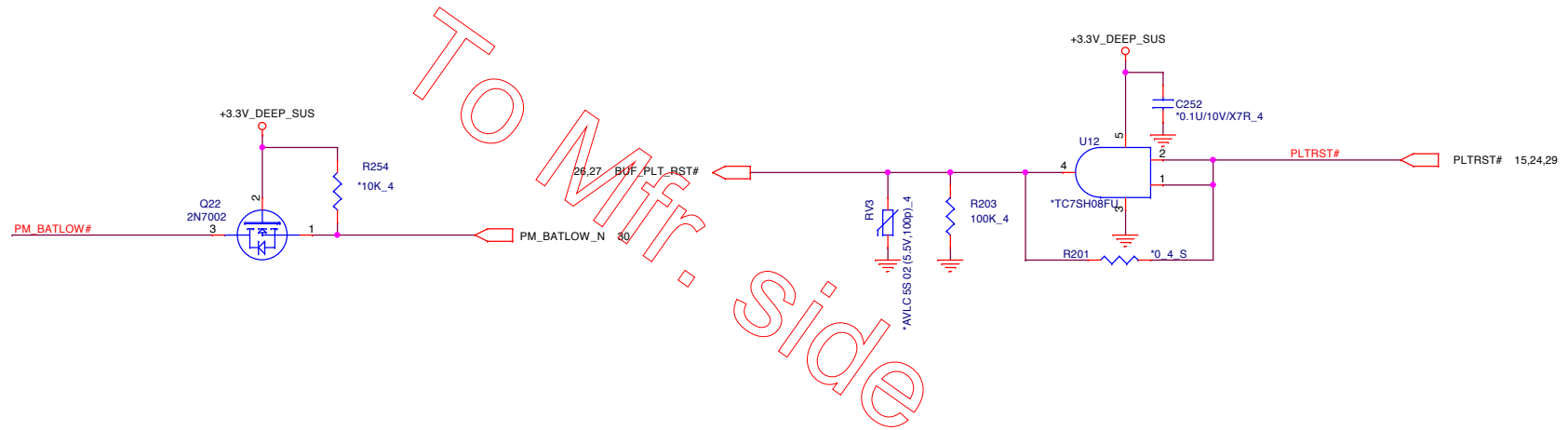
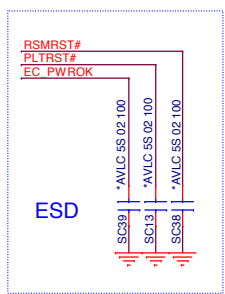
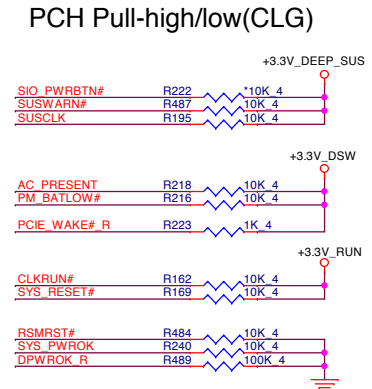
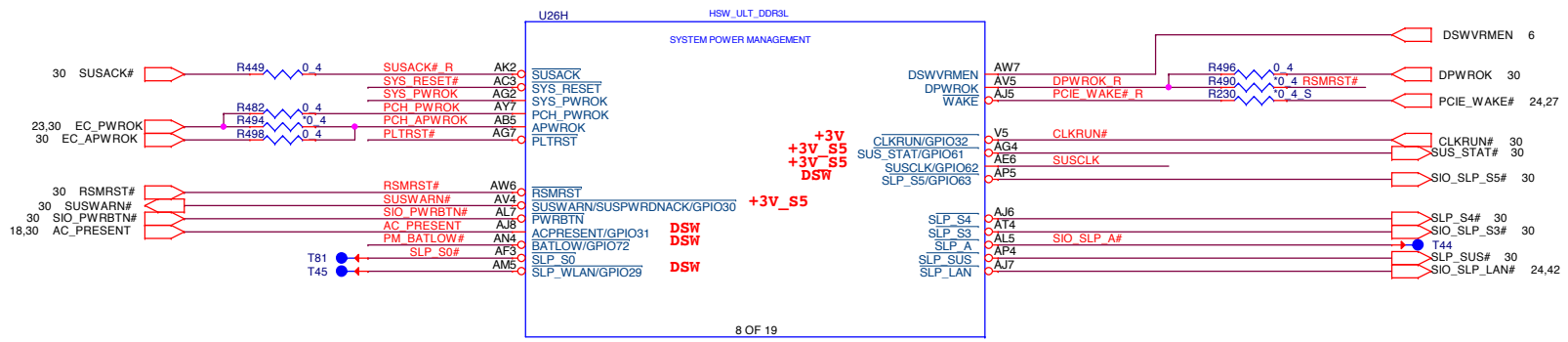


### For EC(IT8587 e-flash) load code from BIOS flash ROM

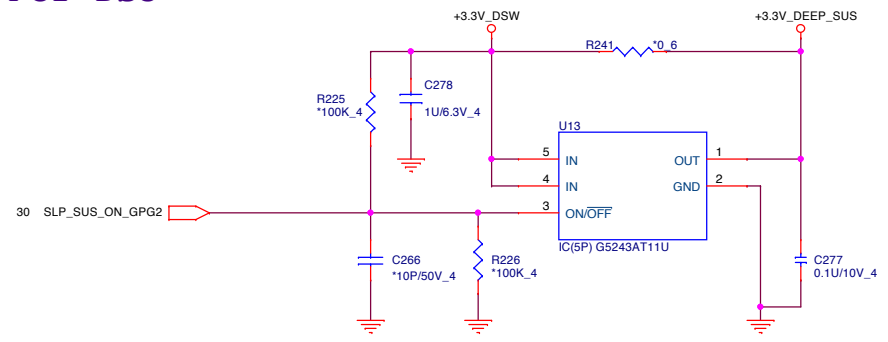


# Haswell ULT (SYSTEM POWER MANAGEMENT)

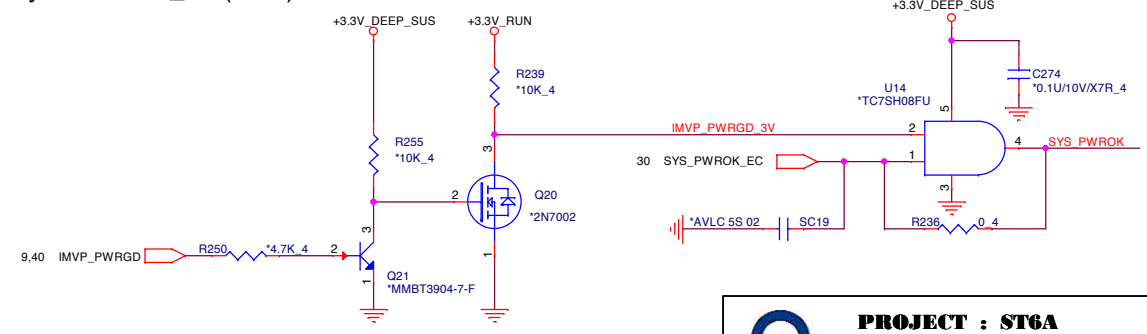
4,6,12,23,24,27,29,31,35,36,41,44 +3.3V\_DSW  
 2,4,6,7,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V\_RUN  
 4,5,6,7,12,14,34 +3.3V\_DEEP\_SUS



## For DS3



## System PWR\_OK (CLG)



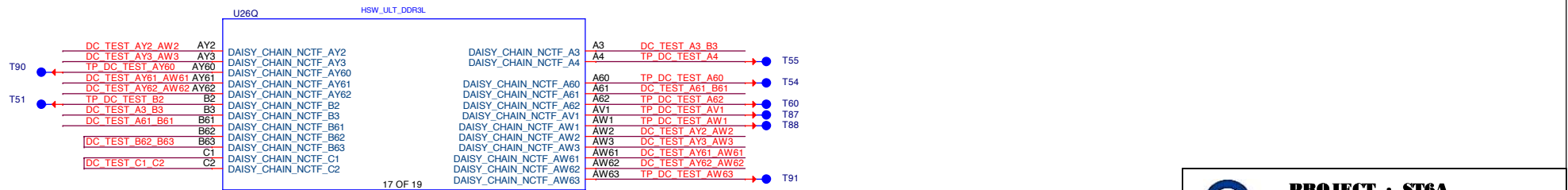
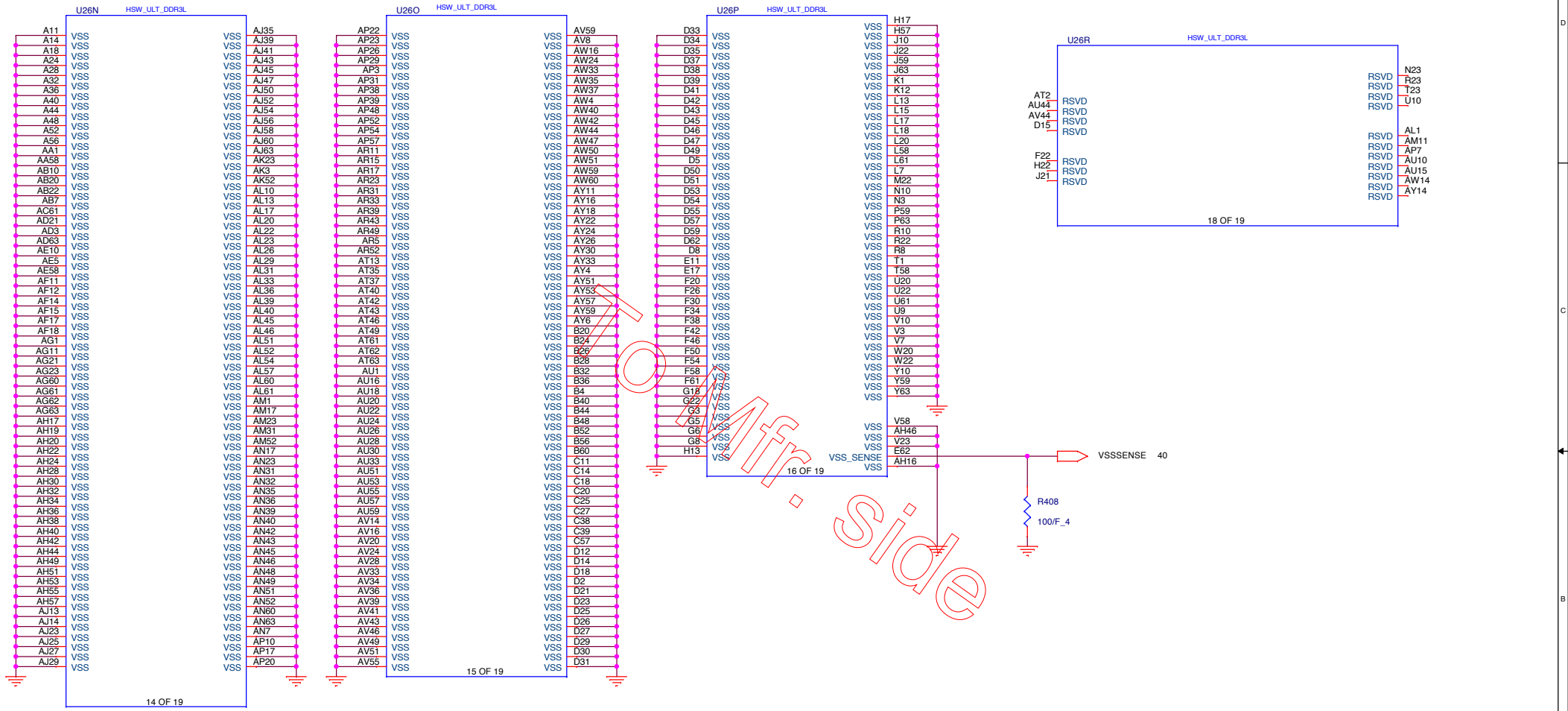
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**Quanta Computer Inc.**

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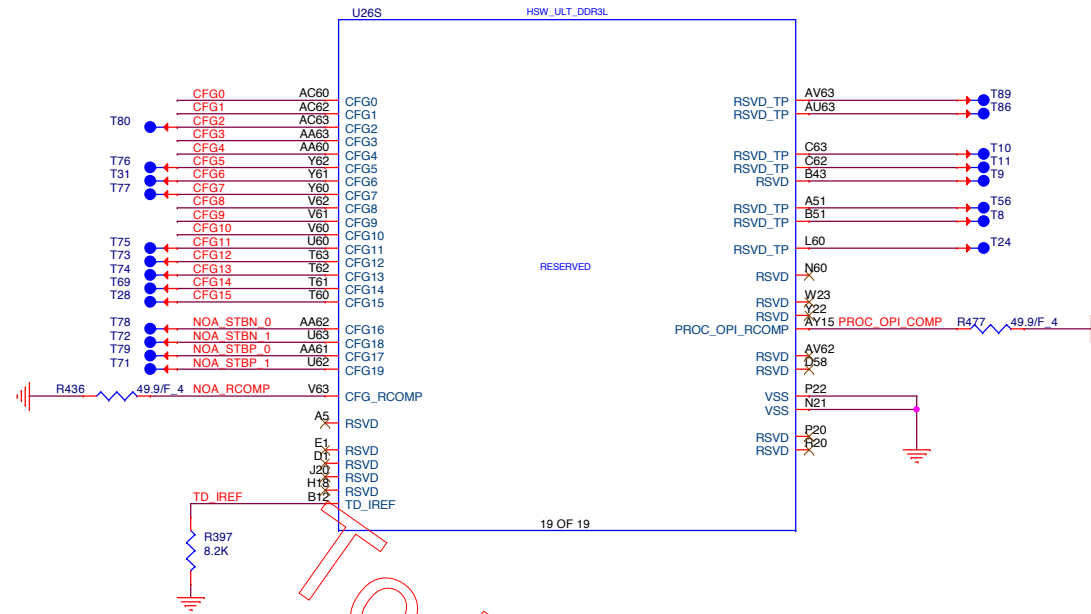


# Haswell ULT (GND)



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**Quanta Computer Inc.**

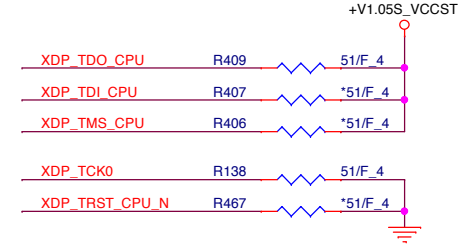
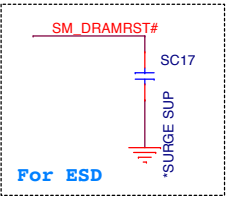
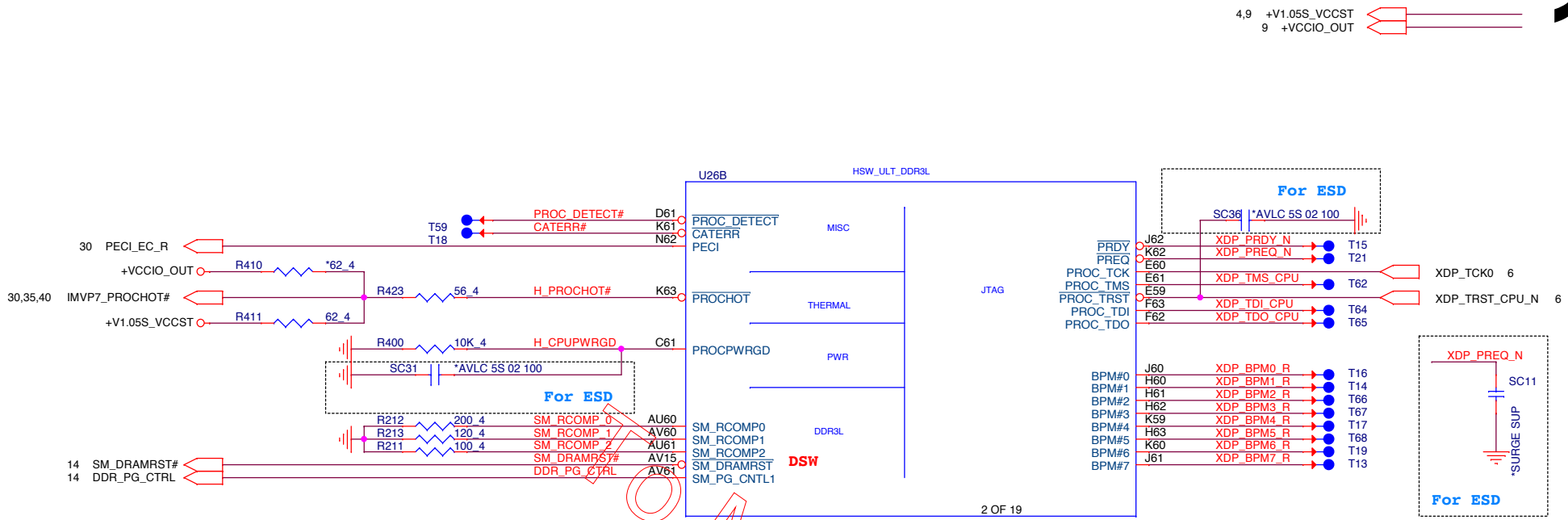
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## Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	

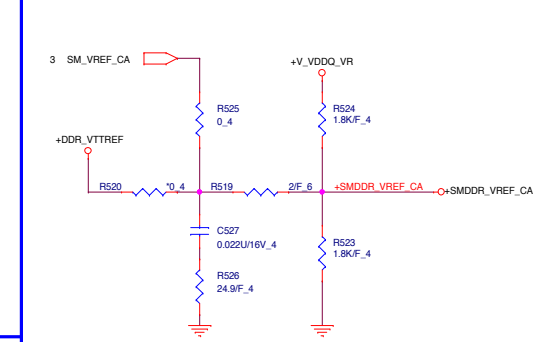
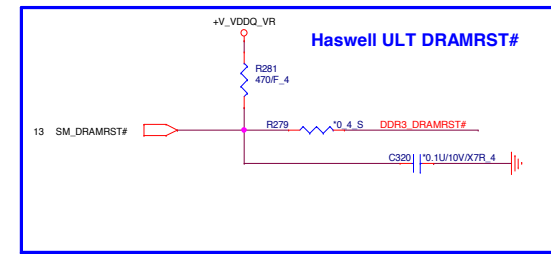
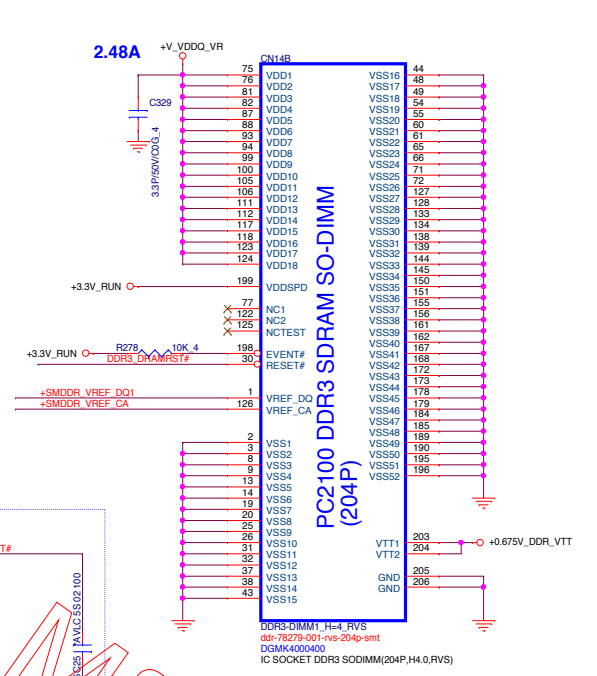
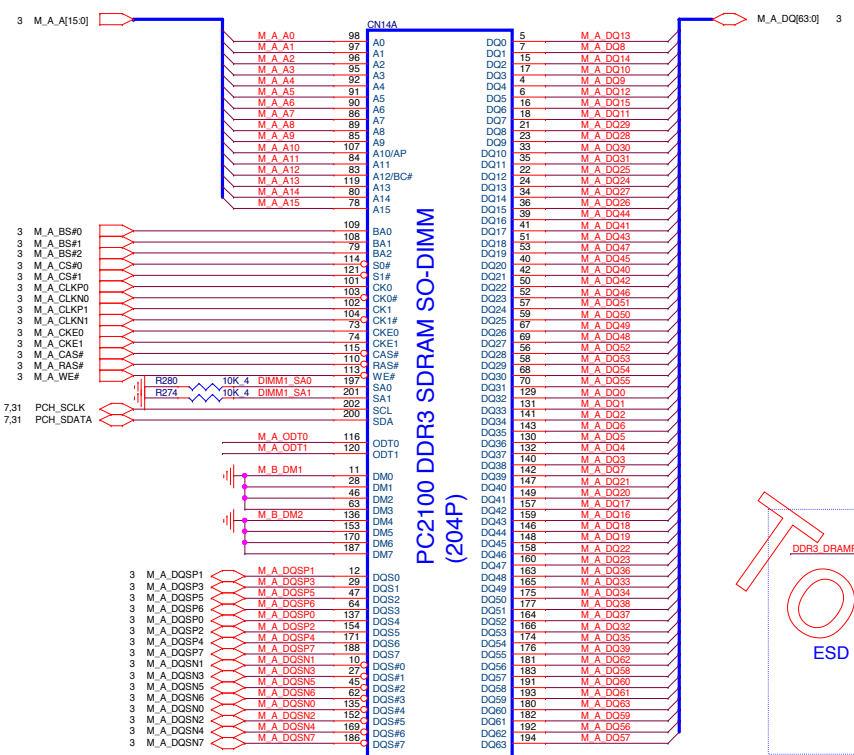




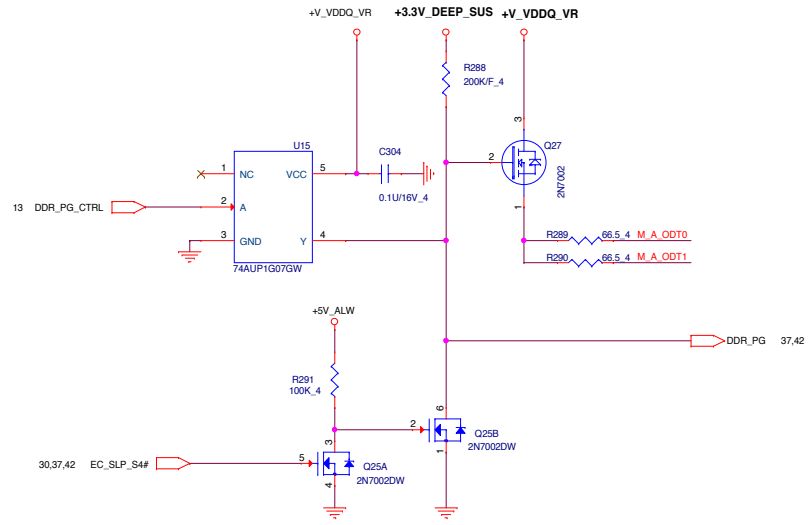
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**Quanta Computer Inc.**

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	<b>Haswell ULT 12/12</b>	1A
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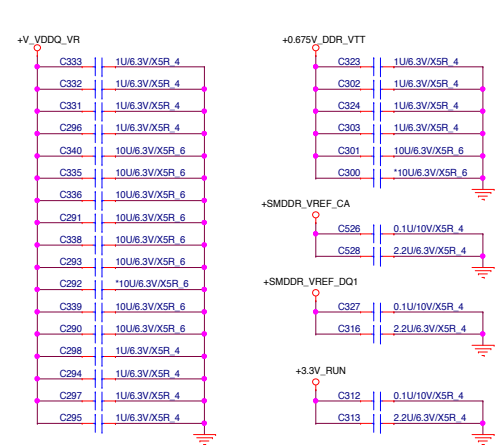
9,37,42 +V\_VDDQ\_VR  
2,4,6,7,8,12,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V\_RUN  
37,42 +0.675V\_DDR\_VTT +5V\_ALW  
12,28,29,35,36,37,38,39,41,42,43,44 +5V\_ALW  
4,5,6,7,8,12,34 +3.3V\_DEEP\_SUS  
37 +DDR\_VTTREF



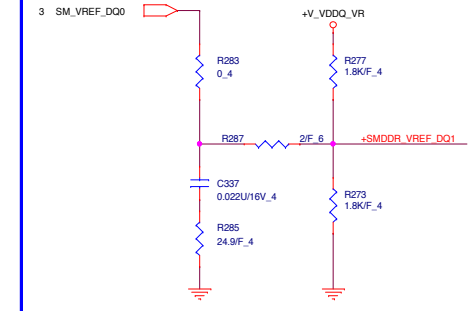
DDR3L SODIMM ODT DERATION



Place these Caps near So-Dimm1



VREF DQ1 Solution



<VGA>

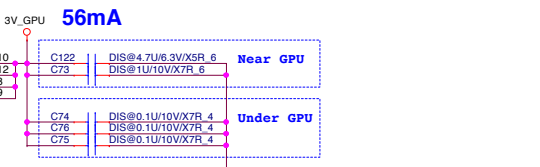
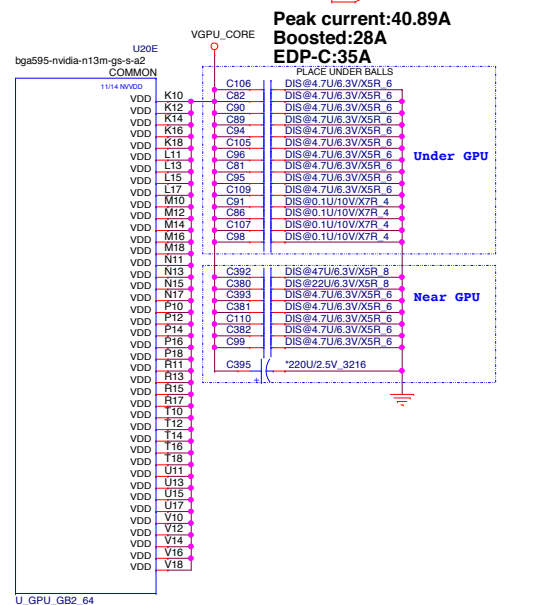
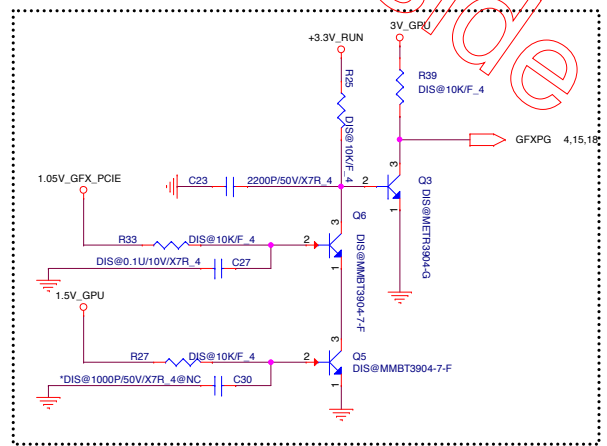
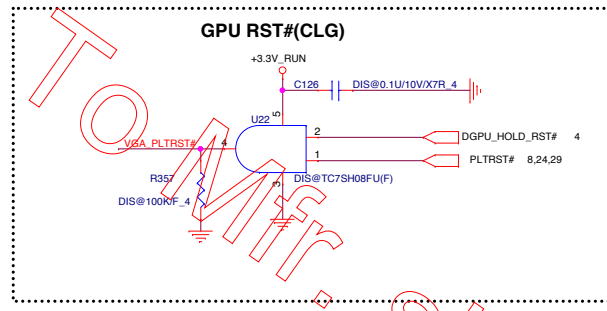
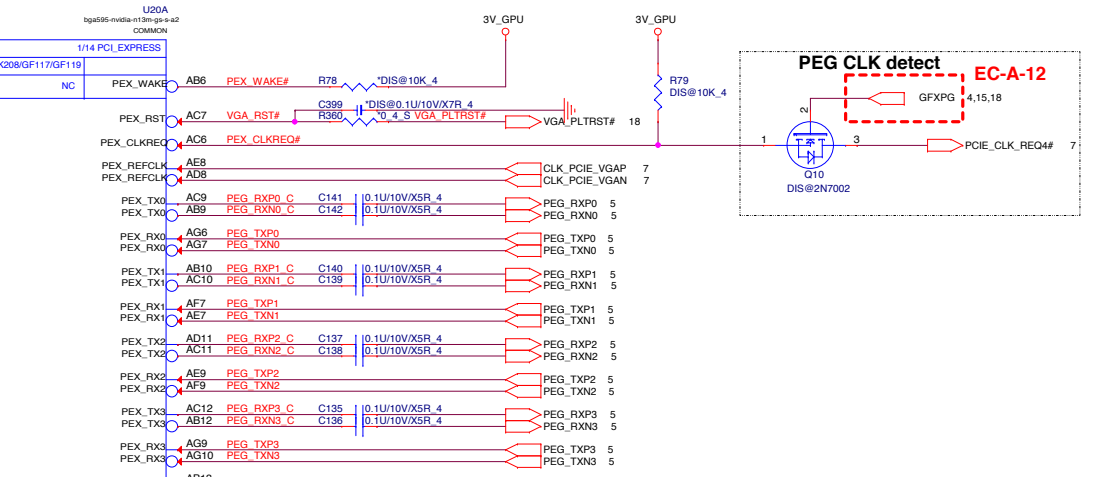
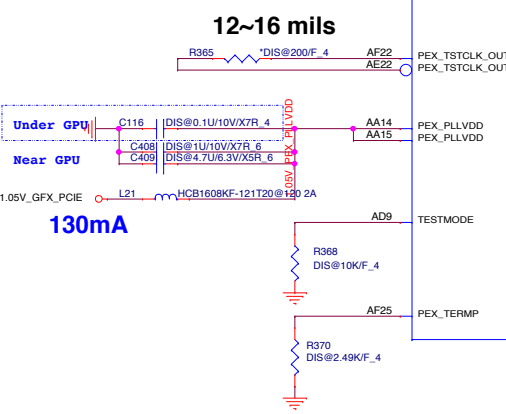
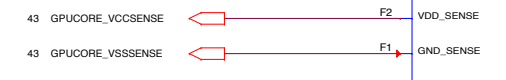
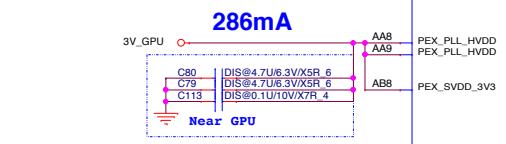
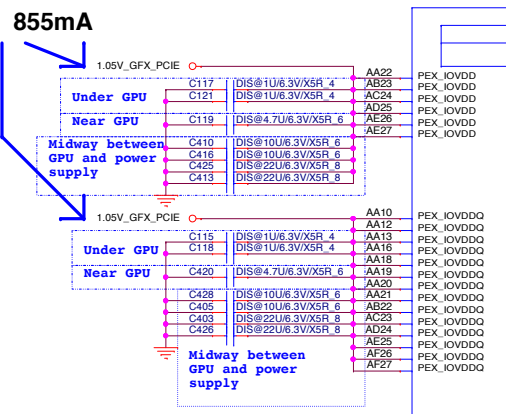
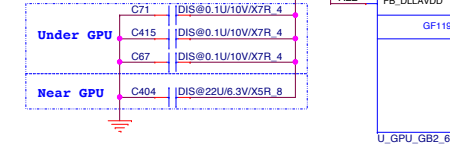
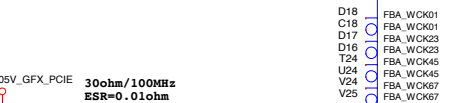
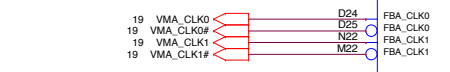
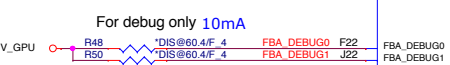
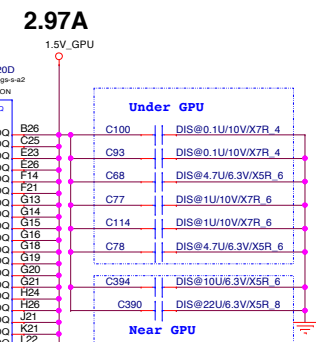
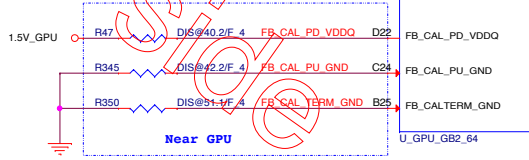
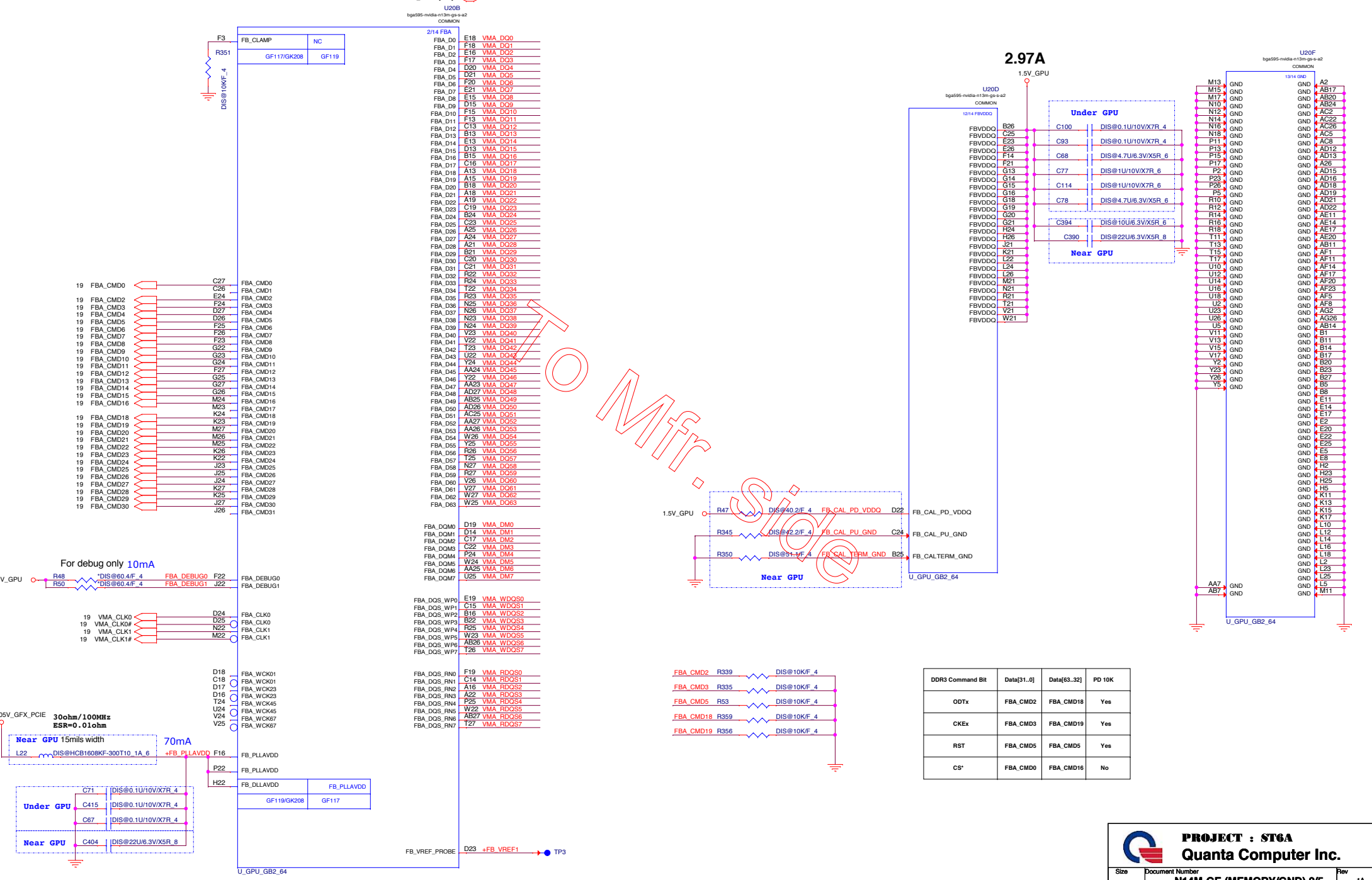
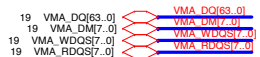


Table 2. GPU Power Rails

GPU Power Rail	Nominal Value	Comments
HWVDD	GPU SKU Specific	GPU Core power rail
FBVDD <sup>2</sup>	1.35 V or 1.5 V	VRAM Core power for Frame Buffer components
FBVDDQ <sup>2</sup>	1.35 V or 1.5 V	VRAM I/O and GPUs Frame Buffer I/O power rail
IFPX_IOVDD <sup>3</sup>	1.05 V or 3.3V	Power I/F blocks
IFPX_PLLVDD <sup>3</sup>	1.05 V or 3.3 V	Integrated Digital Display PLL Power Rails
PEX_IOVDD <sup>4</sup>	1.05 V	GPUs PCIe interface power rail
PEX_SVDD_3V3, PEX_PLL_HVDD	3.3	GPU PCIe PLL Power Rails
PEX_PLLVDD	1.05 V	GPU PCIe PLL Power Rails
FbX_PLL_AVDD	1.05 V or 3.3 V	Frame Buffer PLL Power Rail
FbX_DLL_AVDD (GB2-64 and GB4-128)	1.05 V	Frame Buffer PLL and DLL Power Rail
FbX_PLL_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLLVD, GPCPLL_AVDD, LXS_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
VID_PLLVDD	1.05 V	Video Pixel Clock PLL Analog Power Rail
SP_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
DAC_X_VDD <sup>1</sup>	3.3 V	Powers the DAC interfaces
VDD33(I/V3V3) <sup>1</sup>	3.3 V	Powers slower logic such as GPIOs, I2C, AUX channels and SLI

Notes: 1. The same power plane can be used for VDD33 and DAC\_X\_VDD.  
2. Voltage depends on memory type and SKU.  
3. Voltage depends on the I/F link (see Chapter 8, Digital Displays)  
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.



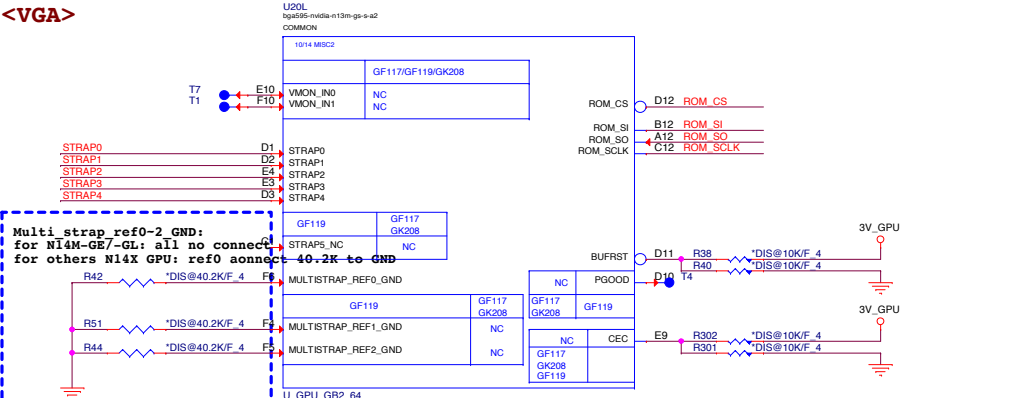
DDR3 Command Bit	Data[31:0]	Data[63:32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

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**Quanta Computer Inc.**

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	<b>N14M-GE (MEMORY/GND) 2/5</b>	1A
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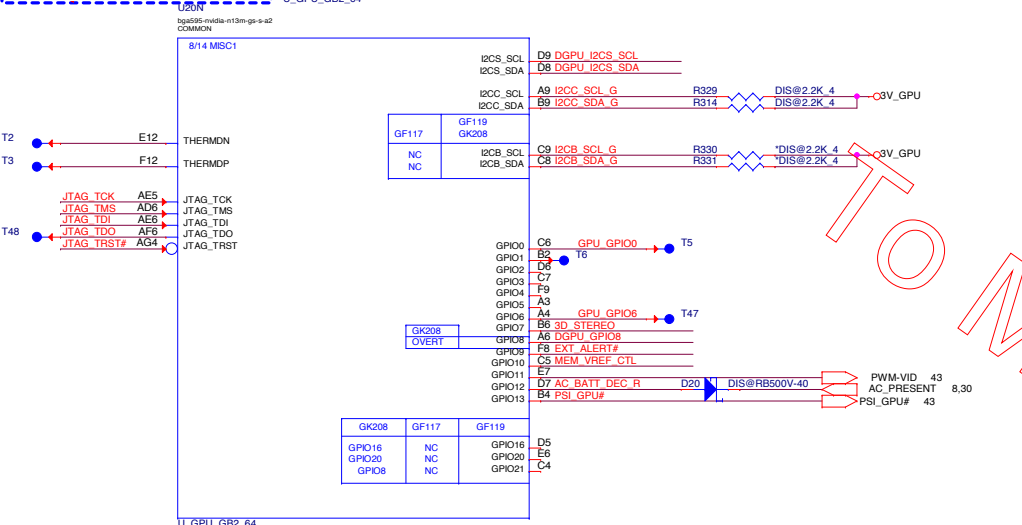




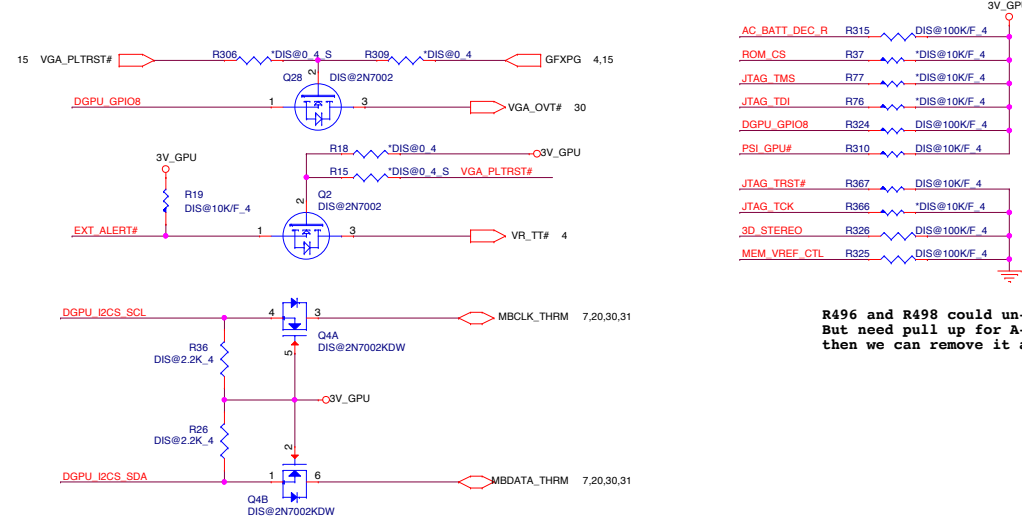
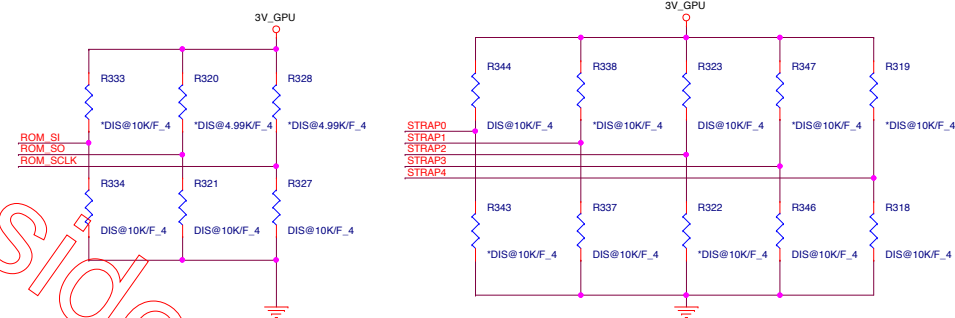


Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PGA_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0111



	Samsung	K4W2G1646E-BC1A	AKD5MGGT532
1GHz	Micron	MT41J128M16JT-093G:K	AKD5MGSTL15
	Hynix	Hynix 128x16 Vram H5TC2G63FFR-11C	AKD5MZDTW04
900MHz	Samsung	K4W4G1646B-HC11	AKD5MGWT516
	Micron	MT41K256M16HA-107G:E	AKD5PGSTL00



R496 and R498 could be un-stuff for cost saving. But need pull up for A-build, if no problem then we can remove it at next build.

Item	Value
Device ID	097970
Package	GBA130F8R-A4
Internal P/N	GF117_28nm
ROM_SI	10kOhm pull down
ROM_SO	10kOhm pull down
ROM_SCLK	10kOhm pull down
Strap0	
Strap1	
Strap2	
Strap3	
Strap4	10kOhm pull down
Open_VREG_SKU	Config C
DDVDD Boost Voltage	0.9V

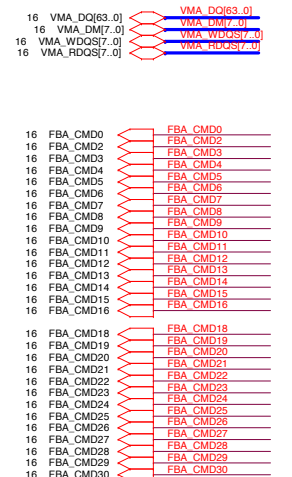
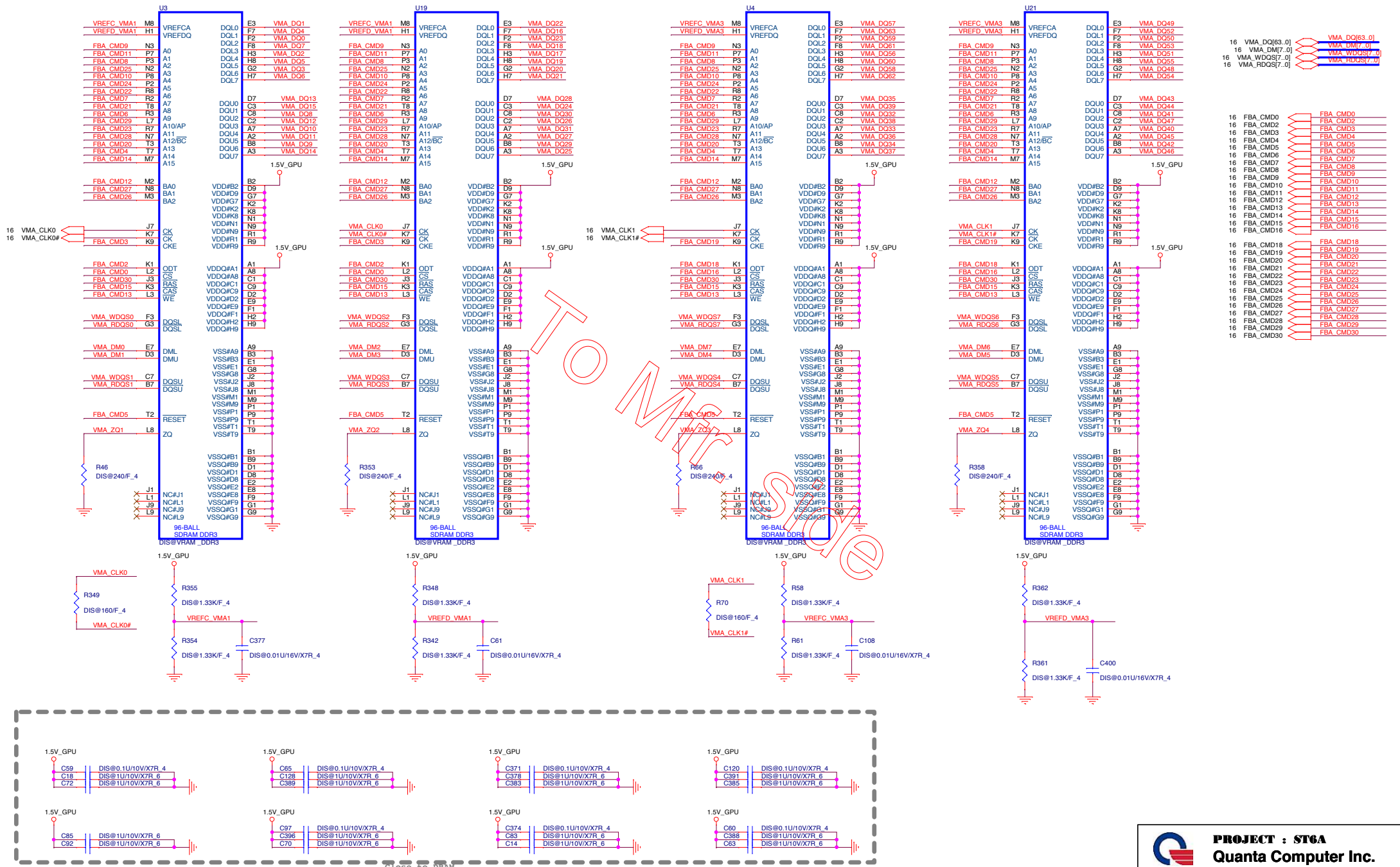
GPU SKU	GPU	VRAM Vendor	Type	Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	Strap 1	Strap 2	Strap 3	Strap 4	Status	
GF117	N14M-GE/GL	Micron	DDR3	1.5V/1.5V	128Mx16	1000MHz	1204	0x1	PO 10K	PO 10K	PO 10K	PU 10K	Production ready	
						900MHz	1150	0x1	PO 10K	PO 10K	PO 10K	PU 10K	Production ready	
		Samsung	DDR3	1.5V/1.5V	128Mx16	1000MHz	K4W2G1646E-BC1A	1204	0x5	PO 10K	PU 10K	PO 10K	PU 10K	Production ready
						900MHz	K4W2G1646E-BC11	1204	0x5	PO 10K	PU 10K	PO 10K	PU 10K	Production ready
		Hynix	DDR3	1.5V/1.5V	128Mx16	1000MHz	H5TQ2G63FFR-10K	1204	0x6	PO 10K	PU 10K	PO 10K	PU 10K	Production ready
						900MHz	H5TQ2G63DFR-11C	1204	0x6	PO 10K	PU 10K	PO 10K	PU 10K	Production ready
		Hynix	DDR4	1.5V/1.5V	128Mx16	1000MHz	H5TC2G63FFR-11C	1204	0x6	PO 10K	PU 10K	PO 10K	PU 10K	Post-production candidate
						900MHz	H5TC2G63FFR-11C	1204	0x6	PO 10K	PU 10K	PO 10K	PU 10K	Post-production candidate
		Samsung	DDR3	1.5V/1.5V	256Mx16	900MHz	K4W4G1646B-HC11	1204	0x4	PO 10K	PU 10K	PO 10K	PU 10K	
						900MHz	MT41K256M16HA-107G:E	1204	0x4	PO 10K	PU 10K	PO 10K	PU 10K	
		Hynix	DDR3	1.5V/1.5V	256Mx16	900MHz	H5TQ4G63MFR-11C	1204	0x3	PO 10K	PU 10K	PO 10K	PU 10K	
						900MHz	H5TQ4G63MFR-11C	1204	0x3	PO 10K	PU 10K	PO 10K	PU 10K	
Hynix	DDR3	1.5V/1.5V	256Mx16	900MHz	H5TQ4G63MFR-11C	1204	0x4	PO 10K	PU 10K	PO 10K	PU 10K			
				900MHz	H5TQ4G63MFR-11C	1204	0x4	PO 10K	PU 10K	PO 10K	PU 10K			

**PROJECT : ST6A**  
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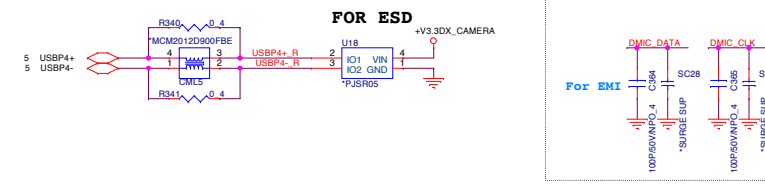
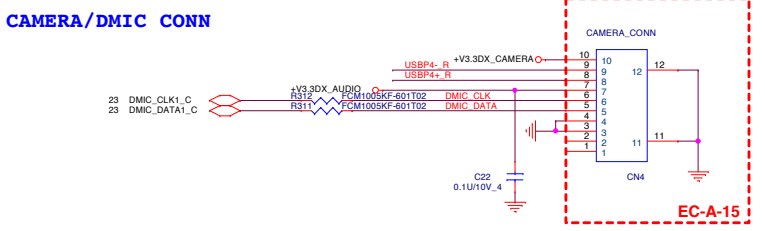
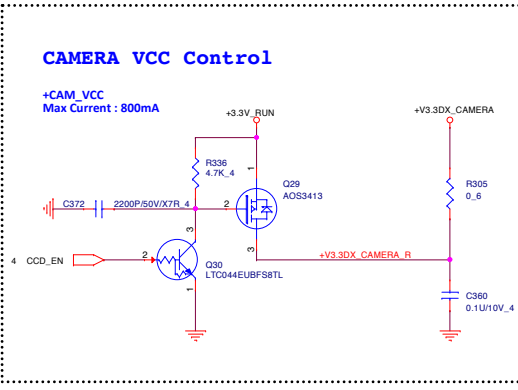
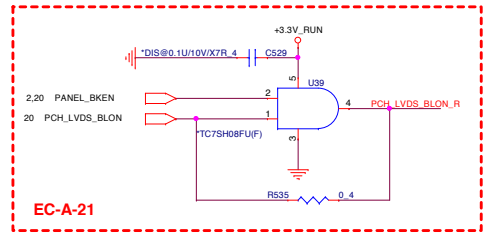
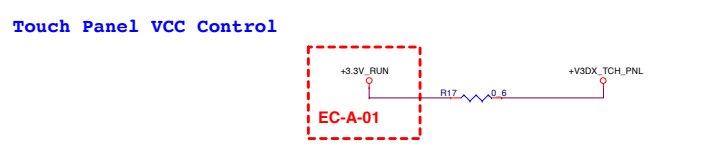
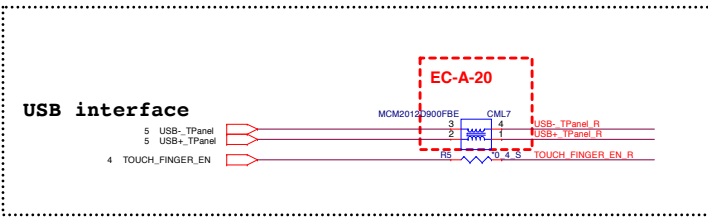
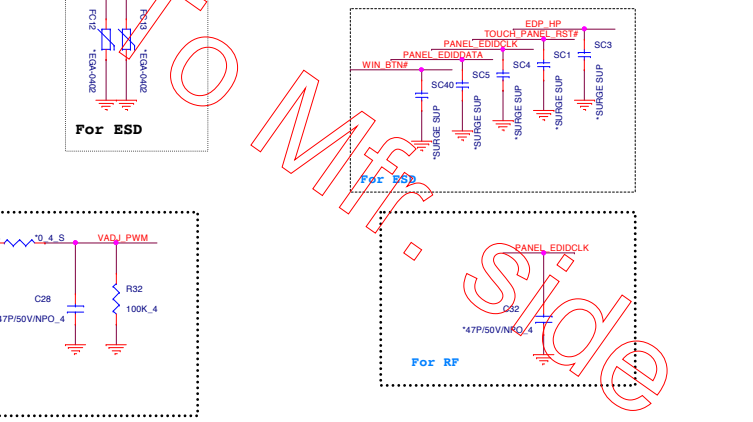
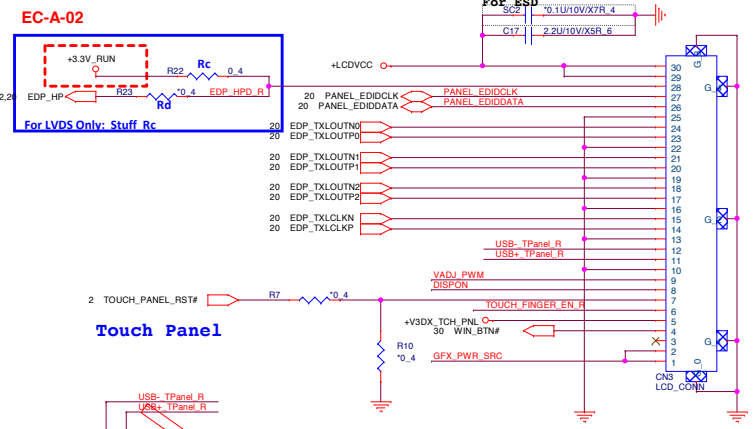
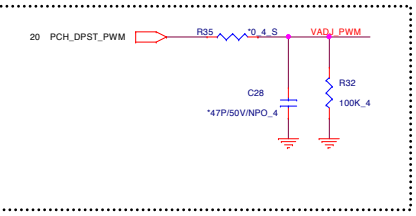
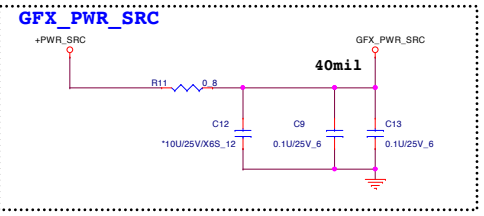
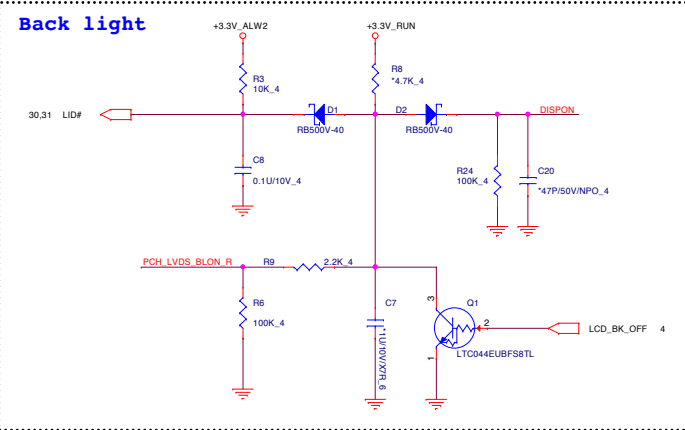
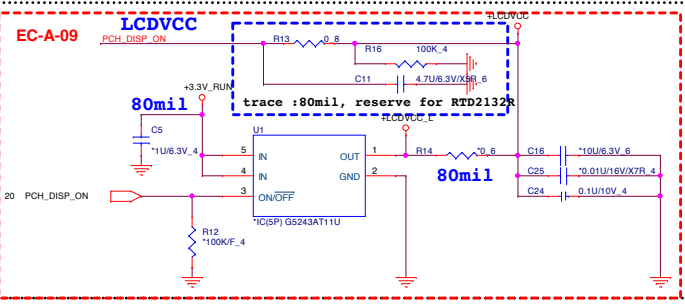
Size Document Number  
**N14M-GE (GPIO/STRAPS) 4/5** Rev 1A

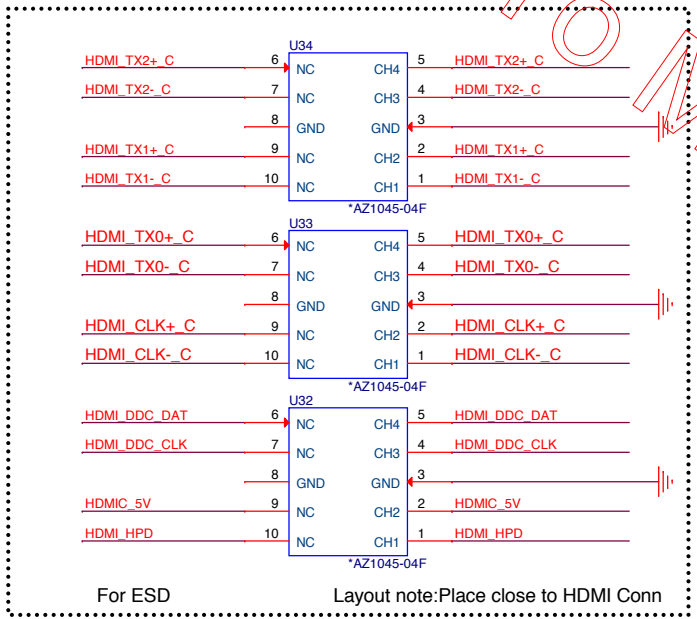
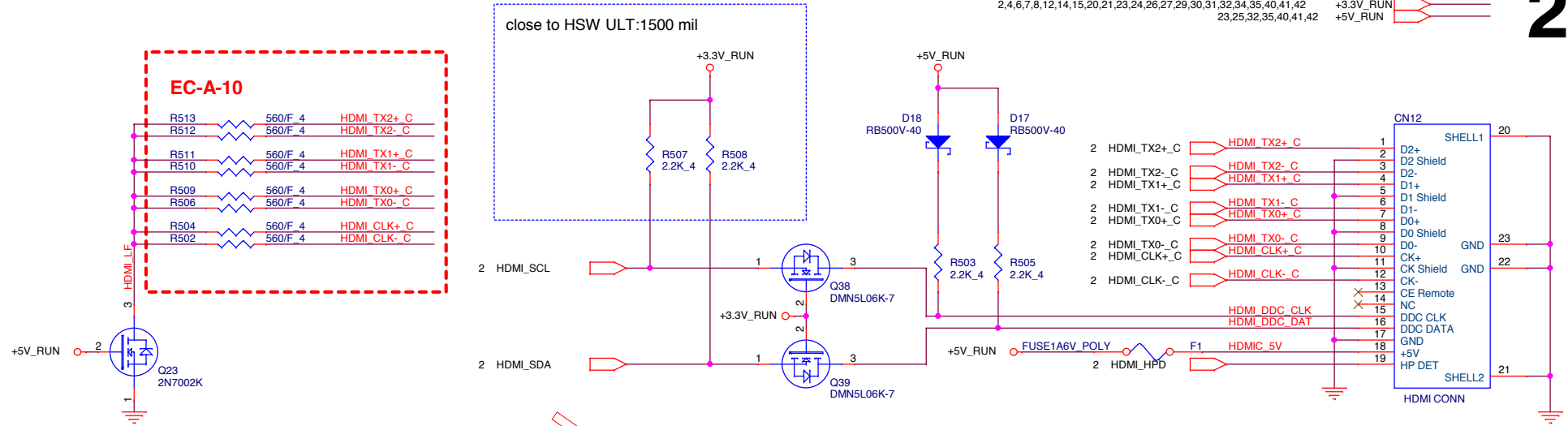
Date: Monday, April 01, 2013 Sheet 18 of 46

# CHANNEL A: DDR3 4Gb x4 Double T Topology for DDR3 Memory

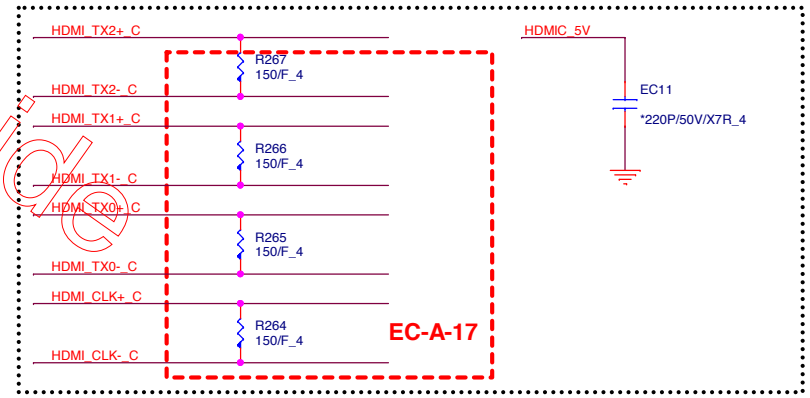




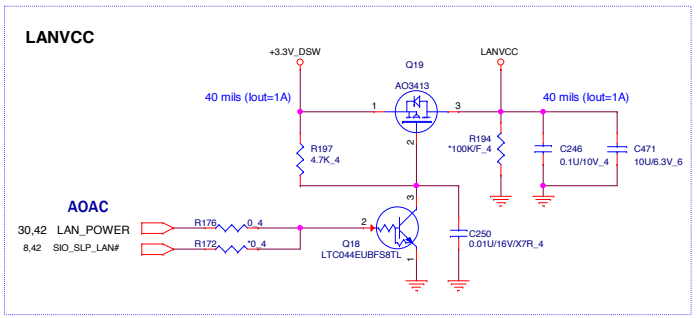




EMI reserve for HDMI



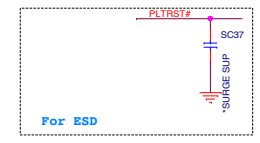
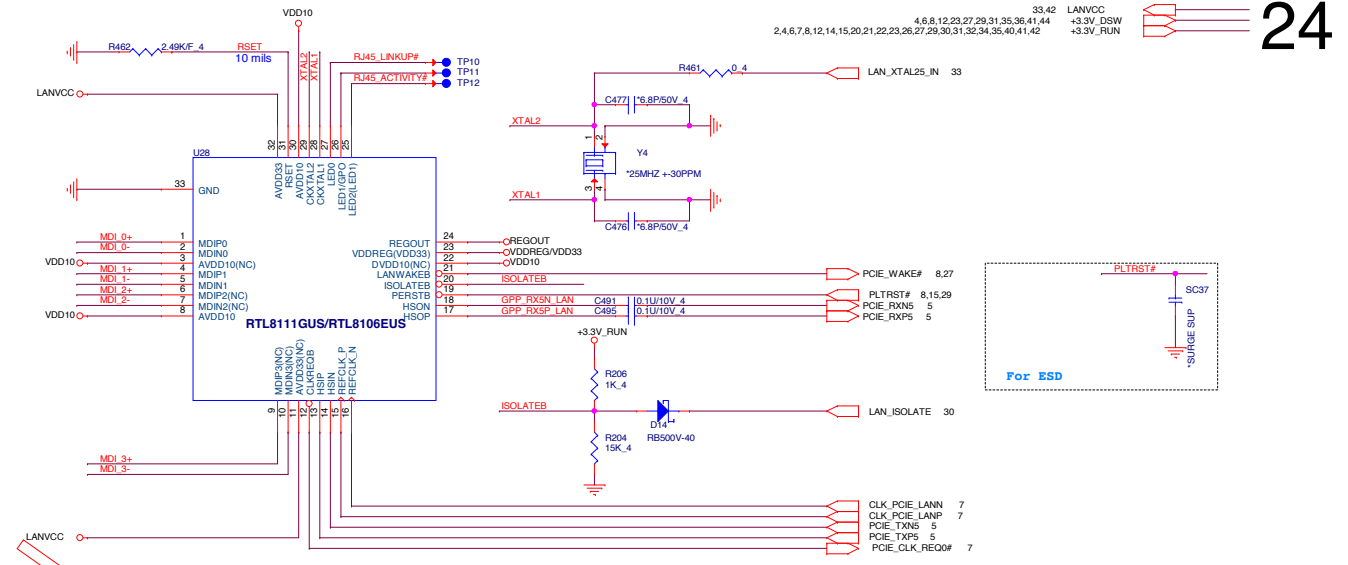




LANVCC  
Trace width>60mil,  
Trace length<200mil

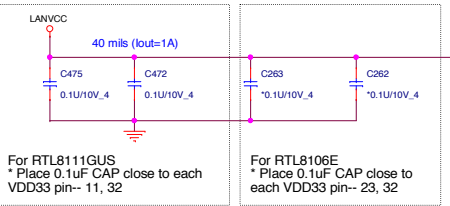
B-stage only 10/100 config.

10/100	RTL8106EUS-CG	AL008106002
1G	RTL8111GUS-CG	AL008111009



For RTL8106E  
\* Place 1uF CAP close to each VDD10 pin-- 30 (reserve)

For RTL8111GUS  
\* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30 For RTL8106E  
\* Place 0.1uF CAP close to each VDD10 pin-- 8, 30  
40 mils (out=1A)



For RTL8111GUS  
\* Place 0.1uF CAP close to each VDD33 pin-- 11, 32

For RTL8106E  
\* Place 0.1uF CAP close to each VDD33 pin-- 23, 32

Remove For Not Using SWR mode  
\* Place close to pin 23

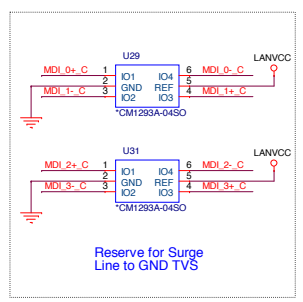
RTL8111G (LDO mode) support  
RTL8106E (LDO mode) doesn't need

RTL8111GUS (SWR mode) support

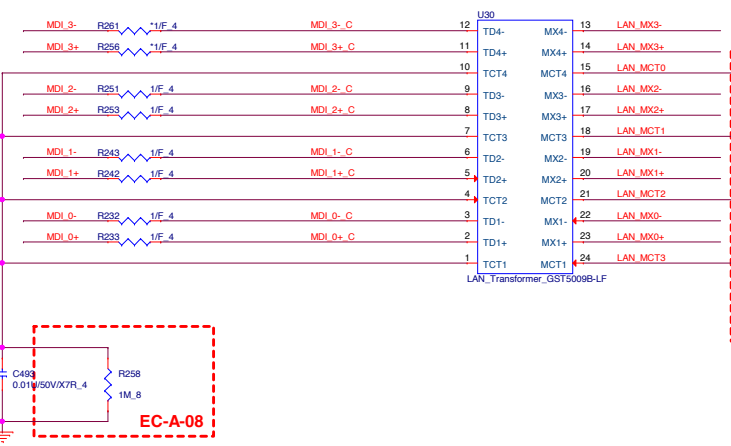
For RTL8111GUS  
\* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

TOMAF Side

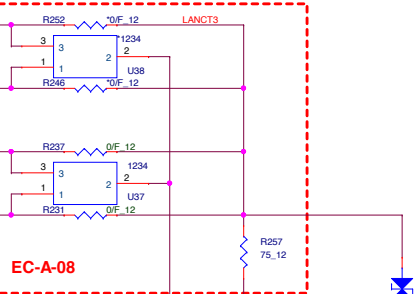
Transformer



Reserve for Surge Line to GND TVS

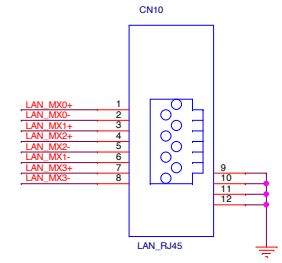


Layout: All termination signal should have 50 mil trace / 50mil spacing

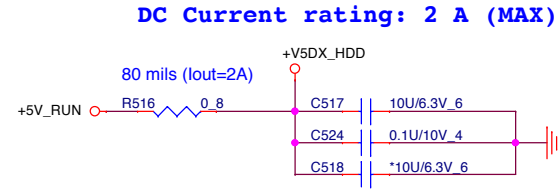
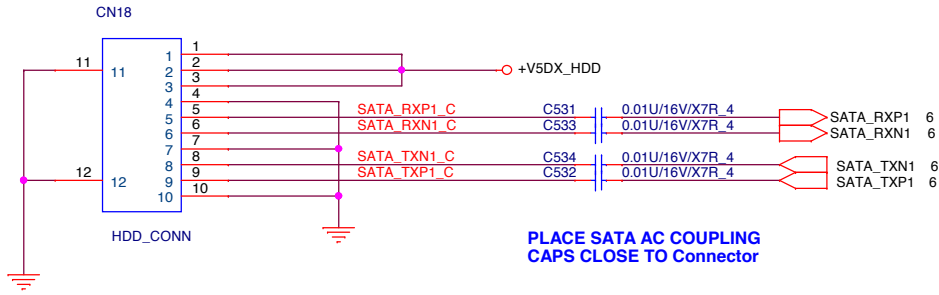


EC-A-08


RJ45 Connector





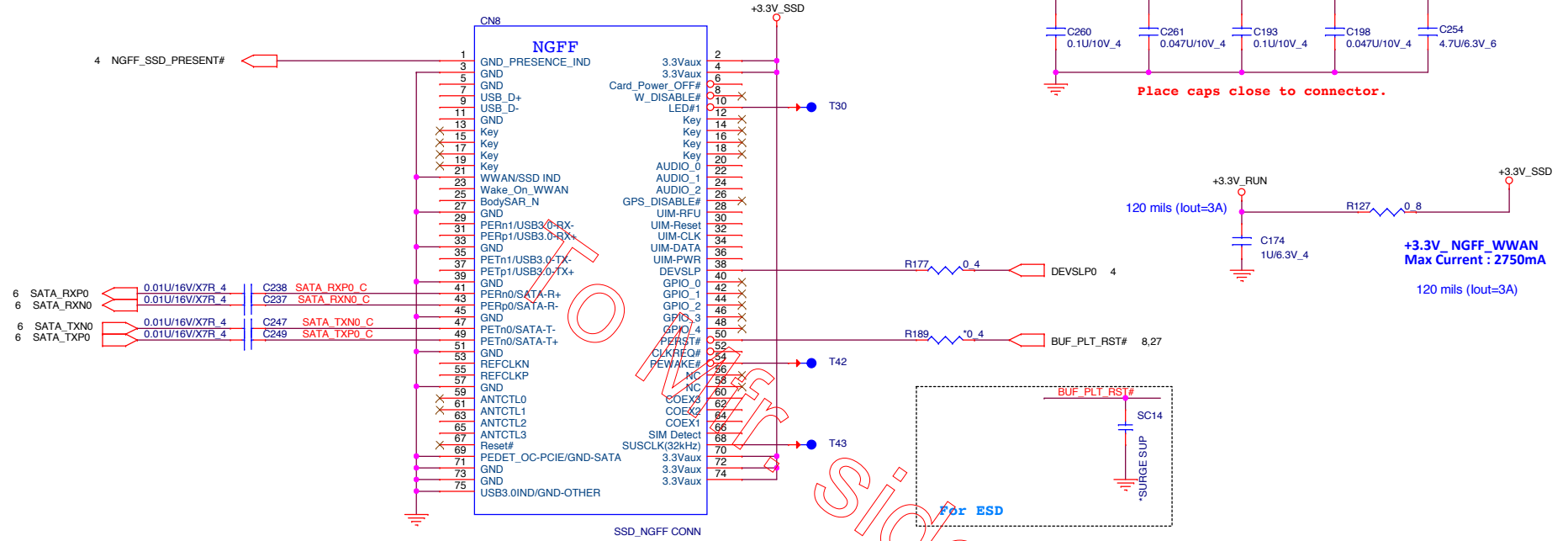


To Mfr. Side


**PROJECT : ST6A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>SATA</b>	1A

### NGFF SSD connector

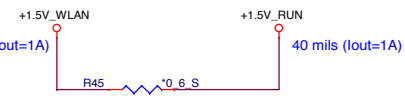
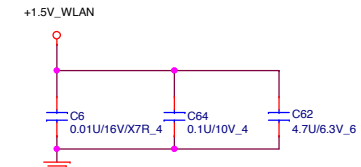
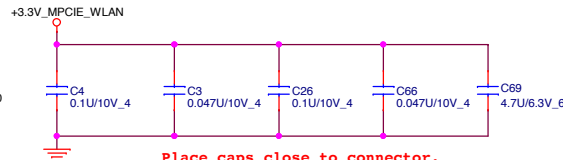
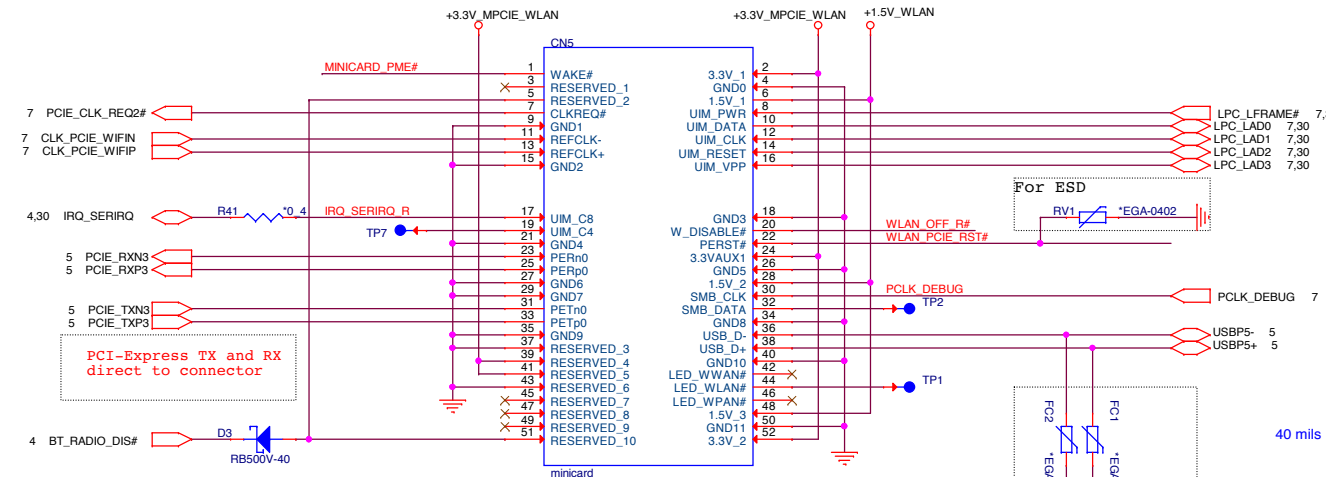


		<b>PROJECT : ST6A</b>	
		<b>Quanta Computer Inc.</b>	
Size	Document Number	<b>SSD NGFF</b>	
Date: Monday, April 01, 2013	Sheet 26 of 46	Rev	1A

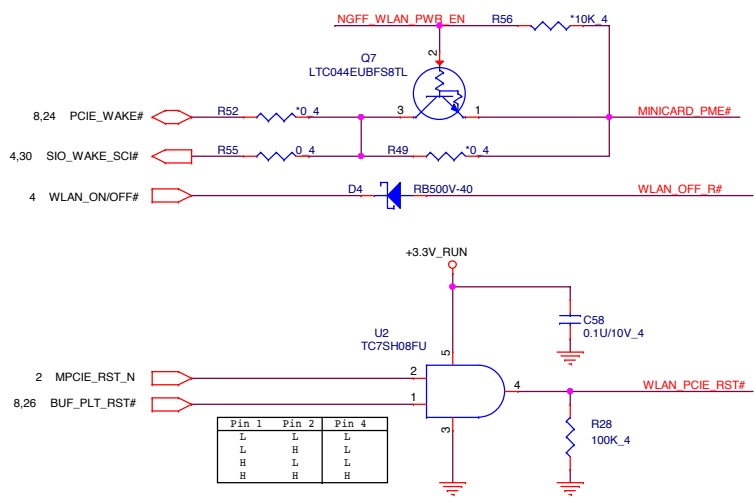
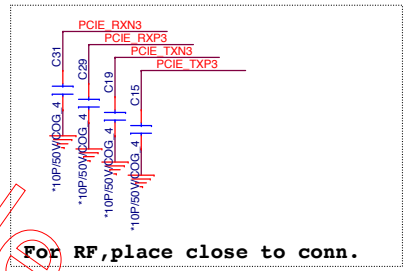
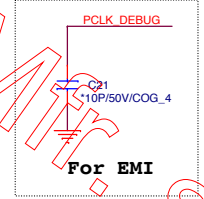
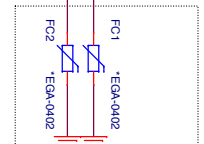
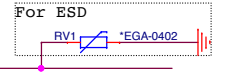
# Mini PCIE Wifi/BT connector

2,4,6,7,8,12,14,15,20,21,22,23,24,26,29,30,31,32,34,35,40,41,42 +3.3V\_RUN  
 4,6,8,12,23,24,29,31,35,36,41,44 +3.3V\_DSW  
 12,23,34,39,42,44 +1.5V\_RUN

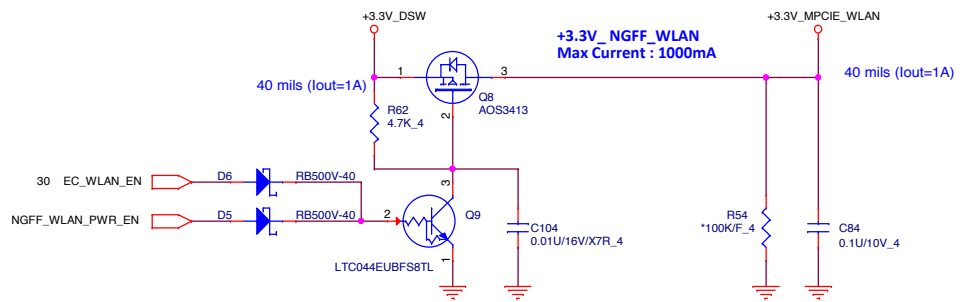
# 27



PCI-Express TX and RX direct to connector

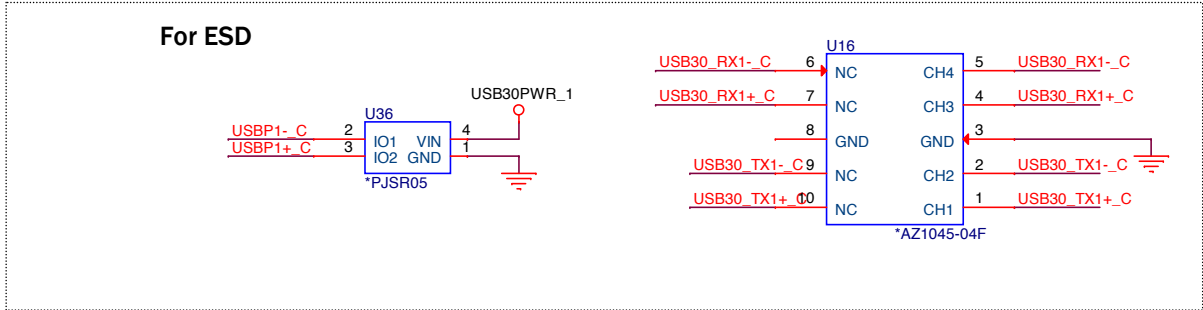
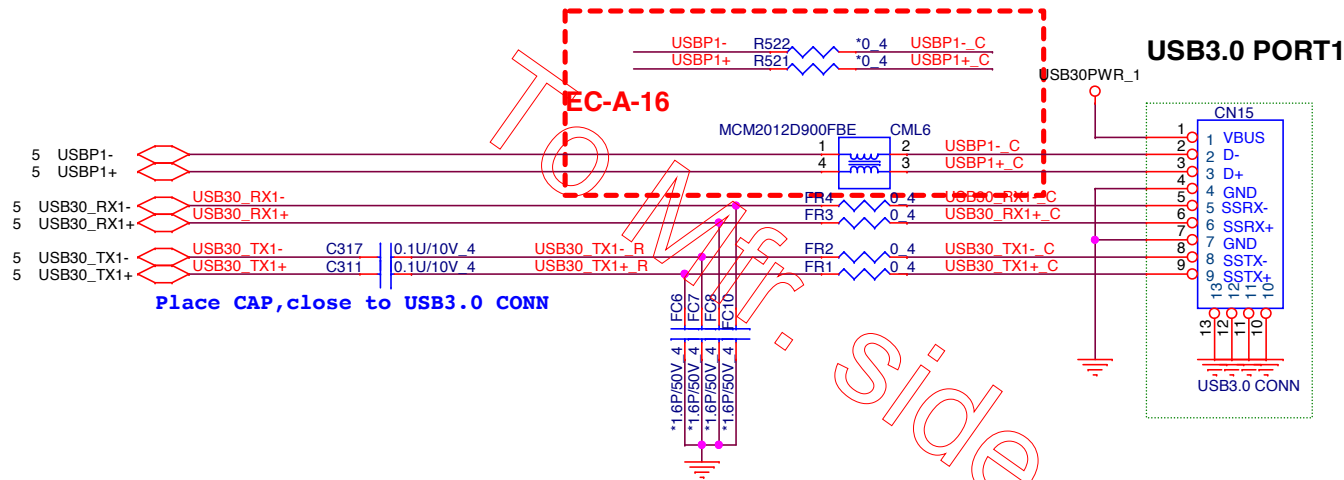
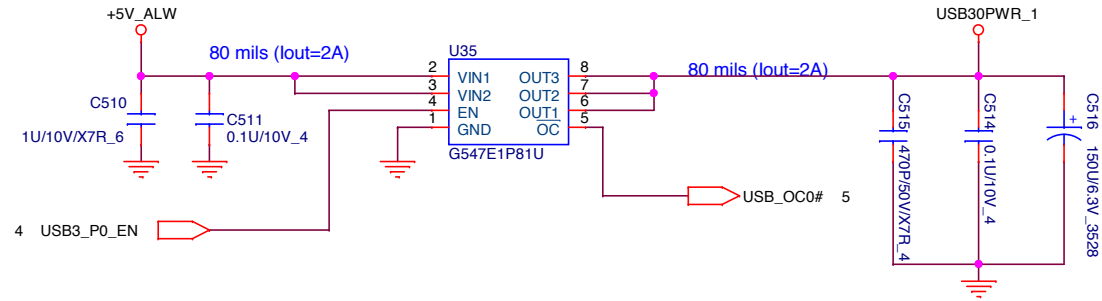


Pin 1	Pin 2	Pin 4
L	L	L
H	L	L
H	H	H



**PROJECT : ST6A**  
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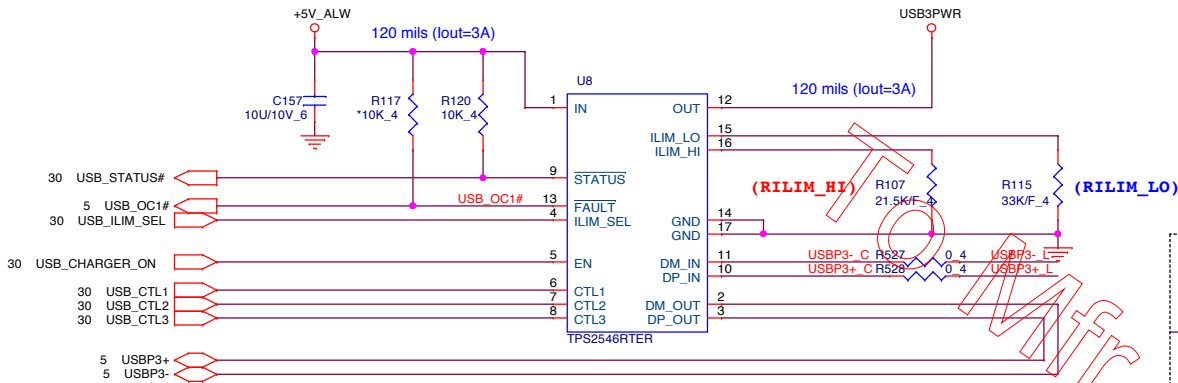
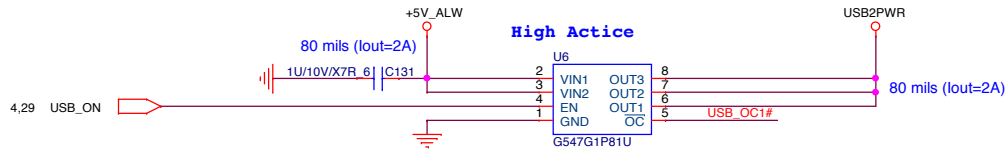
Size	Document Number	Rev
	Wifi/BT MiniPCIE	1A
Date: Monday, April 01, 2013	Sheet 27 of 46	



**PROJECT : ST6A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>USB3.0 x1</b>	1A
Date:	Monday, April 01, 2013	Sheet 28 of 46

# USB 2.0 Port \*2



RILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:

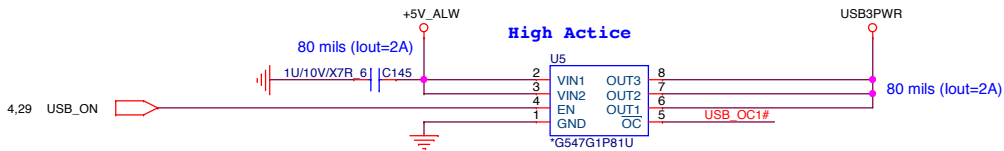
1. ILIM\_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM\_LO < 80.6 kΩ.

The following equation programs the typical current limit:

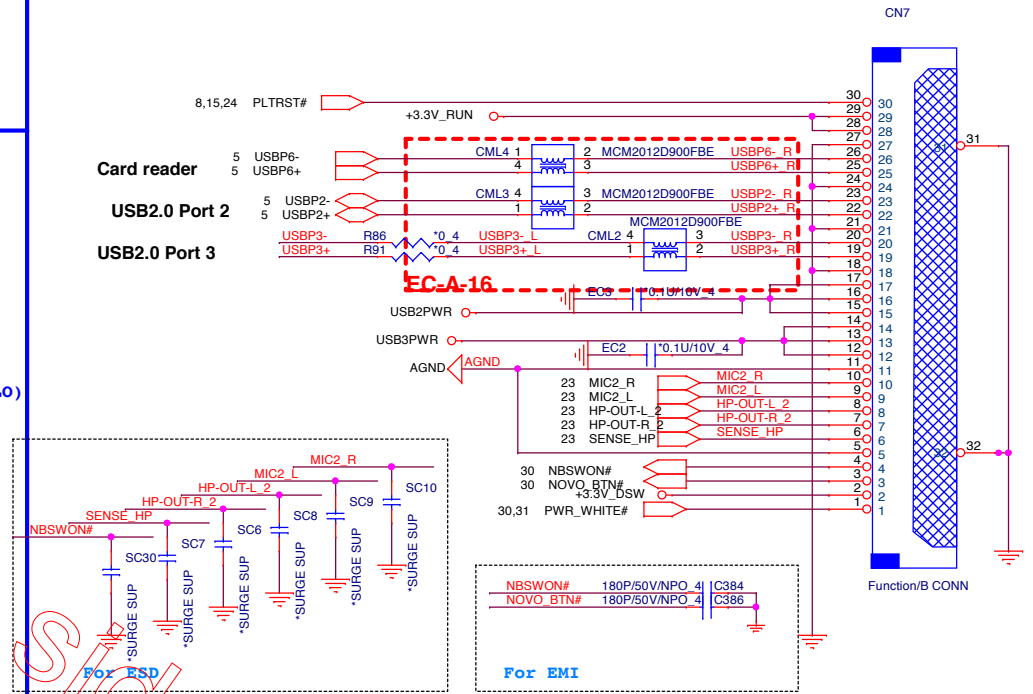
(1)  
RILIM\_XX corresponds to either RILIM\_HI or RILIM\_LO as appropriate.

$$I_{OS\_typ} (mA) = \frac{50,500}{(R_{ILIM\_XX} (k\Omega) + 0.1)}$$

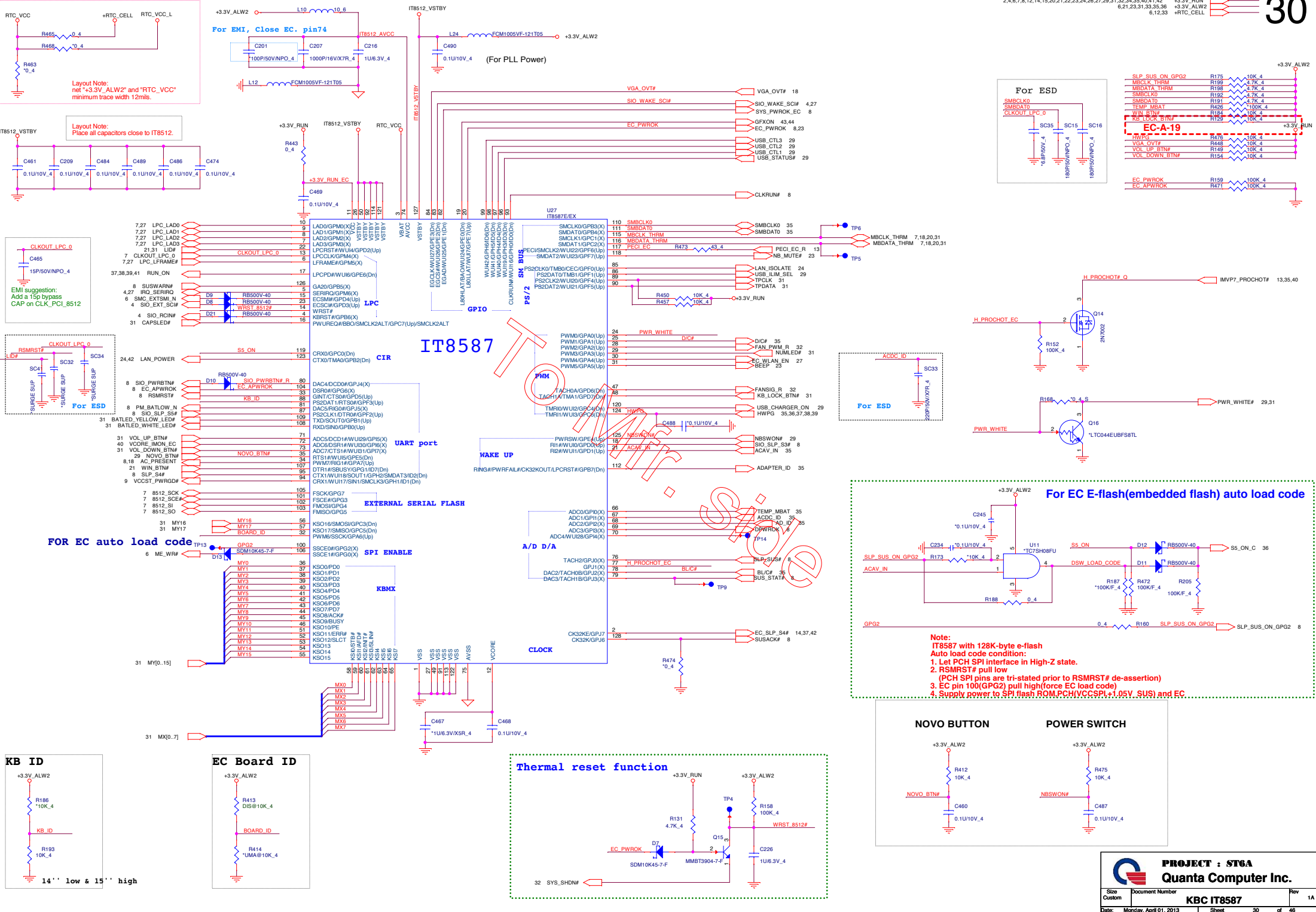


12,14,28,35,36,37,38,39,41,42,43,44 +5V\_ALW  
4,6,8,12,23,24,27,31,35,36,41,44 +3.3V\_DSW  
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,30,31,32,34,35,40,41,42 +3.3V\_RUN

## Card reader USB2.0 Port 2 USB2.0 Port 3



EC-A-04



**Layout Note:**  
net "+3.3V\_ALW2" and "RTC\_VCC"  
minimum trace width 12mils.

**Layout Note:**  
Place all capacitors close to IT8512.

**EMi suggestion:**  
Add a 15p bypass  
CAP on CLK\_PCI\_8512

**For ESD**

**FOR EC auto load code**

**KB ID**

**EC Board ID**

**For EMI, Close EC. pin74**

**For PLL Power**

**GPIO**

**UART port**

**EXTERNAL SERIAL FLASH**

**SPI ENABLE**

**KBMX**

**CLOCK**

**Thermal reset function**

**VGA\_OVT#**

**EC\_PWROK**

**PWM**

**WAKE UP**

**A/D D/A**

**CLOCK**

**Thermal reset function**

**SIO\_WAKE\_SCI#**

**EC\_PWROK**

**PWM**

**WAKE UP**

**A/D D/A**

**CLOCK**

**Thermal reset function**

**For ESD**

**For ESD**

**For ESD**

**For ESD**

**For EC E-flash(auto load code)**

**For EC E-flash(auto load code)**

**NOVO BUTTON**

**POWER SWITCH**

**CLOCK**

**Thermal reset function**

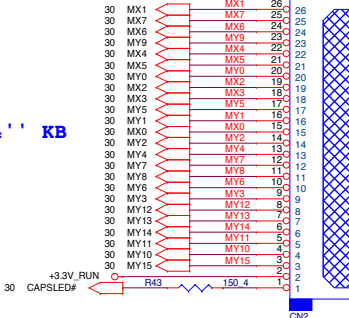
**For EC E-flash(auto load code)**

**POWER SWITCH**

**Note:**  
IT8587 with 128K-byte e-flash  
Auto load code condition:  
1. Let PCH SPI interface in High-Z state.  
2. RSMRST# pull low  
(PCH SPI pins are tri-stated prior to RSMRST# de-assertion)  
3. EC pin 100(GP2) pull high(force EC load code)  
4. Supply power to SPI flash ROM(PCH(VCCSPI+1.05V\_SUS) and EC.

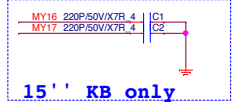
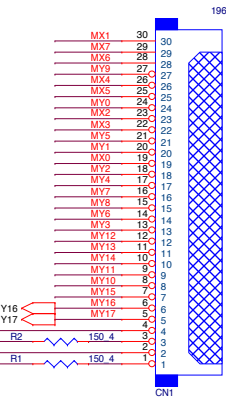
**KEYBOARD**

50584-02801-001

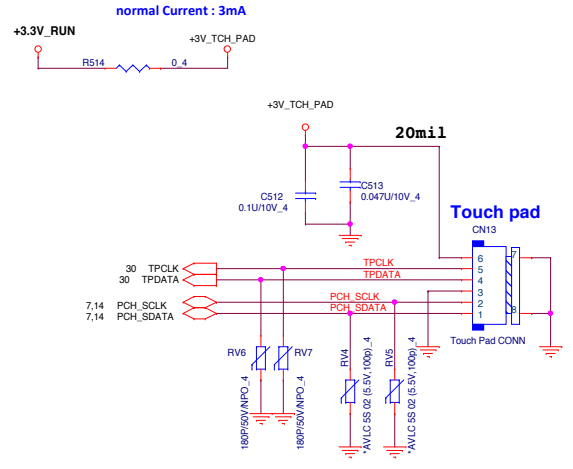


**For EMI**

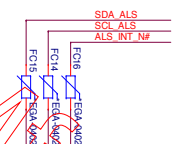
MY15	C34	220P/50V/X7R_4	C38	220P/50V/X7R_4	MY13
MY10	C35	220P/50V/X7R_4	C39	220P/50V/X7R_4	MY12
MY11	C36	220P/50V/X7R_4	C40	220P/50V/X7R_4	MY3
MY14	C37	220P/50V/X7R_4	C41	220P/50V/X7R_4	MY6
MX0	C46	220P/50V/X7R_4	C57	220P/50V/X7R_4	MX1
MY1	C47	220P/50V/X7R_4	C56	220P/50V/X7R_4	MY7
MY5	C48	220P/50V/X7R_4	C55	220P/50V/X7R_4	MY6
MX3	C49	220P/50V/X7R_4	C54	220P/50V/X7R_4	MY9
MX2	C50	220P/50V/X7R_4	C42	220P/50V/X7R_4	MY8
MY0	C51	220P/50V/X7R_4	C43	220P/50V/X7R_4	MY7
MX5	C52	220P/50V/X7R_4	C44	220P/50V/X7R_4	MY4
MX4	C53	220P/50V/X7R_4	C45	220P/50V/X7R_4	MY2



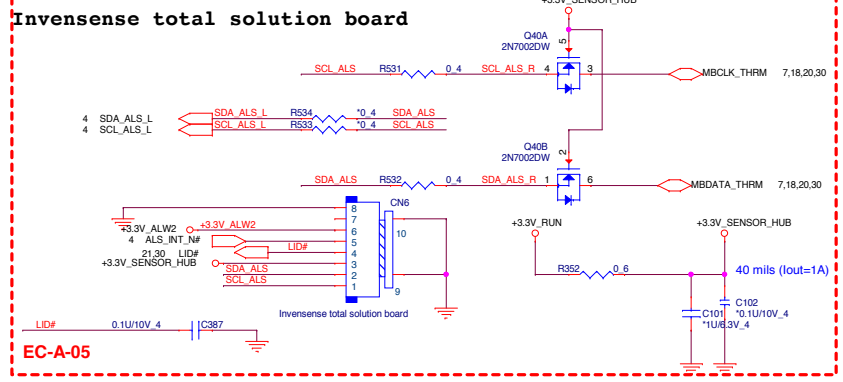
**TP Control**



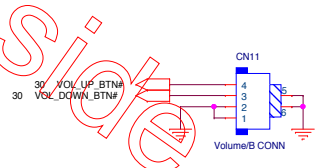
reserve for ESD



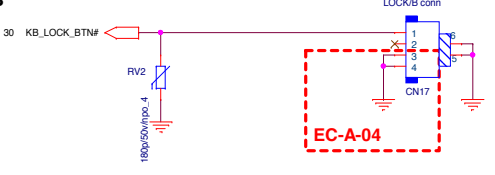
**DB CONN**



**Volume/B**



**LOCK/B**

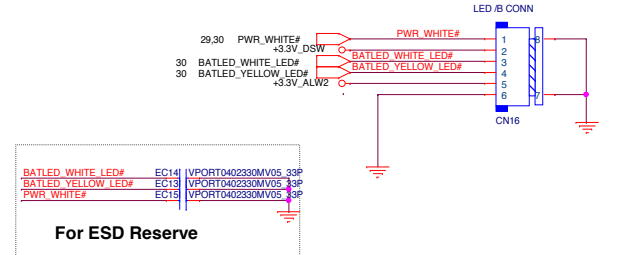


2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,32,34,35,40,41,42

+3.3V\_RUN

**31**

**LED /B**



**For ESD Reserve**

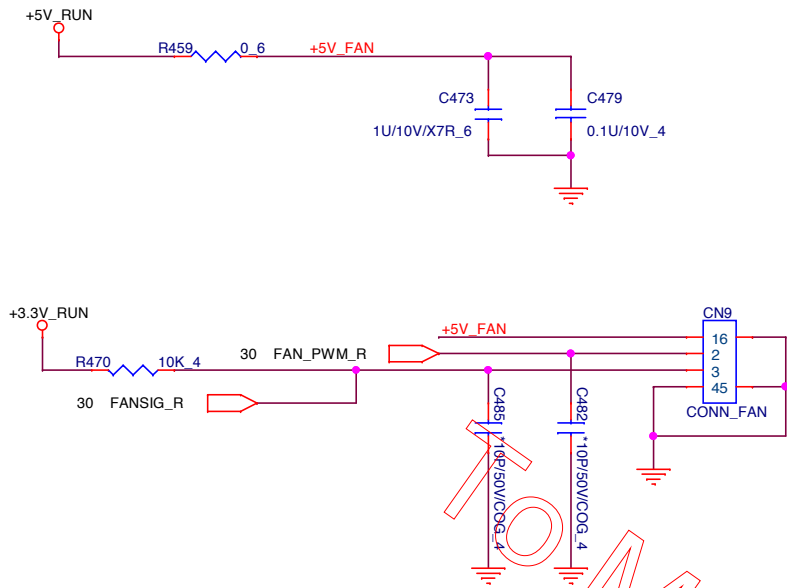
**PROJECT : ST6A**  
**Quanta Computer Inc.**

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	<b>KB/TP/LID</b>	1A
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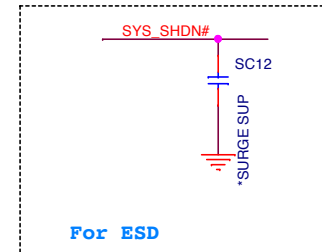
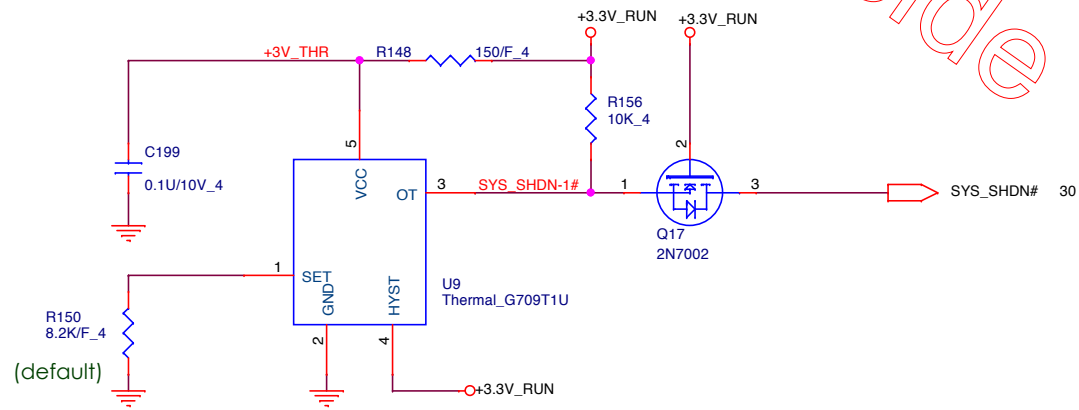
# FAN CONTROL


2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,34,35,40,41,42 +3.3V\_RUN  
22,23,25,35,40,41,42 +5V\_RUN

# 32



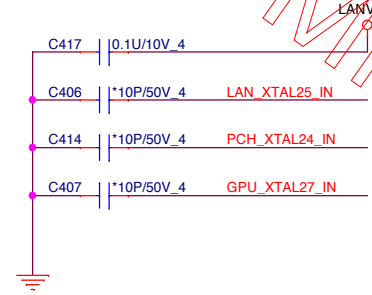
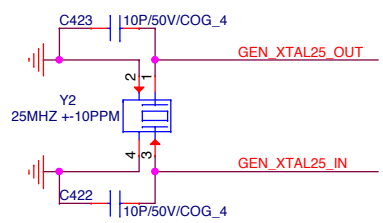
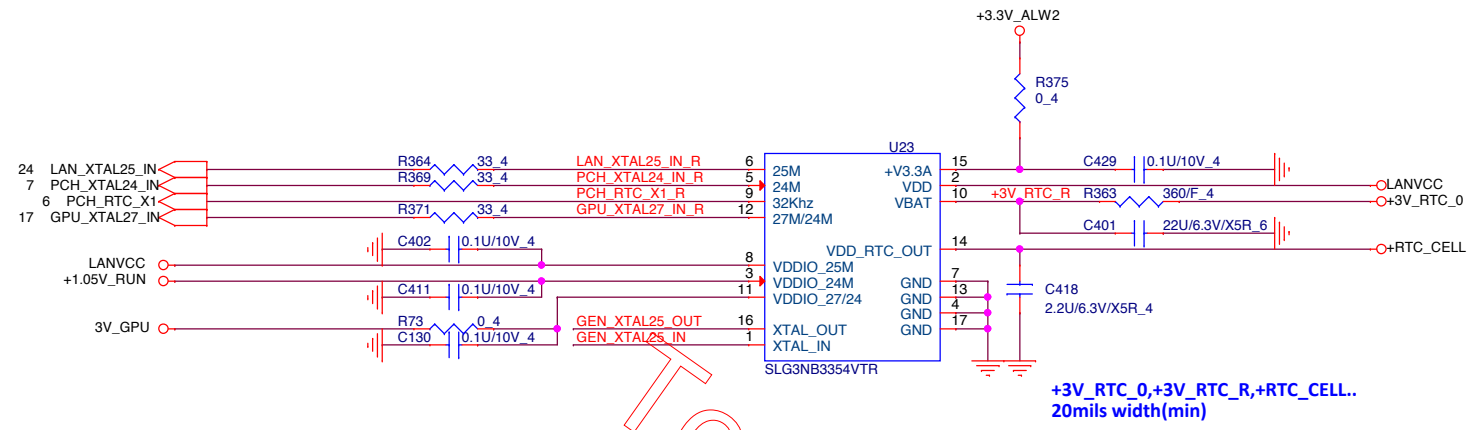
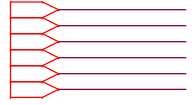
# Thermal Sensor



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	<b>FAN/Thermal</b>	1A
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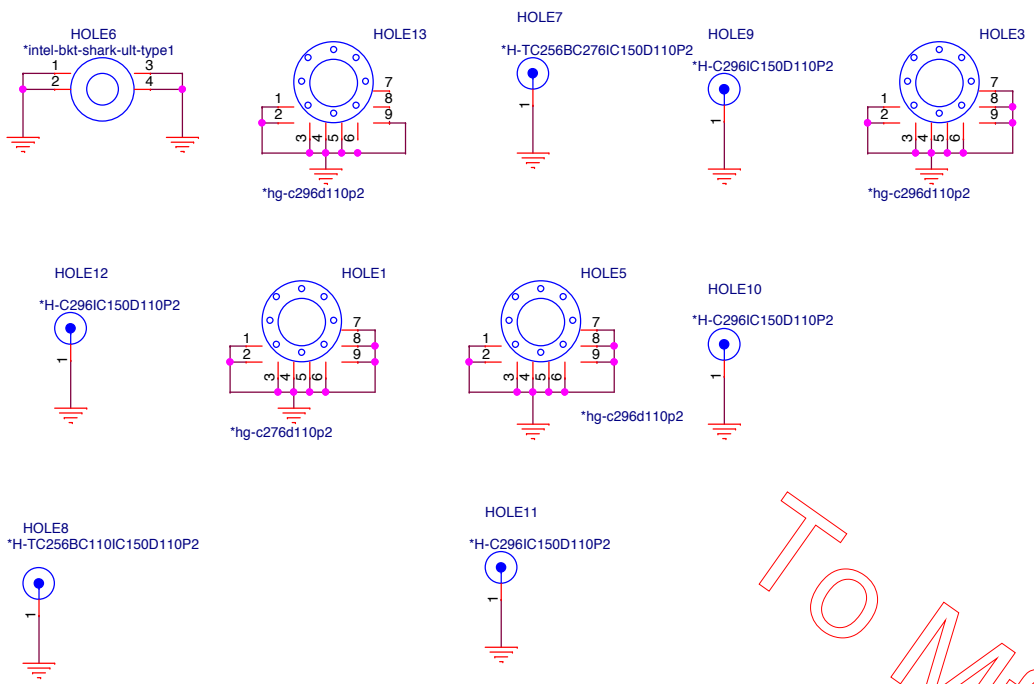
6,21,23,30,31,35,36 +3.3V\_ALW2  
 24,42 LANVCC  
 6 +3V\_RTC\_0  
 6,12,30 +RTC\_CELL  
 6,9,12,34,38,40,42,44 +1.05V\_RUN  
 15,18,34,43,44,45 3V\_GPU



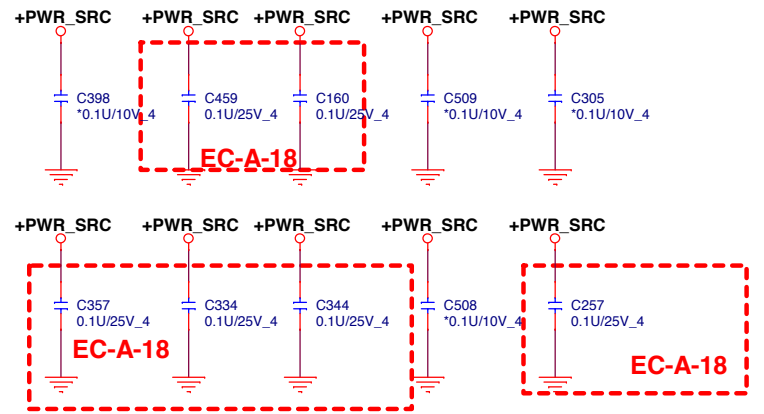
SLG3NB3354VTR(AL003354001)====>DIS  
 32Kx1+24M\*1+25Mx1+27Mx1  
 1.S430-DIS --> SLG3NB3354  
 2.S430-UMA --> SLG3NB3355

TOP Mir Side

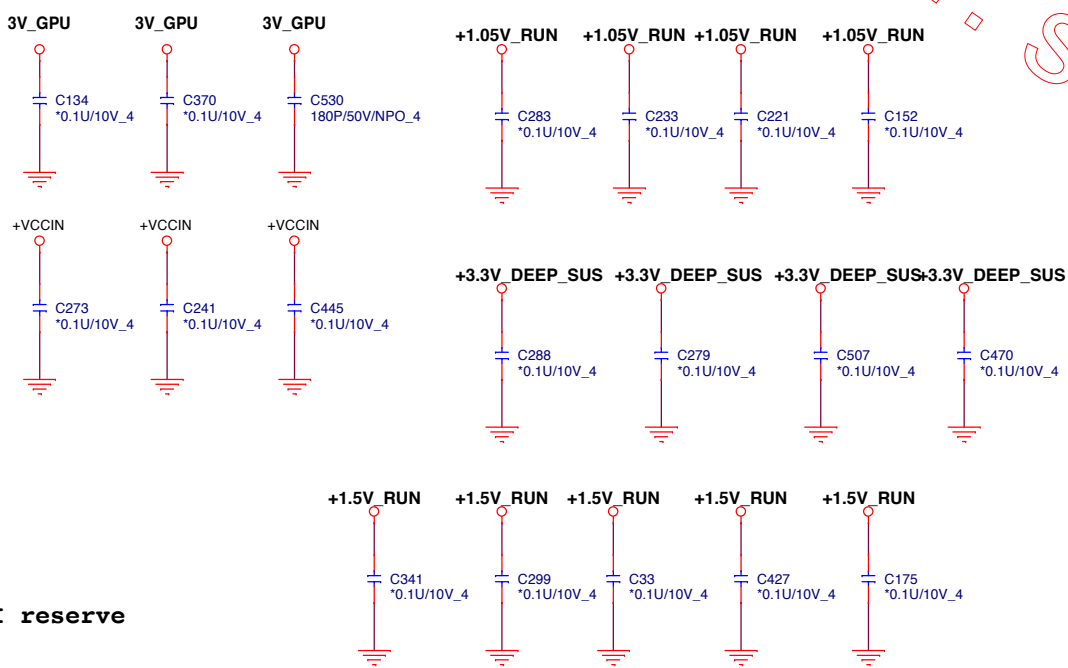
 <b>PROJECT : ST6A</b> <b>Quanta Computer Inc.</b>		Size	Document Number	Rev	
		<b>Green Clock</b>		1A	
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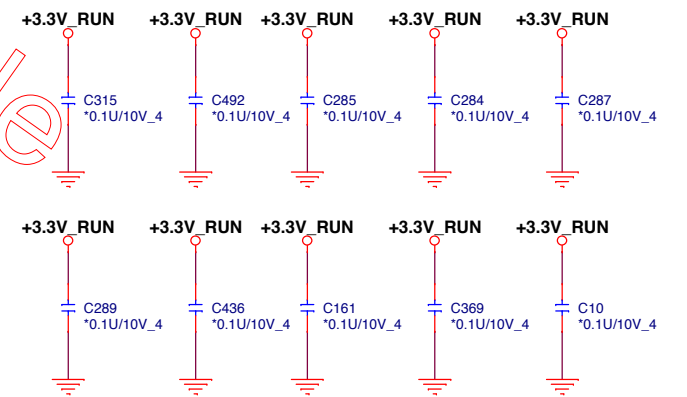
EC-A-18



To Mfr Side

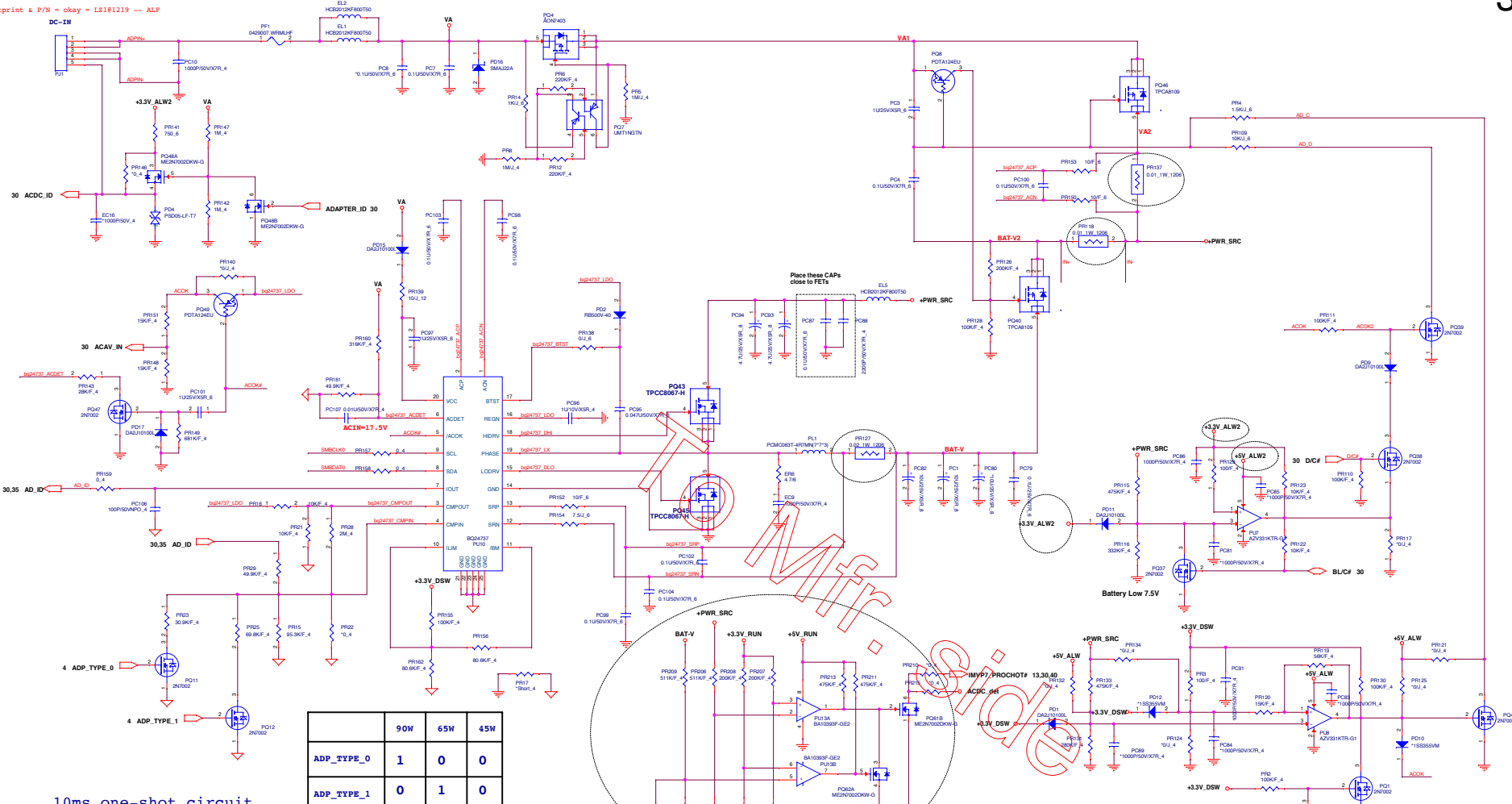


EMI reserve



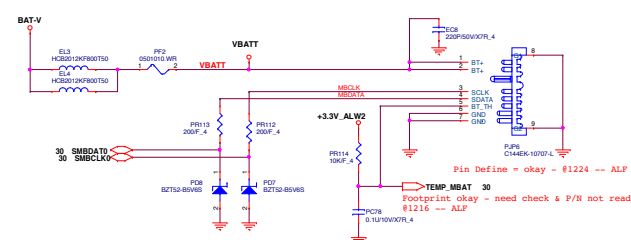
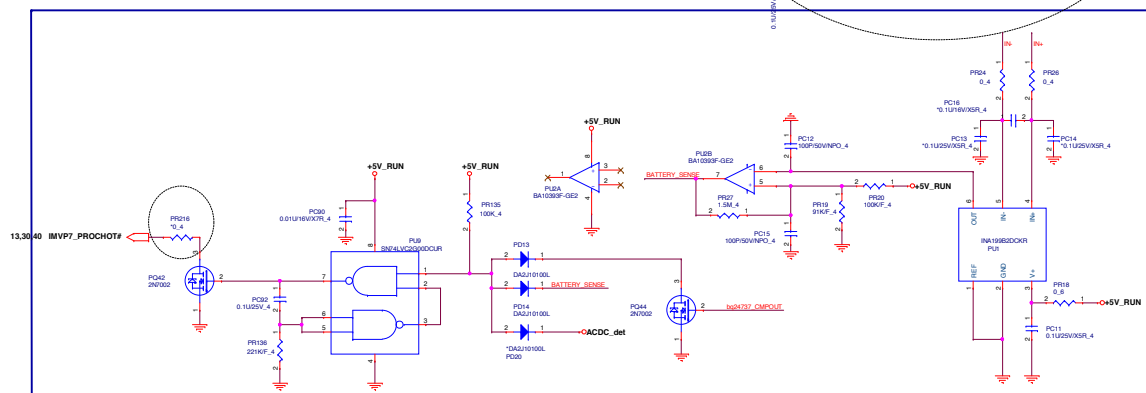
		<b>PROJECT : ST6A</b>	
		<b>Quanta Computer Inc.</b>	
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	<b>Screw Hole/EMI</b>	1A	
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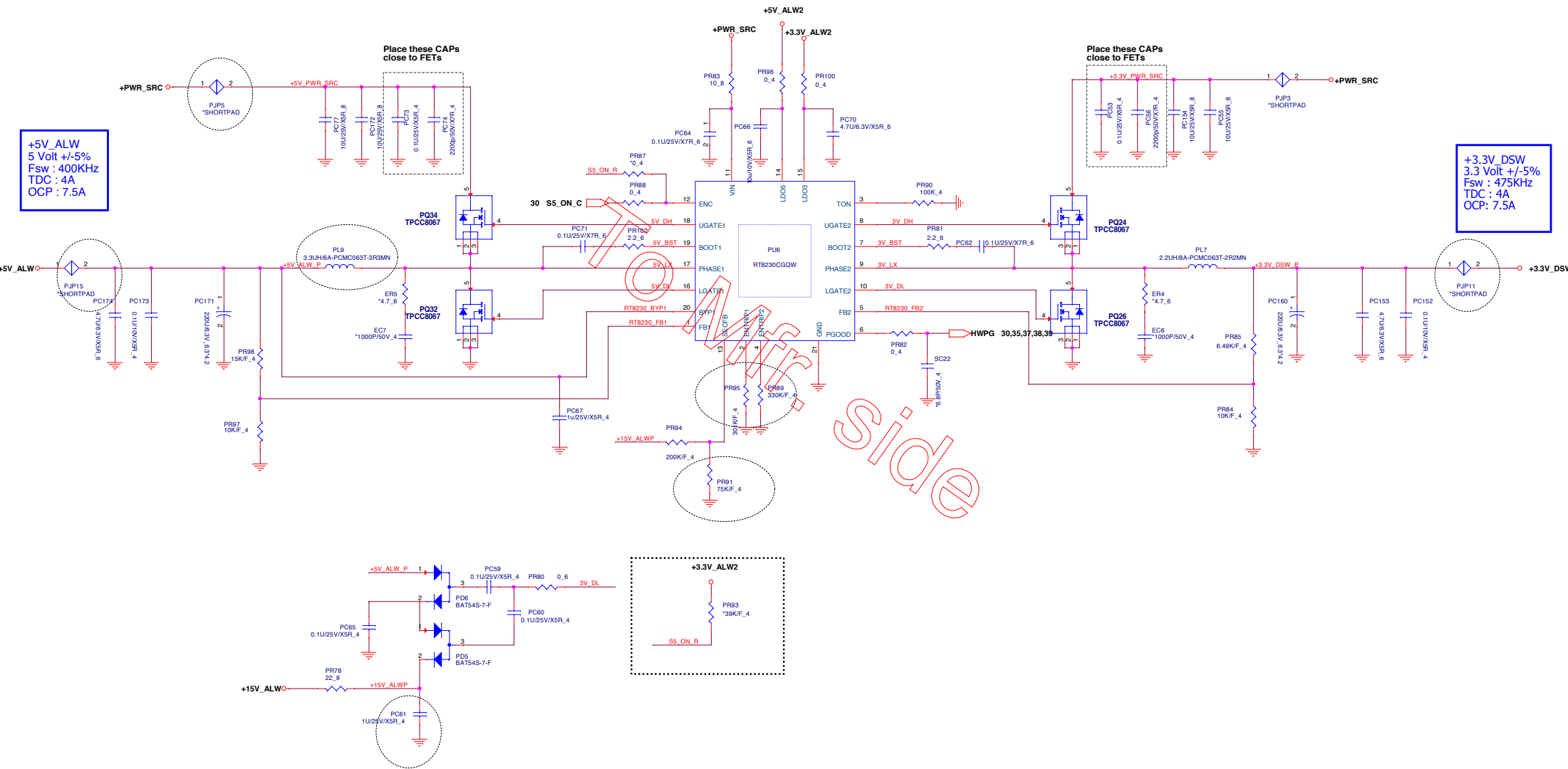
Footprint & P/N = okay = L2181219 -- ALP

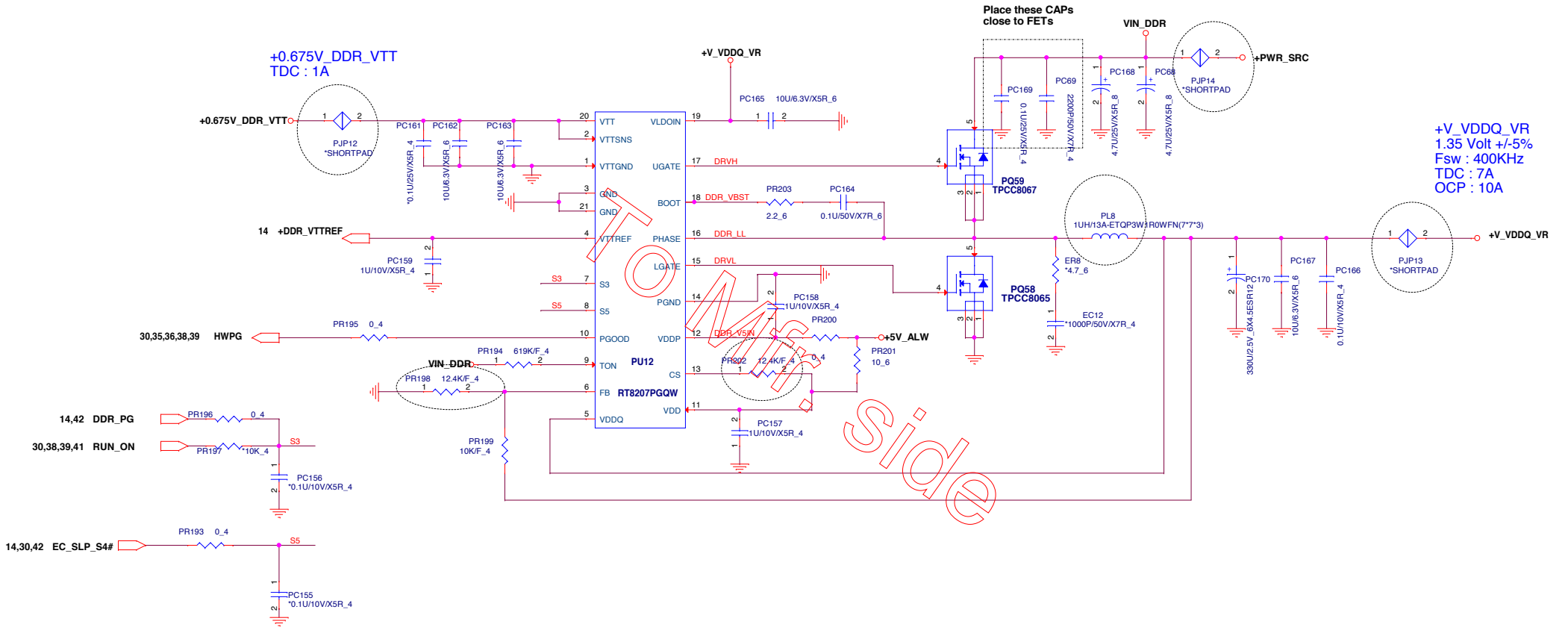


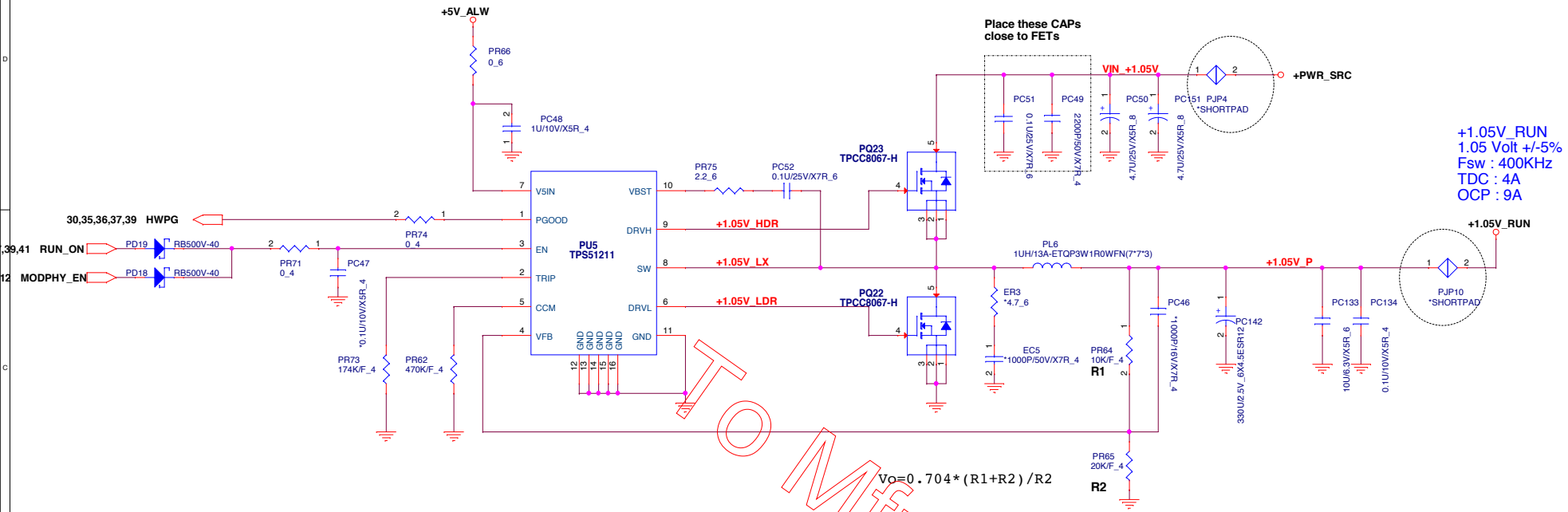
	90W	65W	45W
ADP_TYPE_0	1	0	0
ADP_TYPE_1	0	1	0

10ms one-shot circuit

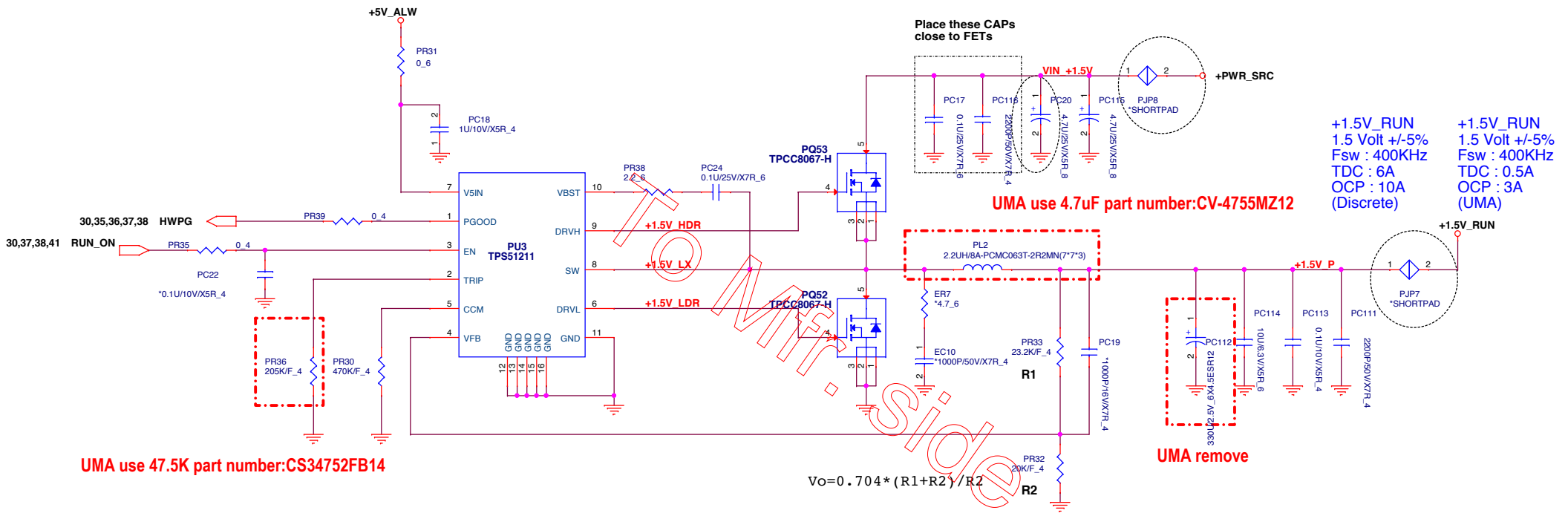








TO Mfr. Side



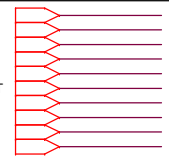




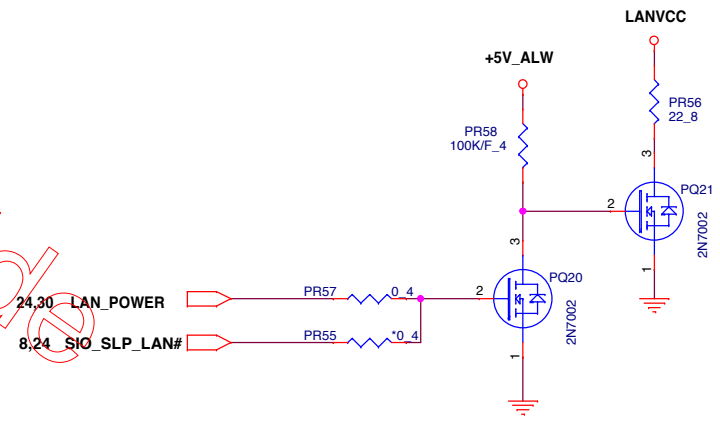
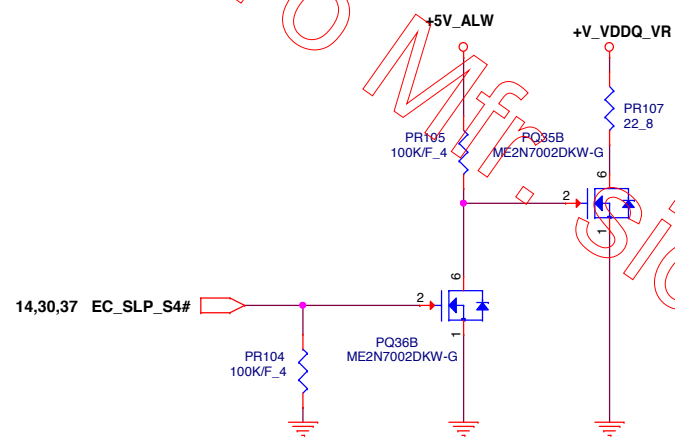
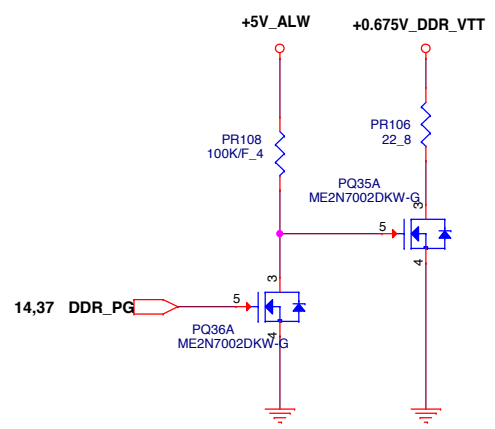
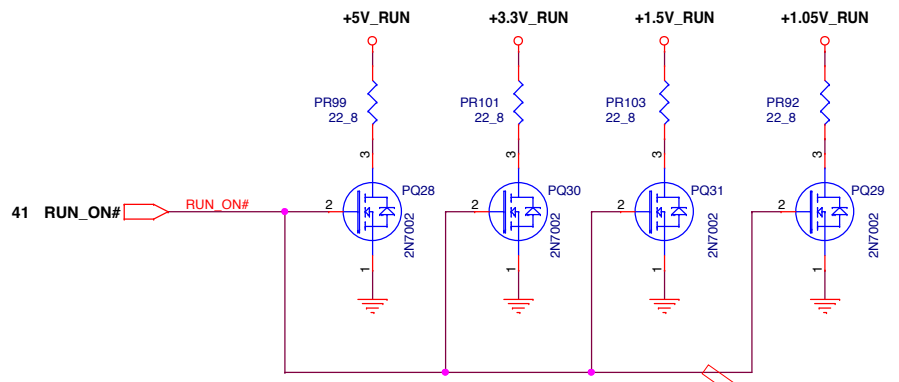



# DISCHARGE

12,14,28,29,35,36,37,38,39,41,43,44	+5V_ALW
22,23,25,32,35,40,41	+5V_RUN
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41	+3.3V_RUN
12,23,27,34,39,44	+1.5V_RUN
6,9,12,33,34,38,40,44	+1.05V_RUN
14,37	+0.675V_DDR_VTT
4,5,6,7,8,12,14,34	+3.3V_DEEP_SUS
9,14,37	+V_VDDQ_VR
24,33	LANVCC
36,41,44	+15V_ALW

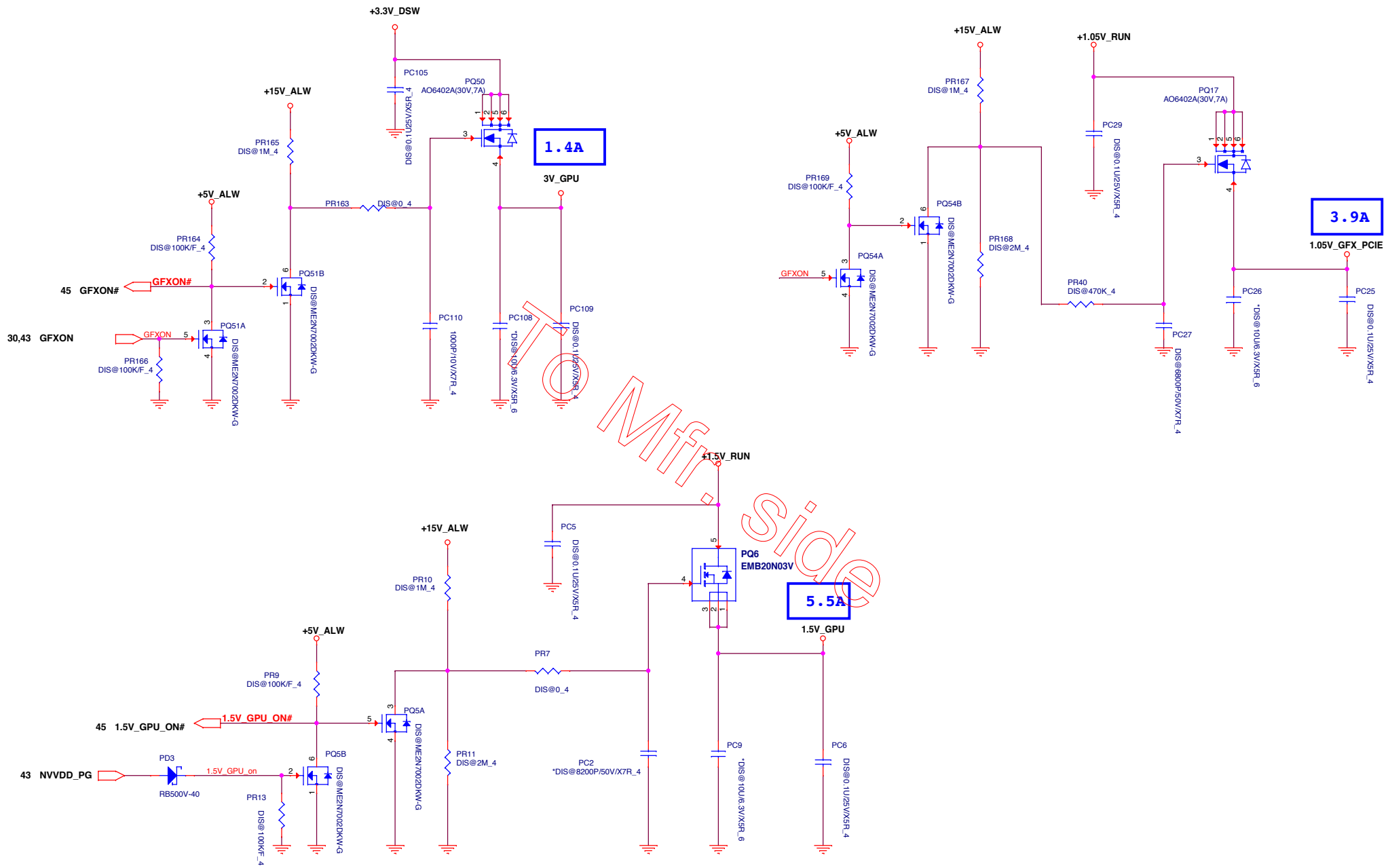
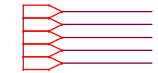


# 43



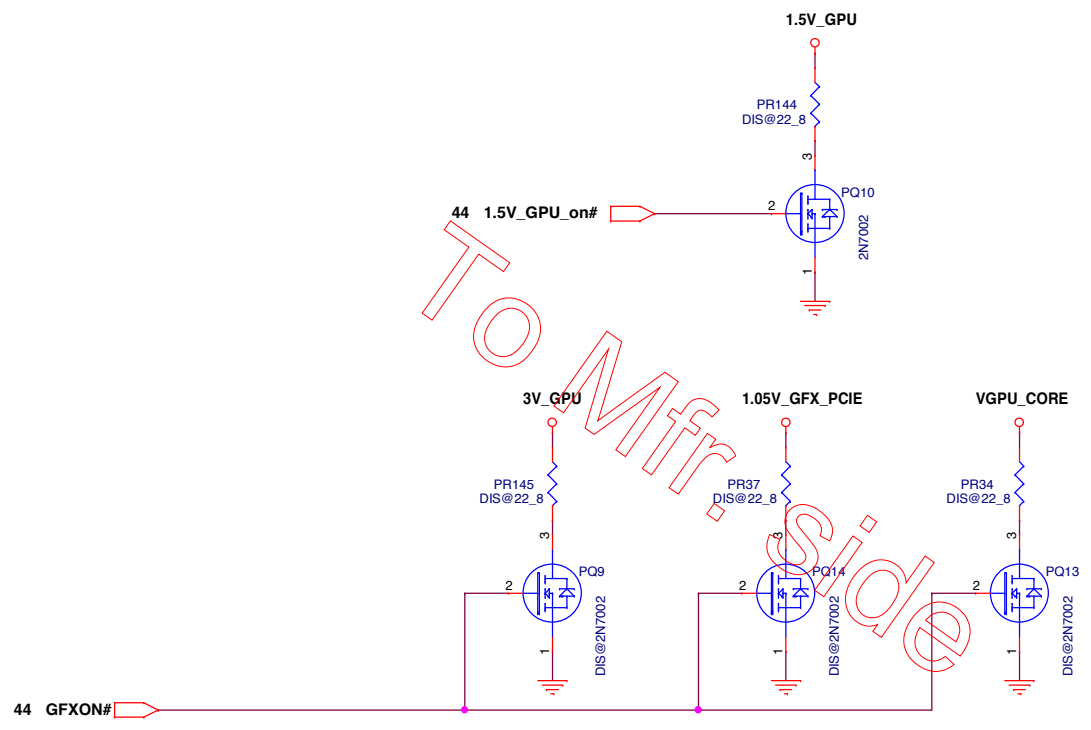
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	Discharge	
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**DISCHARGE**

12,14,28,29,35,36,37,38,39,41,42,43,44 +5V\_ALW  
 2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3V\_RUN  
 12,23,27,34,39,42,44 +1.5V\_RUN  
 6,9,12,33,34,38,40,42,44 +1.05V\_RUN  
 14,37,42 +0.675V\_DDR\_VTT  
 9,14,37,42 +V\_VDDQ\_VR  
 24,33,42 LANVCC  
 36,41,44 +15V\_ALW



TO Mfr  
 @ssida@

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		Size
Document Number <b>Discharge</b>		Date: Monday, April 01, 2013
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SDV~SIV

2013

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	21	02/07		Change touch panel VCC control to +3.3V_RUN and stuff R17
EC-A-02	21	02/07		Add +3.3V_RUN to provide LCD panel EDID VCC and stuff R22
EC-A-03	20	02/08	C147	depop C147 from vendor request
EC-A-04	29,31	02/22	U10,C466	remove U10,C466 for lid change to sensor B
EC-A-05	29,31	03/05		sensor hub remove and reserve light sensor for I2C interface
EC-A-06	29	03/05	R528,R528	add R527,R528 to avoid stub
EC-A-07	7	03/05		CLKREQ change
EC-A-08	24	03/05		lan surge solution change
EC-A-09	21	03/06		RTD2132R support initial PWM to product LCDVCC
EC-A-10	21	03/06	R502,R504,R506,R509 R510,R511,R512,R513	change value to meet design guide
EC-A-11	29	03/13	R107	change to 21.5K for charger limit setting
EC-A-12	15	03/15		Q10 pin2 change to GFXPG control
EC-A-13	20	03/11	U24	depop
EC-A-14	12	03/12		change to +5V_ALW
EC-A-15	21	03/12	CN4	Change to 10 pin conn.
EC-A-16	29	03/18	CML2,CML3,CML4,CML6 R85,R90,R96,R101,R118,R119,R521,R522	CML2,CML3,CML4,CML6 pop for EMI suggestion R85,R90,R96,R101,R118,R119,R521,R522 depop for EMI suggestion
EC-A-17	22	03/18	R264,R265,R266,R267	R264,R265,R266,R267 pop for EMI suggestion
EC-A-18	34	03/18	C160,C257,C334,C357 and C459	C160,C257,C334,C357 and C459 pop for EMI suggestion
EC-A-19	30	03/19		KB_LOCK_BTN# pull up to +3.3V_ALW2
EC-A-20	21	03/19	R20,R21,CML7	delete R20,R21 and add CML7
EC-A-21	21	03/22	U39,R535,C529	reserve to meet LCD off sequence



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	EC list-1	
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