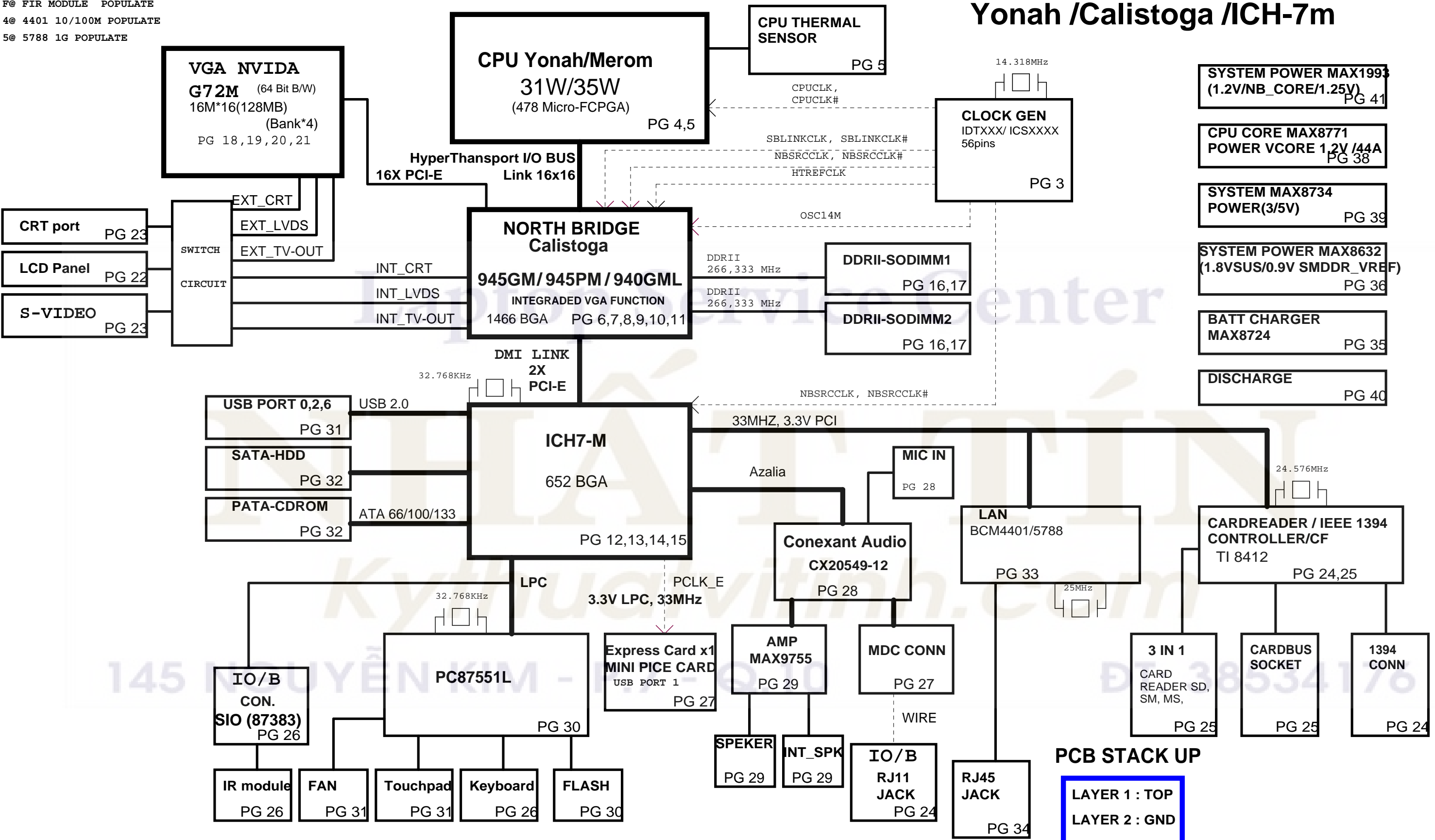


LE4 BLOCK DIAGRAM

Yonah /Calistoga /ICH-7m

BOM MARK
 E@ EXT VGA POPULATE
 I@ INV VGA POPULATE
 F@ FIR MODULE POPULATE
 4@ 4401 10/100M POPULATE
 5@ 5788 1G POPULATE



- SYSTEM POWER MAX1993 (1.2V/NB_CORE/1.25V) PG 41
- CPU CORE MAX8771 POWER VCORE 1.2V /44A PG 38
- SYSTEM MAX8734 POWER(3/5V) PG 39
- SYSTEM POWER MAX8632 (1.8VSUS/0.9V SMDDR_VREF) PG 36
- BATT CHARGER MAX8724 PG 35
- DISCHARGE PG 40

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT

Board Stack up Description

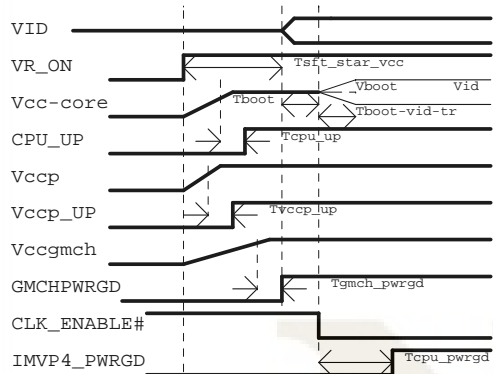
PCB Layers

- Layer 1 TOP(Component,Other)
- Layer 2 Ground Plane
- Layer 3 IN1
- Layer 4 Power Plane
- Layer 5 IN2
- Layer 6 IN3
- Layer 7 Ground Plane
- Layer 8 BOTTOM

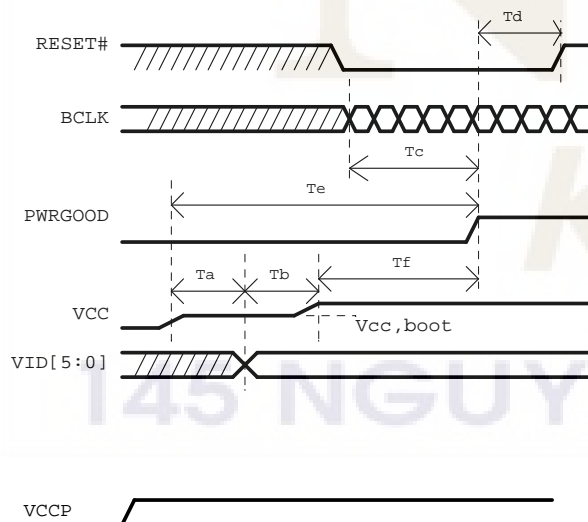
Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5	X	X	X		RVCC_ON
RVCC3	X	X	X		RVCCD
VCC1.5	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL
9VPCU	X	X	X	X	5VPCU

Power On Sequencing Timing Diagram

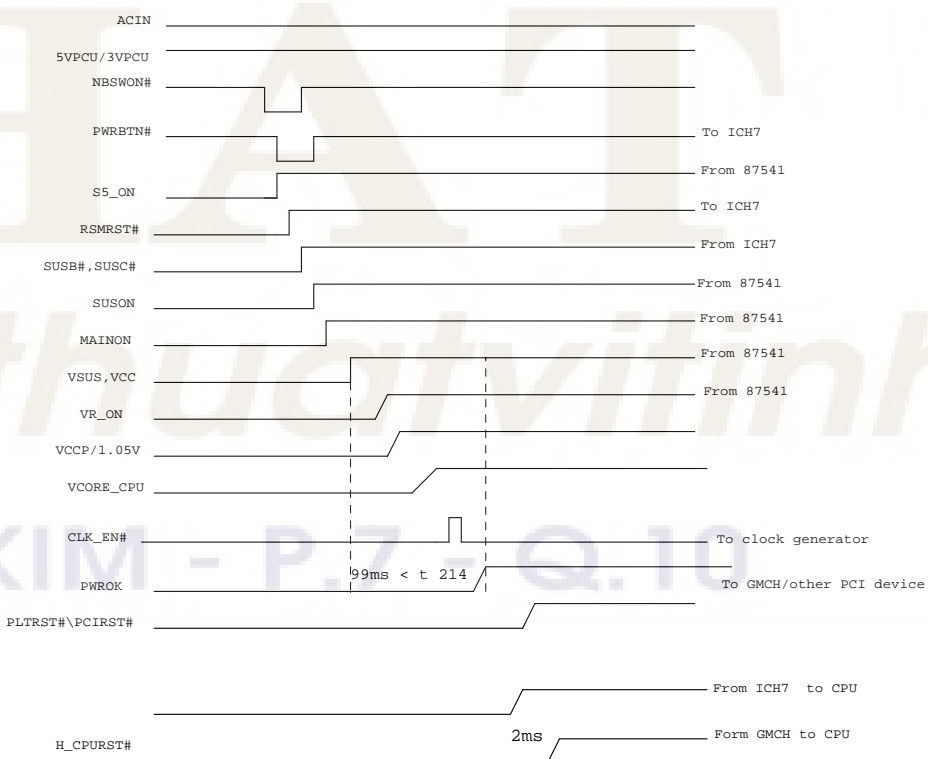


Dothan Power-up Timing Specifications



Ta=VCC and VCCP assertion to VID[5:0] valid
 Tb=VID[5:0] stable to VCC valid
 Tc=BCLK stable to PWRGOOD assertion
 Td=PWRGOOD to RESET# de-assertion time
 Te=Vcc,boot valid to PWRGOOD assertion time

ACIN POWER ON TIMING

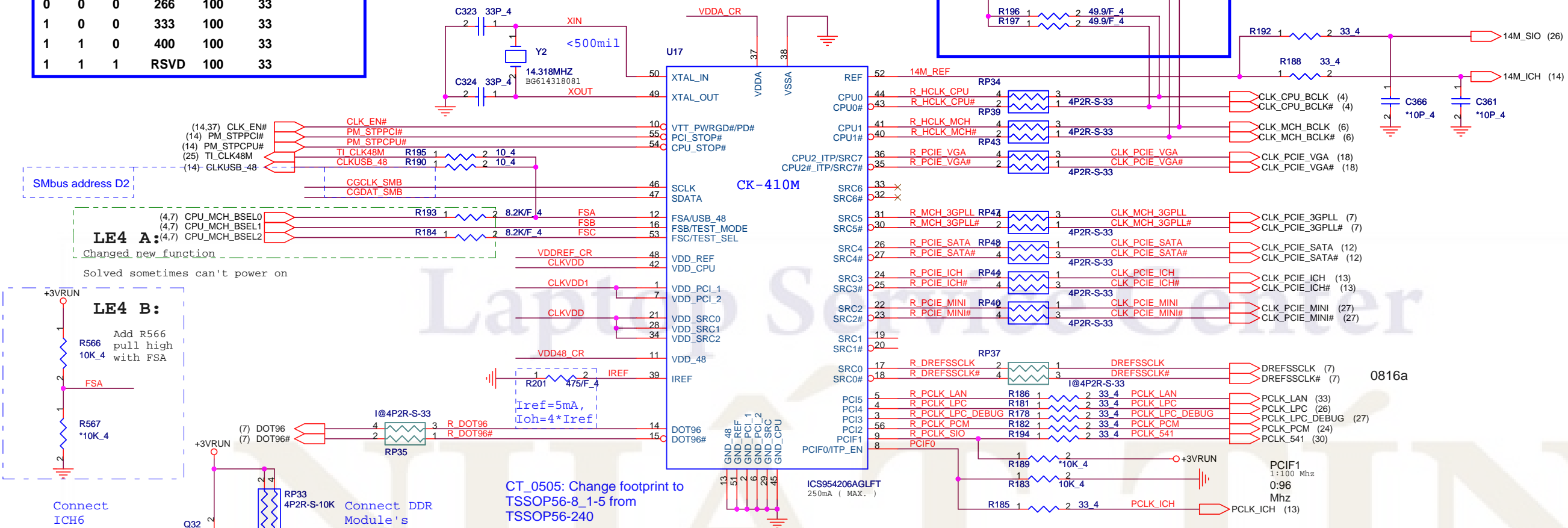


Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE Core voltage for Processor	X				VRON
GMCH_VTT Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM 0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF 0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V	X				MAINON
1.8VSUS 1.8V for DDR II voltage	X	X			SUSON
+2.5V	X				MAINON
3VPCU	X	X	X	X	VL
3VSUS	X	X			SUSON
+3V	X				MAINON
5VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
+5V	X				MAINON
VIN POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD25	REQ1# / GNT1#	PIRQ B/C/D

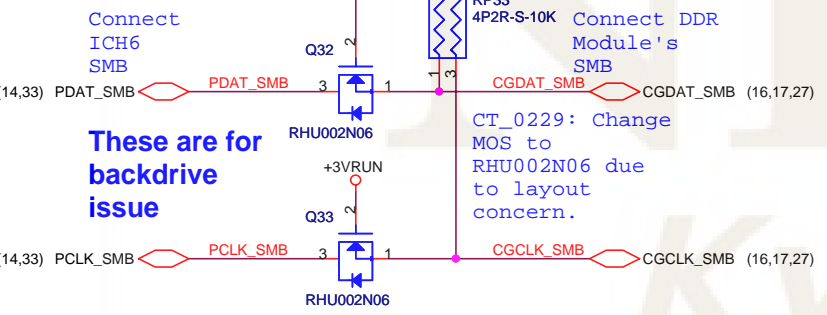
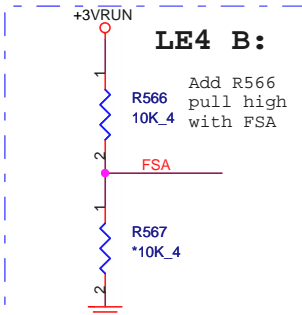
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.



SMBus address D2

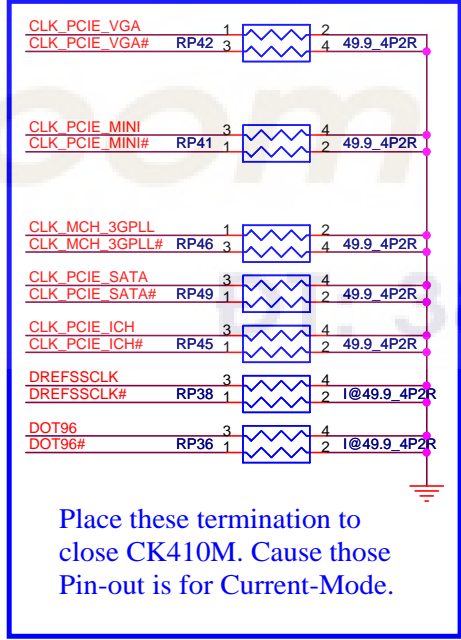
LE4 A:
Changed new function
Solved sometimes can't power on



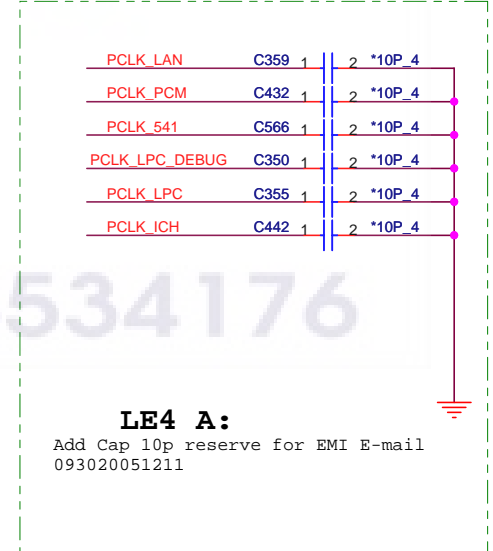
CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

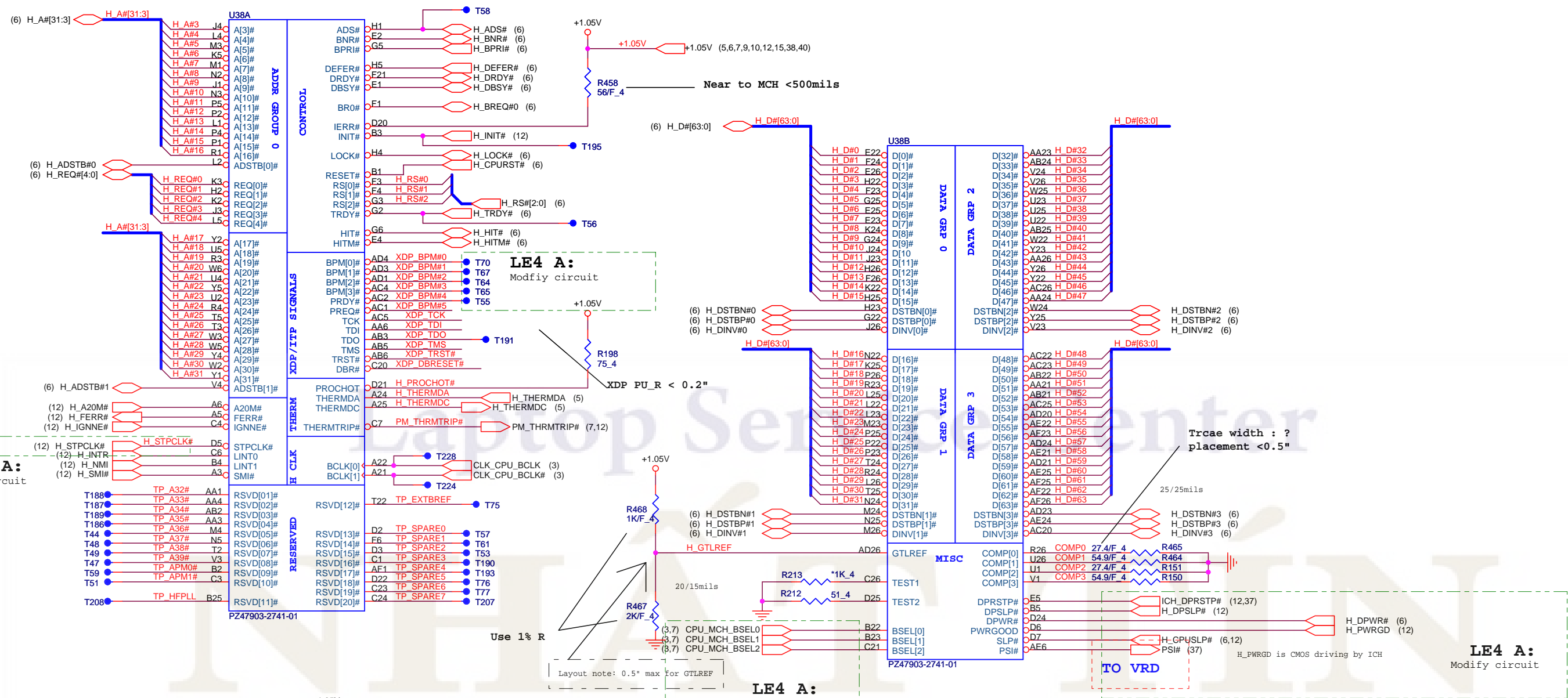


Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.



LE4 A:
Add Cap 10p reserve for EMI E-mail 093020051211

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LE4 A: Modify circuit

Use 1% R

Layout note: 0.5" max for GTLREF

LE4 A: Modify circuit

LE4 B: Add R235 in BOM

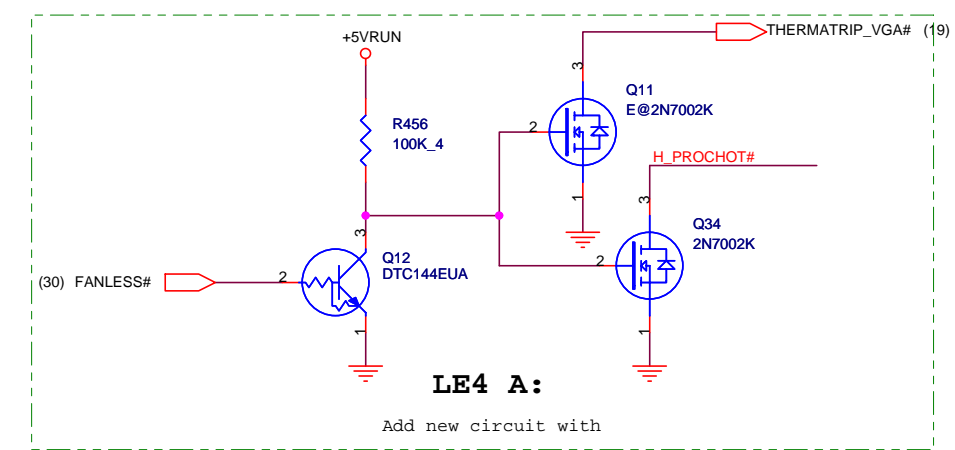
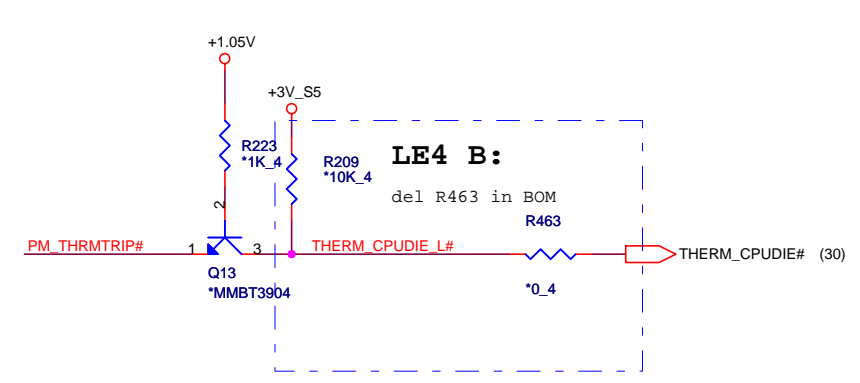
LE4 A: Modify circuit

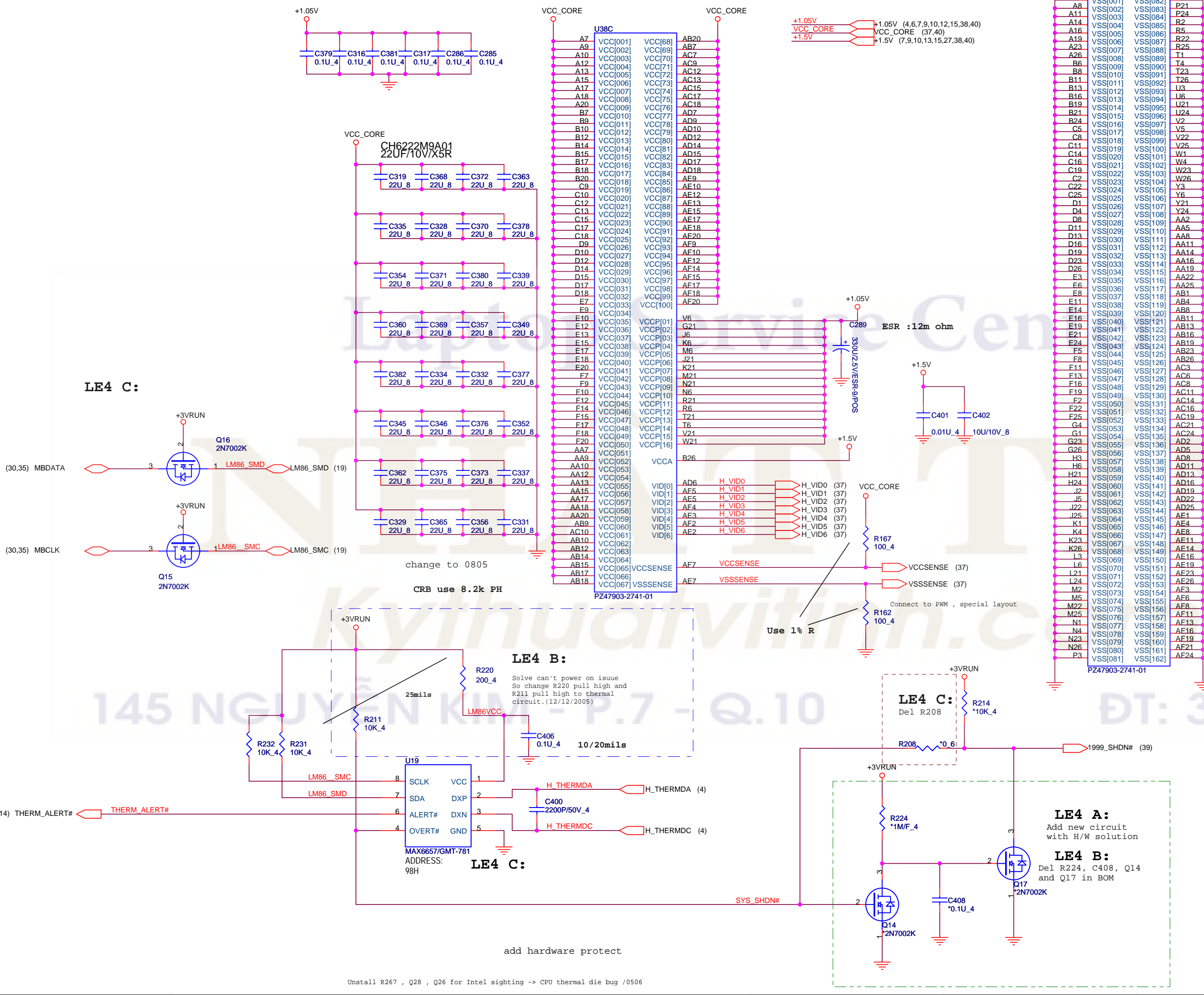
XDP PU_R < 0.2"

Why BMP5 need PH ?

XDP_TCK PD 27.4/1% ?
 XDP_TRST PD 510ohm /5% ?
 XDP_TDI PU 150ohm /1.05V
 XDP_TMS PU 39.2/1%?
 XDP_TDO PU 54.9ohm?
 For ITP700

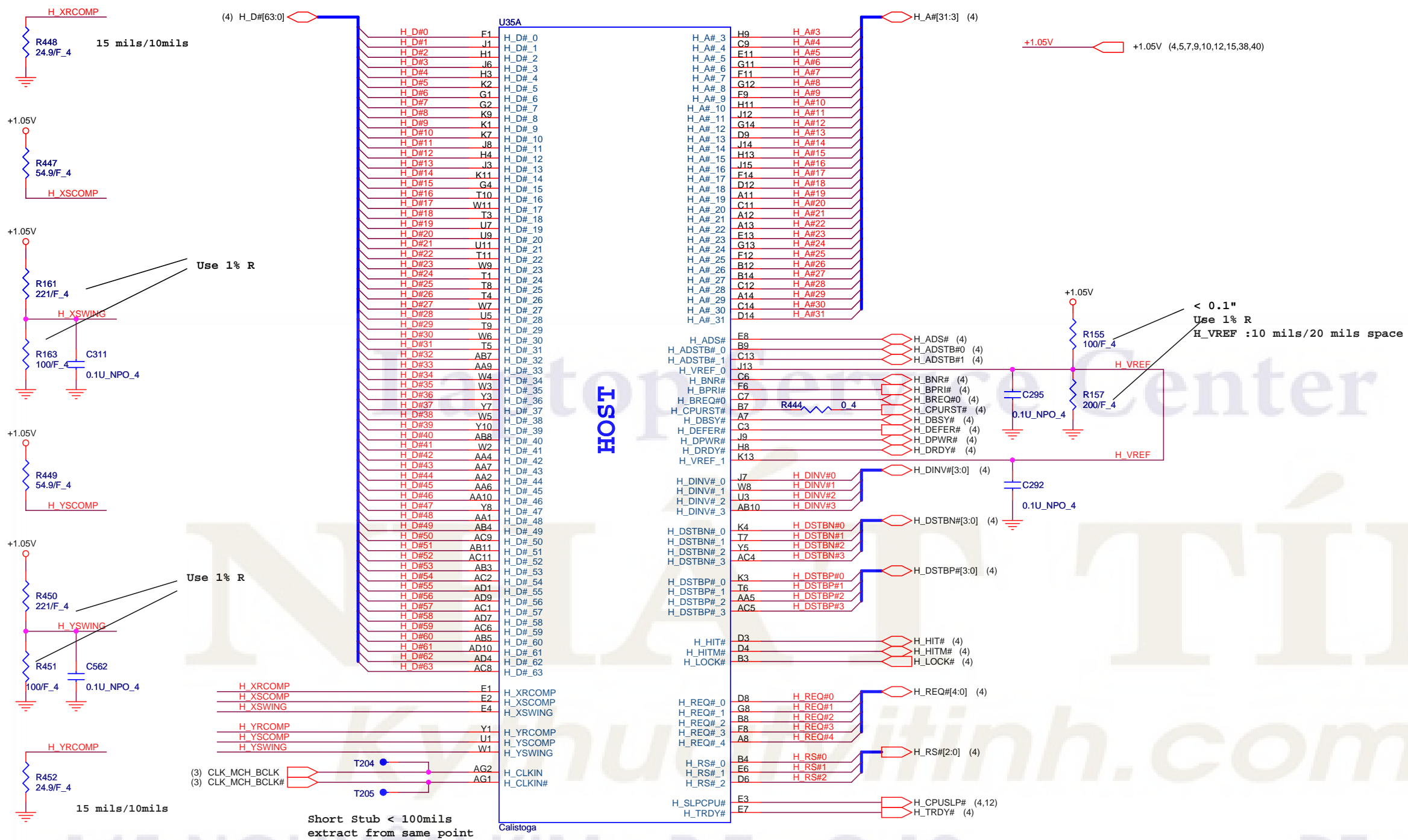
LE4 B: Change netname





PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Yonah/Merom (Power/NC)	1A
Date:	Tuesday, March 14, 2006	Sheet 5 of 42

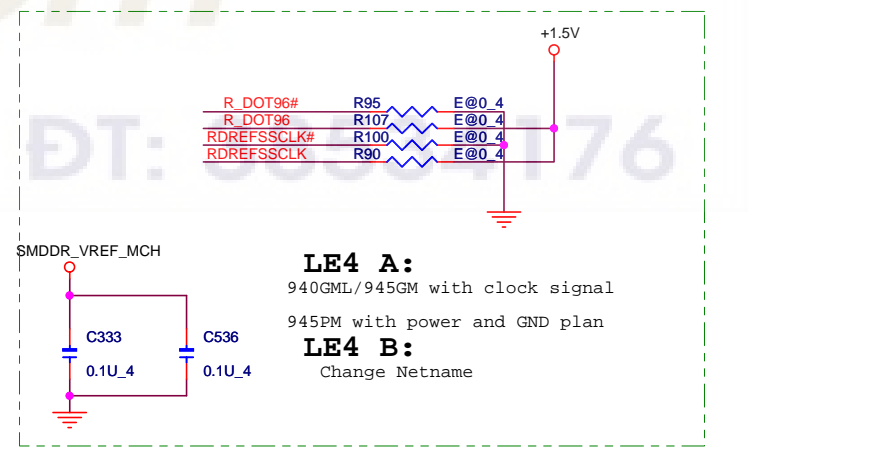
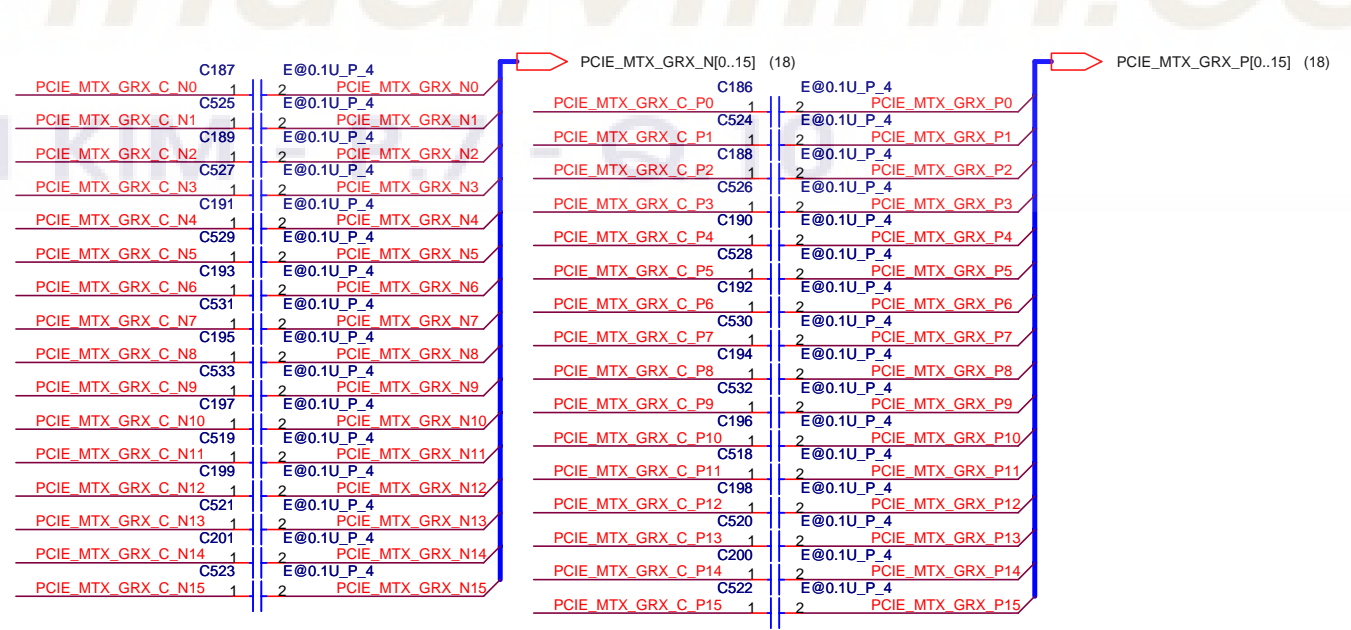
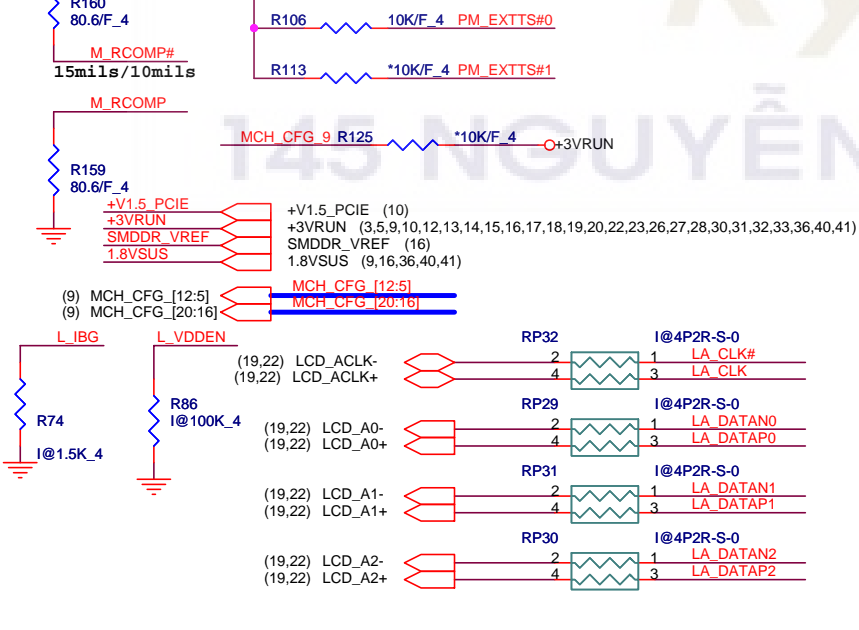
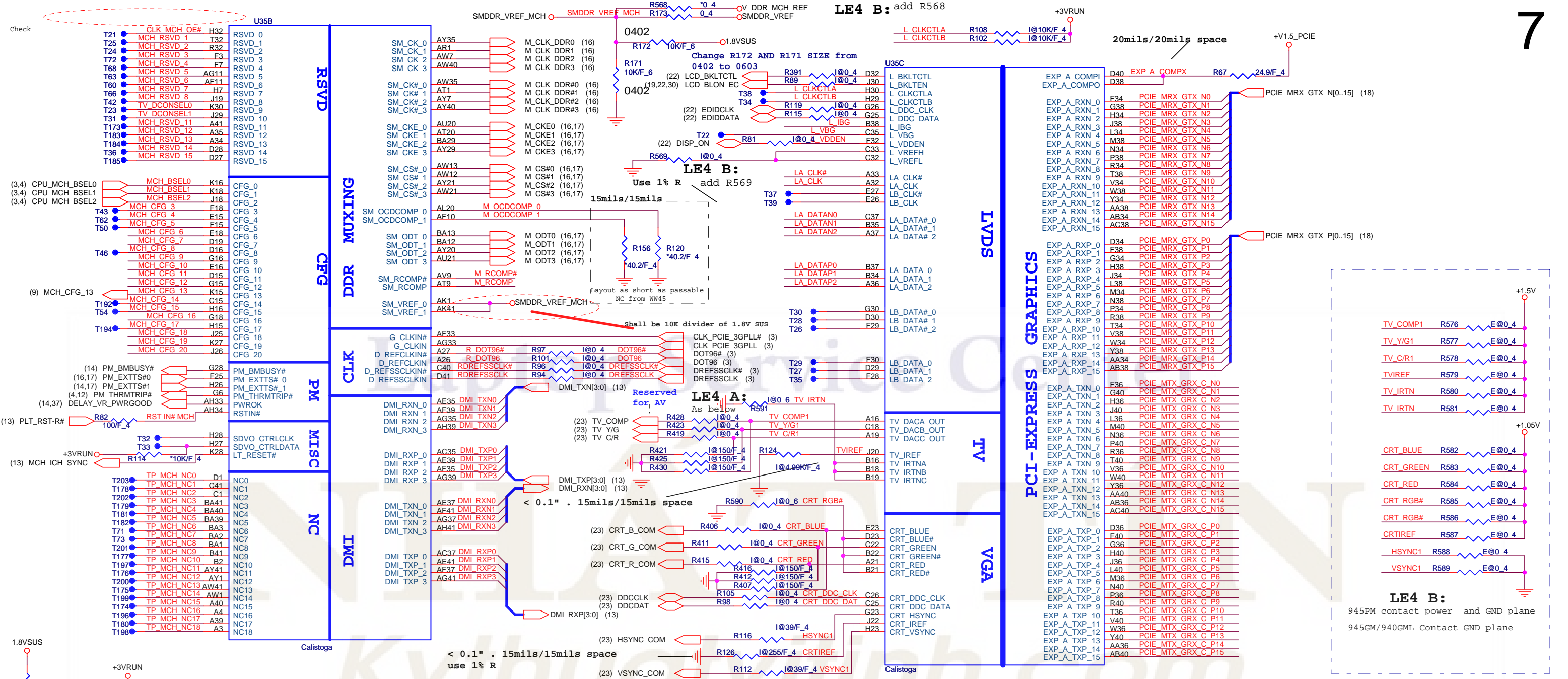


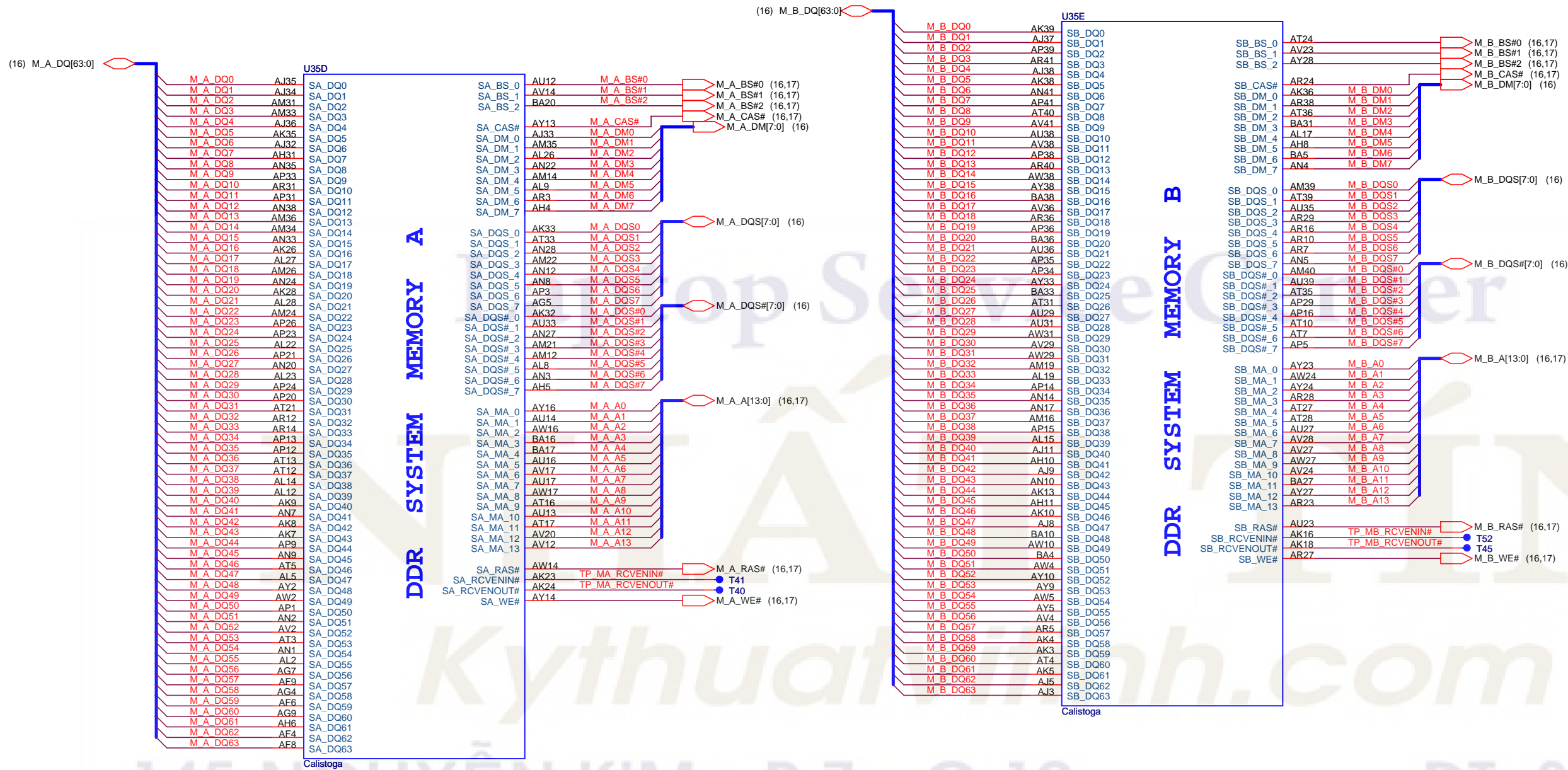
145 NGUYEN KIM - P.7 - Q.10

ĐT: 38534176

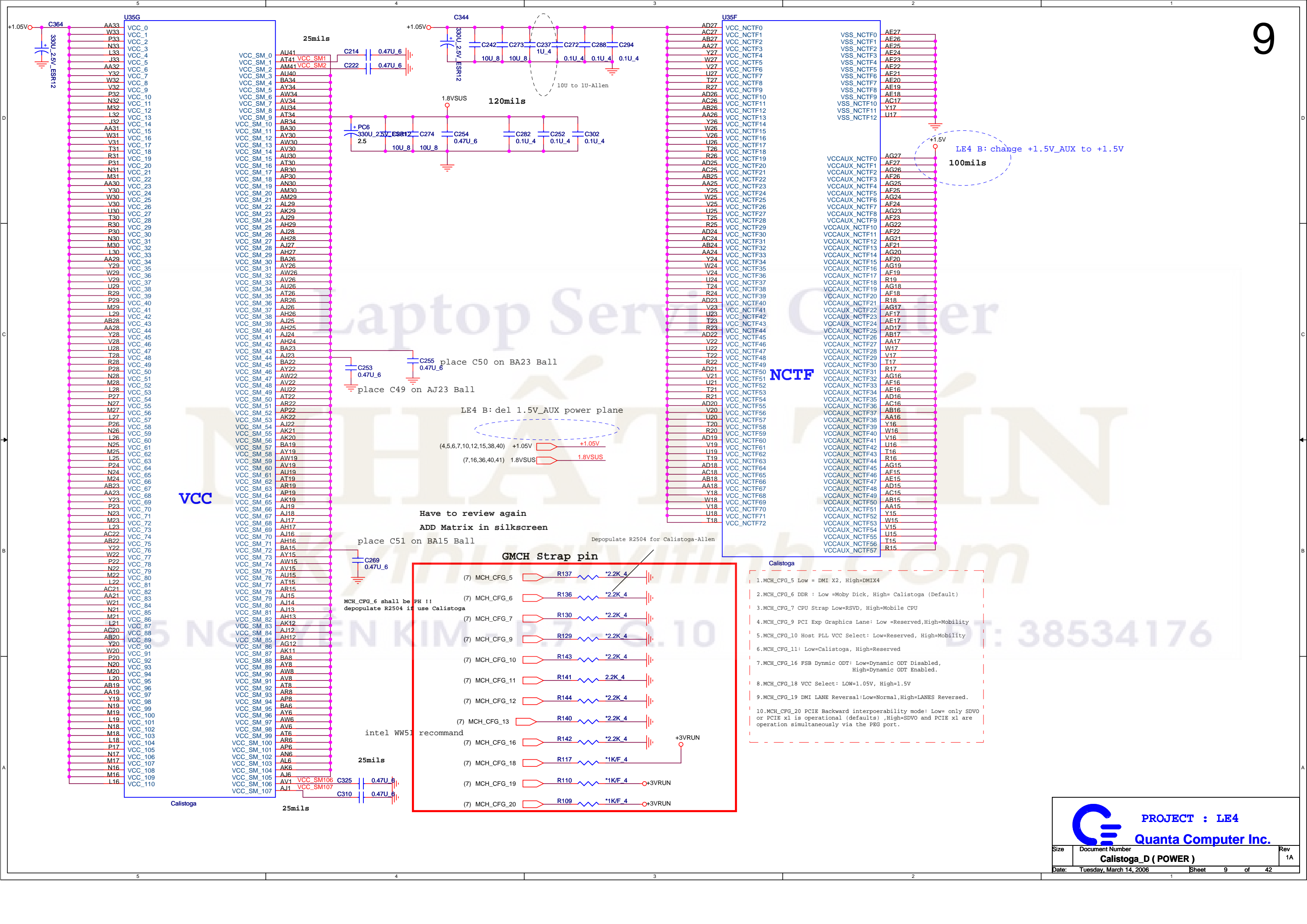
PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_A (Host)	1A
Date:	Tuesday, March 14, 2006	Sheet 6 of 42



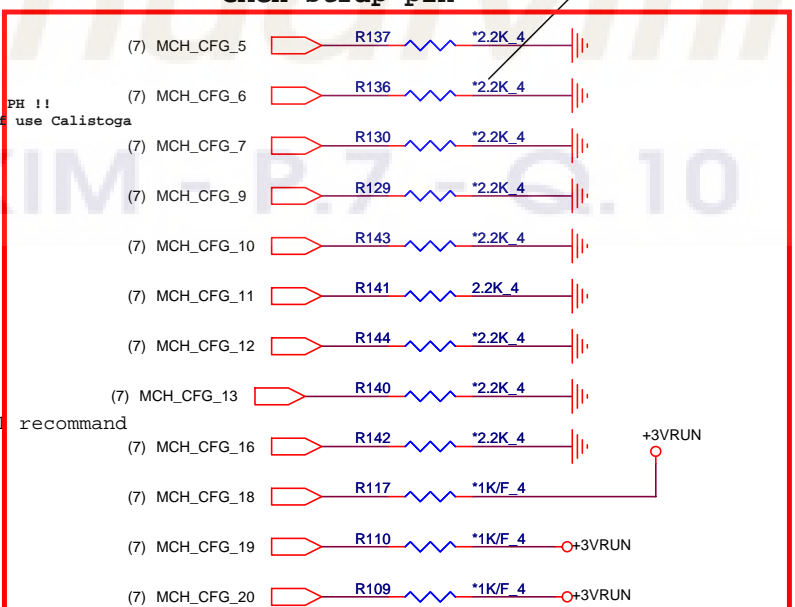


145 NGUYỄN KIM - P.7 - Q.10 DT: 38534176



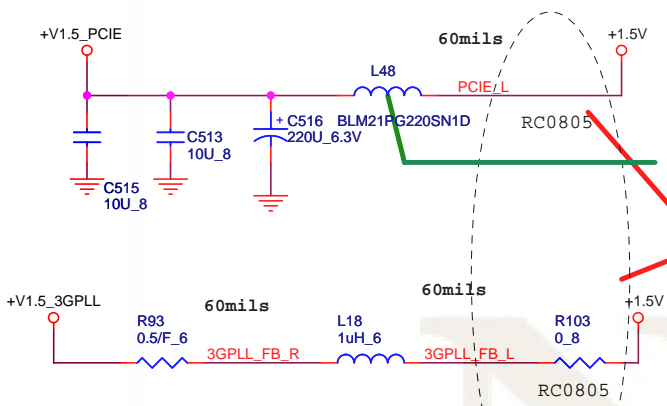
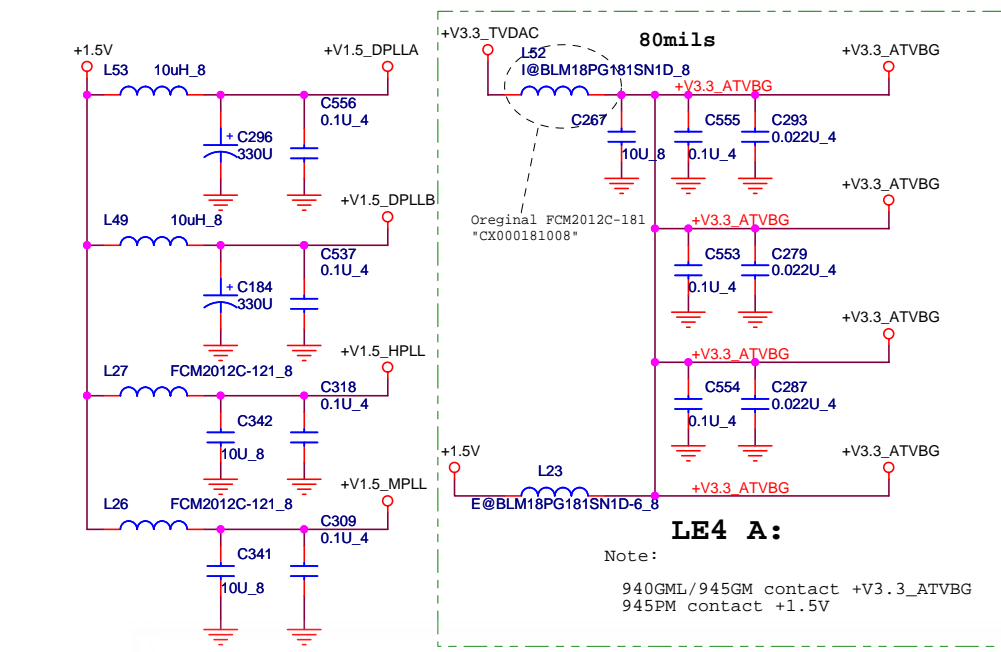
VCC

NCTF

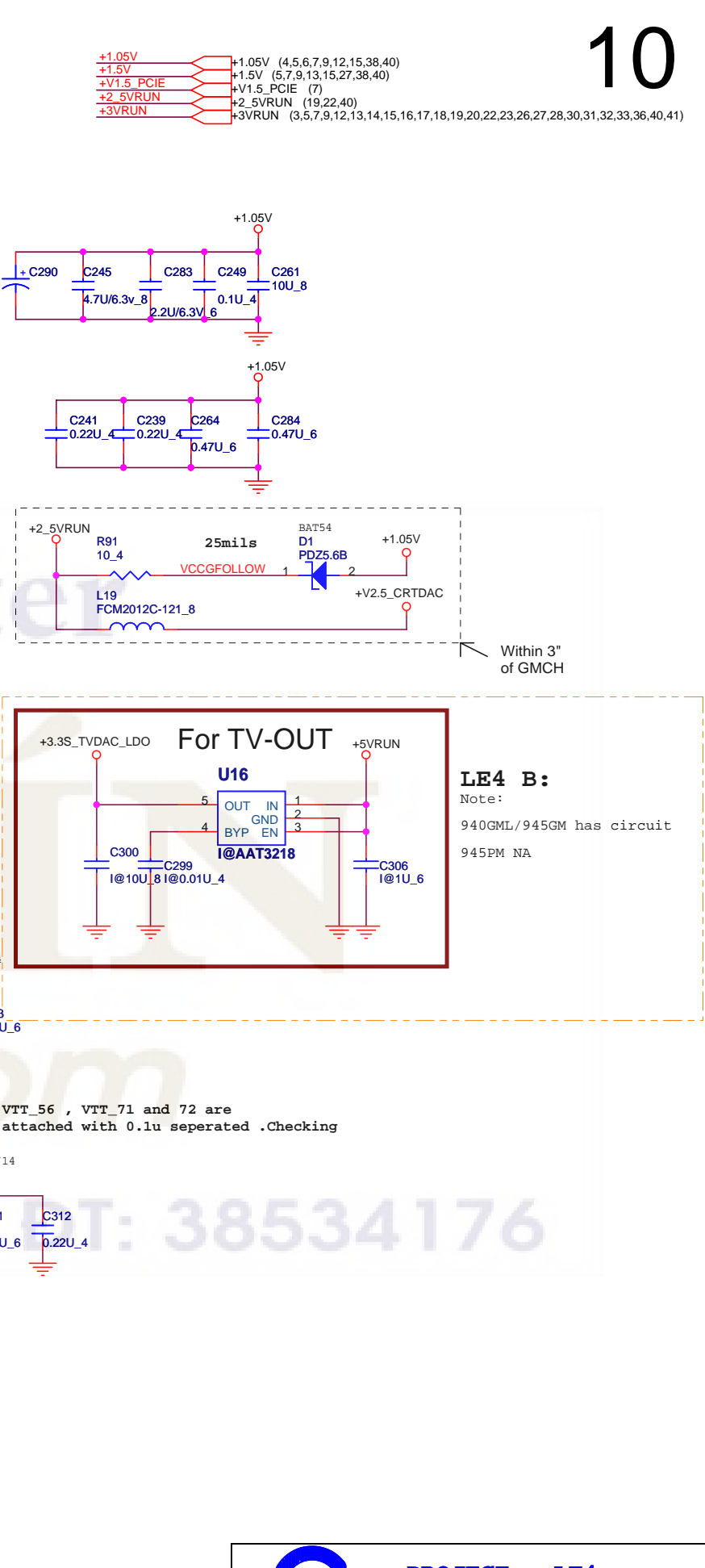
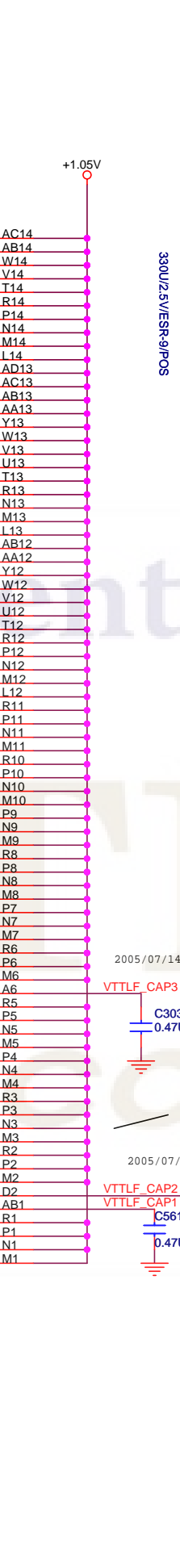
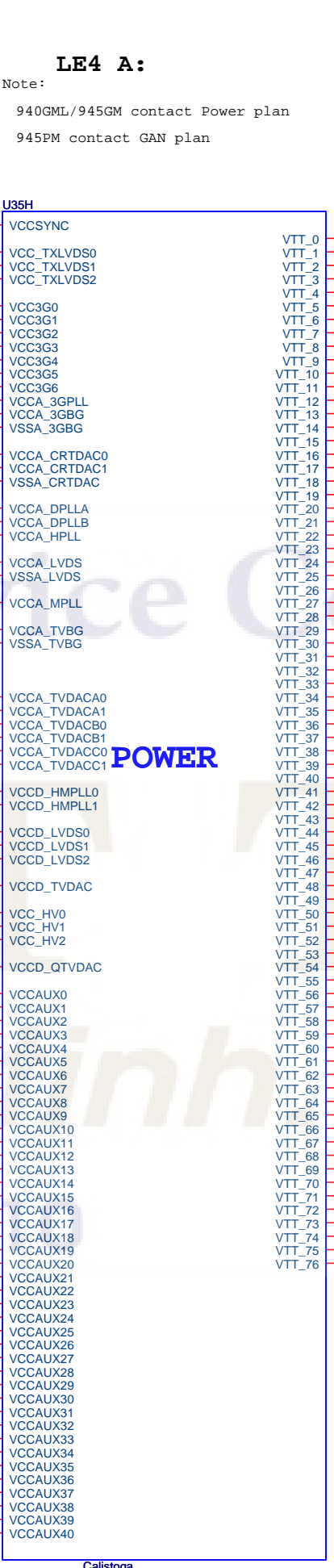
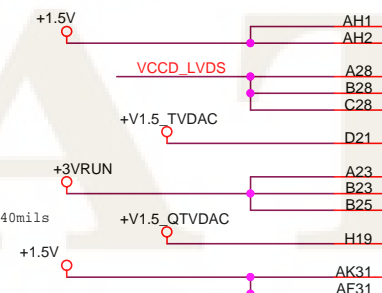
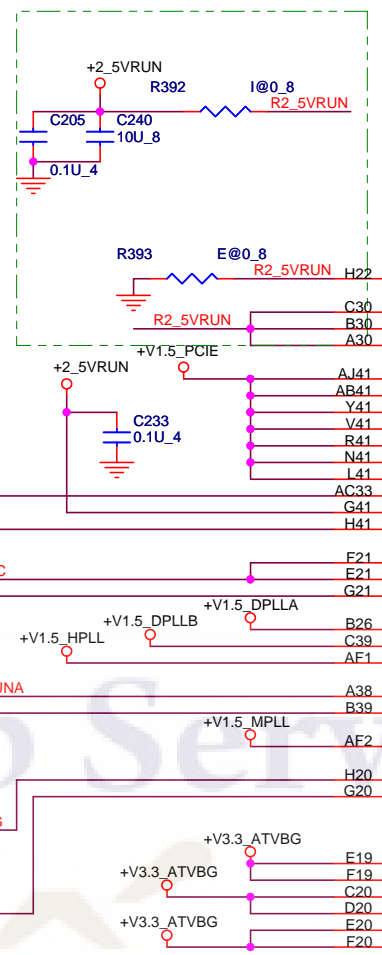
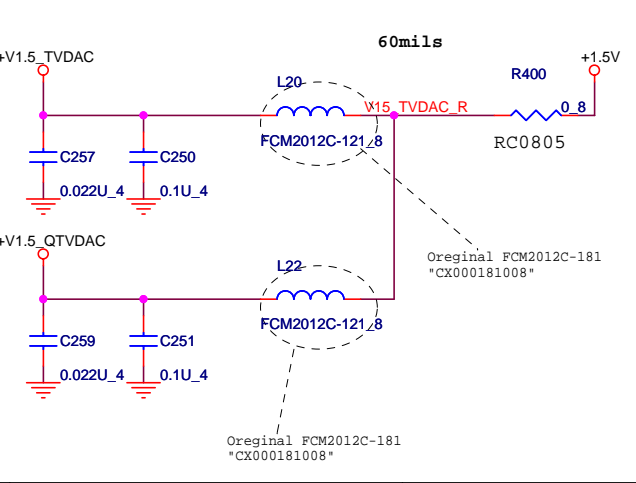
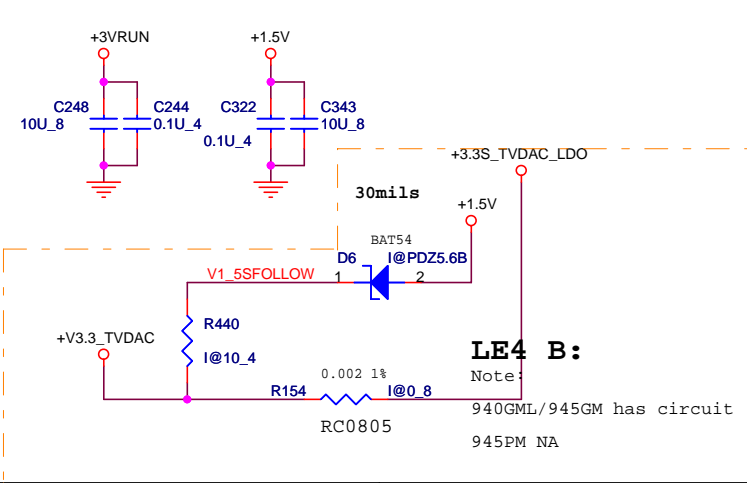
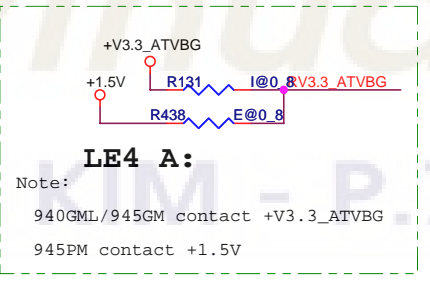
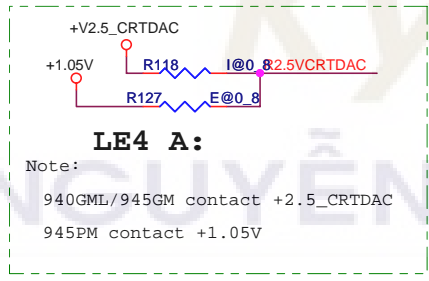
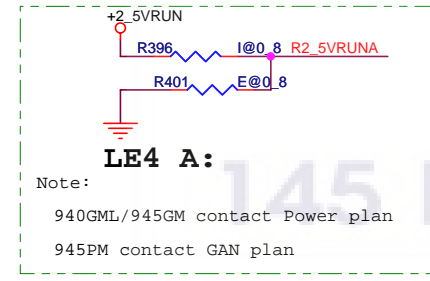
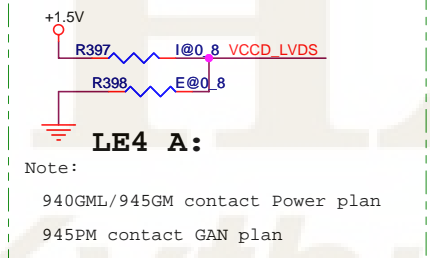


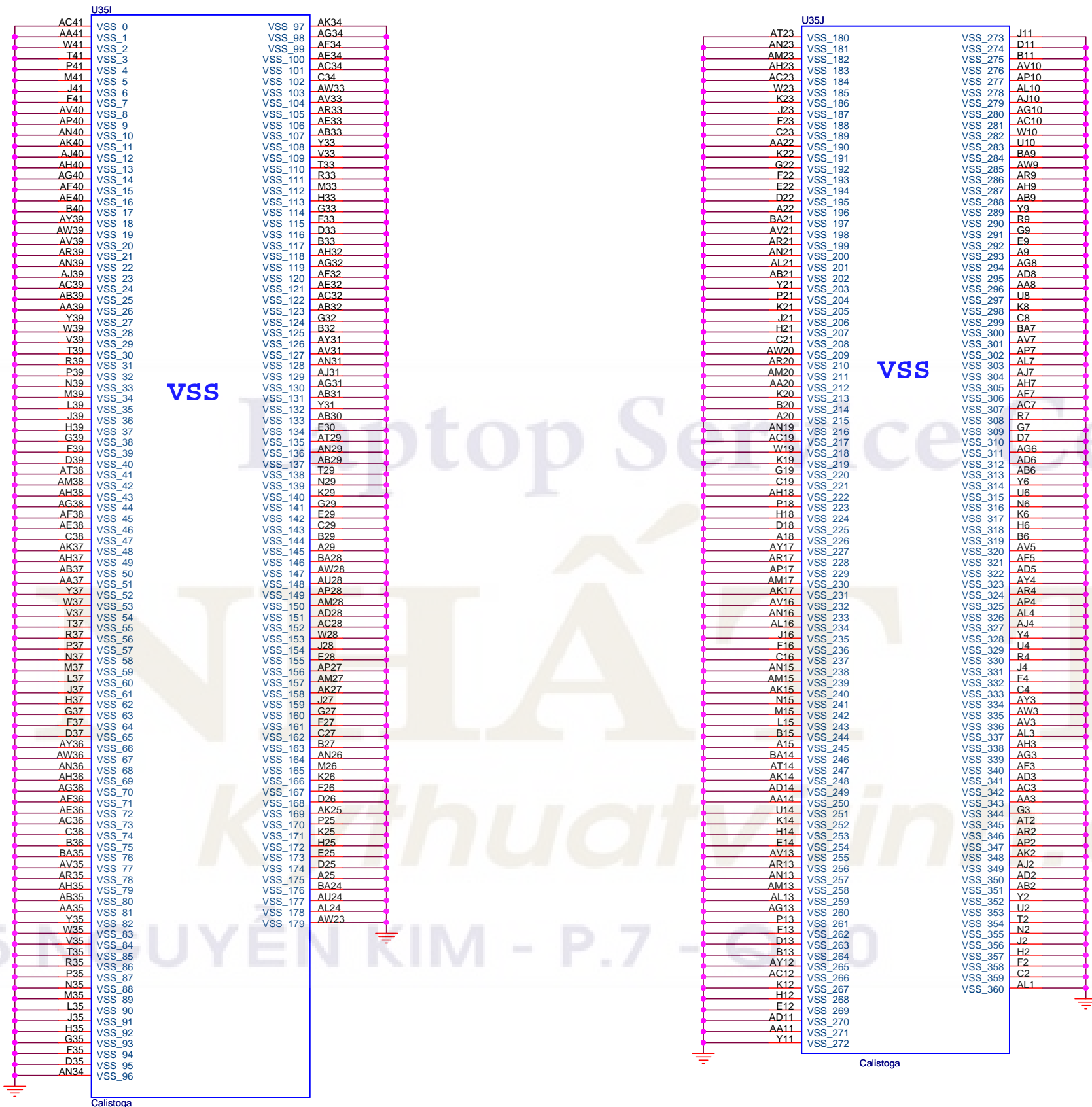
Calistoga

- MCH_CFG_5 Low = DMI X2, High=DMIX4
- MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
- MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
- MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
- MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- MCH_CFG_11: Low=Calistoga, High=Reserved
- MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
- MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- MCH_CFG_20 PCIe Backward interoperability mode: Low= only SDVO or PCIe x1 is operational (defaults) ,High=SDVO and PCIe x1 are operation simultaneously via the PEG port.



LE4 B: del R111, C246
change +1.5V_AUX to 1.5V





VSS

VSS

Calistoga

Calistoga

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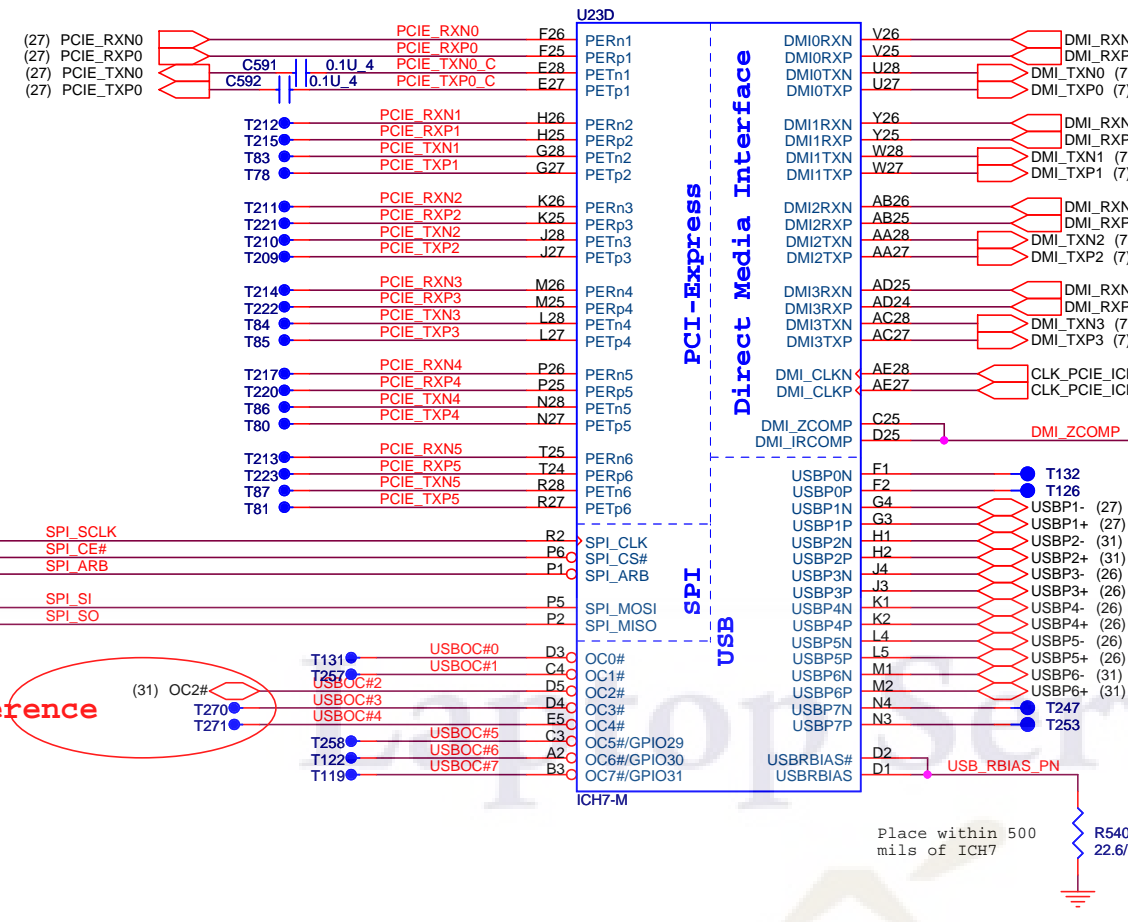


PROJECT : LE4
Quanta Computer Inc.

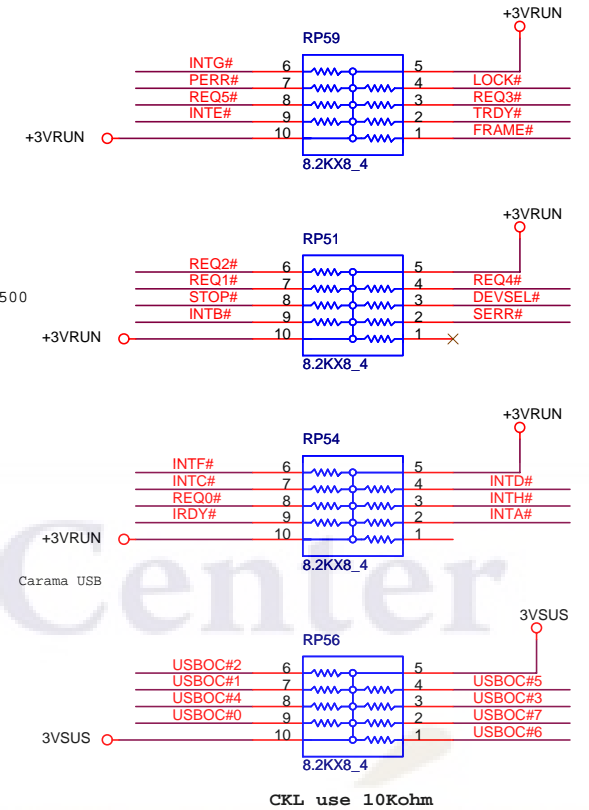
Size	Document Number	Rev
	Calistoga_F (VSS NCTF)	1A
Date:	Wednesday, November 16, 2005	Sheet 11 of 42

MINI CARD PCI-E

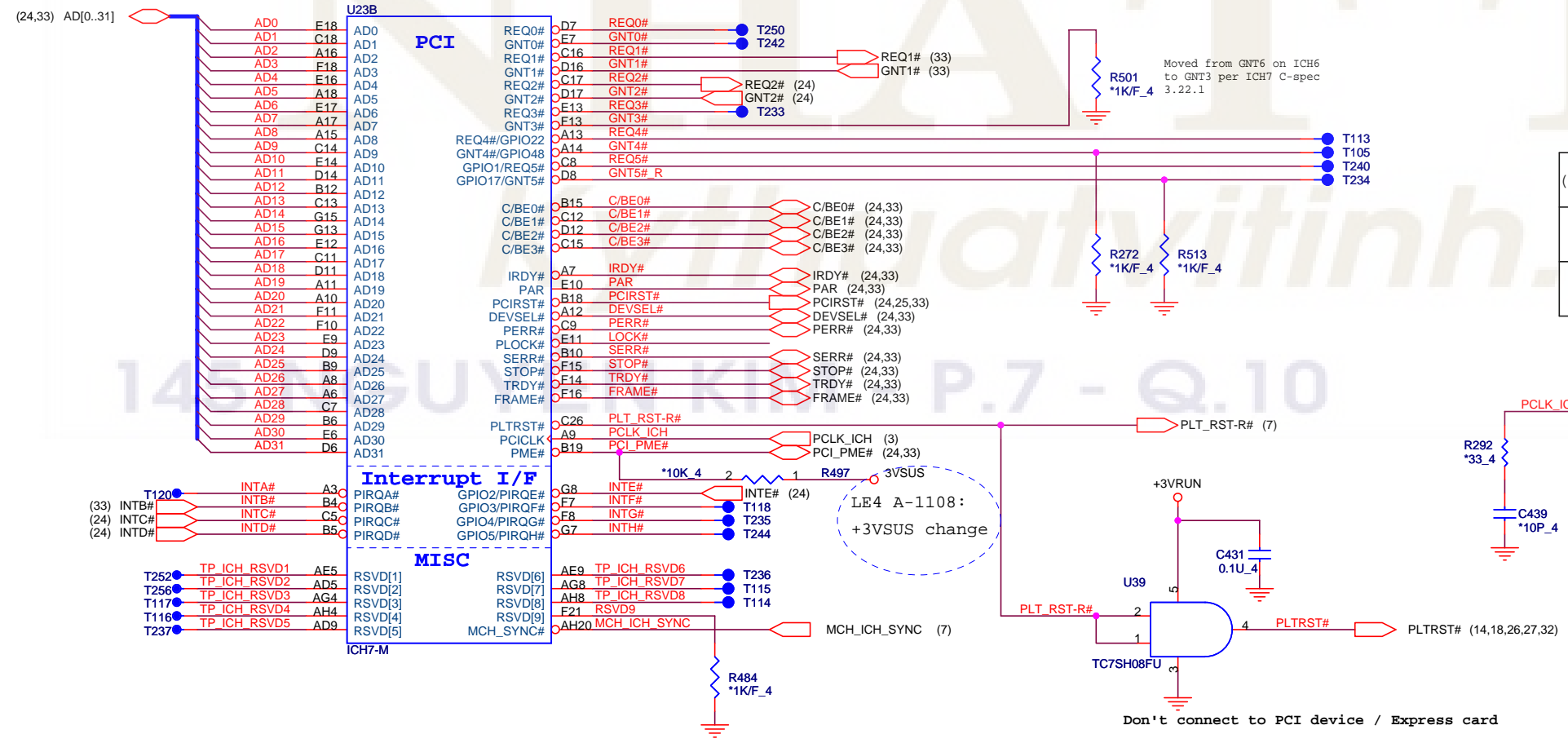
EXPRESS CARD (NEW CARD)



- Bluetooth Module
- Mini PCI e
- MB USB
- IO USB
- IO USB
- IO USB W/O DSUB
- FINGER PRINT
- Can't this USB port spec. for Lenovo
- 25mils/15mils



Difference (31) OC2#



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

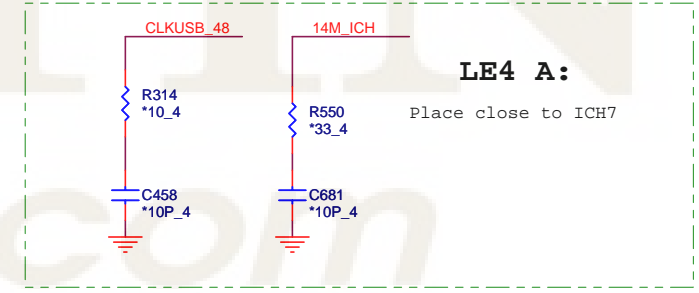
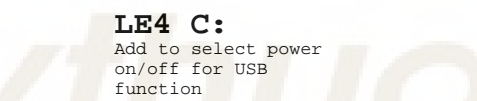
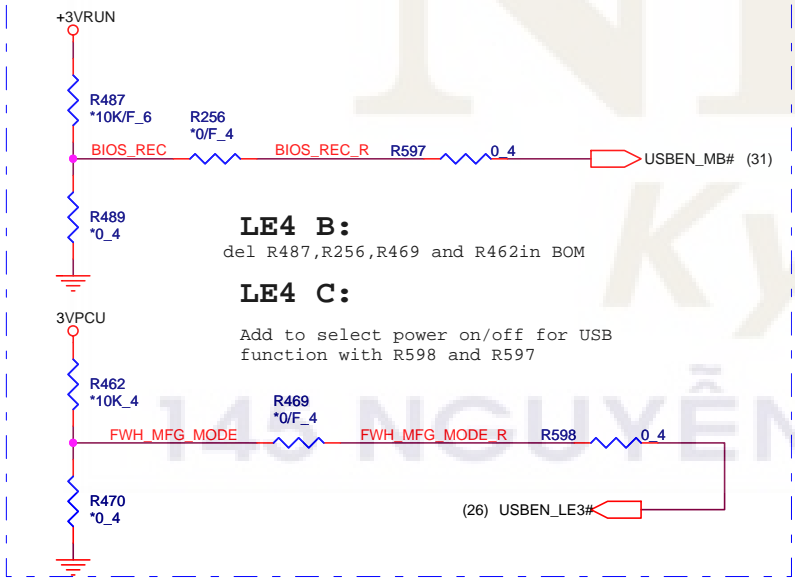
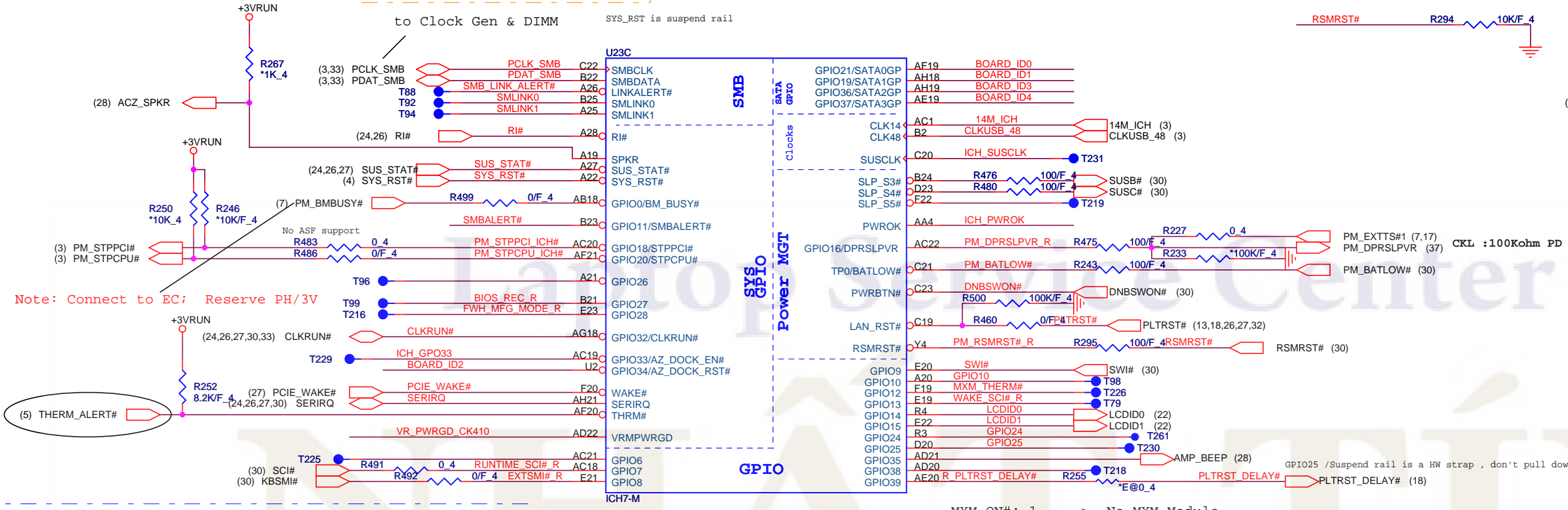
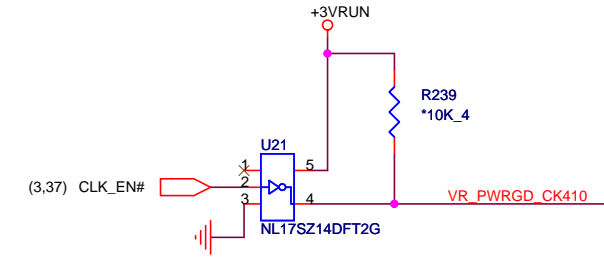
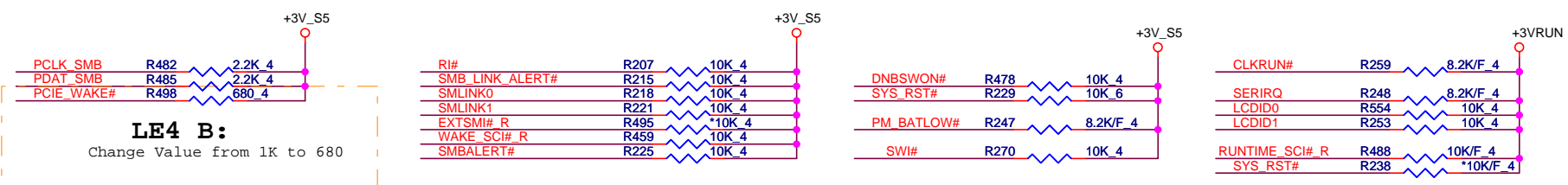
DT: 38534176

PROJECT : LE4
Quanta Computer Inc.

Size Document Number Rev
ICH7-M PCI E (2 of 4) 1A

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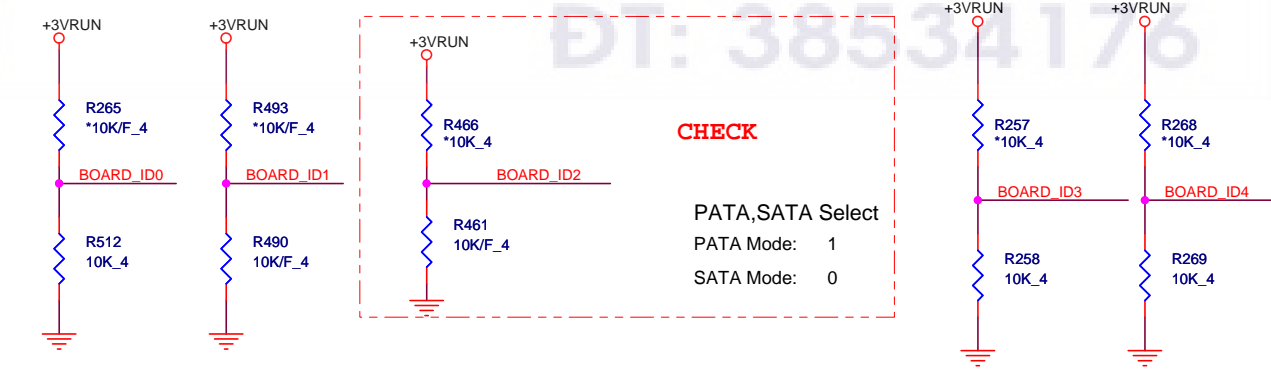
R376
No stuff-->boot
Stuff-->No boot



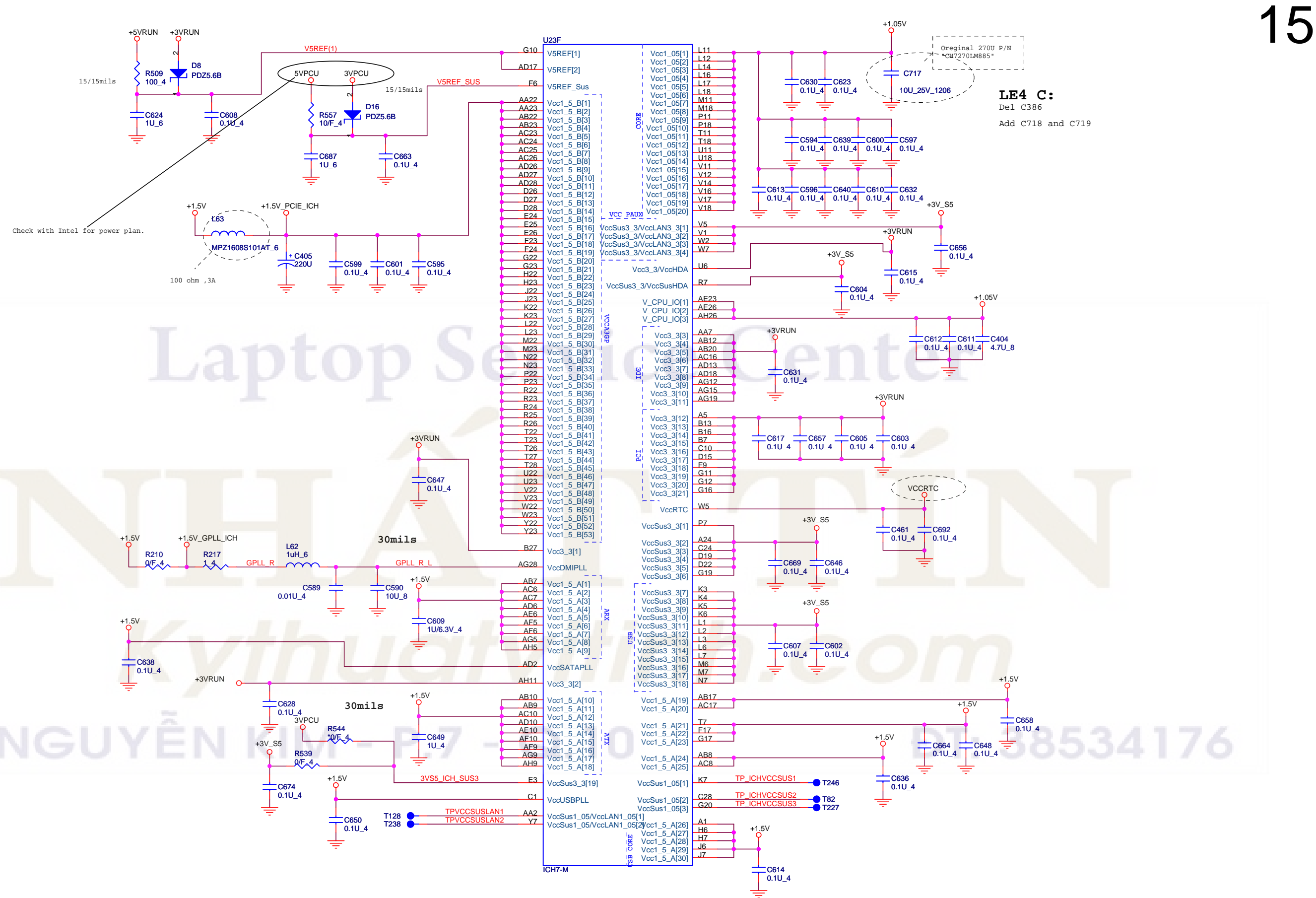
BOARD_ID0 GPIO21	BOARD_ID1 GPIO19	BOARD_ID2 GPIO34	BOARD_ID3 GPIO36	BOARD_ID4 GPIO37
L	L	L	L	L
L	L	L	L	H

LE3--L
LE4--H

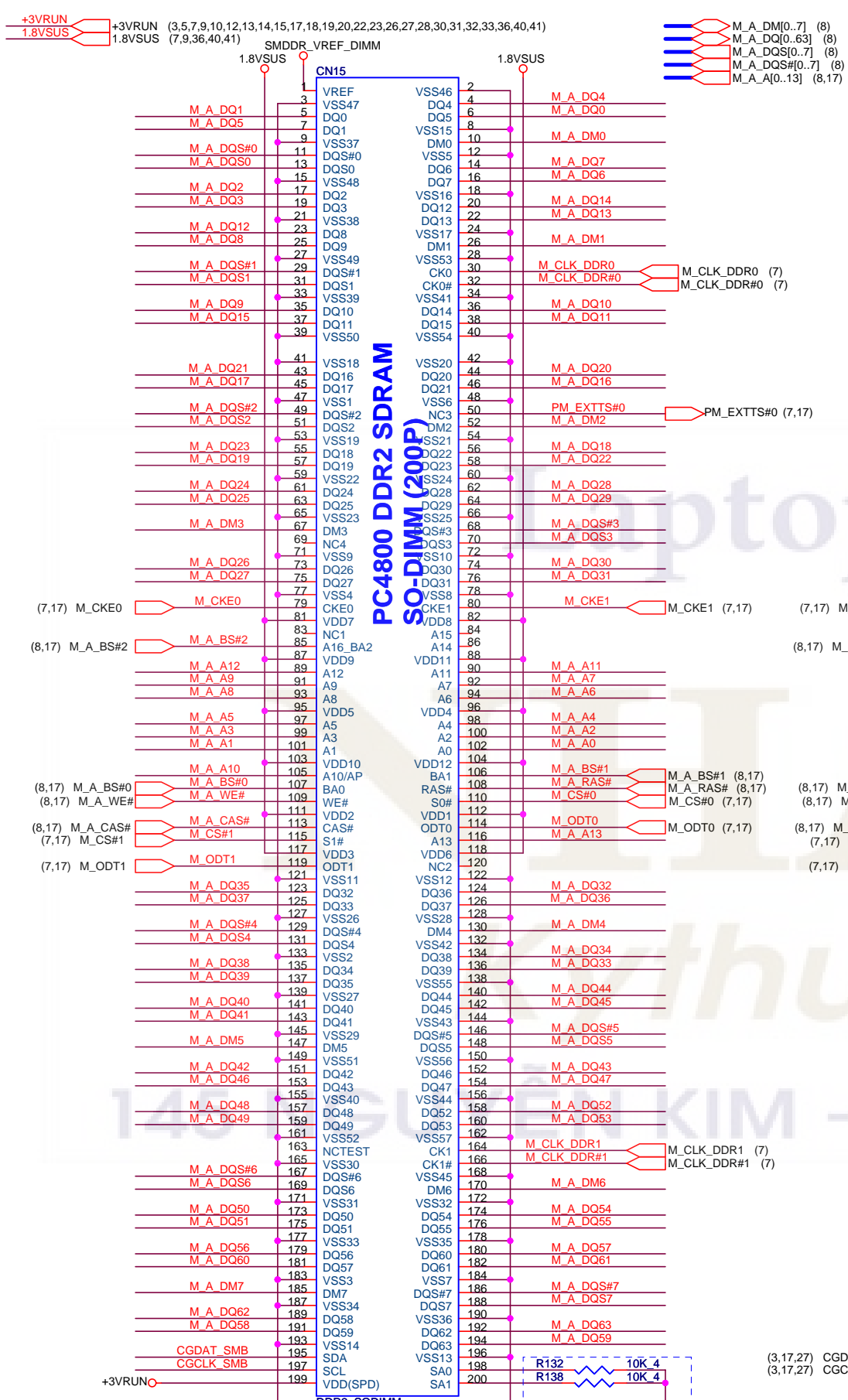
Level is incorrect !!



A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G8	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB11
J5	VSS[49]	VSS[146]	AB14
J24	VSS[50]	VSS[147]	AB16
J25	VSS[51]	VSS[148]	AB19
J26	VSS[52]	VSS[149]	AB21
K24	VSS[53]	VSS[150]	AB24
K27	VSS[54]	VSS[151]	AB27
K28	VSS[55]	VSS[152]	AB28
L13	VSS[56]	VSS[153]	AC2
L15	VSS[57]	VSS[154]	AC5
L24	VSS[58]	VSS[155]	AC9
L25	VSS[59]	VSS[156]	AC11
L26	VSS[60]	VSS[157]	AD1
M3	VSS[61]	VSS[158]	AD3
M4	VSS[62]	VSS[159]	AD4
M5	VSS[63]	VSS[160]	AD7
M12	VSS[64]	VSS[161]	AD8
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD15
M15	VSS[67]	VSS[164]	AD19
M16	VSS[68]	VSS[165]	AD23
M17	VSS[69]	VSS[166]	AE2
M24	VSS[70]	VSS[167]	AE4
M27	VSS[71]	VSS[168]	AE8
M28	VSS[72]	VSS[169]	AE11
N1	VSS[73]	VSS[170]	AE13
N2	VSS[74]	VSS[171]	AE18
N5	VSS[75]	VSS[172]	AE21
N6	VSS[76]	VSS[173]	AE24
N11	VSS[77]	VSS[174]	AE25
N12	VSS[78]	VSS[175]	AF2
N13	VSS[79]	VSS[176]	AF4
N14	VSS[80]	VSS[177]	AF8
N15	VSS[81]	VSS[178]	AF11
N16	VSS[82]	VSS[179]	AF27
N17	VSS[83]	VSS[180]	AF28
N18	VSS[84]	VSS[181]	AG1
N24	VSS[85]	VSS[182]	AG3
N25	VSS[86]	VSS[183]	AG7
N26	VSS[87]	VSS[184]	AG11
P3	VSS[88]	VSS[185]	AG14
P4	VSS[89]	VSS[186]	AG17
P12	VSS[90]	VSS[187]	AG20
P13	VSS[91]	VSS[188]	AG25
P14	VSS[92]	VSS[189]	AH1
P15	VSS[93]	VSS[190]	AH3
P16	VSS[94]	VSS[191]	AH7
P17	VSS[95]	VSS[192]	AH12
P24	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27



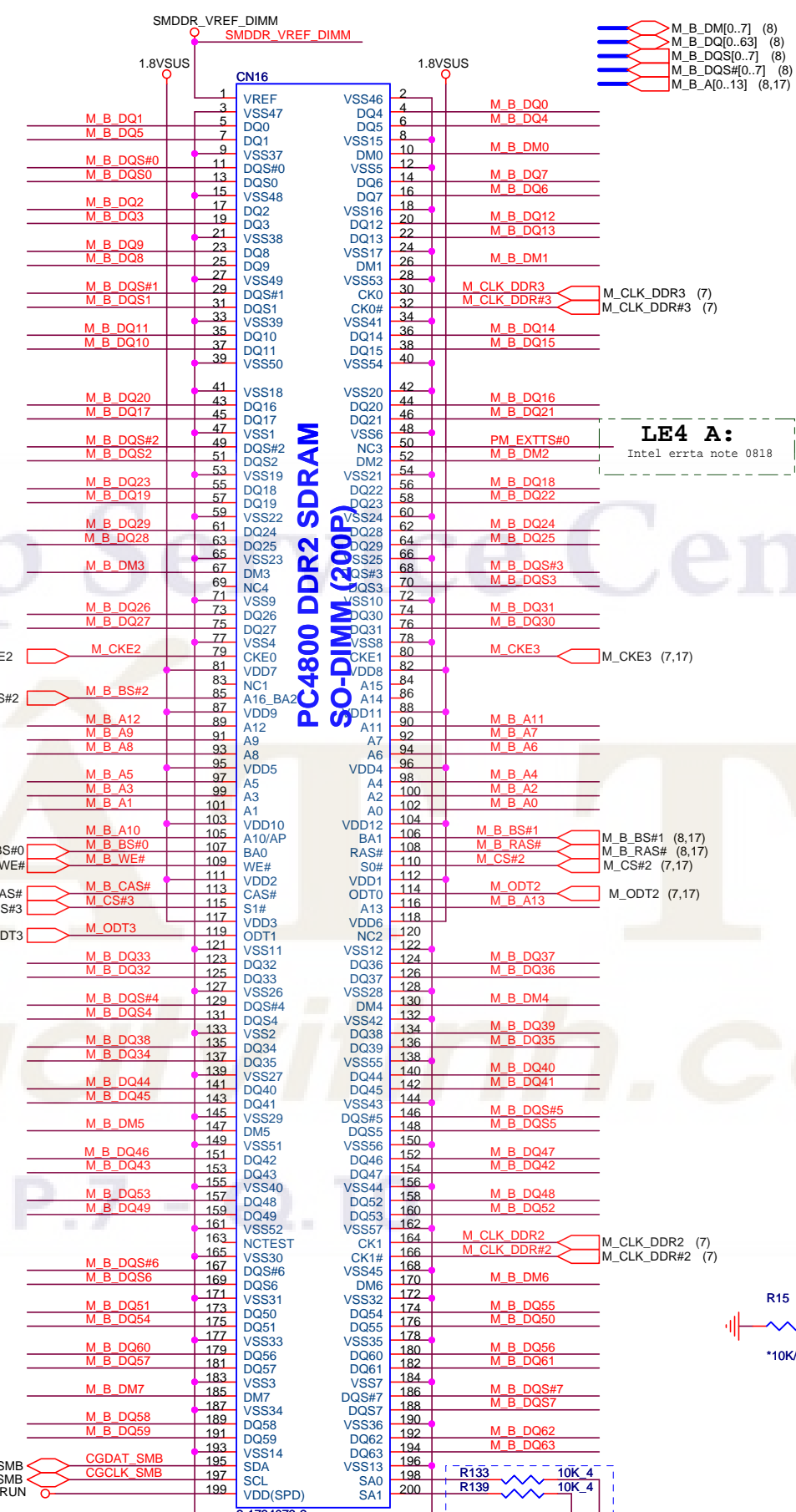
LE4 C:
Del C386
Add C718 and C719



**PC4800 DDR2 SDRAM
SO-DIMM (200P)**

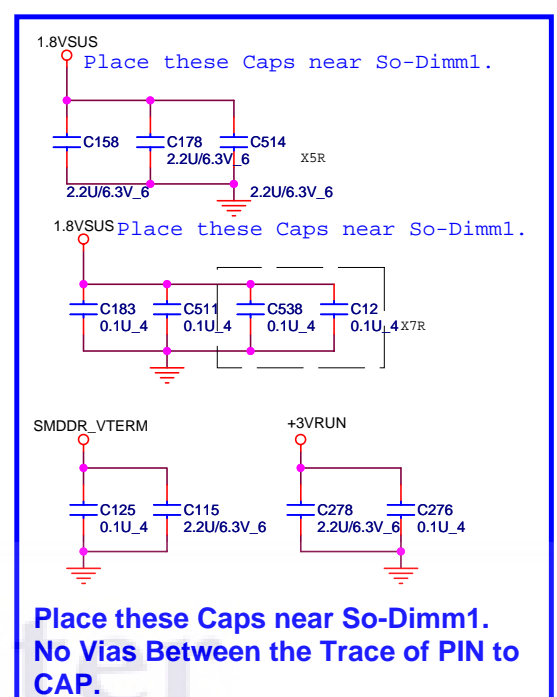
**CLOCK 0,1
CKE 0,1**
H 5.2

SMbus address A0

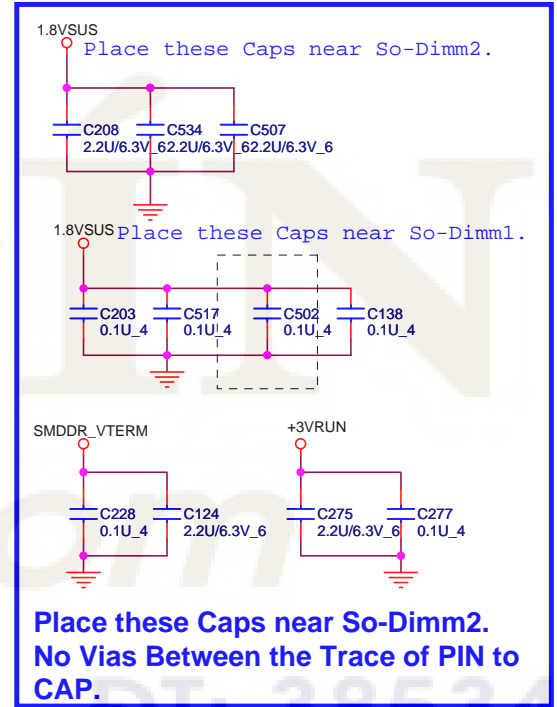


**CLOCK 3,4
CKE 2,3**
H 9.2

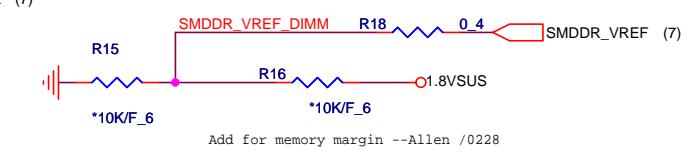
SMbus address A4



**Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.**



**Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.**



Add for memory margin --Allen /0228

LE4 A:
Intel errta note 0818

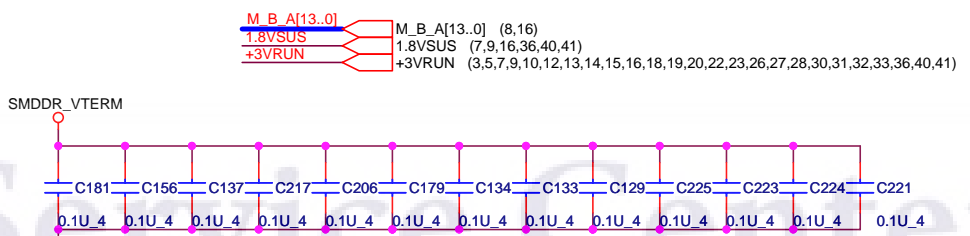
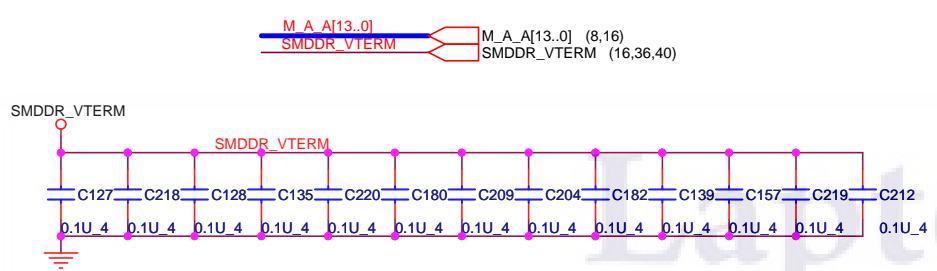
PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	DDR II SO-DIMM (200P)	1A
Date:	Tuesday, March 14, 2006	Sheet 16 of 42

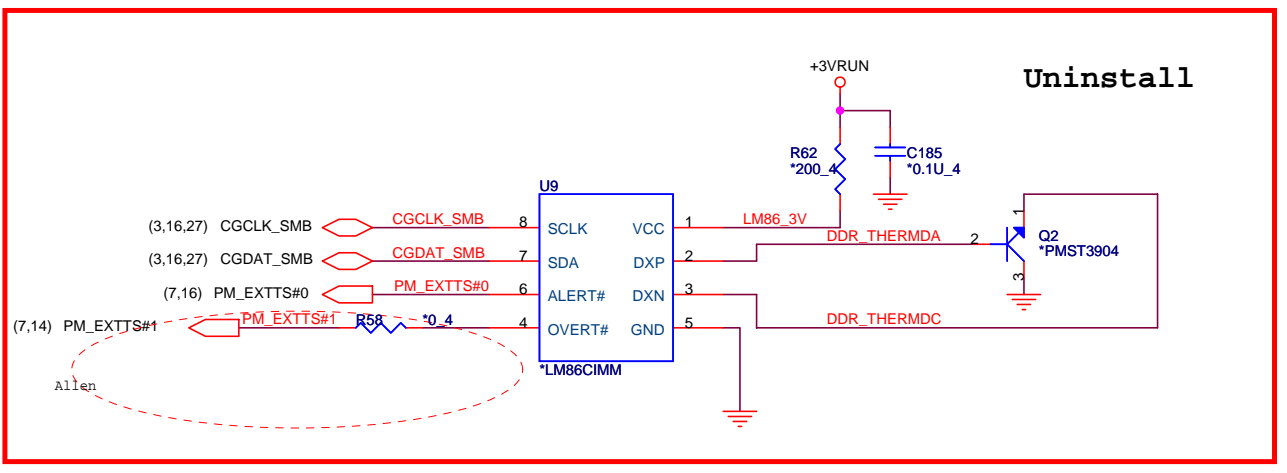
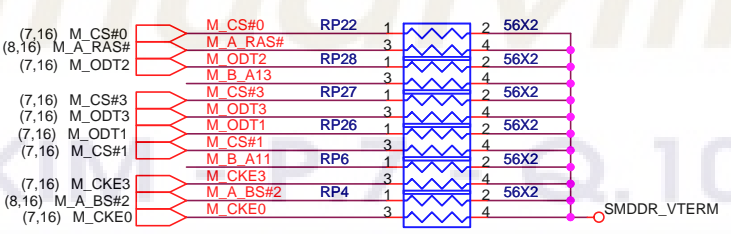
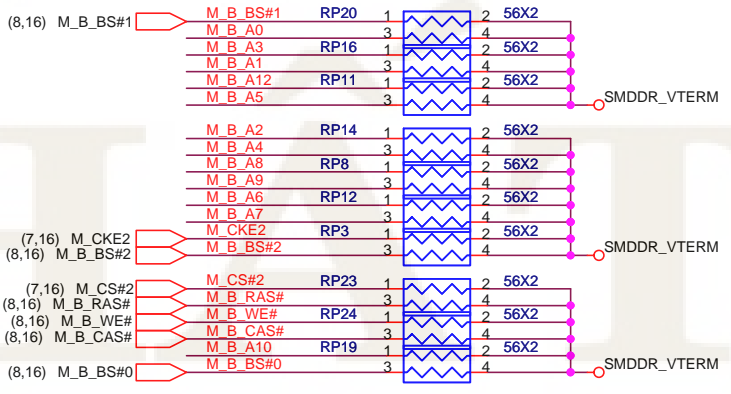
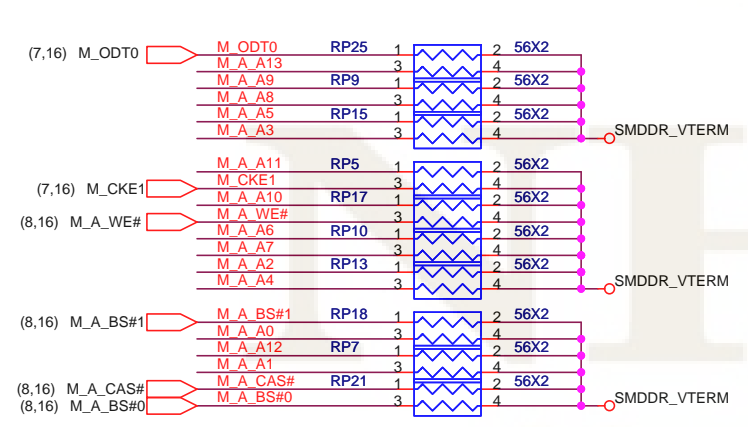
DDRII DUAL CHANNEL A,B.

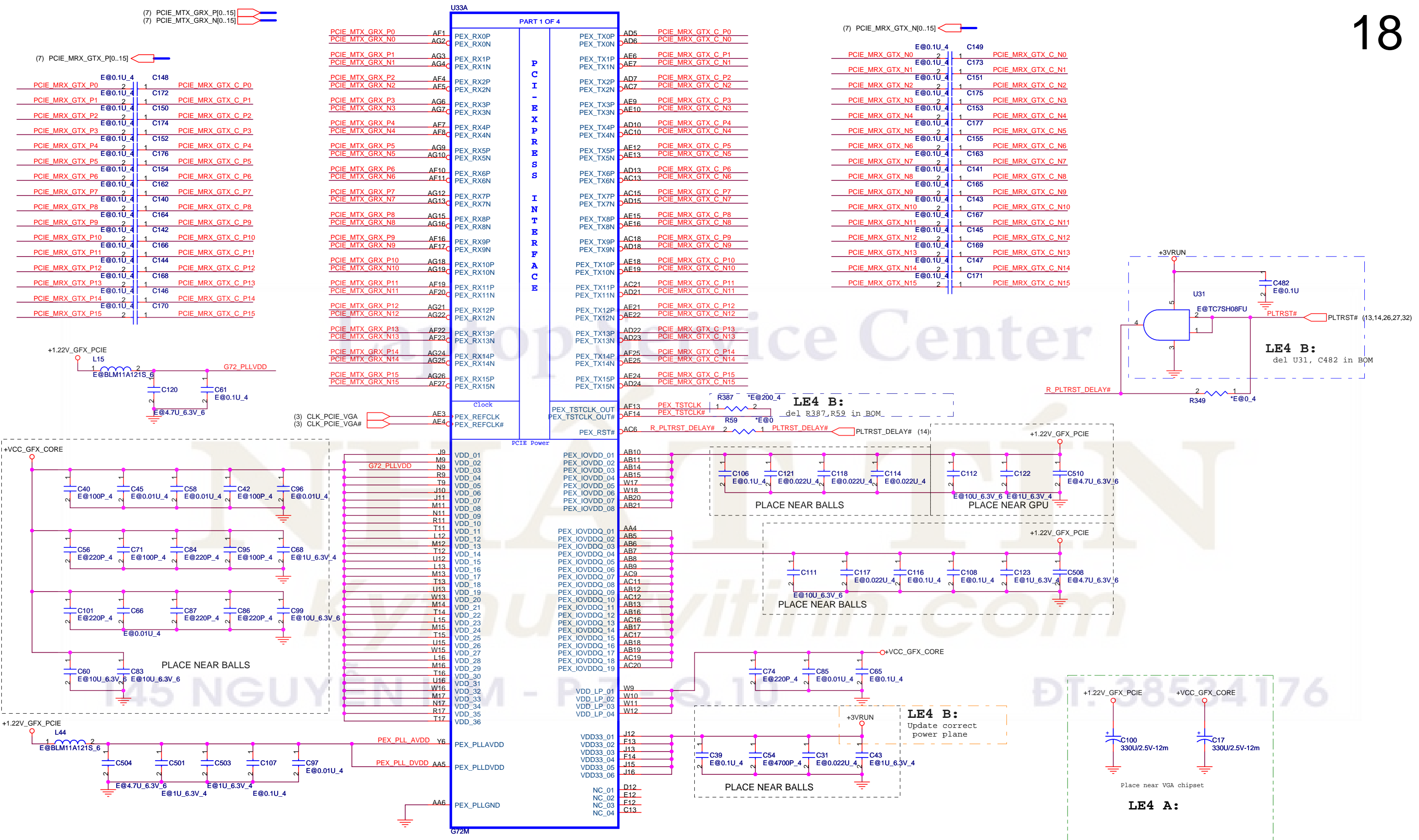
DDRII A CHANNEL

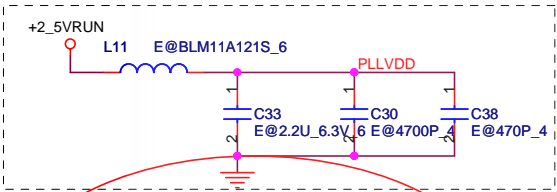
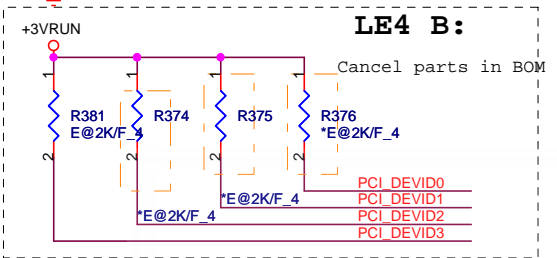
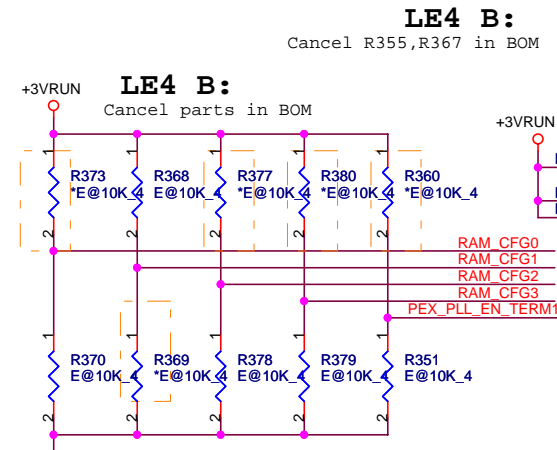
DDRII B CHANNEL



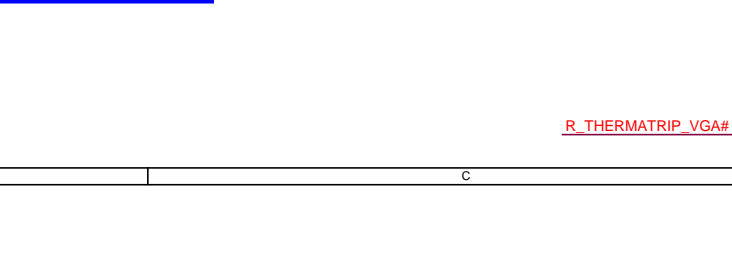
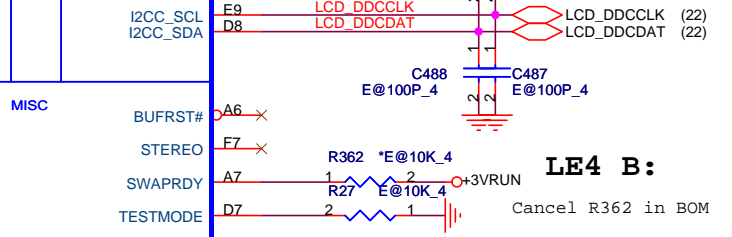
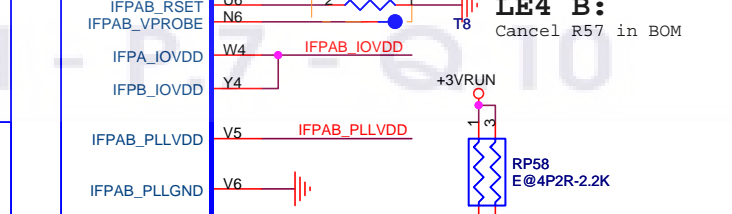
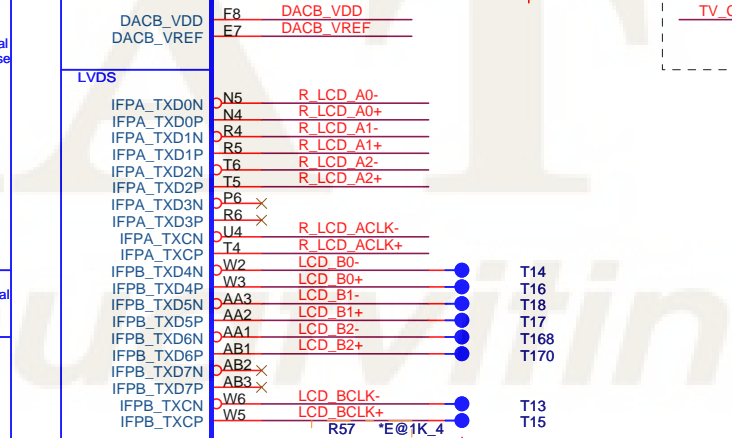
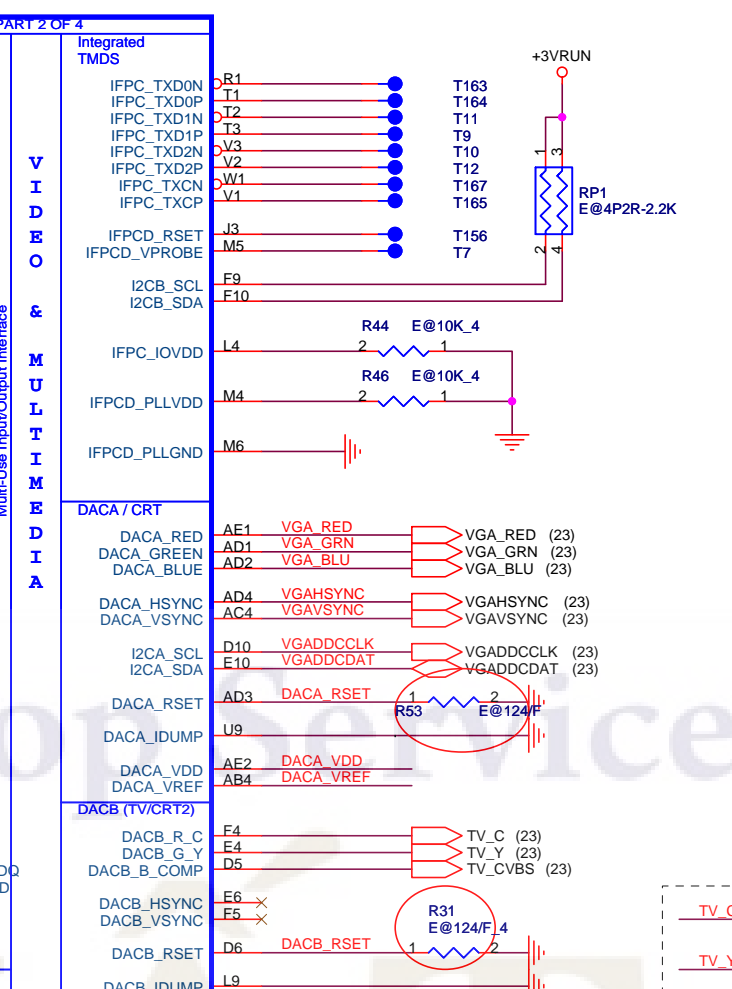
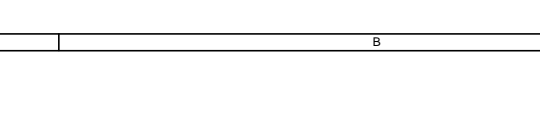
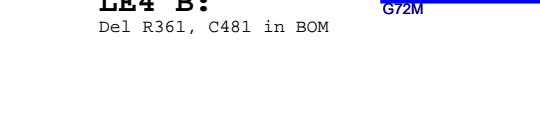
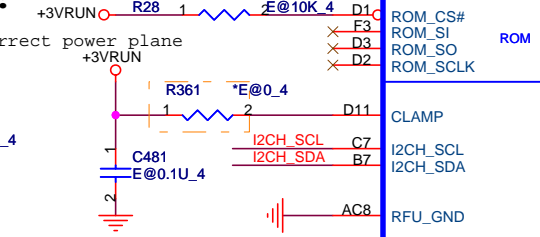
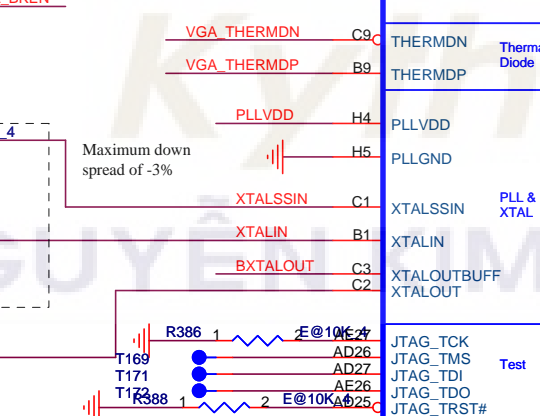
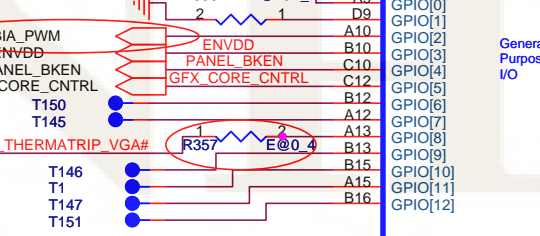
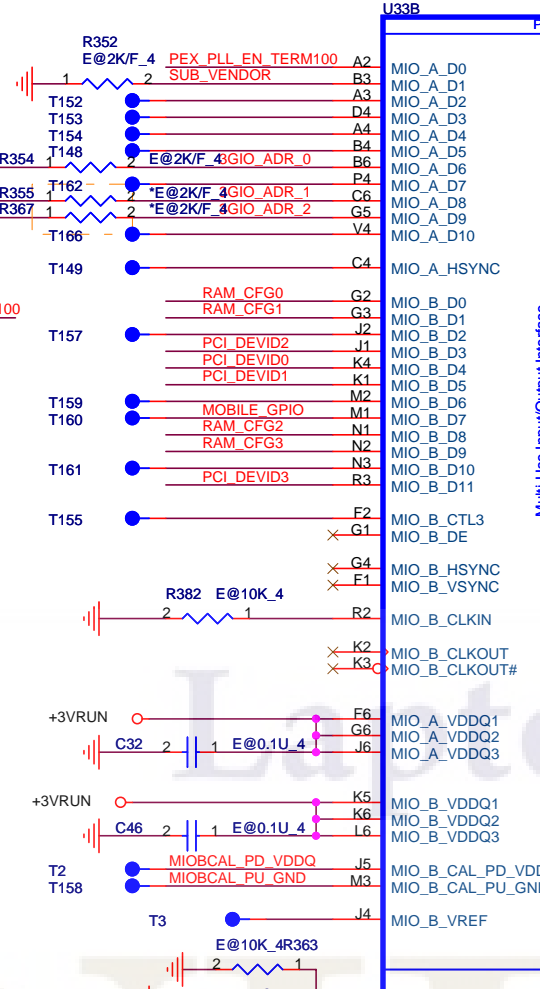
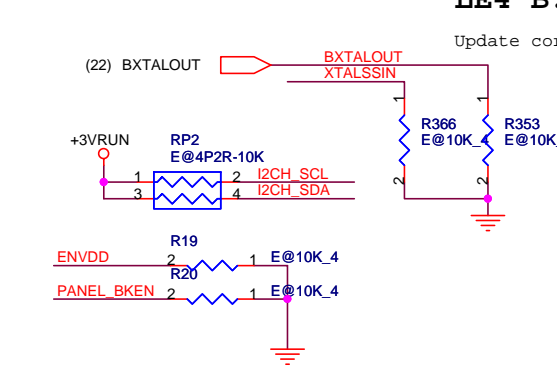
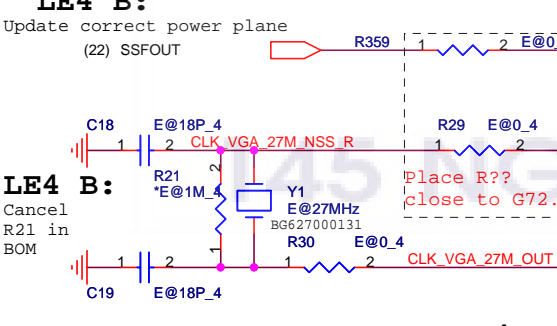
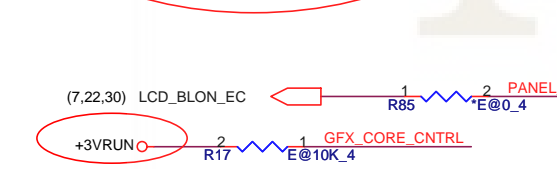
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDRR_VTERM





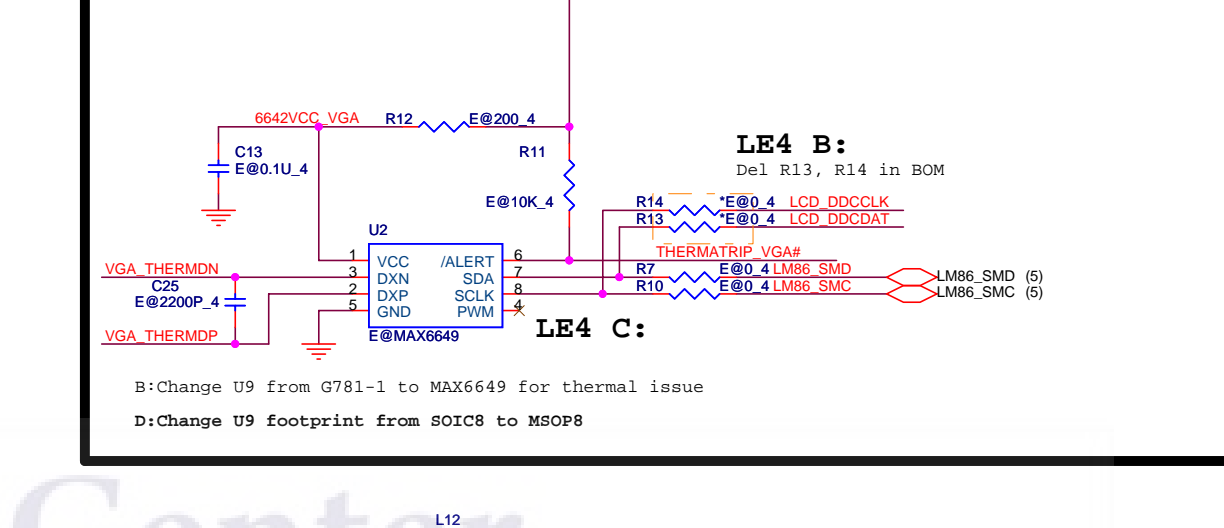


	CFG3	CFG2	CFG1	CFG0
128MB(16M*16)	0	0	1	0
G72M	1	0	0	0



Thermal Sensor for Graphic

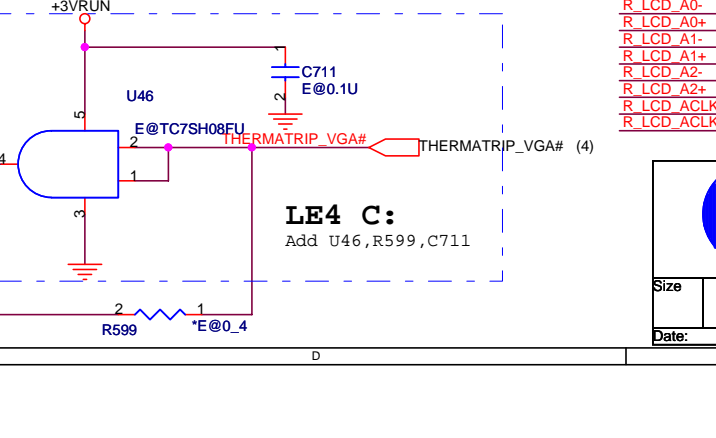
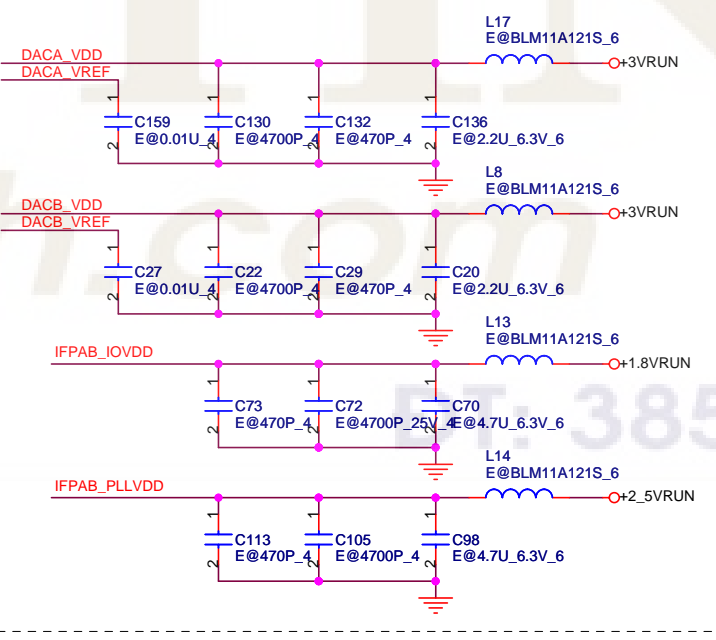
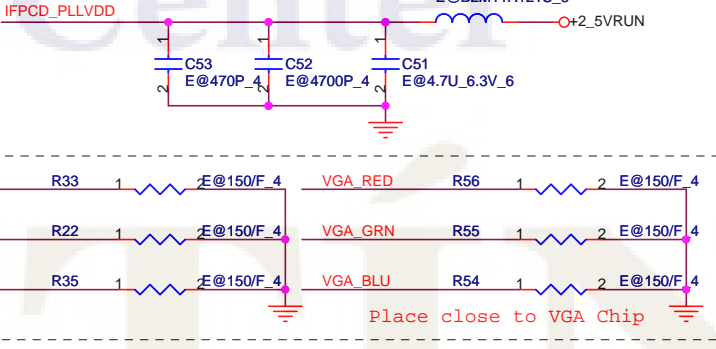
SLAVE ADDRESS: 9A



LE4 B:
Del R13, R14 in BOM

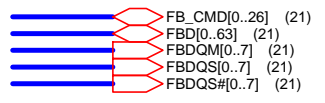
LE4 C:
Add U46, R599, C711

B: Change U9 from G781-1 to MAX6649 for thermal issue
D: Change U9 footprint from SOIC8 to MSOP8



R_LCD_A0-	R72	E@0_4	LCD_A0- (7,22)
R_LCD_A0+	R73	E@0_4	LCD_A0+ (7,22)
R_LCD_A1-	R83	E@0_4	LCD_A1- (7,22)
R_LCD_A1+	R87	E@0_4	LCD_A1+ (7,22)
R_LCD_A2-	R78	E@0_4	LCD_A2- (7,22)
R_LCD_A2+	R79	E@0_4	LCD_A2+ (7,22)
R_LCD_ACLK-	R88	E@0_4	LCD_ACLK- (7,22)
R_LCD_ACLK+	R92	E@0_4	LCD_ACLK+ (7,22)

PROJECT : LE4
Quanta Computer Inc.



U33C Part 3 of 4

MEMORY INTERFACE

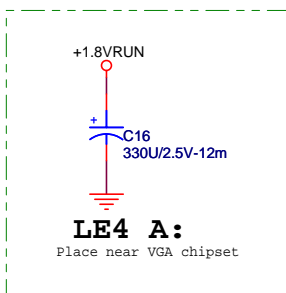
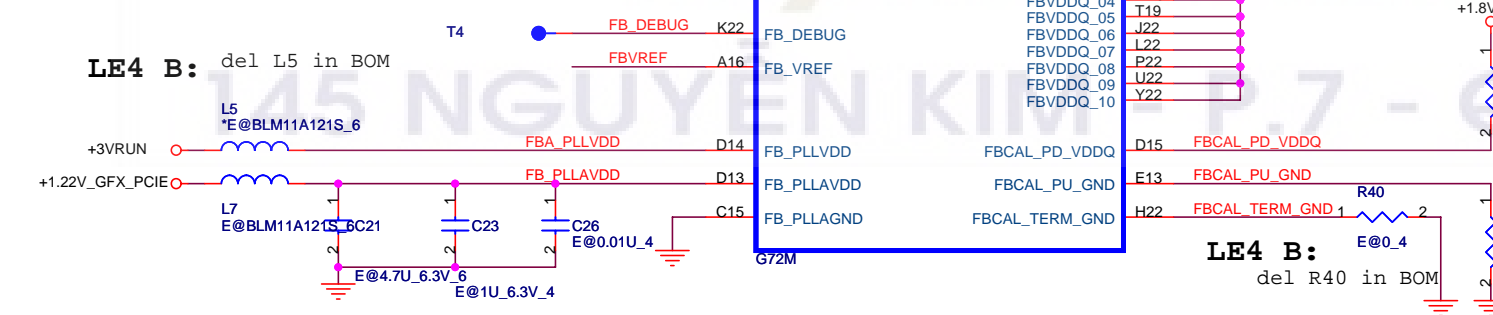
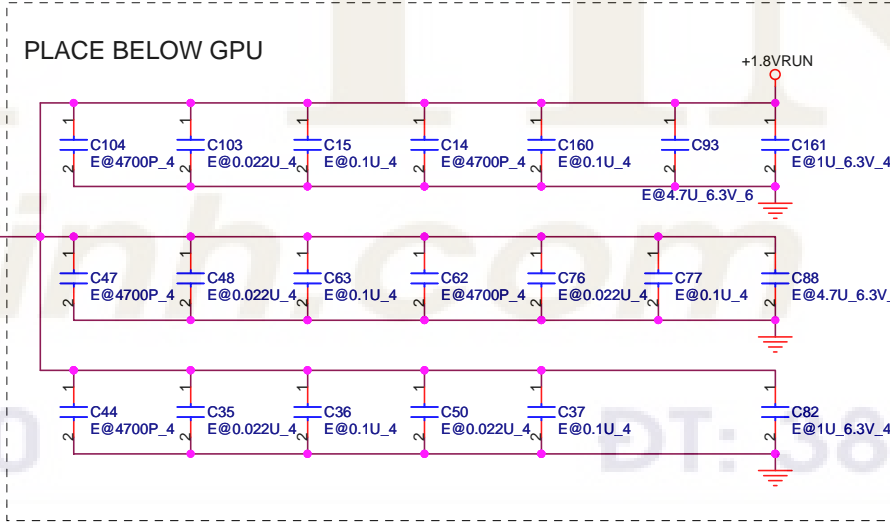
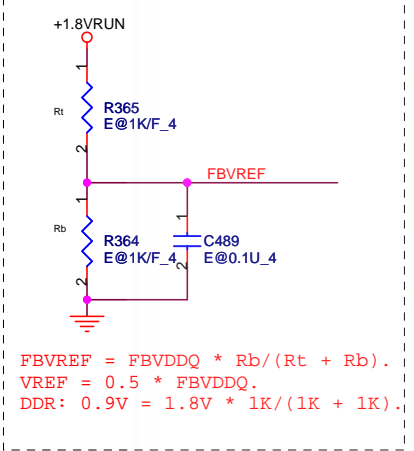
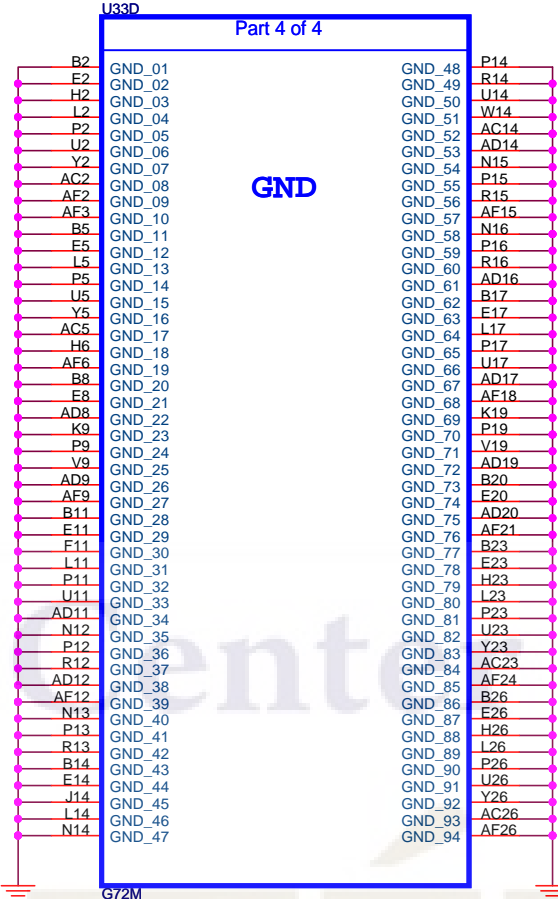
FBD0	A26	FB_DQ0
FBD1	C24	FB_DQ1
FBD2	B24	FB_DQ2
FBD3	A24	FB_DQ3
FBD4	C22	FB_DQ4
FBD5	A25	FB_DQ5
FBD6	B25	FB_DQ6
FBD7	D23	FB_DQ7
FBD8	G22	FB_DQ8
FBD9	J23	FB_DQ9
FBD10	E24	FB_DQ10
FBD11	F23	FB_DQ11
FBD12	J24	FB_DQ12
FBD13	F24	FB_DQ13
FBD14	G23	FB_DQ14
FBD15	H24	FB_DQ15
FBD16	D16	FB_DQ16
FBD17	E16	FB_DQ17
FBD18	D17	FB_DQ18
FBD19	F18	FB_DQ19
FBD20	E19	FB_DQ20
FBD21	F18	FB_DQ21
FBD22	D20	FB_DQ22
FBD23	A19	FB_DQ23
FBD24	B18	FB_DQ24
FBD25	A19	FB_DQ25
FBD26	B19	FB_DQ26
FBD27	D18	FB_DQ27
FBD28	C19	FB_DQ28
FBD29	C16	FB_DQ29
FBD30	C18	FB_DQ30
FBD31	N26	FB_DQ31
FBD32	N25	FB_DQ32
FBD33	R25	FB_DQ33
FBD34	R26	FB_DQ34
FBD35	R27	FB_DQ35
FBD36	T25	FB_DQ36
FBD37	T27	FB_DQ37
FBD38	T26	FB_DQ38
FBD39	AB23	FB_DQ39
FBD40	Y24	FB_DQ40
FBD41	AB24	FB_DQ41
FBD42	AB22	FB_DQ42
FBD43	AC24	FB_DQ43
FBD44	AC22	FB_DQ44
FBD45	AA23	FB_DQ45
FBD46	AA22	FB_DQ46
FBD47	T24	FB_DQ47
FBD48	T23	FB_DQ48
FBD49	R24	FB_DQ49
FBD50	R23	FB_DQ50
FBD51	R22	FB_DQ51
FBD52	T22	FB_DQ52
FBD53	N23	FB_DQ53
FBD54	P24	FB_DQ54
FBD55	AA24	FB_DQ55
FBD56	AA27	FB_DQ56
FBD57	AA26	FB_DQ57
FBD58	AB25	FB_DQ58
FBD59	AB26	FB_DQ59
FBD60	AB27	FB_DQ60
FBD61	AA25	FB_DQ61
FBD62	AA25	FB_DQ62
FBD63	W25	FB_DQ63

FB_CMD0	G27	FB_CMD0
FB_CMD1	D25	FB_CMD1
FB_CMD2	F26	FB_CMD2
FB_CMD3	F25	FB_CMD3
FB_CMD4	G25	FB_CMD4
FB_CMD5	J25	FB_CMD5
FB_CMD6	J27	FB_CMD6
FB_CMD7	M26	FB_CMD7
FB_CMD8	C27	FB_CMD8
FB_CMD9	C25	FB_CMD9
FB_CMD10	D24	FB_CMD10
FB_CMD11	N27	FB_CMD11
FB_CMD12	G24	FB_CMD12
FB_CMD13	J26	FB_CMD13
FB_CMD14	M27	FB_CMD14
FB_CMD15	C26	FB_CMD15
FB_CMD16	M25	FB_CMD16
FB_CMD17	D26	FB_CMD17
FB_CMD18	D27	FB_CMD18
FB_CMD19	K26	FB_CMD19
FB_CMD20	K25	FB_CMD20
FB_CMD21	F24	FB_CMD21
FB_CMD22	F27	FB_CMD22
FB_CMD23	K27	FB_CMD23
FB_CMD24	G26	FB_CMD24
FB_CMD25	B27	FB_CMD25
FB_CMD26	N24	FB_CMD26

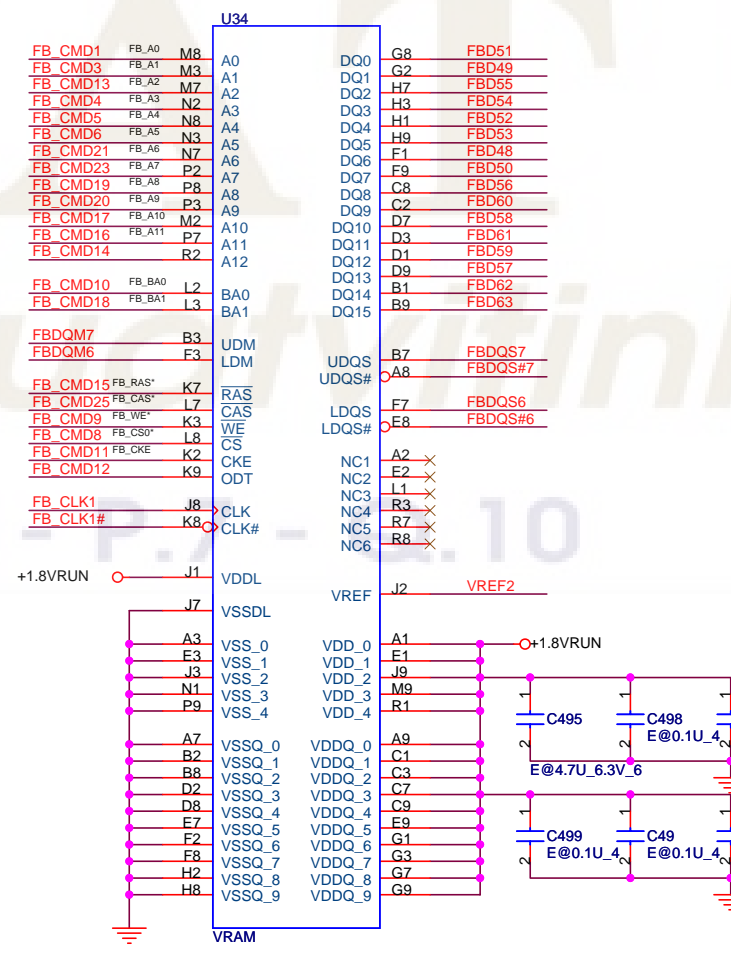
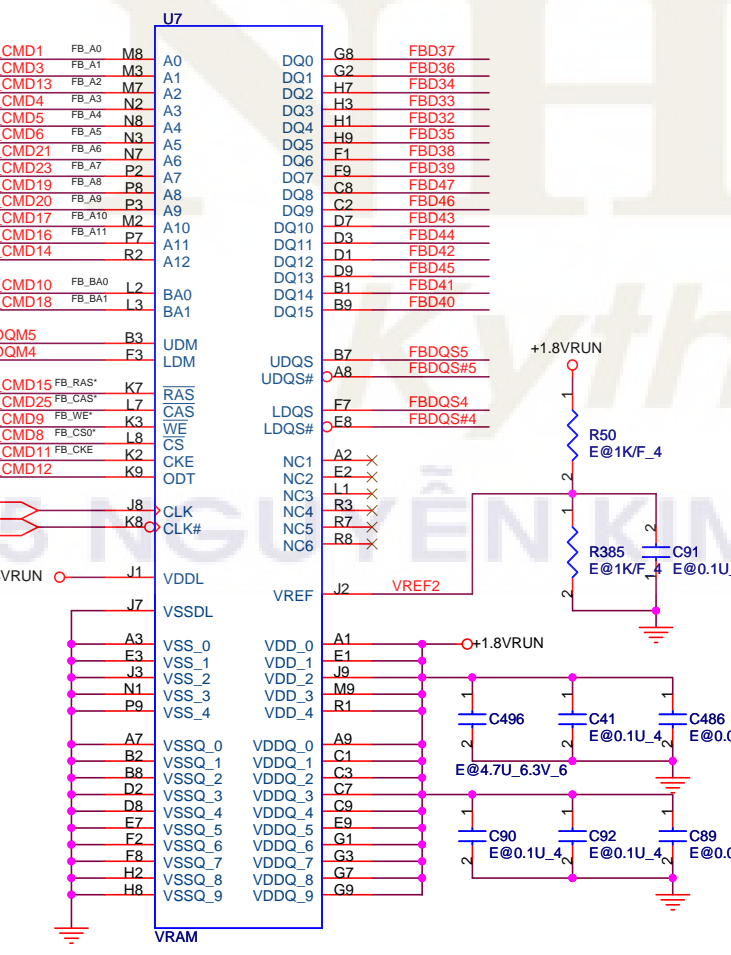
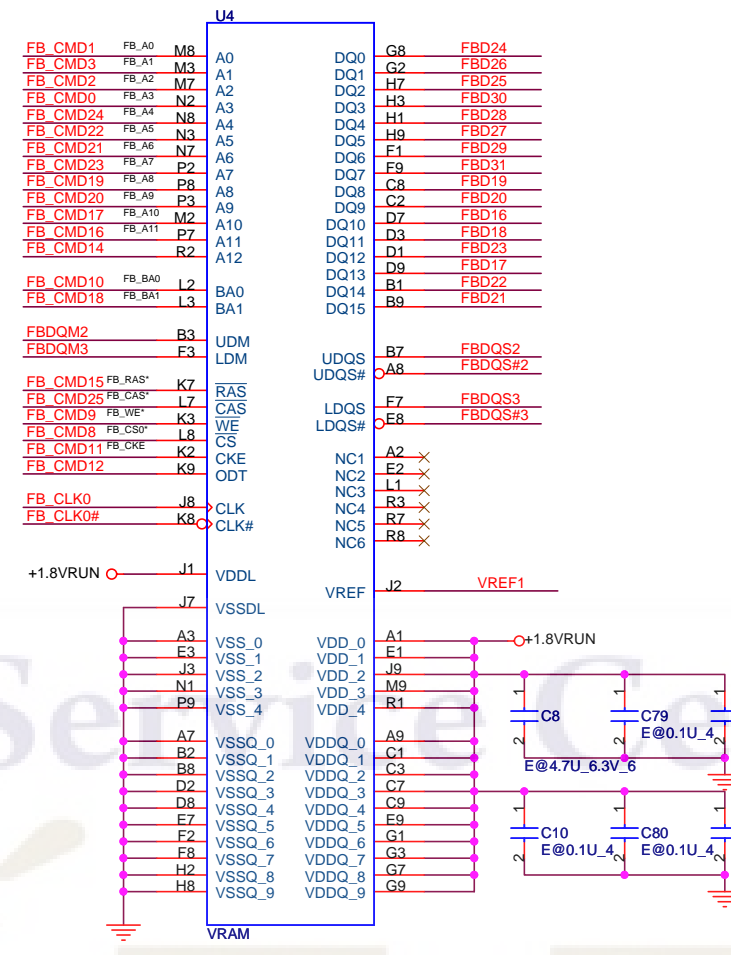
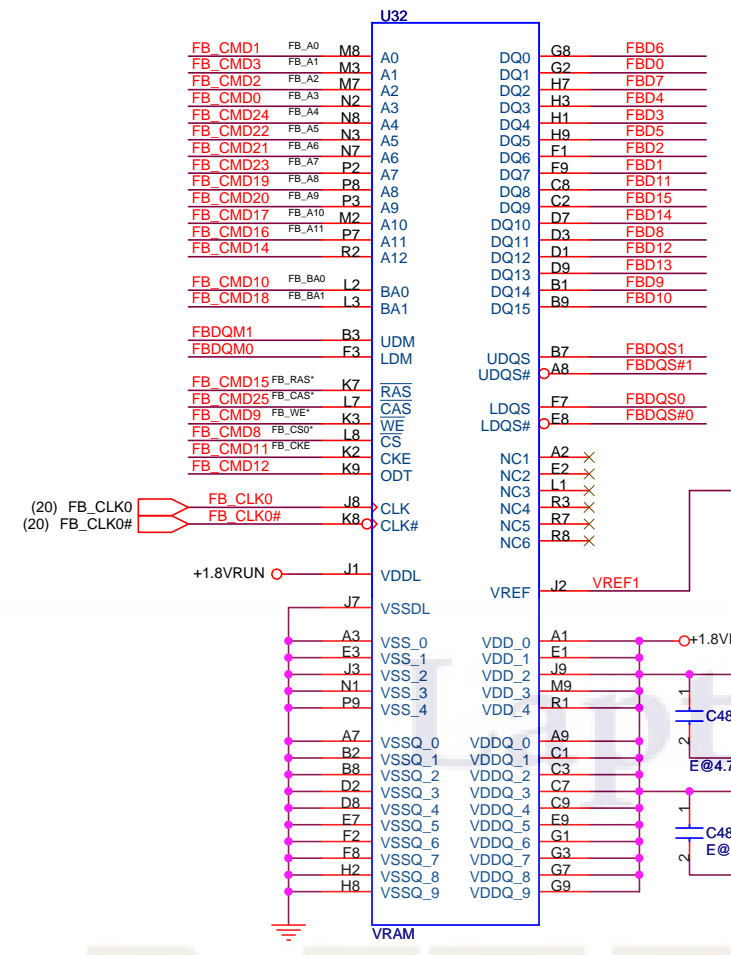
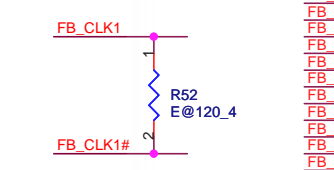
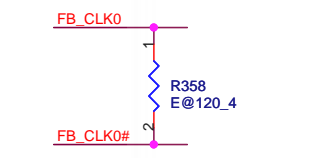
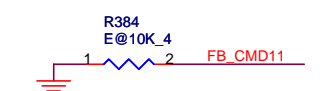
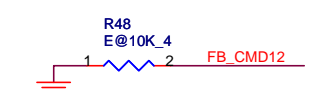
FB_DQM0	D21	FBDQM0
FB_DQM1	E22	FBDQM1
FB_DQM2	E20	FBDQM2
FB_DQM3	A21	FBDQM3
FB_DQM4	V27	FBDQM4
FB_DQM5	W22	FBDQM5
FB_DQM6	V22	FBDQM6
FB_DQM7	V24	FBDQM7

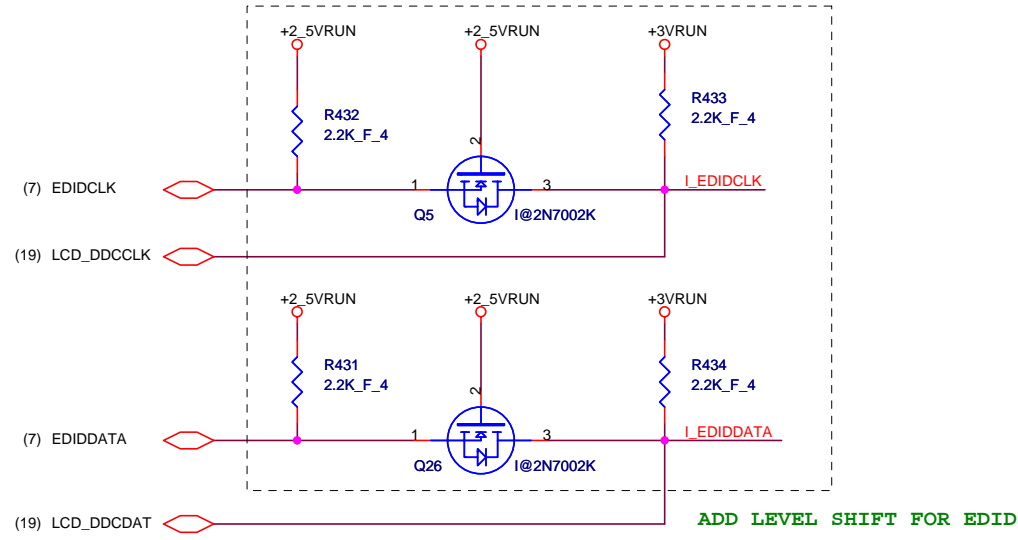
FB_DQS_RN0	A22	FBDQS#0
FB_DQS_RN1	E22	FBDQS#1
FB_DQS_RN2	F21	FBDQS#2
FB_DQS_RN3	B21	FBDQS#3
FB_DQS_RN4	V26	FBDQS#4
FB_DQS_RN5	W23	FBDQS#5
FB_DQS_RN6	V23	FBDQS#6
FB_DQS_RN7	W27	FBDQS#7

FB_DQS_WP0	B22	FBDQS#0
FB_DQS_WP1	D22	FBDQS#1
FB_DQS_WP2	E21	FBDQS#2
FB_DQS_WP3	C21	FBDQS#3
FB_DQS_WP4	V25	FBDQS#4
FB_DQS_WP5	W24	FBDQS#5
FB_DQS_WP6	U24	FBDQS#6
FB_DQS_WP7	W26	FBDQS#7

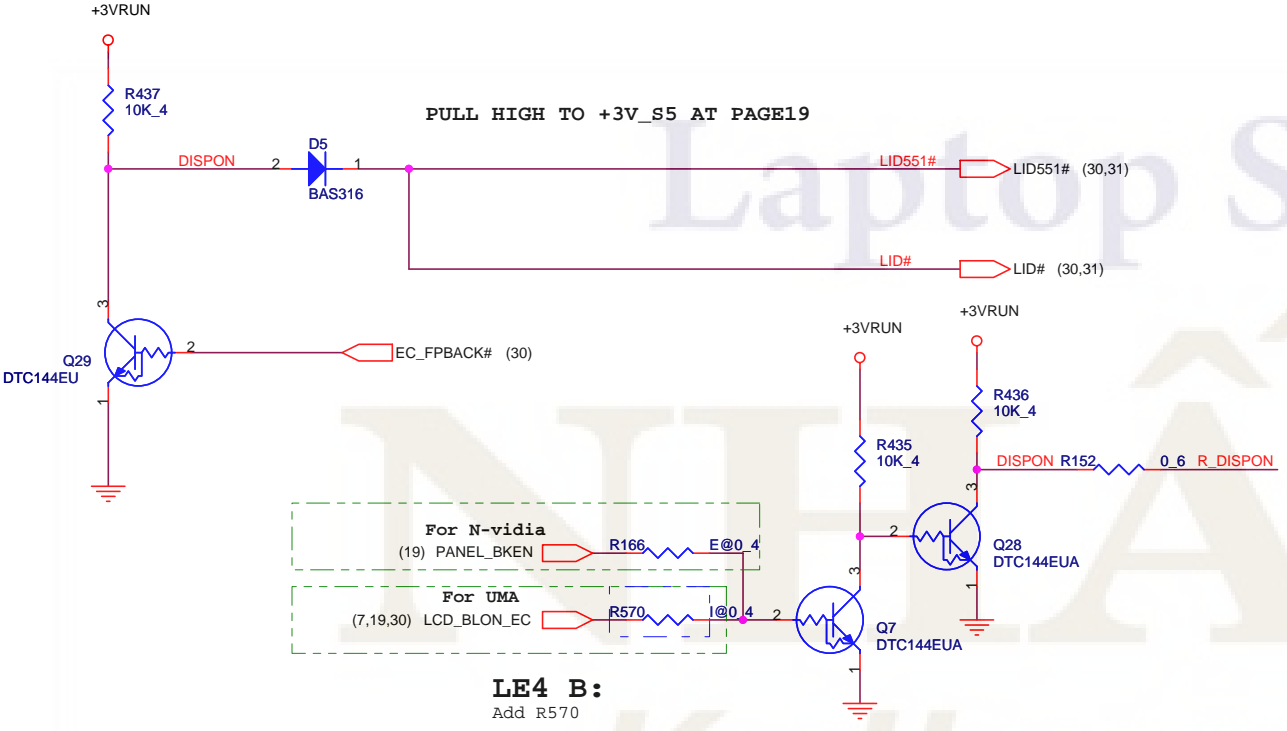


- FB_CMD[0..26] (20)
- FBD[0..63] (20)
- FBDQM[0..7] (20)
- FBDQS[0..7] (20)

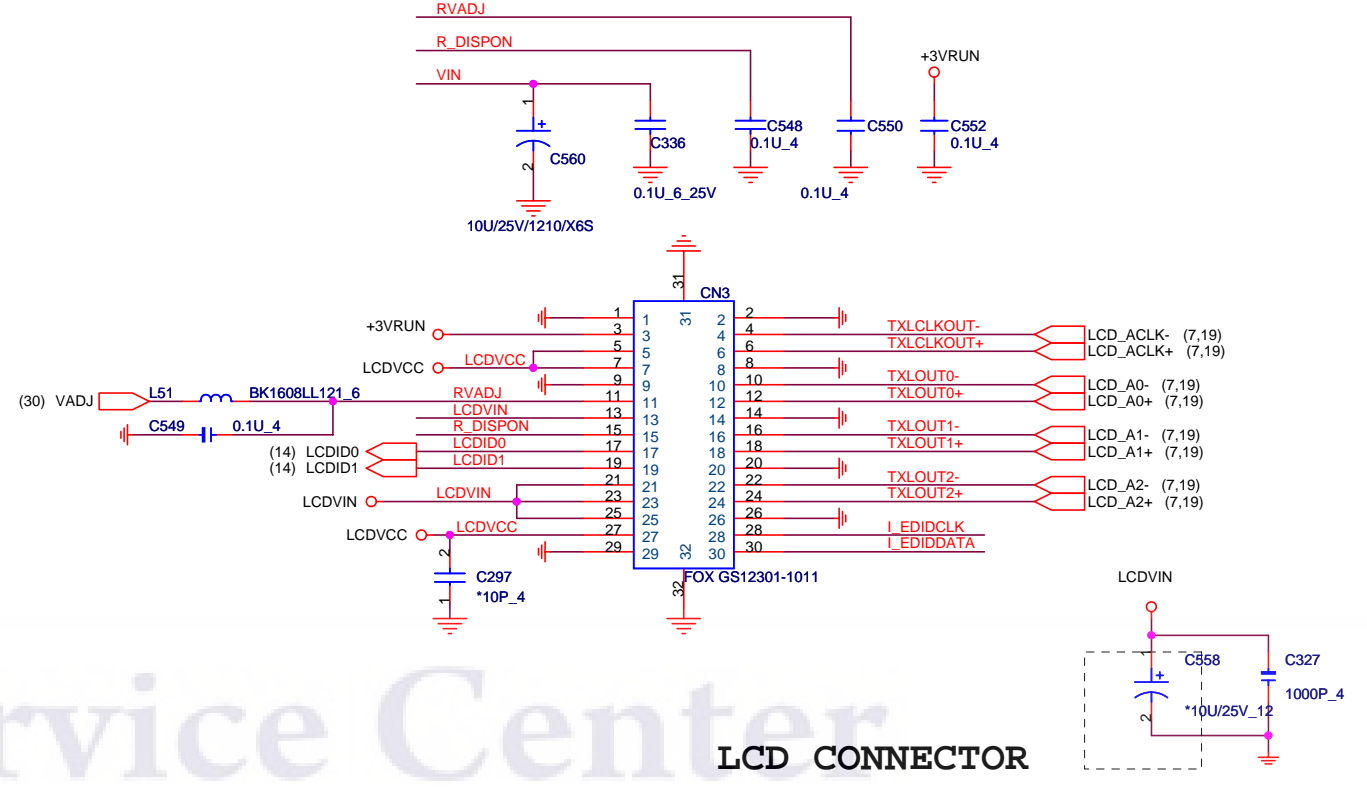




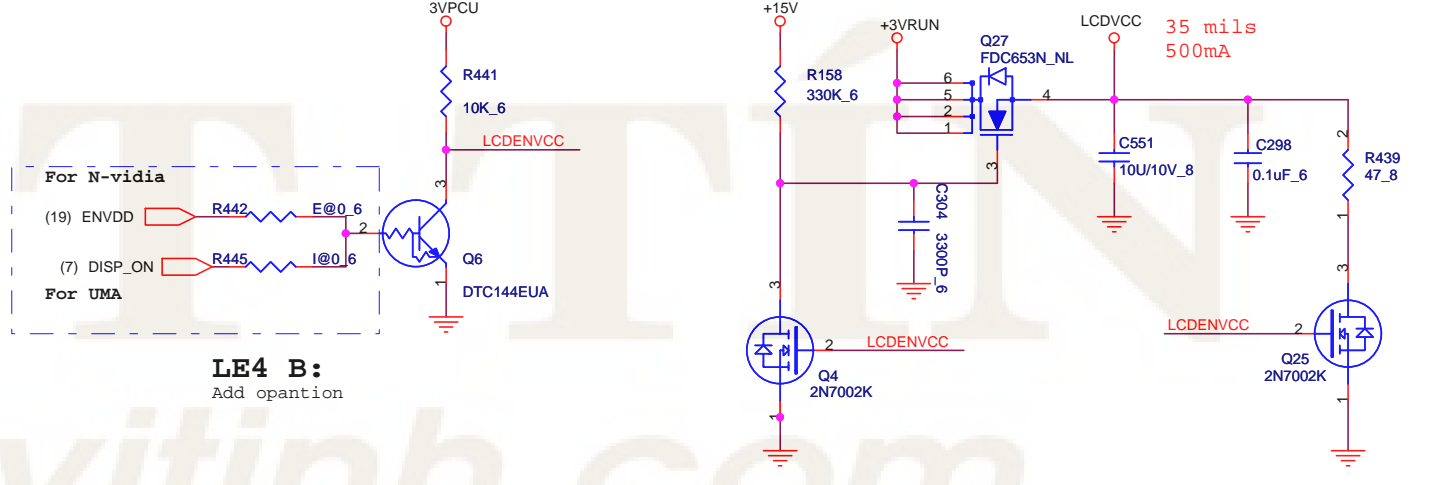
ADD LEVEL SHIFT FOR EDID



LE4 B:
Add R570

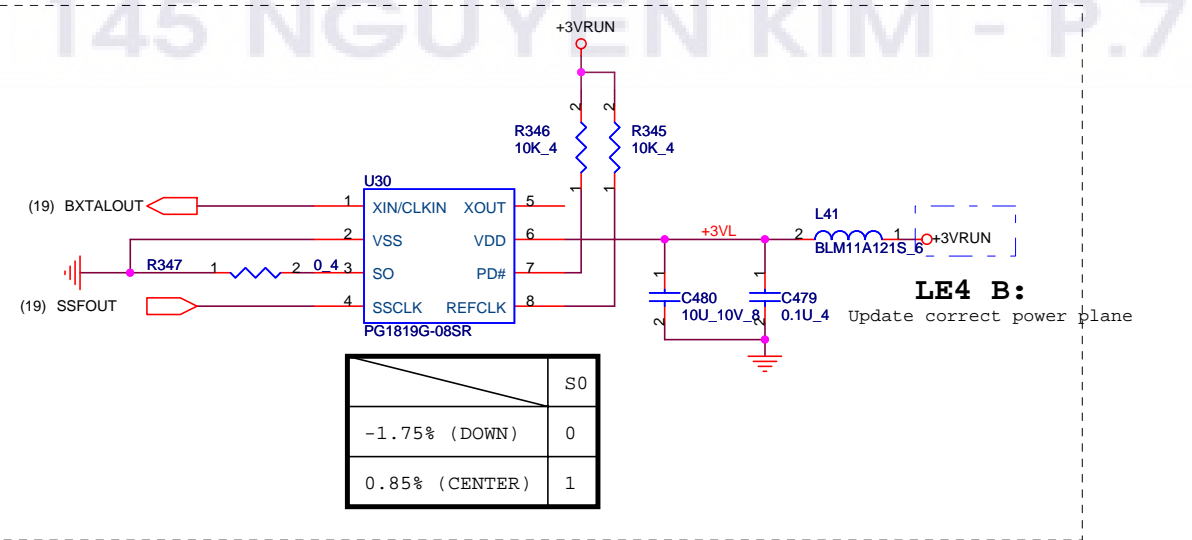


LCD CONNECTOR



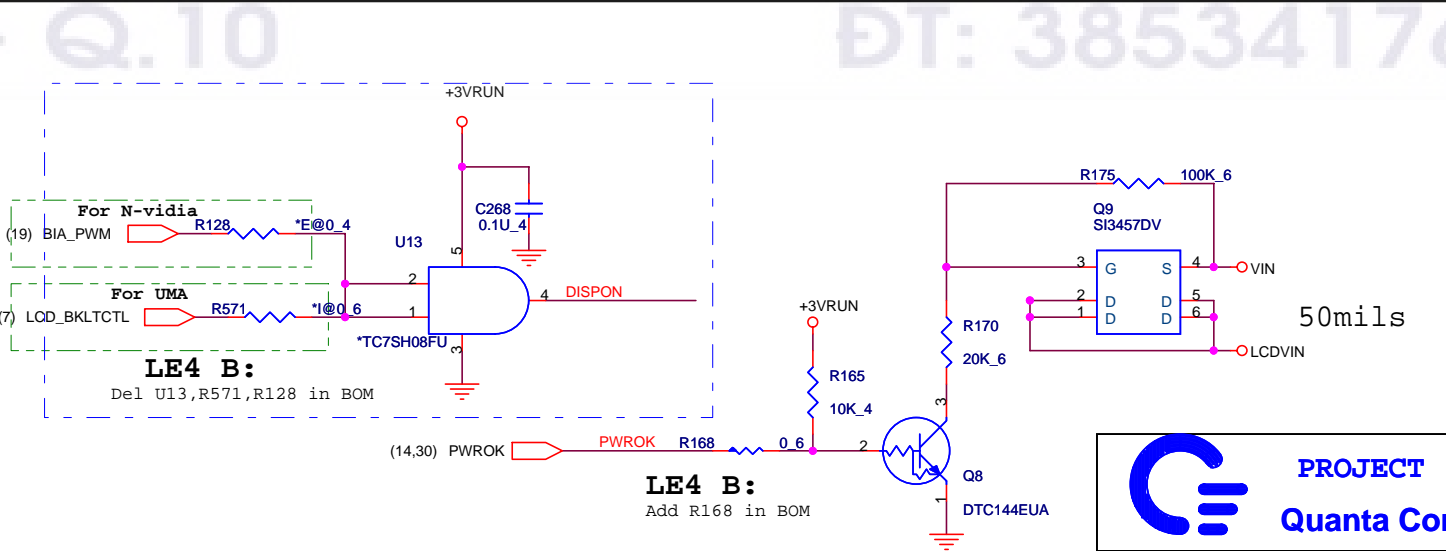
LE4 B:
Add opation

LCD VCC



LE4 B:
Update correct power plane

	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1



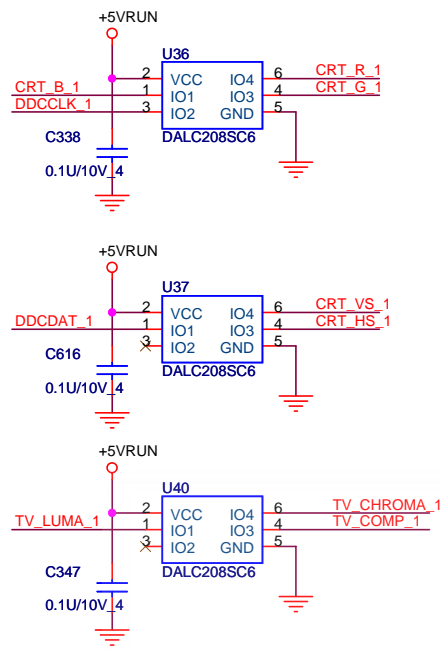
LE4 B:
Del U13, R571, R128 in BOM

LE4 B:
Add R168 in BOM

INVERTER POWER CIRCUIT

PROJECT : LE4
Quanta Computer Inc.

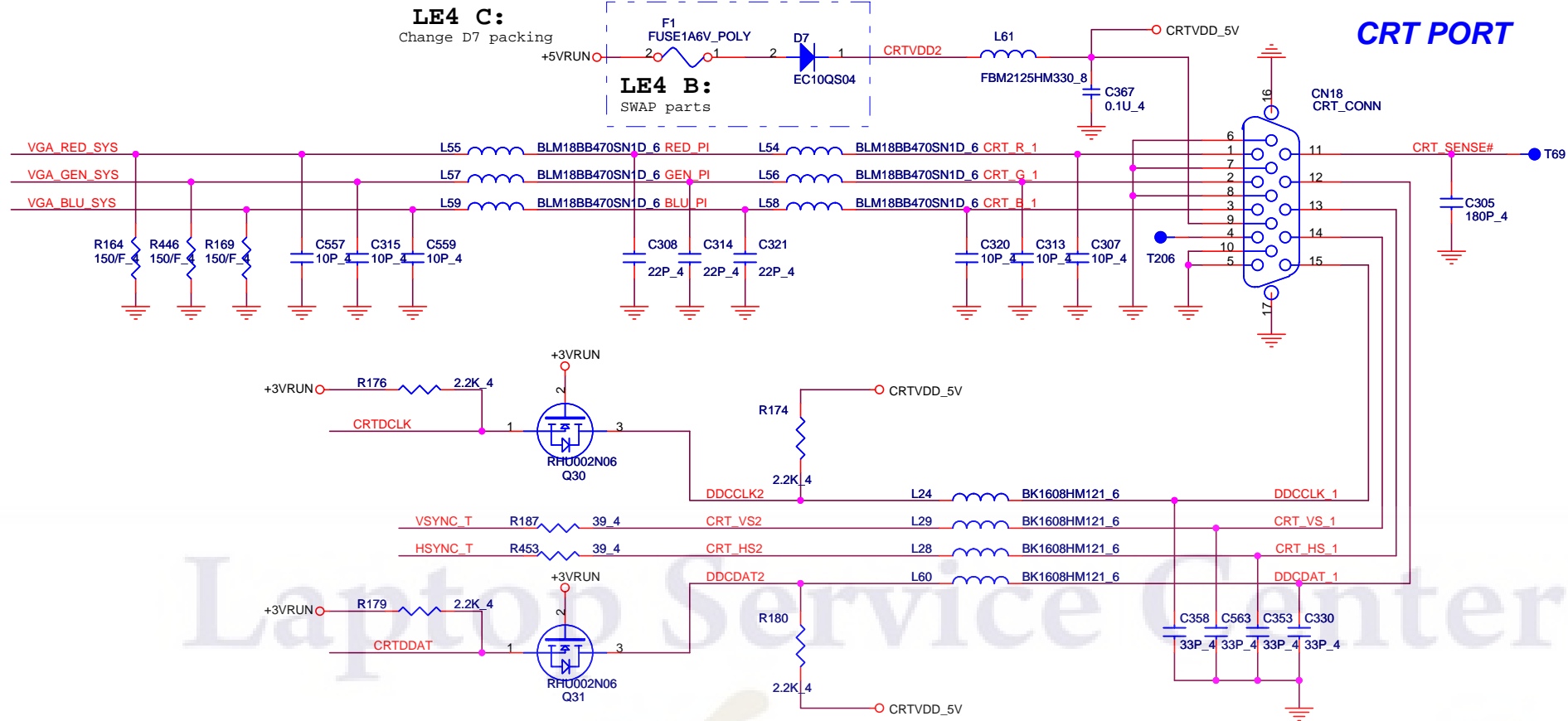
ESD PORTECTION



LE4 C:

Change D7 packing

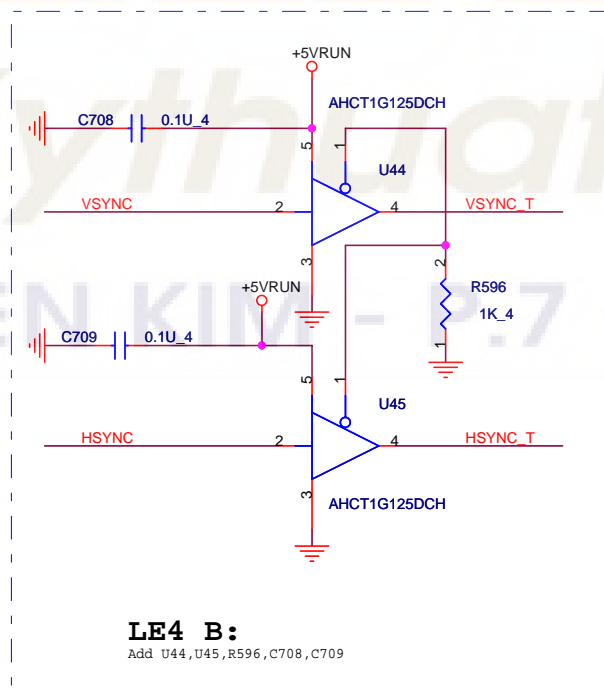
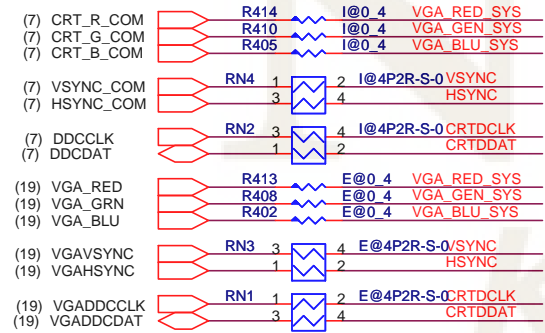
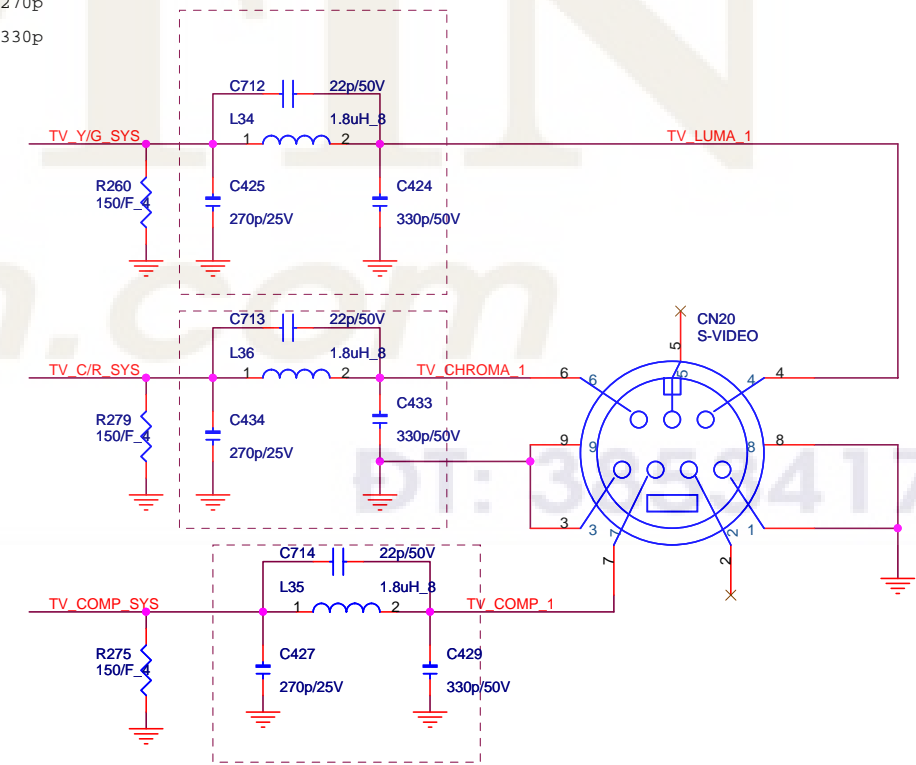
LE4 B:
SWAP parts



TV-OUT

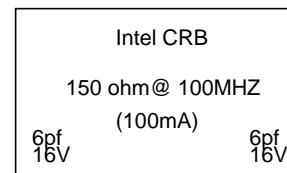
LE4 C:

Change C425, C434 and C427 from 6p to 270p
 Change C424, C433 and C429 from 6p to 330p
 Change L35 size from 0603 to 0805
 Add C712, C713 and C714



LE4 B:

Add U44, U45, R596, C708, C709



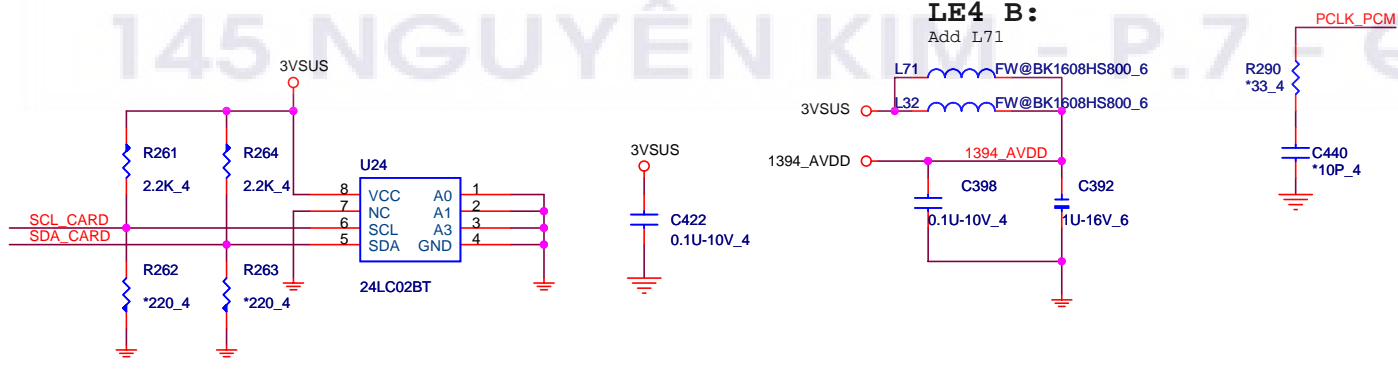
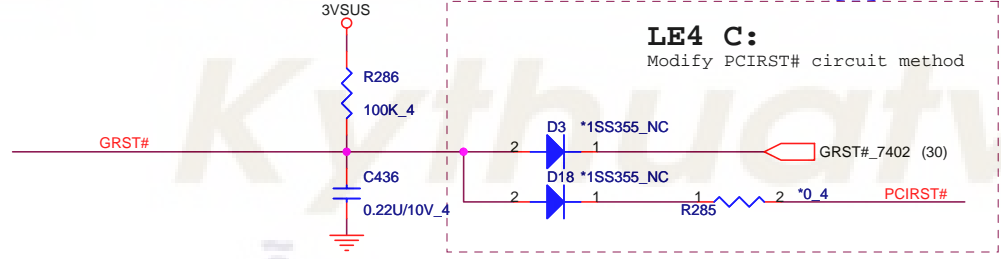
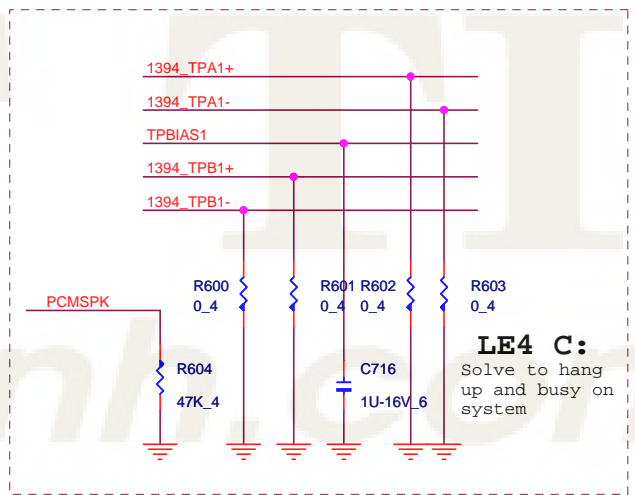
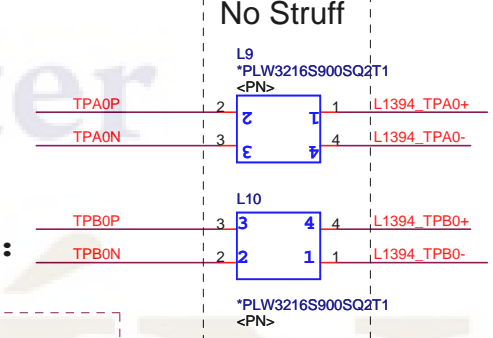
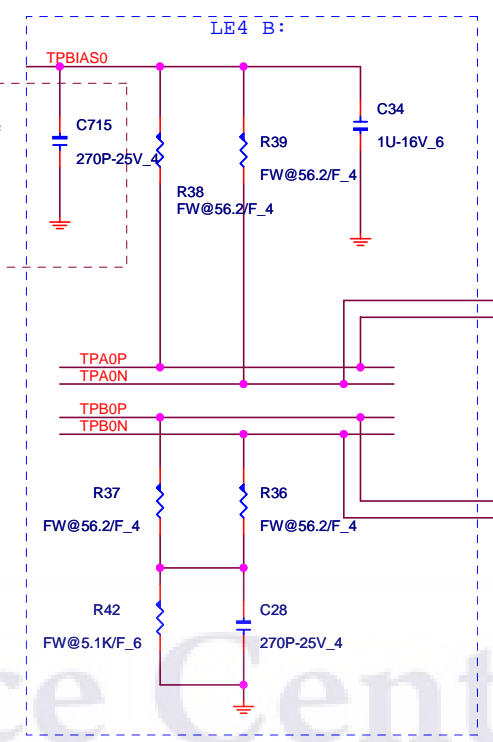
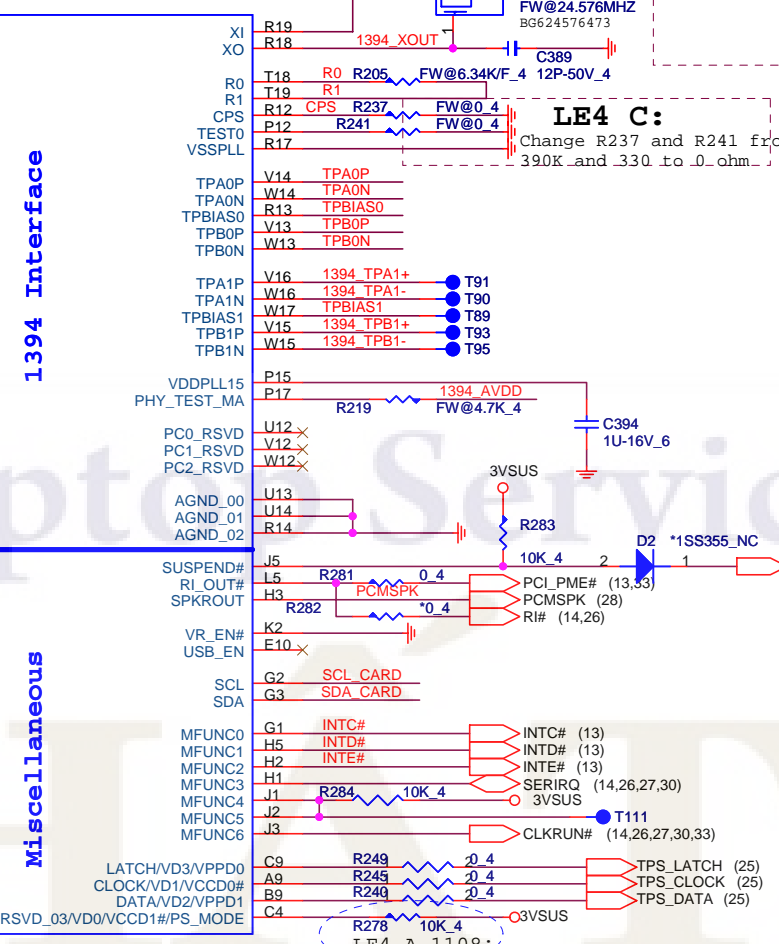
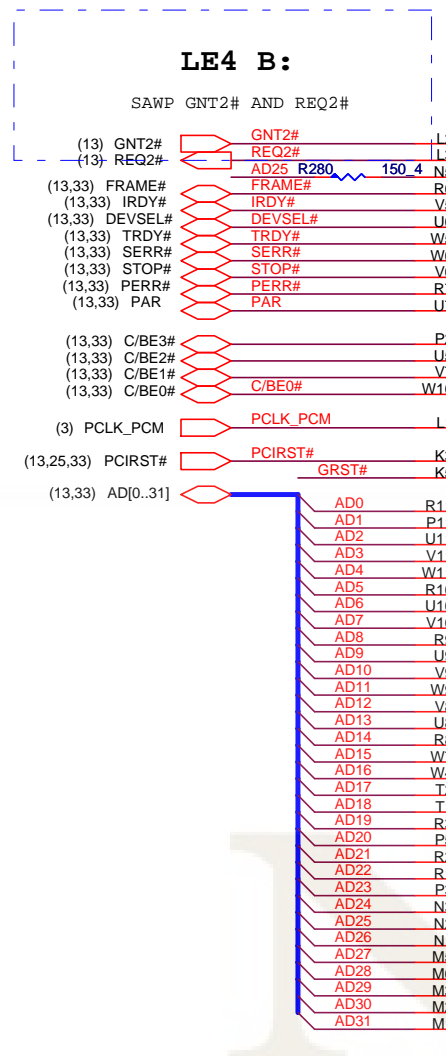
CX8PG181001 (180 ohm, 1.5A)

CH00606TB04 CH00606TB04



PROJECT : LE4
Quanta Computer Inc.

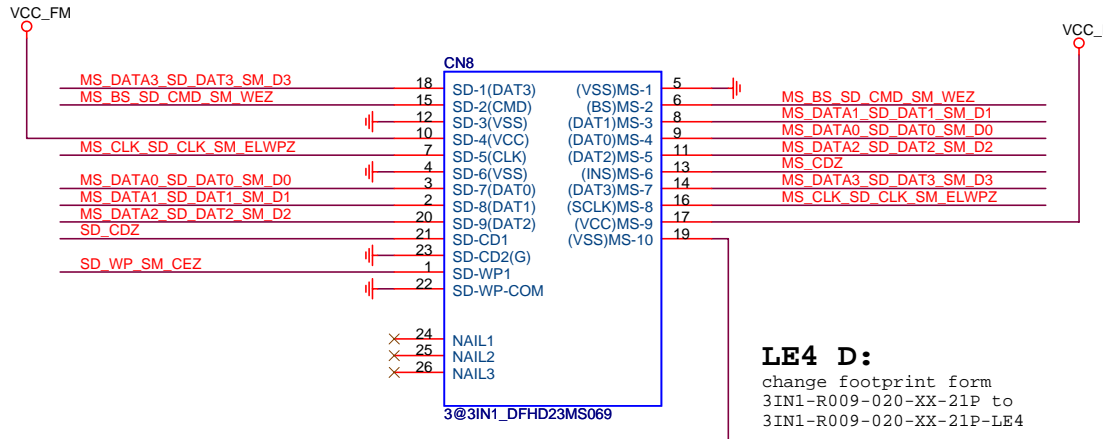
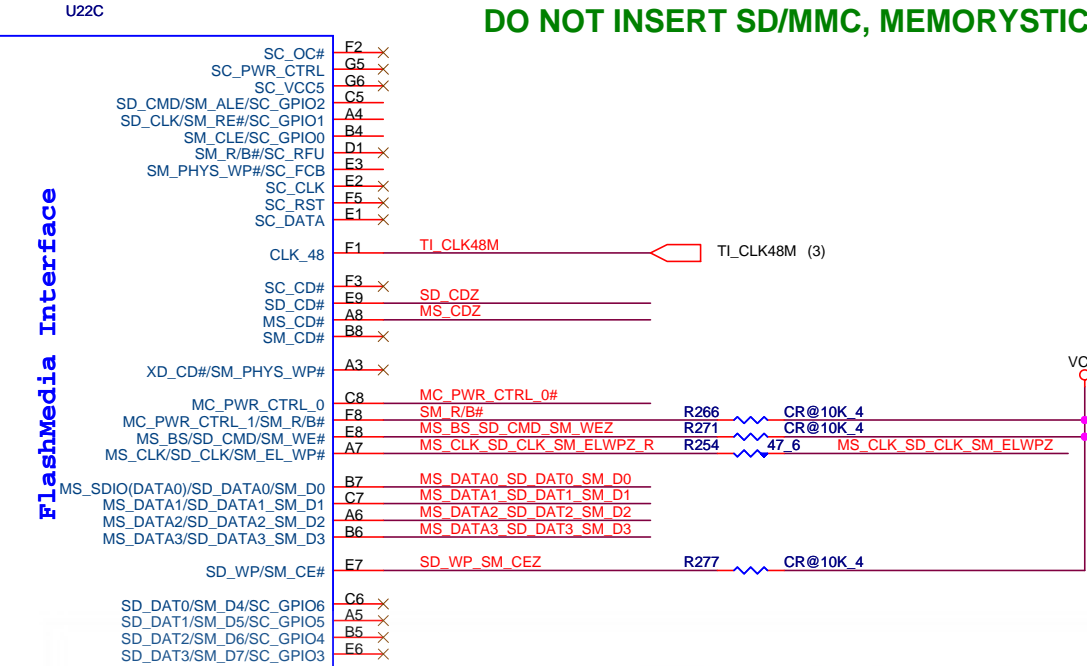
Size	Document Number	Rev
	CRT & TV-OUT CONN	1A
Date:	Tuesday, March 14, 2006	Sheet 23 of 42



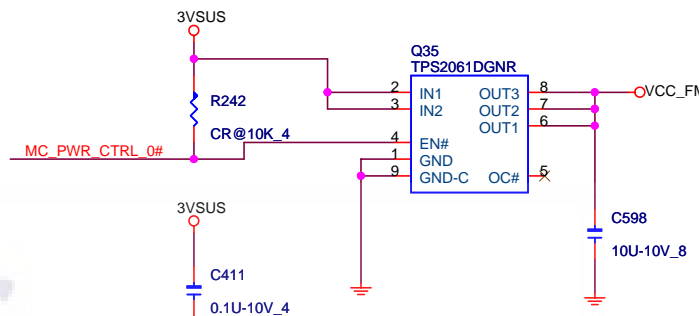
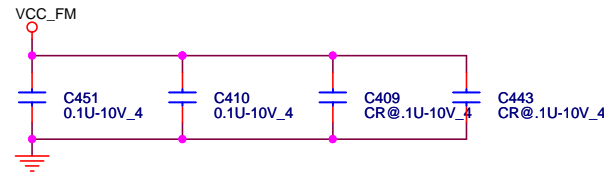
145 NGUYỄN KIỆP P.7-Q.10 ĐT: 38534176

DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

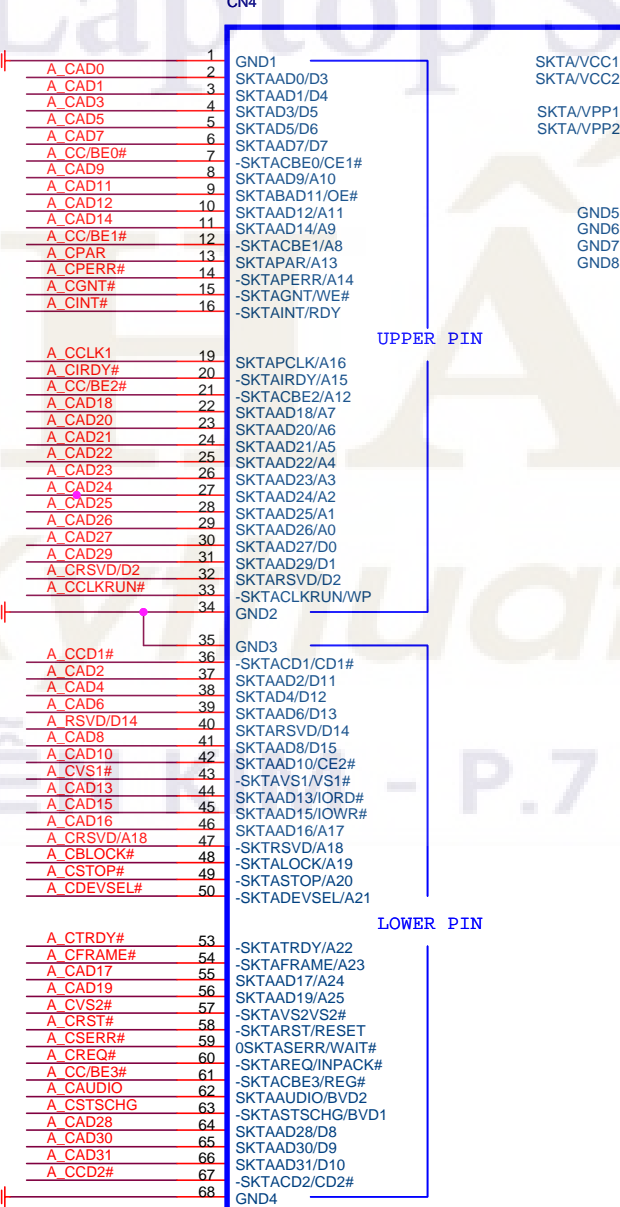
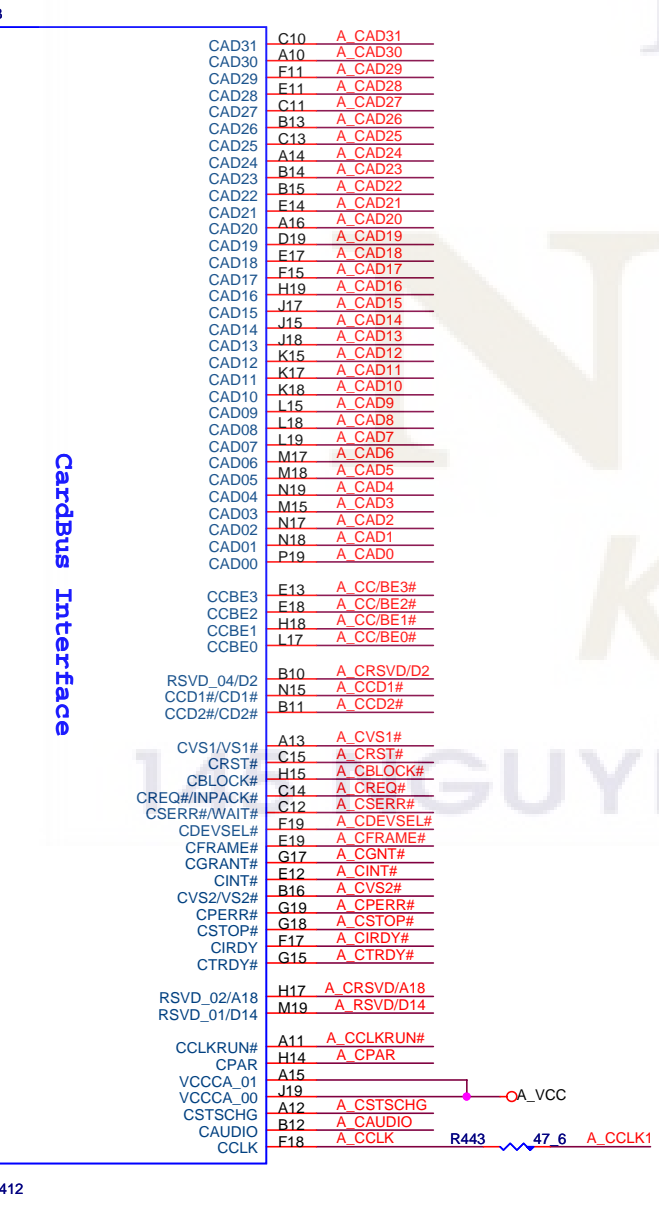
3 IN 1 CARD READER (push-push)



LE4 D:
change footprint form
3IN1-R009-020-XX-21P to
3IN1-R009-020-XX-21P-LE4

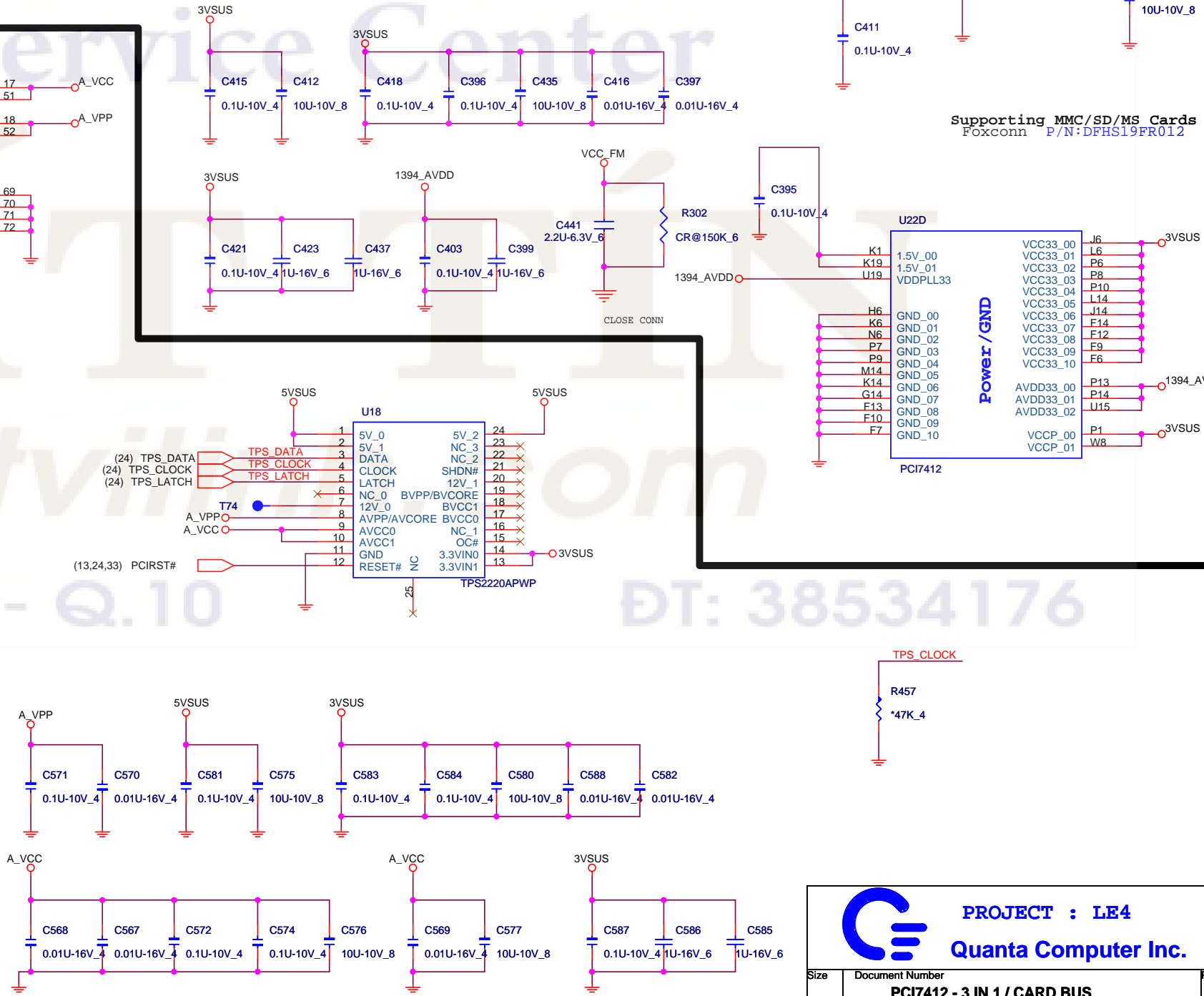


Supporting MMC/SD/MS Cards
Foxconn P/N:DFHS19FR012



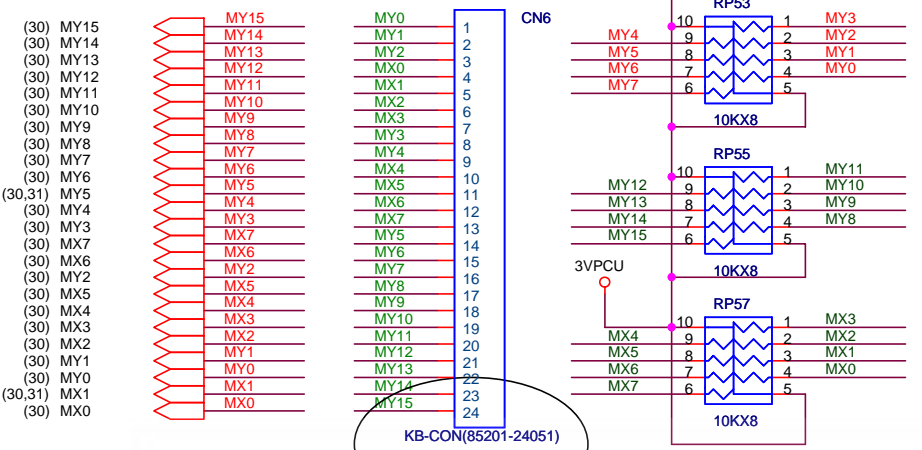
CARD BUS
FOX_1CA4C5G2-TC_CARD BUS

CARD BUS



PROJECT : LE4
Quanta Computer Inc.

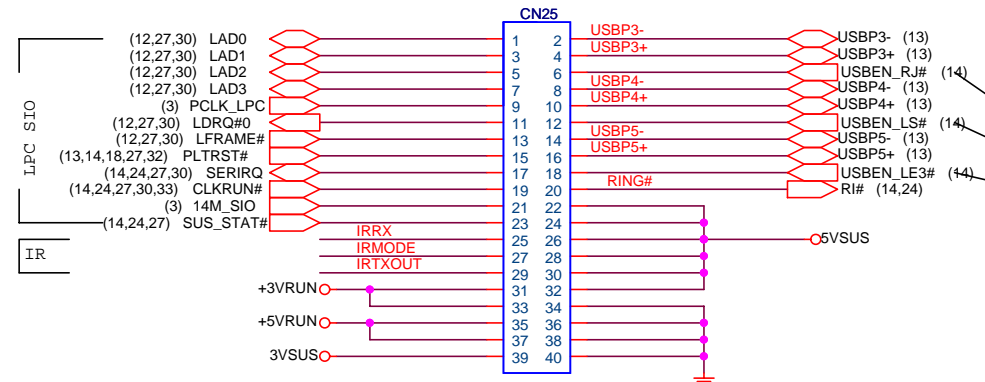
INT K/B



KB-CON(85201-24051)

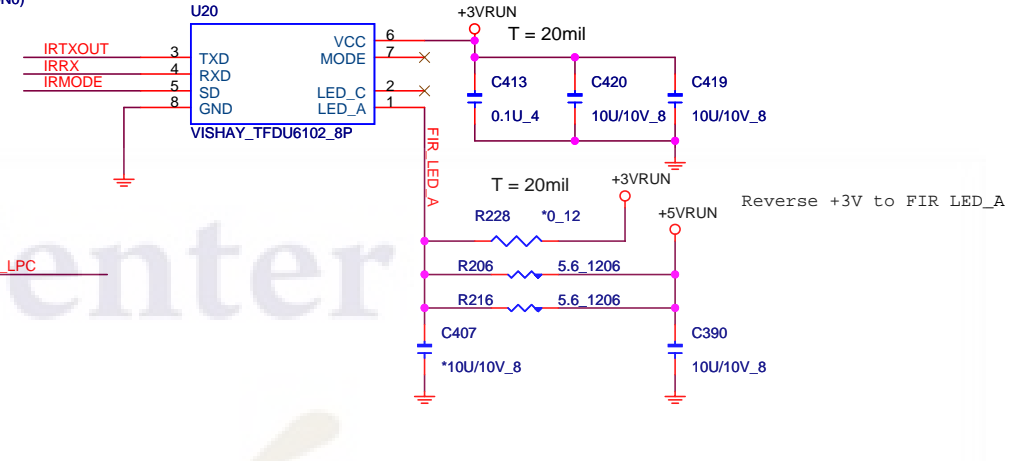
1/27 update keymatrix as same as le1

M/B TO MODEM/B

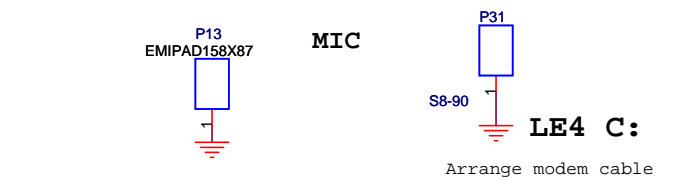
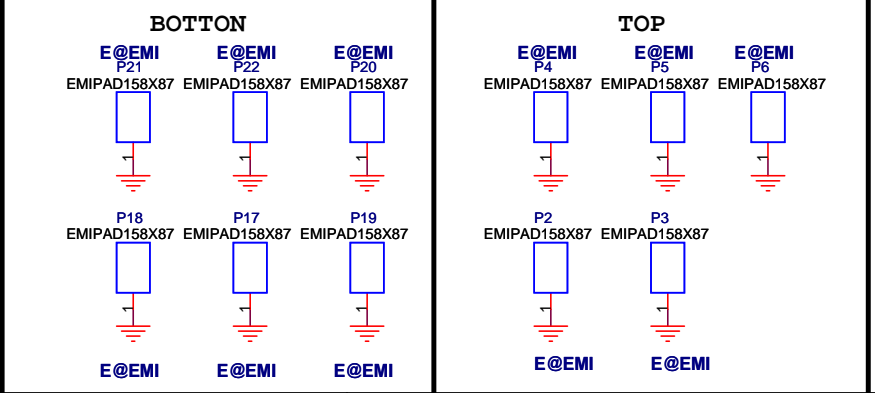
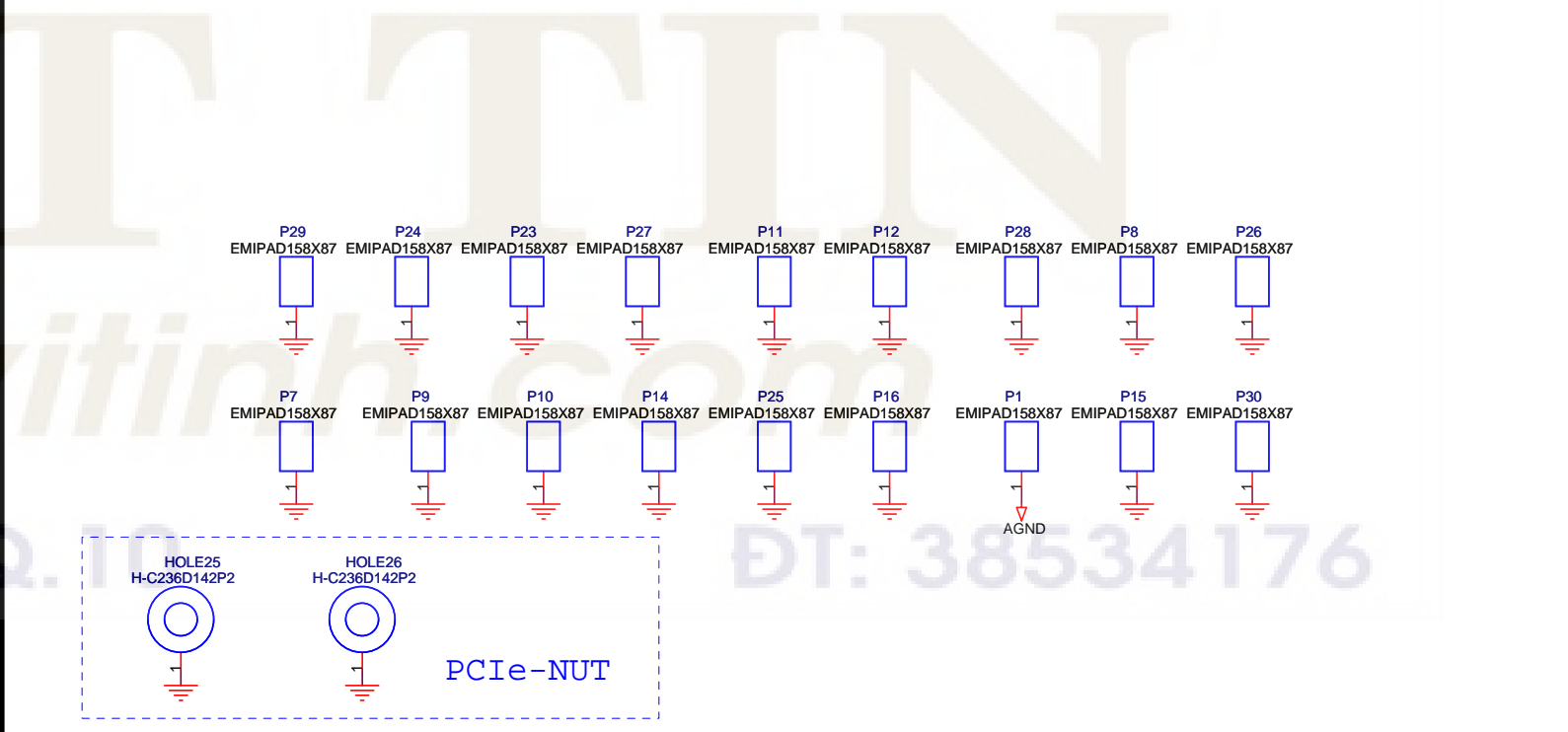
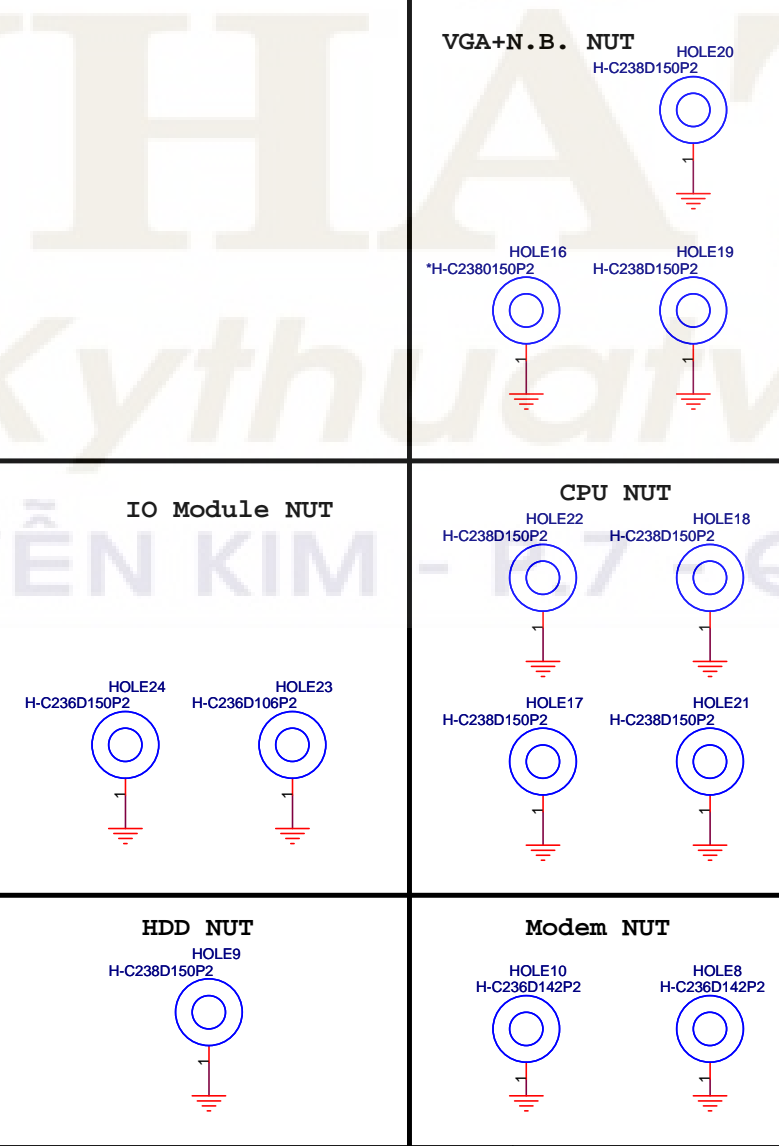
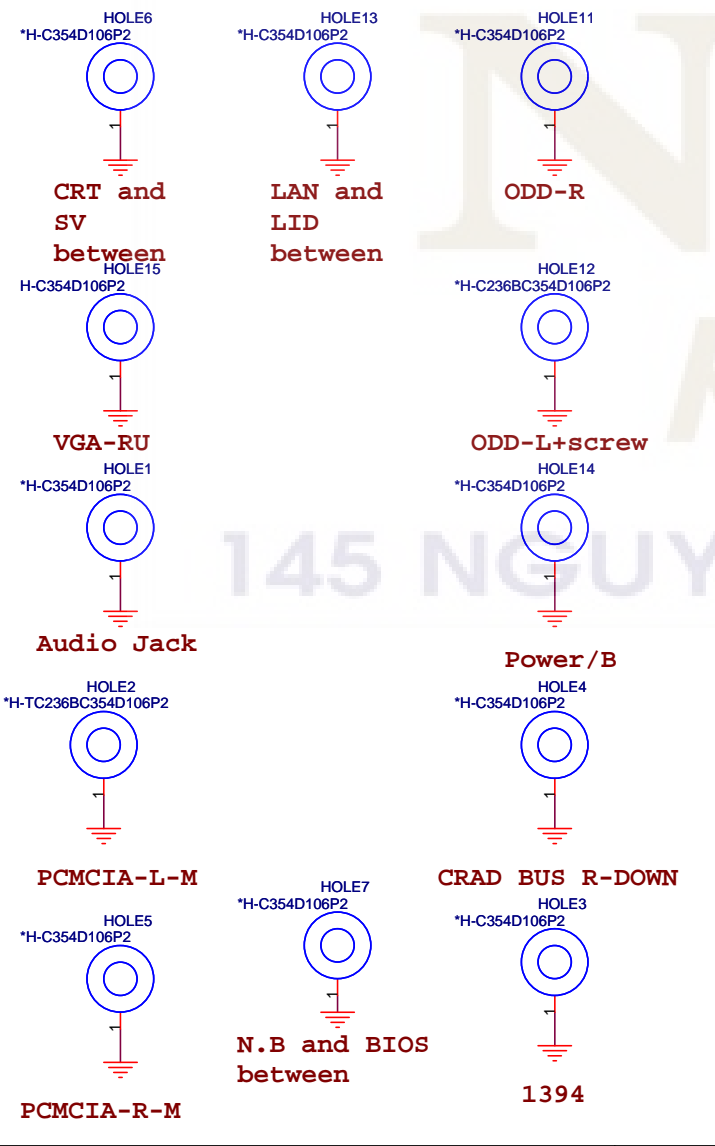


LE4 C:
Change USBEN meaning from OC# to GPIO#

MODEM B TO B(88019-40N0)



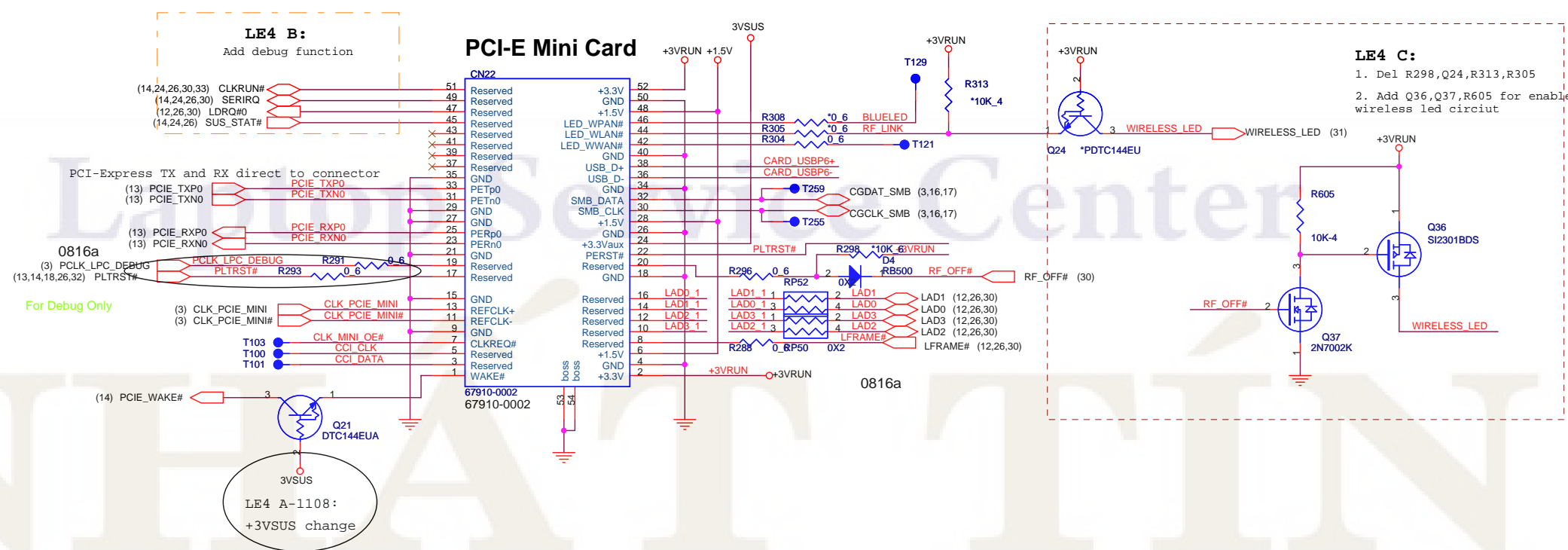
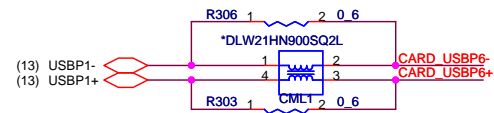
Laptop Service Center



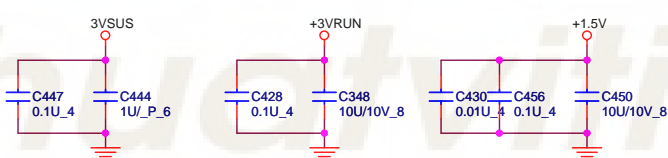
PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	SCREW hole EMI pad	1A
Date:	Tuesday, March 14, 2006	Sheet 26 of 42

Need one more wireless LED /mini card on MB ?
currently , No LED here

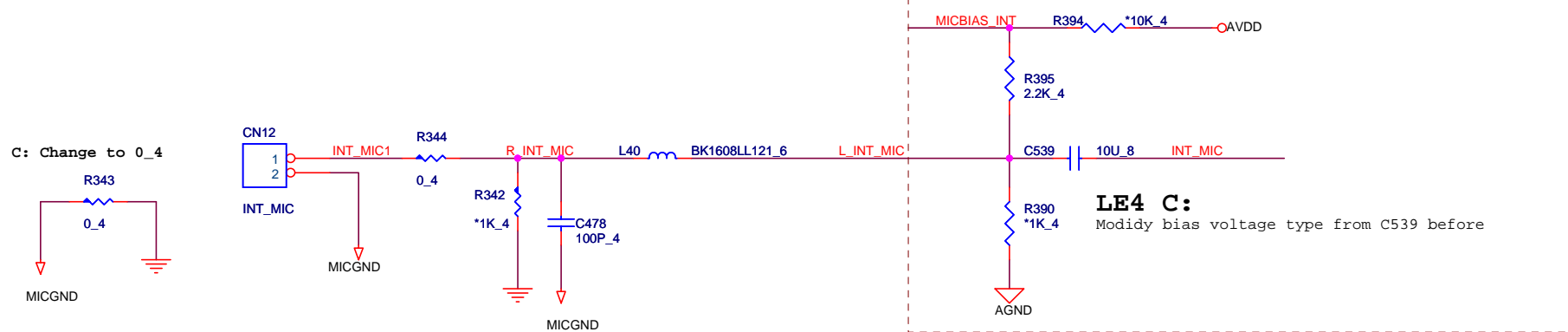
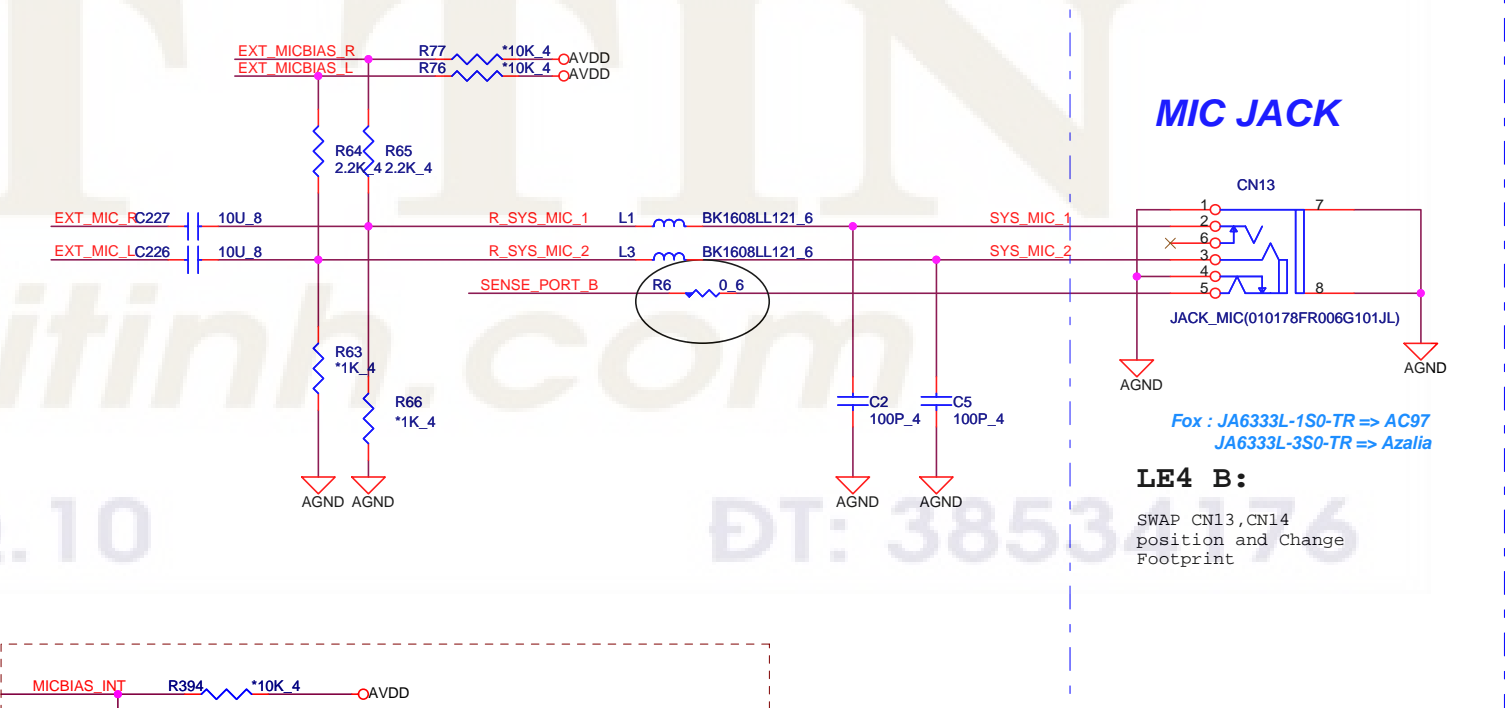
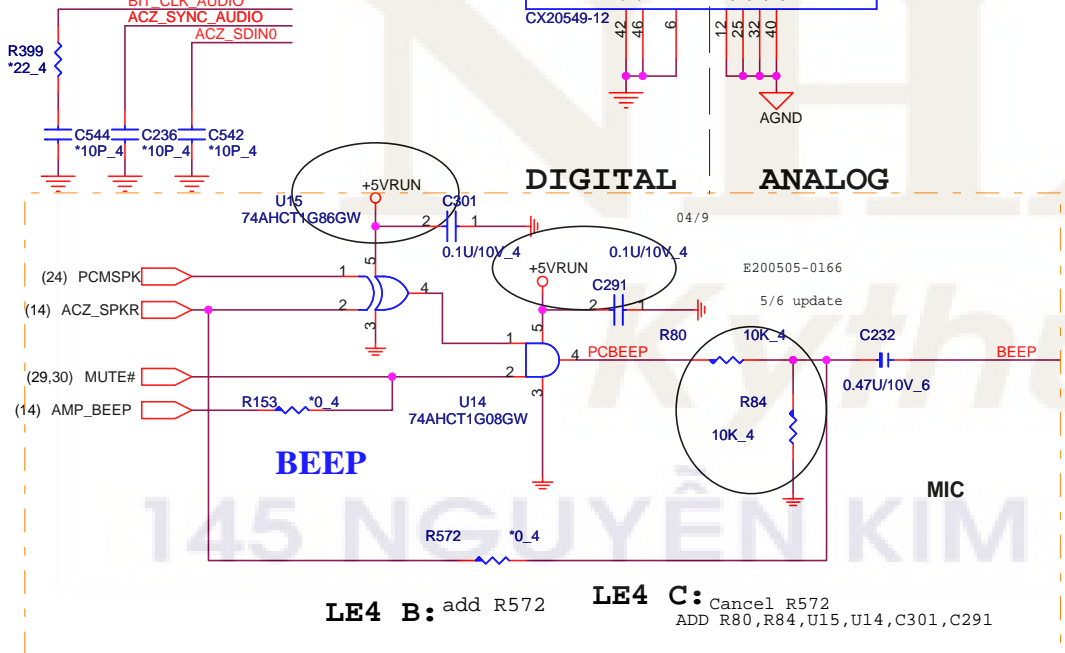
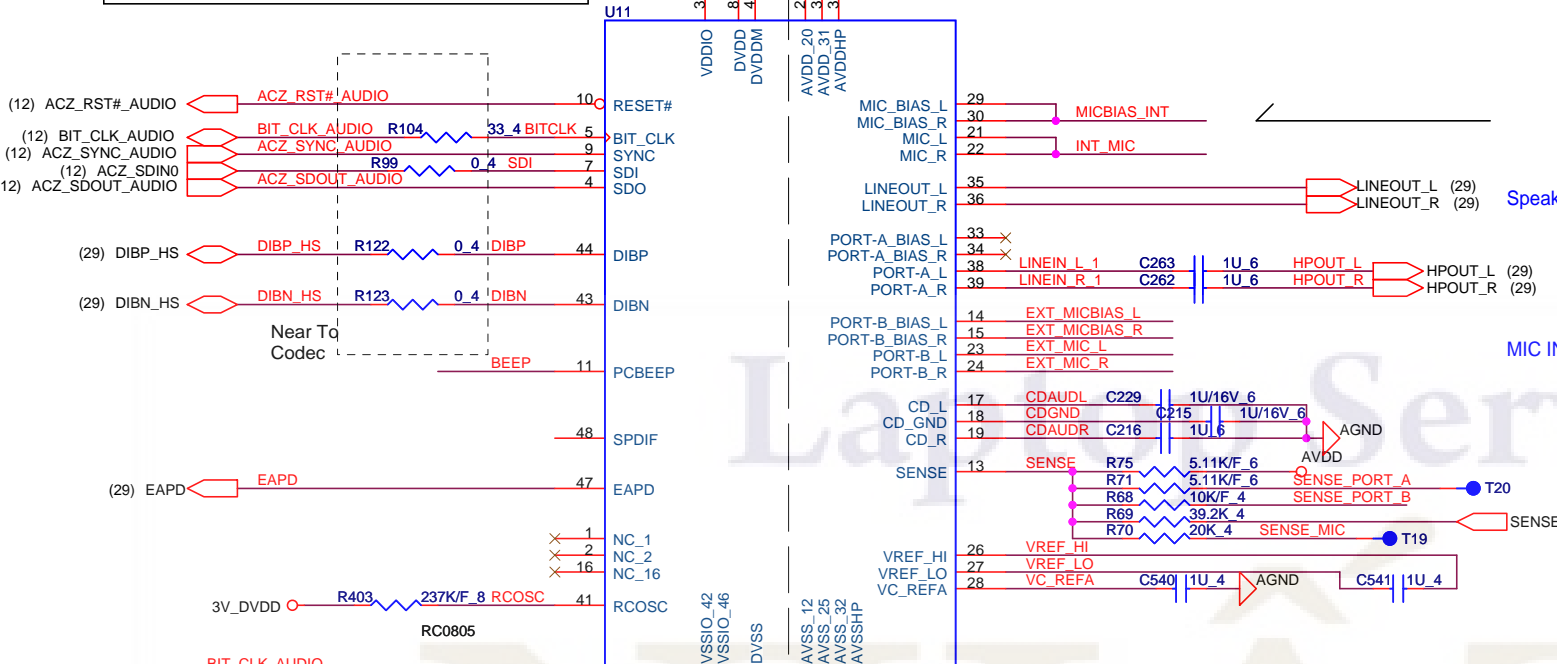
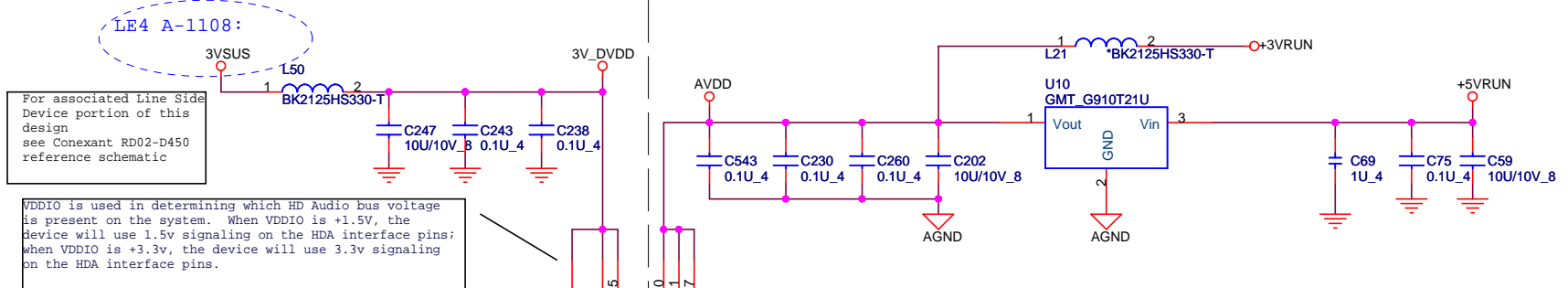


For Debug Only



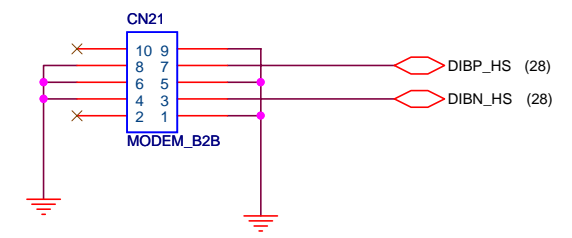
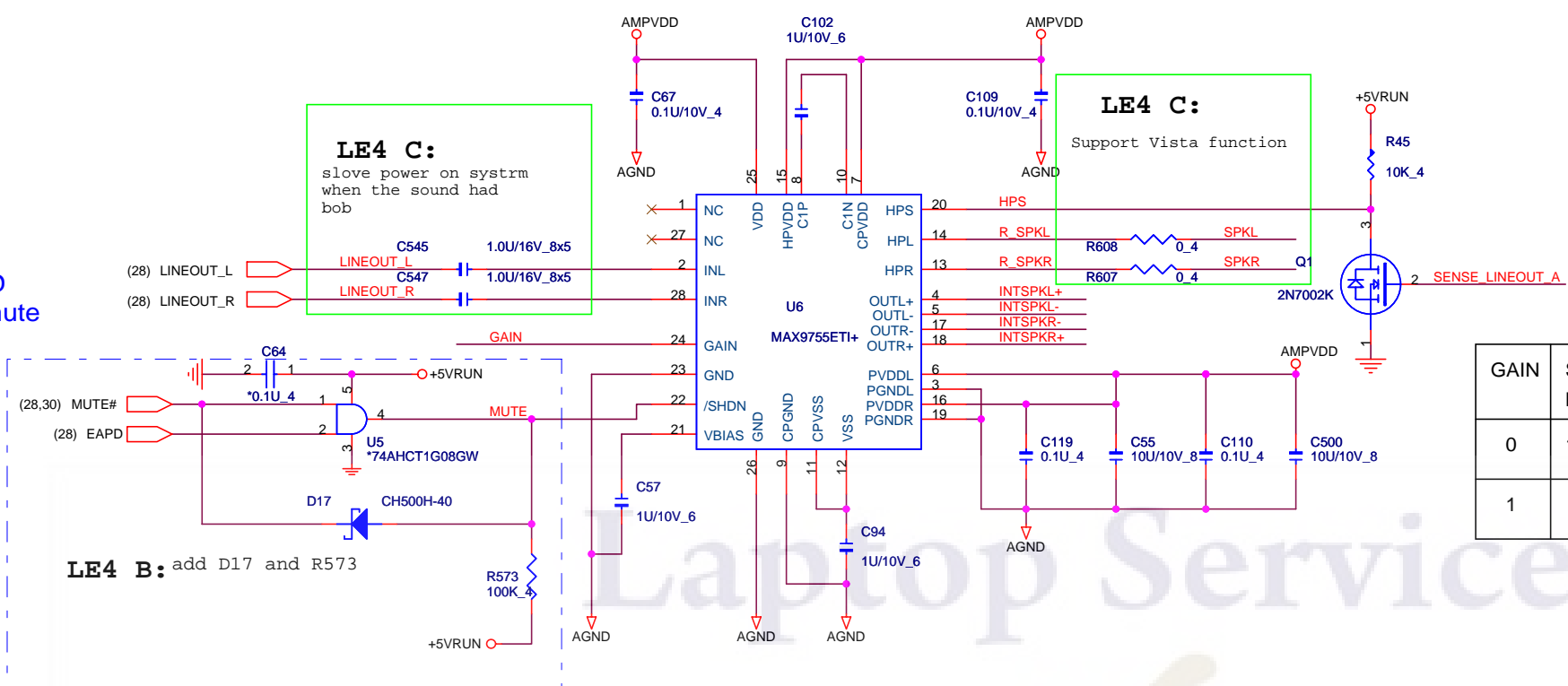
145 NGUYỄN KIM - P.7 - Q.10

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0816a

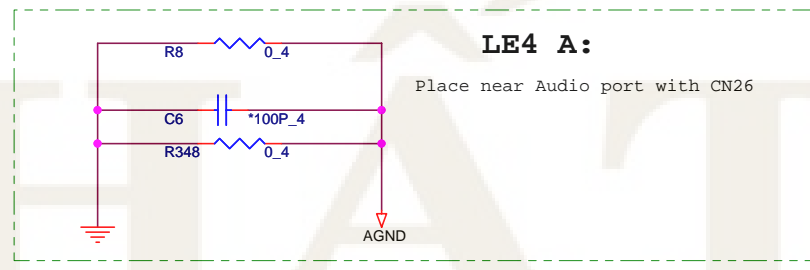
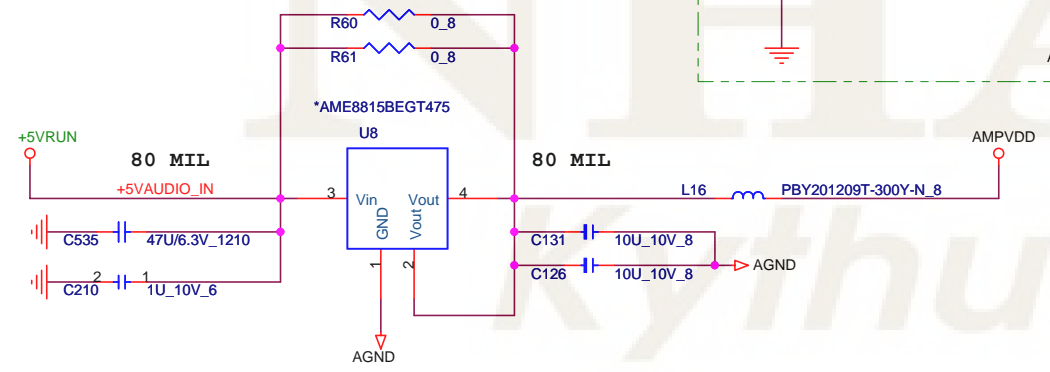
EAPD
low:mute



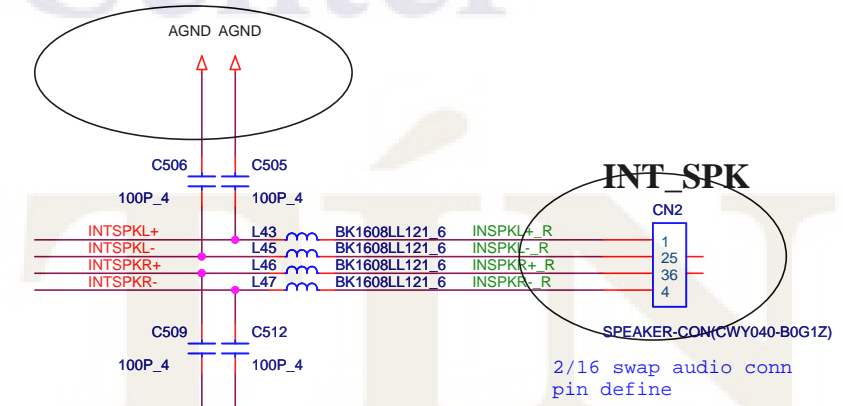
Modem connector

AUDIO POWER

AUDIO POWER

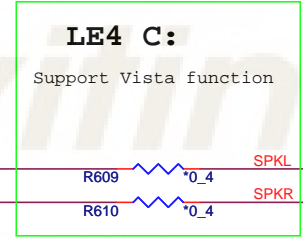


LE4 A:
Place near Audio port with CN26

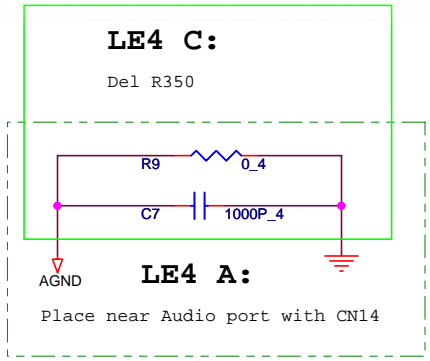


INT_SPK

2/16 swap audio conn pin define

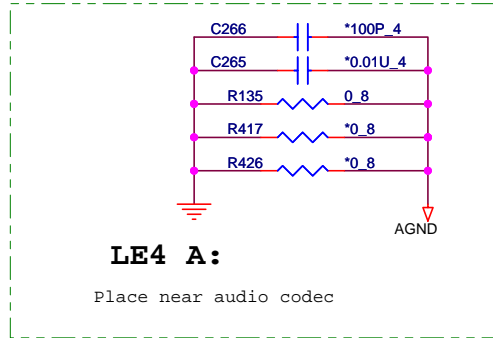


LE4 C:
Support Vista function

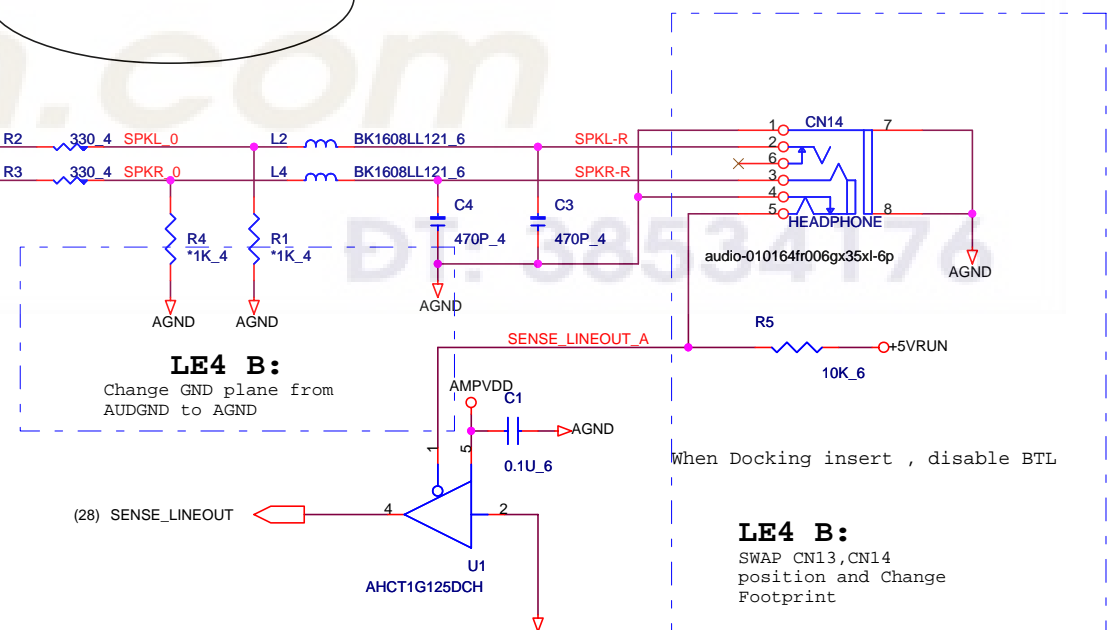


LE4 C:
Del R350

LE4 A:
Place near Audio port with CN14



LE4 A:
Place near audio codec

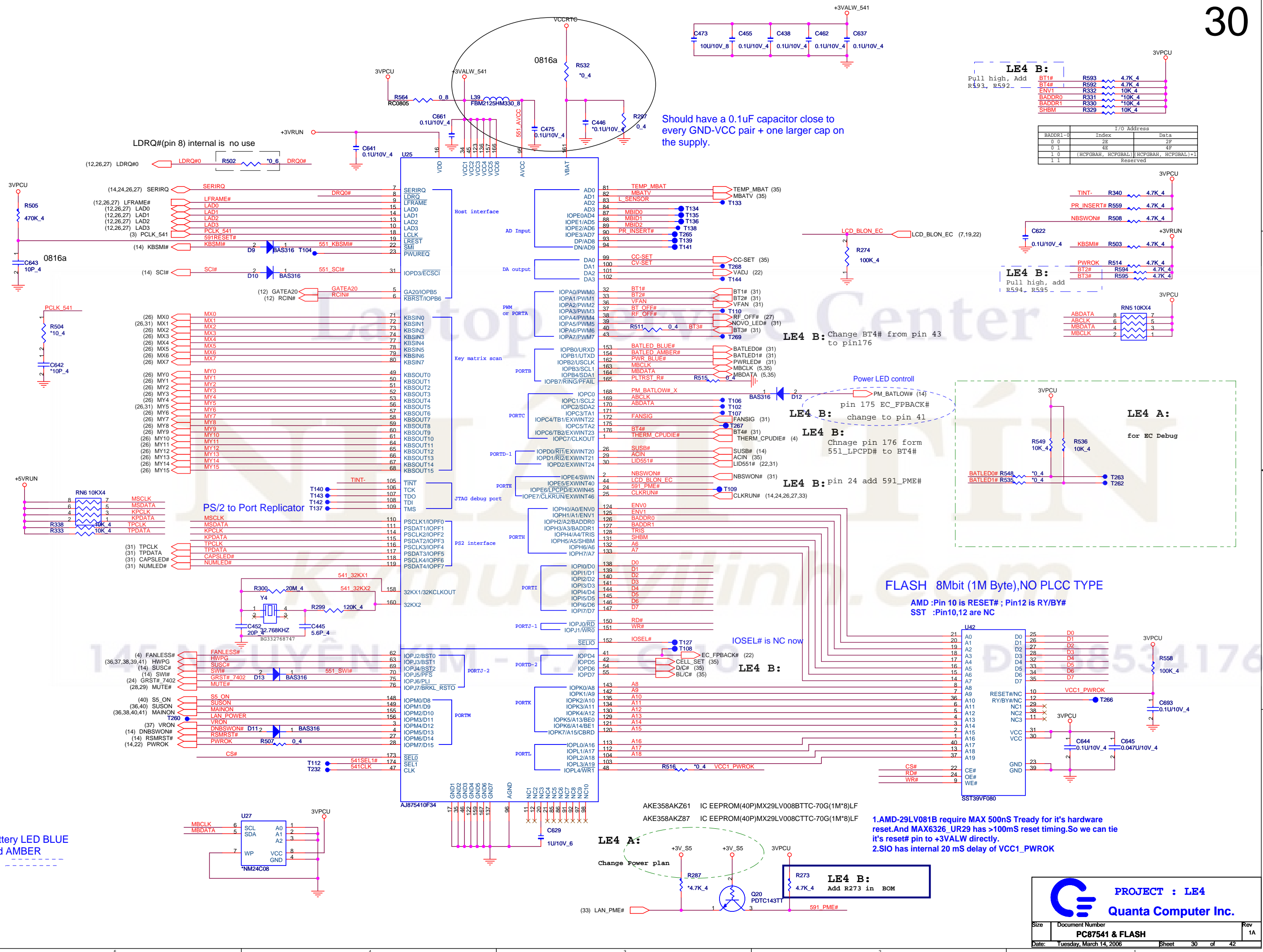


LE4 B:
Change GND plane from AUDGND to AGND

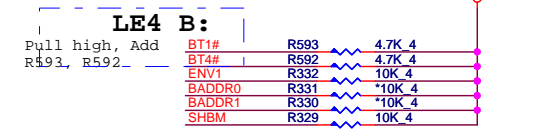
LE4 B:
SWAP CN13, CN14 position and Change Footprint

PROJECT : LE4
Quanta Computer Inc.

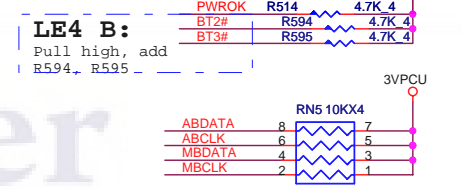
Size	Document Number	Rev
	Audio Amp.	1A
Date:	Tuesday, March 14, 2006	Sheet 29 of 42



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.



I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	



LE4 B: Change BT4# from pin 43 to pin176

LE4 B: change to pin 41

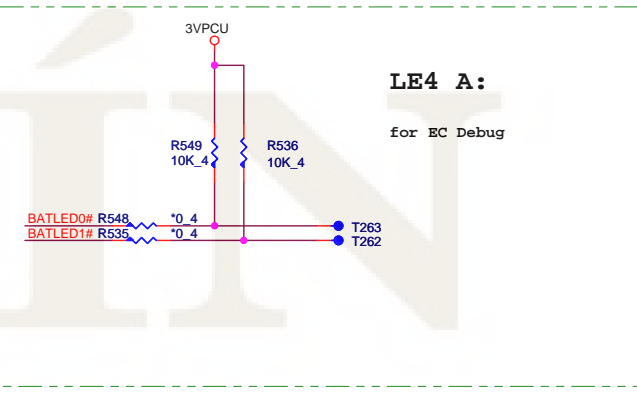
LE4 B: Chnage pin 176 form 551_LPCPD# to BT4#

LE4 B: pin 24 add 591_PME#

LE4 B: IOSEL# is NC now

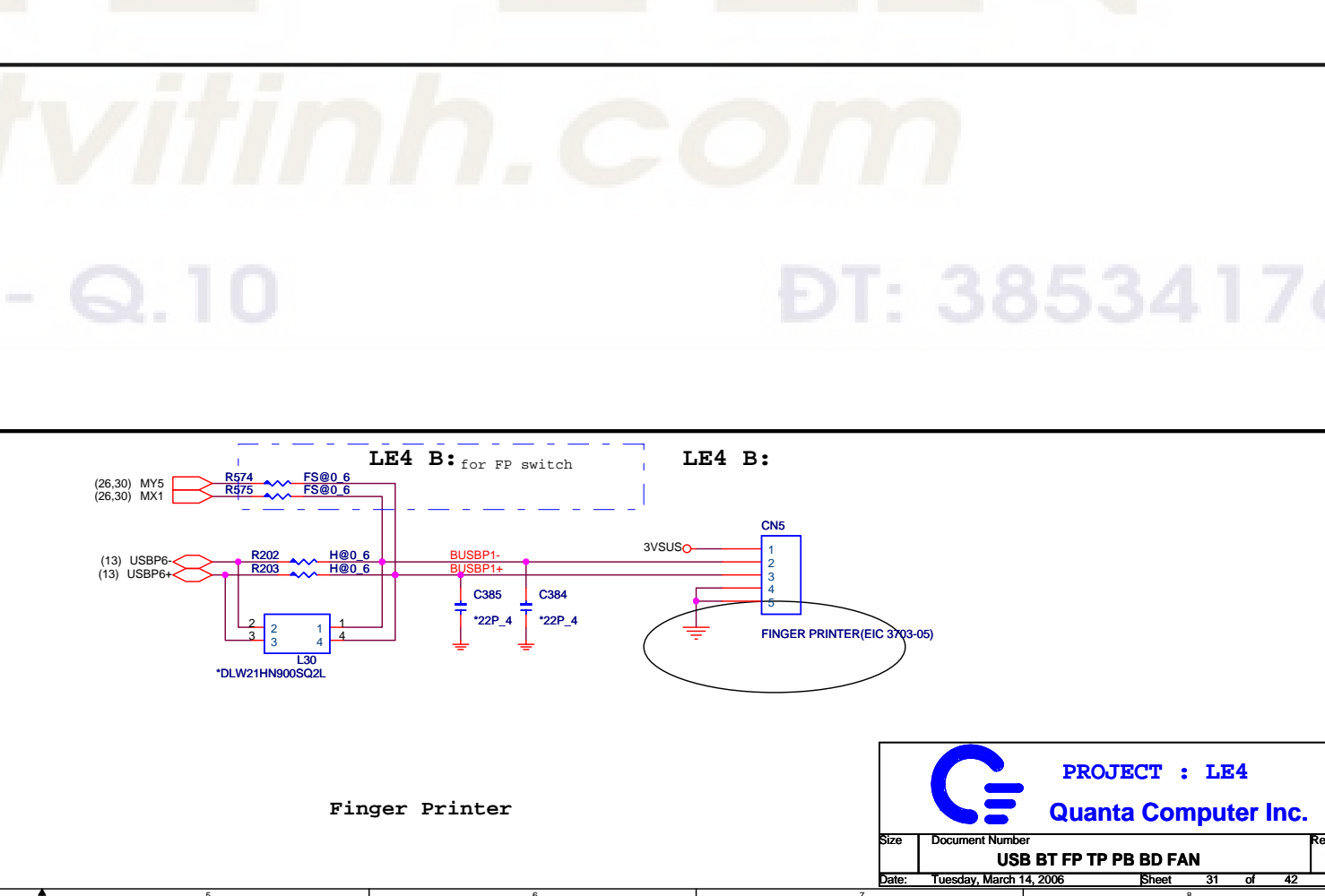
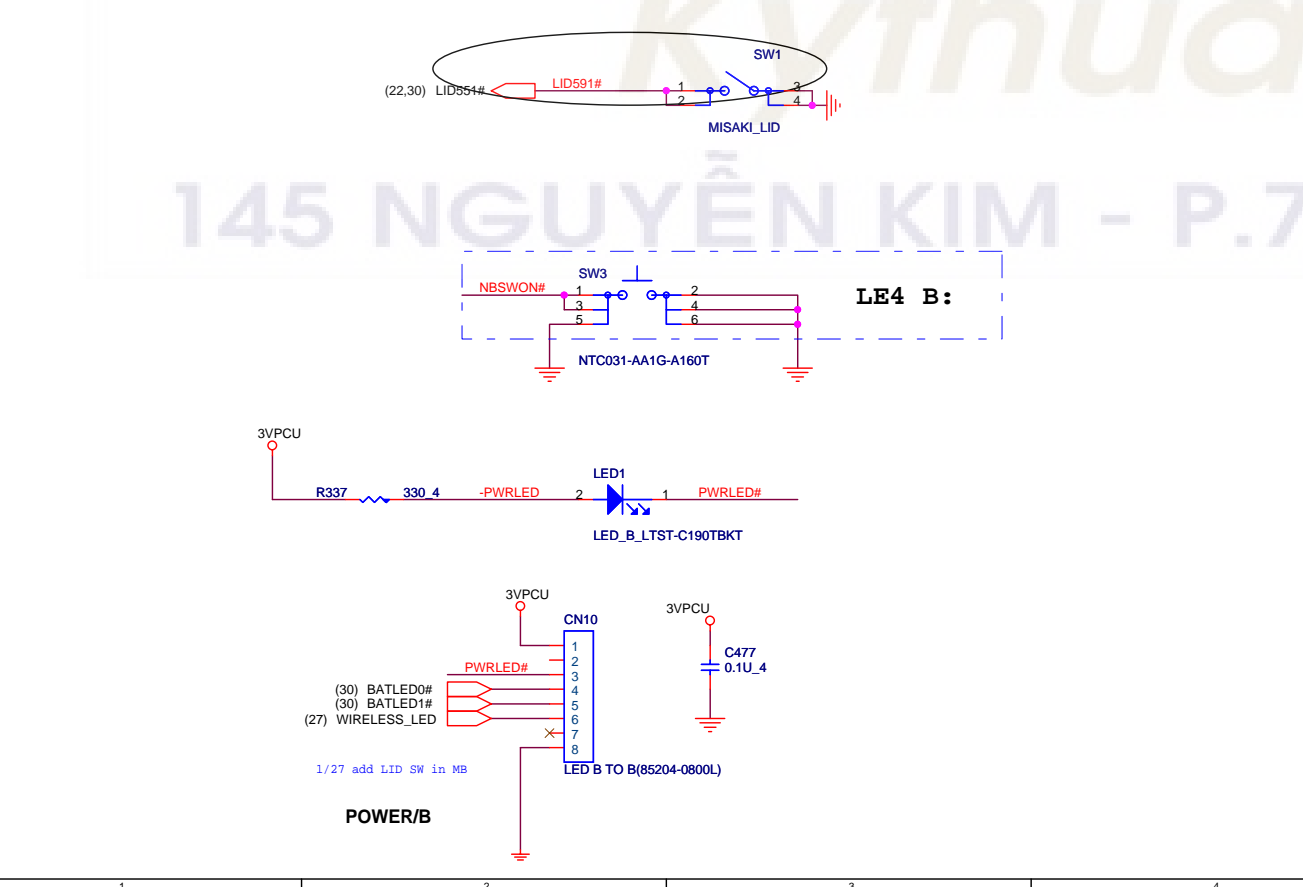
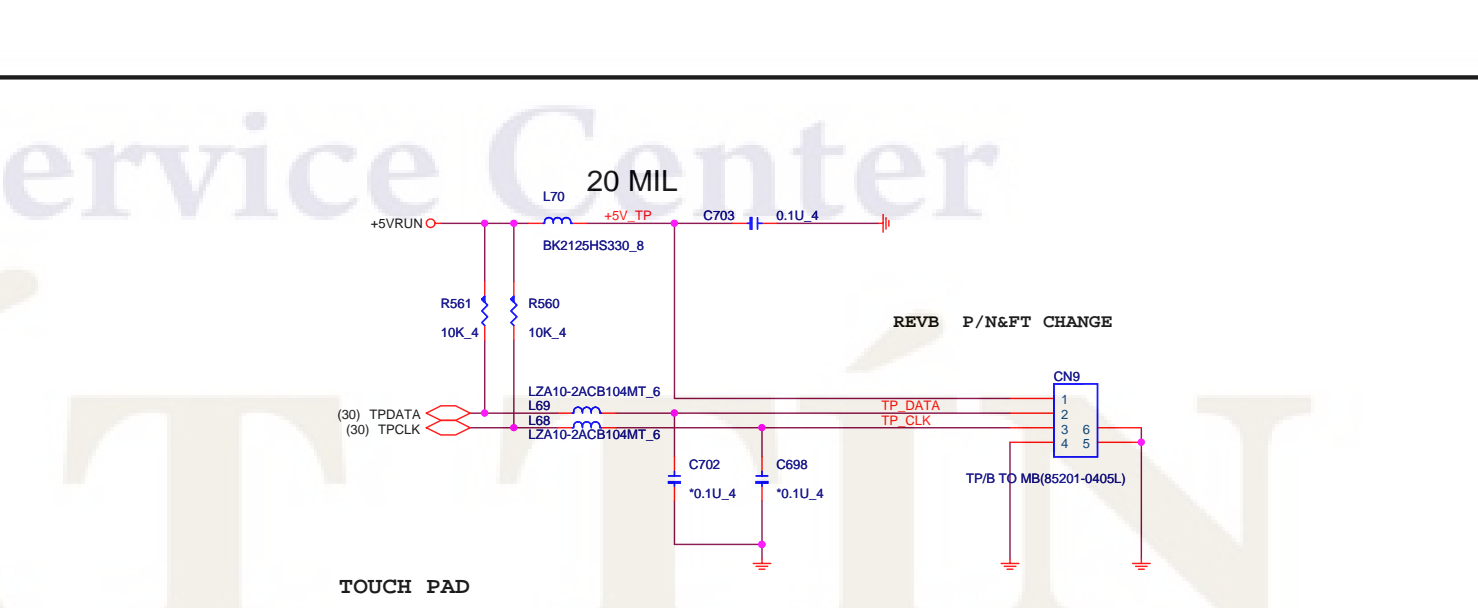
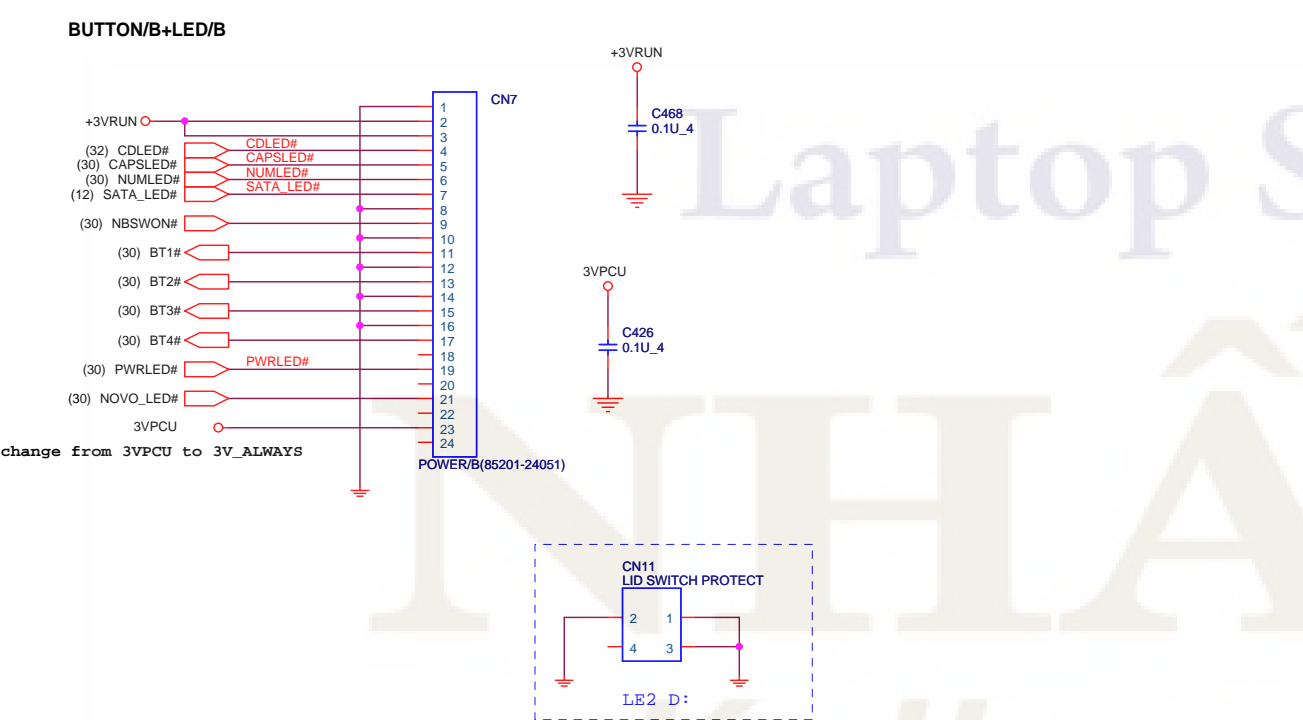
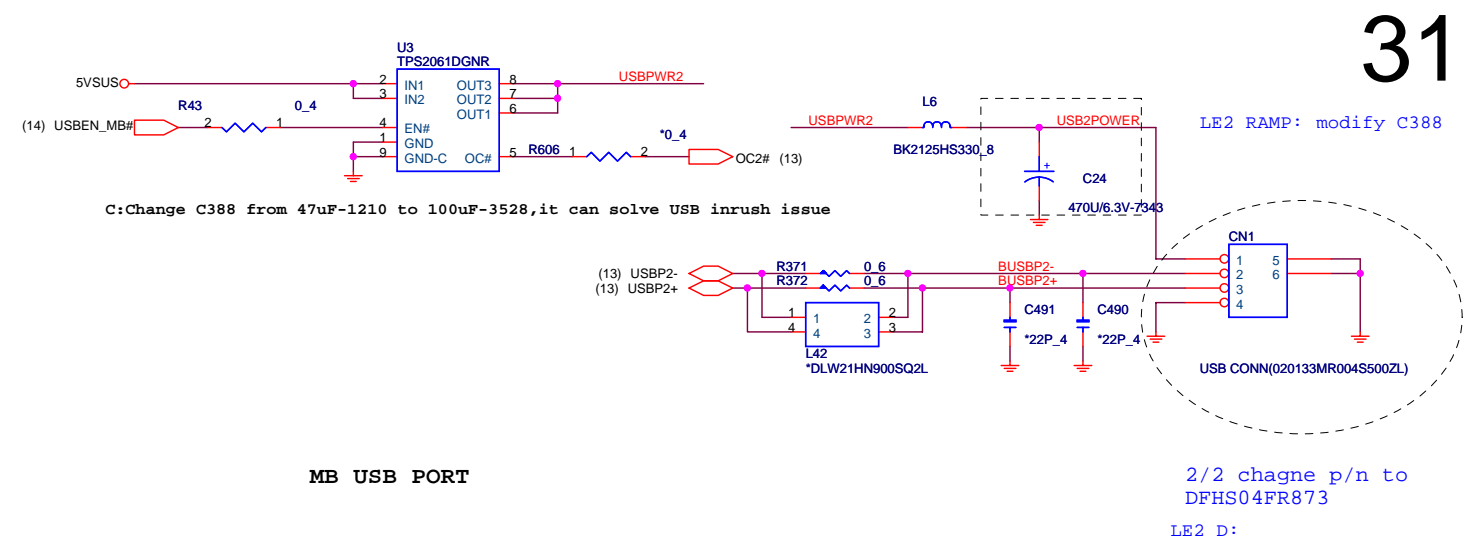
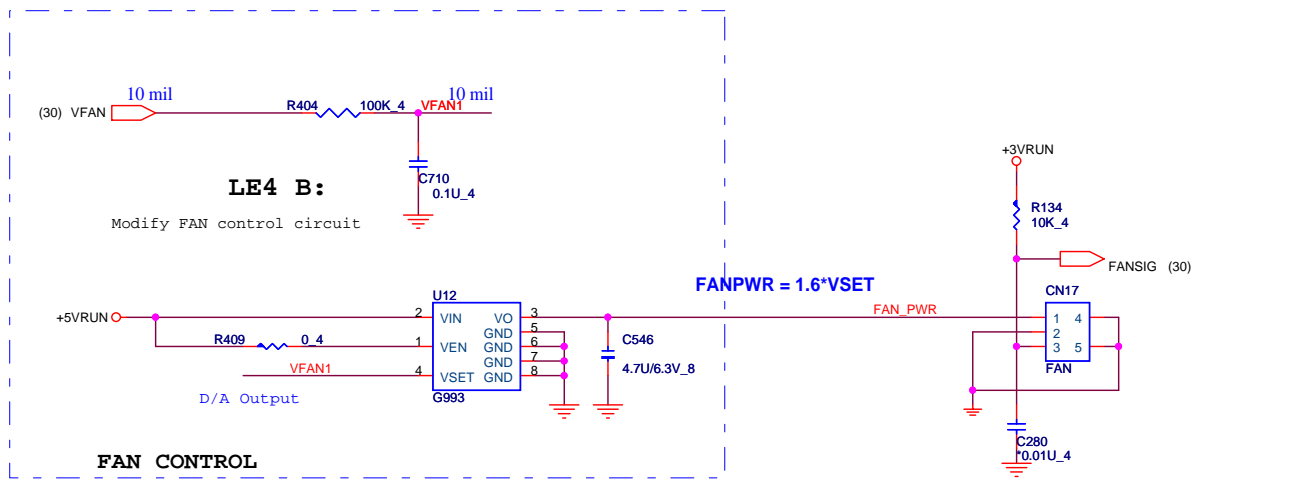
LE4 B:

FLASH 8Mbit (1M Byte),NO PLCC TYPE
 AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
 SST :Pin10,12 are NC



PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	PC87541 & FLASH	1A
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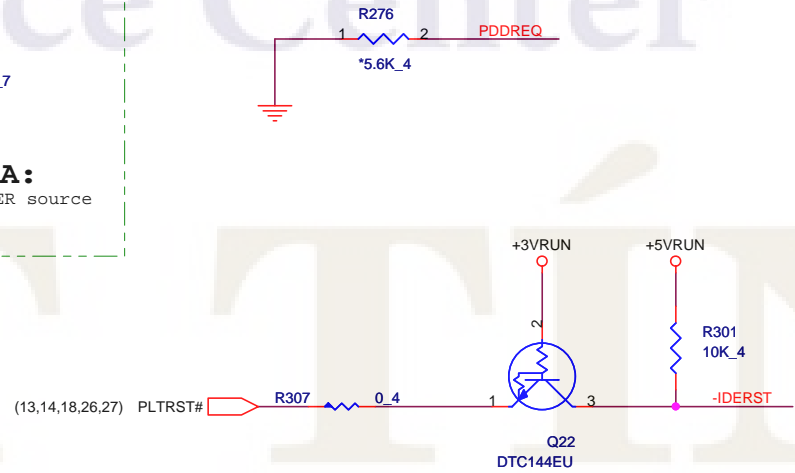
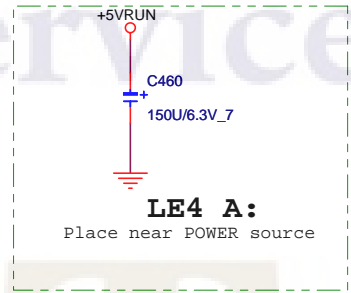
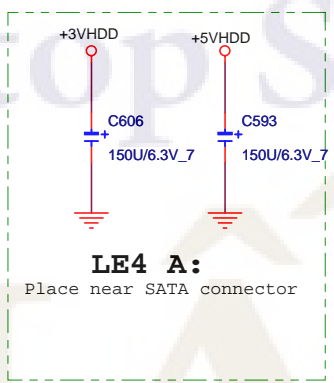
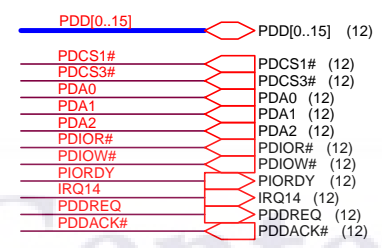
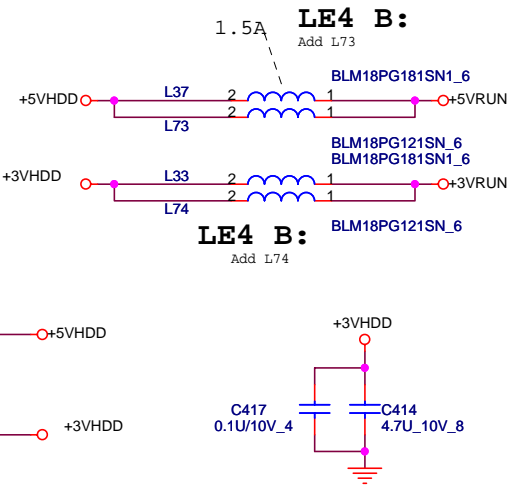
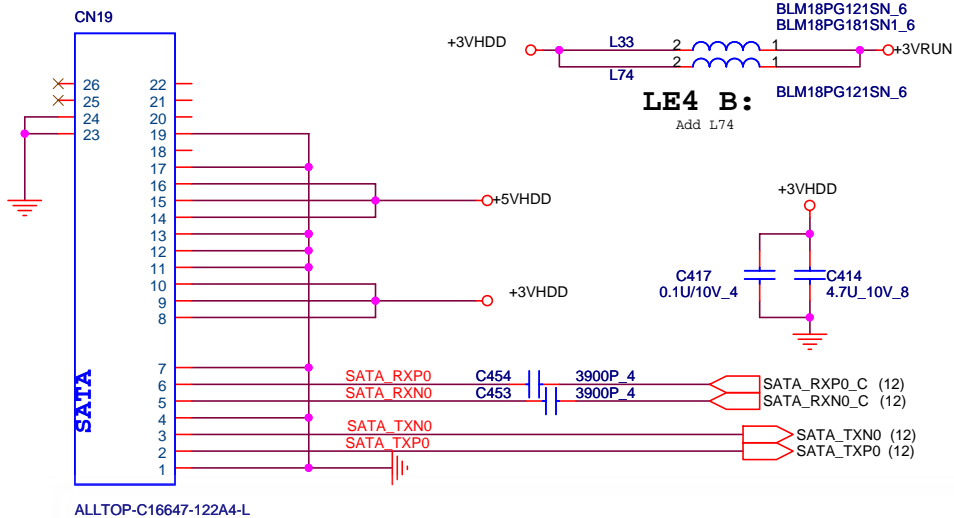


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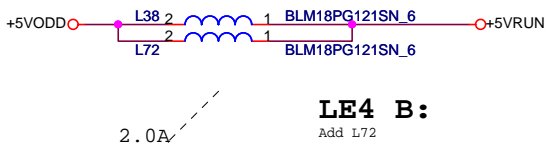
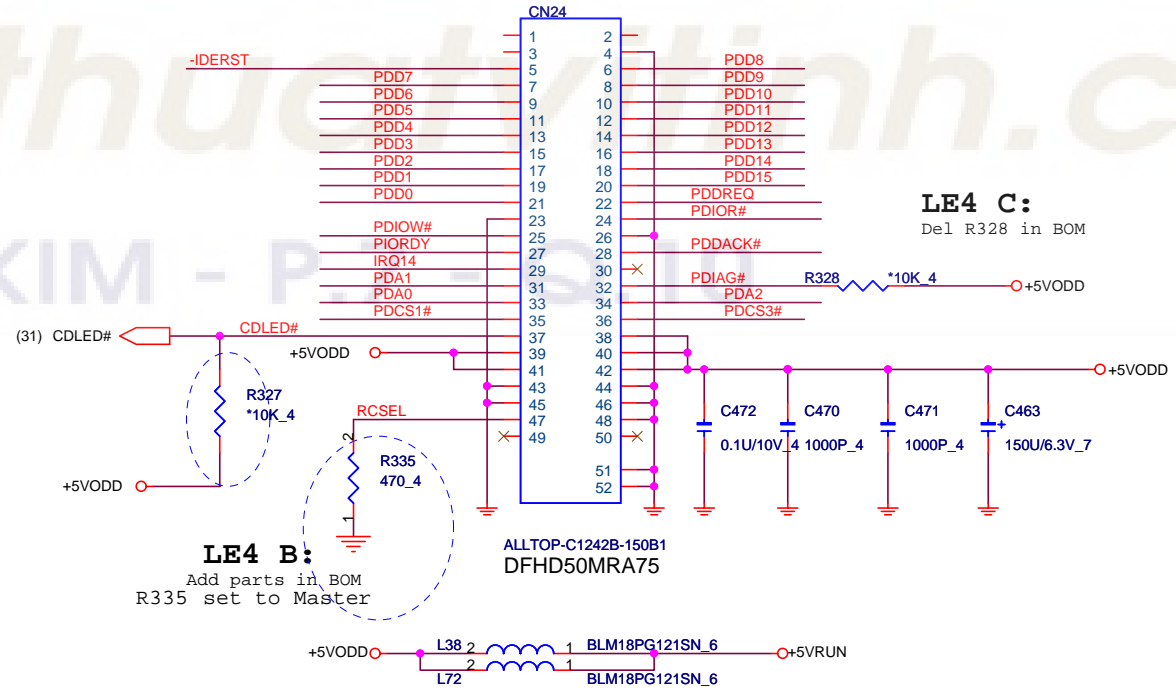
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SATA HDD



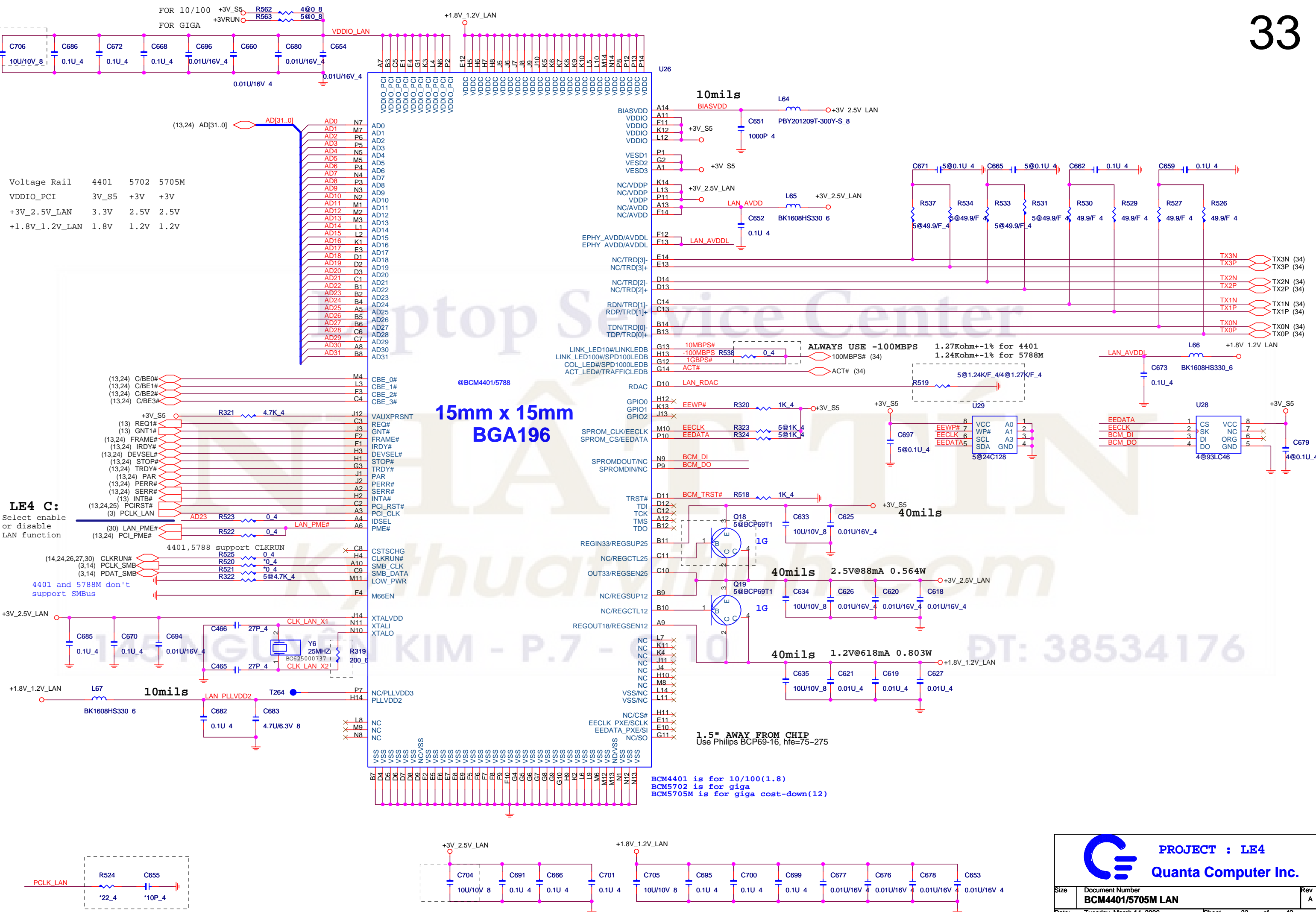
ODD LE4 B:
CN24 change back to LE2 footprint



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Quanta Computer Inc.

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	SATA HDD & PATA ODD	1A
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Voltage Rail	4401	5702	5705M
VDDIO_PCI	3V_S5	+3V	+3V
+3V_2.5V_LAN	3.3V	2.5V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V	1.2V

LE4 C:
Select enable or disable LAN function

4401, 5788 support CLKRUN
4401 and 5788M don't support SMBus

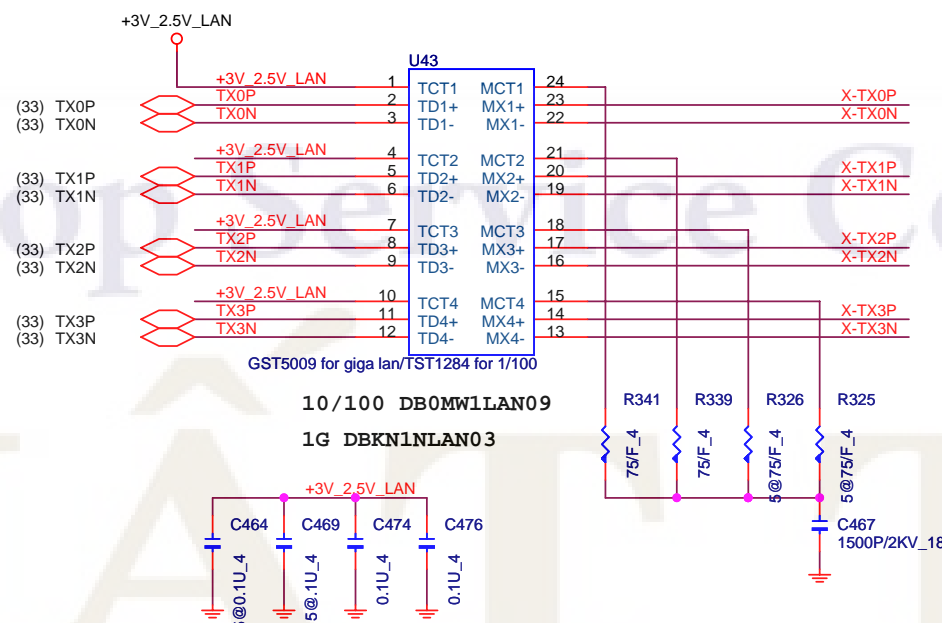
15mm x 15mm BGA196

BCM4401 is for 10/100(1.8)
BCM5702 is for giga
BCM5705M is for giga cost-down(12)

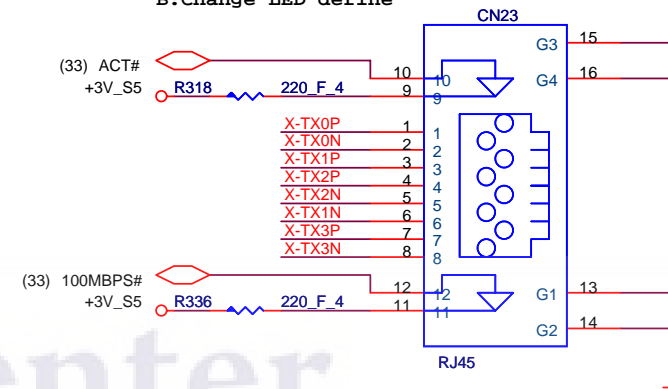
PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	BCM4401/5705M LAN	A
Date:	Tuesday, March 14, 2006	Sheet 33 of 42

B:Change 10/100 LAN transform U23 to ST1284A(DB0MWLAN09)



B:Change LED define



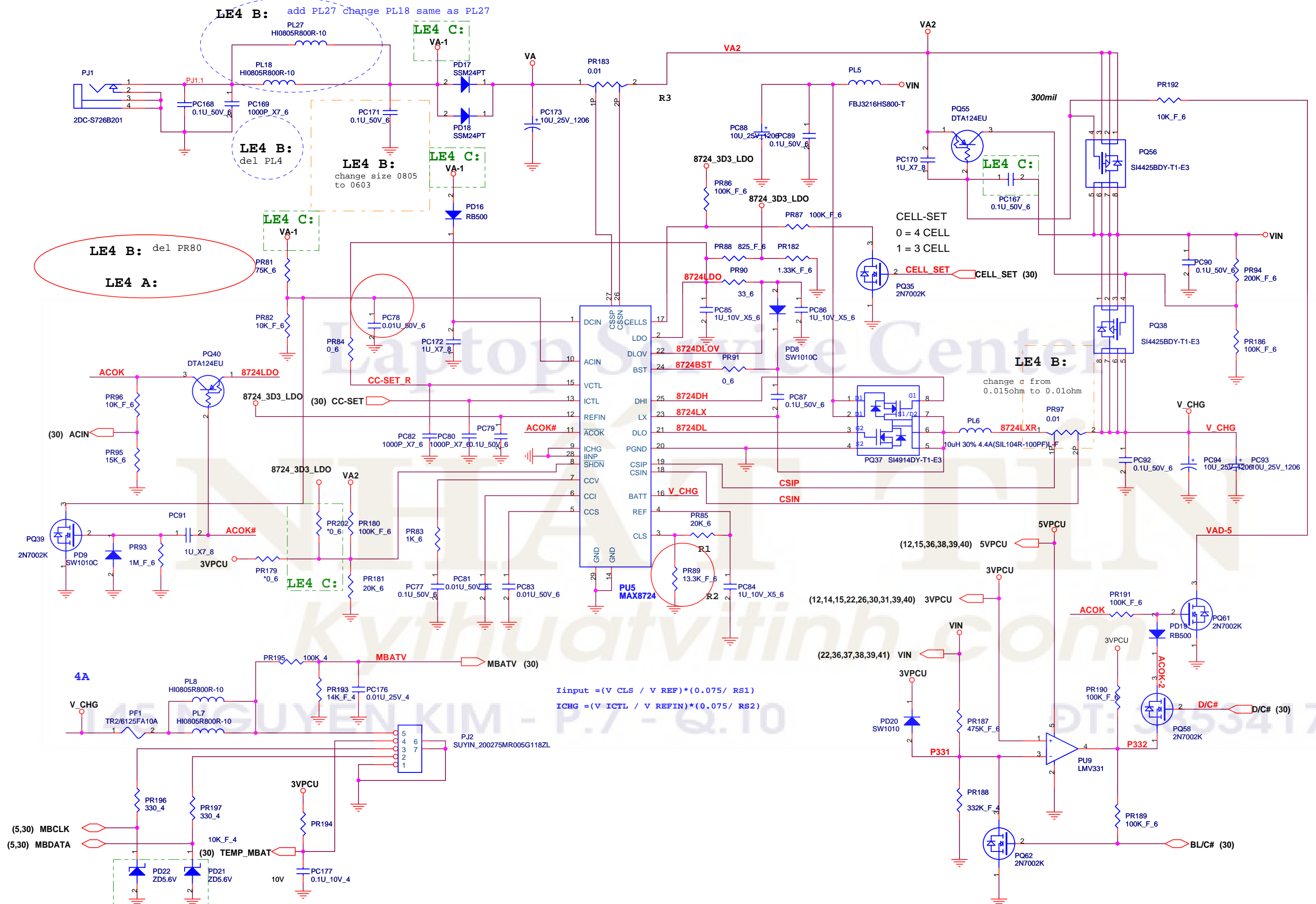
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NHÂN TIẾN

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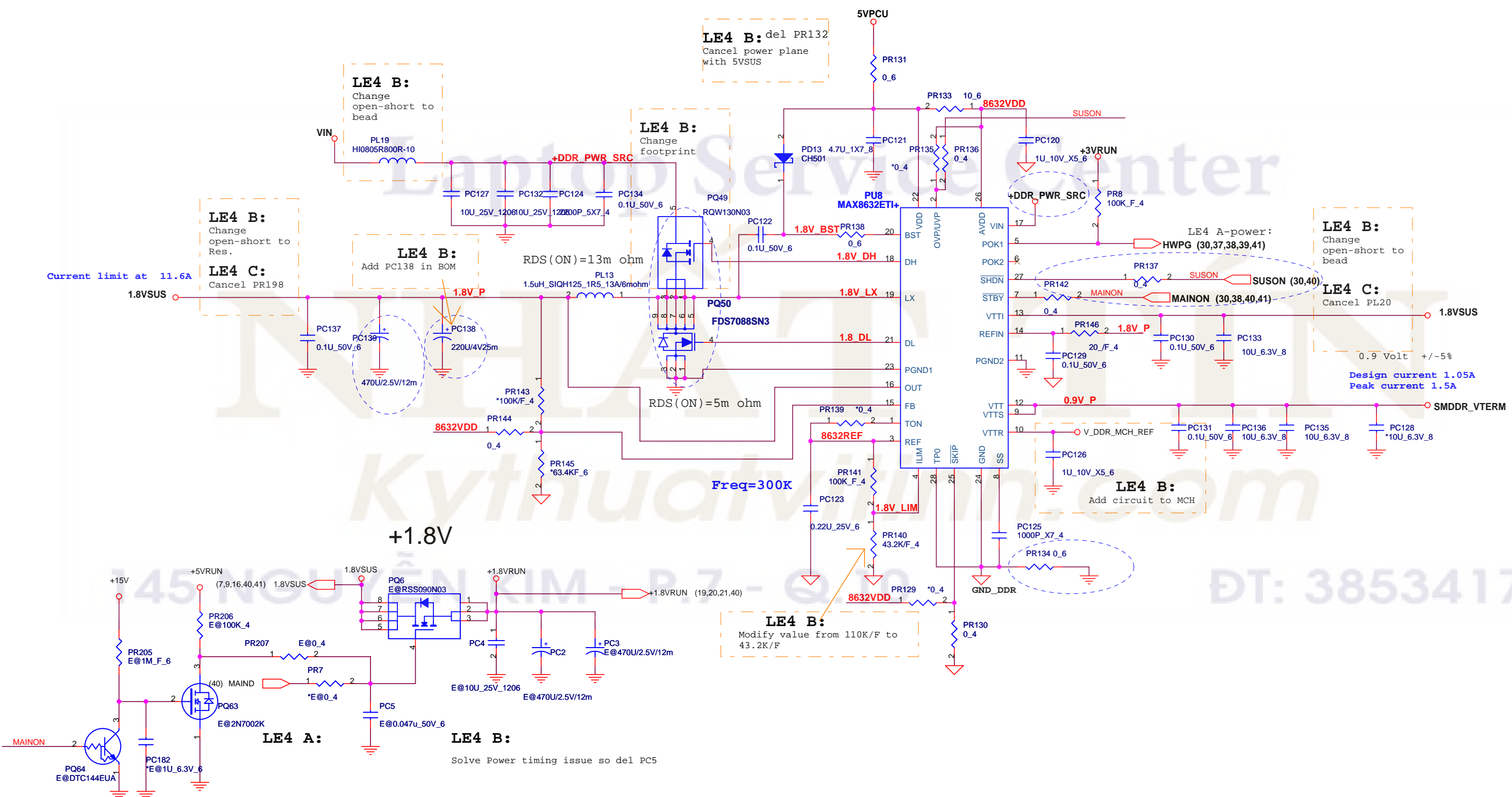
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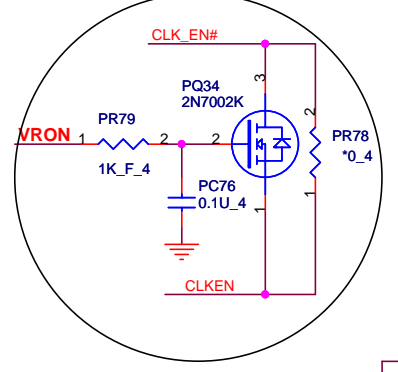


$$I_{input} = (V_{CLS} / V_{REF}) * (0.075 / R_{S1})$$

$$I_{CHG} = (V_{ICTL} / V_{REFIN}) * (0.075 / R_{S2})$$



LE4 B:
Change netname from
VR_PWRGD_CK410# to CLK_EN#



LE4 B: change PC68
10u 25V_1206 to 4.7u_0805

LE4 B:
Change
open-short to
bead

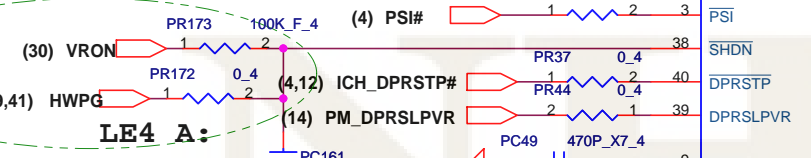
LE4 B:
Change
footprint

LE4 B:
Add PC20 in BOM

LE4 B:
Change
footprint

LE4 B:
Add PC20
in BOM

LE4 B:
Del PC26
parts in
BOM



LE4 A:

LE4 B:
Change rename

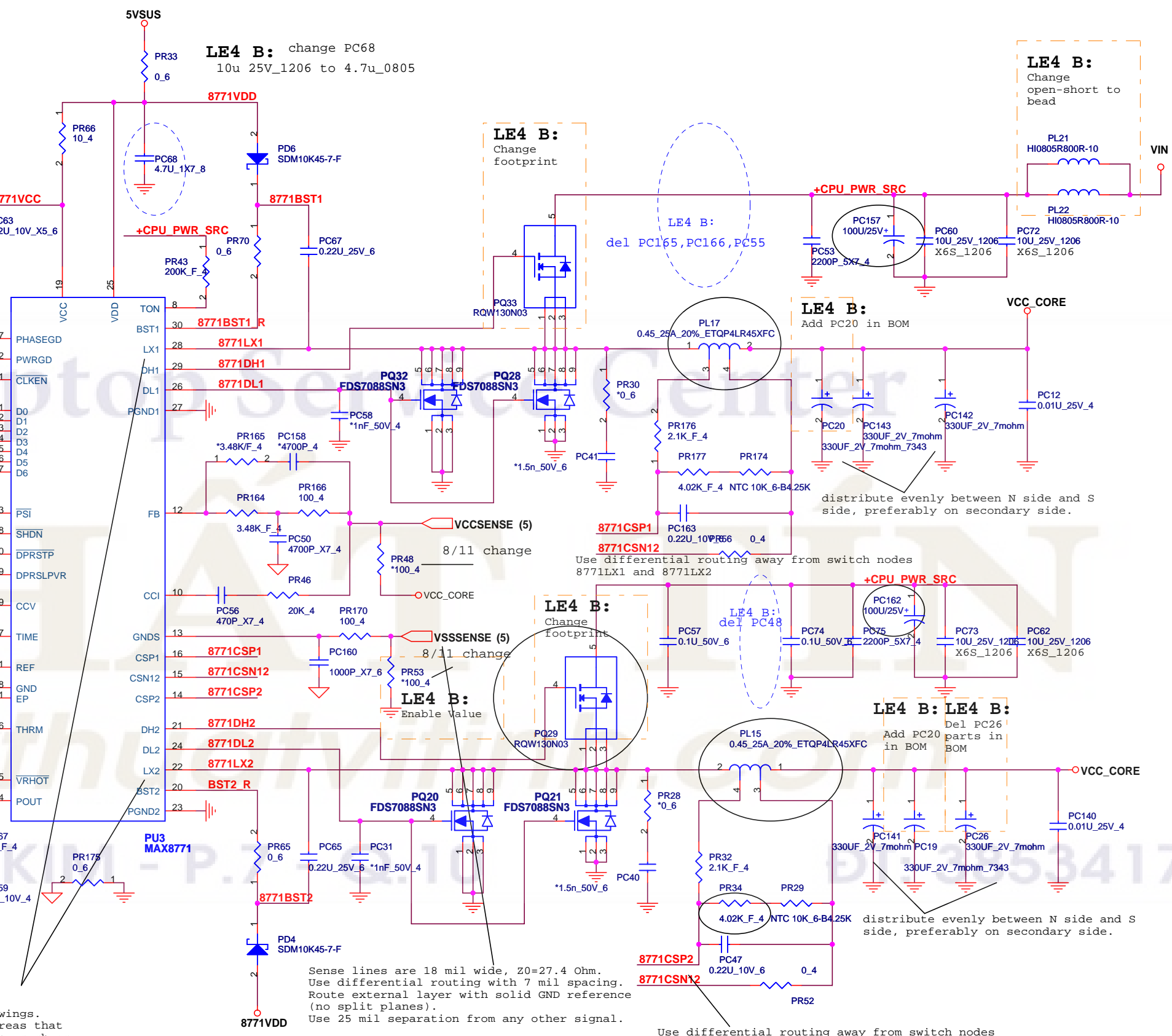
Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

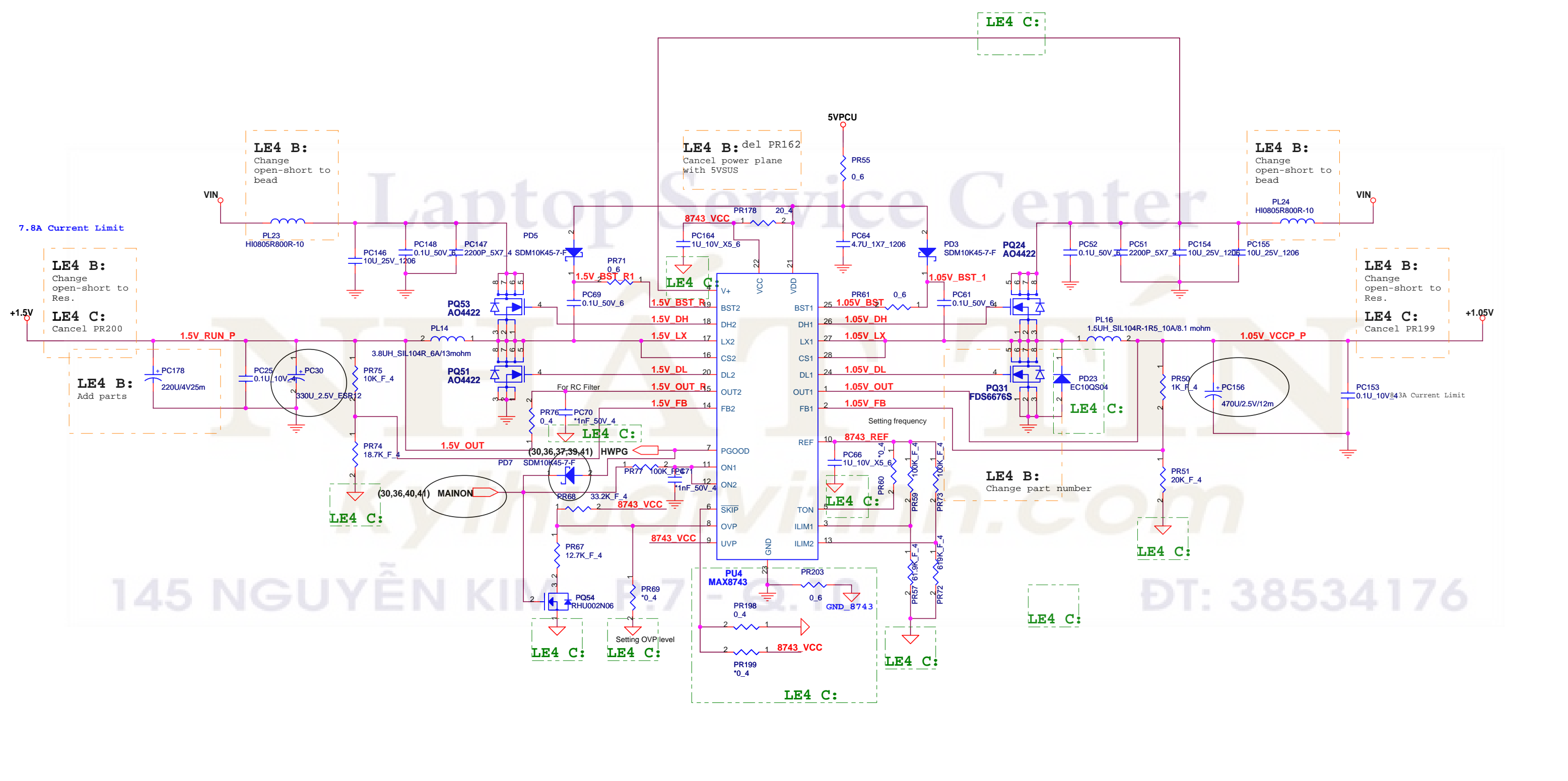
Sense lines are 18 mil wide, Z0=27.4 Ohm. Use differential routing with 7 mil spacing. Route external layer with solid GND reference (no split planes). Use 25 mil separation from any other signal.

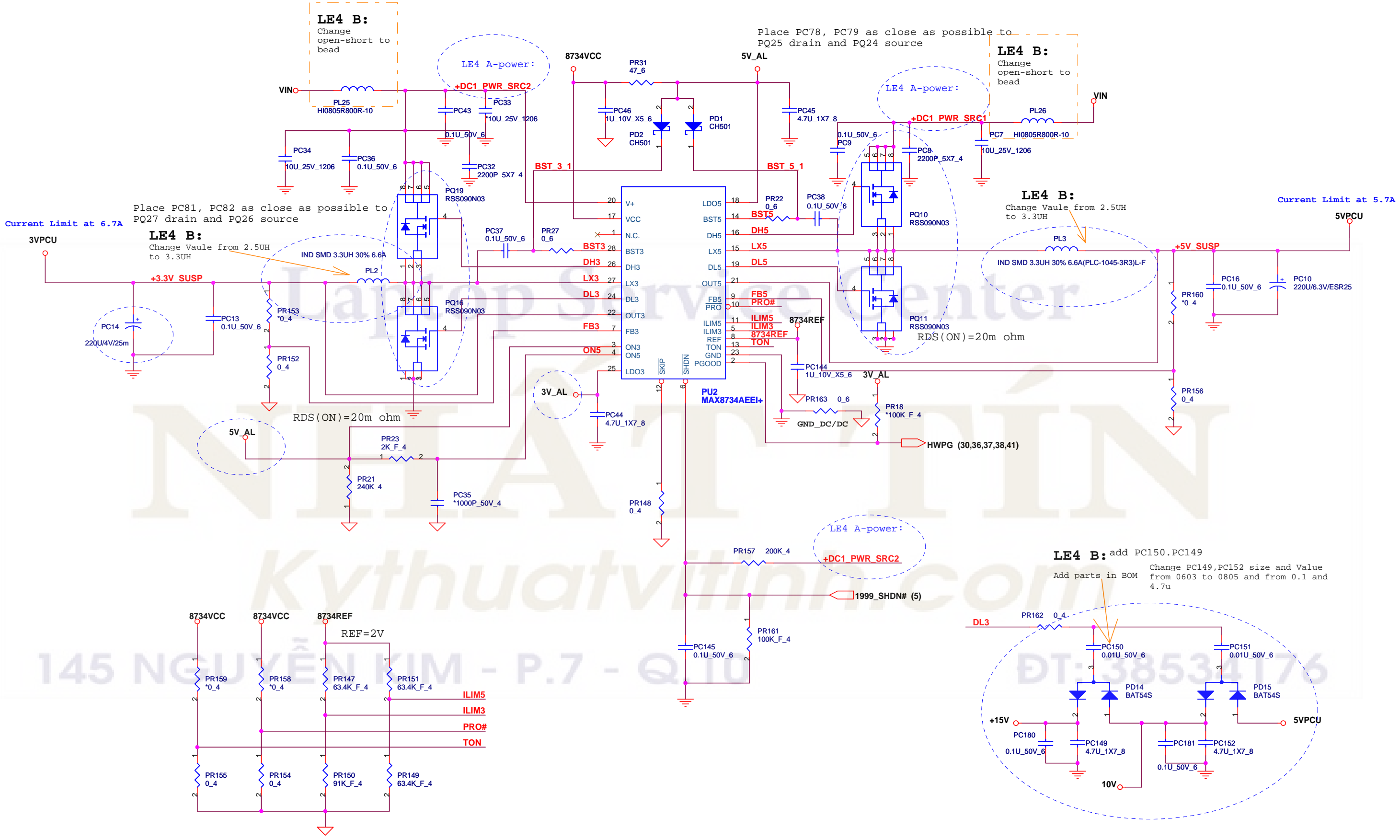
Use differential routing away from switch nodes 8771LX1 and 8771LX2

distribute evenly between N side and S side, preferably on secondary side.

distribute evenly between N side and S side, preferably on secondary side.







LE4 B:
Change open-short to bead

LE4 A-power:
+DC1 PWR_SRC2

Place PC78, PC79 as close as possible to PQ25 drain and PQ24 source

LE4 B:
Change open-short to bead

Place PC81, PC82 as close as possible to PQ27 drain and PQ26 source

LE4 B:
Change Vaule from 2.5UH to 3.3UH

LE4 B:
Change Vaule from 2.5UH to 3.3UH

Current Limit at 5.7A

RDS (ON) = 20m ohm

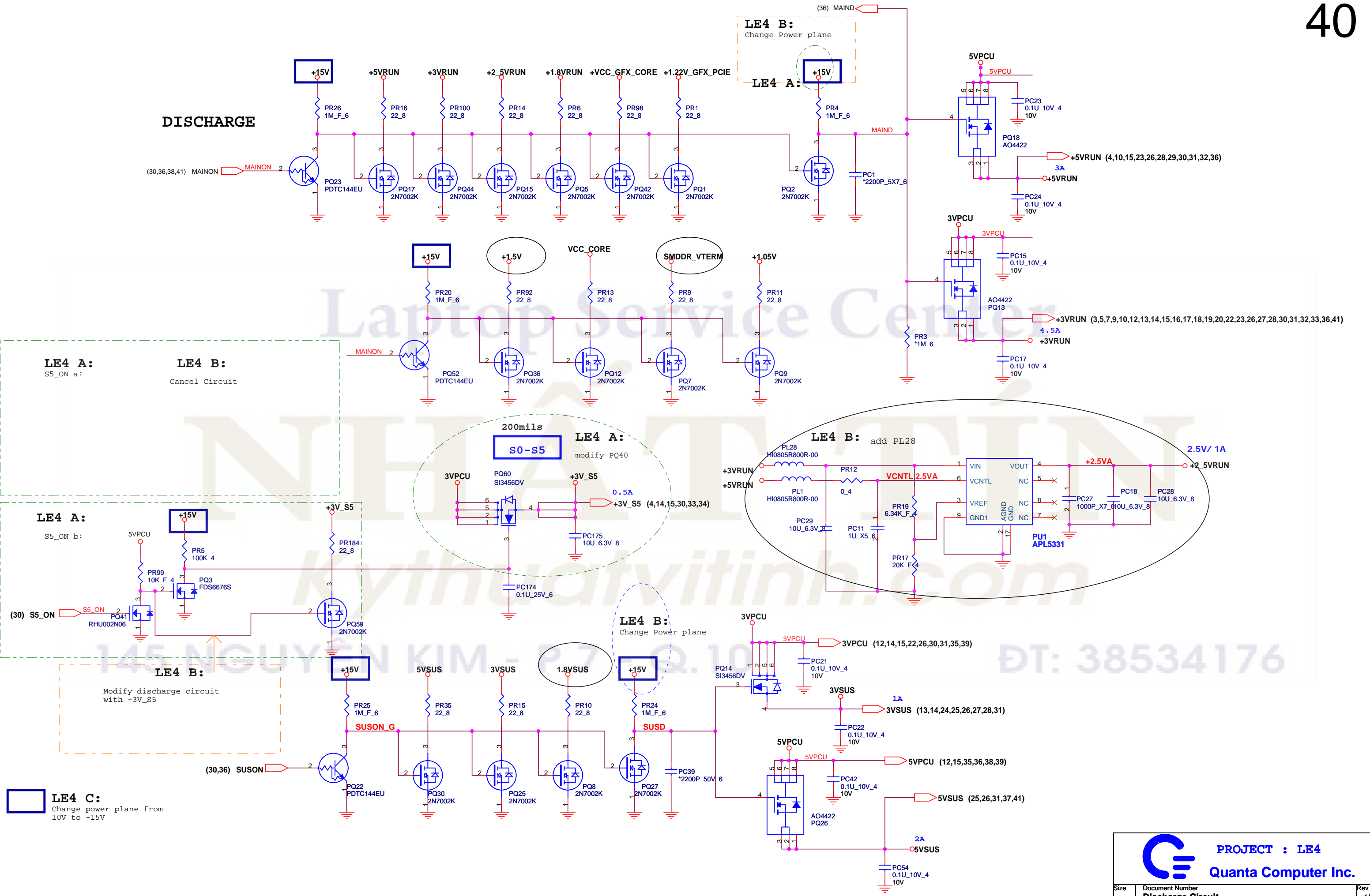
RDS (ON) = 20m ohm

LE4 B: add PC150.PC149
Change PC149,PC152 size and Value from 0603 to 0805 and from 0.1 and 4.7u

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Quanta Computer Inc.

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	D/D (MAX8734)	1A
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DISCHARGE

LE4 A: S5_ON a: Cancel Circuit

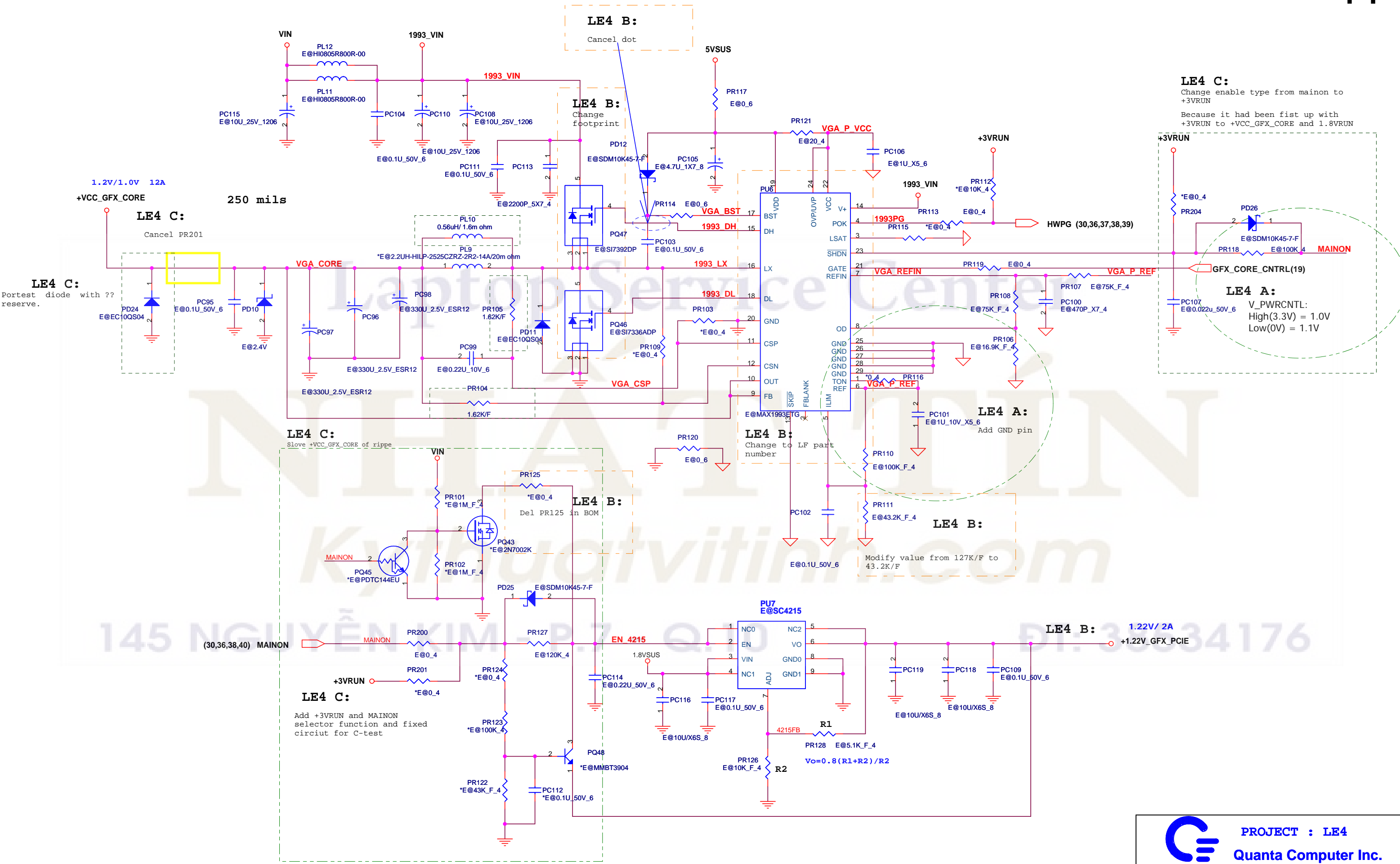
LE4 A: S5_ON b:

LE4 B: Modify discharge circuit with +3V_S5

LE4 C: Change power plane from 10V to +15V

PROJECT : LE4
Quanta Computer Inc.

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	Discharge Circuit	1A
Date:	Tuesday, March 14, 2006	Sheet 40 of 42



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MODEL	REV	CHANGE LIST		CW3 M/B	
				FROM	TO
CW3 M/B	1A	0316~0317	1. ADD EMI Solution (Per EMI Team suggestion)		A1A


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		PROJECT : LE4	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	Change History	1A	
Date:	Wednesday, November 16, 2005	Sheet	42 of 42