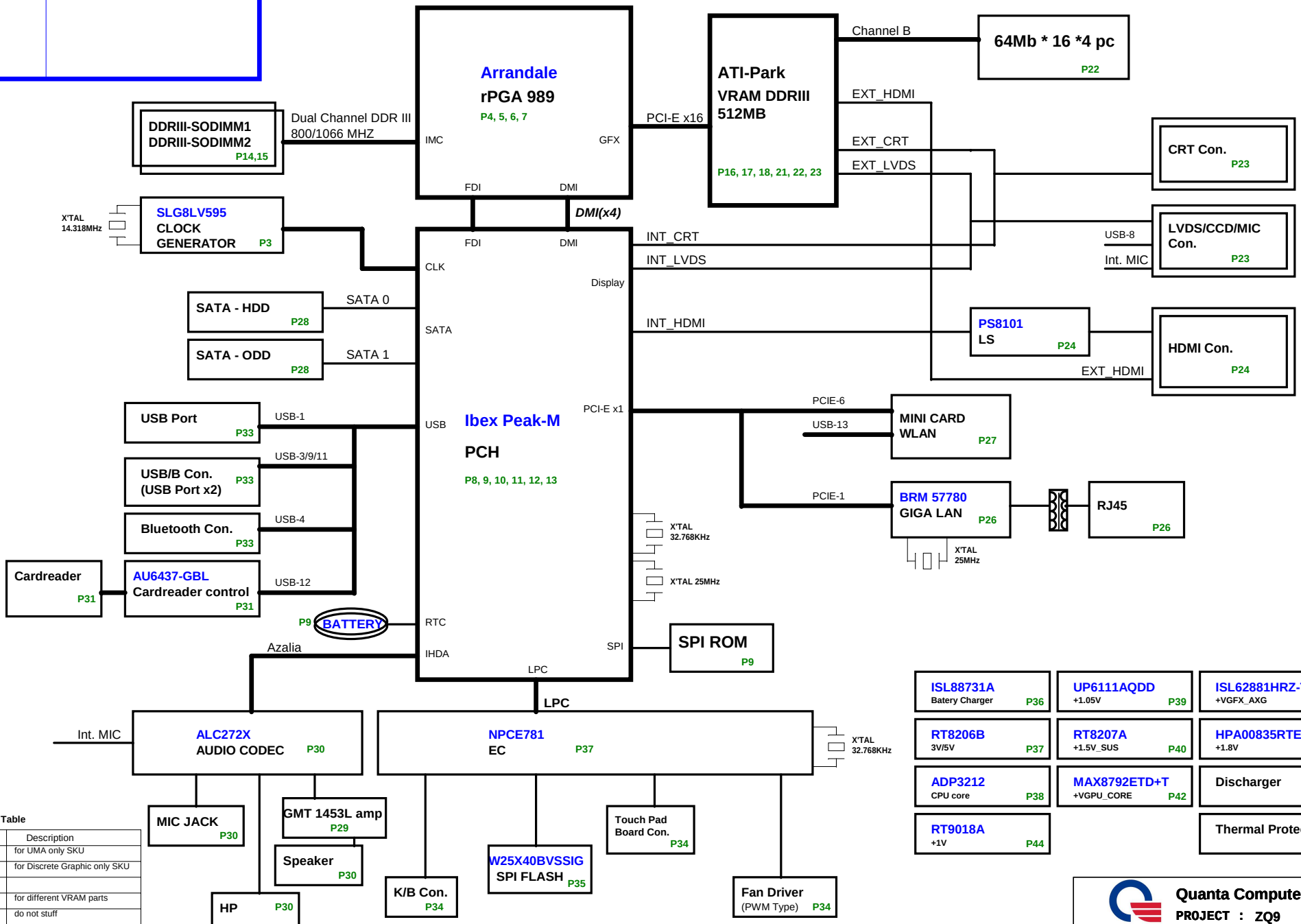
VER : 1A

BOM P/N	Description

ZQ9 SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

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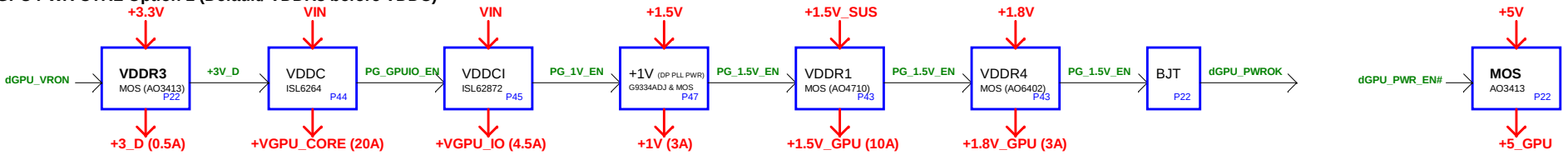
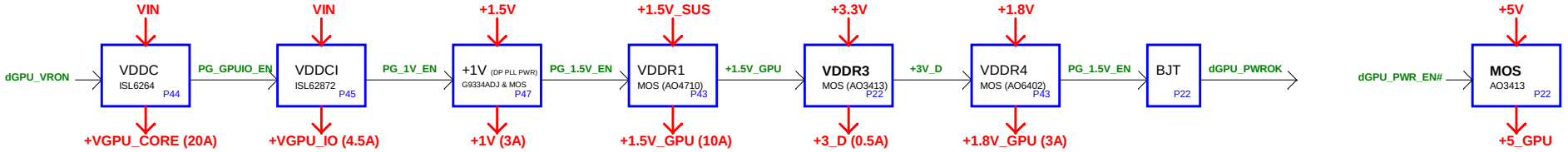
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



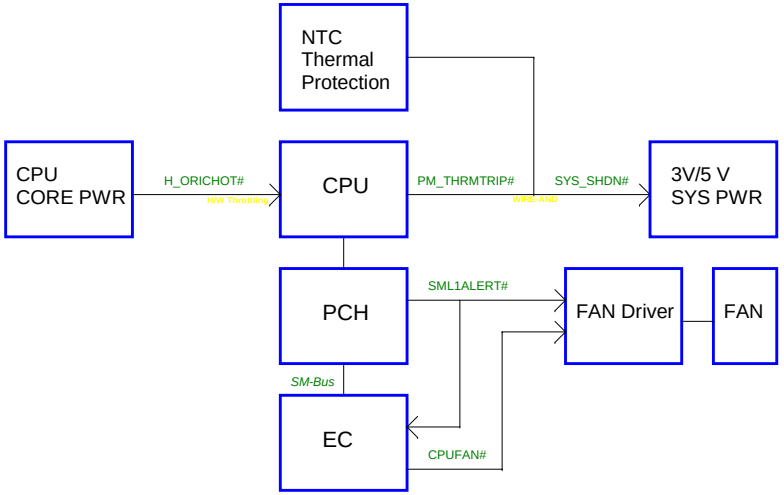
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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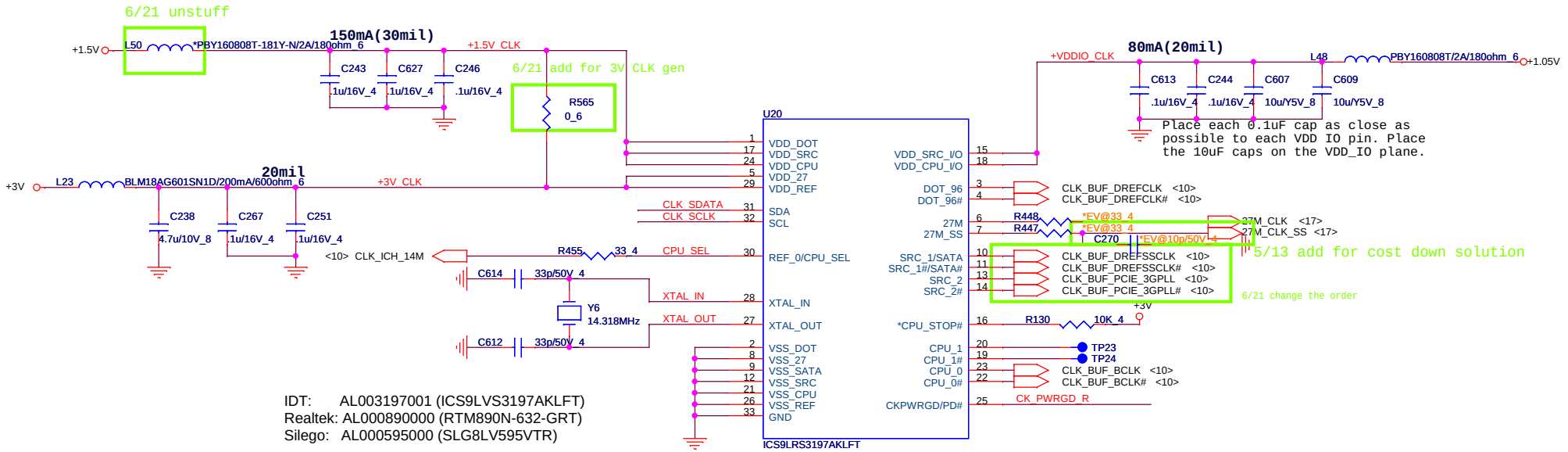
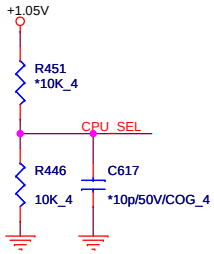


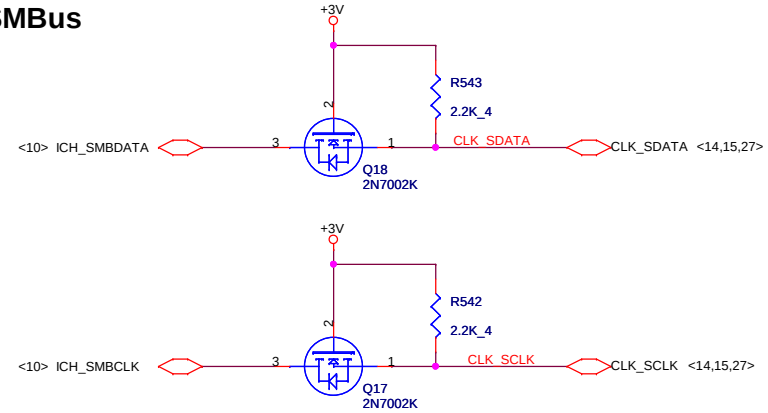
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

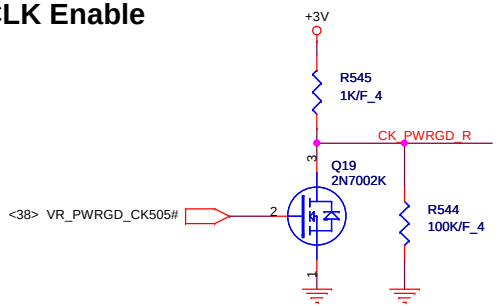


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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	Clock Generator	1A
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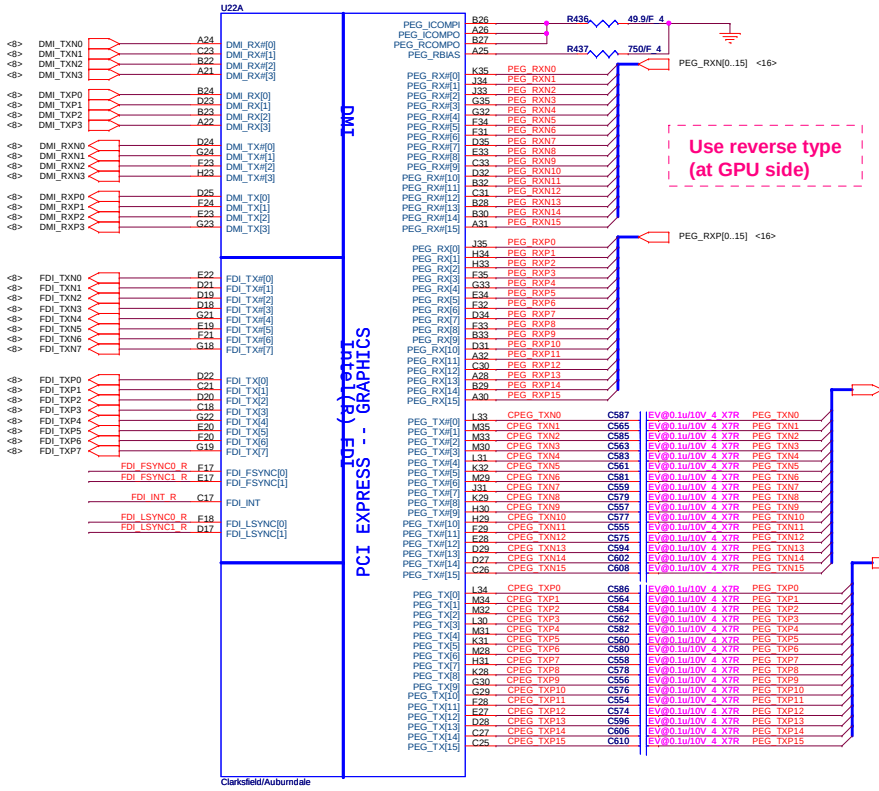
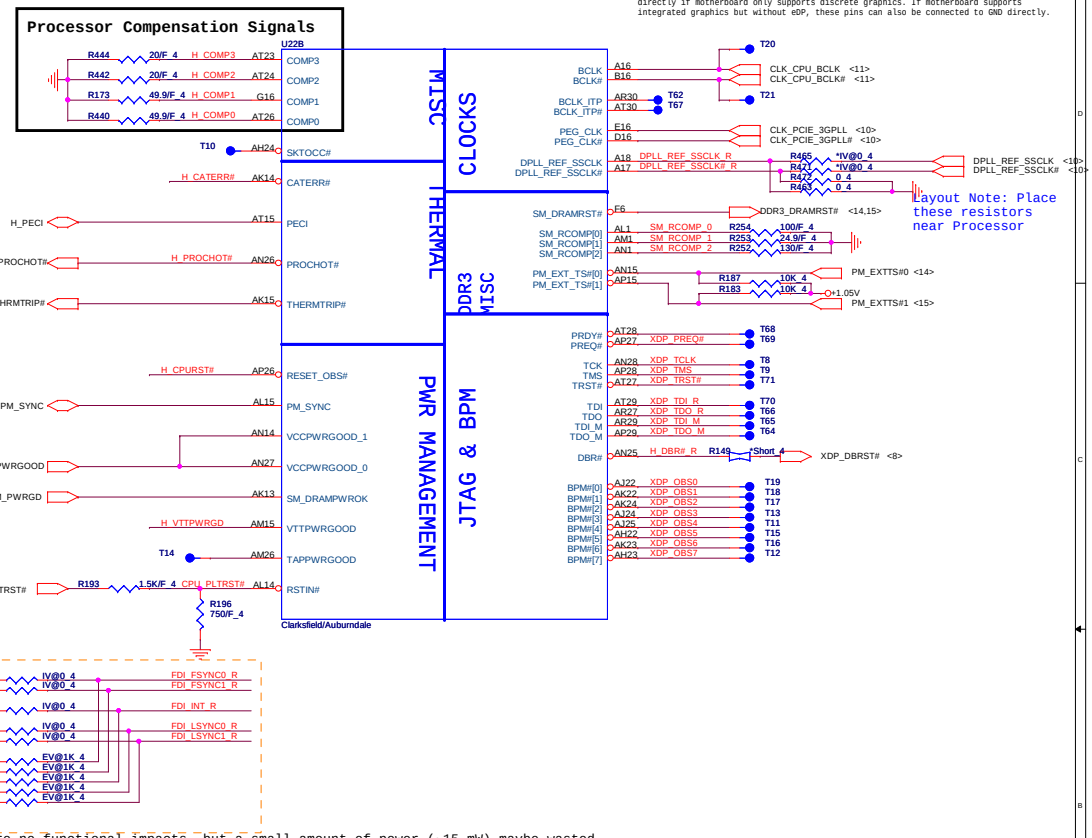
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



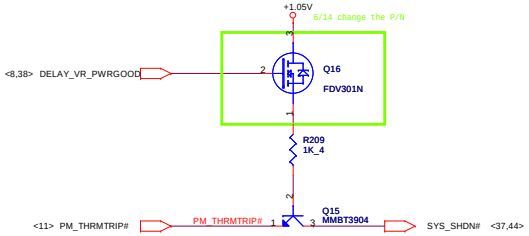
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.

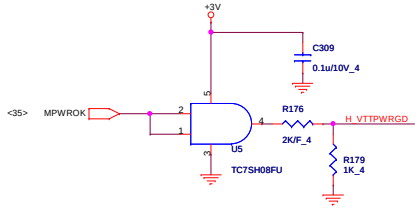


<The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

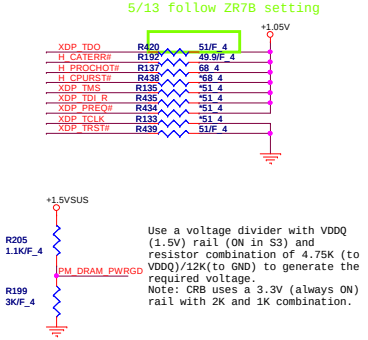
Thermaltrip protect



VTT PWR_Good

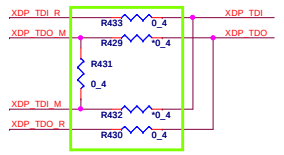


Processor pull-up



JTAG MAPPING

5/13 follow ZR7B setting



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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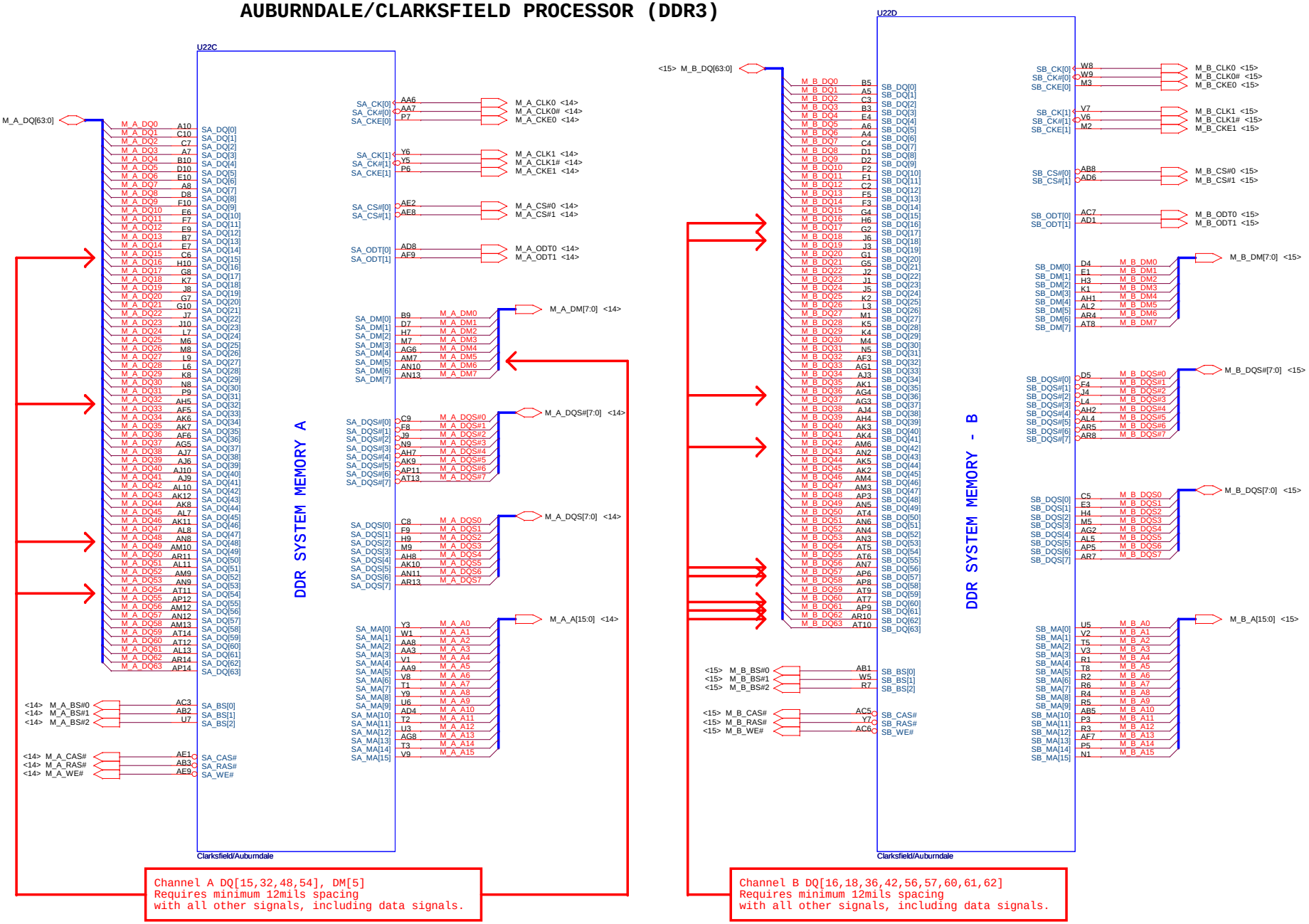
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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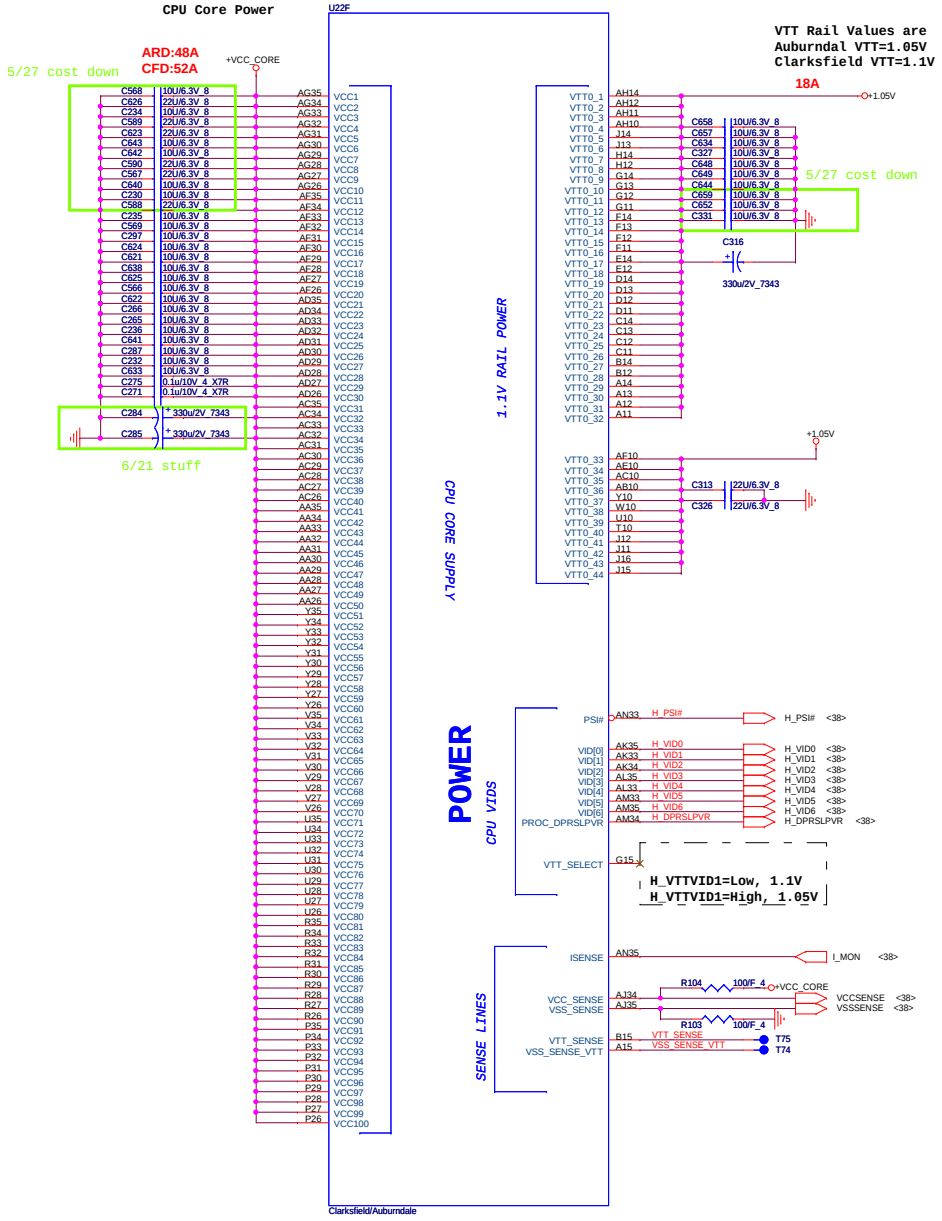
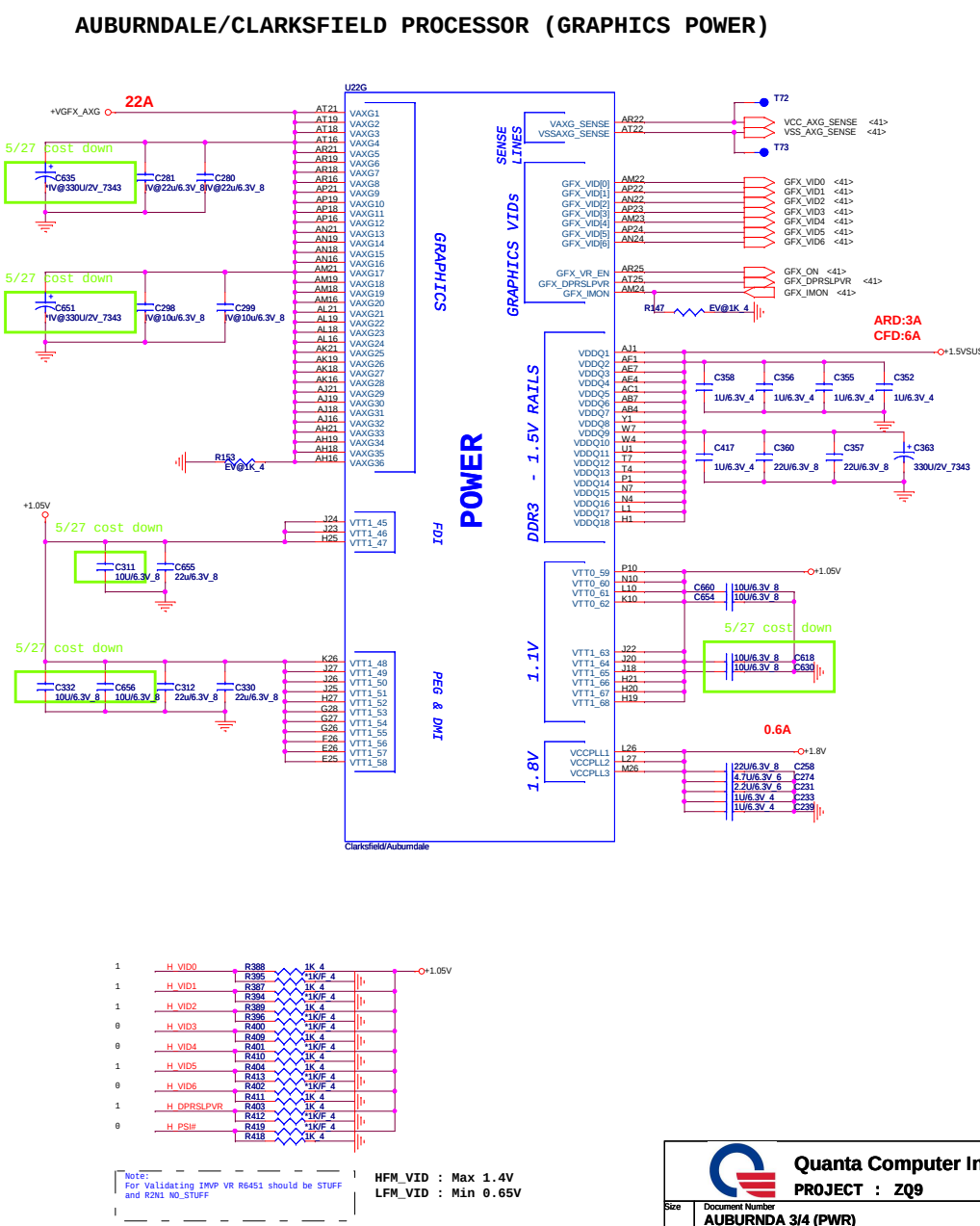


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

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	AUBURNDA 3/4 (PWR)	1A

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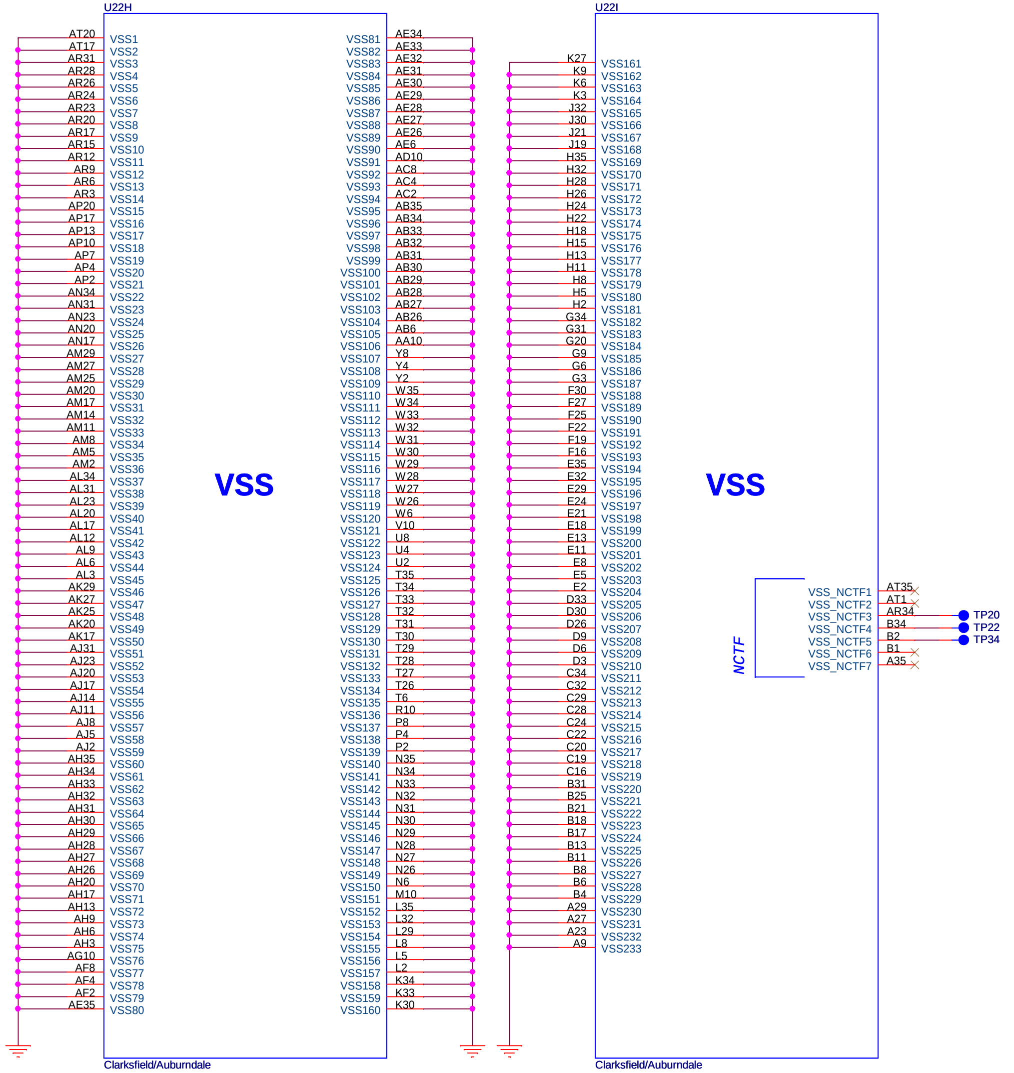
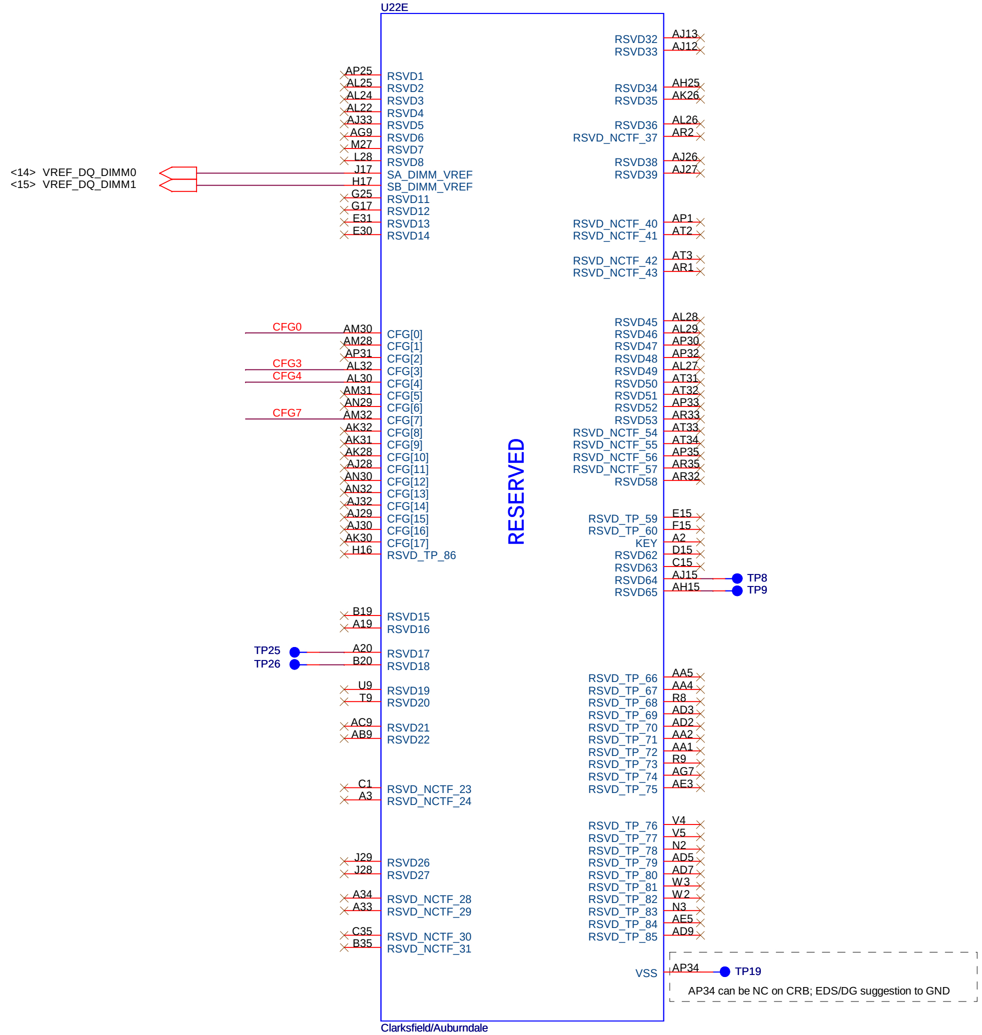
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 3.01K/F_4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 *3.01K
T				CFG7 R126 *3.01K/F_4

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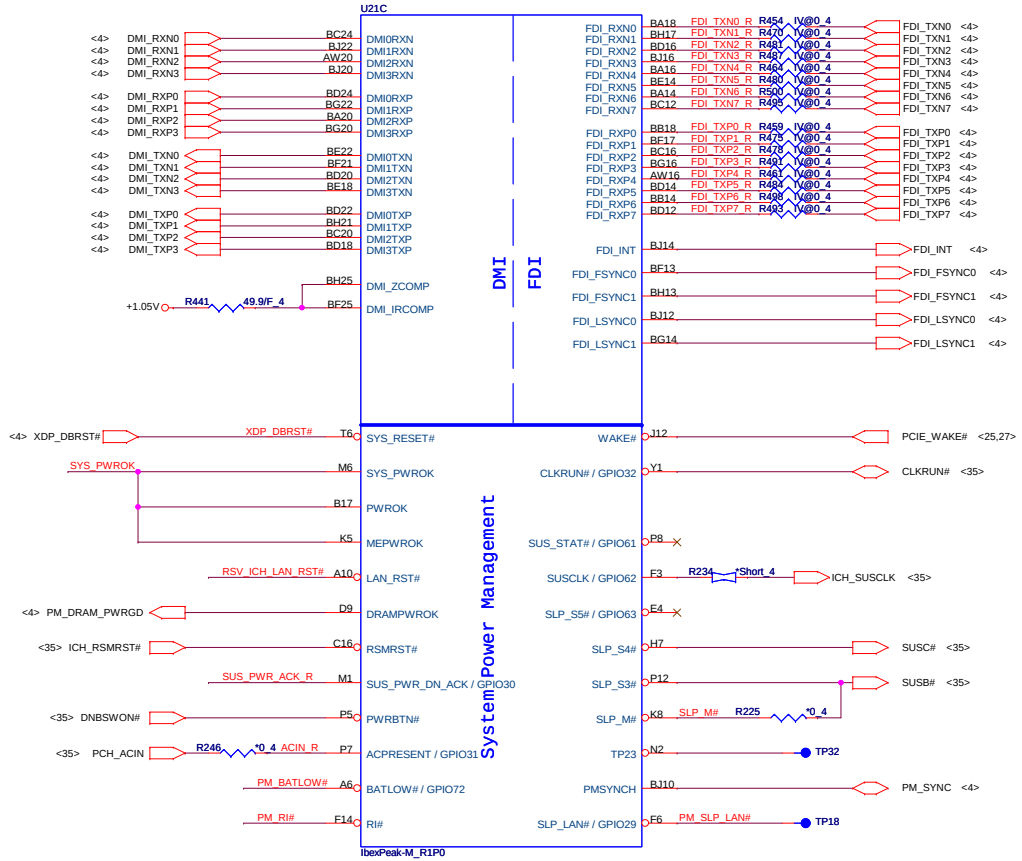
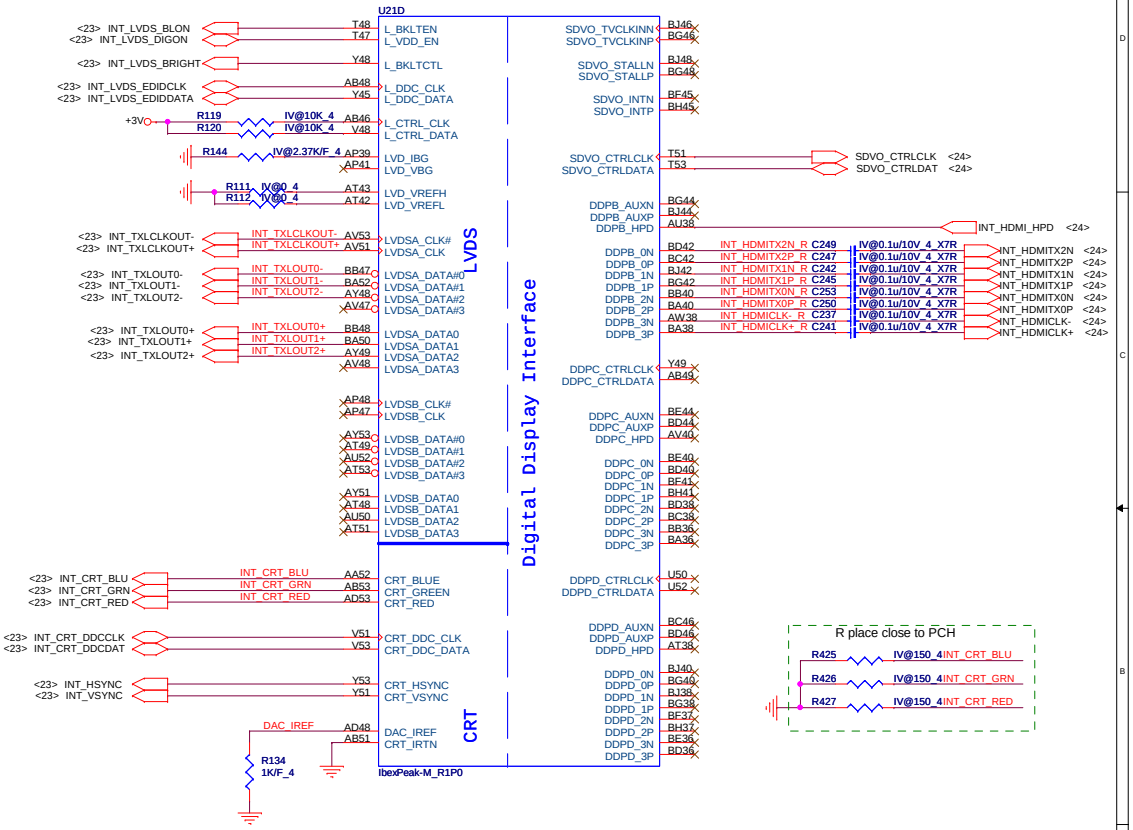
IBEX PEAK-M (DMI,FDI,GPIO)

0-ohm resistor place close to PCH

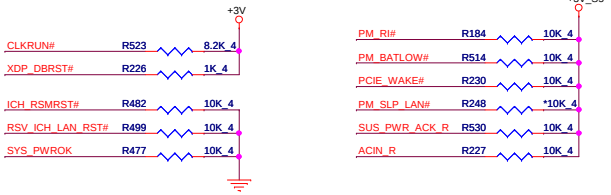


AC-coupling CAP place close to PCH

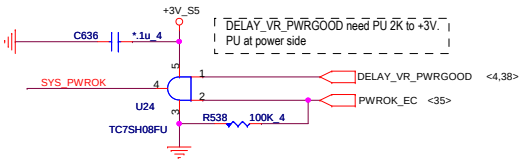
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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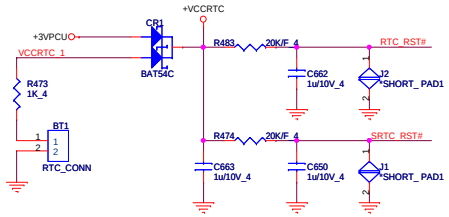
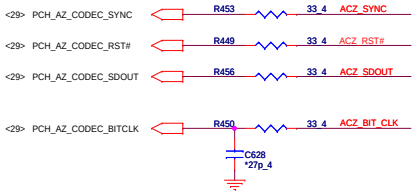
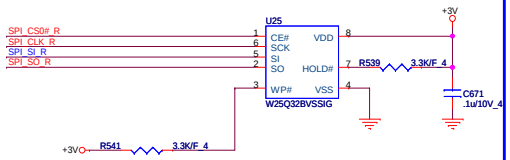
RTC Circuitry

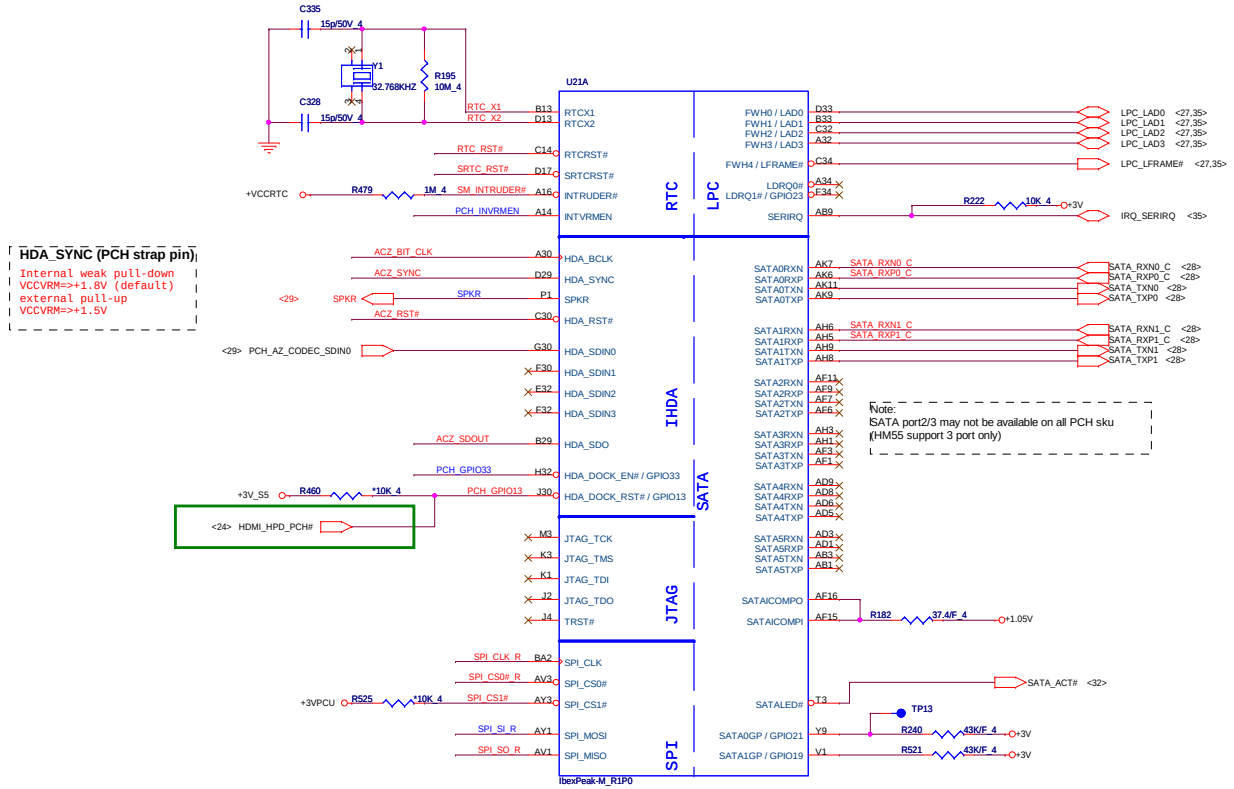


HDA Bus



PCH SPI





HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 *1K/F_4 R145 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K_4 R122 1K_4 R123 *1K_4 R131 *1K_4 +3V <10> PCI_GNT0# <10> PCI_GNT1#
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	<11> RSV_GPIO8 R204 10K_4 +3V_S5 R203 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	<11> CR_WAKE# R244 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 *10K_4

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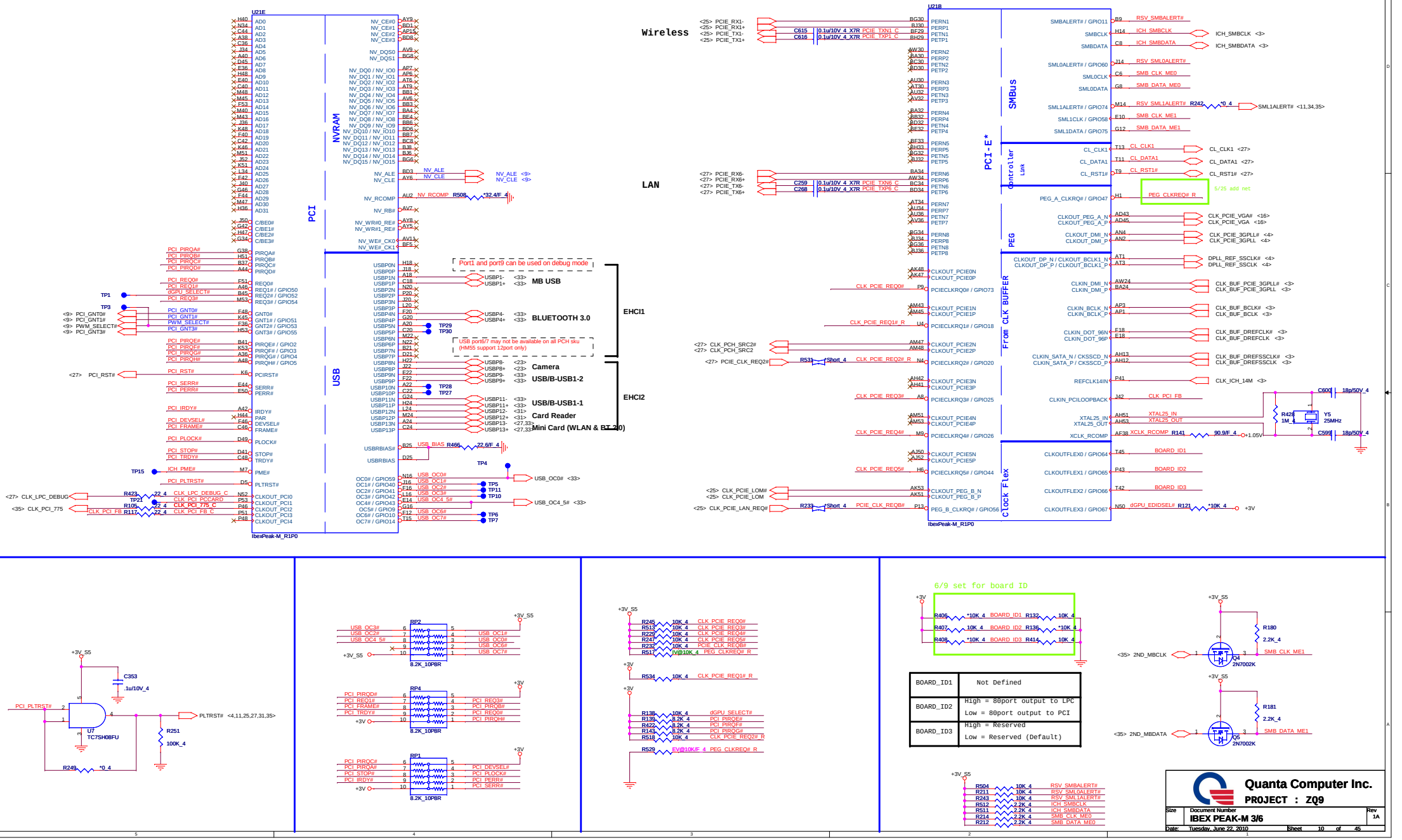
Wireless
LAN
EHCI1
EHCI2
MB USB
BLUETOOTH 3.0
Camera
USB/B-USB1-2
USB/B-USB1-1
Card Reader
Mini Card (WLAN & BT 2.0)
Port1 and port9 can be used on debug mode
USB port6/7 may not be available on all PCH sku (HM55 support 12port only)
PCI
NVRAM
USB
SMBus
PCI-E*
PEG
From CLK BUFFER
Clock Flex
IbexPeak-M_R1P0
6/9 set for board ID
BOARD_ID1 Not Defined
BOARD_ID2 High = 80port output to LPC; Low = 80port output to PCI
BOARD_ID3 High = Reserved; Low = Reserved (Default)
Quanta Computer Inc.
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IBEX PEAK-M 3/6
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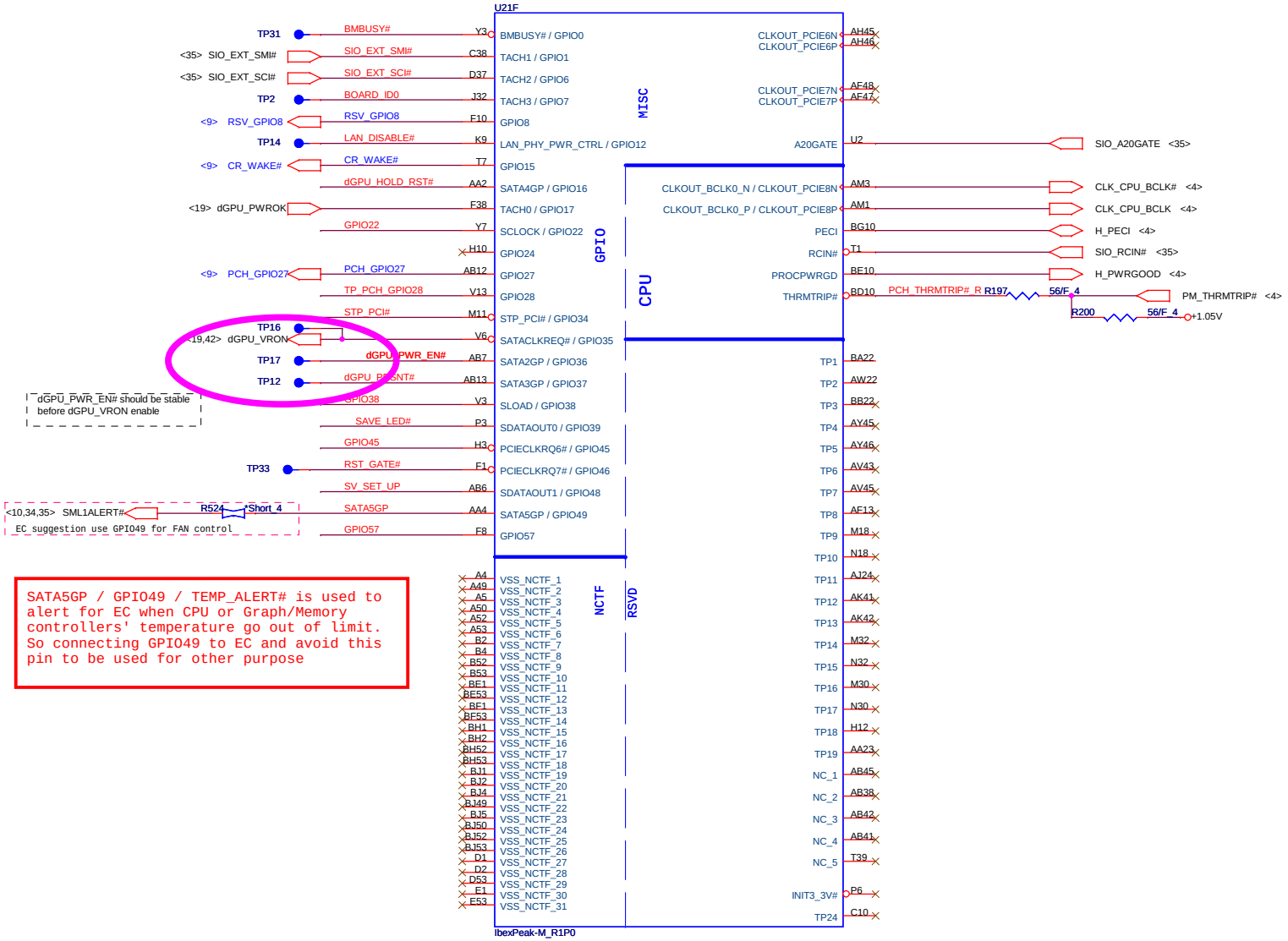
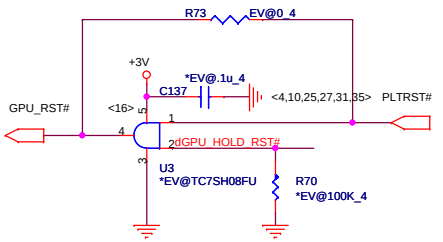
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



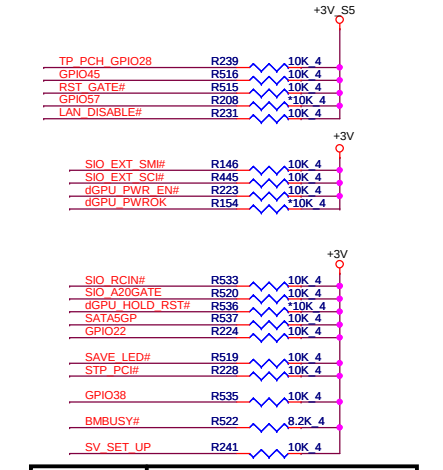
SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#

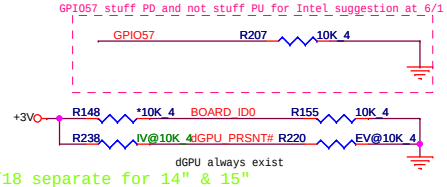
5/18 change for discrete only



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)



5/18 separate for 14" & 15"

BOARD_ID0	High = 15" Low = 14"
RSV_GPIO8	High = Disable Low = Enable

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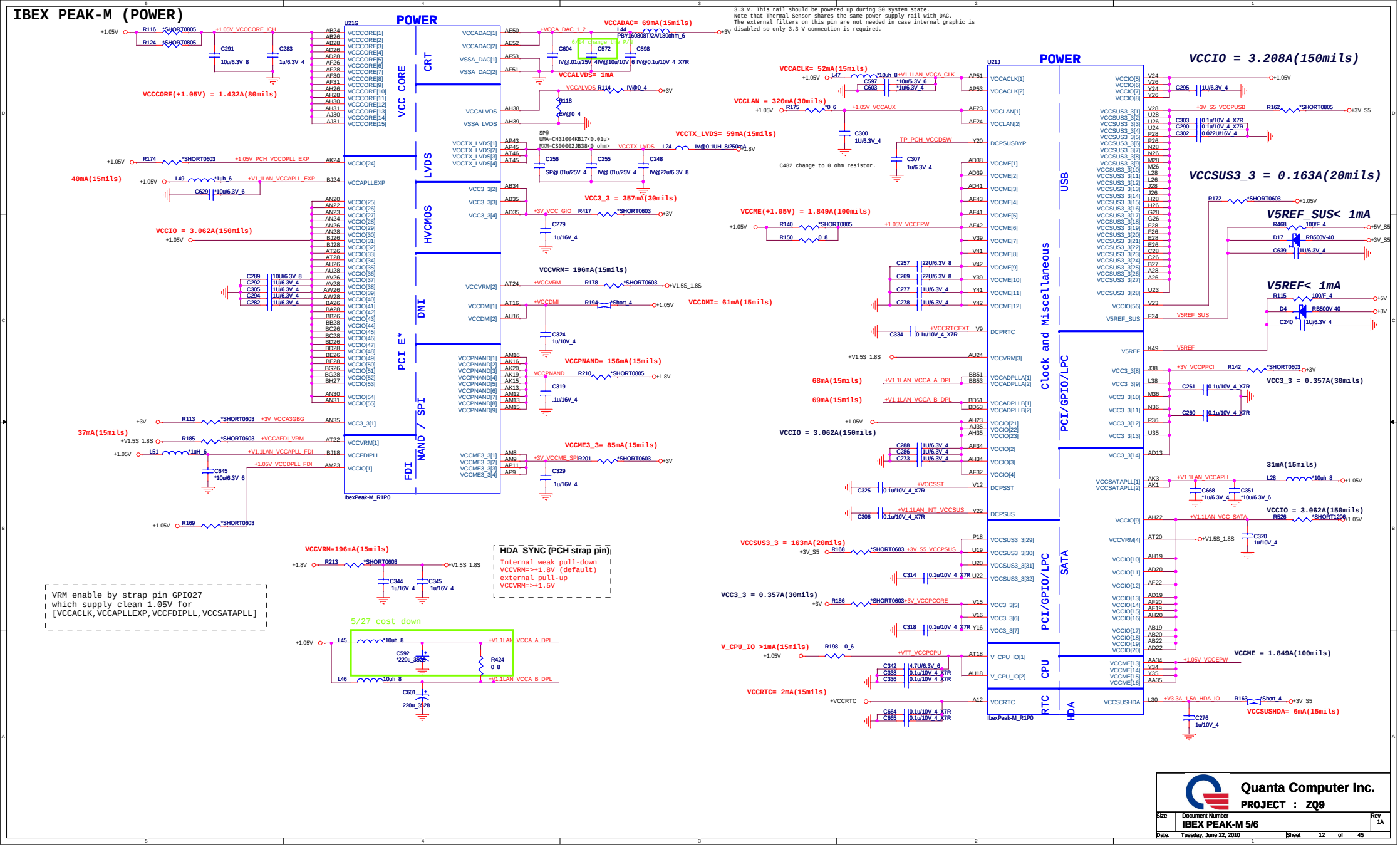
IBEX PEAK-M (POWER)

3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



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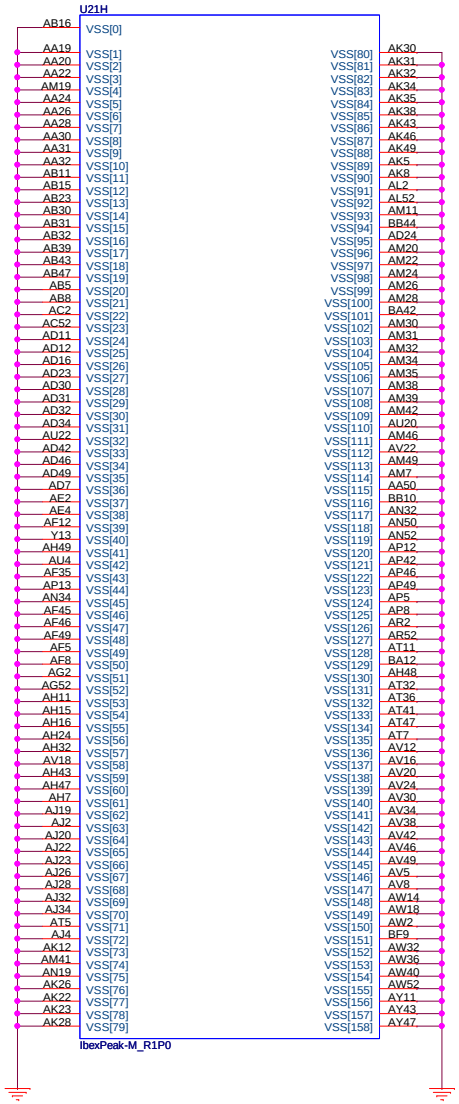
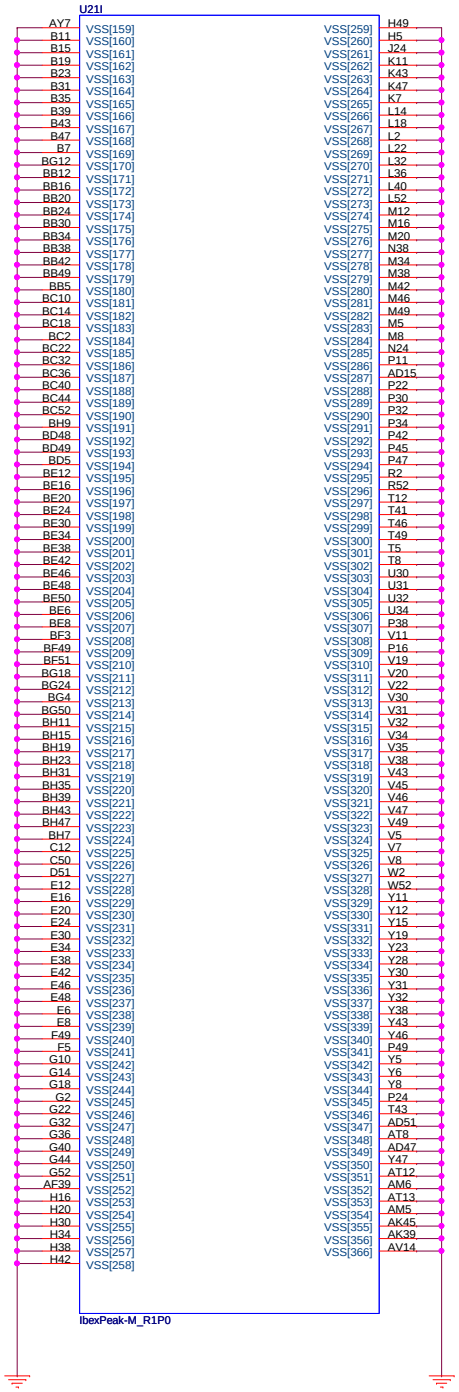
IBEX PEAK-M (GND)





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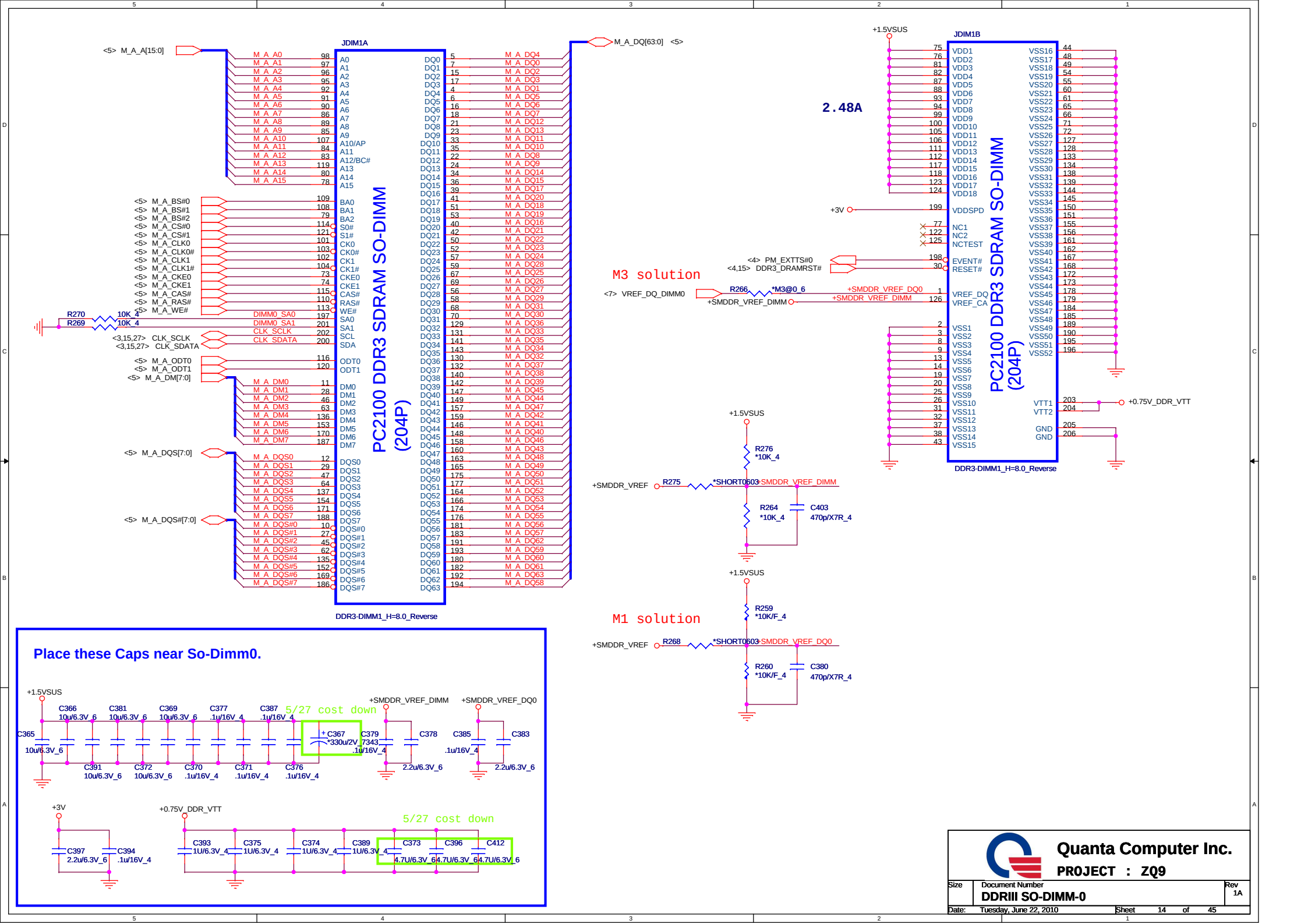
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=8.0_Reverse
<5> M_A_A[15:0]
M_A_DQ[63:0] <5>
<5> M_A_BS#0
<5> M_A_BS#1
<5> M_A_BS#2
<5> M_A_CS#0
<5> M_A_CS#1
<5> M_A_CLK0
<5> M_A_CLK0#
<5> M_A_CLK1
<5> M_A_CLK1#
<5> M_A_CKE0
<5> M_A_CKE1
<5> M_A_RAS#
<5> M_A_CAS#
<5> M_A_WE#
R270 10K_4
R269 10K_4
DIMM0_SA0
DIMM0_SA1
<3,15,27> CLK_SCLK
<3,15,27> CLK_SDATA
CLK_SCLK
CLK_SDATA
<5> M_A_ODT0
<5> M_A_ODT1
<5> M_A_DM[7:0]
<5> M_A_DQS[7:0]
<5> M_A_DQS#[7:0]
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=8.0_Reverse
+1.5VSUS
+3V
2.48A
<4> PM_EXTTS#0
<4,15> DDR3_DRAMRST#
M3 solution
<7> VREF_DQ_DIMM0
R266 *M3@0_6
+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
VREF_DQ
VREF_CA
EVENT#
RESET#
NC1
NC2
NCTEST
VDDSPD
VTT1
VTT2
GND
+0.75V_DDR_VTT
+SMDDR_VREF
R275 *SHORT0603
R276 *10K_4
R264 *10K_4
C403 470p/X7R_4
M1 solution
R268 *SHORT0603
R259 *10K/F_4
R260 *10K/F_4
C380 470p/X7R_4
Place these Caps near So-Dimm0.
5/27 cost down
C366 10u/6.3V_6
C381 10u/6.3V_6
C369 10u/6.3V_6
C377 .1u/16V_4
C387 .1u/16V_4
C365 10u/6.3V_6
C367 *330u/2V_7343
C379 .1u/16V_4
C378 2.2u/6.3V_6
C385 .1u/16V_4
C383 2.2u/6.3V_6
C391 10u/6.3V_6
C372 10u/6.3V_6
C370 .1u/16V_4
C371 .1u/16V_4
C376 .1u/16V_4
C397 2.2u/6.3V_6
C394 .1u/16V_4
C393 1U/6.3V_4
C375 1U/6.3V_4
C374 1U/6.3V_4
C389 1U/6.3V_4
C373 4.7U/6.3V_6
C396 4.7U/6.3V_6
C412 4.7U/6.3V_6
Quanta Computer Inc.
PROJECT : ZQ9
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DDRIII SO-DIMM-0
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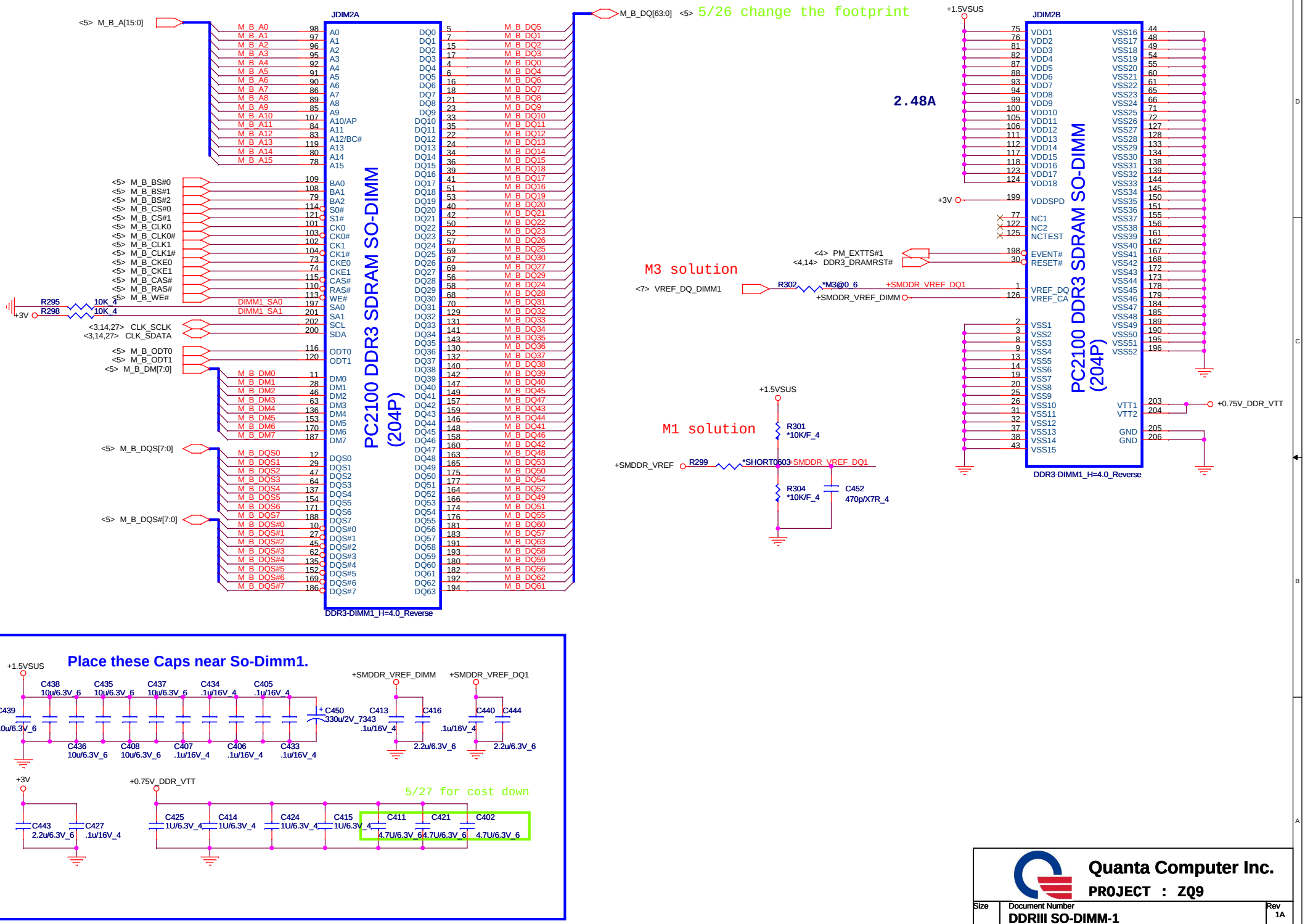
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=4.0_Reverse
<5> M_B_A[15:0]
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_A14
M_B_A15
<5> M_B_BS#0
<5> M_B_BS#1
<5> M_B_BS#2
<5> M_B_CS#0
<5> M_B_CS#1
<5> M_B_CLK0
<5> M_B_CLK0#
<5> M_B_CLK1
<5> M_B_CLK1#
<5> M_B_CKE0
<5> M_B_CKE1
<5> M_B_CAS#
<5> M_B_RAS#
<5> M_B_WE#
R295 10K_4
R298 10K_4
+3V
DIMM1_SA0
DIMM1_SA1
<3,14,27> CLK_SCLK
<3,14,27> CLK_SDATA
<5> M_B_ODT0
<5> M_B_ODT1
<5> M_B_DM[7:0]
<5> M_B_DQS[7:0]
<5> M_B_DQS#[7:0]
M_B_DQ[63:0] <5>
5/26 change the footprint
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=4.0_Reverse
+1.5VSUS
2.48A
+3V
<4> PM_EXTTS#1
<4,14> DDR3_DRAMRST#
M3 solution
<7> VREF_DQ_DIMM1
R302 *M3@0_6
+SMDDR_VREF_DQ1
+SMDDR_VREF_DIMM
M1 solution
R301 *10K/F_4
R304 *10K/F_4
C452 470p/X7R_4
+SMDDR_VREF
R299 *SHORT0603
+0.75V_DDR_VTT
Place these Caps near So-Dimm1.
C438 10u/6.3V_6
C435 10u/6.3V_6
C437 10u/6.3V_6
C434 .1u/16V_4
C405 .1u/16V_4
C439 10u/6.3V_6
C450 330u/2V_7343
C436 10u/6.3V_6
C408 10u/6.3V_6
C407 .1u/16V_4
C406 .1u/16V_4
C433 .1u/16V_4
C413 .1u/16V_4
C416 2.2u/6.3V_6
C440 .1u/16V_4
C444 2.2u/6.3V_6
C443 2.2u/6.3V_6
C427 .1u/16V_4
C425 1U/6.3V_4
C414 1U/6.3V_4
C424 1U/6.3V_4
C415 1U/6.3V_4
C411 4.7U/6.3V_6
C421 4.7U/6.3V_6
C402 4.7U/6.3V_6
5/27 for cost down
Quanta Computer Inc.
PROJECT : ZQ9
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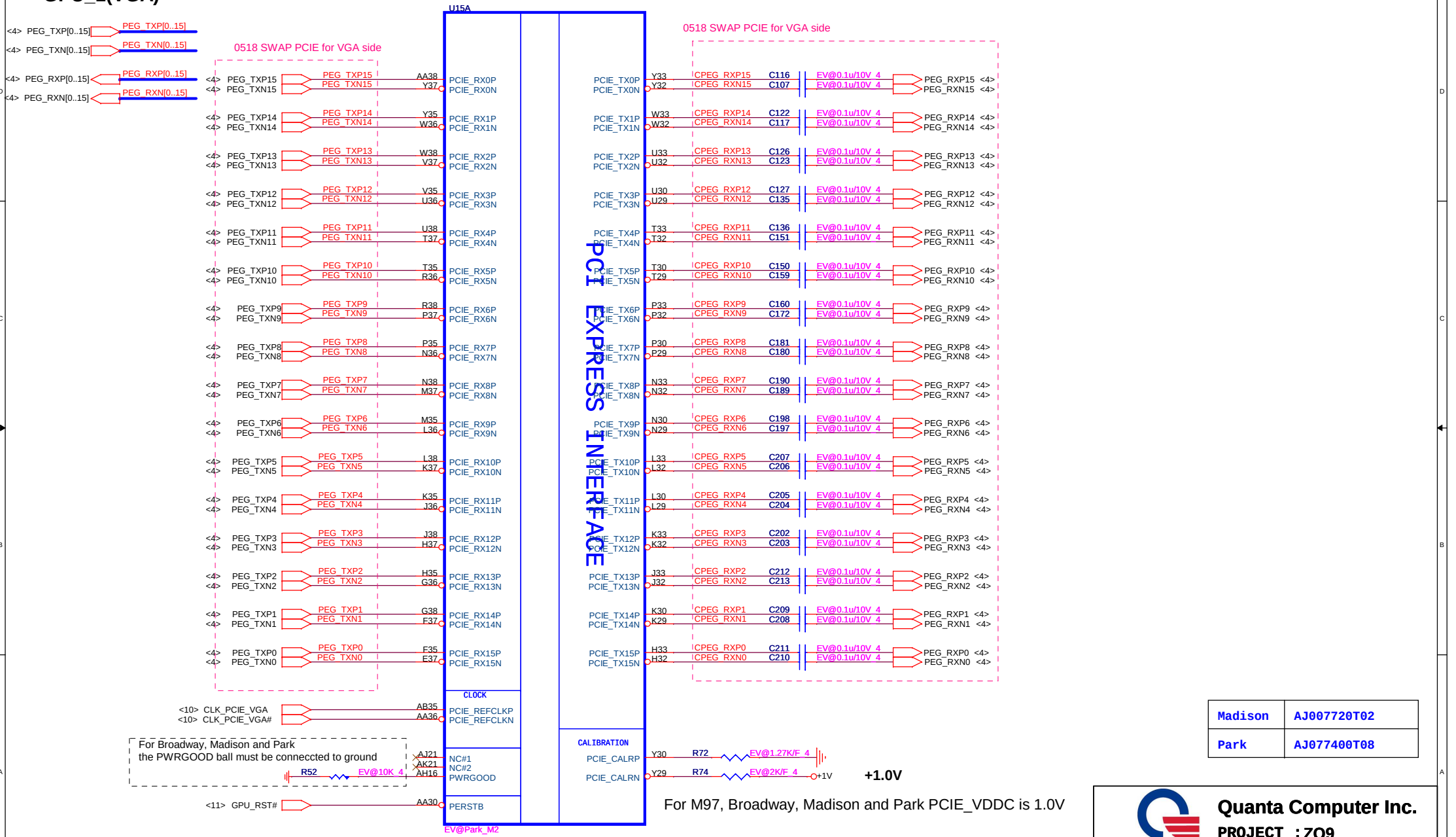
GPU_1(VGA)



Madison	AJ007720T02
Park	AJ077400T08

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	Madison/Park M2-PCIE I/F	1A

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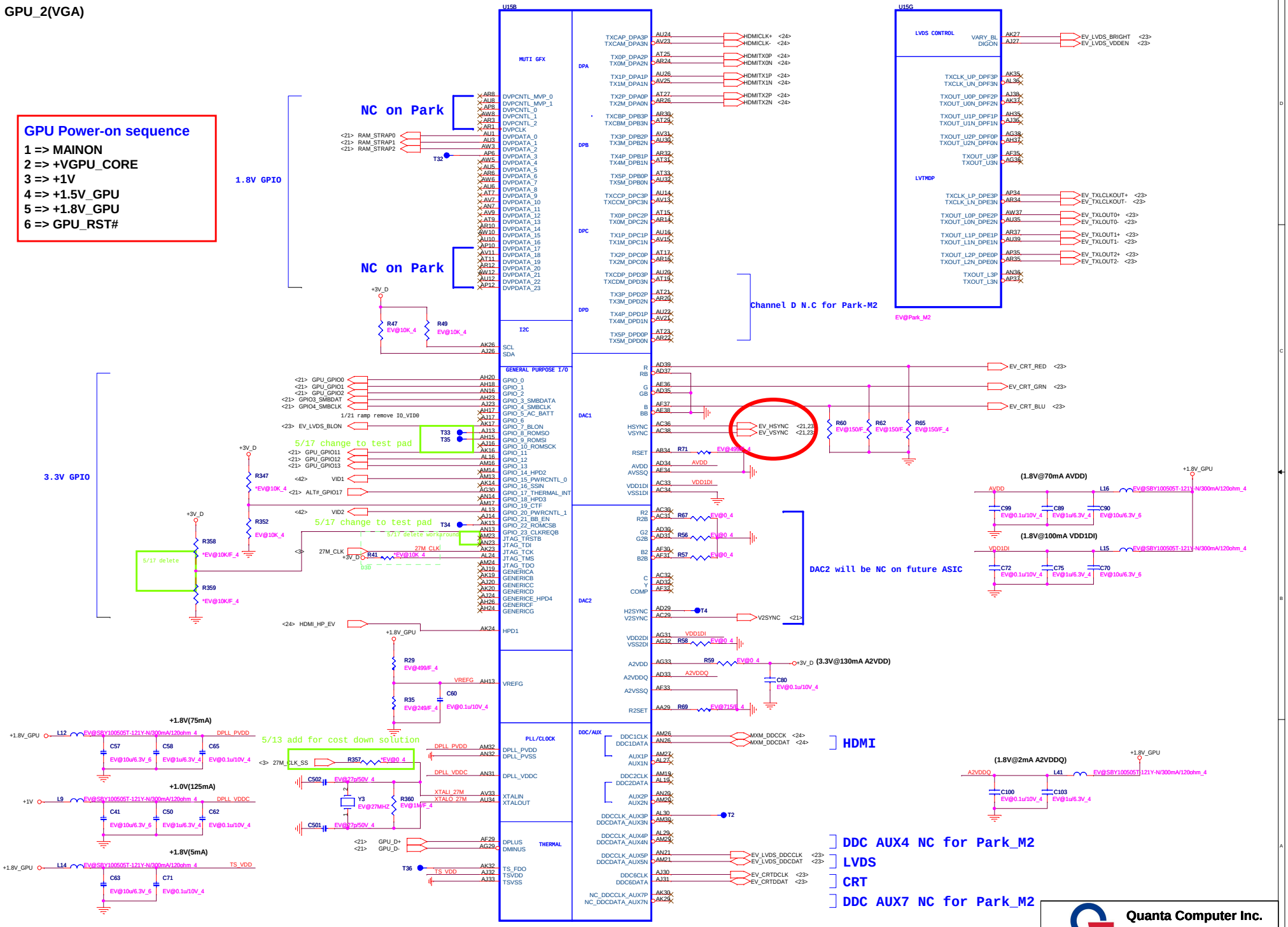
GPU_2(VGA)

GPU Power-on sequence

1 => MAINON
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => GPU_RST#



Quanta Computer Inc.			
PROJECT : ZQ9			
Size	Document Number		Rev
	Madison/Park M2-HOST I/F		1A
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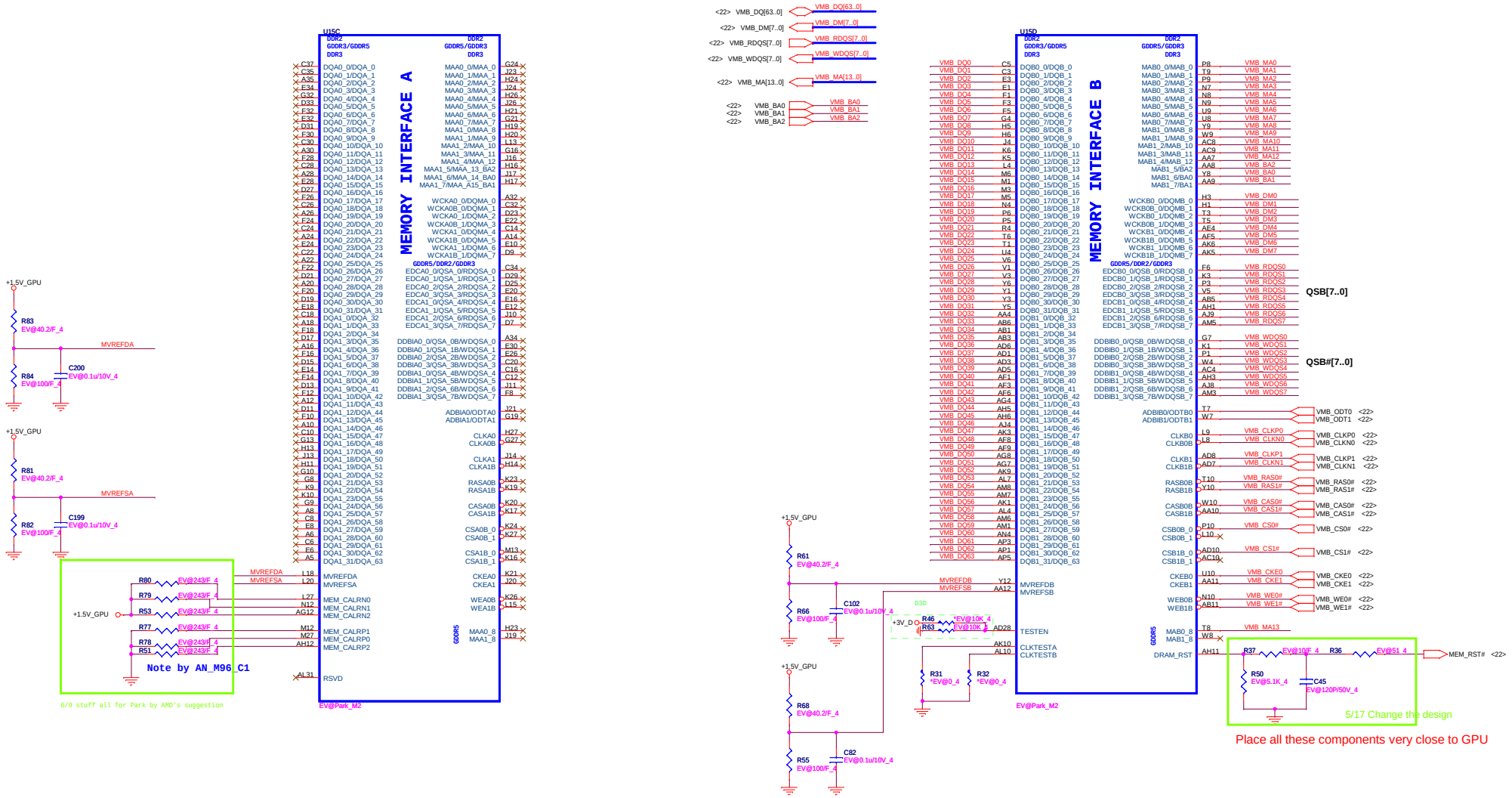
GPU_3(VGA)

Park M2-channel B used(S3 package use Channel A)



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Size	Document Number	Rev
	Madison/Park M2-MEM I/F	1A
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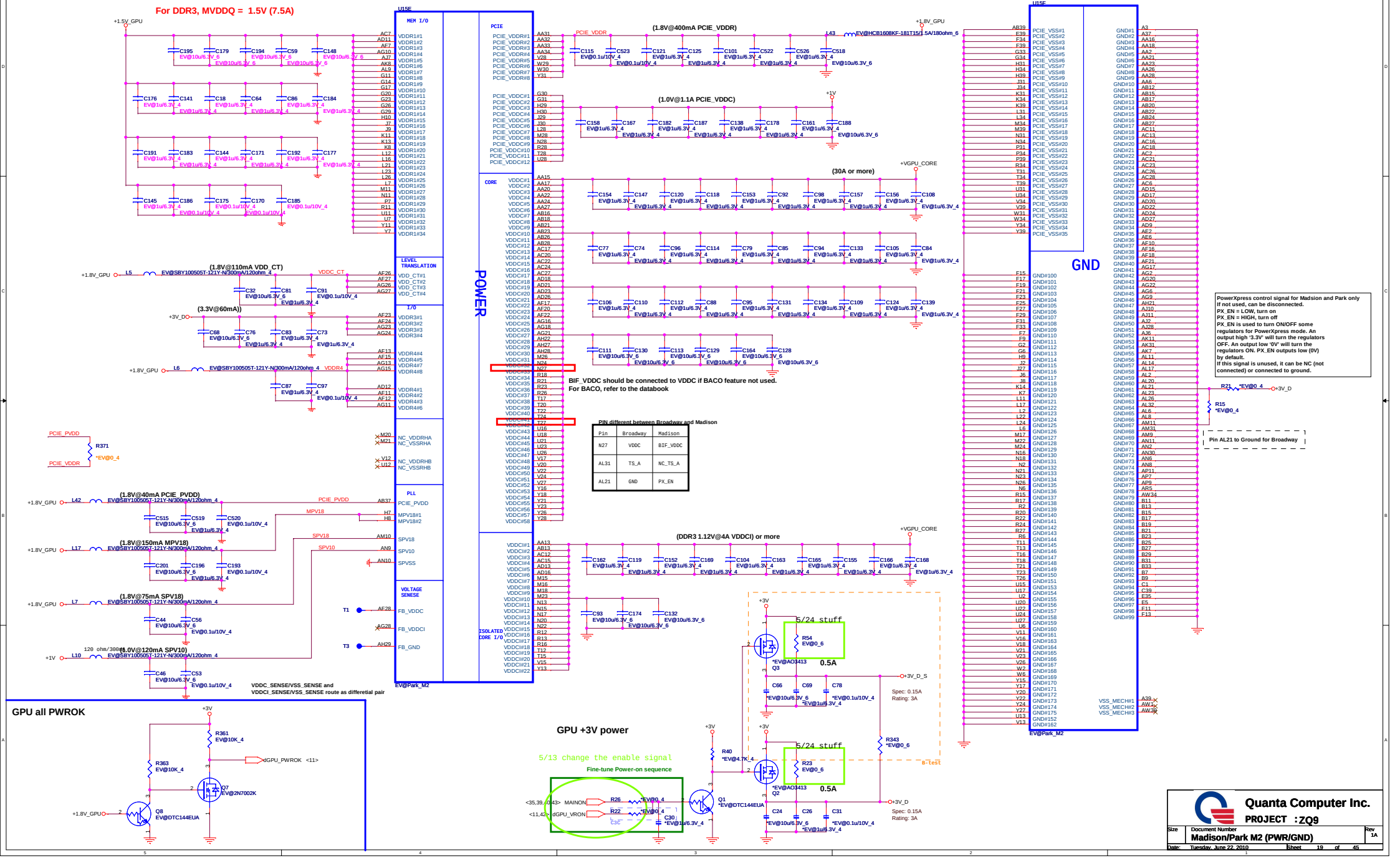
GPU_4(VGA)



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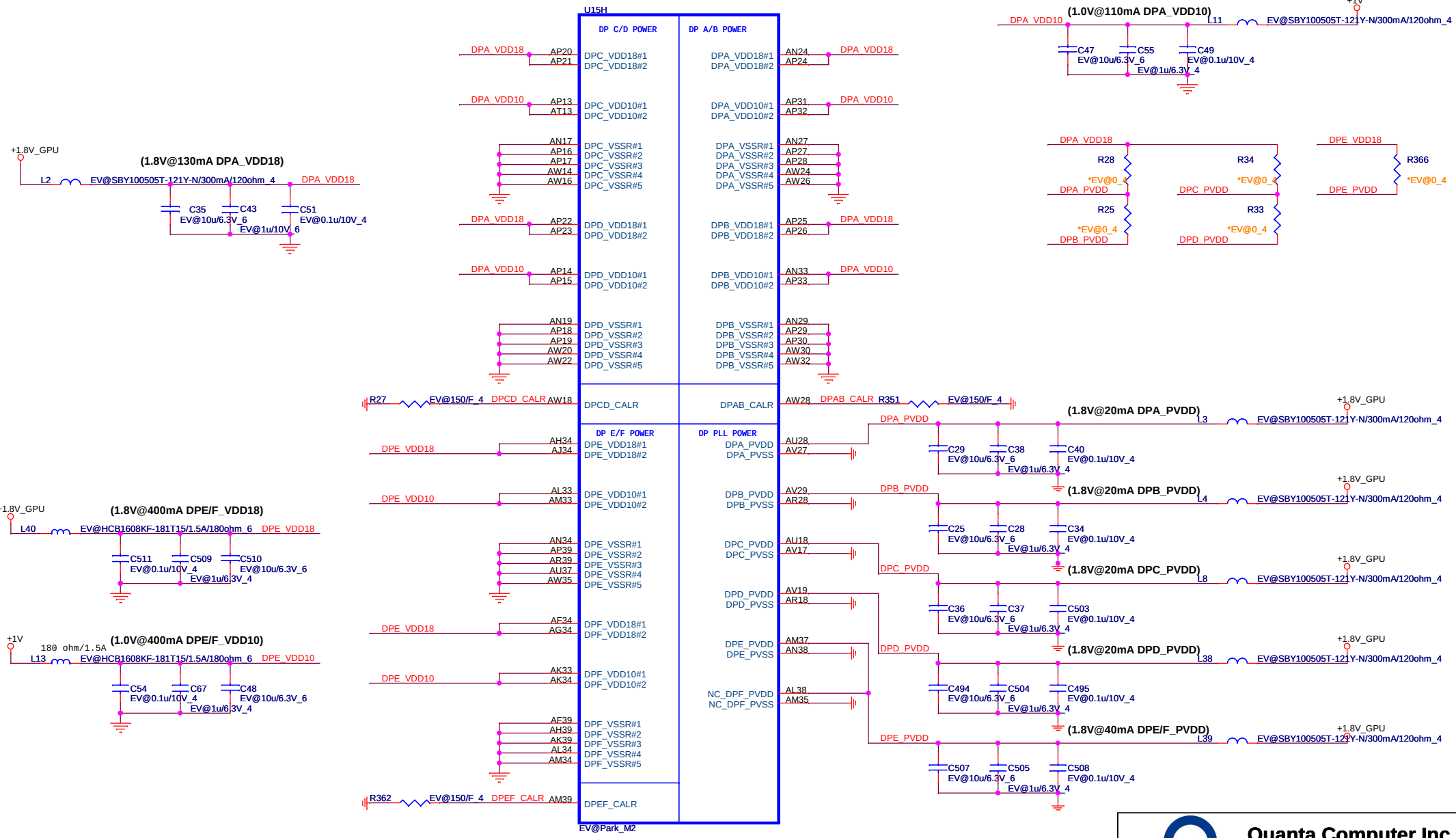
GPU_5(VGA)



Quanta Computer Inc.	
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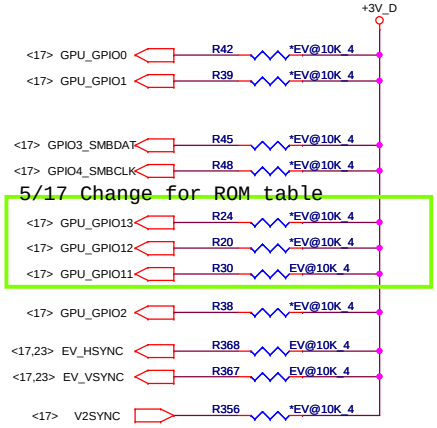
PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

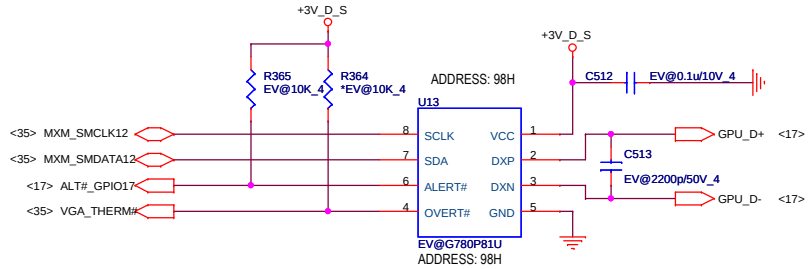
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM(VGA) 5/17 delete EEPROM

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

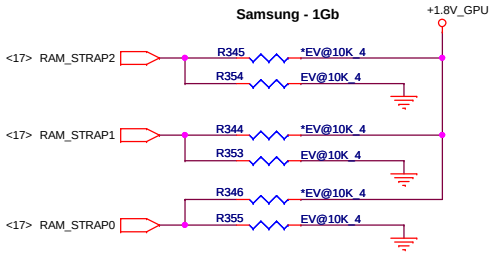
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory size

Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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	Strip/Thermal	1A
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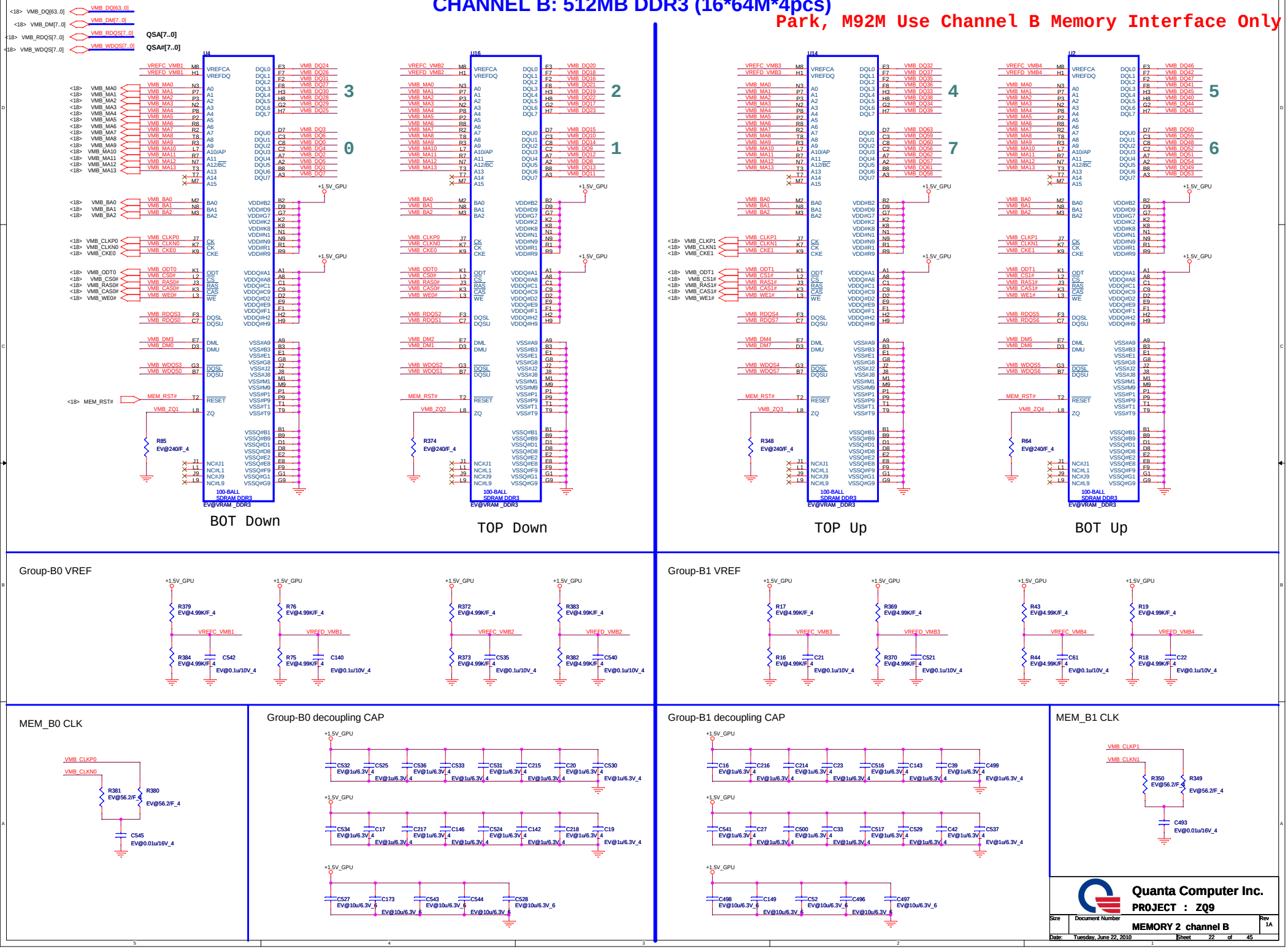
CHANNEL B: 512MB DDR3 (16*64M*4pcs)

Park, M92M Use Channel B Memory Interface Only



Group-B0 VREF

Group-B1 VREF

MEM_B0 CLK

Group-B0 decoupling CAP

Group-B1 decoupling CAP

MEM_B1 CLK

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	MEMORY 2 channel B	1A
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CRT Switch

IV@
EV@

0_ohm Resistor place close to Joint-Point

<8> INT_CRT_RED — INT_CRT_RED — R95 IV@0_4 — VGA_RED
<8> INT_CRT_GRN — INT_CRT_GRN — R94 IV@0_4 — VGA_GRN
<8> INT_CRT_BLU — INT_CRT_BLU — R93 IV@0_4 — VGA_BLU

RN7 IV@0_4P2R
<8> INT_VSYNC — INT_VSYNC — VSYNC
<8> INT_HSYNC — INT_HSYNC — HSYNC

RN8 IV@0_4P2R
<8> INT_CRT_DDCDAT — INT_CRT_DDCDAT — CRTDDATA
<8> INT_CRT_DDCCLK — INT_CRT_DDCCLK — CRTDCLK

<17> EV_CRT_BLU — EV_CRT_BLU — R391 EV@0_4 — VGA_BLU
<17> EV_CRT_GRN — EV_CRT_GRN — R397 EV@0_4 — VGA_GRN
<17> EV_CRT_RED — EV_CRT_RED — R399 EV@0_4 — VGA_RED

RN15 EV@0_4P2R
<17,21> EV_HSYNC — EV_HSYNC — HSYNC
<17,21> EV_VSYNC — EV_VSYNC — VSYNC

RN16 EV@0_4P2R
<17> EV_CRTDCLK — EV_CRTDCLK — CRTDCLK
<17> EV_CRTDDAT — EV_CRTDDAT — CRTDDATA

CRT

+5V — F2 SMD1206P110TFT — D16 SSM22LLPT — CRTVDD5

VGA_RED — L27 BLM18BA750SN1D/0.3A/75ohm_6 — CRT_R1
VGA_GRN — L26 BLM18BA750SN1D/0.3A/75ohm_6 — CRT_G1
VGA_BLU — L25 BLM18BA750SN1D/0.3A/75ohm_6 — CRT_B1

R189 150/F_4 · R177 150/F_4 · R165 150/F_4 · C322 10p/50V_4 · C308 10p/50V_4 · C293 10p/50V_4 · C637 10p/50V_4 · C647 10p/50V_4 · C653 10p/50V_4

C272 0.1u/10V_4_X7R

CN8 CRT-CONN
CRT_R1 — CRT_11 — T22
CRT_G1 — DDCDAT_1
CRT_B1 — CRTHSYNC
CRTVSYNC
DDCCLK_1

6/21 change to 0 ohm

+3V — C301 0.1u/10V_4_X7R — C632 22u/25V_6 — C315 0.1u/10V_4_X7R

U23 CM2009-02QR
CRTVDD5 — VCC_SYNC — SYNC_OUT2 — CRT_VSYNC2 — R458 0_4 — CRTVSYNC
SYNC_OUT1 — CRT_HSYNC2 — R457 0_4 — CRTHSYNC
VCC_DDC — CRT_BYP
BYP
SYNC_IN2 — VSYNC
VCC_VIDEO — SYNC_IN1 — HSYNC
VIDEO_1 — CRT_R1
VIDEO_2 — CRT_G1
VIDEO_3 — CRT_B1
DDC_IN1 — CRTDDCLK — R462 2.7K_4
DDC_IN2 — CRTDDATA — R469 2.7K_4
GND
DDC_OUT1 — DDCCLK_1
DDC_OUT2 — DDCDAT_1

+3V — R452 2.7K_4 — R476 2.7K_4 — CRTVDD5

C661 *1u/10V_4 — CRTVDD5
C620 *10p/50V_4 — CRTVSYNC
C619 *10p/50V_4 — CRTHSYNC
C631 10p/50V_4 — DDCCLK_1
C646 10p/50V_4 — DDCDAT_1

LVDS

0_ohm Resistor place close to Joint-Point

RN1 EV@0_4P2R
<17> EV_LVDS_DDCCLK — EV_LVDS_DDCCLK — LCD_EDIDCLK
<17> EV_LVDS_DDCDAT — EV_LVDS_DDCDAT — LCD_EDIDDATA

RN14 EV@0_4P2R
<17> EV_LVDS_VDDEN — EV_LVDS_VDDEN — LVDS_VDDEN
<17> EV_LVDS_BLON — EV_LVDS_BLON — LVDS_BLON

RN9 IV@0_4P2R
<8> INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK — LCD_EDIDCLK
<8> INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA — LCD_EDIDDATA

RN6 IV@0_4P2R
<8> INT_LVDS_DIGON — INT_LVDS_DIGON — LVDS_VDDEN
<8> INT_LVDS_BLON — INT_LVDS_BLON — LVDS_BLON

RN5 EV@0_4P2R
<17> EV_TXLCLKOUT- — EV_TXLCLKOUT- — TXLCLKOUT-
<17> EV_TXLCLKOUT+ — EV_TXLCLKOUT+ — TXLCLKOUT+
<17> EV_TXLOUT0- — EV_TXLOUT0- — TXLOUT0-
RN2 EV@0_4P2R
<17> EV_TXLOUT0+ — EV_TXLOUT0+ — TXLOUT0+
<17> EV_TXLOUT1- — EV_TXLOUT1- — TXLOUT1-
RN3 EV@0_4P2R
<17> EV_TXLOUT1+ — EV_TXLOUT1+ — TXLOUT1+
<17> EV_TXLOUT2- — EV_TXLOUT2- — TXLOUT2-
RN4 EV@0_4P2R
<17> EV_TXLOUT2+ — EV_TXLOUT2+ — TXLOUT2+

RN10 IV@0_4P2R
<8> INT_TXLCLKOUT+ — INT_TXLCLKOUT+ — TXLCLKOUT+
<8> INT_TXLCLKOUT- — INT_TXLCLKOUT- — TXLCLKOUT-
RN13 IV@0_4P2R
<8> INT_TXLOUT0+ — INT_TXLOUT0+ — TXLOUT0+
<8> INT_TXLOUT0- — INT_TXLOUT0- — TXLOUT0-
RN12 IV@0_4P2R
<8> INT_TXLOUT1+ — INT_TXLOUT1+ — TXLOUT1+
<8> INT_TXLOUT1- — INT_TXLOUT1- — TXLOUT1-
RN11 IV@0_4P2R
<8> INT_TXLOUT2+ — INT_TXLOUT2+ — TXLOUT2+
<8> INT_TXLOUT2- — INT_TXLOUT2- — TXLOUT2-

<35> CONTRAST — R7 EV@0_4
<17> EV_LVDS_BRIGHT — R12 *0_4 — LVDS_BRIGHT
<8> INT_LVDS_BRIGHT — R13 IV@0_4

LVDS

+3V — C8 0.1u/10V_4_X7R — C7 1000p/50V_4
VIN — C2 4.7u/25V_8 — C3 1000p/50V_4

5/7 add
C11 *1u/6.3V_4 — C14 *1u/6.3V_4 — R11 0_6 — LCDVCC

VIN — R8 0.8A — R14 *SHORT0805 — INVCC0

CN5
+3V — R9 2.2K_4 — LCD_EDIDCLK
R10 2.2K_4 — LCD_EDIDDATA
TXLOUT0- — TXLOUT0+
TXLOUT1- — TXLOUT1+
TXLOUT2- — TXLOUT2+
TXLCLKOUT- — TXLCLKOUT+
USBP8- — USBP8+

5/7 add
C12 *1u/6.3V_4 — C13 *1u/6.3V_4 — R5 0_6 — +3V

CCD-USB
CCD_PWR
LVDS_BRIGHT — R6 BLM15AG121SS1/0.5A/120ohm_4 — BL_ON
LVDS

CCD +3V-current budget 0.2A

5/21 Change the LVDS connector and swap

<10> USBP8+ — R2 *0_4 — L1 — USBP8+_R
<10> USBP8- — USBP8-_R
RFCMF1632100M3T/200mA/90ohm
R3 *0_4

+3VPCU — C491 0.1u/10V_4_X7R — HE1 PT3661-BB — LID591# — D13 *VPORT_6

PT3661-BB : AL003661003
EM-6781-T3 : AL006781000

Lid Switch (Hall sensor)

LCD Power

+3V — C1 1U/6.3V_4 — U1 AAT4280-4
IN — OUT — LCDVCC
IN — GND
LVDS_VDDEN — ON/OFF — GND
C6 *.1u/10V_4 · C5 *2.2u/10V_8 · C9 0.1u/10V_4_X7R · C10 *1u/25V_4 · C4 22u/6.3V_8
R4 100K_4

Backlight Control

+3VPCU — R375 *100K_4 — LID591# <35>

LID591#,EC intrnal PU

+3V — D14 BAS316 — R376 10K_4 — BL_ON
R377 10K_4
BL# — Q10 2N7002K — Q9 DTC144EUA — EC_FPBACK# <35>
LVDS_BLON — Q11 2N7002K — R378 100K_4

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Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
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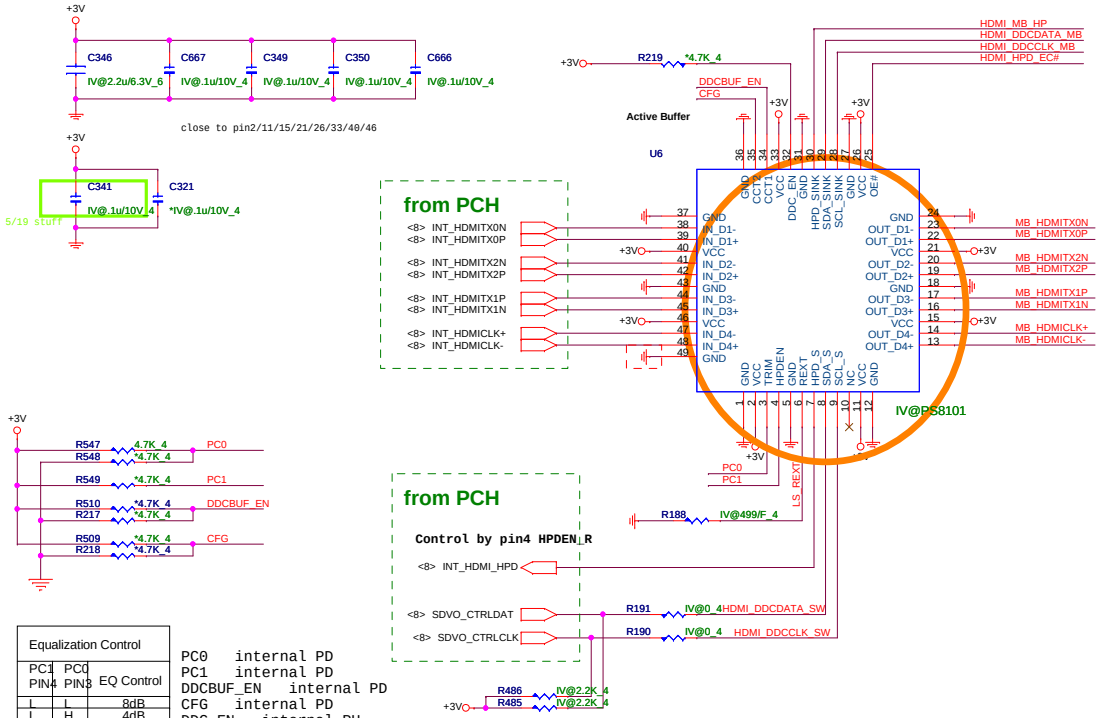
I@ HDMI LEVEL SHIFTER

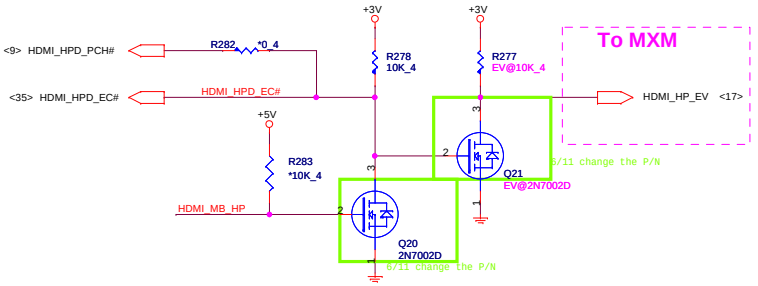
IV@
EV@



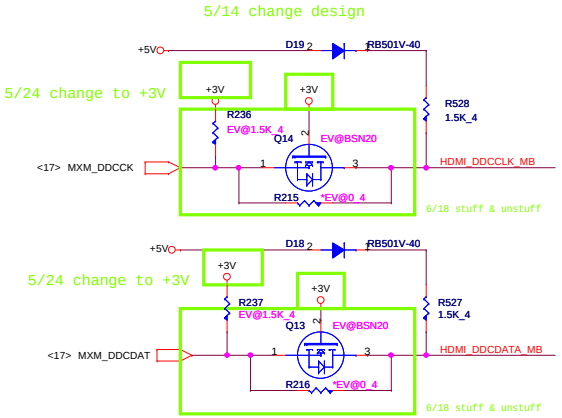
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

SW@HDMI-detect



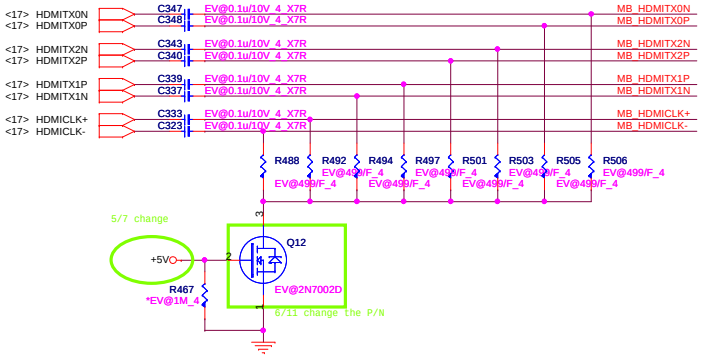
I2C



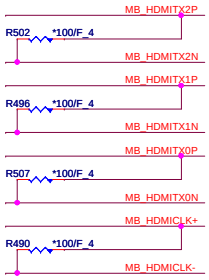
AC-coupling CAP place close to HDMI-connector

Switchable Graphic HDMI source

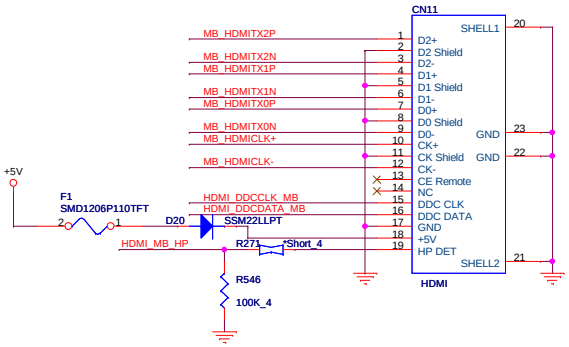
From GPU



EMI

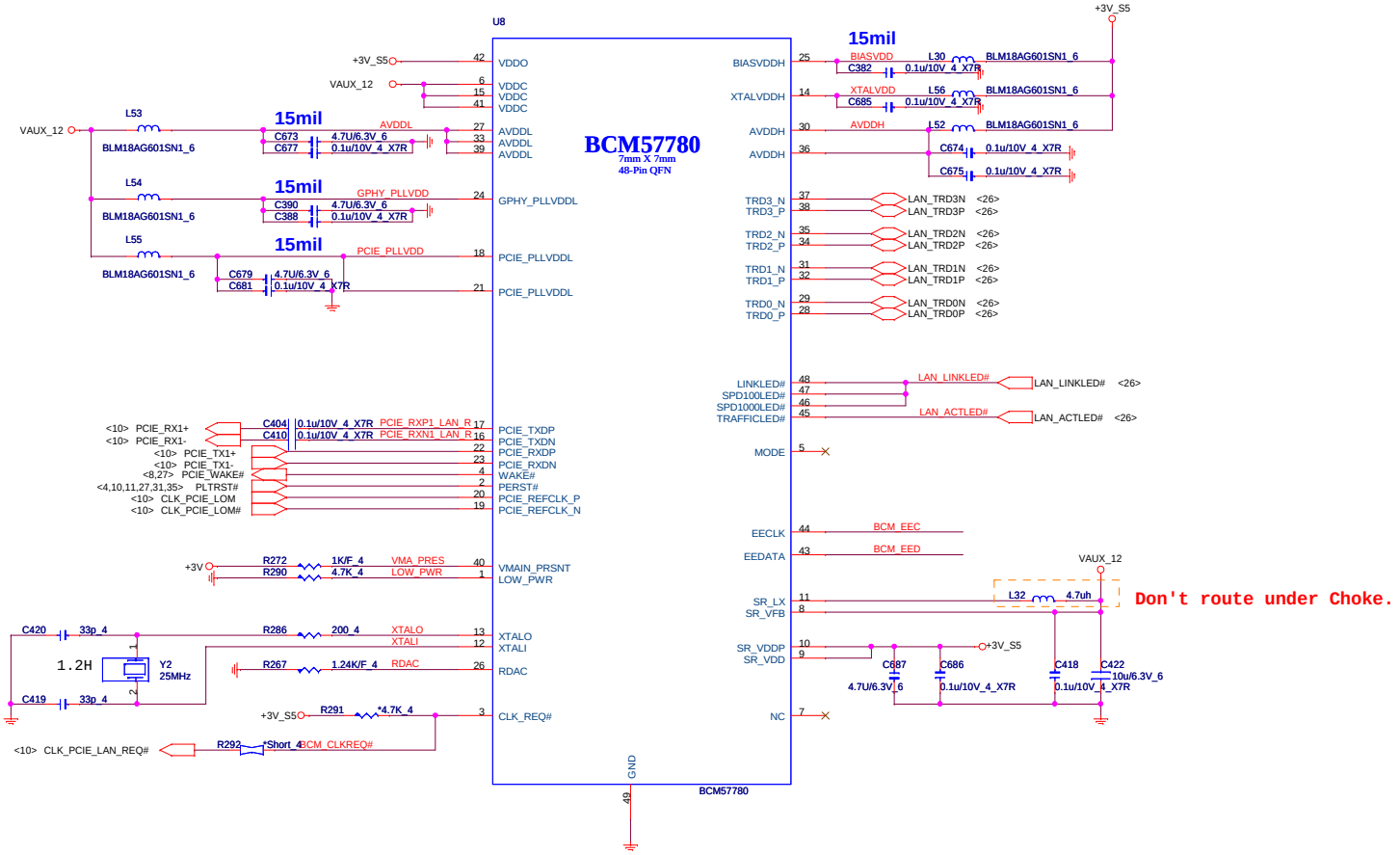


HDMI connector

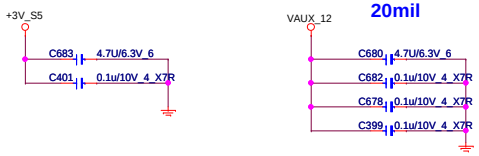


Quanta Computer Inc.
PROJECT : ZQ9
Size | Document Number | Rev
HDMI (PS8101) | 1A
Date: Tuesday, June 22, 2010 | Sheet 24 of 45

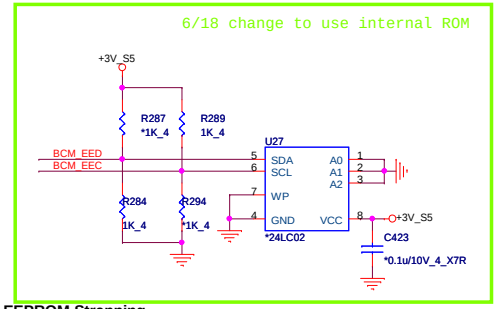
Giga-LAN BCM57780



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

A version Still mount the EEPROM

Quanta Computer Inc.			
PROJECT : ZQ9			
Size	Document Number		Rev
	GLAN BCM57780		1A
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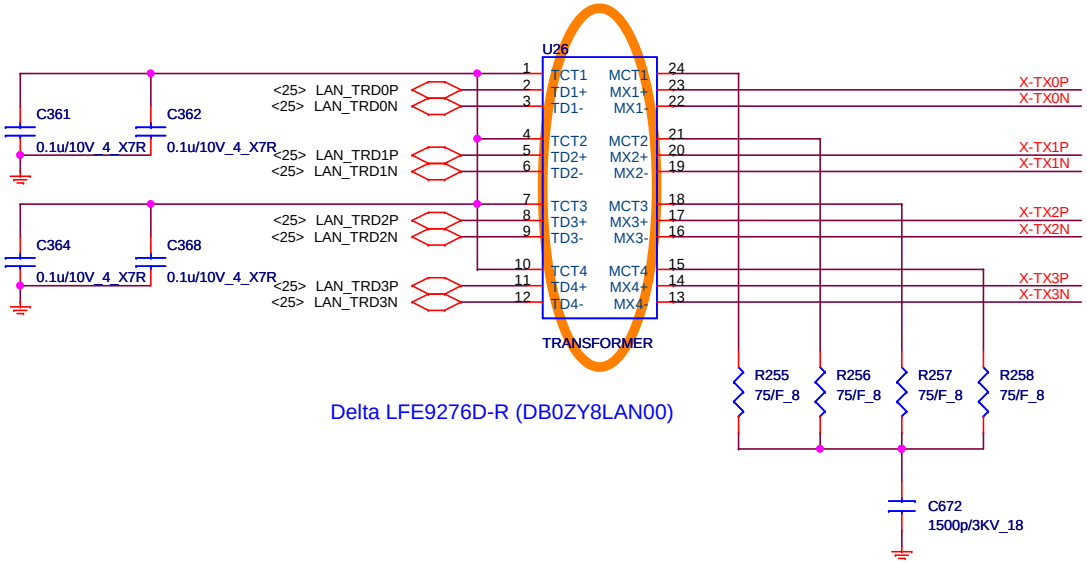
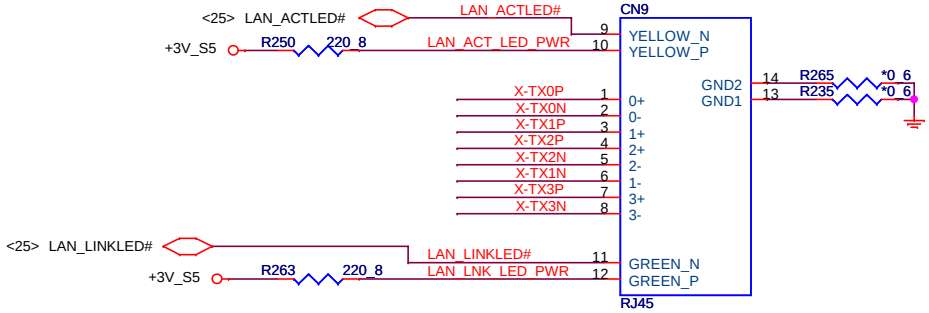
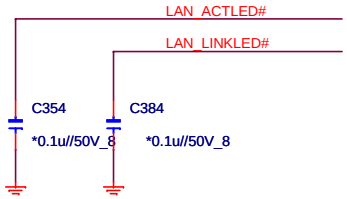
TRANSFORMER



Delta LFE9276D-R (DB0ZY8LAN00)





Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number: LAN Transformer and RJ45	Rev: 1A
Date: Tuesday, June 22, 2010	Sheet 26 of 45	

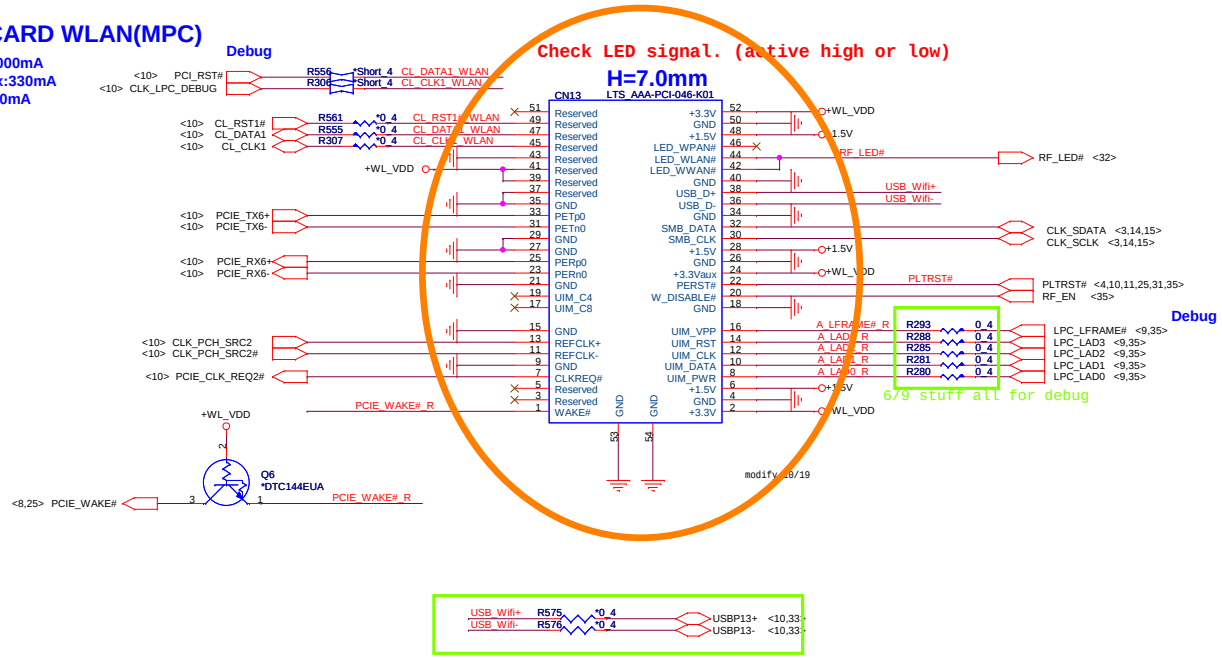
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Debug

Check LED signal. (active high or low)

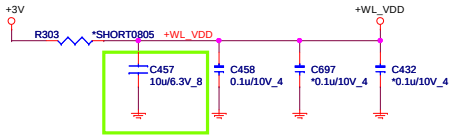
H=7.0mm



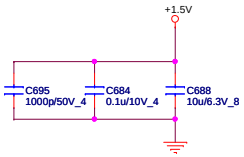
Debug

R293	0_4	LPC_LFRAME# <9,35>
R288	0_4	LPC_LAD3 <9,35>
R285	0_4	LPC_LAD2 <9,35>
R281	0_4	LPC_LAD1 <9,35>
R280	0_4	LPC_LAD0 <9,35>

6/9 stuff all for debug

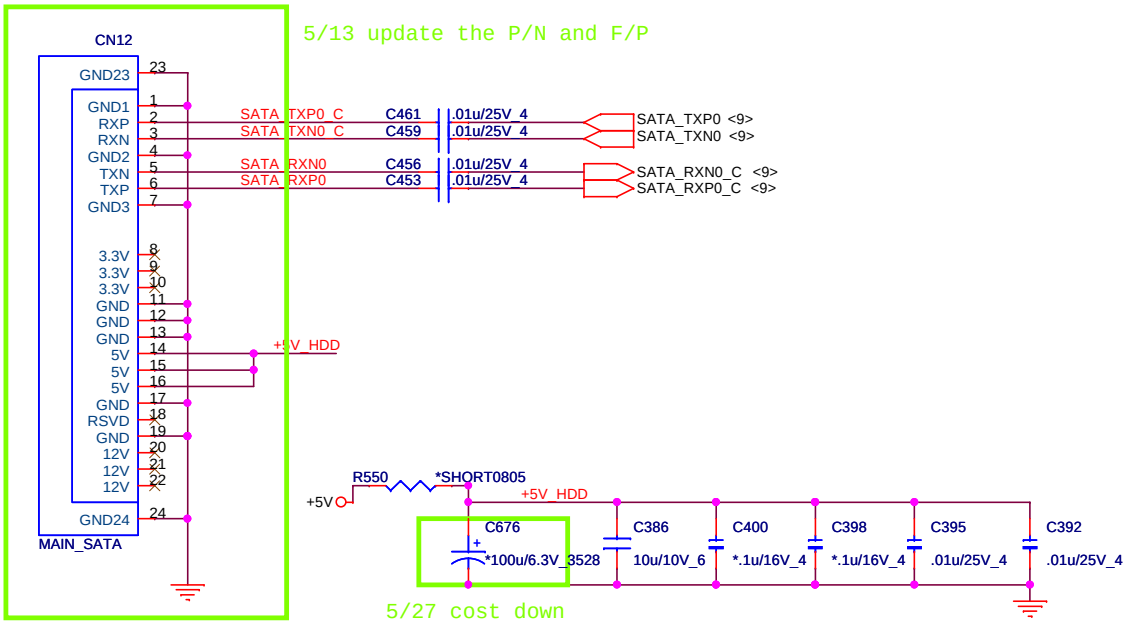


5/13 change to 6.3V

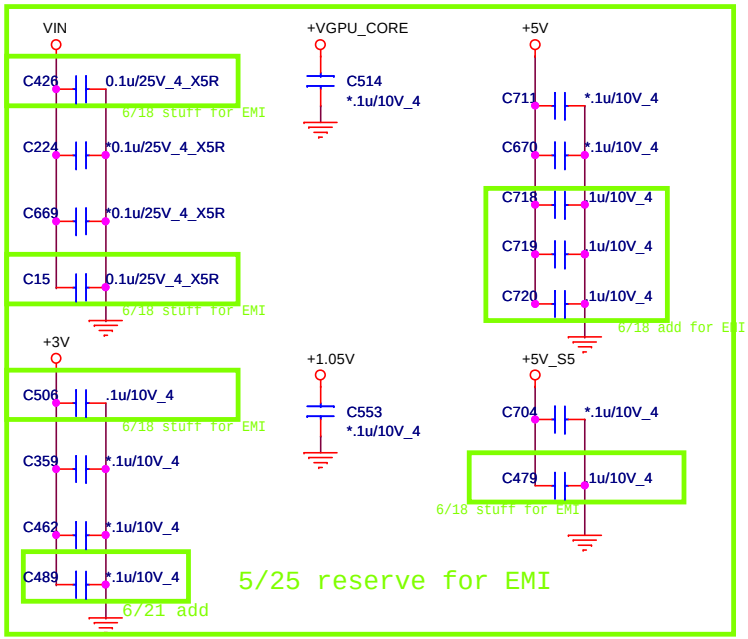


Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Tuesday, June 22, 2010	Sheet 27 of 45	

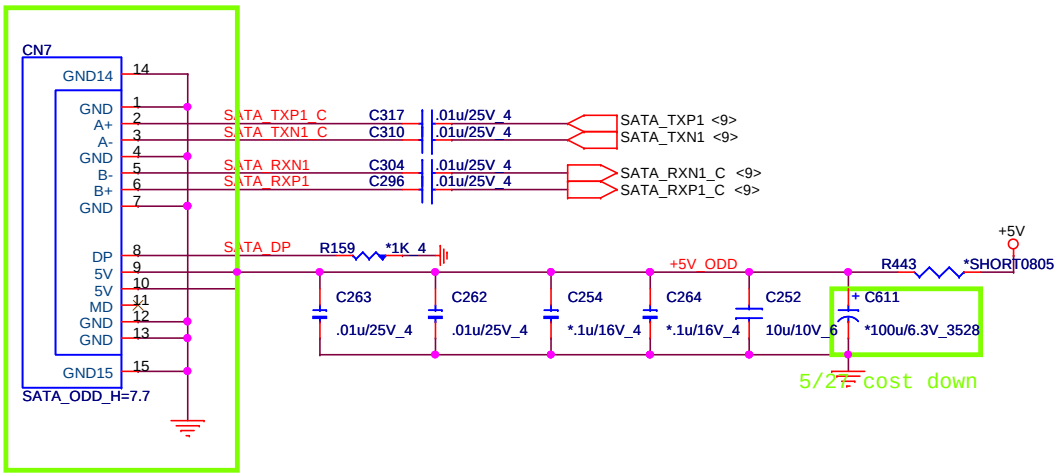
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)

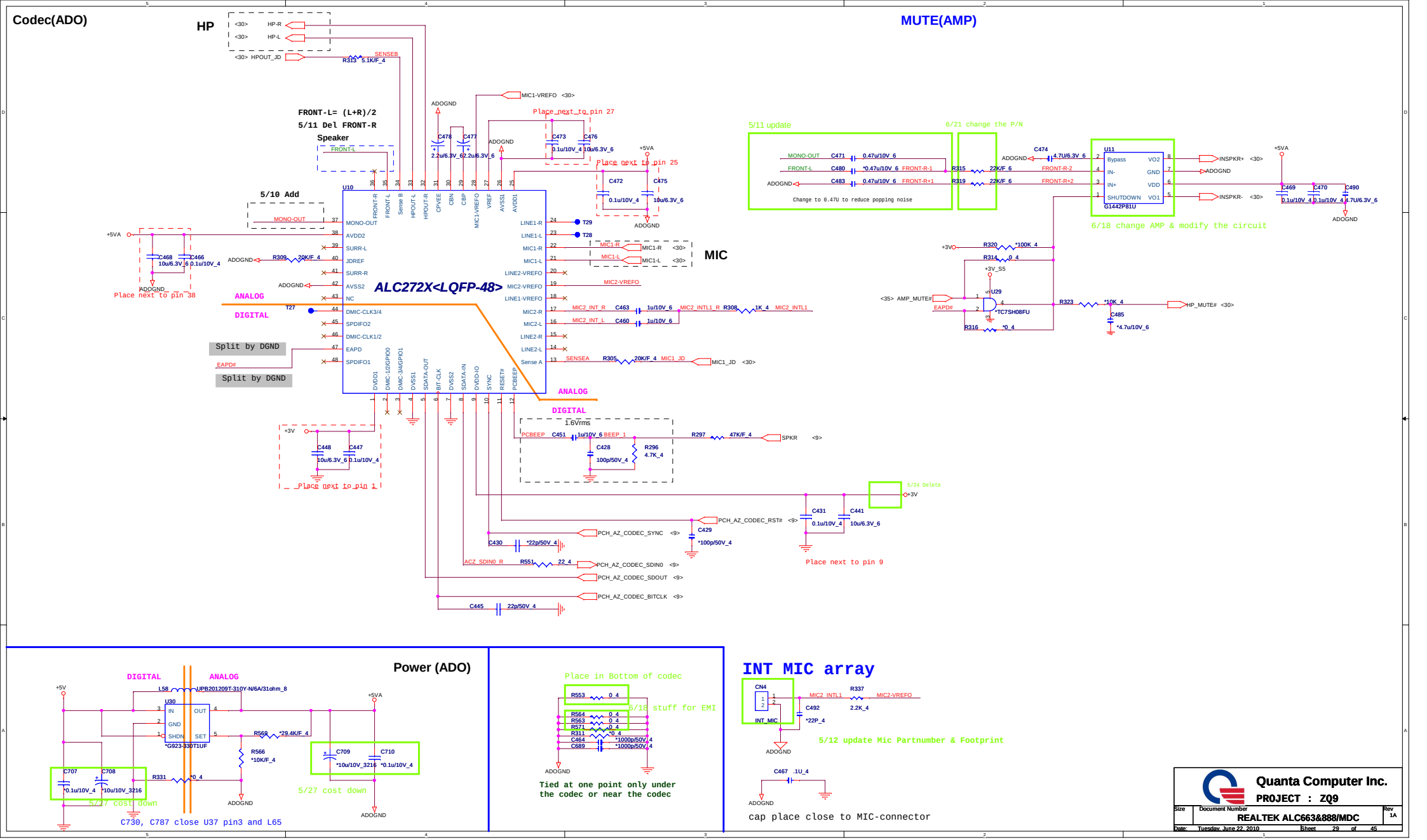


5/26 change the footprint

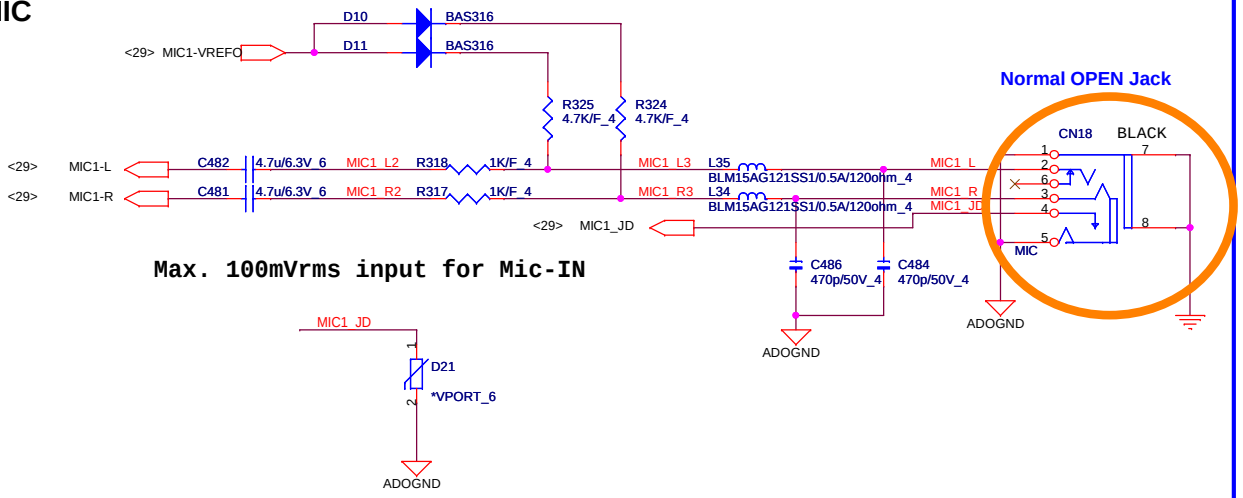
Quanta Computer Inc.

PROJECT : ZQ9

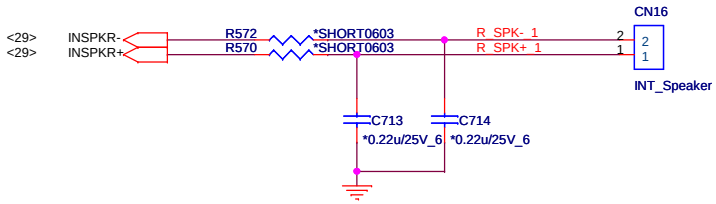
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date: Tuesday, June 22, 2010	Sheet 28 of 45	


Codec(ADO)
HP
MUTE(AMP)
MIC
ALC272X<LQFP-48>
FRONT-L= (L+R)/2
5/11 Del FRONT-R
Speaker
5/10 Add
Split by DGND
Split by DGND
Place next to pin 38
Place next to pin 1
Place next to pin 27
Place next to pin 25
Place next to pin 9
5/11 update
6/21 change the P/N
6/18 change AMP & modify the circuit
5/24 Delete
Change to 0.47U to reduce popping noise
Power (ADO)
C730, C787 close U37 pin3 and L65
5/27 cost down
5/27 cost down
Place in Bottom of codec
6/18 stuff for EMI
Tied at one point only under
the codec or near the codec
INT MIC array
5/12 update Mic Partnumber & Footprint
cap place close to MIC-connector
Quanta Computer Inc.
PROJECT : ZQ9
REALTEK ALC663&888/MDC
Tuesday, June 22, 2010
Sheet 29 of 45

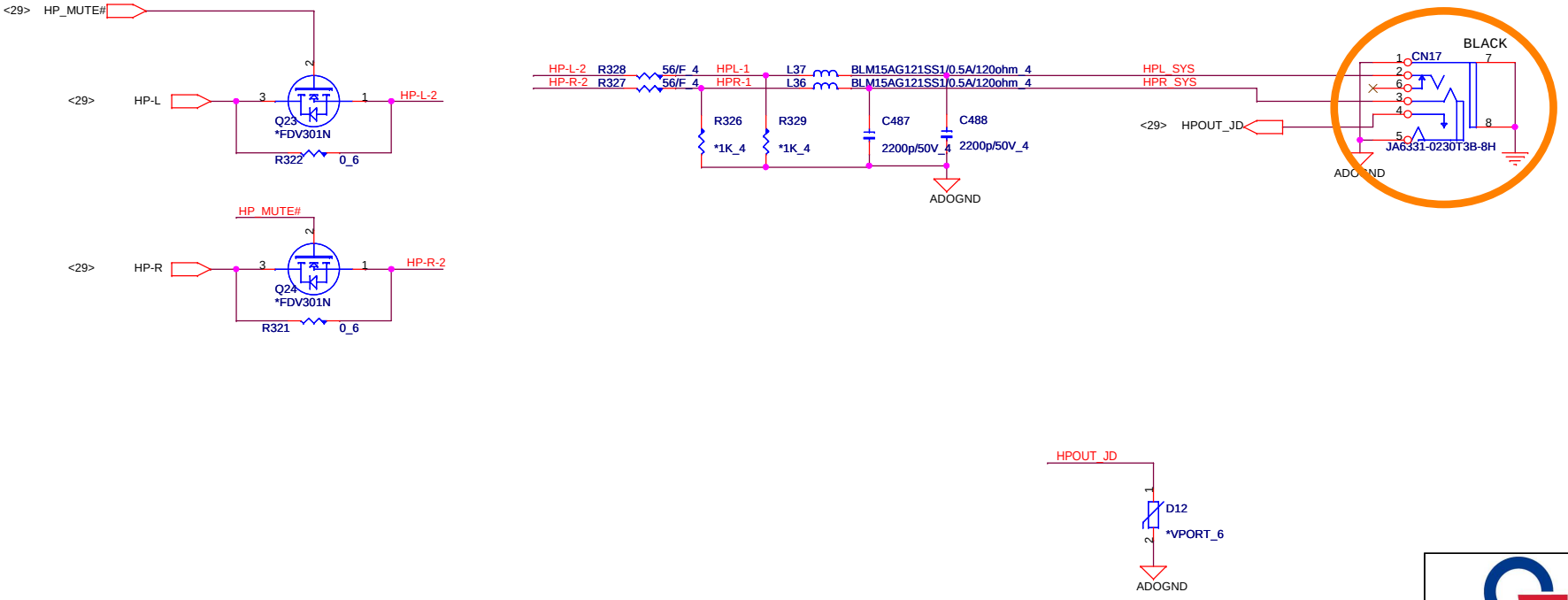
MIC



Internal Speaker



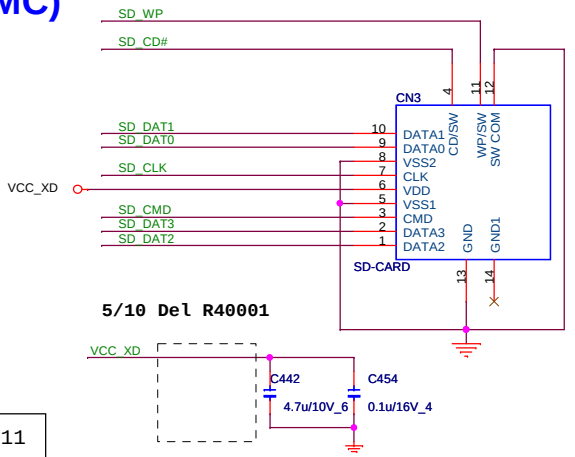
HP/SPDIF



Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Tuesday, June 22, 2010	Sheet 30 of 45	

CARD READER Controller

2 IN 1 CARD READER (SD/MMC)



Main	DFHS11FR011
Second	DFHS11FR033

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt

```
Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input
```

8/14 ZH7 remove R136, R591 and C775

5/10 Modify

CTRL0, CRTL 1 trace length shorter , and surround with GND.

U28 AU6437-GBL

crystal trace width needs at least 10 mils.

8/14 C707 close PIN11, 12

8/14 pin13 output 20mils

SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

DATA0 SD_DAT0
DATA1 SD_DAT1
DATA2 SD_DAT2
DATA3 SD_DAT3

Close to connector

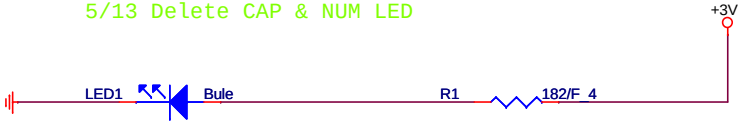
CTRL0 R300 BLM15AG121SS1/0.5A/120ohm_4 SD_CLK
CTRL1 SD_WP
CTRL2 SD_CMD
CTRL3 SD_CD#
C449 *10p/50V_4

PROJECT : ZQ5 Quanta Computer Inc.			
Size	Document Number AU6433 CardReader		Rev 1A
Date:	Tuesday, June 22, 2010	Sheet 31 of 43	

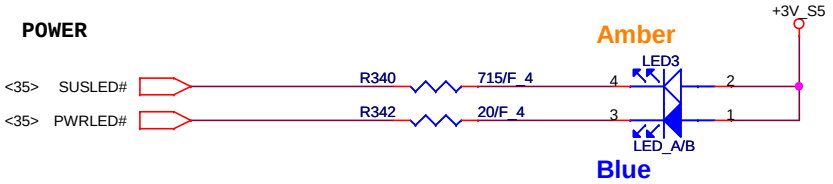
LED

5/13 Delete CAP & NUM LED

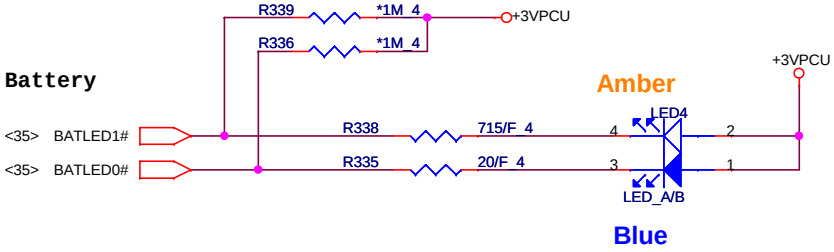
Power LED



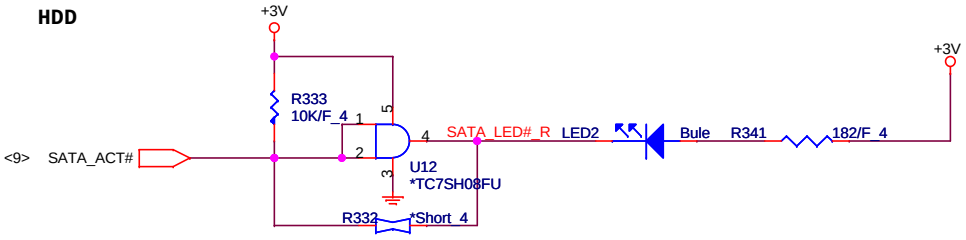
POWER



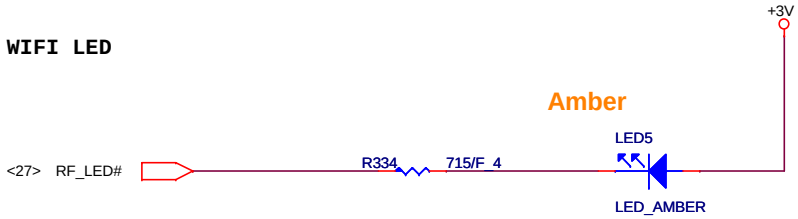
Battery



HDD

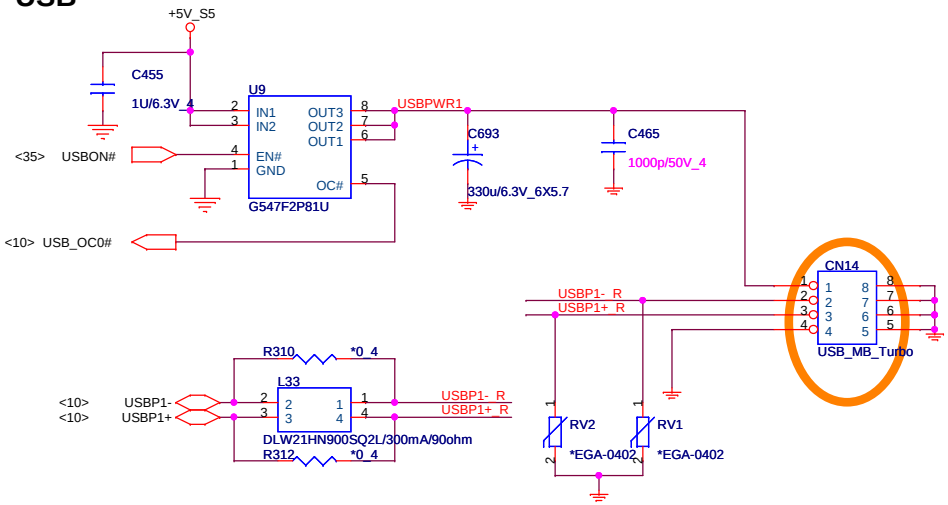


WIFI LED



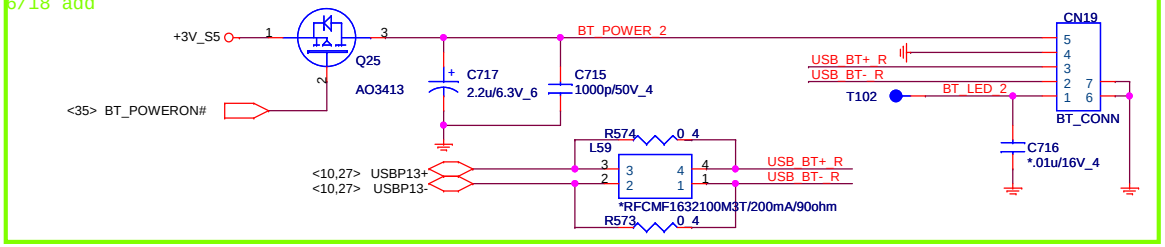
Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 1A
Date: Tuesday, June 22, 2010	Sheet 32 of 45	

USB

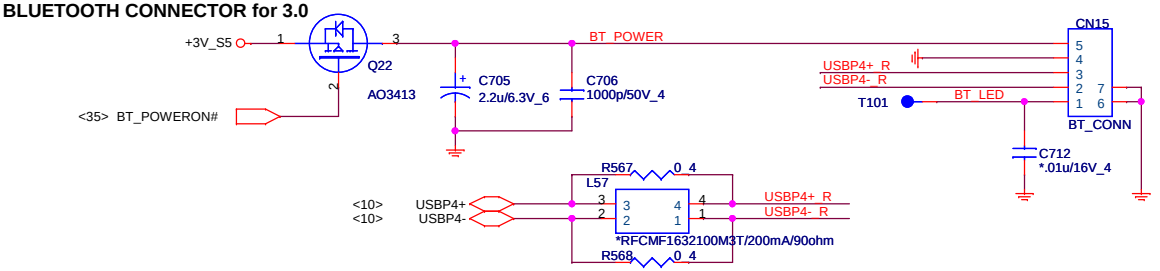


BLUETOOTH CONNECTOR for 2.0

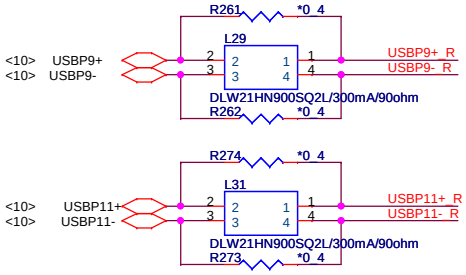
6/18 add

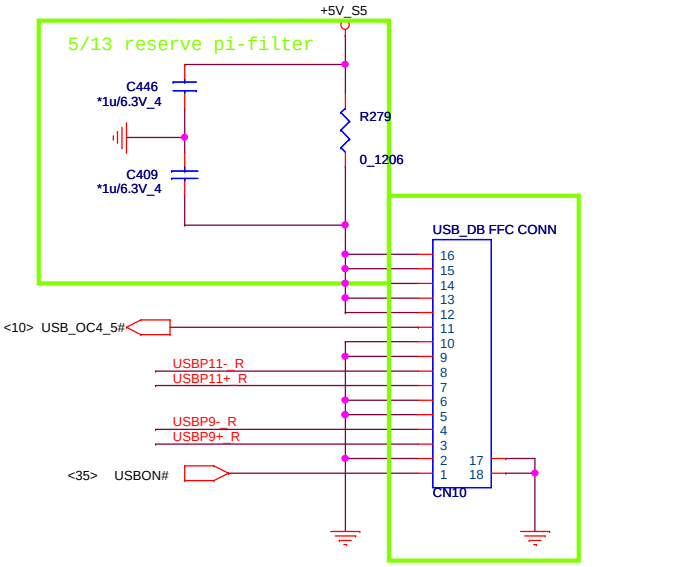


BLUETOOTH CONNECTOR for 3.0



USB/B

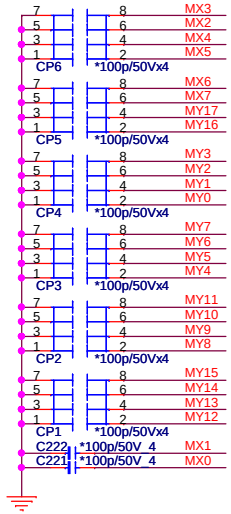


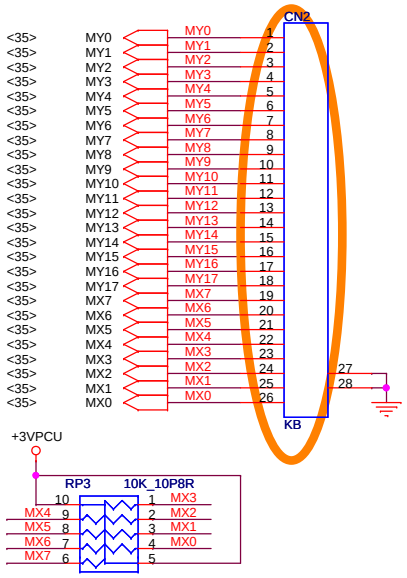


5/11 update the footprint

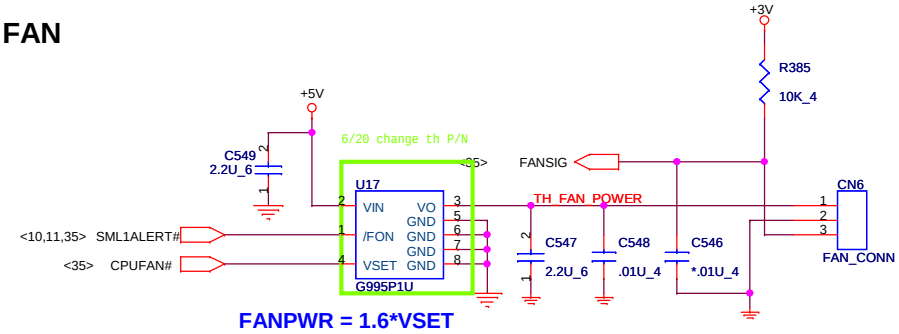
Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number	Rev
	USB/ BT	1A
Date: Tuesday, June 22, 2010	Sheet 33 of 45	

K/B



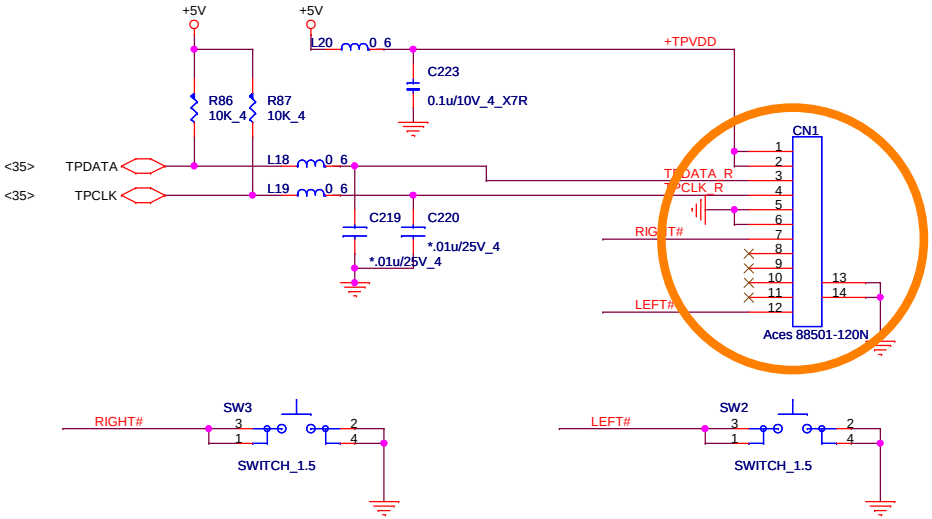


CPU FAN

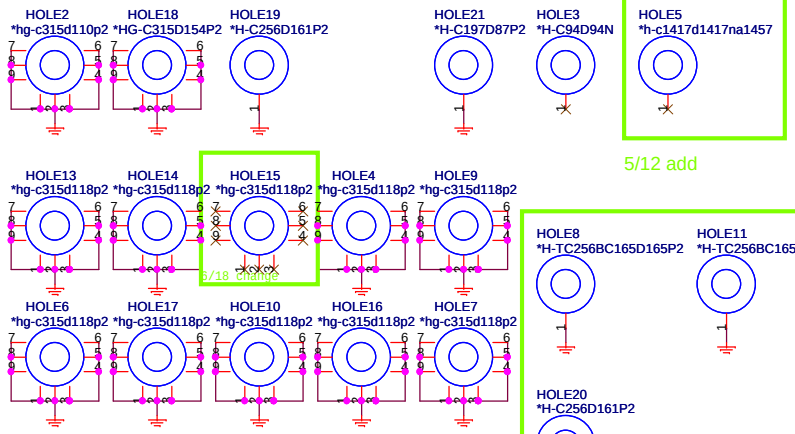


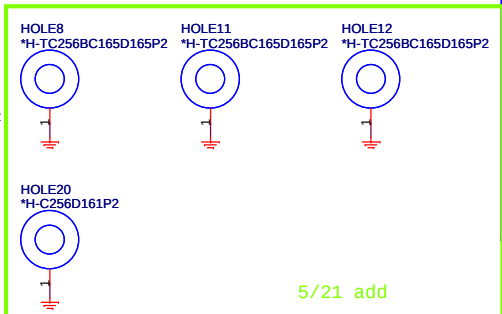
FANPWR = 1.6*VSET

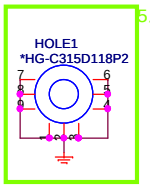
TOUCHPAD & Switch CONN.



HOLE

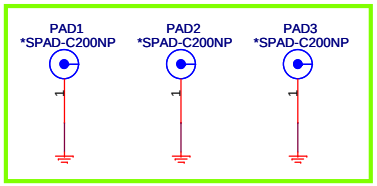






5/24 add

5/27 Delete HOLE4, HOLE22



6/21 add

Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	KB/FAN/TP+FP	1A

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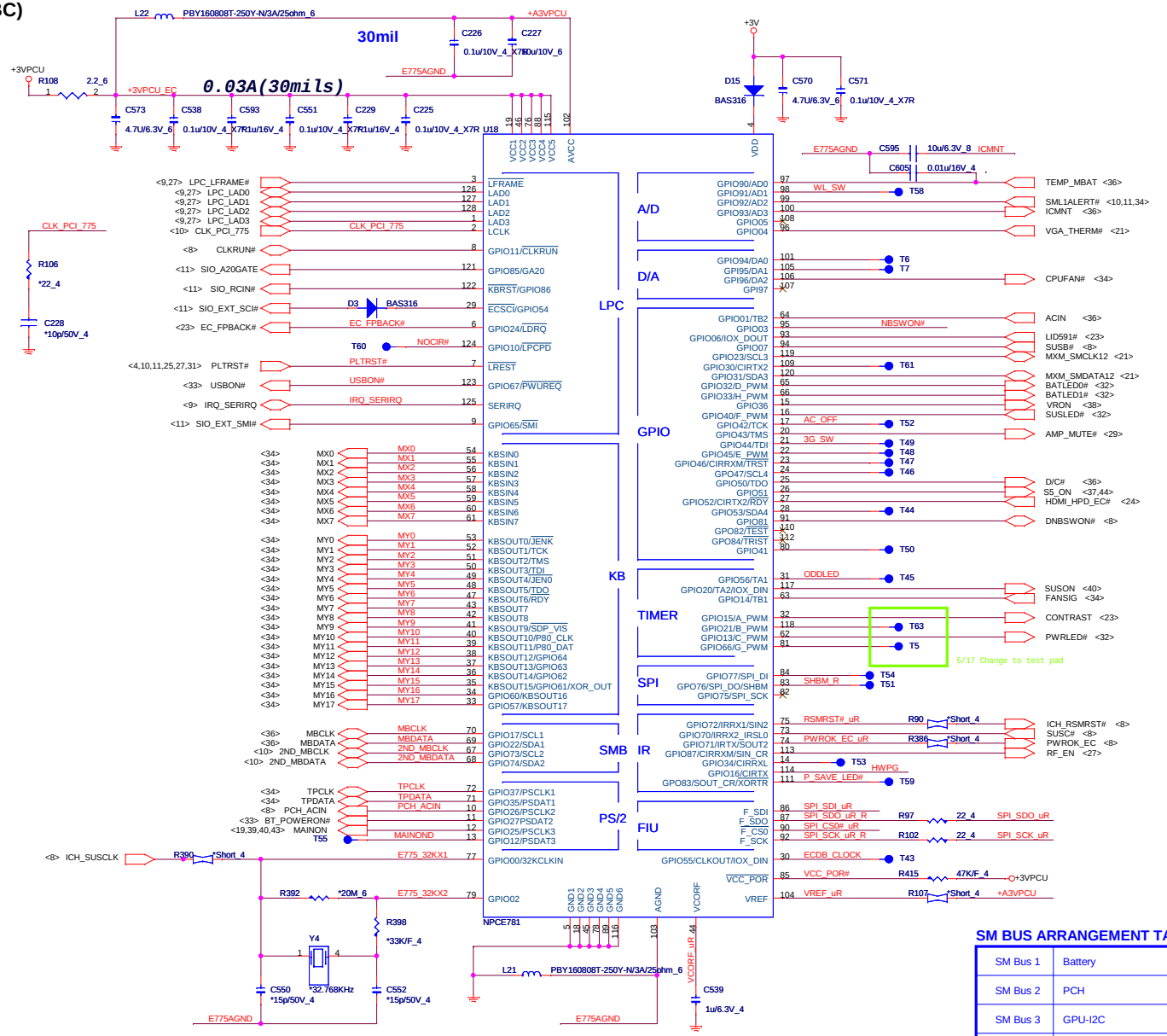
EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

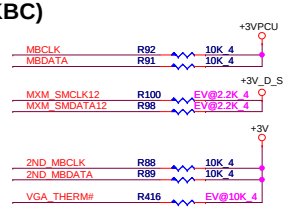
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

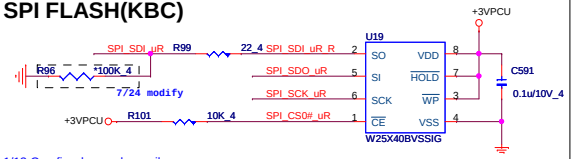
SHBM R405 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

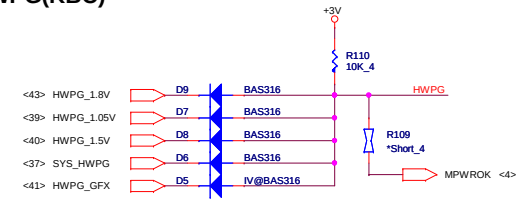


SPI FLASH(KBC)

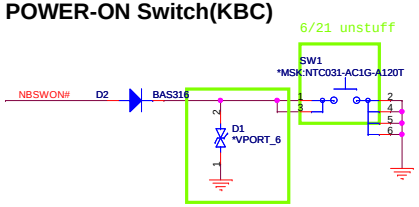


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



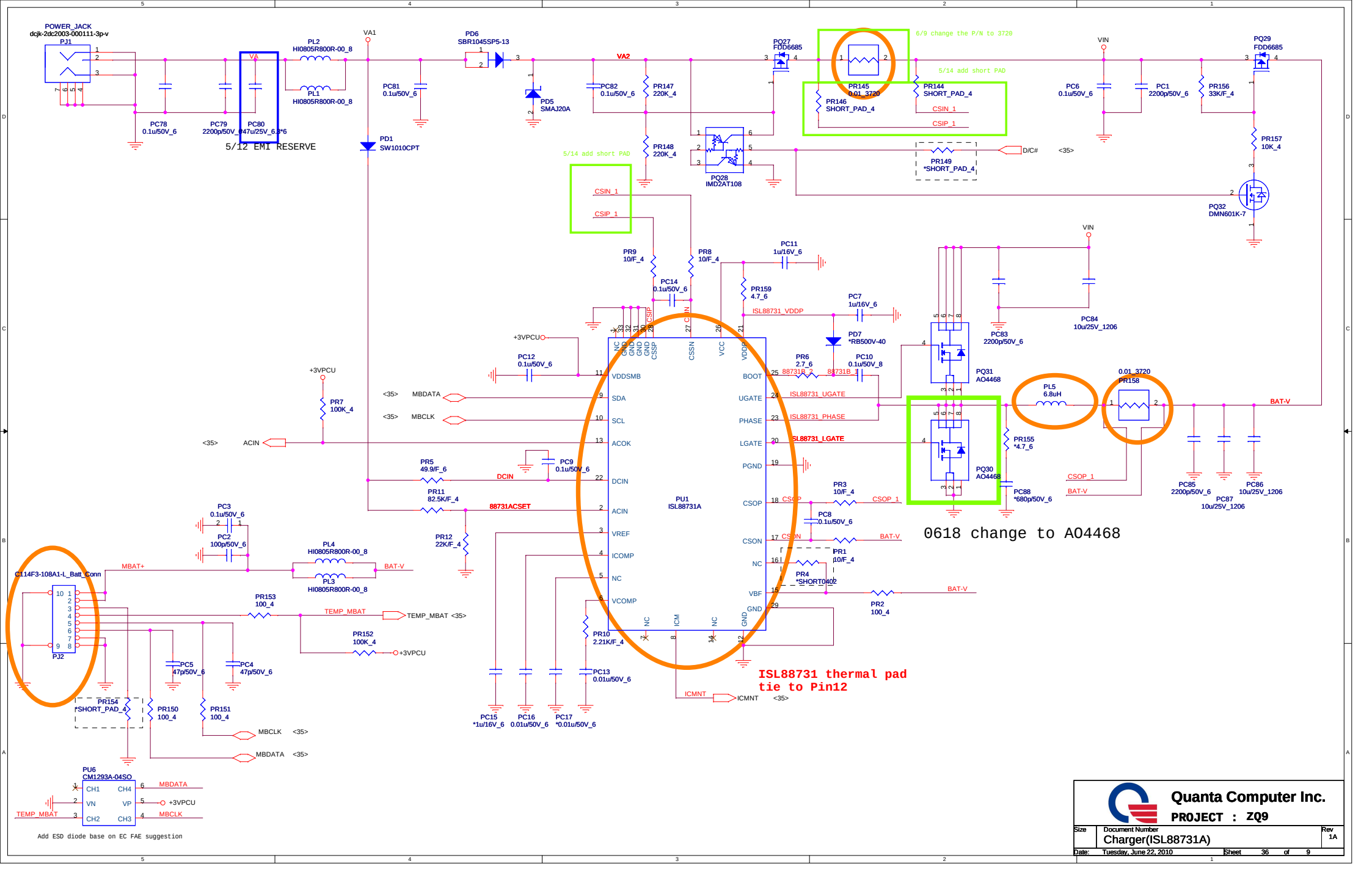
POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	WPCE781 & FLASH	1A
Date: Tuesday, June 22, 2010	Sheet 35 of 45	


POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ1
VA
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA1
PC78
0.1u/50V_6
PC79
2200p/50V_6
PC80
47u/25V_6.3*6
5/12 EMI RESERVE
PC81
0.1u/50V_6
PD1
SW1010CPT
PD6
SBR1045SP5-13
PD5
SMAJ20A
VA2
PC82
0.1u/50V_6
PR147
220K_4
PR148
220K_4
PQ28
IMD2AT108
PQ27
FDD6685
6/9 change the P/N to 3720
PR145
0.01_3720
PR146
SHORT_PAD_4
PR144
SHORT_PAD_4
5/14 add short PAD
CSIN_1
CSIP_1
PR149
*SHORT_PAD_4
D/C#
<35>
VIN
PC6
0.1u/50V_6
PC1
2200p/50V_6
PR156
33K/F_4
PQ29
FDD6685
PR157
10K_4
PQ32
DMN601K-7
PR9
10/F_4
PR8
10/F_4
PC14
0.1u/50V_6
PC11
1u/16V_6
PR159
4.7_6
PC7
1u/16V_6
ISL88731_VDDP
PD7
*RB500V-40
PC10
0.1u/50V_8
PR6
2.7_6
88731B_2
88731B_1
+3VPCU
PC12
0.1u/50V_6
PR7
100K_4
<35>
MBDATA
<35>
MBCLK
<35>
ACIN
PR5
49.9/F_6
DCIN
PC9
0.1u/50V_6
PR11
82.5K/F_4
88731ACSET
PR12
22K/F_4
PU1
ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
CSOP_1
CSON
BAT-V
PR3
10/F_4
PC8
0.1u/50V_6
PR1
10/F_4
PR4
*SHORT0402
PR2
100_4
PR10
2.21K/F_4
PC13
0.01u/50V_6
ICMNT
<35>
PC15
*1u/16V_6
PC16
0.01u/50V_6
PC17
*0.01u/50V_6
ISL88731 thermal pad
tie to Pin12
PQ31
AO4468
PQ30
AO4468
0618 change to AO4468
PL5
6.8uH
0.01_3720
PR158
PR155
*4.7_6
PC88
*680p/50V_6
PC83
2200p/50V_6
PC84
10u/25V_1206
PC85
2200p/50V_6
PC86
10u/25V_1206
PC87
10u/25V_1206
BAT-V
PC3
0.1u/50V_6
PC2
100p/50V_6
PL4
HI0805R800R-00_8
PL3
HI0805R800R-00_8
MBAT+
C114F3-108A1-L_Batt_Conn
PJ2
PR153
100_4
TEMP_MBAT
<35>
PR152
100K_4
+3VPCU
PC5
47p/50V_6
PC4
47p/50V_6
PR154
*SHORT_PAD_4
PR150
100_4
PR151
100_4
MBCLK
<35>
MBDATA
<35>
PU6
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZQ9
Size
Document Number
Charger(ISL88731A)
Rev
1A
Date:
Tuesday, June 22, 2010
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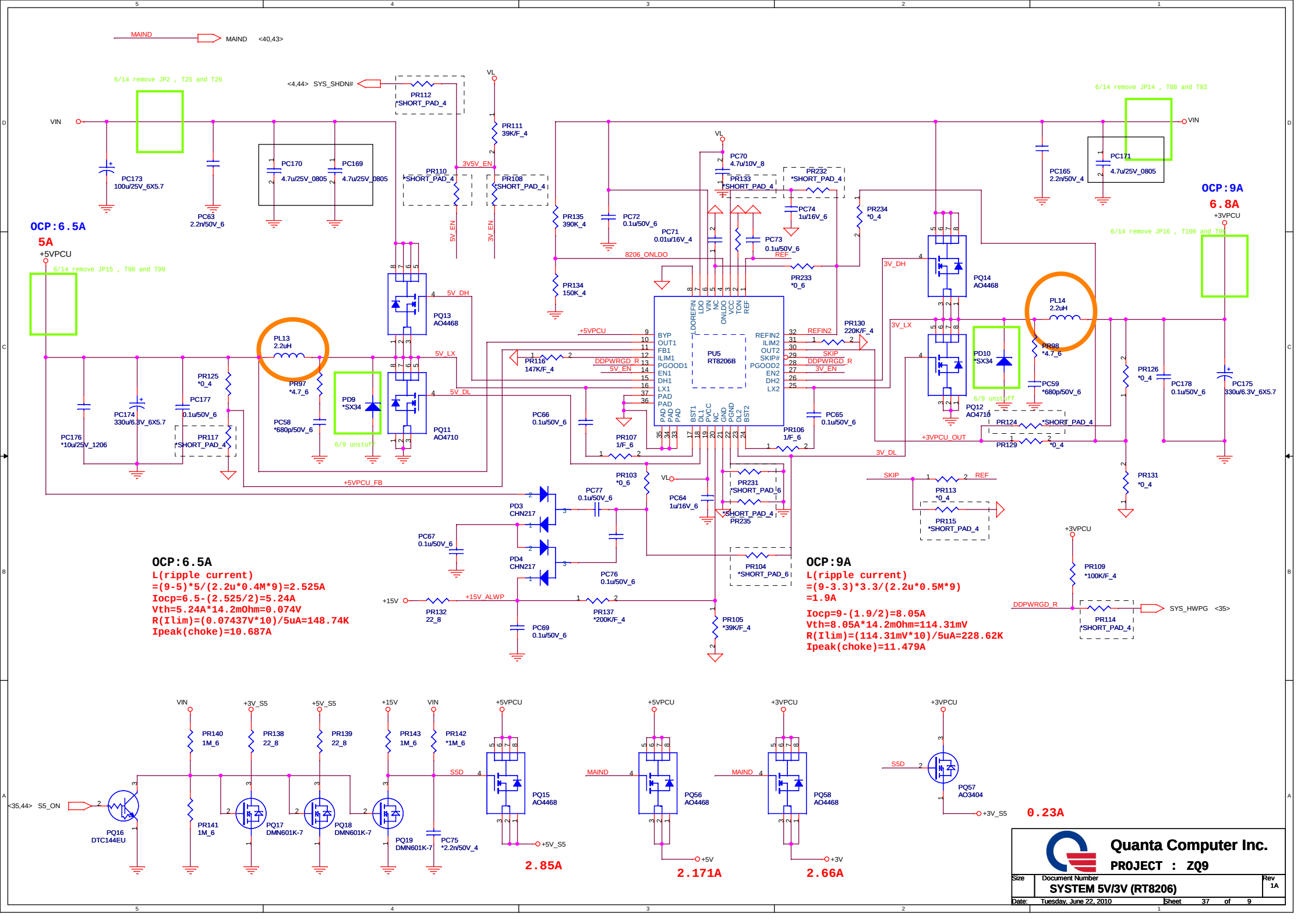
36
of
9


MAIND
MAIND <40,43>
6/14 remove JP2 , T25 and T26
<4,44> SYS_SHDN#
PR112 *SHORT_PAD_4
VL
PR111 39K/F_4
VIN
PC173 100u/25V_6X5.7
PC63 2.2n/50V_6
PC170 4.7u/25V_0805
PC169 4.7u/25V_0805
PR110 *SHORT_PAD_4
PR108 *SHORT_PAD_4
3V5V_EN
5V_EN
3V_EN
OCP:6.5A
5A
+5VPCU
6/14 remove JP15 , T98 and T99
PR135 390K_4
PR134 150K_4
PC72 0.1u/50V_6
PC71 0.01u/16V_4
8206_ONLDO
PC70 4.7u/10V_8
PR133 *SHORT_PAD_4
PR232 *SHORT_PAD_4
PC74 1u/16V_6
PC73 0.1u/50V_6
REF
PR233 *0_6
PR234 *0_4
PQ13 AO4468
PQ11 AO4710
5V_DH
5V_LX
5V_DL
PL13 2.2uH
PR97 *4.7_6
PD9 *SX34
PC58 *680p/50V_6
6/9 unstuff
PR125 *0_4
PC174 330u/6.3V_6X5.7
PC177 0.1u/50V_6
PC176 *10u/25V_1206
PR117 *SHORT_PAD_4
+5VPCU_FB
PU5 RT8206B
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 PVCC NC GND PGND DL2 BST2
PR116 147K/F_4
DDPWRGD_R
5V_EN
REFIN2
PR130 220K/F_4
SKIP
3V_EN
PC66 0.1u/50V_6
PC65 0.1u/50V_6
PR107 1/F_6
PR106 1/F_6
PR103 *0_6
PC77 0.1u/50V_6
PC64 1u/16V_6
PR231 *SHORT_PAD_6
*SHORT_PAD_4
PR235
PR104 *SHORT_PAD_6
PD3 CHN217
PD4 CHN217
PC67 0.1u/50V_6
PC76 0.1u/50V_6
PC69 0.1u/50V_6
+15V
+15V_ALWP
PR132 22_8
PR137 *200K/F_4
PR105 *39K/F_4
OCP:6.5A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)=2.525A
Iocp=6.5-(2.525/2)=5.24A
Vth=5.24A*14.2mOhm=0.074V
R(Ilim)=(0.07437V*10)/5uA=148.74K
Ipeak(choke)=10.687A
6/14 remove JP14 , T88 and T93
VIN
PC165 2.2n/50V_4
PC171 4.7u/25V_0805
OCP:9A
6.8A
+3VPCU
6/14 remove JP16 , T100 and T96
3V_DH
3V_LX
PQ14 AO4468
PQ12 AO4710
PD10 *SX34
PL14 2.2uH
PR98 *4.7_6
PC59 *680p/50V_6
6/9 unstuff
PR124 *SHORT_PAD_4
PR129 *0_4
+3VPCU_OUT
3V_DL
PR126 *0_4
PC178 0.1u/50V_6
PC175 330u/6.3V_6X5.7
PR131 *0_4
SKIP
PR113 *0_4
PR115 *SHORT_PAD_4
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
=1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14.2mOhm=114.31mV
R(Ilim)=(114.31mV*10)/5uA=228.62K
Ipeak(choke)=11.479A
+3VPCU
PR109 *100K/F_4
DDPWRGD_R
PR114 *SHORT_PAD_4
SYS_HWPG <35>
VIN
+3V_S5
+5V_S5
+15V
VIN
+5VPCU
PR140 1M_6
PR138 22_8
PR139 22_8
PR143 1M_6
PR142 *1M_6
S5D
<35,44> S5_ON
PQ16 DTC144EU
PR141 1M_6
PQ17 DMN601K-7
PQ18 DMN601K-7
PQ19 DMN601K-7
PC75 *2.2n/50V_4
PQ15 AO4468
+5V_S5
2.85A
+5VPCU
MAIND
PQ56 AO4468
+5V
2.171A
+3VPCU
MAIND
PQ58 AO4468
+3V
2.66A
+3VPCU
S5D
PQ57 AO3404
+3V_S5
0.23A
Quanta Computer Inc.
PROJECT : ZQ9
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
1A
Date: Tuesday, June 22, 2010
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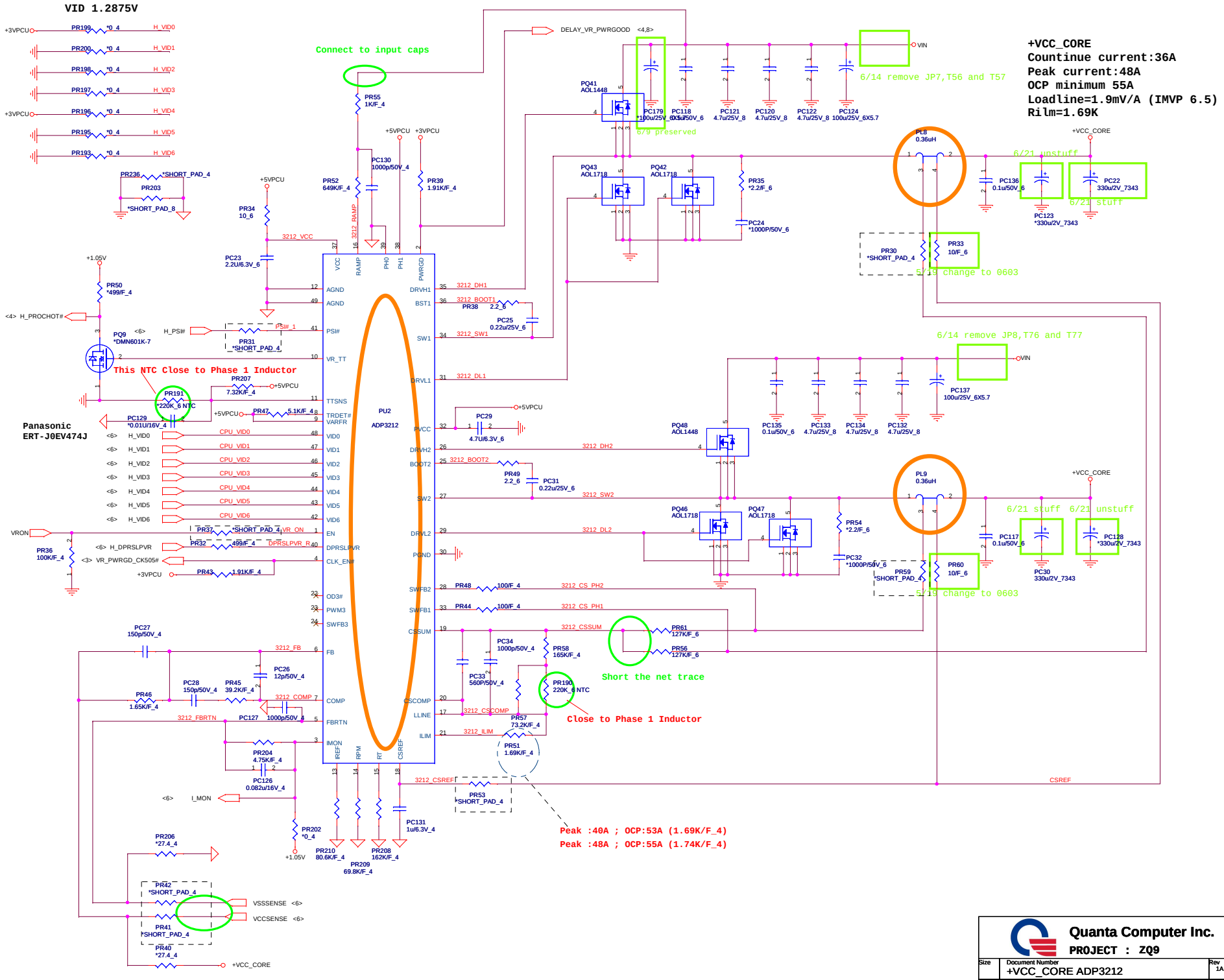
VID 1.2875V
Connect to input caps
+VCC_CORE
Countinue current:36A
Peak current:48A
OCP minimum 55A
Loadline=1.9mV/A (IMVP 6.5)
Rilm=1.69K
6/14 remove JP7,T56 and T57
6/9 preserved
6/14 remove JP8,T76 and T77
6/21 unstuff
6/21 stuff
5/19 change to 0603
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
Short the net trace
Close to Phase 1 Inductor
Peak :40A ; OCP:53A (1.69K/F_4)
Peak :48A ; OCP:55A (1.74K/F_4)
PU2
ADP3212
Quanta Computer Inc.
PROJECT : ZQ9
+VCC_CORE ADP3212
Tuesday, June 22, 2010
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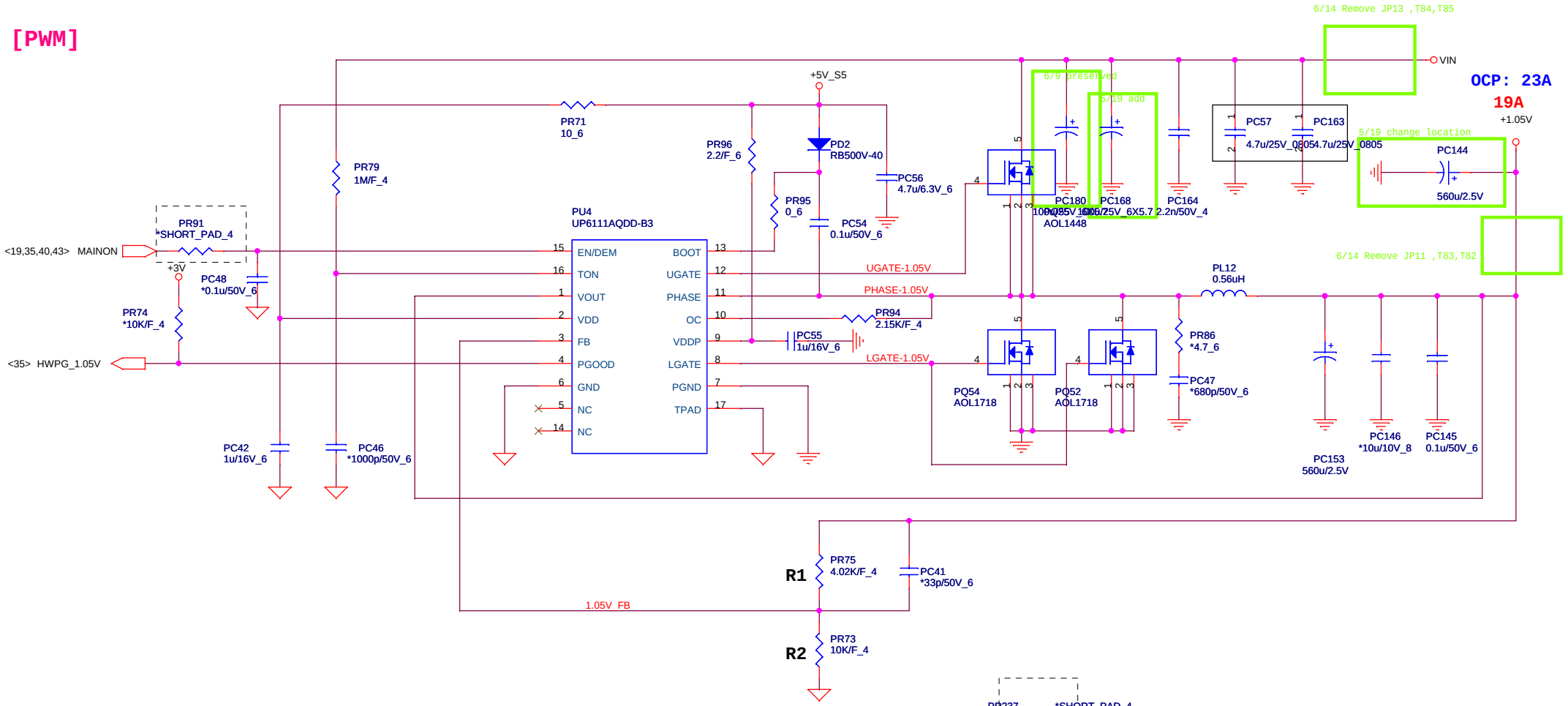

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A

RILIM=2.15mohm*23-3.256/20uA=2.122Kohm

I(choke)peak=29.512A

Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
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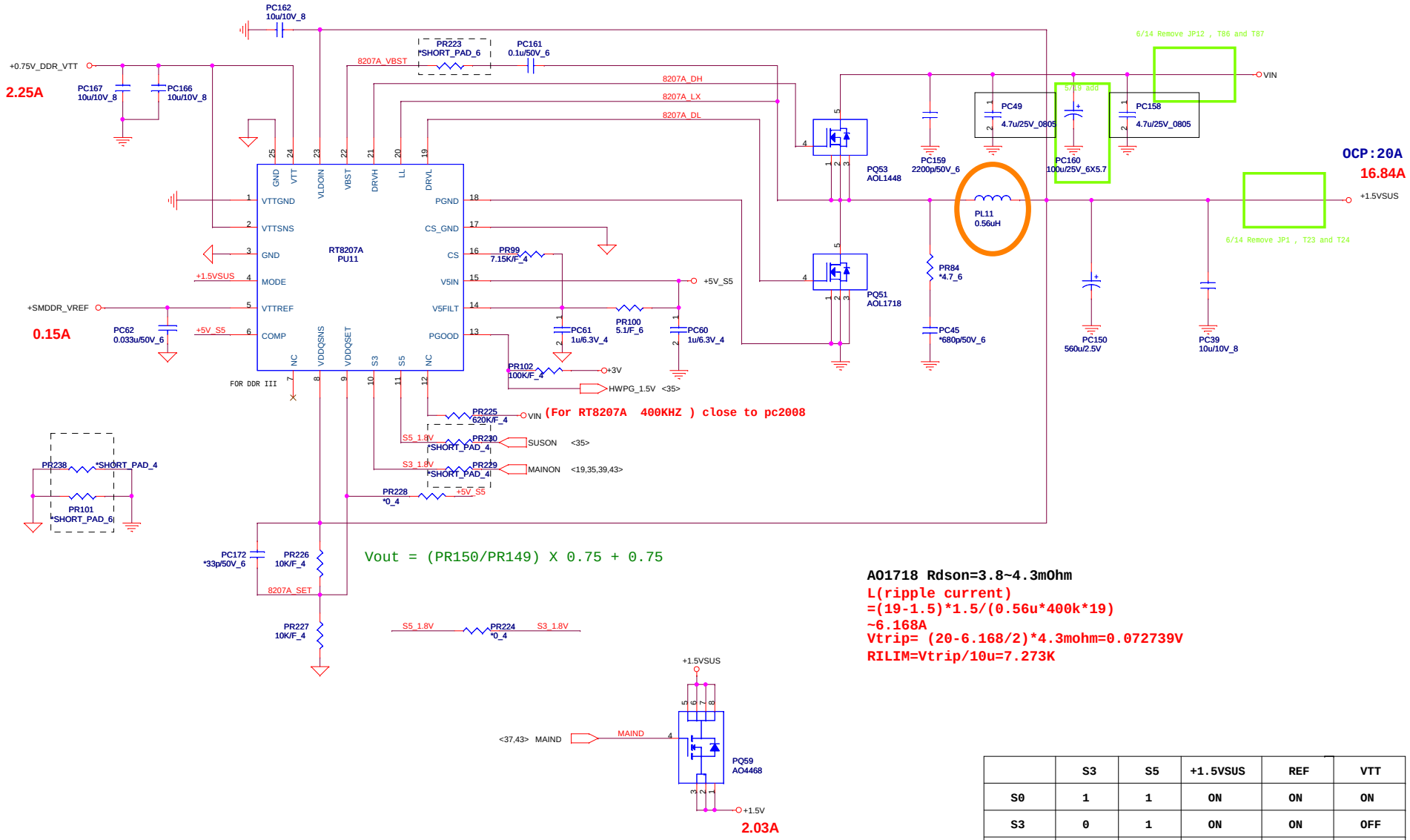
[PWM]



AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(0.56u*400k*19)
~6.168A
Vtrip= (20-6.168/2)*4.3mohm=0.072739V
RILIM=Vtrip/10u=7.273K

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A

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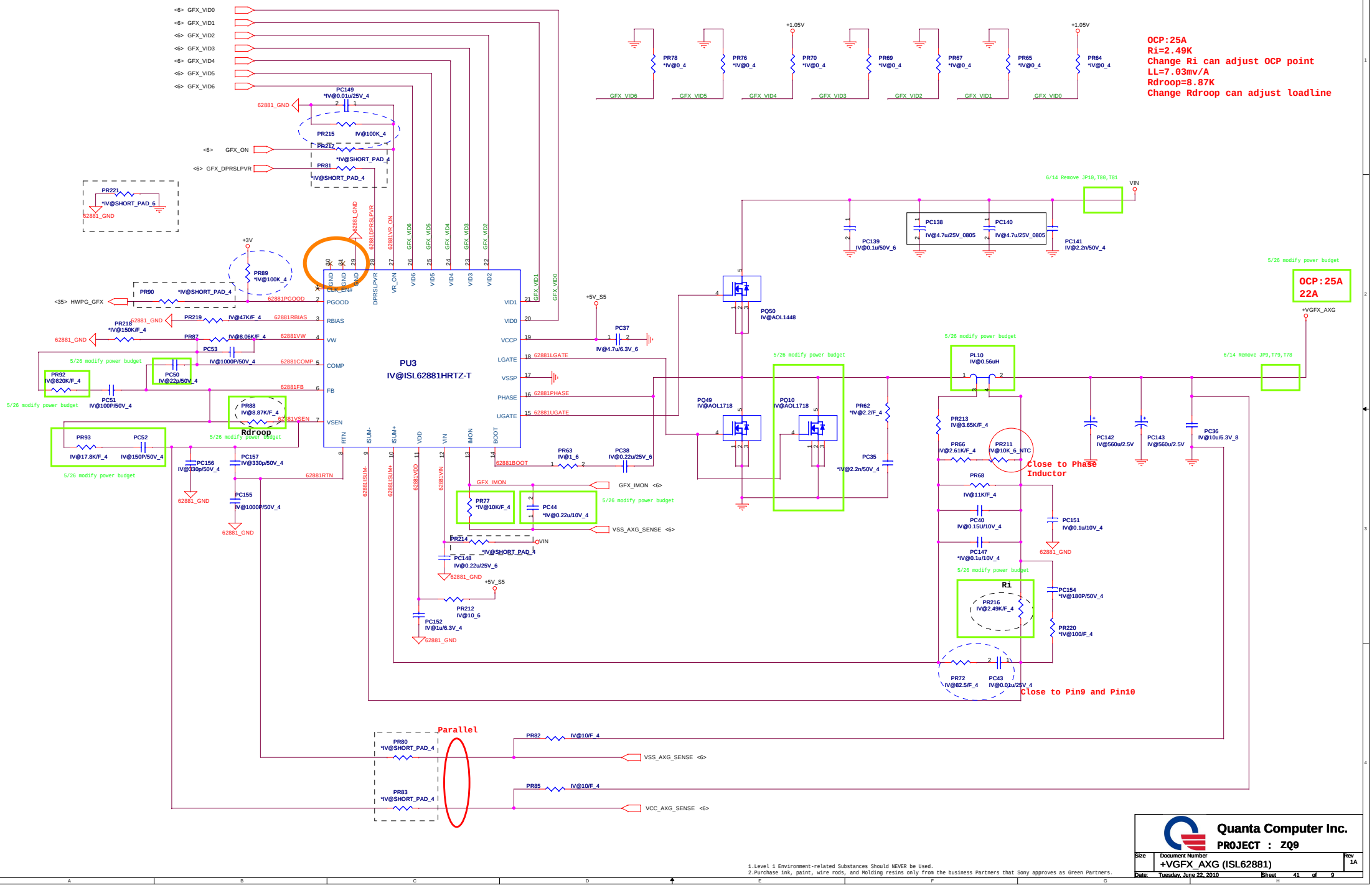
Int_VGA [PWM]

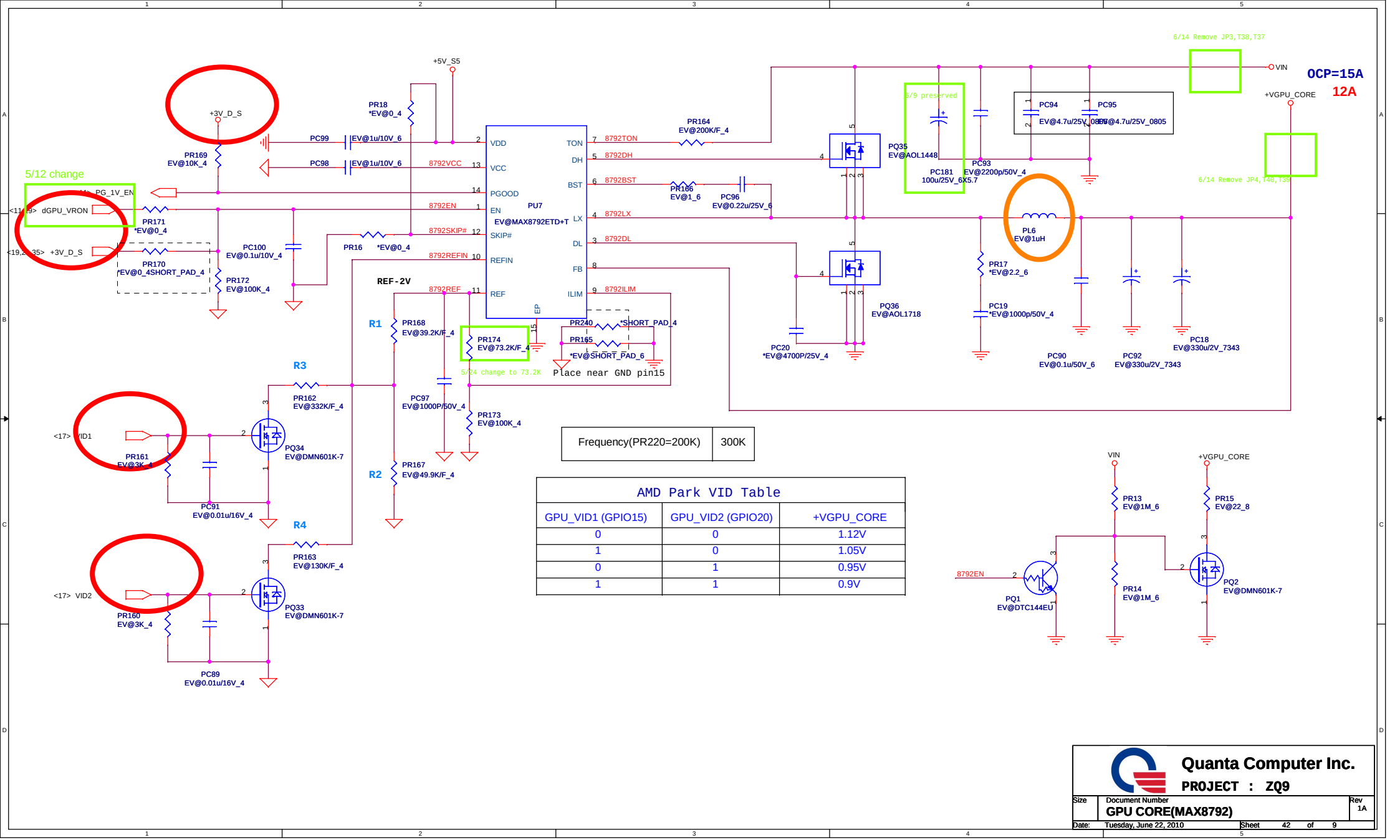


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

Date: Tuesday, June 22, 2010 Sheet 41 of 9


6/14 Remove JP3,T38,T37
OCP=15A
12A
+5V_S5
+3V_D_S
VIN
+VGPU_CORE
5/12 change
PG_1V_EN
dGPU_VRON
+3V_D_S
PR169 EV@10K_4
PR171 *EV@0_4
PR170 *EV@0_4SHORT_PAD_4
PR172 EV@100K_4
PC100 EV@0.1u/10V_4
PR18 *EV@0_4
PC99 EV@1u/10V_6
PC98 EV@1u/10V_6
PR16 *EV@0_4
8792VCC
8792EN
8792SKIP#
8792REFIN
8792REF
REF-2V
PU7
EV@MAX8792ETD+T
VDD
VCC
PGOOD
EN
SKIP#
REFIN
REF
TON
DH
BST
LX
DL
FB
ILIM
EP
8792TON
8792DH
8792BST
8792LX
8792DL
8792ILIM
PR164 EV@200K/F_4
PR166 EV@1_6
PC96 EV@0.22u/25V_6
PR240 *SHORT_PAD_4
PR165 *EV@SHORT_PAD_6
Place near GND pin15
R1
PR168 EV@39.2K/F_4
PR174 EV@73.2K/F_4
5/24 change to 73.2K
R2
PR167 EV@49.9K/F_4
R3
PR162 EV@332K/F_4
PC97 EV@1000P/50V_4
PR173 EV@100K_4
R4
PR163 EV@130K/F_4
<17> VID1
PR161 EV@3K_4
PQ34 EV@DMN601K-7
PC91 EV@0.01u/16V_4
<17> VID2
PR160 EV@3K_4
PQ33 EV@DMN601K-7
PC89 EV@0.01u/16V_4
5/9 preserved
PQ35 EV@AOL1448
PC181 100u/25V_6X5.7
PC93 EV@2200p/50V_4
PC94 EV@4.7u/25V_0805
PC95 EV@4.7u/25V_0805
PL6 EV@1uH
PQ36 EV@AOL1718
PC20 *EV@4700P/25V_4
PR17 *EV@2.2_6
PC19 *EV@1000p/50V_4
PC90 EV@0.1u/50V_6
PC92 EV@330u/2V_7343
PC18 EV@330u/2V_7343
6/14 Remove JP4,T40,T39
Frequency(PR220=200K)
300K
AMD Park VID Table
GPU_VID1 (GPIO15)
GPU_VID2 (GPIO20)
+VGPU_CORE
0 0 1.12V
1 0 1.05V
0 1 0.95V
1 1 0.9V
PR13 EV@1M_6
PR14 EV@1M_6
PR15 EV@22_8
8792EN
PQ1 EV@DTC144EU
PQ2 EV@DMN601K-7
Quanta Computer Inc.
PROJECT : ZQ9
Size
Document Number
GPU CORE(MAX8792)
Rev 1A
Date: Tuesday, June 22, 2010
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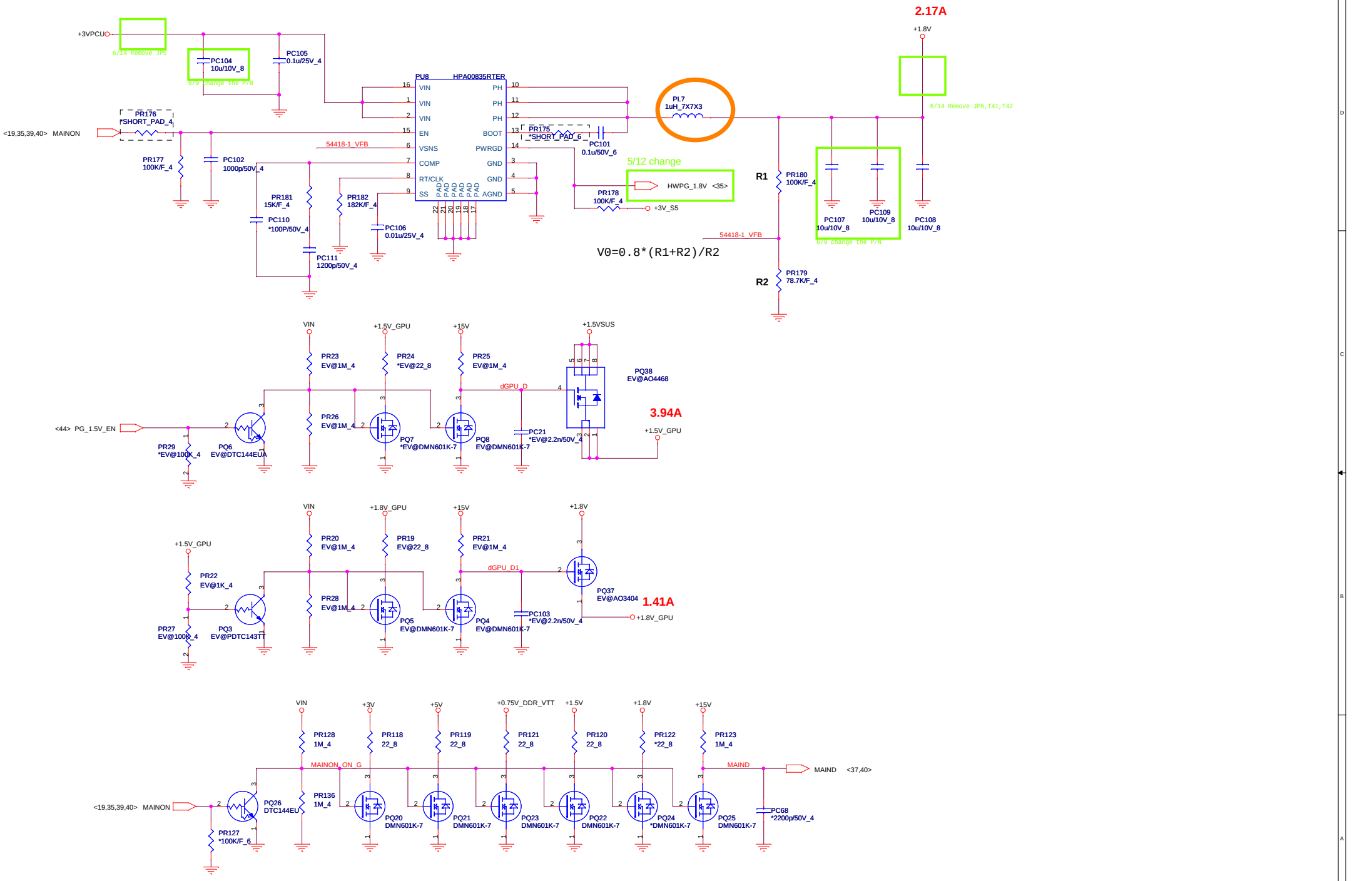
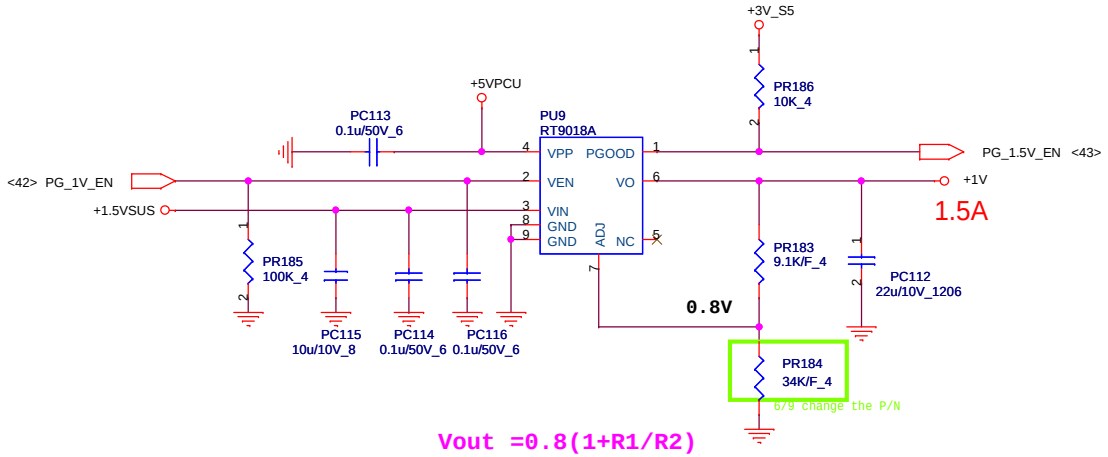


7/7 modify

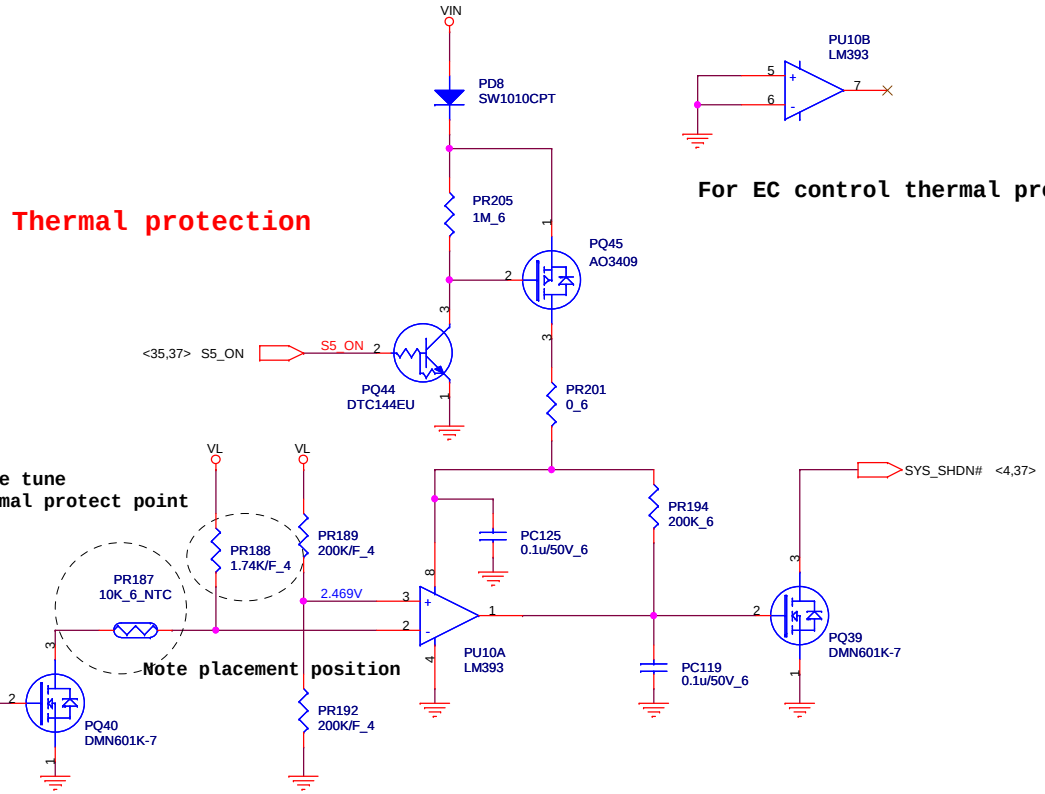
Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	Discharge/1.8V)	1A
Date: Tuesday, June 22, 2010	Sheet 43 of 9	



Vout =0.8(1+R1/R2)
=1V



Thermal protection

For EC control thermal protection (output 3.3V)

Need fine tune
for thermal protect point

Note placement position

Quanta Computer Inc.			
PROJECT : ZQ9			
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Date: Tuesday, June 22, 2010		Sheet 44 of 9	

CHANGE LIST

Model	REV	CHANGE LIST	FROM	To
ZQ9	1A	5/20 delet TP for modify Q23	X	1A
		T7000 TP7010 TP7011 TP7012 TP44	X	1A
		TP7013 TP7025 TP7022 TP7017 TP7028	X	1A
		TP39 TP7020 TP7023 T3502 T3503		
		T3500 T3501 T3506 T3510 T3518		
		T3511 T3517 T3519 T3513 T3515	1A	B2A
		T3516 T3505	1A	B2A
		5/21 swap RP7000 by following layout house's ask	1A	B2A
		add HOLE18 HOLE19 HOLE20 HOLE21 HOLE22	1A	B2A
		change the LVDS connector and swap pin define	1A	B2A
		delete PC4026	1A	B2A
		5/24 delete R30019	1A	B2A
		change PR3011 to 73.2K	1A	B2A
		stuff R3624 & R3527 and unstuff other components for changing +3V_D and +3V_D_S to +3V	1A	B2A
		swap RN5 & RN10 pin defines	1A	B2A
		change footprints of HOLE2, HOLE3, HOLE5, HOLE21 and add HOLE23	1A	B2A
		change Q45 & Q46 left side pull-high voltage to +3V	1A	B2A
		5/25 reserve C1, C2, C3, C4, C507, C508, C509, C503, C511, C515, C516, C519, C520 for EMI	1A	B2A
		5/26 update JDIM7001 & CN14 footprint	1A	B2A
		add PQ4000 change P/N of PL4000, PR4005, PC4022, PR4026, PR4006, PC4020, PR4024, PR4007, PC4018	1A	B2A
		5/27 Delete HOLE4, HOLE22	1A	B2A
	2A	6/9 stuff PC128, unstuff PC22	1A	B2A
		change the footprints C187, C178, C74, R144 to Std.	1A	B2A
		stuff R80, R79, R53 & R77, R78, R51 for Park	1A	B2A
		stuff R132, R407, R414 for board ID	1A	B2A
		stuff R293, R288, R285, R281, R280 for debug	1A	B2A
		change PR145 P/N to 3720	1A	B2A
		preserved PC179, PC180, PC181	1A	B2A
		unstuff PD9, PD10 for cost down	1A	B2A
		change PC104, PC107, PC109 P/N	1A	B2A
		change PR184 P/N	1A	B2A
		6/11 change the P/N of Q12, Q20, Q21	1A	B2A
		6/14 change Q16, PC124, PC137, PC160, PC168, PC173 C572 P/N for EOD parts	1A	B2A
		6/18 unstuff U27, C423, R287 and stuff R284 for using internal ROM for LAN	1A	B2A
		change the AMP P/N and footprint	1A	B2A
		add CN19, C715, C717, Q25, R574, R573 reserve L57, C716 for adding another BT	1A	B2A
		stuff Q13, Q14, R236, R237 & unstuff R215, R216	1A	B2A
		change U11 P/N delete C489, R565, R330	1A	B2A
		reserve R575 & R576	1A	B2A
		stuff R563, R564, R571, C15, C426, C506, C479 & add C718, C719, C720 for EMI's request	1A	B2A
Power parts		6/14 Remove Page37 JP2,JP15,JP16,JP14	1A	B2A
		Page38 JP7,JP8	1A	B2A
		Page39 JP13,JP11	1A	B2A
		Page40 JP12,JP1	1A	B2A
		Page41 JP10,JP9	1A	B2A
		Page42 JP3,JP4	1A	B2A
		Page43 JP5,JP6	1A	B2A
		6/18 Change to Shortpad 0603	1A	B2A
		PR231,PR104,PR222,PR223,PR101,PR221,PR165,PR175	1A	B2A
		Change to Shortpad 0402	1A	B2A
		PR149,PR4,PR154,PR124,PR115,PR114,PR232,PR133,PR108,PR110,PR112		
		PR117,PR30,PR59,PR31,PR37,PR53,PR42,PR41,PR91,PR230,PR229,PR217,PR81,PR90,PR214,PR80,PR83,PR170,PR176	1A	B2A
		Change to Shortpad 0805	1A	B2A
		PR203	1A	B2A
		6/18 Change PQ30 to AO4468 PN:BAM44680003	1A	B2A
		6/19 modify R90, R386, R107, R390, R109, R149, R163, R194, R233, R531, R234, R271, R556, R306, R292, R332,	1A	B2A
		[illegible] to 0402 shortpad		
		6/19 modify [illegible] to 0603 shortpad		
		6/19 modify [illegible] to 0805 shortpad		
		6/19 modify [illegible] to 1206 shortpad		
		6/20 change [illegible] for AMP change , change [illegible] P/N		
		6/21 [illegible]		
	4A			

Quanta Computer Inc.

PROJECT : ZQ9

Change list

DOC NO.	PROJECT MODEL :	ZQ9	APPROVED BY:		DATE:	2009/12/24
	PART NUMBER:		DRAWING BY:		REVISION:	C3A