
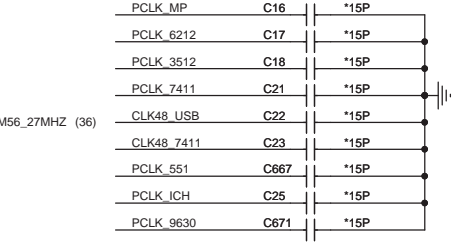
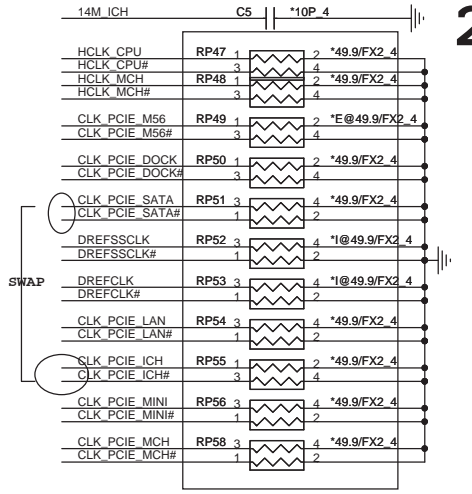
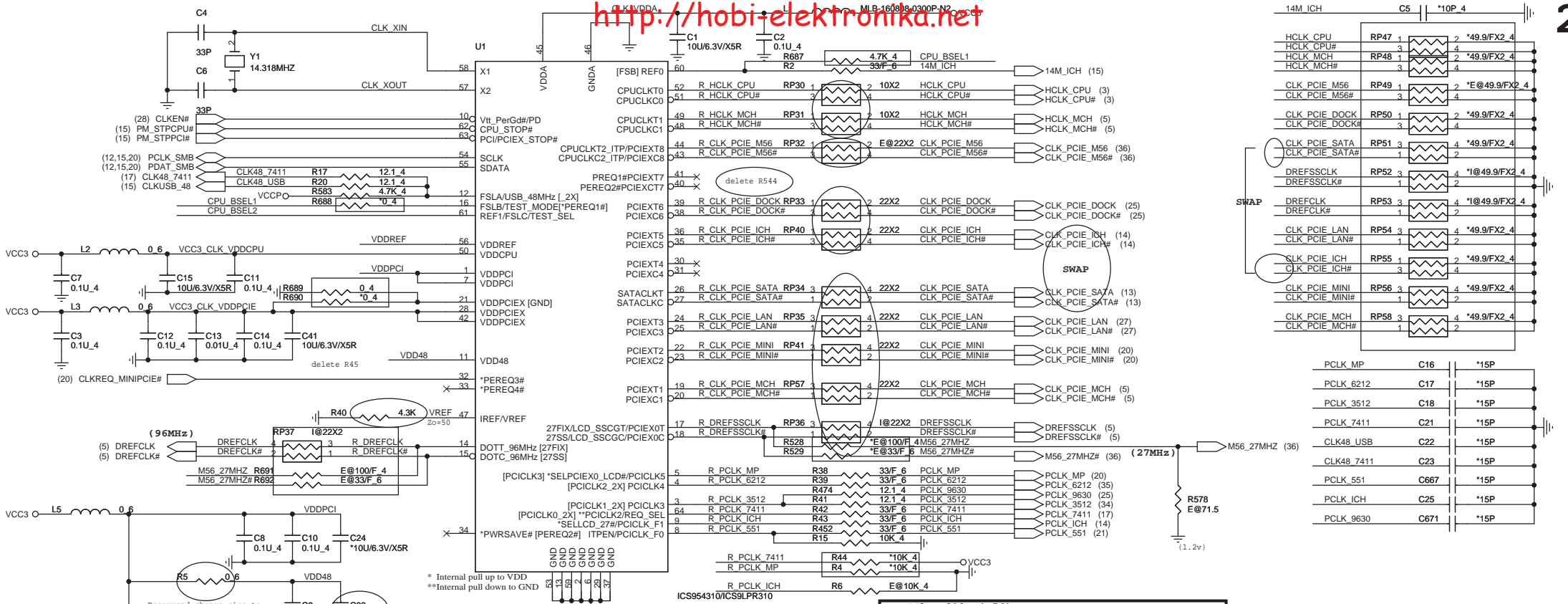


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**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>RJ6 Main Board</b>	<b>1A</b>
Date:	Tuesday, April 11, 2006	Sheet 1 of 40



**ICS91PR310 : (M56)**

ADD R689 0 ohm	Delete R690,R688,R44,R4
R40 4.3K	R528,R529,RP37
R691 100/F	RP47,RP48,RP49,RP50
R62 33	RP51,RP52,RP53,RP54
R687 4.7K	RP55,RP56,RP58

R528,R691 : 100/F ohm (915GM): Don't care R528,R529,R691,R692

**SATA Spread and Frequency Selection Table (SEL\_SATA) :**

SEL_SATA	SS3	SS2	VCO MHz	27,26 MHz	Spread %
1	0	0	tbd	100	-0.2 Down
1	0	1	tbd	100	-0.3 Down
1	1	0	tbd	100	-0.4 Down
1	1	1	tbd	100	-0.5 Down

**SEL\_SRC0 (Pin 17,18) (R4)**

0: LCDCLK Pair  
1: SRCCLK0 pair

**REQ\_SEL (Pin 40,41) (R44)**

0: PCIEXT7/PCIEXC7  
1: PREQ#

**SEL\_LCD (Pin 17,18) (R6)**

0: 27MHZSS/27MHZSS# pair (M56)  
1: LCDCLK pair (945GM)

**IREF (Pin 39) :**

475\_1% : Sets the IREF current to 2.32mA

**LCDCLK Spread and Frequency Selection Table (SEL\_LCD) :**

SEL_LCD	SS3	SS2	SS1	SS0	17,18 MHz	Spread %	SEL_LCD	SS3	SS2	SS1	SS0	17,18 MHz	Spread %
1	0	0	0	0	96	+/-1.5	0	0	0	0	0	27	+/-0.25
1	0	0	0	1	96	+/-1.25	0	0	0	0	1	27	+/-0.5
1	0	0	1	0	96	+/-1.0	0	0	0	1	0	27	+/-0.75
1	0	0	1	1	96	+/-0.8	0	0	0	1	1	27	+/-1
1	0	1	0	0	96	+/-0.6	0	0	1	0	0	27	+/-1.25
1	0	1	0	1	96	+/-0.5	0	0	1	0	1	27	+/-1.5
1	0	1	1	0	96	+/-0.4	0	0	1	1	0	27	+/-1.75
1	0	1	1	1	96	+/-0.3	0	0	1	1	1	27	+/-2
1	1	0	0	0	96	3	0	1	0	0	0	27	-0.5
1	1	0	0	1	96	2.5	0	1	0	0	1	27	-1
1	1	0	1	0	96	2	0	1	0	1	0	27	-1.25
1	1	0	1	1	96	1.75	0	1	0	1	1	27	-1.5
1	1	1	0	0	96	1.5	0	1	1	0	0	27	-1.75
1	1	1	0	1	96	1.25	0	1	1	0	1	27	-2
1	1	1	1	0	96	1	0	1	1	1	0	27	-2.5
1	1	1	1	1	96	0.8	0	1	1	1	1	27	-3

**Spread % Table:**

FSC	FSA	FSA	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
* 0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

**Center/Down Selection Table:**

Signal	Component	945GM	945PM
CLK_PCIE_M56	RP32	NI	33X2
	RP49	NI	49.9
DREFSSCLK	RP36	33X2	NI
	RP52	49.9X2	NI
	R528	NI	121
	R529	NI	33
DREFCLK	RP37	33X2	NI
	RP53	49.9X2	NI
R_PCLK_Ich	R6	NI	10K

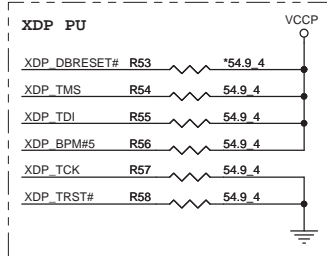
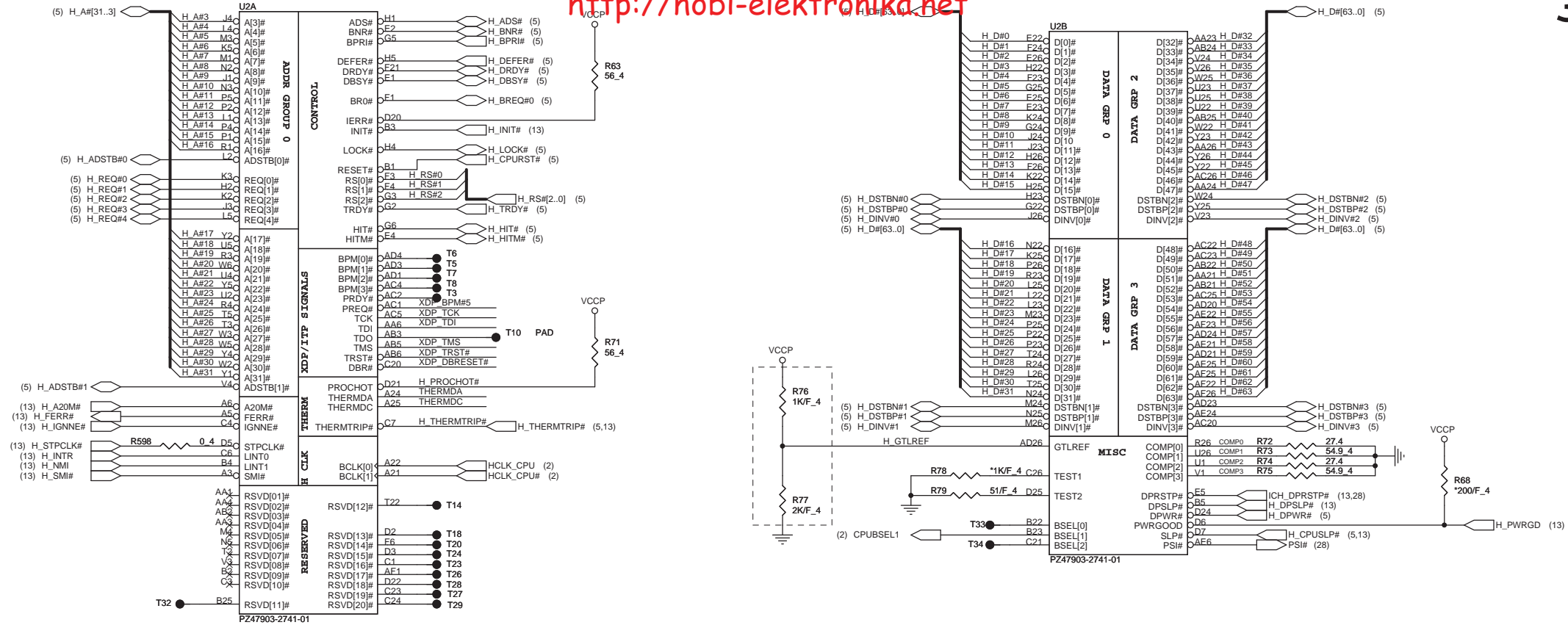
**QUANTA COMPUTER**

**CLOCK GENERATOR**

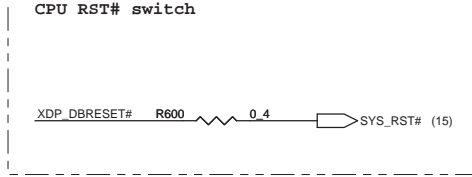
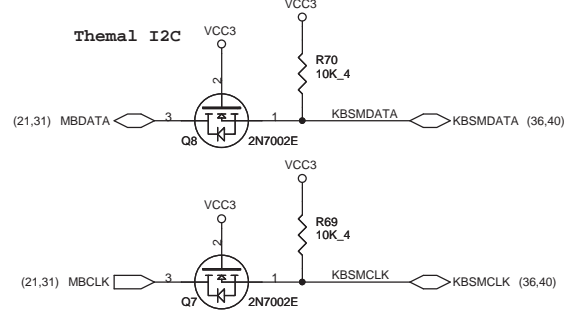
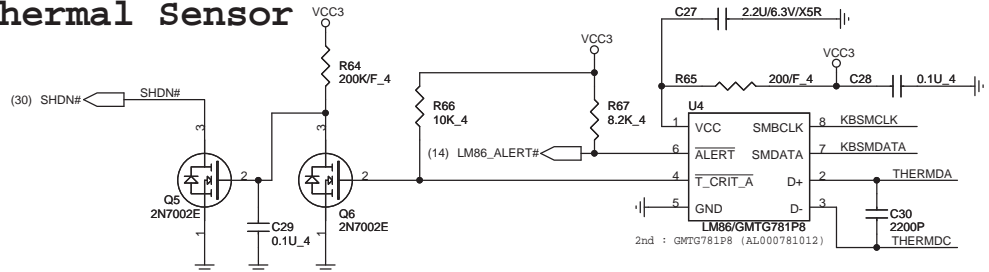
Size Custom Document Number **RJB Main Board** Rev 2A

Date: Wednesday, May 03, 2006 Sheet 2 of 40

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### Thermal Sensor



**QUANTA COMPUTER**

title **CPU1 of 2**

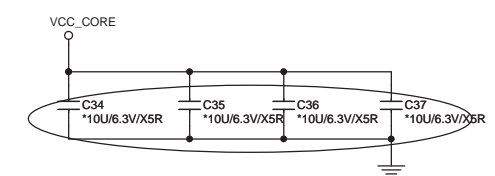
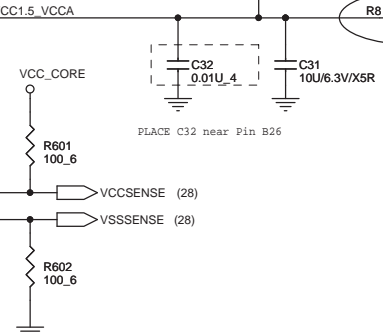
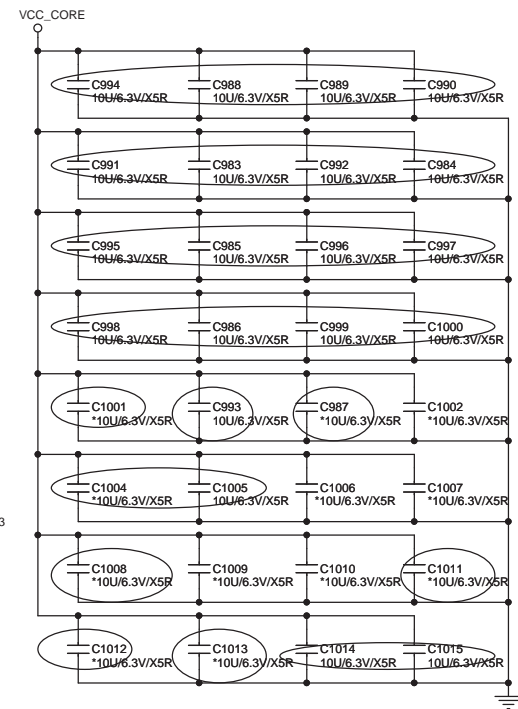
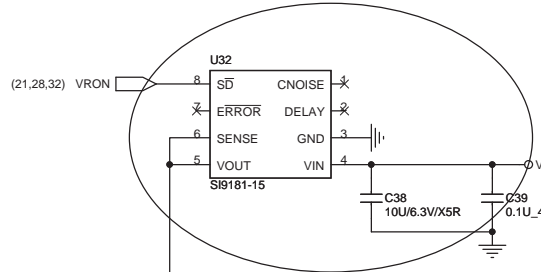
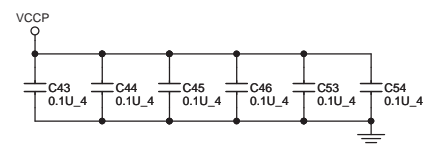
Size Document Number **RJ6 Main Board** Rev 1B

Date: Wednesday, May 03, 2006 Sheet 3 of 40

1.Level 1 Environment-related Substances Should NEVER be Used.  
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U2D	A4	VSS[001]	VSS[082]	P6
	A8	VSS[002]	VSS[083]	P21
	A11	VSS[003]	VSS[084]	P24
	A14	VSS[004]	VSS[085]	R2
	A16	VSS[005]	VSS[086]	R5
	A19	VSS[006]	VSS[087]	R25
	A23	VSS[007]	VSS[088]	T1
	A26	VSS[008]	VSS[089]	T4
	B6	VSS[009]	VSS[090]	T23
	B8	VSS[010]	VSS[091]	T26
	B11	VSS[011]	VSS[092]	U3
	B13	VSS[012]	VSS[093]	U6
	B19	VSS[013]	VSS[094]	U21
	B21	VSS[014]	VSS[095]	U24
	B24	VSS[016]	VSS[097]	V2
	C5	VSS[017]	VSS[098]	V5
	C8	VSS[018]	VSS[099]	V22
	C14	VSS[019]	VSS[100]	W1
	C16	VSS[020]	VSS[101]	W4
	C19	VSS[021]	VSS[102]	W23
	C2	VSS[023]	VSS[104]	W26
	C22	VSS[024]	VSS[105]	Y3
	C25	VSS[025]	VSS[106]	Y6
	D1	VSS[026]	VSS[107]	Y24
	D4	VSS[027]	VSS[108]	D10
	D8	VSS[028]	VSS[109]	D12
	D11	VSS[029]	VSS[110]	D14
	D13	VSS[030]	VSS[111]	D15
	D16	VSS[031]	VSS[112]	D17
	D19	VSS[032]	VSS[113]	D18
	D23	VSS[033]	VSS[114]	E7
	D26	VSS[034]	VSS[115]	E9
	E3	VSS[035]	VSS[116]	E10
	E6	VSS[036]	VSS[117]	E12
	FA	VSS[037]	VSS[118]	E15
	E11	VSS[038]	VSS[119]	E17
	F16	VSS[039]	VSS[120]	E18
	F19	VSS[040]	VSS[121]	E19
	D19	VSS[041]	VSS[122]	E20
	E21	VSS[042]	VSS[123]	F7
	E24	VSS[043]	VSS[124]	F9
	FA	VSS[044]	VSS[125]	F10
	E11	VSS[045]	VSS[126]	F12
	F13	VSS[046]	VSS[127]	F14
	F16	VSS[047]	VSS[128]	F15
	F19	VSS[048]	VSS[129]	F17
	F2	VSS[049]	VSS[130]	F18
	F22	VSS[050]	VSS[131]	F20
	F25	VSS[051]	VSS[132]	AA7
	G4	VSS[052]	VSS[133]	AA9
	G1	VSS[053]	VSS[134]	AA10
	G23	VSS[054]	VSS[135]	AA12
	G26	VSS[055]	VSS[136]	AA13
	H3	VSS[056]	VSS[137]	AA15
	H6	VSS[057]	VSS[138]	AA17
	H21	VSS[058]	VSS[139]	AA18
	H24	VSS[059]	VSS[140]	AA19
	J2	VSS[060]	VSS[141]	AA20
	J5	VSS[061]	VSS[142]	AB9
	J22	VSS[062]	VSS[143]	AC10
	J25	VSS[063]	VSS[144]	AB10
	J25	VSS[064]	VSS[145]	AB12
	K1	VSS[065]	VSS[146]	AB14
	K23	VSS[066]	VSS[147]	AB15
	K26	VSS[067]	VSS[148]	AB17
	L3	VSS[068]	VSS[149]	AB18
	L6	VSS[069]	VSS[150]	AE1
	L21	VSS[070]	VSS[151]	AE19
	L24	VSS[071]	VSS[152]	AE23
	M2	VSS[072]	VSS[153]	AE3
	M5	VSS[073]	VSS[154]	AE6
	M22	VSS[074]	VSS[155]	AE8
	M25	VSS[075]	VSS[156]	AE11
	N1	VSS[076]	VSS[157]	AE13
	N4	VSS[077]	VSS[158]	AE16
	N23	VSS[078]	VSS[159]	AE19
	N26	VSS[079]	VSS[160]	AE21
	P3	VSS[080]	VSS[161]	AE22
		VSS[081]	VSS[162]	AE24

VCC_CORE	A7	VCC[001]	VCC[68]	AB20
	A9	VCC[002]	VCC[69]	AB7
	A10	VCC[003]	VCC[70]	AC7
	A12	VCC[004]	VCC[71]	AC12
	A15	VCC[005]	VCC[72]	AC13
	A17	VCC[006]	VCC[73]	AC15
	A18	VCC[007]	VCC[74]	AC17
	A20	VCC[009]	VCC[76]	AC18
	B7	VCC[010]	VCC[77]	AD7
	B8	VCC[011]	VCC[78]	AD9
	B10	VCC[012]	VCC[79]	AD10
	B12	VCC[013]	VCC[80]	AD14
	B14	VCC[014]	VCC[81]	AD15
	B15	VCC[015]	VCC[82]	AD17
	B17	VCC[016]	VCC[83]	AD18
	B18	VCC[017]	VCC[84]	AE9
	B20	VCC[018]	VCC[85]	AE10
	C3	VCC[019]	VCC[86]	AE12
	C10	VCC[020]	VCC[87]	AE13
	C12	VCC[021]	VCC[88]	AE15
	C13	VCC[022]	VCC[89]	AE17
	C15	VCC[023]	VCC[90]	AE18
	C17	VCC[024]	VCC[91]	AE20
	C18	VCC[025]	VCC[92]	AE9
	D9	VCC[026]	VCC[93]	AE10
	D10	VCC[027]	VCC[94]	AE12
	D12	VCC[028]	VCC[95]	AE14
	D14	VCC[029]	VCC[96]	AE15
	D15	VCC[030]	VCC[97]	AE18
	D18	VCC[031]	VCC[98]	AE18
	E7	VCC[032]	VCC[99]	AE20
	E9	VCC[033]	VCC[100]	
	F10	VCC[035]	VCCP[01]	V6
	F12	VCC[036]	VCCP[02]	J6
	F13	VCC[037]	VCCP[03]	K6
	F15	VCC[038]	VCCP[04]	M6
	F17	VCC[039]	VCCP[05]	J21
	F18	VCC[040]	VCCP[06]	K21
	F20	VCC[041]	VCCP[07]	M21
	F7	VCC[042]	VCCP[08]	N21
	F9	VCC[043]	VCCP[09]	N6
	F10	VCC[044]	VCCP[10]	R6
	F12	VCC[045]	VCCP[11]	T21
	F14	VCC[046]	VCCP[12]	R21
	F15	VCC[047]	VCCP[13]	T6
	F17	VCC[048]	VCCP[14]	V21
	F18	VCC[049]	VCCP[15]	W21
	F20	VCC[050]	VCCP[16]	
	AA7	VCC[051]		
	AA9	VCC[052]		
	AA10	VCC[053]		
	AA12	VCC[054]		
	AA13	VCC[055]		
	AA15	VCC[056]		
	AA17	VCC[057]		
	AA18	VCC[058]		
	AA19	VCC[059]		
	AA20	VCC[060]		
	AB9	VCC[061]		
	AC10	VCC[062]		
	AB10	VCC[063]		
	AB12	VCC[064]		
	AB14	VCC[065]		
	AB15	VCC[066]		
	AB17	VCC[067]		
	AB18	VCC[068]		



PZ47903-2741-01

PZ47903-2741-01

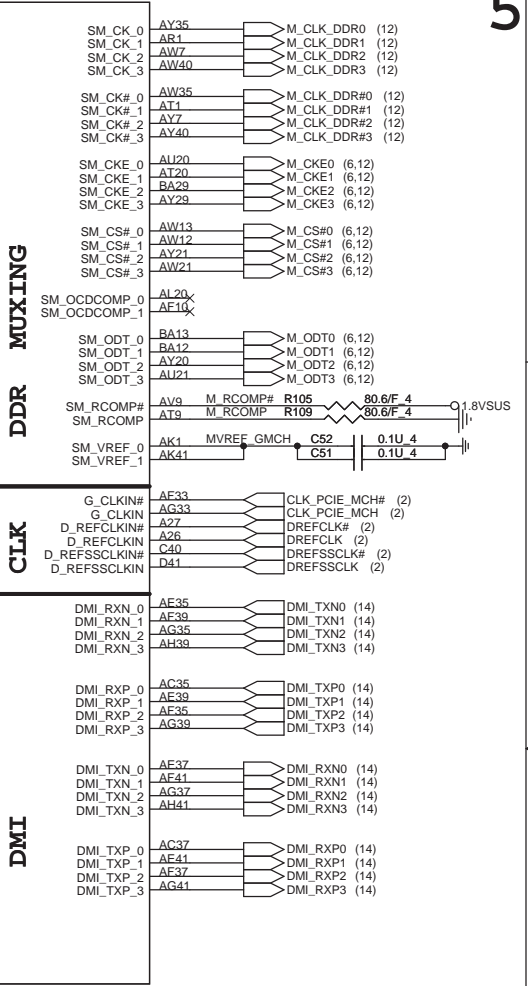
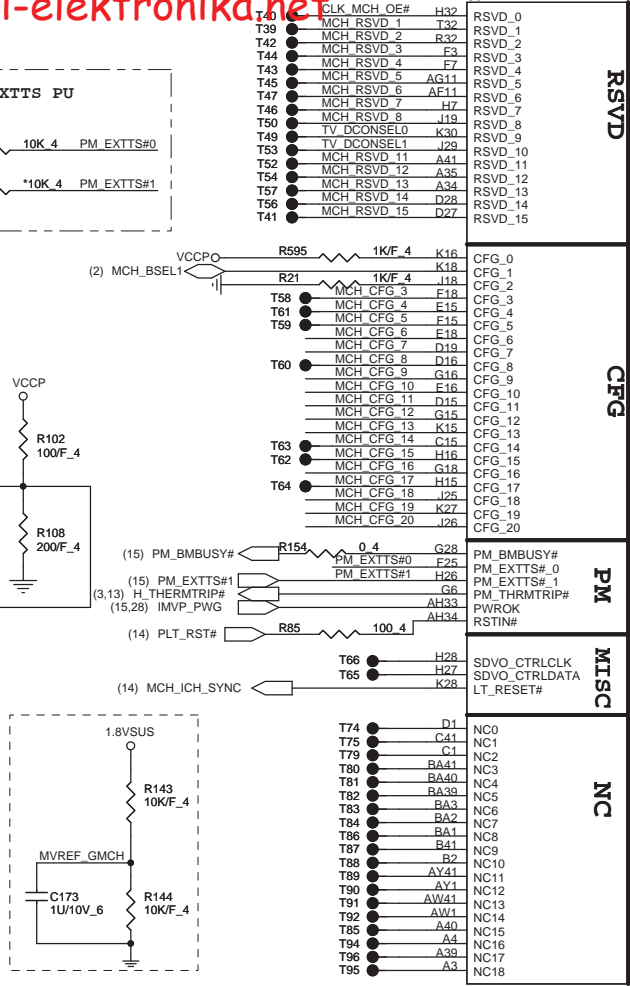
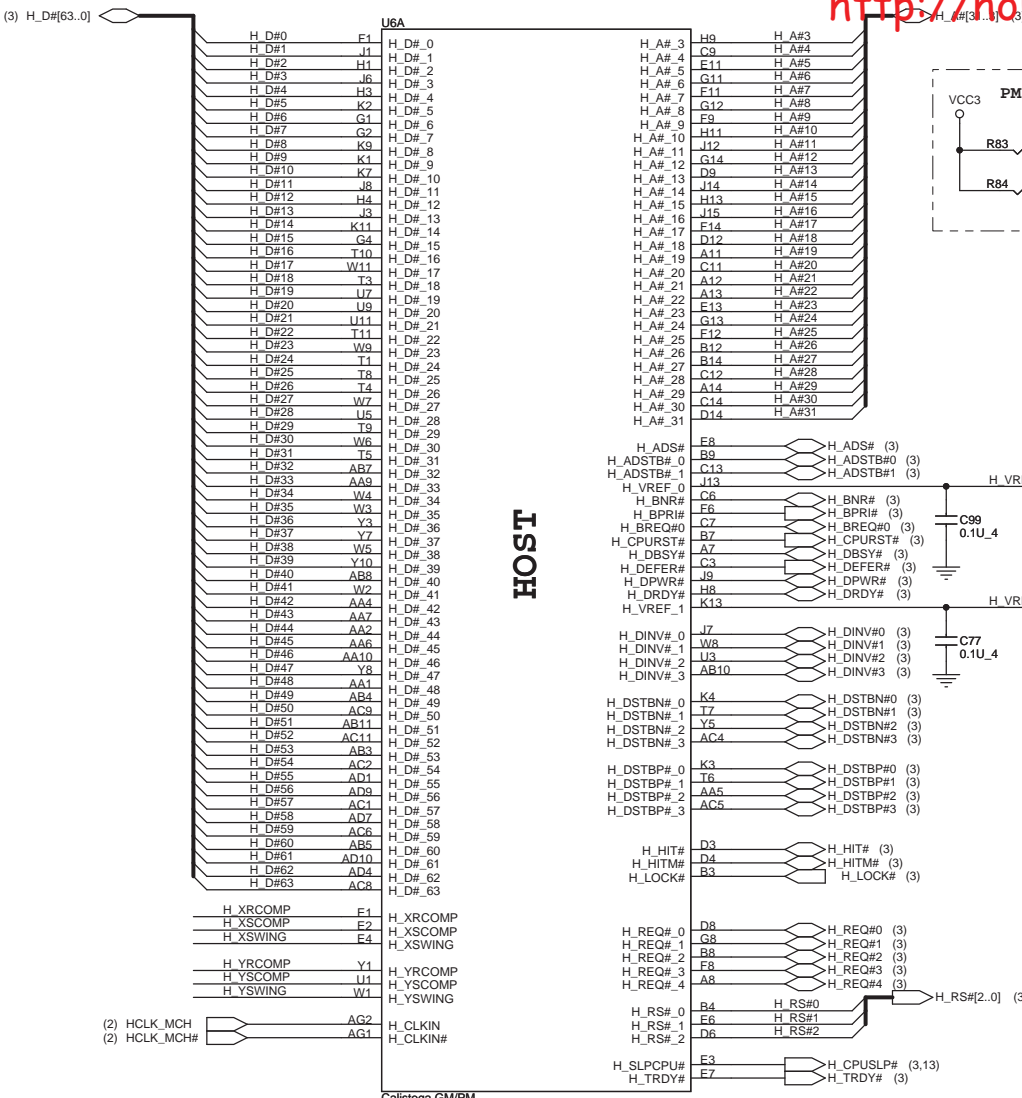
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**QUANTA COMPUTER**

Title: **CPU 2 of 2**

Size: Document Number: **RJ6 Main Board** Rev: 2A

Date: Wednesday, May 03, 2006 Sheet: 4 of 40

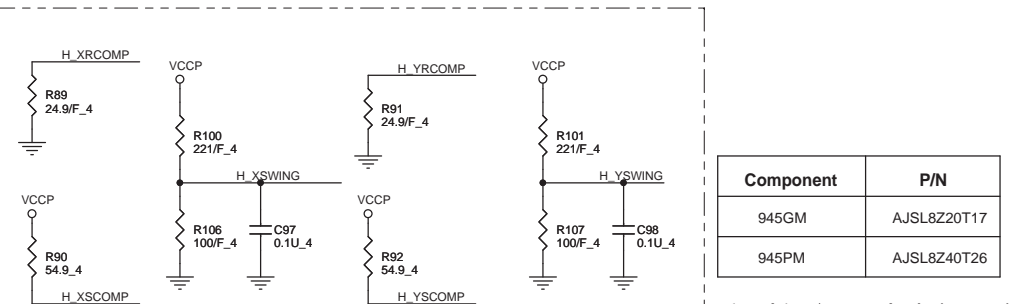


### GMCH Strap pin description

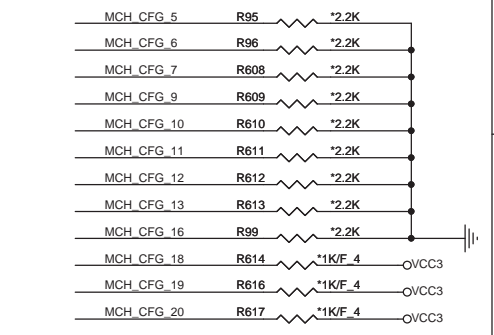
Pin	Low	High
CGF5	DMix2	DMix4
CGF6	RSVD	RSVD for 945GM5
CGF7	RSVD	CPU type: Mobile CPU
CGF9	PCIe Graphics lan : Reverse Lane	PCIe Graphics lan : Normal operation
CGF10	reserved	reserved
CGF11	reserved	reserved
CGF16	FSB Dynamic ODT Disabled	FSB Dynamic ODT Enabled
CGF18	GMCH core: 1.05V	GMCH core: 1.5V
CGF19	DMI LANE Normal	DMI LANE Reversed
CGF20	only SDVO or PCIe x1 is operational	SDVO and PCIe x1 are operation simultaneously via the PEG port

CGF[13:12]  
 00 = Partial clock gating disable  
 01 = XOR mode enabled  
 10 = All-Z mode enabled  
 \* 11 = Normal Operation(Default)

Int.Pull-down : CGF 18,19,20  
 Int.Pull-high : CGF CFG 3-17



Component	P/N
945GM	AJSL8Z20T17
945PM	AJSL8Z40T26



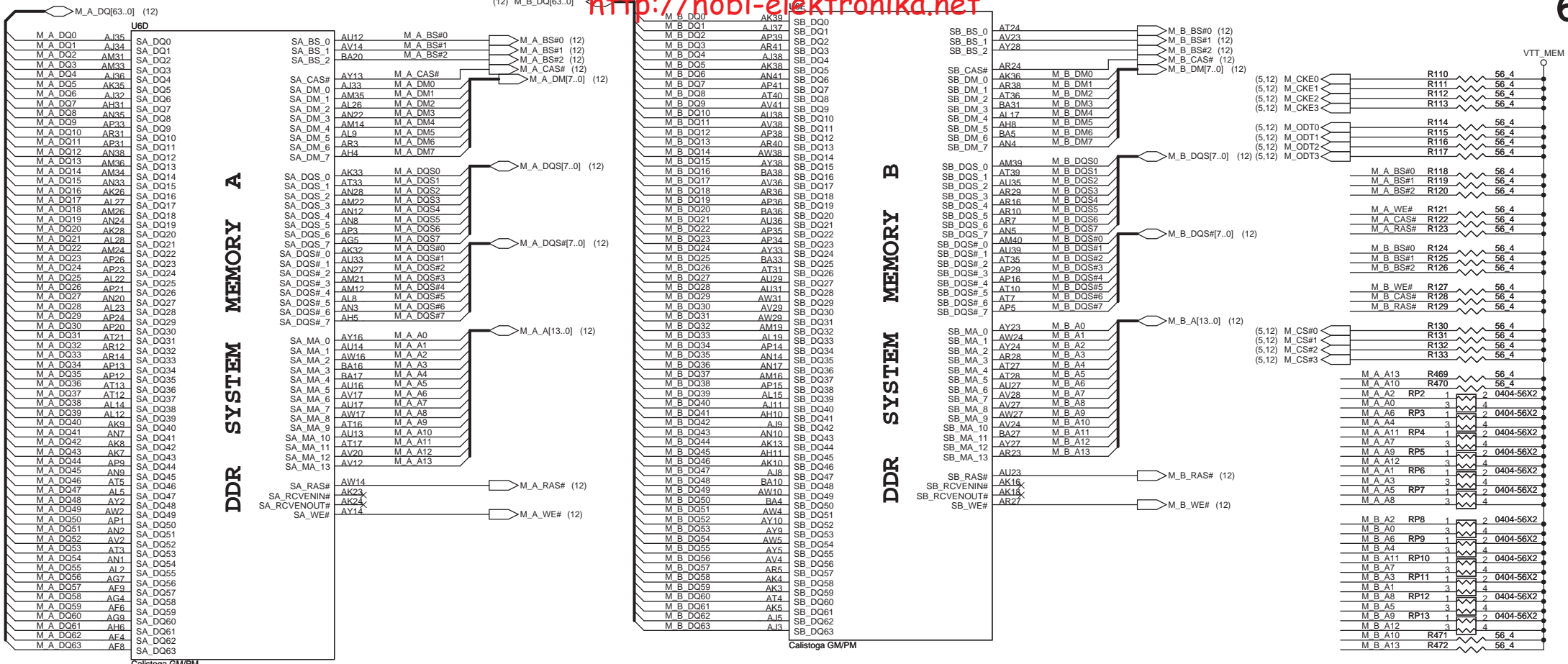
**QUANTA COMPUTER**

File: **GMCH HOST1 of 6**

Size: **RJ6 Main Board**

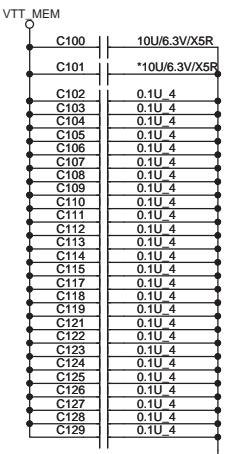
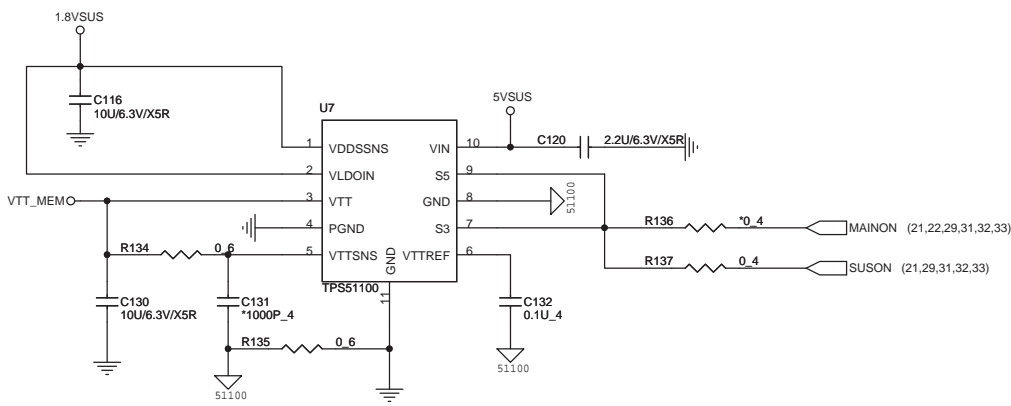
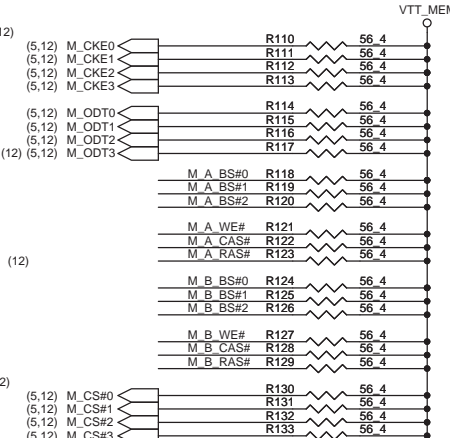
Date: **Wednesday, May 03, 2006** Sheet **5** of **40** Rev **1B**

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DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B



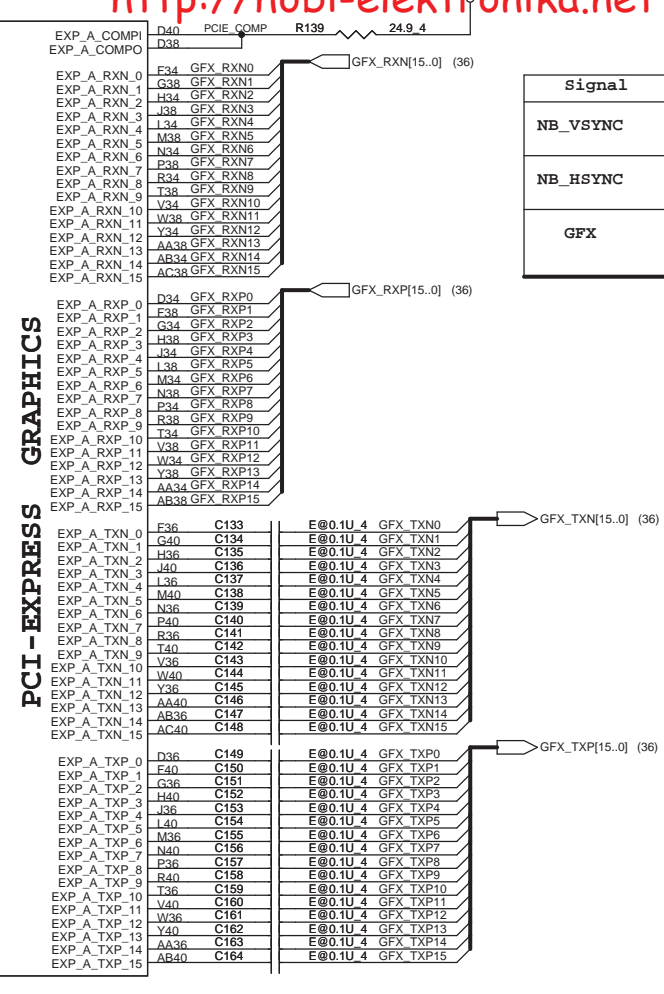
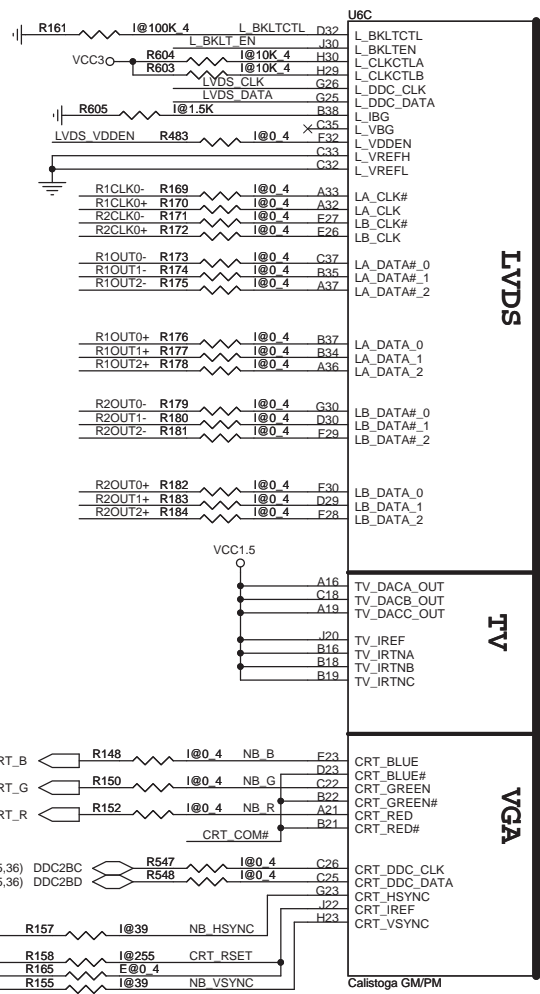
**QUANTA COMPUTER**

GMCH DDR II 2 of 6

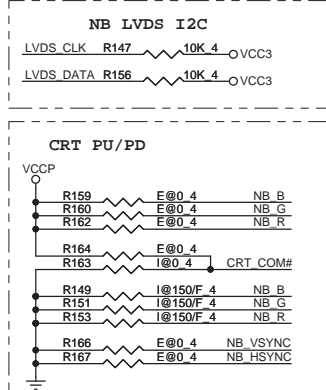
Size: Document Number: RJ6 Main Board Rev 1A

Date: Wednesday, May 03, 2006 Sheet 6 of 40

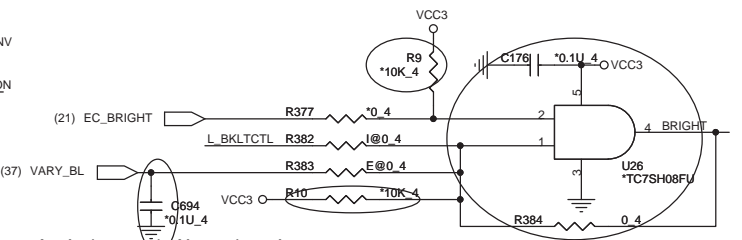
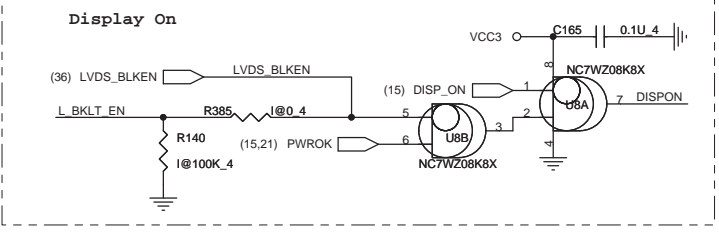
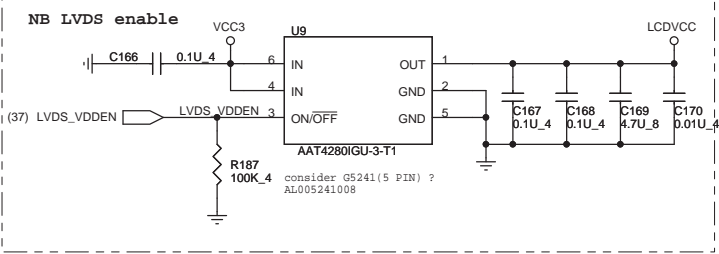
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Signal	945GM	945PM
NB_B	R159 NI	0_4
NB_VSYNC	R155 39_4	NI
NB_HSYNC	R167 NI	0_4
GFX	C133 C164	NI 0.1UF_4



Signal	945GM	945PM
NB_B	R159 NI	0_4
NB_VSYNC	R155 39_4	NI
NB_HSYNC	R167 NI	0_4
GFX	C133 C164	NI 0.1UF_4
CRT_COM#	R164 NI	0_4
L_IBG	R605 1.5K/F_4	
LVDS	R169 0_4	NI
L_BKLT_EN	R140 100K	NI
L_CLKCTLA	R604 10K	
L_CLKCTLB	R603 10K	
LVDS_VDDEN	R483 0_4	NI
DDC2BC	R547 0_4	NI
DDC2BD	R548 0_4	NI
CRT_REST	R158 255	NI
	R165 NI	0



**QUANTA COMPUTER**

File: **GMCH DMI VEDIO 3 of 6**

Size: **RJ6 Main Board**

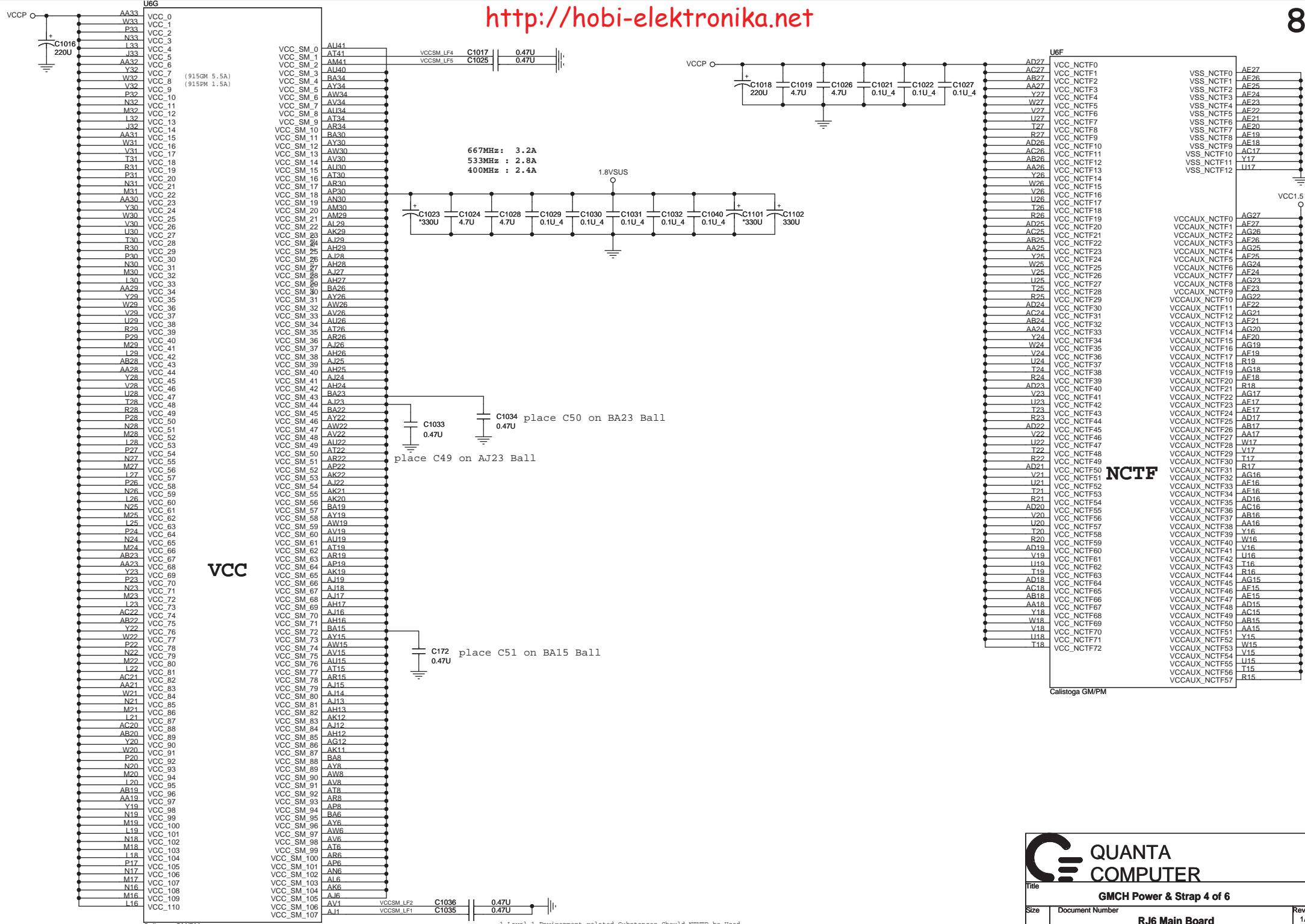
Document Number: **RJ6 Main Board**

Date: **Wednesday, May 03, 2006**

Sheet: **7 of 40**

Rev: **2A**

1. Level 1 Environment-related Substances should NEVER be Used.  
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(915QM 5.5A)  
(915PM 1.5A)

667MHz : 3.2A  
533MHz : 2.8A  
400MHz : 2.4A

place C50 on BA23 Ball  
place C49 on AJ23 Ball

place C51 on BA15 Ball

NCTF

Calistoga GM/PM

**QUANTA COMPUTER**

GMCH Power & Strap 4 of 6

**RJ6 Main Board**

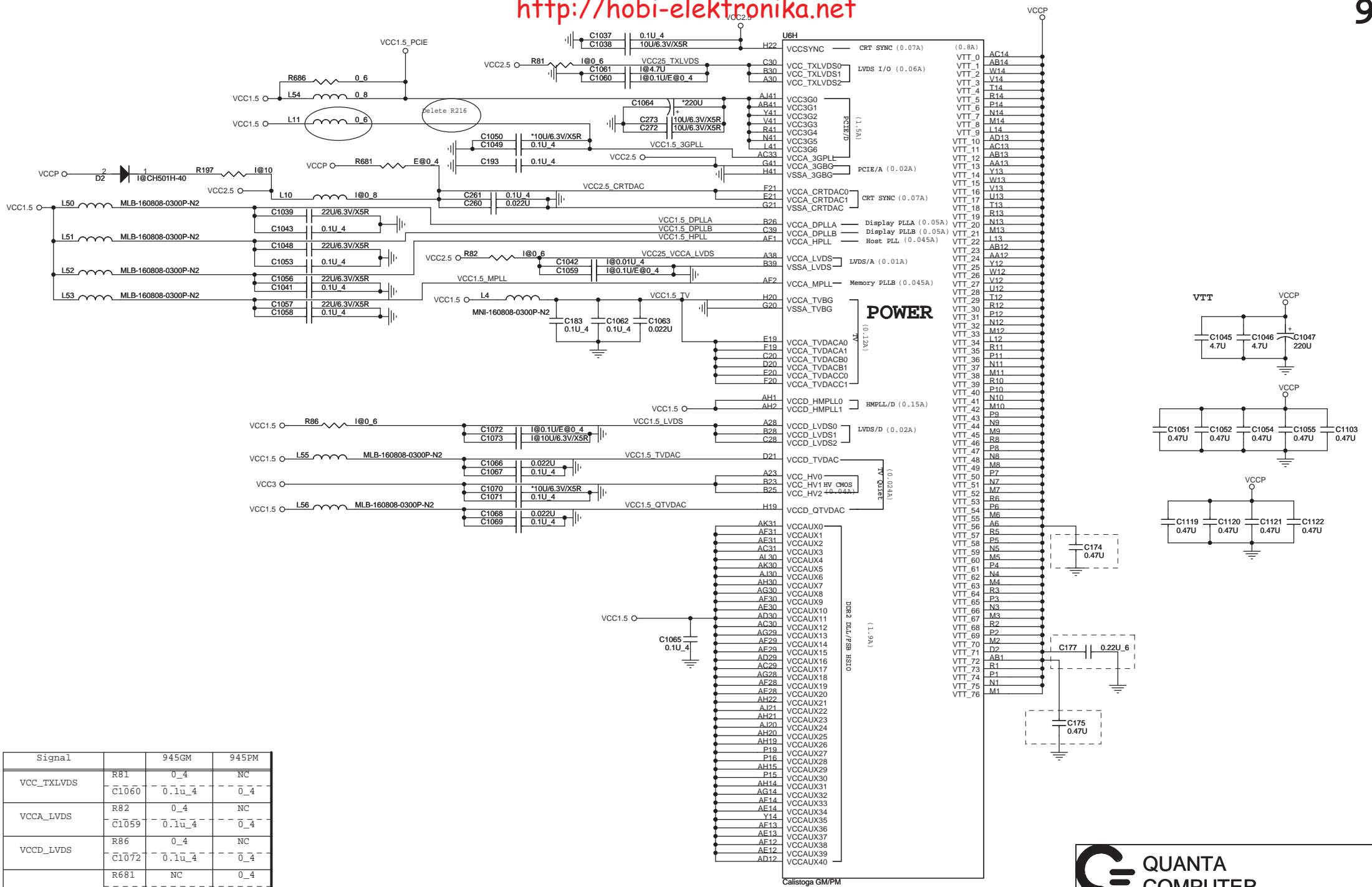
Rev 1A

Wednesday, May 03, 2006

Sheet 8 of 40

1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





Signal	945GM	945PM	
VCC_TXLVDS	R81 C1060	0_4 0_1u_4	NC 0_4
VCCA_LVDS	R82 C1059	0_4 0_1u_4	NC 0_4
VCCD_LVDS	R86 C1072	0_4 0_1u_4	NC 0_4
VCC2.5_CRTDAC	R681 R197 L10 D2	NC I0 MNI-160808-0300P-N2 CH501H-40	0_4 NC NC NC

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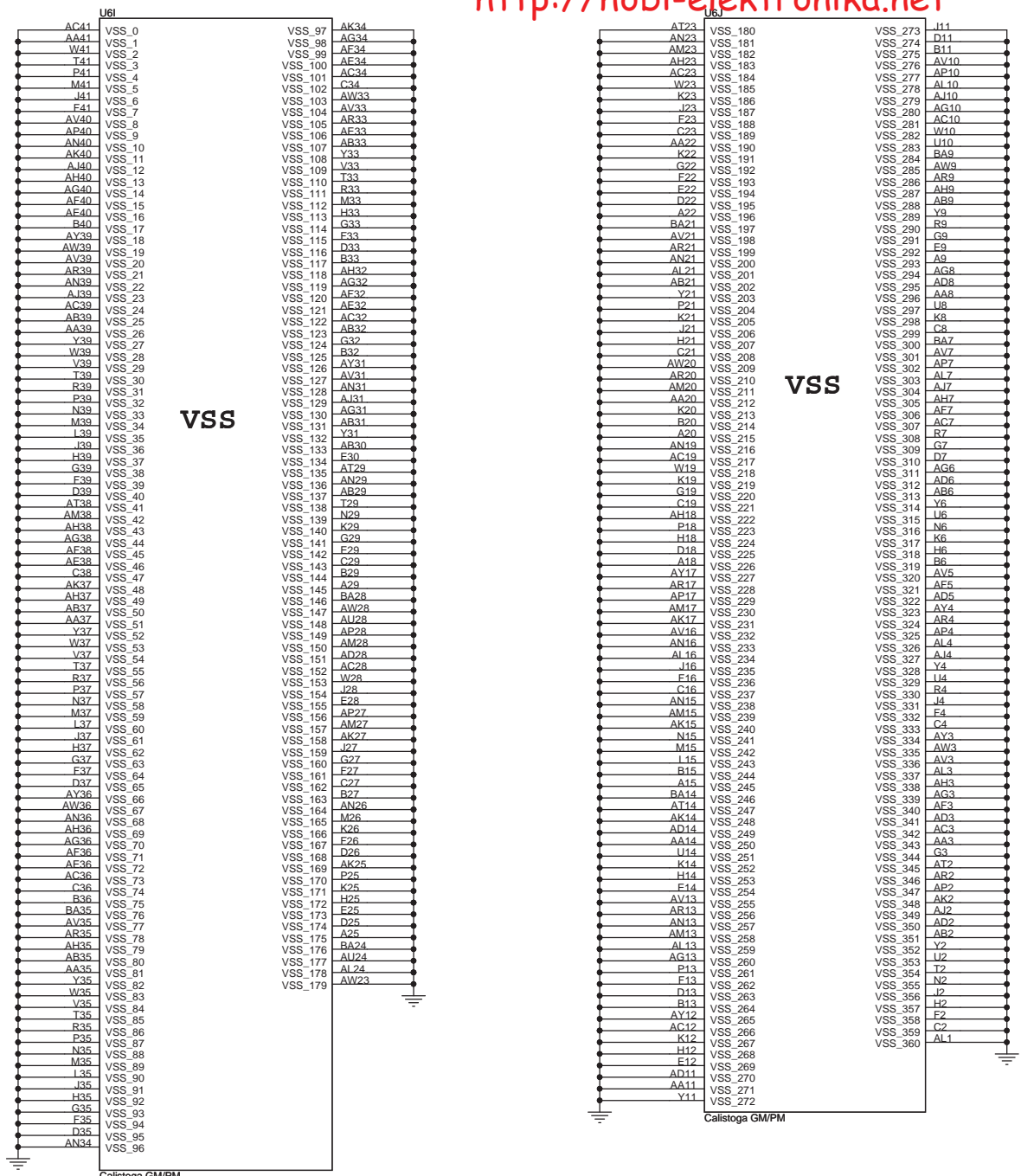
**QUANTA COMPUTER**

GMCH Power 2.5 of 6

Rev 2A

Document Number: RJ6 Main Board

Date: Wednesday, May 03, 2006 Sheet 9 of 40



Callistoga GM/PM

Callistoga GM/PM

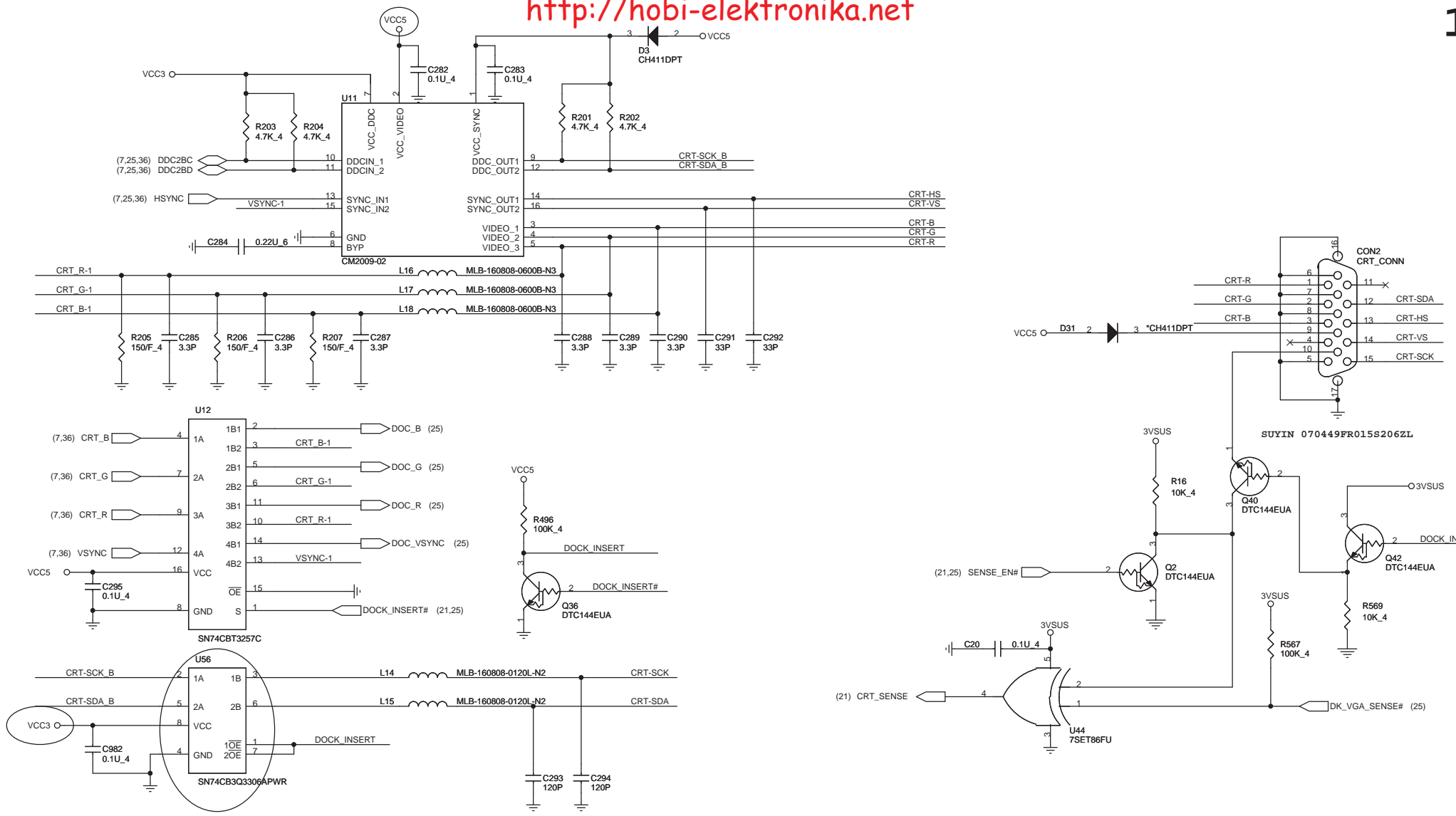
1.Level 1 Environment-related Substances should NEVER be Used.  
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**QUANTA COMPUTER**

Title: **GMCH GND 6 of 6**

Size: Document Number **RJ6 Main Board** Rev 1A

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SN74CBT3257

OE	S	1A
H	H	L
H	L	H
L	H	H
L	L	L

	SENSE_EN#	MB CRT	DOCK CRT	DOCK DVI	CRT_SENSE
All no Plug	L	H	H	L	L
MB CRT Plug	L	L	H	L	H
DOCK CRT Plug	L	H	L	L	H
DOCK DVI Plug	L	H	H	H	H
SENSE EN	H	X	X	X	L
DOCK CRT/DVI Plug	L	H	L	H	L
DOCK CRT/MB CRT Plug	L	L	L	L	L

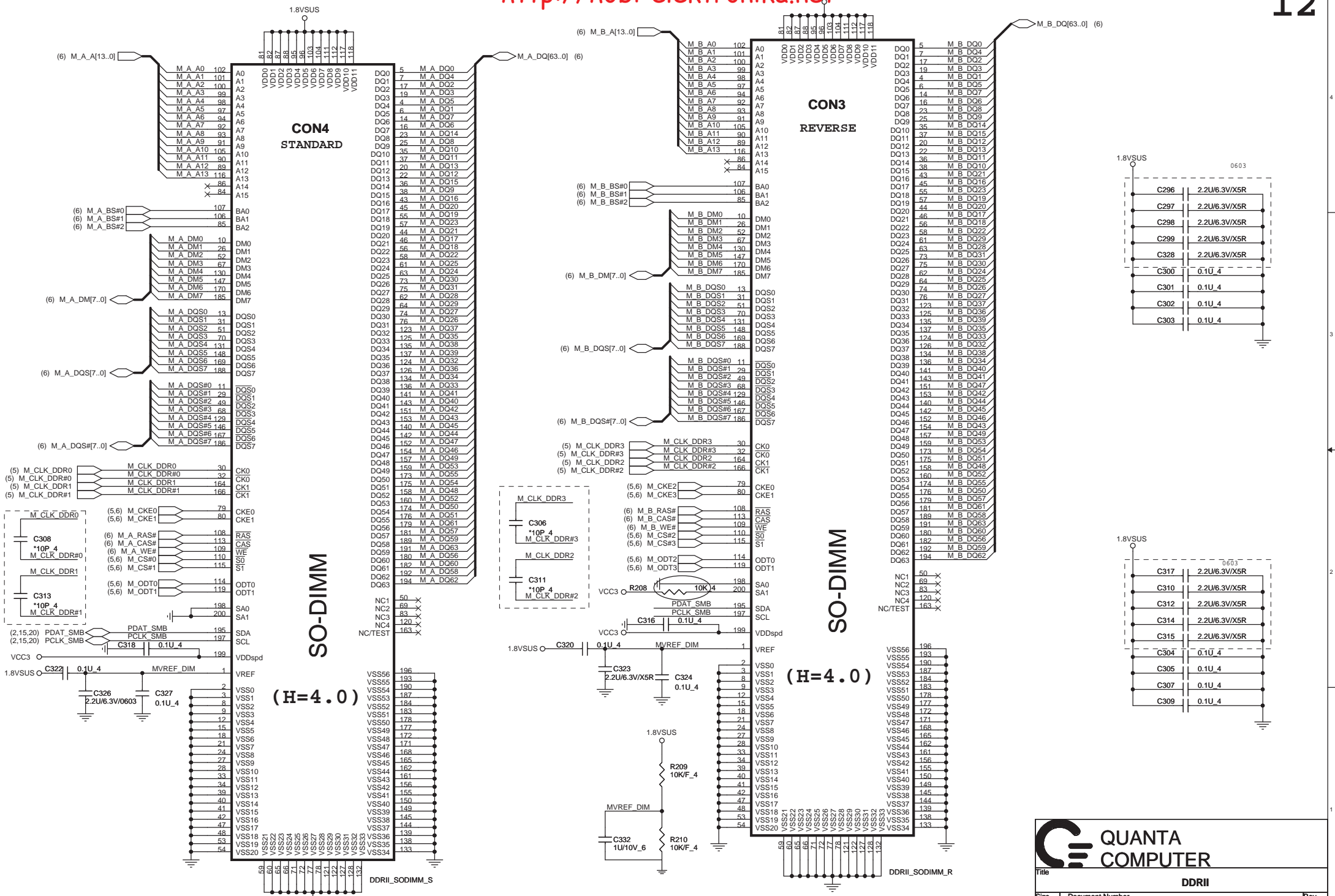
1. Level 1 Environment-related Substances Should NEVER be Used.  
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**QUANTA COMPUTER**

Title: **CRT**

Size: Document Number **RJ6 Main Board** Rev **2A**

Date: Wednesday, May 03, 2006 Sheet 11 of 40



**QUANTA COMPUTER**

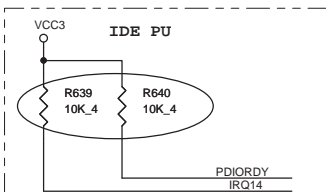
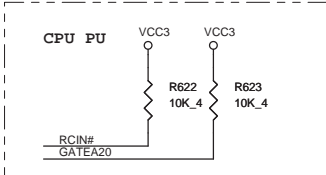
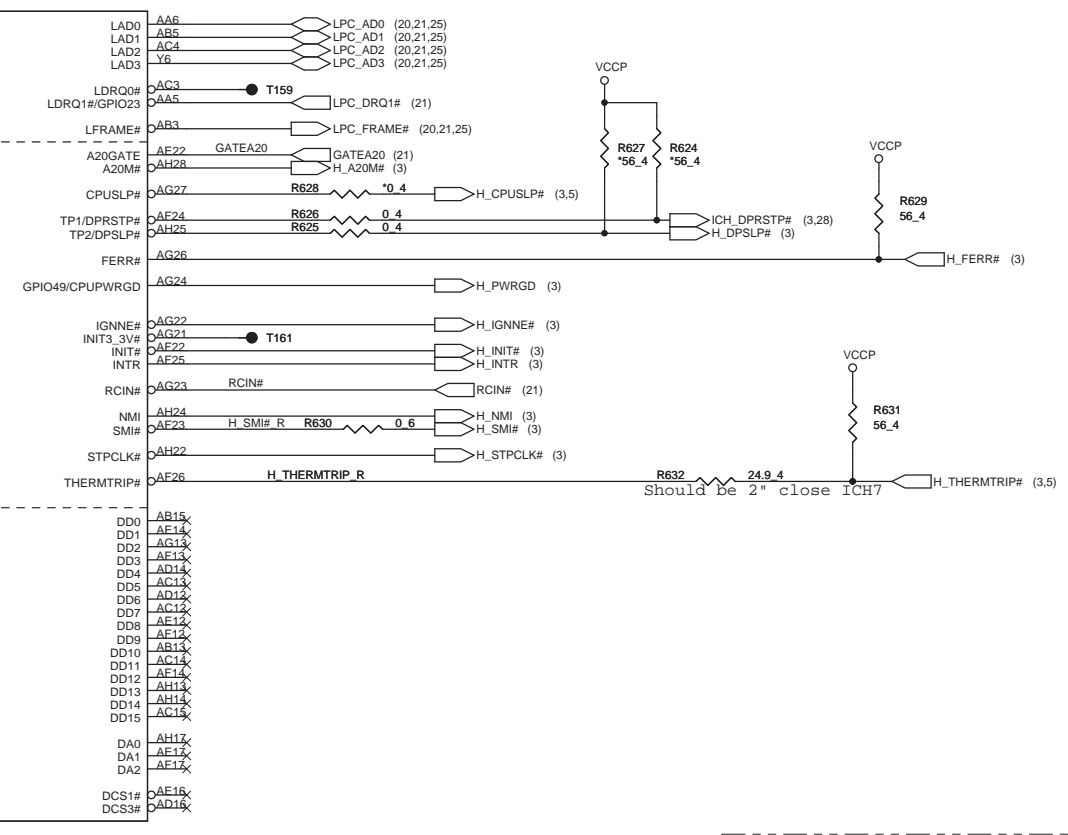
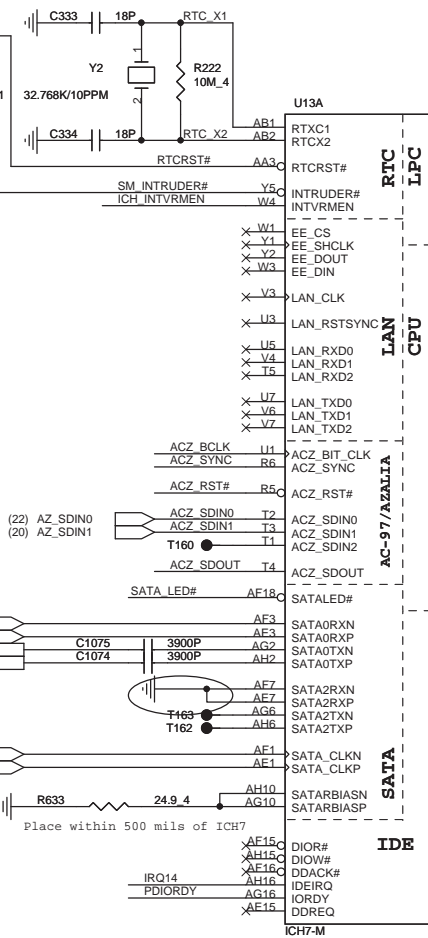
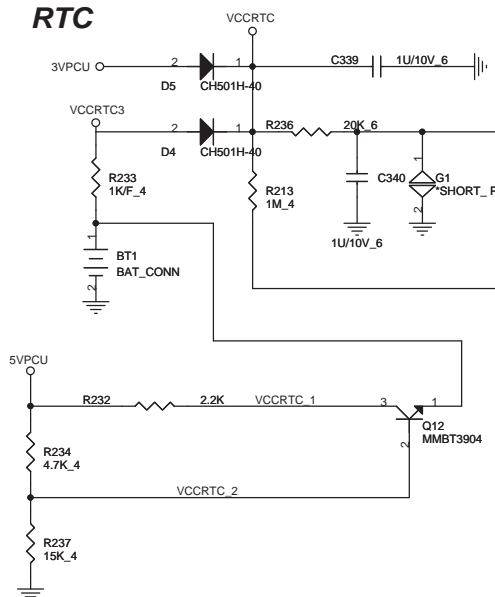
Title: **DDRII**

Size: Document Number: **RJ6 Main Board** Rev: 2A

Date: Tuesday, May 09, 2006 Sheet: 12 of 40

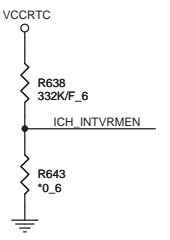
1.Level 1 Environment-related Substances Should NEVER be Used.  
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RTC

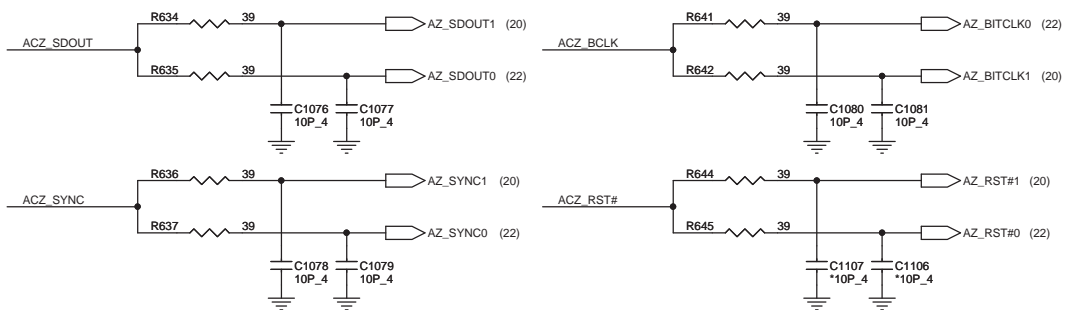


ICH7 internal VR enable strap

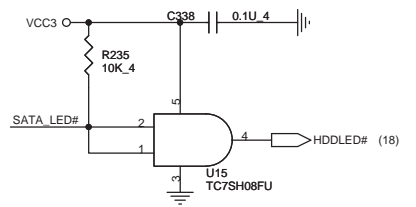
	INTVRMEN
Enable (default)	1
Disable	0



HD Audio to Codec and Modem



SATA LED



**QUANTA COMPUTER**

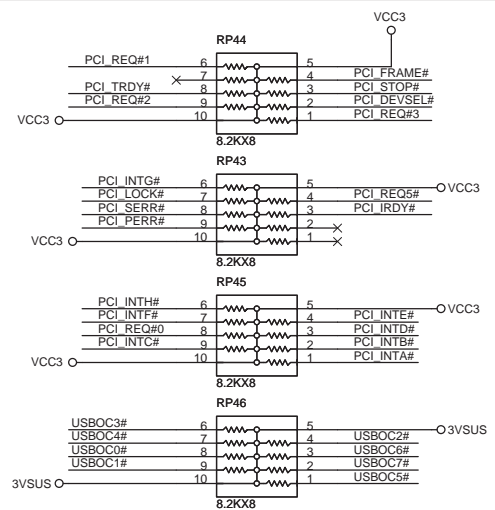
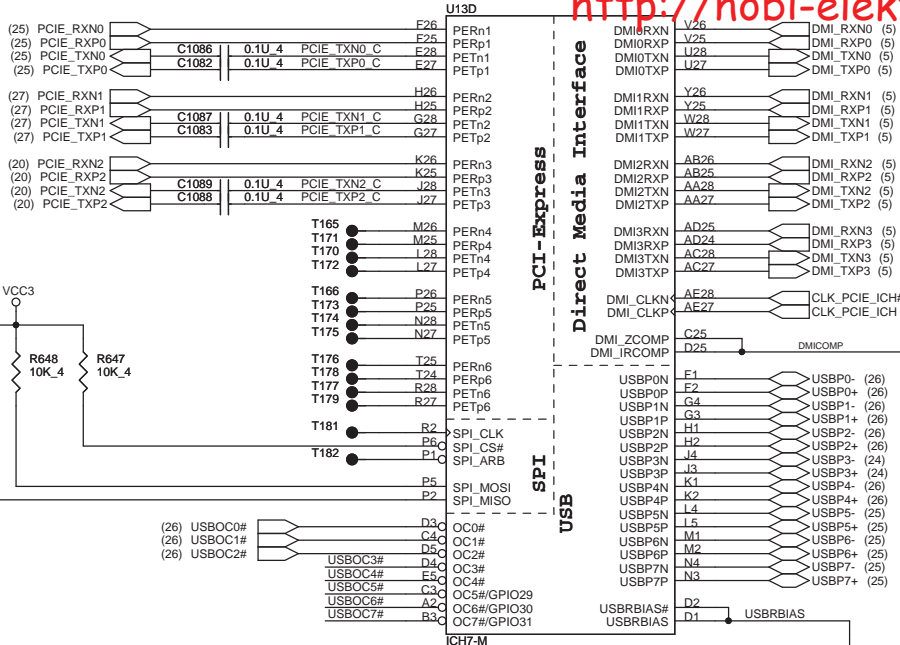
Title: **ICH7-M HOST1 of 4**

Size: Document Number **RJ6 Main Board** Rev 2A

Date: Wednesday, May 03, 2006 Sheet 13 of 40

1. Level 1 Environment-related Substances Should NEVER be Used.  
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Docking  
Giga LAN  
MINI PCIE

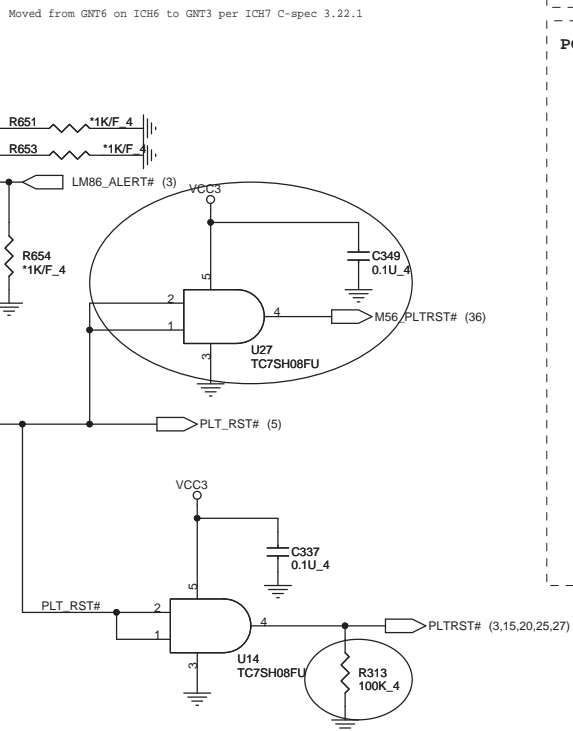
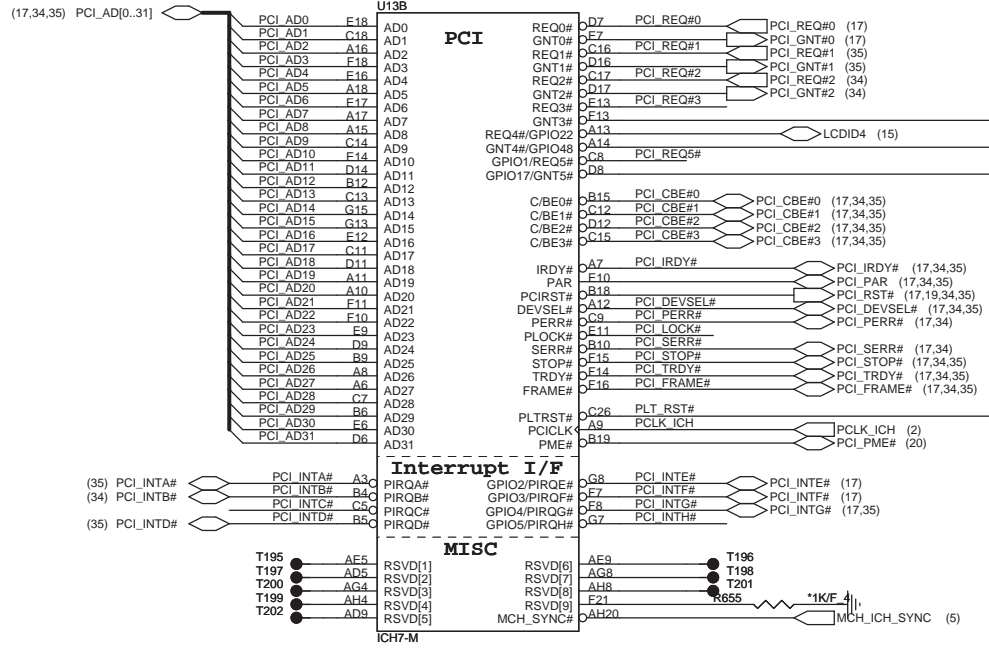


ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

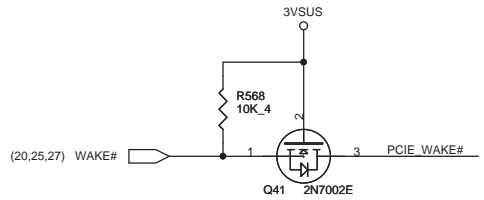
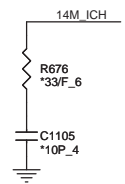
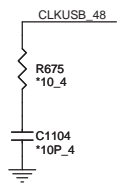
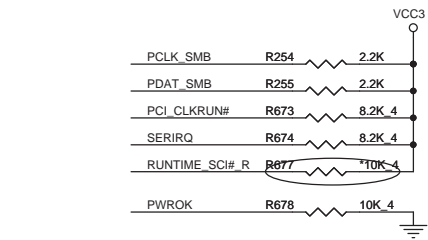
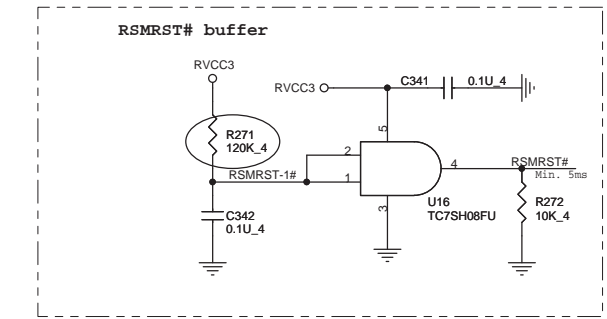
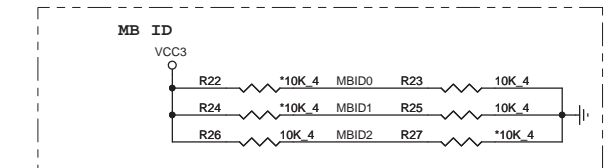
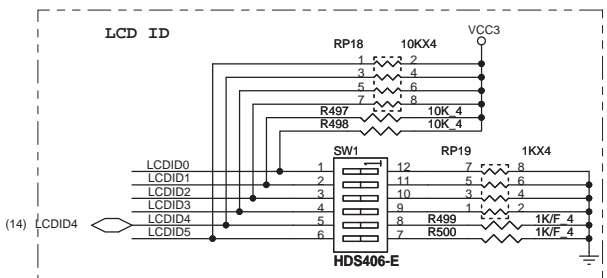
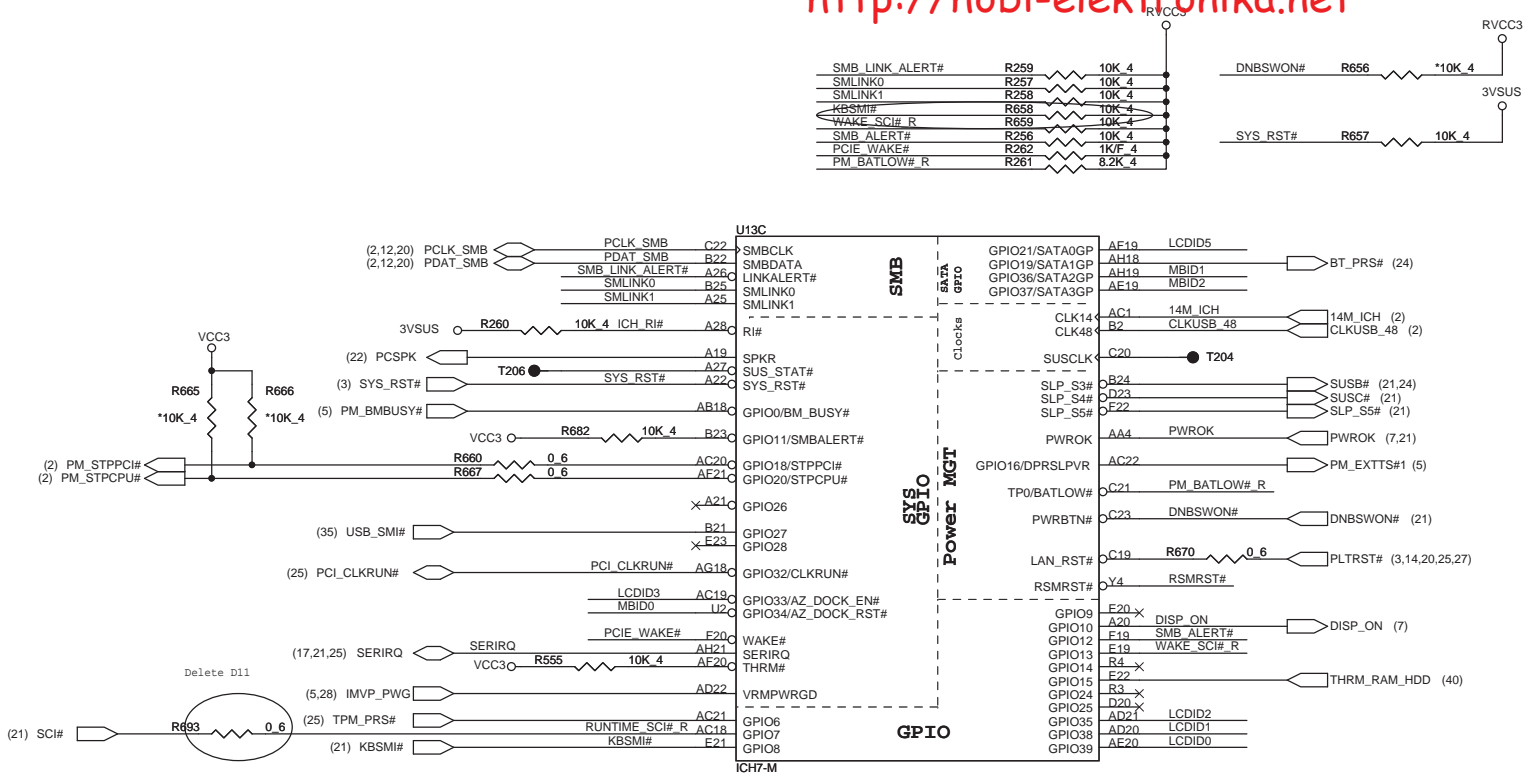
PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	PIRQ E/F/G
SI1512	AD28	REQ2# / GNT2#	PIRQ B
VT6212	AD27	REQ1# / GNT1#	PIRQ A/D/G
Interrupts	PCI DEVICE		
PIRQA	USB UHCI controller1, 4	VT6212	
PIRQB	Audio and Modem ; option for SMBus	SI1512	
PIRQC	USB UHCI controller3 ; SATA/IDE Native Mode		
PIRQD	USB UHCI controller2	VT6212	
PIRQE	INT LAN; option for SCI, TCO, HPET#0,1,2	PCI7411	
PIRQF	option for SCI, TCO, HPET#0,1,2	PCI7411	
PIRQG	option for SCI, TCO, HPET#0,1,2	PCI7411	VT6212
PIRQH	USB EHCI controller; option for SCI, TCO, HPET#0,1,2		



Title		ICHT7-M PCIE 2 of 4	
Size	Document Number	RJ6 Main Board	
Date	Wednesday, May 03, 2006	Sheet	14 of 40

1.Level 1 Environment-related Substances Should NEVER be used.  
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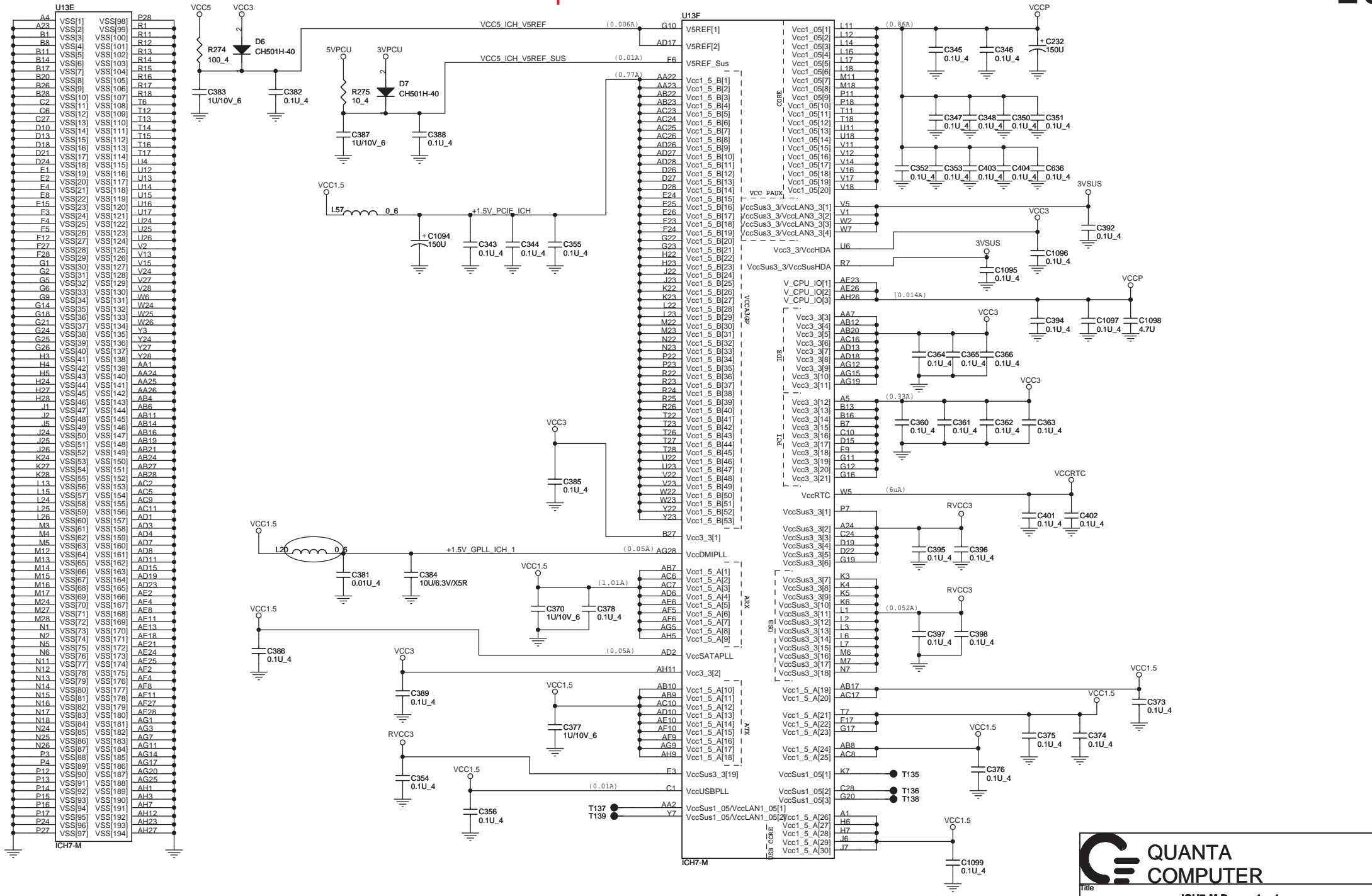
**QUANTA COMPUTER**

Title: **ICH7-M GPIO 3 of 4**

Size: Document Number **RJ6 Main Board** Rev 2A

Date: Tuesday, May 09, 2006 Sheet 15 of 40

1.Level 1 Environment-related Substances Should NEVER be Used.  
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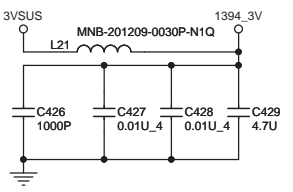
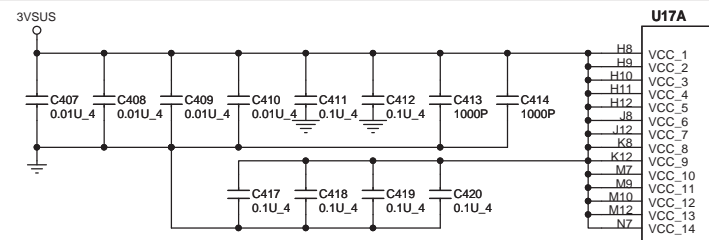
**QUANTA COMPUTER**

ICH7-M Power 4 o 4

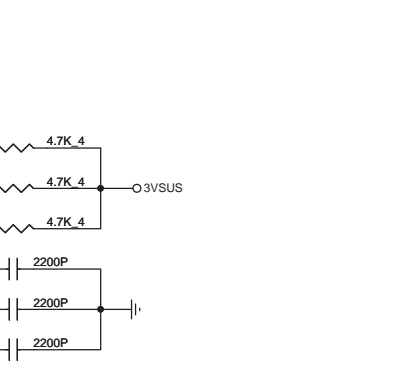
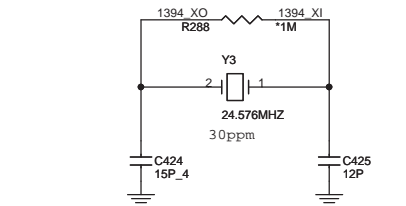
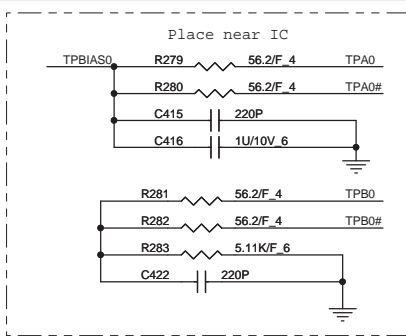
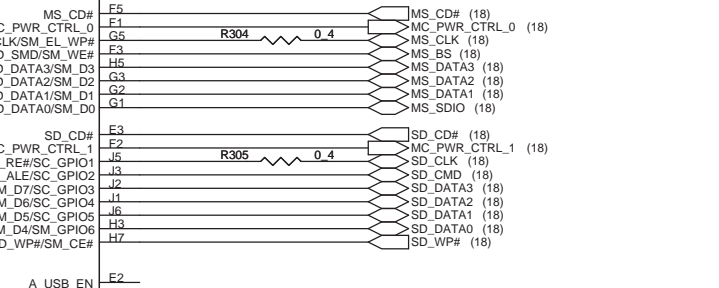
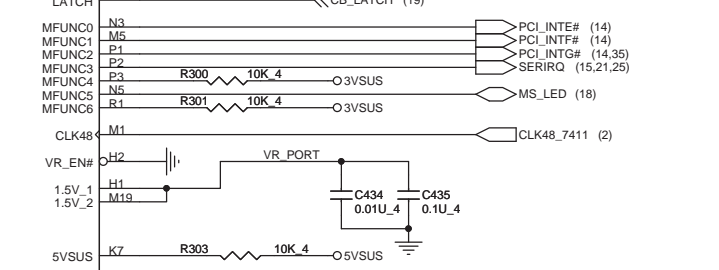
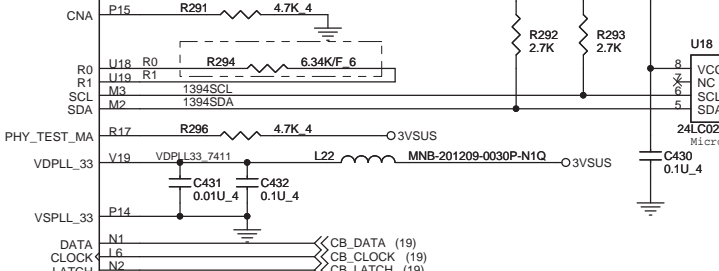
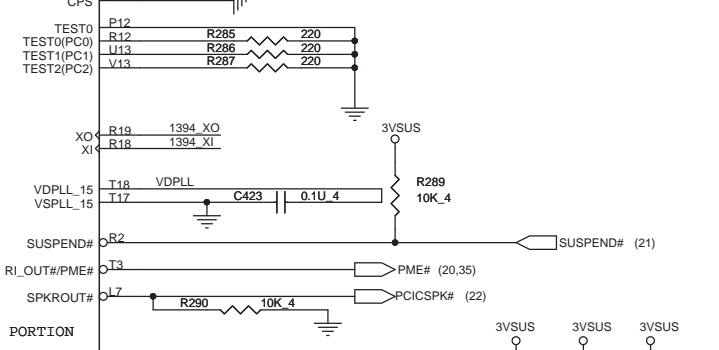
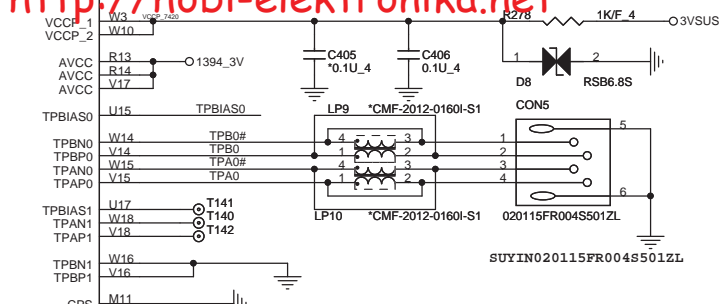
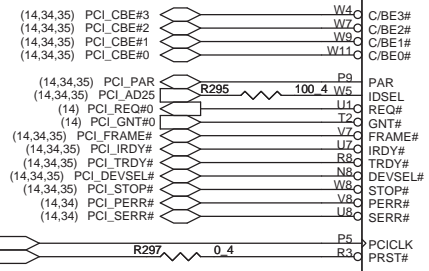
Rev 2A

Wednesday, May 03, 2006





PCI AD31 U2	AD31
PCI AD30 V1	AD30
PCI AD29 V2	AD29
PCI AD28 U3	AD28
PCI AD27 W2	AD27
PCI AD26 V3	AD26
PCI AD25 U4	AD25
PCI AD24 V4	AD24
PCI AD23 V5	AD23
PCI AD22 U5	AD22
PCI AD21 R6	AD21
PCI AD20 R6	AD20
PCI AD19 W6	AD19
PCI AD18 V6	AD18
PCI AD17 U6	AD17
PCI AD16 R7	AD16
PCI AD15 V8	AD15
PCI AD14 U8	AD14
PCI AD13 R9	AD13
PCI AD12 N9	AD12
PCI AD11 V10	AD11
PCI AD10 U10	AD10
PCI AD9 R10	AD9
PCI AD8 N10	AD8
PCI AD7 V11	AD7
PCI AD6 U11	AD6
PCI AD5 R11	AD5
PCI AD4 W12	AD4
PCI AD3 V12	AD3
PCI AD2 U12	AD2
PCI AD1 N11	AD1
PCI AD0 W13	AD0



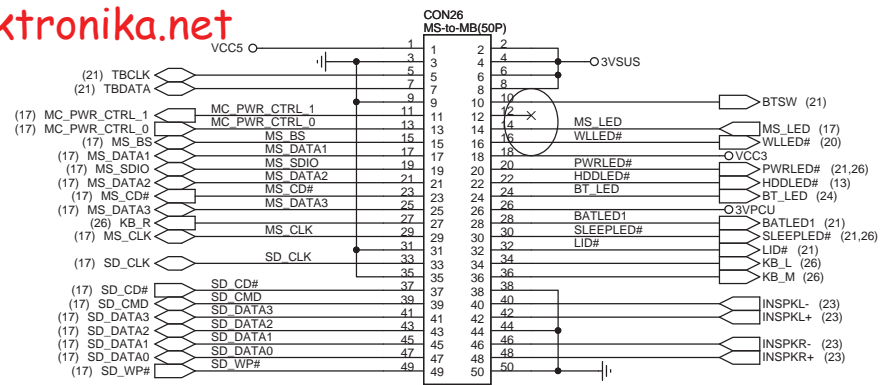
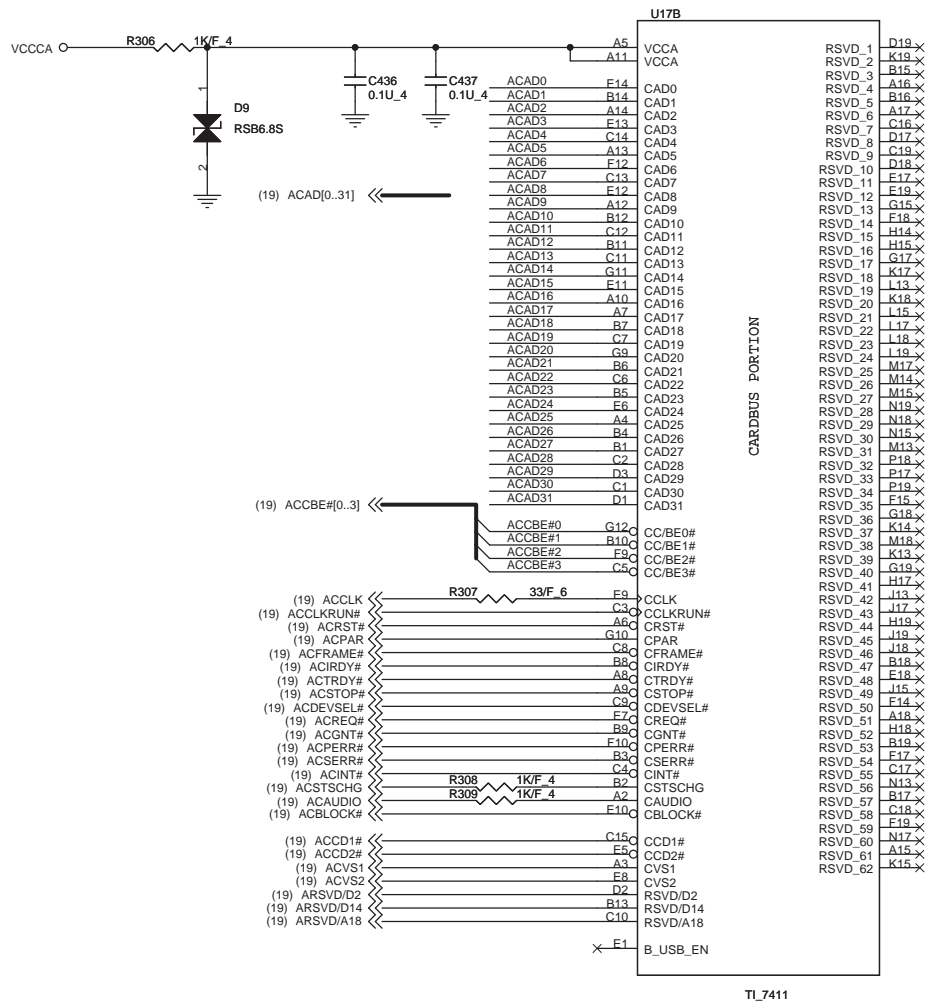
**QUANTA COMPUTER**

Title: **TI-7411 CardBus Control - A**

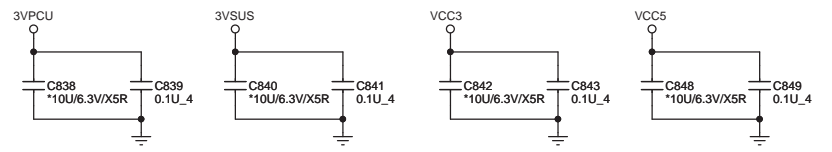
Size: Document Number **RJ6 Main Board** Rev 1A

Date: Tuesday, May 09, 2006 Sheet 17 of 40

1. Level 1 Environment-related Substances Should NEVER be Used.  
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ACBS 88078-050xx-50p-ruv



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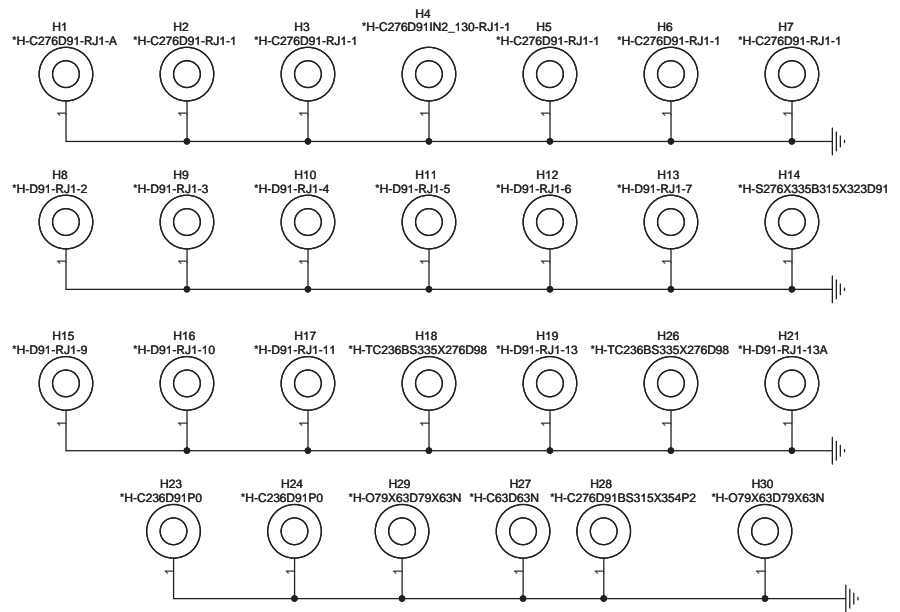
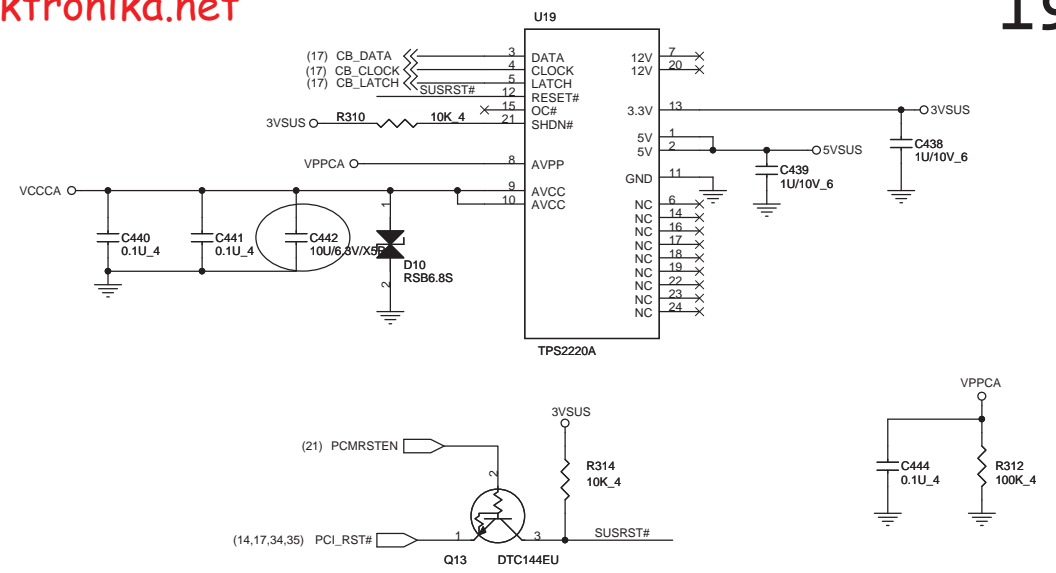
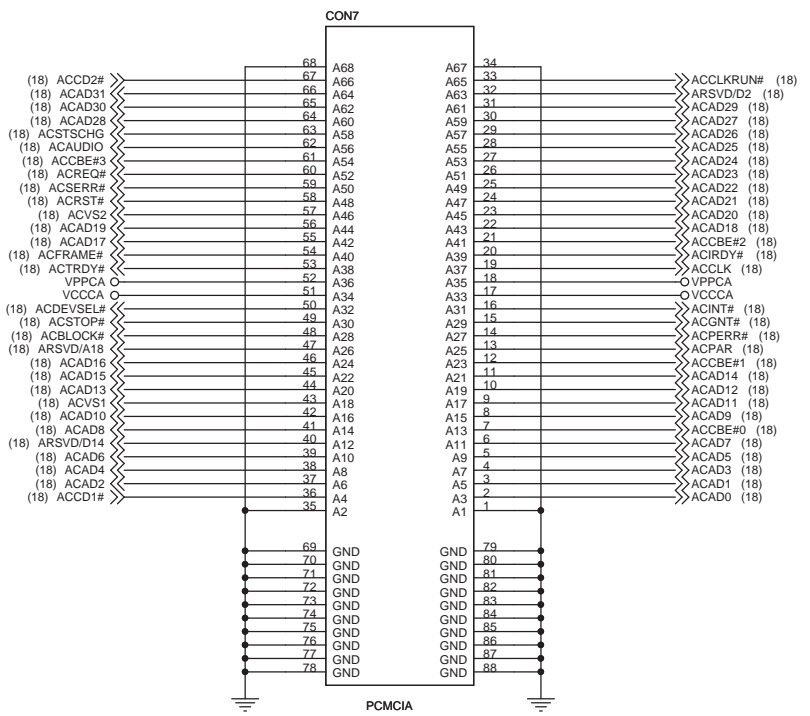
**QUANTA COMPUTER**

Title: **TI-7411 CardBus Control -- B**

Size: Document Number **RJ6 Main Board** Rev **2A**

Date: Tuesday, May 09, 2006 Sheet 18 of 40

(18) ACAD[0..31] <<<
(18) ACCBE#[0..3] <<<

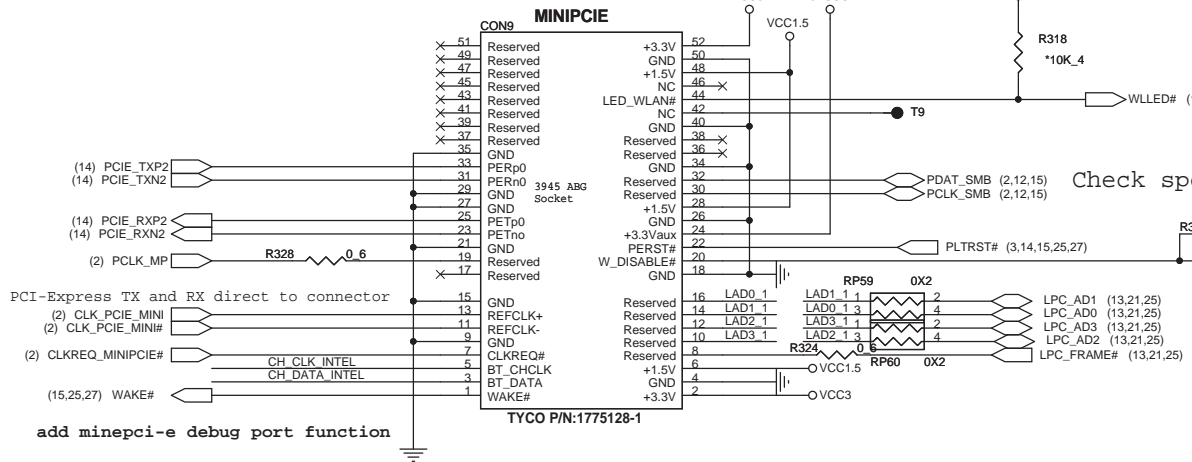
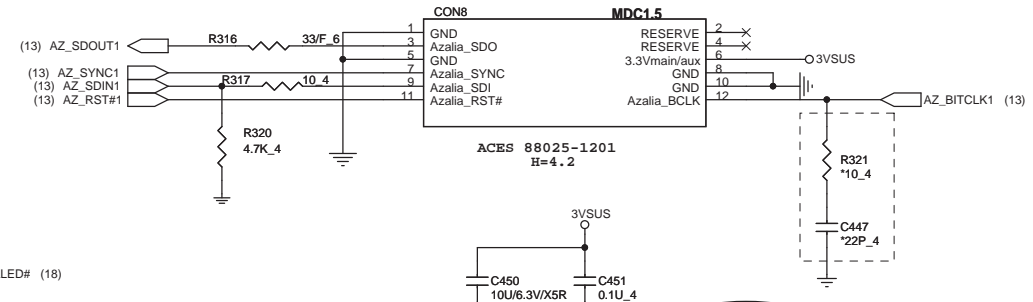


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QUANTA COMPUTER
Title: CARDBUS SLOT
Size: Document Number
Date: Tuesday, May 09, 2006
Sheet: 19 of 40
Rev: 1A

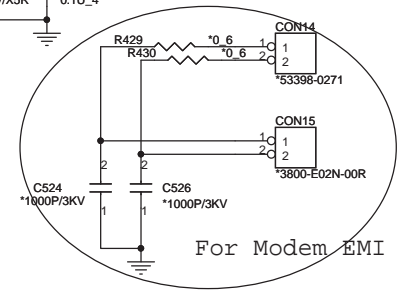
LED\_GP : LED WLEN LINK  
Output Current : 7mA  
Blink rate : 1 flash per every 3 sec.

WLSW:  
Low : disable the radio.  
High : Enable the radio.

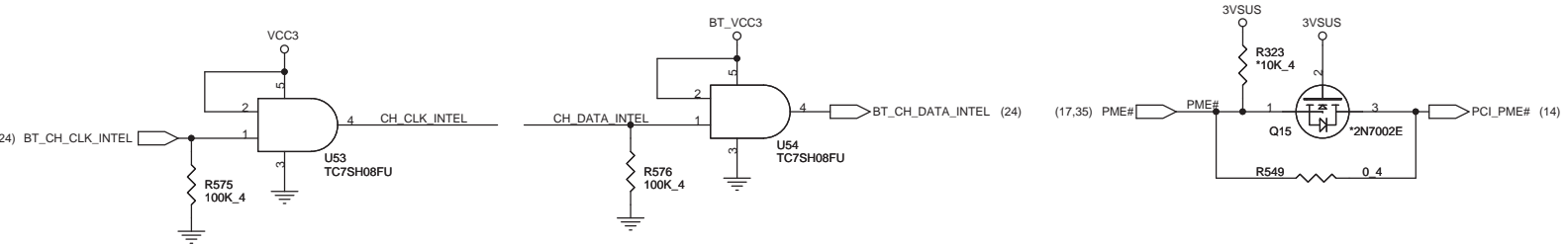
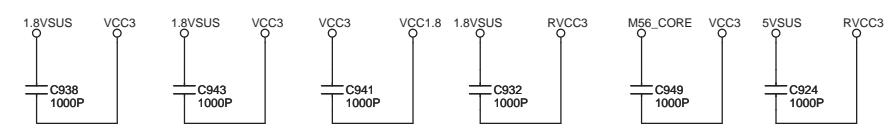
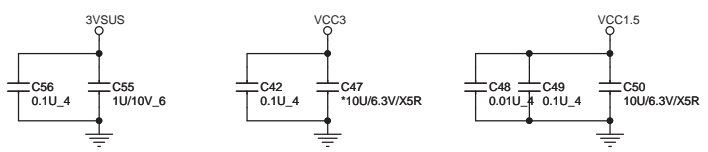
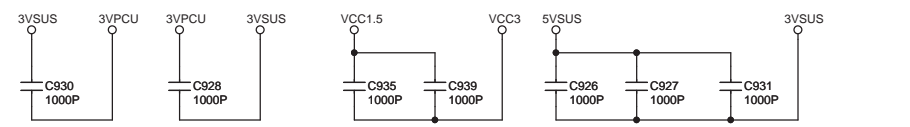
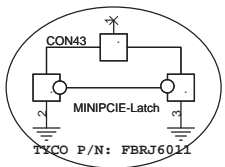


Check spec, which power used

Need Check

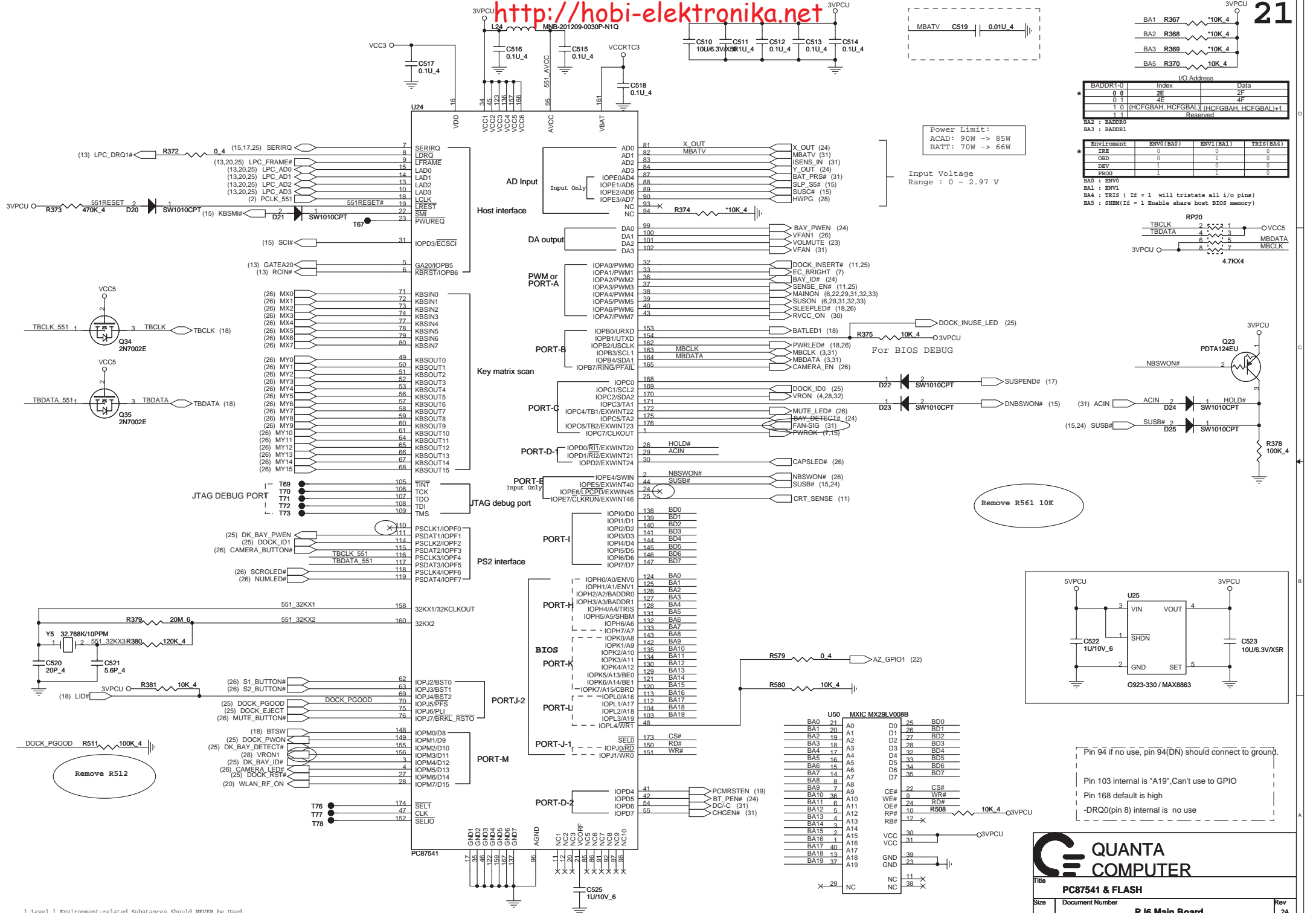


For Modem EMI



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QUANTA COMPUTER  
Title: MINIPICIE / MDC  
Size: Document Number Rev 2A  
RJ6 Main Board  
Date: Wednesday, May 03, 2006 Sheet 20 of 40



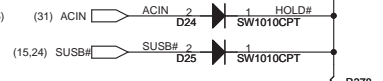
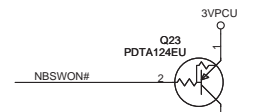
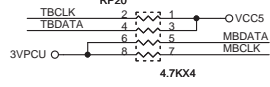
Power Limit:  
ACAD: 90W -> 85W  
BATT: 70W -> 66W

Input Voltage  
Range : 0 - 2.97 V

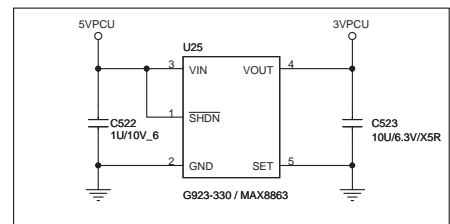
BADDR1-0	Index	Data
0 0	2E	2F 0
0 1	4E	4F 0
1 0 (HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)	1 1
1 1	Reserved	

Environment	ENV0(BA0)	ENV1(BA1)	TRIS(BA4)
TRIS	0	0	0
OSD	0	1	0
DEV	1	0	0
PROG	1	1	0

BA0 : ENV0  
BA1 : ENV1  
BA4 : TRIS ( If = 1 will tristate all i/o pins)  
BA5 : SHEN(If = 1 Enable share host BIOS memory)



Remove R561 10K



Pin 94 if no use, pin 94(DN) should connect to ground.  
Pin 103 internal is "A19", Can't use to GPIO  
Pin 168 default is high  
-DRQ0(pin 8) internal is no use

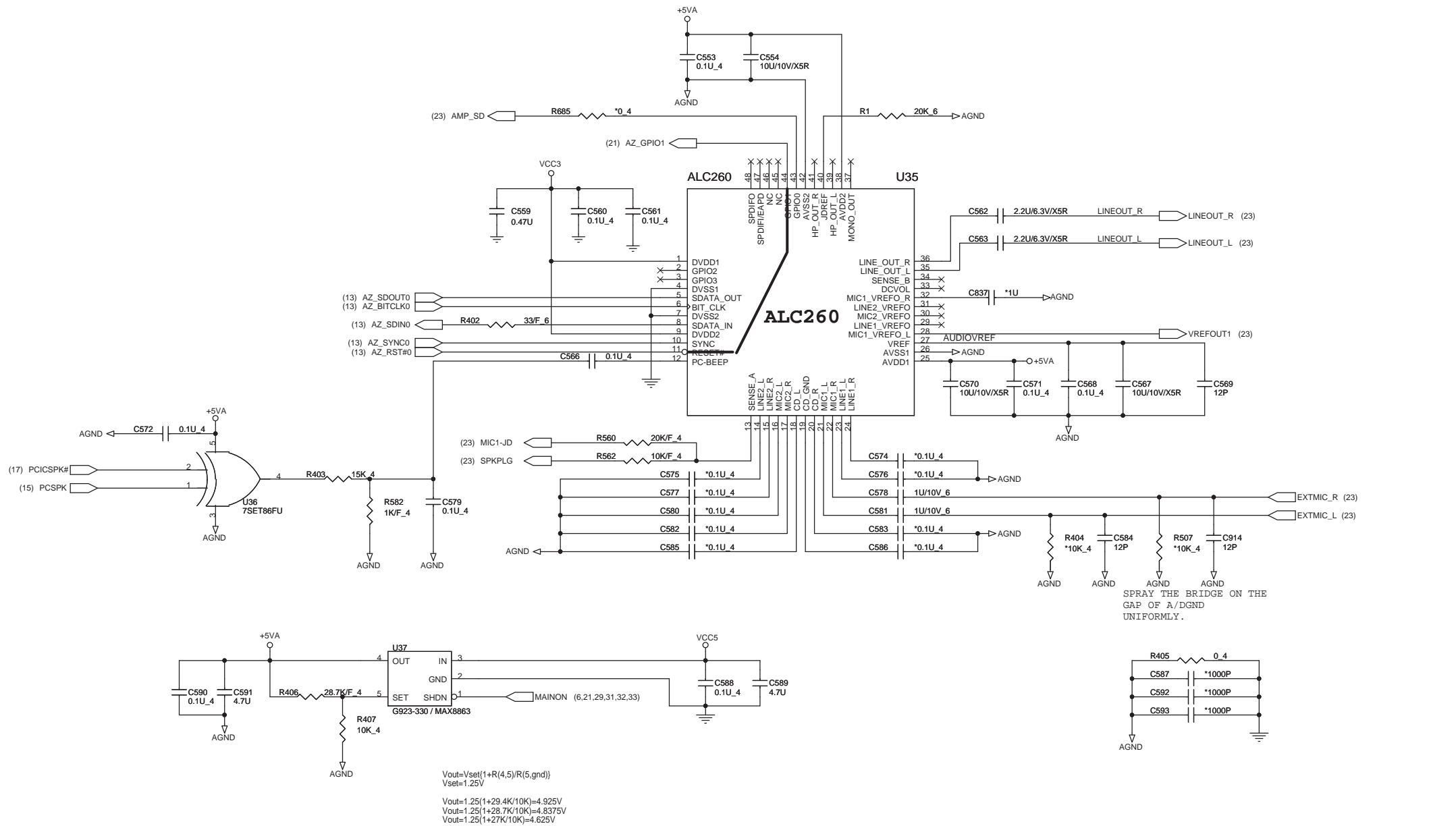
U50 MXIC MX29LV008B

BA0	21	A0	D0	25	BD0
BA1	20	A1	D1	26	BD1
BA2	18	A2	D2	27	BD2
BA3	18	A3	D3	28	BD3
BA4	17	A4	D4	32	BD4
BA5	16	A4	D5	33	BD5
BA6	15	A6	D6	34	BD6
BA7	14	A5	D7	35	BD7
BA8	8	A7			
BA9	7	A8	CE#	22	CS#
BA10	36	A10	WE#	9	WR#
BA11	6	A11	RD#	24	RD#
BA12	5	A11	DC/C#	10	R508
BA13	4	A12	RP#	12	X
BA14	3	A14	RB#	12	X
BA15	2	A15			
BA16	1	A16	VCC	30	3VPCU
BA17	40	A16	VCC	31	
BA18	13	A18	GND	39	
BA19	37	A19	GND	23	
			GND	11	X
			NC	38	X



Title		PC87541 & FLASH	
Size	Document Number	Rev	
		RJ6 Main Board	
Date:	Wednesday, May 03, 2006	Sheet	21 of 40

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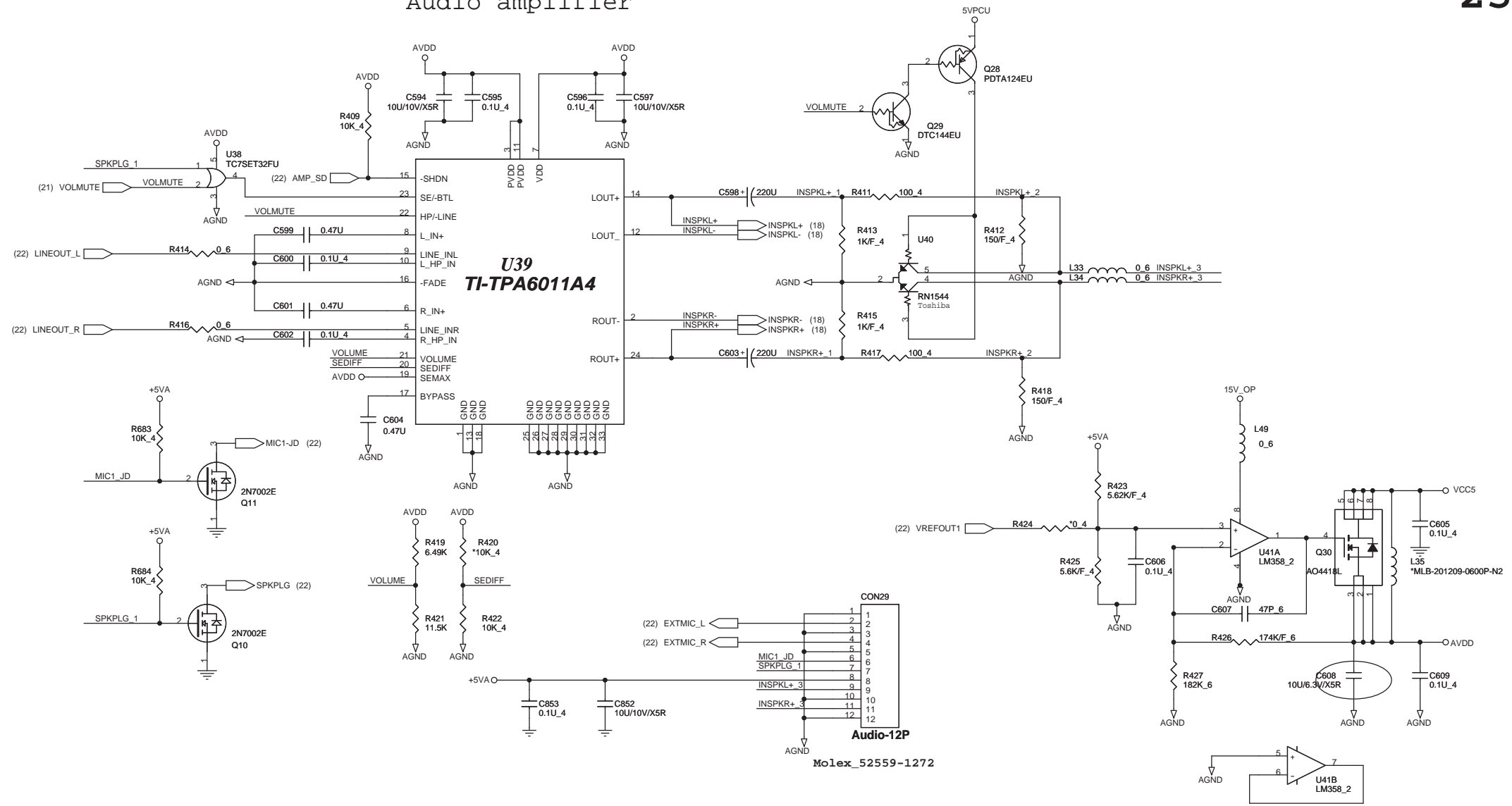
$V_{out} = V_{set} \frac{1+R(4,5)/R(5,gnd)}{1}$   
 $V_{set} = 1.25V$   
 $V_{out} = 1.25 \frac{1+29.4K/10K}{1} = 4.925V$   
 $V_{out} = 1.25 \frac{1+28.7K/10K}{1} = 4.8375V$   
 $V_{out} = 1.25 \frac{1+27K/10K}{1} = 4.625V$

**QUANTA COMPUTER**

Title: **Audio ALC260**

Size	Document Number	Rev
	<b>RJ6 Audio Board</b>	<b>1B</b>
Date:	Tuesday, May 09, 2006	Sheet 22 of 40

1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



R419	FROM	TO	GAIN
	2.85	2.89	8 dB
*	6.49K	2.96	10 dB

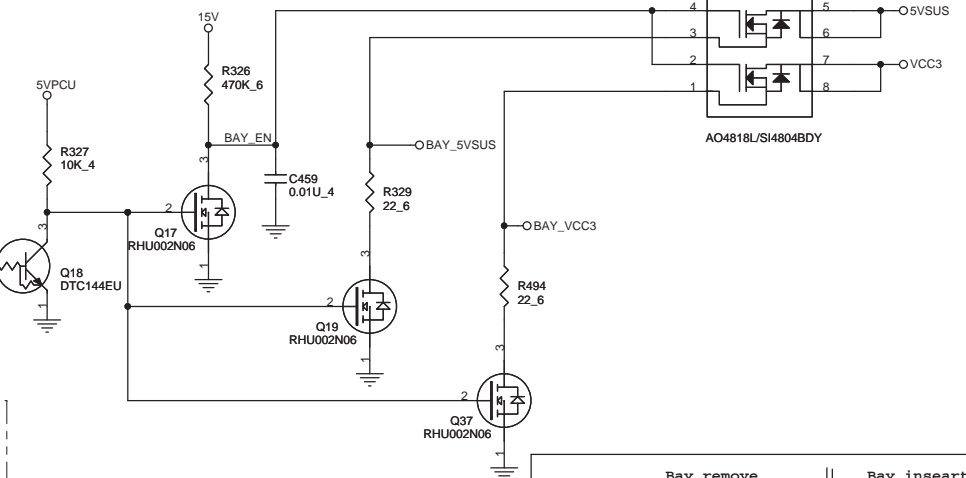
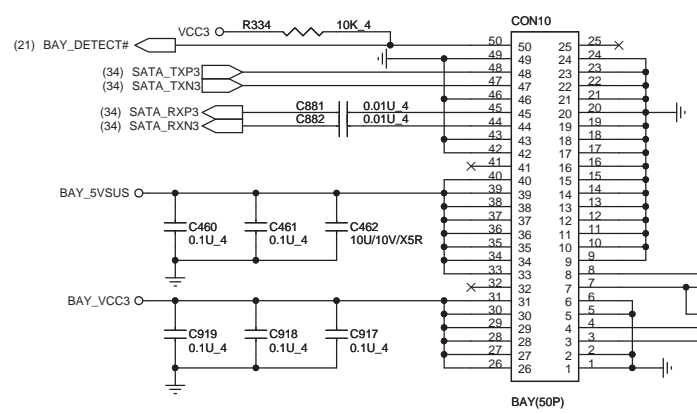
1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

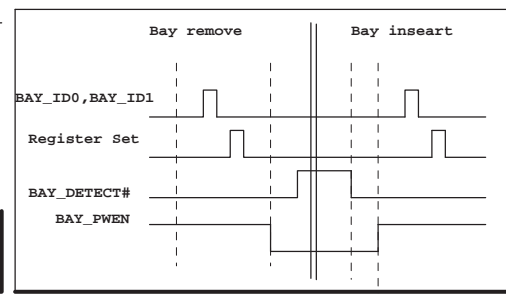
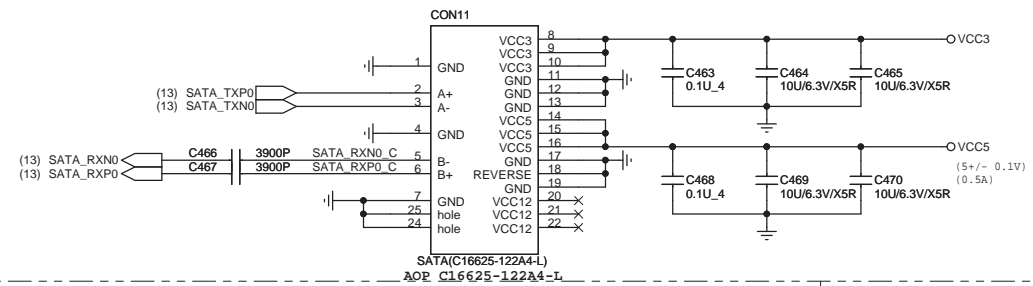
Title: **AUDIO AMP**

Size: Document Number **RJ6 Audio Board** Rev **1B**

Date: Tuesday, May 09, 2006 Sheet 23 of 40

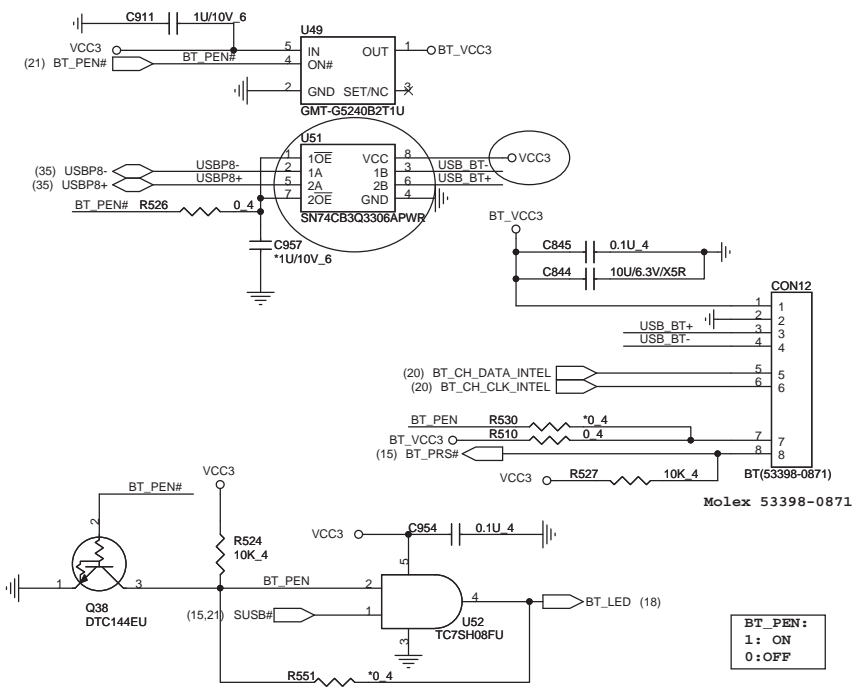


**HDD CONNECTOR**

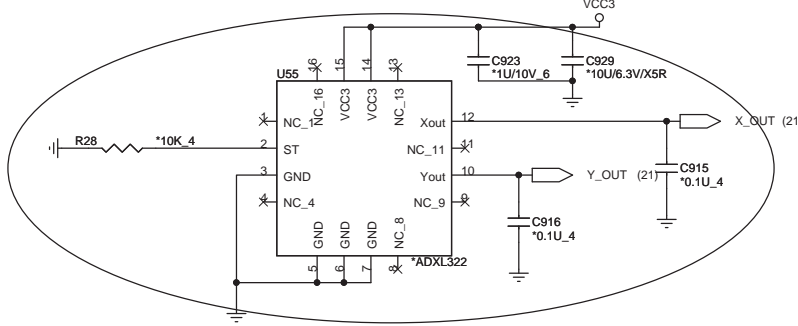


BAY_ID#	
0	SATA Device
1	USB Device

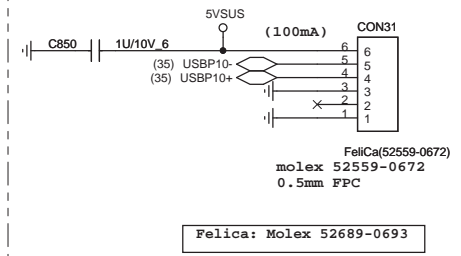
**Bluetooth**



Remove WWAN circuit (con36, R506, D28, D27, C912, C910, C913) (P24)



**FeliCa**



BT\_PEN#:  
 1: ON  
 0: OFF

1. Level 1 Environment-related Substances should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

Document Number: **RJ6 Main Board**

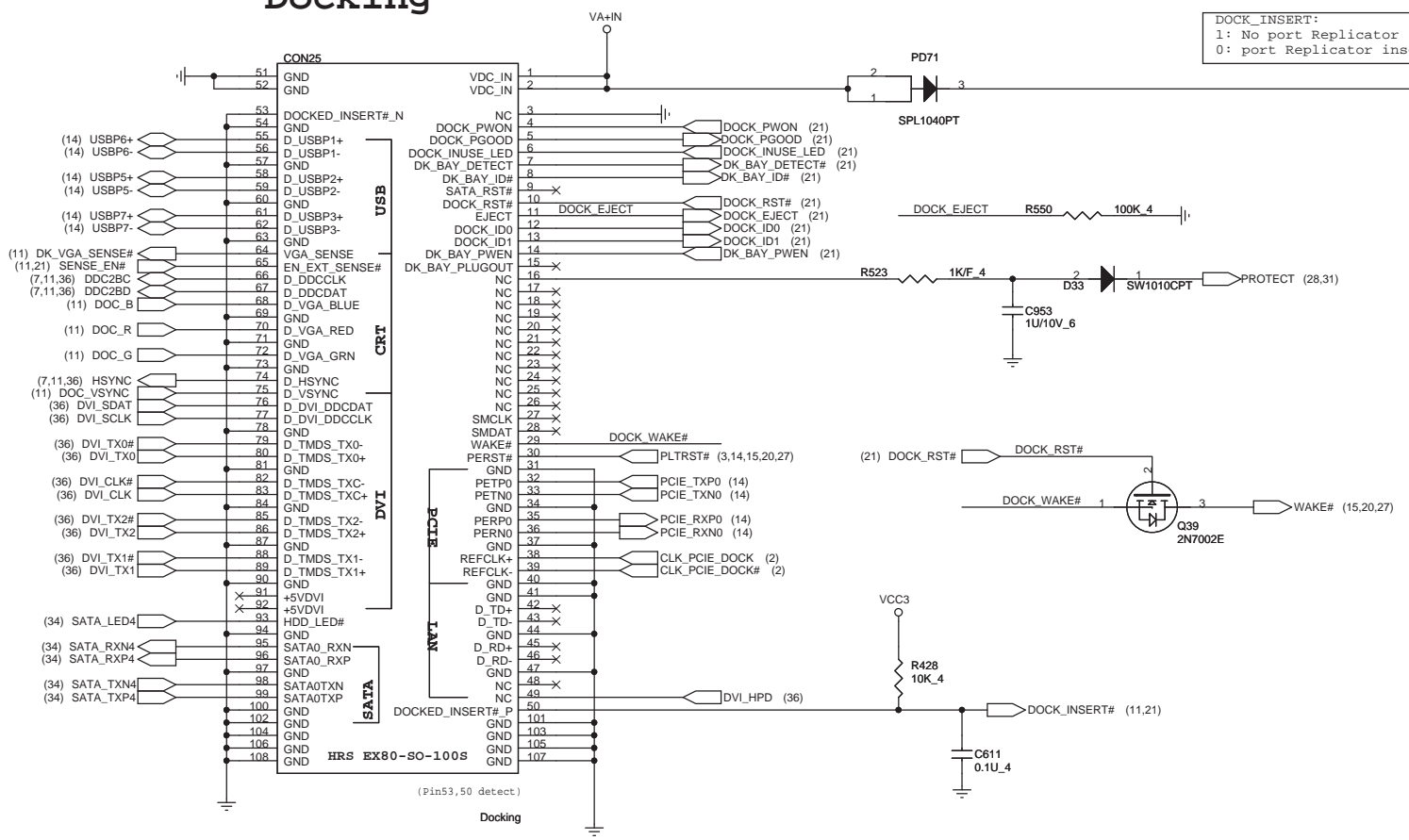
Rev: 2A

Date: Tuesday, May 09, 2006

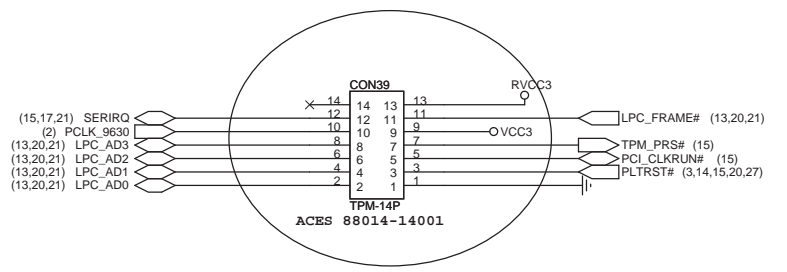
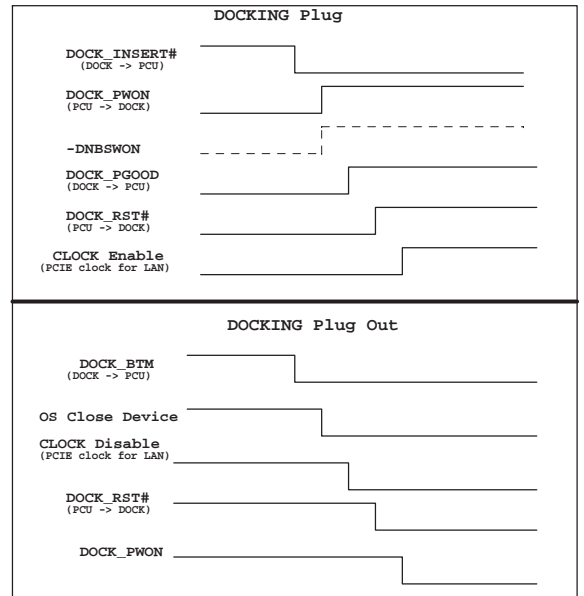
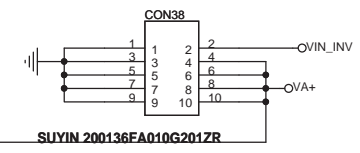
Sheet 24 of 40



# Docking



DOCK\_INSERT:  
1: No port Replicator insert  
0: port Replicator insert



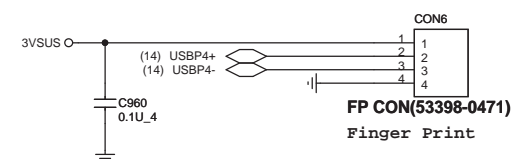
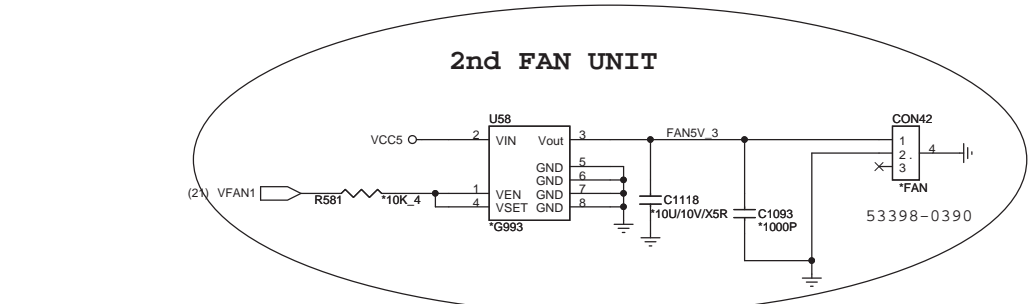
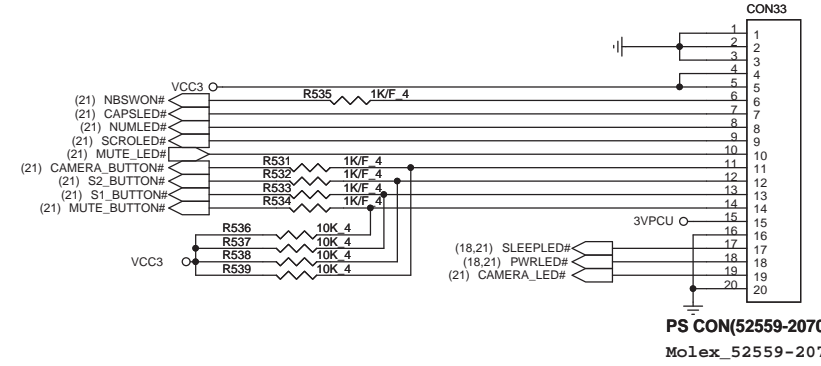
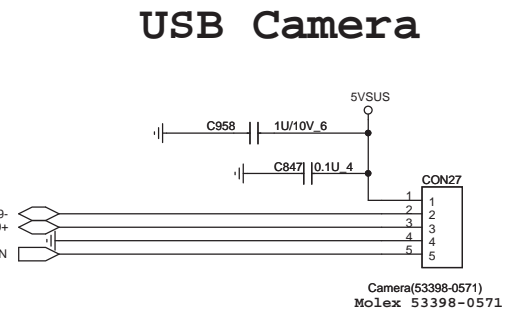
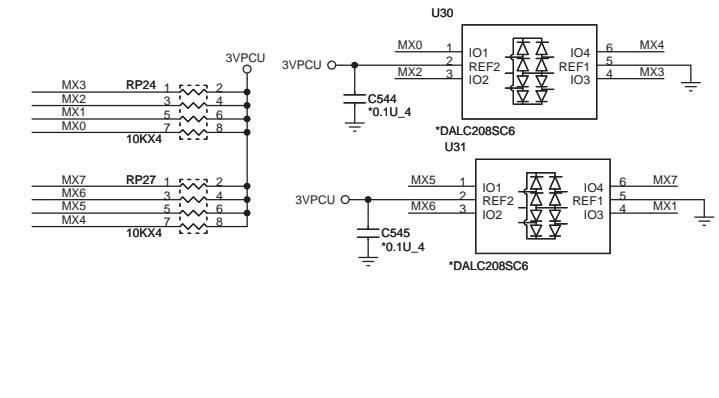
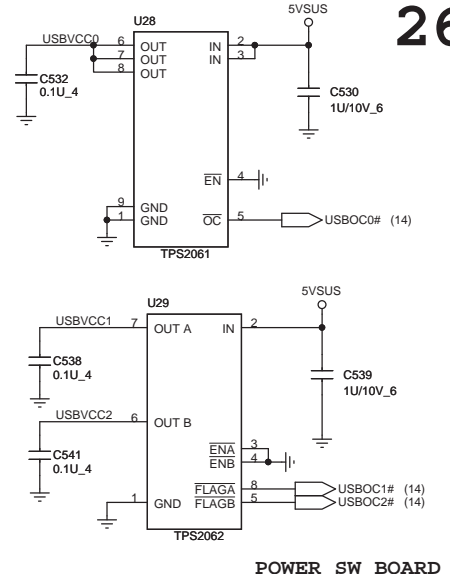
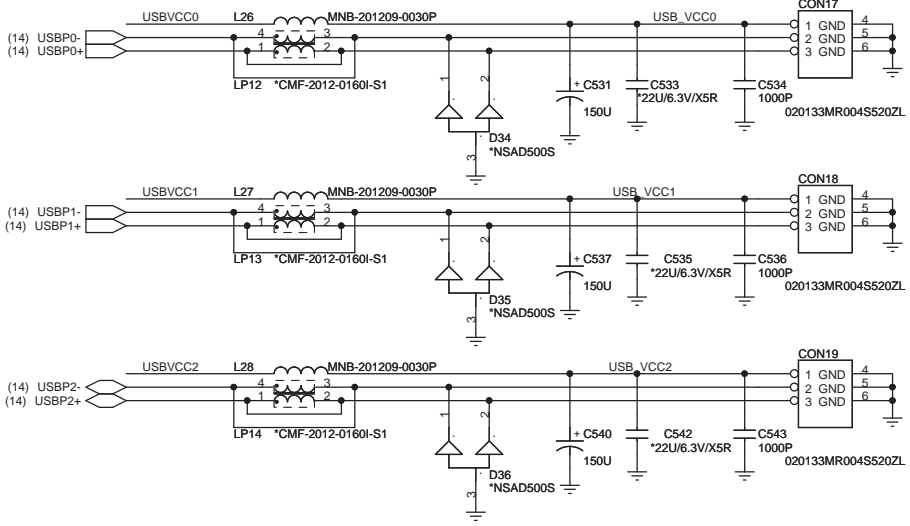
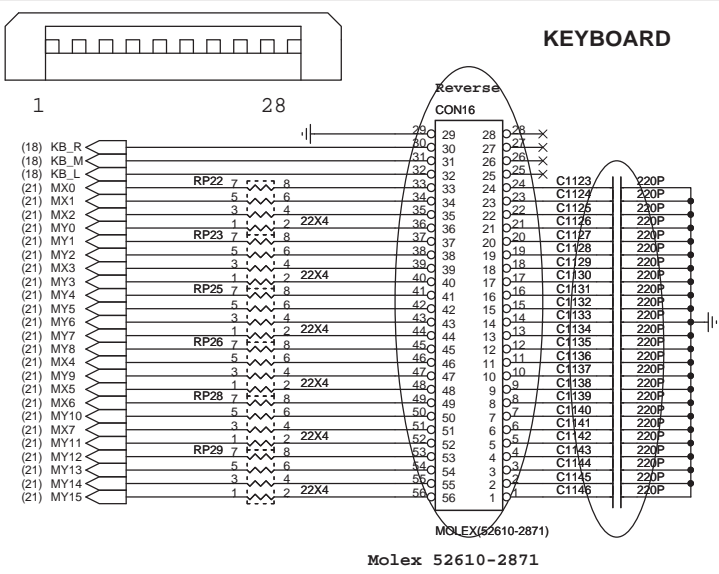
1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

Title: **Docking/TPM**

Size: Document Number **RJ6 Main Board** Rev **1A**

Date: Wednesday, May 03, 2006 Sheet 25 of 40



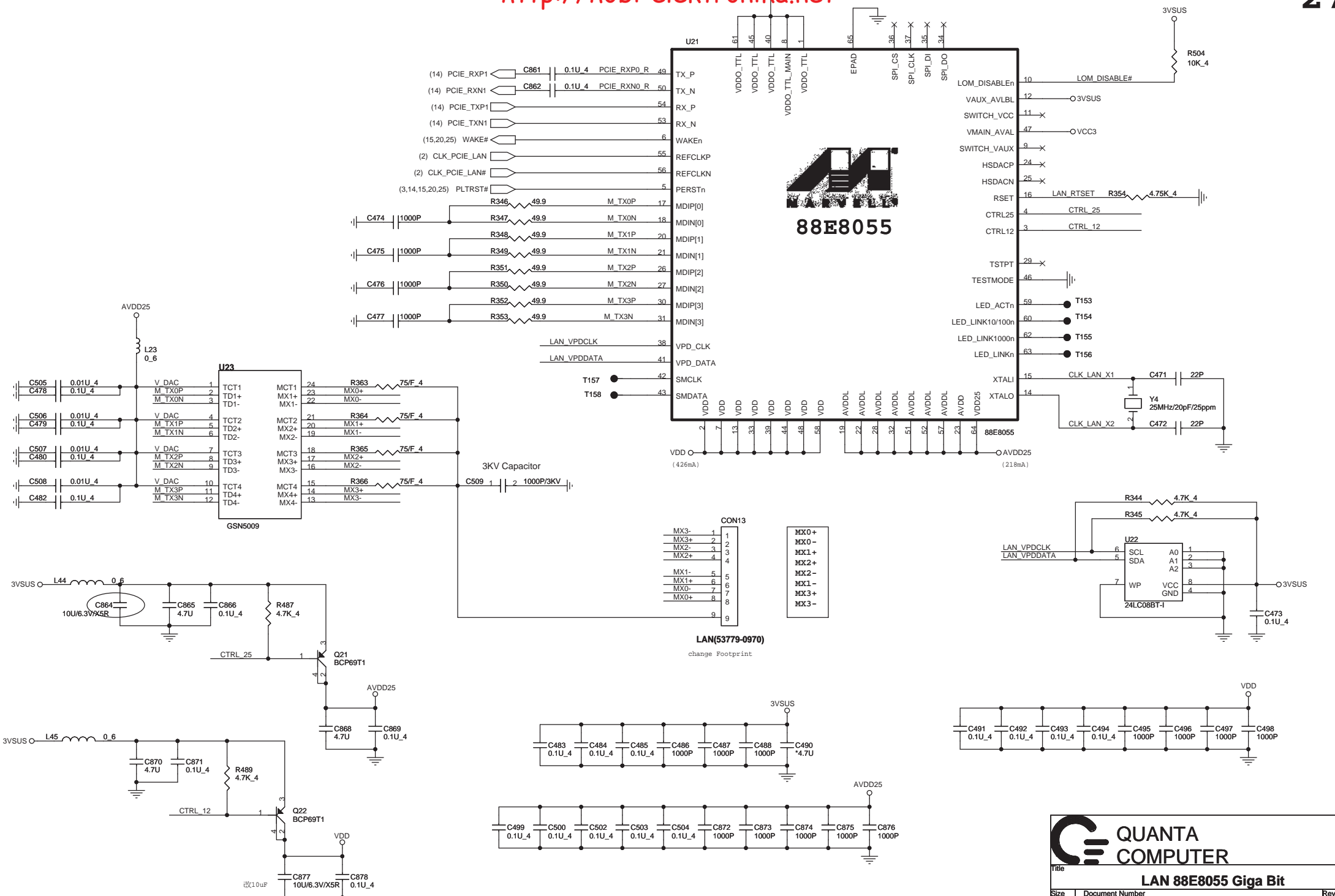
1.Level 1 Environment-related Substances Should NEVER be Used.  
 2.Purchase ink, paint, wire rods, and Welding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

Title: **K/B ,USB**

Size: Document Number **RJ6 Main Board** Rev **2A**

Date: Wednesday, May 03, 2006 Sheet 26 of 40



1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

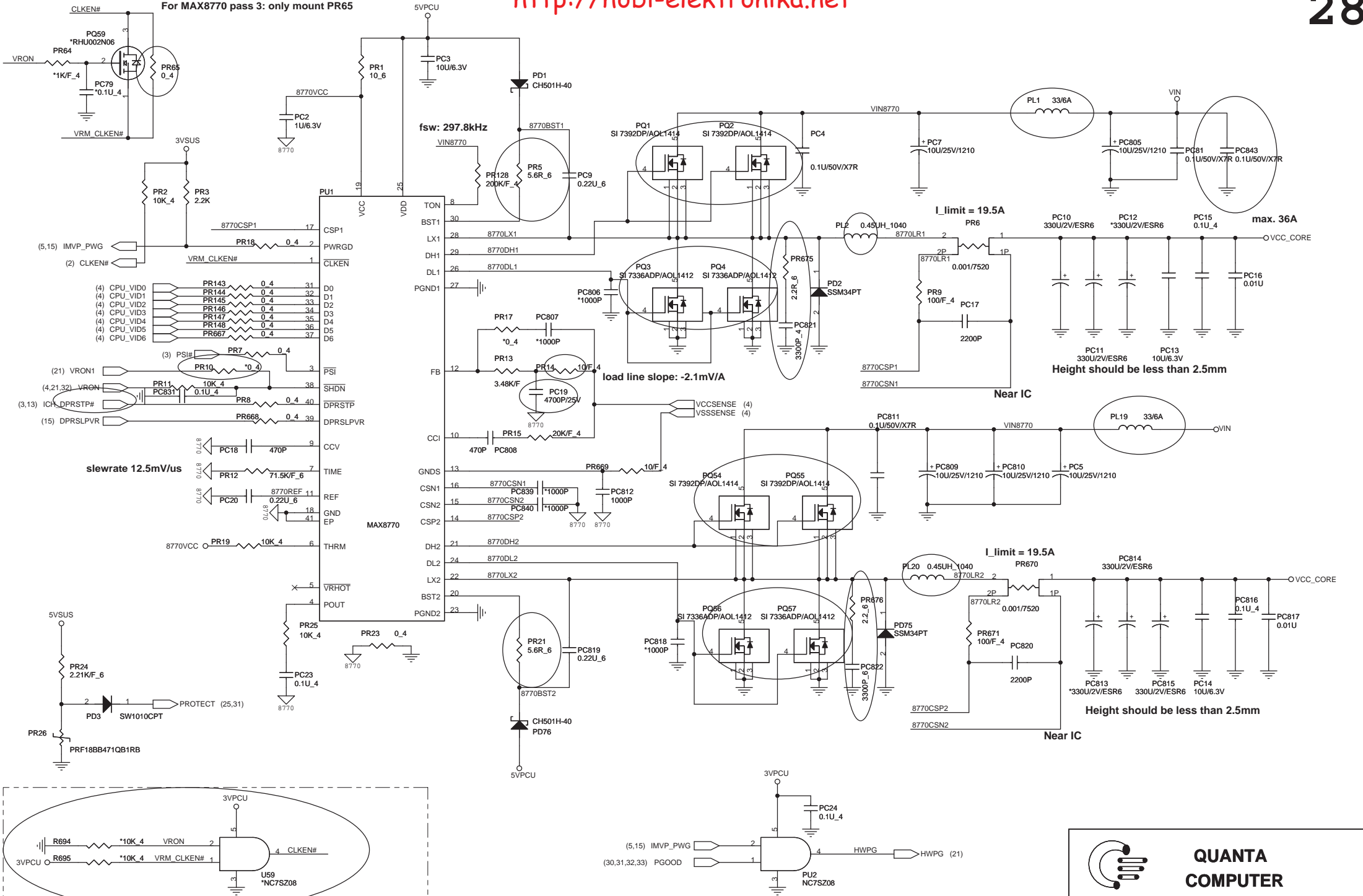
Title: LAN 88E8055 Giga Bit

Size: RJ6 Main Board

Document Number: Rev 1B

Date: Tuesday, May 09, 2006 Sheet 27 of 40

For MAX8770 pass 2: mount PR64, PQ59, PC79  
For MAX8770 pass 3: only mount PR65



slewrate 12.5mV/us

fsw: 297.8kHz

load line slope: -2.1mV/A

I\_limit = 19.5A

max. 36A

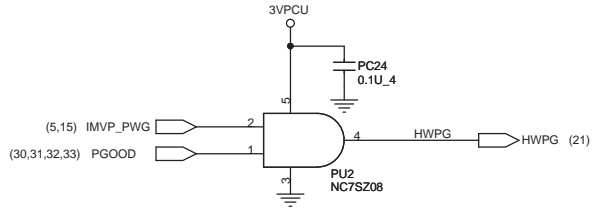
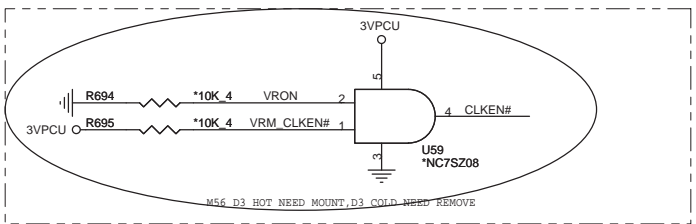
Height should be less than 2.5mm

Near IC

I\_limit = 19.5A

Height should be less than 2.5mm

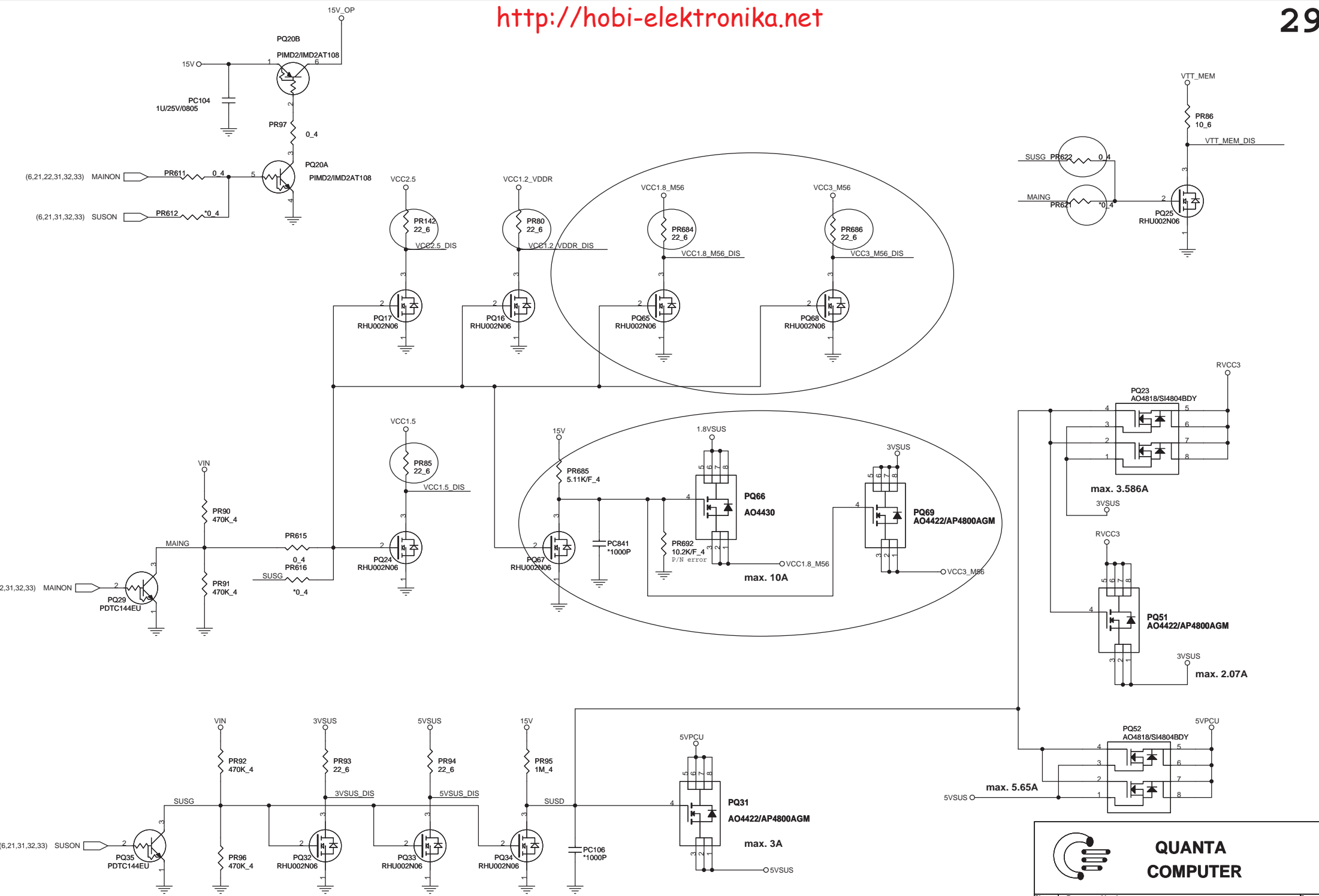
Near IC




1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>RJ6 Main Board (VCC_CORE)</b>	<b>2A</b>
Date:	Friday, May 05, 2006	Sheet 28 of 40

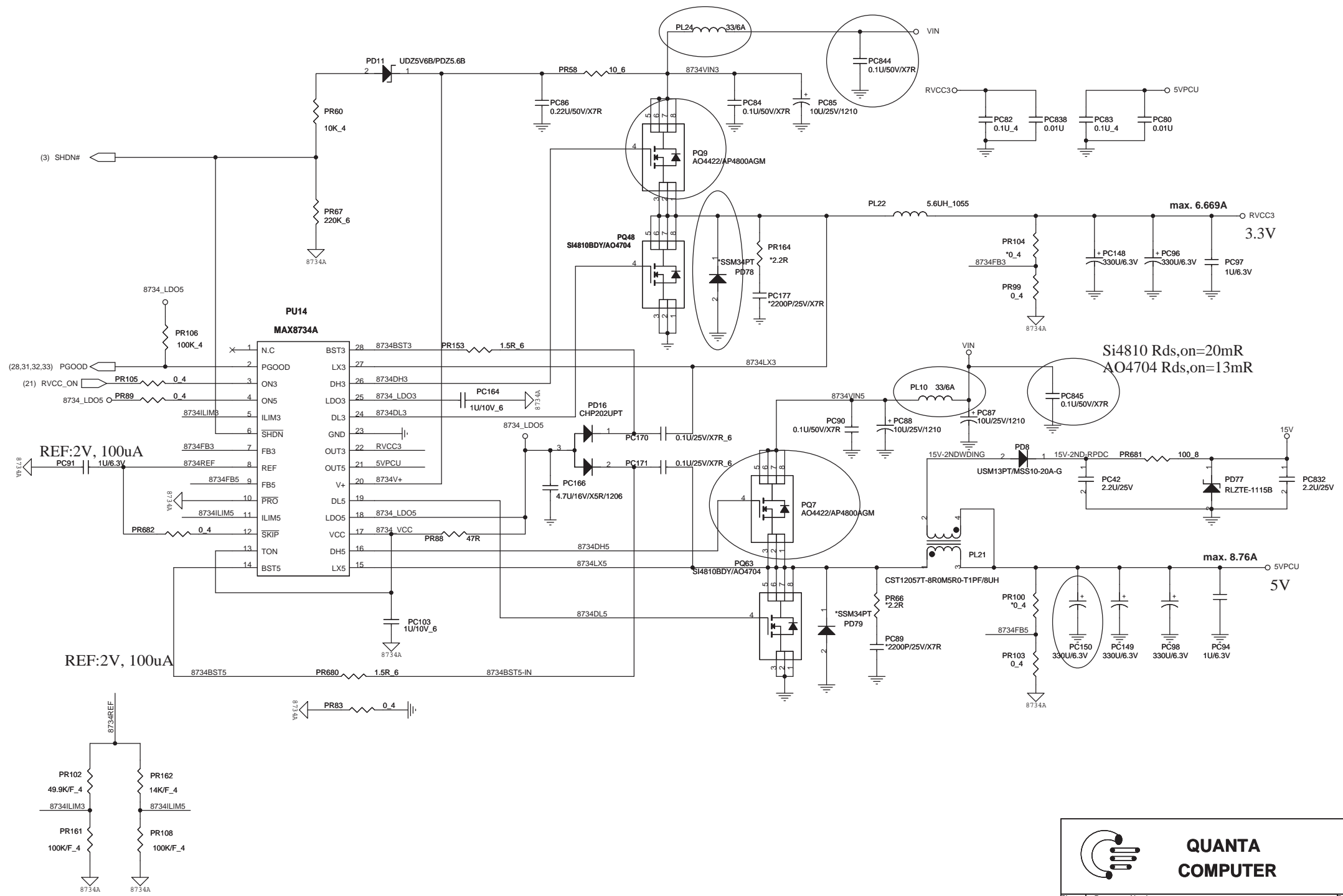


1.Level 1 Environment-related Substances Should NEVER be Used.  
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.




**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>R.J6 Main Board (LOAD SW/DISCHARGE)</b>	<b>2A</b>
Date:	Wednesday, May 03, 2006	Sheet 29 of 40

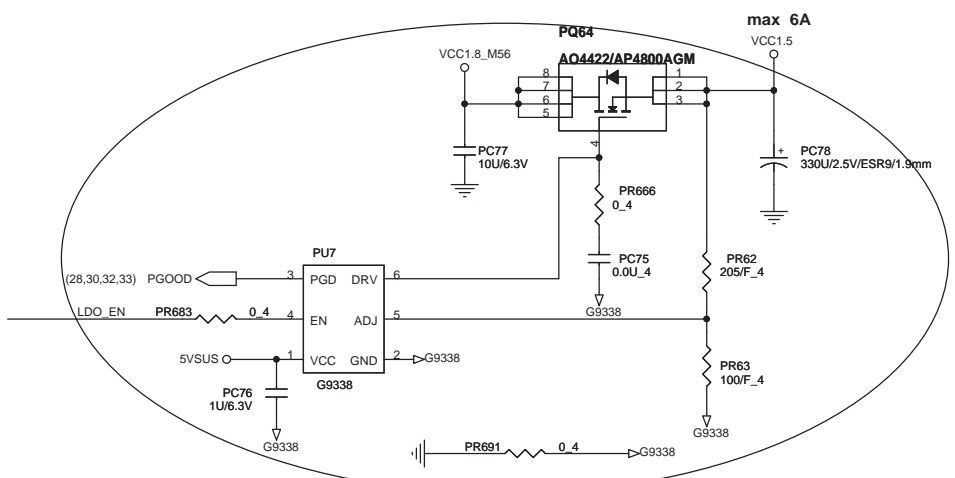
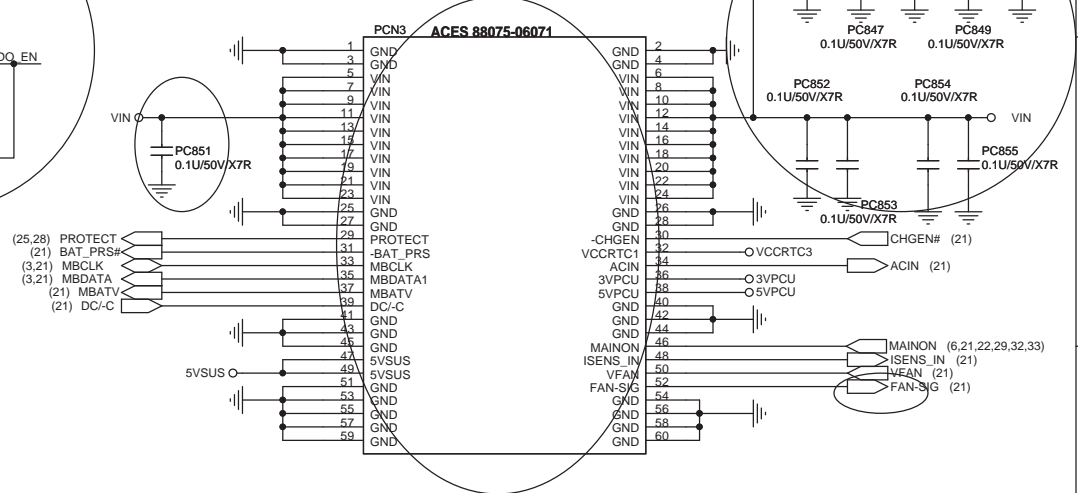
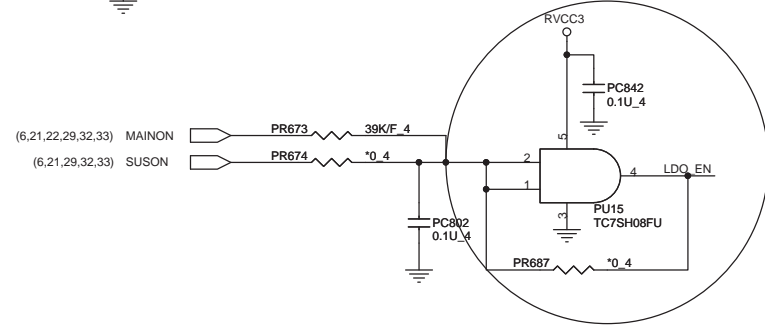
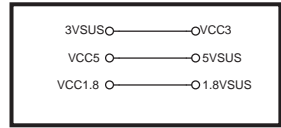
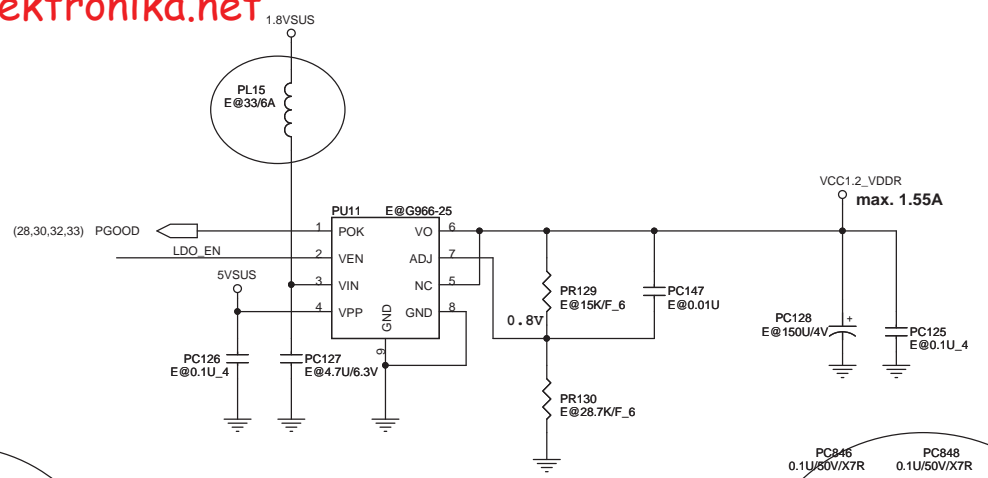
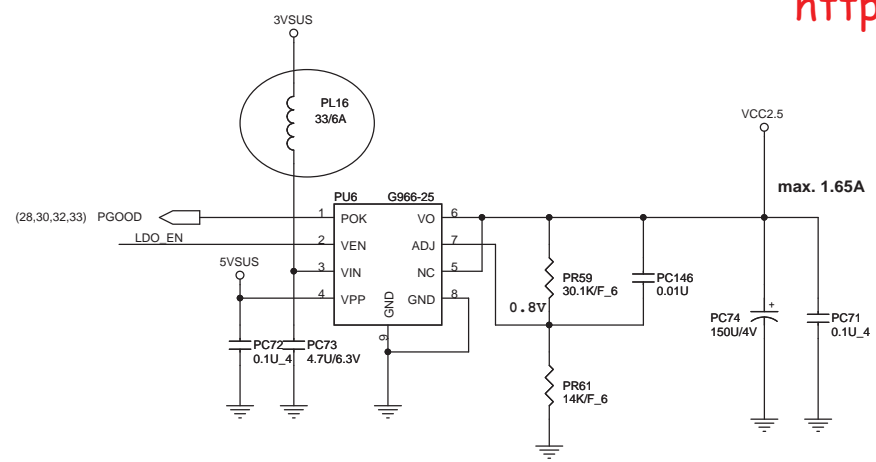


1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.




**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>RJ6 Main Board (5V/3V/12V)</b>	<b>1B</b>
Date:	Friday, May 05, 2006	Sheet 30 of 40

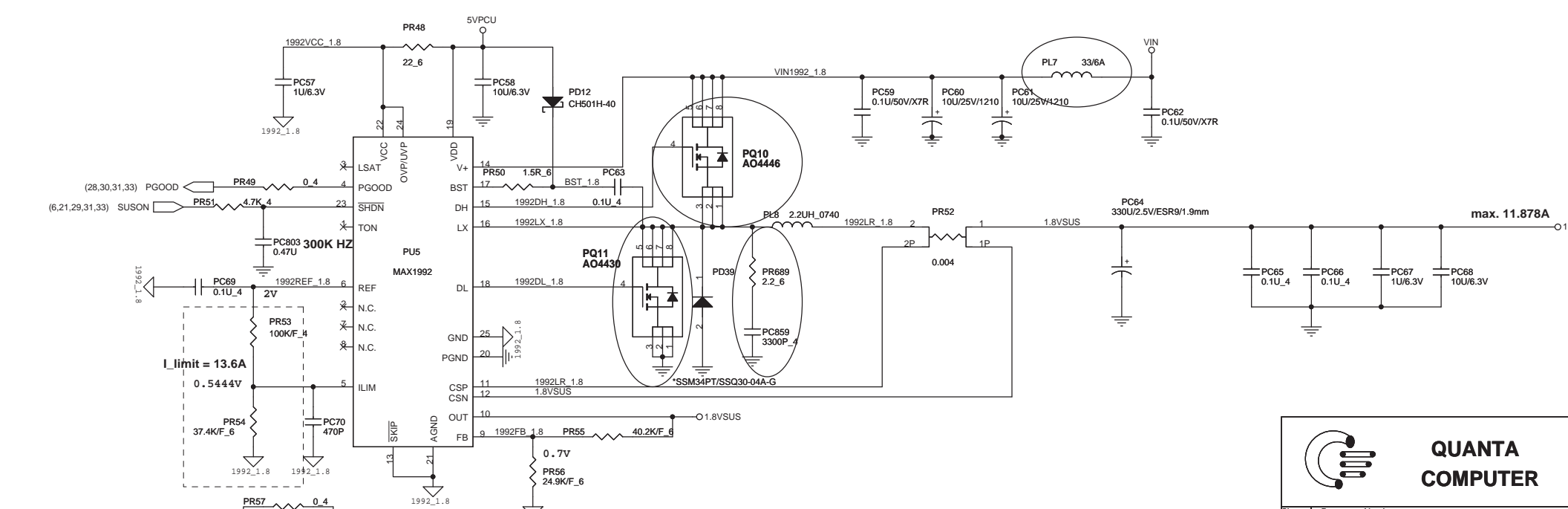
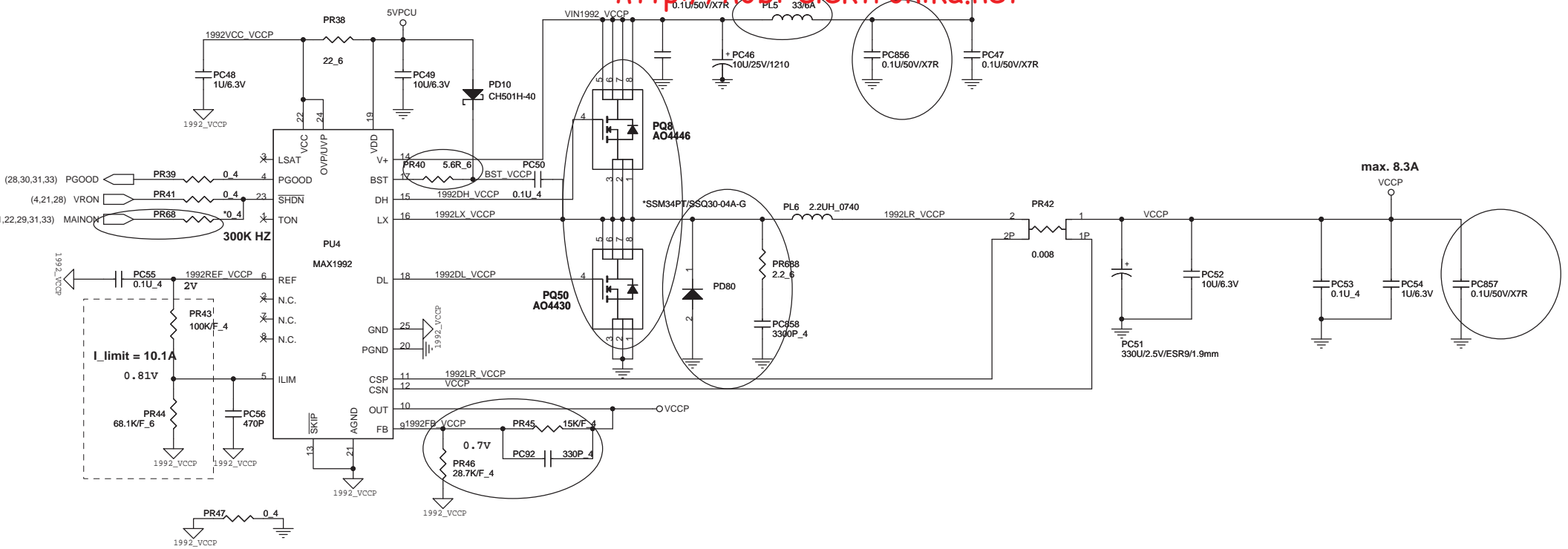


1. Level 1 Environment-related Substances should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.




**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>RJ6 Main Board (LDO)</b>	<b>2A</b>
Date:	Monday, May 08, 2006	Sheet 31 of 40



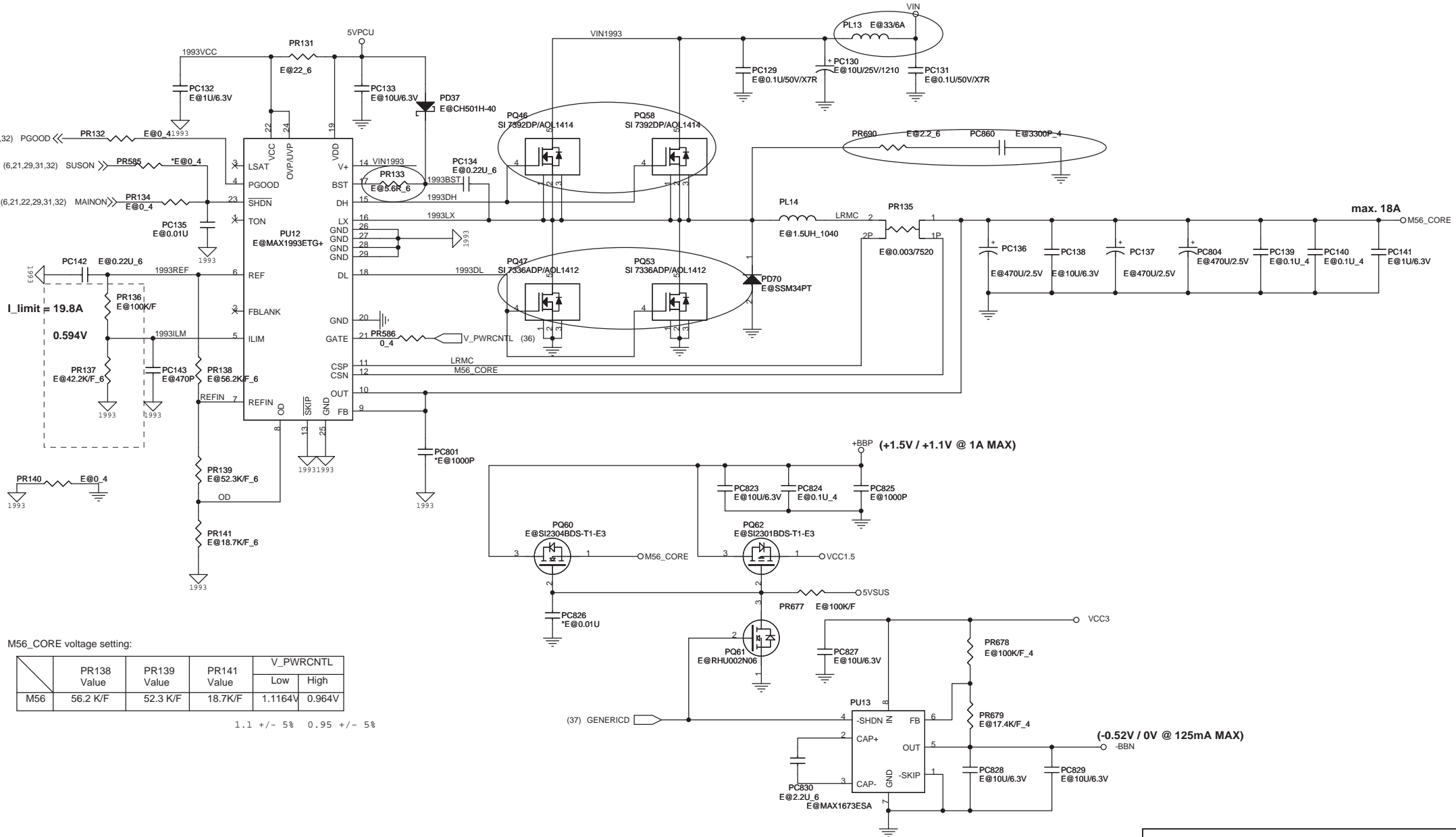
1. Level 1 Environment-related Substances should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>RJ6 Main Board (1.8VSUS/VCCP)</b>	<b>1B</b>
Date:	Wednesday, May 03, 2006	Sheet 32 of 40





M56\_CORE voltage setting:

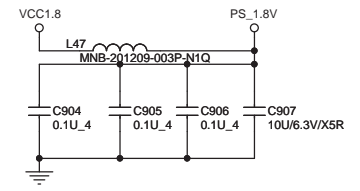
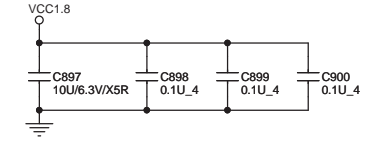
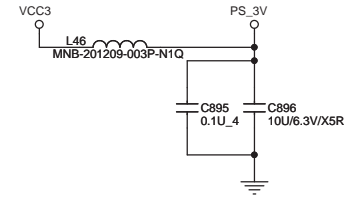
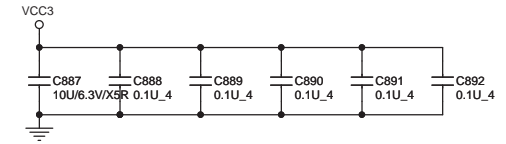
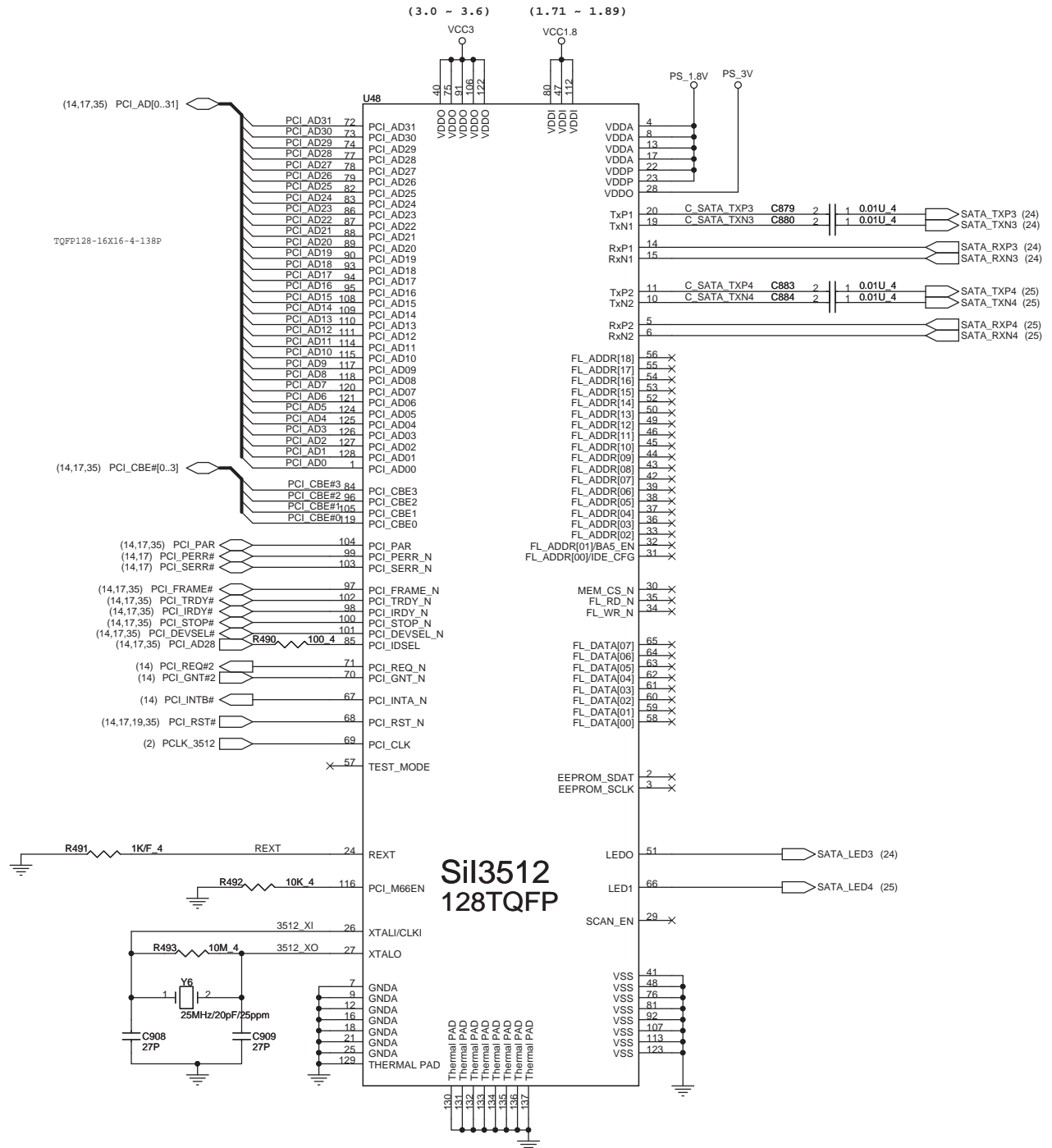
	PR138 Value	PR139 Value	PR141 Value	V_PWRCNTL	
				Low	High
M56	56.2 K/F	52.3 K/F	18.7K/F	1.1164V	0.964V

1.1 +/- 5% 0.95 +/- 5%

1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA  
COMPUTER

Size	Document Number	Rev
	<b>RJ6 Main Board (M56_CORE)</b>	<b>2A</b>
Date:	Wednesday, May 03, 2006	Sheet 33 of 40



Sil3512 128TQFP

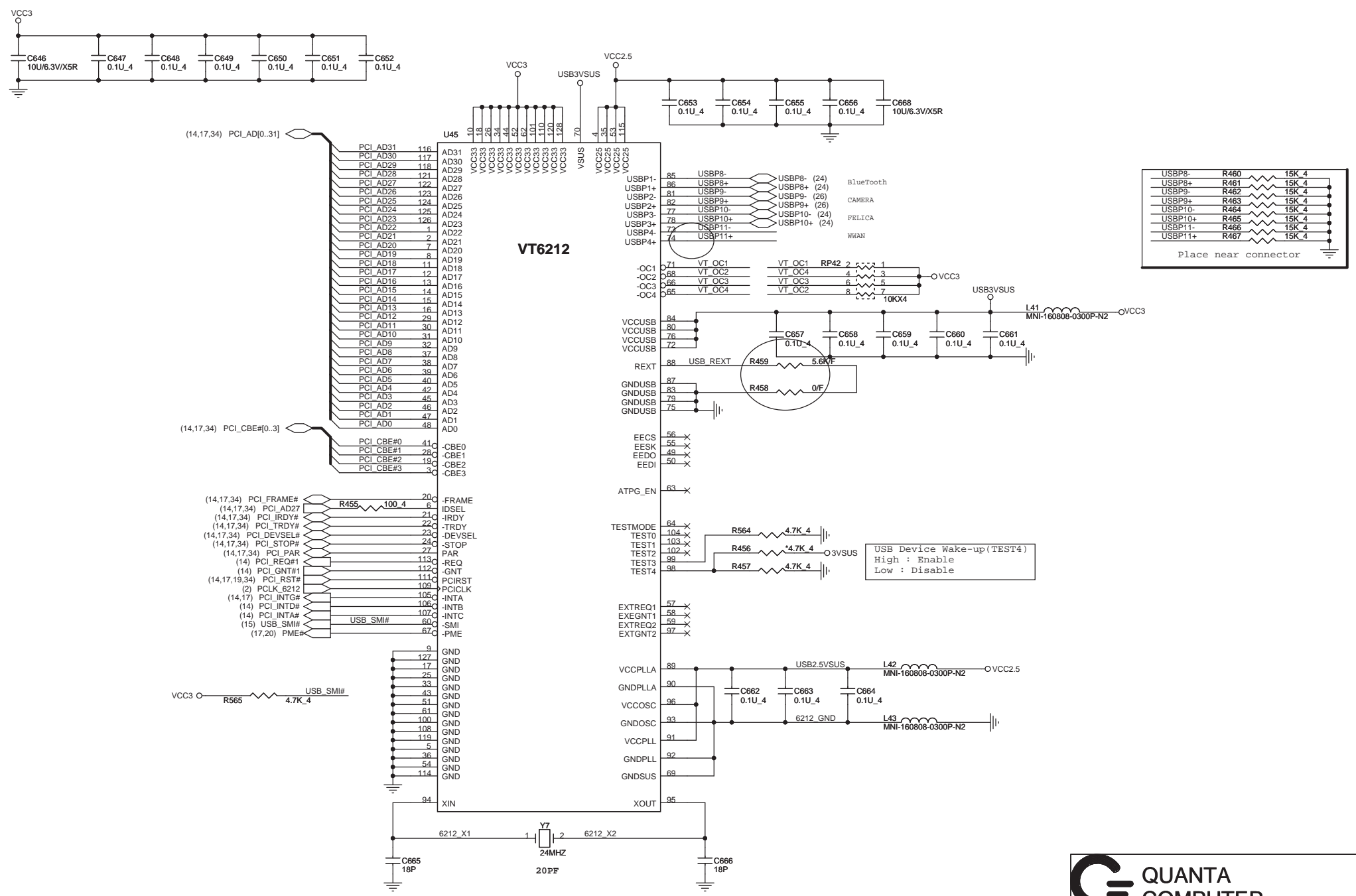
**QUANTA COMPUTER**

Title: **PCI-SATA Sil3512**

Size: Custom Document Number: **RJ6 Main Board** Rev: 1B

Date: Tuesday, May 09, 2006 Sheet 34 of 40

1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



USBP8-	R460	15K 4
USBP8+	R461	15K 4
USBP9-	R462	15K 4
USBP9+	R463	15K 4
USBP10-	R464	15K 4
USBP10+	R465	15K 4
USBP11-	R466	15K 4
USBP11+	R467	15K 4

Place near connector

USB Device Wake-up (TEST4)  
High : Enable  
Low : Disable

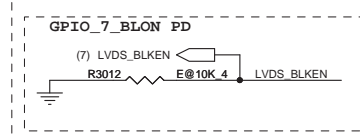
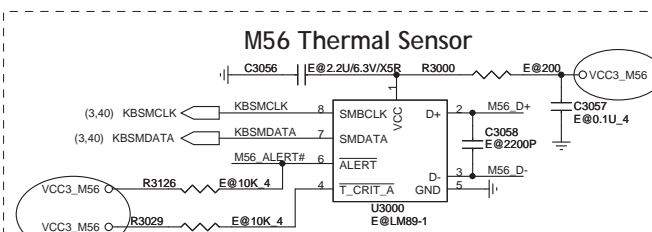
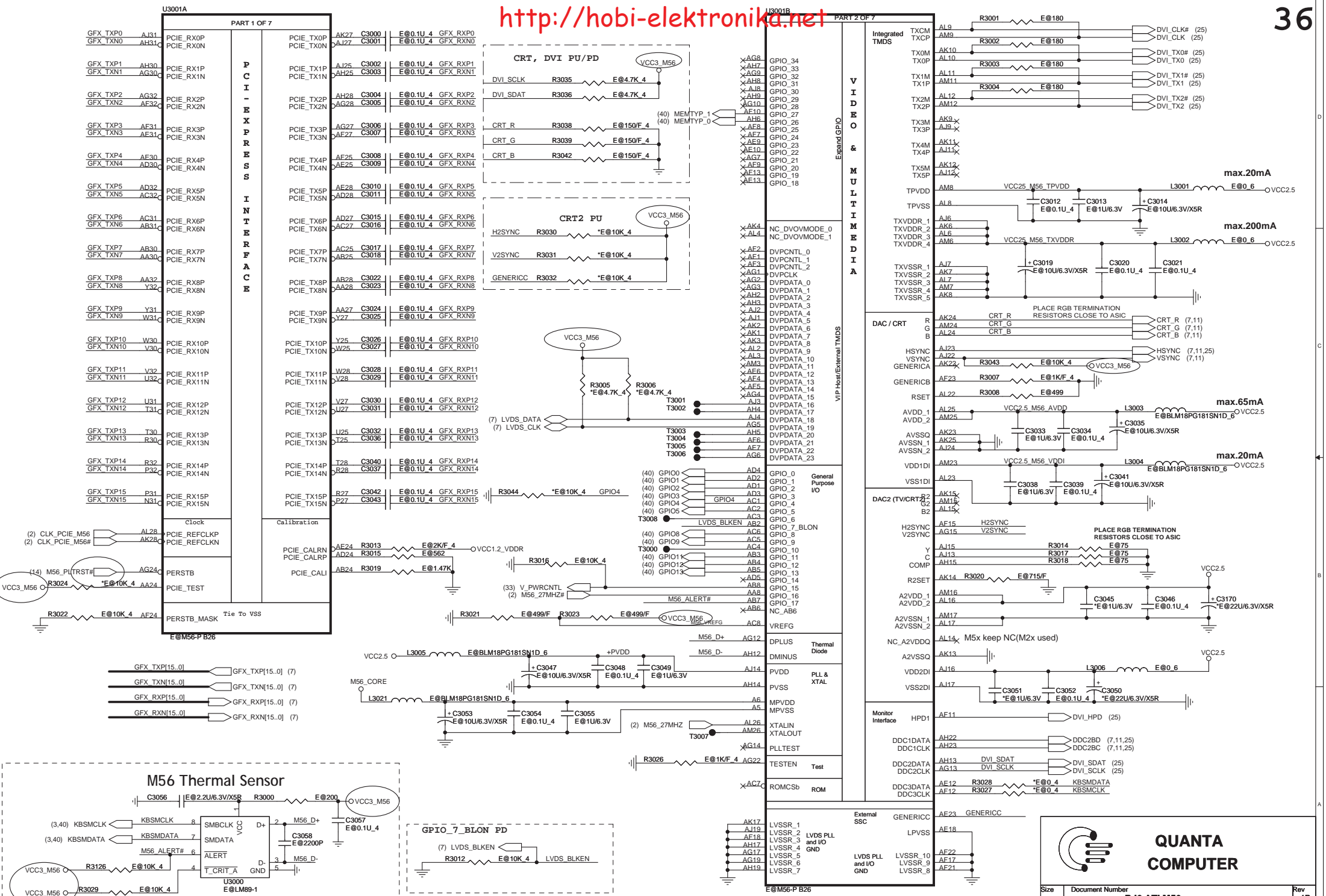
1. Level 1 Environment-related Substances Should NEVER be Used.  
2. Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

Title: **USB Controller VT6212**

Size: Custom Document Number: **RJ6 Main Board** Rev: 2A

Date: Tuesday, May 09, 2006 Sheet: 35 of 40



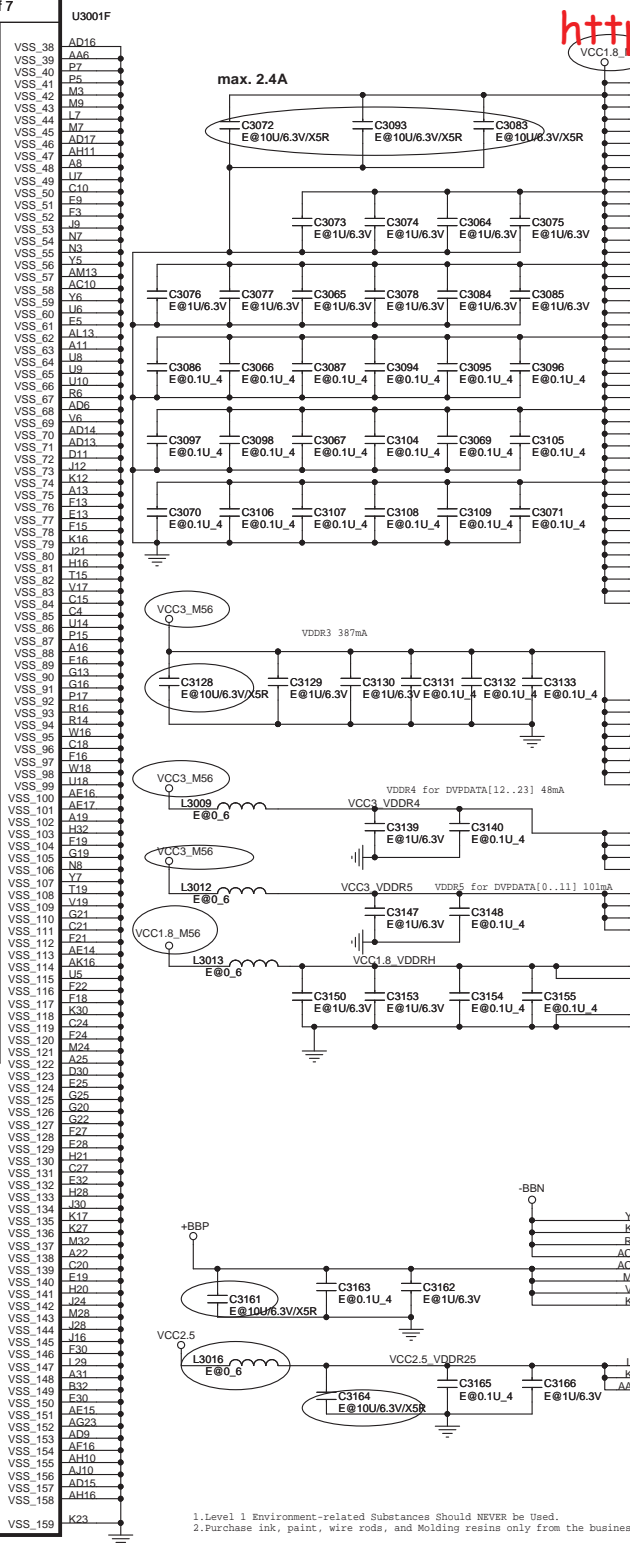
1. Level 1 Environment-related Substances should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and holding resins only from the business partners that Sony approves as green partners.

**QUANTA  
COMPUTER**

Size	Document Number	Rev
	<b>RJ6 ATI M56</b>	<b>1B</b>
Date: <b>Wednesday, May 03, 2006</b>		Sheet <b>36</b> of <b>40</b>

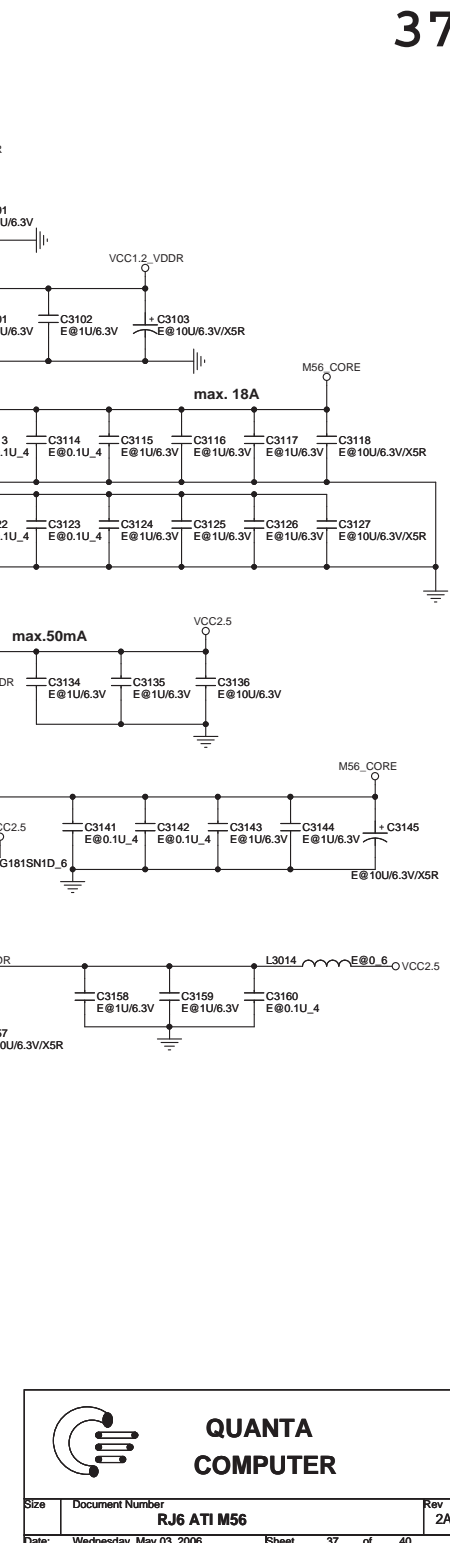
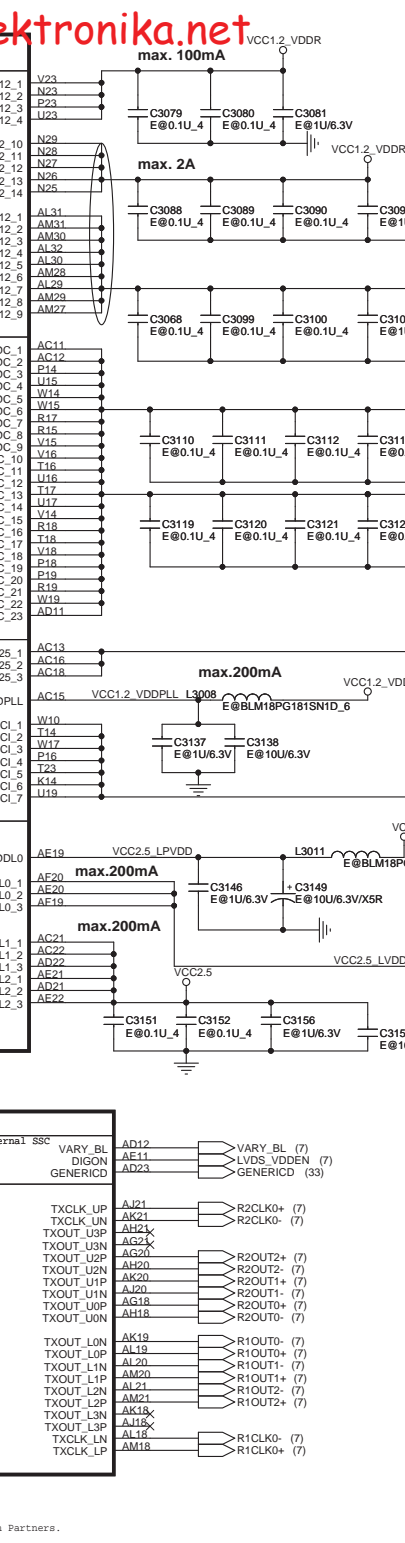
Part 6 of 7

AH27	PCIE_VSS_1	VSS_38
AC23	PCIE_VSS_2	VSS_39
R27	PCIE_VSS_3	VSS_40
P25	PCIE_VSS_4	VSS_41
R25	PCIE_VSS_5	VSS_42
R25	PCIE_VSS_6	VSS_43
T26	PCIE_VSS_7	VSS_44
U26	PCIE_VSS_8	VSS_45
W26	PCIE_VSS_9	VSS_46
Y26	PCIE_VSS_10	VSS_47
AB26	PCIE_VSS_11	VSS_48
AC26	PCIE_VSS_12	VSS_49
AD25	PCIE_VSS_13	VSS_50
AE26	PCIE_VSS_14	VSS_51
AF26	PCIE_VSS_15	VSS_52
AG26	PCIE_VSS_16	VSS_53
AH26	PCIE_VSS_17	VSS_54
AC28	PCIE_VSS_18	VSS_55
Y28	PCIE_VSS_19	VSS_56
U28	PCIE_VSS_20	VSS_57
P28	PCIE_VSS_21	VSS_58
AH29	PCIE_VSS_22	VSS_59
AF29	PCIE_VSS_23	VSS_60
Y29	PCIE_VSS_24	VSS_61
U29	PCIE_VSS_25	VSS_62
W29	PCIE_VSS_26	VSS_63
AB27	PCIE_VSS_27	VSS_64
W26	PCIE_VSS_28	VSS_65
AJ26	PCIE_VSS_29	VSS_66
AJ32	PCIE_VSS_31	VSS_68
AK29	PCIE_VSS_32	VSS_69
P29	PCIE_VSS_33	VSS_70
R29	PCIE_VSS_35	VSS_72
T29	PCIE_VSS_36	VSS_73
U29	PCIE_VSS_37	VSS_74
W29	PCIE_VSS_38	VSS_75
Y29	PCIE_VSS_39	VSS_76
AA29	PCIE_VSS_40	VSS_77
AD29	PCIE_VSS_41	VSS_78
AE29	PCIE_VSS_42	VSS_79
AF29	PCIE_VSS_43	VSS_80
AG29	PCIE_VSS_44	VSS_81
AH29	PCIE_VSS_45	VSS_82
AK26	PCIE_VSS_46	VSS_83
AK30	PCIE_VSS_47	VSS_84
AG26	PCIE_VSS_48	VSS_85
NA29	PCIE_VSS_49	VSS_86
R31	PCIE_VSS_50	VSS_87
AF30	PCIE_VSS_51	VSS_88
AC30	PCIE_VSS_52	VSS_89
Y30	PCIE_VSS_53	VSS_90
P30	PCIE_VSS_54	VSS_91
U30	PCIE_VSS_55	VSS_92
AA31	PCIE_VSS_56	VSS_93
U30	PCIE_VSS_57	VSS_94
AD31	PCIE_VSS_58	VSS_95
AK32	PCIE_VSS_59	VSS_96
AJ28	PCIE_VSS_60	VSS_97
Y30	PCIE_VSS_61	VSS_98
AJ30	PCIE_VSS_62	VSS_99
AK31	PCIE_VSS_63	VSS_100
AA23	PCIE_VSS_64	VSS_101
AG31	PCIE_VSS_65	VSS_102
NA24	PCIE_VSS_66	VSS_103
P24	PCIE_VSS_67	VSS_104
R24	PCIE_VSS_68	VSS_105
R24	PCIE_VSS_69	VSS_106
T24	PCIE_VSS_70	VSS_107
U24	PCIE_VSS_71	VSS_108
V24	PCIE_VSS_72	VSS_109
W24	PCIE_VSS_73	VSS_110
Y24	PCIE_VSS_74	VSS_111
AA24	PCIE_VSS_75	VSS_112
AD24	PCIE_VSS_76	VSS_113
V25	PCIE_VSS_77	VSS_114
AE25	PCIE_VSS_78	VSS_115
R26	PCIE_VSS_79	VSS_116
AA26	PCIE_VSS_80	VSS_117
AF27	PCIE_VSS_81	VSS_118
AE27	PCIE_VSS_82	VSS_119
L3015	PCIE_PVSS	VSS_120
B1	VSS_1	VSS_123
L1	VSS_2	VSS_124
P1	VSS_3	VSS_125
U1	VSS_4	VSS_126
Y1	VSS_5	VSS_127
AD7	VSS_6	VSS_128
AE8	VSS_7	VSS_129
AL1	VSS_8	VSS_130
A2	VSS_9	VSS_131
VSS_10	VSS_10	VSS_132
AD10	VSS_11	VSS_133
ER	VSS_12	VSS_134
HR	VSS_13	VSS_135
VSS_14	VSS_14	VSS_136
VSS_15	VSS_15	VSS_137
VSS_16	VSS_16	VSS_138
VSS_17	VSS_17	VSS_139
VSS_18	VSS_18	VSS_140
VSS_19	VSS_19	VSS_141
VSS_20	VSS_20	VSS_142
VSS_21	VSS_21	VSS_143
VSS_22	VSS_22	VSS_144
VSS_23	VSS_23	VSS_145
VSS_24	VSS_24	VSS_146
VSS_25	VSS_25	VSS_147
VSS_26	VSS_26	VSS_148
VSS_27	VSS_27	VSS_149
VSS_28	VSS_28	VSS_150
VSS_29	VSS_29	VSS_151
VSS_30	VSS_30	VSS_152
VSS_31	VSS_31	VSS_153
VSS_32	VSS_32	VSS_154
VSS_33	VSS_33	VSS_155
VSS_34	VSS_34	VSS_156
VSS_35	VSS_35	VSS_157
VSS_36	VSS_36	VSS_158
VSS_37	VSS_37	VSS_159



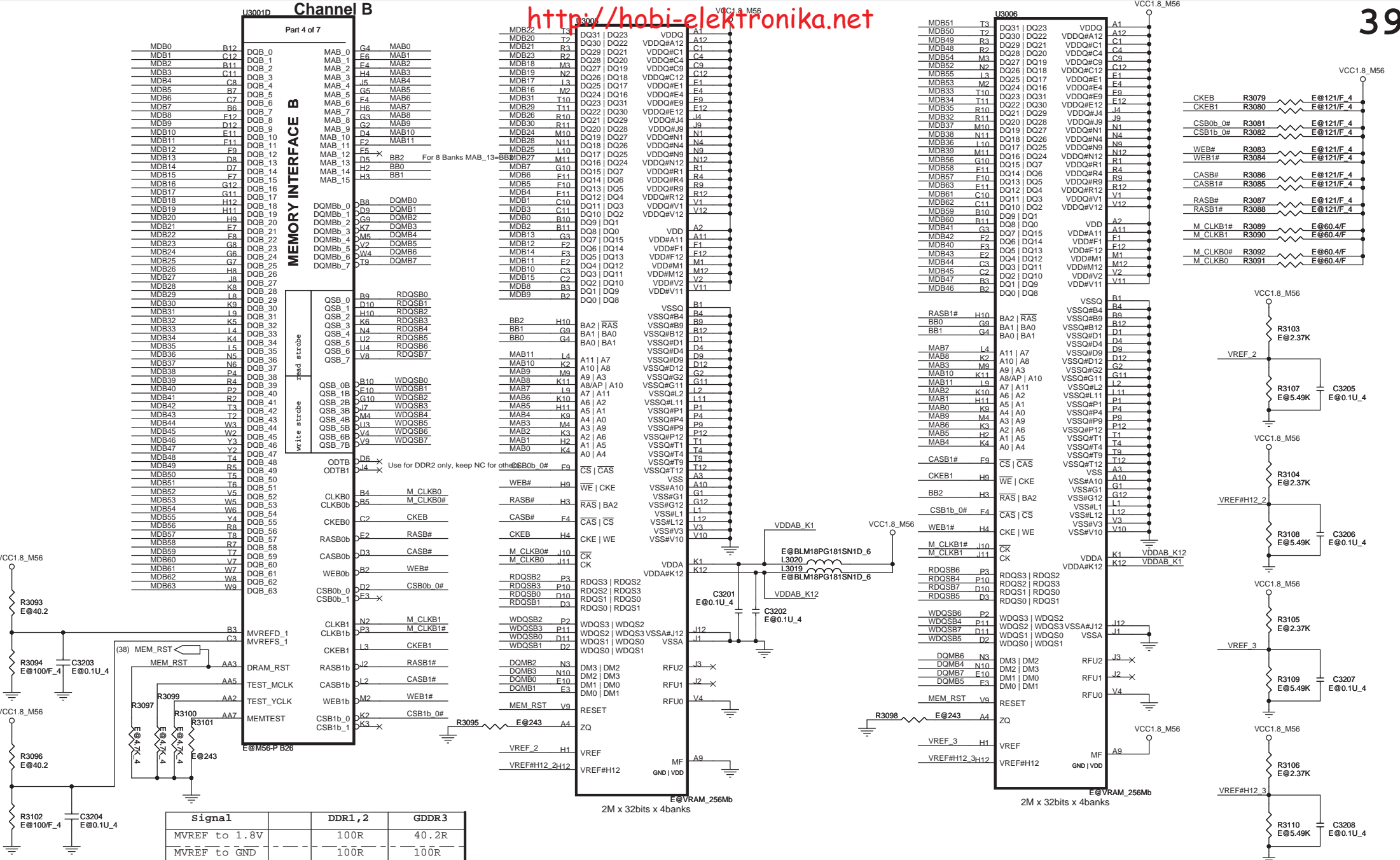
U3001F

C1	VDD1.1
J1	VDD1.2
M1	VDD1.3
L7	VDD1.4
R1	VDD1.5
H10	VDD1.6
AA1	VDD1.7
A3	VDD1.8
PA	VDD1.9
I17	VDD1.10
N9	VDD1.11
P10	VDD1.12
V11	VDD1.13
A9	VDD1.14
Y10	VDD1.15
P10	VDD1.16
R9	VDD1.17
Y9	VDD1.18
AM13	VDD1.19
A11	VDD1.20
M10	VDD1.21
N10	VDD1.22
Y8	VDD1.23
V11	VDD1.24
K21	VDD1.25
H13	VDD1.26
A15	VDD1.27
J20	VDD1.28
H11	VDD1.29
K11	VDD1.30
K19	VDD1.31
A18	VDD1.32
L23	VDD1.33
K12	VDD1.34
K24	VDD1.35
L24	VDD1.36
H19	VDD1.37
K13	VDD1.38
J32	VDD1.39
F32	VDD1.40
A30	VDD1.41
C32	VDD1.42
V17	VDD1.43
C15	VDD1.44
C4	VDD1.45
U14	VDD1.46

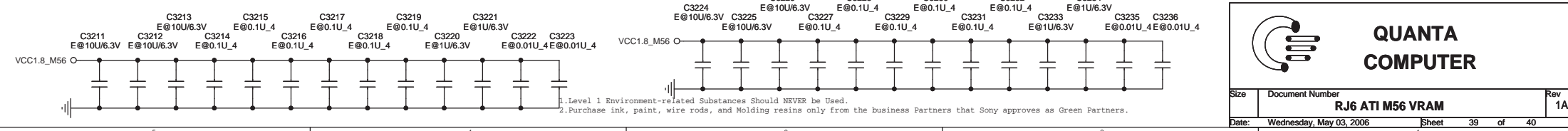



1. Level 1 Environment-related Substances should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





Signal	DDR1, 2	GDDR3
MVREF to 1.8V	100R	40.2R
MVREF to GND	100R	100R





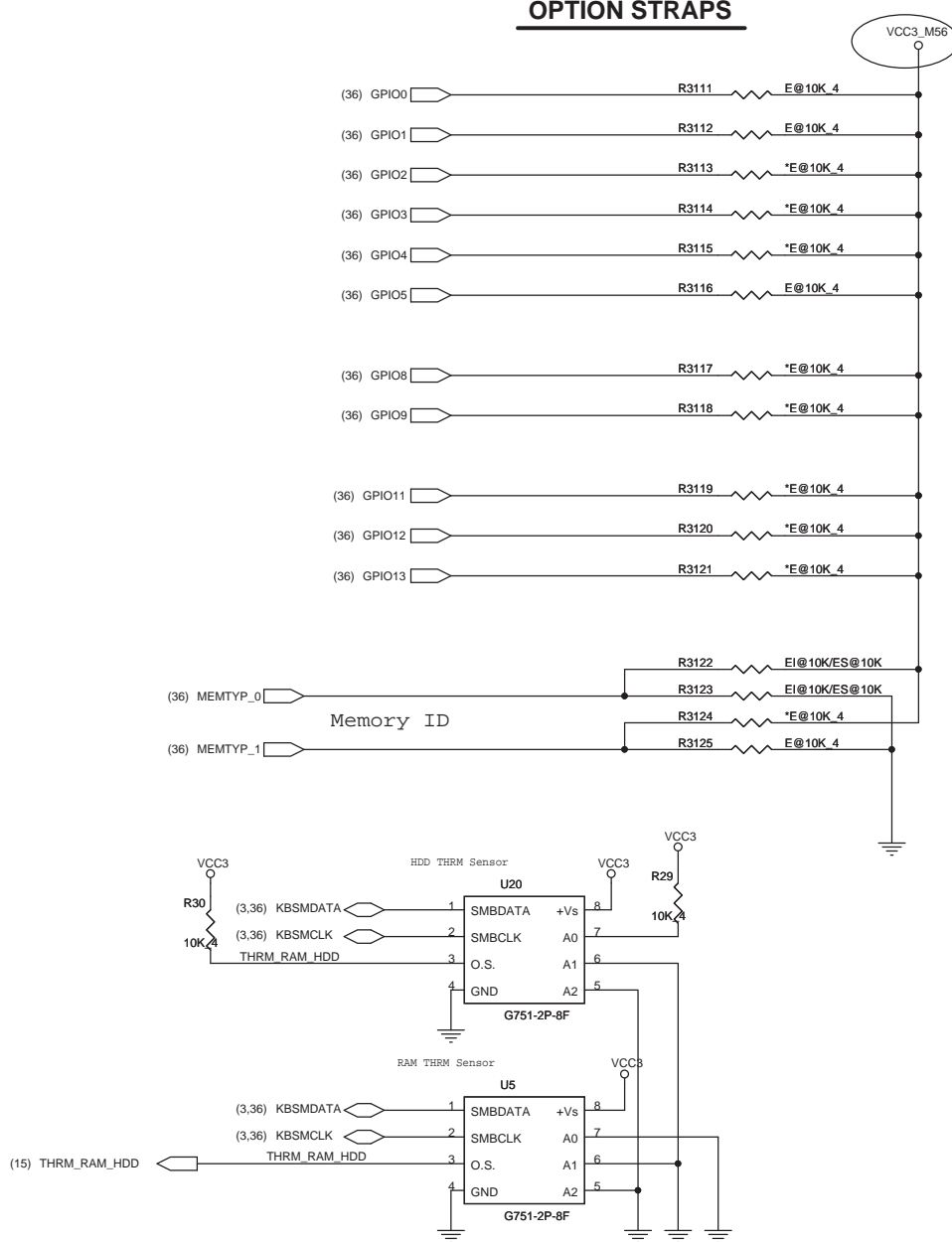
# QUANTA COMPUTER

Size	Document Number	Rev	
	<b>R/J6 ATI M56 VRAM</b>	1A	
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**OPTION STRAPS**

M56-P Strap

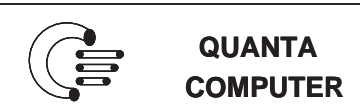


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	(recommended) Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0 (internal pull-down)
Reserved	GPIO(3:2)	(recommended) ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB(Default) 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYN	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port devices present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYN	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

**VRAM Straps**

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYP[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - TBD 11 - TBD	00



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