Compal Confidential

QIWG5/QIWG6 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13X

2012-02-01

LA-7981P

REV:1.0

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Compal Electronics, Inc.

Title: Cover Page

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ZZZ: LA7981 G5_DAZ@ DAZ_PCB DAZ0N100101
ZZZ1: G5_DA@ DA_PCB DA80000Q010
ZZZ2: G5_DA@ DA_PCB DA400016P10
ZZZ3: G5_DA@ DA_PCB DA400016Q10
ZZZ4: G5_DA@ DA_PCB DA400018T10

ZZZ5: LA7981 G6_DAZ@ DAZ_PCB DAZ0N200101
ZZZ7: G6_DA@ DA_PCB DA80000Q010
ZZZ6: G6_DA@ DA_PCB DA400016P10
ZZZ8: G6_DA@ DA_PCB DA400016Q10
ZZZ9: G6_DA@ DA_PCB DA400016R10
ZZZ10: G6_DA@ DA_PCB DA400016S10
ZZZ11: G6_DA@ DA_PCB DA400018T10

LS7983P PWR/B

QIWG6

LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B
LS7984P LED/B
LS7985P ODD/B

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Intel Ivy Bridge
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Dual Channel
DDR3 1066MHz(1.5V)
DDR3 1333MHz(1.5V)
DDR3 1600MHz(1.5V)

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  SDXC/MMC
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(Port 0/Port 1 support SATA3)

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Title	Block Diagram	
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW			
Full ON	HIGH	HIGH	HIGH	HIGH	ON			
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Right Side CR-BD)
	UHCI1	2	USB Port (Left Side) USB3.0
		3	USB Port (Left Side) USB3.0
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
GPU:N13M-GE	N13M@
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Cameara	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@
G5/G6/G9(Low/Mid END)	nonBBH@
G9 High-END	BBH@
G9	G9 @
G5/G6/G9(Low/Mid END)	15_nonBBH@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

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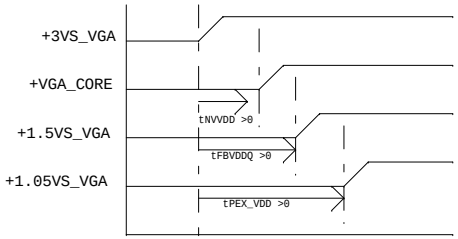
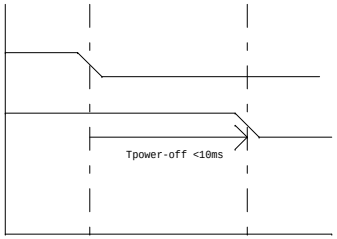
Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GL (28nm)	??
N13M-GE (28nm)	???

GPU	FB Memory (GDDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL N13M-GE	Samsung 2500MHz	K4G10325FG-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ1H24BFR-T2C						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 2500MHz	K4G20325FG-HC04						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ2H24MFR-T2C						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

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Title: VGA Notes List

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PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

+V1.05S_VCCP

R1
24.9_0402_1%

JCPU1A

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_COMP

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

DMI

<16> DMI_CRX_PTX_N0	B27	DMI_RX#[0]
<16> DMI_CRX_PTX_N1	B25	DMI_RX#[1]
<16> DMI_CRX_PTX_N2	A25	DMI_RX#[2]
<16> DMI_CRX_PTX_N3	B24	DMI_RX#[3]
<16> DMI_CRX_PTX_P0	B28	DMI_RX[0]
<16> DMI_CRX_PTX_P1	B26	DMI_RX[1]
<16> DMI_CRX_PTX_P2	A24	DMI_RX[2]
<16> DMI_CRX_PTX_P3	B23	DMI_RX[3]
<16> DMI_CTX_PRX_N0	G21	DMI_TX#[0]
<16> DMI_CTX_PRX_N1	E22	DMI_TX#[1]
<16> DMI_CTX_PRX_N2	F21	DMI_TX#[2]
<16> DMI_CTX_PRX_N3	D21	DMI_TX#[3]
<16> DMI_CTX_PRX_P0	G22	DMI_TX[0]
<16> DMI_CTX_PRX_P1	D22	DMI_TX[1]
<16> DMI_CTX_PRX_P2	F20	DMI_TX[2]
<16> DMI_CTX_PRX_P3	C21	DMI_TX[3]

Intel(R) FDI

<16> FDI_CTX_PRX_N0	A21	FDI0_TX#[0]
<16> FDI_CTX_PRX_N1	H19	FDI0_TX#[1]
<16> FDI_CTX_PRX_N2	E19	FDI0_TX#[2]
<16> FDI_CTX_PRX_N3	F18	FDI0_TX#[3]
<16> FDI_CTX_PRX_N4	B21	FDI1_TX#[0]
<16> FDI_CTX_PRX_N5	C20	FDI1_TX#[1]
<16> FDI_CTX_PRX_N6	D18	FDI1_TX#[2]
<16> FDI_CTX_PRX_N7	E17	FDI1_TX#[3]
<16> FDI_CTX_PRX_P0	A22	FDI0_TX[0]
<16> FDI_CTX_PRX_P1	G19	FDI0_TX[1]
<16> FDI_CTX_PRX_P2	E20	FDI0_TX[2]
<16> FDI_CTX_PRX_P3	G18	FDI0_TX[3]
<16> FDI_CTX_PRX_P4	B20	FDI1_TX[0]
<16> FDI_CTX_PRX_P5	C19	FDI1_TX[1]
<16> FDI_CTX_PRX_P6	D19	FDI1_TX[2]
<16> FDI_CTX_PRX_P7	F17	FDI1_TX[3]
<16> FDI_FSYNC0	J18	FDI0_FSYNC
<16> FDI_FSYNC1	J17	FDI1_FSYNC
<16> FDI_INT	H20	FDI_INT
<16> FDI_LSYNC0	J19	FDI0_LSYNC
<16> FDI_LSYNC1	H17	FDI1_LSYNC

+V1.05S_VCCP

R7
24.9_0402_1%

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

eDP

EDP_COMP	A18	eDP_COMPIO
	A17	eDP_ICOMPO
eDP_HPD	B16	eDP_HPD#
	C15	eDP_AUX
	D15	eDP_AUX#
	C17	eDP_TX[0]
	E16	eDP_TX[1]
	C16	eDP_TX[2]
	G15	eDP_TX[3]
	C18	eDP_TX#[0]
	E16	eDP_TX#[1]
	D16	eDP_TX#[2]
	F15	eDP_TX#[3]

PCI EXPRESS* - GRAPHICS

PCIE_CRX_GTX_N[0..15] <23>

PEG_RX#[0]	K33	PCIE_CRX_GTX_N15
PEG_RX#[1]	M35	PCIE_CRX_GTX_N14
PEG_RX#[2]	L34	PCIE_CRX_GTX_N13
PEG_RX#[3]	J35	PCIE_CRX_GTX_N12
PEG_RX#[4]	J32	PCIE_CRX_GTX_N11
PEG_RX#[5]	H34	PCIE_CRX_GTX_N10
PEG_RX#[6]	H31	PCIE_CRX_GTX_N9
PEG_RX#[7]	G33	PCIE_CRX_GTX_N8
PEG_RX#[8]	G30	PCIE_CRX_GTX_N7
PEG_RX#[9]	F35	PCIE_CRX_GTX_N6
PEG_RX#[10]	E34	PCIE_CRX_GTX_N5
PEG_RX#[11]	E32	PCIE_CRX_GTX_N4
PEG_RX#[12]	D33	PCIE_CRX_GTX_N3
PEG_RX#[13]	D31	PCIE_CRX_GTX_N2
PEG_RX#[14]	B33	PCIE_CRX_GTX_N1
PEG_RX#[15]	C32	PCIE_CRX_GTX_N0

PCIE_CRX_GTX_P[0..15] <23>

PEG_RX[0]	J33	PCIE_CRX_GTX_P15
PEG_RX[1]	L35	PCIE_CRX_GTX_P14
PEG_RX[2]	K34	PCIE_CRX_GTX_P13
PEG_RX[3]	H35	PCIE_CRX_GTX_P12
PEG_RX[4]	H32	PCIE_CRX_GTX_P11
PEG_RX[5]	G34	PCIE_CRX_GTX_P10
PEG_RX[6]	G31	PCIE_CRX_GTX_P9
PEG_RX[7]	F33	PCIE_CRX_GTX_P8
PEG_RX[8]	F30	PCIE_CRX_GTX_P7
PEG_RX[9]	E35	PCIE_CRX_GTX_P6
PEG_RX[10]	E33	PCIE_CRX_GTX_P5
PEG_RX[11]	F32	PCIE_CRX_GTX_P4
PEG_RX[12]	D34	PCIE_CRX_GTX_P3
PEG_RX[13]	E31	PCIE_CRX_GTX_P2
PEG_RX[14]	C33	PCIE_CRX_GTX_P1
PEG_RX[15]	B32	PCIE_CRX_GTX_P0

PCIE_CTX_GRX_N[0..15] <23>

PEG_TX#[0]	M29	PCIE_CTX_GRX_C_N15	C1	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N15
PEG_TX#[1]	M32	PCIE_CTX_GRX_C_N14	C2	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N14
PEG_TX#[2]	M31	PCIE_CTX_GRX_C_N13	C3	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N13
PEG_TX#[3]	L32	PCIE_CTX_GRX_C_N12	C4	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N12
PEG_TX#[4]	L29	PCIE_CTX_GRX_C_N11	C5	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N11
PEG_TX#[5]	K31	PCIE_CTX_GRX_C_N10	C6	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N10
PEG_TX#[6]	K28	PCIE_CTX_GRX_C_N9	C7	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N9
PEG_TX#[7]	J30	PCIE_CTX_GRX_C_N8	C8	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_N8
PEG_TX#[8]	J28	PCIE_CTX_GRX_C_N7	C9	0.1U_0402_10V7K PCIE_CTX_GRX_N7
PEG_TX#[9]	H29	PCIE_CTX_GRX_C_N6	C10	0.1U_0402_10V7K PCIE_CTX_GRX_N6
PEG_TX#[10]	G27	PCIE_CTX_GRX_C_N5	C11	0.1U_0402_10V7K PCIE_CTX_GRX_N5
PEG_TX#[11]	E29	PCIE_CTX_GRX_C_N4	C12	0.1U_0402_10V7K PCIE_CTX_GRX_N4
PEG_TX#[12]	F27	PCIE_CTX_GRX_C_N3	C13	0.1U_0402_10V7K PCIE_CTX_GRX_N3
PEG_TX#[13]	D28	PCIE_CTX_GRX_C_N2	C14	0.1U_0402_10V7K PCIE_CTX_GRX_N2
PEG_TX#[14]	F26	PCIE_CTX_GRX_C_N1	C15	0.1U_0402_10V7K PCIE_CTX_GRX_N1
PEG_TX#[15]	E25	PCIE_CTX_GRX_C_N0	C16	0.1U_0402_10V7K PCIE_CTX_GRX_N0

PCIE_CTX_GRX_P[0..15] <23>

PEG_TX[0]	M28	PCIE_CTX_GRX_C_P15	C17	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P15
PEG_TX[1]	M33	PCIE_CTX_GRX_C_P14	C18	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P14
PEG_TX[2]	M30	PCIE_CTX_GRX_C_P13	C19	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P13
PEG_TX[3]	L31	PCIE_CTX_GRX_C_P12	C20	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P12
PEG_TX[4]	L28	PCIE_CTX_GRX_C_P11	C21	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P11
PEG_TX[5]	K30	PCIE_CTX_GRX_C_P10	C22	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P10
PEG_TX[6]	K27	PCIE_CTX_GRX_C_P9	C23	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P9
PEG_TX[7]	J29	PCIE_CTX_GRX_C_P8	C24	NI3P@0.1U_0402_10V7K PCIE_CTX_GRX_P8
PEG_TX[8]	J27	PCIE_CTX_GRX_C_P7	C25	0.1U_0402_10V7K PCIE_CTX_GRX_P7
PEG_TX[9]	H28	PCIE_CTX_GRX_C_P6	C26	0.1U_0402_10V7K PCIE_CTX_GRX_P6
PEG_TX[10]	G28	PCIE_CTX_GRX_C_P5	C27	0.1U_0402_10V7K PCIE_CTX_GRX_P5
PEG_TX[11]	E28	PCIE_CTX_GRX_C_P4	C28	0.1U_0402_10V7K PCIE_CTX_GRX_P4
PEG_TX[12]	F28	PCIE_CTX_GRX_C_P3	C29	0.1U_0402_10V7K PCIE_CTX_GRX_P3
PEG_TX[13]	D27	PCIE_CTX_GRX_C_P2	C30	0.1U_0402_10V7K PCIE_CTX_GRX_P2
PEG_TX[14]	E26	PCIE_CTX_GRX_C_P1	C31	0.1U_0402_10V7K PCIE_CTX_GRX_P1
PEG_TX[15]	D25	PCIE_CTX_GRX_C_P0	C32	0.1U_0402_10V7K PCIE_CTX_GRX_P0

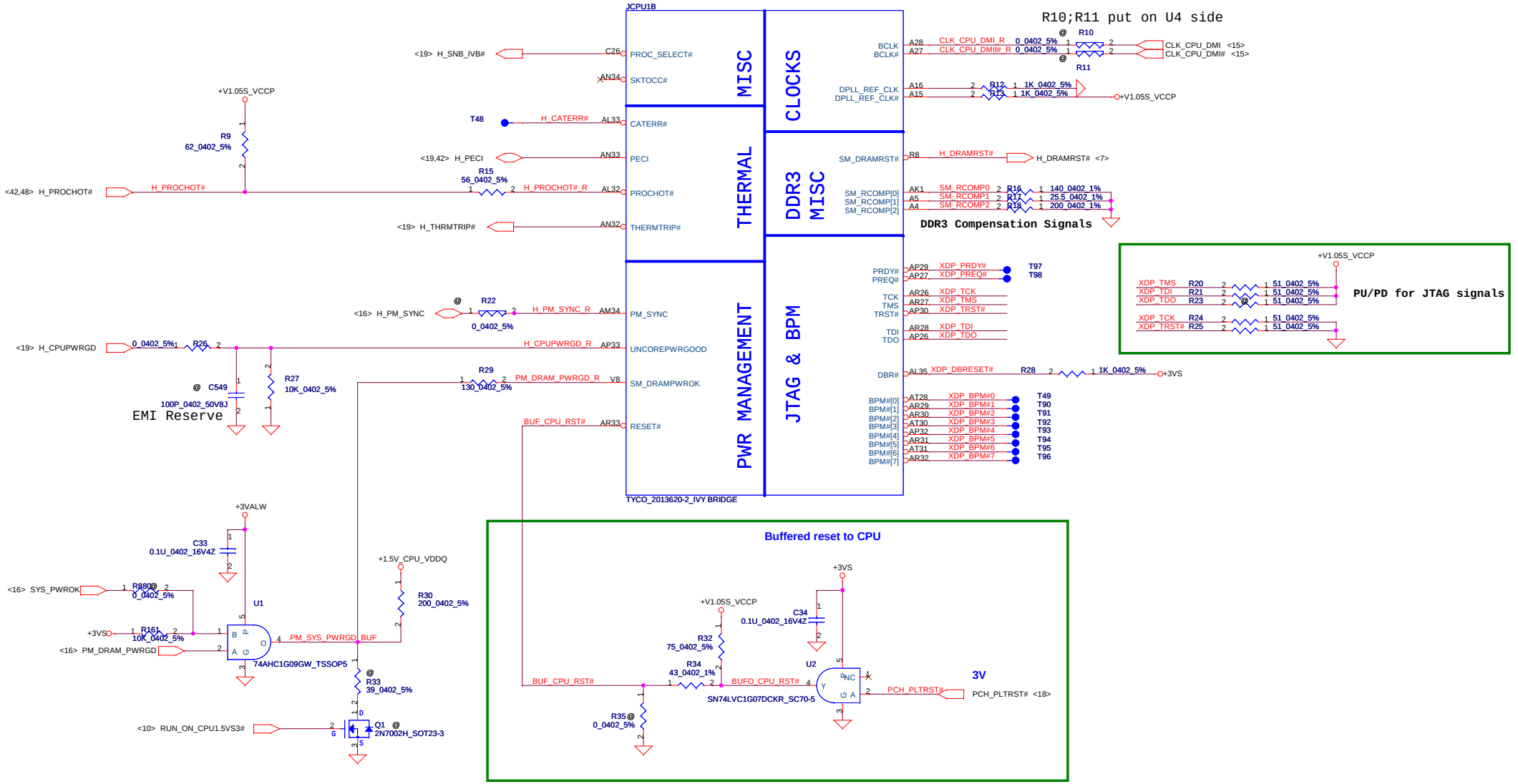
TYCO_2013620-2_IVY BRIDGE

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PROCESSOR(1/7) DMI,FDI,PEG

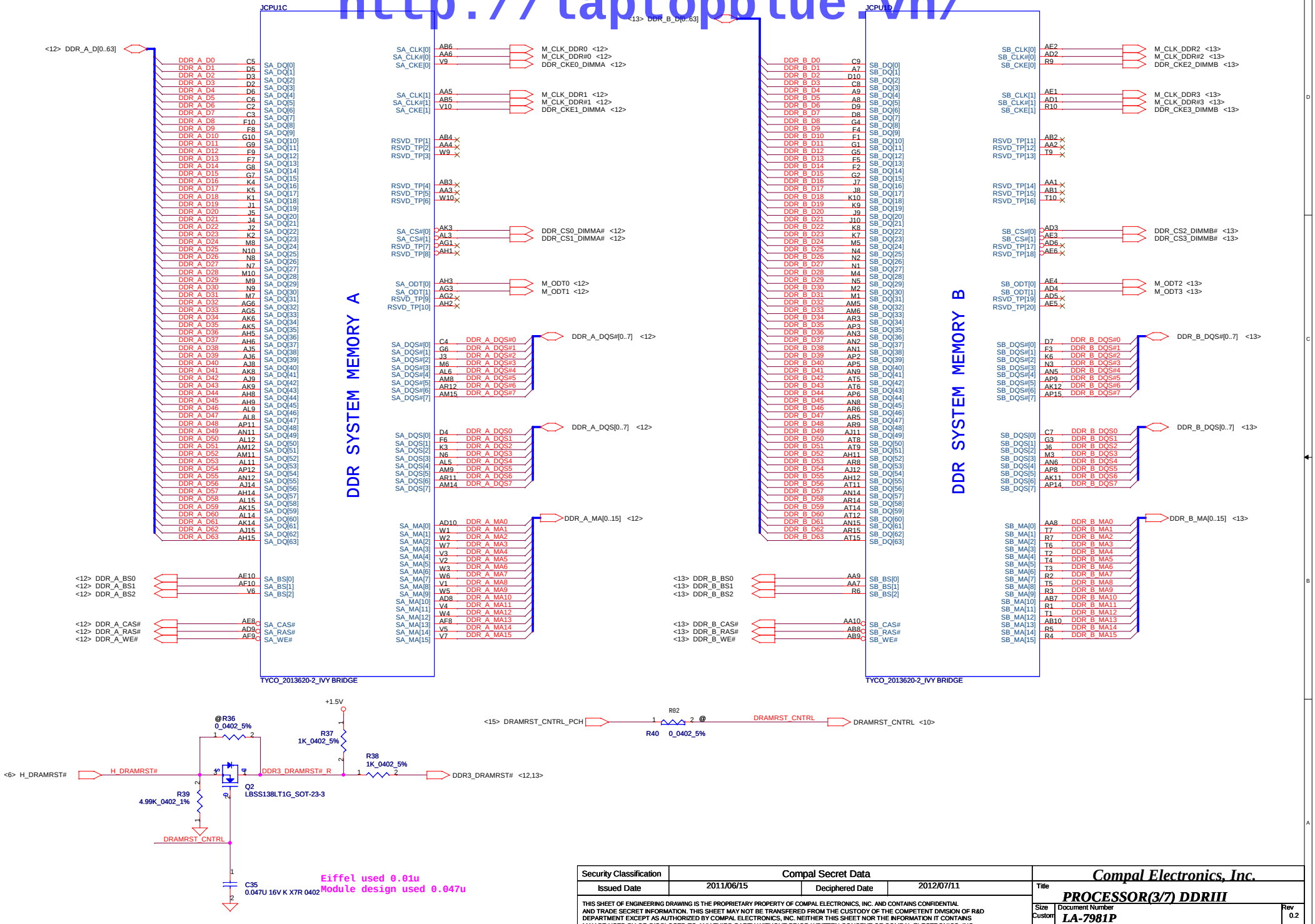
Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 5 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	PROCESSOR(2/7) PM,XDP,CLK		
Size	Document Number		Rev
Custom	LA-7981P		0.2
Date:	Tuesday, February 14, 2012	Sheet	6 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

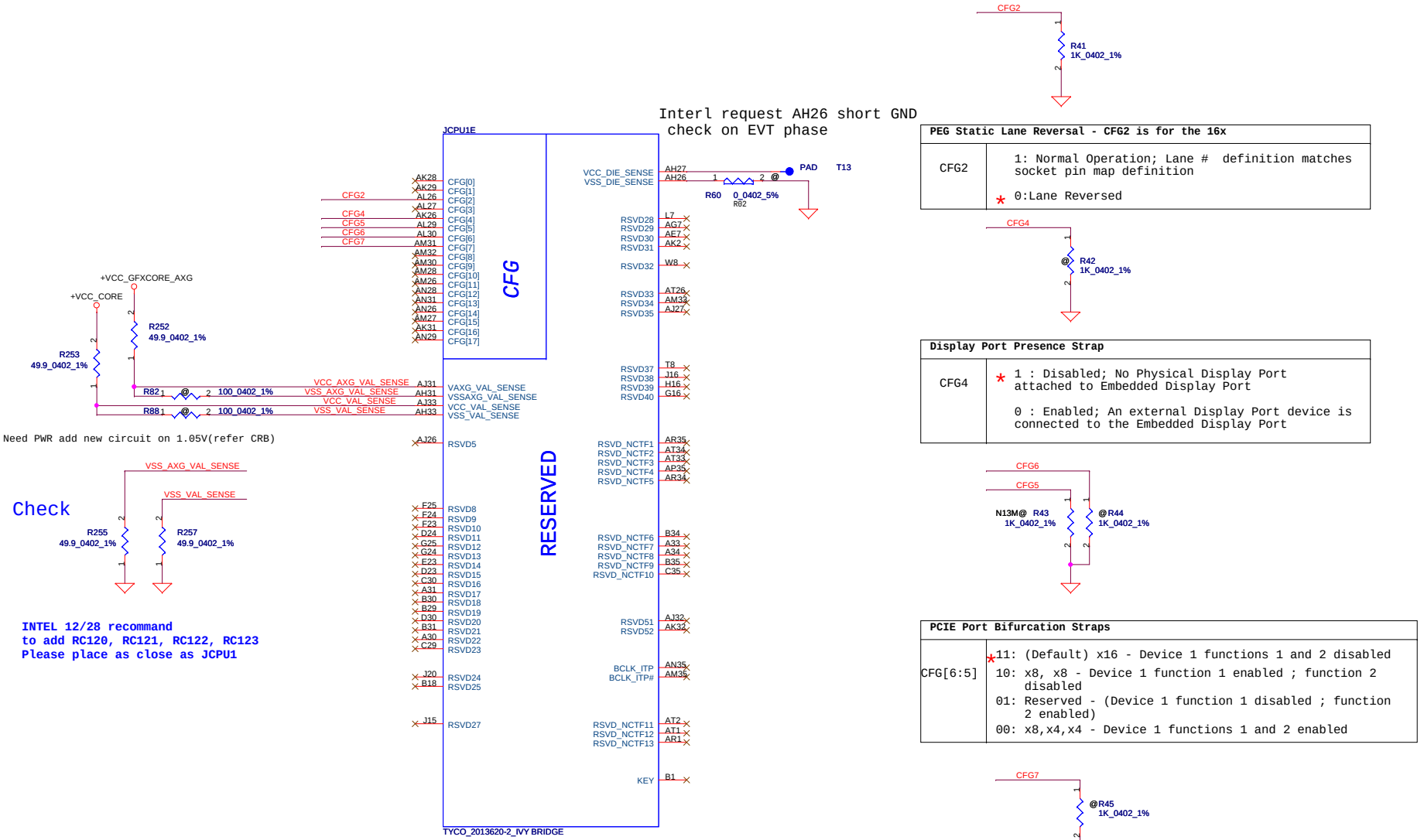
Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 7 of 60

CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 8 of 60

POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

TYCO_2013620-2_IVY BRIDGE

+V1.05S_VCCP

C99 0.1U_0402_10V6K

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# VIDSCLK VIDSOUT

H_CPU_SVIDALRT# R47 43_0402_5%

H_CPU_SVIDCLK 0_0402_5% R48 @

H_CPU_SVIDDAT 0_0402_5% R49 @

VR_SVID_ALRT# <55>
VR_SVID_CLK <55>
VR_SVID_DAT <55>

R50 130_0402_5% +V1.05S_VCCP

0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

+VCC_CORE

R51 100_0402_1%

VCC_SENSE VSS_SENSE

VCCSENSE_R R52 @0_0402_5%

VSSSENSE_R R53 @0_0402_5%

VCCSENSE <55>
VSSSENSE <55>

VCCIO_SENSE VSS_SENSE_VCCIO

VSSIO_SENSE_L R74 10_0402_1% VSSIO_SENSE

VCCIO_SENSE <52,53>

R66 @ 100_0402_1%

R54 100_0402_1%

R74 & R79 put together

VSSIO_SENSE_L <53>

R79 10_0402_1%

+V1.05S_VCCP

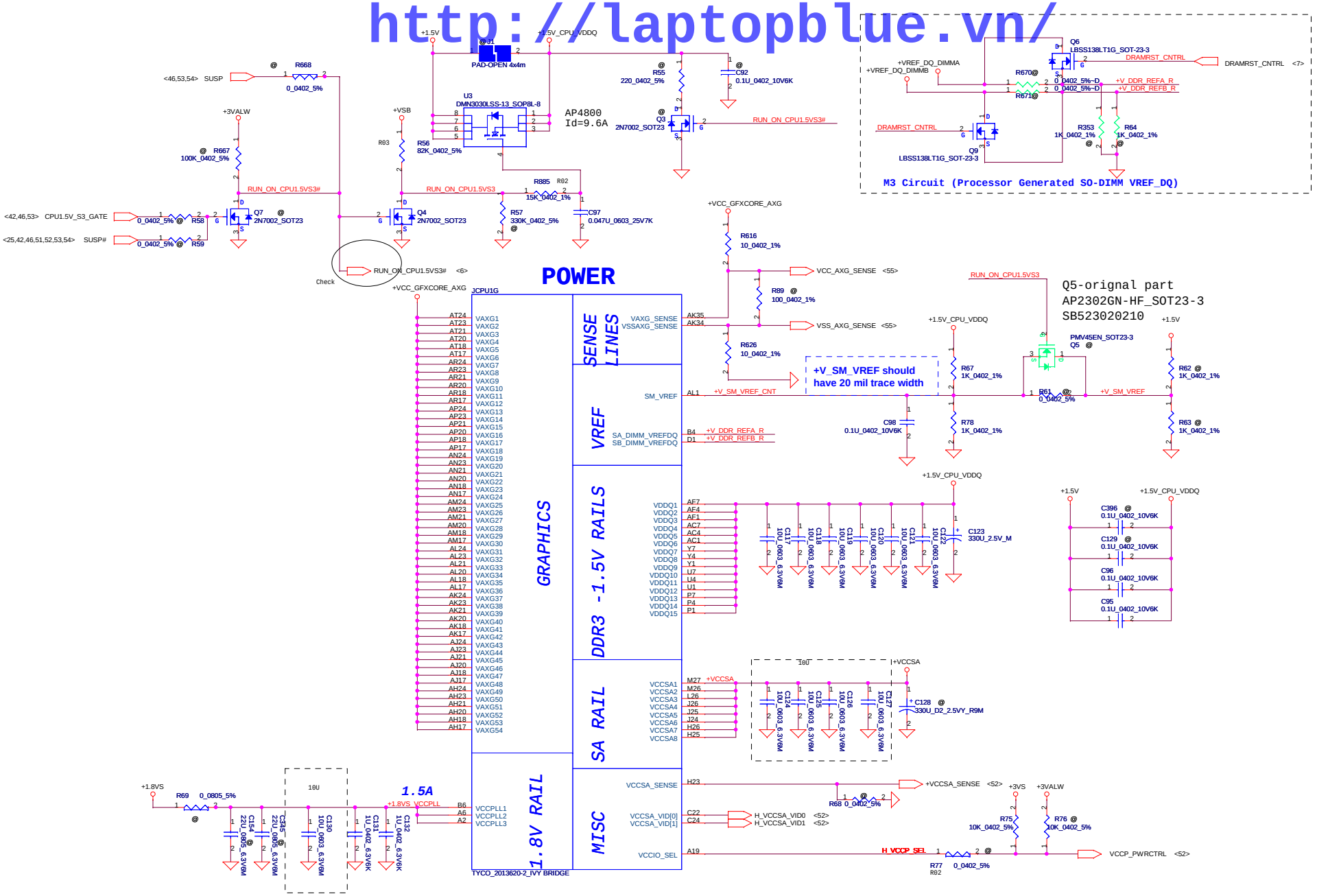
VSS_SENCE 100ohm +-1% pull-down to GND near processor

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: LA-7981P | Rev: 0.2

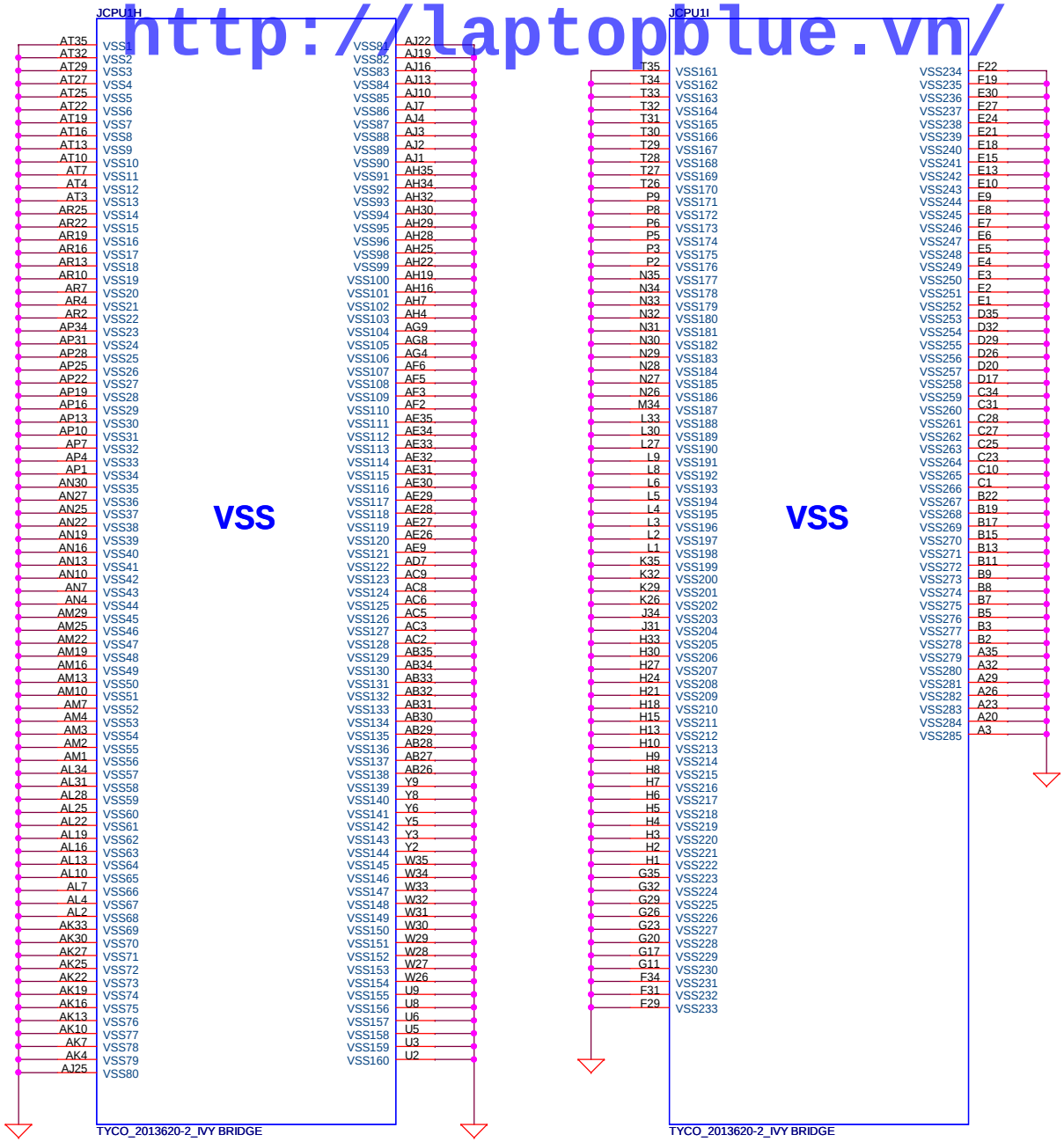
Date: Tuesday, February 14, 2012 | Sheet 9 of 60



IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0
Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: LA-7981P		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 10 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **PROCESSOR(7/7) VSS**

Size	Document Number	Rev
Custom	LA-7981P	0.2

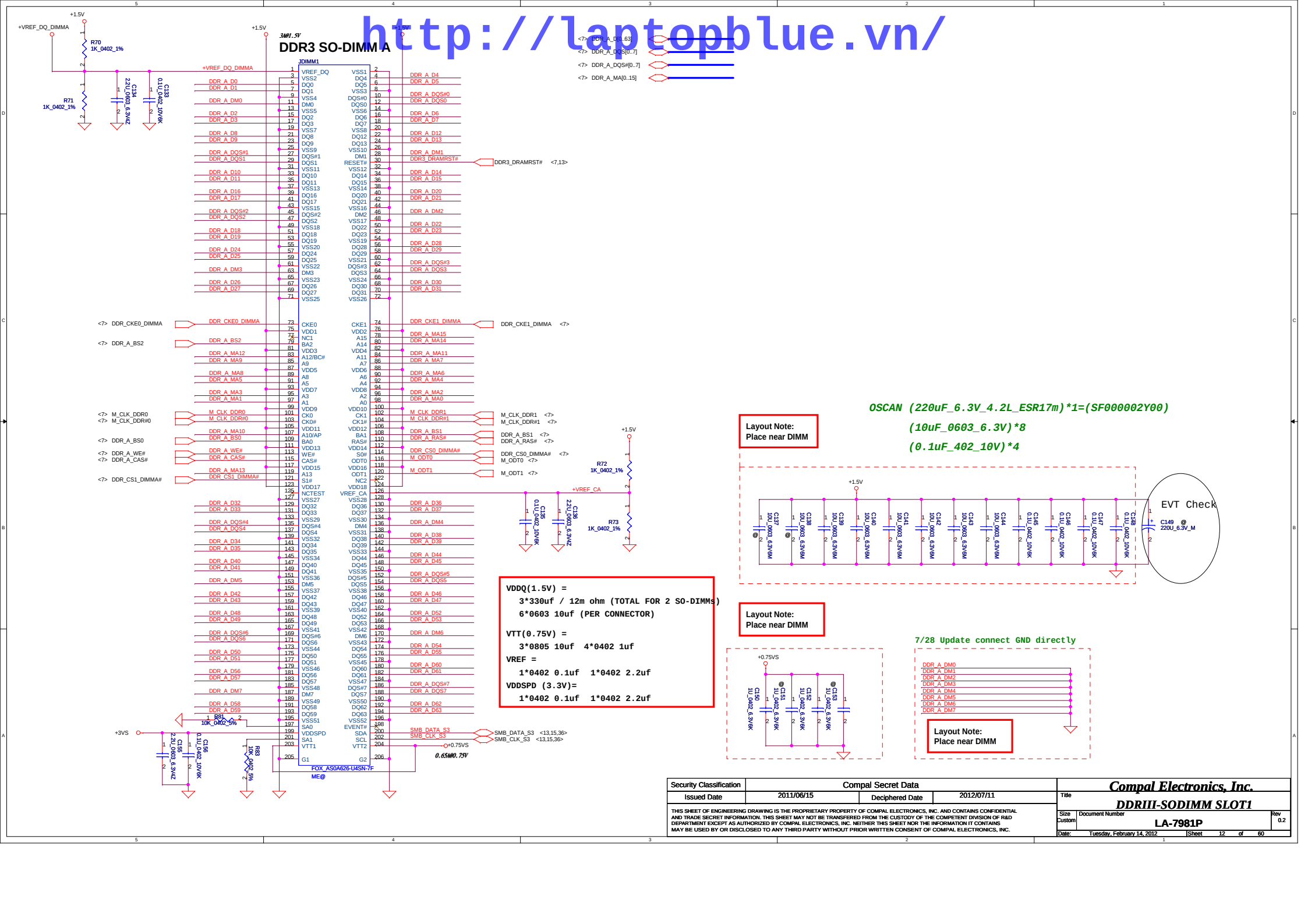
Date: Tuesday, February 14, 2012 | Sheet 11 of 60

DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@



VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

7/28 Update connect GND directly

Layout Note:
Place near DIMM

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: LA-7981P | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 12 of 60

For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

JDIMM2

FOX_AS0A626-U8SN-7F
ME@

<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_MA[0..15]

DDR3_DRAMRST# <7,12>
DDR_CKE3_DIMMB <7>
M_CLK_DDR3 <7>
M_CLK_DDR#3 <7>
DDR_B_BS1 <7>
DDR_B_RAS# <7>
DDR_CS2_DIMMB# <7>
M_ODT2 <7>
M_ODT3 <7>
SMB_DATA_S3 <12,15,36>
SMB_CLK_S3 <12,15,36>
+0.75VS

Layout Note: Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note: Place near DIMM

Layout Note: Place near DIMM

```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf

  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size | Document Number: **LA-7981P** | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 13 of 60

W=20mils +RTCVCC R99 1K_0402_5% C179 1U_0603_10V4Z
W=20mils +RTCBATT CLRP1 SHORT PADS

PCH_RTCX1 PCH_RTCX2 R98 10M_0402_5% Y1 32.768KHZ_12.5PF_CM31532768DZFT C180 18P_0402_50V8J C181 18P_0402_50V8J

+RTCVCC R101 1M_0402_5% SM_INTRUDER# R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN

* H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS R105 @ 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
* LOW= Disable (Default)

+3V_PCH R106 @ 1K_0402_5% HDA_SDOUT

* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
* 1.8V when sampled low
Needs to be pulled High for Chief River platfrom

<41> HDA_BITCLK_AUDIO R112 33_0402_5% HDA_BIT_CLK
<41> HDA_SYNC_AUDIO R114 33_0402_5% HDA_SYNC_R
<41> HDA_RST_AUDIO# R116 33_0402_5% HDA_RST#
<41> HDA_SDOUT_AUDIO R118 33_0402_5% HDA_SDOUT

+3V_PCH R121 @ 200_0402_5% PCH_JTAG_TDO R125 @ 100_0402_1%
+3V_PCH R122 @ 200_0402_5% PCH_JTAG_TMS R126 @ 100_0402_1%
+3V_PCH R123 @ 200_0402_5% PCH_JTAG_TDI R128 @ 100_0402_1%

DPDG1.1

CMOS
+RTCVCC C183 1U_0603_10V4Z R103 20K_0402_5% R100 20K_0402_5% C182 1U_0603_10V4Z
CLRP2 SHORT PADS CLRP3 SHORT PADS

PCH_RTCX1 PCH_RTCX2 PCH_RTCRST# PCH_SRTCRST# SM_INTRUDER# PCH_INTVRMEN

U4A

RTCX1	A20	RTC	
RTCX2	C20		
RTCRST#	D20		
SRTCRST#	G22		
INTRUDER#	K22		
INTVRMEN	C17		
HDA_BCLK	N34	IHDA	
HDA_SYNC	L34		
SPKR	T10		
HDA_RST#	K34		
HDA_SDIN0	E34		
HDA_SDIN1	G34		
HDA_SDIN2	C34		
HDA_SDIN3	A34		
HDA_SDO	A36		
HDA_DOCK_EN# / GPIO33	C36		
HDA_DOCK_RST# / GPIO13	N32		
JTAG_TCK	J3	JTAG	
JTAG_TMS	H7		
JTAG_TDI	K5		
JTAG_TDO	H1		
SPI_CLK	T3	SPI	
SPI_CS0#	Y14		
SPI_CS1#	T1		
SPI_MOSI	V4		
SPI_MISO	U3		

PANTHER-POINT_FCBGA989

<42> ME_FLASH R109 0_0402_5% HDA_SDOUT
R107 @ 1K_0402_1% PCH_GPIO33
+3V_PCH 10K_0402_5% R264 @

PCH_JTAG_TCK R110 51_0402_5% PCH_JTAG_TMS PCH_JTAG_TDI PCH_JTAG_TDO

+5VS Q10 LBSS138LT1G_SOT-23-3 HDA_SYNC
R878 1M_0402_5% R175 @ 0_0402_5%

SPI_CLK_PCH_R SPI_SB_CS0# SPI_SB_CS1# SPI_SI SPI_SO_R

check with vender
Del Q10 check with codec
VDDIO using 3VALW

SPI_CLK_PCH_R R124 33_0402_5% @ C190 22P_0402_50V8J @

R124;c190 close to U4.T3 pin

LPC
FWH0 / LAD0 C38 LPC_AD0 — LPC_AD0 <36,42>
FWH1 / LAD1 A38 LPC_AD1 — LPC_AD1 <36,42>
FWH2 / LAD2 B37 LPC_AD2 — LPC_AD2 <36,42>
FWH3 / LAD3 C37 LPC_AD3 — LPC_AD3 <36,42>
FWH4 / LFRAME# D36 LPC_FRAME# — LPC_FRAME# <36,42>
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 — SERIRQ <42>

EC and Mini card debug port

+3VS R104 10K_0402_5%

SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7 — SATA_ITX_C_DRX_N0 0.01U_0402_25V7K — C184 — SATA_ITX_DRX_N0
SATA0TXP AP5 — SATA_ITX_C_DRX_P0 0.01U_0402_25V7K — C185 — SATA_ITX_DRX_P0
CAP on Conn, side

SATA_DTX_C_IRX_N0 SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0 <40>
SATA_DTX_C_IRX_P0 <40>
SATA_ITX_DRX_N0 <40>
SATA_ITX_DRX_P0 <40>
HDD

SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10

SATA
SATA2RXN AD7 — SATA_DTX_C_IRX_N2
SATA2RXP AD5 — SATA_DTX_C_IRX_P2
SATA2TXN AH5 — SATA_ITX_C_DRX_N2
SATA2TXP AH4 — SATA_ITX_C_DRX_P2

SATA_DTX_C_IRX_N2 <40>
SATA_DTX_C_IRX_P2 <40>
SATA_ITX_C_DRX_N2 <40>
SATA_ITX_C_DRX_P2 <40>
ODD

SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1

SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1

SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11
SATAICOMPI Y10 — SATA_COMP — R111 37.4_0402_1% — +1.05VS_VCC_SATA

SATA3RCOMPO AB12
SATA3COMPI AB13 — SATA3_COMP — R113 49.9_0402_1% — +1.05VS_SATA3

SATA3RBIAS AH1 — RBIAS_SATA3 — R115 750_0402_1%

SATALED# P3 — SATALED# — R117 10K_0402_5% — +3VS
SATA0GP / GPIO21 V14 — PCH_GPIO21 — R119 10K_0402_5% — +3VS
SATA1GP / GPIO19 P1 — BBS_BIT0_R — R187 10K_0402_5% — +3VS

+3VS R266 3.3K_0402_5% SPI_WP#1
R221 3.3K_0402_5% SPI_HOLD#1
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#

8MB SPI ROM FOR ME
& Non-share ROM.

R291 0_0402_5% SPI_SB_CS1# SPI_SO_R R188 33_0402_5%
U6 CS# SO WP# GND VCC HOLD# SCLK SI
SPI_CS1# SPI_SO1 SPI_WP#1 SPI_HOLD#1 SPI_CLK1 SPI_SI1
R199 0_0402_5% SPI_CLK_PCH_R SPI_SI R196 33_0402_5%
16M W25Q16BVSSIG SOIC 8P

U6 Rersver 4M+2M Solution

R130 0_0402_5% SPI_SB_CS0# SPI_SO_R R131 33_0402_5%
U5 CS# SO WP# GND VCC HOLD# SCLK SI
SPI_CS0# SPI_SO_L SPI_WP#
C191 0.1U_0402_16V4Z
R132 0_0402_5% SPI_HOLD# SPI_CLK_PCH SPI_SI_R R133 33_0402_5%
32M W25Q32BVSSIG SOIC 8P

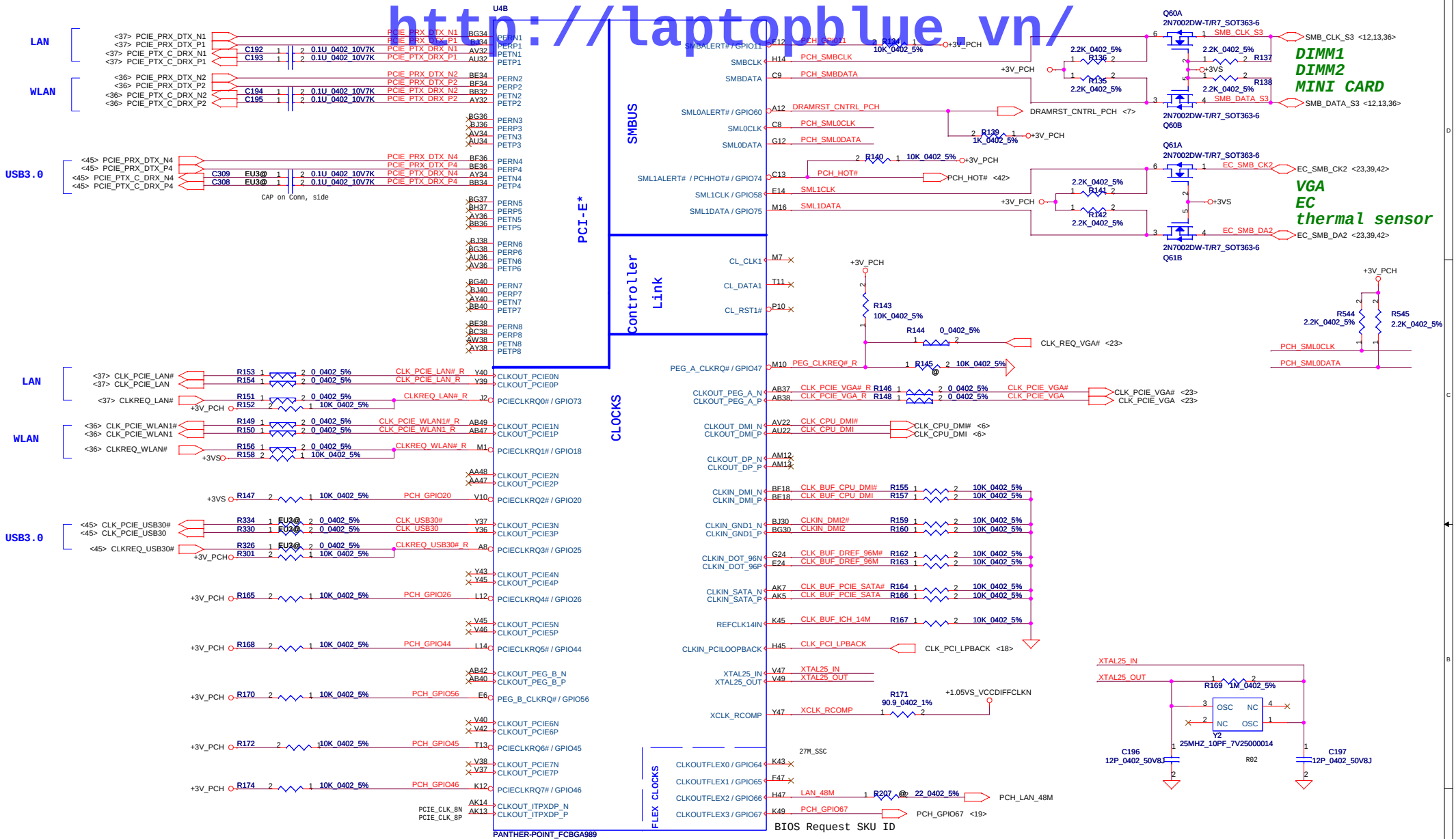
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 14 of 60



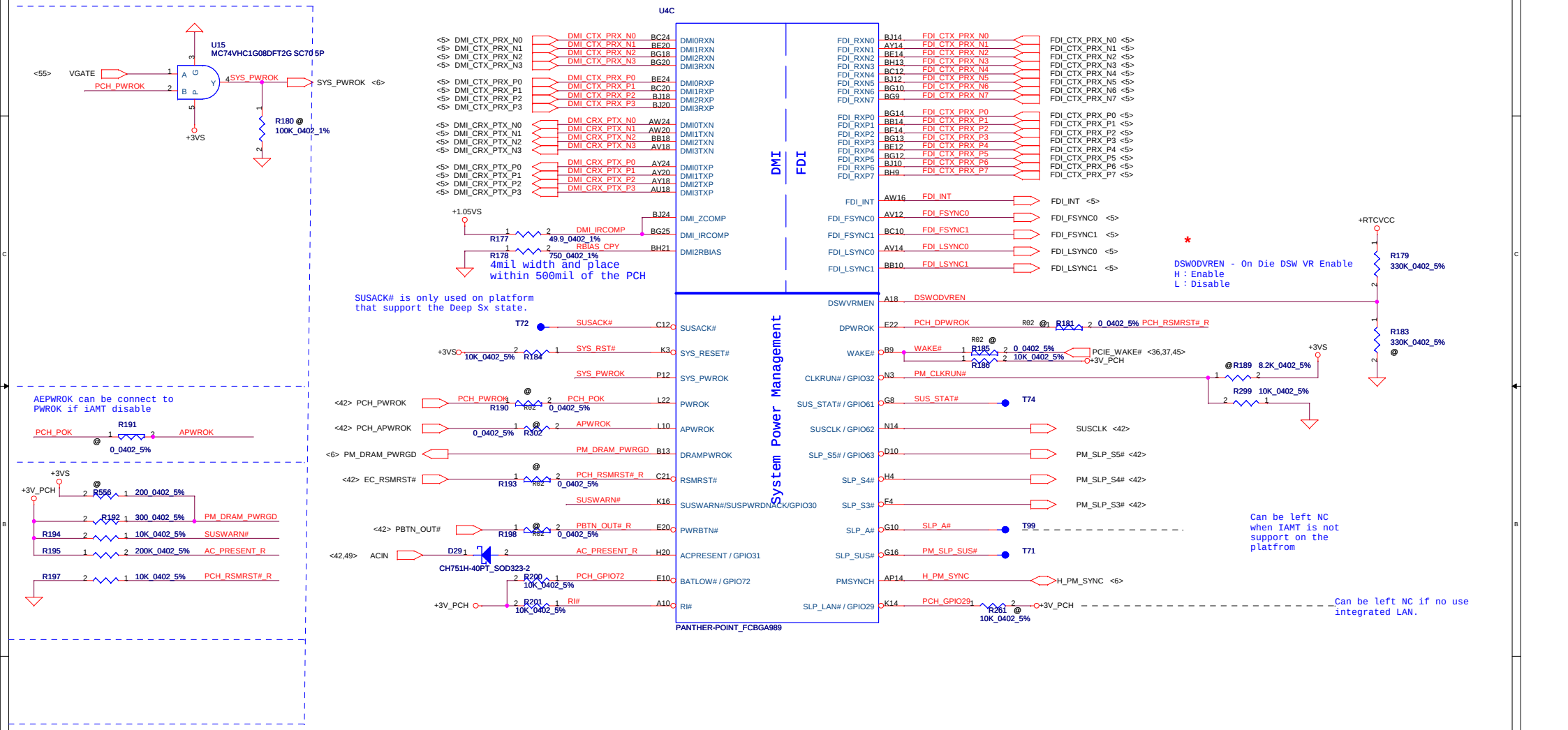
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 15 of 60



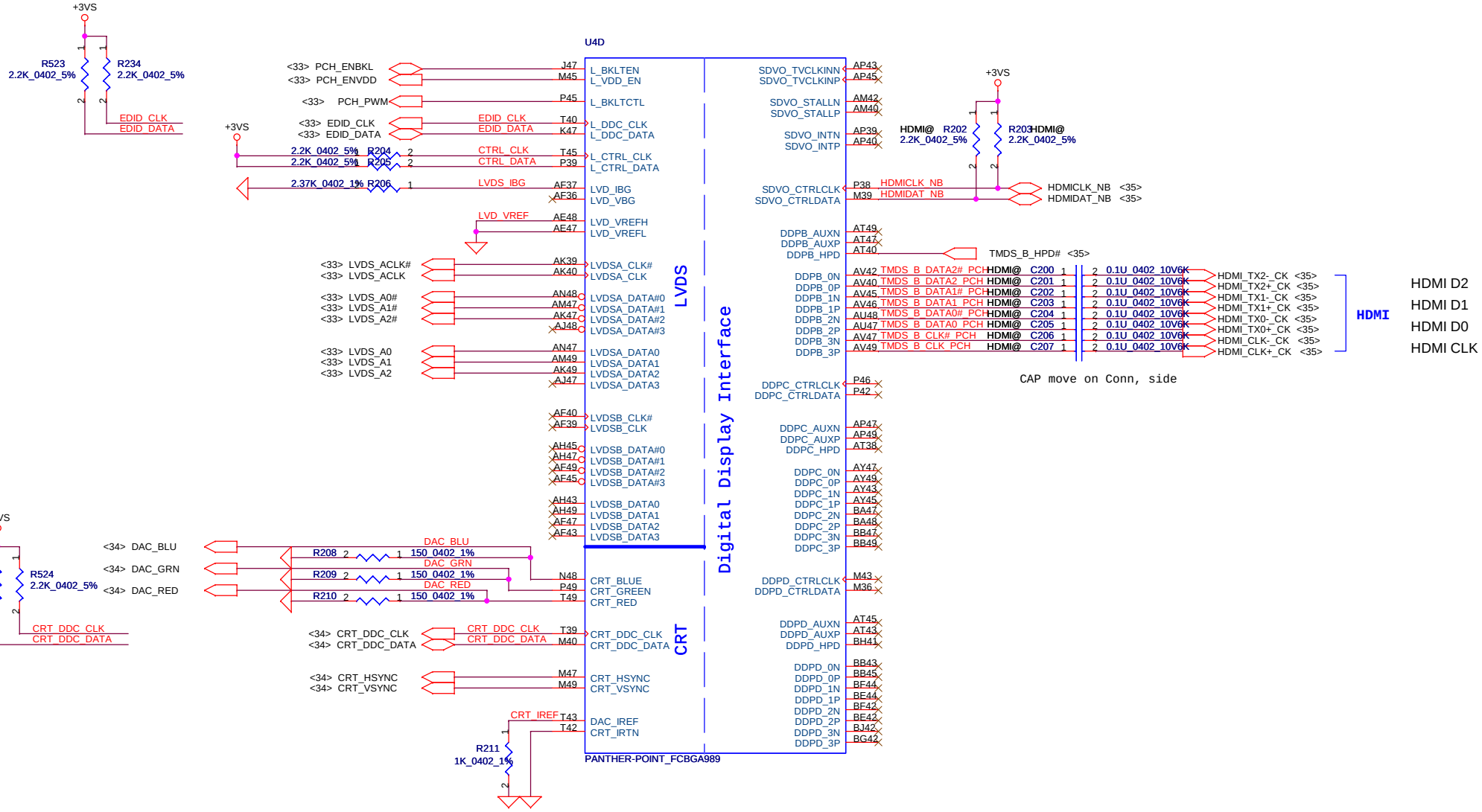
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 16 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size B	Document Number LA-7981P		Rev 0.2
Date: Tuesday, February 14, 2012	Sheet 17 of 60		

+3VS

RP2: PCI_PIRQA#, PCI_PIRQD#, PCI_PIRQC#, PCI_PIRQB# — 8.2K_0804_8P4R_5%

RP1: PCH_GPIO2, DGPU_PWR_EN_R, PCH_GPIO4, ODD_DA#_R — 8.2K_0804_8P4R_5%

R213	8.2K_0402_5%	PCH_GPIO5	
R225	8.2K_0402_5%	PCH_WL_OFF#	
R292	@ 8.2K_0402_5%	PCH_GPIO51	PPT EDS DOC#474146
R557	@ 8.2K_0402_5%	PCH_GPIO53	
R259	8.2K_0402_5%	DGPU_PWR_EN1	
R212	8.2K_0402_5%	DGPU_HOLD_RST#_R	
R214	@ 8.2K_0402_5%	DGPU_HOLD_RST#_R	

Boot BIOS Strap bit1 BBS1

	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	Reserved
	1	1	* SPI (Default)
	0	0	LPC

DGPU_PWR_EN_R — R319 @ — NVDD_PWR_EN 0_0402_5%

GPIO55

PCH_WL_OFF# — R215 @ 1K_0402_5%

A16 swap overide Strap/Top-Block Swap Override jumper

PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

U4E — PANTHER-POINT_FCBGA989

RSVD: TP1–TP24 (BG26, BJ26, BH25, BJ16, BG16, AH38, AH37, AK43, AK45, C18, N30, H3, AH12, AM4, AM5, Y13, K24, L24, AB46, AB45, B21, M20, AY16, BG46); RSVD1–RSVD29 (AY7, AV7, AU3, BG4, AT10, BC8, AU2, AT4, AT3, AT1, AY3, AT5, AV3, AV1, BB1, BA3, BB5, BB3, BB7, BE8, BD4, BF6, AV5, AV10, AT8, AY5, BA2, AT12, BF3)

USB3: USB3_RX1_N, USB3_RX3_N, USB3_RX4_N, USB3_RX1_P, USB3_RX3_P, USB3_RX4_P, USB3_TX1_N, USB3_TX3_N, USB3_TX4_N, USB3_TX1_P, USB3_TX3_P, USB3_TX4_P

PCI: PCI_PIRQA#, PCI_PIRQB#, PCI_PIRQC#, PCI_PIRQD#; DGPU_HOLD_RST# R553, NVDD_PWR_EN R692, DGPU_PWR_EN R691; PCH_GPIO51, PCH_GPIO53, PCH_WL_OFF#; ODD_DA# R715; PCH_GPIO2, PCH_GPIO4, PCH_GPIO5; PCI_PME#; PCH_PLTRST#; CLK_PCI_LPBACK R219, CLK_PCI_EC R220, CLK_PCI_DB R173

USB: USBP0N/P — USB20_N1/P1 (CR-B/D USB); USBP1N/P — USB20_N2/P2 (LEFT USB); USBP2N/P — USB20_N3/P3 (LEFT USB); USB DEBUG=PORT1 AND PORT9; USBP5N/P — USB20_N5/P5 (USB Camera); USBP9N/P — USB20_N9/P9 (RIGHT USB); USBP10N/P — USB20_N10/P10 (WLAN); USBP11N/P — USB20_N11/P11 (CARD READER); USBP13N/P — USB20_N13/P13 (Bluetooth)

USBRBIAS — R218 22.6_0402_1% Within 500 mils

USB_OC0# Share with USB_OC4# due to same power switch

OC0#/GPIO59 — USB_OC1#, USB_OC4#; OC1#/GPIO40 — USB_OC2#; OC2#/GPIO41 — USB_OC3#; OC3#/GPIO42 — USB_OC4#; OC4#/GPIO43 — USB_OC5#; OC5#/GPIO9 — SMIB; OC6#/GPIO10 — USB_OC7#

RP3: 10K_1206_8P4R_5% — USB_OC5#, USB_OC2#, USB_OC7#

RP4: 10K_1206_8P4R_5% — USB_OC1#, USB_OC4#, USB_OC3#

+3V_PCH

R03: SMIB — R262 10K_0402_5%

R222 0_0402_5%

<23,36,37,42,45> PLT_RST# — U7@ MC74VHC1G08DFT2G SC70 5P — PCH_PLTRST#

C208 @ 1U_0402_6.3V4Z

R223 100K_0402_5% — +3VS

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: LA-7981P | Rev: 0.2

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PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

PCH_GPIO70	Function
0	14/15"
1	17"

PCH_GPIO071	
0	USB3.0 by PCH
1	USB3.0 by NEC

+3V_PCH — Weak internal pull-high — R235 10K_0402_5% — EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 @ 1K_0402_5% — PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 @ 10K_0402_5% — PCH_GPIO27

<46,54> DGPU_PWROK — PU on power side — DGPU_PWROK_R

<36> BT_DISABLE — BT_DISABLE

<40> ODD_EN — ODD_EN

<36,40> PCH_BT_ON#

R244 @ 10K_0402_5% — PCH_GPIO37 — R881 10K_0402_5%

R250 @ 10K_0402_5% — PCH_GPIO36 — R547 10K_0402_5%

BIOS Request SKU ID

R711 @ 10K_0402_5% — PCH_GPIO38

R246 @ 10K_0402_5% — PCH_GPIO67 — PCH_GPIO67 <15>

R709 10K_0402_5%

R293 10K_0402_5%

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

U4F — PANTHER-POINT_FCBGA989

GPIO:
BMBUSY# / GPIO0 (T7)
TACH1 / GPIO1 (A42) — PCH_GPIO1
TACH2 / GPIO6 (H36) — PCH_GPIO6
TACH3 / GPIO7 (E38) — EC_SCI#
GPIO8 (C10) — EC_SMI#
LAN_PHY_PWR_CTRL / GPIO12 (C4) — PCH_GPIO12
GPIO15 (G2) — EC_LID_OUT#
SATA4GP / GPIO16 (U2) — PCH_GPIO16
TACH0 / GPIO17 (D40) — DGPU_PWROK_R
SCLOCK / GPIO22 (T5) — BT_DISABLE
GPIO24 (E8) — ODD_EN
GPIO27 (E16) — PCH_GPIO27
GPIO28 (P8) — PCH_GPIO28
STP_PCI# / GPIO34 (K1) — PCH_BT_ON#
GPIO35 (K4) — PCH_GPIO35
SATA2GP / GPIO36 (V8) — PCH_GPIO36
SATA3GP / GPIO37 (M5) — PCH_GPIO37
SLOAD / GPIO38 (N2) — PCH_GPIO38
SDATAOUT0 / GPIO39 (M3) — PCH_GPIO39
SDATAOUT1 / GPIO48 (V13) — PCH_GPIO48
SATA5GP / GPIO49 / TEMP_ALERT# (V3) — PCH_GPIO49
GPIO57 (D6) — PCH_GPIO57

CPU/MISC:
TACH4 / GPIO68 (C40) — PCH_GPIO68
TACH5 / GPIO69 (B41) — PCH_GPIO69
TACH6 / GPIO70 (C41) — PCH_GPIO70
TACH7 / GPIO71 (A40) — PCH_GPIO71
A20GATE (P4) — GATEA20 <42>
PECI (AU16) — PCH_PECI_R — H_PECI <6,42>
RCIN# (P5) — KBRST# — KBRST# <42>
PROCPWRGD (AY11) — H_CPUPWRGD <6>
THRMTRIP# (AY10) — PCH_THRMTRIP#_R — H_THRMTRIP# <6>
INIT3_3V# (T14)
DF_TVS (AY1)
TS_VSS1 (AH8)
TS_VSS2 (AK11)
TS_VSS3 (AH10)
TS_VSS4 (AK10)
NC_1 (P37) — NV_CLE

NCTF:
VSS_NCTF_1 (A4)
VSS_NCTF_2 (A44)
VSS_NCTF_3 (A45)
VSS_NCTF_4 (A46)
VSS_NCTF_5 (A5)
VSS_NCTF_6 (A6)
VSS_NCTF_7 (B3)
VSS_NCTF_8 (B47)
VSS_NCTF_9 (BD1)
VSS_NCTF_10 (BD49)
VSS_NCTF_11 (BE1)
VSS_NCTF_12 (BE49)
VSS_NCTF_13 (BF1)
VSS_NCTF_14 (BF49)
VSS_NCTF_15 (BG2)
VSS_NCTF_16 (BG48)
VSS_NCTF_17 (BH3)
VSS_NCTF_18 (BH47)
VSS_NCTF_19 (BJ4)
VSS_NCTF_20 (BJ44)
VSS_NCTF_21 (BJ45)
VSS_NCTF_22 (BJ46)
VSS_NCTF_23 (BJ5)
VSS_NCTF_24 (BJ6)
VSS_NCTF_25 (C2)
VSS_NCTF_26 (C48)
VSS_NCTF_27 (D1)
VSS_NCTF_28 (D49)
VSS_NCTF_29 (E1)
VSS_NCTF_30 (E49)
VSS_NCTF_31 (F1)
VSS_NCTF_32 (F49)

R236 10K_0402_5% — GATEA20 <42>

KBRST# — R226 10K_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

R216 2.2K_0402_5% — H_SNB_IVB# <6>

R217 1K_0402_5% — CLOSE TO THE BRANCHING POINT

Weak internal PU,Do not pull low

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (6/9) GPIO, CPU, MISC
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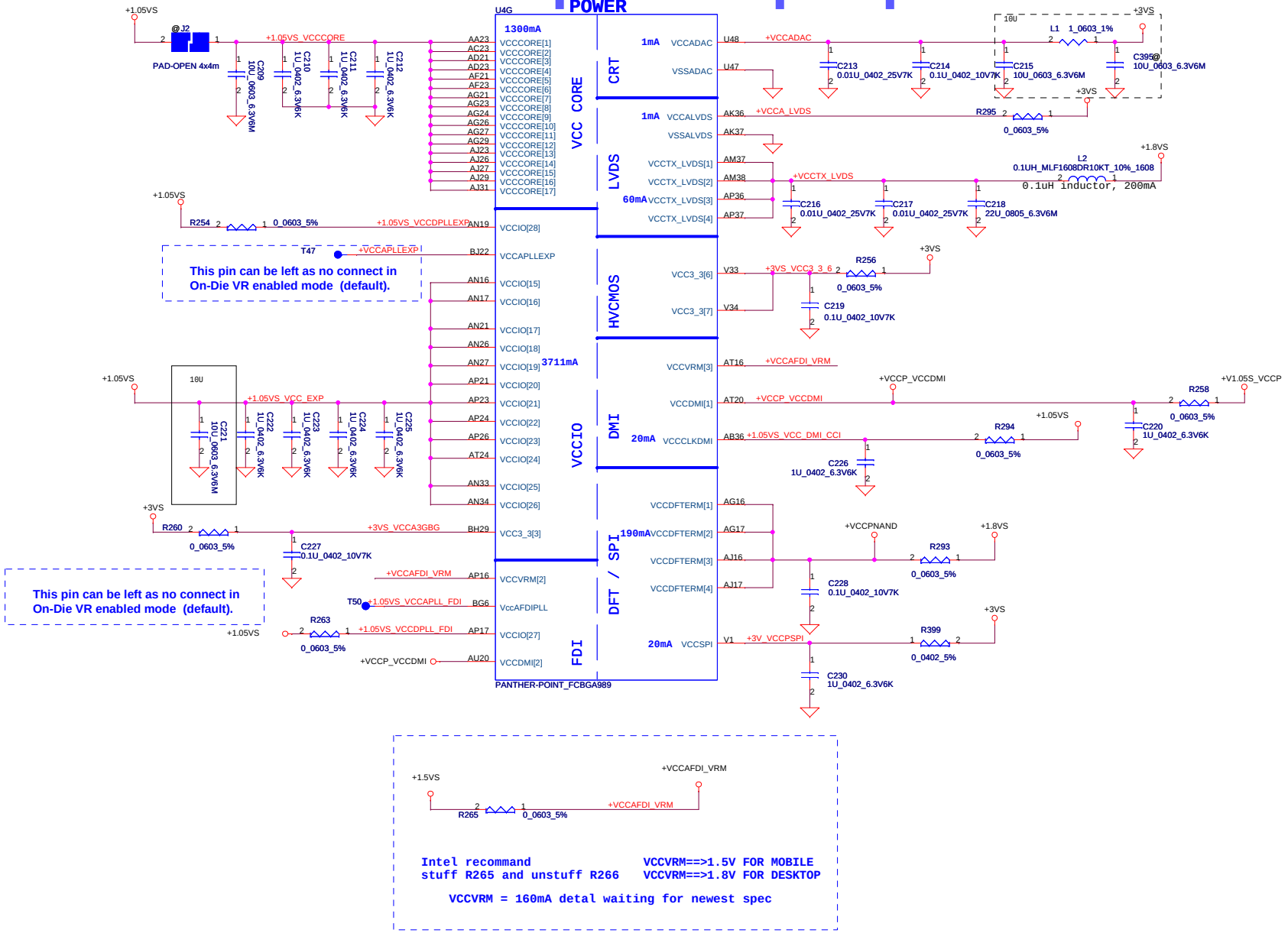
Compal Electronics, Inc.



L1 Change to 1 ohm P/N
S RES 1/10W 1 +-1% 0603

PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-7981P | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 20 of 60

Have Internal VRM

POWER

U4J

PANTHER-POINT_FCBGA989

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2
,VCCAPLLSATA

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2
,VCCAPLLSATA

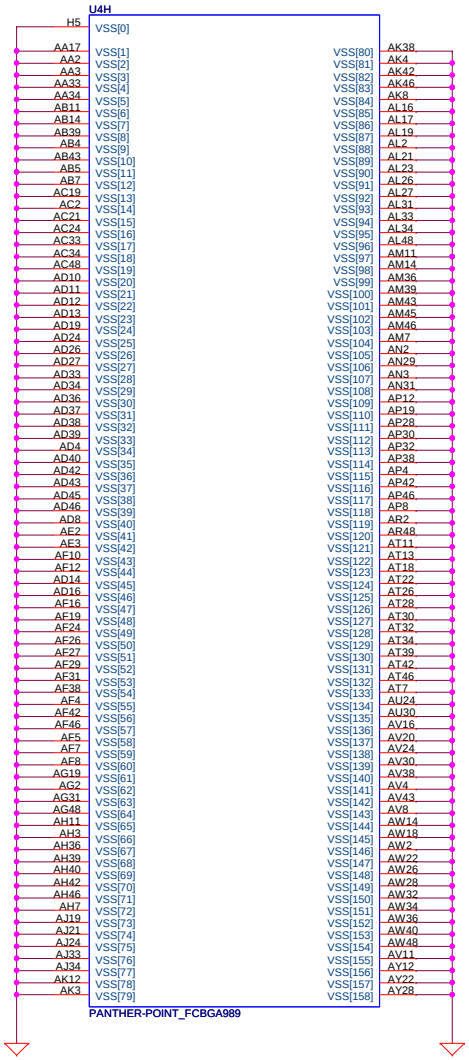
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

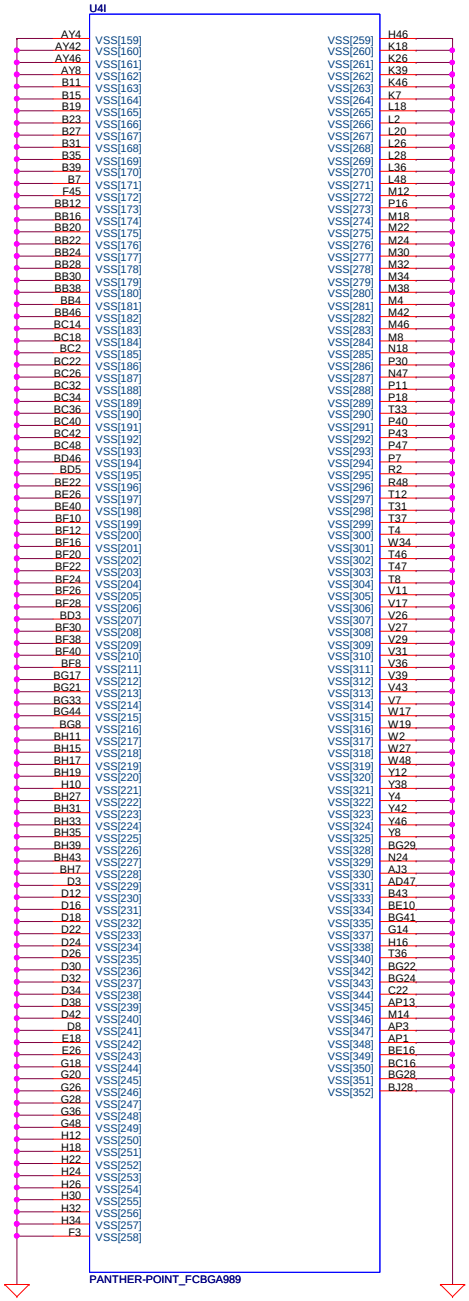
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-7981P | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 21 of 60





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	LA-7981P	0.2

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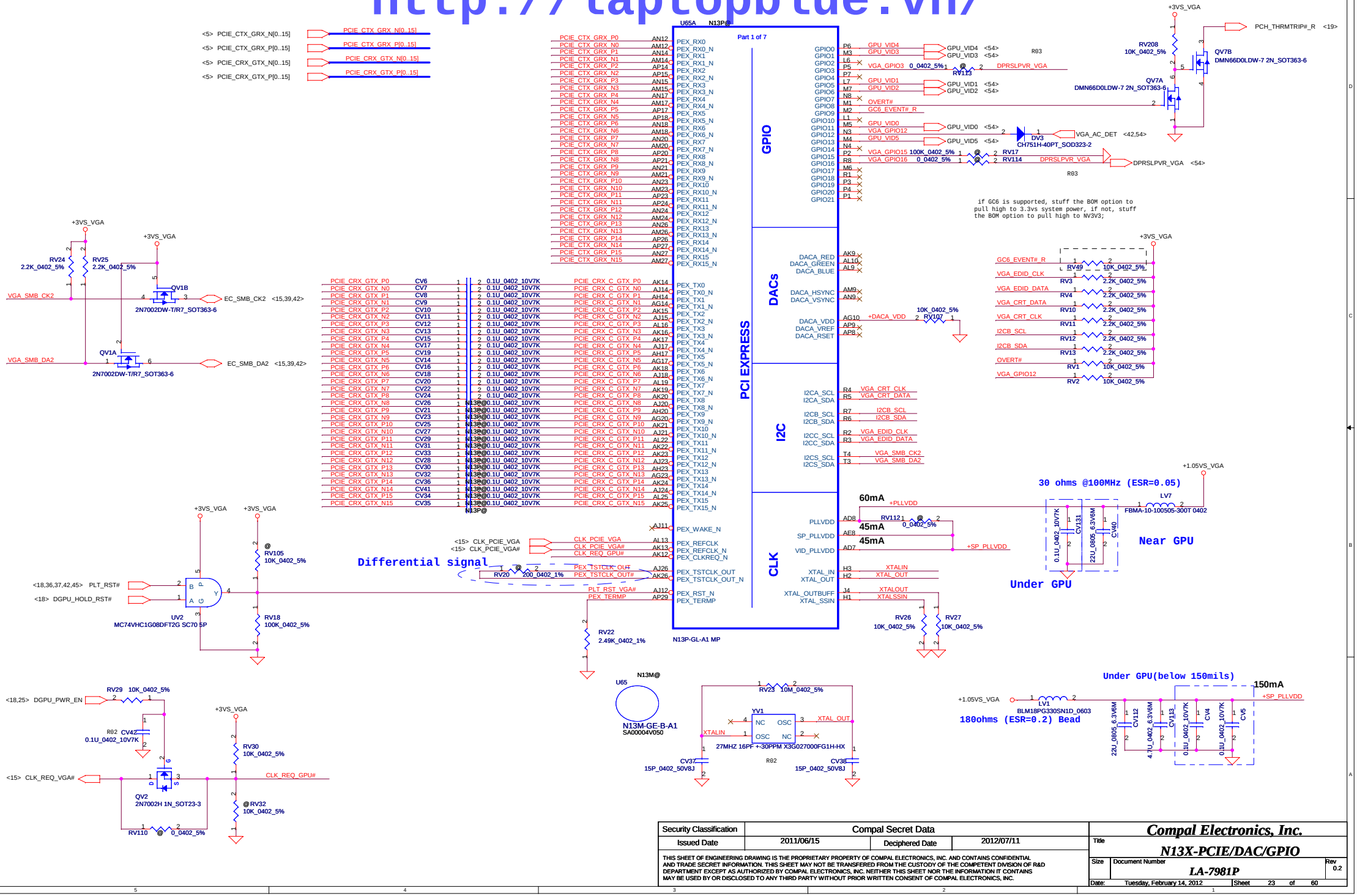

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-PCIE/DAC/GPIO**

Size	Document Number	Rev
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U65D

Part 4 of 7

LVDS/TMDS

IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6

IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4

IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5

IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2

IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2

IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4

IFPF_AUX_I2CZ_SCL AE3
IFPF_AUX_I2CZ_SDA_N AE2

N13P-GL-A1 MP

N13P@

NC

NC P8
NC AC6
NC AJ28
NC AJ4
NC AJ5
NC AL11
NC C15
NC D19
NC D20
NC D23
NC D26
NC H31
NC T8
NC V32

VDD_SENSE L4 VCCSENSE_VGA → VCCSENSE_VGA <54>

GND_SENSE L5 VSSSENSE_VGA → VSSSENSE_VGA <54>

trace width: 16mils
differential voltage sensing.
differential signal routing.

TEST

TESTMODE AK11 TESTMODE
JTAG_TCK AM10 TV2
JTAG_TDI AM11 TV3
JTAG_TDO AP12 TV4
JTAG_TMS AP11 TV5
JTAG_TRST_N AN11 RV34 10K_0402_5%
RV33 10K_0402_5%

SERIAL

ROM_CS_N H6 ROM_CS
ROM_SCLK H4 ROM_SCLK → ROM_SCLK <32>
ROM_SI H5 ROM_SI → ROM_SI <32>
ROM_SO H7 ROM_SO → ROM_SO <32>

GENERAL

BUFRST_N L2 RV35 10K_0402_5%
CEC L3 RV230 N13P@ 10K_0402_5% +3VS_VGA
R02 3V3 on N13P-GL/ for CEC signal
MULTI_STRAP_REF0_GND J1 RV38 N13P@40.2K_0402_1%

STRAP0 J2 STRAP0 → STRAP0 <32>
STRAP1 J7 STRAP1 → STRAP1 <32>
STRAP2 J6 STRAP2 → STRAP2 <32>
STRAP3 J5 STRAP3 → STRAP3 <32>
STRAP4 J3 STRAP4 → STRAP4 <32>

THERMDP K3
THERMDN K4

Reserve 1MB SPI ROM FOR VBIOS ROM

+3VS_VGA
CV295 0.1U_0402_16V4Z @
20mils
RV229 @ 10K_0402_5%
@ RV225 10K_0402_5%
UV15 @
@RV224 0_0402_5%
@RV226 0_0402_5%
ROM_CS
ROM_SO
ROM_CS_R
ROM_SO_R
CS# DO WP# GND
VCC HOLD# CLK DIO
ROM_HOLD#
MX25L1005AMC-12G SOP
@RV228 0_0402_5%
@RV227 0_0402_5%
ROM_SCLK_R
ROM_SI_R
ROM_SCLK
ROM_SI

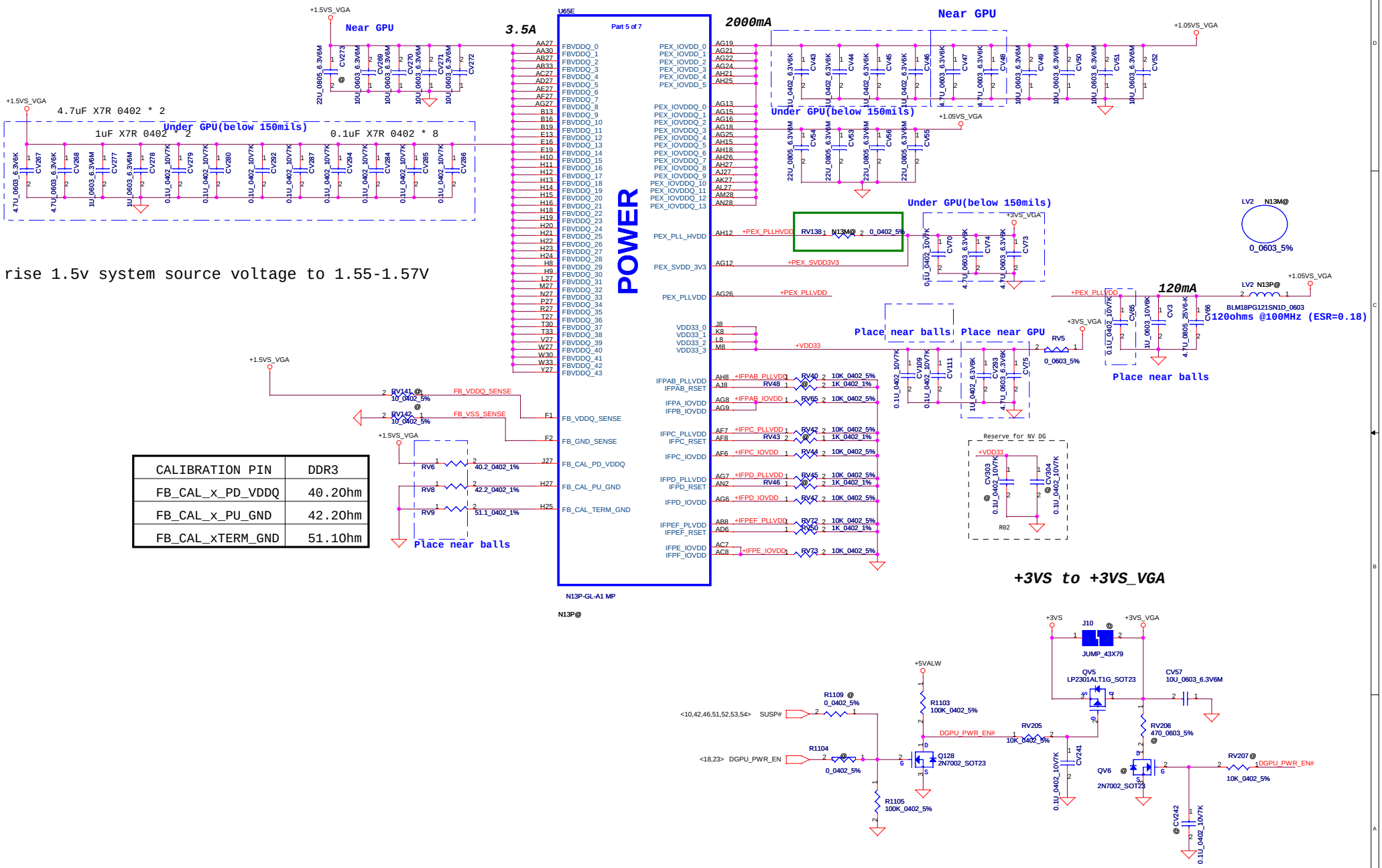
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N13X-LVDS/HDMI/DP/THM

Size | Document Number: LA-7981P | Rev: 0.2

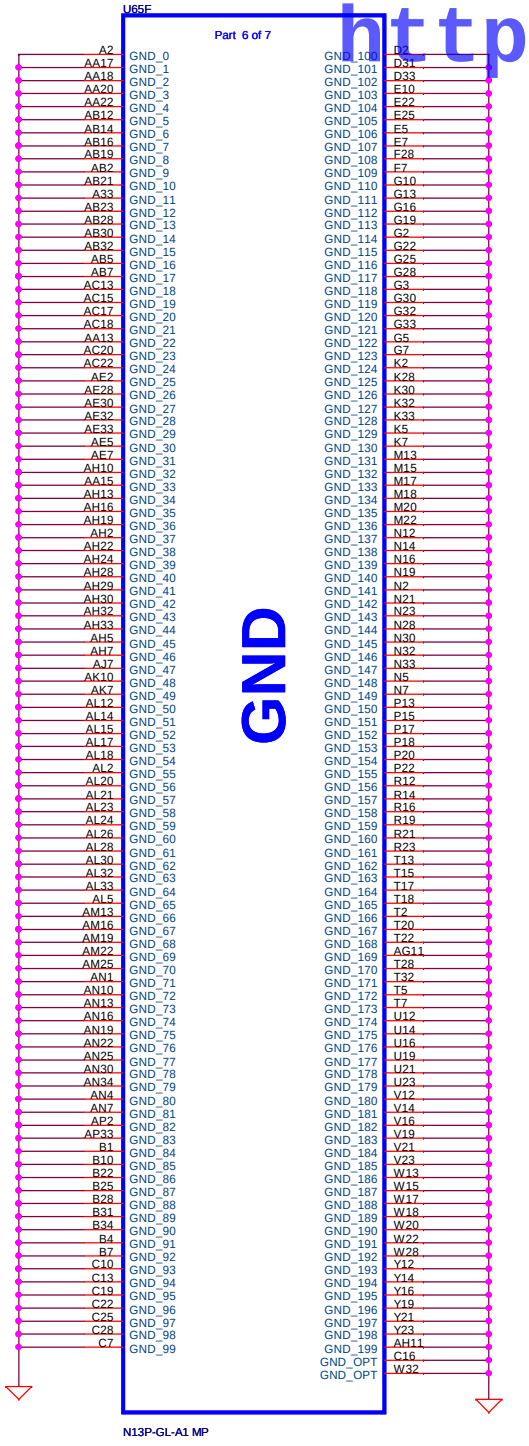
Date: Tuesday, February 14, 2012 | Sheet 24 of 60

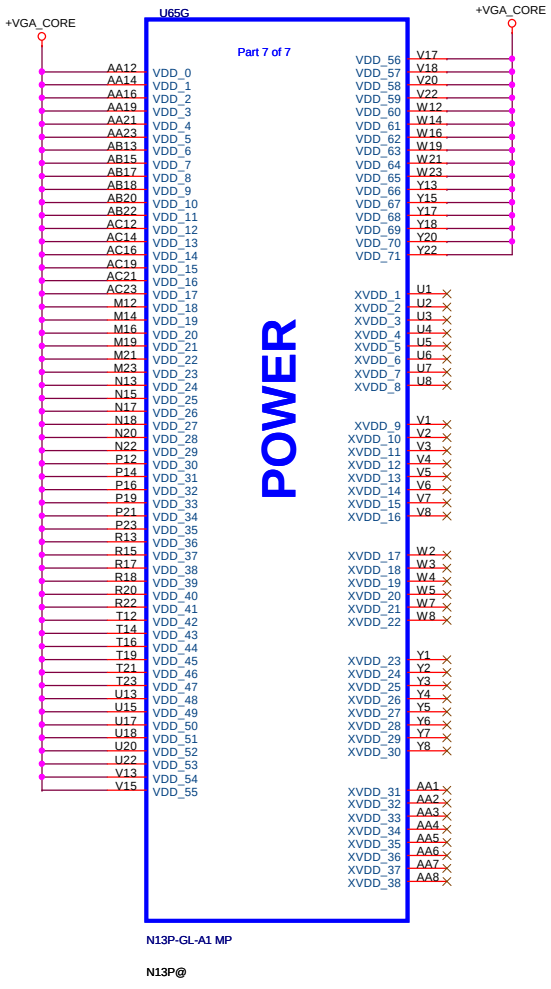


CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.	
Title	N13X-POWER
Size	Document Number: LA-7981P
Rev	0.2
Date: Tuesday, February 14, 2012	Sheet 25 of 60





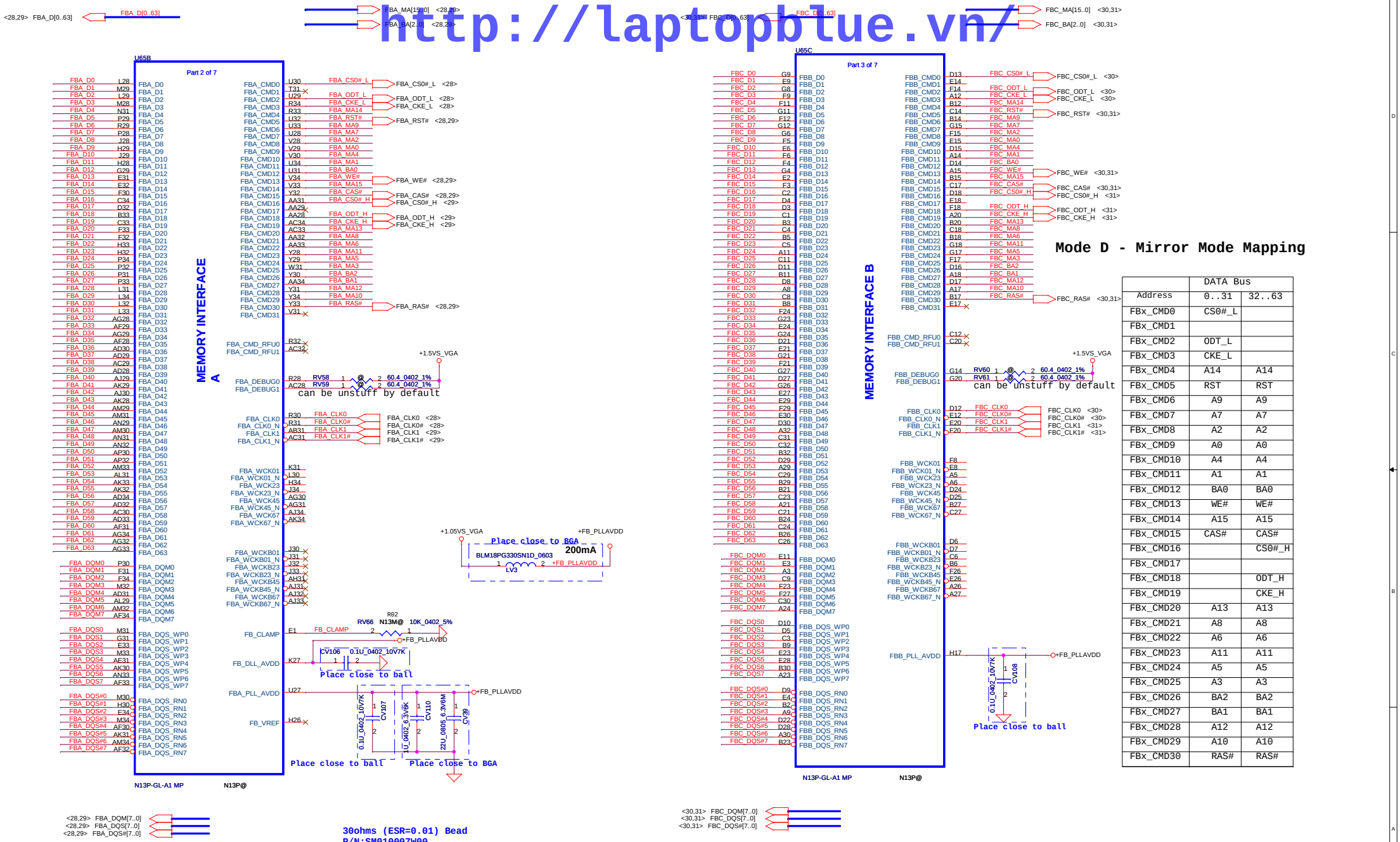
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13-VGA CORE, GND**

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 | Sheet 26 of 60



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

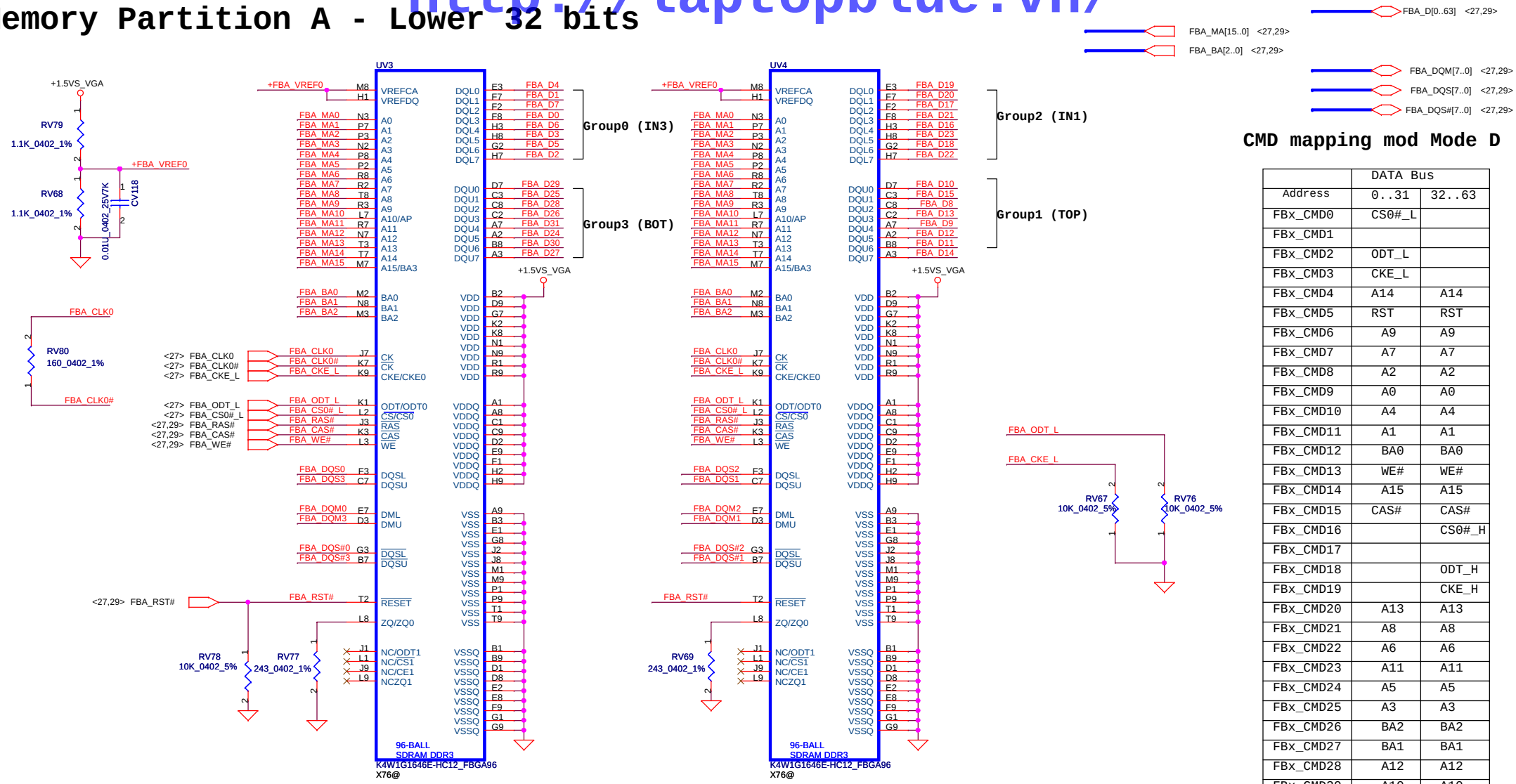
Compal Electronics, Inc.

Title: **N13X-MEM Interface**

Size	Document Number	Rev
	LA-7981P	0.2

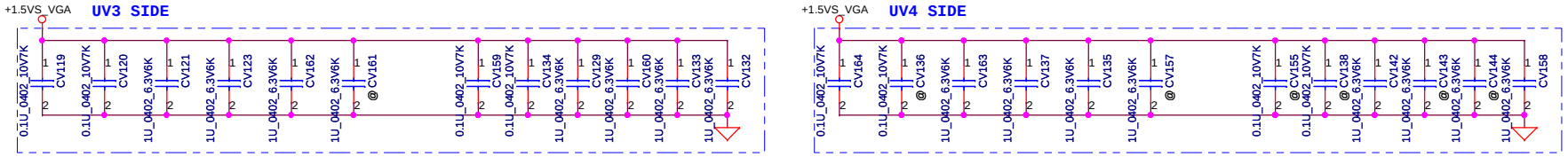
Date: Tuesday, February 14, 2012 | Sheet 27 of 60

Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

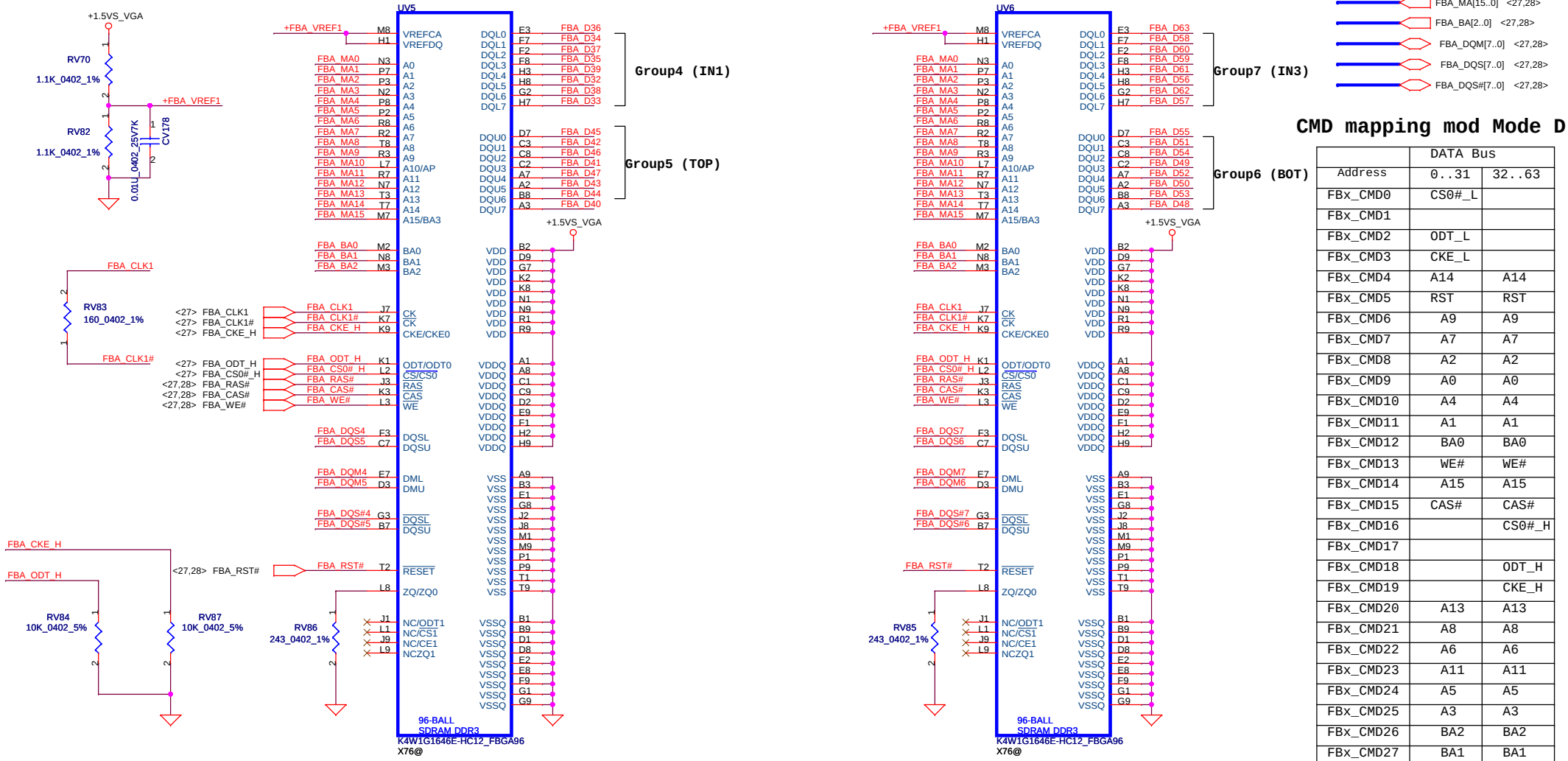
Compal Electronics, Inc.

Title: N13X-VRAM A Lower

Size | Document Number: LA-7981P | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 28 of 60

Memory Partition A - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

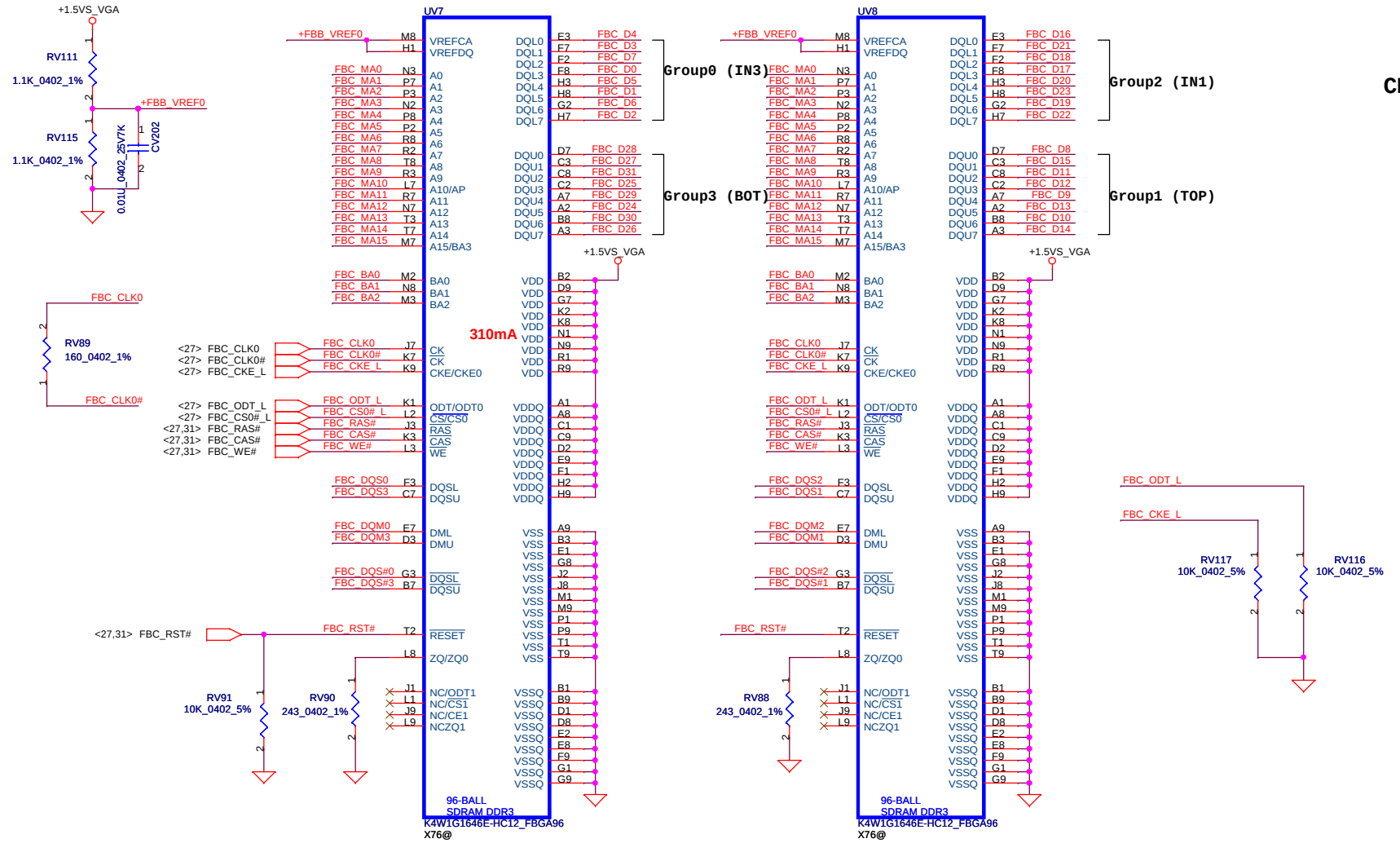
Compal Electronics, Inc.

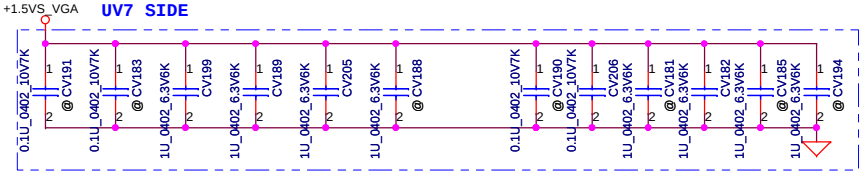
Title: **N13X-VRAM A Upper**

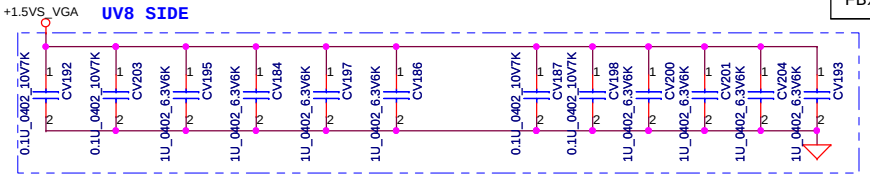
Size | Document Number: **LA-7981P** | Rev: 0.2

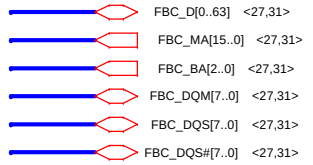
Date: Tuesday, February 14, 2012 | Sheet 29 of 60

Memory Partition C - Lower 32 bits









CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

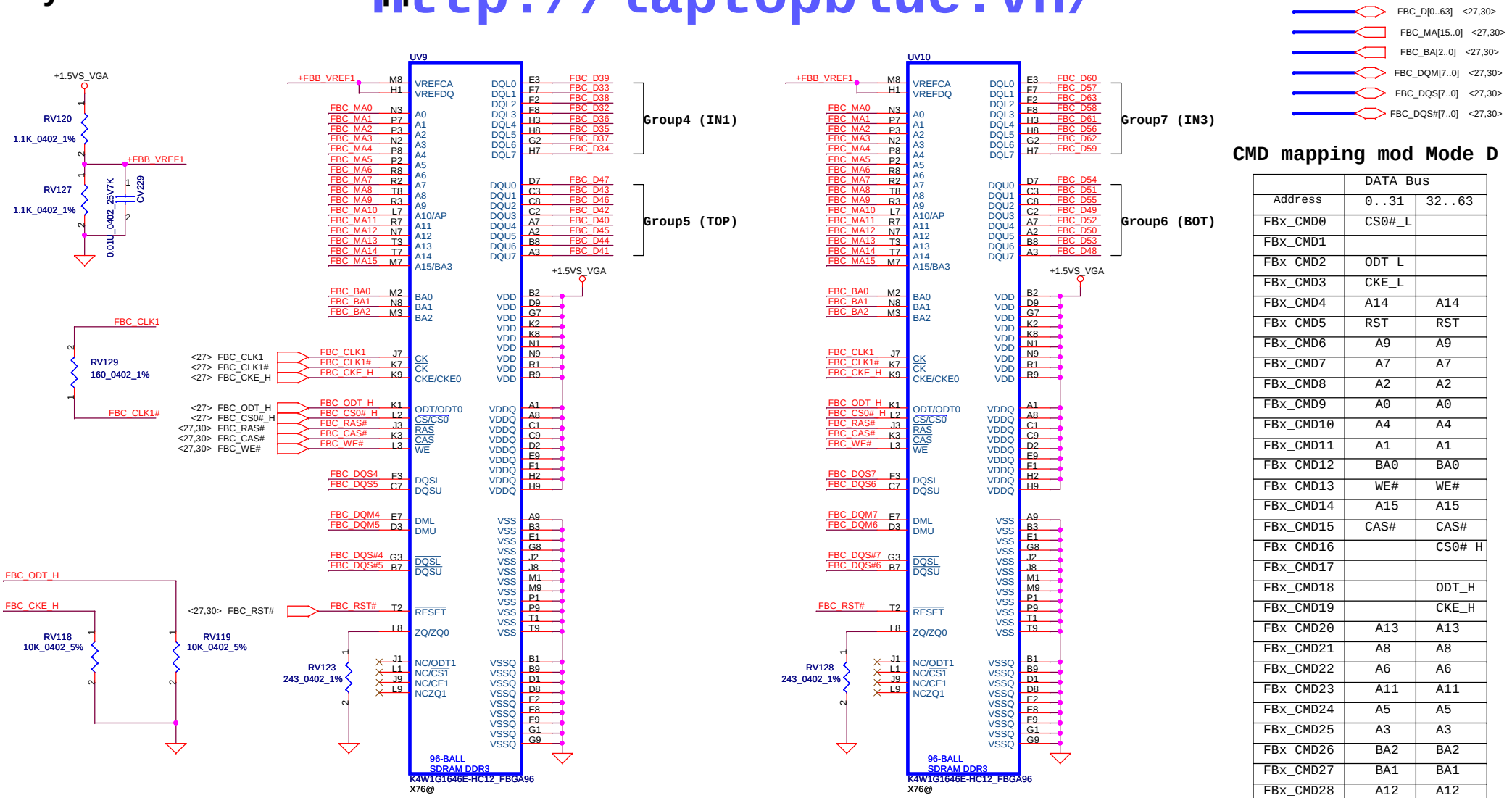
Compal Electronics, Inc.

Title: **N13X-VRAM C Lower**

Size: Custom | Document Number: **LA-7981P** | Rev: 0.2

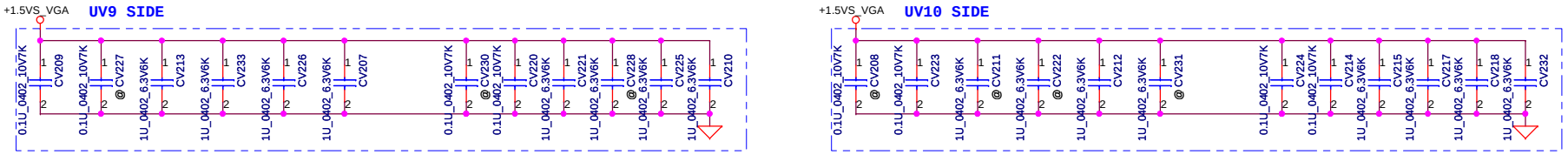
Date: Tuesday, February 14, 2012 | Sheet 30 of 60

Memory Partition C - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-VRAM C Upper**

Size	Document Number	Rev
Custom	LA-7981P	0.2

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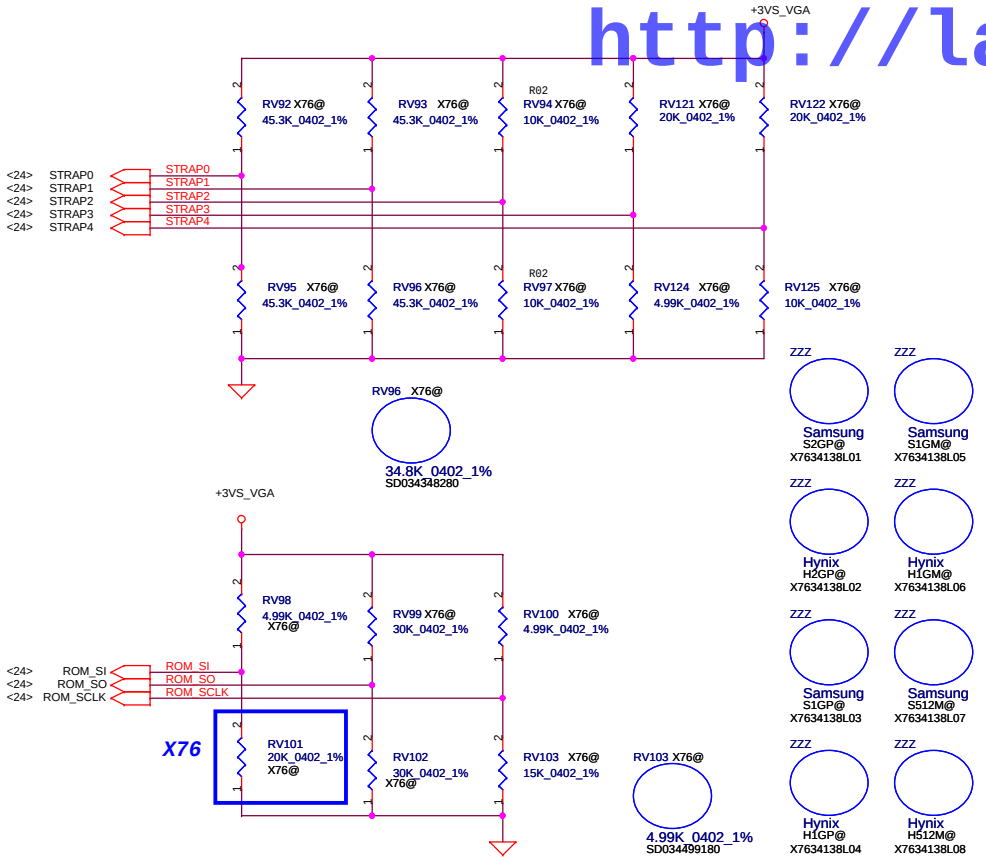

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

USER Straps

User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

PCIE_MAX_SPEED

0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

For N13P-GL strap table

X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

For N13M-GE strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE	900 MHz	128M* 16* 4 1GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N13M-GE	900 MHz	128M* 16* 4 1GB	Hynix (2Gb) H5TQ1G63DFR-11C	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N13M-GE	900 MHz	64M* 16* 4 512MB	Samsung (1Gb) K4W1G1646G-BC11	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N13M-GE	900 MHz	64M* 16* 4 512MB	Hynix (1Gb) H5TQ1G63DFR-11C	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N13X_MISC

Size: Custom | Document Number: LA-7981P | Rev: 0.2

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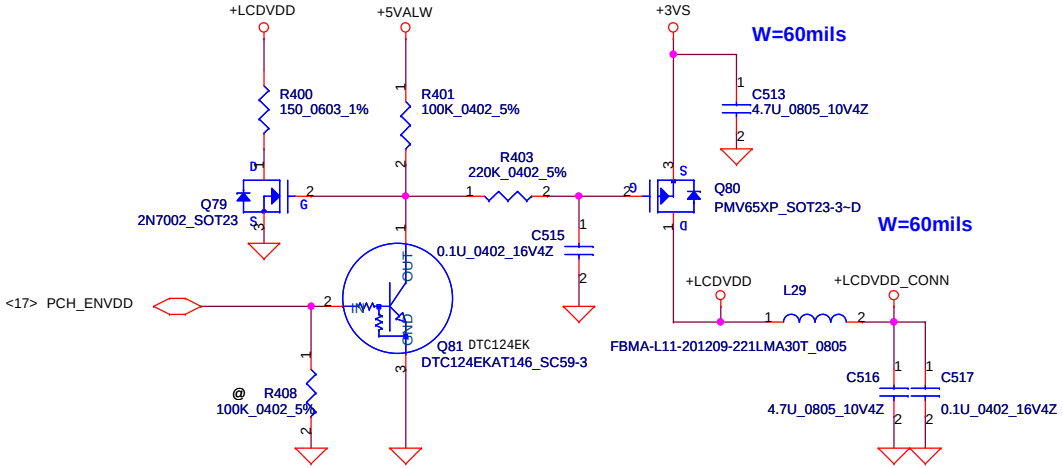
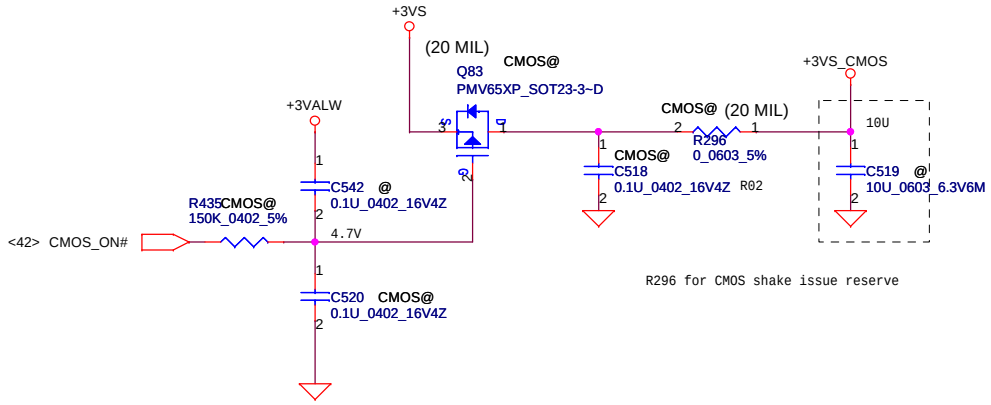
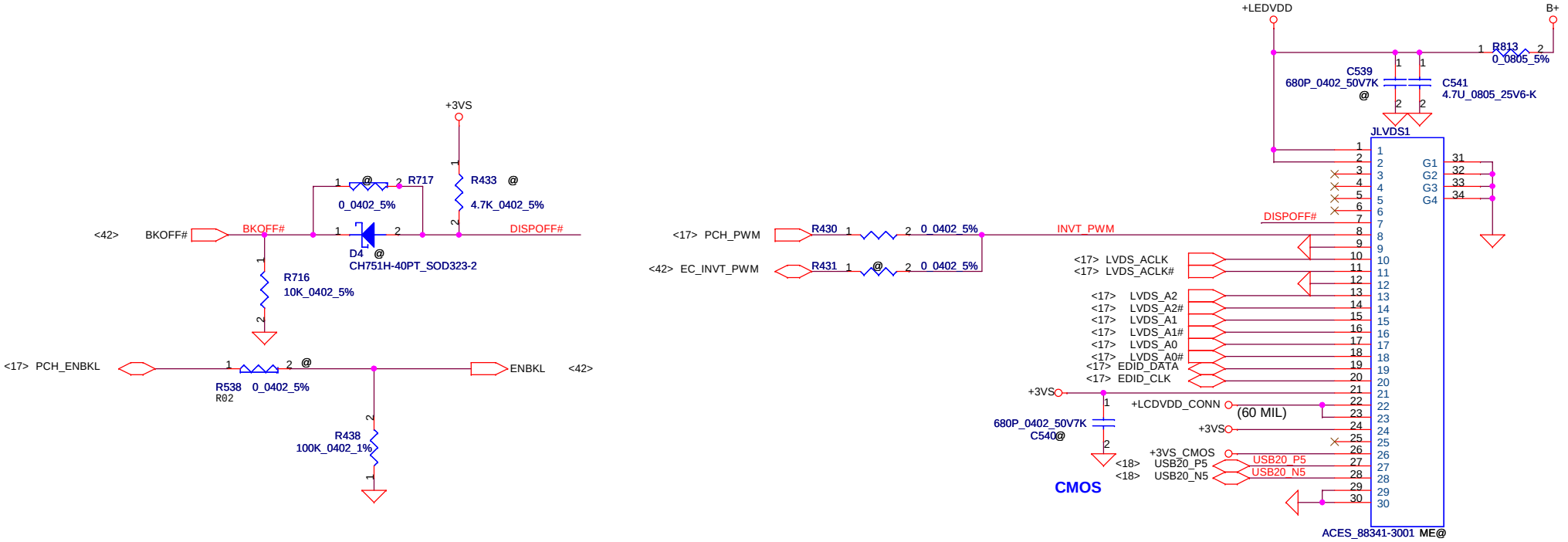
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	LA-7981P	0.2

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CRT Connector

+5VS
@ D5 BAT54S-7-F_SOT23-3 — BLUE
@ D6 BAT54S-7-F_SOT23-3 — GREEN
@ D7 BAT54S-7-F_SOT23-3 — RED

<17> DAC_RED
<17> DAC_GRN
<17> DAC_BLU
FCM1608CF-121T03 0603 L30 — RED
FCM1608CF-121T03 0603 L31 — GREEN
FCM1608CF-121T03 0603 L32 — BLUE
R445 150_0402_1%
R443 150_0402_1%
R446 150_0402_1%
CLOSE TO CONN
C522 10P_0402_50V8J
C523 10P_0402_50V8J
C524 10P_0402_50V8J
C525 10P_0402_50V8J
C526 10P_0402_50V8J
C527 10P_0402_50V8J

+5VS
D10 RB491D_SC59-3
+CRT_VCC
F1 1.1A_6V_SMD1812P110TF
W=40mils
+CRT_VCC_F
C521 0.1U_0402_16V4Z
CONTE_80431-5K1-152
JCRT1 ME@
PAD T66
NC11
RED
CRT_DDC_DAT_CONN
GREEN
JVGA_HS
BLUE
JVGA_VS
CRT_DDC_CLK_CONN
C528 100P_0402_50V8J
R437 0_0402_5%
R436 0_0402_5%
R434 0_0402_5%
R432 0_0402_5%
EMI Request

+CRT_VCC
R448 1K_0402_5%
C529 0.1U_0402_16V4Z
<17> CRT_HSYNC
U23 SN74AHCT1G125DCKR_SC70-5
CRT_HSYNC_1
FCM1608CF-121T03 0603 L33
JVGA_HS
@ C530 10P_0402_50V8J

+CRT_VCC
R451 1K_0402_5%
C531 0.1U_0402_16V4Z
<17> CRT_VSYNC
U24 SN74AHCT1G125DCKR_SC70-5
CRT_VSYNC_1
FCM1608CF-121T03 0603 L34
JVGA_VS
@ C532 10P_0402_50V8J

D8 @
JVGA_VS
JVGA_HS
+5VS
CRT_DDC_CLK_CONN
CRT_DDC_DAT_CONN
AZC099-04S.R7G_SOT23-6

+3VS
+CRT_VCC
Pull high at chipset/VGA side
R456 2.2K_0402_5%
R457 2.2K_0402_5%
<17> CRT_DDC_DATA
2N7002DW-T/R7_SOT363-6 Q62B
CRT_DDC_DAT_CONN
<17> CRT_DDC_CLK
2N7002DW-T/R7_SOT363-6 Q62A
CRT_DDC_CLK_CONN
@ C533 100P_0402_50V8J
@ C534 68P_0402_50V8K

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	LA-7981P	0.2

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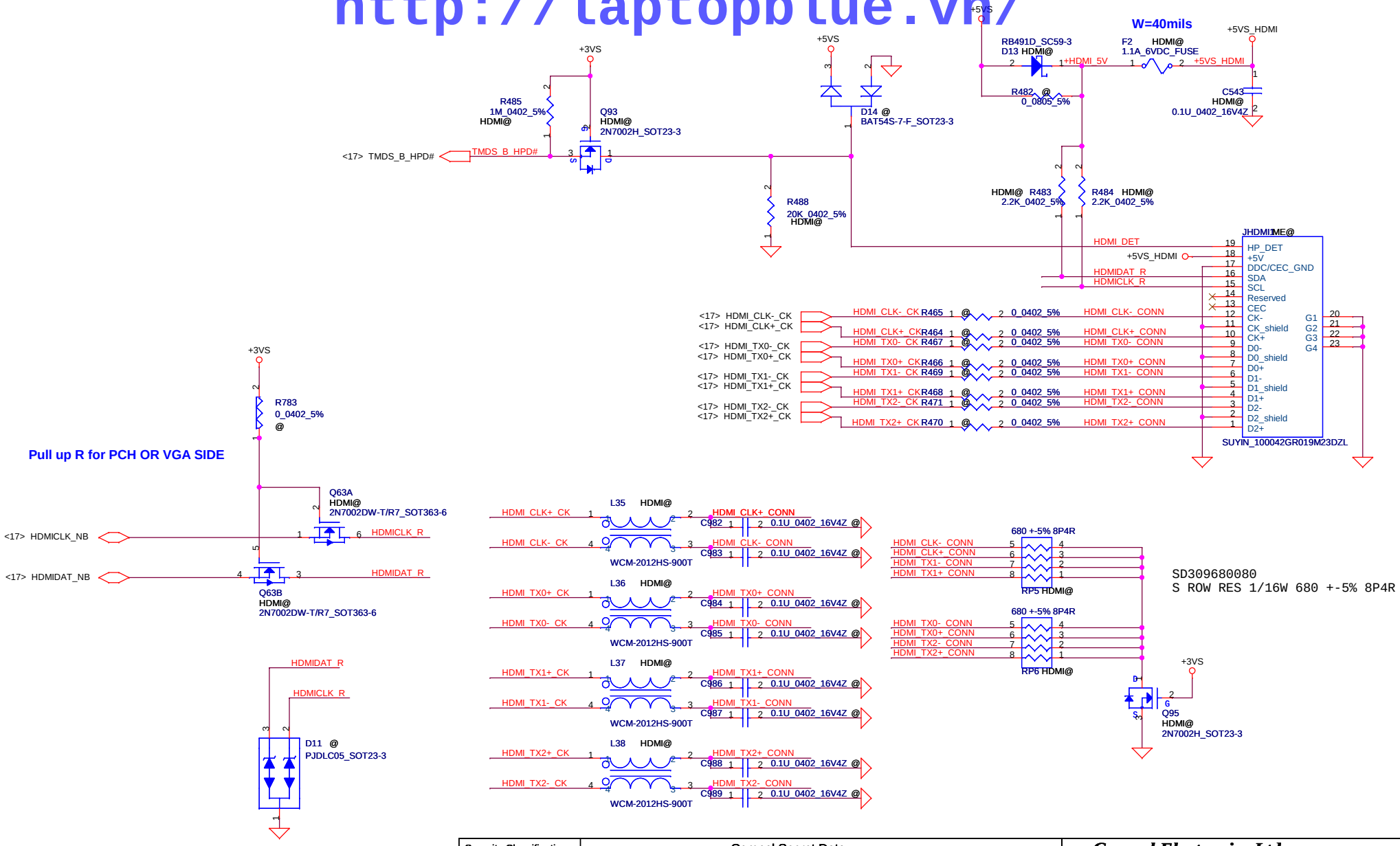

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-7981P	0.2

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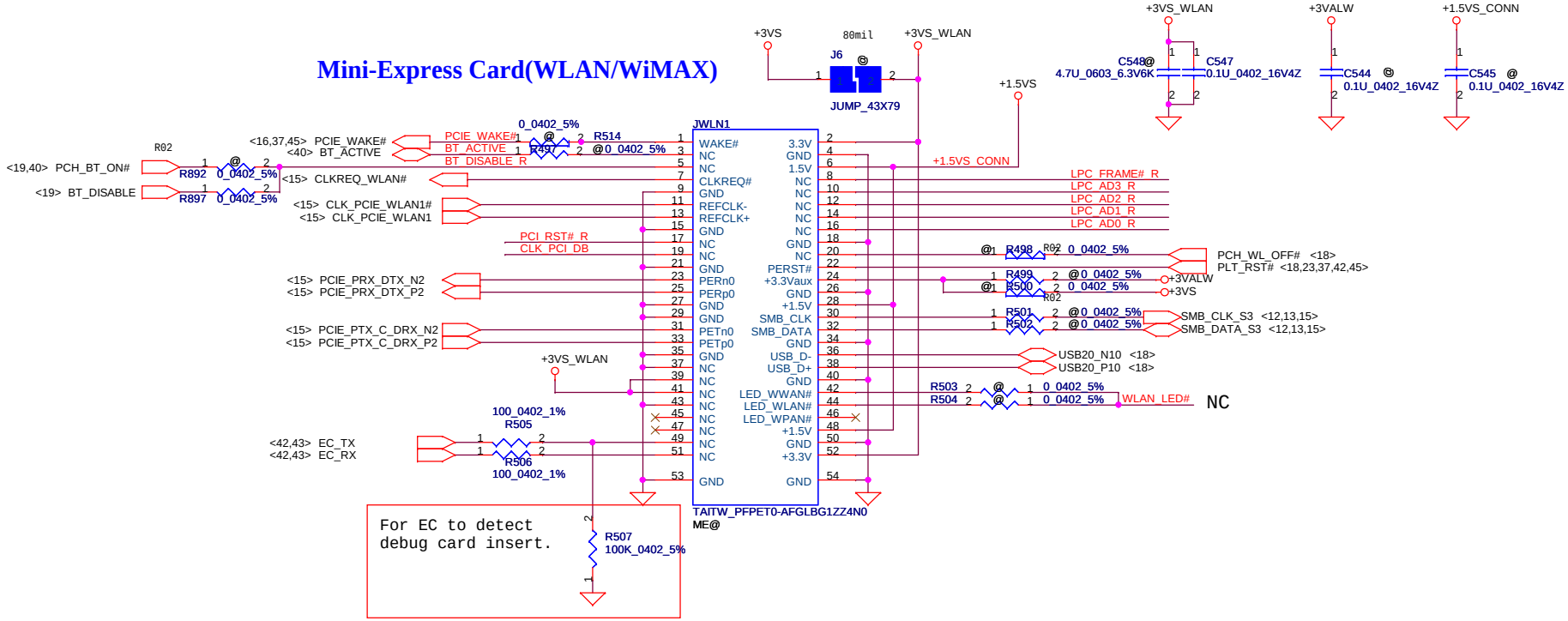
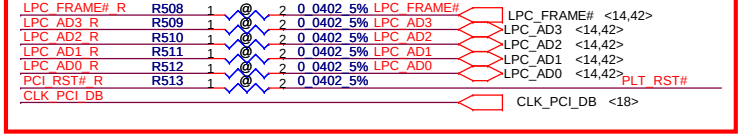
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

Size	Document Number	Rev
	LA-7981P	0.2

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Layout Notice : Place as close chip as possible.

+3VALW +3V_LAN J18 JUMP_43X79 Q105 PMV65XP_SOT23-3-D

<42> LAN_PWR_ON# LAN_PWR_ON# R176 10K_0402_5% C976 0.1U_0402_16V7K

Close together

+1.1_DVDDL R1357 0_0402_5% +LX_R L74 SWR@ 4.7UH_SIA4012-4R7M_20% +LX

C935 1000P_0402_50V7K @ C936 0.1U_0402_16V4Z C937 10U_0603_6.3V6M 10U

Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

L77 FBMA-L11160808601LMA10T_2P L78 SWR@ FBMA-L11160808601LMA10T_2P

+1.1_AVDDL_L +1.1_AVDDL +1.1_DVDDL

C967 0.1U_0402_16V4Z C980 1U_0402_6.3V4Z C317 4.7U_0603_6.3V6K

Place close to Pin34

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN R525 4.7K_0402_5% @ <18,23,36,42,45> PLT_RST# PLT_RST#

U41 8162@ AR8162-AL3A-R

SA000050E00_S IC AR8161-AL3A-R QFN 40P E-LAN CTRL
SA000052J10_S IC AR8162-AL3A-R QFN 40P E-LAN CTRL

H --> Overclocking mode
L --> Not overclocking mode

Overclocking mode stick

+3V_LAN +AVDDH_AVDD3.3 R1367 0_0402_5%

C948 0.1U_0402_16V4Z C949 1U_0402_6.3V4Z

Place close to Pin16

Place Close to Chip

U41 GIGA@ Atheros AR8151/AR8161

<15> PCIE_PRX_DTX_N1 C946 0.1U_0402_16V7K PCIE_PRX_C_DTX_N1 29 TX_N
<15> PCIE_PRX_DTX_P1 C947 0.1U_0402_16V7K PCIE_PRX_C_DTX_P1 30 TX_P
<15> PCIE_PTX_C_DRX_N1 36 RX_N
<15> PCIE_PTX_C_DRX_P1 35 RX_P
<15> CLK_PCIE_LAN# 32 REFCLK_N
<15> CLK_PCIE_LAN 33 REFCLK_P
PLT_RST# 2 PERST#
<16,36,45> PCIE_WAKE# R1369 0_0402_5% PCIE_WAKE#_R 3 WAKE#
<42> LAN_WAKE# R1370 0_0402_5%
25 SMCLK
26 SMDATA
28 NC
27 TESTMODE
+3V_LAN R521 4.7K_0402_5%
Vendor recommand reseve the PU resistor close LAN chip
LAN_XTALO 7 XTLO
LAN_XTALI 8 XTLI
+3V_LAN R520 4.7K_0402_5%
<15> CLKREQ_LAN# 4 CLKREQ#
+1.1_AVDDL 13 AVDDL
+1.1_AVDDL 19 AVDDL
+1.1_AVDDL 31 AVDDL
+1.1_AVDDL_L 34 AVDDL
+1.1_AVDDL 6 AVDDL_REG/AVDDL
41 GND
AR8161-AL3A-R_QFN40_5X5

LED_0 38 ACTIVITY
LED_1 39 LAN_LINK#
LED_2 23
ACTIVITY <38>
LAN_LINK# <38>
R65 R02 LDO@ 10K_0402_5%

TRXN0 12 MDI0- MDI0- <38>
TRXP0 11 MDI0+ MDI0+ <38>
TRXN1 15 MDI1- MDI1- <38>
TRXP1 14 MDI1+ MDI1+ <38>
TRXN2 18 MDI2- MDI2- <38>
TRXP2 17 MDI2+ MDI2+ <38>
TRXN3 21 MDI3- MDI3- <38>
TRXP3 20 MDI3+ MDI3+ <38>

RBIAS 10 LAN_RBIAS R1371 2.37K_0402_1%
Place Close to PIN1

VDD33 1 +3V_LAN
LX 40 +LX +LX
VDDCT/ISOLAN 5 +1.7_VDDCT R1372 30K_0402_5% +3VS
DVDDL/PPS 24
DVDDL_REG/DVDDL 37 +1.1_DVDDL
AVDDH/AVDD33 16 +AVDDH_AVDD3.3
AVDDH 22 +2.7_AVDDH +2.7_AVDDH
AVDDH_REG 9 +2.7_AVDDH

Place Close to PIN1

+3V_LAN C950 1000P_0402_50V7K @ C951 0.1U_0402_16V4Z C952 1U_0402_6.3V4Z C953 10U_0603_6.3V6M @ C954 10U_0603_6.3V6M 10U

C956 0.1U_0402_16V4Z Near Pin13
C957 0.1U_0402_16V4Z Near Pin19
C958 0.1U_0402_16V4Z Near Pin31
C959 1U_0402_6.3V4Z C960 0.1U_0402_16V4Z Near Pin6
C961 0.1U_0402_16V4Z C962 1U_0402_6.3V4Z Near Pin9
C963 0.1U_0402_16V4Z Near Pin22
C964 0.1U_0402_16V4Z C965 1U_0402_6.3V4Z Near Pin37

LAN_XTALI LAN_XTALO Y6 25MHZ_10PF_7V25000014 NC OSC OSC NC
C968 15P_0402_50V8J C969 15P_0402_50V8J

3.3V : Enable switching regulator
0V : Disable switching regulator

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-AR8151/8161

Size: Custom | Document Number: LA-7981P | Rev: 0.2

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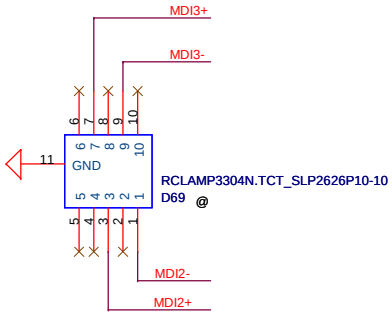
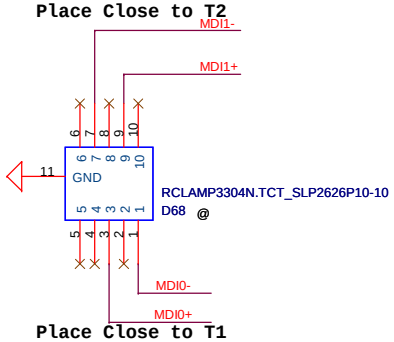
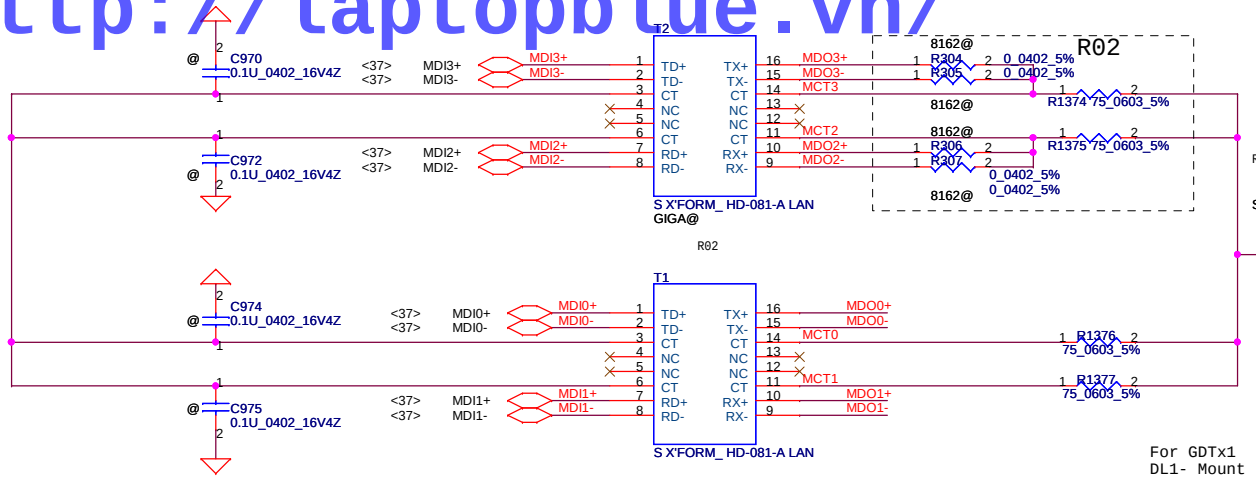


Place Close to T2



Place Close to T1

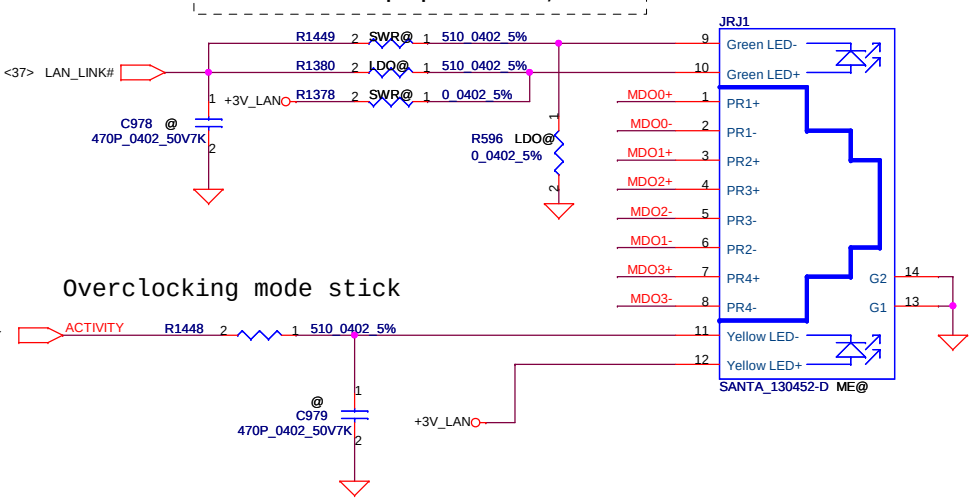


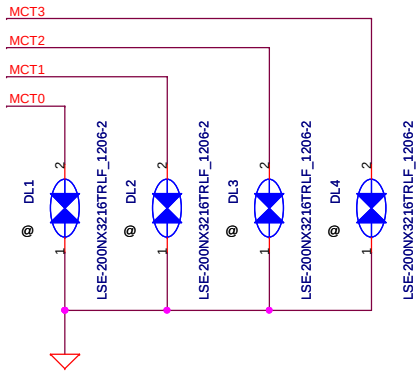
R308 change to C 10P 50V 0603 Rev0.5

S CER CAP 10P 50V J NPO 0603
R308 0_0603_5%
C973 10P_0603_50V

For GDTx1
DL1- Mount
DL2/DL3/DL4- NC
R308- 75 ohm
R1374/R1375/R1376/R1377- 0 ohm

LDO Mode: pop R1380;R596
SWR Mode: pop R1449;R1378





Reserve for EMI go rural solution

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN_Transformer

Size	Document Number	Rev
B	LA-7981P	0.2

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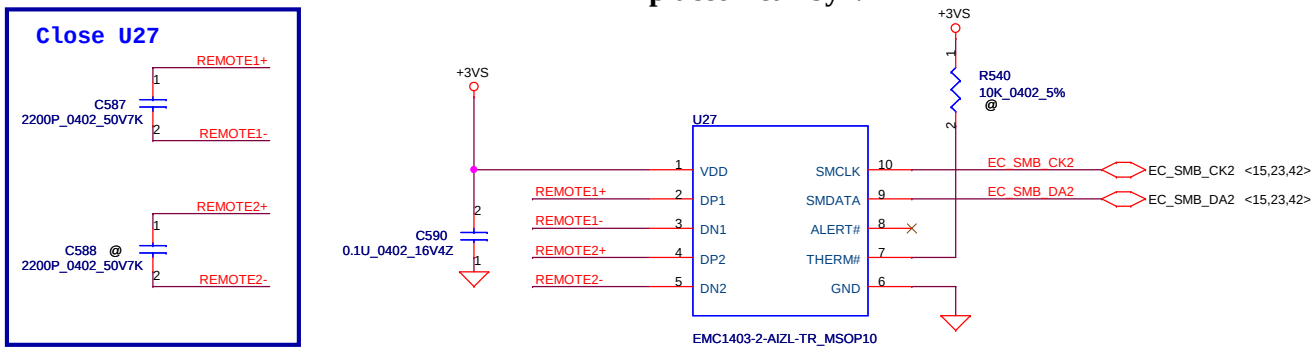
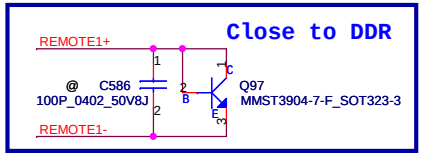
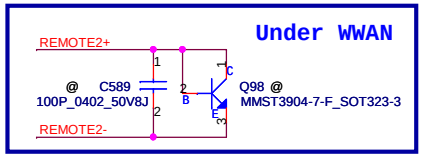
SMSC thermal sensor placed near by VRAM

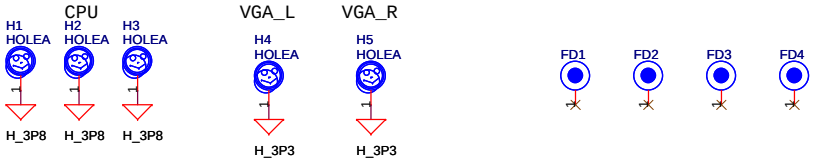


Address 1001_101xb

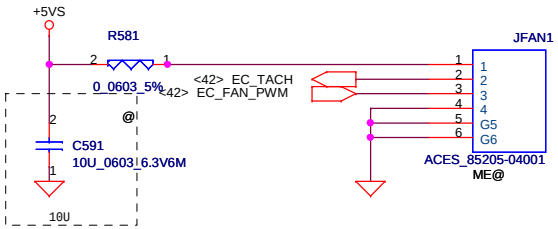


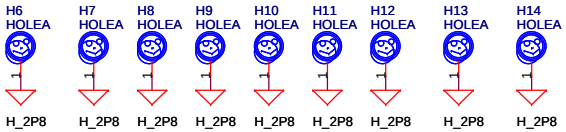


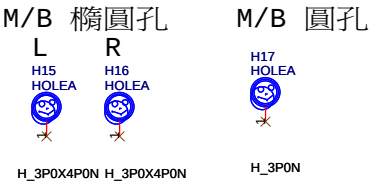
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn



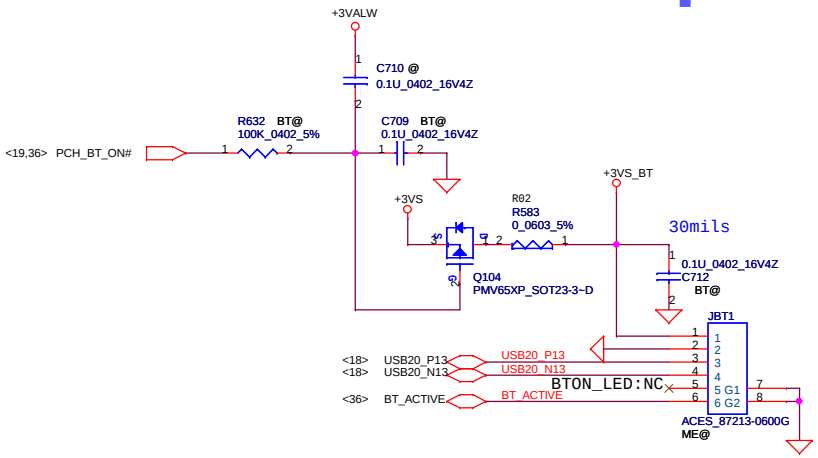




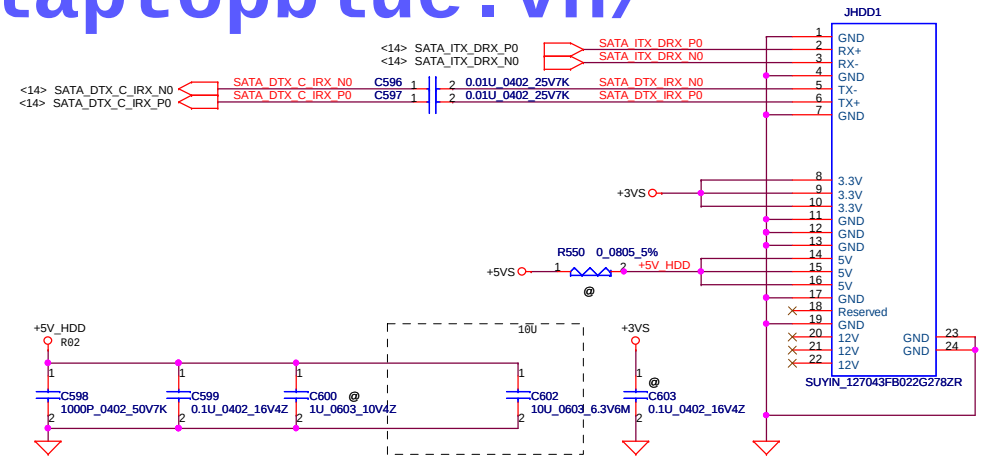
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.			
Title: Fintek-Thermal IC/FAN/screw			
Size: B	Document Number: LA-7981P		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 39 of 60		

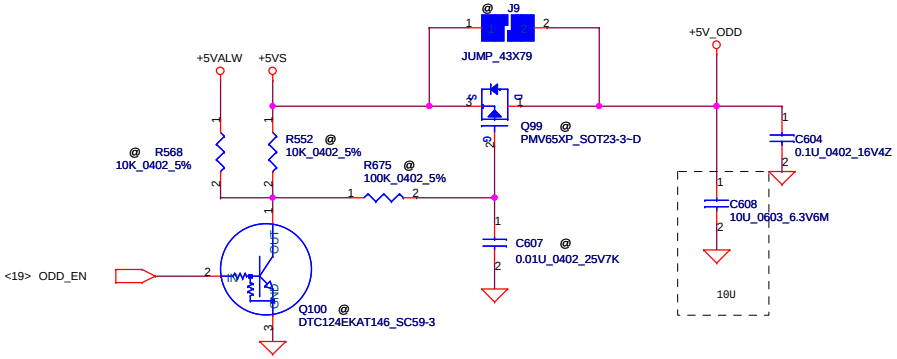
BT MODULE CONN



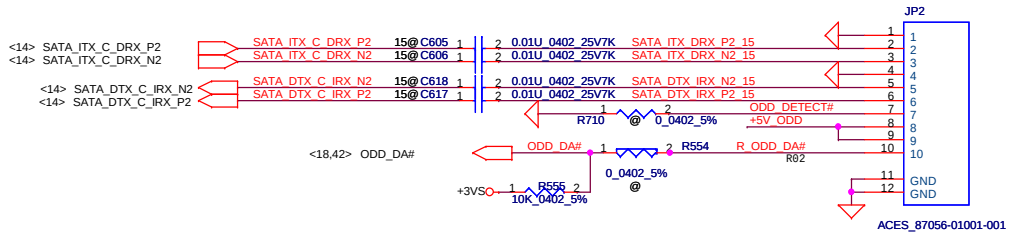
SATA HDD Conn.



ODD Power Control

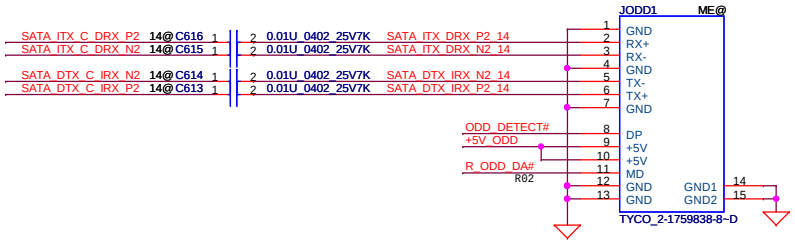


FOR 15"
SATA ODD FFC Conn.



Co-lay

FOR 14"
SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

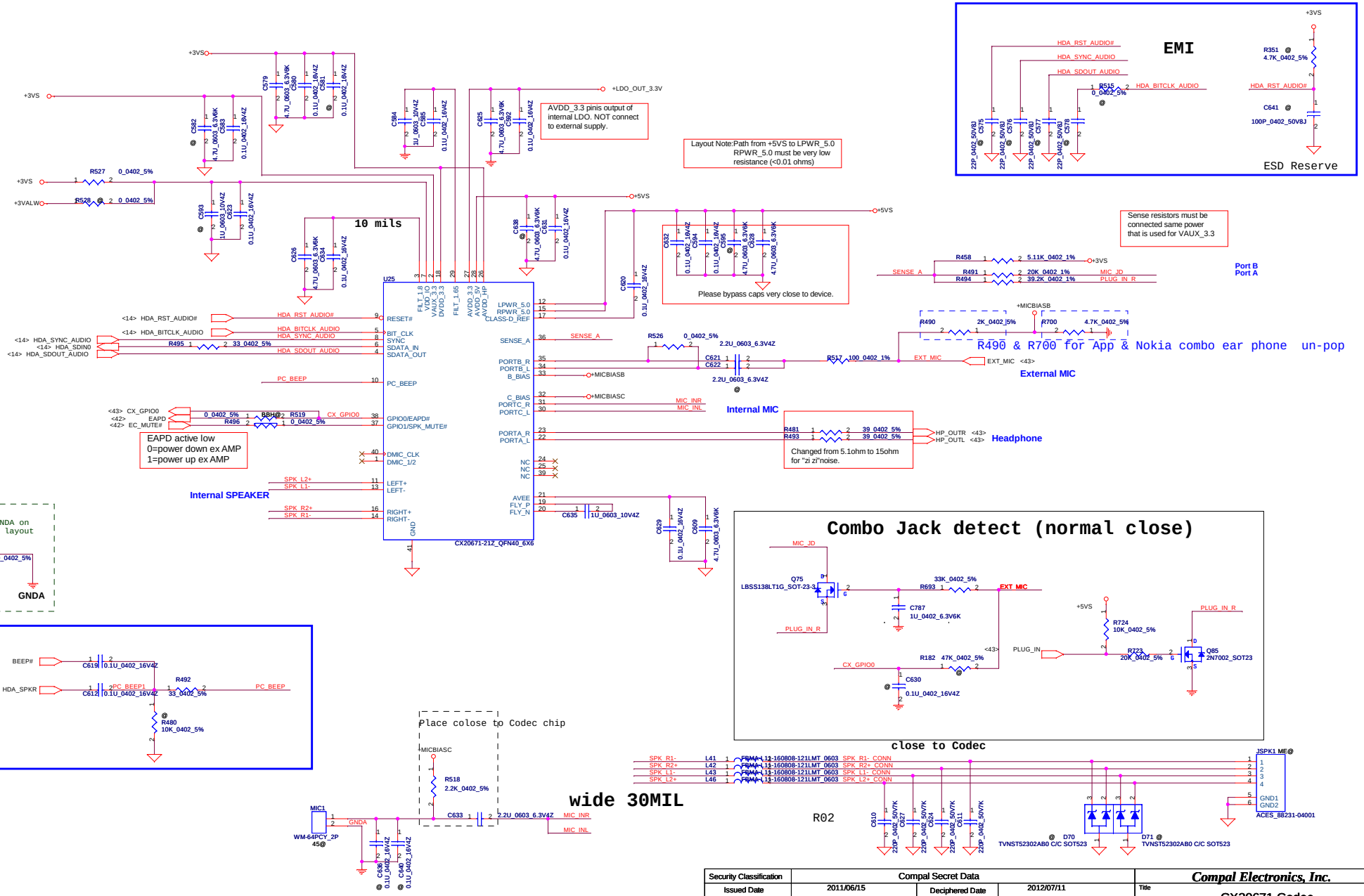
Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 | Sheet 40 of 60

CX20671
High Definition Audio Codec SoC With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CX20671 Codec

Size: Custom | Document Number: LA-7981P | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 41 of 60

Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

Capsensor Board For best buy use

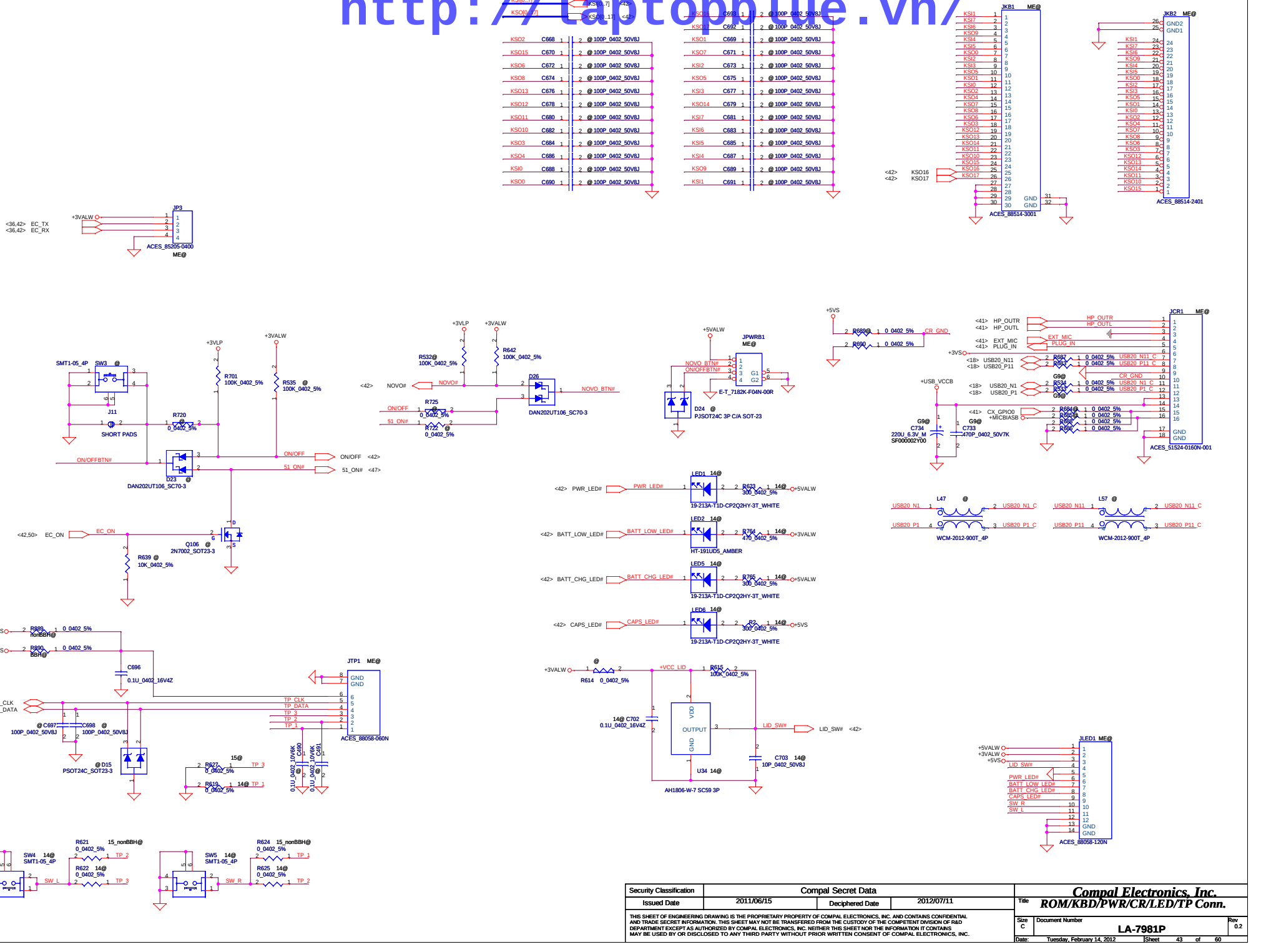
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 42 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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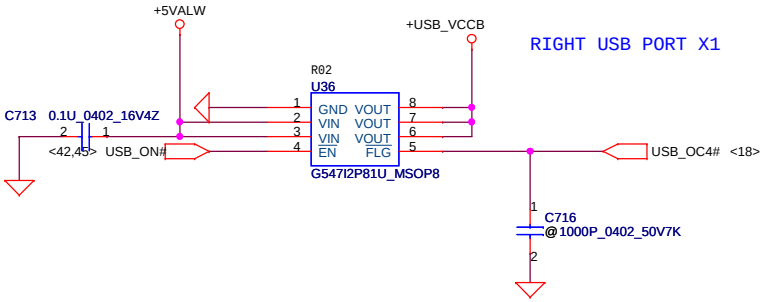
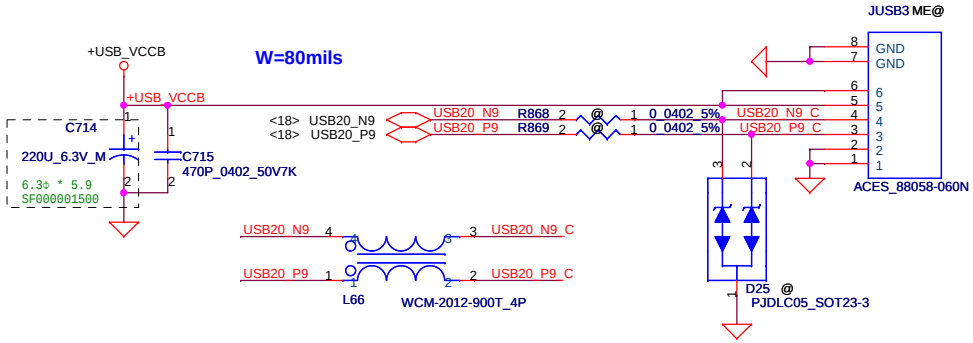
Title	Compal Electronics, Inc.		
	ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA-7981P		Rev 0.2
Date: Tuesday, February 14, 2012	Sheet 43 of 60		

Right Ext.USB Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: USB ext. ports

Size	Document Number	Rev
B	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 44 of 60

+1.5V to +1.05V Transfer

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

For EMI request

Place TX AC coupling Cap (C843~C850). Close to connector

2A/Active Low

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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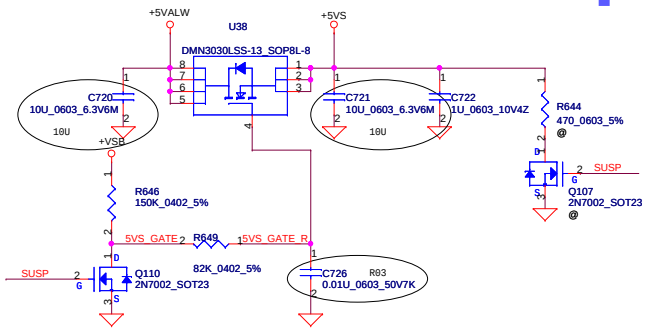
Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

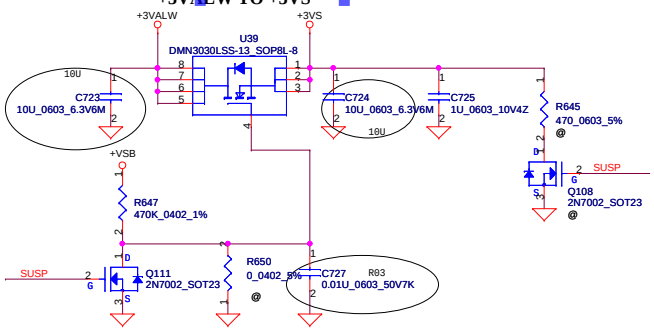
Size: Custom | Document Number | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 45 of 60

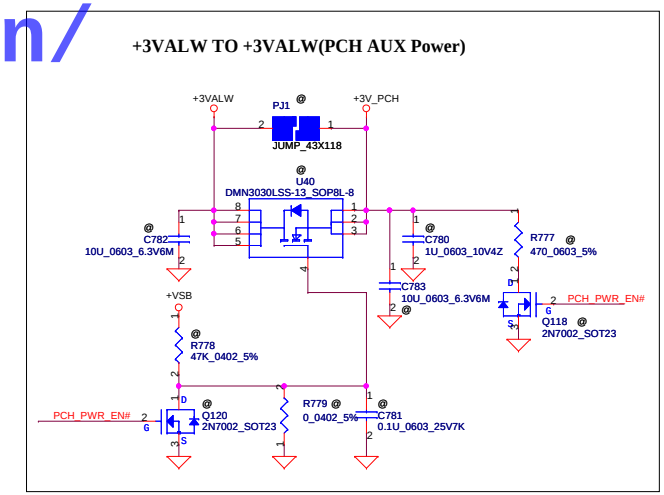
+5VALW TO +5VS

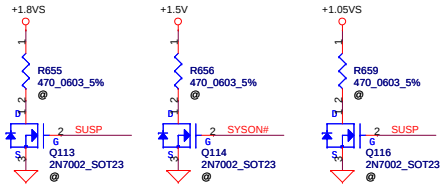


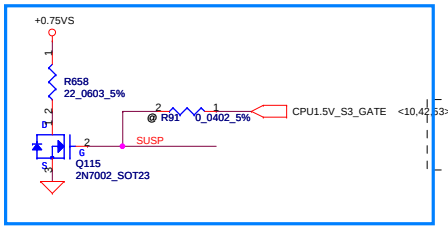
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)

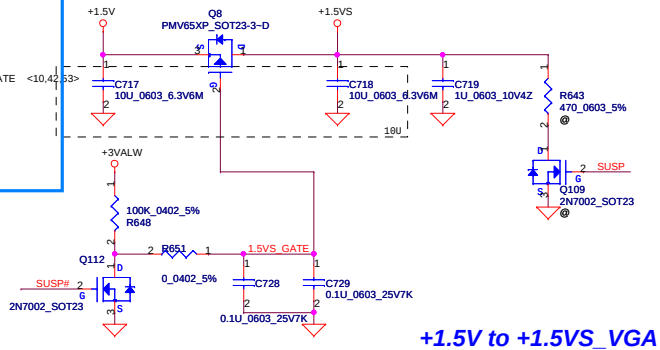


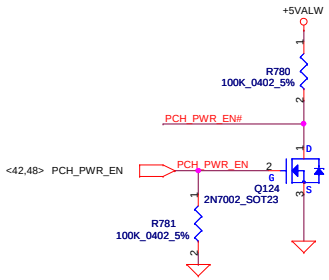


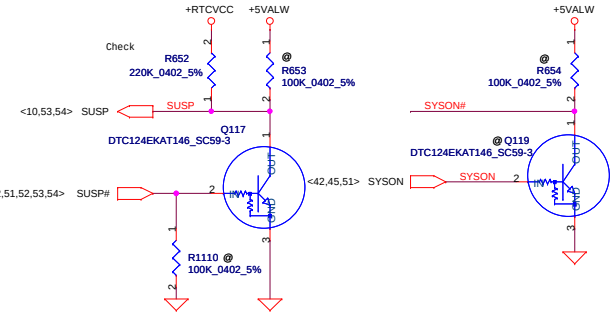


For Intel S3 Power Reduction.

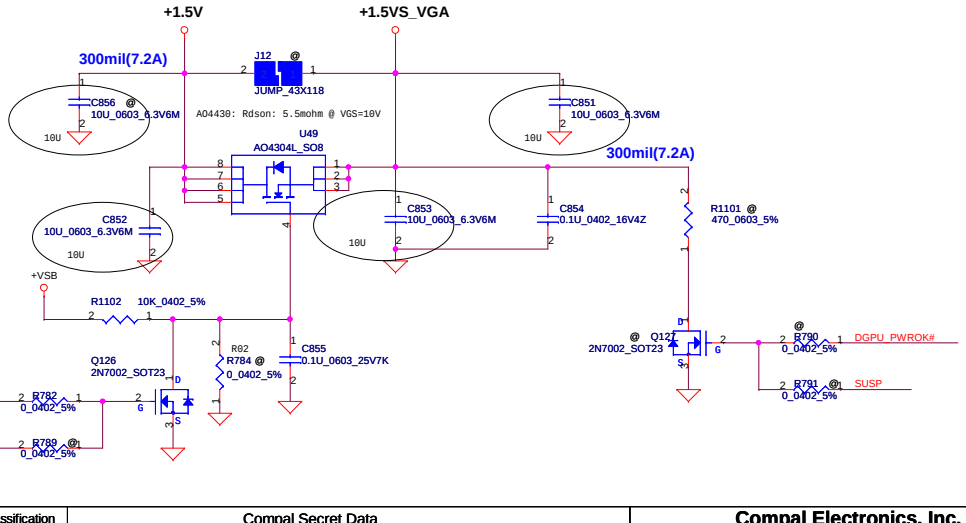
+1.5V to +1.5VS

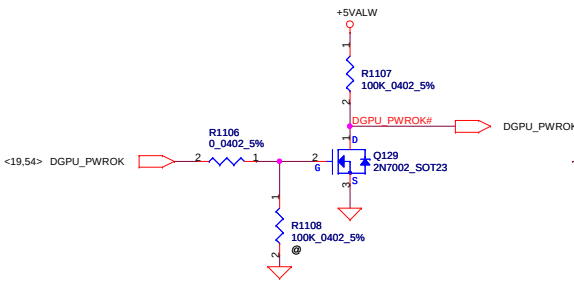






+1.5V to +1.5VS_VGA Transfer





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-7981P	0.2

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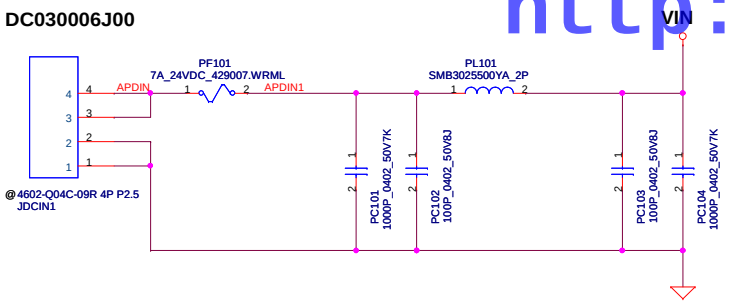
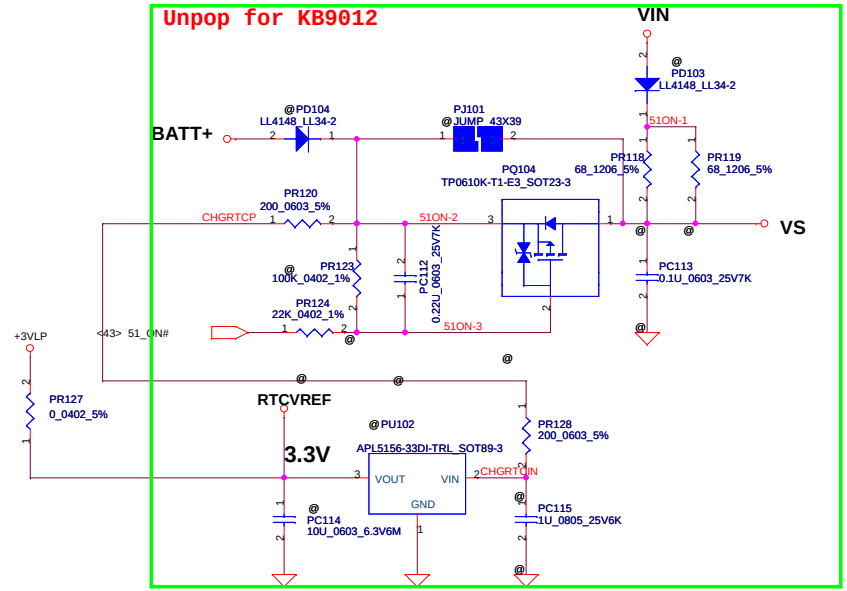
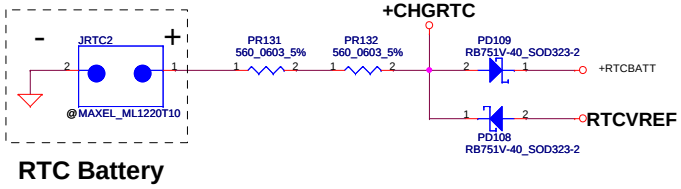
DC030006J00







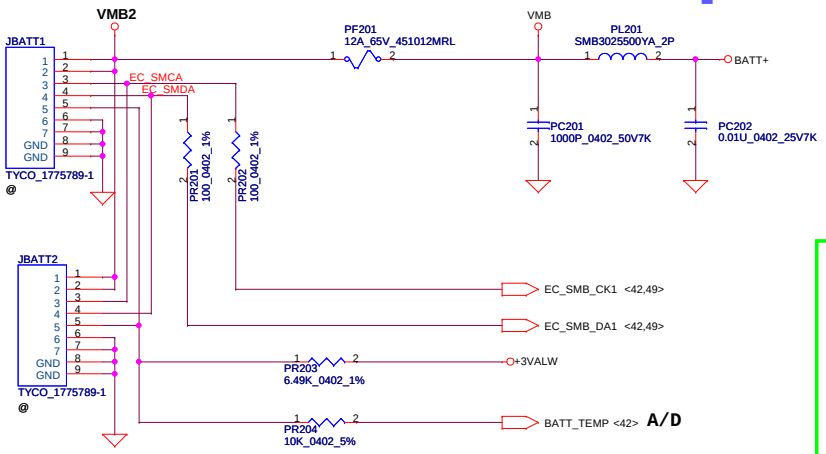
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 47 of 60

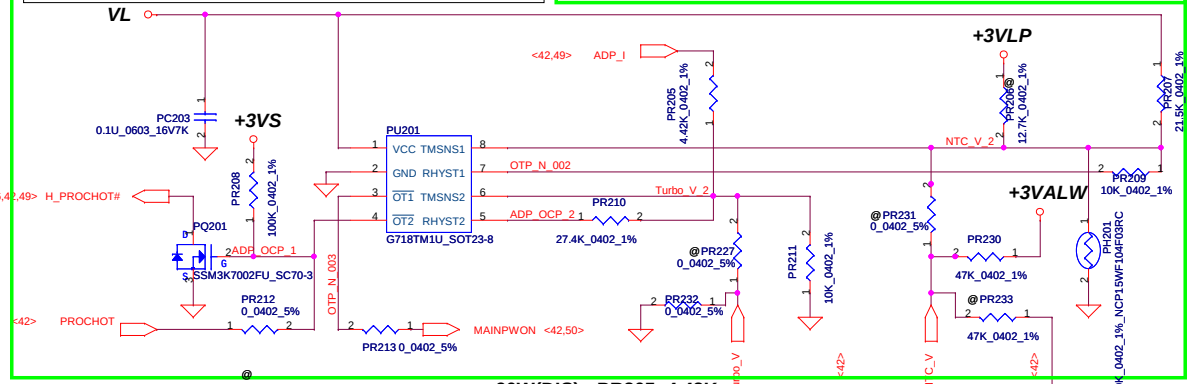


ADP_I need to write Charge Options Register (0x12H)=> bit6=1

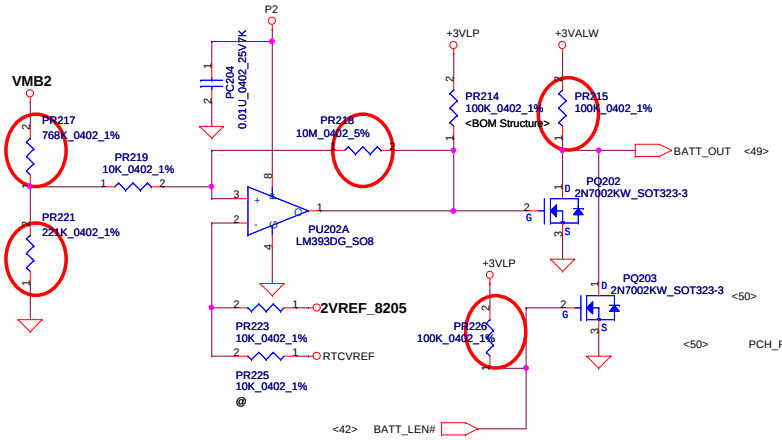
0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output

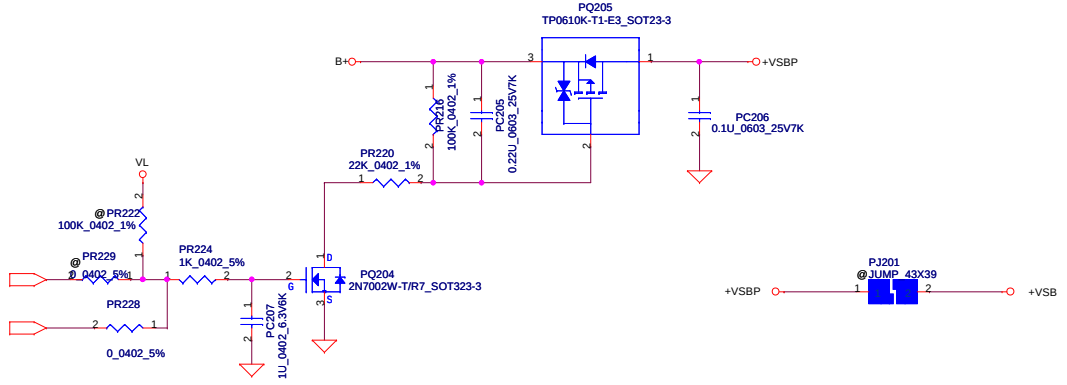
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211,PQ201,PR208,PR212



90W(DIS) : PR205=4.42K
PR210=27.4K
65W(UMA) : PR205=402(SD034020080)
PR210=5.11K





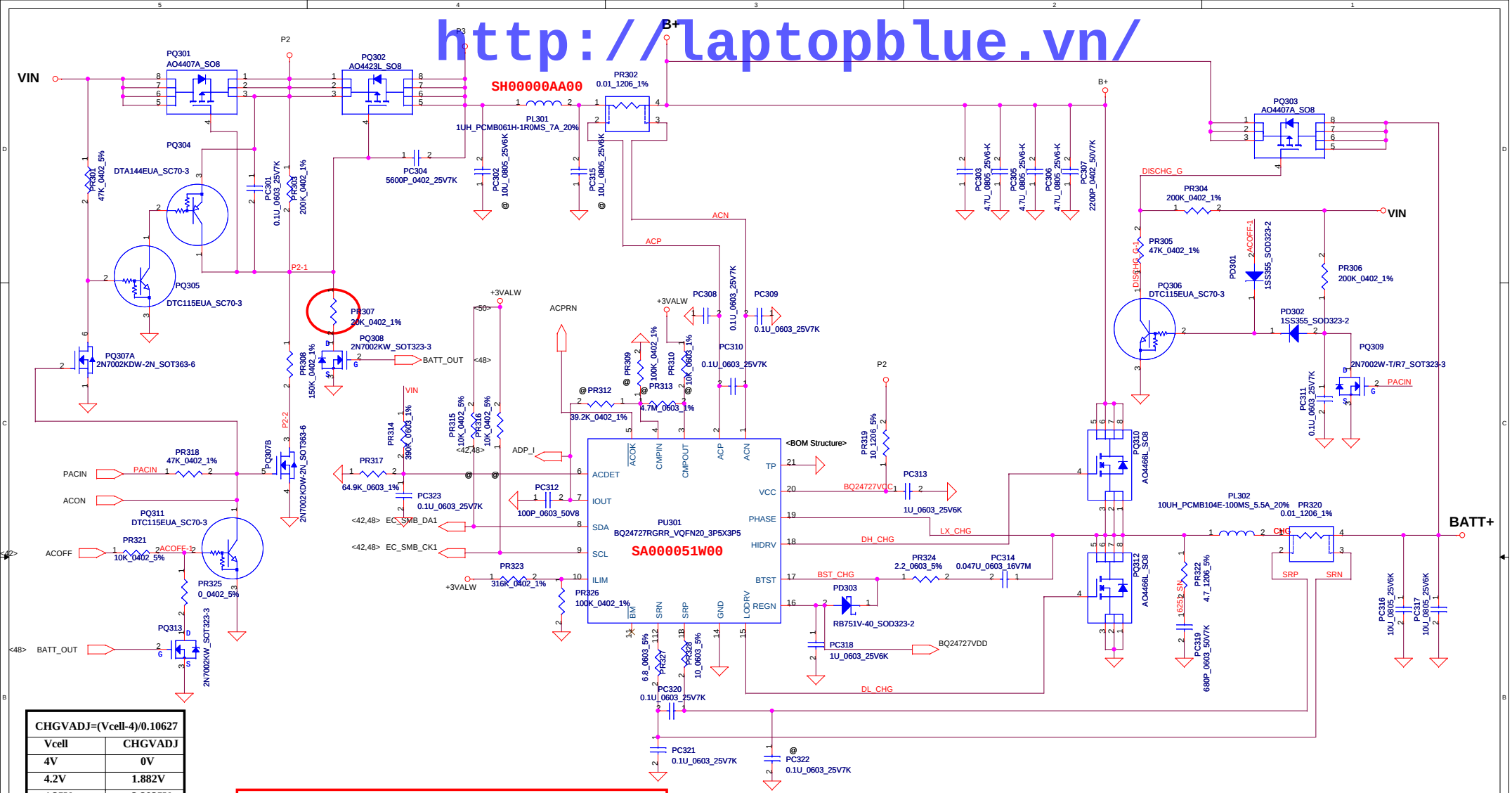
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 48 of 60



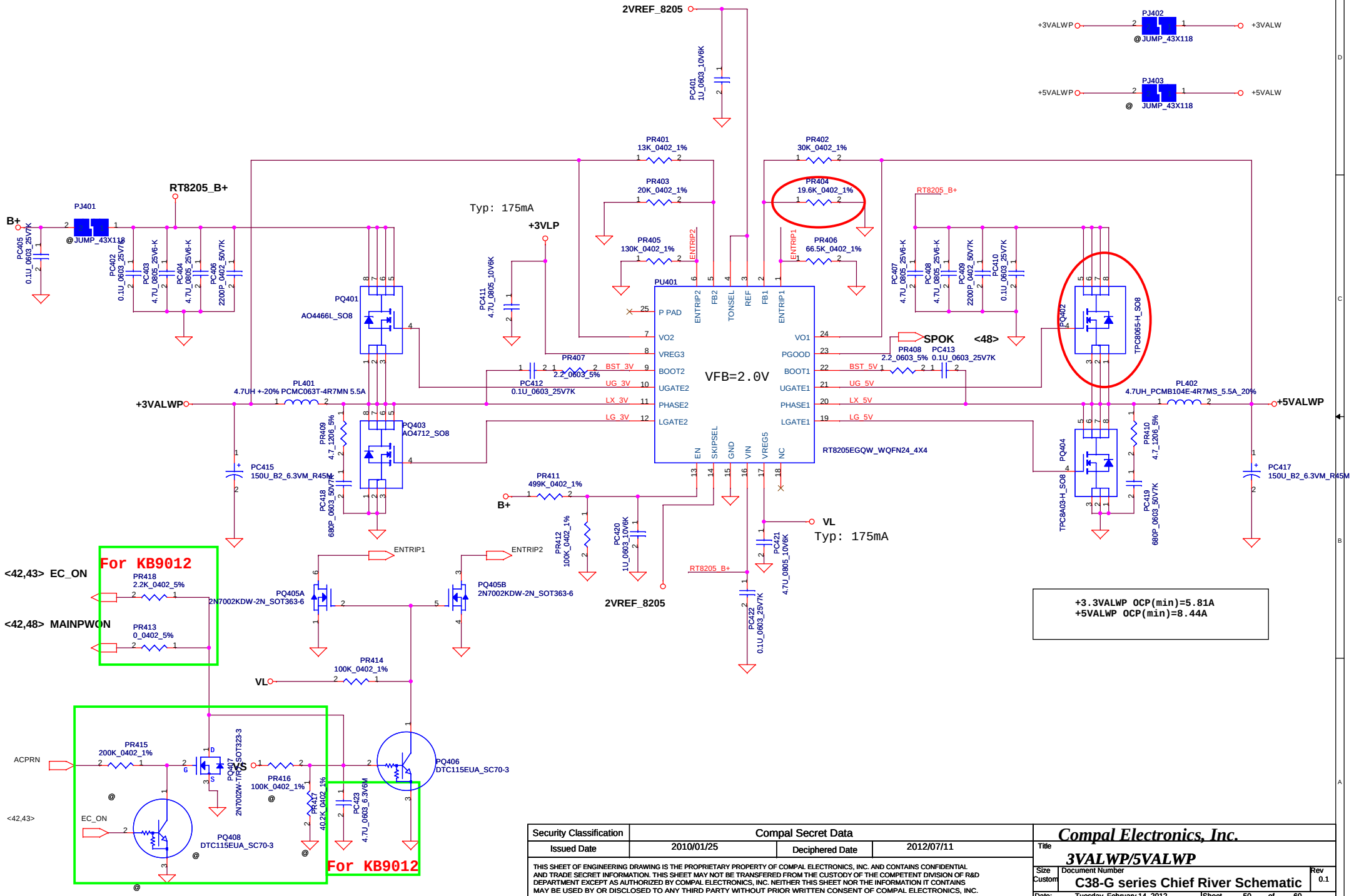
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

Compal Electronics, Inc.	
Title	CHARGER
Size	Document Number: C38-G series Chief River Schematic
Rev	0.1
Date: Tuesday, February 14, 2012	Sheet 49 of 60

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



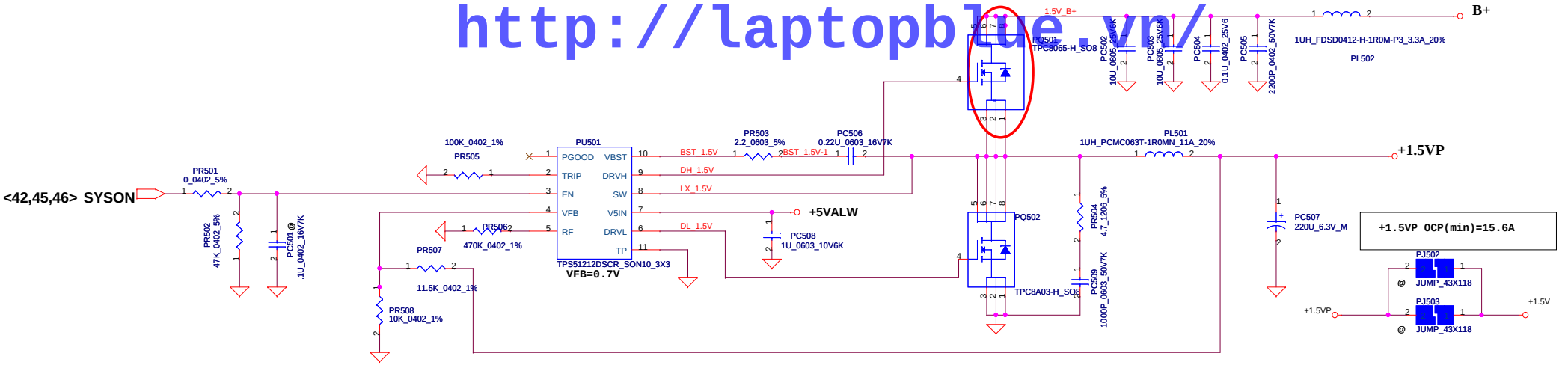
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

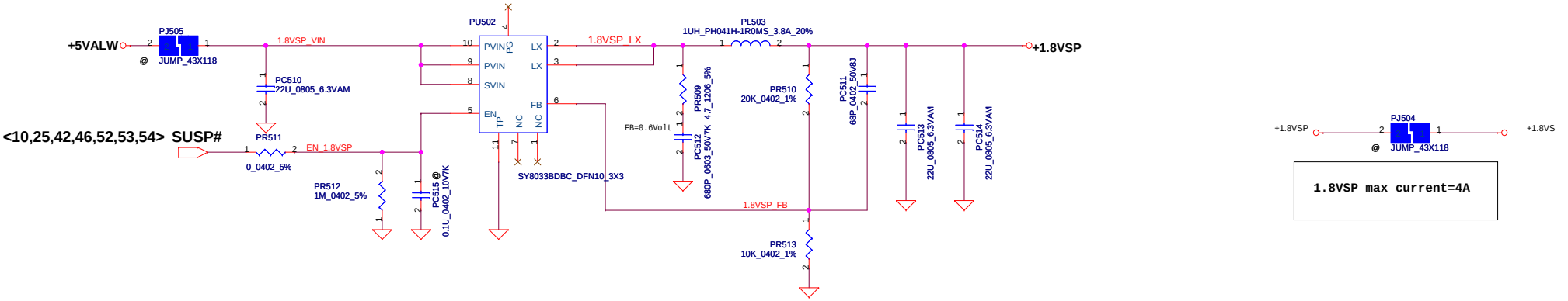
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1

Date: Tuesday, February 14, 2012 Sheet 50 of 60





Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 51 of 60

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

PU601 TPS51461RGER_QFN24_4X4
PU602 TPS51212DSCR_SON10_3X3
PQ601 TPC8037-H_SO8
PQ602 TPC8A03-H_SO8
PQ603 SSM3K7002FU_SC70-3

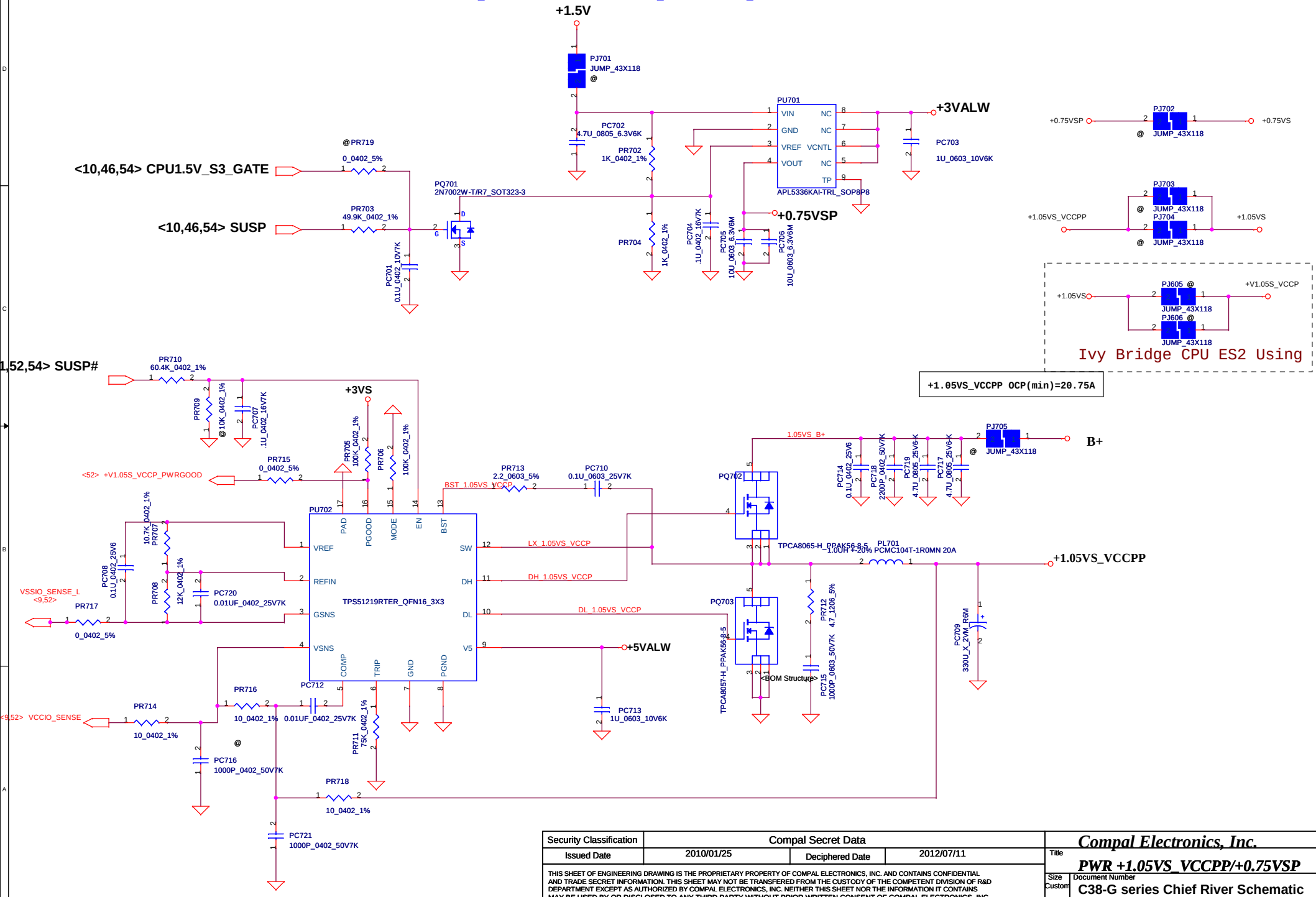
Security Classification	Compal Secret Data
Issued Date	2010/01/25
Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR +VCCSAP/1.0

Size: C | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 52 of 60



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	PWR +1.05VS_VCCPP/+0.75VSP		
Size	Document Number		Rev
Custom	C38-G series Chief River Schematic		0.1
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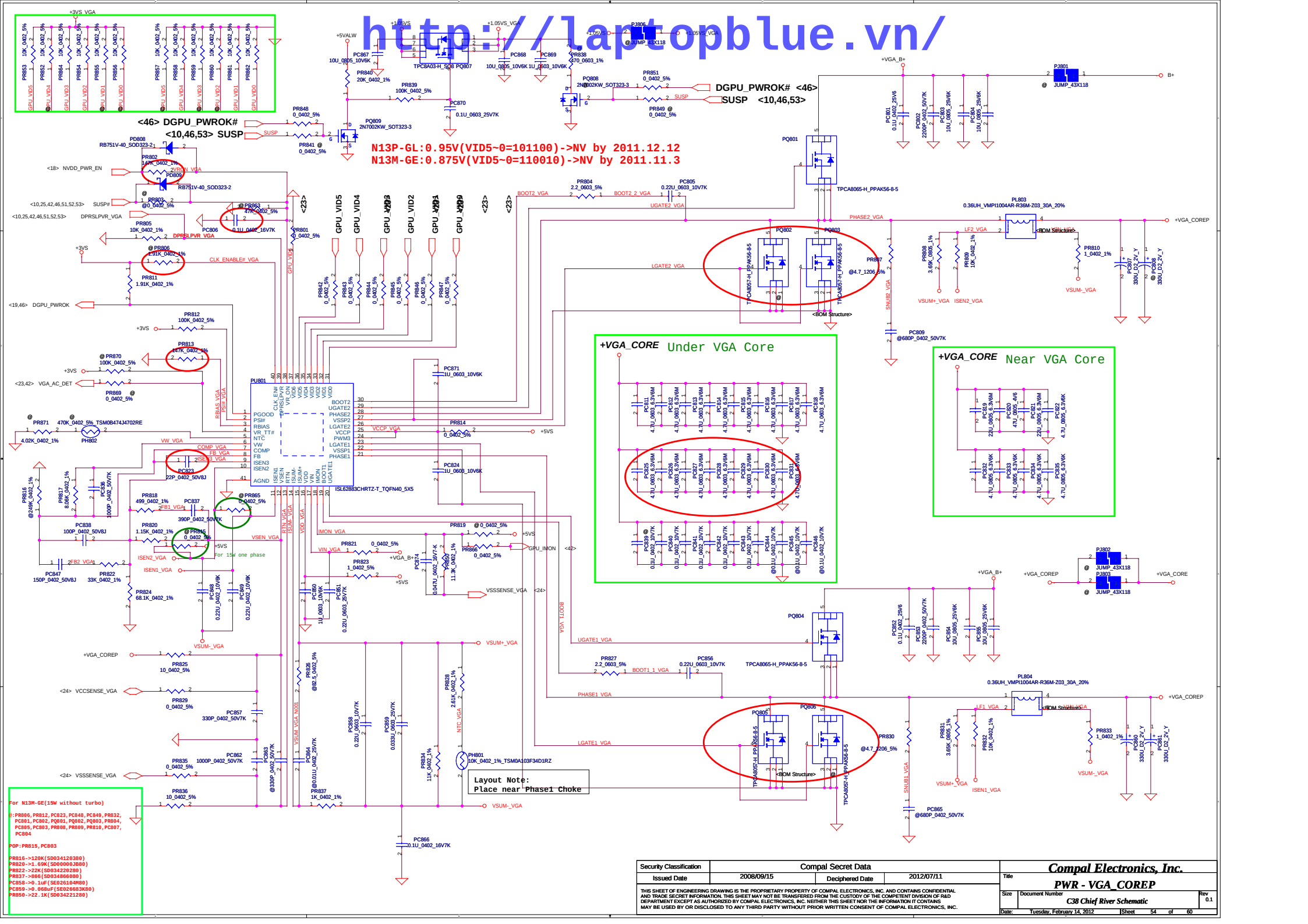

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

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Title: **PWR - VGA_COREP**

Size	Document Number	Rev
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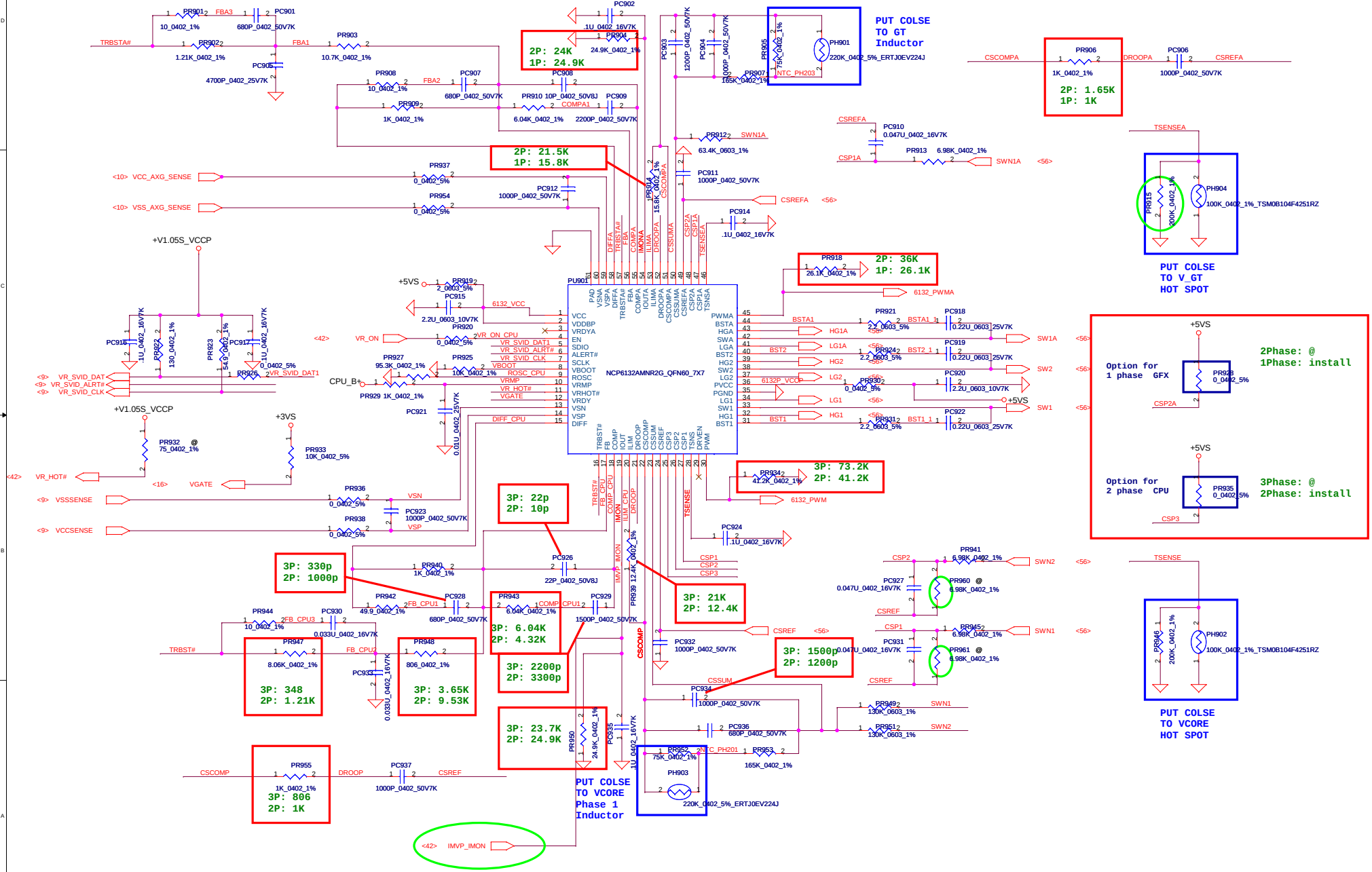
PR915,PR946=200K(setting 113 degreeC)
PR915,PR946=8.25K(setting 93 degreeC)



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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Title: PWR-CPU_CORE

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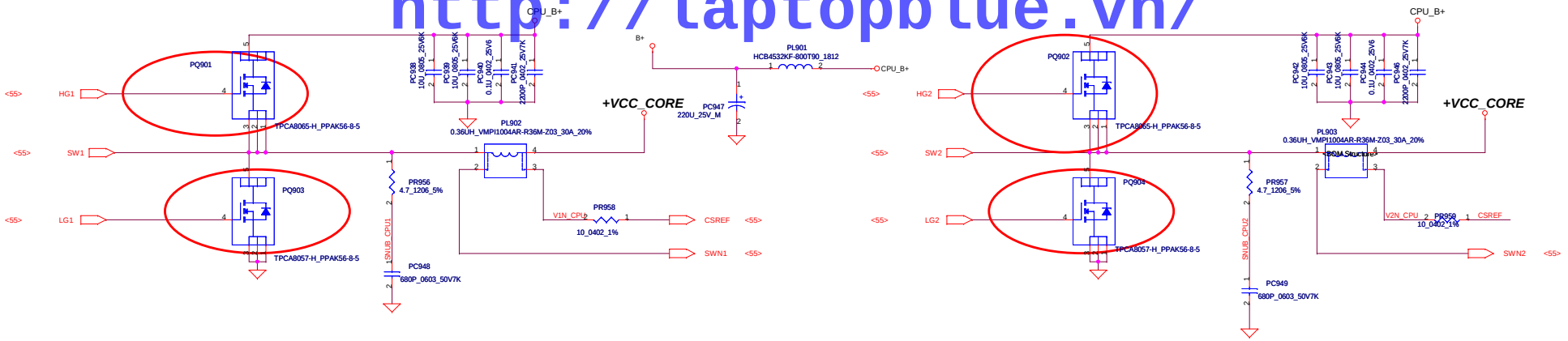
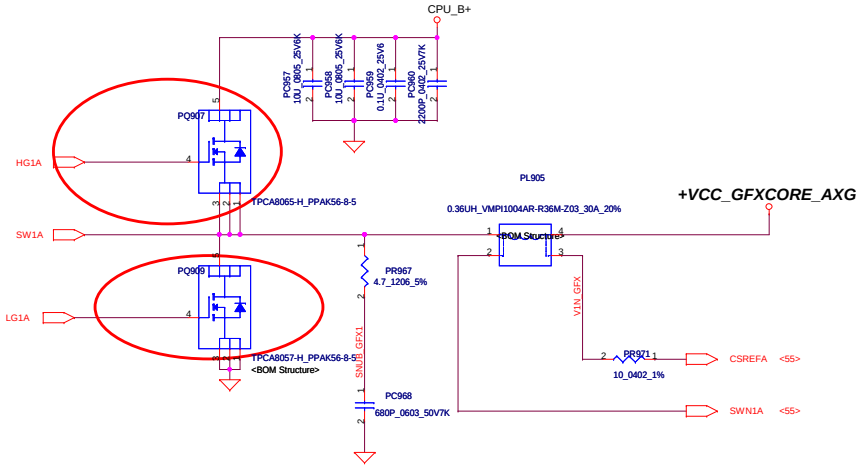


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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Title: PWR-CPU_CORE

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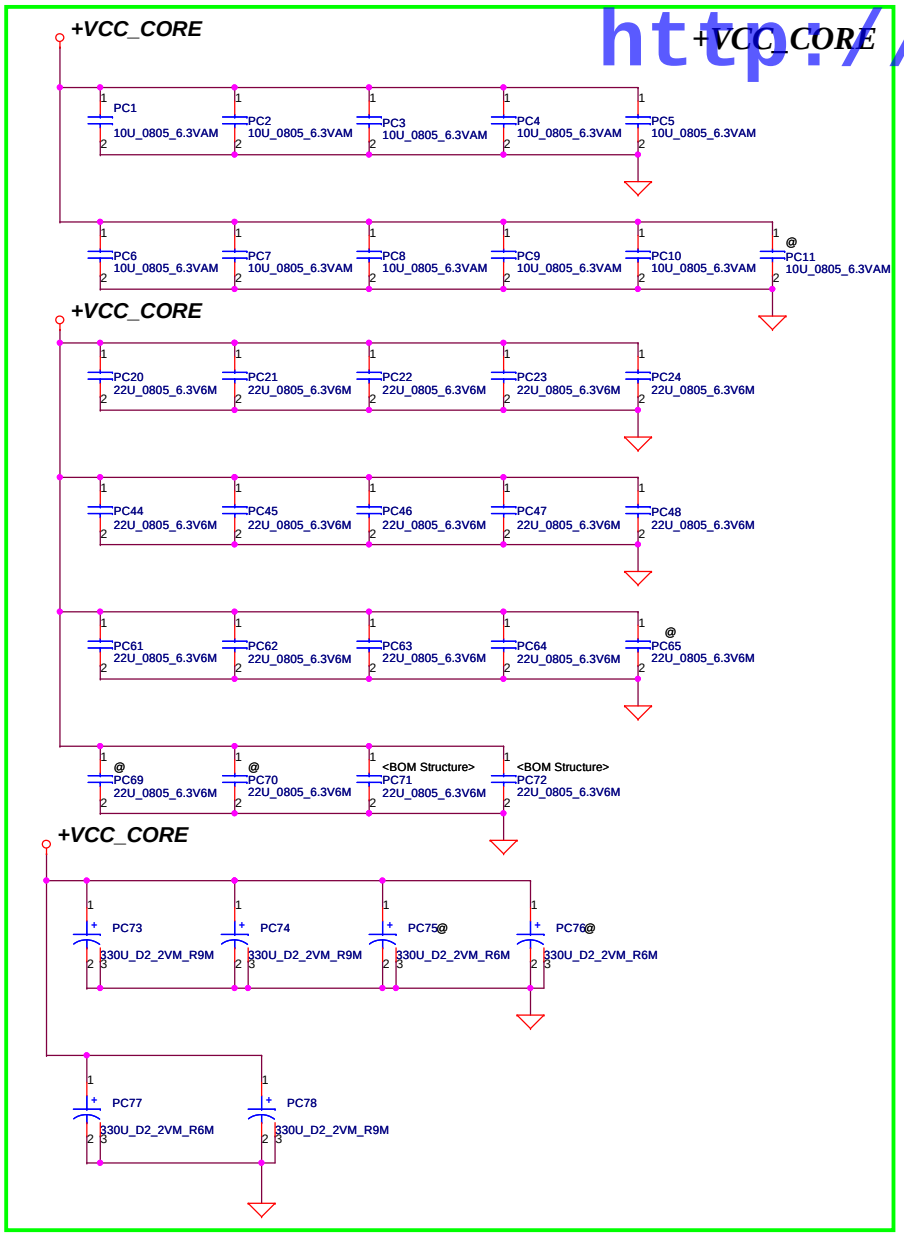
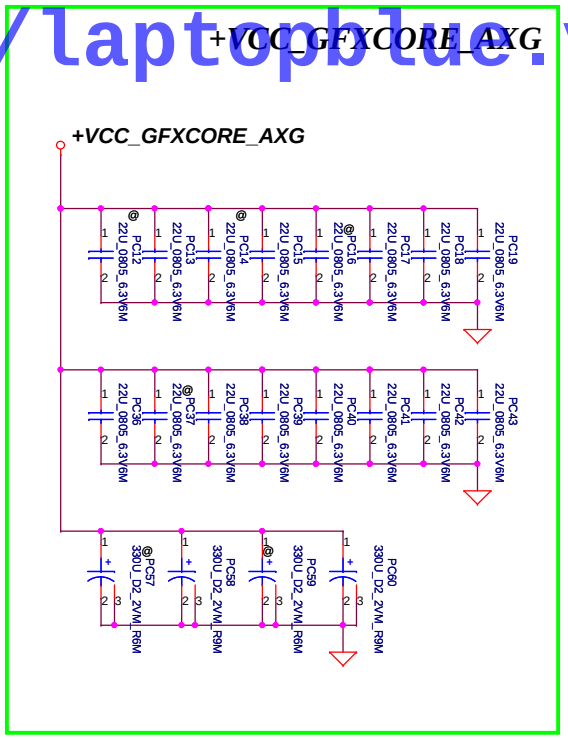
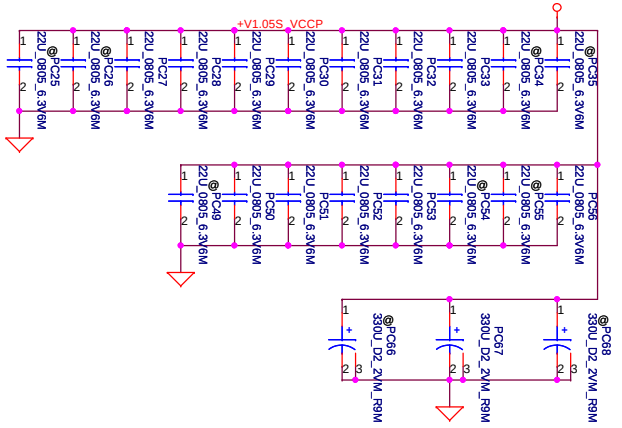




Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

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Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	C38-G series Chief River Schematic	0.1

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	add PR865 for ISL62883 one phase solution and unpop for two phase solution.	P54	add PR865	2011.08.29	DVT
2	unpop PR315,PR316 for SMBus SPEC.	P49	unpop PR315,PR316	2011.08.29	DVT
3	delet PSI#_VGA for NV chip.	P54		2011.10.14	DVT2
4	change NTC_V pull high voltage from +3VLP to +3VALW	P48			
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1

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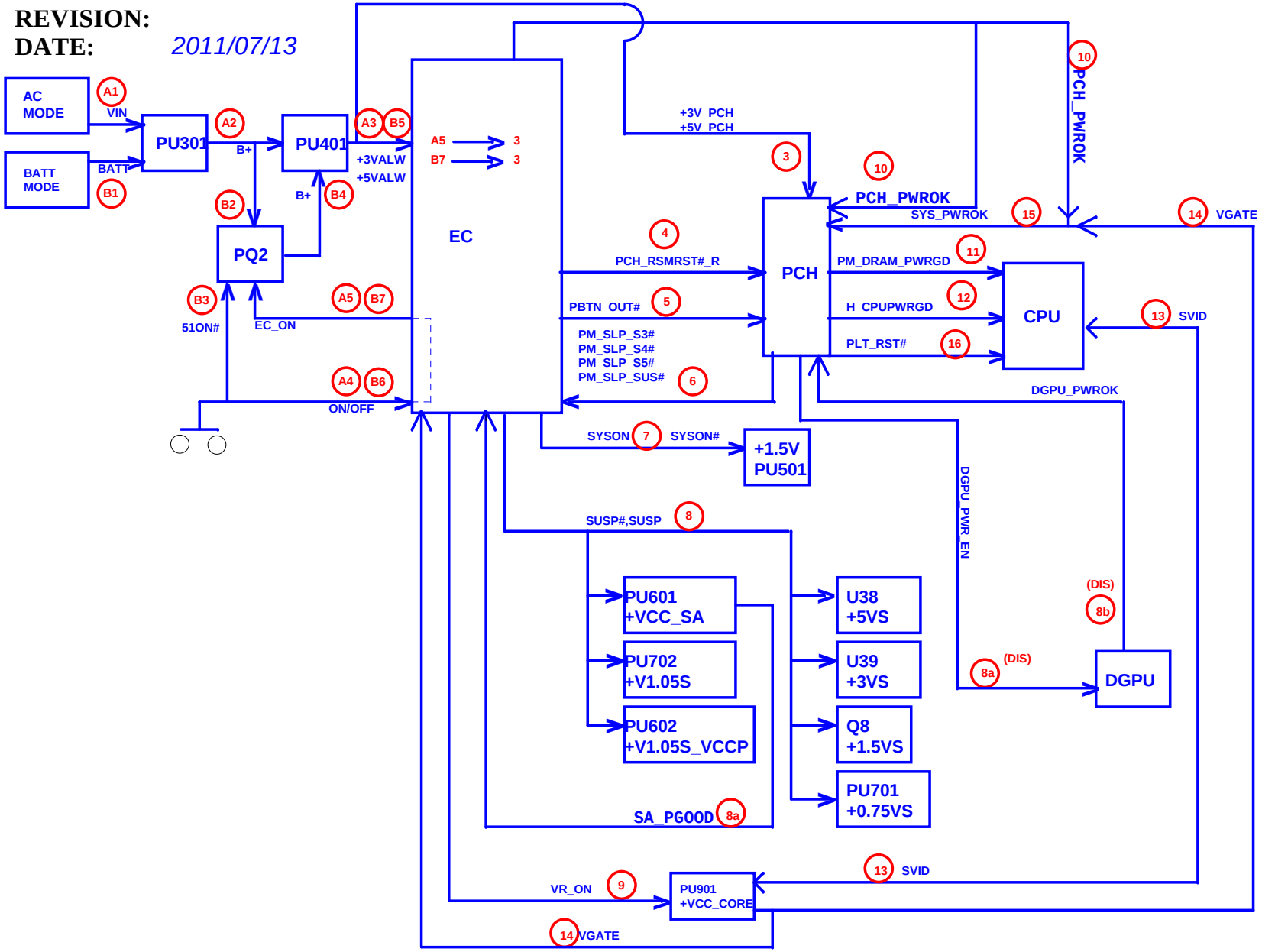
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: ***Power sequence***

Size	Document Number	Rev
Custom	*LA-7981P*	0.2

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Item	Reason for change	PG#	Modify List	Date	Phase
1	GPU 13M GPU Device loss (Pcie lan x8 issue)	8	Add R43		DVT
2	HDD no function	40	Add R550		DVT
3	10/100 lan no function & change to overclocking mode	37	ADD R1372 ; DEL R31		DVT
4	For DGPU_PWROK leakage issue.(Let timing +5VS > +3VS)	46	Change C726 from 0.1uF to 0.01uF		DVT
5	For S3 can't wake up	10	Change R56 from 15K to 4.7K change R885 from 0 ohm to 15K		DVT
6	Can unstuff RV66 for N13P-GL & as NV DG	27	RV66 change to N13M@		DVT
7	GPU N13P-GL QS sample change strap	32	RV94 change from 45.3K to 10K		DVT
8	PCH 25Mhz for vender crystal test report change CL to 12pF	15	C196;C197		DVT
9	GPU 27Mhz for vender crystal test report change CL to 15pF	23	CV37;CV38		DVT
10	EC_LID_OUT# internal PD 20K, follow ORB change R230 from 10k to 1K	19	R230		DVT
11	For GPIO70;GPIO71 voltage level issue (internal Pull High 20k)	19	R705;R706 Change from 10K to 200K		DVT
12	for DVT board ID Change R695 from 33k to 18k	42	R695		DVT
13	LAN Surge test fail change P/N from SP050006E00 to SP050006W00	27	T1;T2		DVT
14	Del ODD Power Control function component	40	R568;Q100;R675;C607;Q99		DVT
15	AO4430L(SB000007O10)EOL Change to AO4304 (SB00000RV00)	46	U49		DVT
16	Del (PCH AUX Power) Reserve component no use	46	C780;C781;C782;C783;R778;Q120;U40		DVT
17	PCH(U4) P/N Change from SA00004NQ30 to SA00004NQ80	14	U4		DVT
18	NV-GPU (U65)P/N change N13M from SA00004V000 to SA00004V010 N13P Keep SA000051A00	23	U65		DVT
19	EXT USB 3.0 IC PCIE_WAKE# ; CLKREQ_USB30# leakage on S4	45	Swap Q125;Q121 pin1 & pin3		DVT
20	No function	45	DEL R769		DVT
21	add LAN LDO mode function	37;38	ADD R65;R596;R1449;R1380		DVT
22	USB_OC0# Share with USB_OC4# due to same power switch	18	short USB_OC0#;USB_OC4# ; del R267		DVT
23	Add Capsensor B/D Conn. For best buy use	42	ADD JCAP1 Conn.		DVT

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Item	Reason for change	PG#	Modify List	Date	Phase
24	L1 change to 1 ohm R	20	L1 change to R footprint		DVT
25	Reserve 0 ohm for CMOS Camera shake	33	add R296 0 ohm		DVT
26	Reserve 0 ohm for U49 MOS VGS 20V will burn out issue	46	add R784 0 ohm		DVT
27	For HDD +5VS Power plant del C601; change C598 pin1 power name for good power plant	40	change from +5VS to +5V_HDD ;DEL C601		DVT
28	For Audio jack support APPLE and NOKIA function Reserve	43	add R684;R685;R688;R686 0ohm R		DVT DVT
29	For standard part cost down change 10uF 0805 type to 0603 type	10,20 21,33 37,39 40,46	C124;C125;C126;C127;C130;C221;C215;C395; C231;C519;C937;C953;C954;C591;C608;C602; C720;C721;C723;C724;C782;C783;C717;C718; C856;C852;C851;C853		DVT DVT
30	change Crystal foot print follow standard parts from 5032 to 3225 package	15;23; 37	Y2;Y6;YV1		DVT
31	change 0ohm to short-pad (R0402_0ohm)	7;8; 10;15 16;20; 33;36; 40;43	R40;R60;R77;R144;R190;R193;R198;R181;R185; R265;R538;R498;R500;R583;R614		DVT DVT DVT
32	Reserve BT_DISABLE (GPI022) for combo card(BT+WLAN)	19	ADD R892;R897		DVT
33	U35;U36 Change footprint without thermal PAD type	44;45	U35;U36		DVT
34	PU 10K with 3V3 on N13P-GL/ for CEC signal	24	RV230		DVT
35	VGA_GPIO3;VGA_GPIO16 change connect DPRSLPVR_VGA to PSI#_VGA	23;54	RV113;RV114		DVT
36	Fix VGA power on CLKREQ has drop (QV2 gate add 0.1uF)	23	CV42		DVT
37	LED5 和LED2 Location sawp ; Location name D9 change to LED6	43	LED2;LED5;LED6		DVT
38	For Lan surge fail add 0 ohm on MDO2-;MDO2+;MDO3-;MDO3+	38	R304;R305;R306;R307		DVT
39	Change UV2 PN from SA007080B90 to SA00000OH00	23	UV2	09/28	DVT
40	Change 2M BIOS ROM from SA00003FO00 to SA00003FO10	14	U6	09/29	DVT
41	Correct PCIE_PRX_DTX_P4/N4 of U32 (SWAP)	45	U32	10/03	DVT
42	Reserve +5VS to JCR1, add R689 ,R690	43	R689 (@),R690	10/03	DVT
43	Update Power sheet of 1003 version	47~58		10/04	

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Title	HW-PIR2
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Item	Reason for change	PG#	Modify List	Date	Phase
44	CPU Symbol Update	5,6,7, 8,9,10,11	Location : Jcpu1		PVT
45	Change 10P 50V Cap from 1206 to 0603	38	Location : C973		PVT
46	S3 Reduction	53	Reserve PR719 for 0.75V		PVT
47	LAN CO-lay x1 GDT & 75ohm	38	Location : R308,R304,R305,R306,R307,DL1,DL2,DL3,DL4		PVT
48	R750 for Power request	42	Location :R750		PVT
49	JUSB3 From 4PIN TO 6 PIN FOR VOLTAGE DROP	44	Location : JUSB3		PVT
50	Add C535 100pF on +3VLP for ESD request - Pony	42	Location : C535		PVT
51	FOR TP POWER SOLUTION	42	Location : R598.R603		PVT2
52	FOR POWER REQUEST	42	Location : R738		PVT2
52	Change C from 0.22Uf to 0.11uF	5 23	Location : C1,C2,C3,C4,C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26,C27,C28,C29,C30, C31,C32, CV6,CV7,CV8,CV9,CV10,CV11,CV12,CV13,CV15, CV17,CV19,CV14,CV16,CV18,CV20,CV22,CV24, CV26,CV21,CV23,CV25,CV27,CV29,CV31,CV33, CV28,CV30,CV32,CV36,CV41,CV34,CV35,		SVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: HW-PIR2

Size: Custom | Document Number: LA-7981P | Rev: 0.1

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