

Compal Confidential

Lotus M/B Schematics Document

14": Elise; 15.6" Exige

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2011/10/27

Version 0.1

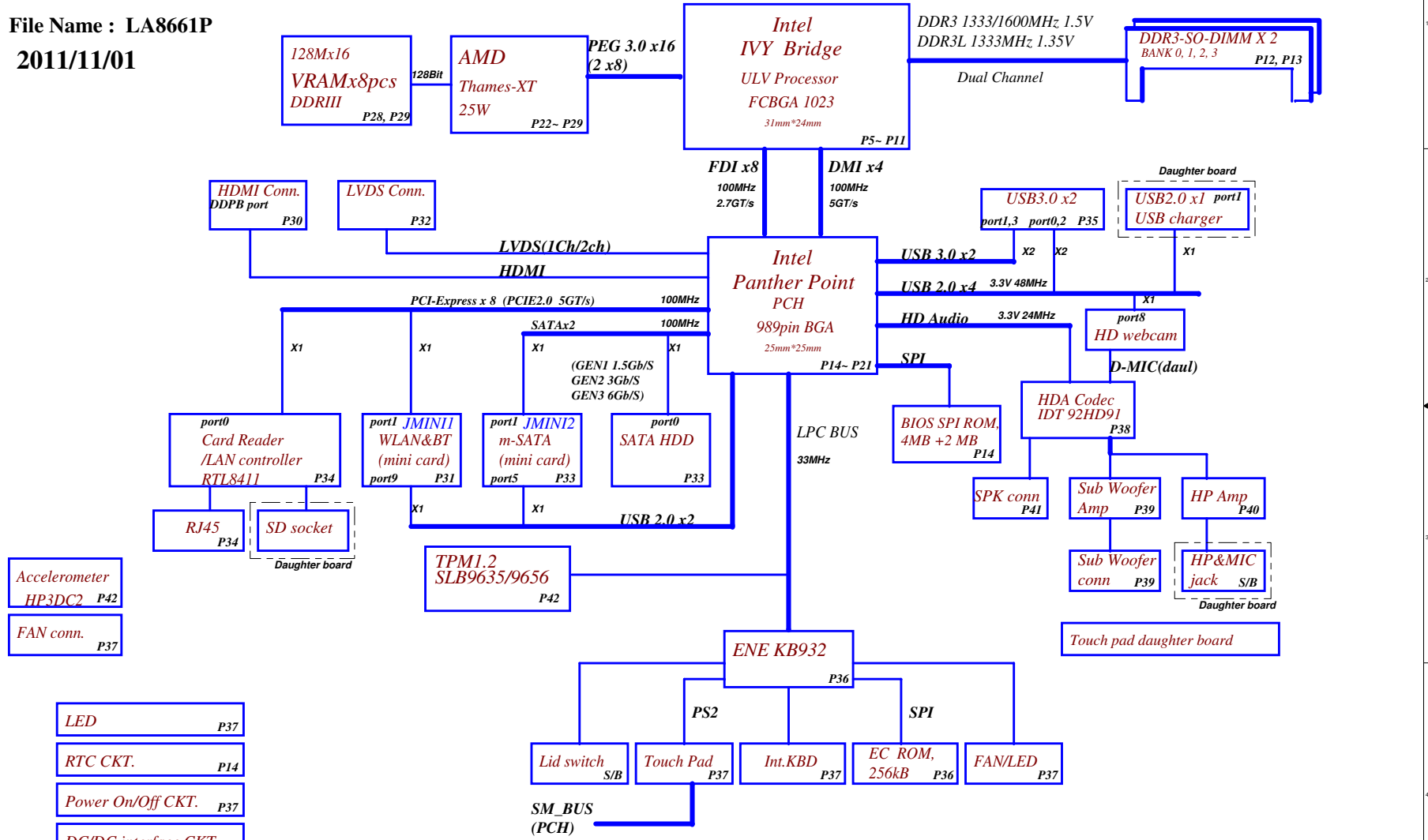
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Model Name : Lotus

File Name : LA8661P

2011/11/01



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QAU30/50 (LA-8661P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+3VALW_EC	+3VALW always to KBC	ON	ON	ON
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resistor)	ON	ON	ON
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+VGA_CORE	GPU power	PX	OFF	OFF
+3VGS	GPU power	PX	OFF	OFF
+1.8VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF
+1.0VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	



EC SM Bus2 address

Device	Address
PCH (Reserve)	

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CRK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CRK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CRK2 EC_SMB_DA2	KB930						V			V	V
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	PCIE LAN CARD READER	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	mini WLAN	CLKOUTFLEX2	None
	CLKOUT_PCIE2	None	CLKOUTFLEX3	DGPU_PRSN#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
CLKOUT_PCIE7	None			
CLKOUT_PEG_B	None			

Symbol Note :
 : means Digital Ground
 : means Analog Ground

Project ID 30UMA@ 30DIS@ 50UMA@ 50DIS@

PCB	LA-8661P	LA-8662P
	PX@	UMA@

BY SKU		
TPM	9635@	9656@
CPU	CPUM1A1@	
	CPUM2A2@	
	CPUDIS@	
VRAM	X76@	H2G@
	M2G@	S2G@

Option	@	CONN@	USB30@	PX@	UMA@	DIS@	THA@
UMA	X	X	V	X	V	X	X
DIS	X	X	V	V	X	V	V

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

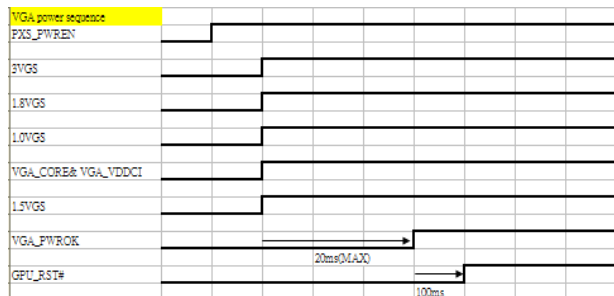
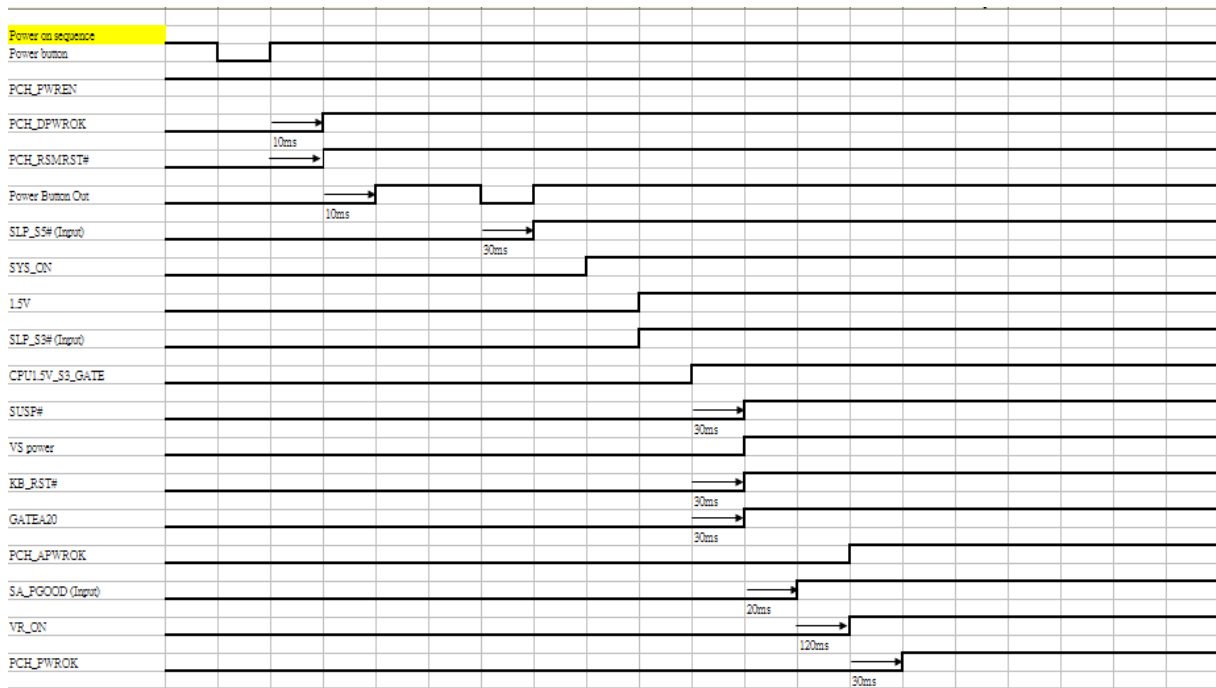
SATA	DESTINATION
SATA0	SATA, JHDD1
SATA1	m-SATA, JM1N2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (left Side)
		1	USB2.0 (right Side)
		2	USB2.0 (left Side)
	UHCI1	3	None
		4	None
		5	None
		6	None
7		None	
8		Camera	
EHCI2	UHCI4	9	Mini Card(WLAN& BT)
		10	None
	UHCI5	11	None
		12	None
UHCI6	13	None	

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	USB3.0 (left Side)
	4	None

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UCPU1 CPUIDIS01@
I5-2467M CPU
SA00004X000

UCPU1 CPUIDIS02@
I5-2367M CPU
SA000051H20

UCPU1 CPUIDIS03@
I5-2367M CPU
SA000051H20

UCPU1 CPUIDIS04@
I5-3317U CPU
SA00005K600

UCPU1 CPUUMA3@
I5-2367M CPU
SA000051H20

UCPU1 CPUUMA4@
I7W 1.5GHz GT2 ES2 QBP7
SA00005B010

UCPU1 CPUUMAS@
I7W 1.7GHz no onlg ES2 QBT0
SA00005B020

UCPU1 CPUUMA1@
I7W 1.5GHz no onlg ES2 QBP8
SA00005AZ10

UCPU1 CPUUMA2@
I7W 1.5GHz no onlg ES2 QBT9
SA00005AZ20

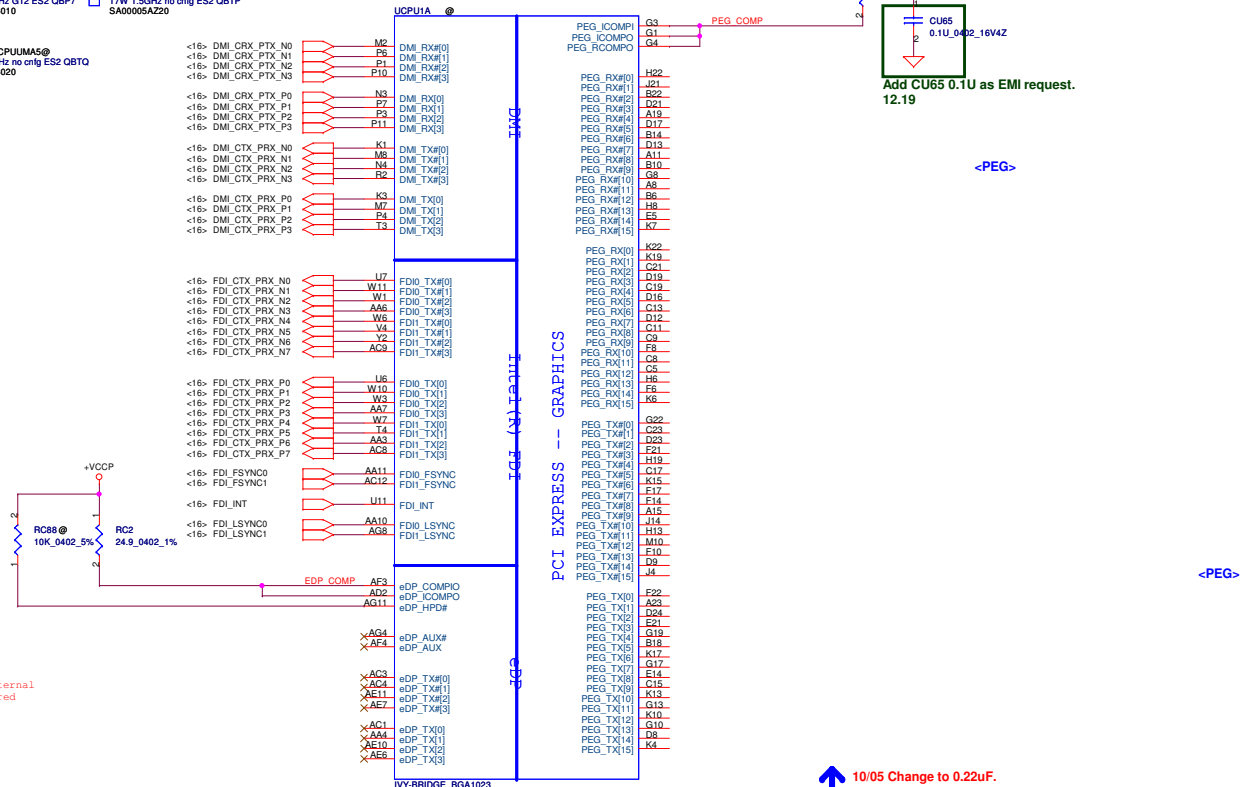
Sandy Bridge:
Intel Core i5-2467M: SA00004X000 (4619HY32L01)

Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QBT9: SA00005AZ20(4619HZ32L02)

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

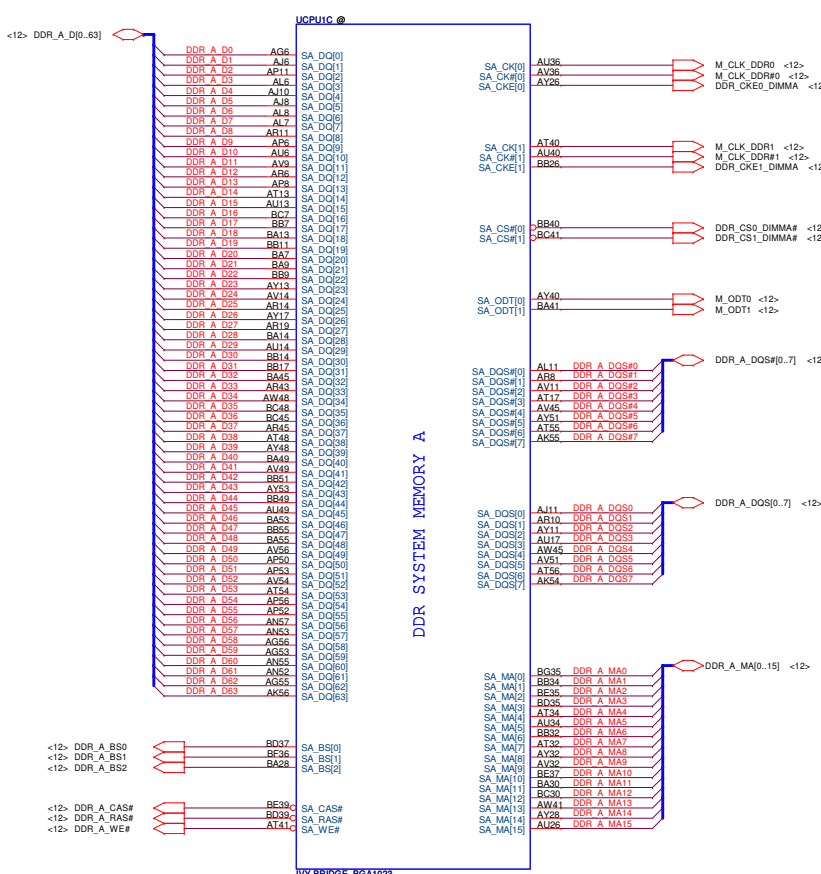
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

NOTE:eDP_COMPIO and eDP_ICOMPO should not be left floating even if Internal Graphic is disabled since they are shared with other interfaces

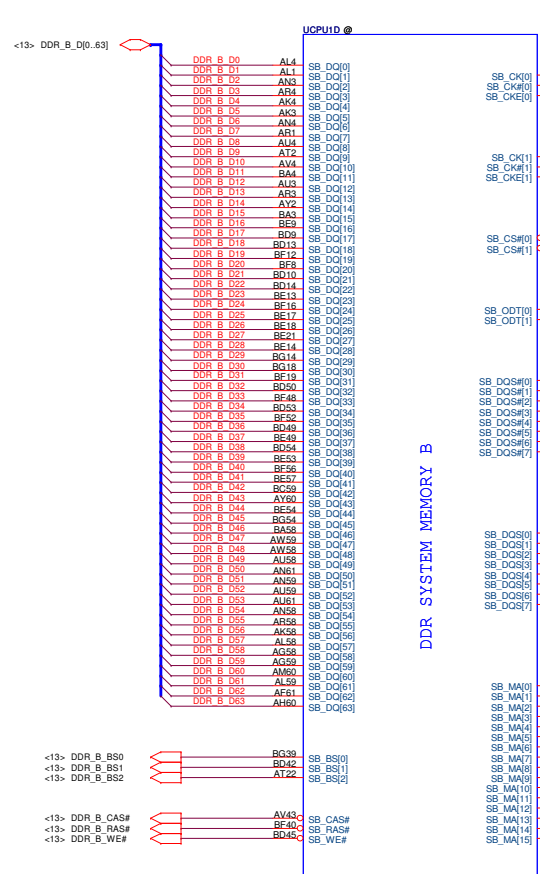


10/05 Change to 0.22uF.
Typ- suggest 220nF. The change in AC capacitor value from 180nF to 265nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

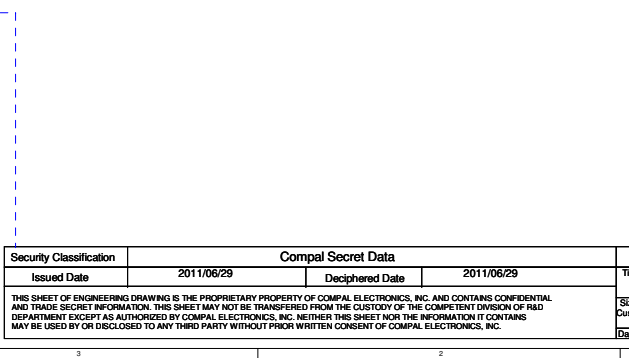
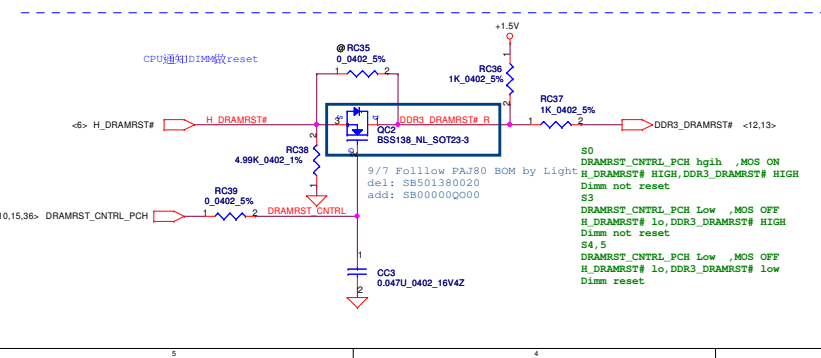
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DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

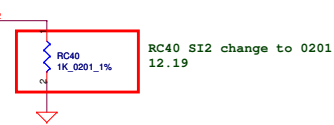


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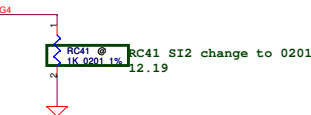
CFG Straps for Processor

PEG bus is reversed, need to PD.

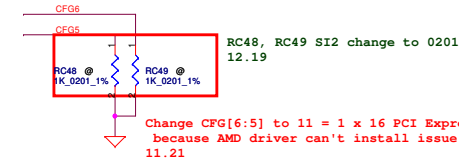
11.01



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

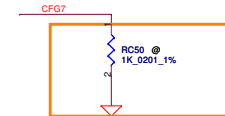


Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express *

12/16: Change to 0201 for SI2 because standoff PAD

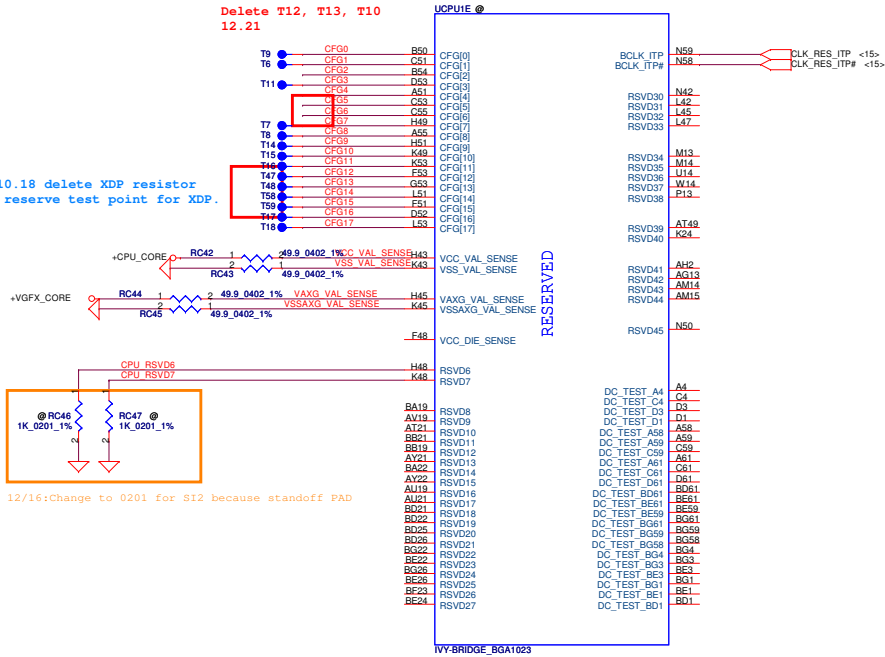


PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Change to part G.

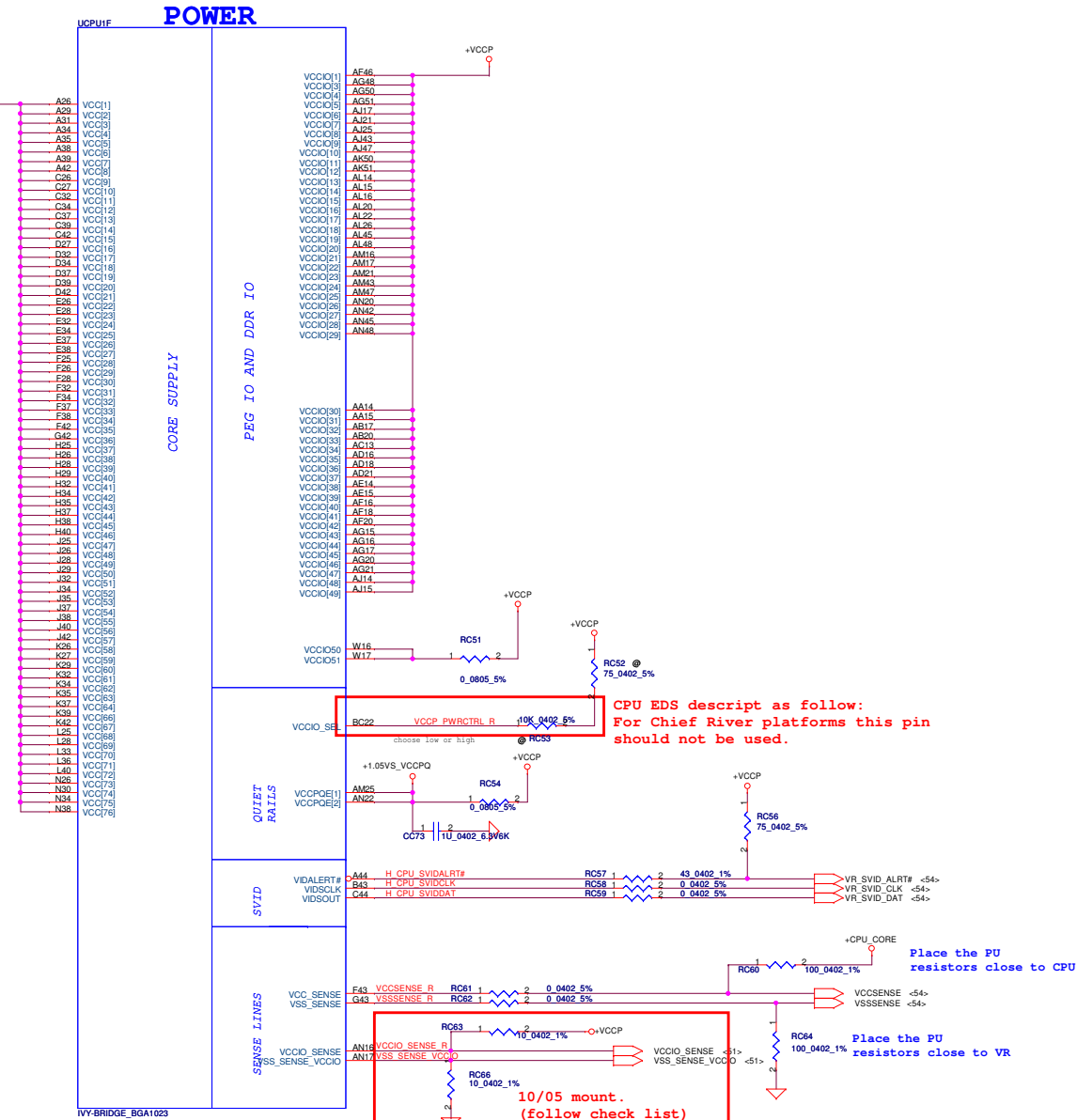
Delete T12, T13, T10 12.21

2011.10.18 delete XDP resistor just reserve test point for XDP.

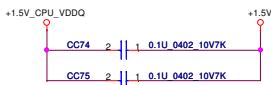


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Title PROCESSOR(47) R5VD.CFG		
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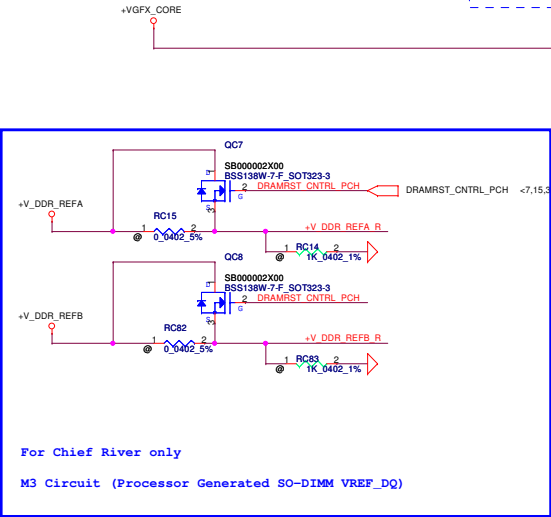


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• Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
 • VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

POWER



For Chief River only
 M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

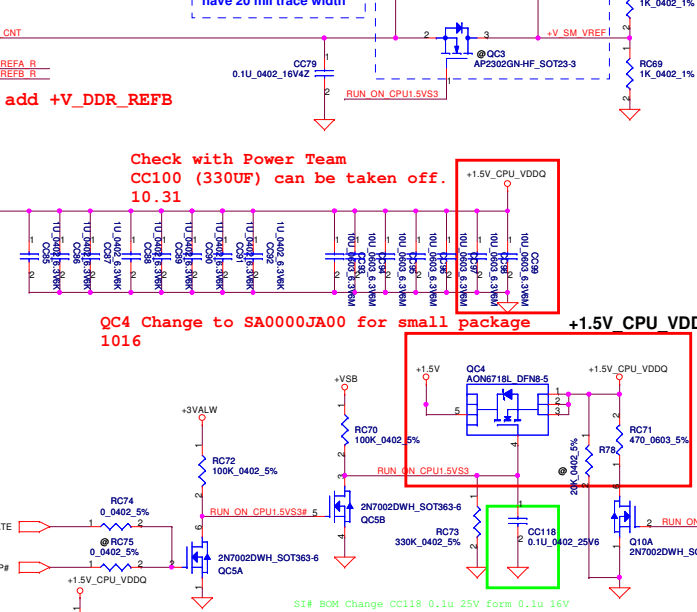
10/03 add +V_DDR_REFB

- AA46 VAXG[1]
- AB47 VAXG[2]
- AB50 VAXG[3]
- AB51 VAXG[4]
- AB52 VAXG[5]
- AB53 VAXG[6]
- AB54 VAXG[7]
- AB56 VAXG[8]
- AB58 VAXG[9]
- AB59 VAXG[10]
- AC41 VAXG[11]
- AD47 VAXG[12]
- AD48 VAXG[13]
- AD50 VAXG[14]
- AD51 VAXG[15]
- AD52 VAXG[16]
- AD53 VAXG[17]
- AD54 VAXG[18]
- AD56 VAXG[19]
- AD59 VAXG[20]
- AE46 VAXG[22]
- AE48 VAXG[23]
- AE49 VAXG[24]
- P47 VAXG[25]
- P48 VAXG[26]
- P49 VAXG[27]
- P51 VAXG[28]
- P52 VAXG[29]
- P53 VAXG[30]
- P56 VAXG[31]
- P58 VAXG[32]
- P61 VAXG[33]
- T58 VAXG[34]
- T59 VAXG[35]
- T61 VAXG[36]
- L46 VAXG[37]
- V47 VAXG[38]
- V48 VAXG[39]
- V50 VAXG[40]
- V51 VAXG[41]
- V52 VAXG[42]
- V53 VAXG[43]
- V55 VAXG[44]
- V56 VAXG[45]
- V58 VAXG[46]
- V59 VAXG[47]
- W50 VAXG[48]
- W51 VAXG[49]
- W52 VAXG[50]
- W53 VAXG[51]
- W55 VAXG[52]
- W56 VAXG[53]
- W61 VAXG[54]
- Y48 VAXG[55]
- Y61 VAXG[56]

- VREF
- SM_VREF
- SA_DIMM_VREFDQ
- SE_DIMM_VREFDQ
- DDR3 - 1.5V RAILS
- VDDQ[1]
- VDDQ[2]
- VDDQ[3]
- VDDQ[4]
- VDDQ[5]
- VDDQ[6]
- VDDQ[7]
- VDDQ[8]
- VDDQ[9]
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- VDDQ[49]
- VDDQ[50]
- VDDQ[51]
- VDDQ[52]
- VDDQ[53]
- VDDQ[54]
- VDDQ[55]
- VDDQ[56]

- GRAPHICS
- QUIET RAILS
- SENSE LINES
- 1.8V RAIL
- SA RAIL
- SENSE LINES
- VCCSA_VID Lines

- UCPU1G
- AVX3 +V_SM_VREF_CNT
- BE7 +V_DDR_REFA_R
- BG7 +V_DDR_REFB_R
- 10/03 add +V_DDR_REFB
- VDDQ[1] A128
- VDDQ[2] A133
- VDDQ[3] A136
- VDDQ[4] A140
- VDDQ[5] AL30
- VDDQ[6] AL34
- VDDQ[7] AL38
- VDDQ[8] AL42
- VDDQ[9] AN33
- VDDQ[10] AN36
- VDDQ[11] AN40
- VDDQ[12] AN43
- VDDQ[13] AN46
- VDDQ[14] AN49
- VDDQ[15] AN52
- VDDQ[16] AR30
- VDDQ[17] AR32
- VDDQ[18] AR34
- VDDQ[19] AR36
- VDDQ[20] AR40
- VDDQ[21] AR41
- VDDQ[22] AW28
- VDDQ[23] BA40
- VDDQ[24] BB28
- VDDQ[25] BC33
- VCCDQ[1] AM28
- VCCDQ[2] AN26
- BC43 BA43
- VCCSA_VID[0] D48
- VCCSA_VID[1] D49



Check with Power Team
 CC100 (330UF) can be taken off.
 10.31

QC4 Change to SA0000JA00 for small package
 1016

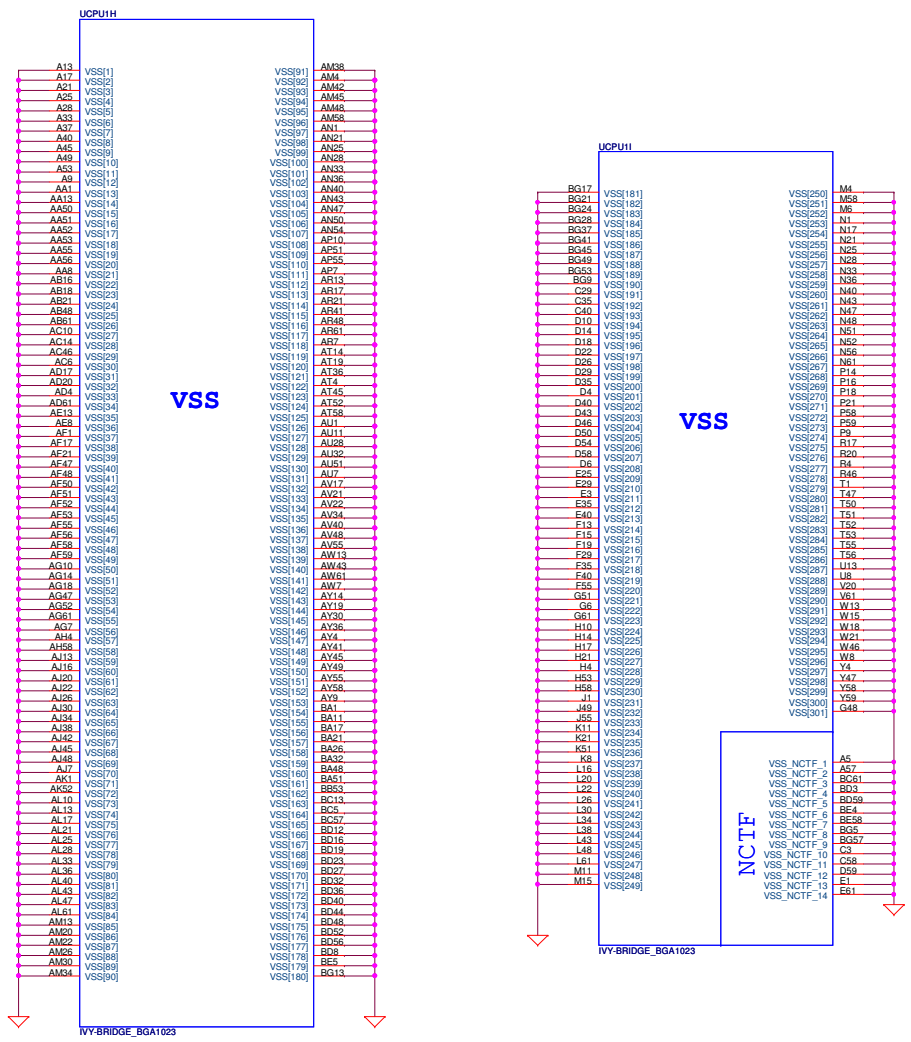
Follow DG 0.71 page 6

VID[0]	VID[1]	2011	2012
0	0	0.30 V	Yes
1	1	0.30 V	Yes
1	0	0.725 V	No
1	1	0.675 V	Yes

Delete CC25 330U cap 10.19
 (after check with power)

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Compal Electronics, Inc.		
Title	PROCESSOR(6/7) PWR	
Size	Document Number	Rev
Custom	LA-8661P	0.1
Date:	Friday, March 02, 2012	Sheet 10 of 58

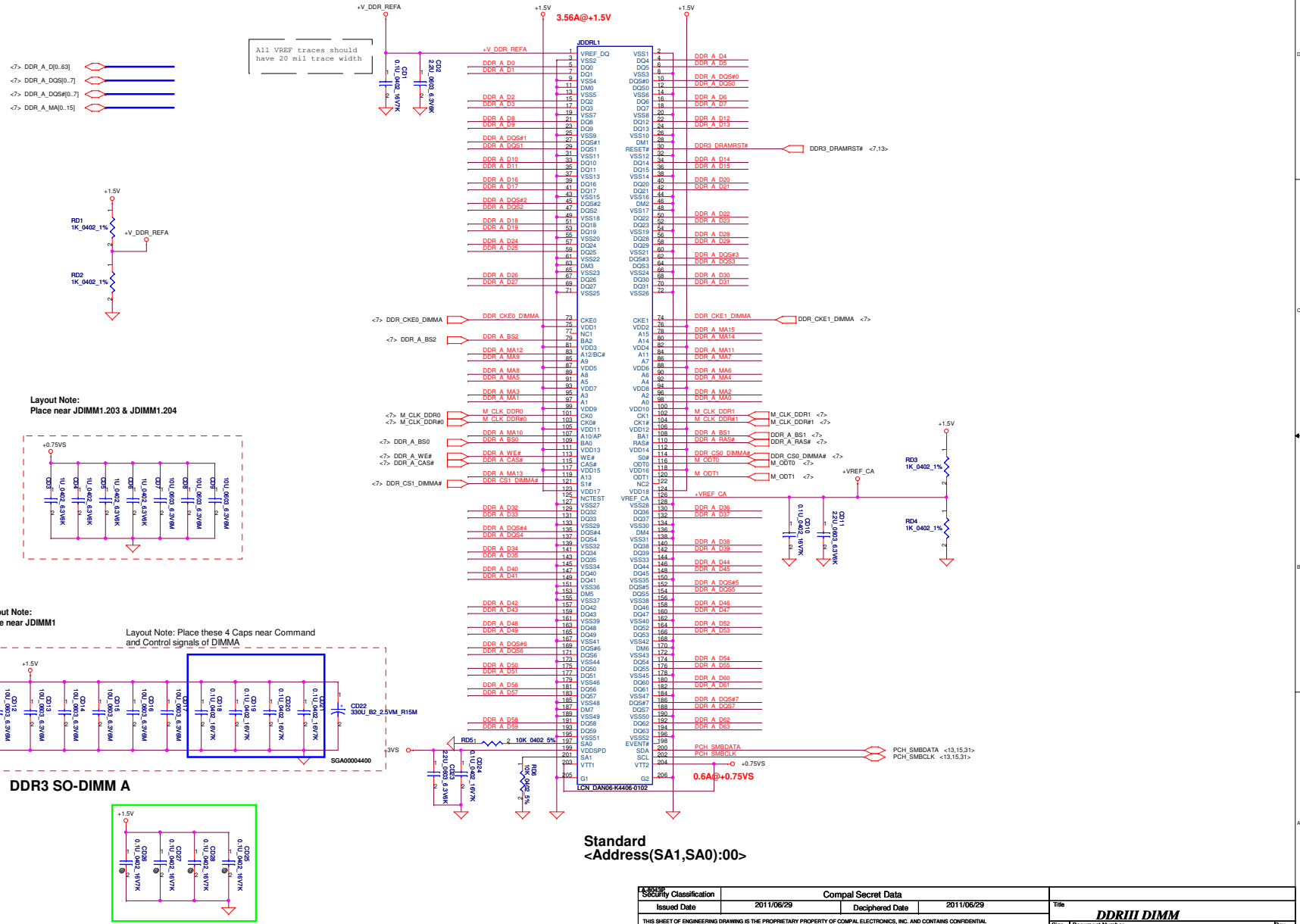


IY-BRIDGE_BGA1023

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Compal Electronics, Inc.		
Title PROCESSOR(7/7) VSS		
Size Custom	Document Number LA-8041P	Rev 0.1
Date Friday, March 02, 2012	Sheet 11	of 58

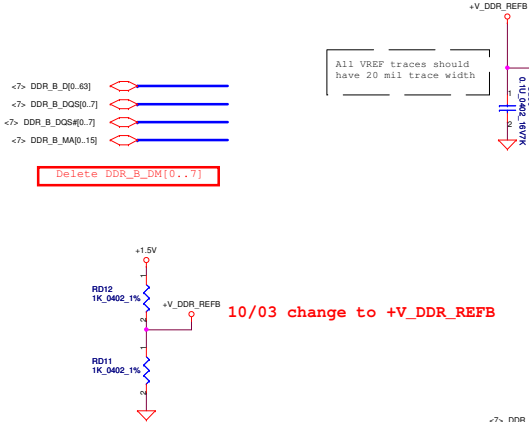
DDR3 SO-DIMM A



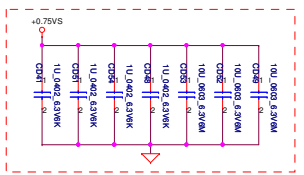
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	DDRIII DIMM	
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Size	Document Number	Date		Sheet	Rev
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10/03 change to +V_DDR_REFB

DDR3 SO-DIMM B

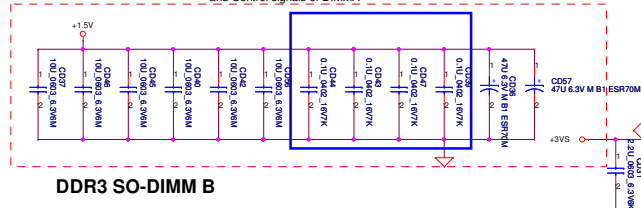


Layout Note: Place near JDIMM1.203 & JDIMM1.204

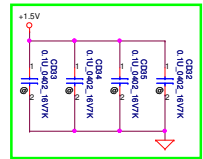


Layout Note: Place near JDIMM1

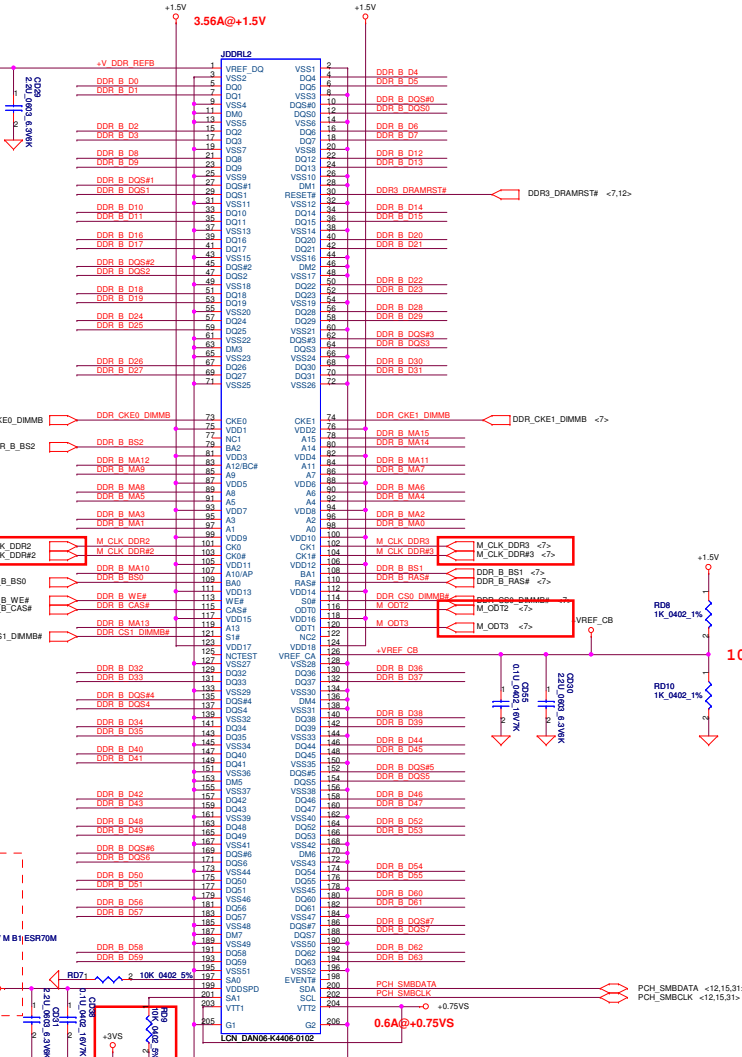
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

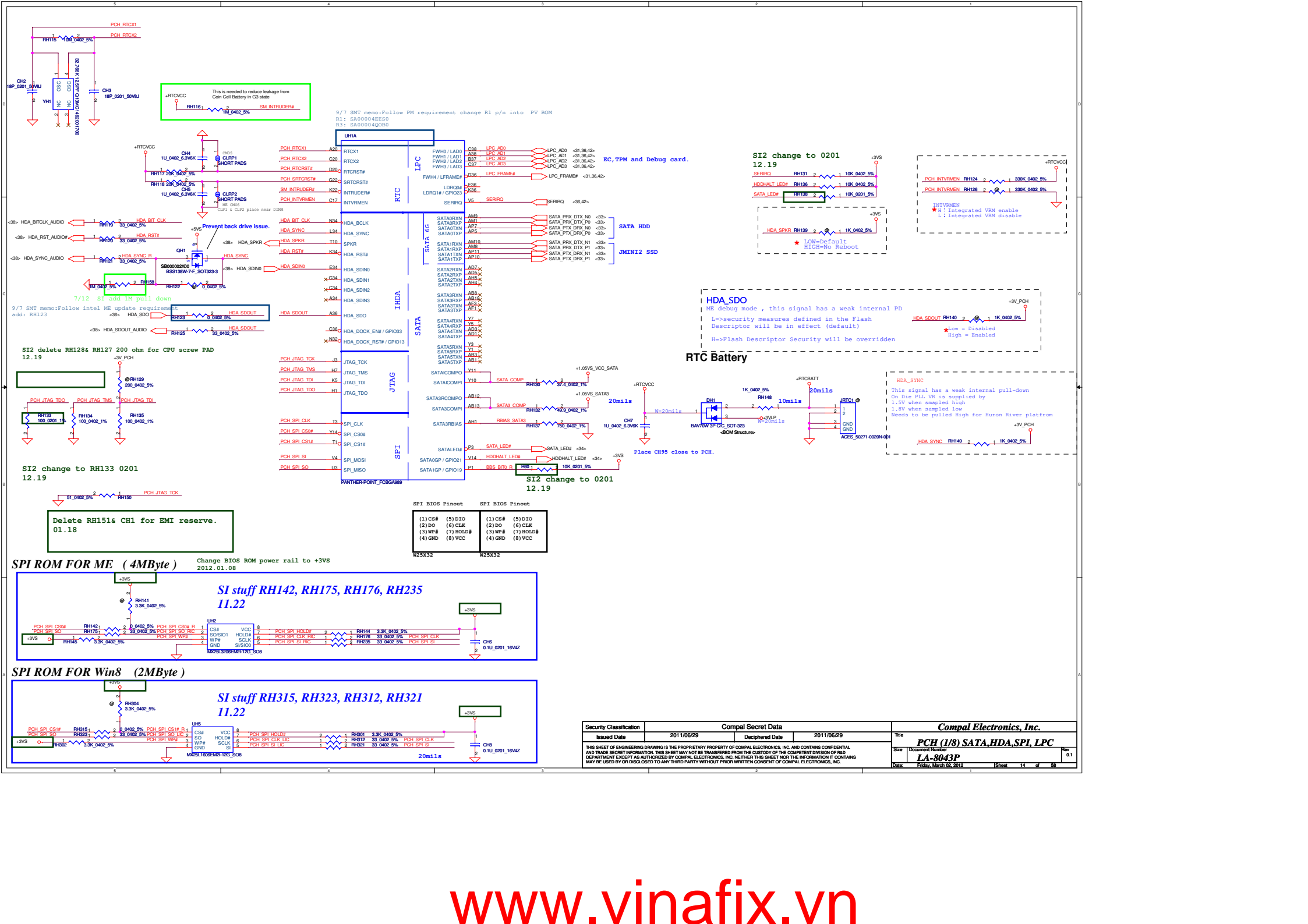


DDR3 SO-DIMM B



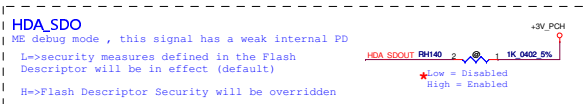
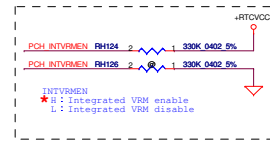
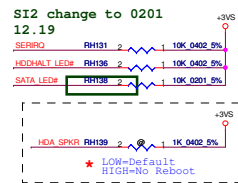
SIF 8/16 Reserve 4 pcs 0.1uF for EMI noise issue



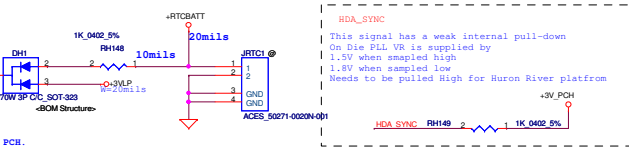


9/7 SMT memo: Follow PM requirement change R1 p/n into PV BOM
 R1: SA00048E80
 R3: SA00044Q080

EC, TPM and Debug card.

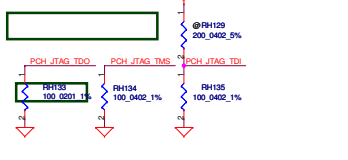


RTC Battery

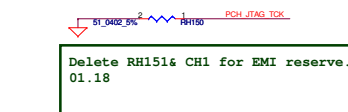


SPI BIOS Pinout	SPI BIOS Pinout
(1) CS#	(1) CS#
(2) DIO	(2) DIO
(3) WP#	(3) WP#
(4) GND	(4) GND
(5) DIO	(5) DIO
(6) CS#	(6) CS#
(7) HOLD#	(7) HOLD#
(8) VCC	(8) VCC

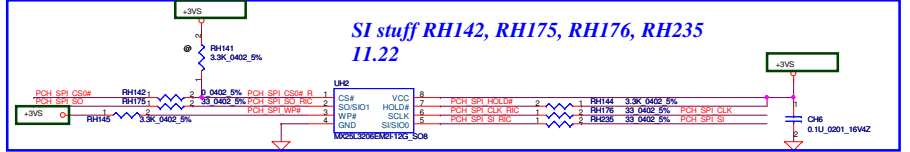
SI2 delete RH128# RH127 200 ohm for CPU screw PAD 12.19



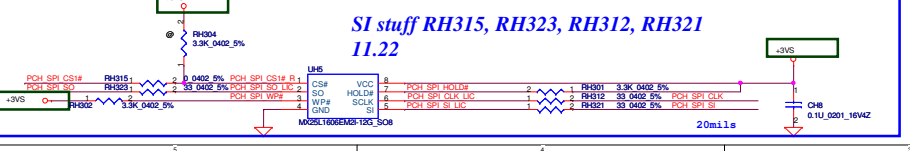
SI2 change to RH133 0201 12.19



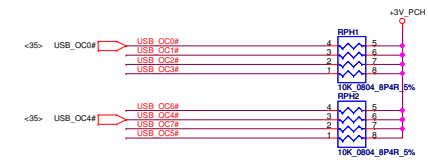
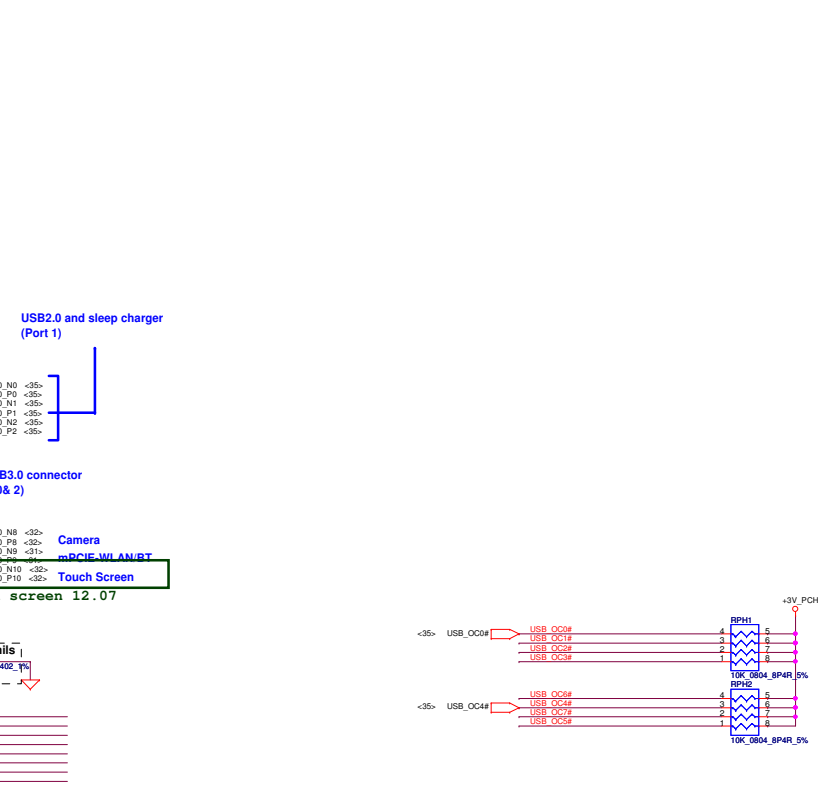
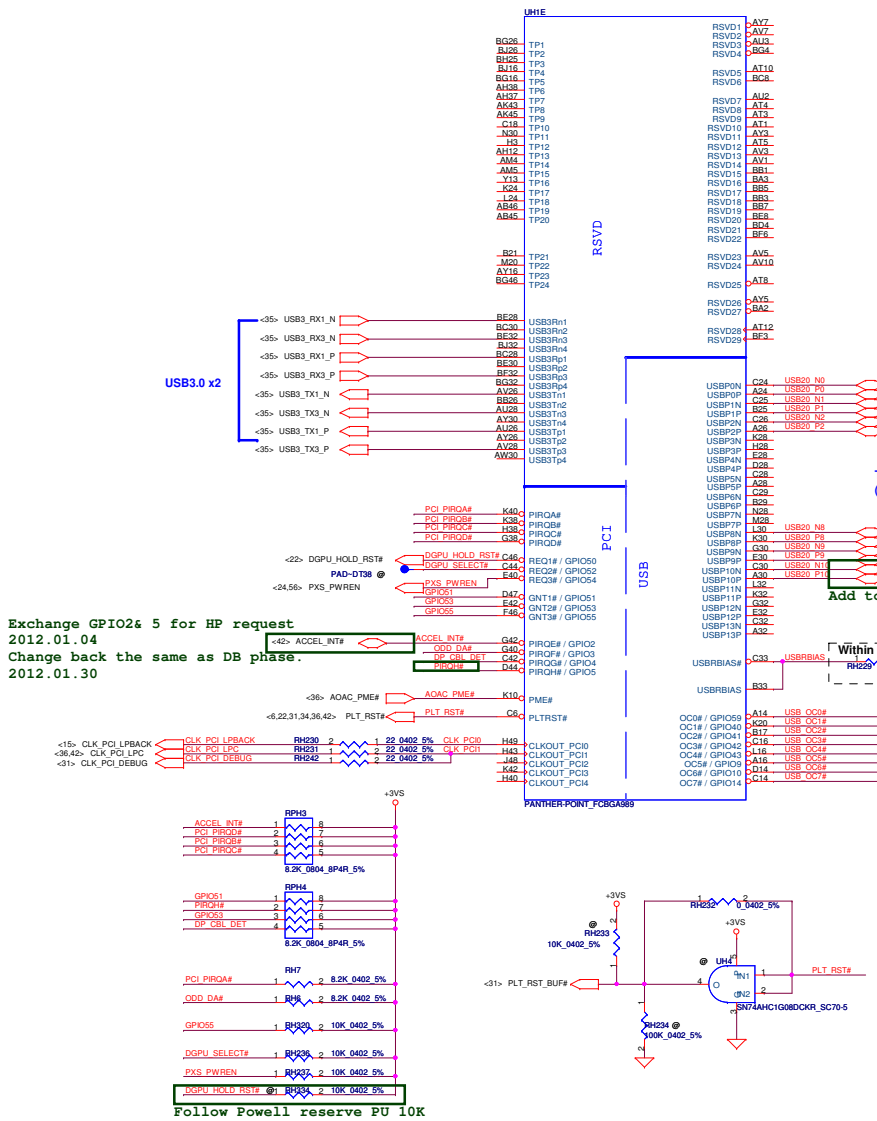
SPI ROM FOR ME (4MByte)



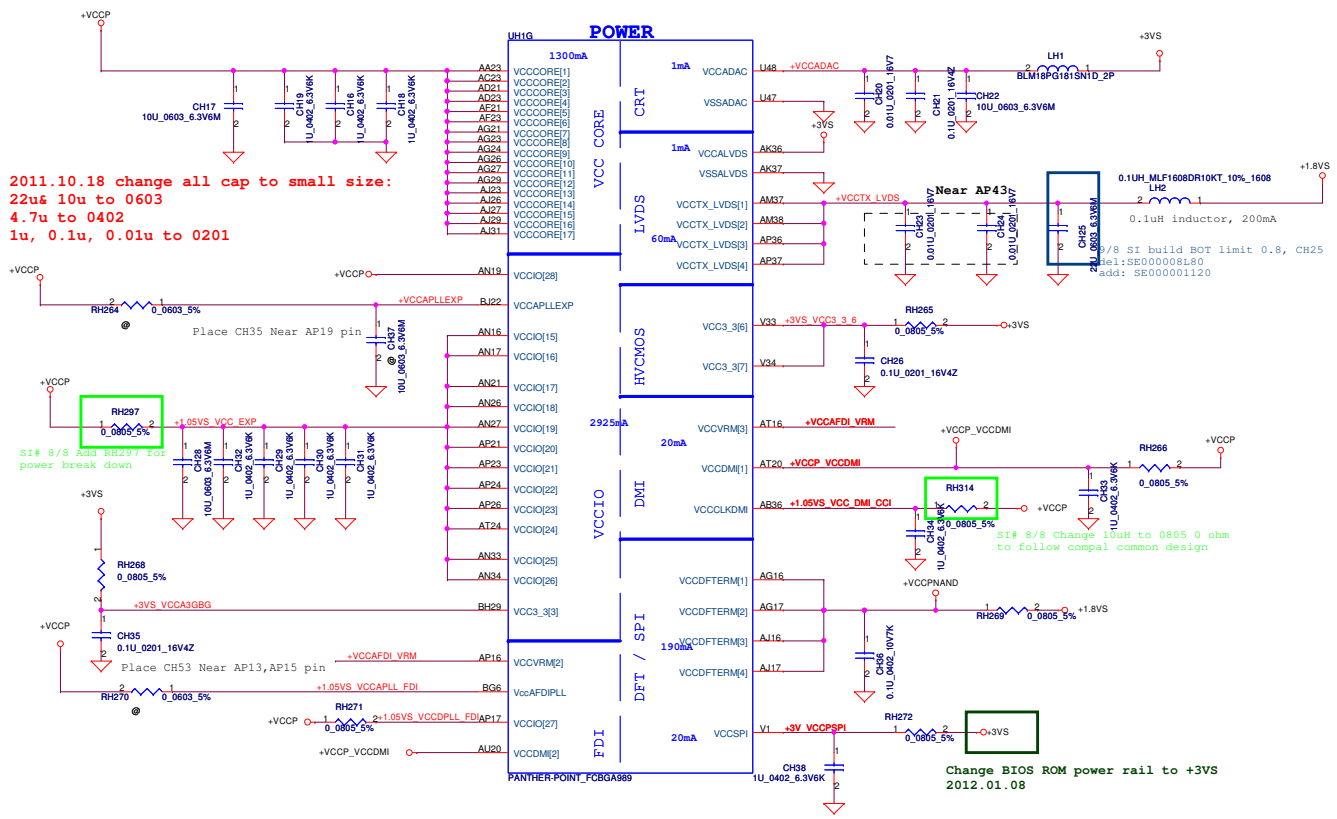
SPI ROM FOR Win8 (2MByte)



Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Compal Electronics, Inc.
				PCH (I/8) SATA, HDA, SPI, LPC
				Doc# LA-8043P
				Rev 0.1
				Date: Friday, March 02, 2012 Sheet 14 of 58



Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	PCH (4/8) PCI, USB, NVRAM	
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PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPILA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_IVDS	1.8	0.06

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Title	PCH (6/8) PWR	
Size	Document Number	Rev
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UHH		
HS	VSS	AK
VSS[0]		
AA17	VSS[80]	AK38
AA2	VSS[81]	AK4
AA3	VSS[82]	AK5
AA33	VSS[83]	AK6
AA34	VSS[84]	AL16
AB11	VSS[85]	AL17
AB14	VSS[86]	AL2
AB28	VSS[87]	AL21
AB4	VSS[88]	AL22
AB43	VSS[89]	AL23
AB5	VSS[90]	AL26
AB7	VSS[91]	AL27
AC18	VSS[92]	AL31
AC2	VSS[93]	AL34
AC21	VSS[94]	AL33
AC24	VSS[95]	AL34
AC33	VSS[96]	AL48
AC45	VSS[97]	AM11
AC4	VSS[98]	AM14
AD10	VSS[99]	AM36
AD11	VSS[100]	AM39
AD12	VSS[101]	AM43
AD13	VSS[102]	AM45
AD19	VSS[103]	AM46
AD24	VSS[104]	AM7
AD26	VSS[105]	AN2
AD27	VSS[106]	AN3
AD28	VSS[107]	AN3
AD34	VSS[108]	AN31
AD38	VSS[109]	AP12
AD37	VSS[110]	AP19
AD38	VSS[111]	AP28
AD39	VSS[112]	AP30
AD4	VSS[113]	AP32
AD40	VSS[114]	AP38
AD42	VSS[115]	AP4
AD43	VSS[116]	AP42
AD45	VSS[117]	AP46
AD46	VSS[118]	AP6
AD8	VSS[119]	AR2
AE2	VSS[120]	AR46
AE3	VSS[121]	AT11
AE3	VSS[122]	AT13
AE10	VSS[123]	AT18
AD14	VSS[124]	AT22
AD16	VSS[125]	AT26
AE16	VSS[126]	AT28
AE19	VSS[127]	AT30
AE24	VSS[128]	AT32
AE26	VSS[129]	AT34
AE27	VSS[130]	AT39
AE28	VSS[131]	AT42
AE31	VSS[132]	AT46
AE38	VSS[133]	AT7
AE4	VSS[134]	AL24
AE42	VSS[135]	AL30
AE46	VSS[136]	AV16
AE5	VSS[137]	AV20
AE7	VSS[138]	AV24
AE8	VSS[139]	AV30
AC10	VSS[140]	AV38
AC2	VSS[141]	AV4
AG31	VSS[142]	AV48
AG46	VSS[143]	AV9
AH11	VSS[144]	AW14
AH3	VSS[145]	AW18
AH38	VSS[146]	AW2
AH39	VSS[147]	AW22
AH40	VSS[148]	AW26
AH42	VSS[149]	AW28
AH46	VSS[150]	AW32
AH7	VSS[151]	AW34
A119	VSS[152]	AW36
A121	VSS[153]	AW40
A124	VSS[154]	AW48
A133	VSS[155]	AV11
A134	VSS[156]	AY12
AK12	VSS[157]	AY22
AK3	VSS[158]	AY28
	VSS[159]	

PANTHER-POINT_FCBGA989

UH1		
VSS	AK	H
VSS[159]		H46
VSS[160]		K18
VSS[161]		K26
VSS[162]		K32
VSS[163]		K46
VSS[164]		K7
VSS[165]		L18
VSS[166]		L2
VSS[167]		L20
VSS[168]		L26
VSS[169]		L28
VSS[170]		L38
VSS[171]		L48
VSS[172]		M12
VSS[173]		M18
VSS[174]		M22
VSS[175]		M24
VSS[176]		M30
VSS[177]		M32
VSS[178]		M34
VSS[179]		M38
VSS[180]		MM
VSS[181]		MM2
VSS[182]		MM4
VSS[183]		MM6
VSS[184]		M8
VSS[185]		N18
VSS[186]		P30
VSS[187]		M47
VSS[188]		P11
VSS[189]		P18
VSS[190]		P33
VSS[191]		P40
VSS[192]		P42
VSS[193]		P47
VSS[194]		P7
VSS[195]		R2
VSS[196]		R48
VSS[197]		T12
VSS[198]		T31
VSS[199]		T37
VSS[200]		T4
VSS[201]		W34
VSS[202]		L46
VSS[203]		T47
VSS[204]		T8
VSS[205]		V11
VSS[206]		V17
VSS[207]		V26
VSS[208]		V27
VSS[209]		V31
VSS[210]		V36
VSS[211]		V38
VSS[212]		V43
VSS[213]		V7
VSS[214]		W17
VSS[215]		W19
VSS[216]		W2
VSS[217]		W27
VSS[218]		W48
VSS[219]		X12
VSS[220]		X28
VSS[221]		Y4
VSS[222]		Y46
VSS[223]		Y6
VSS[224]		Y8
VSS[225]		BC29
VSS[226]		N24
VSS[227]		AJ3
VSS[228]		AD47
VSS[229]		B43
VSS[230]		BE10
VSS[231]		BC41
VSS[232]		G14
VSS[233]		H16
VSS[234]		I36
VSS[235]		BC22
VSS[236]		BC24
VSS[237]		C22
VSS[238]		AP13
VSS[239]		M14
VSS[240]		AP3
VSS[241]		AP1
VSS[242]		BE16
VSS[243]		BC16
VSS[244]		BC28
VSS[245]		BU29
VSS[246]		
VSS[247]		
VSS[248]		
VSS[249]		
VSS[250]		
VSS[251]		
VSS[252]		
VSS[253]		
VSS[254]		
VSS[255]		
VSS[256]		
VSS[257]		
VSS[258]		

PANTHER-POINT_FCBGA989

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Size	C	Rev	0.1	Sheet 22 of 58

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Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title
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Size	C	Rev	0.1	
Date	Friday, March 02, 2012		Sheet	26 of 58

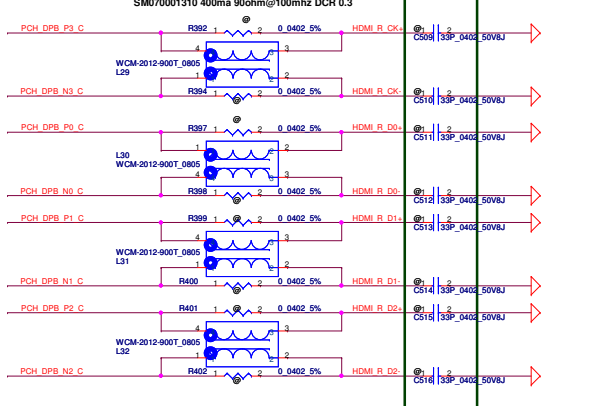
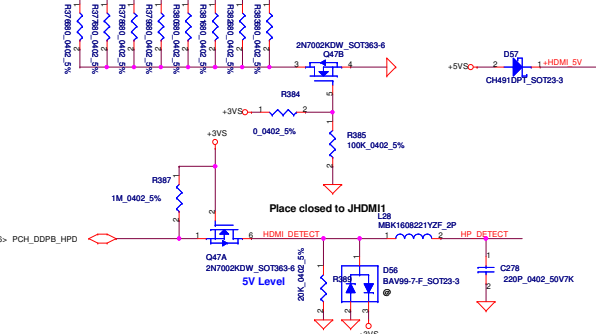
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Size	C	Date	Friday, March 02, 2012	<small>Rev</small> 0.1 <small>Sheet 28 of 58</small>

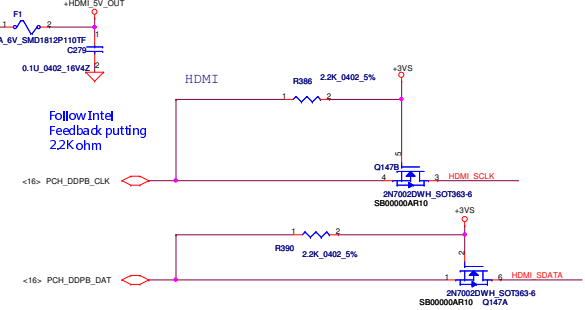
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Size	C	Date	Friday, March 02, 2012	<small>Rev</small> 0.1 <small>Sheet 29 of 58</small>

PCH_DPB_P3_C	0.1U 0402 16V7K	1	2	C270	PCH_DPB_P3	<16>
PCH_DPB_N3_C	0.1U 0402 16V7K	1	2	C271	PCH_DPB_N3	<16>
PCH_DPB_P2_C	0.1U 0402 16V7K	1	2	C272	PCH_DPB_P2	<16>
PCH_DPB_N2_C	0.1U 0402 16V7K	1	2	C273	PCH_DPB_N2	<16>
PCH_DPB_P1_C	0.1U 0402 16V7K	1	2	C274	PCH_DPB_P1	<16>
PCH_DPB_N1_C	0.1U 0402 16V7K	1	2	C275	PCH_DPB_N1	<16>
PCH_DPB_P0_C	0.1U 0402 16V7K	1	2	C276	PCH_DPB_P0	<16>
PCH_DPB_N0_C	0.1U 0402 16V7K	1	2	C277	PCH_DPB_N0	<16>

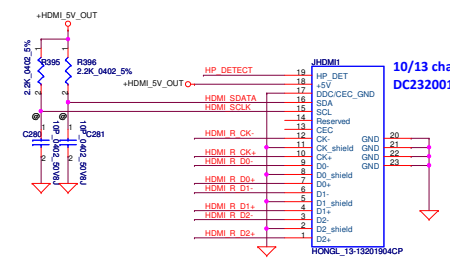


Follow EMI request add 33pF cap to GND.
11.02

Del HDMI Repeater PS8271



5V PULL UP IN CONNECTER SIDE

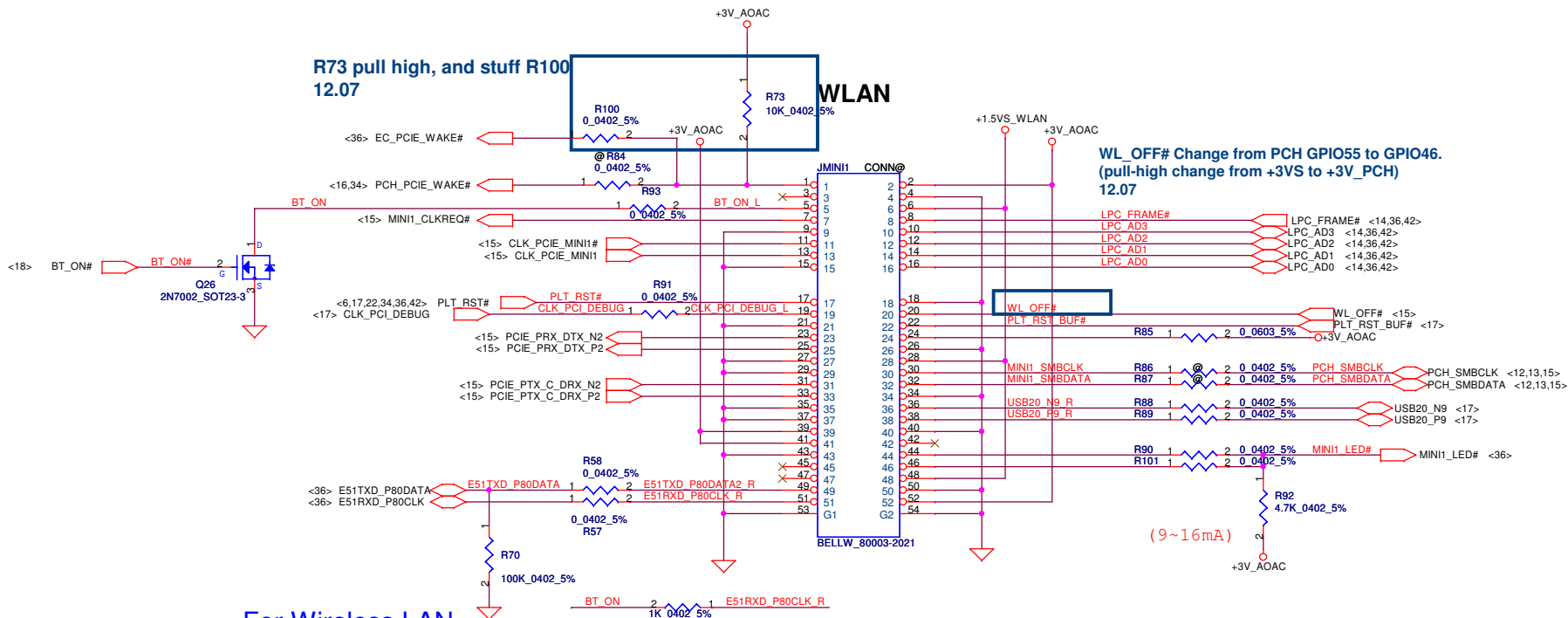


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				IA-8042P
				Rev 0.1
				Date: Friday, March 02, 2012 Sheet 30 of 58

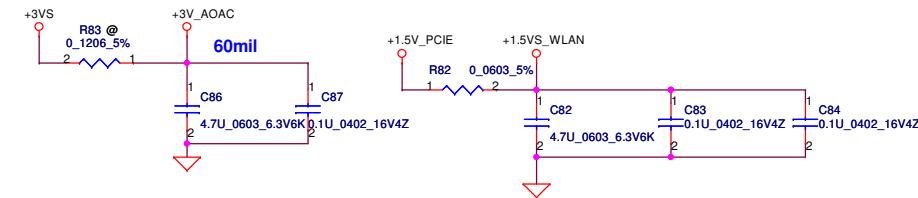
R73 pull high, and stuff R100
12.07

WLAN

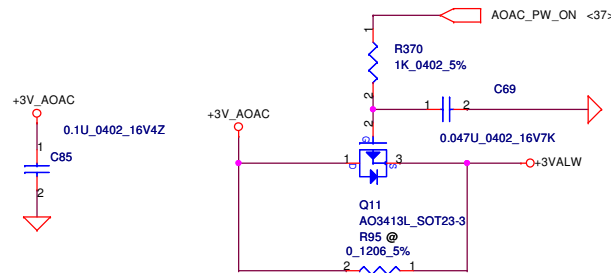
WL_OFF# Change from PCH GPIO55 to GPIO46.
(pull-high change from +3VS to +3V_PCH)
12.07



For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



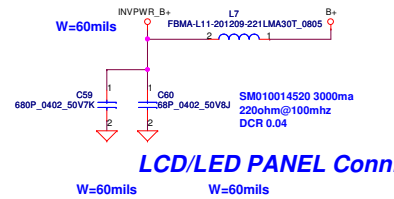
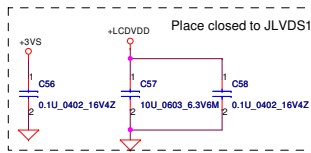
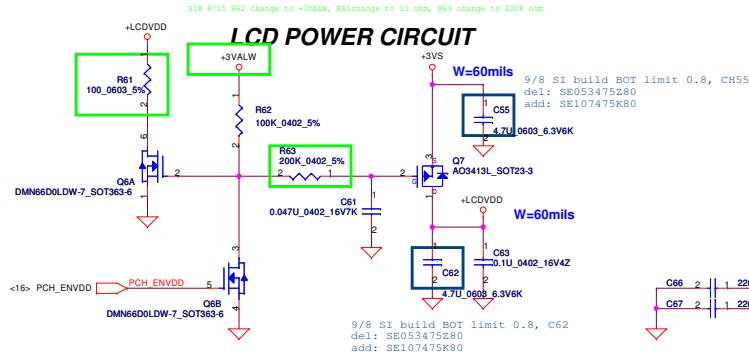
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	MiniCard & WLAN
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				Date	Friday, March 02, 2012
				Sheet	31 of 58
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				LA-8042P	

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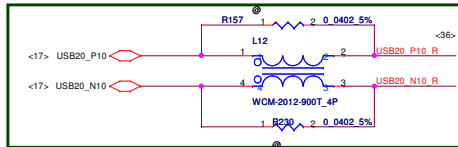
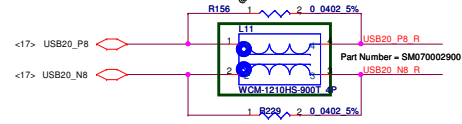
www.vinafix.vn

LCD POWER CIRCUIT

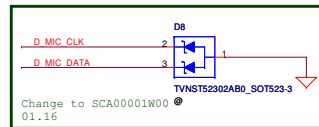


Delete INVT_PWM because EC pin 25 need to connect to BATT_TEMP

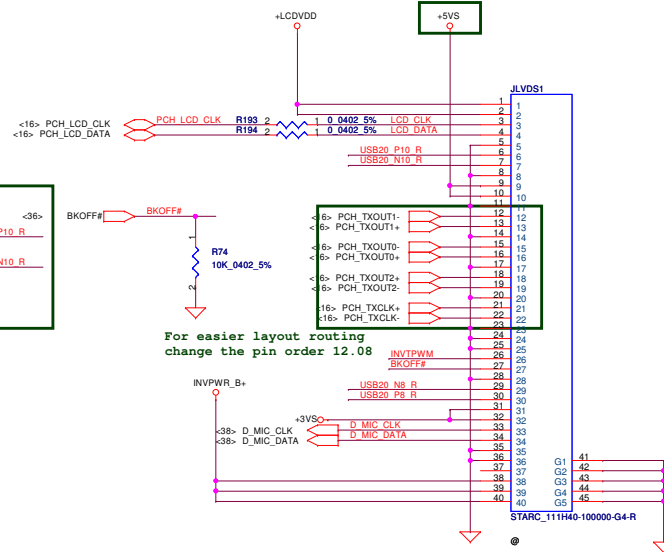
Change to smaller package 01.16



Port 10 for touch screen 12.07



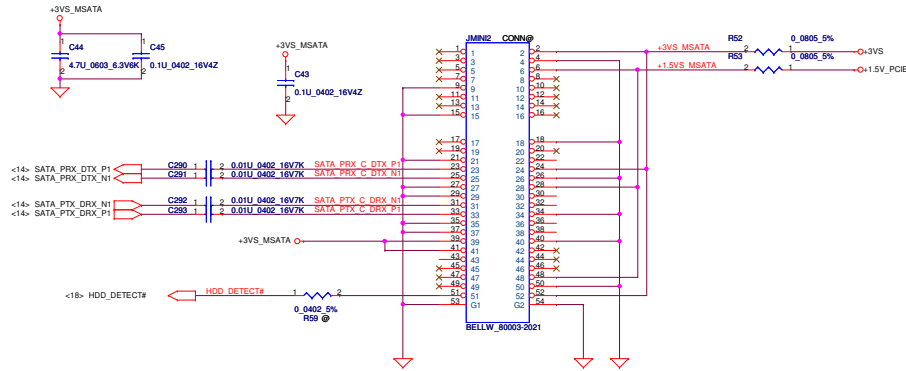
+3VS& +5VS for touch screen (choose one when getting spec) 12.09



For easier layout routing change the pin order 12.08

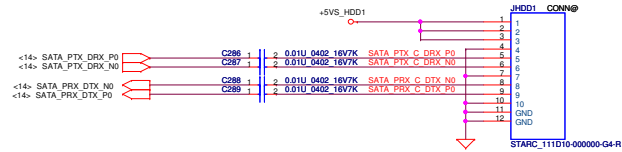
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Compal Electronics, Inc.
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Date: Friday, March 02, 2012				Rev 0.1
Sheet 32 of 58				

mSATA Conn.

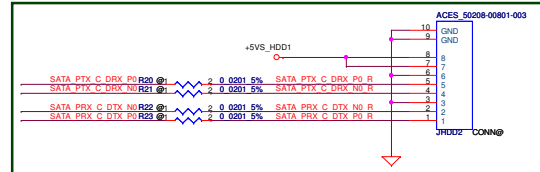
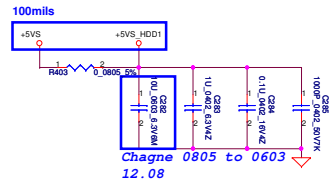


Exchange port 0 & port 1 for SI as customer request
11.30

Change footprint to Starconn (PAD is bigger)
11.30

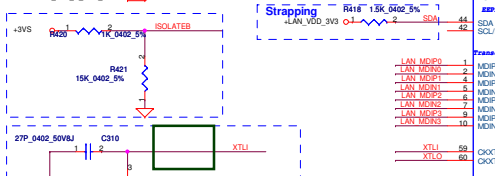
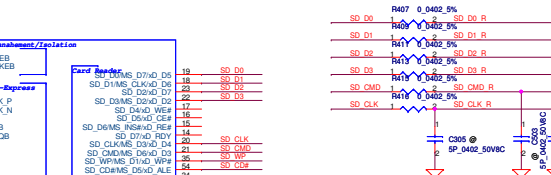
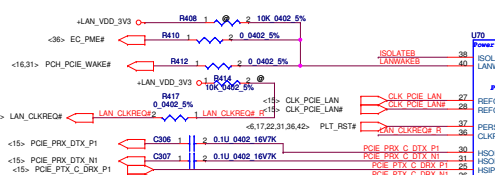
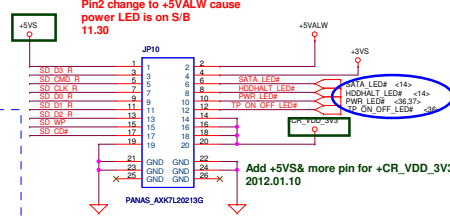
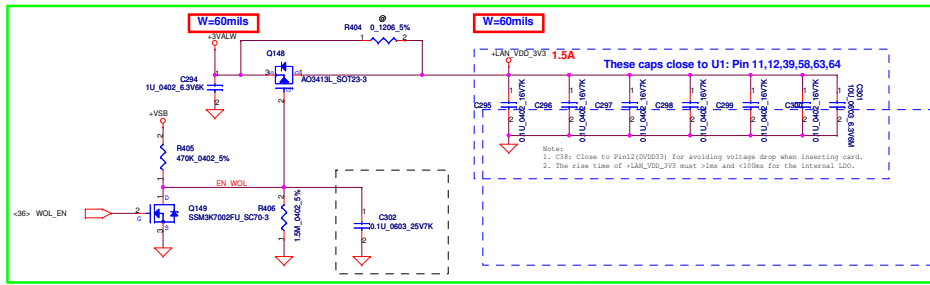


SATA connector



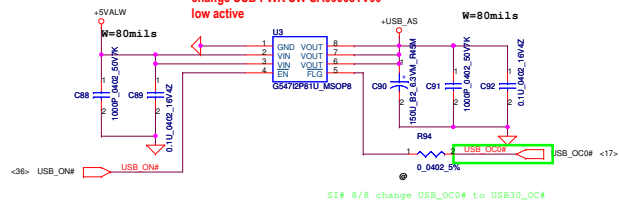
Co-layout for wire type connector
01.16
Change connector to ACES_50376
01.31
Change connector to ACES_50208 because current limit issue
02.06

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Size	Document Number		Rev	0.1
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			Sheet	33 of 58

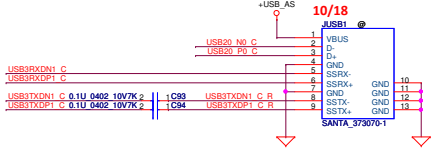


USB3.0

USB3.0 need support 2.5A
change USB_PWR SW SA00003TV00
low active

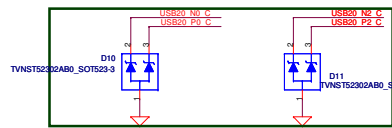


Change conn to SANTA-373070
10/18

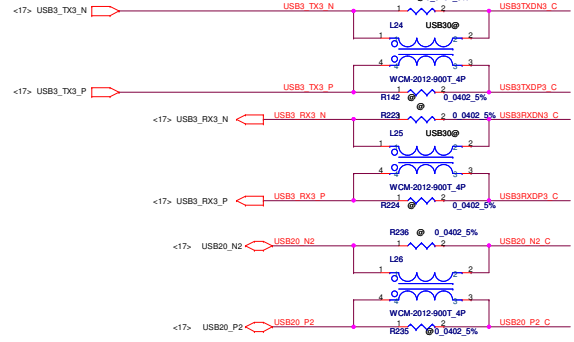
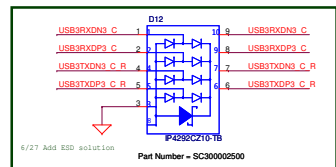
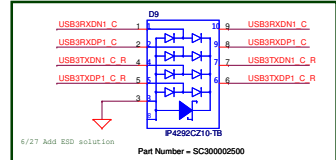
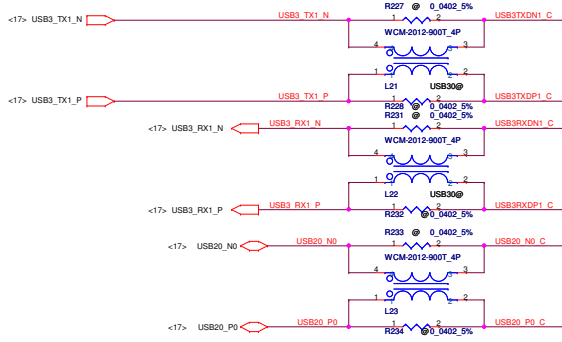
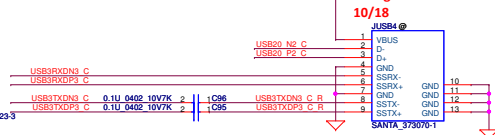


Change P/N from SCA0000T00 to SCA00001L00

11.01
Change P/N to SCA00001W00 for smaller size, 10*10 choke

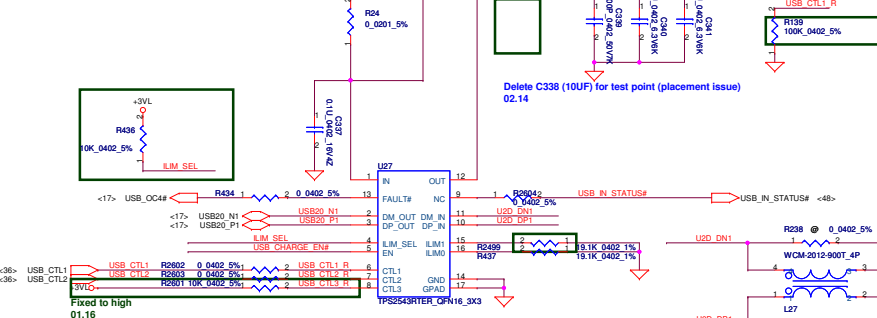


Change conn to SANTA-373070
10/18

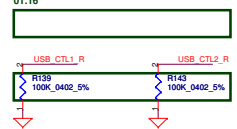


USB2.0 & charger

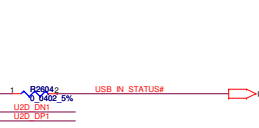
USB charger footprint need change to TPS2543
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)



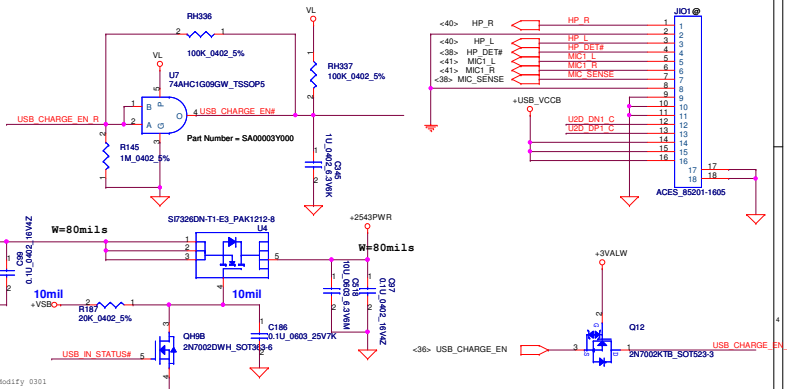
Delete pull-high resistors
01.16



Delete C338 (10uF) for test point (placement issue)
02.14

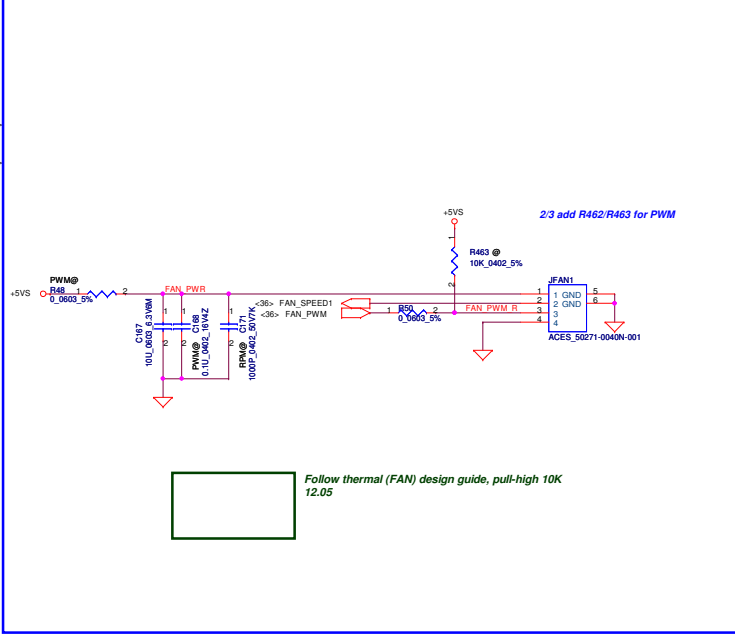
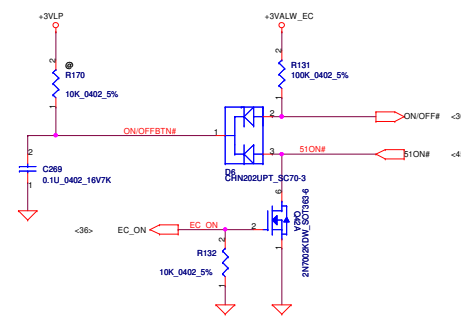


Follow EMI request add choke
11.08

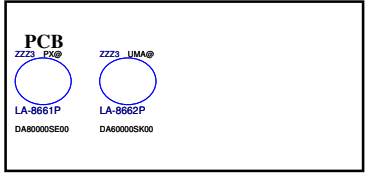
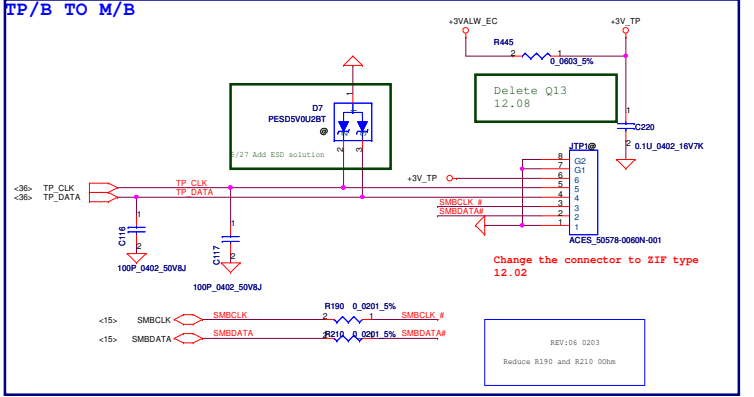
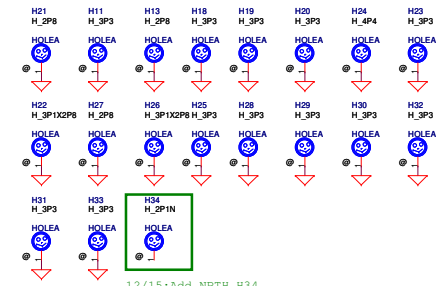
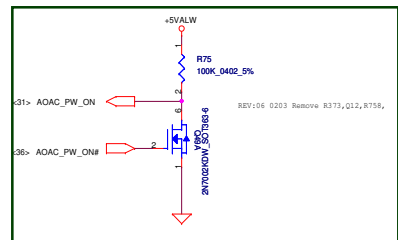
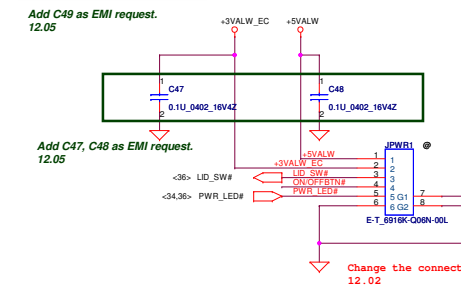
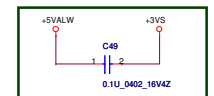
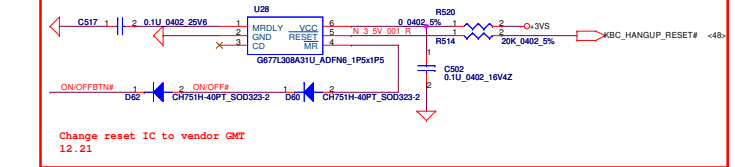
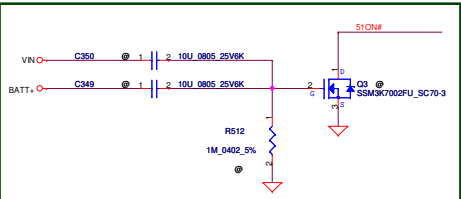
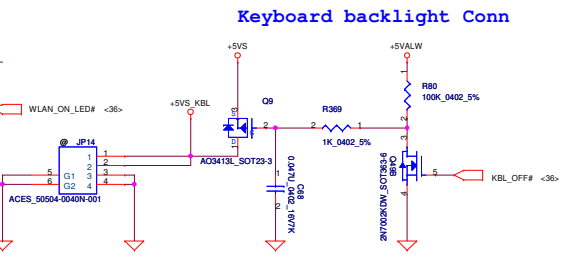
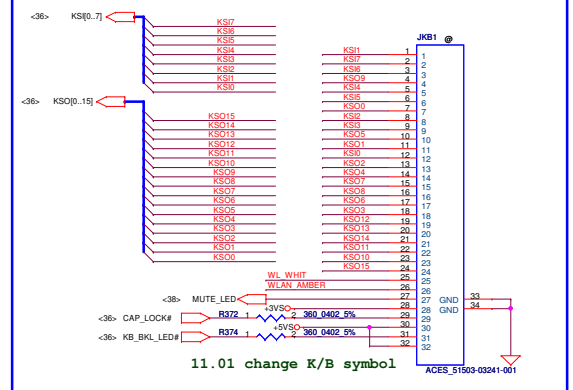
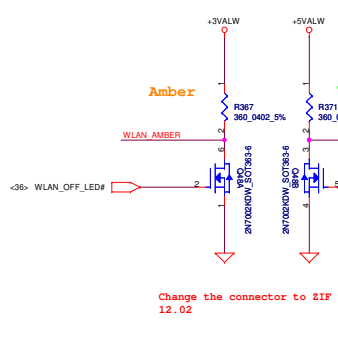


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C	C		USB Con & Daughter Con	
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PWM Fan Control circuit



KSD15	C228	1	2	100P_0402_50VBJ
KSD14	C227	1	2	100P_0402_50VBJ
KSD13	C226	1	2	100P_0402_50VBJ
KSD12	C228	1	2	100P_0402_50VBJ
KSD11	C231	1	2	100P_0402_50VBJ
KSD10	C230	1	2	100P_0402_50VBJ
KSD9	C233	1	2	100P_0402_50VBJ
KSD8	C232	1	2	100P_0402_50VBJ
KSD7	C235	1	2	100P_0402_50VBJ
KSD6	C234	1	2	100P_0402_50VBJ
KSD5	C237	1	2	100P_0402_50VBJ
KSD4	C236	1	2	100P_0402_50VBJ
KSD3	C240	1	2	100P_0402_50VBJ
KSD2	C238	1	2	100P_0402_50VBJ
KSD1	C241	1	2	100P_0402_50VBJ
KSD0	C239	1	2	100P_0402_50VBJ
KSD7	C243	1	2	100P_0402_50VBJ
KSD6	C242	1	2	100P_0402_50VBJ
KSD5	C245	1	2	100P_0402_50VBJ
KSD4	C244	1	2	100P_0402_50VBJ
KSD3	C248	1	2	100P_0402_50VBJ
KSD2	C246	1	2	100P_0402_50VBJ
KSD1	C249	1	2	100P_0402_50VBJ
KSD0	C250	1	2	100P_0402_50VBJ

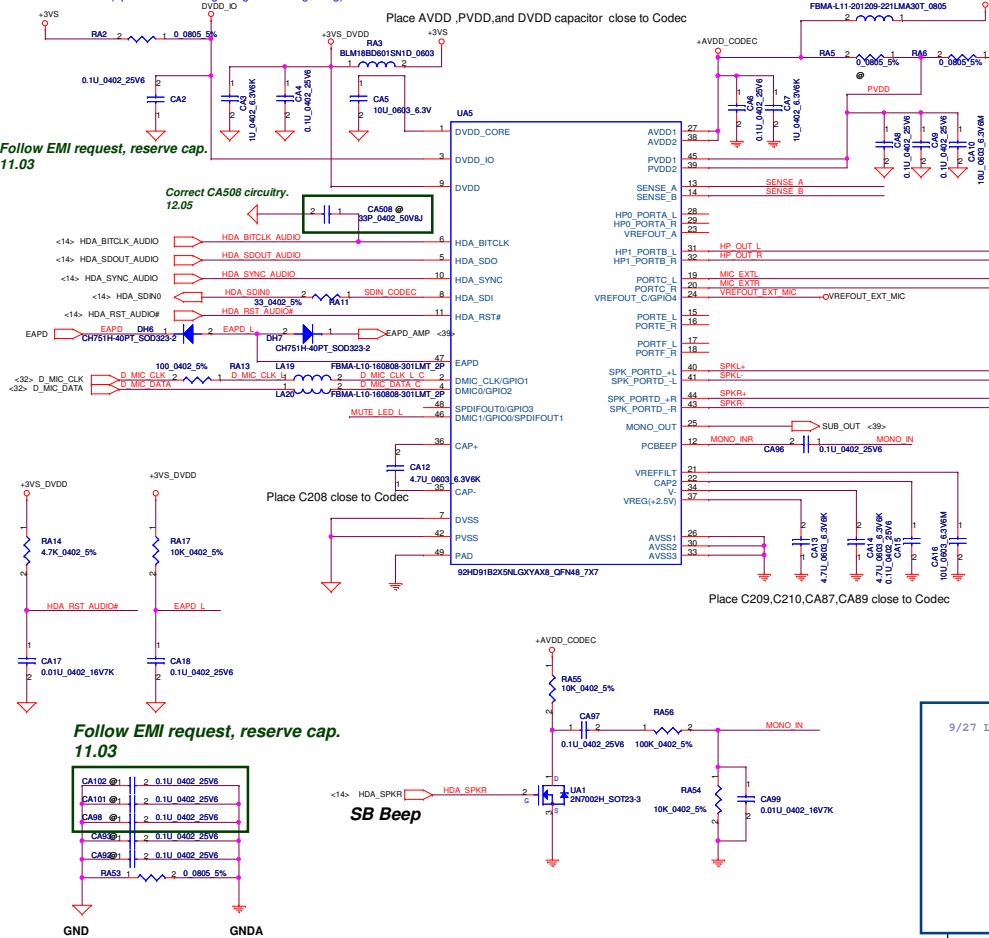


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				KB/TP/LED/FAN/Screw/Gsensor	
				Size	Document Number
				LA-8041P	
				Date	Sheet
				Saturday, March 03, 2012	37 of 88

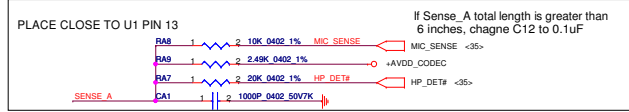
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DVDD_IO should match with HDA Bus level (optional for 3.3V signaling or 1.5V signaling)

Follow EMI request, reserve cap. 11.03

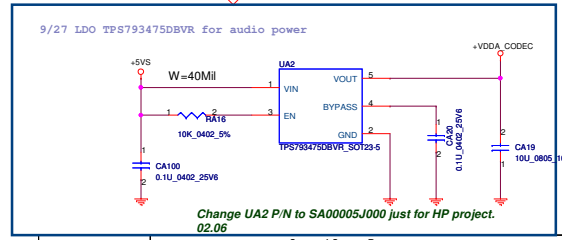


Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals.

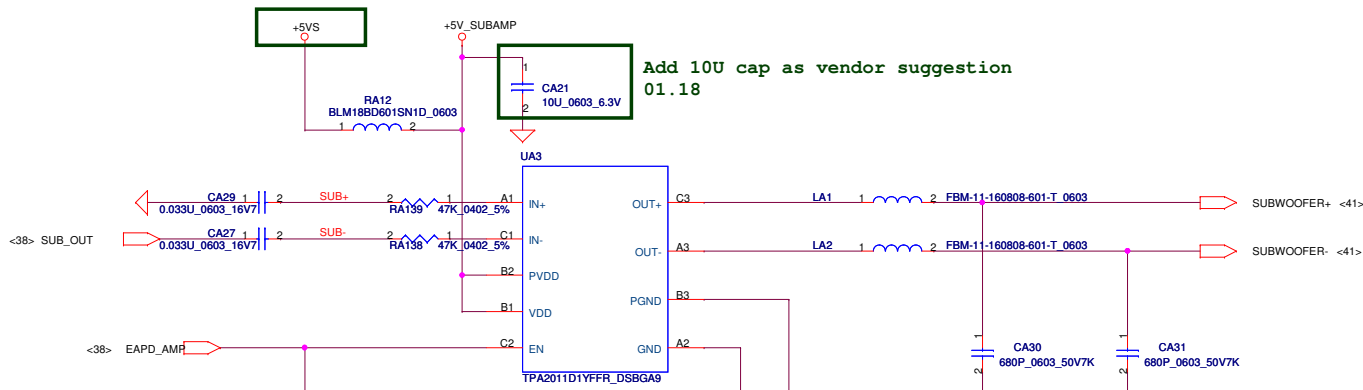


HP Jack
Ext MIC

Internal SPKR (front stereo speaker)

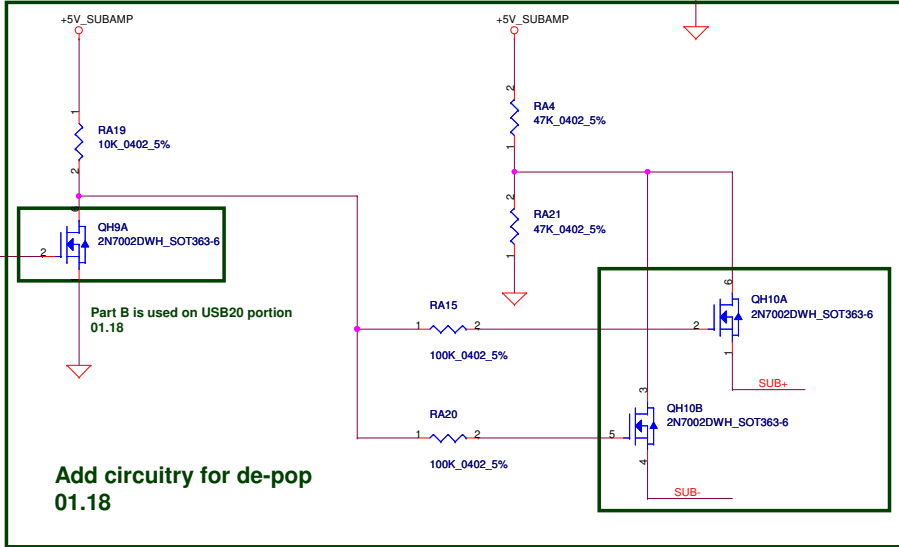


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Add 10U cap as vendor suggestion
01.18

2011.10.28 Change Sub-woofer Amp to TPA2011D1
2011.12.19 Change P/N from SA00004Z700 to SA00005FR00 for HP.



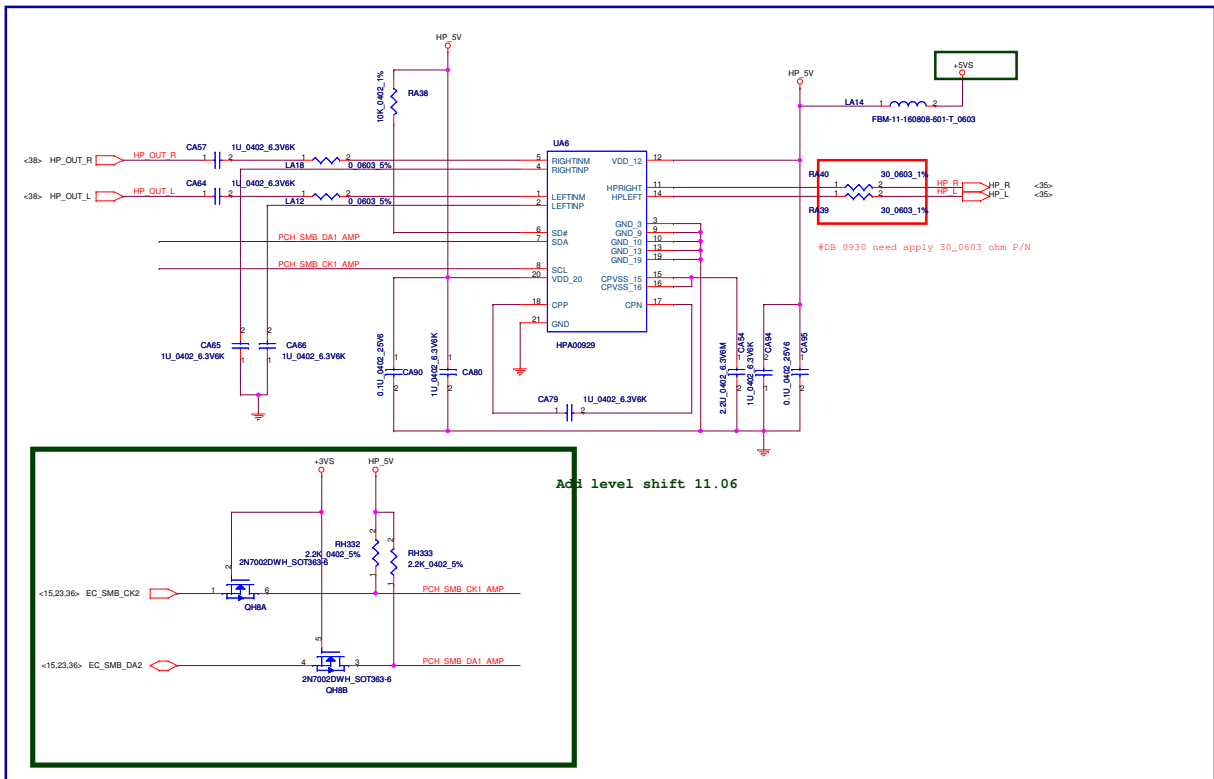
Part B is used on USB20 portion
01.18

Add circuitry for de-pop
01.18

QH10 must change to BJT before SMT
(Footprint is compatible from BJT & MOTFET)
01.18
BJT P/N: SB00000VH00

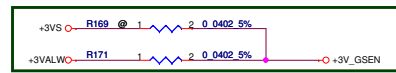
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Title	Audio Woofer Amplifier			
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Headphone amplifier

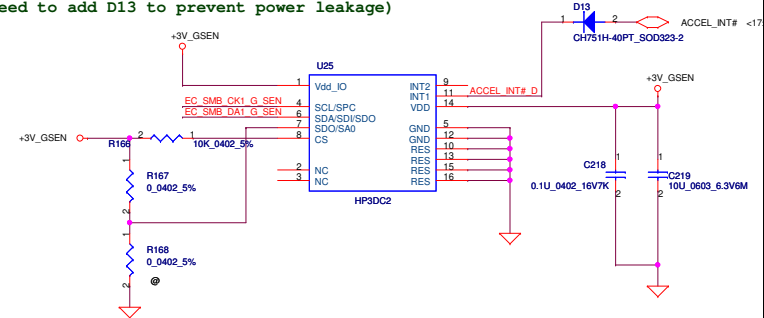


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Title	Audio SPK/HP Amplifier		Size	Document Number
Doc.	Wednesday, March 07, 2012	Sheet	40 of 58	Rev 0.1

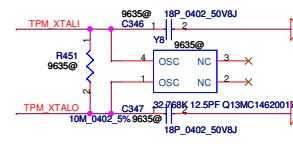
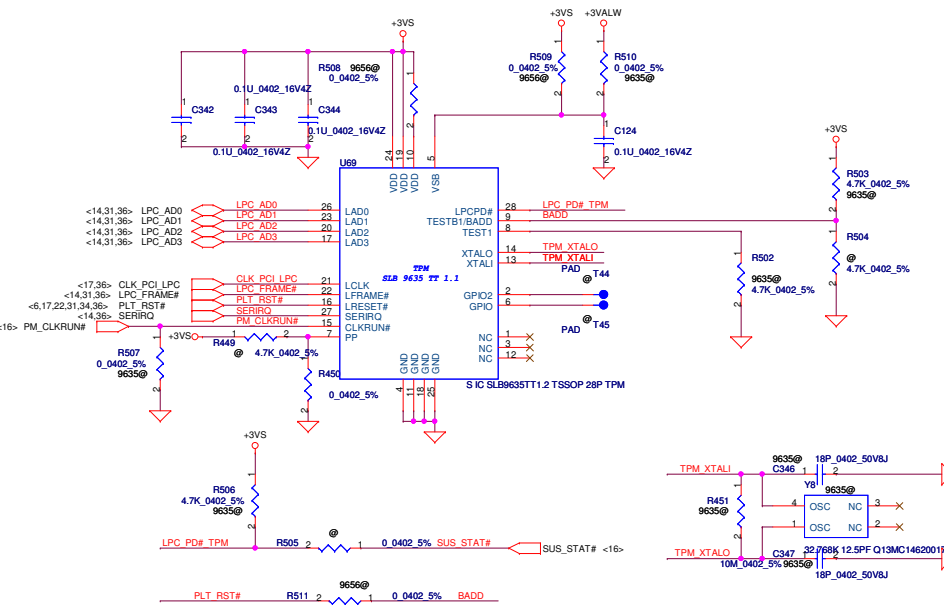
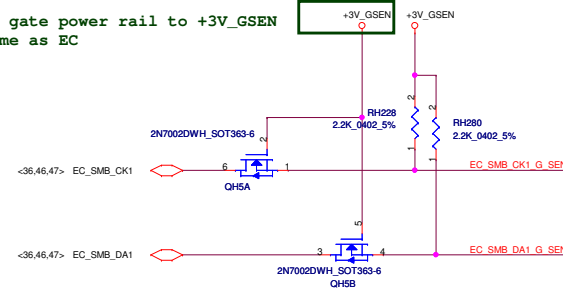
G-sensor Address: 0x50/0x52
11.01



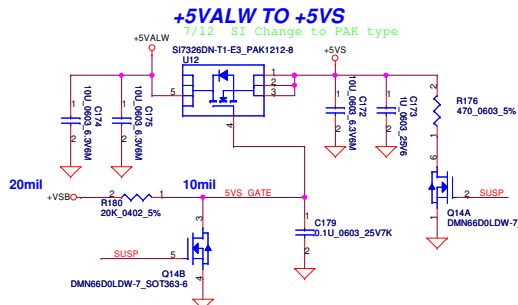
G-sensor Power Rail Change to +3VALW
(Note: Need to add D13 to prevent power leakage)
01.05



Change gate power rail to +3V_GSEN
The same as EC
01.19

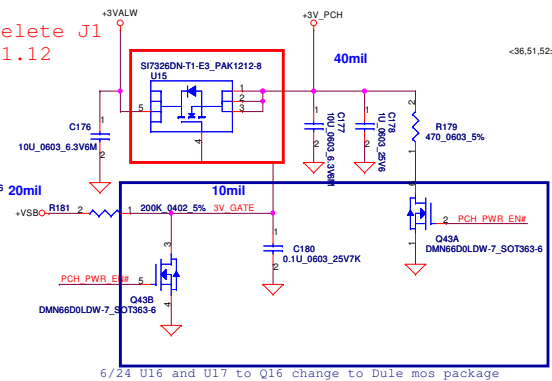


Security Classification	Compal Secret Data		Title	
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Size	Document Number	Rev	0.1	
	LA3262P_DIS_M64			
Date:	Wednesday, March 07, 2012	Sheet	42	of 58



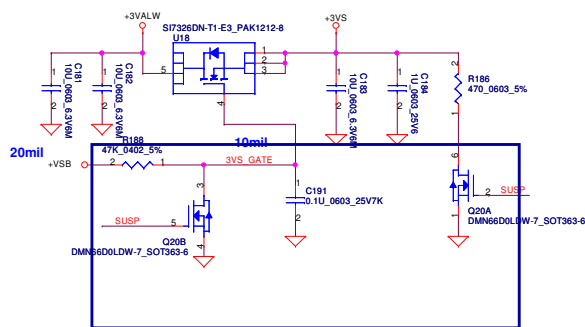
10.21 Change to PAK type
 +3VALW TO +3VALW(PCH AUX Power)
 Short J1 for PCH VCCSUS3.3

Delete J1
 01.12

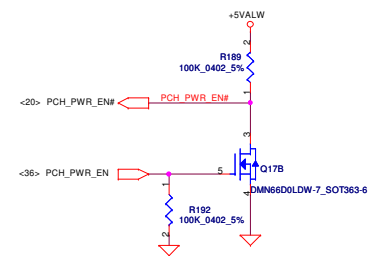
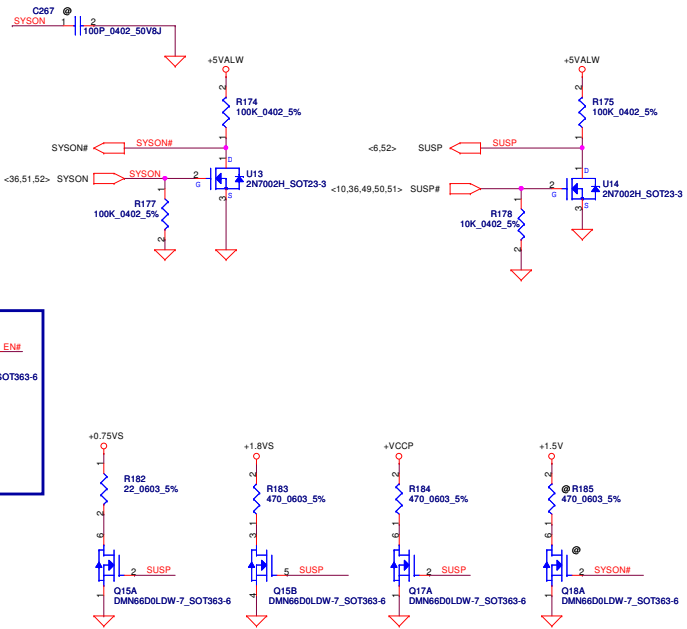


6/24 U16 and U17 to Q16 change to Dule mos package

+3VALW TO +3VS



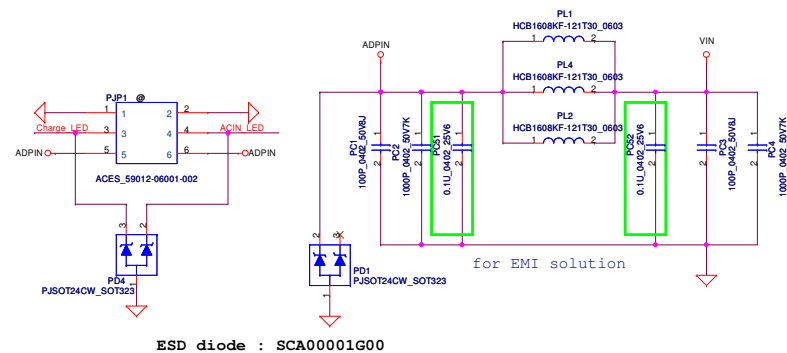
6/24 Q20 and Q21 to Q20 change to Dule mos package



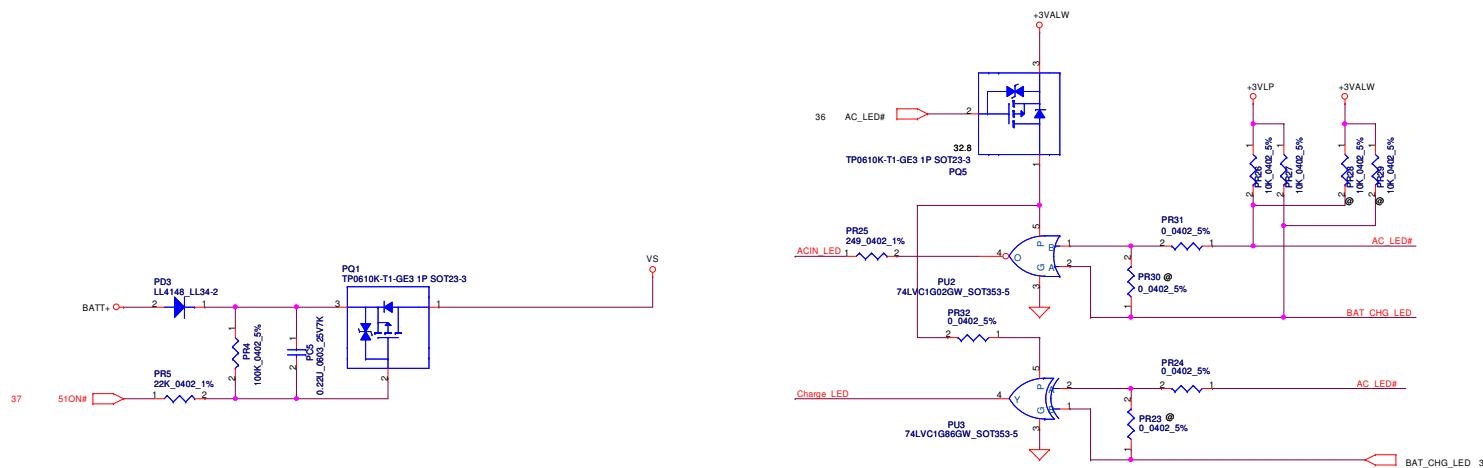
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	DC Interface
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Size	Document Number	Rev			
Custom	LA-8661P	0.1			
Date:	Friday, March 02, 2012	Sheet	43	of	58

QAZ60 Strap pin Table		@:un_install	
Netname	setting	BOM config	
CPU	CFG2	1	RC40 @ 1: Normal Operation; Lane # definition matchesocket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @ 1 : Disabled; No Physical Display Portattached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @ 1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @ H : Integrated VRM enable L : Integrated VRM disable
	HDA_SPKR	L	RH139 @ H:No Reboot L:Default
	HDA_SYNC	H	RH149 This signal has a weak internal pull-downOn Die PLL VR is supplied by H:1.5V when smaped high L:1.8V when sampled low Needs to be pulled High for Huron River platfrom
	HDA_SDOOUT	L	RH140 @ ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @ On Die DSW VR Enable H : Enable L : Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @ On-Die PLL Voltage Regulator This signal has a weak internal pull up H : On-Die voltage regulator enable L : On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246 FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
GPIO27	H	RH250 @ PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable	

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				Document Number	LA-8041P
Date:	Friday, March 02, 2012	Sheet	44	of 58	



KBC output		Input to Battery		
AC_LED#	BAT_CHG_LED	ACIN_LED	Charge_LED	LED Status
0	0	1	0	White LED light
0	1	0	1	Amber LED light
1	0	0	0	X (don't care)
1	1	0	0	X (don't care)

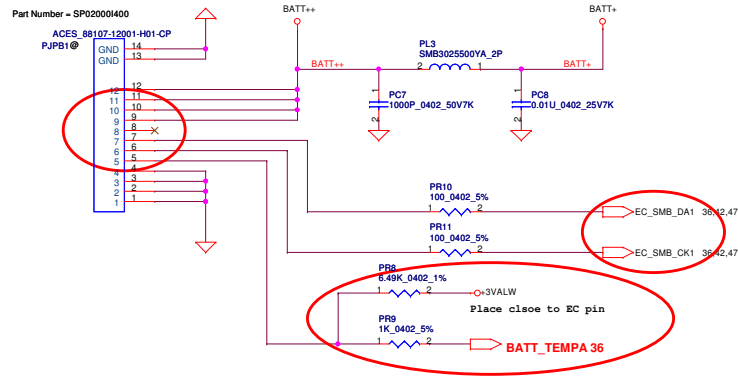


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Issued Date	2011/10/03	Deciphered Date
		2014/12/31

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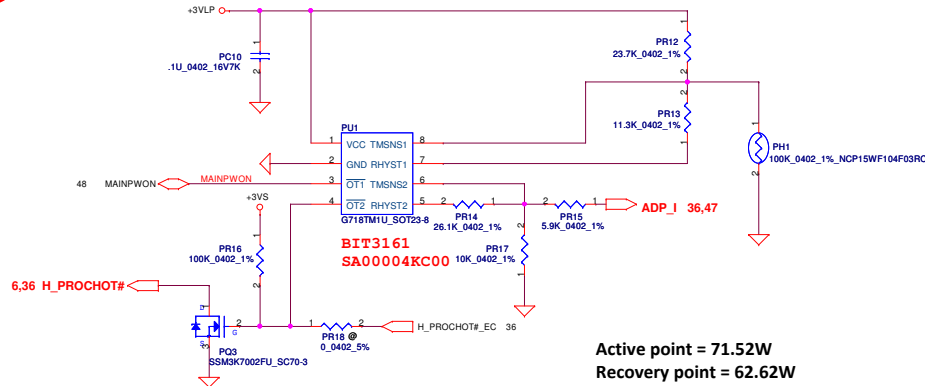
Compal Electronics, Inc.	
Title	PWR- DCIN / Vin Detector
Size	Document Number
Custom	LA-8551P
Date:	Saturday, March 03, 2012
Sheet	45 of 59
Rev	0.1

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

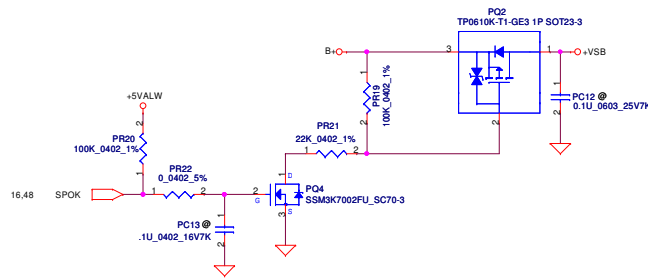


PH1 under CPU bottom side :
CPU thermal protection at 90 +3 degree C
Recovery at 56 +3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset * Rtml) / (3 * Rtml - Rset)
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



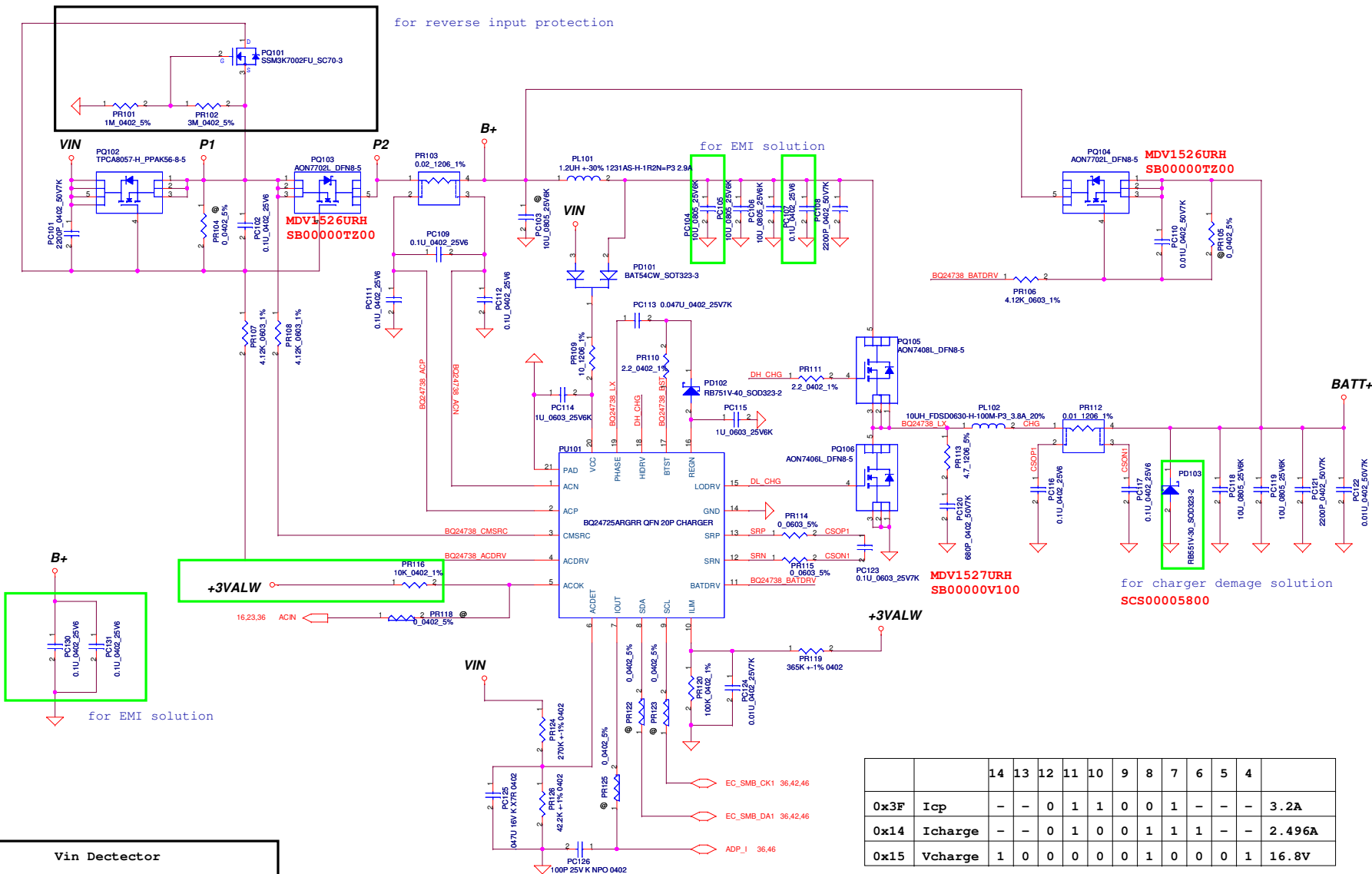
Active point = 71.52W
Recovery point = 62.62W



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Compal Electronics, Inc.	
Title	PWR- BATTERY CONN
Size	Document Number
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Date	Saturday, March 03, 2012
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for reverse input protection



Vin Detector

	Min.	Typ.	Max.
L-->H	17.45V	17.92V	18.42V
H-->L	16.89V	17.52V	18.16V

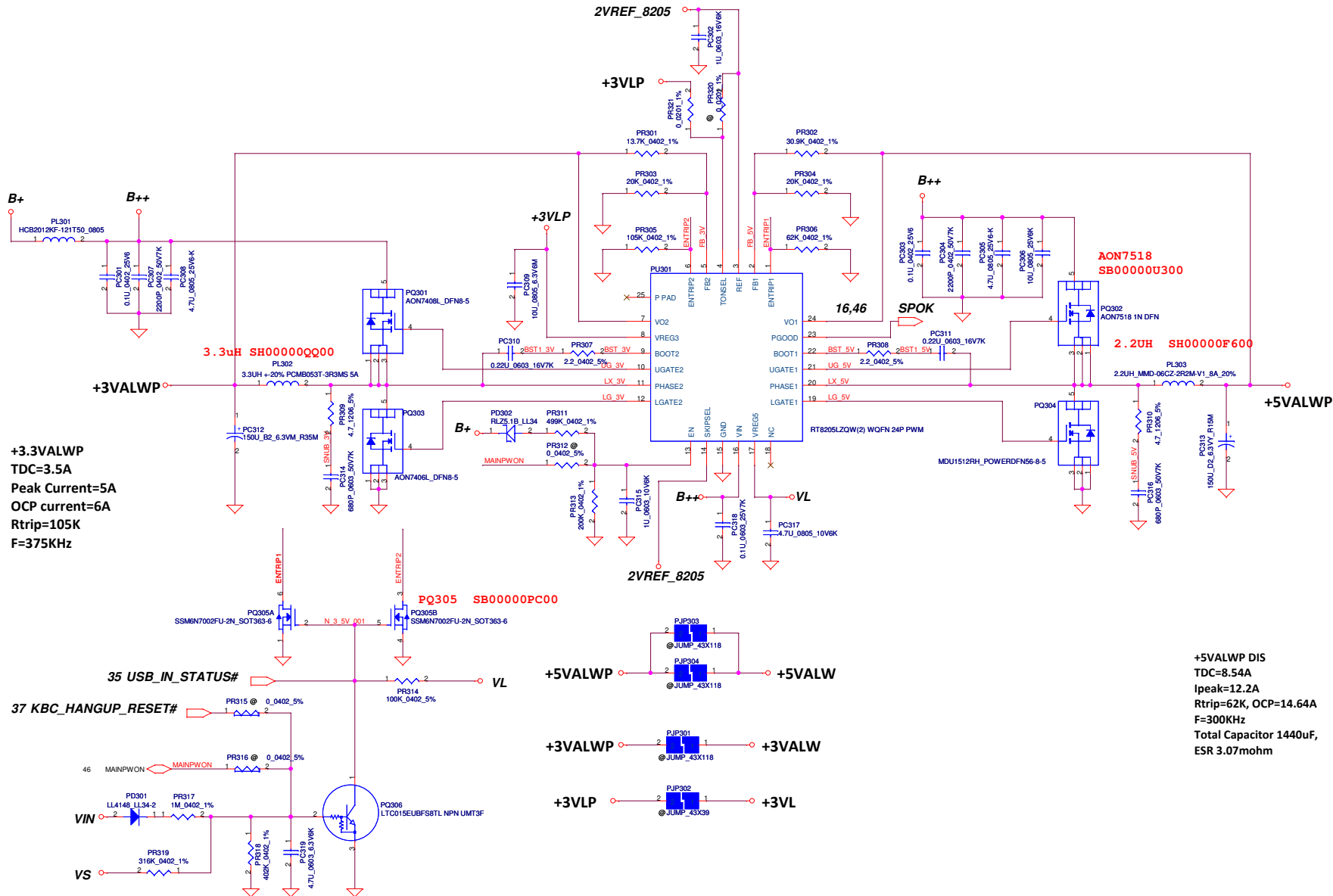
ILIM and external DPM
3.54A

		14	13	12	11	10	9	8	7	6	5	4	
0x3F	Icp	-	-	0	1	1	0	0	1	-	-	-	3.2A
0x14	Icharge	-	-	0	1	0	0	1	1	1	-	-	2.496A
0x15	Vcharge	1	0	0	0	0	0	1	0	0	0	1	16.8V

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Size	Document Number	Rev		
	LA-8551P	0.1		
Date	Saturday, March 03, 2012	Sheet	47	of 59

Compal Electronics, Inc.

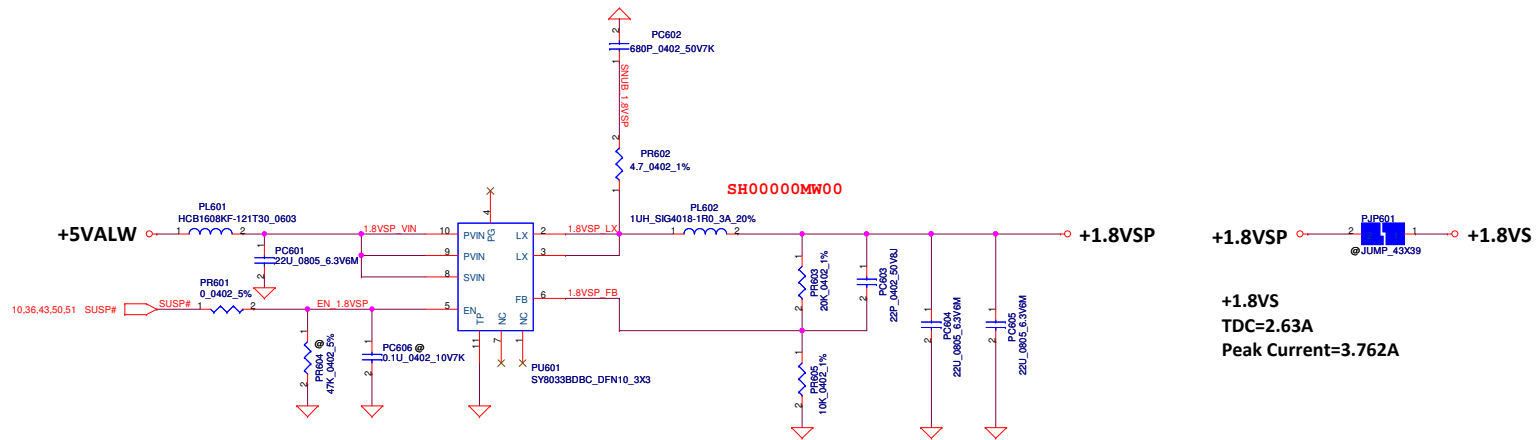
PWR-CHARGER



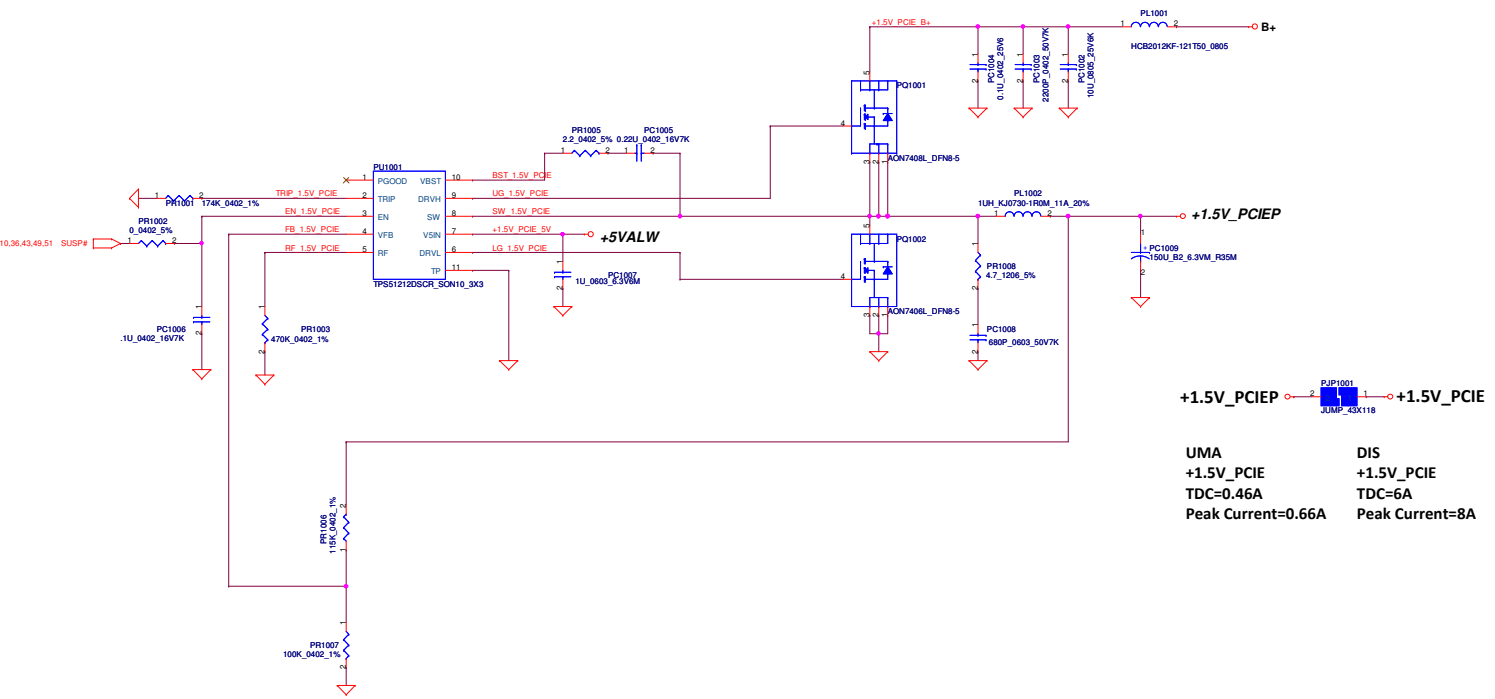
+3.3VALWP
TDC=3.5A
Peak Current=5A
OCP current=6A
Rtrip=105K
F=375KHz


+5VALWP DIS
TDC=8.5A
I_{peak}=12.2A
Rtrip=62K, OCP=14.64A
F=300KHz
Total Capacitor 1440uF,
ESR 3.07mohm

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			Document Number LA-8551P
			Rev 0.1
			Date: Saturday, March 03, 2012 Sheet 48 of 59

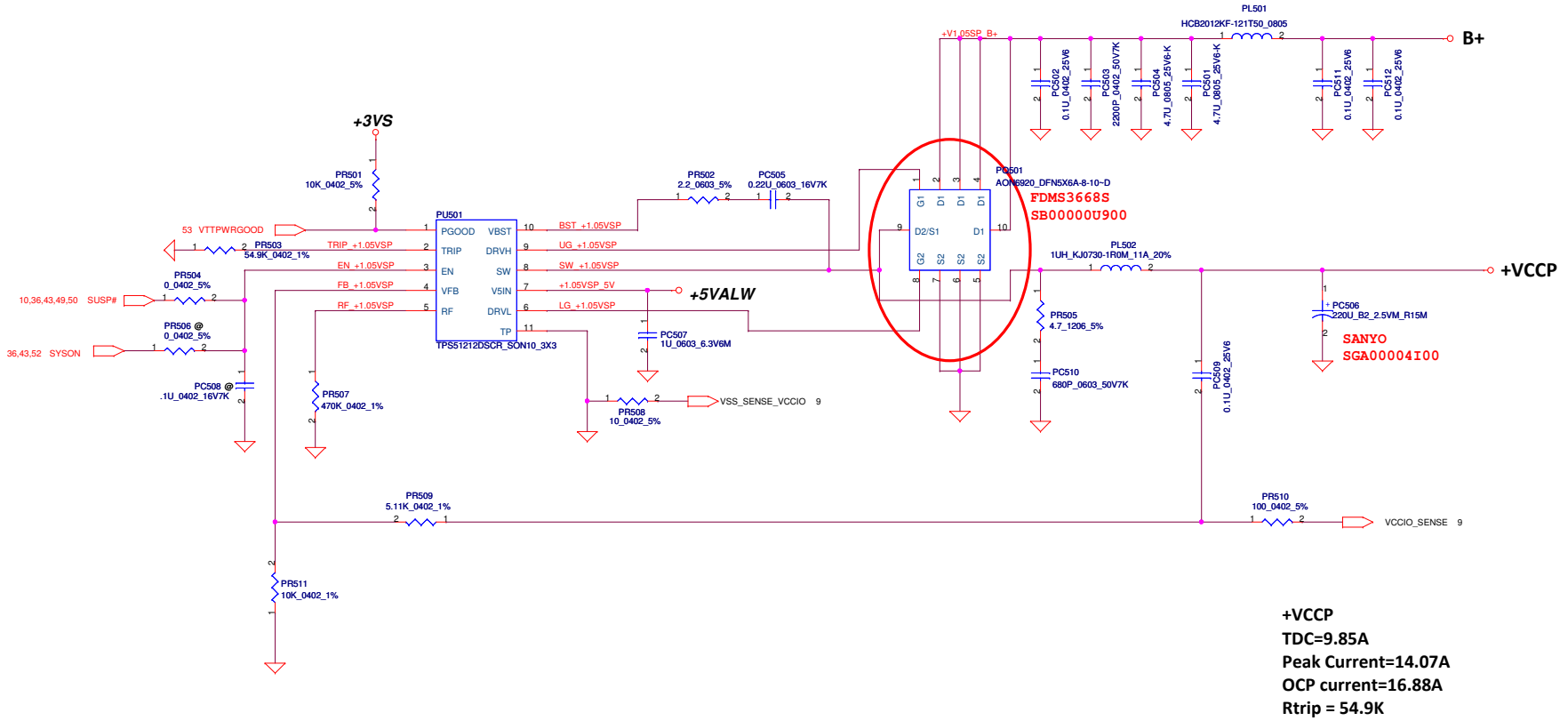


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				Rev 0.1 Sheet 49 of 59



+1.5V_PCIEP  **+1.5V_PCIE**
UMA **DIS**
+1.5V_PCIE **+1.5V_PCIE**
TDC=0.46A **TDC=6A**
Peak Current=0.66A **Peak Current=8A**

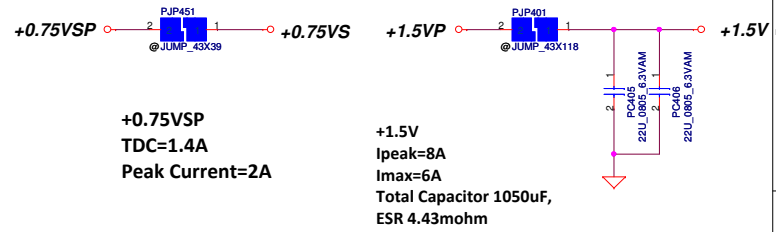
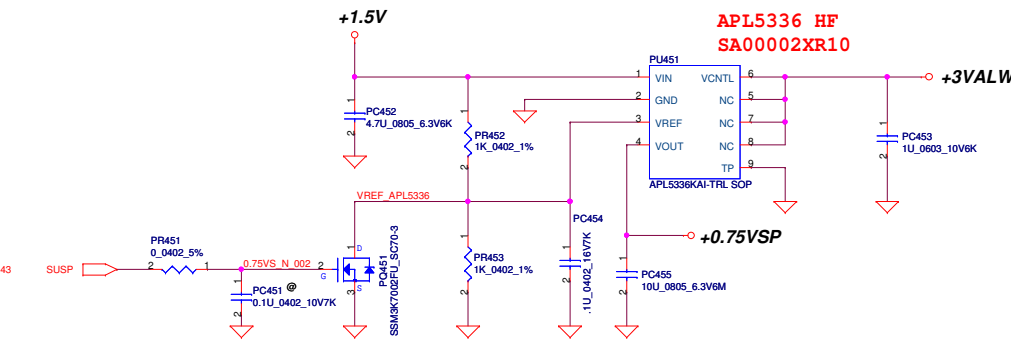
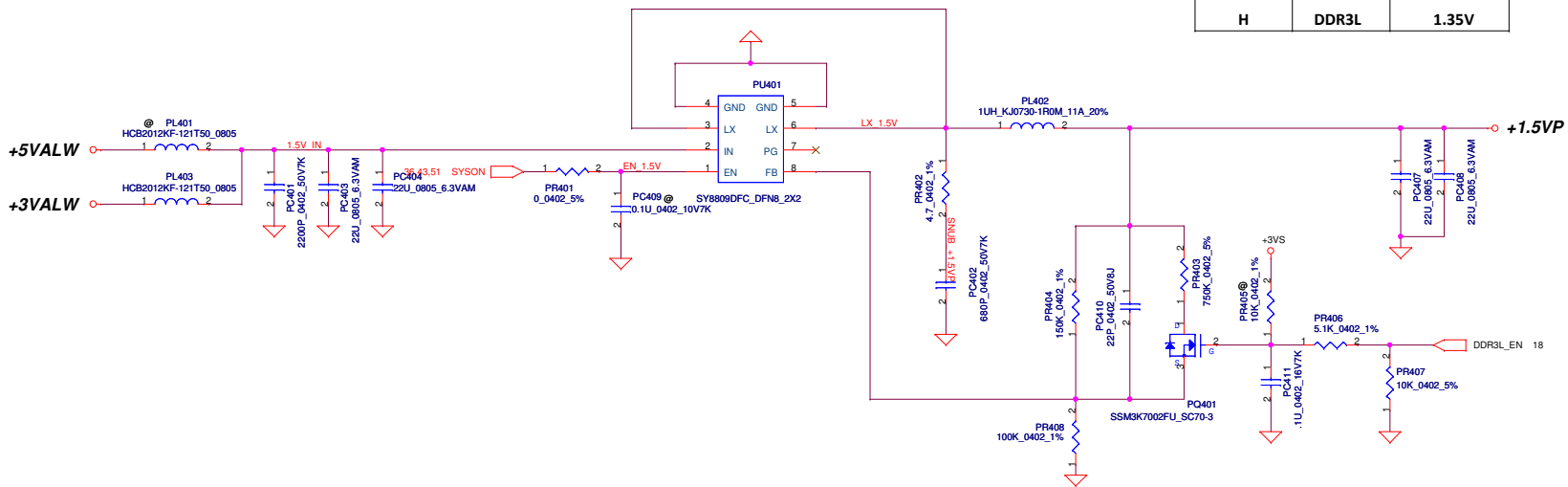
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Issued Date	2011/10/03	Deciphered Date	2014/12/31	Title	PWR- VGA VDDC
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+VCCP
TDC=9.85A
Peak Current=14.07A
OCP current=16.88A
Rtrip = 54.9K

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				Size	Document Number
	Customer	LA-8551P	0.1		
Date:	Saturday, March 03, 2012	Sheet	51	of 59	

DDR3L_EN		1.5VP
L	DDR3	1.5V
H	DDR3L	1.35V

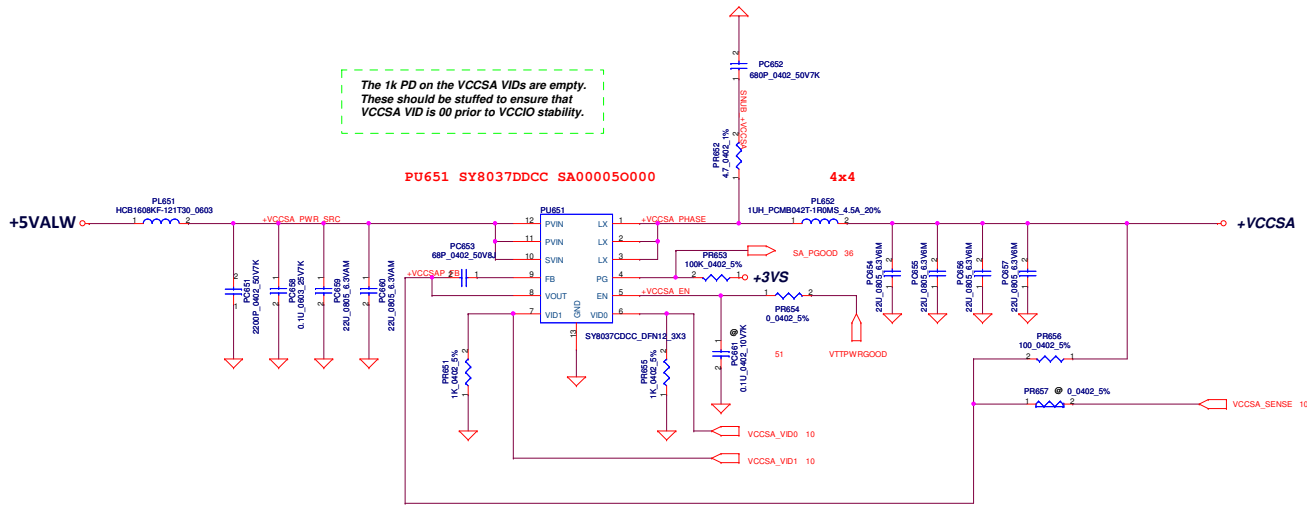


+1.5V
 Ipeak=8A
 Imax=6A
 Total Capacitor 1050uF,
 ESR 4.43mohm
 HW side:
 C106 330uF 17m
 C218 390uF 10m
 VGA@ CV122 390uF 10m
 @ C189 330uF 15m

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Compal Electronics, Inc.		
Title PWR- 1.5VP/0.75VSP		
Size	Document Number	Rev
Custom	LA-8551P	0.1
Date:	Saturday, March 03, 2012	Sheet 52 of 59

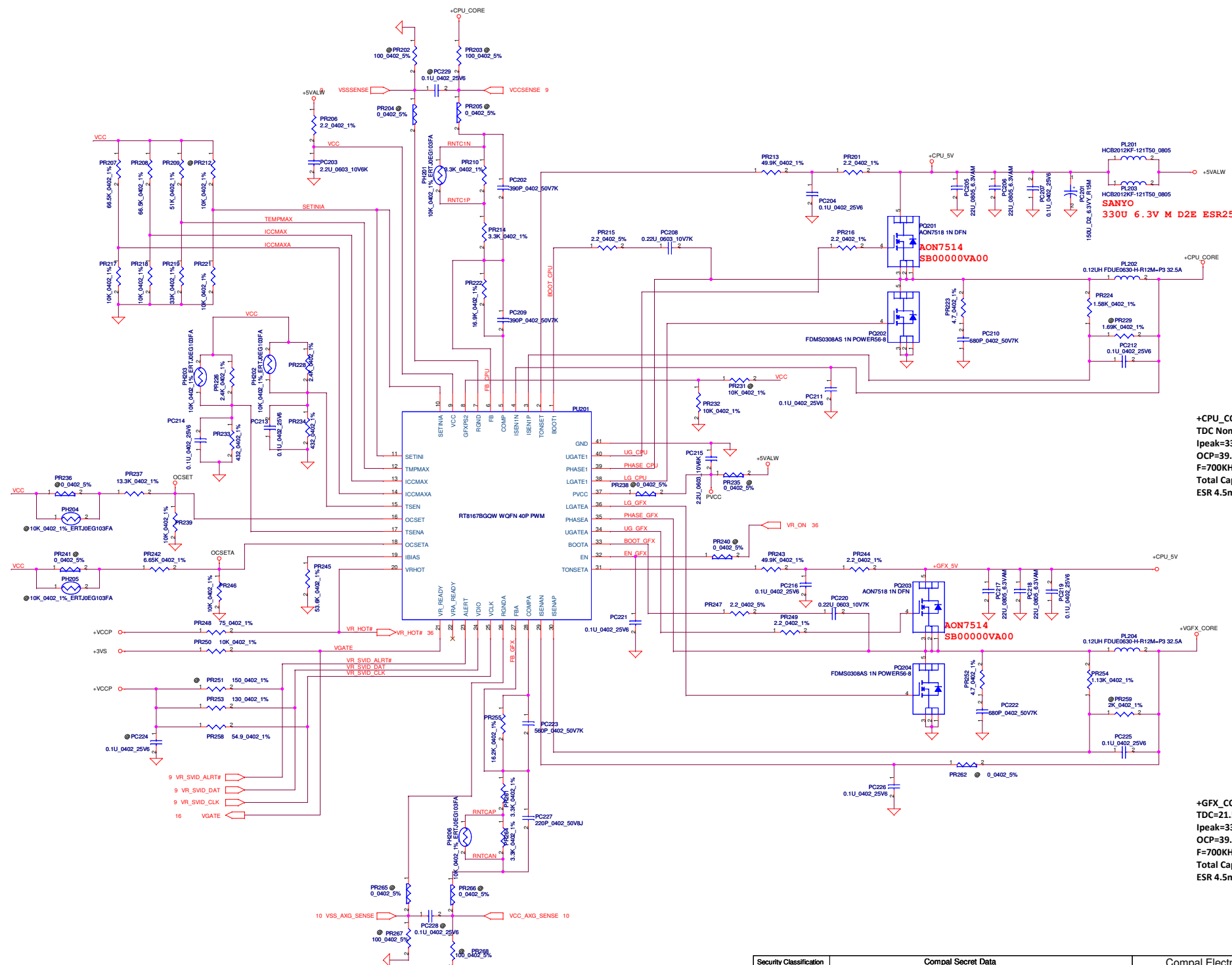
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



+VCCSA
Icdc=3A
Imax=4A

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Size	C	Document Number	LA-8551P	Rev
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QCL70



SANYO
330U 6.3V M D2E ESR25M TPE H1.8

+CPU_CORE
TDC Nom=16A
Ipeak=33A
OCP=39.6A
F=700KHz
Total Capacitor 470uF,
ESR 4.5mohm

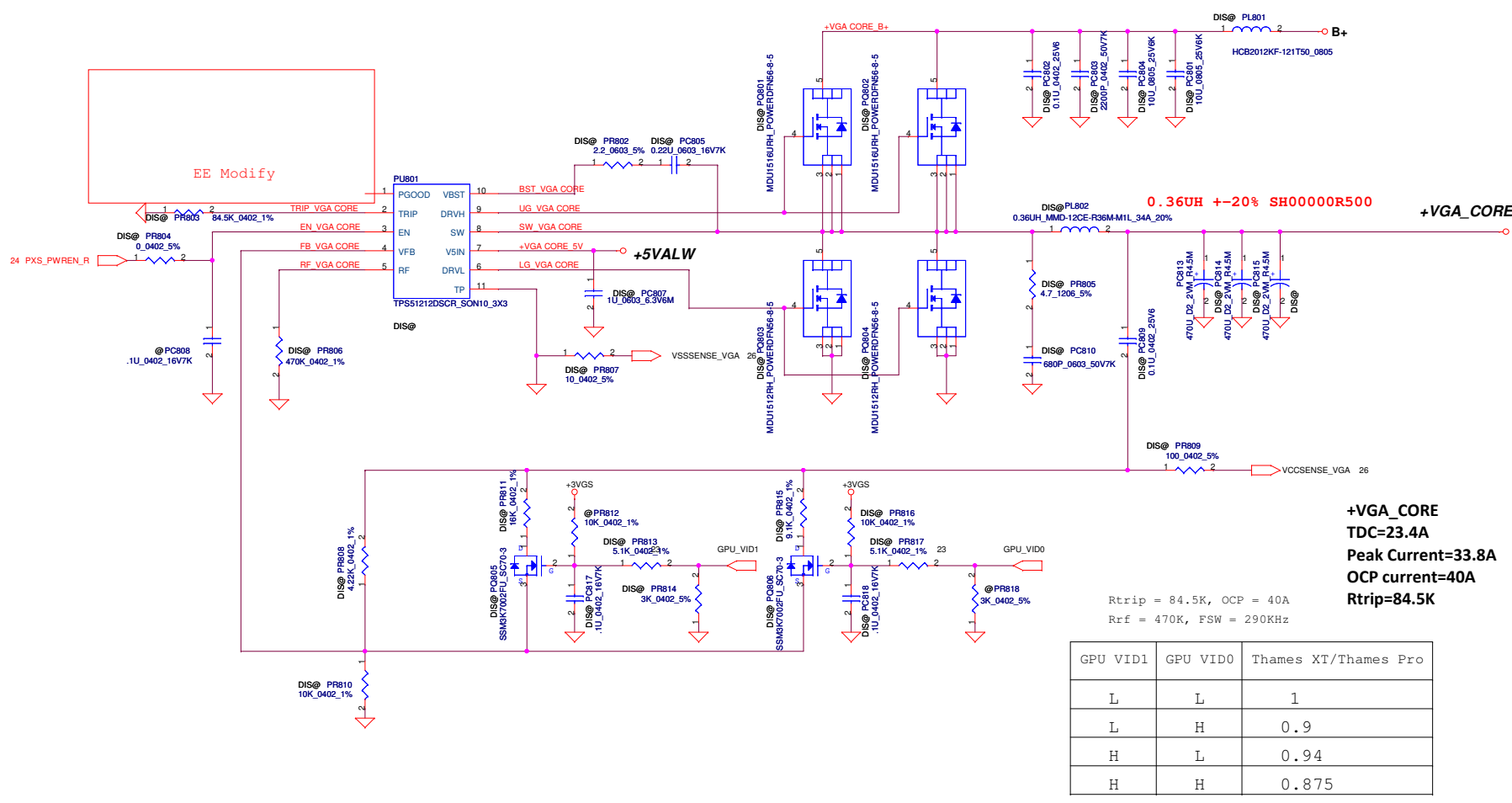
+GFX_CORE
TDC=21.5A
Ipeak=33A
OCP=39.6A
F=700KHz
Total Capacitor 470uF
ESR 4.5mohm

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Doc Number	LA-8551P	Rev	1.0	Date: Saturday, March 03, 2012 Sheet 54 of 59	



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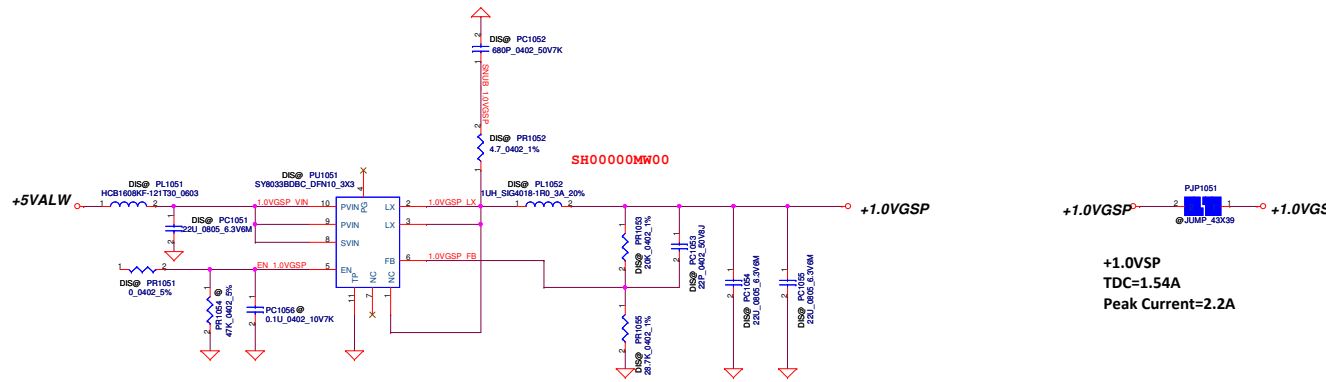


+VGA_CORE
TDC=23.4A
Peak Current=33.8A
OCP current=40A
Rtrip=84.5K

Rtrip = 84.5K, OCP = 40A
 Rrf = 470K, FSW = 290KHz

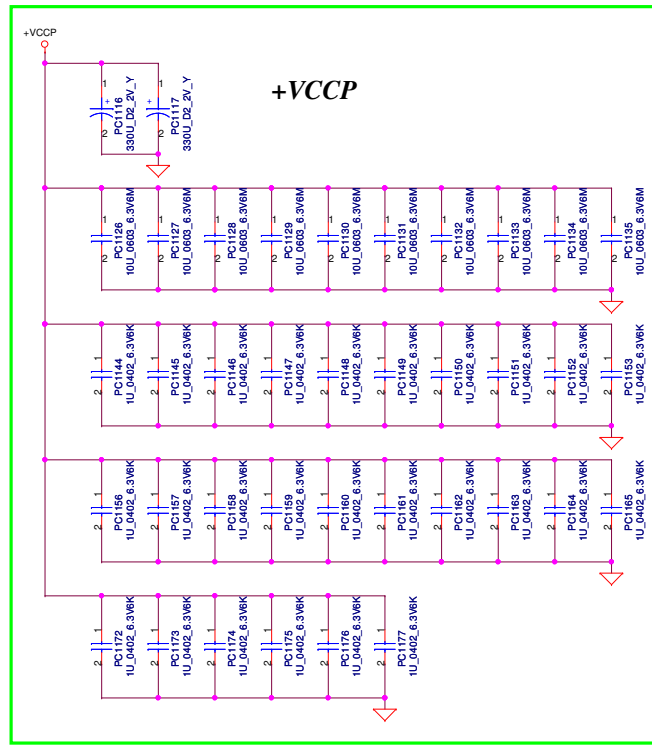
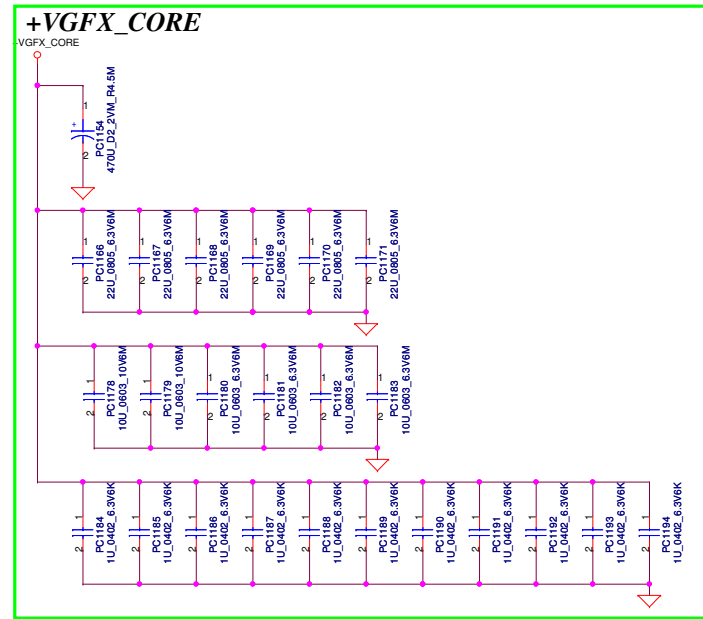
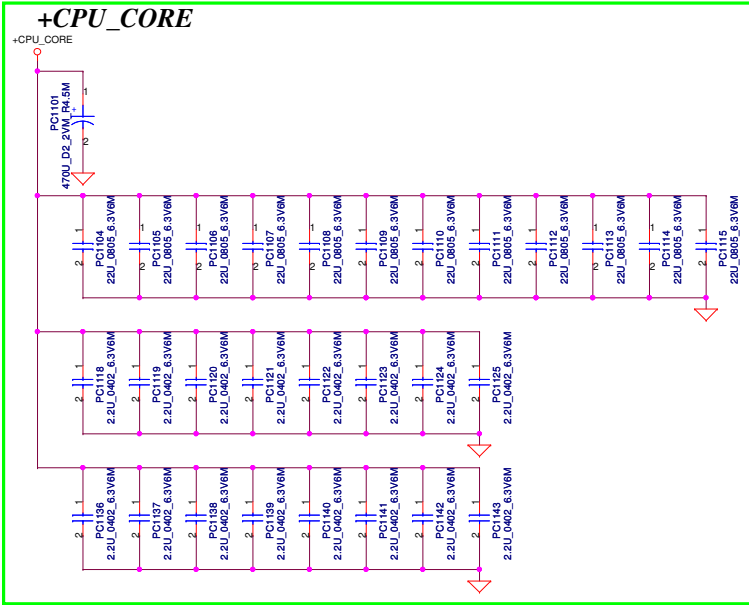
GPU VID1	GPU VID0	Thames XT/Thames Pro
L	L	1
L	H	0.9
H	L	0.94
H	H	0.875

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Size	Document Number	Customer	Rev	Date	
Custom	LA-8551P		0.1	Wednesday, March 07, 2012	
			Sheet 55 of 59		



+1.0VSP
TDC=1.54A
Peak Current=2.2A

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Issued Date		Deciphered Date		PWR - PROCESSOR DECOUPLING	
2011/10/03		2014/12/31		Document Number	
				LA-8551P	
				Date: Saturday, March 03, 2012	
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				Row 0.1	

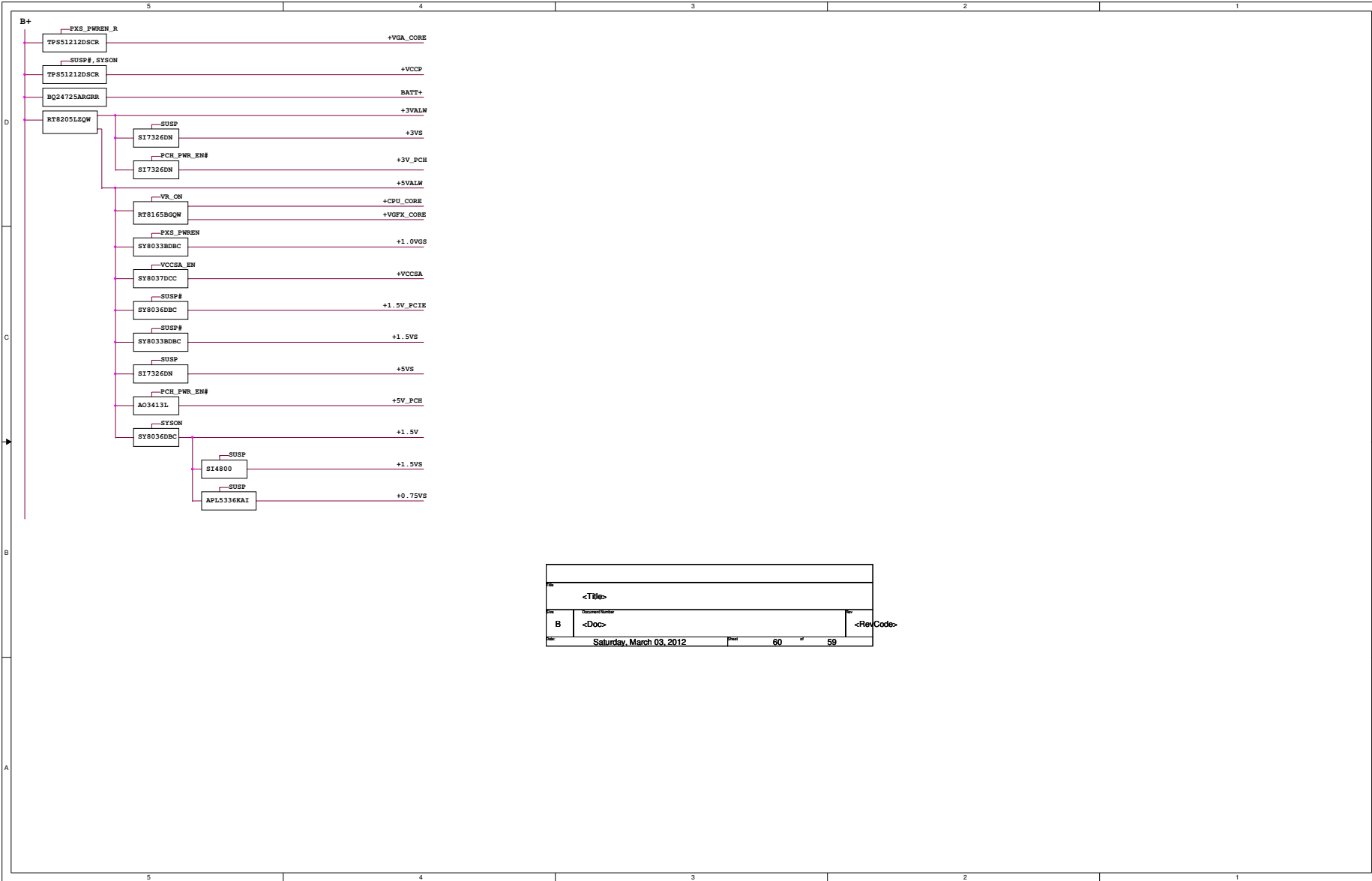
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	change PC111 to 0402	2011/11/28		For layout space		
2	47	remove PR121	2011/11/28		0ohm, not needed		
3	47	change PR124 to 270K, PR126 to 42.2K	2011/11/28		change Vin detector setting		
4	47	change PC125 to 0.047uF	2011/11/28				
5	47	change PR125 to 0ohm, PC126 to 100pF	2011/11/28		F&E review recomment		
6	47	change PR119 to 365K	2011/11/28		modify charge Ilimit to 3.54A		
7	47	change PR111 to 0ohm	2011/11/28				
8	47	add PL101	2011/11/28				
9	46	delete PD5, PD6	2011/11/28		imbedded battery, ESD diode is not needed		
10	46	SMC, SMD exchange	2011/11/28				
11	46	delete pin8 and pin5, add battery temp sense at pin5.	2011/11/28		EC request to need one detect pin if SMB communication fail.		
12	47	change FQ302 to AON7518	2011/11/28				
13	50, 52	change PU1001, PU401 from SY8036HDCC to SY8036LDC	2011/11/28				
14	53	change PU651 from SY8037DCC to SY8037ADCC	2011/11/28				
15	52	add FQ401, PR406, PR407, PC411	2011/11/28				
16	56	change PR1055 to 28.7K	2011/11/28		for correct 1.0V voltage		
17	54	change PL202, PL204 to SH00000PP00, 0.12uH	2011/11/28				
18	54	change PU201 to RT8167, SA00005AU00	2011/11/28				
19	54	change FQ201, FQ203 to AON7518, SB00000U300	2011/11/28				
20	54	change FQ202, FQ204 to FDMS0308AS, SB00000U400	2011/11/28				
21	55	change PL802 to 0.36uH, SH00000HD00	2011/11/28				
22	52	change PU401 to SY8809DFC	2011/11/29				
23	45, 48	change PD2, PD301 DIO CD4148WN-1 1206	2011/11/29		For cost and layout space		
24	51	add PC511, PC512	2011/12/11				
25	54	change PL201 to 0805, and add PL203	2011/12/11				
26	48	add PR320	2011/12/11		tune frequency		
27	55	change PC813, PC814, PC815, PC816 tp 330uF 9m	2011/12/11				
28	47	change PQ101 to SB000009610	2011/12/11				
29	54	change PR210, PR214, PR261, PR264 to 3.3K; PR222 to 15.8K; PR255 to 10.5K; PC202, PC209 to 270p; PC223 to 220p; PC227 to 560p; PR224, PR254 to 1.82K; PR207 to 127K	2011/12/11		Fine tune CPU, GFX transient		
30	47, 54	change PR111, PR110, PR216, PR249 to 2.2 ohm	2011/12/12		For EMI solution		
31	53, 56	change PL602, PL1052 to SH00000MMW00	2011/12/12		For crack issue		
32	55	change PL802 to SH00000HQ00	2011/12/12		For thermal solution		
33	48	change PL303 to SH00000ON00	2011/12/12		For thermal solution		
34	47	change PR114, PR115 to 0 ohm	2011/12/14		Prevent charger damaged by negative output voltage		
35	54	change PR207 to 66.5K	2011/12/14		For GFX GT2 current limit		
36	54	change PR237 to 23.7K +-1% 0402	2011/12/23				
37	54	change PR241 to 1/16W 0 +-5% 0402	2011/12/23				
38	54	change PR242 to 23.7K +-1% 0402	2011/12/23				
39	47	change PQ103, PQ104 to SB00000TZ00	2011/12/23				
40	47, 48	change PQ106, PQ303 to SB00000H700	2011/12/23				
41	54	change PR210, PR261, PR264 to 3.3K +-1% 0402	2011/12/23				
42	53	change PL651 to SY8037CDCC	2012/1/11		For latch mode		
43	57	change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/11		For height limit		
44	46	Delete PC11	2012/1/12		For ME request		

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45	47	change PR114 to 10, PR115 to 6.8ohm, add PD103	2012/1/30		For Charger issue		
46	47	Add PC130, PC131, PC104, PC107	2012/1/30		For EMI solution		
47	48	Add PR321	2012/1/30		Choose working frequency to improve efficiency and thermal		
48	50	change 1.5VPCIE Circuit	2012/1/30		Change input voltage form 5V to 19V to slove thermal issue		
49	52	Add PL403	2012/1/30		Choose input voltage to slove thermal issue		
50	54	Change PR224 to 1.58Kohm, PC209 to 220PF, PC202 to 390PF, PR222 to 16.9Kohm, PR237 to 21.5K	2012/1/30		Base on SI layout, FAE review recommand value		
51	48	change PL303 to SH00000F600	2012/1/30		For thermal issue		
52	45	Delete PD2, PR2, FR3, PC6	2012/1/30		For Layout space		
53	47, 48, 54	Change PQ302, PQ201, PQ203 to AON7514	2012/1/30		For efficiency		
54	51	Delete FJP501	2012/1/30		For Layout space		
55	55	Change PC813, PC814, PC815 to 470uF, delete PC816 Change PL802 0.36uF to 13*13*3.5 size	2012/1/30		For thermal issue		
56	55	Add PC820, PC821, PC822	2012/1/30		For VGA transient voltage		
57	57	Change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/30		For ME request		
58	47	change PQ102 to TPCA8057	2012/1/30				
59	54	change PC223 to 560pF, PC227 to 220pF	2012/2/17		For FAE suggesstion		
60	48	change PQ302 to AON7518	2012/2/17		For efficiency		
61	55	change PL802 to 13*13*3 size	2012/2/17		For thermal solution		
62	47	change PR114, PR115 to 0 ohm, PD103 to SCS00005800	2012/2/17		For HP and soucer request		
63	54	change PC201 to 330uF	2012/2/17		For acoustic solution		
64	45	change LED circuit	2012/2/23				
65	48	change PL303 to 3.3uH 10*10*3H, PC313 to 150U_B2_6.3VM_R35M, remove 5V output jumper	2012/2/23		For thermal solution		
66	53	change PU651 to SY8037DDCC	2012/2/23		For ULV CPU and latch mode		
67	55	change FR812 and FR816 power to +3VGS	2012/2/23		For leakage issue		
68	45	change LED circuit	2012/2/29				
69	54	change PC209 to 390pF, PR237 to 13.3Kohm, PR254 to 1.13Kohm, PR255 to 16.2Kohm, PR242 to 6.65Kohm	2012/2/29		Base on PV layout		
70	45	change PL1, PL2 to 0603 size, add PL4	2012/2/29		EMI request		

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