ZZZ0 PCB M/B DAZ@

ZZZ1 LA-7071P M/B DA@

ZZZ2 LS-7071P USB IO/B DA@

ZZZ3 LS-7074P HDD/B DA@

ZZZ4 LS-7075P LED/B DA@

ZZZ5 LA-7076P TP/B DA@

PCB DAZ0I200101

MB	DA60000KP10
USB IO/B	DA60000KQ10
HDD/B	DA400011R10
LED/B	DA400011T10
TP/B	DA400013910

Compal Confidential

P1VE6 LA7071P Schematics Document

AMD Ontario Processor with DDRIII + Hudson M1

11.6" M/B

2011-03-17

Rev : 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

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Title: Cover Page

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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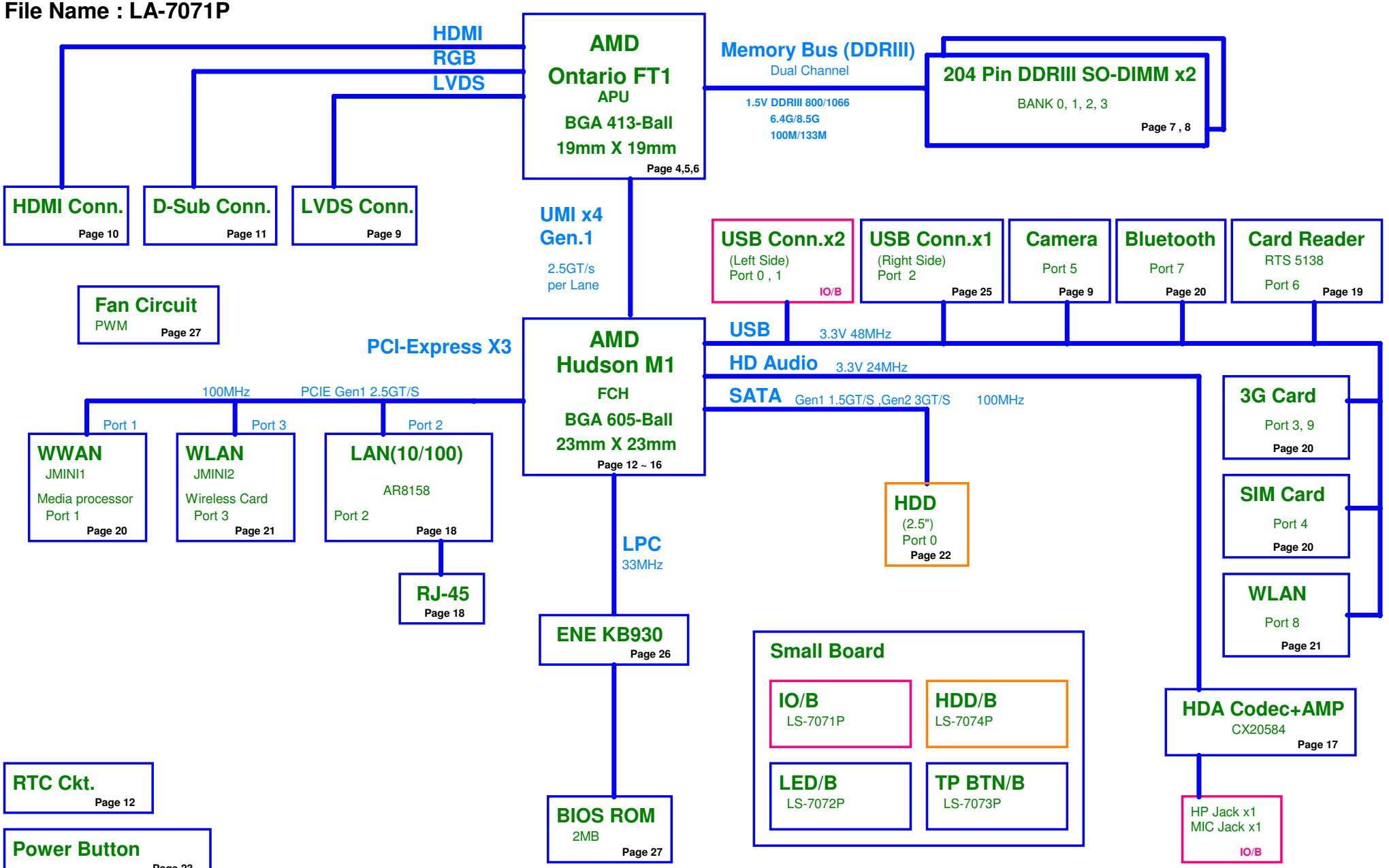
Compal Confidential

Model Name : P1VE6
File Name : LA-7071P

Brazos Platform



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Title: Block Diagrams

Size	Document Number	Rev
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	16H

EC SM Bus2 address

Device	Address	HEX
SB-TSI	1001-100xb	98H

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90

BOM Structure

```
HDMI@ : HDMI function
BT@   : BT function
CONN@ : Connetors
45@   : 45 Level
3G@   : 3G function
N3G@  : None 3G function
CMBS@ : Combo Jack POPO noise Solution
NCMBS@: None Combo Jack POPO noise Solution
```

FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left conn
Port1	Left conn
Port2	Right conn
Port3	WWAN
Port4	SIM
Port5	USB Camera
Port6	CardReader
Port7	BT
Port8	WiMax
Port9	WWAN
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	NC
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	NC
	PCIE1	WWAN
	PCIE2	LAN
	PCIE3	WLAN

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Board ID / SKU ID Table for AD channel

Vcc	+3VALW
Ra	100K +/- 5%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	PCB Revision
0	0	0 V	0 V	0 V	0.1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

*

SMBUS Control Table

	Source	BATT	DIMM	MINI Card	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB930	V					
EC_SMB_CK2 EC_SMB_DA2	KB930						V
HDMI_DATA HDMI_CLK	APU FT1					V	
EDID_DATA EDID_CLK	APU FT1				V		
FCH_SMDAT0 FCH_SMCLK0	FCH M1		V	V			

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Title: Notes List

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R9	R352	Display
mount	@	LVDS
@	mount	eDP

APU C50 P/N change to SA00004KD50
Tock 2010/12/30

SA00004KD50

U1B

DISPLAYPORT 1 / DISPLAYPORT 0 / CLK / SER / CTRL / JTAG / DP MISC / VGA DAC / TEST

S IC ONTARIO CMC50AFPB22GT 1G BGA ABO!

8/31 Change U1 P/N to SA00004DF00 S IC ONTARIO ZM121034B1238 1.2G BGA 413P

Change R10, R11 to RP1
Michael 2010/12/23

10/05 Add 100p(C405) on LDT_RST#

Reserve C432, C433, C434, C435
Michael 2010/11/18

Power Circuit

9/9 Change R24 from @ to mount R26 from mount to @
9/15 Change R24 from mount to @

Connection to EC, FCH input need to pull-down

Add C429 for APU_PROCHOT#
Michael 2010/11/18

Close to APU

Power Circuit

9/6 Add R379, R380 for APU_VDDNB_RUN_FB_L

8/25 Pull-up 100k(@ R352) to +3VS on LTDP0_HPD for eDP

Reserve R389 for eDP function
Tock 2010/12/30

10/01 Remove T1,T3~T7,T11,T12,T31,T32

9/9 Add R386 (1k@) to +1.8VS on TEST35
9/13 Change R30 from mount to @, R386 from @ to mount (AMD Recommend)

Reserve C438 for ALLOW_STOP#
Michael 2010/11/18

If FCH internal pull-up disabled, level-shifter could be deleted.
Need BIOS to disable internal pull-up!!

2N7002DW-T/R7

Vgs(th): min 1.0V
Typ 1.6V
Max 2.0V

If Q8 or R429, R432 implemented,
EC side pull-up need to be mounted

8/19 Change Q2A Q2B SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

9/17 Remove JHDT1 R40, R44, R45, R46 , Add T26~T32

9/20 Delete R41~R43

AMD Debug

Reserve C421 for APU_PWRGD
Michael 2010/11/18

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Title: FT1 CTRL/DP/CRT

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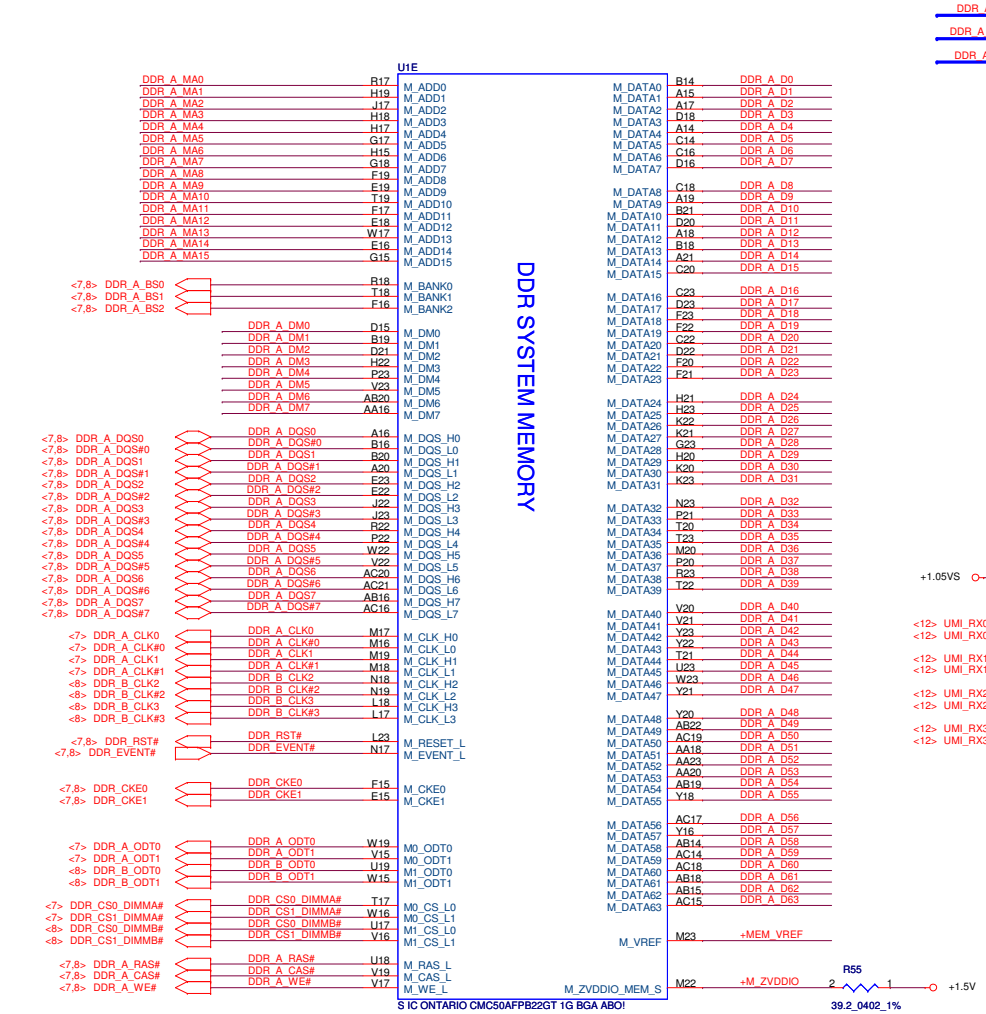
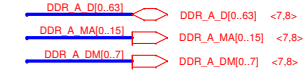


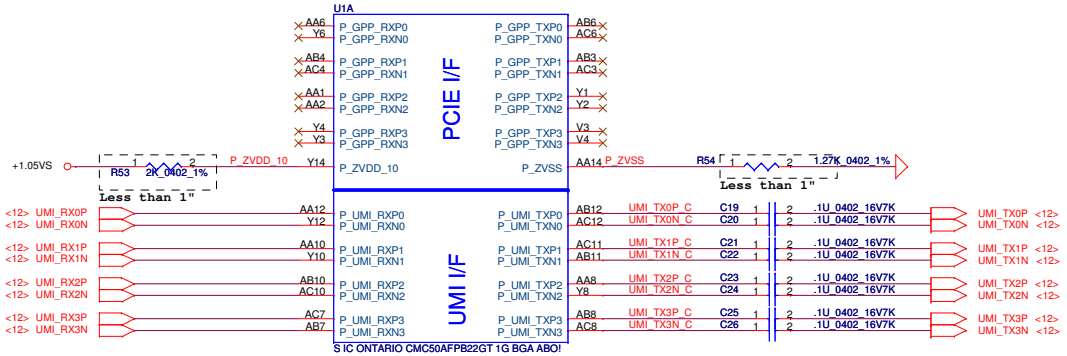


8/22 Delete C11~C18 (No VGA)

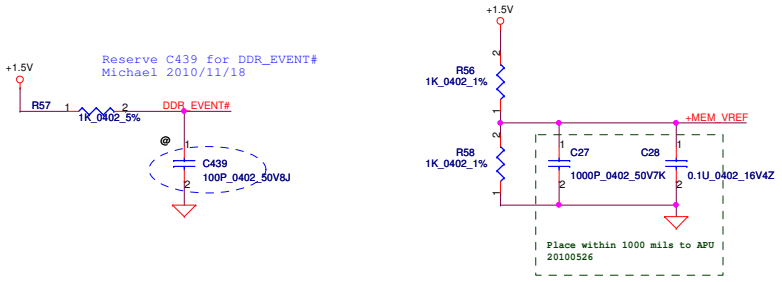
9/6 Change PCI-E from FCH to APU

9/6 Update PCI-E port List

9/15 Change PCI-E from APU to FCH



9/11 Delete DDR Signal link to JDIMM2



Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: FT1 DDRIII/UMI/PCIE

Size	Document Number	Rev
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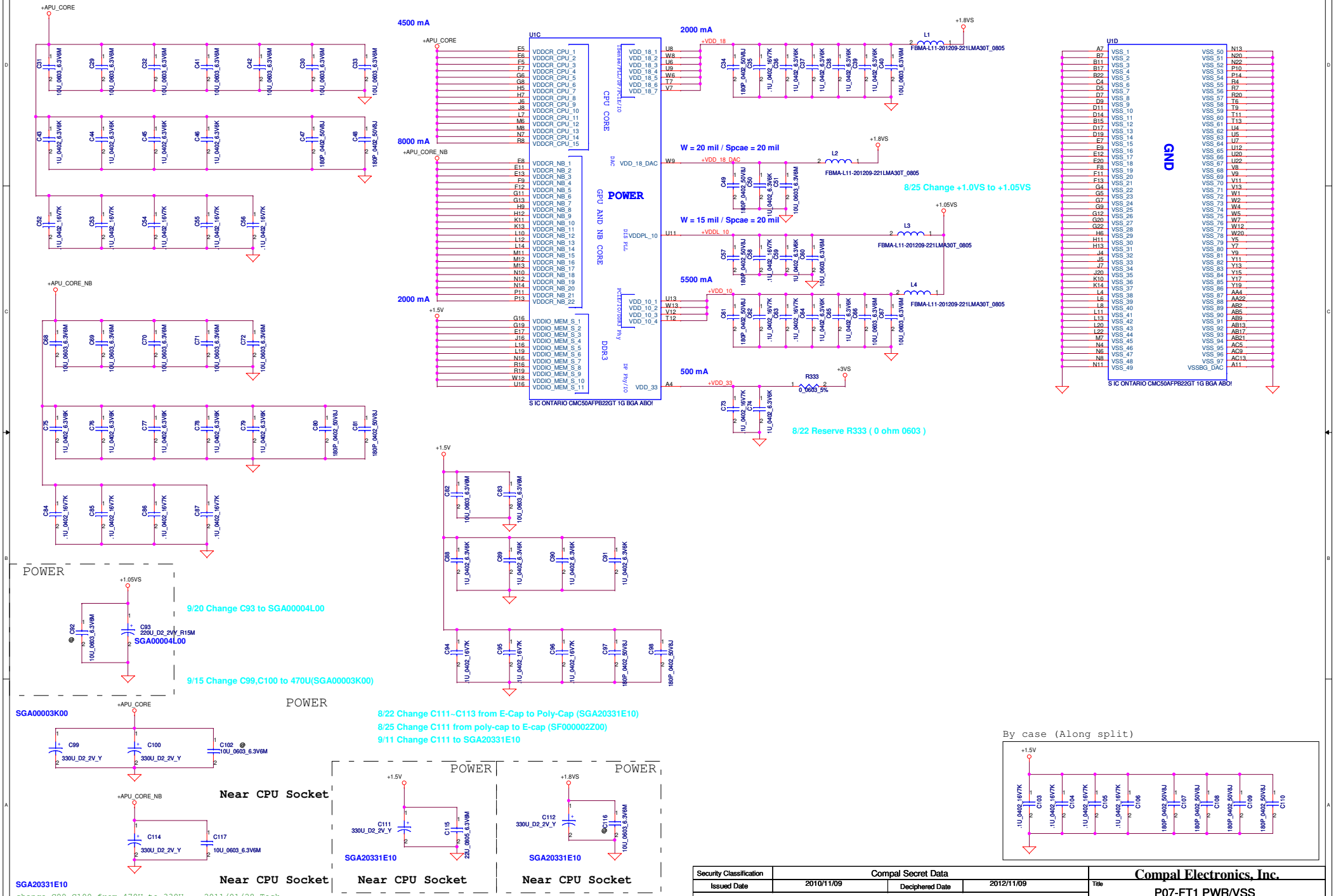

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: P07-FT1 PWR/VSS

Size: C | Document Number: P1VE6 Schematics | Rev: 1.0

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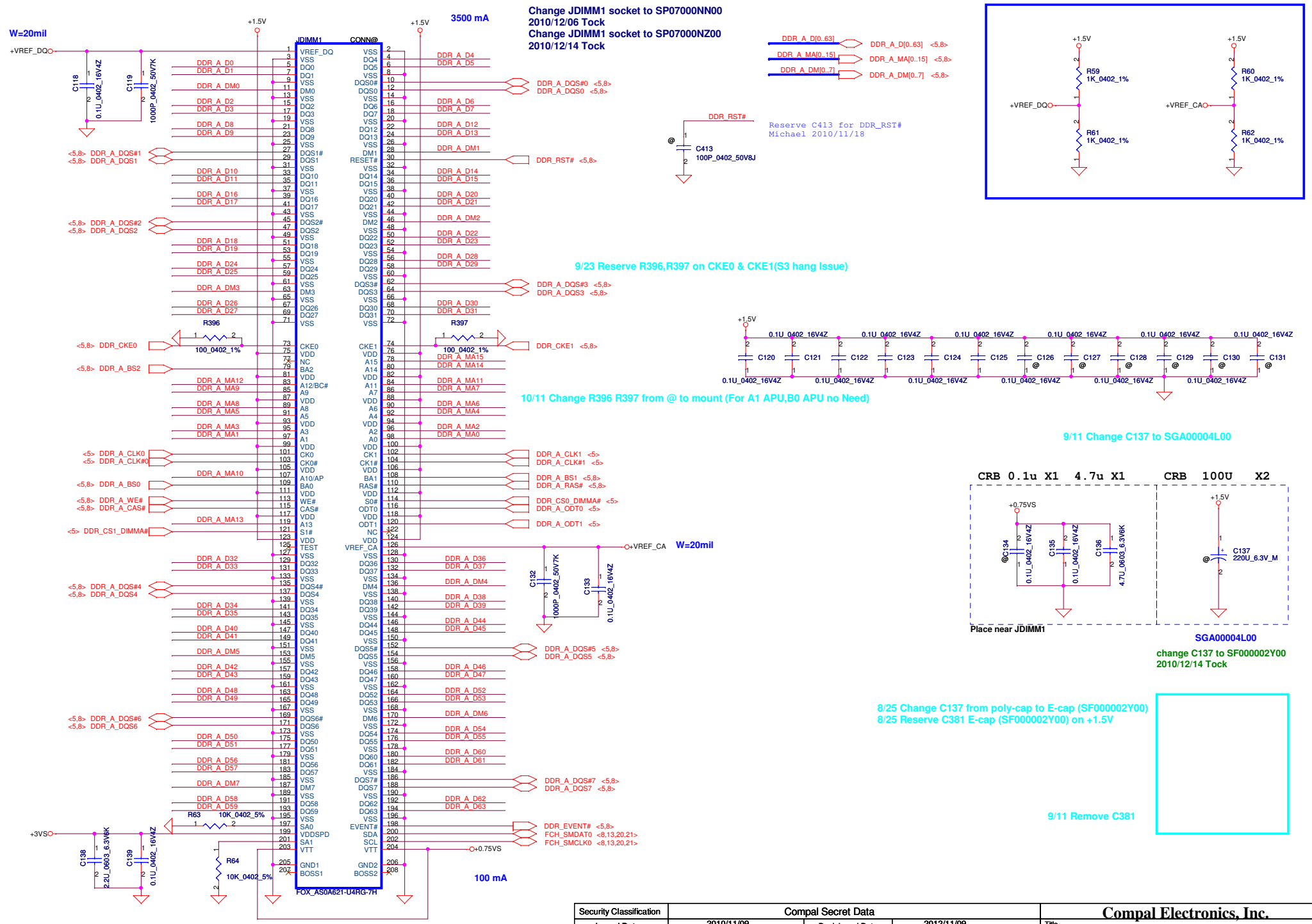

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: DDR3 SODIMM-I Socket

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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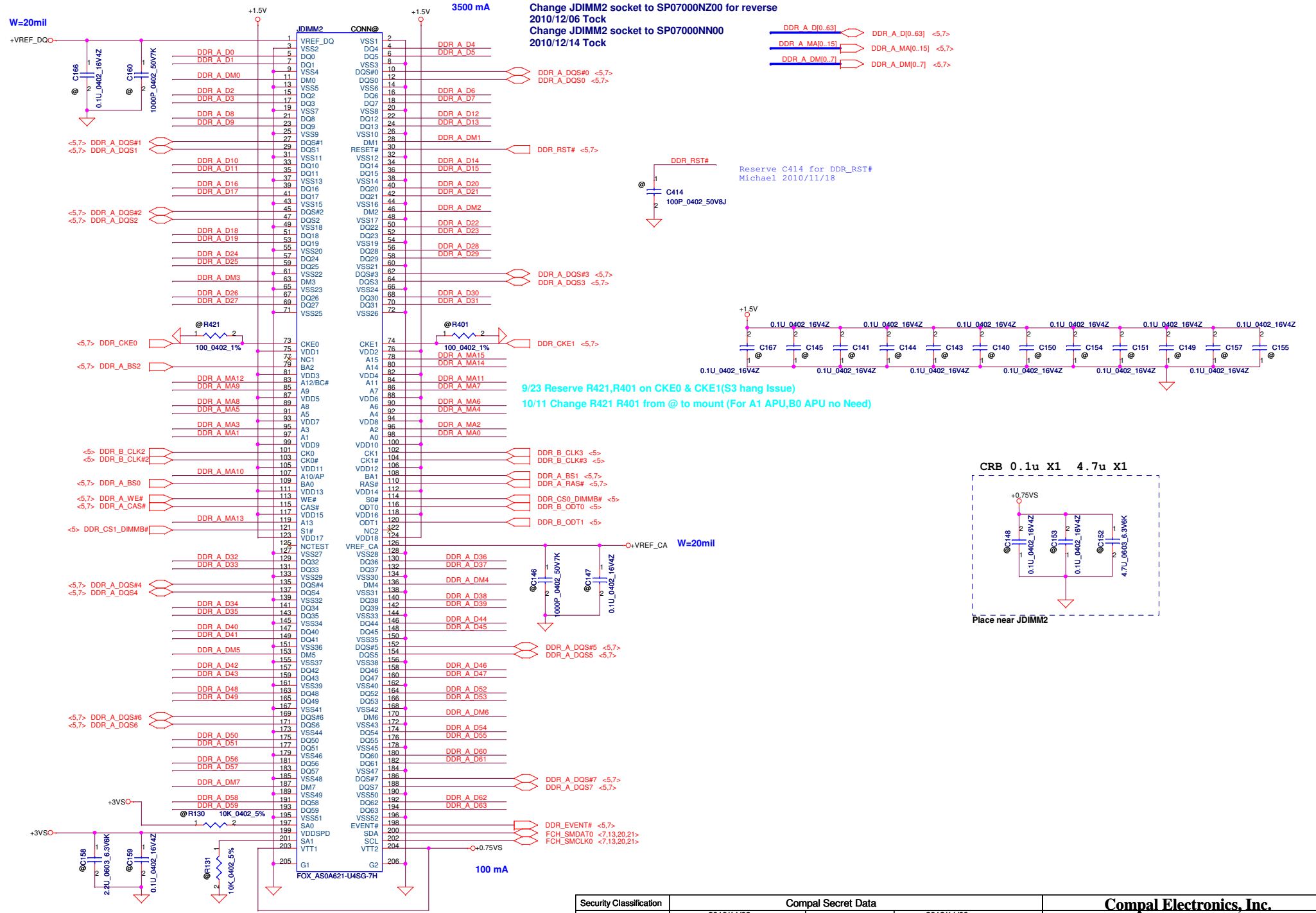

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: DDR3 SODIMM-II Socket

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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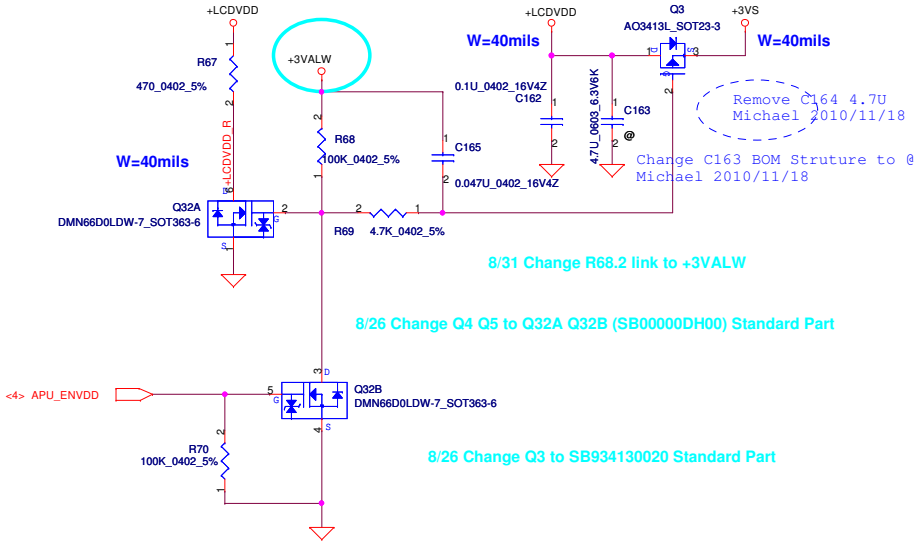
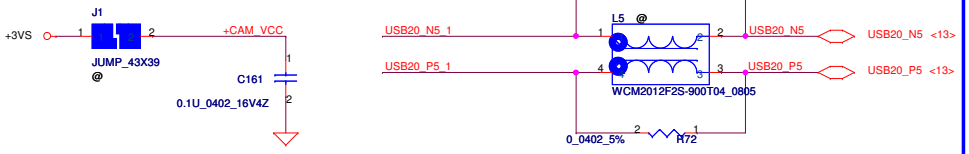
LCD POWER CIRCUIT

11/02 Change Q3 PN to SB934130020
2011/02/11 Change Q3 PN to SB000006R10



9/9 Reserve 100k PD to GND on INVTPWM 9/17 Change R387 from @ to mount

Camera



9/15 Remove D1 L5 R71 R72 C166 C167 for layout spacing
9/23 Add D1 L5 R71 R72 C166 C167 for ESD
9/23 Remove D1 C166 C167
9/24 Swap L5

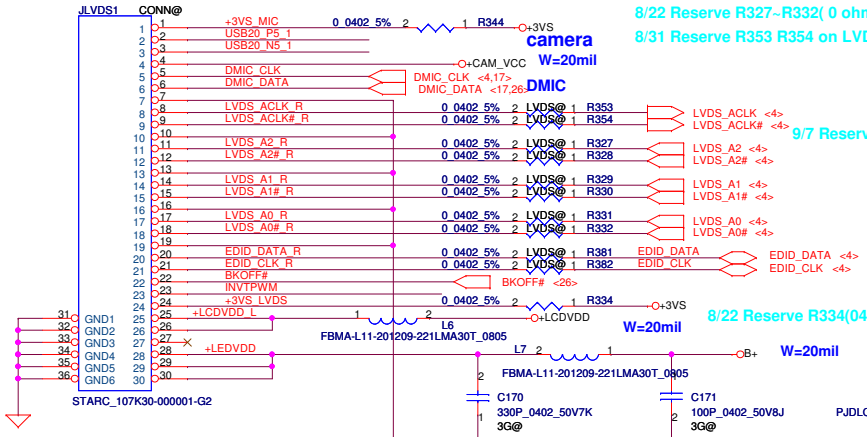
CMOS & LCD/PANEL BD. Conn.

DMIC

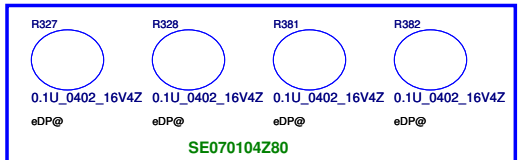
Add R344 0 ohm for +3VS_MIC
Michael 2010/11/18

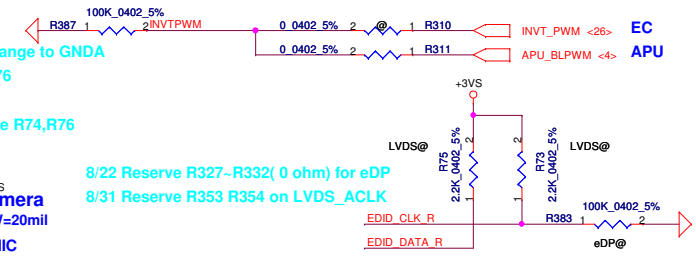
Connect DMIC_CLK,
DMIC_DATA
to JLVDS1 pin 5 and 6
Michael 2010/11/18

8/25 JLVDS1.5 change to INT_MIC0 JLVDS1.6 change to GNDA
8/31 Update JLVDS1 Pin definition Delete R74 R76
9/13 Update LVDS Pin definition, Add R74,R76
9/13 Add Net Name +3VS_DMIC 10/01 Remove R74,R76

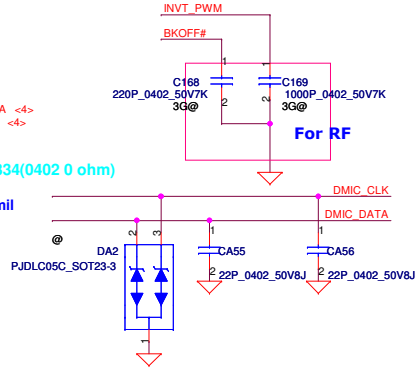


change JLVDS1 to SP010011S00
2010/12/14 Tock

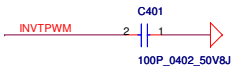




8/22 Reserve R327~R332(0 ohm) for eDP
8/31 Reserve R353 R354 on LVDS_ACLK
9/7 Reserve R381,R382(0 ohm)R383(100k@) for eDP
8/22 Reserve R334(0402 0 ohm)



10/04 Add 100p(C401) on INVT_PWM



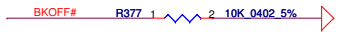
10/04 Change C401 on INVTPWM

R75
100K_0402_5%
eDP@
SD028100380

*

Display	LVDS	eDP
R327	0 ohm	0.1uF
R328	0 ohm	0.1uF
R381	0 ohm	0.1uF
R382	0 ohm	0.1uF
R383	@	100k ohm
R73	2.2k ohm	@
R75	2.2k ohm	100k ohm

9/3 Pull-Down 10k(R377) to GND on BKOFF#



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Compal Electronics, Inc.

Title: LVDS / Camera / DMIC

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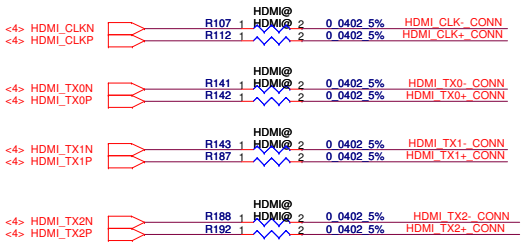


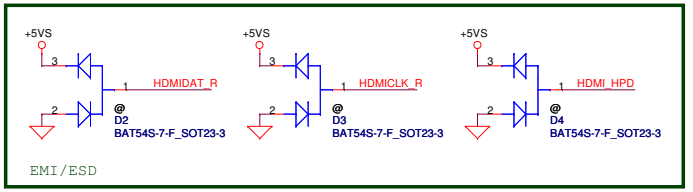
Change RP13 to R107 , R112
Tock 2010/12/30

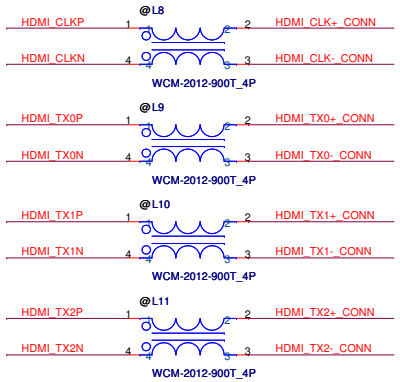
Change RP14 to R141 , R142
Tock 2010/12/30

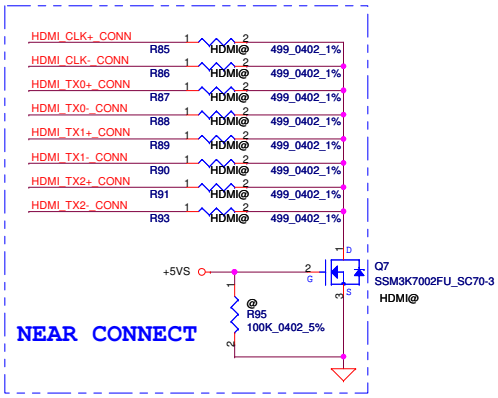
Change RP15 to R143 , R187
Tock 2010/12/30

Change RP16 to R188 , R192
Tock 2010/12/30

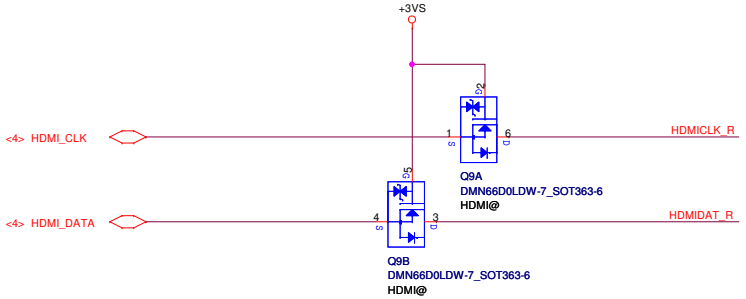
Swap HDMI Net of RP13~RP16 for layout
Tock 2010/12/24





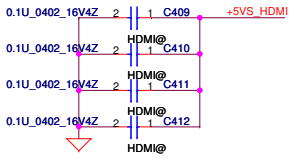


8/26 Change Q7 to SB000009610 Standard Part

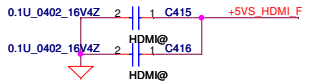


8/19 Change Q9A Q9B to SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

10/29 Add C409~C412(0.1U) on +5VS_HDMI



10/29 Add C415~C416(0.1U) on +5VS_HDMI_F

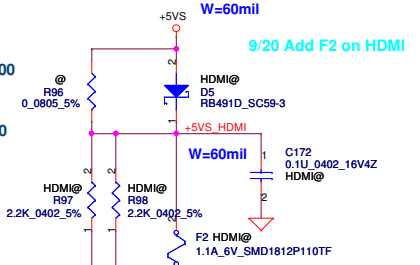


W=60mil

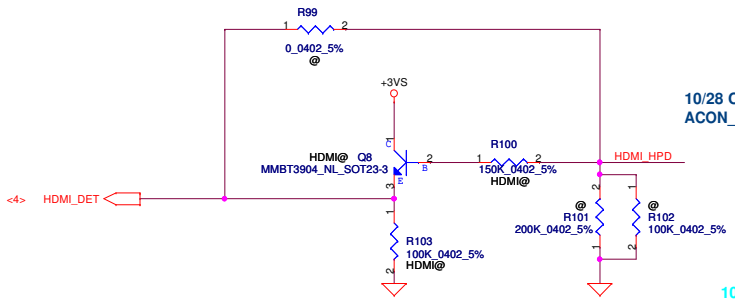
9/20 Add F2 on HDMI

10/27 Change D5 P/N from SC1B491D000 to SCS00003H00

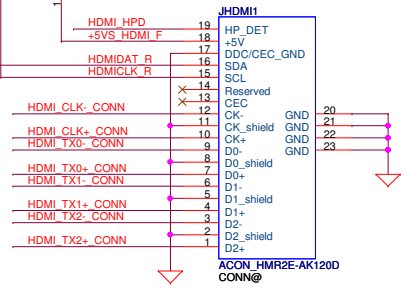
10/27 Change F2 P/N from SP04301P120 to SP040001B00



9/20 Change R99 from HDMI@ to @
9/20 Change Q8,R100 from @ to HDMI@



10/28 Change JHDMI1 footprint from
ACON_HMR2E-AK120D_19P-T to ACON_HMR2E-AK120D_19P-S



10/07 Update JHDMI1 footprint from ACON_HMR2E-AK120D_19P
to ACON_HMR2E-AK120D_19P-T

11/16 Update JHDMI1 Symbol (ACON_HMR2E-AK120D_19P)

8/23 Update JHDMI1 Symbol (SUYIN_100042GR019S268ZR_19P-T)

9/7 Update JHDMI1 Symbol (ACON_HMR2E-AK120D_19P)

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Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: HDMI Connector

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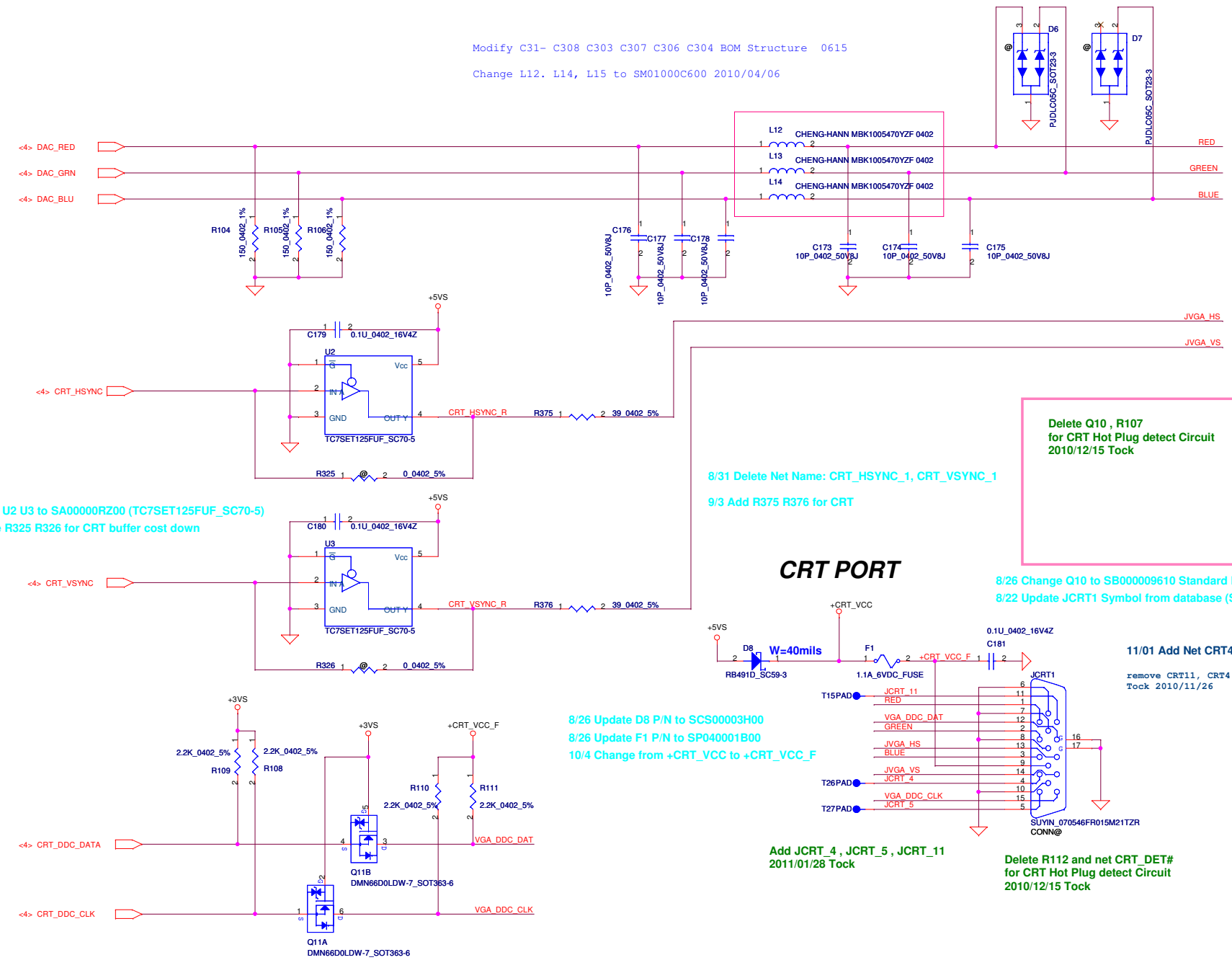
Close to CRT CONN for ESD.

Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

Change L12. L14, L15 to SM01000C600 2010/04/06



8/21 Change U2 U3 to SA00000RZ00 (TC7SET125FUF_SC70-5)
8/21 Reserve R325 R326 for CRT buffer cost down

8/31 Delete Net Name: CRT_HSYNC_1, CRT_VSYNC_1

9/3 Add R375 R376 for CRT

Delete Q10 , R107
for CRT Hot Plug detect Circuit
2010/12/15 Tock

8/26 Change Q10 to SB000009610 Standard Part
8/22 Update JCRT1 Symbol from database (SUYIN_070546FR015M21TZR_15P)

CRT PORT

8/26 Update D8 P/N to SCS00003H00
8/26 Update F1 P/N to SP040001B00
10/4 Change from +CRT_VCC to +CRT_VCC_F

11/01 Add Net CRT4, CRT11 on JCRT.4 , JCRT.11

remove CRT11, CRT4
Tock 2010/11/26

Add JCRT_4 , JCRT_5 , JCRT_11
2011/01/28 Tock

Delete R112 and net CRT_DET#
for CRT Hot Plug detect Circuit
2010/12/15 Tock

8/19 Change Q11A Q11B to SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: CRT PORT

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9/9 Add R384(@ 0 ohm) R385(0 ohm) on PCI-E RST
9/20 C183.2 link to R119.2 Follow CRB

10/08 Update U5 to SA000046H70 S IC 218-0792006 A13 HUDSON-M1 605P ABO!

Watchdog timer on NB_PWRGD enable for pull-up disable for pull-down 20100527

9/9 Change R117 R122 from mount to @
9/15 PU PE_GPIO1 100k to +5VALW

PE_GPIO0, PE_GPIO1 are for DIS only
It's no function for UMA
P1VE6 follow P5WE6 Tock 2010/11/26

9/2 Change R120 from 0603 to 0402

9/16 Change U4,C182 from @ to mount,
R120, R115 from mount to @

9/27 Change R115 from @ to mount

WWAN FCH TX
LAN FCH TX
WLAN FCH TX

WWAN FCH RX
LAN FCH RX
WLAN FCH RX

10/11 Change Y1 from SJ100006600 to SJ132P7KW10

Close to FCH

10/05 PD 10k(R405) on CLKRUN

9/6 Change PCI-E from FCH to APU
9/15 Change PCI-E from APU to FCH

8/25 Update JBATT1 Symbol (LOTES_AAA-BAT-019-K01_2P)

close to FCH within 1"

8/21 Delete R130,R131(No VGA)

LAN
WLAN
WWAN

8/23 Add R348 R349 for WWAN PCIE

9/6 Change D10 to SC600000B00 Standard Part
9/13 Add NONCHARGE@ for D10 R244
12/07 Remove BOM structure NONCHARGE@ for D10 R244 Tock

C396 near to PR12
Michael 2010/11/18

10/04 Add 100p(C396) on H_PWRGD_L

reserve C359 for RF
Tock 2010/12/28

9/1 Add R372 on CLK_48M_CR
9/7 Change R372 to 22 ohm

W=20mil

10/07 Change R140 from 560 to 1k ohm

11/01 Add Net U5_G22 on U5.G22

W=20mil

9/13 Add Net Name +RTCBATT1_RR
9/13 Change Net Name +RTCBATT1 to +RTCBATT2
9/13 Add C392,R392,D23(CHARGE@) for RTC Charge Circuit
10/07 Change R392 from 1k to 0 ohm
10/08 Change R392 from 0 ohm to 1k ohm
11/01 Change R392 from 1k to 0 ohm
12/07 Remove R392 , C392 , D23 Tock

reserve R388 , C361 for RF
Tock 2010/12/29

change R388,C361 BS from @ to 3G@ for RF solution
Tock 2011/03/16

SA000046HA0

8/25 Change FCH(U5) PN to SA000046H30

11/04 Change U5 PN to SA000046HA0 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 0FA)

For Clear CMOS, near to RAM door

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: FCH PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

Date: Thursday, March 17, 2011 | Sheet 12 of 37

Change to RP3 to R150 , R153 , R154 , R161
Tock 2010/12/30

Change R145, R147, R151, R152 to RP4
Michael 2010/12/23

Change RP4 to R145, R147, R151, R152 for layout
Tock 2010/12/27

Swap net of RP3 & RP5 for layout
Tock 2010/12/27

Reserve C418 for KB_RST#, C426 for PBTN_OUT Michael 2010/11/18

Reserve C417 for EC_RSMRST# Michael 2010/11/18

8/31 Pull up 10k(R359) to +3VS on WWAN_CLKREQ#

Reserve C431 for H_THERMTRIP# Michael 2010/11/18

8/31 Delete Net : SATA_DET#

Reserve C422 for ICH_POK Michael 2010/11/18

8/22 Delete Net : R161 R162

change RP5 to R162 , R163 , R164 , R186
Tock 2010/12/30

Reserve C474 for USB_OC1#
Tock 2011/01/07

Reserve C358 for RF
Tock 2010/12/28

co-lay 22P on C358 for 3G @ for RF solution
Tock 2011/03/16

Pull-down for enable high performance mode
20100527 (required for M1)

Reserve C427 , C440, C441, C442, C445 for SCI, SMI, PCIE_WAKE#, GATE20, PCI_PME#
Michael 2010/11/18

10/27 Change R408 R410 from @ to mount
10/28 Add R413 R414 on GPIO192 for project ID

R406	R407	Board ID
mount	@	P1VE6
@	mount	P1VS6

change R407,R408,R410,R413 from 10K to 1K
11/26 Tock

change R406 BOM to P0@ , R407 BOM to P1@
2011/01/04 Tock

9/15 Update USB Port List
9/1 Update USB Port List
8/23 USB port8 link to SIM

8/31 Change R182 from mount to @
Change R183 from @ to mount
9/15 Change R178 from @ to mount

Internal Pull-Up available

EC_PWM3	EC_PWM2	ROM TYPE
NC	L	SPI ROM
NC	NC	Reserved
L	L	Reserved
L	H	LPC ROM *

S IC 218-0792006 A13 HUDSON-M1 FCBGA 0FA

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: FCH HDA/USB/ACPI

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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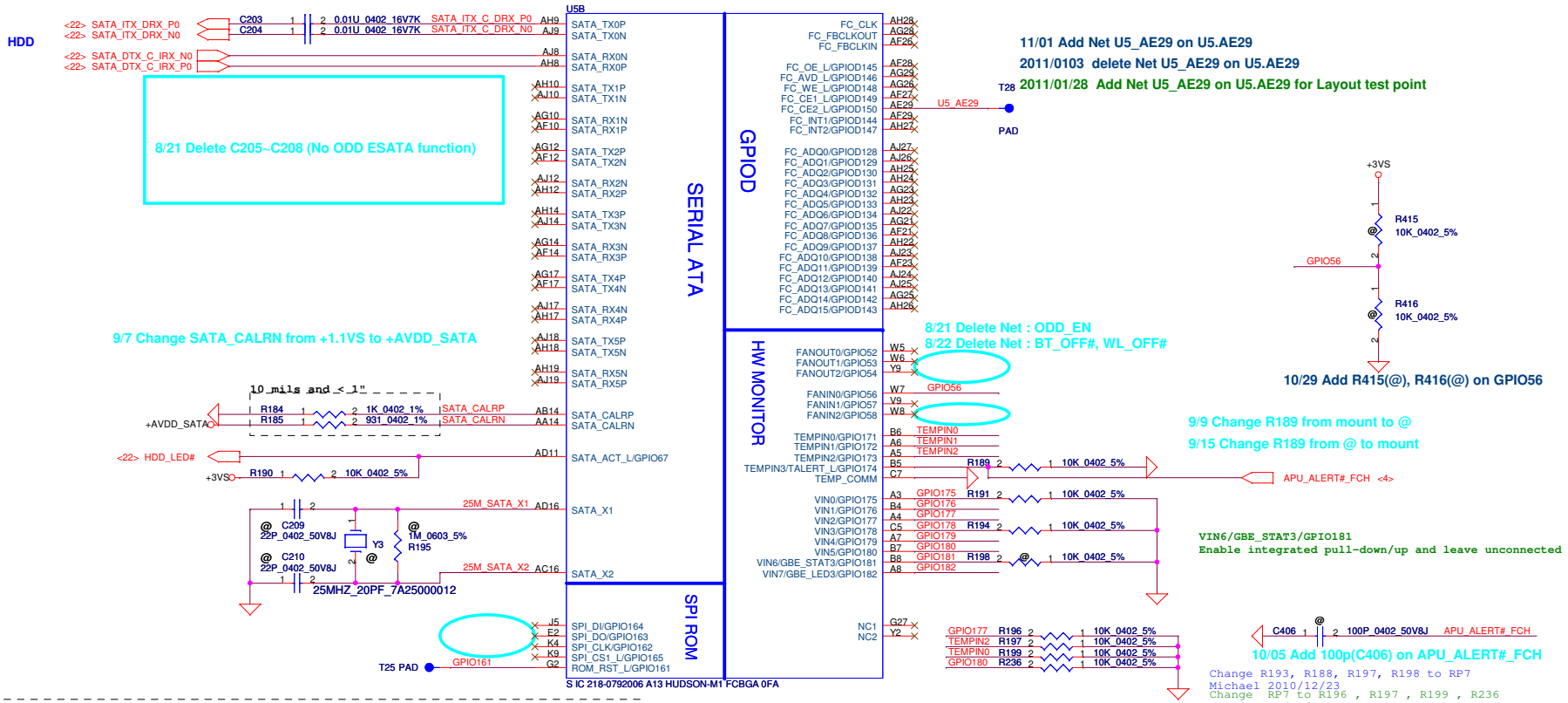


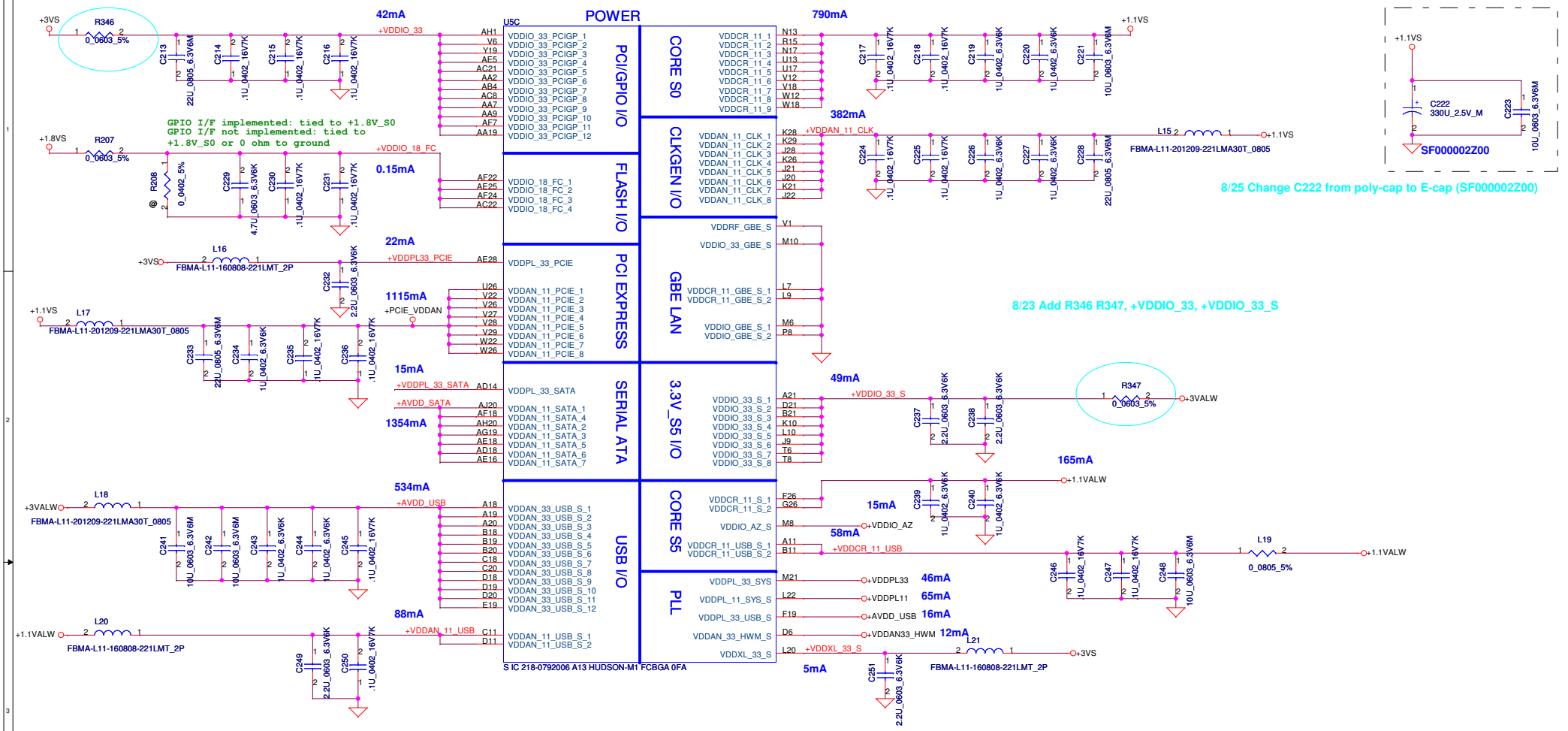
Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

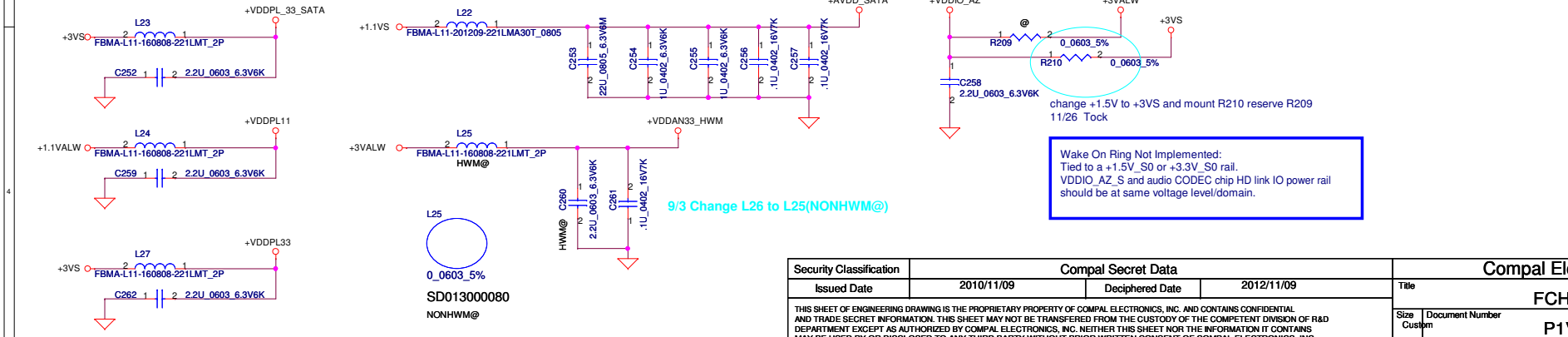
Compal Electronics, Inc.

Title: FCH-SATA/SPI

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

Date: Thursday, March 17, 2011 | Sheet 14 of 37





Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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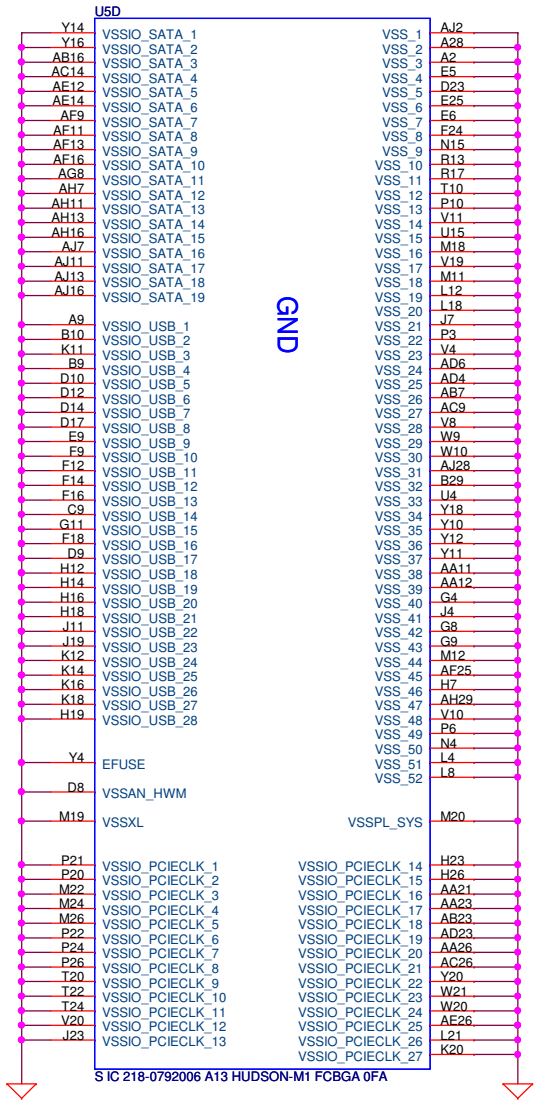
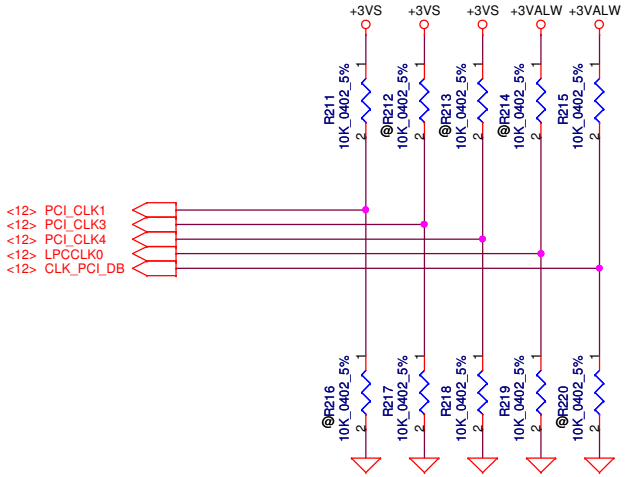


REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 *	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode *				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP *	CLKGEN Mode Internal *	internal EC DISABLE *	External CLKGEN Mode				



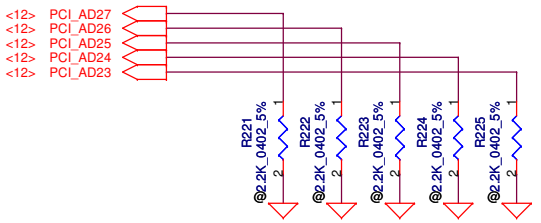
9/13 Change R211 from mount to @, R216 from @ to mount
9/13 Change R211 from @ to mount, R216 from mount to @

DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK *	ILA AUTORUN Disabled *	Selects FC PLL *	Disable I2C ROM *	Required Setting *
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function check default



Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: B | Document Number: P1VE6 Schematics | Rev: 1.0

Date: Thursday, March 17, 2011 | Sheet 16 of 37

08/19 Follow NTUC0

11/04 Change RA19 RA20 from 47k to 10k

Remove RA55,RA56 and add RA340 for power consumption
11/26 Tock

change RA19 from 10K to 33 ohm
Tock 2011/02/11

reserve DA21,DA22 by vender review
Tock 2010/12/08

08/21 Follow PAV70

Int. Speaker Conn.

20mil

10/26 Remove DA4 CA46 CA47 RA23 RA24
10/28 Add JSPK1 (2 pin)
10/28 Add DA4 CA46 CA47 RA23 RA24

Delete JSPK1
2010/12/15 Tock

Change RA31/ RA32 package to 0402
Michael 2010/11/18

40 mil

20 mil

9/3 Change CA38~ CA43 from 4.7U to 2.2U
Change RA16 from 1k to 100 ohm

9/25 Add RA54~RA56

Change RA54 package to 0603
Michael 2010/11/18

60 mil

11/16 Change CA5,CA8,CA11,CA13,CA17,CA18,CA19,CA23,CA25, package from 0805 to 0603
11/17 Change CA13 CA17 CA18 package from 0603 to 0805

9/6 Update QA2 symbol
10/11 Change RA40 to 0 ohm (1206)
10/12 Change RA40 to 0.1 ohm (1206)
12/08 Change RA40 to 0 ohm (1206) Tock

Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Internal AMIC
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

10/26 Remove SPKR+ SPKR- function

10/28 Reserve CA57 CA58 for EMI

11/01 Change CA57, CA58 from @ to mount

Remove CA57 , CA58
Tock 2010/11/29

Add INT Mic circuit on port F
Tock 2010/11/26

change RA17 from 0 ohm to 100 ohm
Tock 2011/01/03

9/1 Add CA49 RA41 on HP_SENSE

08/31 Reserve CA48(22P) on HDA_SDOUT_AUDIO

9/6 UA1 Pin 1 link to GNDA
9/7 Change UA1 Pin1 to GND
9/13 Add RA49 for DMIC
9/13 Add RA50~RA53 for DMIC
10/01 Remove RA50,R52

Layout Note: close to UA1

Add net GPIO_0 by vender review
Tock 2011/01/03

9/7 Add 0.1U (CA50) between GND & GNDA

Remove RA36,RA37,RA38,RA39
Add CA51,CA52,CA53,CA54
by vender review
Tock 2010/12/08

10/11 Update UA1 PN:SA000034020
10/12 Update UA1 PN:SA000034010 (-11Z)
12/08 Update UA1 PN:SA000034020 (-21Z) Tock

Add INT Mic circuit on port F
Tock 2010/11/26

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

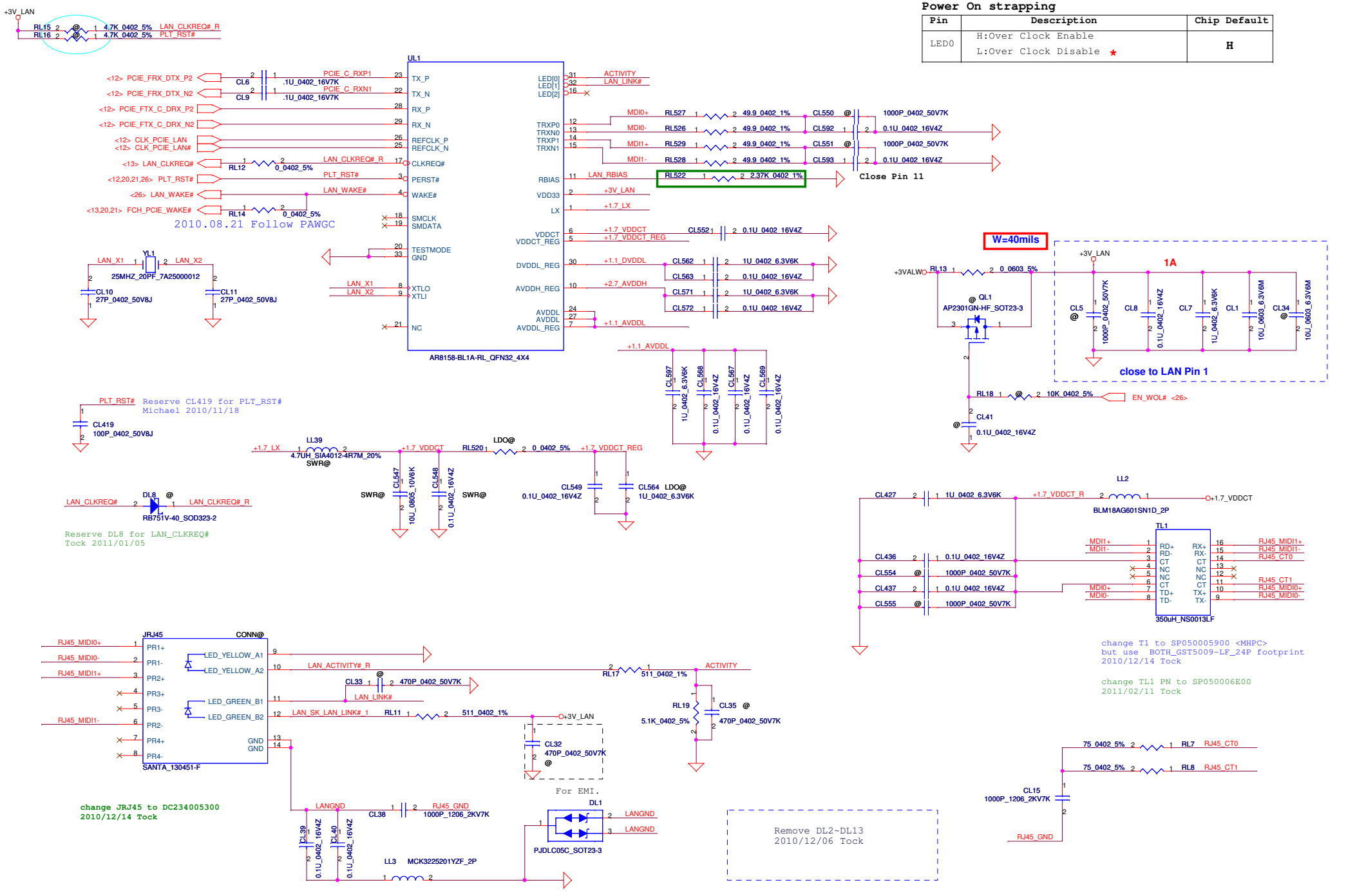
Title: Audio Codec CX20584

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

Date: Thursday, March 17, 2011 | Sheet 17 of 37

Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H



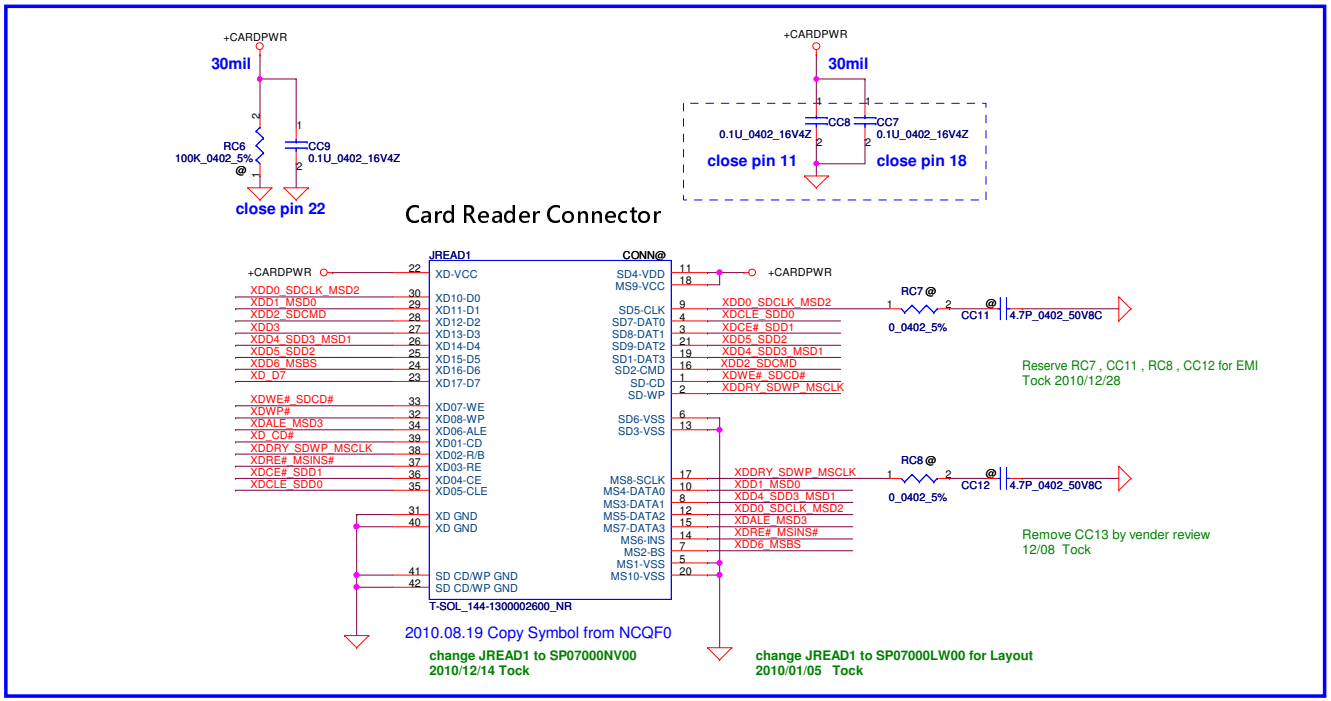
Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

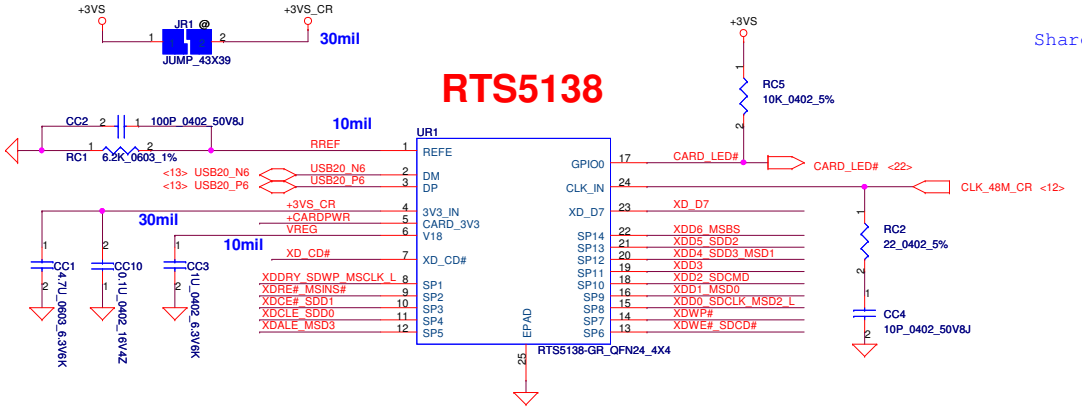
Title: LAN AR8158

Size	Document Number	Rev
Custom	P1VE6 Schematics	1.0

Date: Thursday, March 17, 2011 Sheet 18 of 37



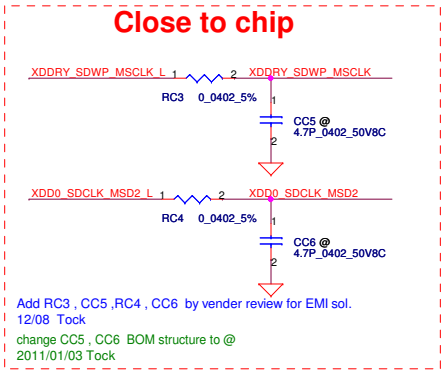
2010.11.02 Del LED circuit



Share Pin

	XD	SD	MS
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE		MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP		
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1		MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3		
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

Change net name from XDD5_SDD2_MS_D5 to XDD5_SDD2
11/26 Tock



Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: CARD READER RTS5138

Size	Document Number	Rev
Custom	P1VE6 Schematics	1.0

Date: Thursday, March 17, 2011 Sheet 19 of 37

Mini-Express Card for WWAN

+1.5VS — 3G@ R335 0_0805_5% — +1.5VS_WWAN

W=40mil

+1.5VS_WWAN: 3G@ C263 0.1U_0402_16V4Z; 3G@ C264 0.01U_0402_25V7K; 3G@ C265 47P_0402_50V8J; 3G@ C266 4.7U_0603_6.3V6K

W=40mil

+3VS_WWAN: 3G@ C268 0.1U_0402_16V4Z; 3G@ C269 0.01U_0402_25V7K; 3G@ C270 0.1U_0402_16V4Z; 3G@ C271 0.01U_0402_25V7K; 3G@ C272 47P_0402_50V8J <21,26> BT_ON#; 10U_0805_10V6K

C293 22P_0402_50V8J @

Reserve C293 for RF
Tock 2010/12/28

8/31 Change MCP@ to 3G_MP@

8/22 Reserve R335 (0 ohm 0805) Add net +1.5VS_WWAN

8/25 Change C269,C275 to SE000004880 Standard Part

10/04 Add 100p(C402) on BT_ON#

+3VS: C267 BT@ 0.1U_0402_16V4Z

R226 BT@ 10K_0402_5%

BT@ C402 100P_0402_50V8J

9/3 Reserver +3VALW for BT (R378 R374)

2011/02/11 Change Q13 PN to SB000006R10

+3VALW +3VS: R374 0_0603_5% @; BT@ R378 0_0603_5%

Q13 BT@ AO3413L_SOT23-3

+3VS_BT: C273 BT@ 0.1U_0402_16V4Z

BT MODULE CONN

Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T 06/29

10/27 Add R412 (0 ohm) on FCH_PCOE_WAKE#

9/2 Change ICH_PCIE_WAKE# to FCH_PCIE_WAKE#

+3VS: 3G@ R227 0_1206_5%

+3VS_WWAN: @ R228 0_1206_5%

+3VALW

+3VS_WWAN: @ C274 150U_B_6.3VM_R40M

Close to WWAN CONN

8/26 Change Q13 to SB934130020 Standard Part

JMINI1 CONN@

<13,18,21> FCH_PCIE_WAKE# — FCH_PCIE_WAKE# — @ R412 0_0402_5%

<13> WWAN_CLKREQ# — WWAN_CLKREQ#

<12> CLK_PCIE_WWAN# / <12> CLK_PCIE_WWAN

<12> PCIE_FRX_DTX_N1 / <12> PCIE_FRX_DTX_P1

<12> PCIE_FTX_C_DRX_N1 / <12> PCIE_FTX_C_DRX_P1

+3VS_WWAN — C275 10U_0805_10V6K 3G@ — WWAN_WAKEUP_R#

+UIM_PWR, UIM_DATA, UIM_CLK, UIM_RST, UIM_VPP

+1.5VS_WWAN

WXMIT_OFF# — R229 3G@ 0_0402_5% — WXMIT_OFF# <26>, PLT_RST# <12,18,21,26>

10/04 Add 100p(C398) on UIM_RST

10/06 Remove C398

R230 3G@ 0_0402_5% — FCH_SMCLK0 <7,8,13,21>

R231 3G@ 0_0402_5% — FCH_SMDAT0 <7,8,13,21>

USB20_MINI_N, USB20_MINI_P

WLAN_LED# R — R232 3G@ 0_0402_5% — WWAN_LED# <21,22>, WLAN_LED# <21,22>

(9~16mA)

PLAST_SSM010-52-B-K

JBT1: USB20_P7 <13>, USB20_N7 <13>; ACES_88266-04001 CONN@

9/1 Change R230 R231 from NON3G@ to mount

8/22 Update JBT1 Symbol from database (ACES_88266-04001_4P)

USB20_MINI_N — R246 @ 0_0402_5% — USB20_N3 <13>

USB20_MINI_P — R248 @ 0_0402_5% — USB20_P3 <13>

USB20_MINI_P — R250 3G@ 0_0402_5% — USB20_P9 <13>

USB20_MINI_N — R252 3G@ 0_0402_5% — USB20_N9 <13>

9/9 Remove D9

change JMIN1 to SP07000QC00
2010/12/14 Tock

10/31 Add R417~R420 for co-lay USB port3 & port9

11/01 Change R417 R418 from mount to @
Change R419 R420 from mount to @ SW request (P0VE6-0045)

Change R417, R418 to RP9 Michael 2010/12/23

Change R419, R420 to RP10 Michael 2010/12/23

Swap USB net of RP10 for layout
Tock 2010/12/24

Change RP9 to R246 , R248 Tock 2010/12/30

Change RP10 to R250 , R252 Tock 2010/12/30

C282 3G@ 1U_0402_6.3V6K +UIM_PWR

C283 3G@ 0.1U_0402_16V4Z

C284 3G@ 56P_0402_50V8

C285 3G@ 56P_0402_50V8

C278 3G@ 100P_0402_50V8J UIM_RST

C279 @ 22P_0402_50V8J

C280 @ 22P_0402_50V8J UIM_CLK

C281 3G@ 22P_0402_50V8J

W=20mil

JSIM1: +UIM_PWR, UIM_RST, UIM_CLK, <13> USB20_P4, UIM_VPP, UIM_DATA, <13> USB20_N4, +UIM_PWR

VCC, RST, CLK, Reserved, GND, VPP, I/O, Reserved, CD, GND, GND

3G@ C276 56P_0402_50V8; @ C277 22P_0402_50V8J

R233 @ 10K_0402_5%

ACON_SCR4W-8K1000 CONN@

change JSIM1 to SP07000NW00
2010/12/28 Tock

PLT_RST# — 3G@ C479 100P_0402_50V8J

9/1 Change R234 from mount to @

+3VALW — R234 10K_0402_5% @ — <26> WWAN_WAKEUP# — R235 @ 0_0402_5% — WWAN_WAKEUP_R#

Modifiy 05/11

Reserve for SIM card does not meet rise time and pull-up is needed.

8/22 Update JP1 Symbol from database (TAITW_PMPAT7-08GLBS1N14H0_9P)

10/06 Change C278 to 100p

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: Mini-Card/BT CONN

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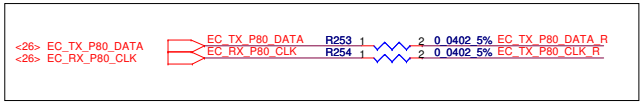
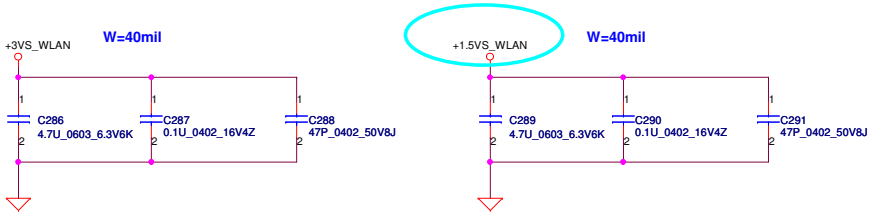
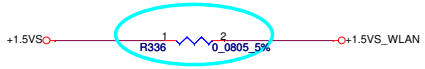


Mini-Express Card for WLAN

Change R236, R237 to RP11
Michael 2010/12/23

Change RP11 to R253 , R254
Michael 2010/12/30

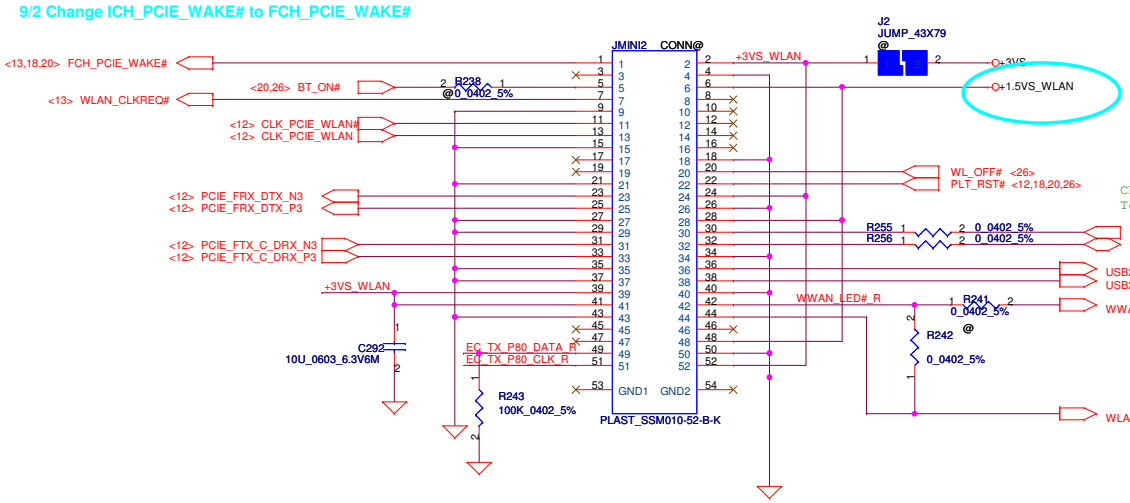


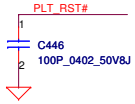


8/22 Reserve R336 (0 ohm 0805) Add net +1.5VS_WLAN

change JMIN2 to SP07000QC00
2010/12/14 Tock

9/2 Change ICH_PCIE_WAKE# to FCH_PCIE_WAKE#





Add C446 on PLT_RST# for switching noise
Tock 2010/12/28

Change RP12 to R255 ,R256
Tock 2010/12/30

9/20 Add R393 R394 for SMBus

9/17 Remove R239,R240

(9~16mA)

5/12 Update WLAN connector(the same as KAV60)
6/1 Revised 37、39、41、42、43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

Compal Electronics, Inc.			
Title: WLAN	WLAN		
Size: Custom	Document Number: P1VE6 Schematics	LA-6222P	Rev: 1.0
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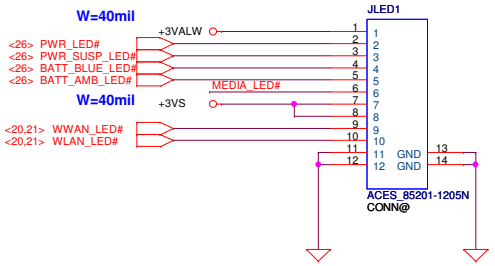
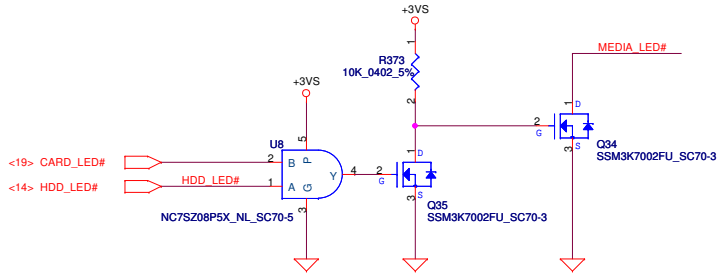
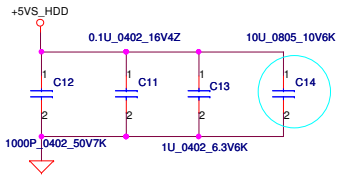
LED PCB CONN





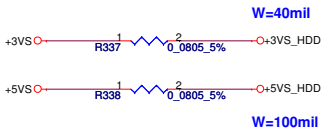
8/22 Update JP2 Symbol from database (ACES_85201-1605N_16P)
8/24 Update JLED1 Symbol from database (ACES_85201-1205N_12P) & Update pin definition
9/1 Add LED Circuit (LED2~4(SC597UDB000)LED5(SC5191NB000), R360~R369, Q33)
9/1 Change All LED power to 5V
9/9 Change LED2~4 footprint to LED_HT-297DQ-GQ_4P
9/11 Remove LED portion

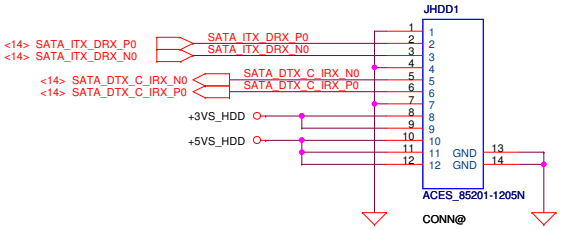
9/1 Add R373, Q34, Q35 for MEDIA_LED#



Add C11~C14 from HDD board
2011/01/07 Tock

SATA HDD Conn.





8/22 Change C298 from 10U 6.3V to 10U 10V
8/22 Reserve R337 R338 Add net +3VS_HDD,+5VS_HDD
9/1 Change Q33 to SB000009610(SSM3K7002FU_SC70-3)
change JHDD1 to SP01000E400 , delete C293 ~ C298
2010/12/14 Tock

Modify JHDD1 pin define
2010/12/15 Tock

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: SATA CONN./LED/B CONN./BATT CONN.

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B	P1VE6 Schematics	1.0

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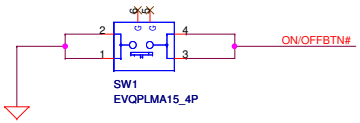
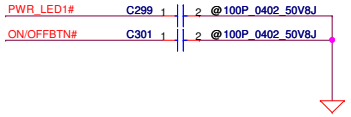
ON/OFF Button

updated SW1 symbol for SN100002K00
2010/12/06 Tock



FOR EMI



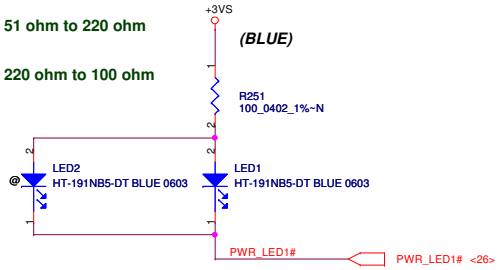
9/6 Change D13 from mount to @
10/05 Remove D13

9/1 Remove LED2 LED3 circuit, Change 70@ to mount

9/20 Add LED2 LED3 Circuit
9/21 Remove LED2 LED3 Circuit

change R251 from 51 ohm to 220 ohm
2011/03/07 Tock

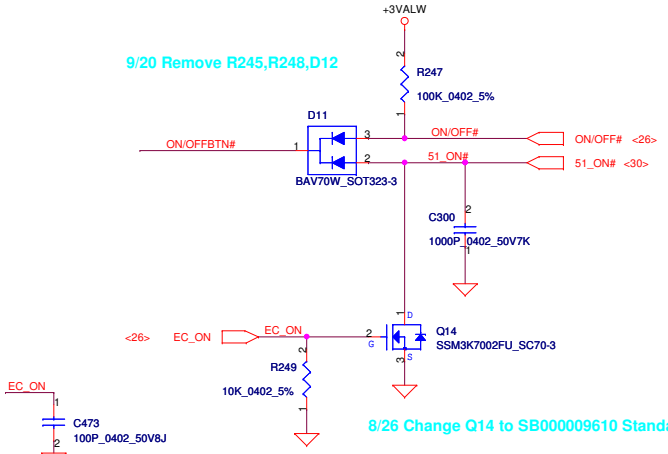
change R251 from 220 ohm to 100 ohm
2011/03/16 Tock

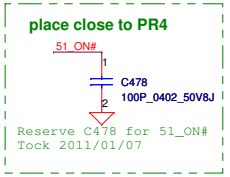


10mil

8/26 Change D11 to SC600000B00 Standard Part

9/20 Remove R245,R248,D12

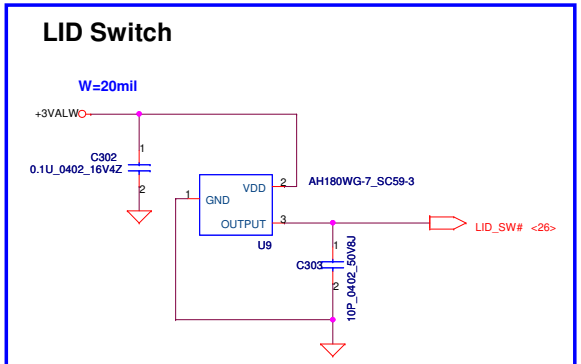




8/26 Change Q14 to SB000009610 Standard Part

9/24 Change U9 to SA00001TC00

LID Switch



Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: ON/OFF / PWR SW/ LID SW

Size	Document Number	Rev
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Change CP1 to C398 , C419 , C448 , C449
Change CP2 to C453 , C450 , C452 , C451
Change CP3 to C457 , C454 , C456 , C455
Tock 2010/12/30

Change CP4 to C461 , C458 , C460 , C459
Change CP5 to C465 , C462 , C464 , C463
Change CP6 to C469 , C466 , C468 , C467
Tock 2010/12/30

KSO15 C398 100P_0402_50V8J
KSO14 C419 100P_0402_50V8J
KSO13 C448 100P_0402_50V8J
KSO12 C449 100P_0402_50V8J

KSO7 C461 100P_0402_50V8J
KSO6 C458 100P_0402_50V8J
KSO5 C460 100P_0402_50V8J
KSO4 C459 100P_0402_50V8J

KSI7 C453 100P_0402_50V8J
KSO11 C450 100P_0402_50V8J
KSO10 C452 100P_0402_50V8J
KSI6 C451 100P_0402_50V8J

KSO3 C465 100P_0402_50V8J
KSI3 C462 100P_0402_50V8J
KSO2 C464 100P_0402_50V8J
KSO1 C463 100P_0402_50V8J

KSI5 C457 100P_0402_50V8J
KSO9 C454 100P_0402_50V8J
KSI4 C456 100P_0402_50V8J
KSO8 C455 100P_0402_50V8J

KSO0 C469 100P_0402_50V8J
KSI2 C466 100P_0402_50V8J
KSI1 C468 100P_0402_50V8J
KSI0 C467 100P_0402_50V8J

Swap KB signal for layout
Tock 2010/12/24

JKB1
KSI0 KSI1 KSI2 KSO0 KSO1 KSO2 KSI3 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSI4 KSO9 KSI5 KSI6 KSO10 KSO11 KSI7 KSO12 KSO13 KSO14 KSO15
G2 G1
ACES_85202-24051
CONN@

KSI[0..7] KSI[0..7] <26>
KSO[0..15] KSO[0..15] <26>

8/22 Update JKB1 Symbol from database (ACES_85202-24051_24P)
8/23 Update KB pin definition

INT_KBD Conn.

To TP/B Conn.

8/22 Update JP3 Symbol from database (ACES_85201-0605N_6P)
8/22 Reserve R339 (0 ohm 0402) Add Net name +5VS_TP
8/24 Update JTP1 Symbol from database (ACES_85201-0405N_4P)
& Update pin definition

W=20mil

<26> TP_DATA
<26> TP_CLK
+5VS
0_0402_5%
R339
TP_DATA
TP_CLK
+5VS_TP
D14
@
PJDLC05C_SOT23-3
JTP1
G1 G2
ACES_85201-0405N
CONN@

Combo Jack

+LDO_OUT_3.3V
RA14 CMBS@ 0_0402_5%
CA25 10U_0805_10V6K @
COM_MIC_R
CMBS@ QA36 MMBT3906H_SOT23-3
RA35 2.2K_0402_5% NCMBS@
CMBS@ RA30 100K_0402_5%
RA59 220_0402_5% CMBS@
RA13 CMBS@ 2K_0402_5%
COM_MIC
COM_MIC <17>
CA28 10U_0805_10V6K CMBS@
RA57 15K_0402_1% CMBS@
CMBS@ RA50 10K_0402_5%
<17> GPIO_0
DA10 CMBS@ RB491D_SC59-3
HP_SENSE
RA52 100K_0402_5% CMBS@
QA3 CMBS@ BSS138_NL_SOT23-3
RA58 270K_0402_5% CMBS@
CA26 1U_0603_10V6K CMBS@

change RA59 from 750 to 220 ohm
by vender review for bo bo noise
Tock 2011/03/16

Add RA58 for net GPIO_1
by vender review for pop issue
Tock 2010/12/08

change GPIO_1 to GPIO_0
Tock 2011/01/03

change RA57 from 47K to 15K ohm
by vender review for bo bo noise
Tock 2011/03/16

change RA12 BOM structure to @
by vender review for pop issue
Tock 2010/12/08

RA14
1K_0402_5%
NCMBS@

change RA52,DA10,CA26 BOM structure to @
by vender review for pop issue
Tock 2010/12/08

11/17 Add Combo solution circuit for P0VE6 "POPO" noise

11/17 Move HP JACK and MIC JACK Circuit to IO Board.

Add net INT_MIC0 on JIO1 pin 2
Tock 2010/11/26

<17> INT_MIC0
<17> MIC1_L
<17> MIC1_R
+MIC1_VREFO
<17> MIC_PLUG#
<17> COM_MIC
<17> HP_LEFT
<17> HP_RIGHT
HP_SENSE
+5VS
<25,26> USB_ON#
+5VALW
<13> USB_OC0#
<13> USB20_P0
<13> USB20_N0
<13> USB20_P1
<13> USB20_N1
JIO1
CONN@
ACES_85202-24051

Add IO connector
Michael 2010/11/18

change RA9 from 20K to 0 ohm
Tock 2011/03/03

COM_MIC_PLUG#
COM_MIC_PLUG# <17>
RA9 0_0402_5%
QA1A 2N7002KDWH_SOT363-6
HP_PLUG#
HP_PLUG# <17>
HP_SENSE
RA36 0_0402_5%
QA1B 2N7002KDWH_SOT363-6
RA41 20K_0402_5%
CA49 @ 0.1U_0402_16V4Z
QA4 BSS138_NL_SOT23-3
RA55 10K_0402_5%
COM_MIC
CA29 1U_0603_10V6K

Add QA4,RA55,CA29,RA36 for Internal Mic
can't record issue . Tock 2011/02/21

remove CA4 change QA1 , QA2 from SB501380020 <BSS138> to SB00000E010 <2N7002>. Tock 2011/02/24

change CA49 BOM structure to @
change RA41 from 47K to 4.7K
by vender review for pop issue
Tock 2010/12/08

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: KB Conn/TP/IO Conn

Size: B | Document Number: P1VE6 Schematics | Rev: 1.0

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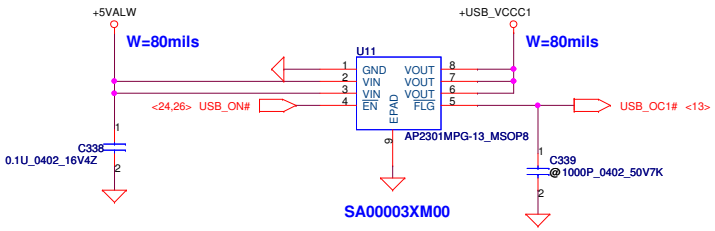
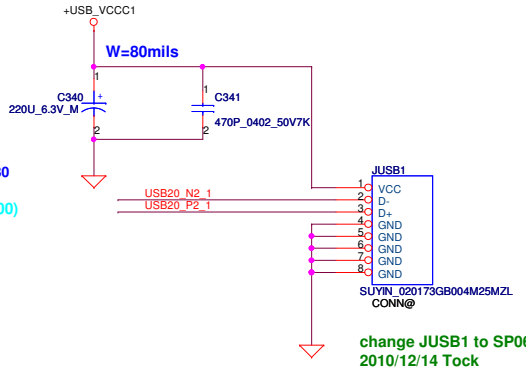
11/17 Move Left Side USB CONN. Circuit to IO board

Right Side USB CONN.

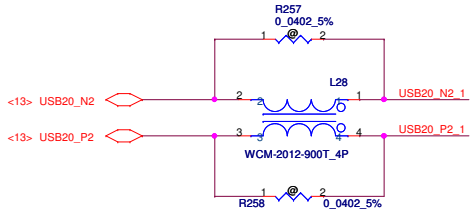


Change C340 to SF000001500
2010/12/14 Tock



change JUSB1 to SP060004B00
2010/12/14 Tock

9/28 Swap L28



8/25 Change C340 from poly-cap to E-cap (SF000001500)

delete D17 for DFB issue
2011/02/25 Tock

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: USB PORTS

Size: B | Document Number: P1VE6 Schematics | Rev: 1.0

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place close to PU4 and PU7

SUSP# C475 100P_0402_50V8J C476 100P_0402_50V8J

Reserve C475,C476 for SUSP#
Tock 2011/01/07

@C349 22P_0402_50V8J @R265 33_0402_5% LPC_CLK0_EC

PLT_RST# C420 100P_0402_50V8J

Reserve C420 for PLT_RST#
Michael 2010/11/18

+3VALW R267 47K_0402_5% EC_RST# C350 0.1U_0402_16V4Z

+3VALW 10/1 ENE Recommand

R269 47K_0402_5% KSO1
R270 47K_0402_5% KSO2
R271 @ 1K_0402_5% EC_SMI#
R266 2.2K_0402_5% EC_SMB_DA1
R272 2.2K_0402_5% EC_SMB_CK1

C353 10P_0402_50V8J R275 22_0402_5%

Reserve for EMI please close to U12

+3VS +3VALW
R276 @ 2.2K_0402_5% EC_SMB_CK2
R277 @ 2.2K_0402_5% EC_SMB_DA2
R279 @ 10K_0402_5% EC_SCI#

8/31 EC_SCI# Pull up to +3VALW
8/23 Delete R280

Reserve C436, C437 for SMB
Michael 2010/11/18

EC_SMB_CK2 @C436 100P_0402_50V8J EC_SMB_DA2 @C437 100P_0402_50V8J

C407 @ 100P_0402_50V8J APU_ALERT# EC

10/05 Add 100p(C407) on APU_ALERT# EC

EC_XCLK1 EC_XCLK0
C354 15P_0402_50V8J C355 15P_0402_50V8J
X1 32.768KHZ_12.5PF_Q13MC14610002

8/23 Change R282 from mount to @
X1 C354 C355 from @ to mount
8/26 Change R282 from @ to mount
X1 C354 C355 from mount @

10/11 Change C354,C355, X1 from @ to mount

Board ID
Analog Board ID definition,
Please see page 3.

+3VALW
Ra R283 100K_0402_5%
AD_BID0
Rb R284 8.2K_0402_5% C357 0.1U_0402_16V4Z

change R284 from 0 ohm to 8.2K , 2011/01/28 Tock
change R283 from 0 ohm to 100K , 2011/02/11 Tock

8/21 Change R262 from 0 ohm 0805 to 0 ohm 0603

+3VALW R262 0_0603_5% +3VALW_EC
W=40mils
C342 0.1U_0402_16V4Z C343 0.1U_0402_16V4Z C344 0.1U_0402_16V4Z C345 0.1U_0402_16V4Z C346 1000P_0402_50V7K C347 1000P_0402_50V7K

L29 FBMA-L11-160808-800LMT_0603 +EC_VCCA
W=20mils
C348 0.1U_0402_16V4Z ECAGND

U12

11/02 Change C353 to 10p R275 to 22 ohm

8/23 Change R271 R279 from mount to @

<24> KSI[0..7] KSI[0..7]
<24> KSO[0..15] KSO[0..15]

9/5 Change R276 R277 from mount to @

8/25 Delete KSO16 KSO17

Battery
APU

8/24 Delete Net FAN_SPEED1

8/23 Change R282 from mount to @
8/26 Change R282 from @ to mount

R282 @ 0_0402_5% EC_XCLK1 EC_XCLK0
<12> SUSCLK R358 @ 100K_0402_5%

8/31 Add 100k(R358) pull-down on SUSCLK

10/11 Change R282 R358 from mount to @

SLP_S3# @C424 100P_0402_50V8J
SLP_S5# @C425 100P_0402_50V8J
ON/OFF# C428 100P_0402_50V8J

Reserve C424, C425, for SLP_S3#, SLP_S5# Michael 2010/11/18

Reserve C428 for ON/OFF# Michael 2010/11/18

KB930QF-A1_LQFP128_14X14
SA00003QQ10

8/23 Pull up 10k (R345) to +3VALW on USB_ON#
8/31 Change EC_MUTE# Pull-up to +3VS(@)

Reserve C403, C443, C444 for ADP_I, TP_CLK, DATA
Michael 2010/11/18

ADP_I @C403 100P_0402_50V8J
TP_CLK @C443 100P_0402_50V8J
TP_DATA @C444 100P_0402_50V8J

+3VS +3VALW
EC_MUTE# R259 @ 10K_0402_5%
USB_ON# R345 10K_0402_5%

+5VS
TP_CLK R263 4.7K_0402_5%
TP_DATA R264 4.7K_0402_5%

8/26 Change D18 to SCS00002G00 Standard Part
9/23 Reserve R395 on ACIN
10/08 Change D18 to SCS00000Z00

+3VALW R268 200K_0402_5%
D18 RB751V-40_SOD323-2
ACIN <31>
EC_ACIN C352 100P_0402_50V8J
R395 @ 0_0402_5%

9/23 Update EC pin definition follow P5WE6
10/04 Add 100p(C399) on ACOFF

Delete EC_FAN_PWM Tock 2011/01/28

ACOFF C399 100P_0402_50V8J

8/23 Delete DAC_BRIG
8/25 Delete CHG_ON#
8/31 Add EN_FAN1 on U12.70

Follow PAWGC

D19 @ RB751V-40_SOD323-2
ICH_POK_EC ICH_POK <13>
R273 0_0402_5% R274 @ 10K_0402_5% +3VS

LID_SW# C470 220P_0402_50V7K

Reserve C470 for LID_SW#
Tock 2011/01/07

9/25 Change VLDT_EN to VLDT_EN#

EDP_BIST @ R285 100K_0402_5%

Add EDP_BIST and Reserve C390 , R285
Tock 2010/12/30

+3VALW LID_SW# R278 100K_0402_5%

EDP_BIST R390 eDP@ 0_0402_5% DMIC_DATA
DMIC_DATA <9,17>

place close to PU2

FSTCHG C477 100P_0402_50V8J
VR_ON C400 100P_0402_50V8J
VGATE @ C423 100P_0402_50V8J

Reserve C477 for FSTCHG
Tock 2011/01/07

Reserve C423 for VGATE
Michael 2010/11/18

APU_ENBKL <4> R281 100K_0402_5% C447 100P_0402_50V8J

Reserve C447 for APU_ENBK
Tock 2011/01/07

PME Follow PAWGC

+3VALW
Ra R398 @ 0_0402_5%
AD_PID0
Rb R399 @ 8.2K_0402_5% C393 @ 0.1U_0402_16V4Z

+3VALW R322 10K_0402_5%
<18> LAN_WAKE# R323 @ 0_0402_5% EC_PME#
R324 @ 0_0402_5%
<13> PCI_PME# Q29 SSM3K7002FU_SC70-3 @
+3VALW

Project ID

EC_PROCHOT# C430 100P_0402_50V8J
LAN_WAKE# C471 100P_0402_50V8J
BKOFF# C472 100P_0402_50V8J

Reserve C430 for EC_PROCHOT# Michael 2010/11/18

Reserve C471,C472 for LAN_WAKE# , BKOFF# Tock 2011/01/07

10/27 Change C356 from 10V_0805 to 6.3V_0603

C356 4.7U_0603_6.3V6K

20mil L30 ECAGND FBMA-L11-160808-800LMT_0603

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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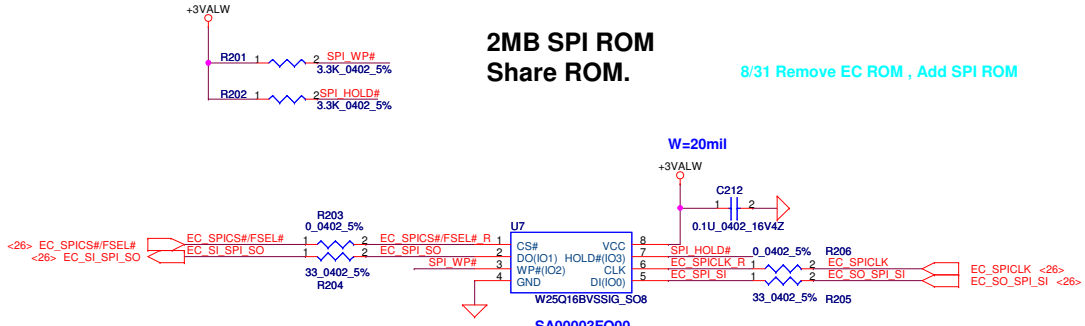
2MB SPI ROM
Share ROM.

8/31 Remove EC ROM , Add SPI ROM

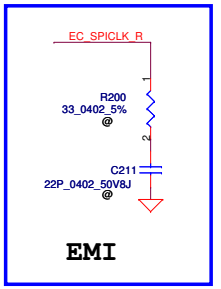


SA00003FO00

Layout Note:
R204 close to U7

Layout Note:
R203 R205 R206 close to U12

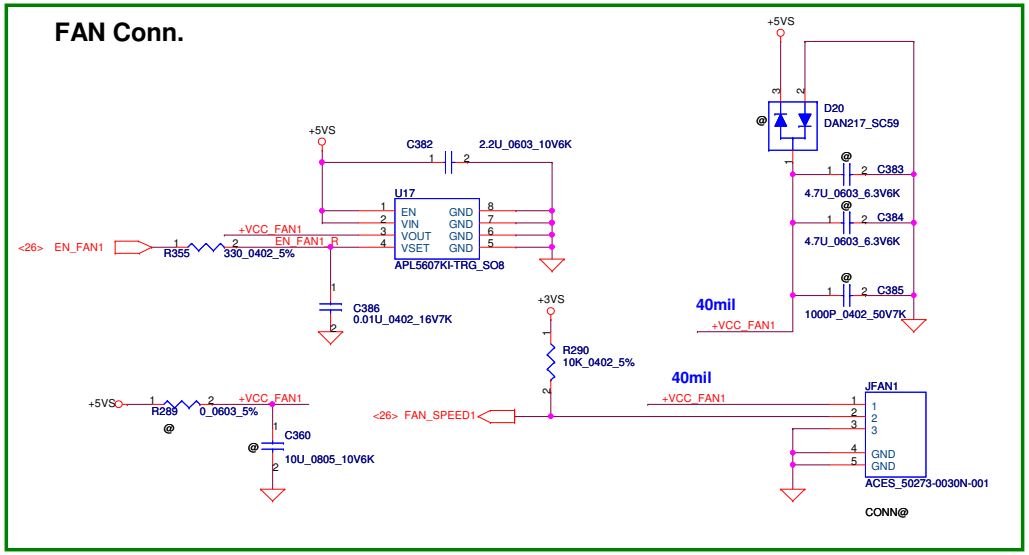
9/2 Change EC_SPICLK to EC_SPICLK_R



Delete U17,C382,C386,R355,D20,C383,C384,C385
for Fan control IC circuit
2010/12/15 Tock

Add U17,C382,C386,R355,D20,C383,C384,C385
for Fan control IC circuit
2011/01/19 Tock

FAN Conn.



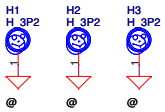
8/24 Update JFAN1 Symbol from database (ACES_85205-03001_3P) & Update pin definition
8/24 Delete R290

8/25 Update JFAN1 Symbol from database (ACES_85205-04001_4P) & Update pin definition
8/25 Add R290 10k pull-up tp +3VS

8/31 Reserve U17,C382~C386, R355~R357, D20 (Fan Drive Circuit)

change JFAN1 footprint from ACES_85205-04001_4P to ACES_50273-0030N-001_3P , 2011/01/28 Tock ,
delete EC_FAN_PWM and R356,R357 , 2011/01/28 Tock ,

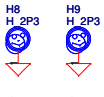
3P2 x 3 (APU)



3P0N x 1

9/15 Update the Screw Hole
9/20 Add H20 (H_3P4X3P2N)
10/07 Change H13 from GND to LANGND
10/07 Change H13 from LANGND to GND

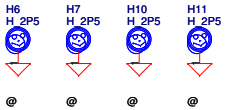
2P3 x 2

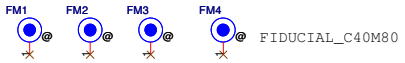


Update the Screw Hole
2010/12/16 Tock

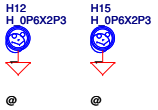
Update the Screw Hole
2010/12/22 Tock

2P5 x 4

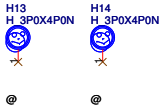




0P6X2P3 x 2



3P0X4P0N x 2



Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: Screw / EC ROM /FAN

Size	Document Number	Rev
B	P1VE6 Schematics	1.0

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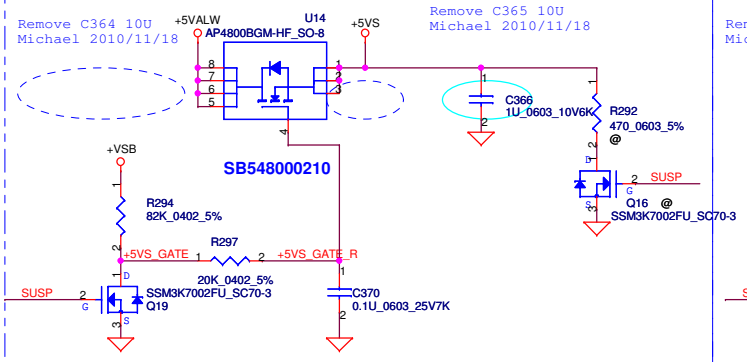
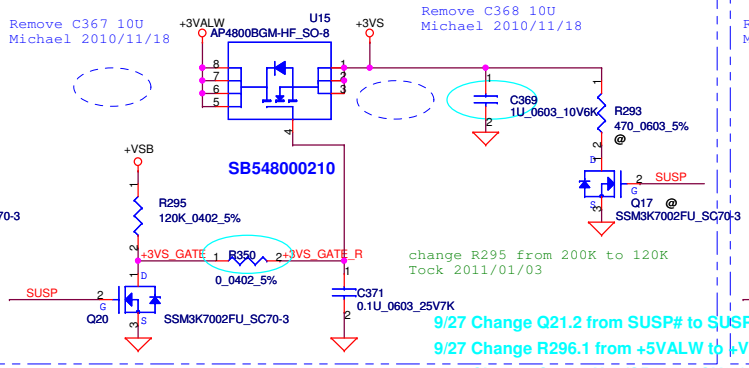
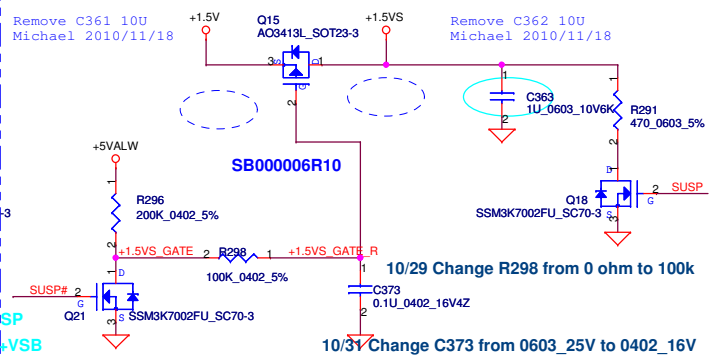
+5VALW TO +5VS



+3VALW TO +3VS



+1.5V to +1.5VS



10/27 Change R291 Q18 from @ to mount

10/29 Change R298 from 0 ohm to 100k

10/31 Change C373 from 0603_25V to 0402_16V

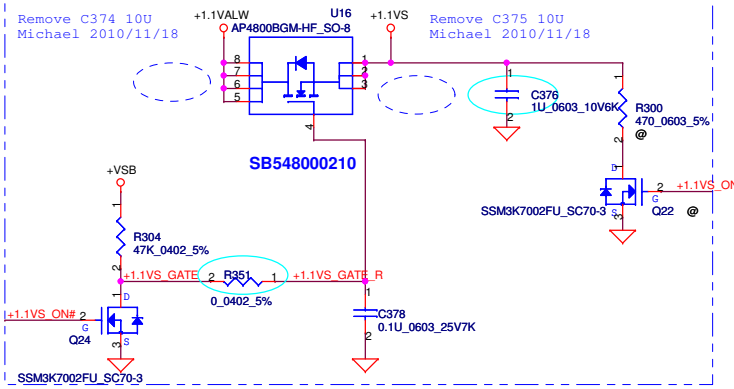
9/27 Change Q21.2 from SUSP# to SUSP

9/27 Change R296.1 from +5VALW to +VSB

9/27 Change Q15 to U19(SB00000GV00)

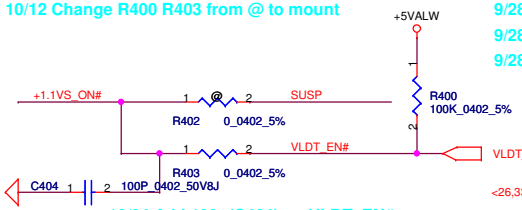
2011/02/11 Change Q15 to SB000006R10

+1.1ALW to +1.1VS



10/12 Change R402 from mount to @

10/12 Change R400 R403 from @ to mount



10/04 Add 100p(C404) on VLDT_EN#

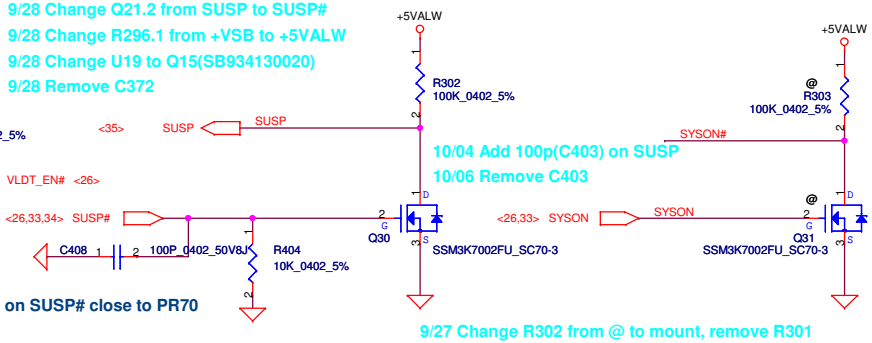
10/06 Change C404 on +1.1VS_ON#

9/28 Change Q21.2 from SUSP to SUSP#

9/28 Change R296.1 from +VSB to +5VALW

9/28 Change U19 to Q15(SB934130020)

9/28 Remove C372



10/27 Add C408(100P) on SUSP# close to PR70

9/27 Change R302 from @ to mount, remove R301

9/27 Change R304.1 from +5VALW to +VSB

10/12 Change R294 to 100k

10/12 Change R295, R296 to 200k

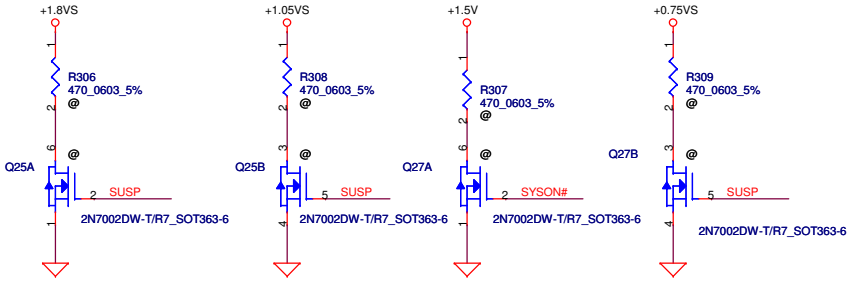
10/12 Change R304 to 47k

10/12 Change R294 to 82k

10/12 Change R297 to 20k

Change Q25 package to SOT363-6
Remove Q26
Michael 2010/11/18

Change Q27 package to SOT363-6
Remove Q28
Michael 2010/11/18



8/19 Change Q16~Q22 Q24~Q28 toSB000009610(SSM3K7002FU_SC70-3)

8/19 Change Q29 Q30 to Q23A Q23B (SB00000DH00 S TR DMN66D0LDW-7 2N SOT363-6)

8/21 Change U14~U16 to SB548000310 (SI4800BDY-T1-E3_SO8)

8/23 Remove R305 R299 Add R350 R351 for Sequence

8/24 Change Q23A Q23B to Q30 Q31(@) (SB000009610 SSM3K7002FU_SC70-3)

8/25 Change C363,C366,C369,C376 to SE080105K80 Standard Part

8/25 Change C361,C362,C364,C365,C367,C368,C374,C375 to SE000004880 Standard Part

8/26 Change U14, U15, U16 to SB00000GV00 Standard Part

9/3 Delete C377(DIS@)

9/23 Reserve R400~403, Q36 for VLDT_EN

9/25 Remove R401 Q36 on VLDT_EN

9/25 Add 10k(R404) PD on SUSP#

10/31 Change C361 C362 from mount to @

Security Classification	Compal Secret Data		
Issued Date	2010/11/09	Deciphered Date	2012/11/09

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: P1VE6 Schematics | Rev: 1.0

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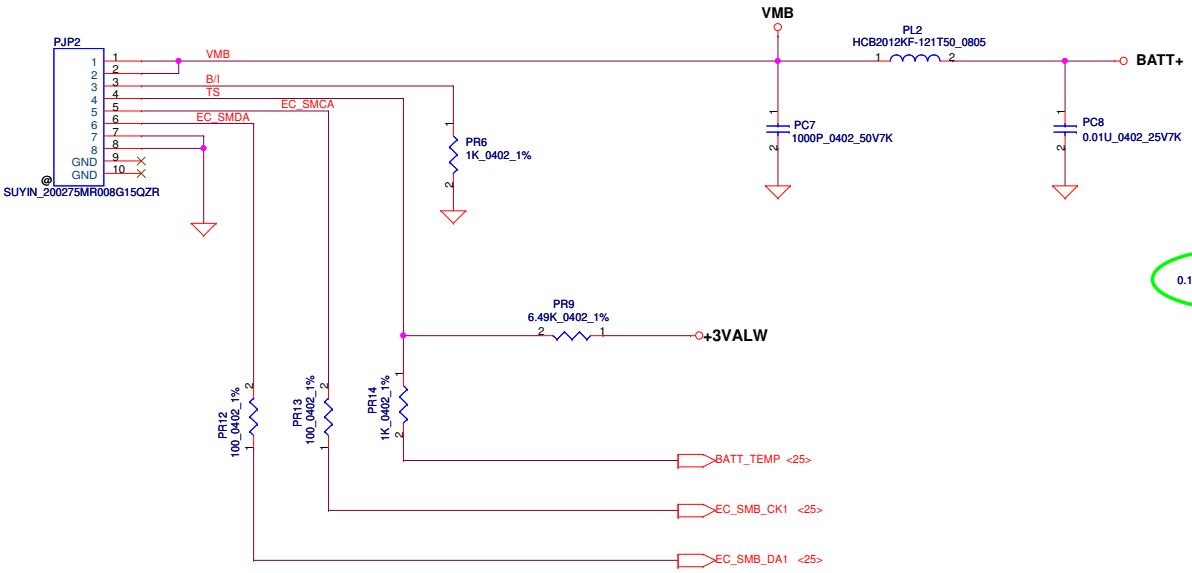
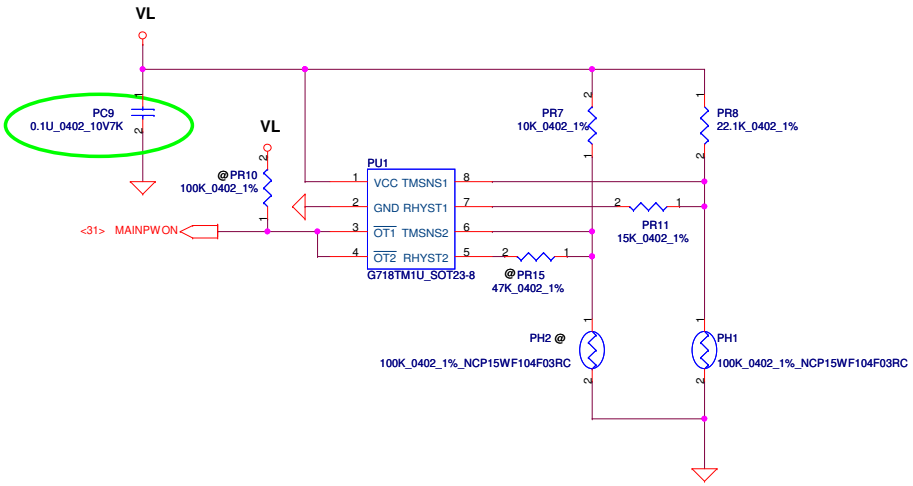
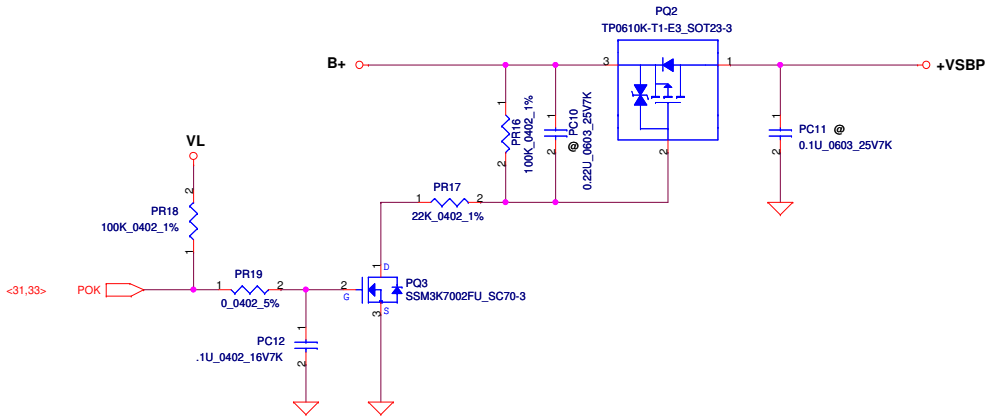


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 72 degree C





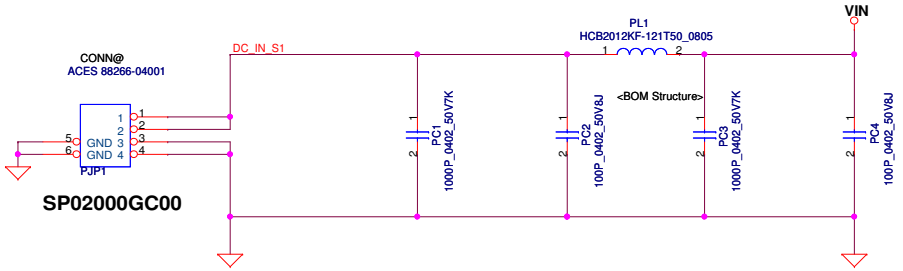
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

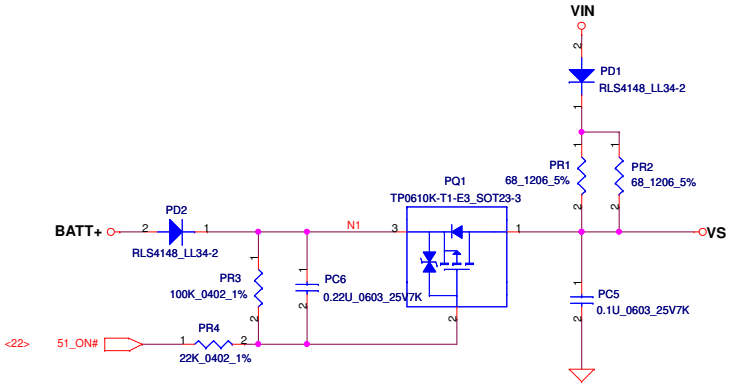
Compal Electronics, Inc.

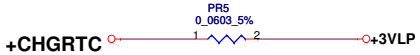
Title: BATTERY CONN / OTP

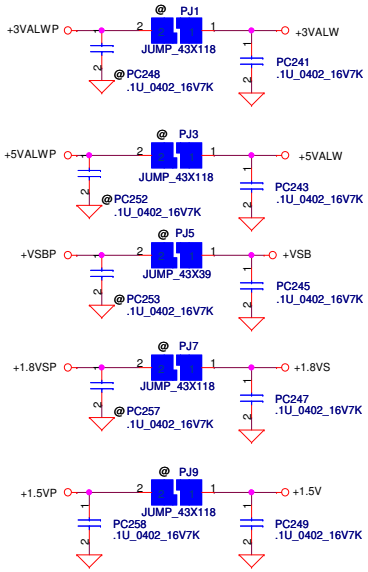
Size	Document Number	Rev
		1.0

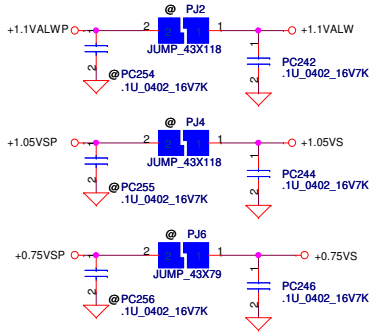
Date: Thursday, March 17, 2011 | Sheet 29 of 37











Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: DCIN/VIN DECTOR

Size	Document Number	Rev
		1.0

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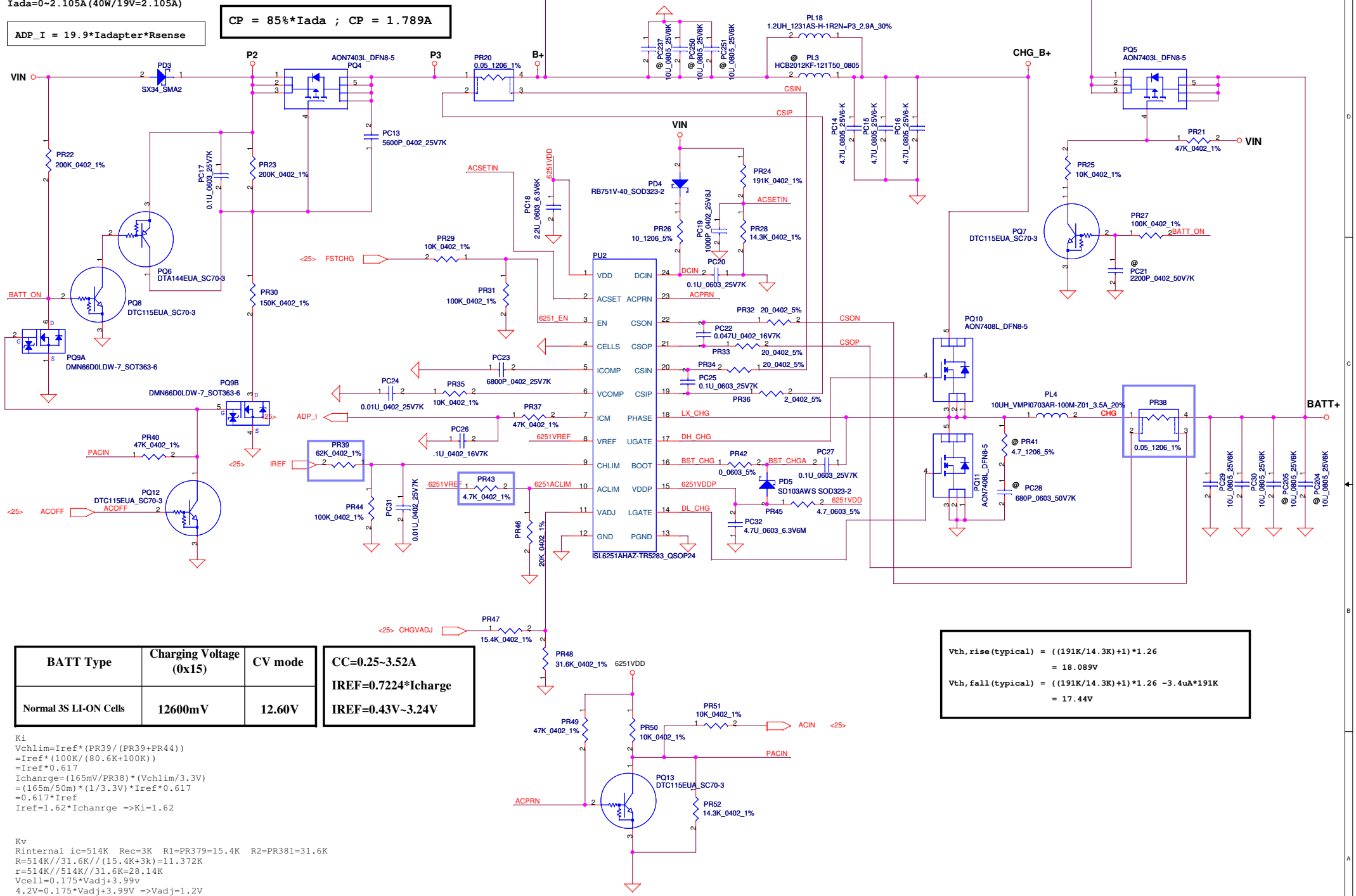
Iada=0~2.105A(40W/19V=2.105A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 1.789A



BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.25~3.52A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

```
Vth,rise(typical) = ((191K/14.3K)+1)*1.26
                  = 18.089V
Vth,fall(typical) = ((191K/14.3K)+1)*1.26 -3.4uA*191K
                  = 17.44V
```

Ki

```
Vchlim=Iref*(PR39/(PR39+PR44))
=Iref*(100K/(80.6K+100K))
=Iref*0.617
Ichanrge=(165mV/PR38)*(Vchlim/3.3V)
=(165m/50m)*(1/3.3V)*Iref*0.617
=0.617*Iref
Iref=1.62*Ichanrge =>Ki=1.62
```

Kv

```
Rinternal ic=514K  Rec=3K  R1=PR379=15.4K  R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451
```

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		1.0

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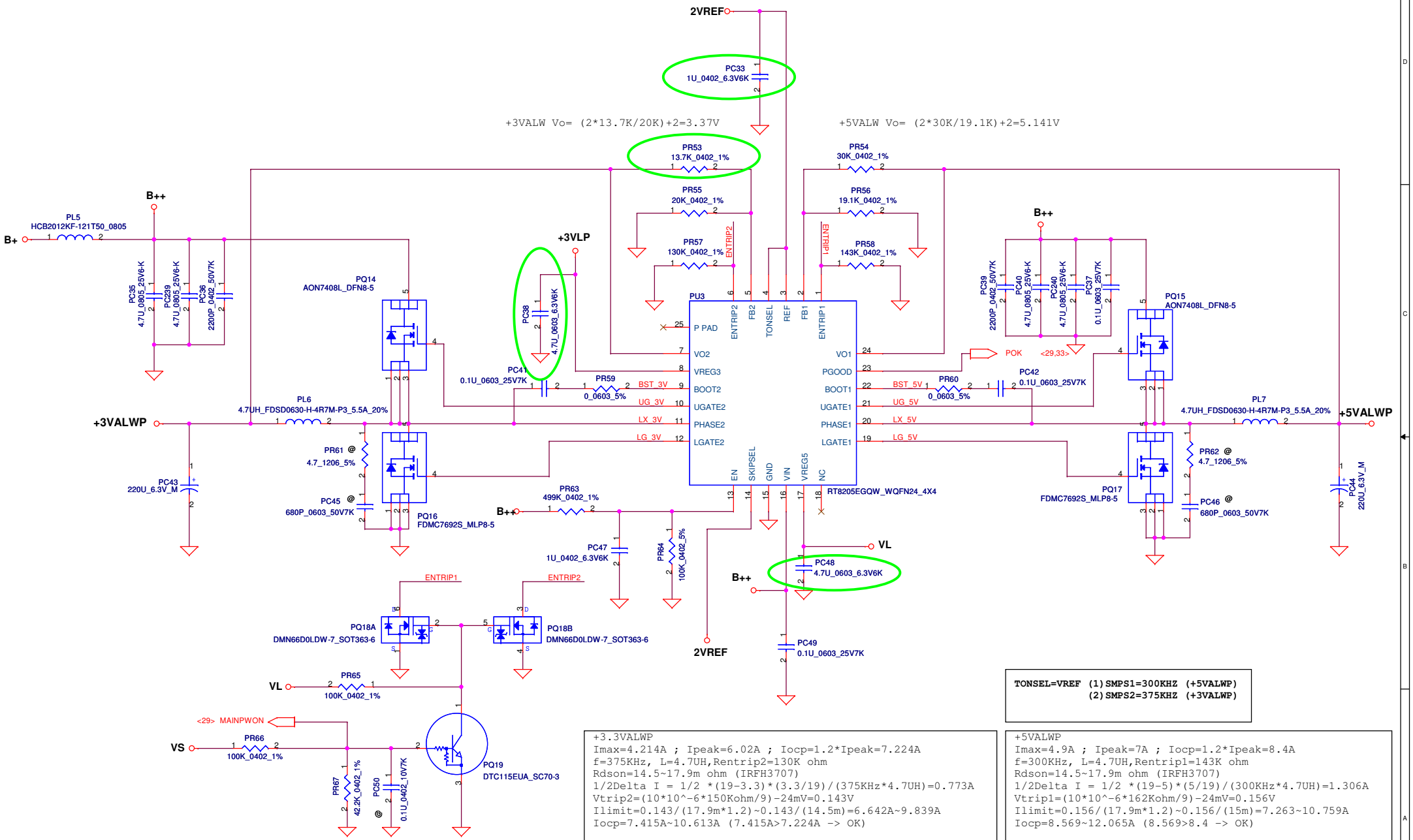


TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ (+3VALWP)

+3.3VALWP
Imax=4.214A ; Ipeak=6.02A ; Iocp=1.2*Ipeak=7.224A
f=375KHz, L=4.7UH,Rentrip2=130K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 *(19-3.3)*(3.3/19)/(375KHz*4.7UH)=0.773A
Vtrip2=(10*10^-6*150Kohm/9)-24mV=0.143V
Ilimit=0.143/(17.9m*1.2)~0.143/(14.5m)=6.642A~9.839A
Iocp=7.415A~10.613A (7.415A>7.224A -> OK)

+5VALWP
Imax=4.9A ; Ipeak=7A ; Iocp=1.2*Ipeak=8.4A
f=300KHz, L=4.7UH,Rentrip1=143K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vtrip1=(10*10^-6*162Kohm/9)-24mV=0.156V
Ilimit=0.156/(17.9m*1.2)~0.156/(15m)=7.263~10.759A
Iocp=8.569~12.065A (8.569>8.4 -> OK)

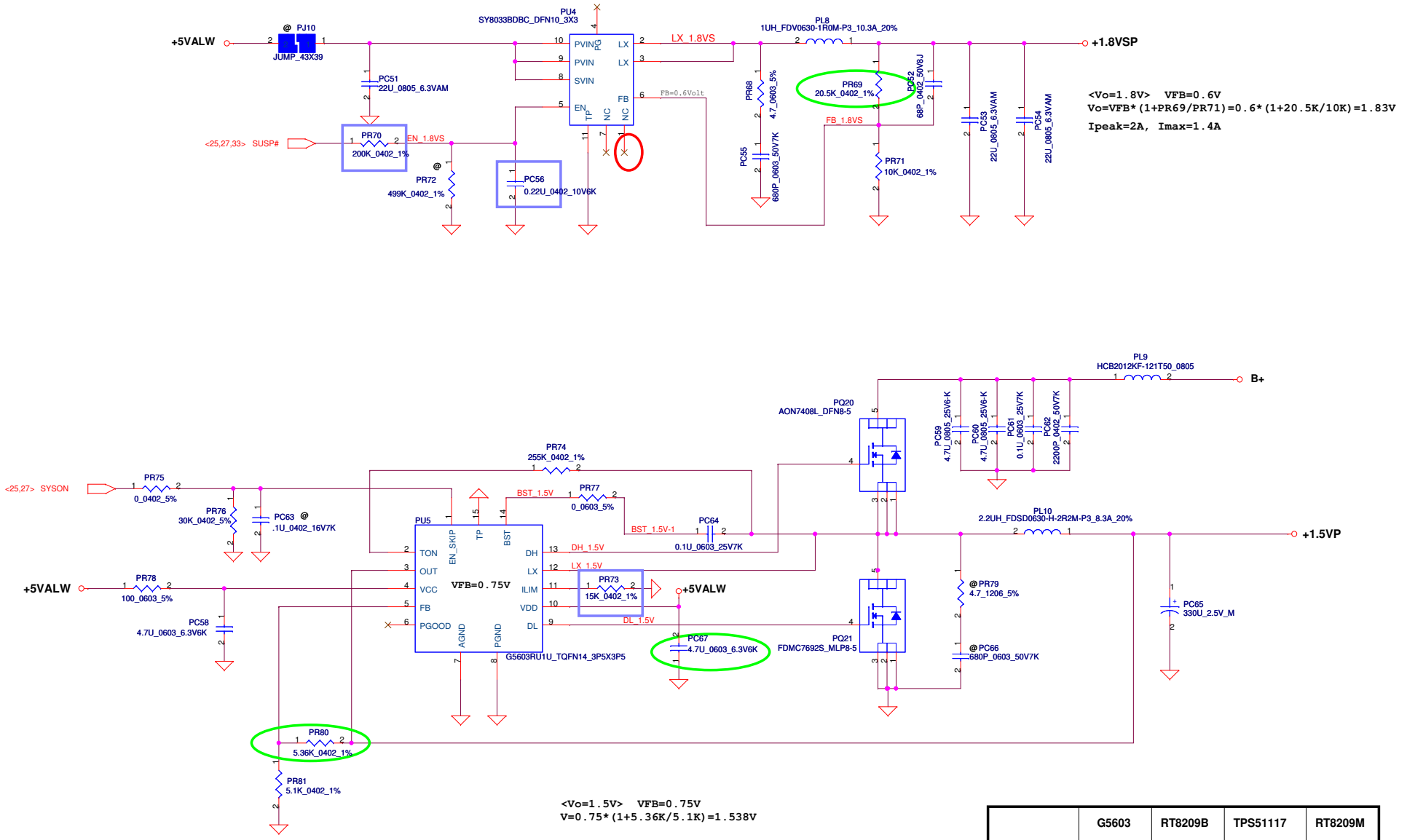
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
	1.0	

Date: Thursday, March 17, 2011 Sheet 32 of 37



	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.821A	7.235A	8.000A	8.178A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

Compal Electronics, Inc.

Title: 1.8VSP/1.5VP

Size: Custom | Document Number | Rev: 1.0

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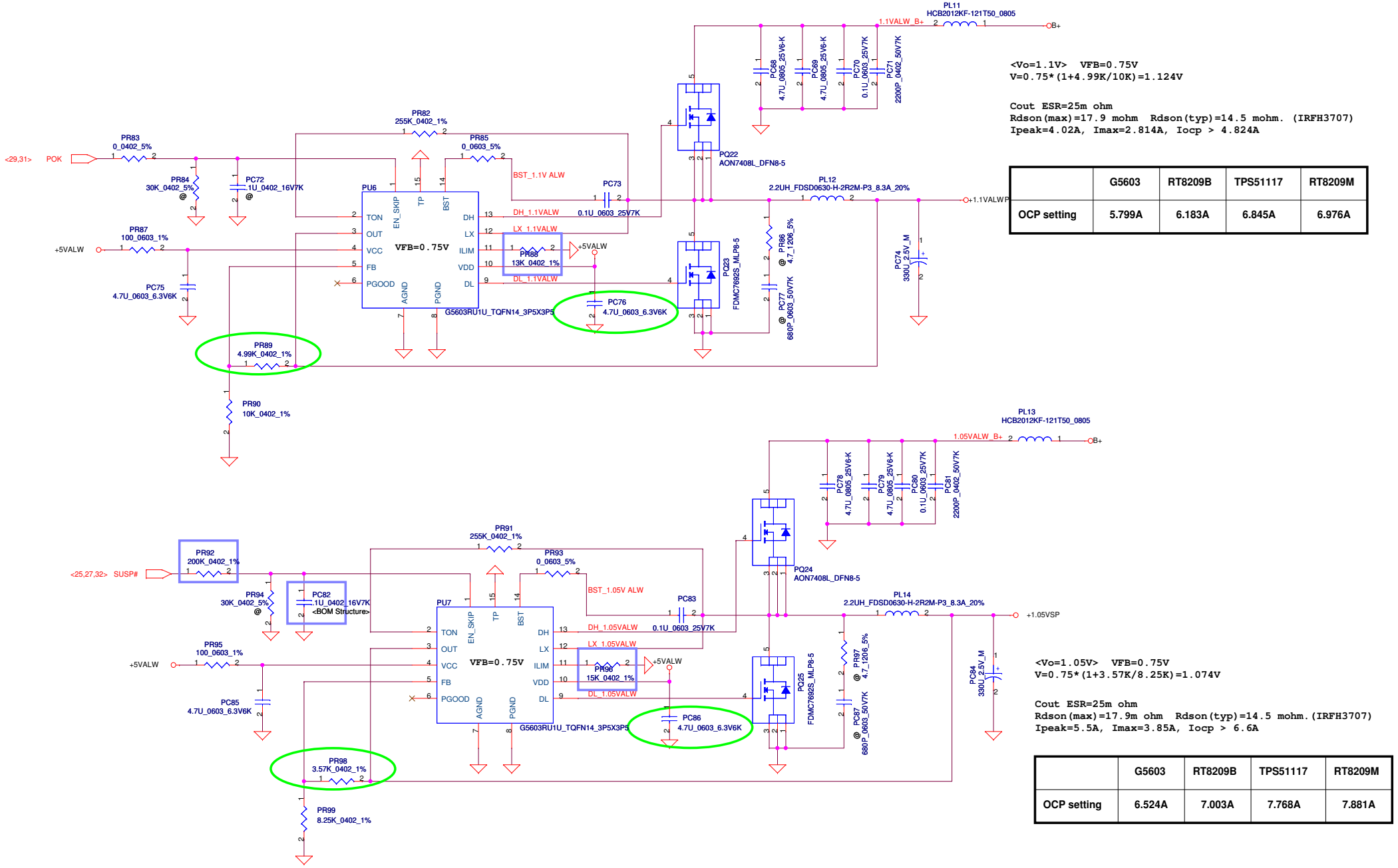


	G5603	RT8209B	TPS51117	RT8209M
OCP setting	5.799A	6.183A	6.845A	6.976A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.524A	7.003A	7.768A	7.881A

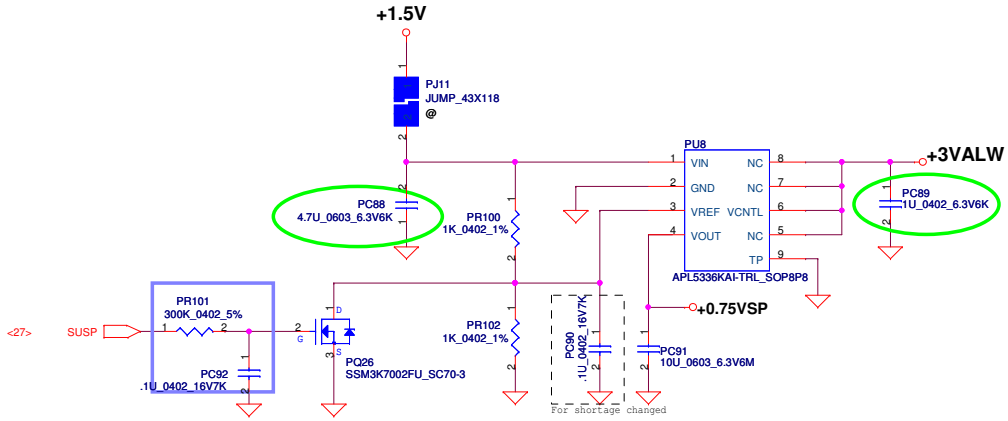
	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

Compal Electronics, Inc.

Title: 1.1VALWP/1.0VSP

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, March 17, 2011 | Sheet 34 of 37



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: 0.75VSP

Size	Document Number	Rev
		1.0

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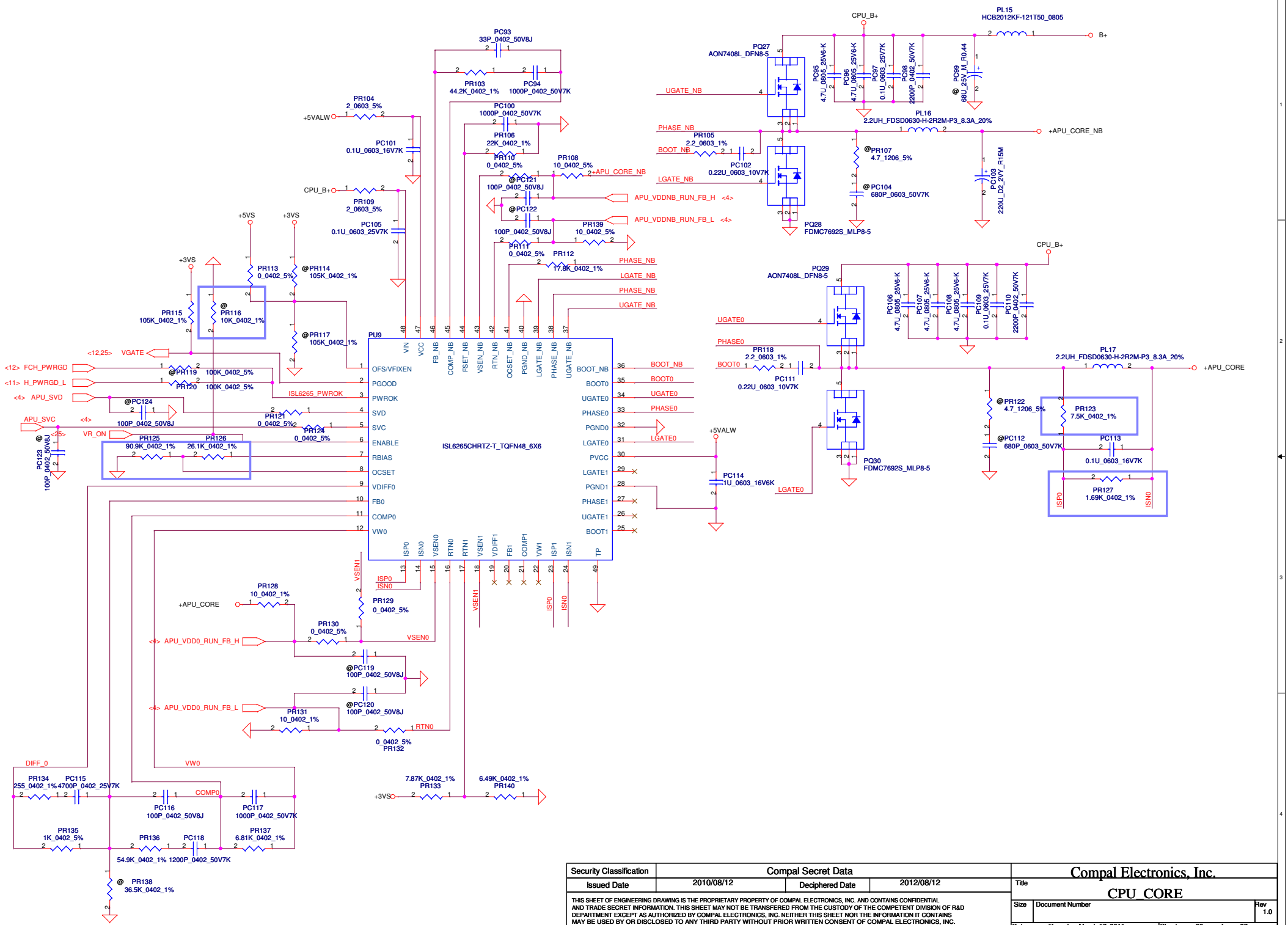

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: CPU_CORE

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		1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/VIN DECTOR power sequence	1	30	Add PC248 for +3VALWP PC252 for +5VALWP PC253 for +VSBP PC254 for +1.1VALWP PC255 for +1.05VSP PC256 for +0.75VSP PC257 for +1.8VSP	20101228	EVT
2		Modify charger power sequence	1	31	delete PC234	20101228	EVT
3		Modify 3VALWP/5VALWP power sequence	1	32	delete PC34	20101228	EVT
4		Modify charger power sequence	1	31	Chang PD5 from SCS00000Z00 (RB751V-40_SOD323-2 to SCS00005I00 (SD103AWS SOD323-2)	20110104	EVT
5		Modify charger power sequence	1	31	Chang PD3 from SCS00001I80 (B340A SMA) to SCS00000W00 (SX34_SMA2) Chang PQ4&PQ5 fromSB00000KI00(SI7121DN-T1-GE3 1P POWERPAK1212-8) to SB00000KZ00(AON7403L_DFN8-5)	20110106	EVT
6		Modify 3VALWP/5VALWP power sequence	1	32	Chang PL6 &PL7 from SH00000F900(4.7UH_FDVE0630-H-4R7M= P3_5.5A_20%) to SH00000MB00(4.7UH_FDSD0630-H-4R7M-P3_5.5A_20%)	20110110	EVT
7		Modify 1.8VSP/1.5VP power sequence	1	33	Chang PL10 from SH00000F800(2.2UH_FDVE0630-H-2R2M=P3_8.3A_20% to SH00000M700(2.2UH_FDSD0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
8		Modify 1.1VALWP/1.05VSP power sequence	1	34	Chang PL12 &PL14 from SH00000F800(2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700(2.2UH_FDSD0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
9		Modify CPU_CORE power sequence	1	36	Chang PL16 &PL17 from SH00000F800(2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700(2.2UH_FDSD0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
10		Modify CPU_CORE power sequence	1	36	Chang PR112 from SD034237280 (23.7k_0402_1%) to SD034178280 (17.8k_0402_1%) Chang PR123 from SD000002680 (6.98k_0402_1%) to SD034750180 (7.5k_0402_1%) Chang PR127 from SD034187180 (1.87k_0402_1%) to SD00000JB80 (1.69k_0402_1%)	20110110	EVT
11		Modify 1.8VSP/1.5VP power sequence	2	33	add PC258 to +1.5V output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
12		Modify 1.1VALWP/1.05VSP power sequence	2	34	add PC259 to +1.1VALWP output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
13		Modify 1.8VSP/1.5VP power sequence	3	33	delete co-lay PC258 for +1.5V output capacitor	20110225	PVT
14		Modify 1.1VALWP/1.05VSP power sequence	3	34	delete co-lay PC259 for +1.1VALW output capacitor	20110225	PVT
15		Modify charger power sequence	3	31	delete co-lay PJ32 modify PQ4 PQ5 footprint from AON7403L_DFN8-5 to SIS412DN-T1-GE3_POWERPAK8-5	20110226	PVT
16		Modify charger power sequence	3	31	change charger IC from G5209 to ISL6251 change output choke from 8.2u to 10u	20110226	PVT
17		Modify DCIN/VIN DECTOR power sequence	3	30	Add PC258 for +1.5V jump by RF test	2010302	PVT
18							
19							
20							
21							
22							
23							

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title	PIR (PWR)	
Size: Custom	Document Number	Rev: 1.0
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