

LCFC Confidential


BMWQ1/Q2 M/B Schematics Document

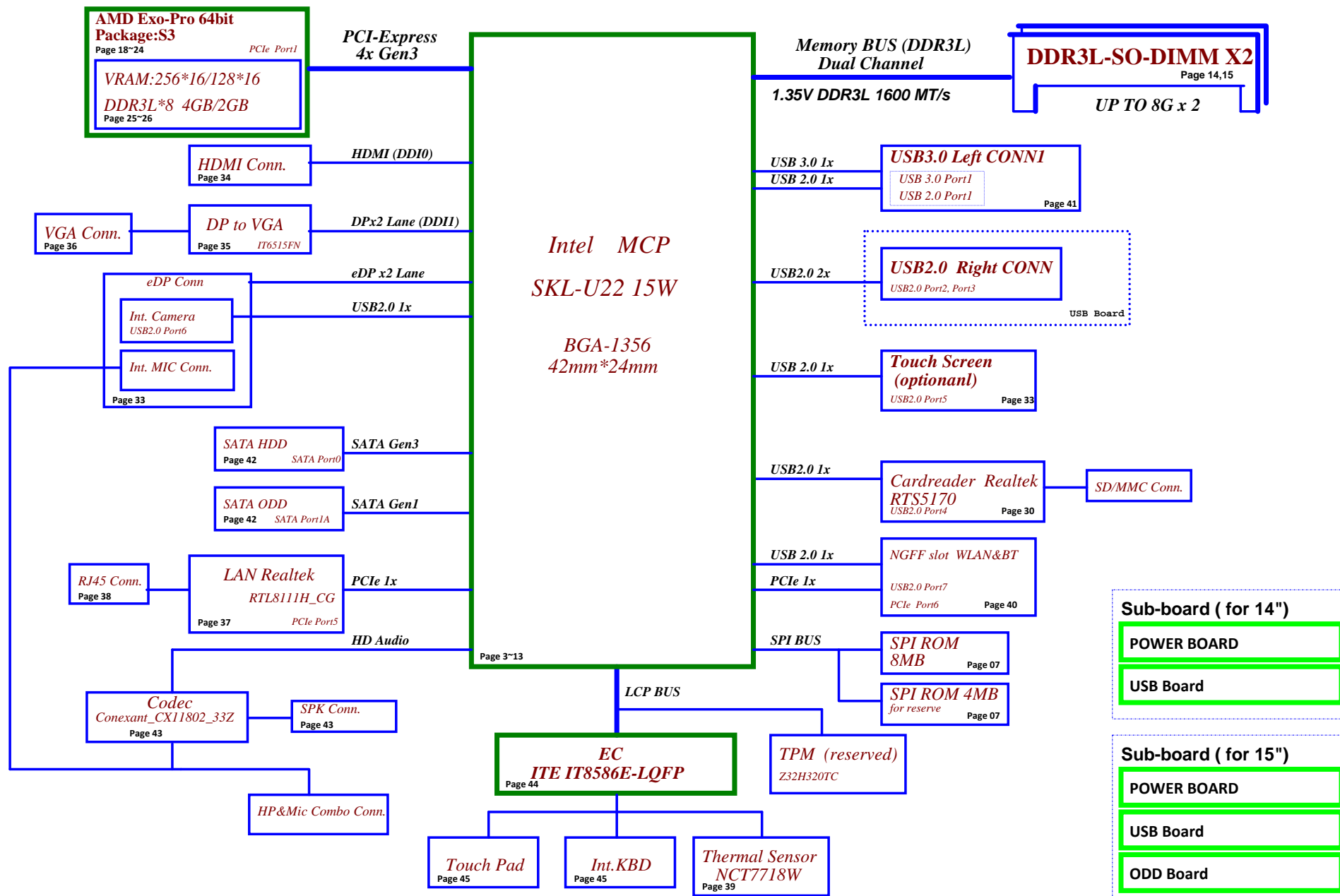
Intel Skylake U22 with DDRIII + AMD Exo-Pro-S3 GPU

2015-06-02

REV:0.3

www.rosefix.com

Security Classification	LC Future Center Secret Data			Title		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.35V +VCCST	+5VS
				+3VS
State				+VCCIO
				+VCCSTG
				+VCCSA
				+VCC_GT
				+CPU_CORE
				+0.675VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function	BOM Structure	BTO Item
USB3.0	1	USB3.0 CONN left	@
	2	NC	14@
	3	NC	15@
	4	NC	14or15@
	5	NC	14or17@
	6	NC	AOAC@
USB2.0	1	USB3.0 CONN Left	
	2	USB2.0 CONN1 Right	Cannonlake@
	3	USB2.0 CONN2 Right	CD@
	4	Camera	DUALMIC@
	5	Cardreader	EMC@
	6	Touch Panel	EMC_15@
	7	BT	EMC_NS@
	8	NC	EMC_PX@
	9	NC	EMC_PXNS@
	10	NC	ES@
PCIE	1	NC	EXO@
	2	NC	GCLK@
	3	NC	ME@
	4	NC	NTS@
	5	LAN	PCH_SDIO@
	6	WLAN	
	7	used as SATA	
	8	used as SATA	
SATA	X4 PCIE (9-12)	DGPU	PX@
	0	HDD	RANKA@
	1A	ODD	RANKB@
	1B	used as PCIE	Realtek_SD@
	2	used as PCIE	SINGLEMIC@
			SINGLERANK@
			DUALRANK@
			TS@
			TPM@
			UMA@

SMBUS Control Table

	SOURCE	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger	DGPU
EC_SMB_CK1	IT8586E	V	V	X	X	X	X	X	V	X
EC_SMB_DA1	+3VALW	V	+3VALW	X	X	X	X	X	V	X
EC_SMB_CK2	IT8586E	X	V	X	X	V	V	X	X	V
EC_SMB_DA2	+3VS	X	+3VS	X	X	+3VS	+3VALW_PCH	X	X	+3VGS
PCH_SMB_CLK	PCH	X	X	V	V	X	V	X	X	X
PCH_SMB_DATA	+3VALW_PCH	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X	X

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

Device	Address
Thermal Sensor NCT7718W	1001_100xb
PCH	need to update
DGPU	need to update

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

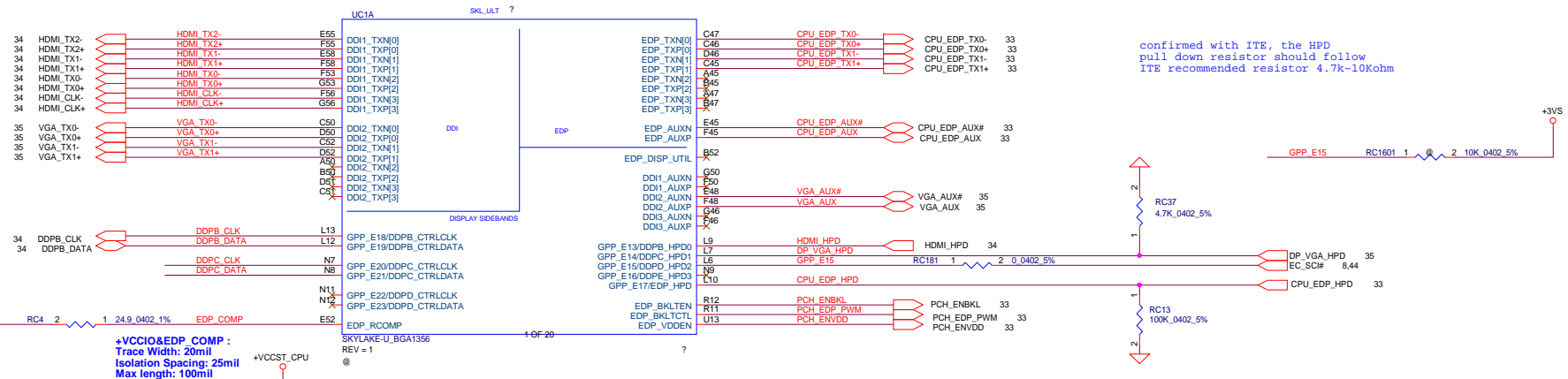
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

DP TO VGA Converter



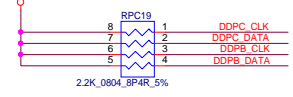
confirmed with ITE, the HPD pull down resistor should follow ITE recommended resistor 4.7k-10kOhm

+VCCIO&EDP COMP :
Trace Width: 20mil
Isolation Spacing: 25mil
Max length: 100mil

check PROCHOT# circuit with PWR

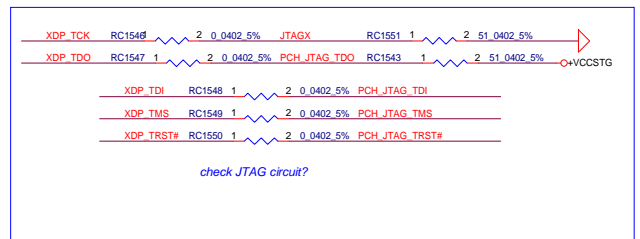
check H_THRMTRIP# if need to connector to EC

check DDPB_CLK pull high or not?



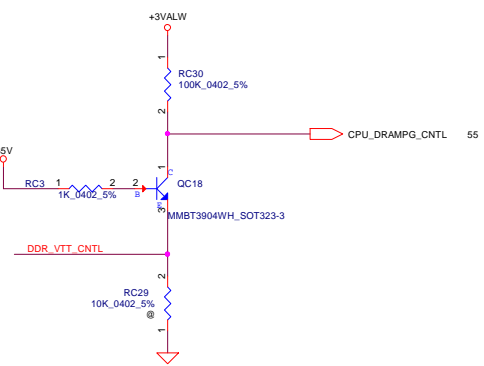
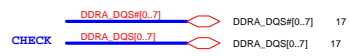
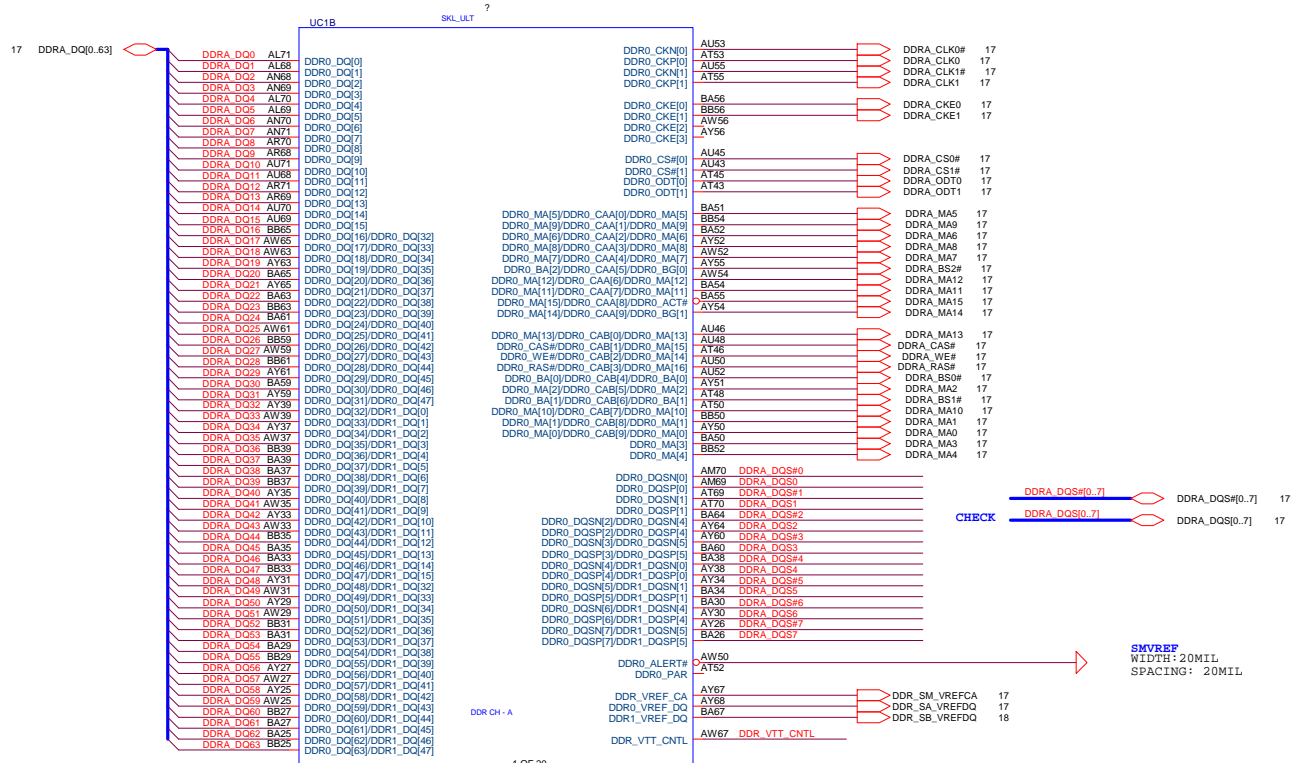
DDP_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC



check JTAG circuit?

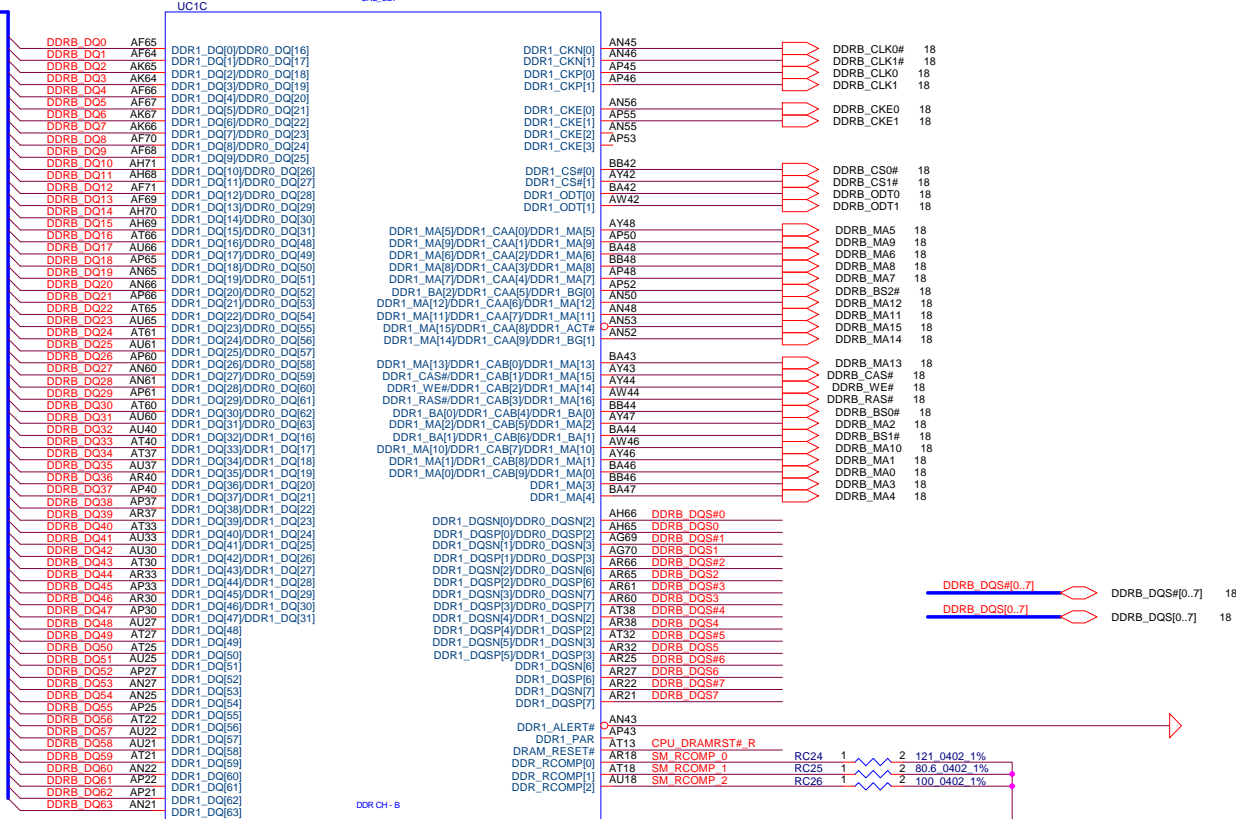
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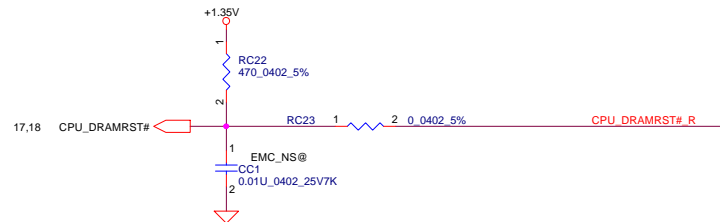
SKYLAKE-U_BGA1356
REV = Y

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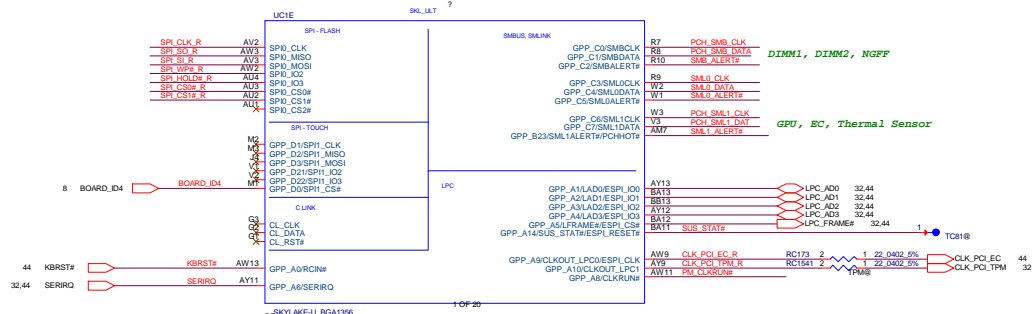
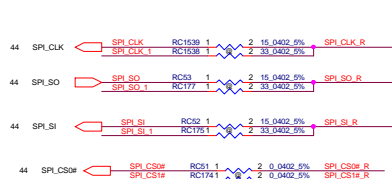
18 DDRB_DQ[0..63]



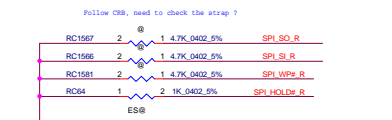
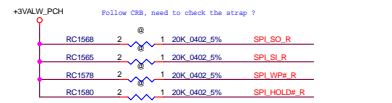
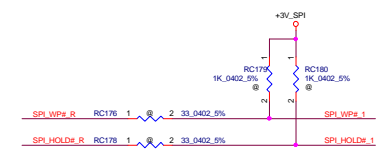
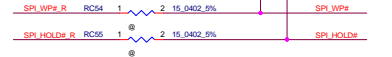
Need to check the resistor value



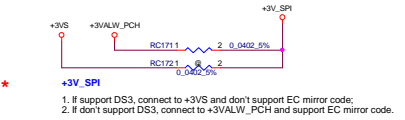
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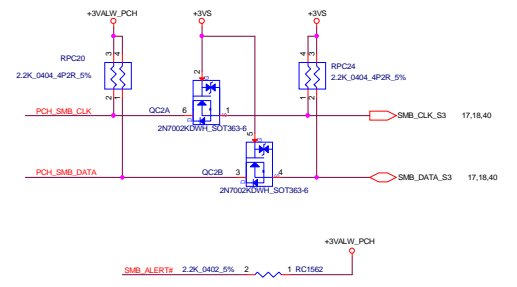
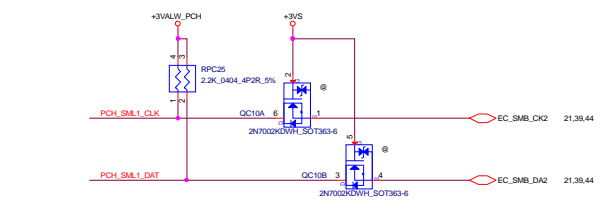
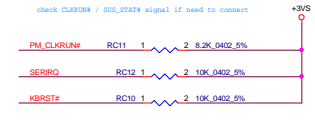
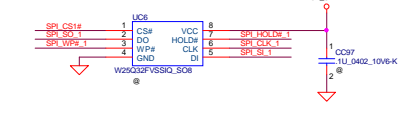
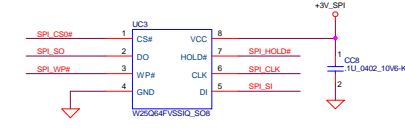
Check with B105, SPI is Dual mode or quad mode



Based on W1W36 SKL U8Y W0M, RC64 populated, and RC61 de-populated for SKL U ES sample. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.



- * 1. If support DS3, connect to +3VS and don't support EC mirror code;
- 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.



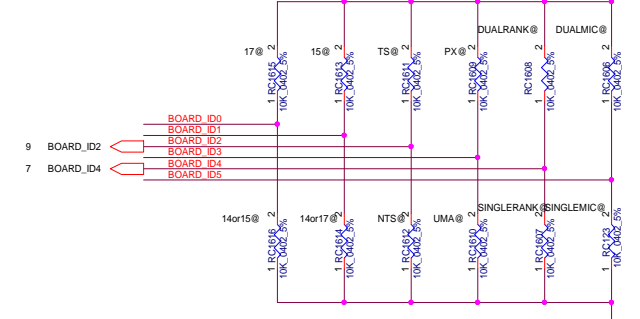
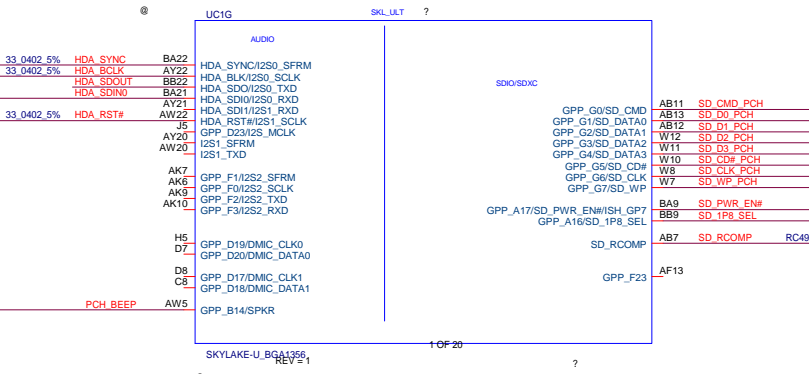
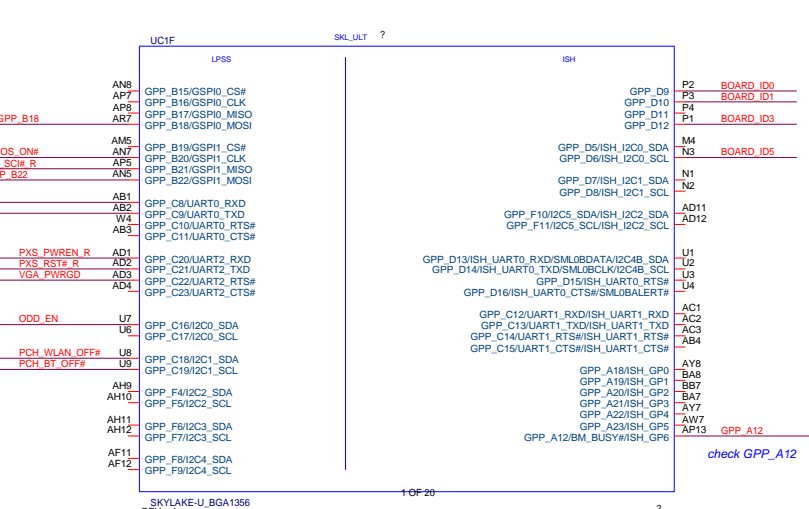
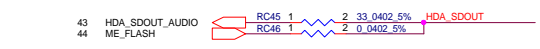
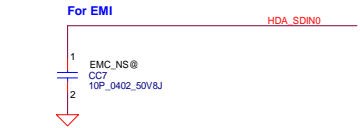
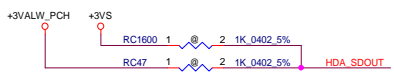
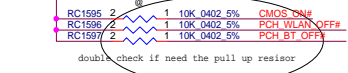
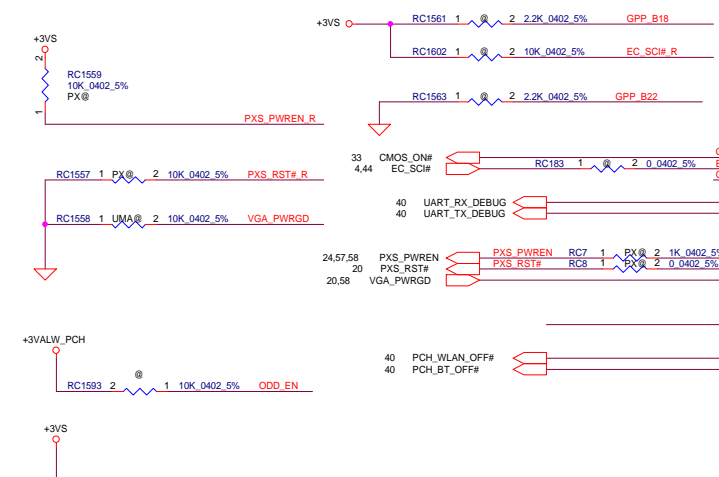
This signal has a weak internal pull-down. 0 = LPC is selected for EC. (Default) 1 = SPI is selected for EC.

Notes:

- The internal pull-down is disabled after RSMRST# de-asserts.
- This signal is in the primary welf Raising edge of RSMRST#

To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST#. (Refer to W1W52_W1W0V)

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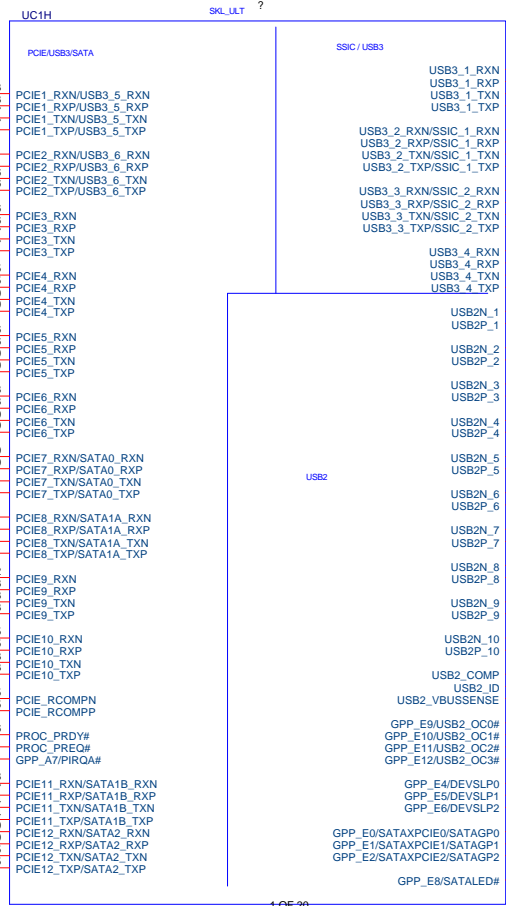


Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11	Reserved
Board_ID2	0 Non-Touch	RC1612
	1 Touch	RC1611
Board_ID3	0	RC1610
	1 DIS	RC1609
Board_ID4	0 SingleRank	RC1607
	1	DualRank RC1608
Board_ID5	0 SingleMIC	RC123
	1 DualMIC	RC1606

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) * 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) * 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) * 1 = LPC	0	Rising edge of PCH_PWROK

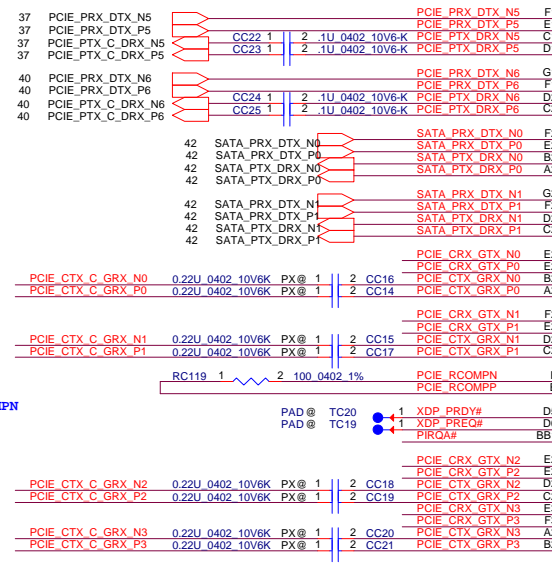
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PCIE1



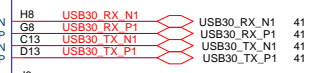
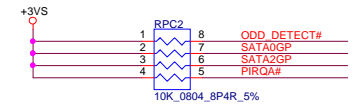
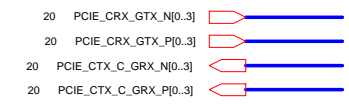
LAN PCIE5

WLAN PCIE6

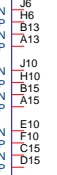


third-part dGPU PCIEP9

PCIE_RCOMP and PCIE_RCOMPMP
Trace Width: 12-15mil
Differential between RCOMP/RCOMPMP



LEFT USB (3.0)



LEFT USB (3.0)
RIGHT USB (2.0)

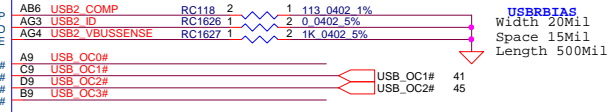
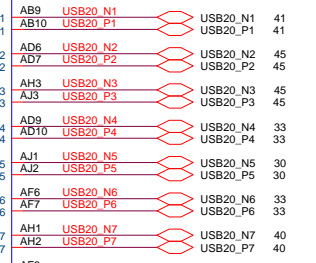
RIGHT USB (2.0)

Camera

Card reader

Touch panel

BT



USBRBTAS
Width 20Mil
Space 15Mil
Length 500Mil



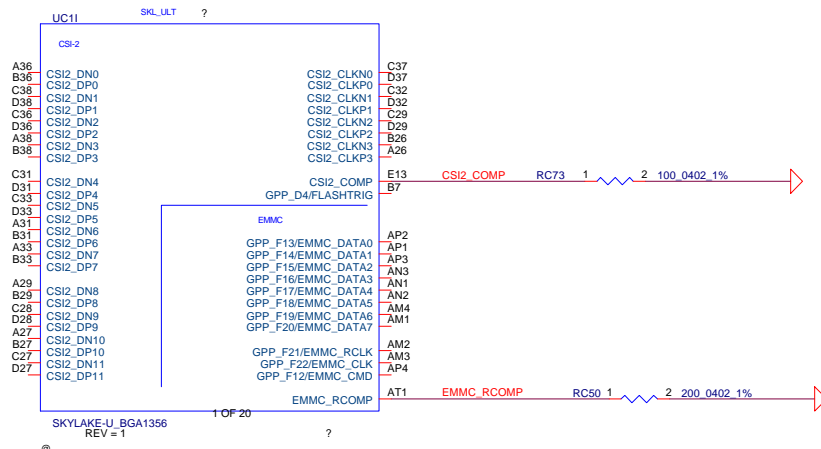
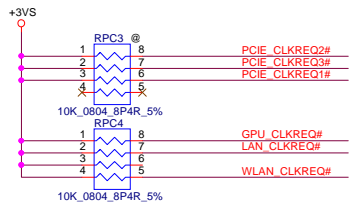
SKYLAKE-U_BGA1356
REV = 1

+3VS

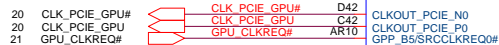
+3VALW_PCH

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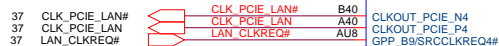
check the Pull up resistor



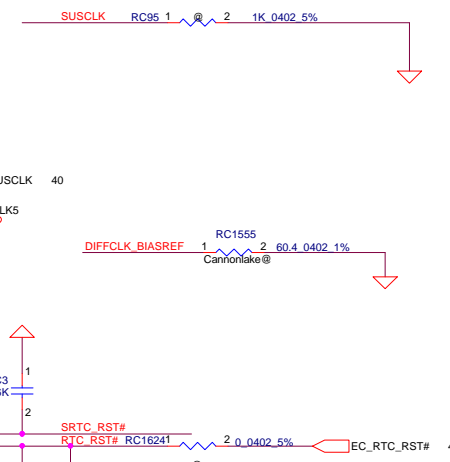
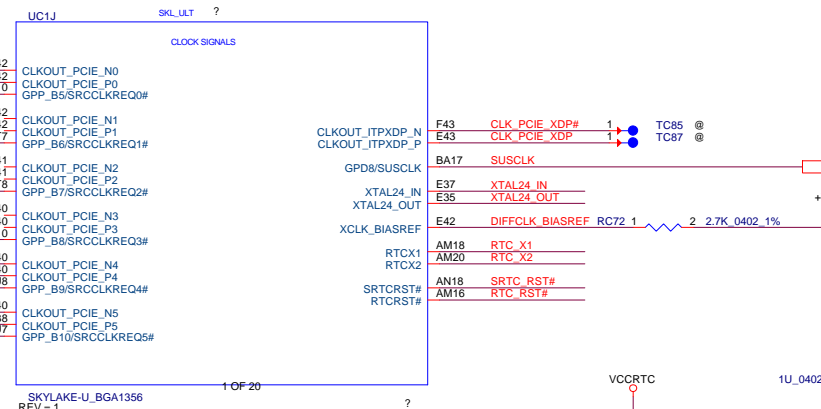
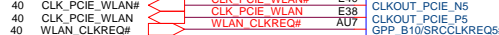
PCIE CLK0 GPU



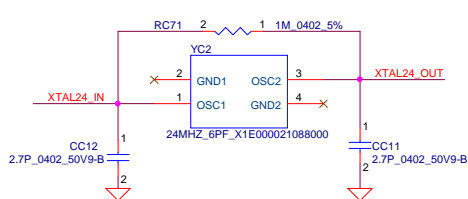
PCIE CLK5 LAN



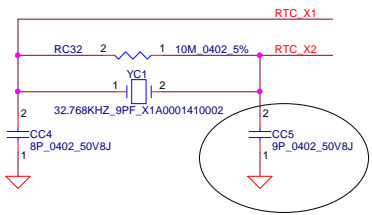
PCIE CLK6 WLAN



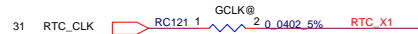
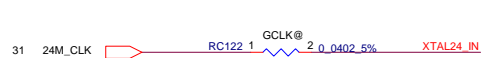
check if need to change to 1M_0402_1% follow PDG, CRB is 1M_0402_5%



need to use 38.4MHz (30ohm) for Cannonlake-u

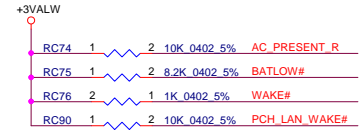
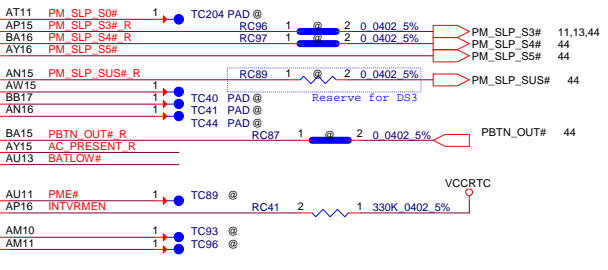
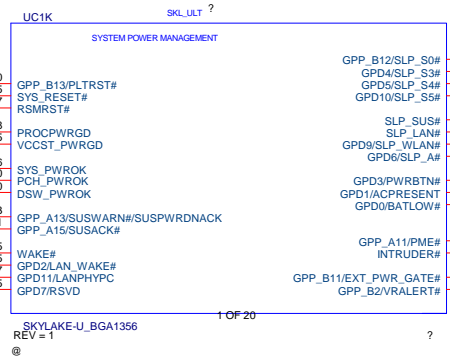
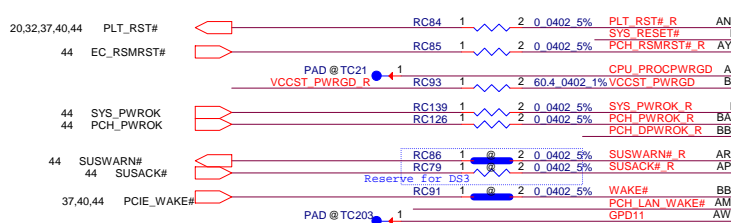


when single end external clock generator used, this pin should be grounded

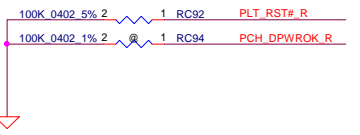
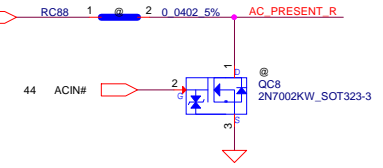
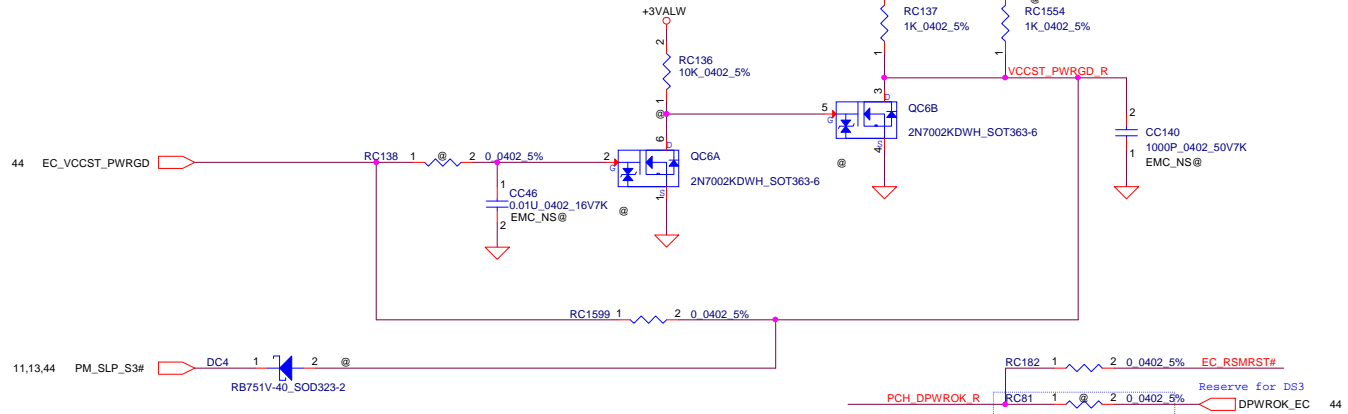
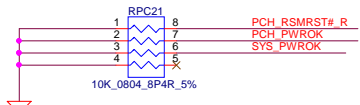
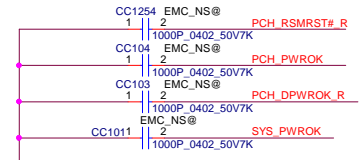
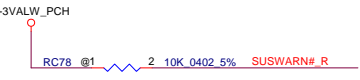


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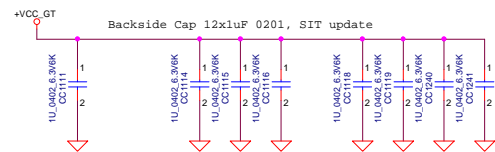
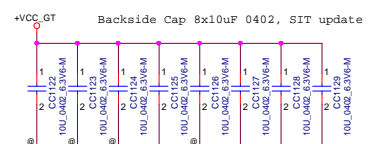
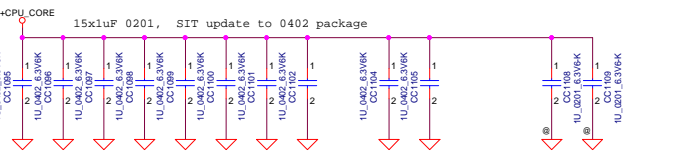
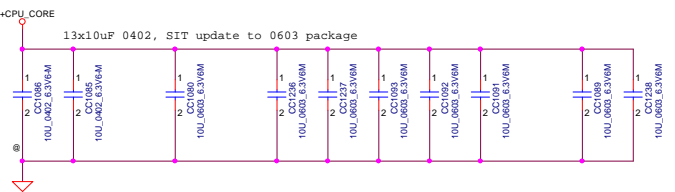
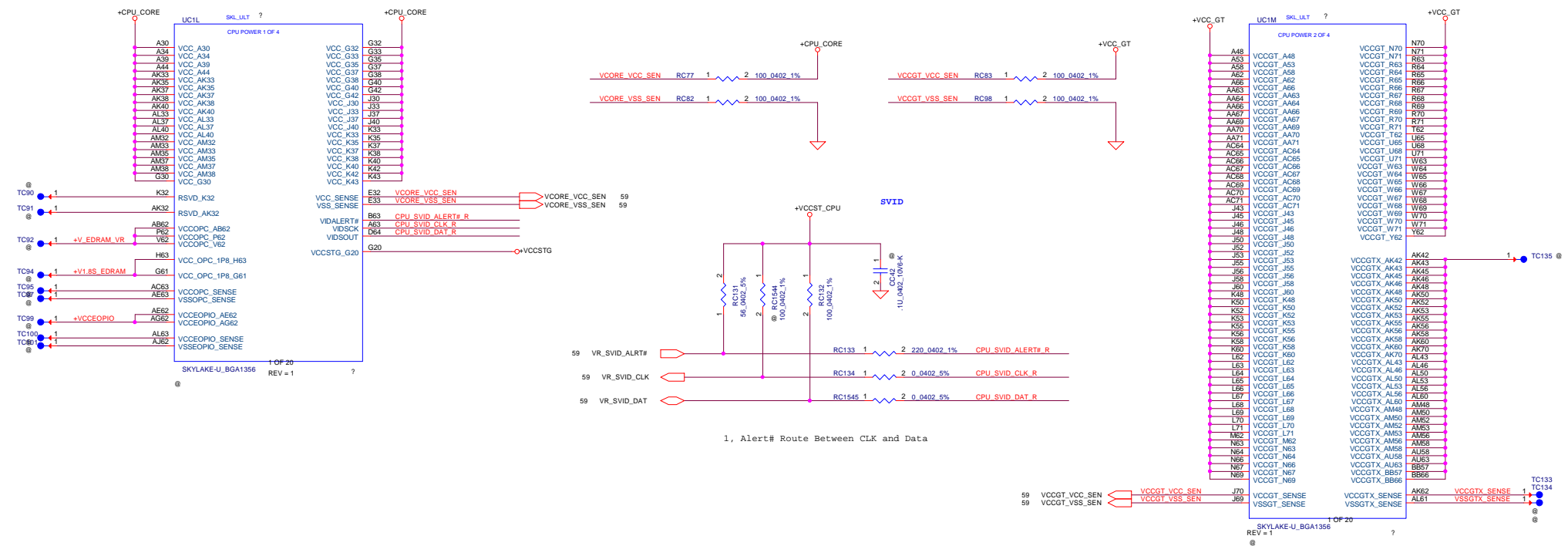
check if need one buffer



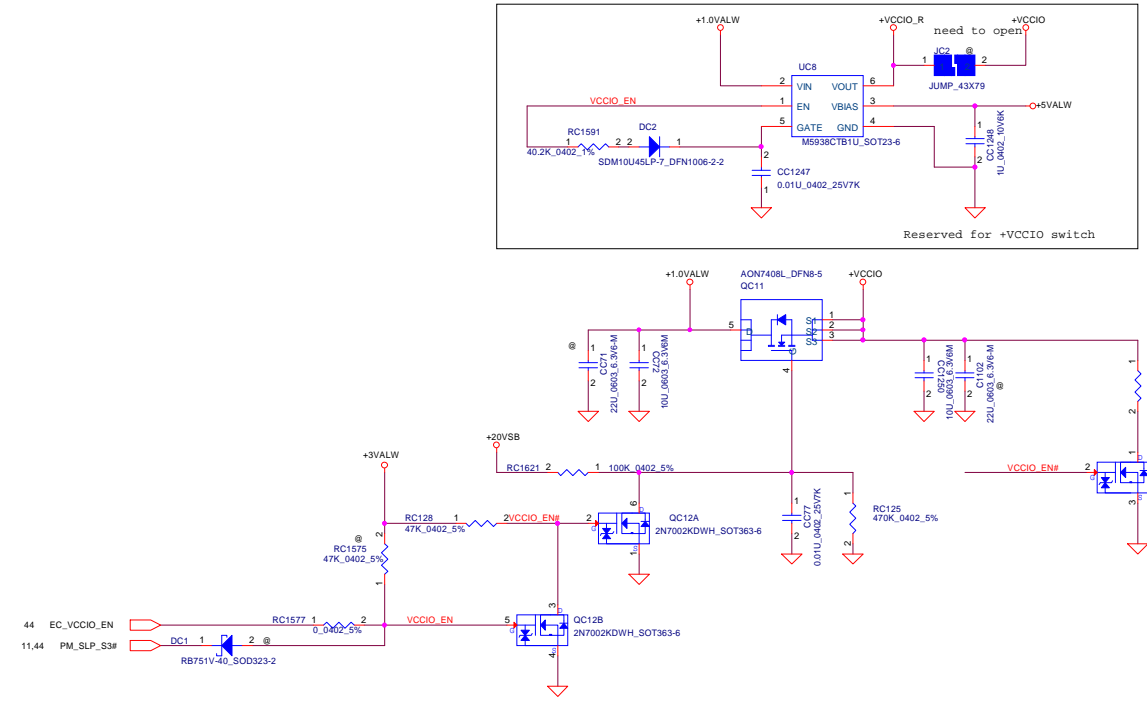
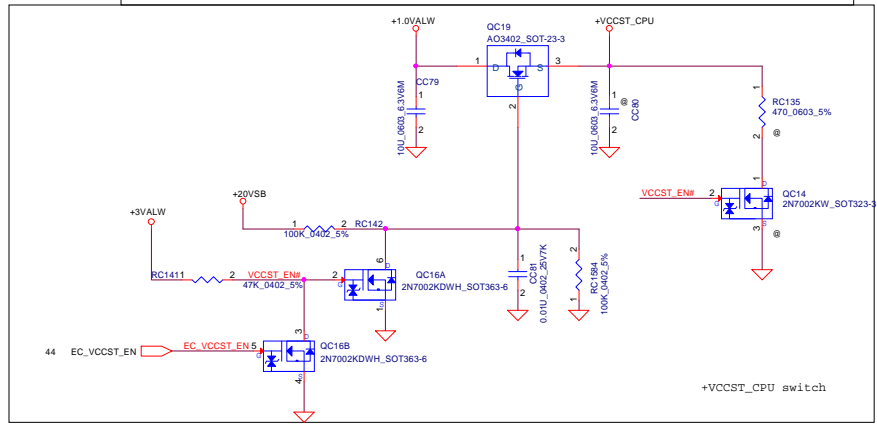
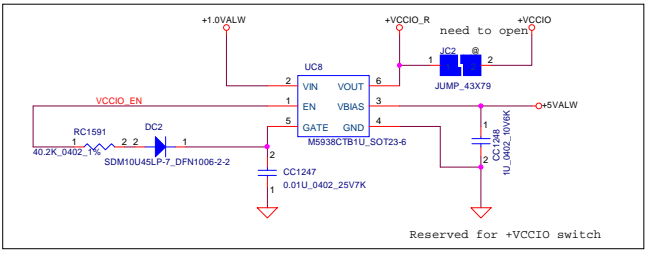
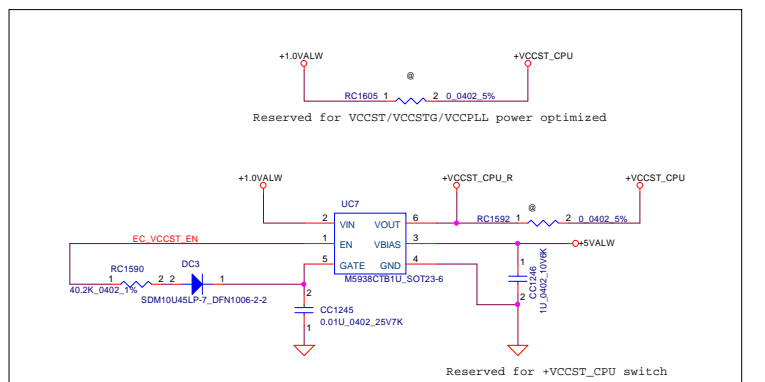
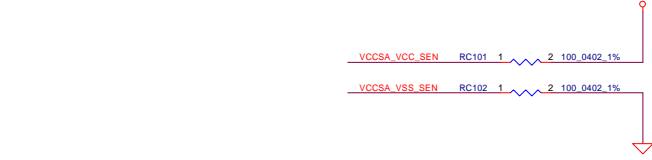
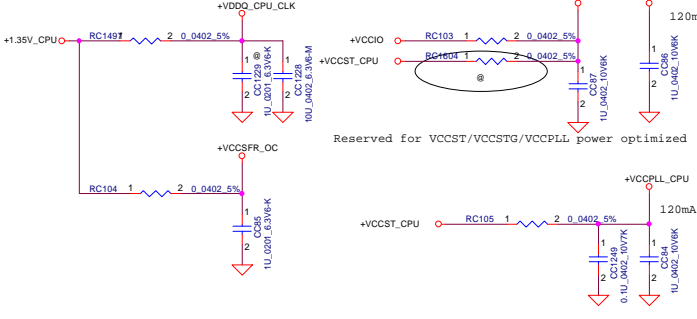
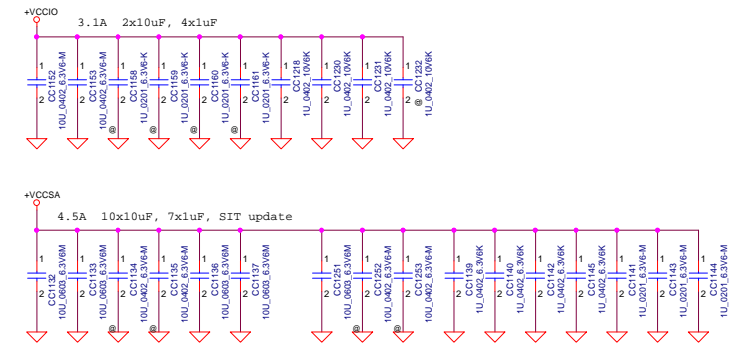
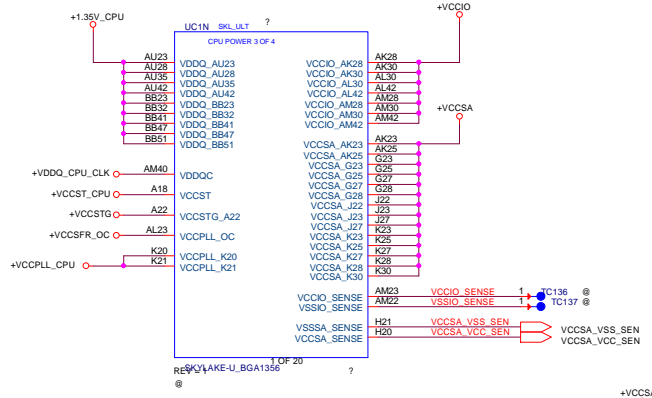
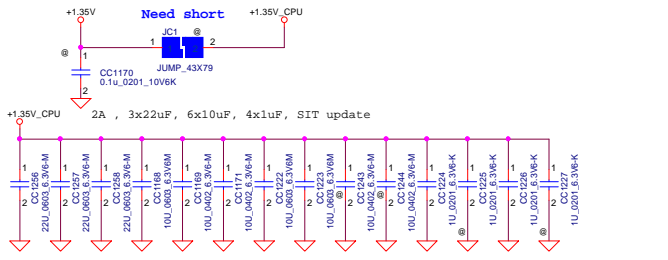
Follow CRB change to 1kohm



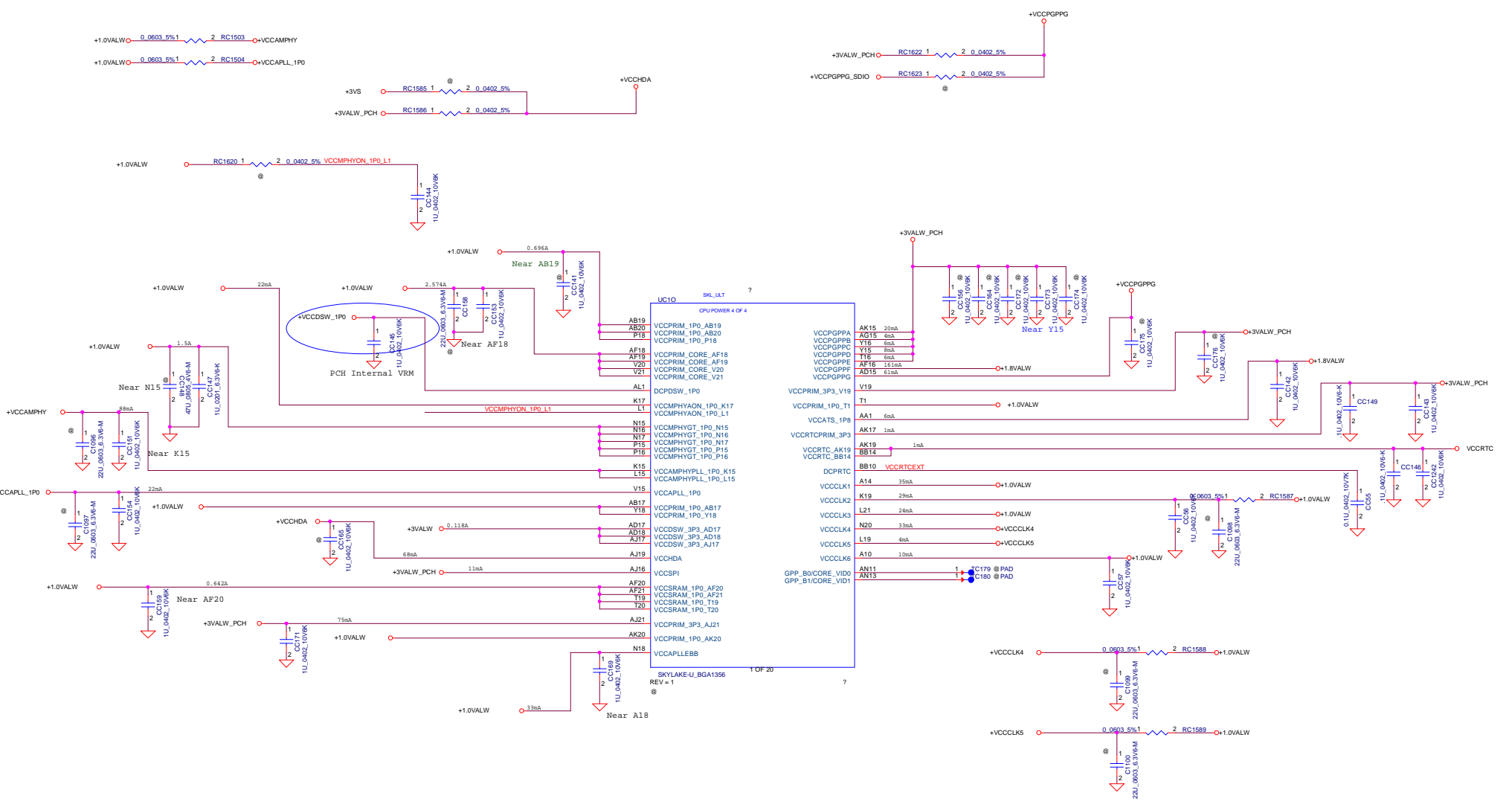
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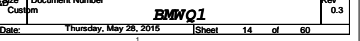
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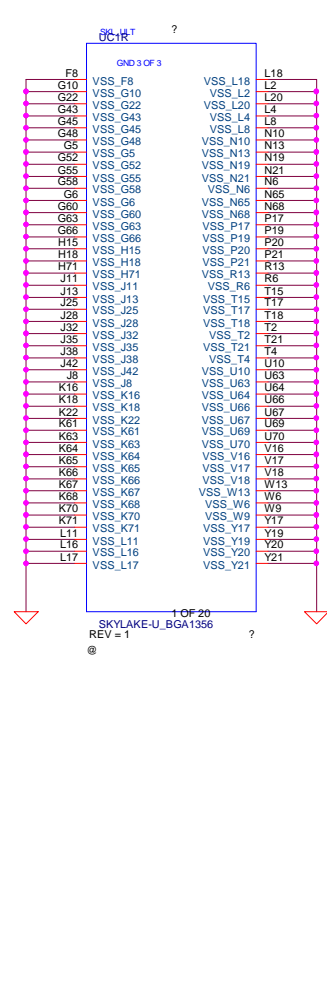
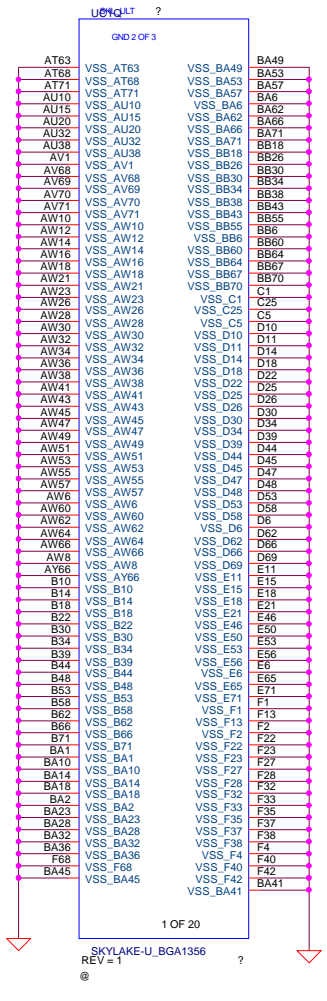
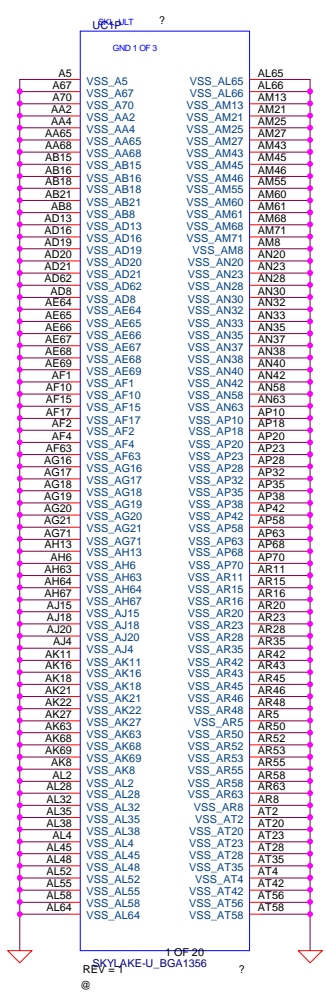
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Issued Date	2014/12/11	Deciphered Date	2015/12/11
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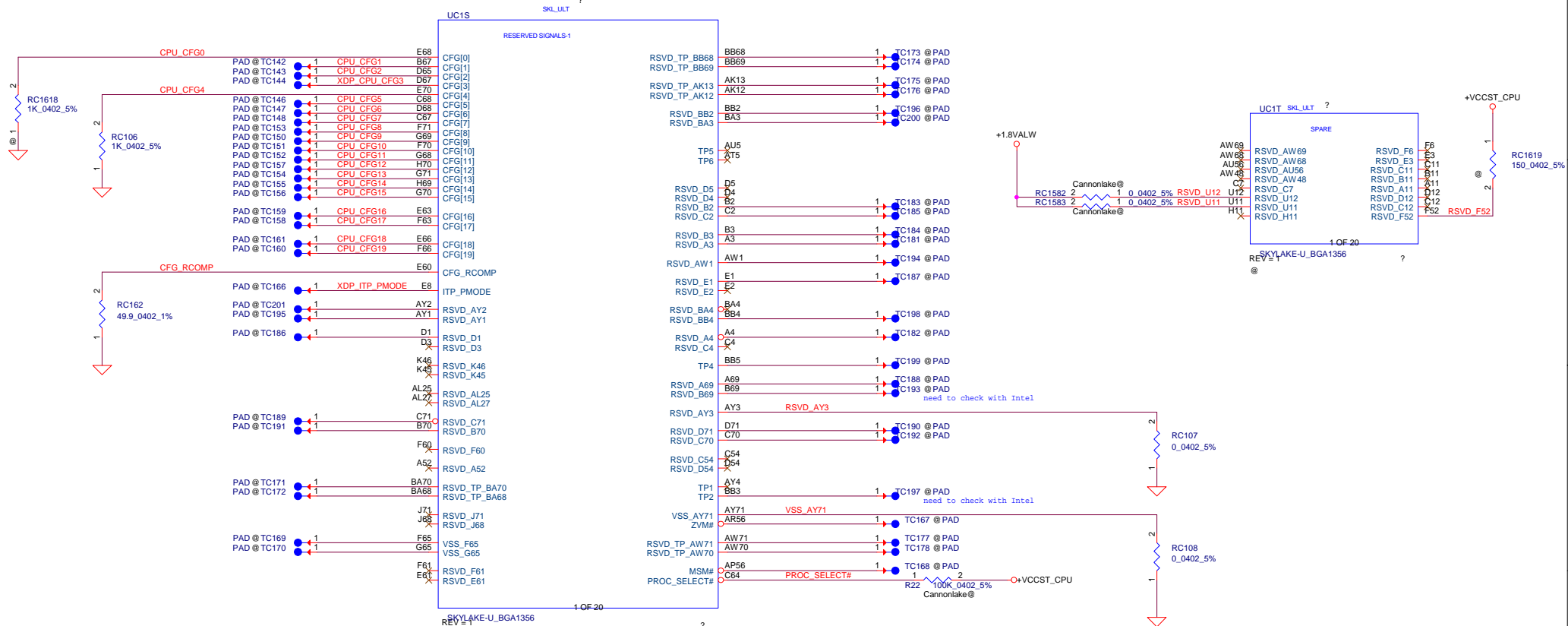


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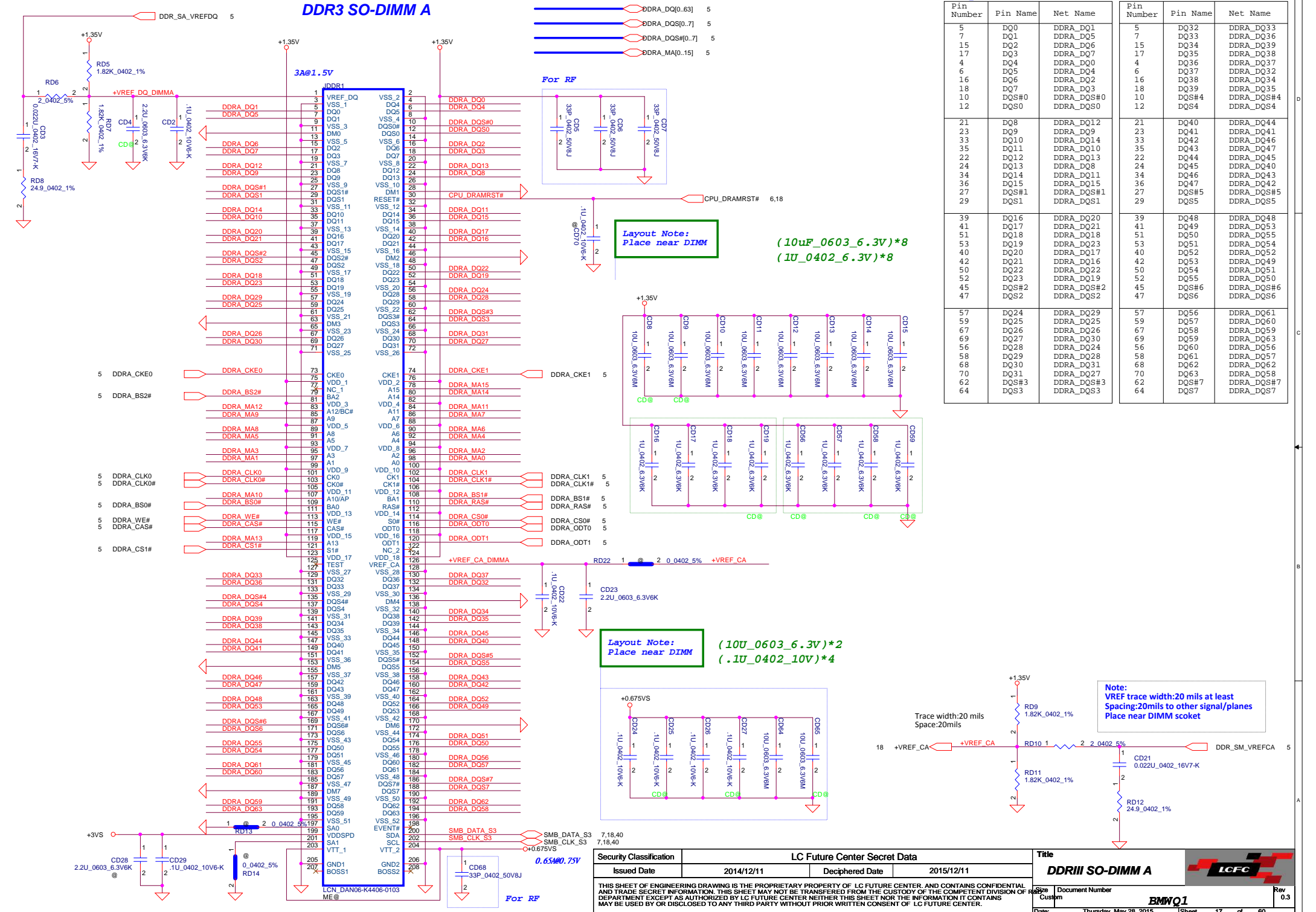
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Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	-1 = eDP Disabled -0 = eDP Enabled *	1

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				Date	Thursday, May 28, 2015

DDR3 SO-DIMM A



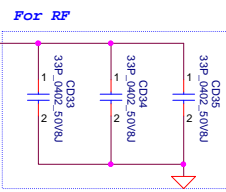
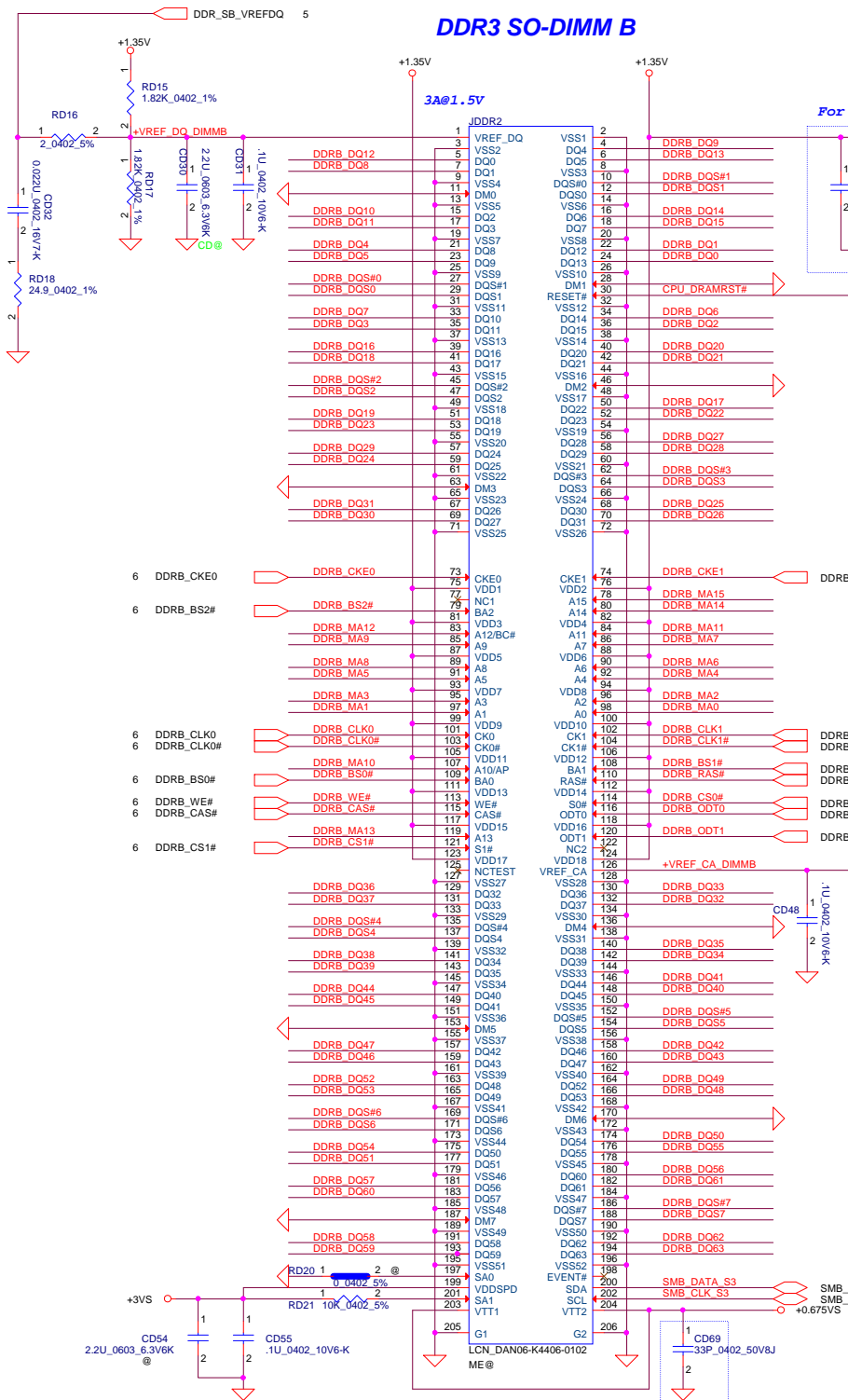
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7	DQ1	DDRA_DQ5	7	DQ33	DDRA_DQ36
15	DQ2	DDRA_DQ6	15	DQ34	DDRA_DQ39
17	DQ3	DDRA_DQ7	17	DQ35	DDRA_DQ38
4	DQ4	DDRA_DQ0	4	DQ36	DDRA_DQ37
6	DQ5	DDRA_DQ4	6	DQ37	DDRA_DQ32
16	DQ6	DDRA_DQ2	16	DQ38	DDRA_DQ34
18	DQ7	DDRA_DQ3	18	DQ39	DDRA_DQ35
10	DQS#0	DDRA_DQS#0	10	DQS#4	DDRA_DQS#4
12	DQS0	DDRA_DQS0	12	DQS4	DDRA_DQS4
21	DQ8	DDRA_DQ12	21	DQ40	DDRA_DQ44
23	DQ9	DDRA_DQ9	23	DQ41	DDRA_DQ41
33	DQ10	DDRA_DQ14	33	DQ42	DDRA_DQ46
35	DQ11	DDRA_DQ10	35	DQ43	DDRA_DQ47
22	DQ12	DDRA_DQ13	22	DQ44	DDRA_DQ45
24	DQ13	DDRA_DQ8	24	DQ45	DDRA_DQ40
34	DQ14	DDRA_DQ11	34	DQ46	DDRA_DQ43
36	DQ15	DDRA_DQ15	36	DQ47	DDRA_DQ42
27	DQS#1	DDRA_DQS#1	27	DQS#5	DDRA_DQS#5
29	DQS1	DDRA_DQS1	29	DQS5	DDRA_DQS5
39	DQ16	DDRA_DQ20	39	DQ48	DDRA_DQ48
41	DQ17	DDRA_DQ21	41	DQ49	DDRA_DQ53
51	DQ18	DDRA_DQ18	51	DQ50	DDRA_DQ55
53	DQ19	DDRA_DQ23	53	DQ51	DDRA_DQ54
40	DQ20	DDRA_DQ17	40	DQ52	DDRA_DQ52
42	DQ21	DDRA_DQ16	42	DQ53	DDRA_DQ49
50	DQ22	DDRA_DQ22	50	DQ54	DDRA_DQ51
52	DQ23	DDRA_DQ19	52	DQ55	DDRA_DQ50
45	DQS#2	DDRA_DQS#2	45	DQS#6	DDRA_DQS#6
47	DQS2	DDRA_DQS2	47	DQS6	DDRA_DQS6
57	DQ24	DDRA_DQ29	57	DQ56	DDRA_DQ61
59	DQ25	DDRA_DQ25	59	DQ57	DDRA_DQ60
67	DQ26	DDRA_DQ26	67	DQ58	DDRA_DQ59
69	DQ27	DDRA_DQ30	69	DQ59	DDRA_DQ63
56	DQ28	DDRA_DQ24	56	DQ60	DDRA_DQ56
68	DQ29	DDRA_DQ28	68	DQ61	DDRA_DQ57
68	DQ30	DDRA_DQ31	68	DQ62	DDRA_DQ62
70	DQ31	DDRA_DQ27	70	DQ63	DDRA_DQ58
62	DQS#3	DDRA_DQS#3	62	DQS#7	DDRA_DQS#7
64	DQS3	DDRA_DQS3	64	DQS7	DDRA_DQS7

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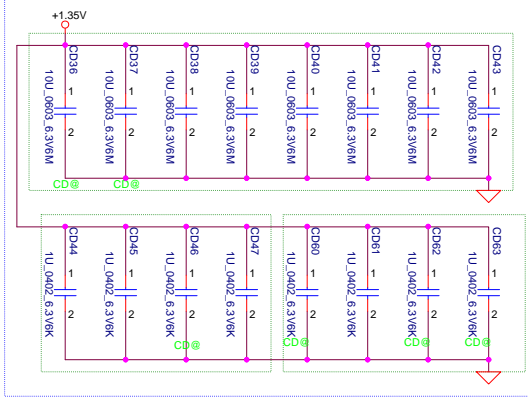
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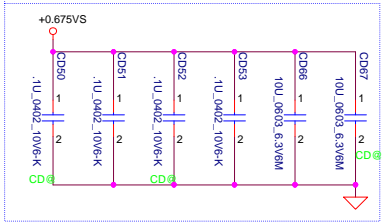
DDR3 SO-DIMM B



Layout Note:
Place near DIMM
(10uF_0603_6.3V)*8
(1U_0402_6.3V)*8



Layout Note:
Place near DIMM
(10U_0603_6.3V)*2
(.1U_0402_10V)*4



Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR3_DQ12
7	DQ1	DDR3_DQ8
15	DQ2	DDR3_DQ10
17	DQ3	DDR3_DQ11
4	DQ4	DDR3_DQ9
6	DQ5	DDR3_DQ13
16	DQ6	DDR3_DQ14
18	DQ7	DDR3_DQ15
10	DQS#0	DDR3_DQS#1
12	DQS#0	DDR3_DQS#1
21	DQ8	DDR3_DQ4
23	DQ9	DDR3_DQ5
33	DQ10	DDR3_DQ7
35	DQ11	DDR3_DQ3
22	DQ12	DDR3_DQ1
24	DQ13	DDR3_DQ0
34	DQ14	DDR3_DQ6
36	DQ15	DDR3_DQ2
27	DQS#1	DDR3_DQS#0
29	DQS#1	DDR3_DQS#0
39	DQ16	DDR3_DQ16
41	DQ17	DDR3_DQ18
51	DQ18	DDR3_DQ19
53	DQ19	DDR3_DQ23
40	DQ20	DDR3_DQ20
42	DQ21	DDR3_DQ21
50	DQ22	DDR3_DQ17
52	DQ23	DDR3_DQ22
45	DQS#2	DDR3_DQS#2
47	DQS#2	DDR3_DQS#2
57	DQ24	DDR3_DQ29
59	DQ25	DDR3_DQ24
67	DQ26	DDR3_DQ31
69	DQ27	DDR3_DQ30
56	DQ28	DDR3_DQ27
58	DQ29	DDR3_DQ28
68	DQ30	DDR3_DQ25
70	DQ31	DDR3_DQ26
62	DQS#3	DDR3_DQS#3
64	DQS#3	DDR3_DQS#3
129	DQ32	DDR3_DQ36
131	DQ33	DDR3_DQ37
141	DQ34	DDR3_DQ38
143	DQ35	DDR3_DQ39
130	DQ36	DDR3_DQ33
132	DQ37	DDR3_DQ32
140	DQ38	DDR3_DQ35
142	DQ39	DDR3_DQ34
135	DQS#4	DDR3_DQS#4
137	DQS#4	DDR3_DQS#4
147	DQ40	DDR3_DQ44
149	DQ41	DDR3_DQ45
157	DQ42	DDR3_DQ47
159	DQ43	DDR3_DQ46
146	DQ44	DDR3_DQ41
148	DQ45	DDR3_DQ40
158	DQ46	DDR3_DQ42
160	DQ47	DDR3_DQ43
152	DQS#5	DDR3_DQS#5
154	DQS#5	DDR3_DQS#5
163	DQ48	DDR3_DQ52
165	DQ49	DDR3_DQ53
175	DQ50	DDR3_DQ54
177	DQ51	DDR3_DQ51
164	DQ52	DDR3_DQ49
166	DQ53	DDR3_DQ48
174	DQ54	DDR3_DQ50
176	DQ55	DDR3_DQ55
169	DQS#6	DDR3_DQS#6
171	DQS#6	DDR3_DQS#6
181	DQ56	DDR3_DQ57
183	DQ57	DDR3_DQ60
191	DQ58	DDR3_DQ58
193	DQ59	DDR3_DQ59
180	DQ60	DDR3_DQ56
182	DQ61	DDR3_DQ61
192	DQ62	DDR3_DQ62
194	DQ63	DDR3_DQ63
186	DQS#7	DDR3_DQS#7
188	DQS#7	DDR3_DQS#7

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Power-Up/Down Sequence

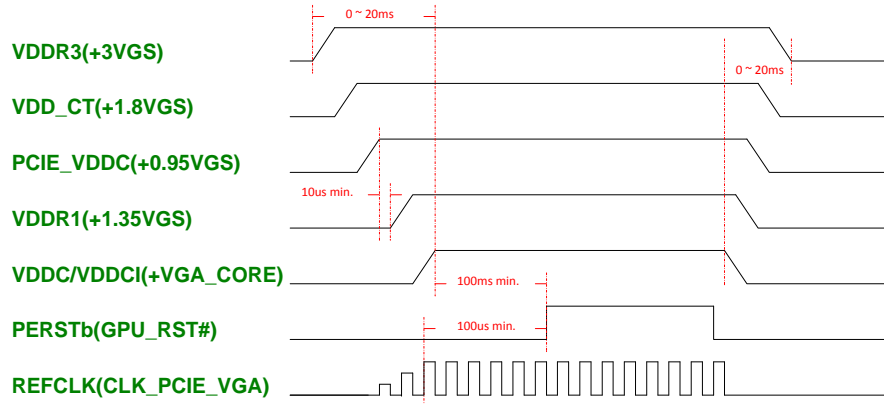
"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/ μ s).

For power down, reversing the ramp-up sequence is recommended.




CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	X 1= support
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	X 1= Enable
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	X 0= Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. (Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C (New)	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646E-BC1A (New no AVL)	001	8.45K	2K

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9 PCIe_CTX_C_GRX_P[3..0] PCIe_CTX_C_GRX_P[3..0]

9 PCIe_CTX_C_GRX_N[3..0] PCIe_CTX_C_GRX_N[3..0]

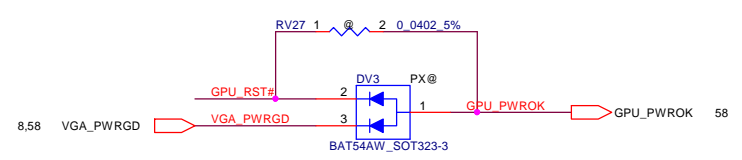
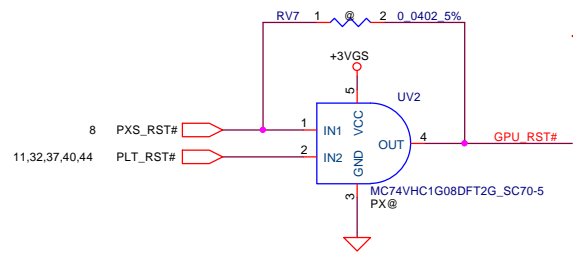
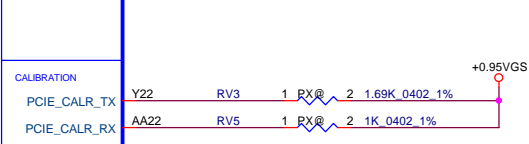
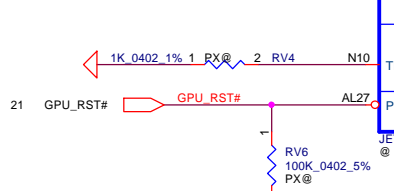
PCIE_CRX_GTX_P[3..0] PCIe_CRX_GTX_P[3..0] 9

PCIE_CRX_GTX_N[3..0] PCIe_CRX_GTX_N[3..0] 9



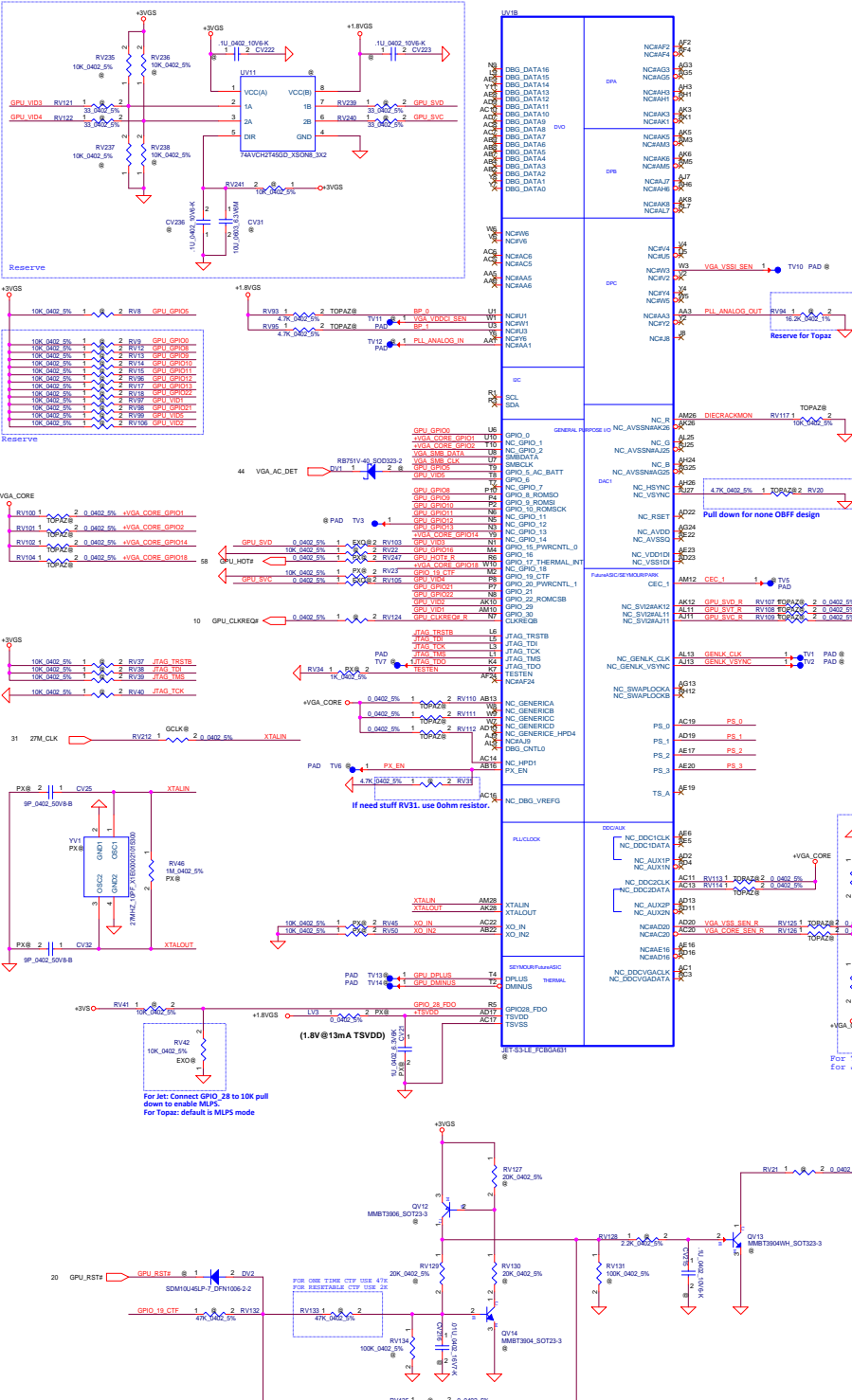
10 CLK_PCIE_GPU CLK_PCIE_GPU AK30

10 CLK_PCIE_GPU# CLK_PCIE_GPU# AK32



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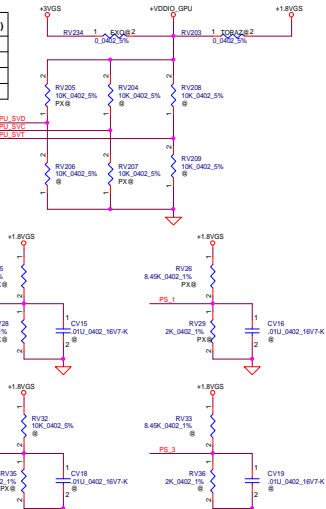


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET

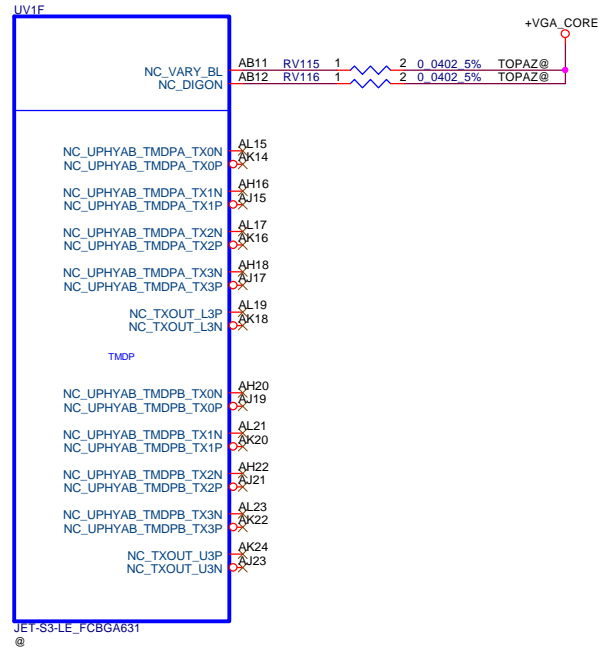
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_3[1]	ROM_CFG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	X
PS_3[2]	ROM_CFG[1]	Define the memory aperture size when STRAP_BIOS_ROM_EN = 0	100 = 2GBMB
PS_3[4]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_3[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of auto-capable display outputs.	1
PS_3[11]	STRAP_BIF_GENL_EN_L	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	1 = GEN3 is supported
PS_3[12]	STRAP_BIF_CLK_MLEN	0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.	0
PS_3[13]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_3[14]	STRAP_TX_CPD_DRV_FULL_SWING	0 = The transmitter full-swing is enabled. 1 = The transmitter full-swing is disabled.	1
PS_3[15]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1 = Enable
PS_3[1]	N/A	Reserved.	0
PS_3[2]	N/A	Reserved.	0
PS_3[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable X
PS_3[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_3[5]	N/A	Reserved.	1
PS_3[11]	BOARD_CONFIG[0]	Board configuration related strapings, such as for memory ID	X
PS_3[12]	BOARD_CONFIG[1]	00 = Hynix 556M16 01 = Hynix 128M16 02 = Samsung 256M16 03 = Samsung 256M16 04 = Micron 256M16	01 = Hynix 128M16 02 = Samsung 256M16 11 = Micron 128M16
PS_3[13]	BOARD_CONFIG[2]	Determines the maximum number of digital display audio endpoints that will be generated by the OS and used (combine with PS_3[5])	11 = No usable endpoints. 10 = One usable endpoint. 01 = Two usable endpoints. 00 = Three usable endpoints. 01 = Four usable endpoints. 00 = Five usable endpoints. 00 = Six usable endpoints. 00 = Six usable endpoints.
PS_3[14]	AUD_PORT_CONN_PINSTRAP[1]		11 = No usable endpoints.
PS_3[15]	AUD_PORT_CONN_PINSTRAP[0]		11

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Capacitor Value (nF)	Bits [5:4]	R_pu (Ω)	R_pd (Ω)	Bits [3:1]
680	00	NC	4750	000
82	01	8450	2000	001
50	10	4500	2000	010
NC	11	6900	4900	011
		4500	4900	100
		3240	5620	101
		3420	10000	110
		4750	NC	111

Note: 0402 1% resistors are required.



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+1.8VGS
0.0603_5%
1 2 RV48
PX@

(1.8V@40mA DP_VDDR)

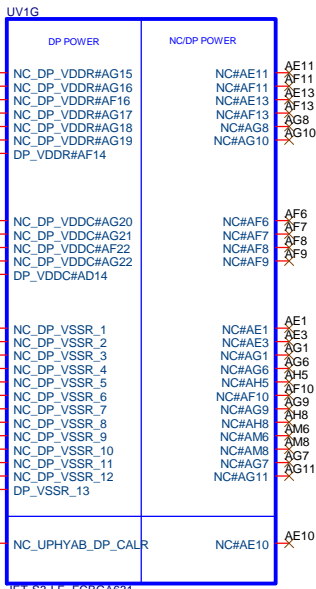
+DP_VDDR

+0.95VGS
0.0603_5%
1 2 RV47
PX@

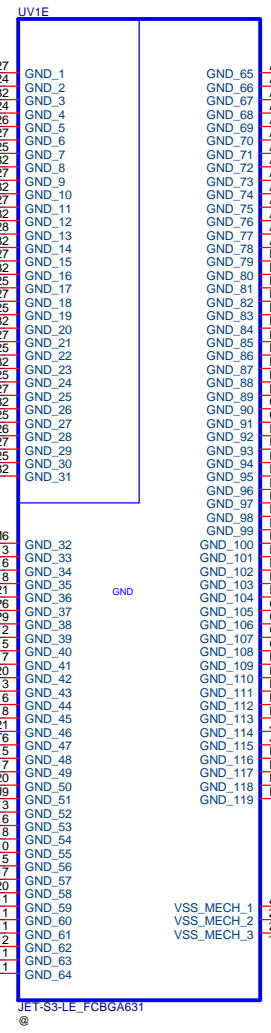
(0.95V@32mA DP_VDDC)

+DP_VDDC

RV49 1 2
150_0402_1%
AF17



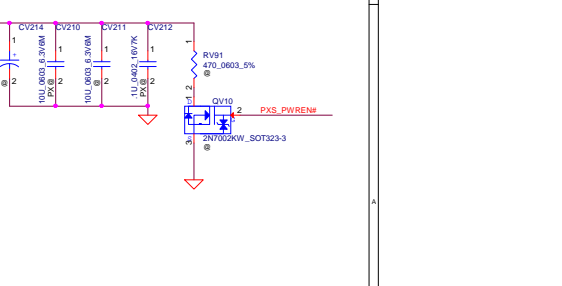
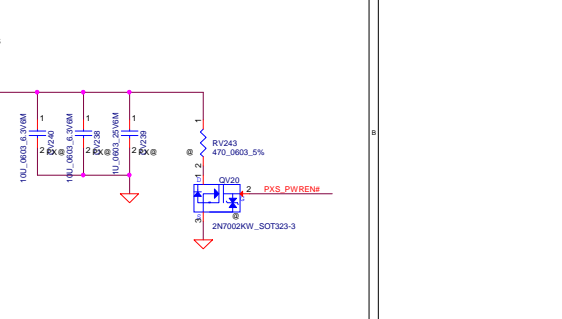
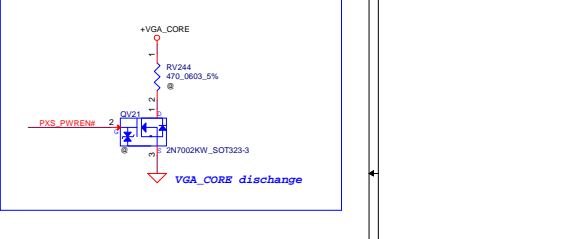
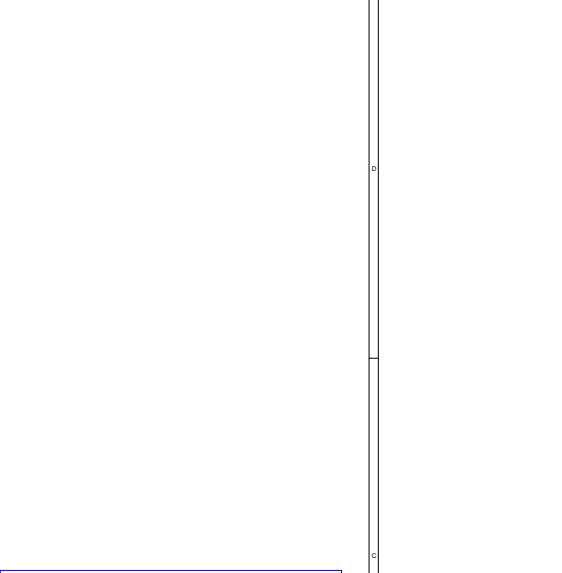
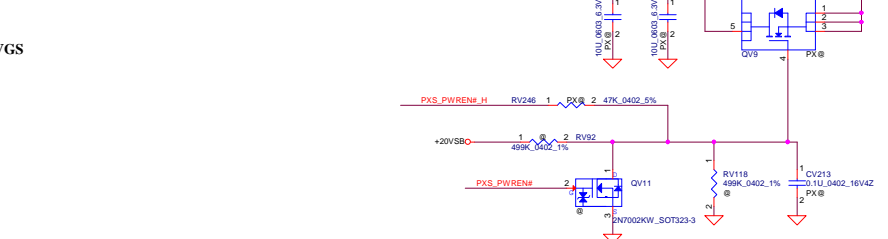
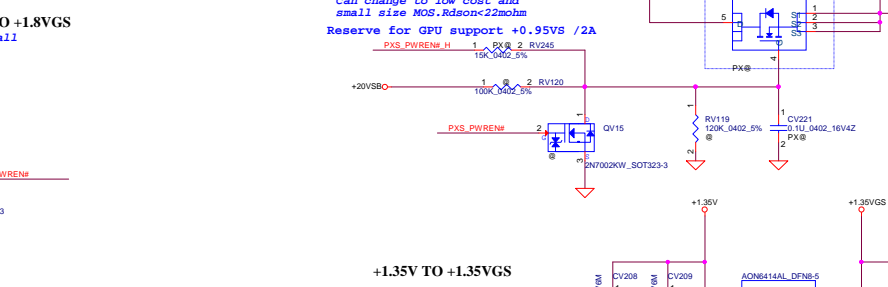
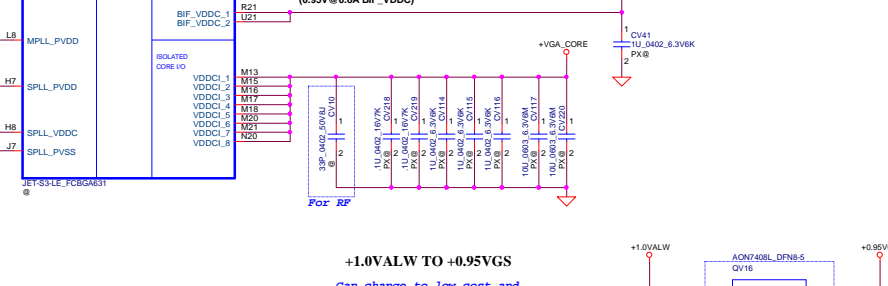
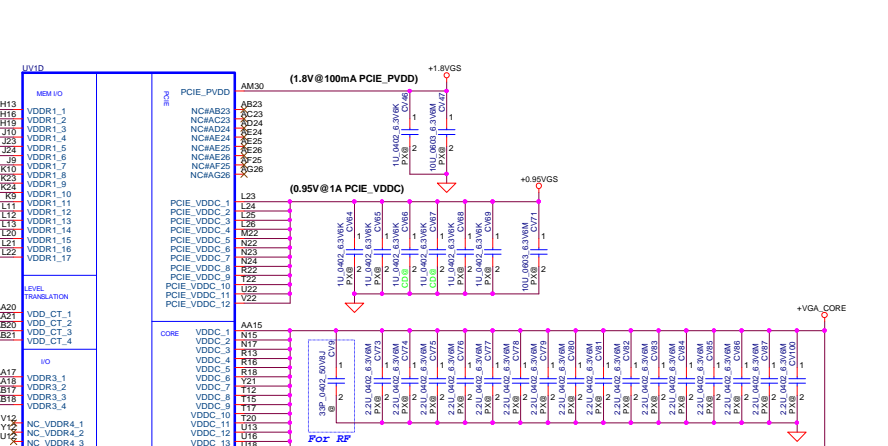
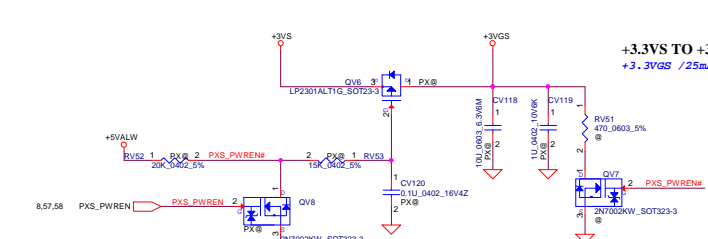
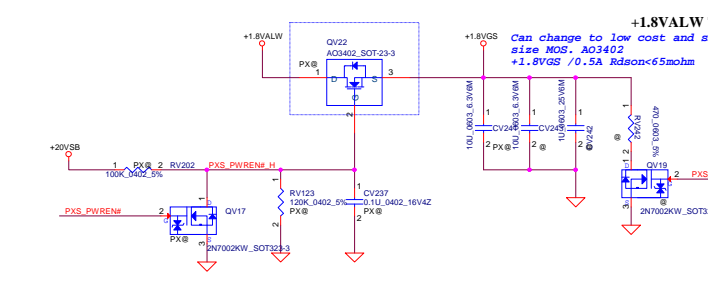
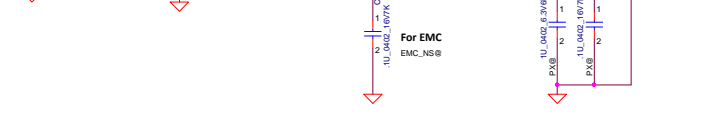
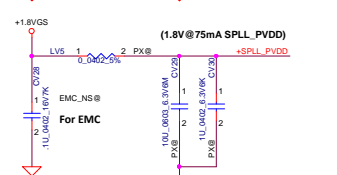
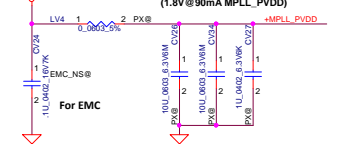
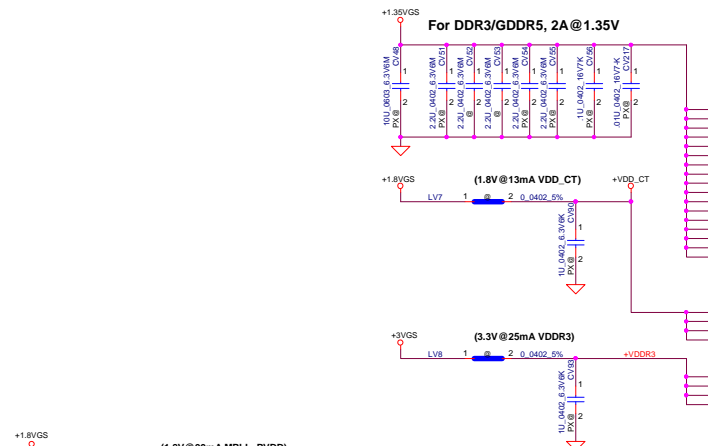
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JET-S3-LE_FCBGA631

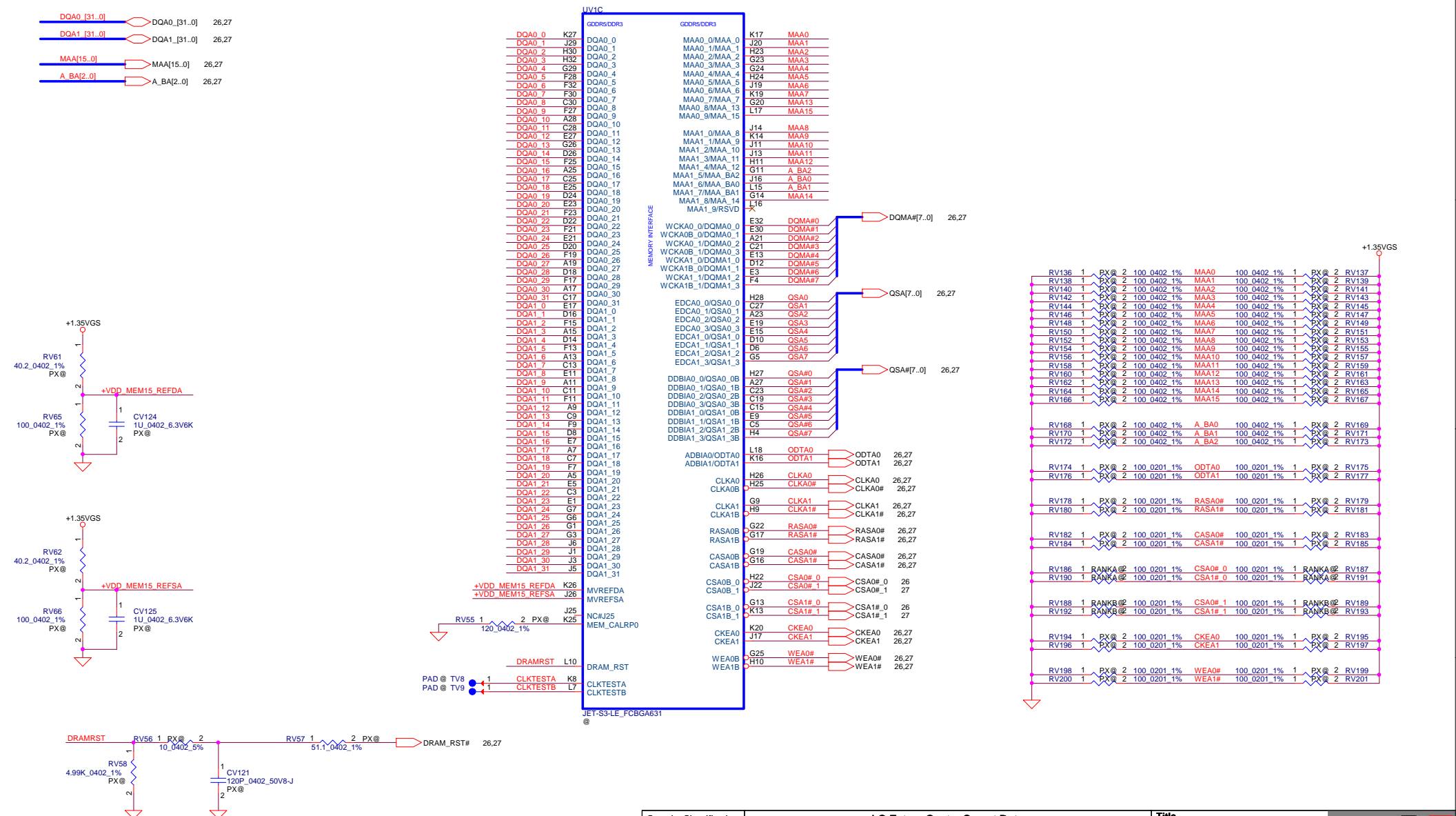
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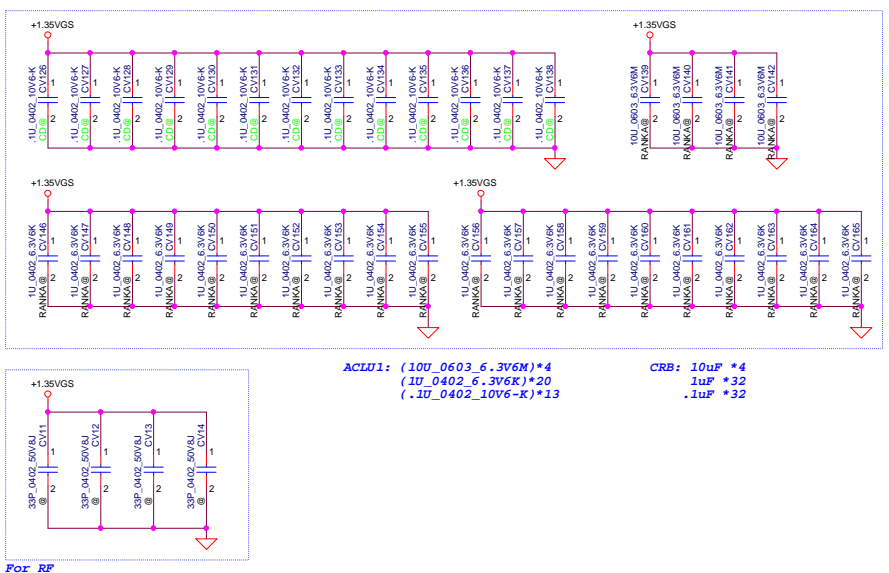
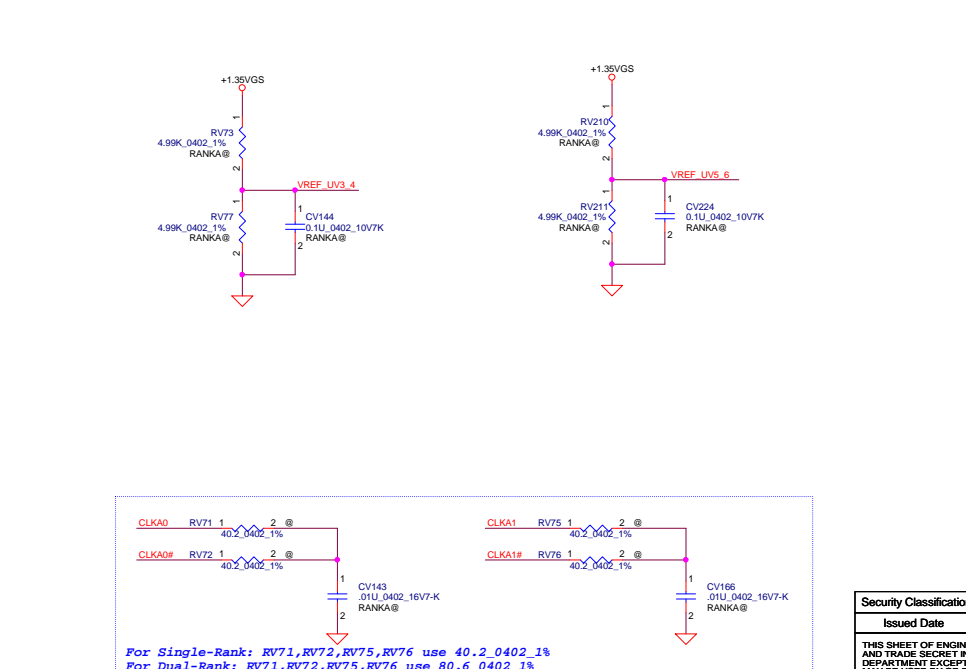
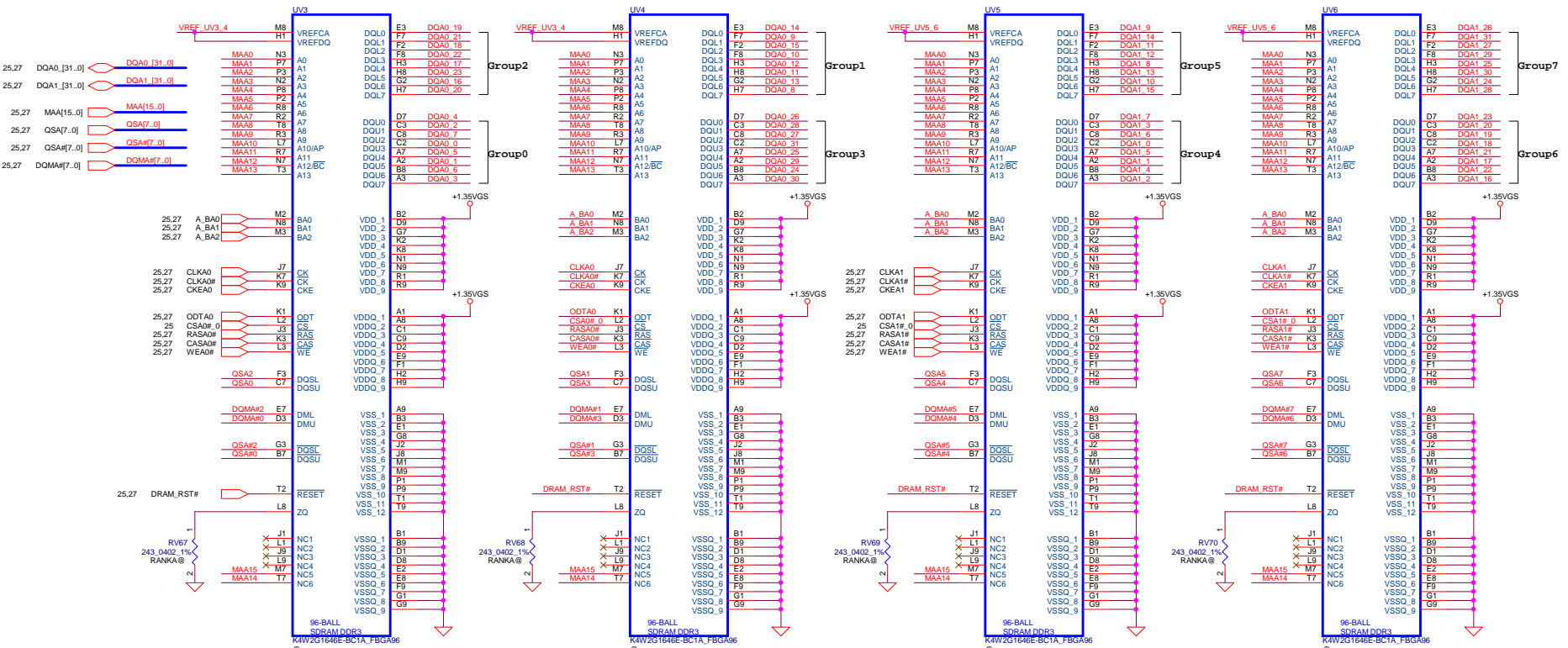


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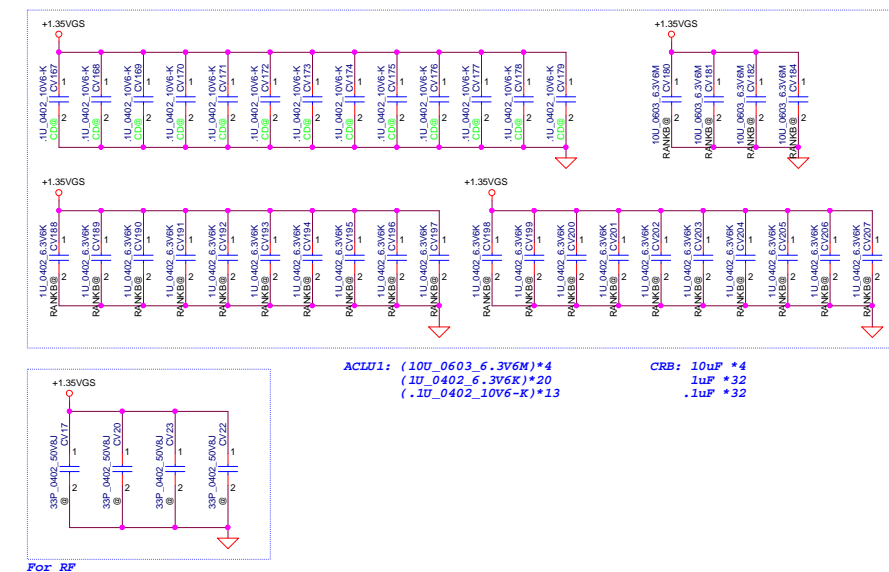
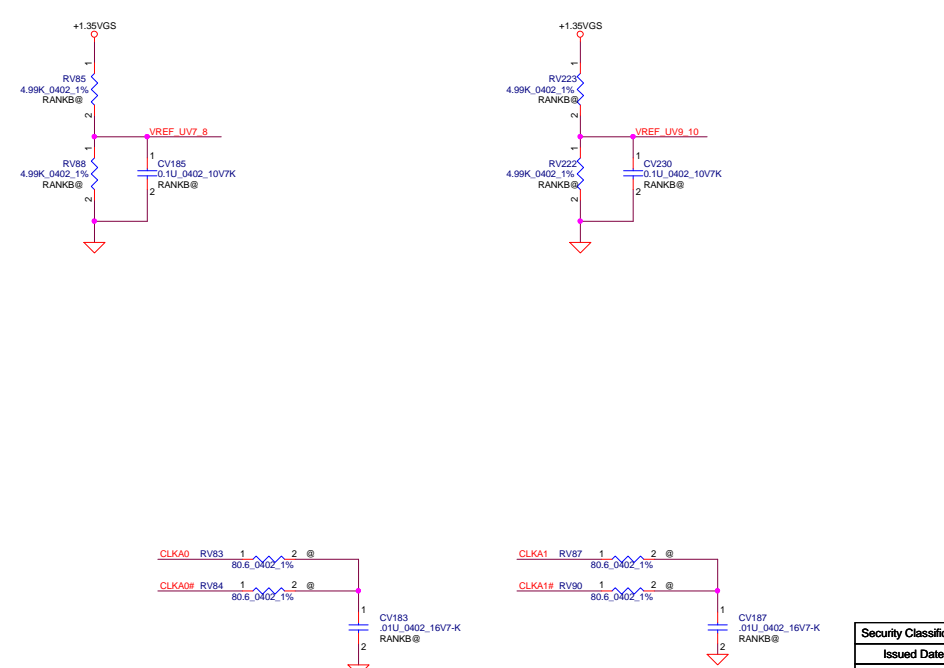
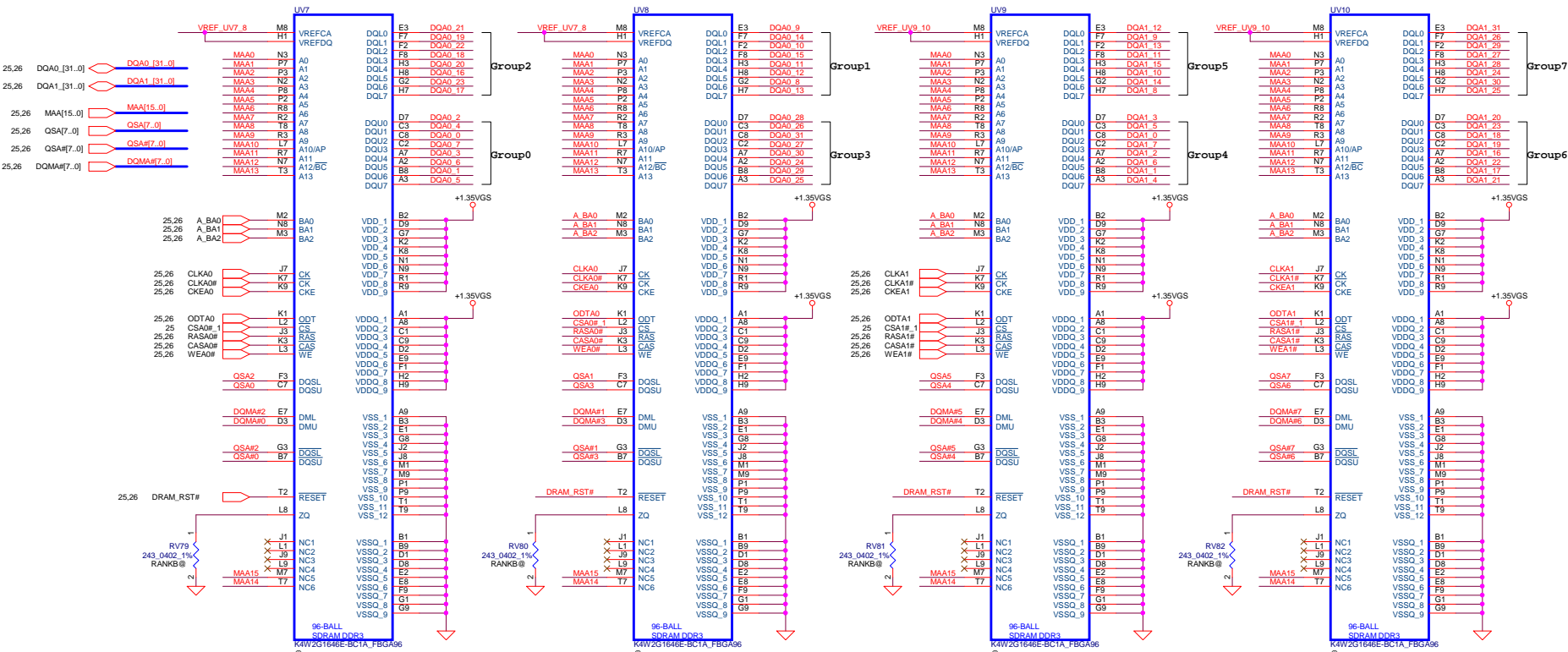
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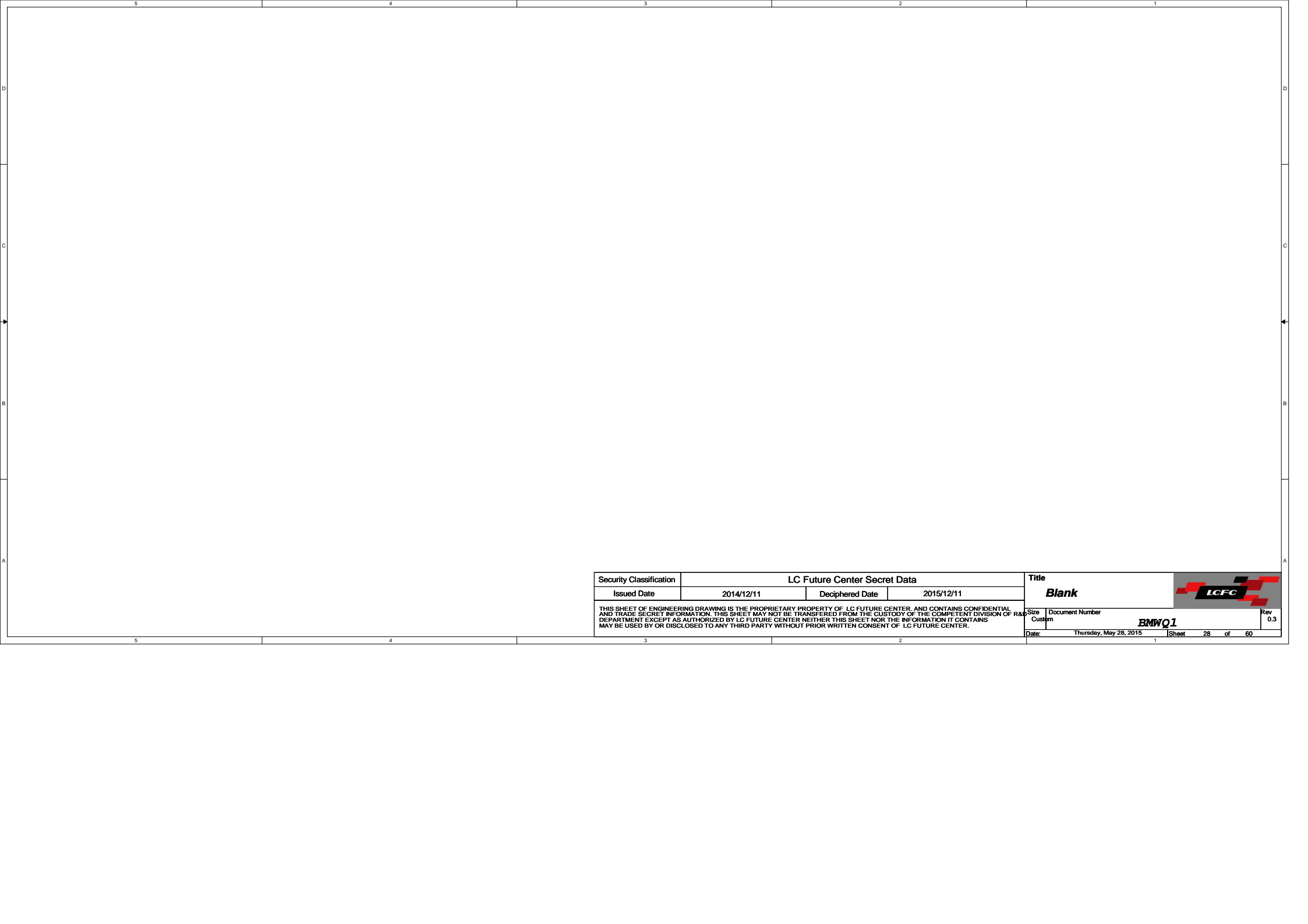
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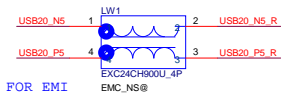
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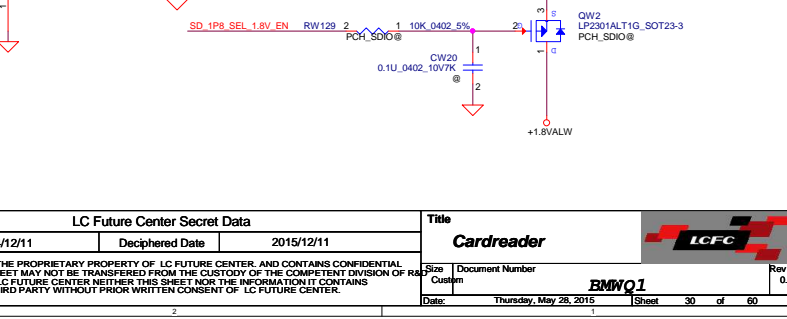
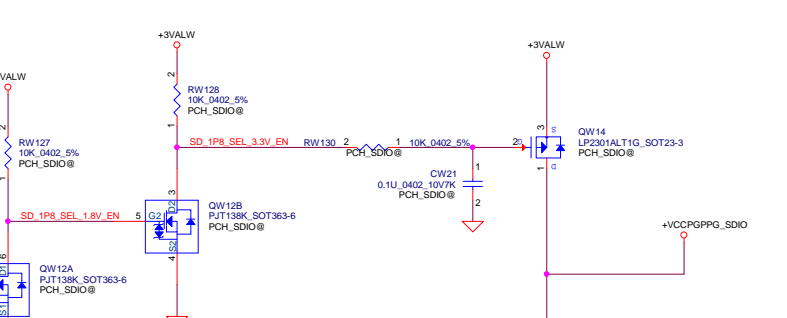
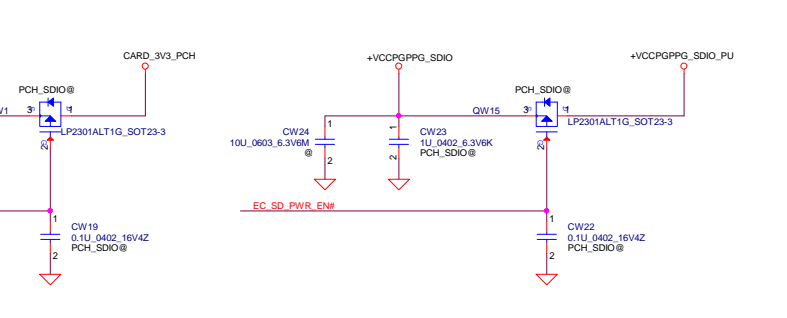
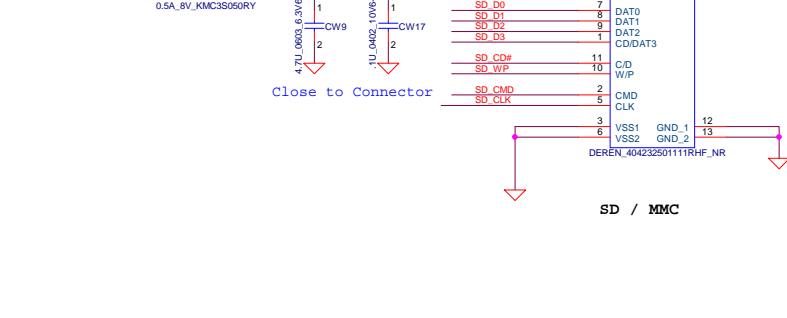
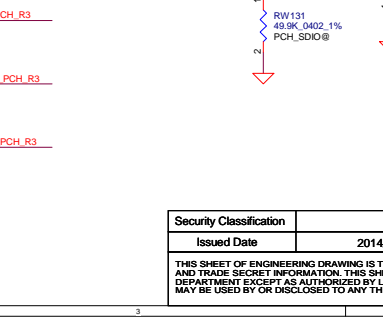
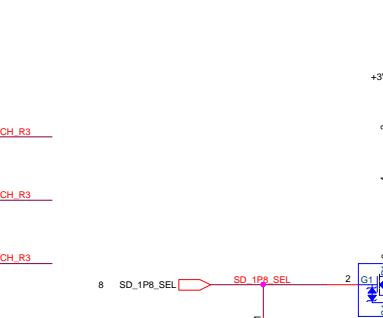
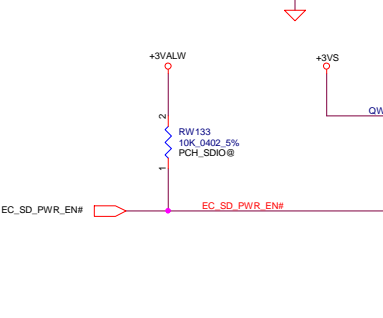
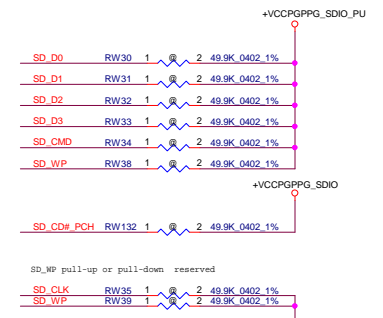
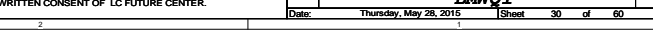
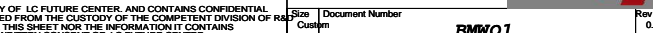
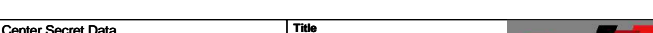
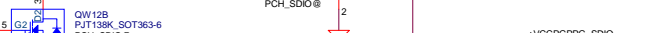
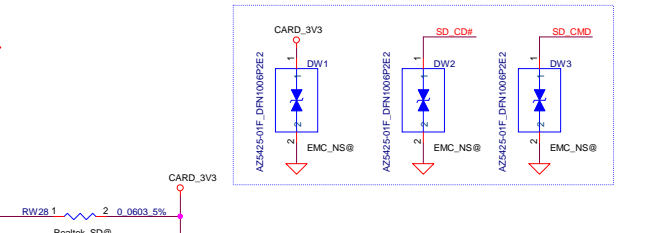
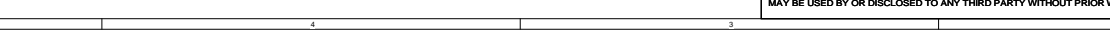
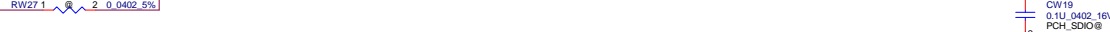
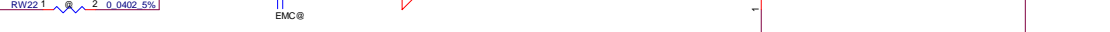
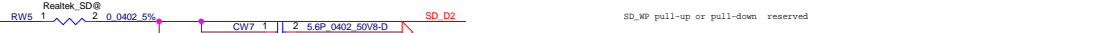
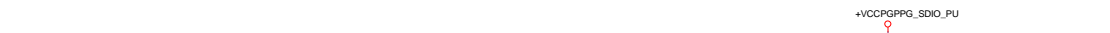
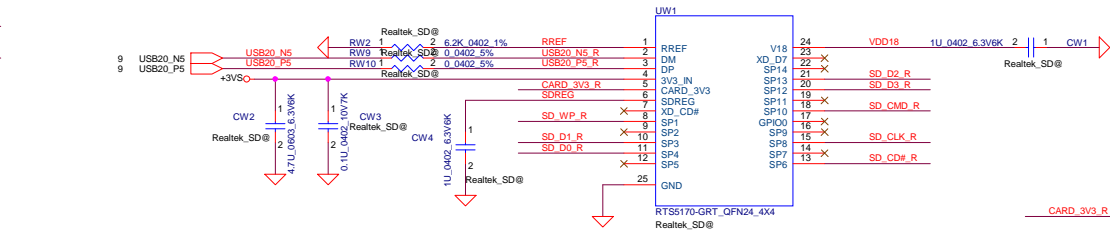
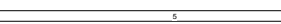
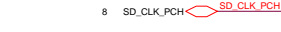
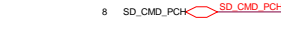
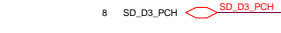
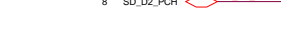
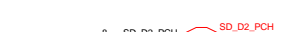
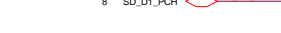
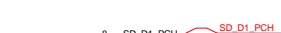
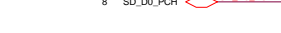
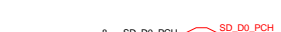
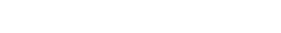
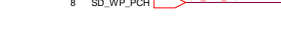
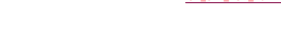
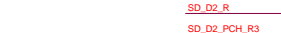
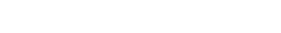
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				Custom	0.3
				Date:	Thursday, May 28, 2015
				Sheet	28 of 60

5	4	3	2	1
A	B	C	D	A
Security Classification				LC Future Center Secret Data
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				Document Number
				Rev
				Date: Thursday, May 28, 2015
				Sheet 29 of 60
				BMQ1
				0.3

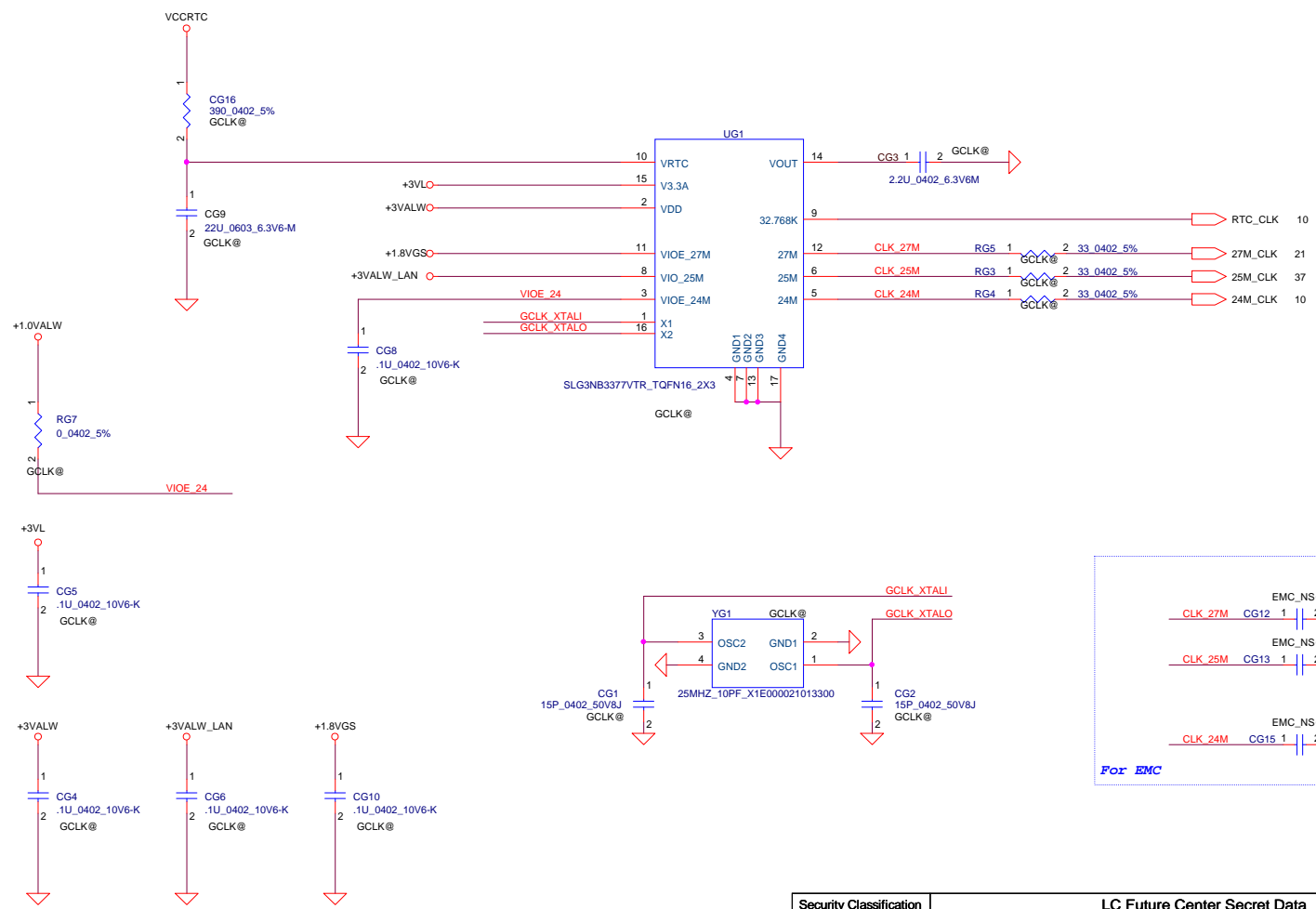





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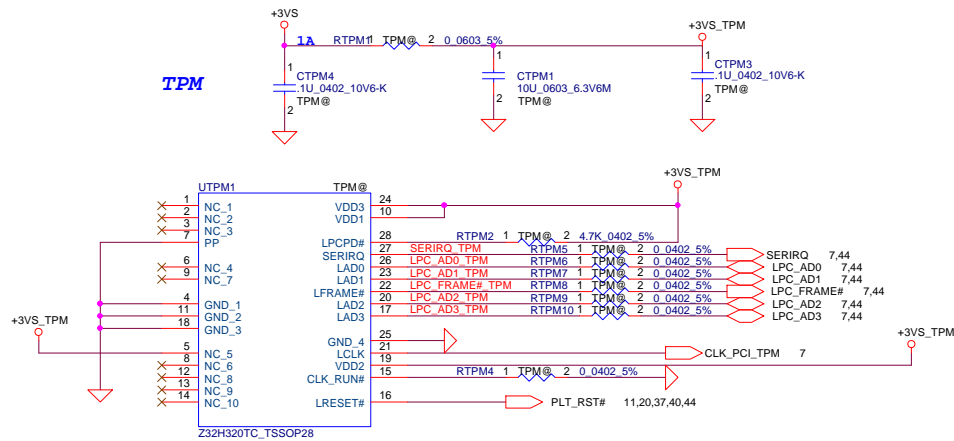




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Size	Document Number	Customer	Rev	0.3	
Date	Thursday, May 28, 2015	Sheet	30	of 60	



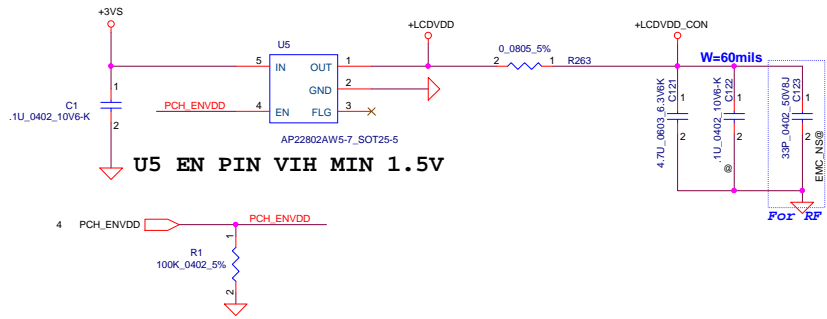
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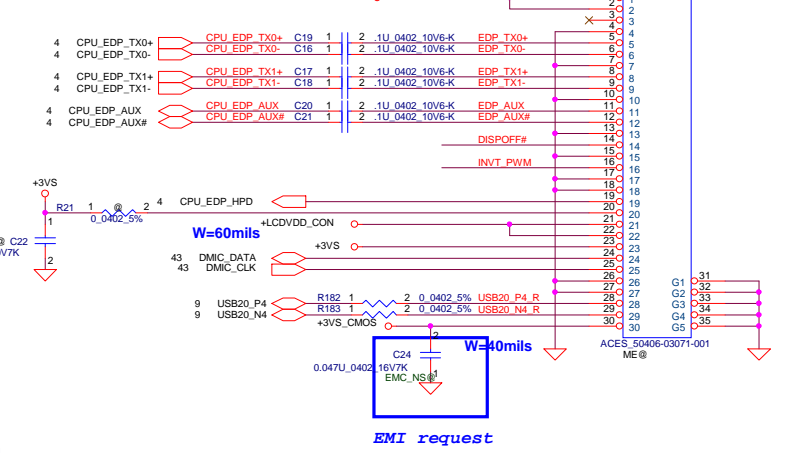
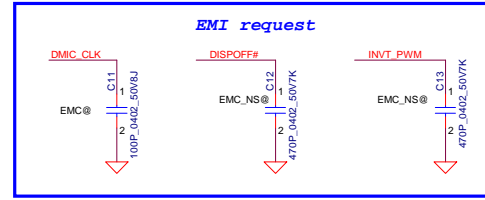
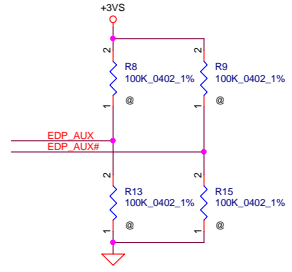
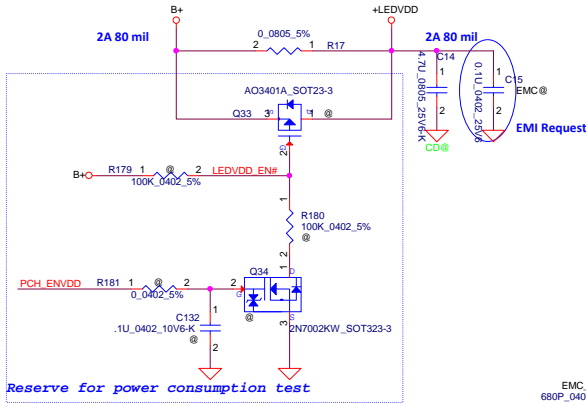
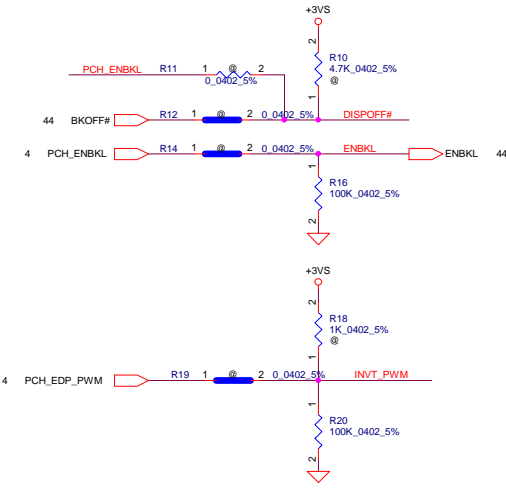
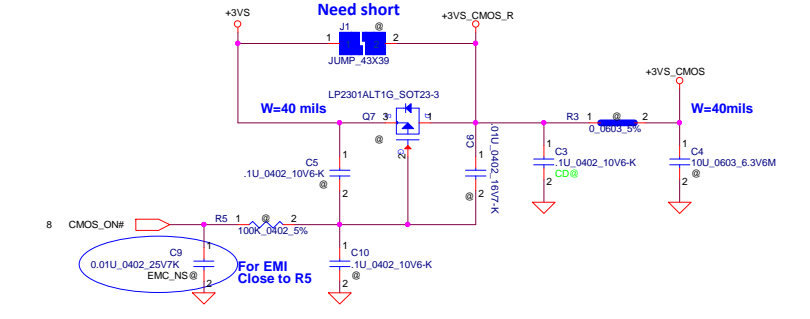


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Issued Date	2014/12/11	Deciphered Date	2015/12/11	TPM		
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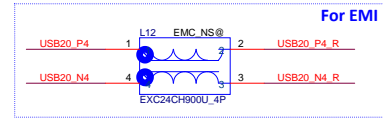
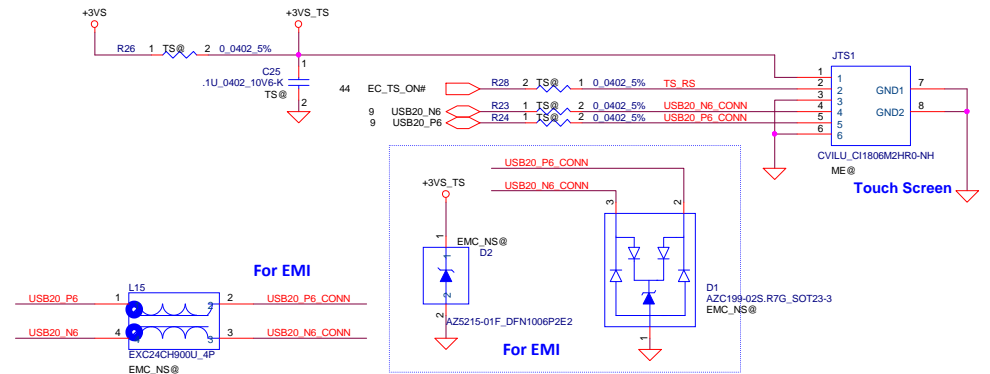
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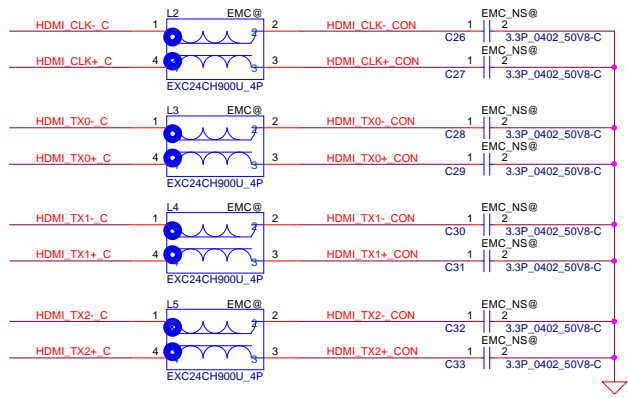


CMOS Camera

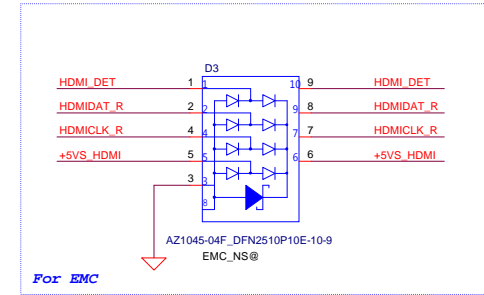
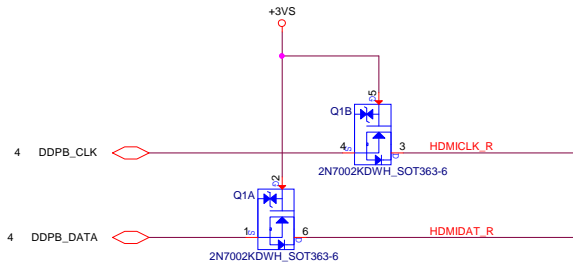
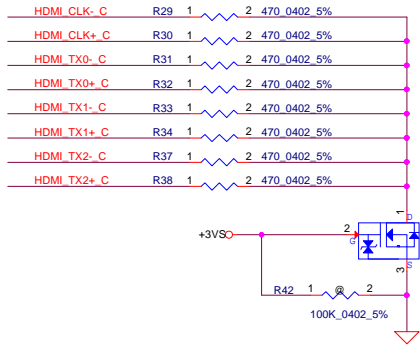


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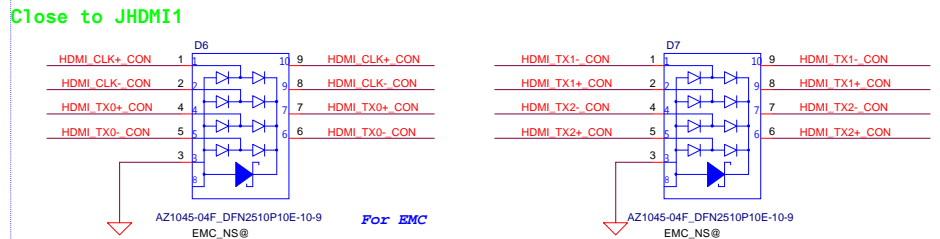
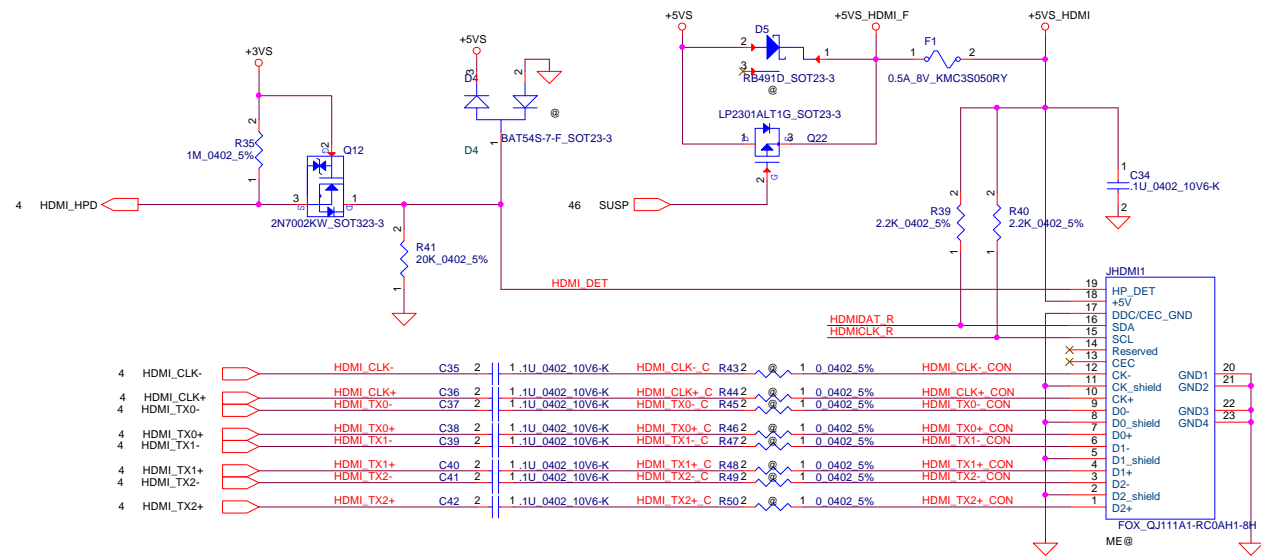




For EMC



For EMC

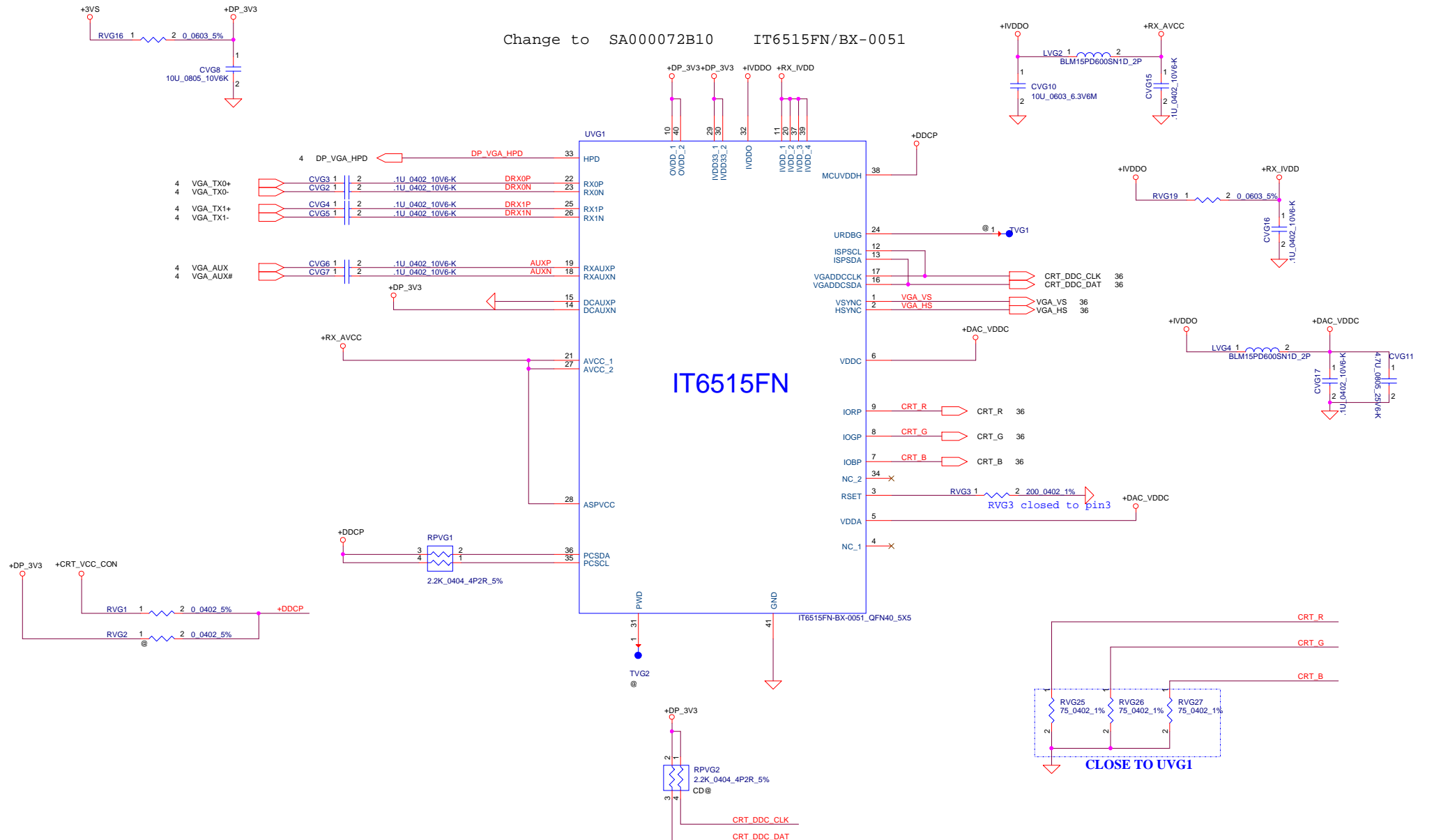


For EMC

For EMC

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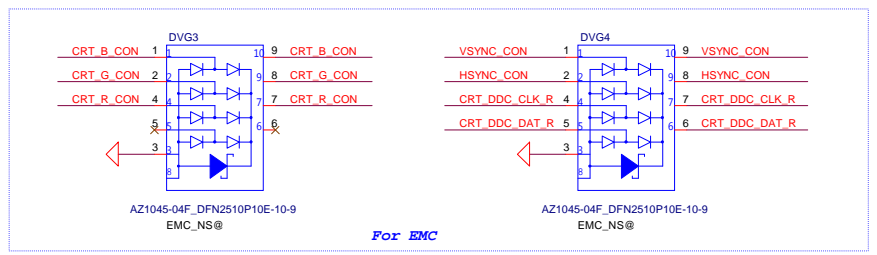
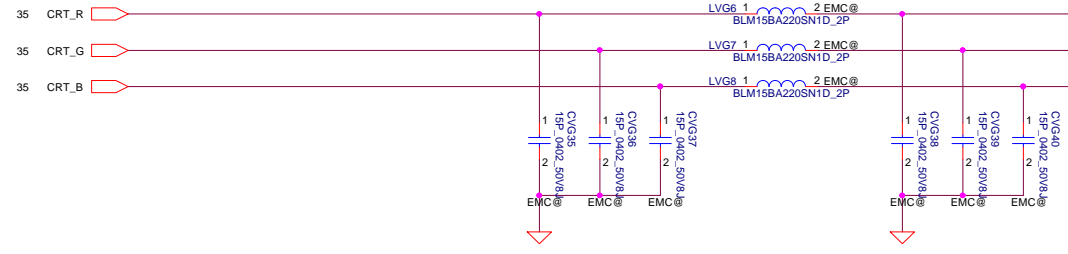
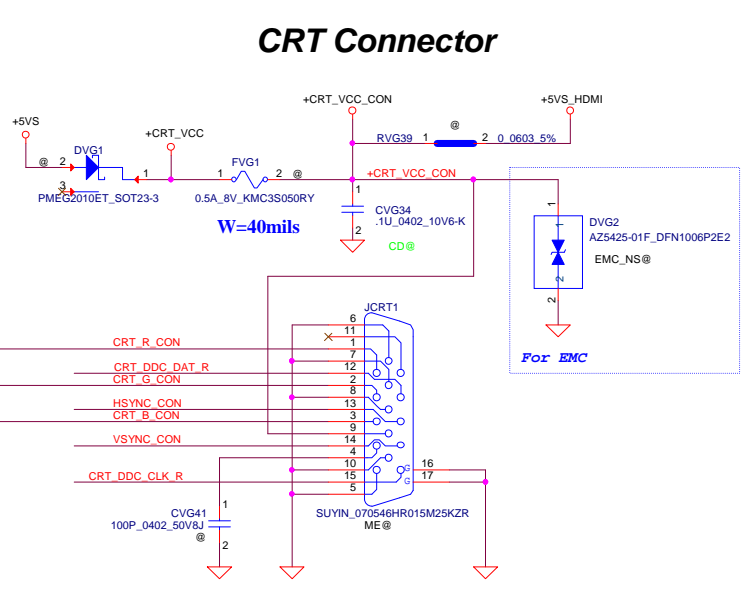
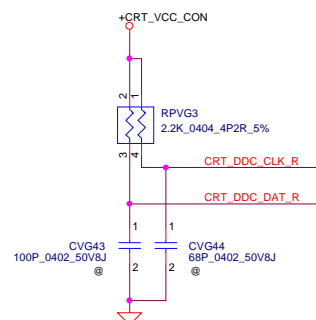
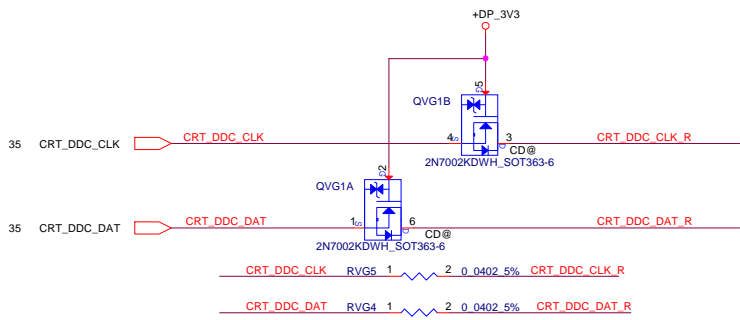
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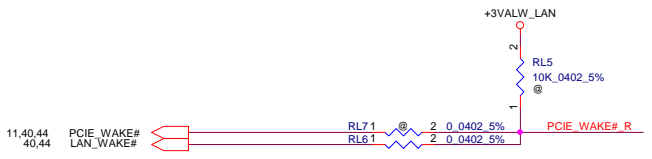
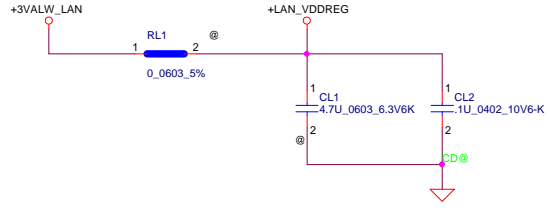
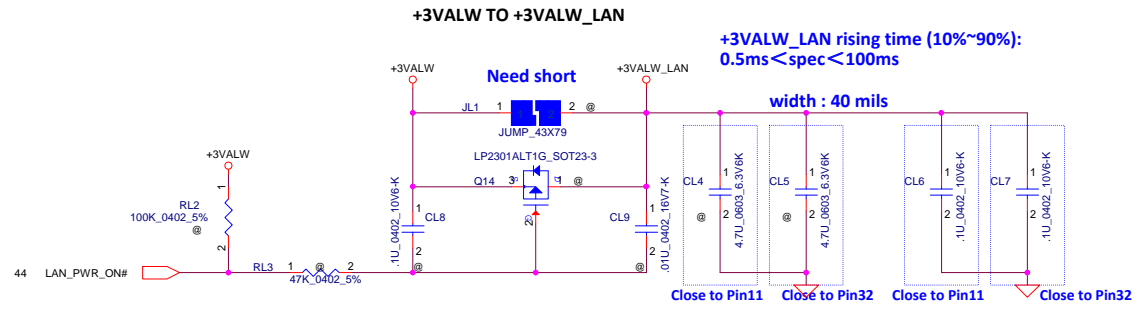
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Document Number	BMWQ1	
Rev	0.3	



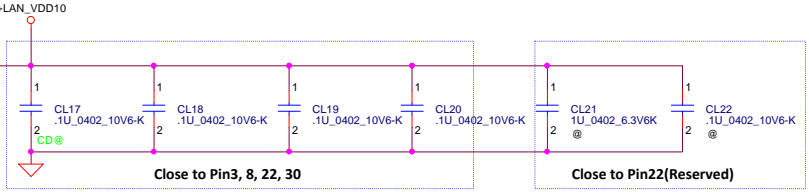
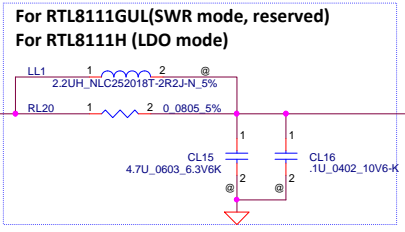
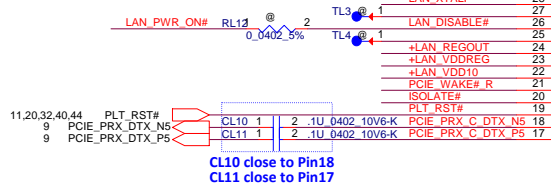
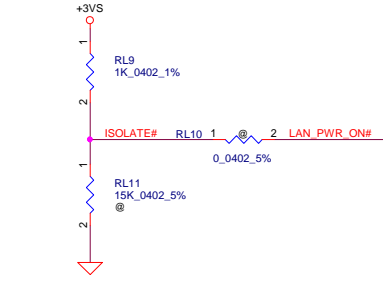
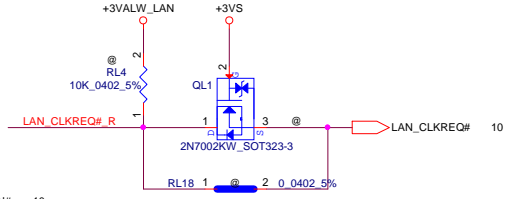
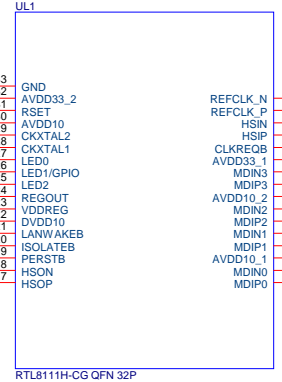
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Title	Document Number	Rev
CRT_CONN	BMWQ1	0.3
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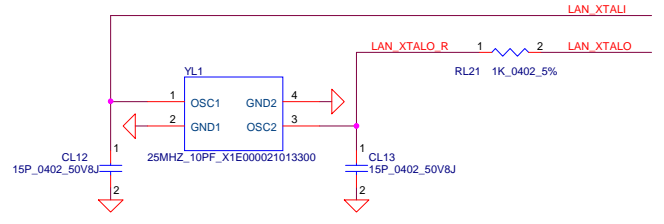




manual change the Codec PN to RTL8111H-CG QFN

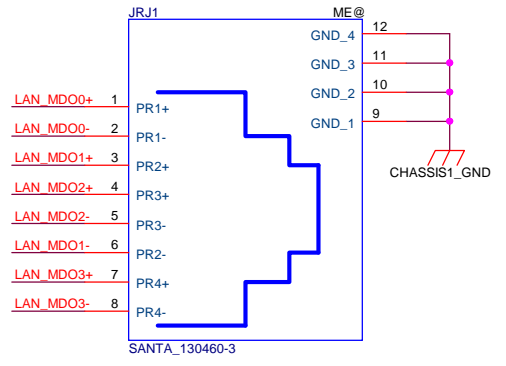
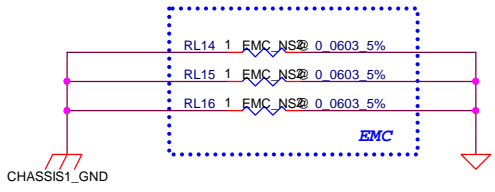
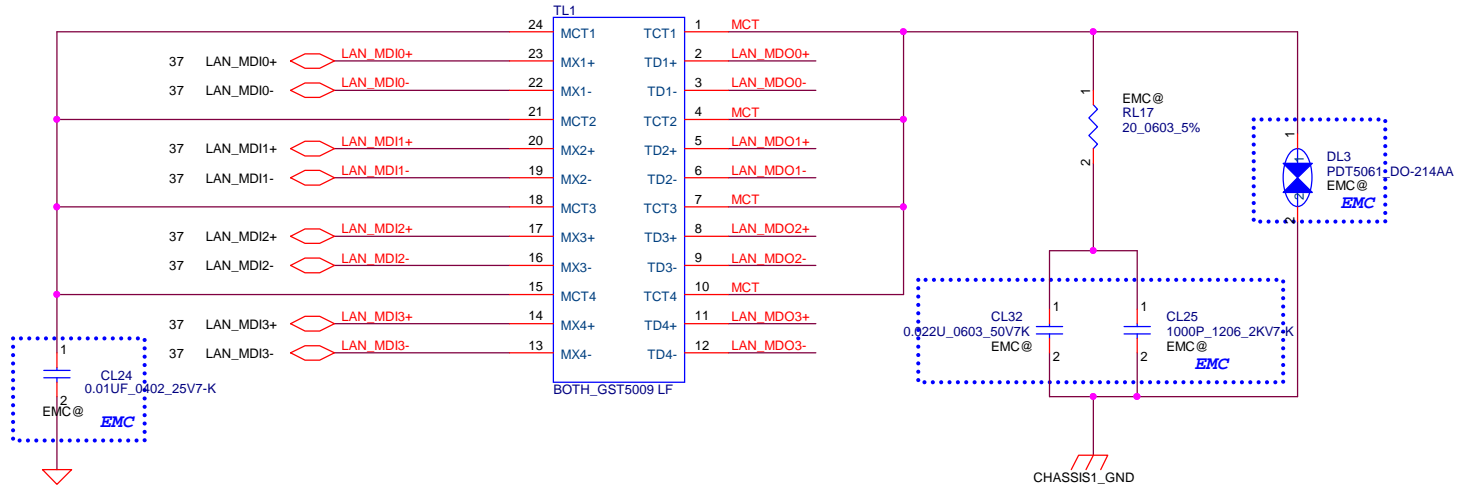
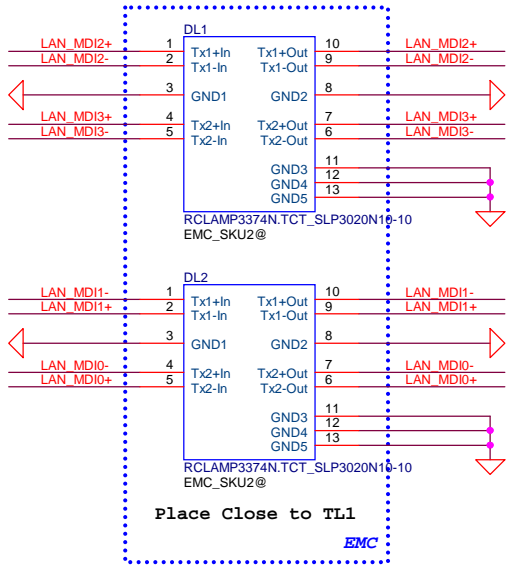


Layout Note: LL1 must be within 200mil to Pin24, CL15, CL16 must be within 200mil to LL1, +LAN_REGOUT: Width =60mil



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Size	Document Number	Date		Sheet	Rev
Custom	BMWQ1	Thursday, May 28, 2015		37	0.3
				of	60

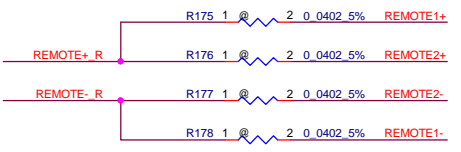
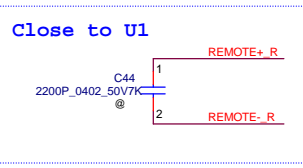
DL1/DL2
1'S PN:SC300003M00



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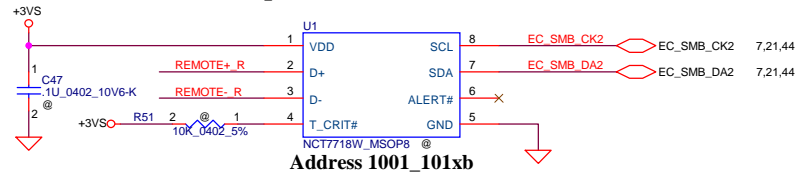


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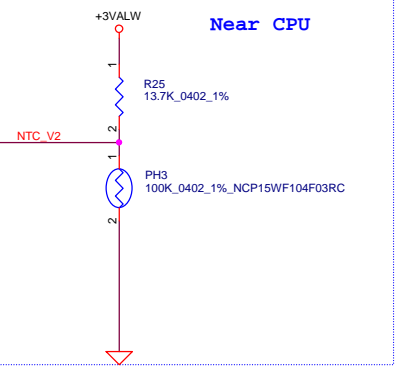
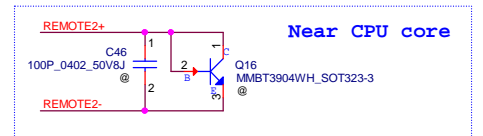
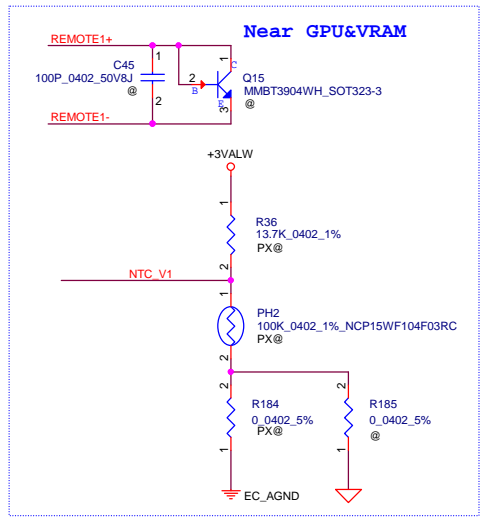


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

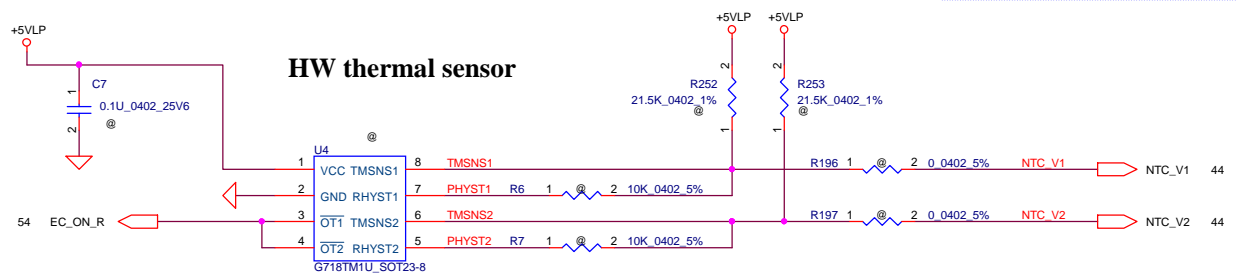


Address 1001_101xb



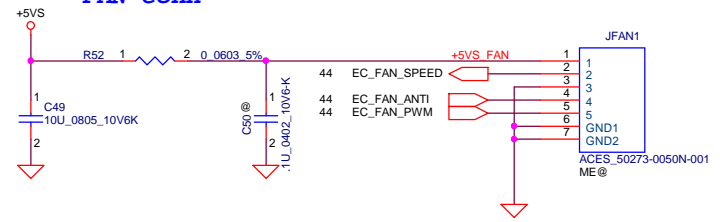
for layout optimized, change the EC_AGND to GND

HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

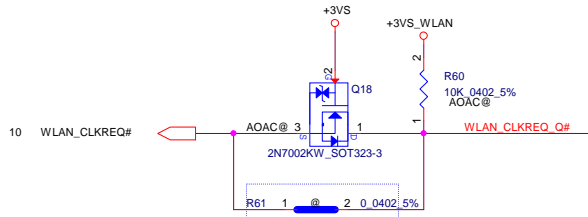
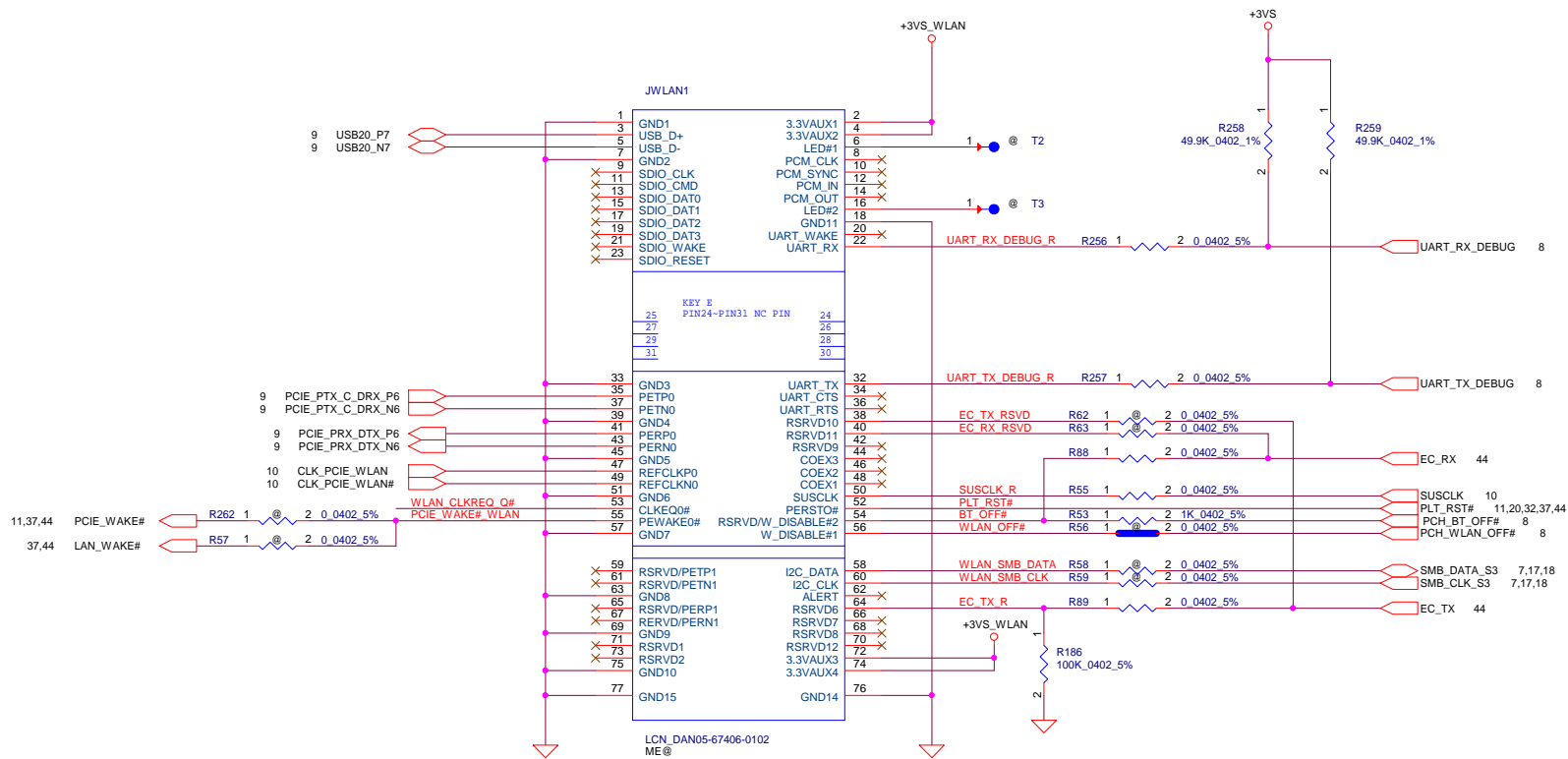
FAN Conn



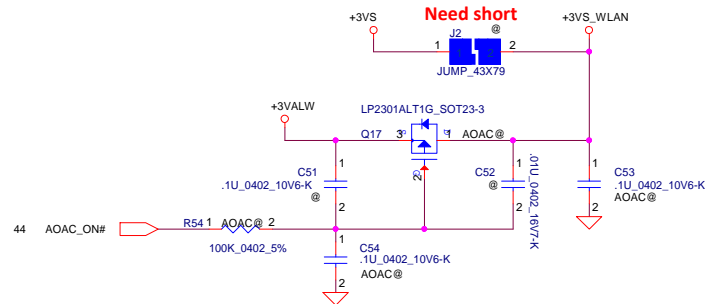
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Title		
Thermal sensor/FAN CONN/TPM		
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Date:	Thursday, May 28, 2015	Sheet 39 of 60
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Mini-Express Card(WLAN/WiMAX)



If support AOAC, NC R61;
if not support AOAC, stuff R61.

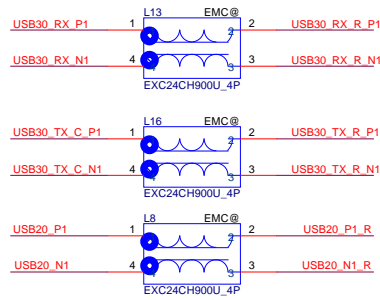
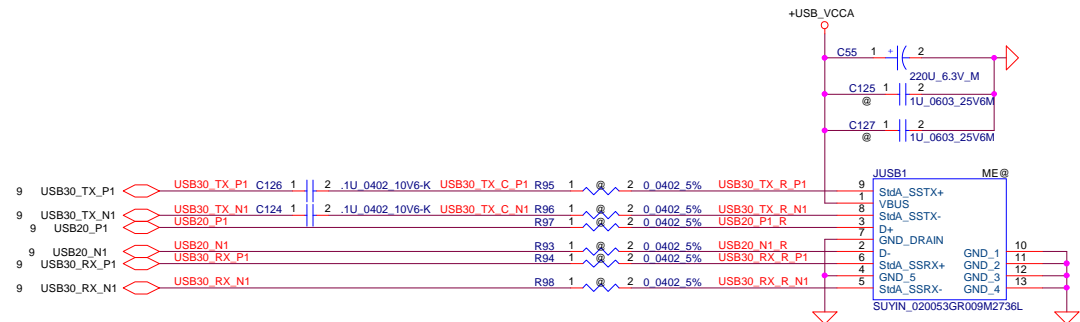
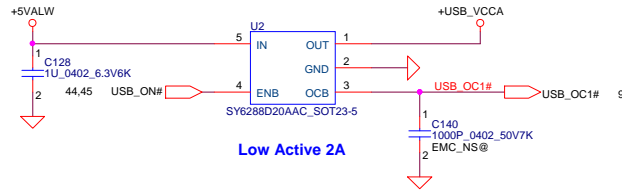


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Issued Date	2014/12/11	Deciphered Date
		2015/12/11

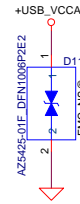
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Size	Document Number	Rev
Custom	BMWQ1	0.3
Date:	Thursday, May 28, 2015	Sheet 40 of 60

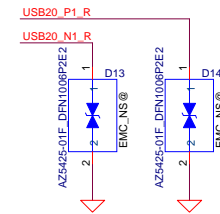
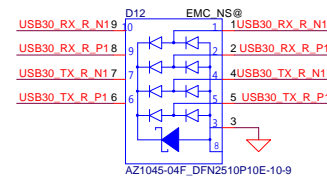
LEFT SIDE USB3.0 PORT x1



EMC

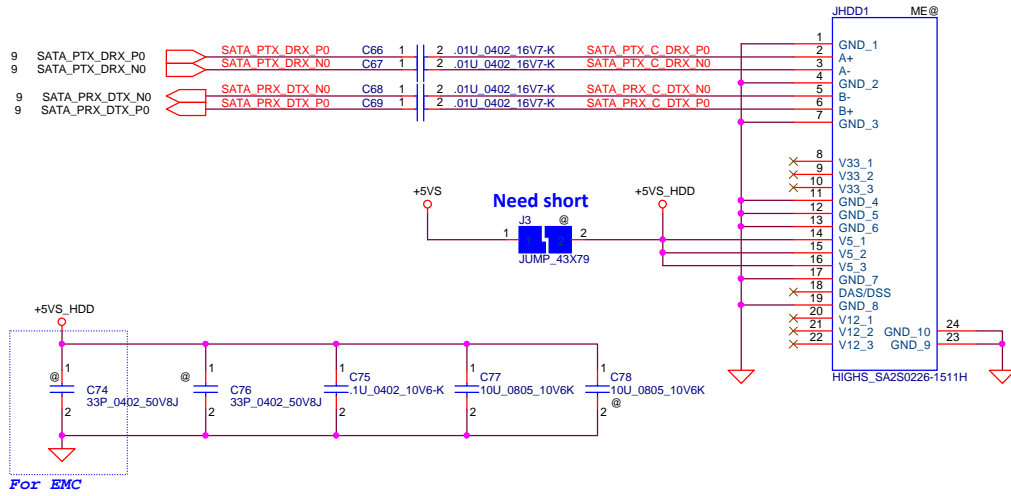


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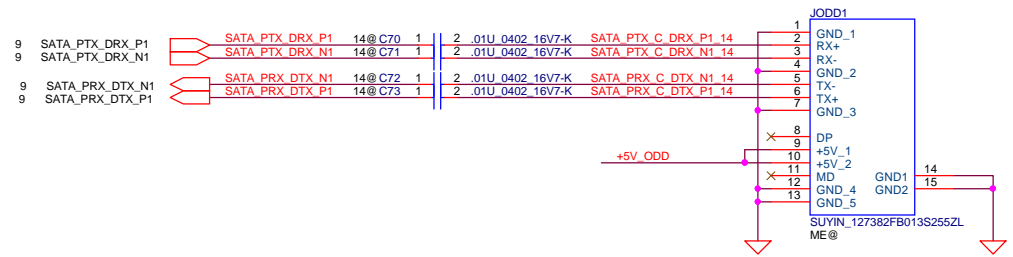


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			Document Number	0.3
			Custom	BMWQ1
			Date:	Thursday, May 28, 2015
			Sheet	41 of 60

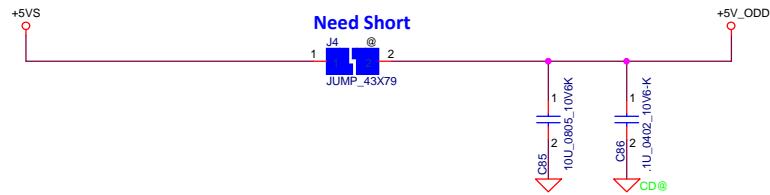
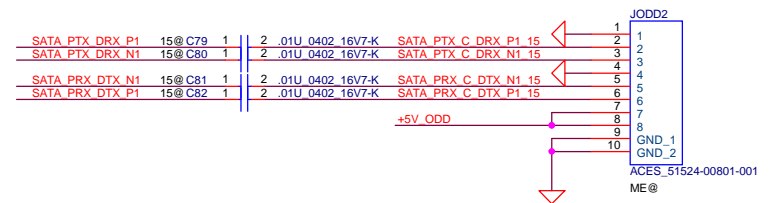
SATA HDD Conn.



FOR 14" SATA ODD Conn.

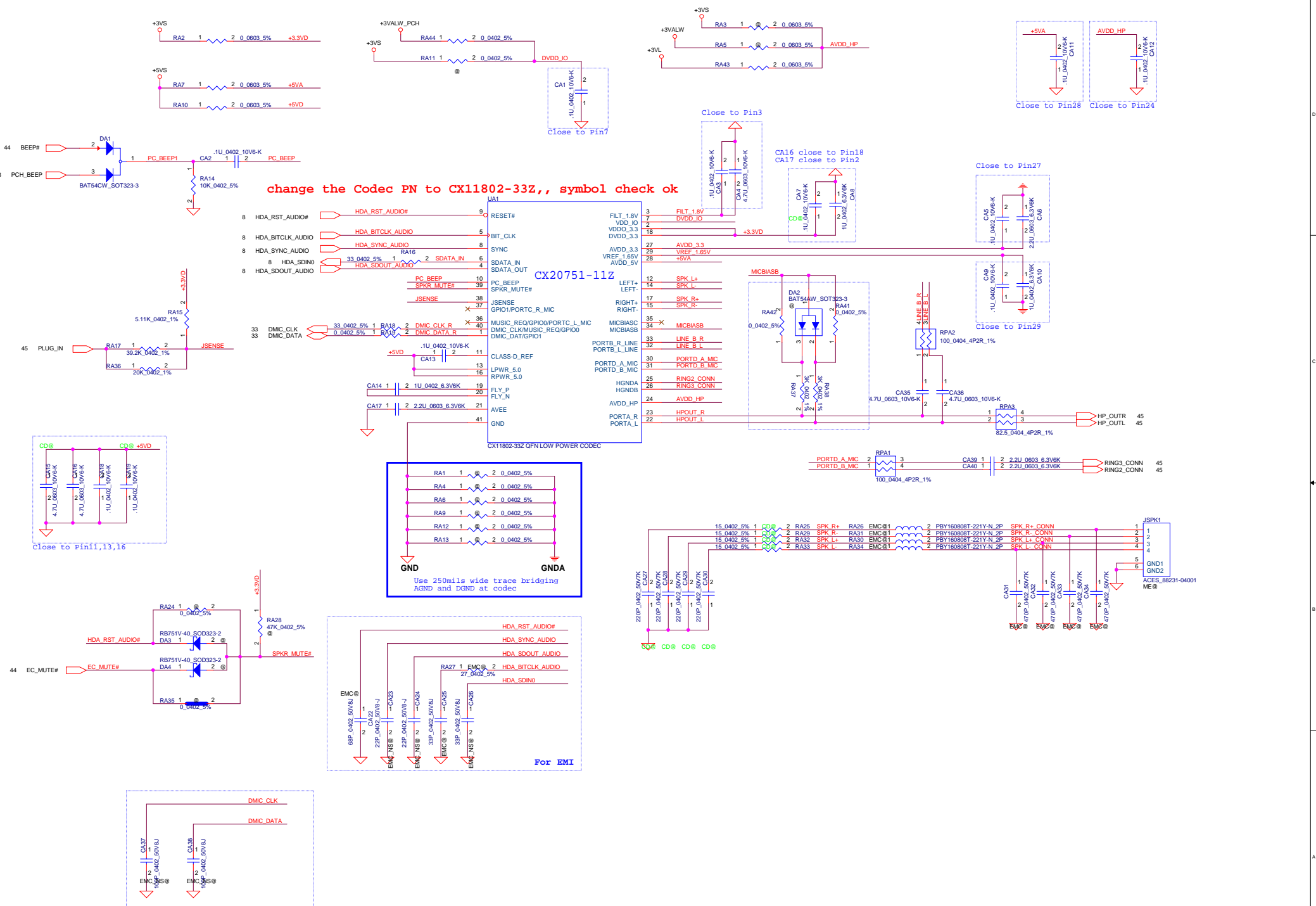


FOR 15" SATA ODD FFC Conn



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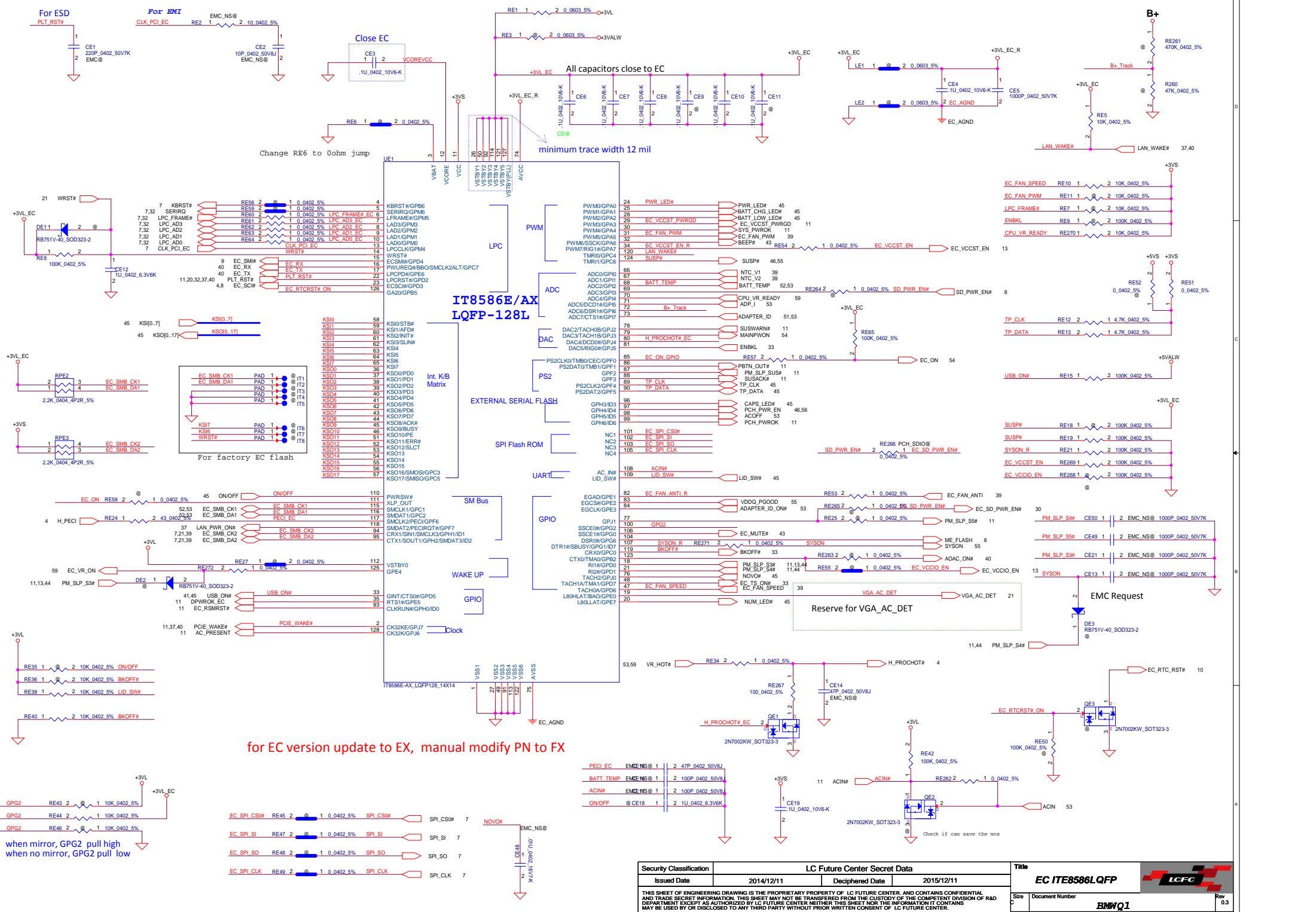
change the Codec PN to CX1802-33Z,, symbol check ok

CX20751-11Z

CX1802-33Z QFN LOW POWER CODEC

For EMI

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				Customer	BMVQ1
				Date	Thursday, May 28, 2015
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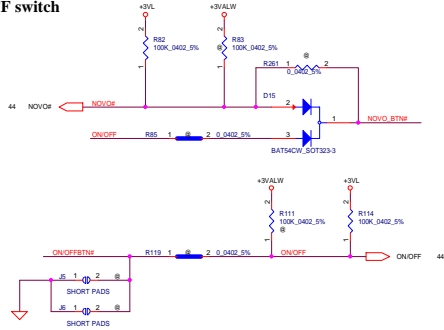


for EC version update to EX, manual modify PN to FX

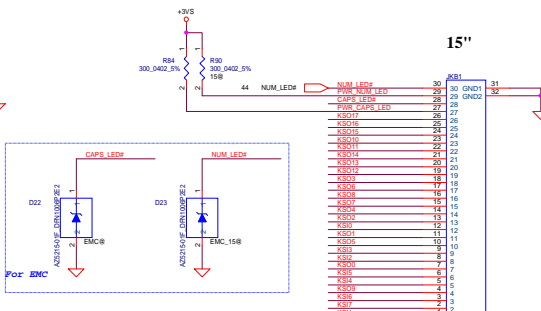
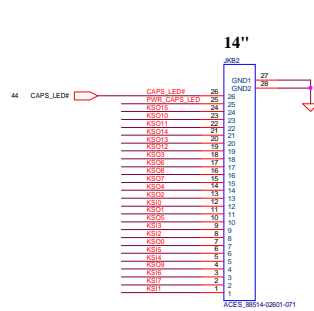
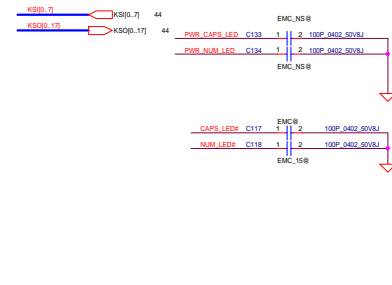
when mirror, GPG2 pull high
when no mirror, GPG2 pull low

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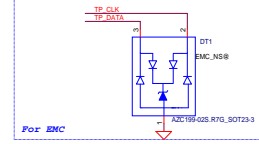
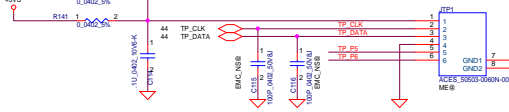
ON/OFF switch



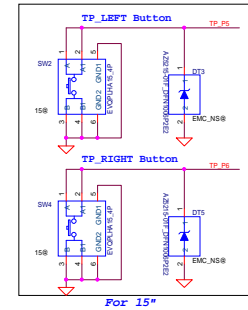
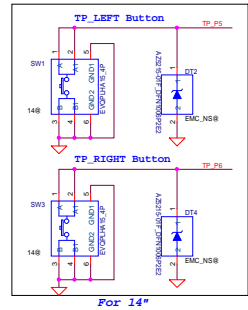
K/B Connector



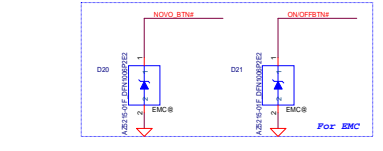
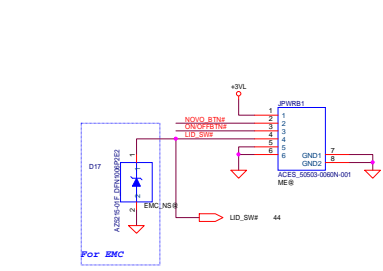
TP/B Connector



For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R

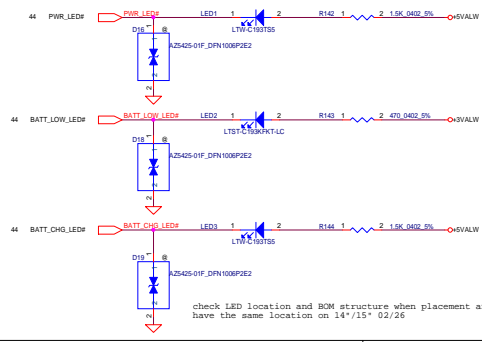
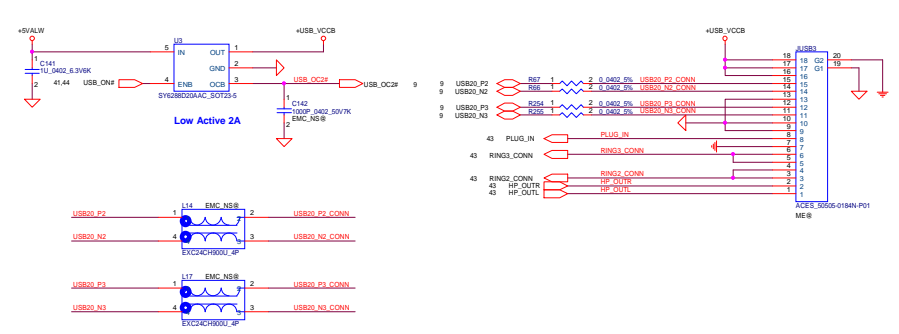


PWR/B Connector



USB I/O Connector

Right Side USB2.0 Port X 2 (USB/B)



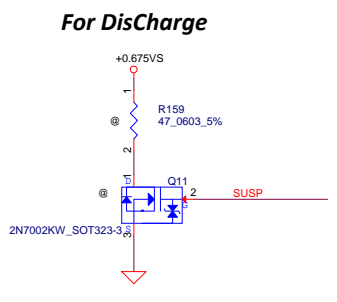
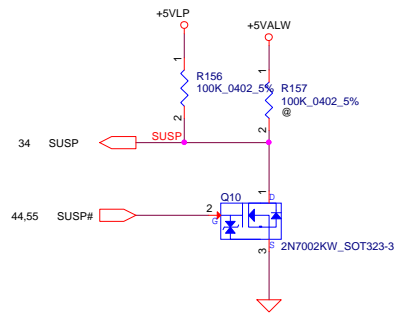
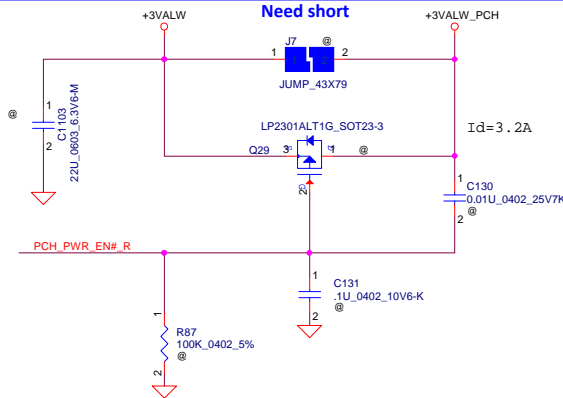
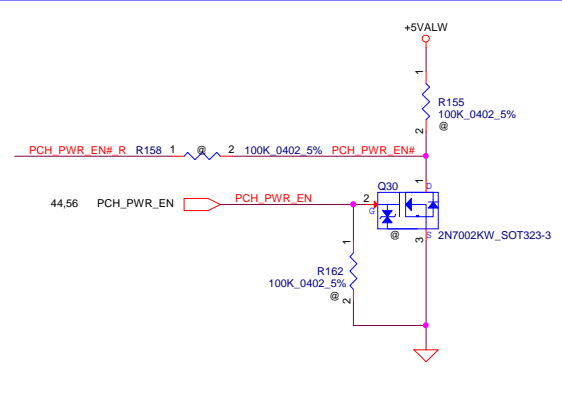
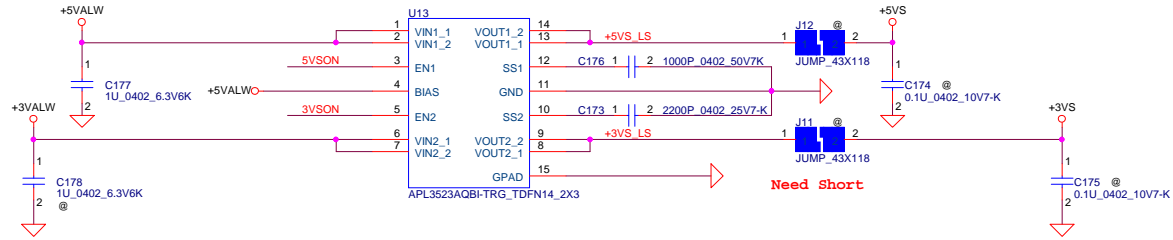
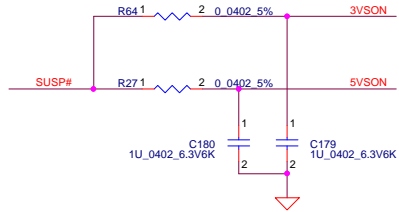
check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14"/15" 02/26

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Site Code	Document Number	Rev	Rev
	EMV01	0.3	0.3
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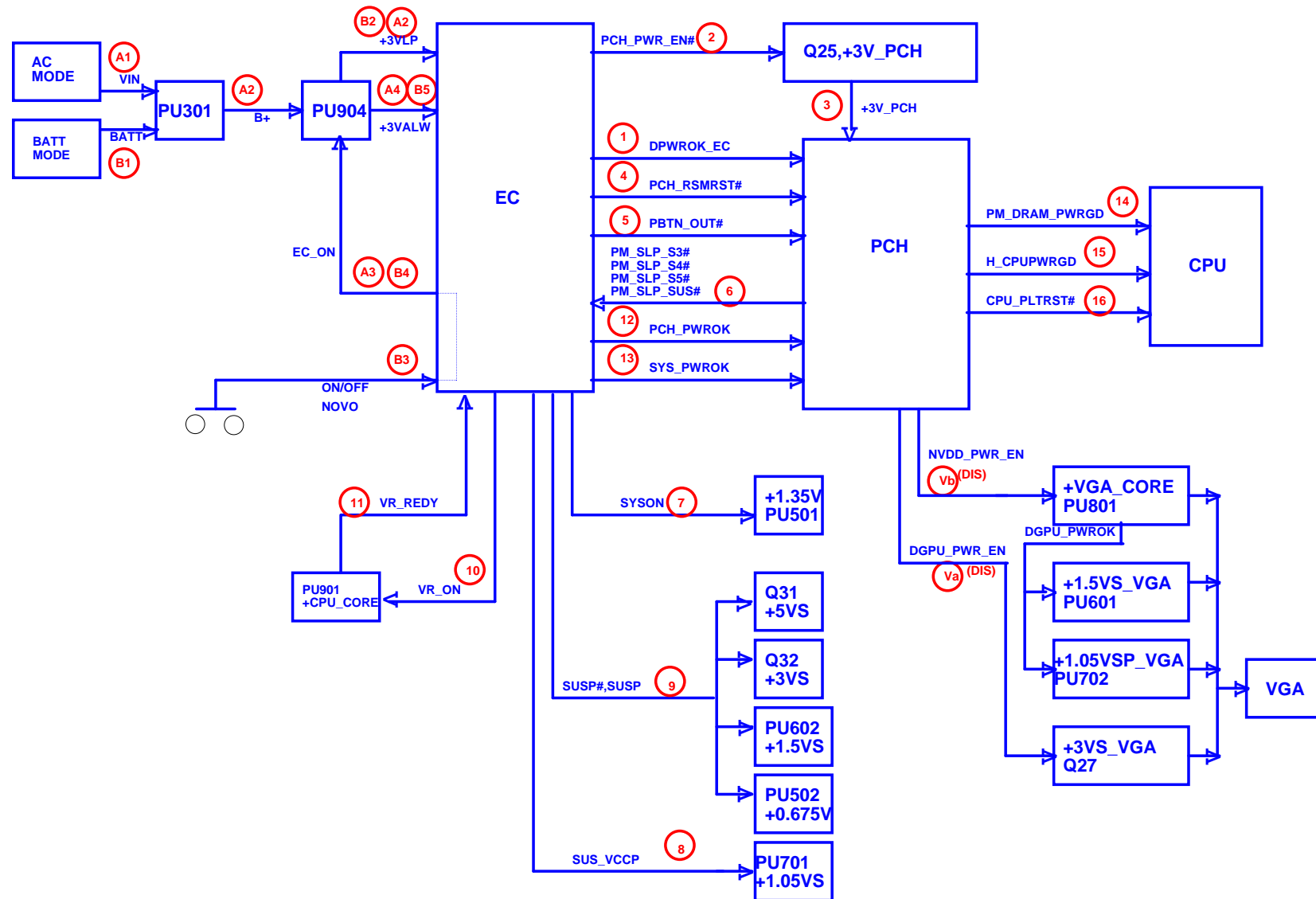
Load Switch
+5VALW To +5VS
+3VALW To +3VS


+3VS, C173 --> 2.74ms
+5VS, C176 --→ 2.03ms

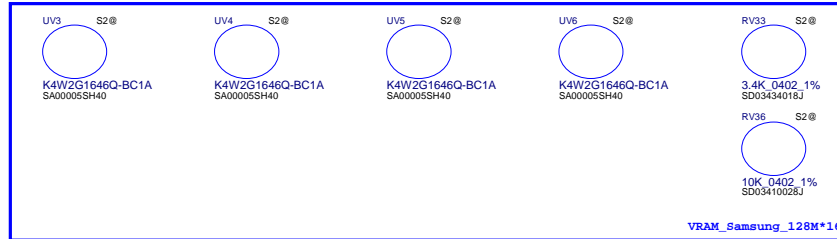
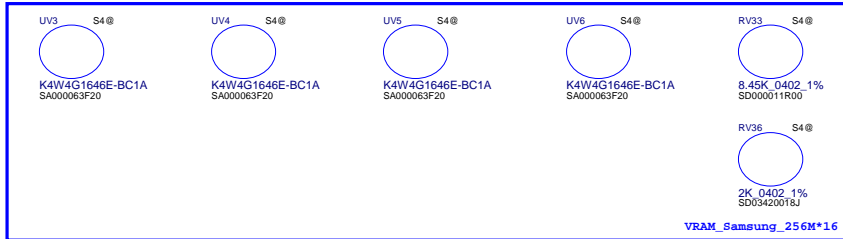
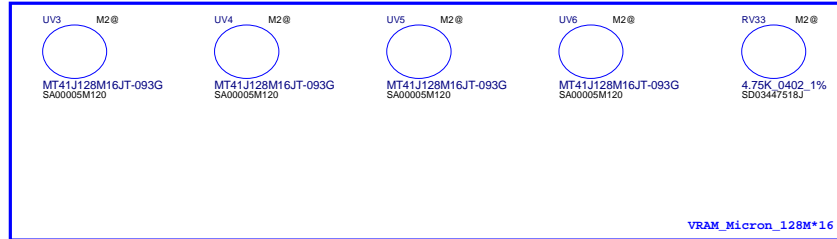
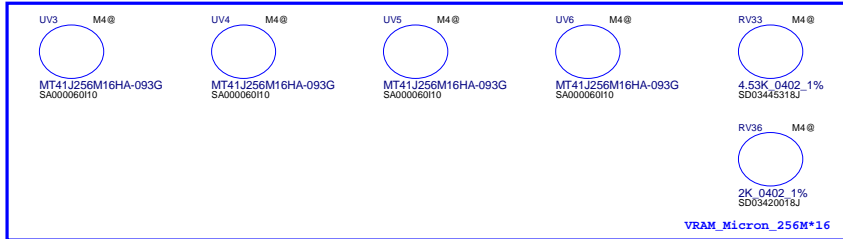
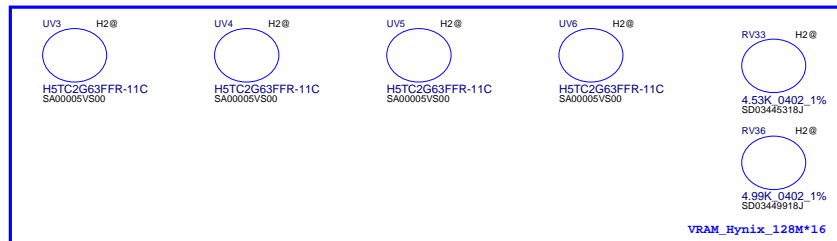
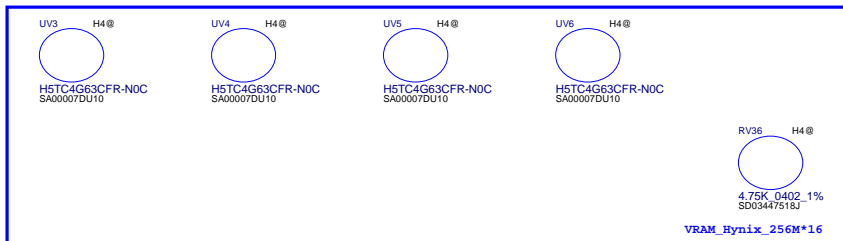
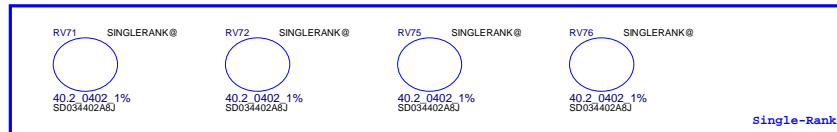
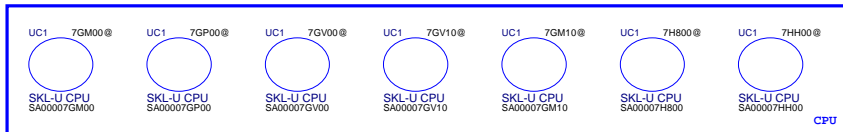
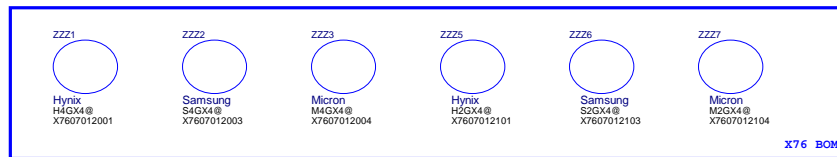
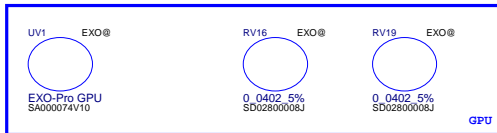
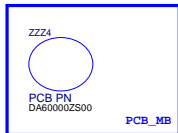
VIN 5V and 3.3V (VBIAS=5V), I_{MAX}(per channel)=6A, R_{ds}=16mohm



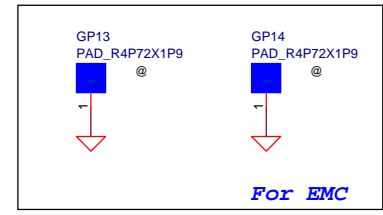
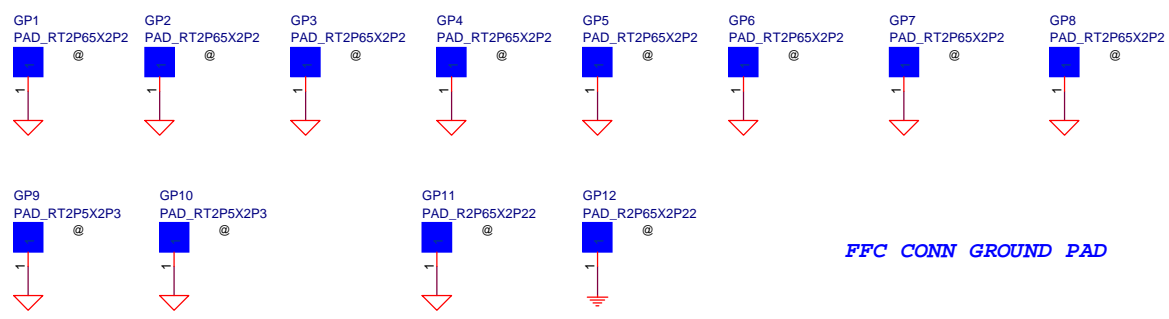
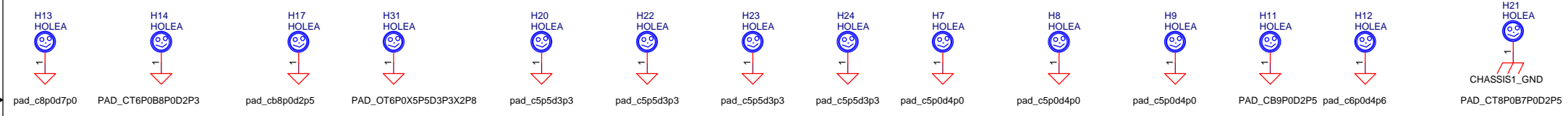
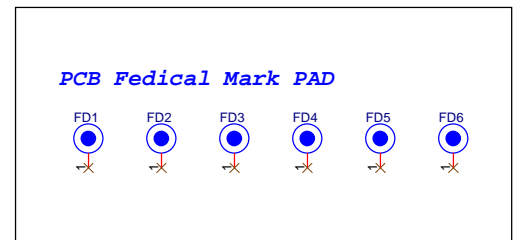
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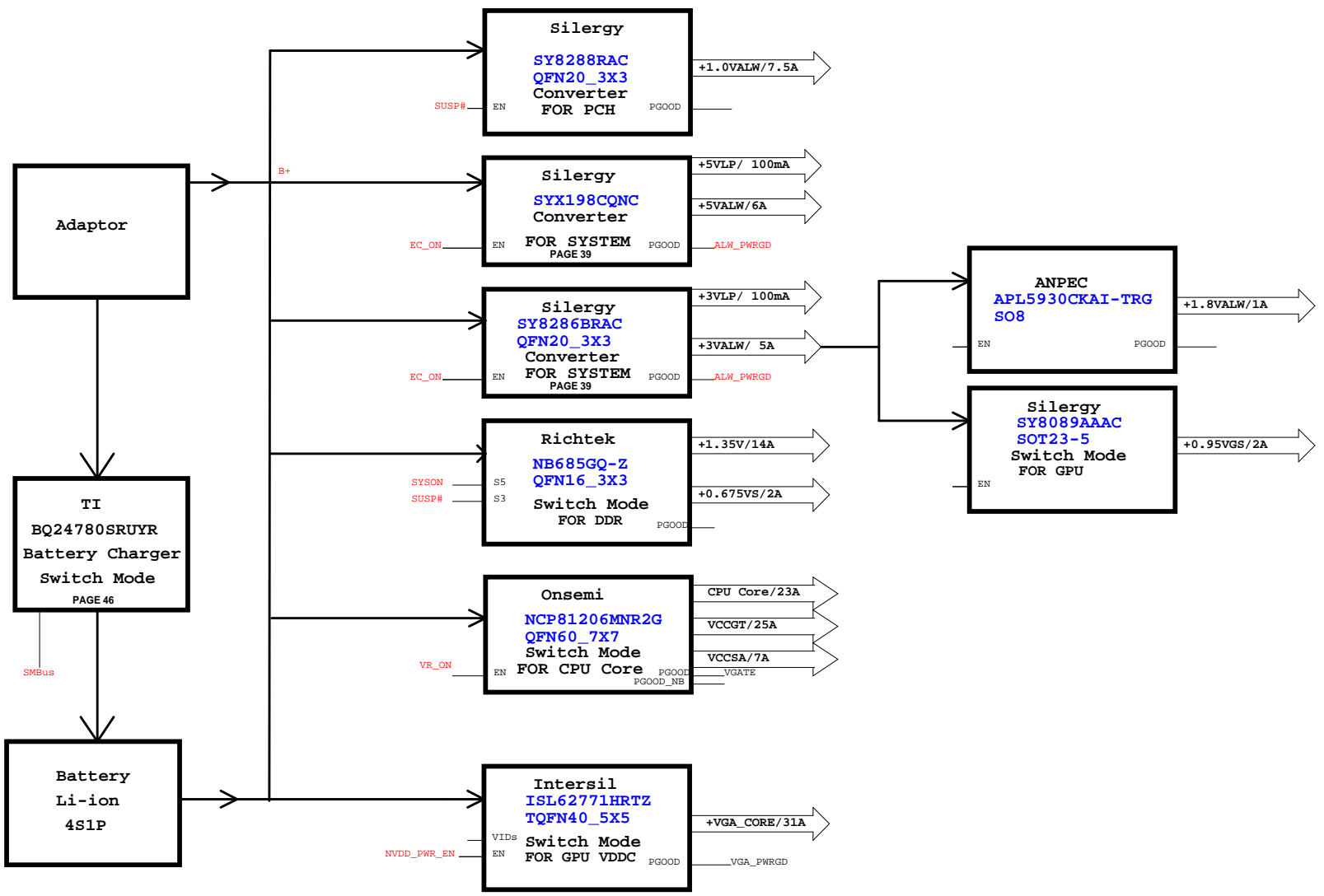



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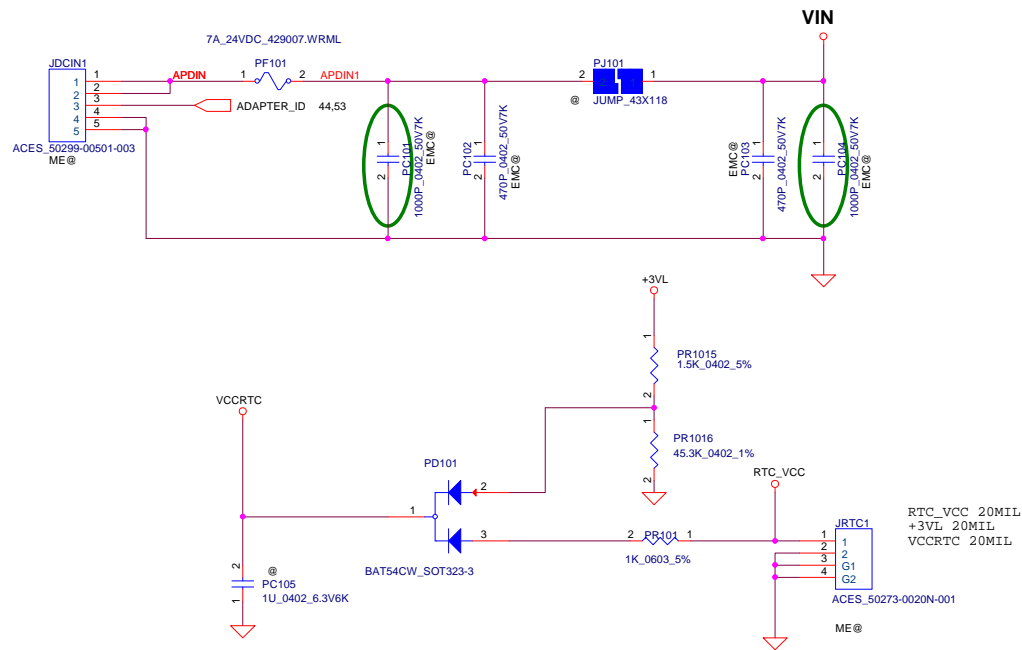


FFC CONN GROUND PAD

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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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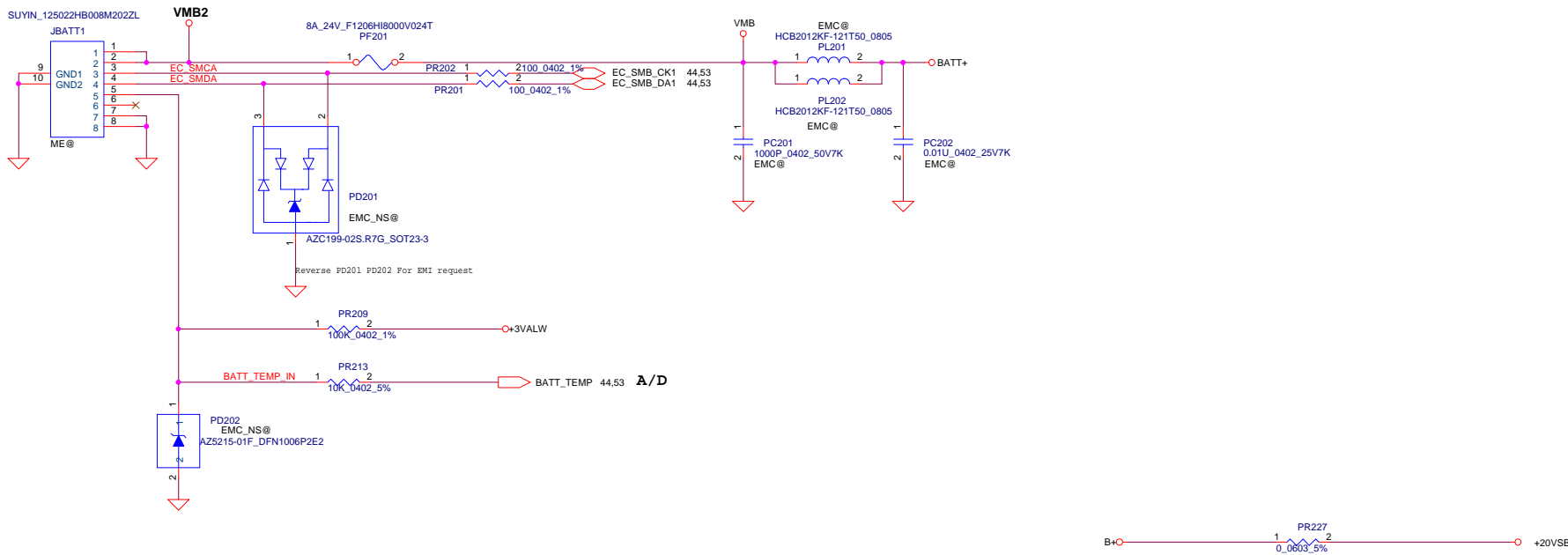
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Issued Date	2013/08/08	Deciphered Date	2013/08/05


Title	DCIN / RTC
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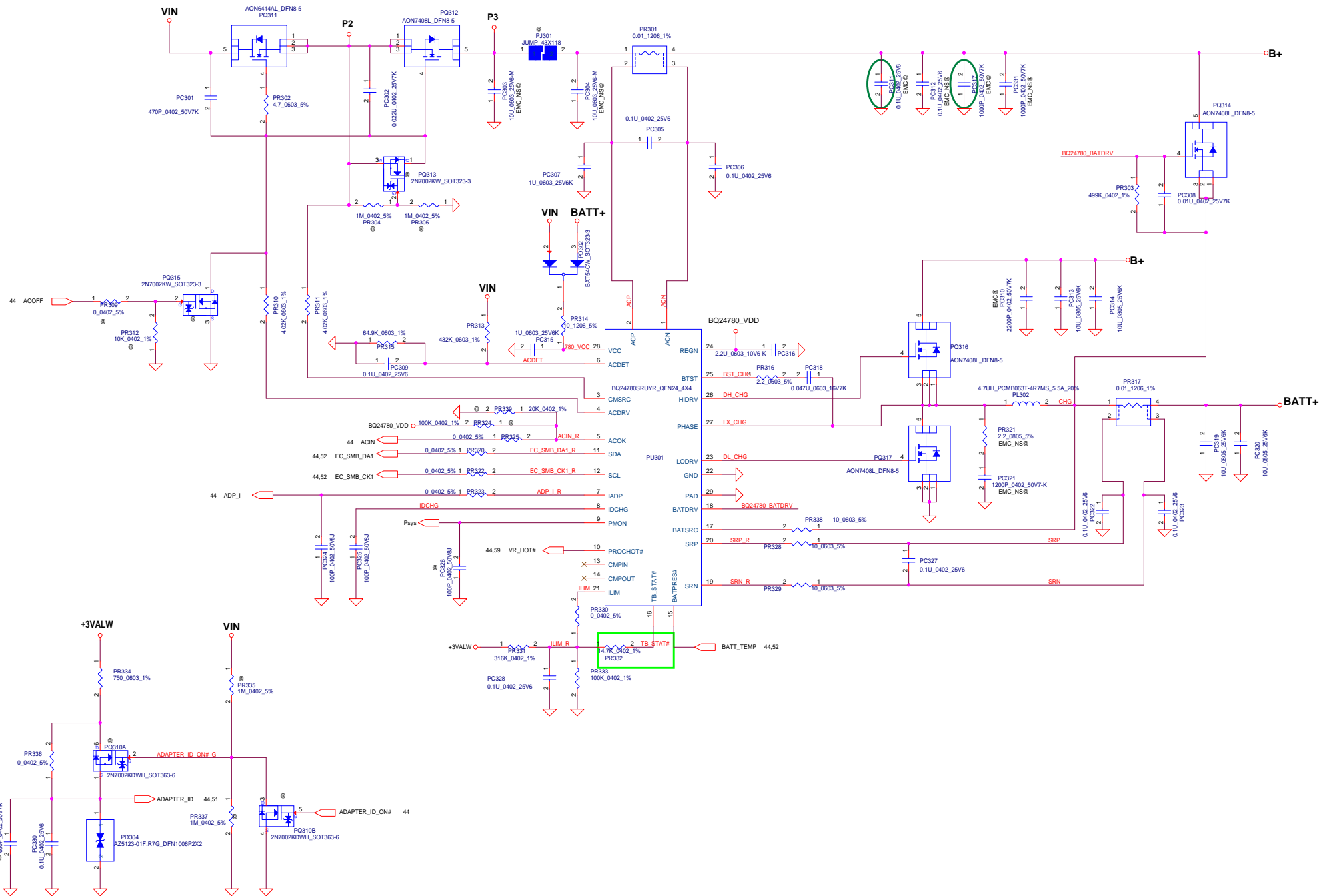



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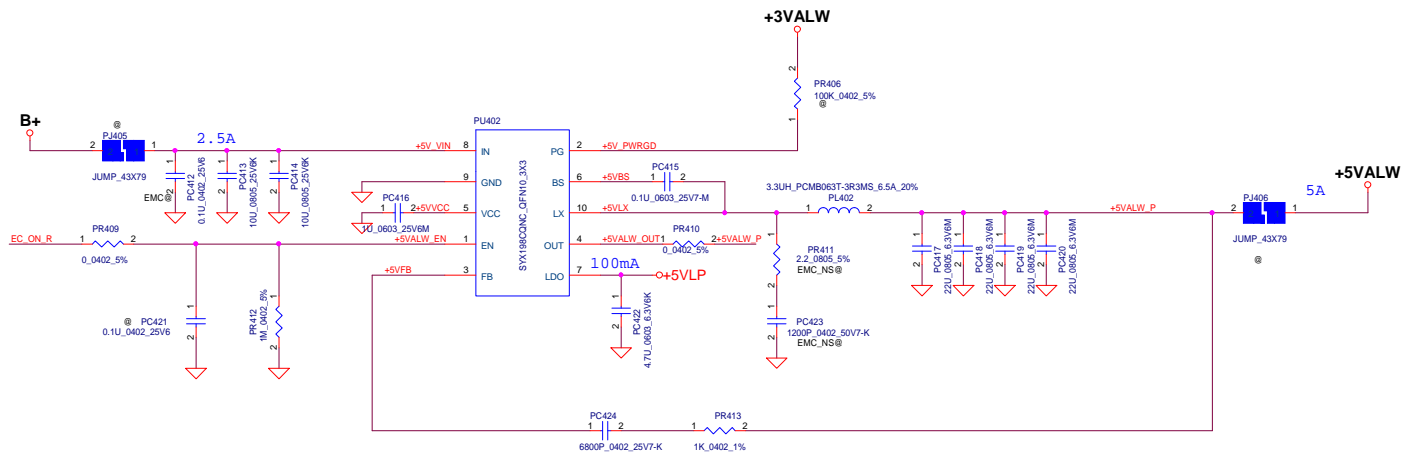
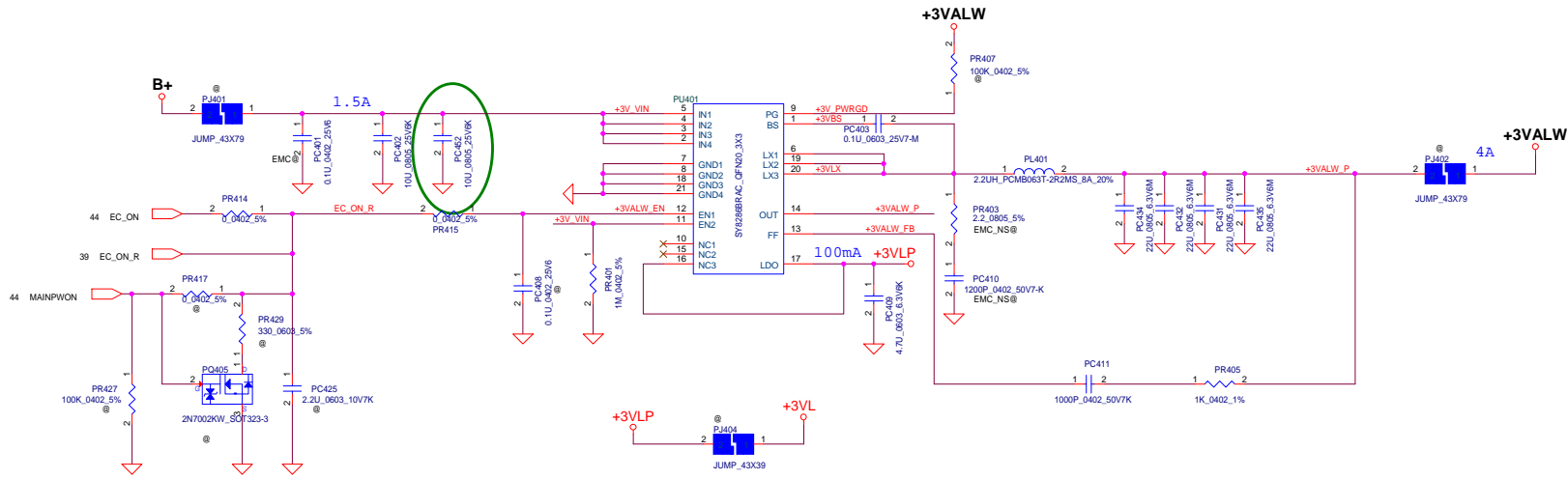
Size	Document Number	Rev
Custom	BMWQ1&Q2	0.3
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	BATTERY CONN/OTP		
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				Custom	BMWQ1&Q2	0.3
				Date:	Thursday, May 28, 2015	Sheet 52 of 60



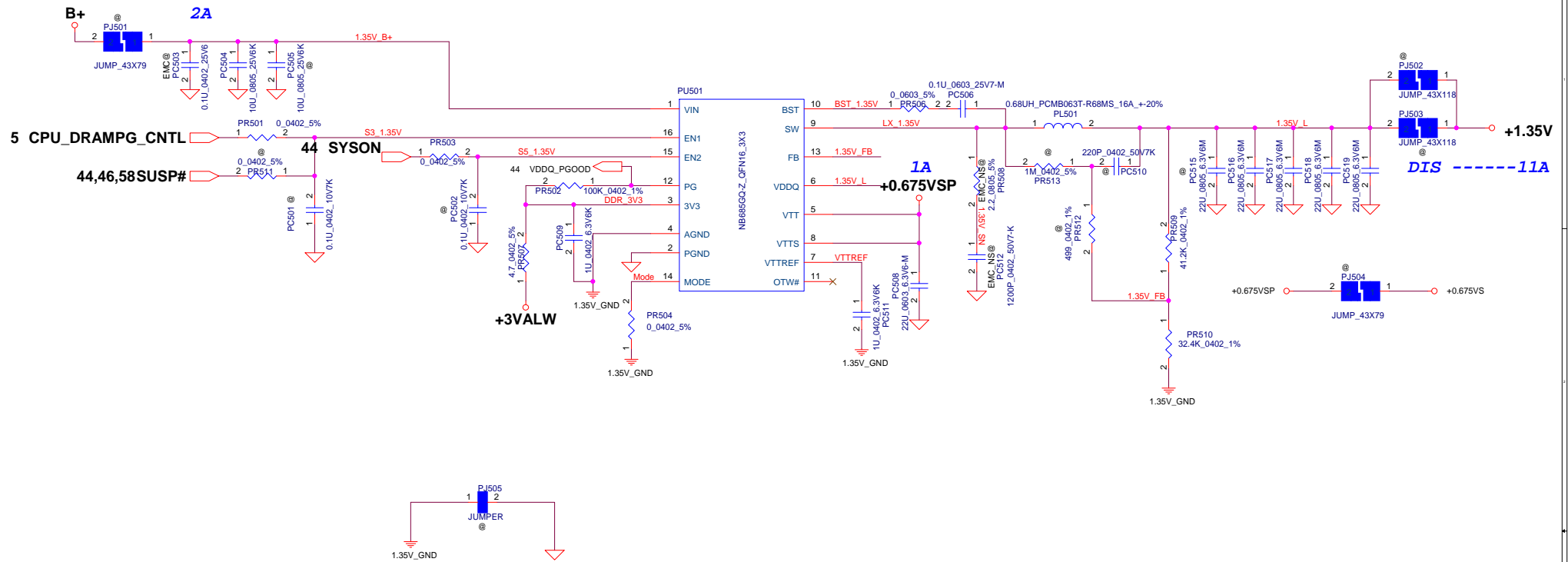
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Size	Document Number	Rev	0.3
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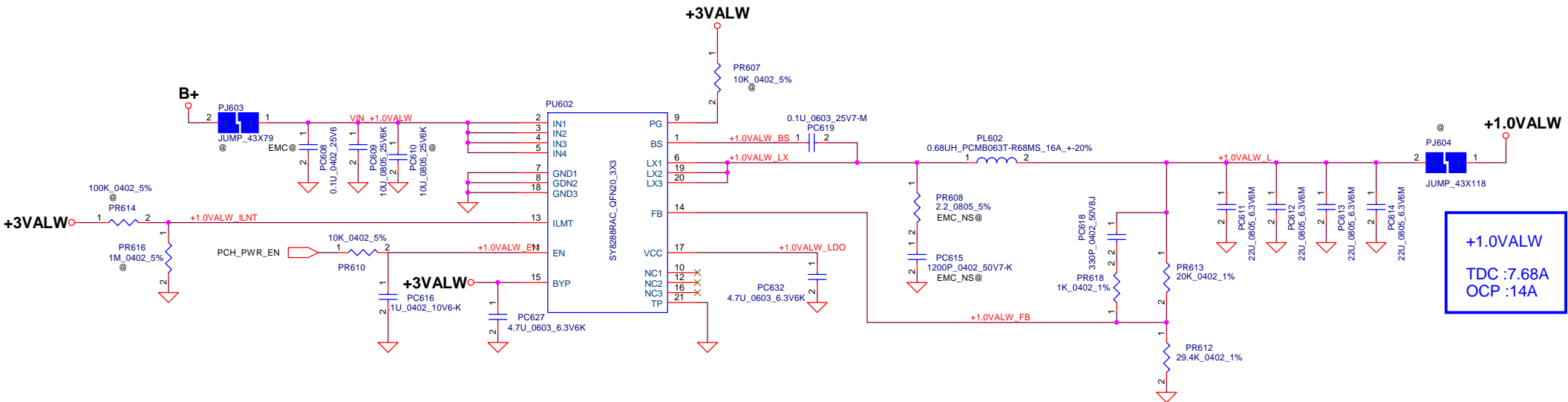
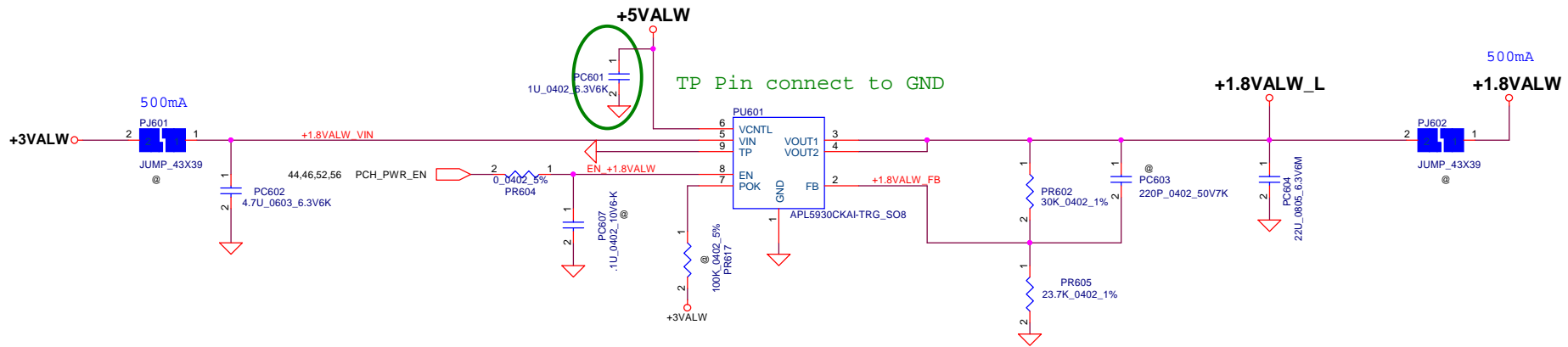
6800pf soft start 2ms
47nf soft start 7ms

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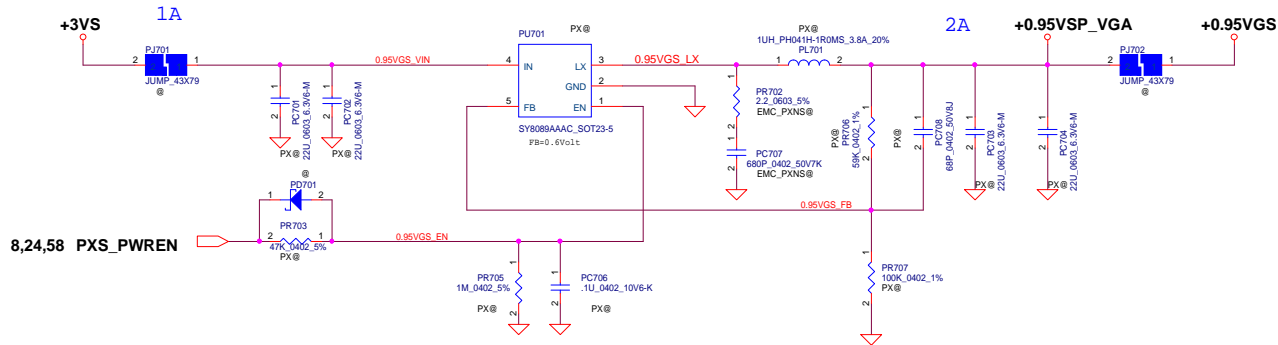


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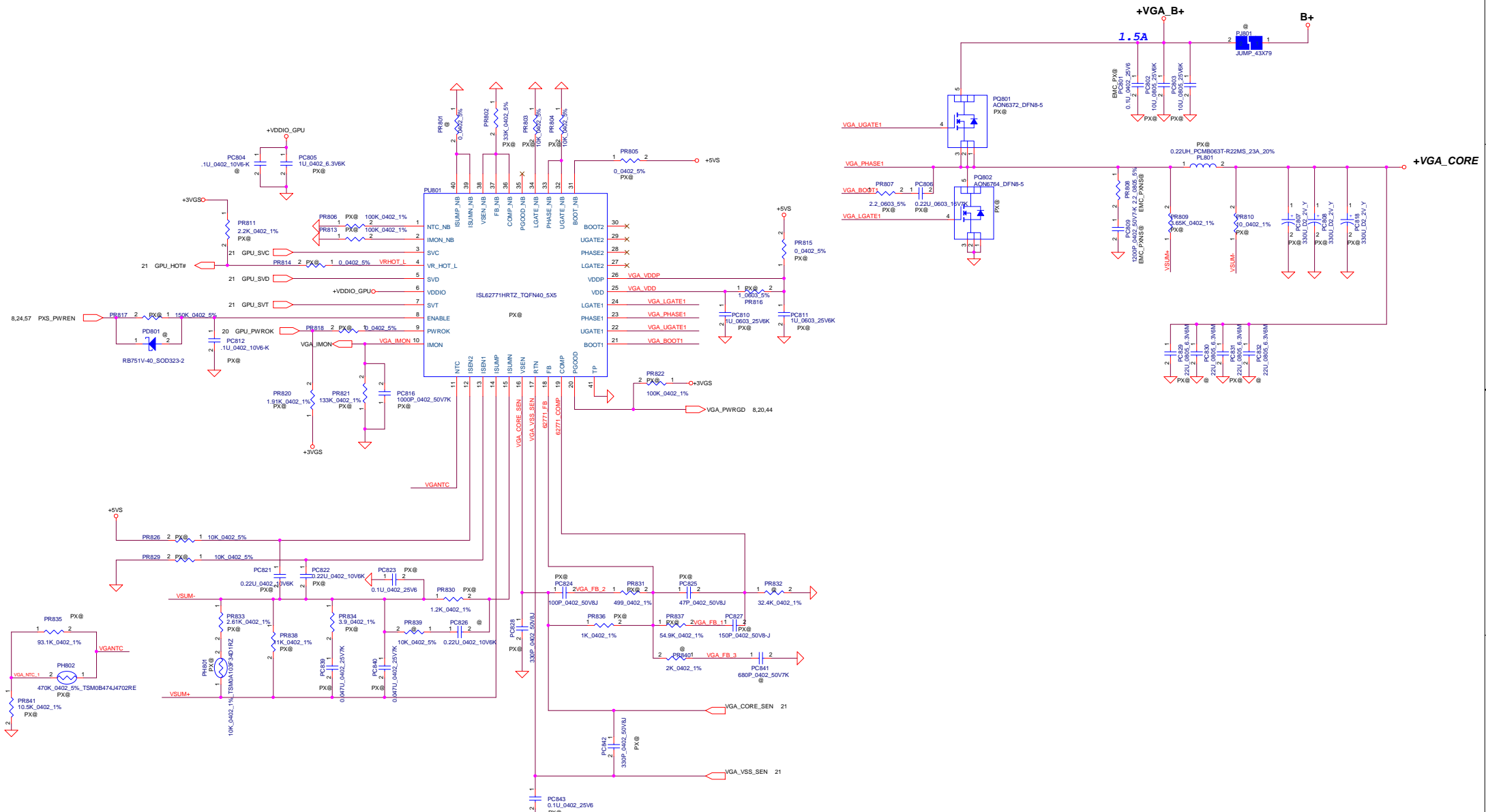
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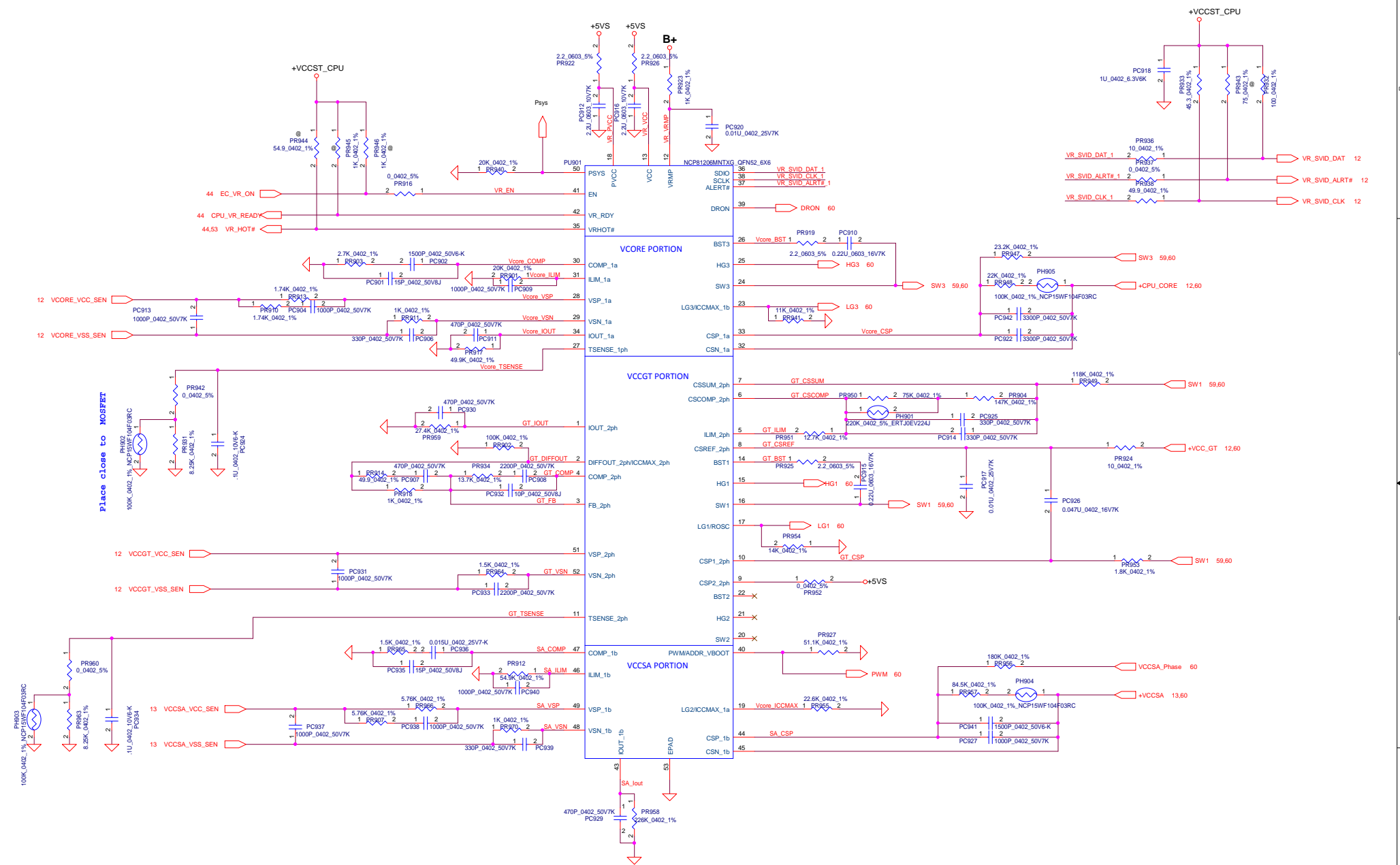


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