

# LCFC Confidential


## G Project M/B Schematics Document

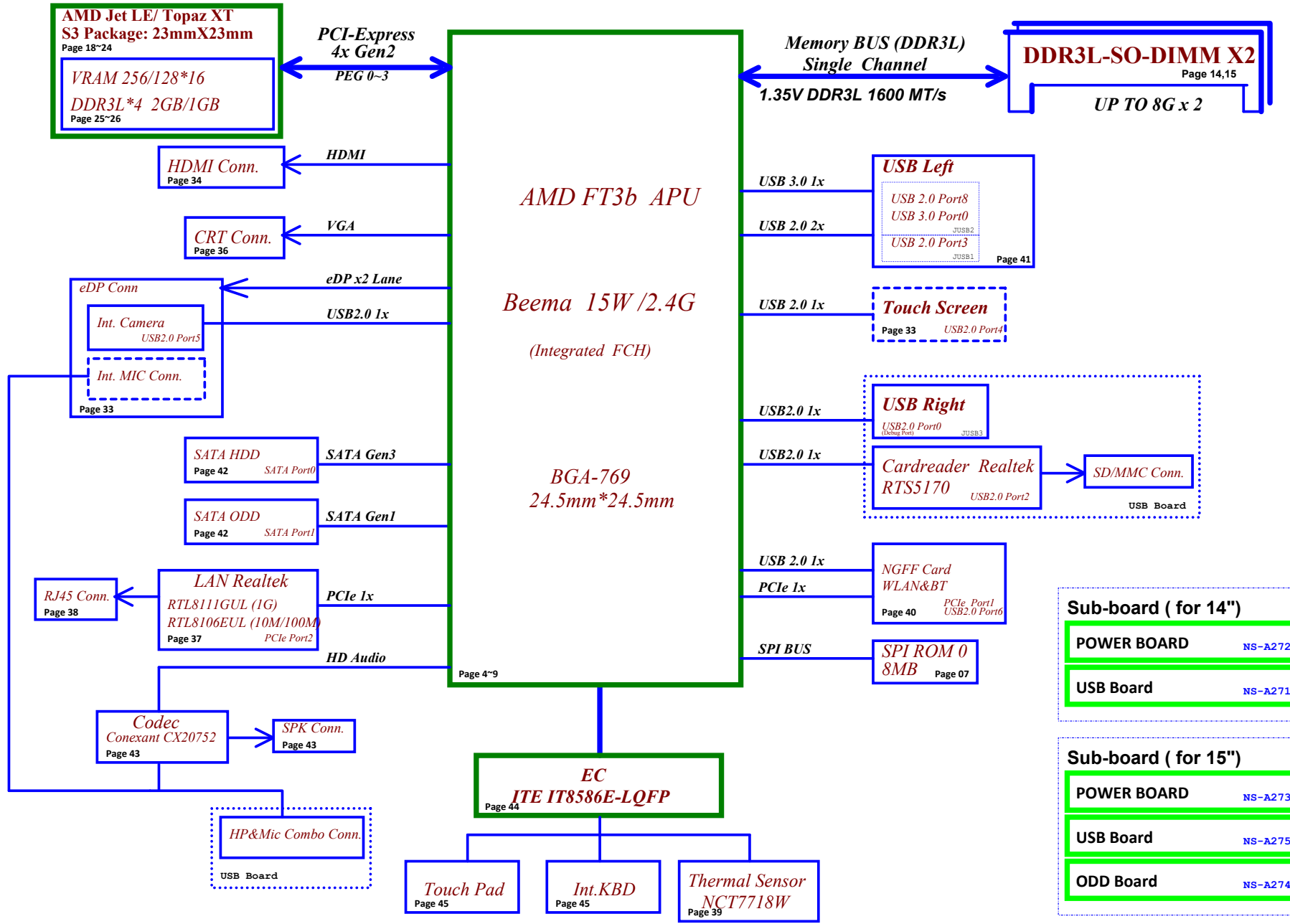
AMD FT3B Beema SOC with DDRIIL

AMD JET-LE

2014-2-12

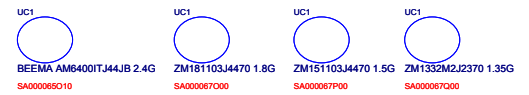
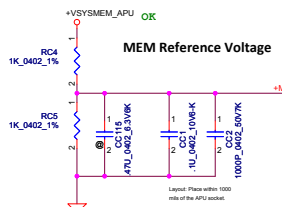
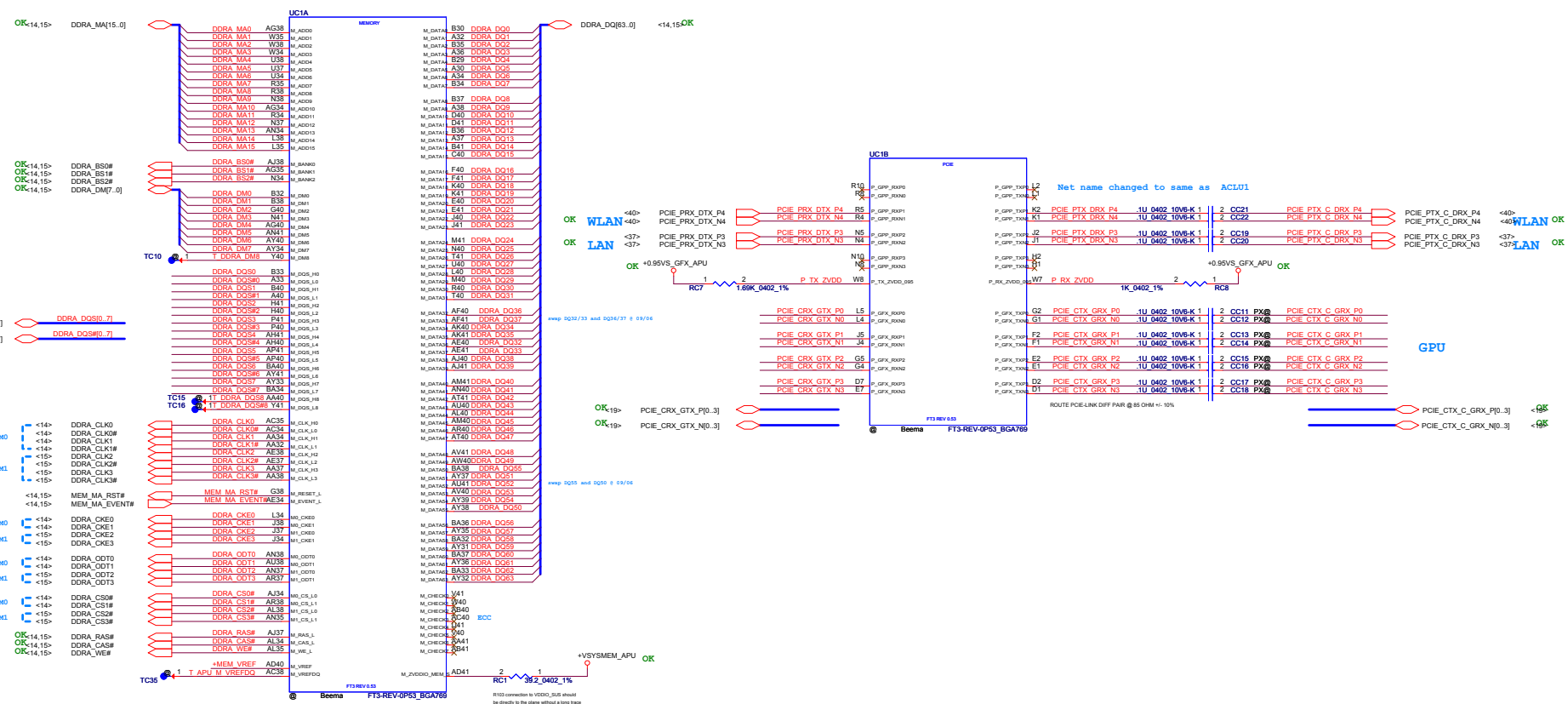
REV: 0.4

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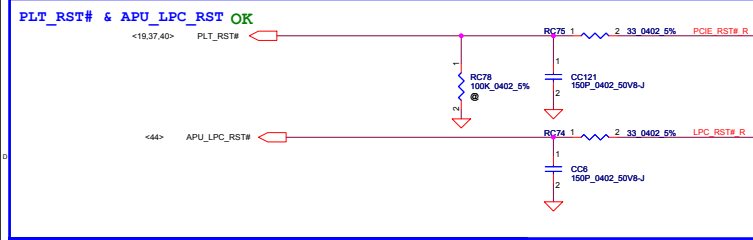
- Sub-board ( for 14" )**
- POWER BOARD** NS-A272
  - USB Board** NS-A271
- Sub-board ( for 15" )**
- POWER BOARD** NS-A273
  - USB Board** NS-A275
  - ODD Board** NS-A274



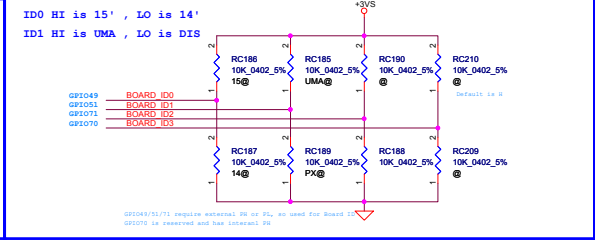


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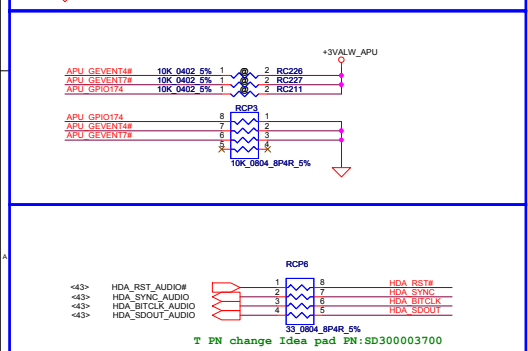
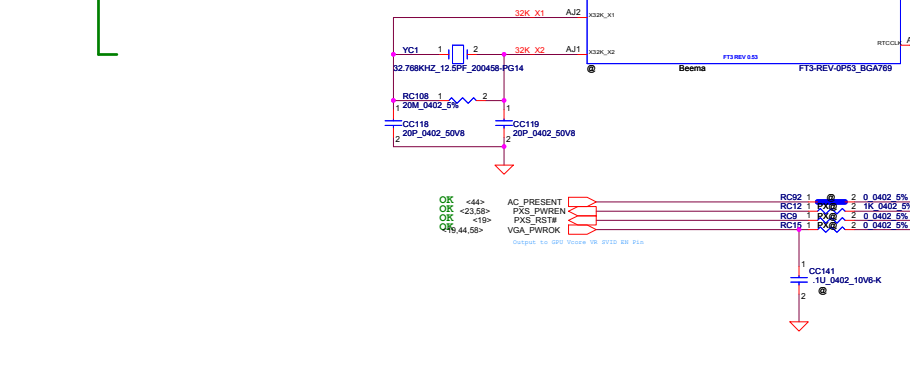
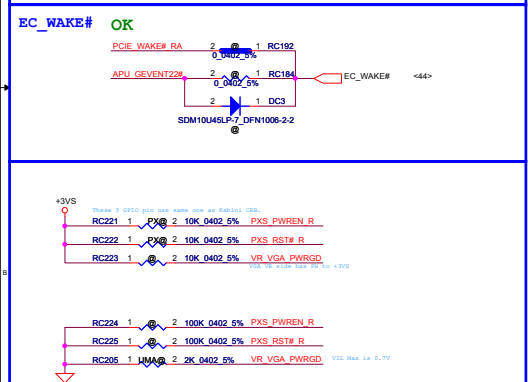
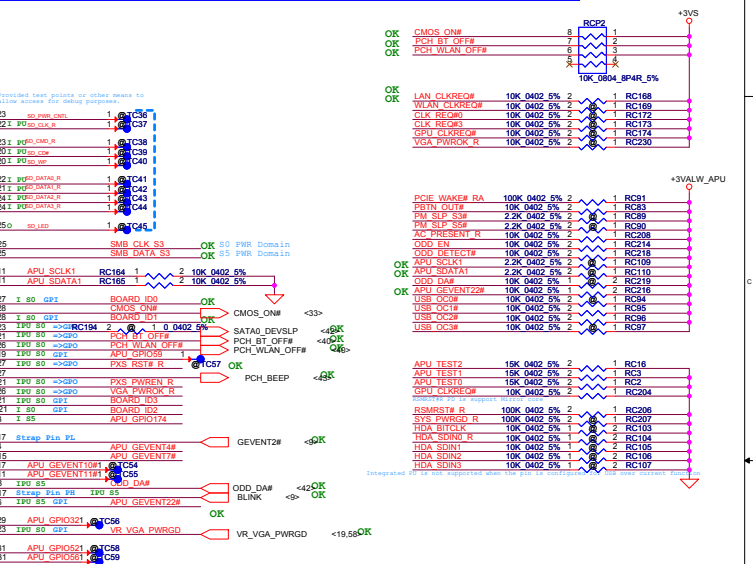
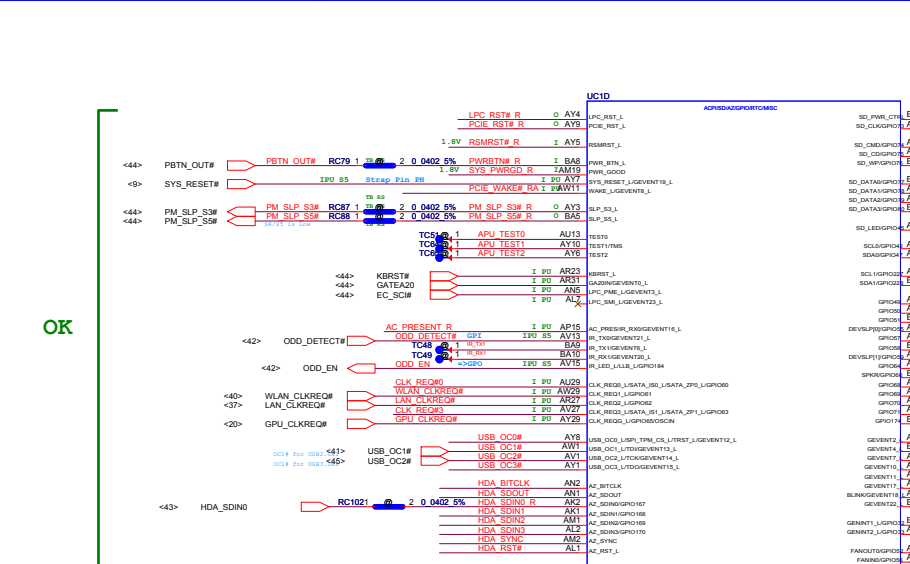
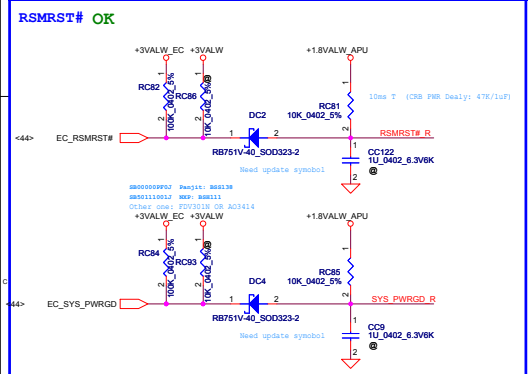
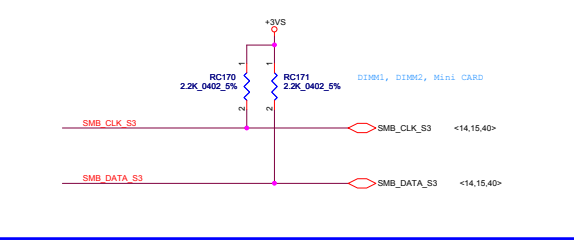




Broad ID OK



SMB\_CLK\_S3 OK

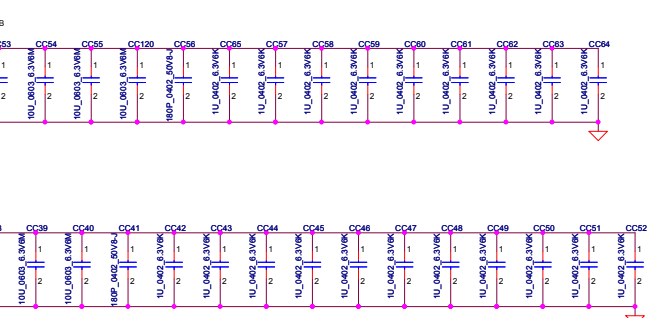
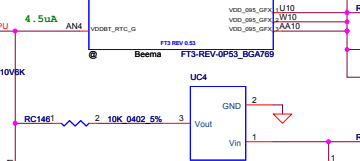
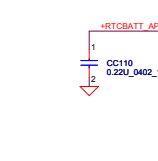
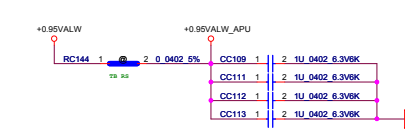
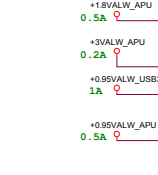
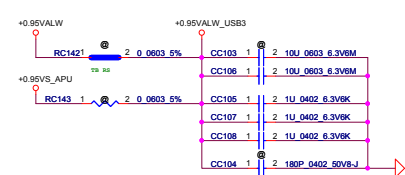
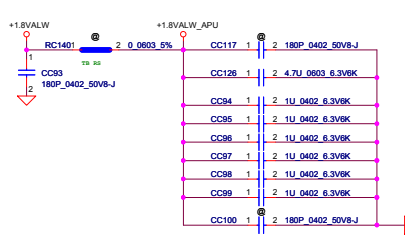
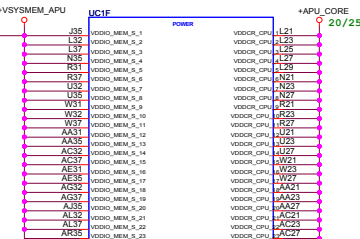
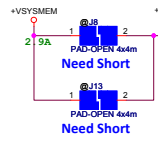
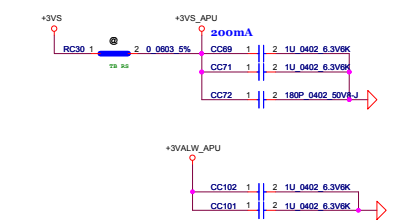


T PN change Idea pad PN:SD300003700

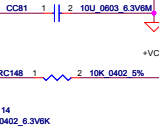
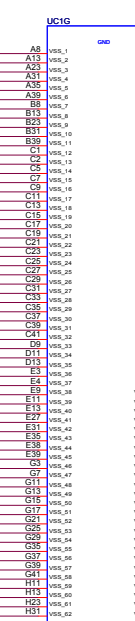
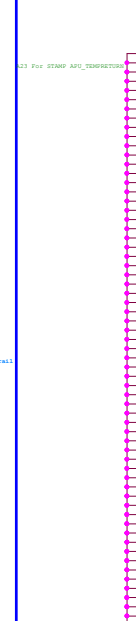
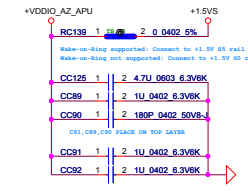
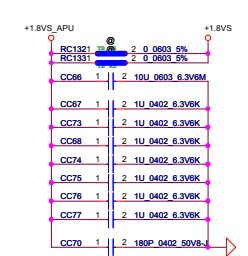




All RLC follow CRB, need double check with DG.

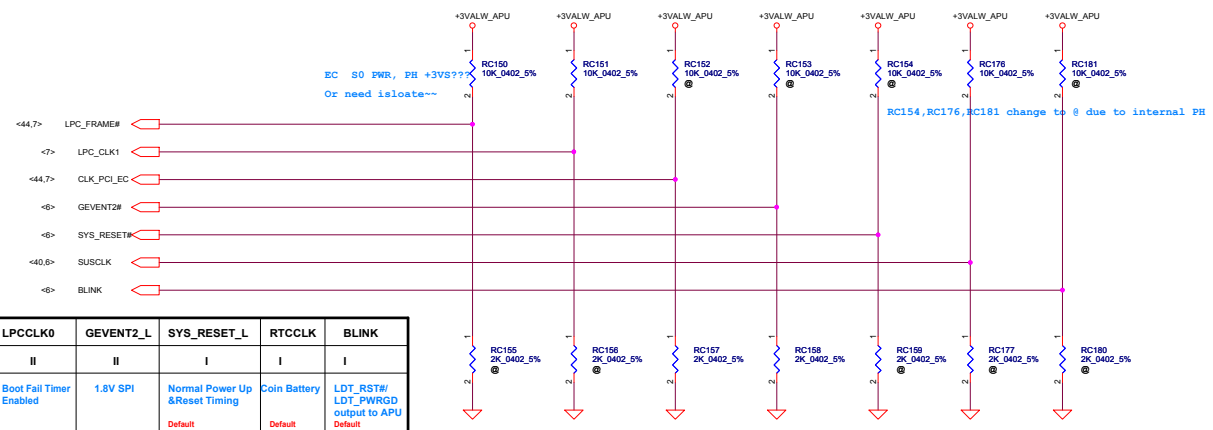


SA000063Q00 BCD: AP2138N-1.5TRG1  
 SA000063Q00 ANPEC: AP1510215AITRG



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**STRAP PINS**

Signal	LFRAME_L	LPCCCLK1	LPCCCLK0	GEVENT2_L	SYS_RESET_L	RTCCLK	BLINK
Type	II	II	II	II	I	I	I
PULL HIGH	SPI ROM <i>Default</i>	Internal CLK Gen <i>Default</i>	Boot Fail Timer Enabled	1.8V SPI	Normal Power Up & Reset Timing <i>Default</i>	Coin Battery <i>Default</i>	LDT_RST#/ LDT_PWRGD output to APU <i>Default</i>
PULL LOW	LPC ROM	External CLK Gen	Boot Fail Timer Disabled <i>Default</i>	3.3V SPI <i>Default</i>	Reserved	Direct DC	Reserved

Type I straps become valid immediately after capture with the rising edge of RSMRST\_L.  
 Type II straps become valid after PWR\_GOOD is asserted  
 All Strap pins must be configured with either external pull-up or pull-down resistors.

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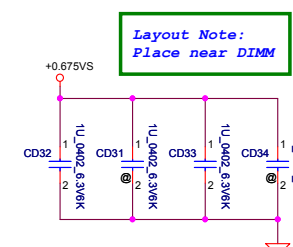
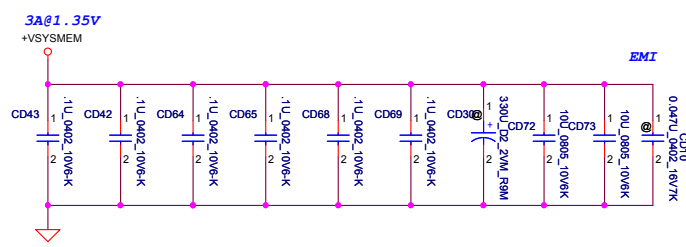
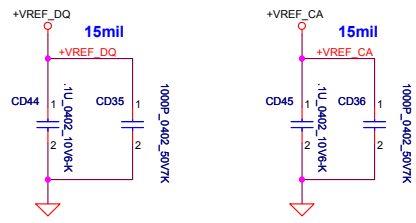
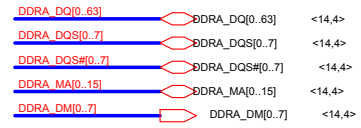
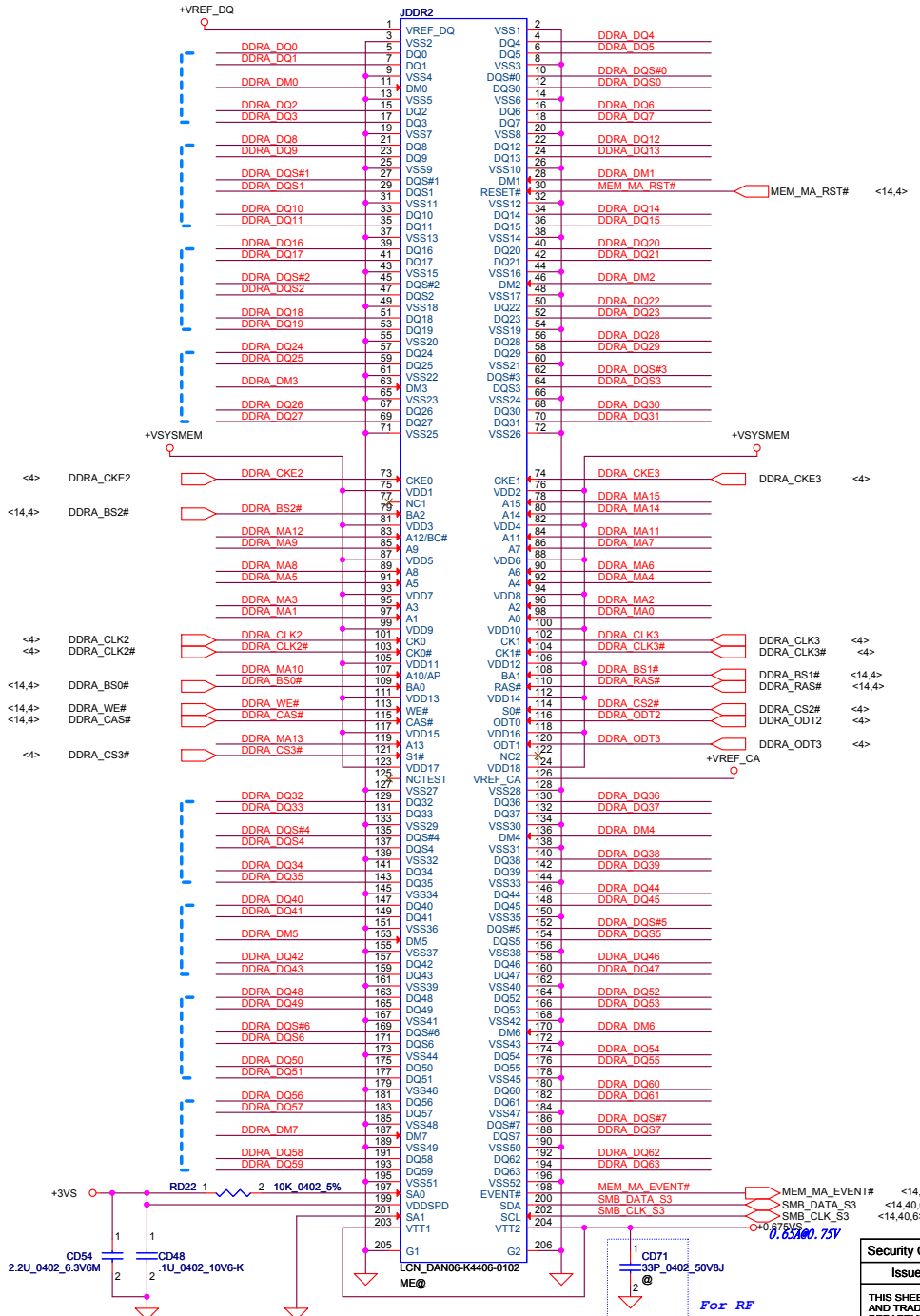
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# DDR3 SO-DIMM B




**Layout Note:**  
Place near DIMM


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## VGA Note list need to be update!

### Power-Up/Down Sequence

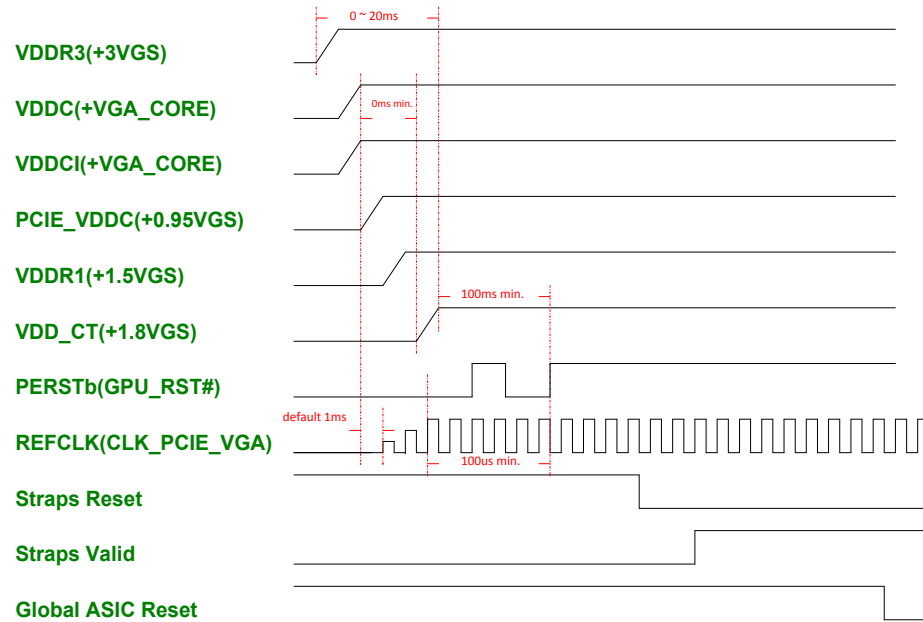
"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.

The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.

VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).

For power down, reversing the ramp-up sequence is recommended.

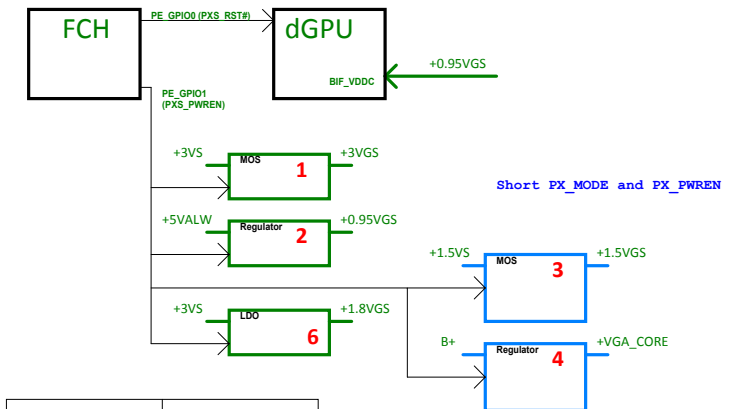


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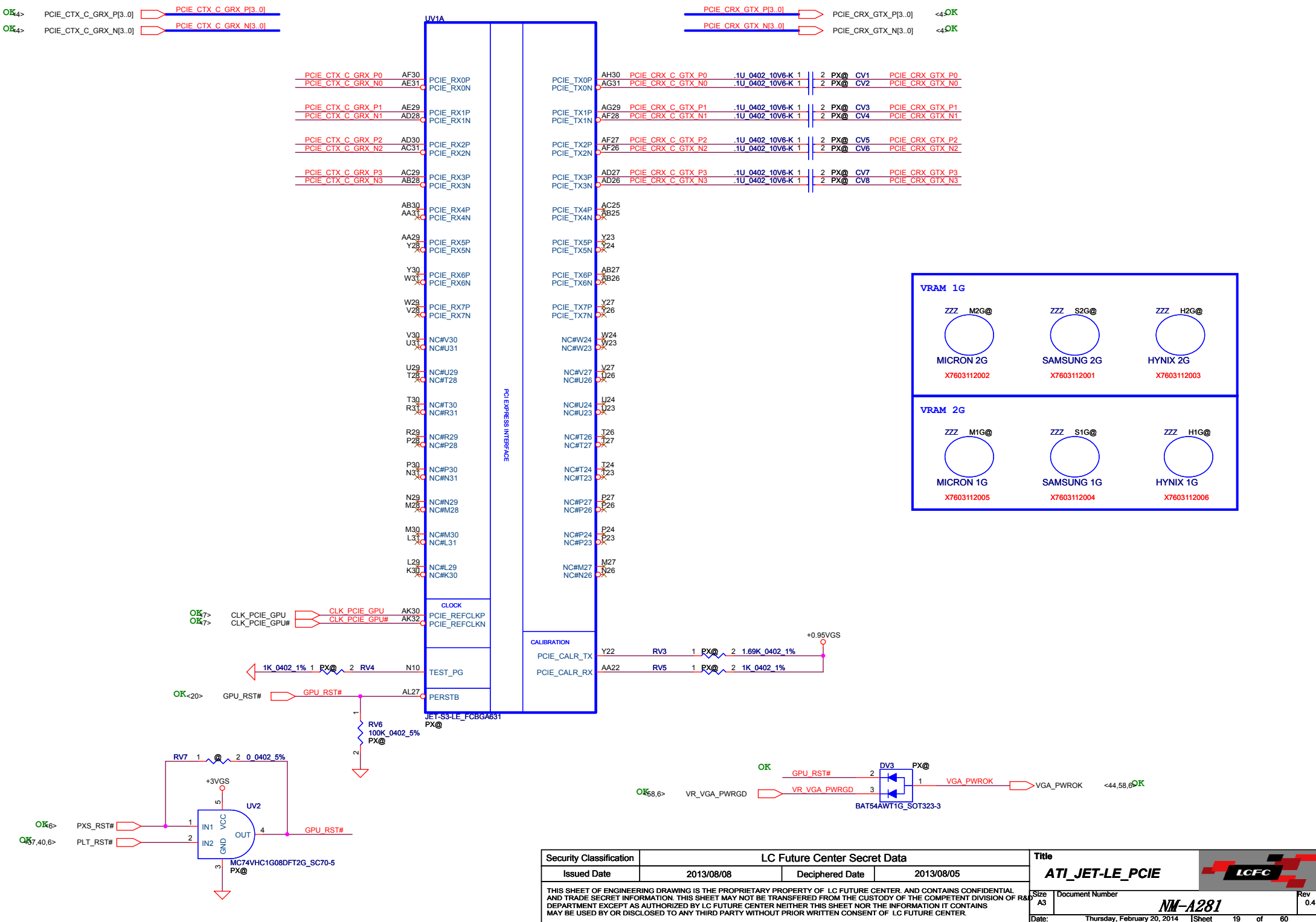
PE\_GPIO0 : Low -> Reset dGPU ; High -> Normal operation  
 PE\_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

dGPU Power Pins	Voltage	Max current
VDD_CT, DP_VDDR, SPLL_PVDD, MPLL_PVDD, PCIE_PVDD, TSVDD, VDDR4, AVDD, VDD1DI	1.8V	1243mA
DP_VDDC, SPLL_VDDC, PCIE_VDDC, BIF_VDDC	0.95V	4560mA
VDDR3	3.3V	25mA
VDDR1	1.5V	1.5A
VDDC	0.8~1.125V	TBD
VDDCI	0.8~1.1V	8.8A

## PX5.5

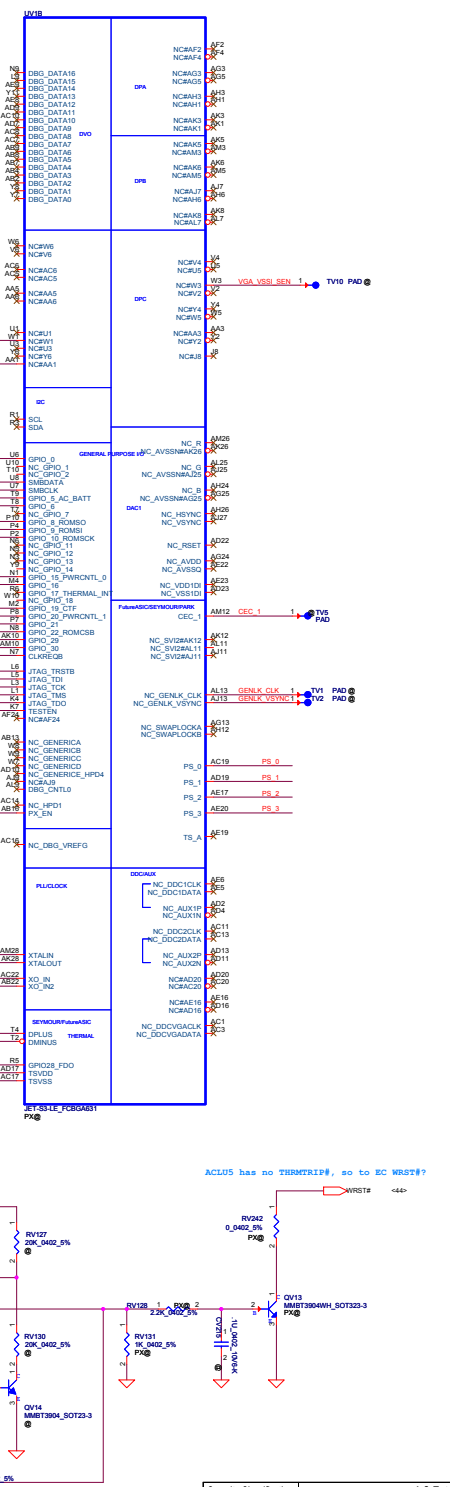
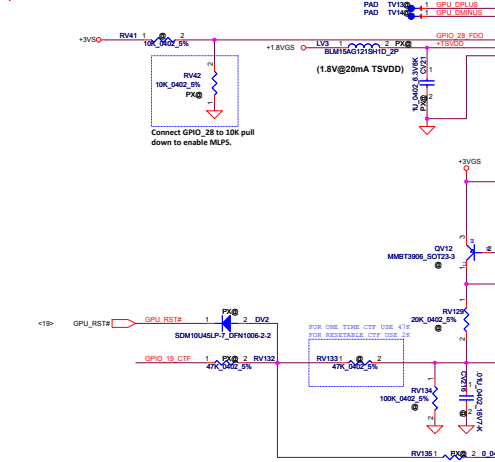
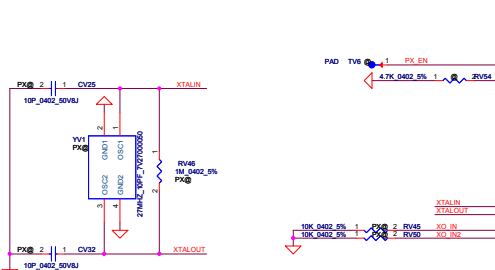
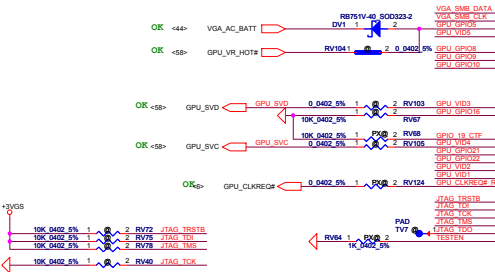
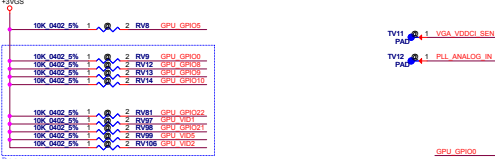
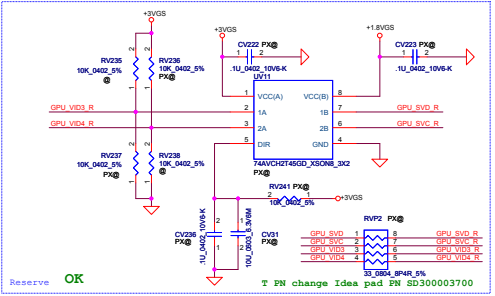


Name	Pin Assignment
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192



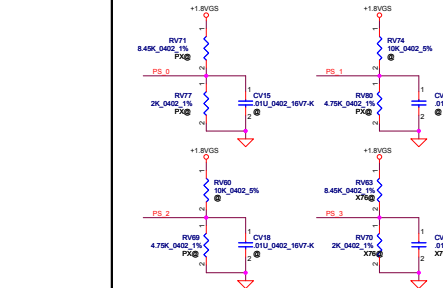
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**CONFIGURATION STRAPS**  
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET

MIPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_0[2]	ROM_CONFIG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0	100 = 256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[6]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	X
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported 0 = PCIe GEN3 is not supported	0 = Not support
PS_1[2]	STRAP_BIF_CLK_PM_LEN	0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CPD_DRV_LUL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[10]	STRAP_TX_DEEMPH_LEN	0 = Tx deemphases disabled 1 = Tx deemphases enabled	X
PS_2[1]	N/A	Reserved.	N/A
PS_2[2]	N/A	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	1 = Disable the external BIOS ROM device. 0 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capability enabled 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[6]	N/A	Reserved	N/A
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap options such as for memory ID	X
PS_3[2]	BOARD_CONFIG[1]	10 = Hynix IG 11 = Micron IG 12 = Samsung IG	
PS_3[3]	BOARD_CONFIG[2]	Determines the maximum number of digital display audio endpoints that will be presented for the OS and user. (Combine with PS_0[6])	11 = No usable endpoints. 10 = One usable endpoint. 01 = Two usable endpoints. 00 = Three usable endpoints. 01 = Four usable endpoints. 00 = Five usable endpoints. 00 = Six usable endpoints. 00 = All endpoints are usable.
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]		X
PS_3[5]	AUD_PORT_CONN_PINSTRAP[0]		X

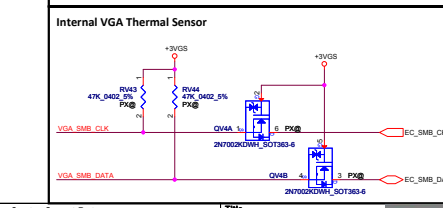
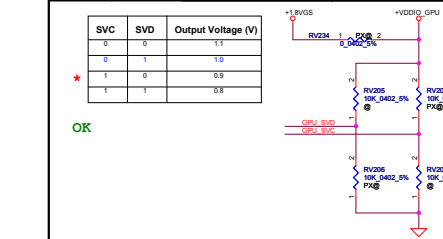


MIPS	Bit				BOM			
	5	4	3	2	1	R_pu (Ω)	R_pd (Ω)	C (nF)
PS_0 [5:1]	1	1	0	0	1	RV71=8.45k	RV72=2k	CV15=NC
PS_1 [5:1]	1	1	0	0	0	RV73=4.75k	RV74=4.75k	CV16=NC
PS_2 [5:1]	1	1	0	0	0	RV60=NC	RV69=4.75k	CV17=NC
PS_3 [5:1]	1	1	X	X	X	RV60=X76	RV69=X76	CV18=X76

Capacitor Value (nF)	Bits [5:4]			
	5	4	3	2
680	00	00	3240	5620
82	01	01	3400	10000
10	10	10	4750	NC
NC	11	11	NC	111

Note: 0402 1% resistors are required



No GPIO Reserve for NV GPU

UV1F

NC\_VARY\_BL  
NC\_DIGON

AB11  
AB12

NC\_UPHYAB\_TMDPA\_TX0N  
NC\_UPHYAB\_TMDPA\_TX0P  
NC\_UPHYAB\_TMDPA\_TX1N  
NC\_UPHYAB\_TMDPA\_TX1P

AL15  
AK14  
AH16  
AJ15

NC\_UPHYAB\_TMDPA\_TX2N  
NC\_UPHYAB\_TMDPA\_TX2P  
NC\_UPHYAB\_TMDPA\_TX3N  
NC\_UPHYAB\_TMDPA\_TX3P

AL17  
AK16  
AH18  
AJ17

NC\_TXOUT\_L3P  
NC\_TXOUT\_L3N

AL19  
AK18

TMDP

NC\_UPHYAB\_TMDPB\_TX0N  
NC\_UPHYAB\_TMDPB\_TX0P  
NC\_UPHYAB\_TMDPB\_TX1N  
NC\_UPHYAB\_TMDPB\_TX1P

AH20  
AJ19  
AL21  
AK20


NC\_UPHYAB\_TMDPB\_TX2N  
NC\_UPHYAB\_TMDPB\_TX2P  
NC\_UPHYAB\_TMDPB\_TX3N  
NC\_UPHYAB\_TMDPB\_TX3P

AH22  
AJ21  
AL23  
AK22

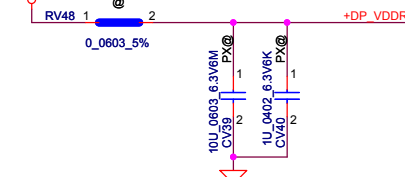
NC\_TXOUT\_U3P  
NC\_TXOUT\_U3N

AK24  
AJ23

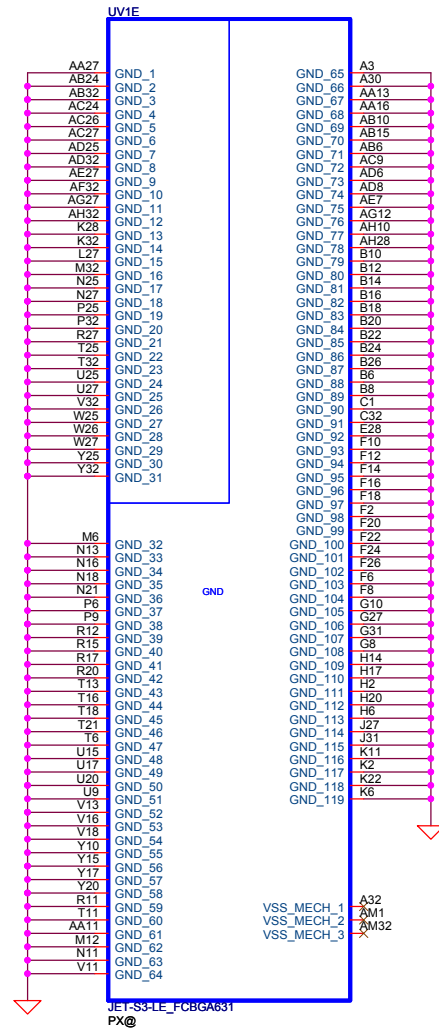
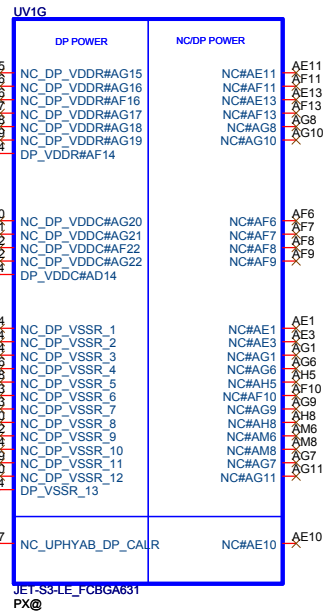
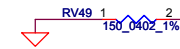
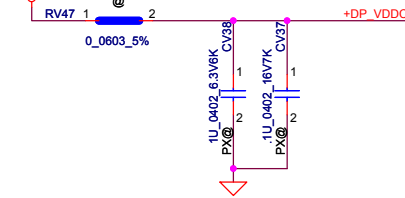
JET-S3-LE\_FCBGA831  
PX@

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				Date:	Thursday, February 20, 2014	Sheet 21 of 60

+1.8VGS @ (1.8V@425mA DP\_VDDR)

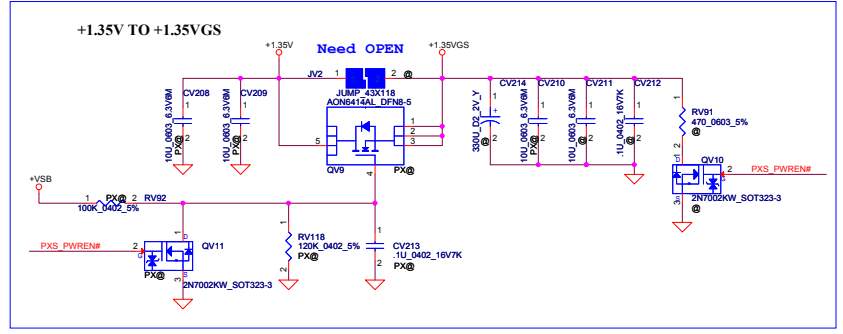
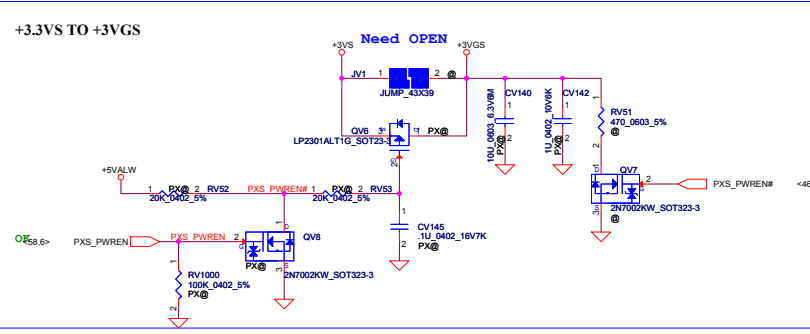
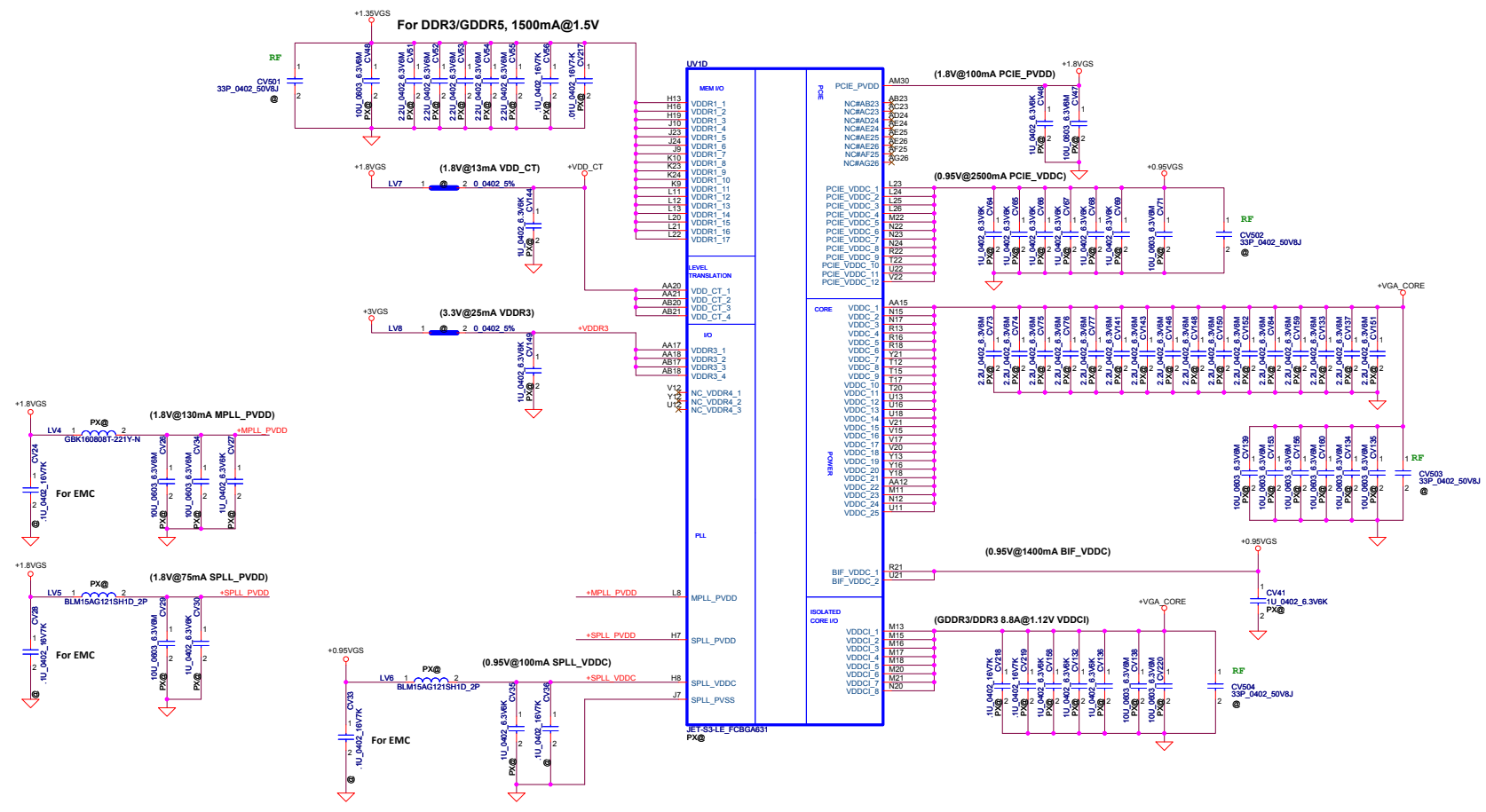


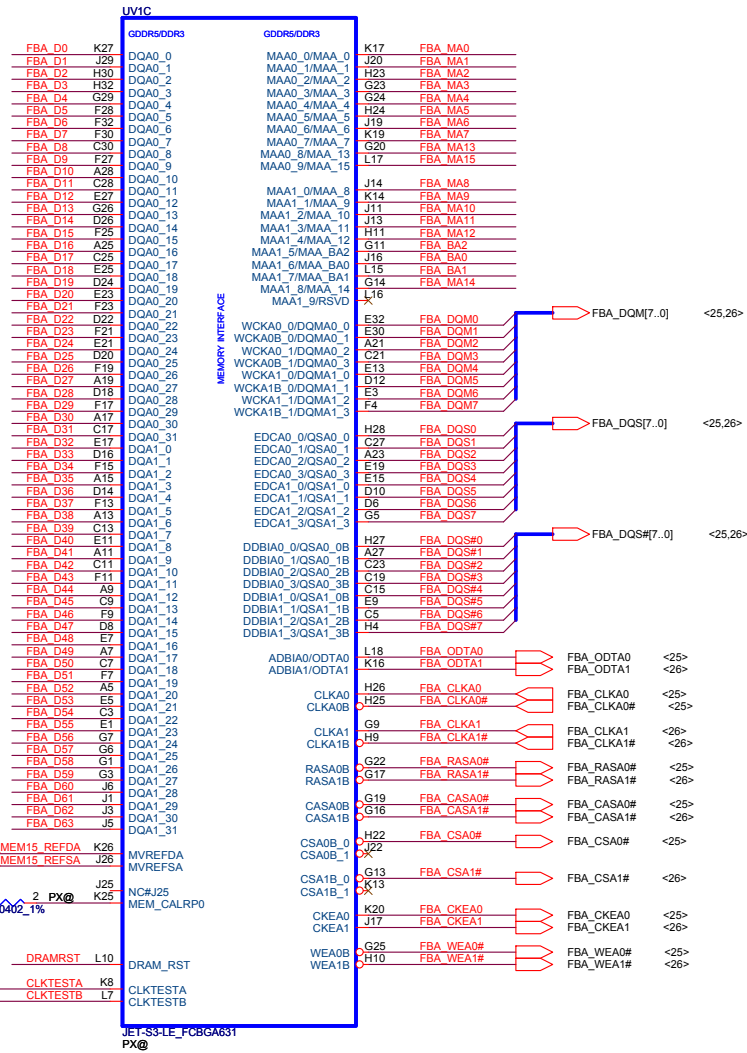
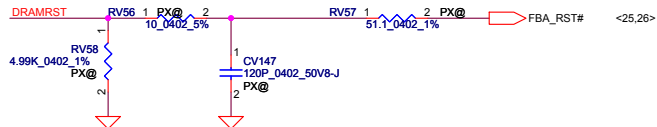
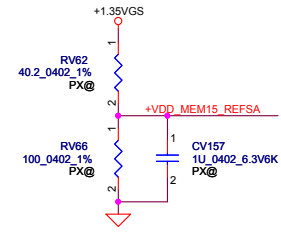
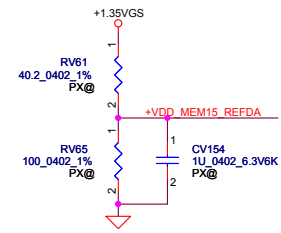
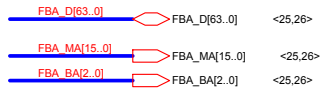
+0.95VGS @ (0.95V@560mA DP\_VDDC)



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Title		
ATI_JET-LE_DP Power		
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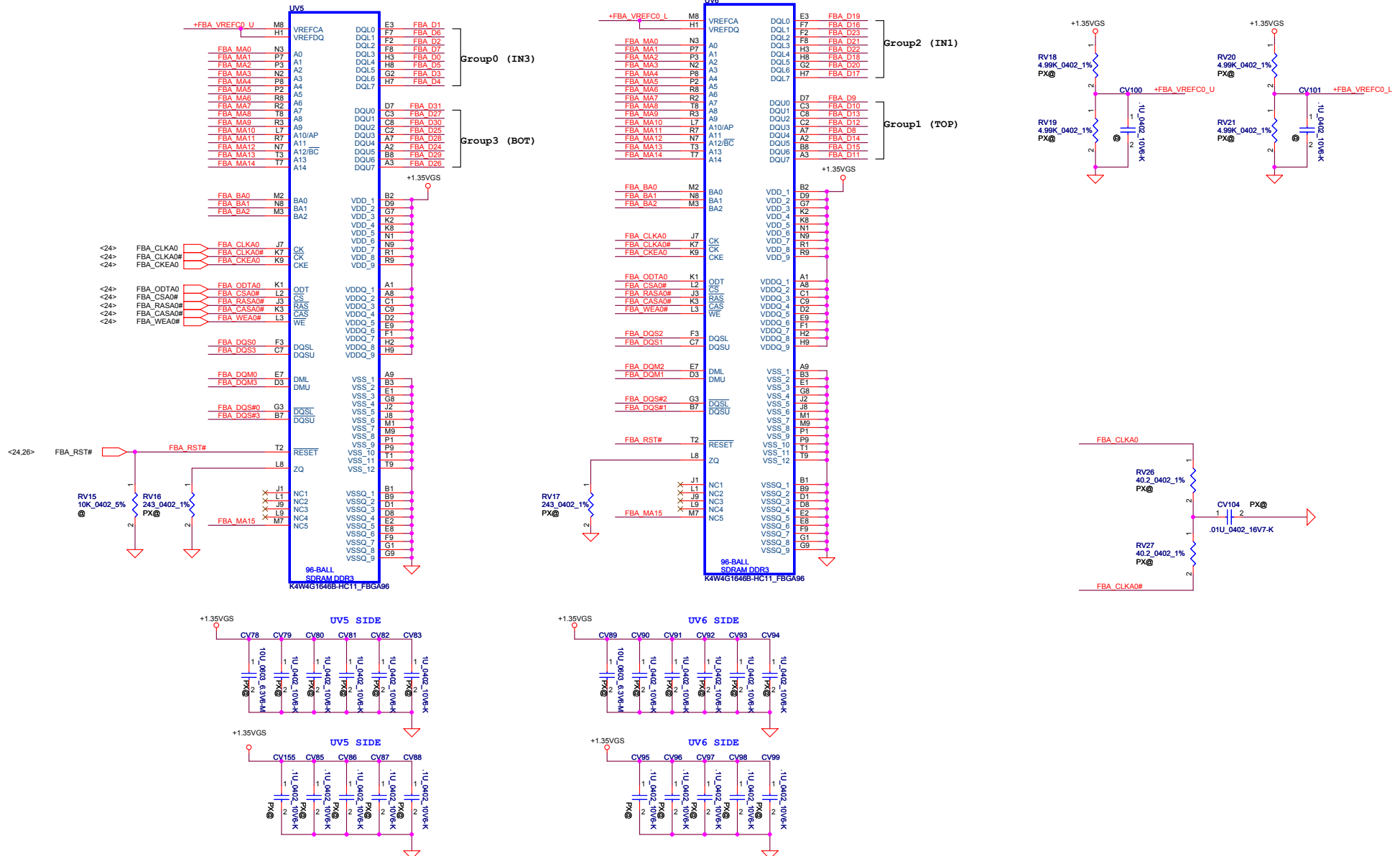
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ATI_JET-LE_MEM IF		
Size	Document Number	Rev
Custom	NM-A281	0.4
Date:	Thursday, February 20, 2014	Sheet 24 of 60



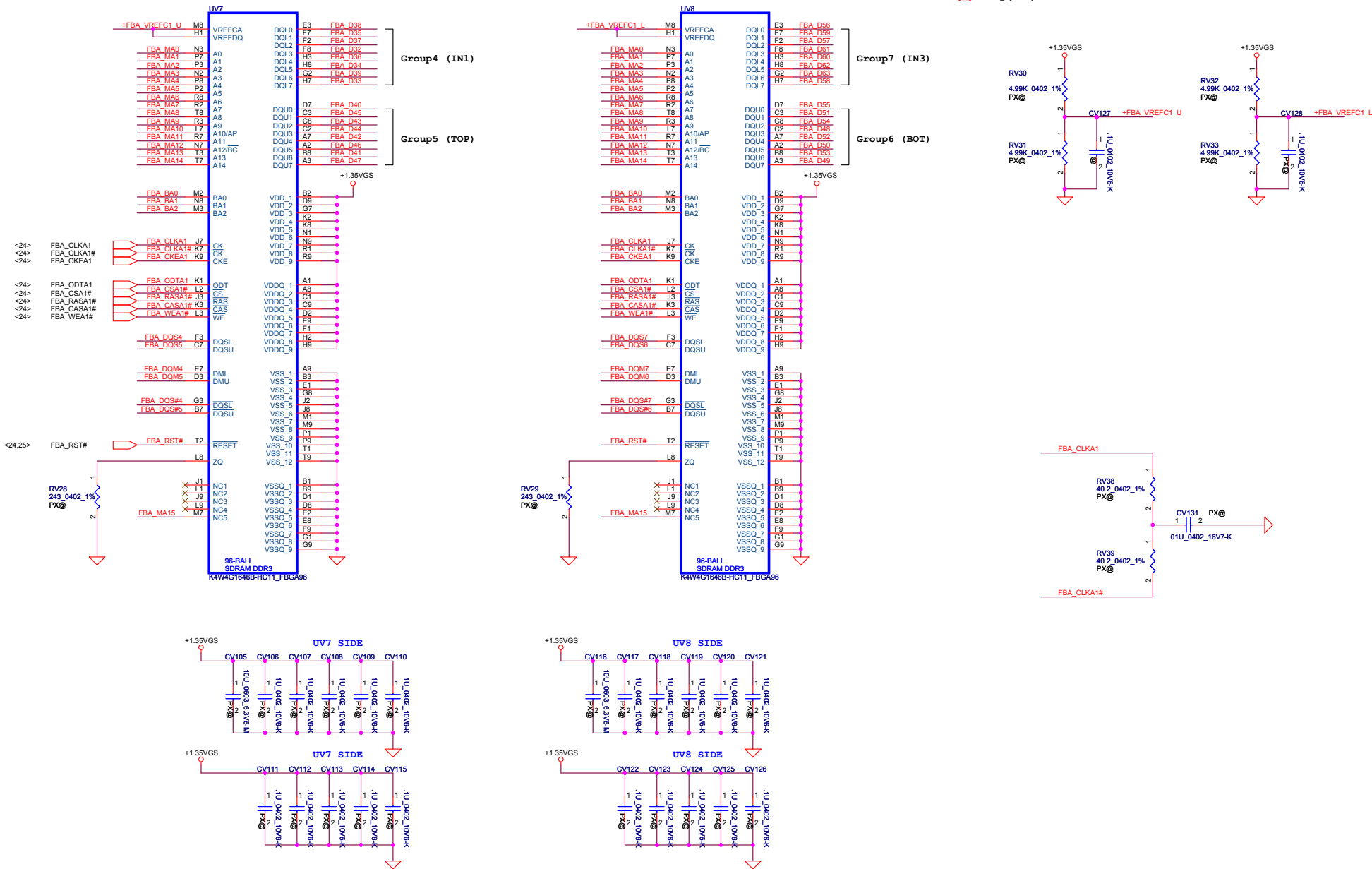
# Memory Partition A - Lower 32 bits


- FBA\_MA[15..0] <24,26>
- FBA\_BA[2..0] <24,26>
- FBA\_DQS[3..0] <24>
- FBA\_DQM[3..0] <24>
- FBA\_DQS# [3..0] <24>
- FBA\_D[31..0] <24>

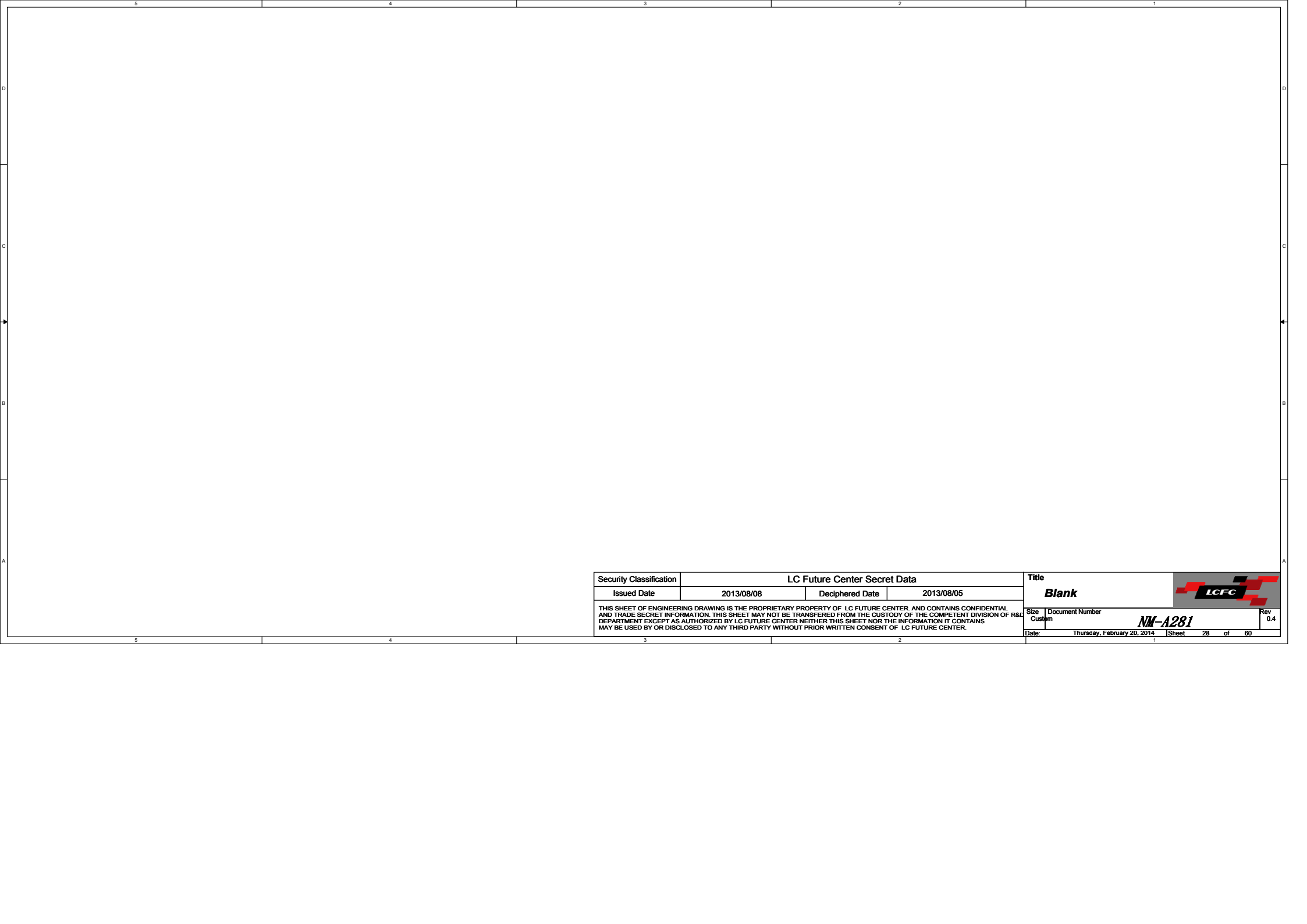
ACLU5 swap the VRAM Data @ 08/26  
 VRAM 8 pcs change to 4 pcs @ 09/26




# Memory Partition A - Upper 32 bits

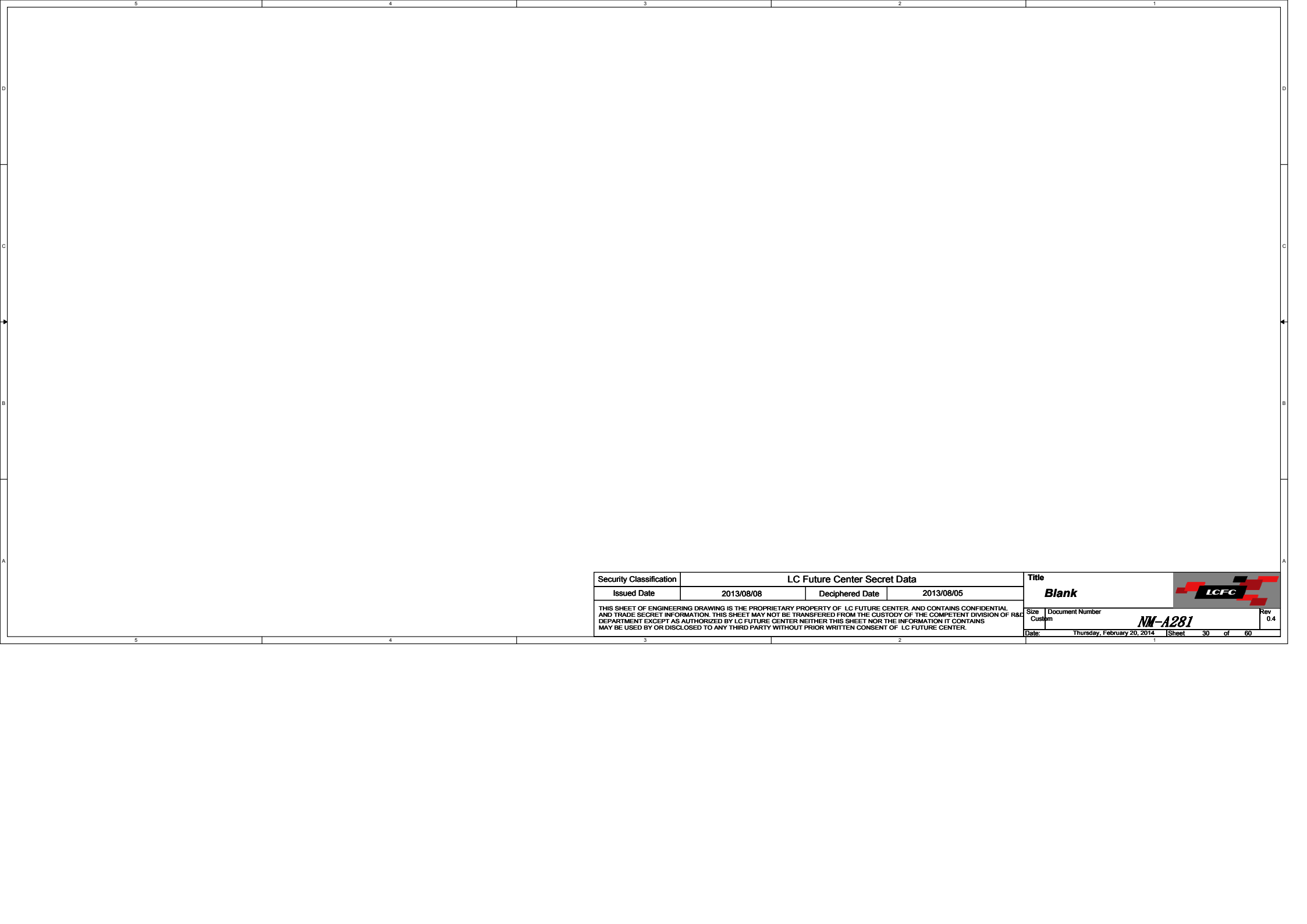



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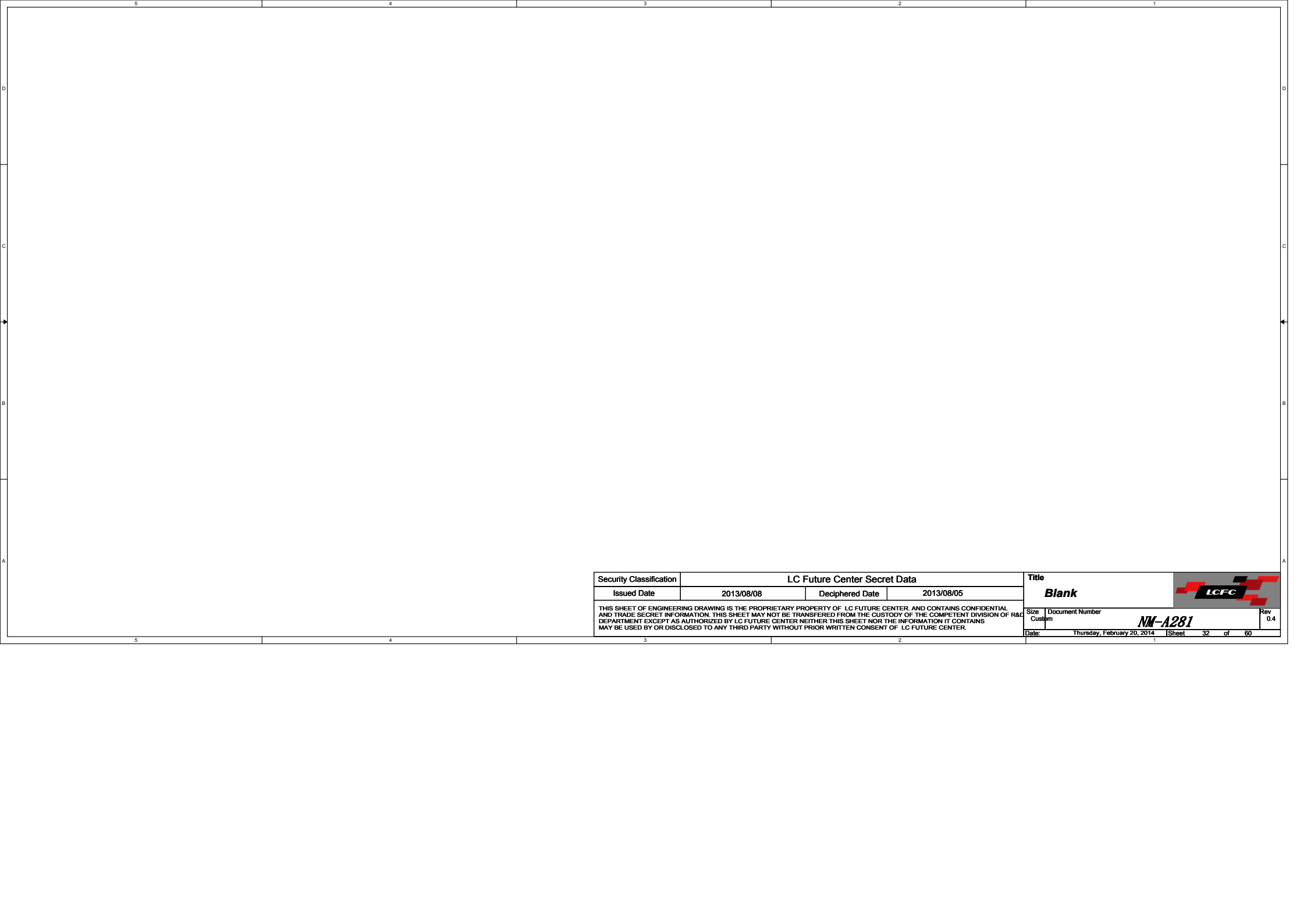
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5	4	3	2	1			
5	4	3	2	1			
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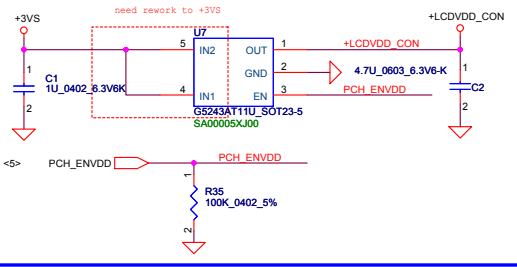
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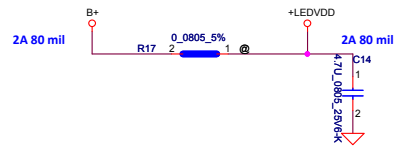
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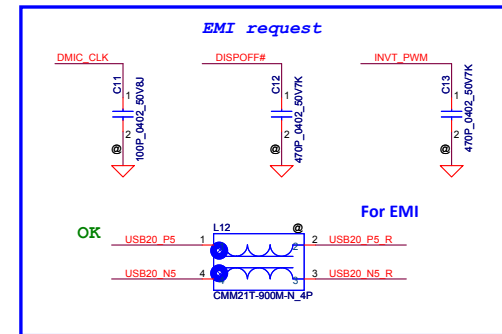
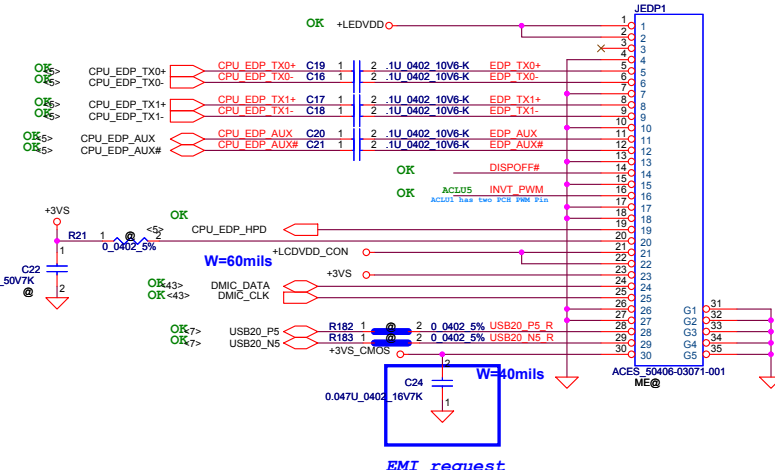
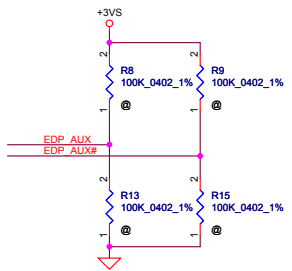
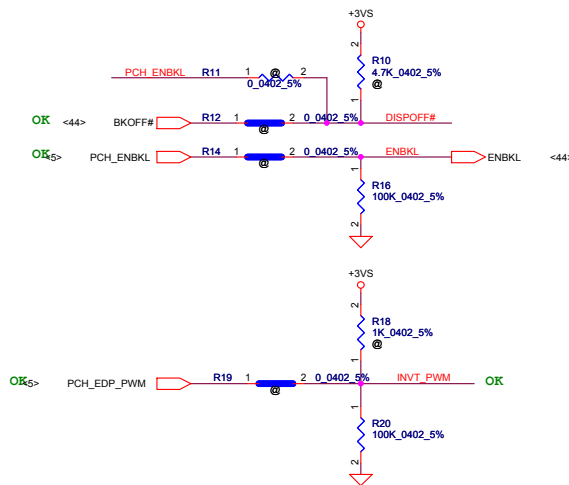
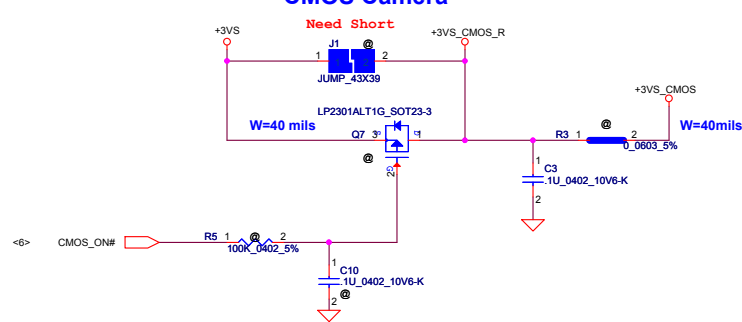
### LCD POWER CIRCUIT OK



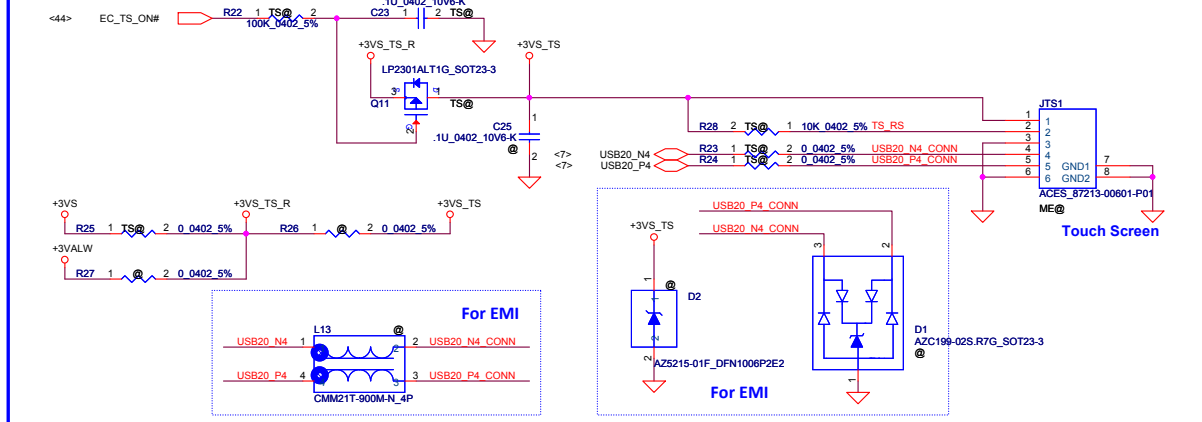
### B+ to +LEDVDD POWER OK



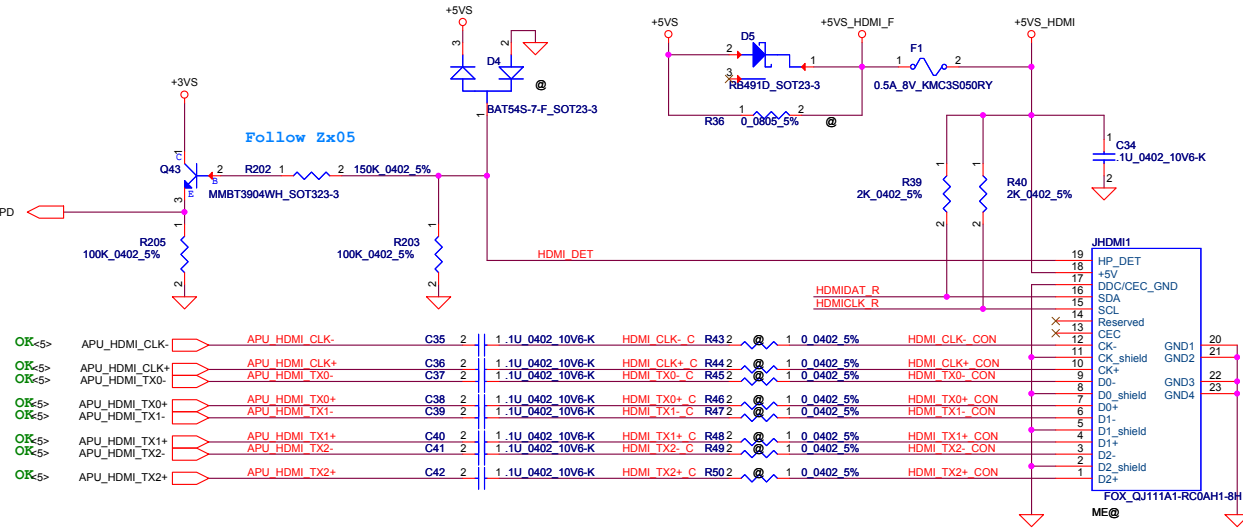
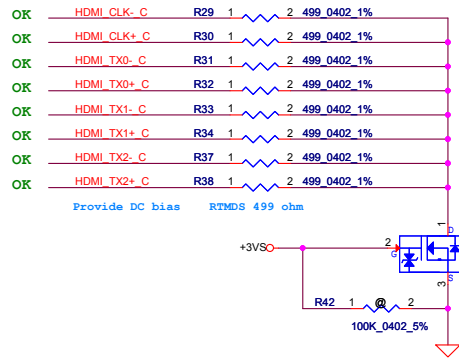
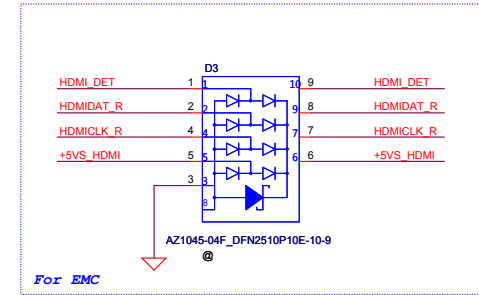
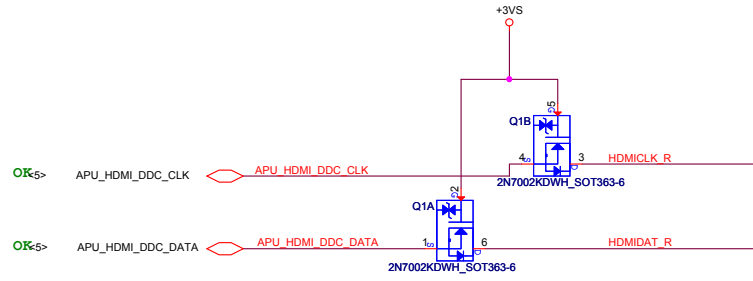
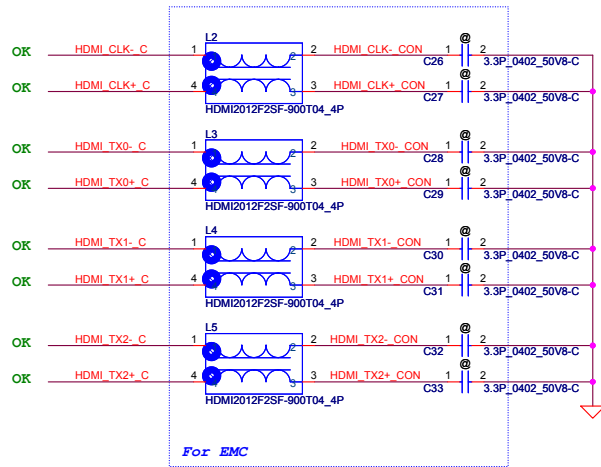
### CMOS Camera OK



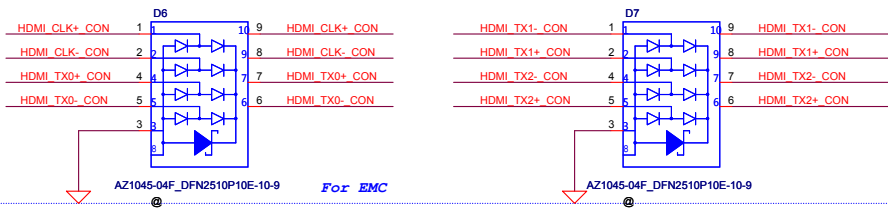
### Touch Screen OK



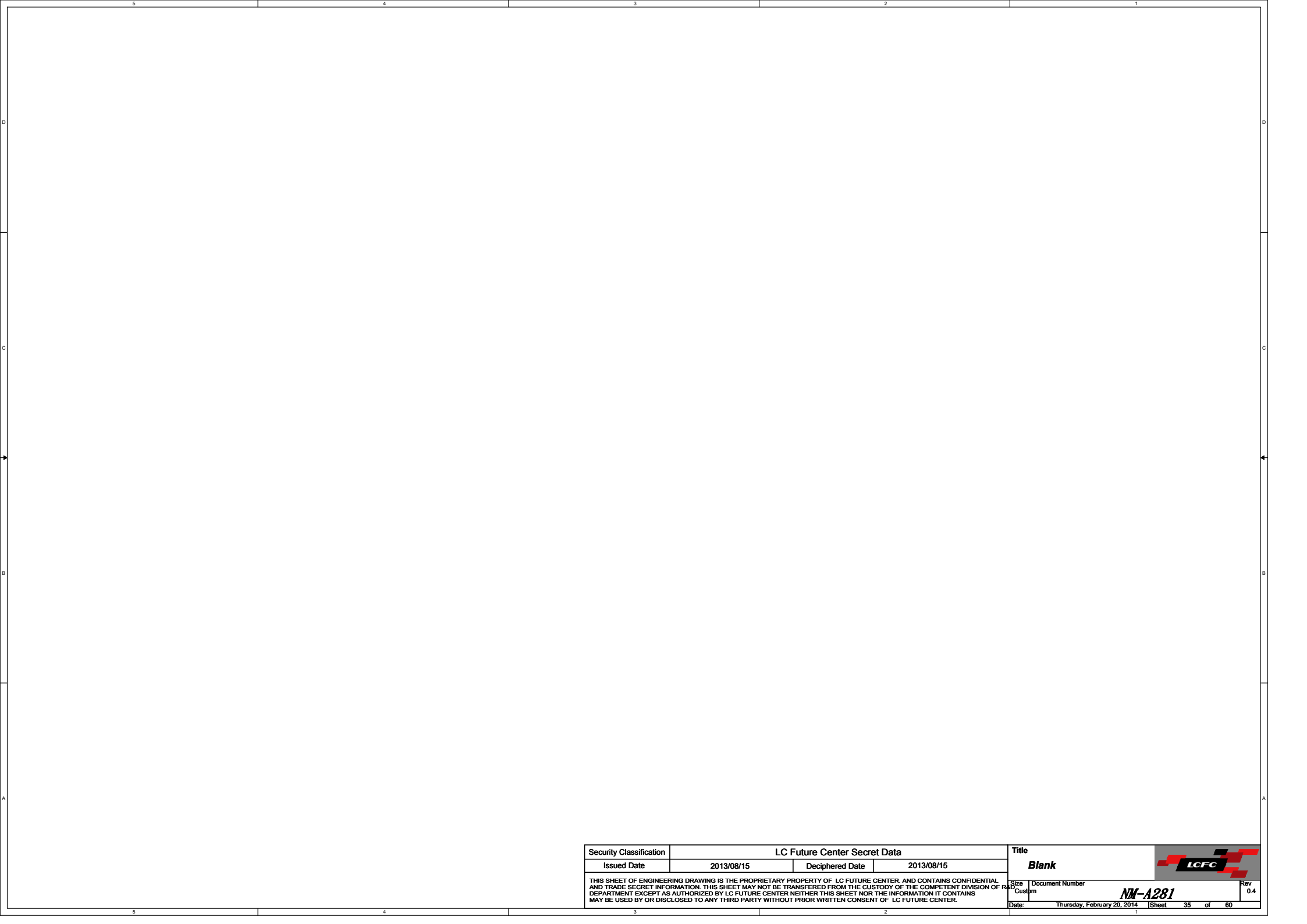
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Close to JHDMI1

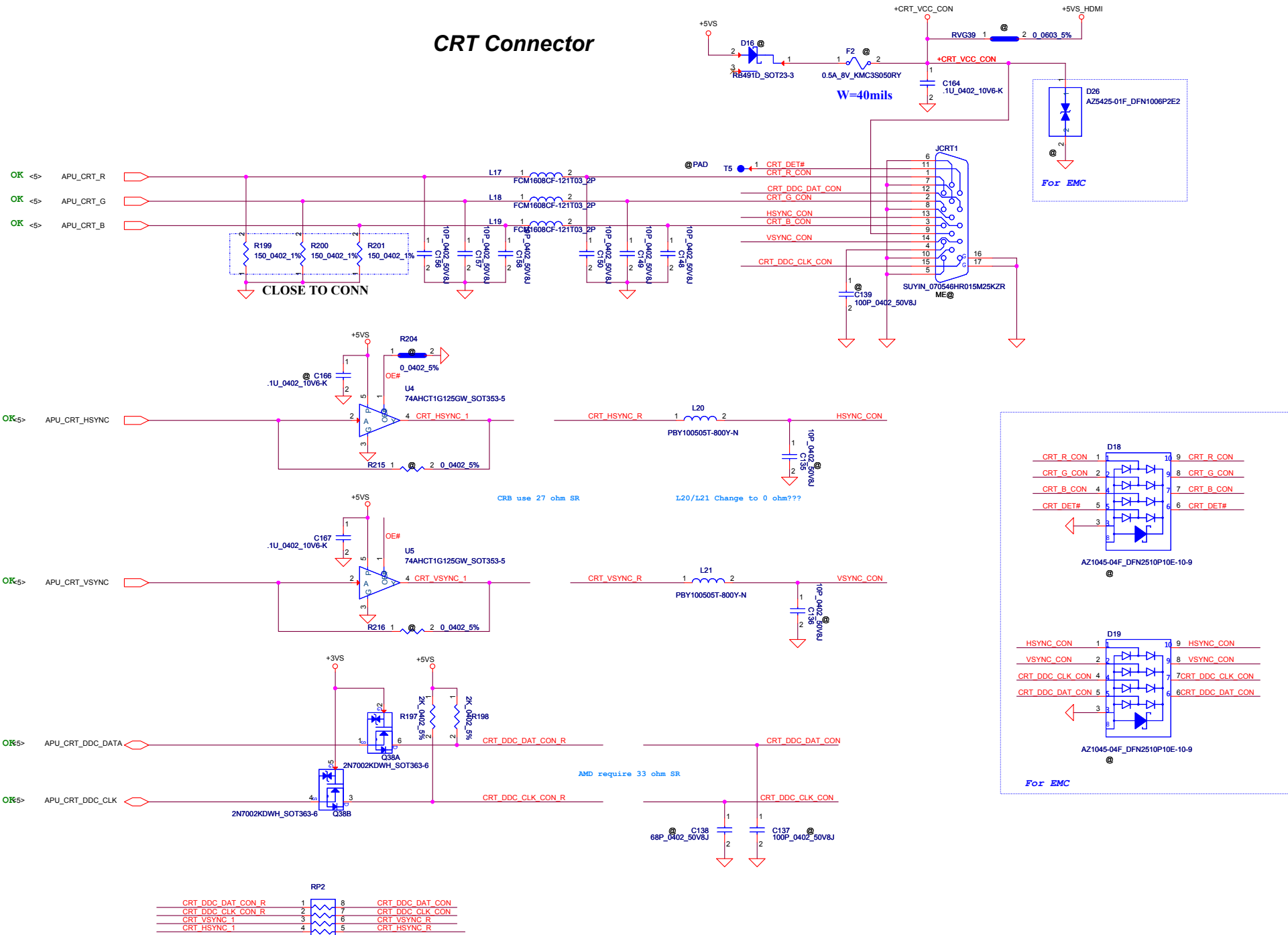


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# CRT Connector



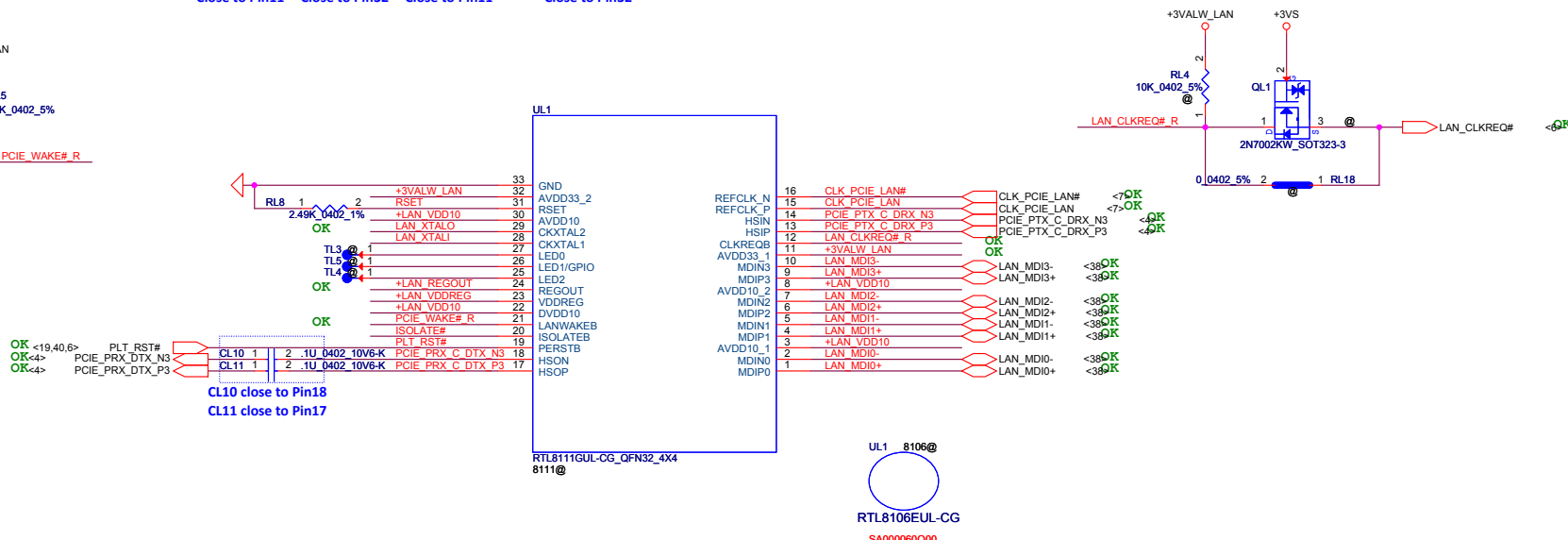
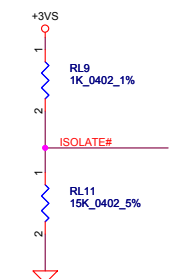
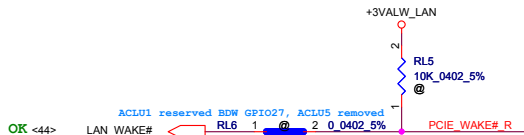
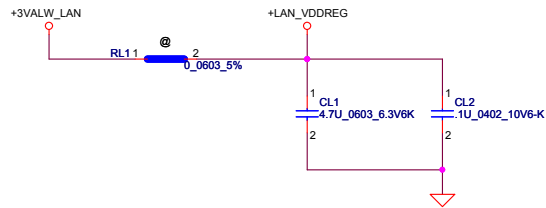
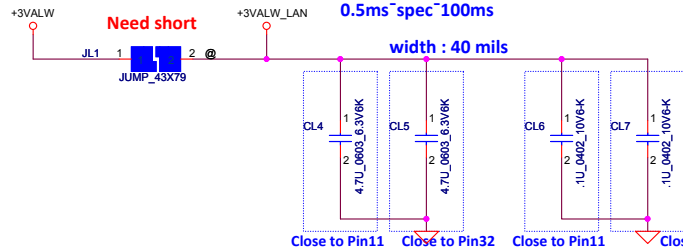
T PN change Idea pad PN SD300003700

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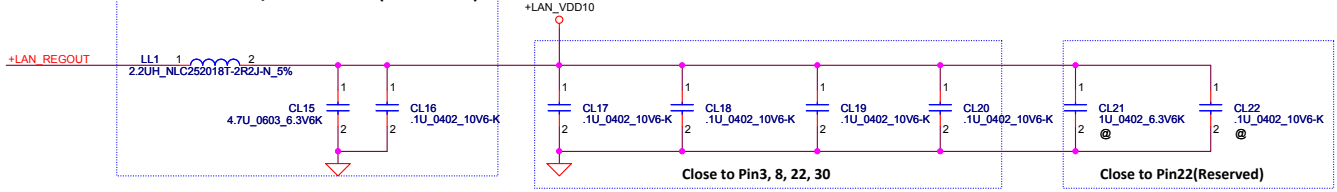
Title		LCFC	
CRT		Size	Rev
Custom	Document Number	NM-A281	0.4
Date:	Thursday, February 20, 2014	Sheet	36 of 60

+3VALW TO +3VALW\_LAN

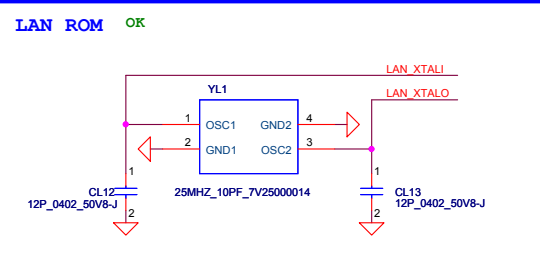
+3VALW\_LAN rising time (10%~90%):  
0.5ms spec~100ms



For RTL8111GUL/ RTL8106EUL (SWR mode)

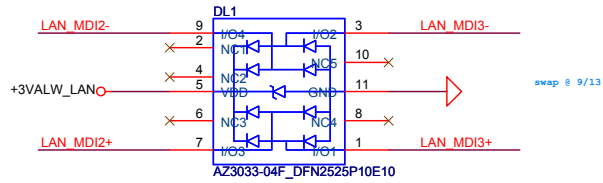


Layout Note: LL1 must be within 200mil to Pin36,  
CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil

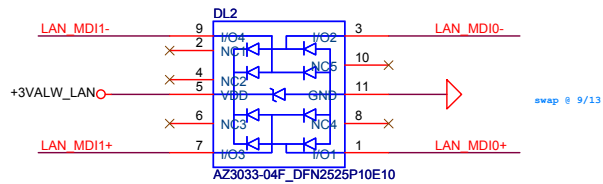


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Issued Date		2013/08/08		Deciphered Date		2013/08/05		LAN_RTL8111GUL/RTL8106E LCFC	
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	NM-A281		Thursday, February 20, 2014				Sheet		37 of 60

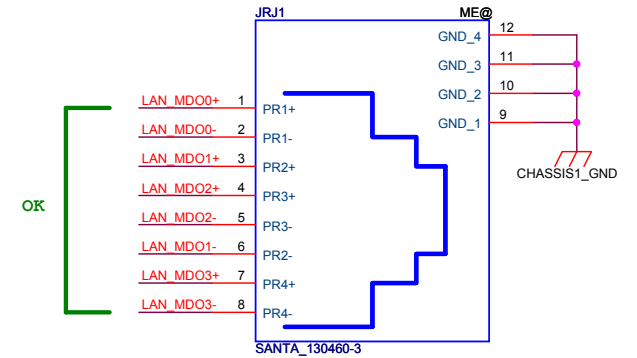
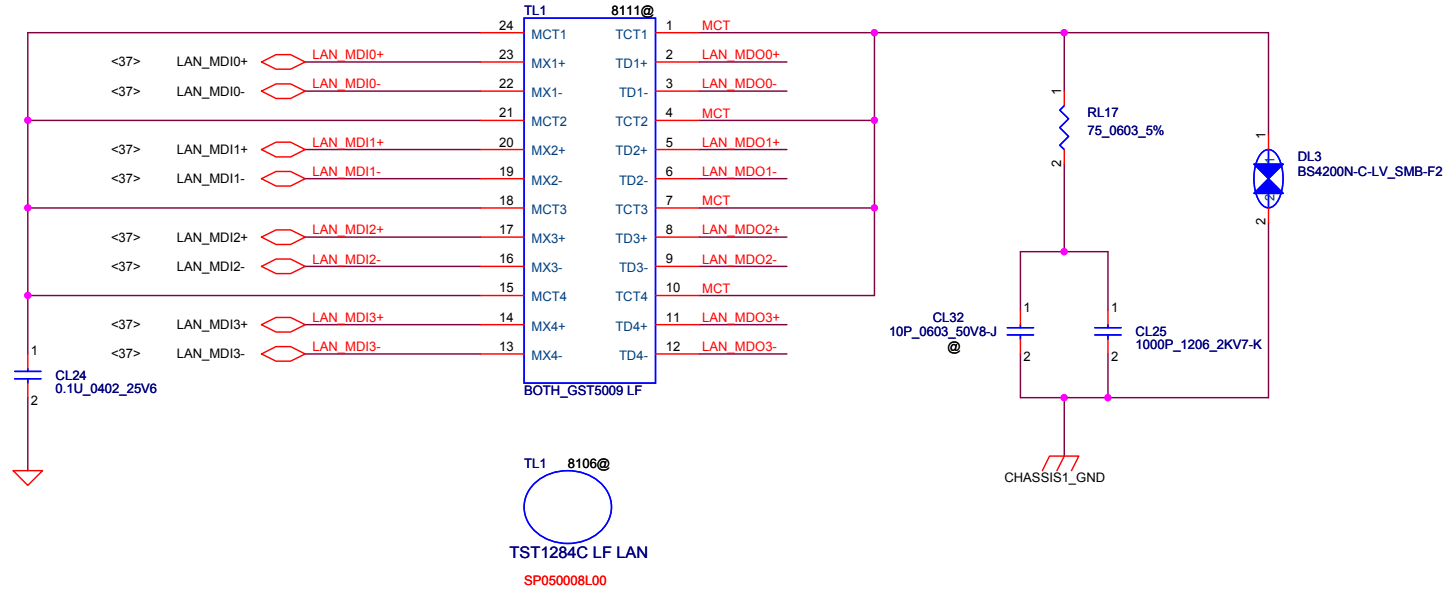
**DL1/DL2**  
1'S PN:SC30003M00




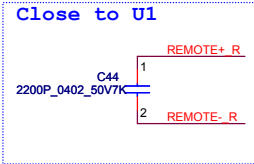
Place Close to TL1



Place Close to TL2

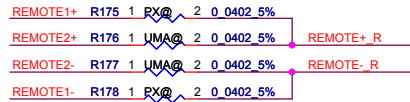
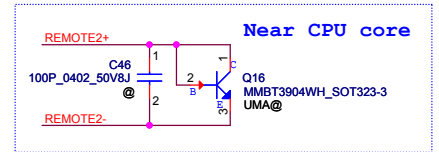
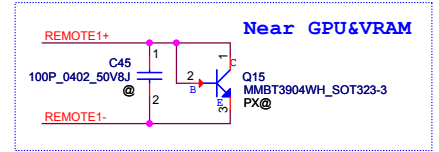
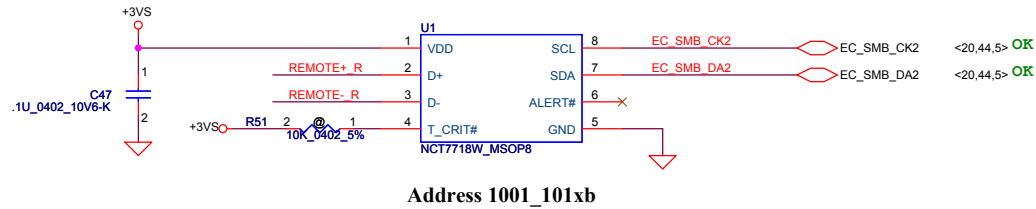


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Document Number	
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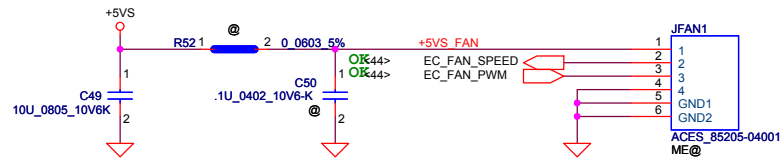
**SMSC thermal sensor placed near DIMM**

OK



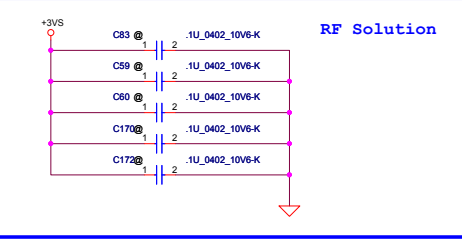
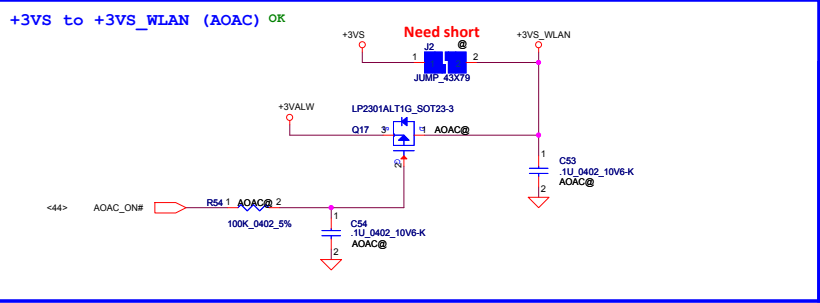
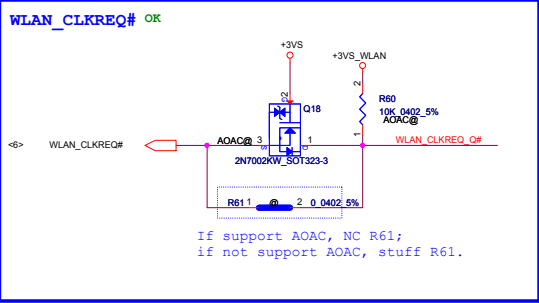
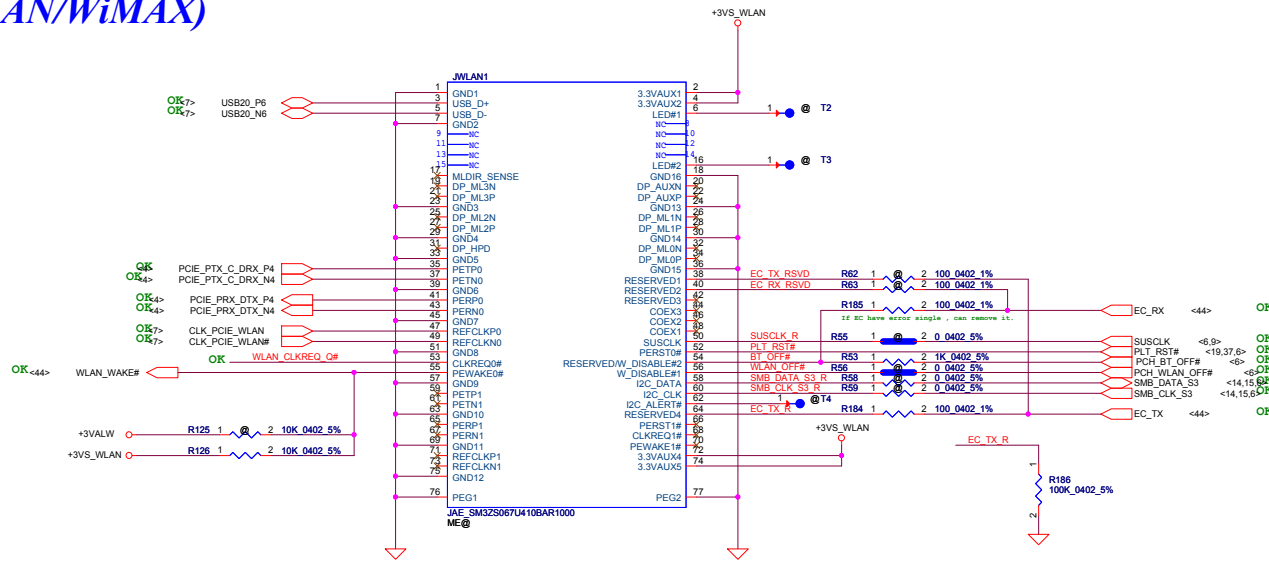
REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

**FAN Conn**



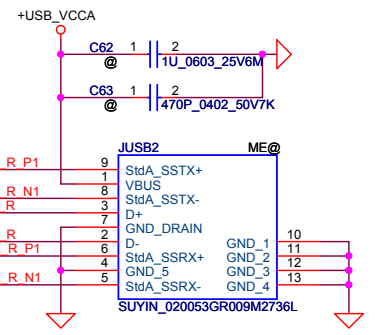
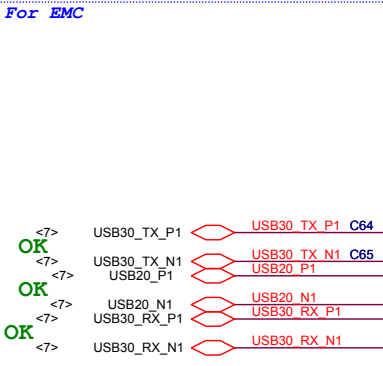
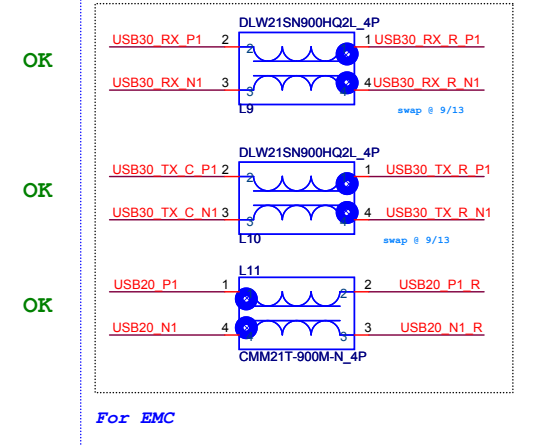
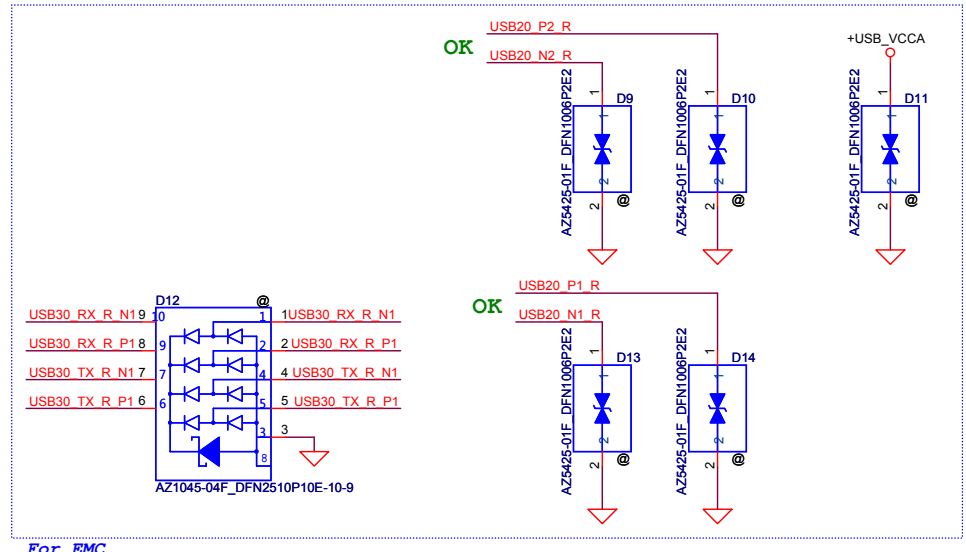
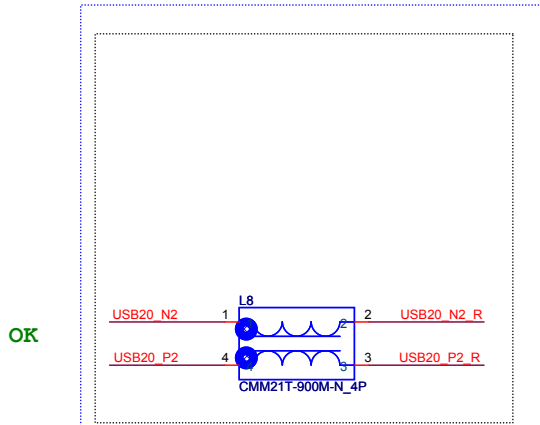
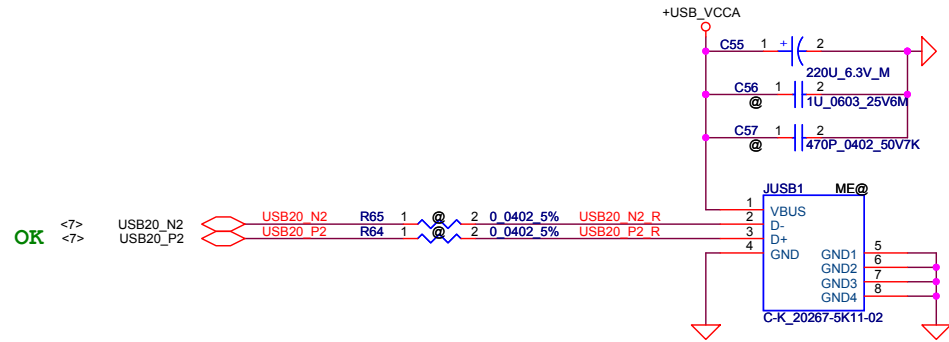
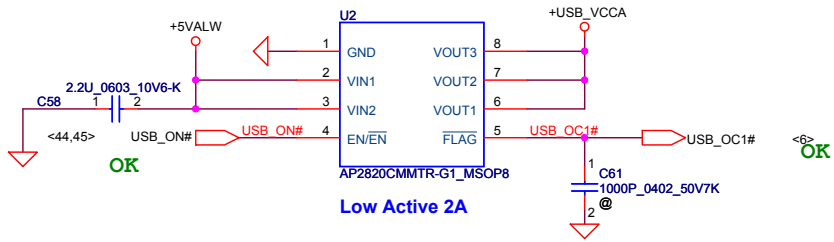
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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# Mini-Express Card(WLAN/WiMAX)





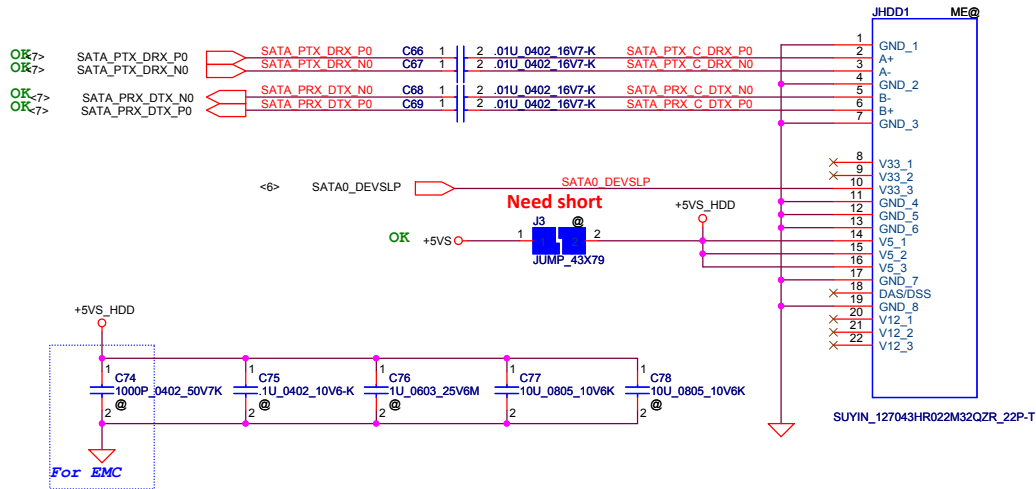
# LEFT SIDE USB3.0 PORT X2



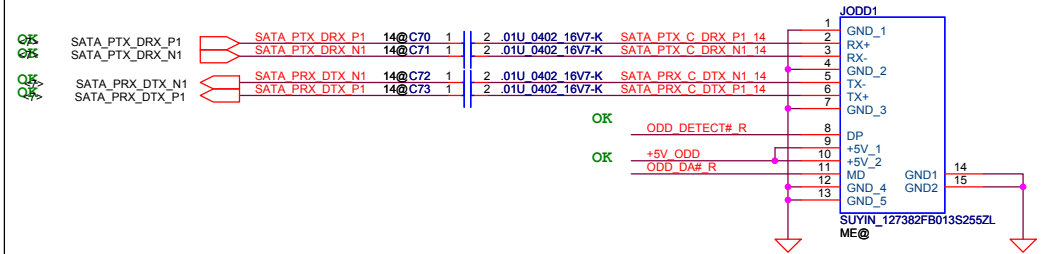
Security Classification			
LC Future Center Secret Data			
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title	
USB2.0/USB3.0 PORT (LEFT)	
Size	Document Number
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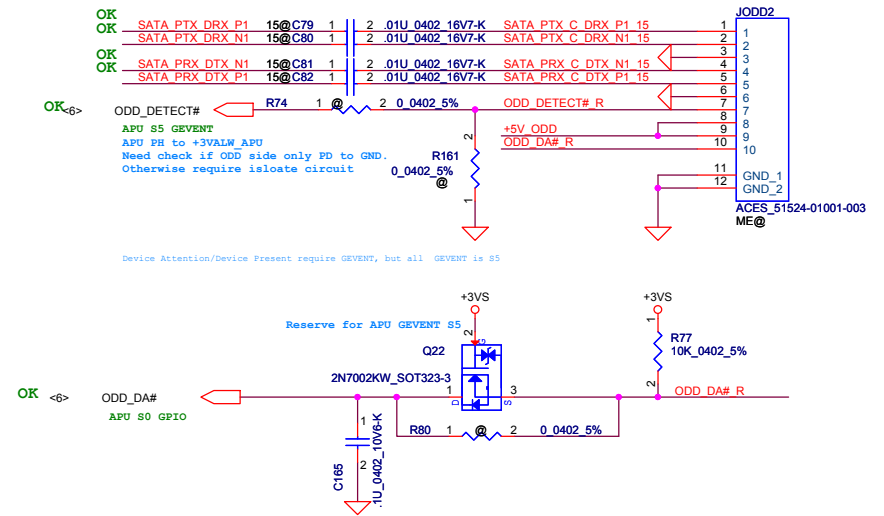
### SATA HDD Conn.



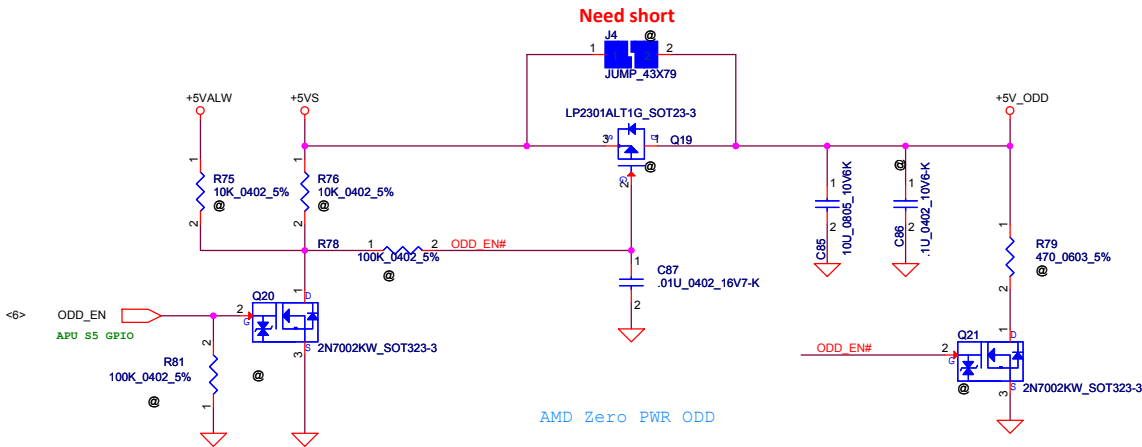
### FOR 14" SATA ODD Conn.



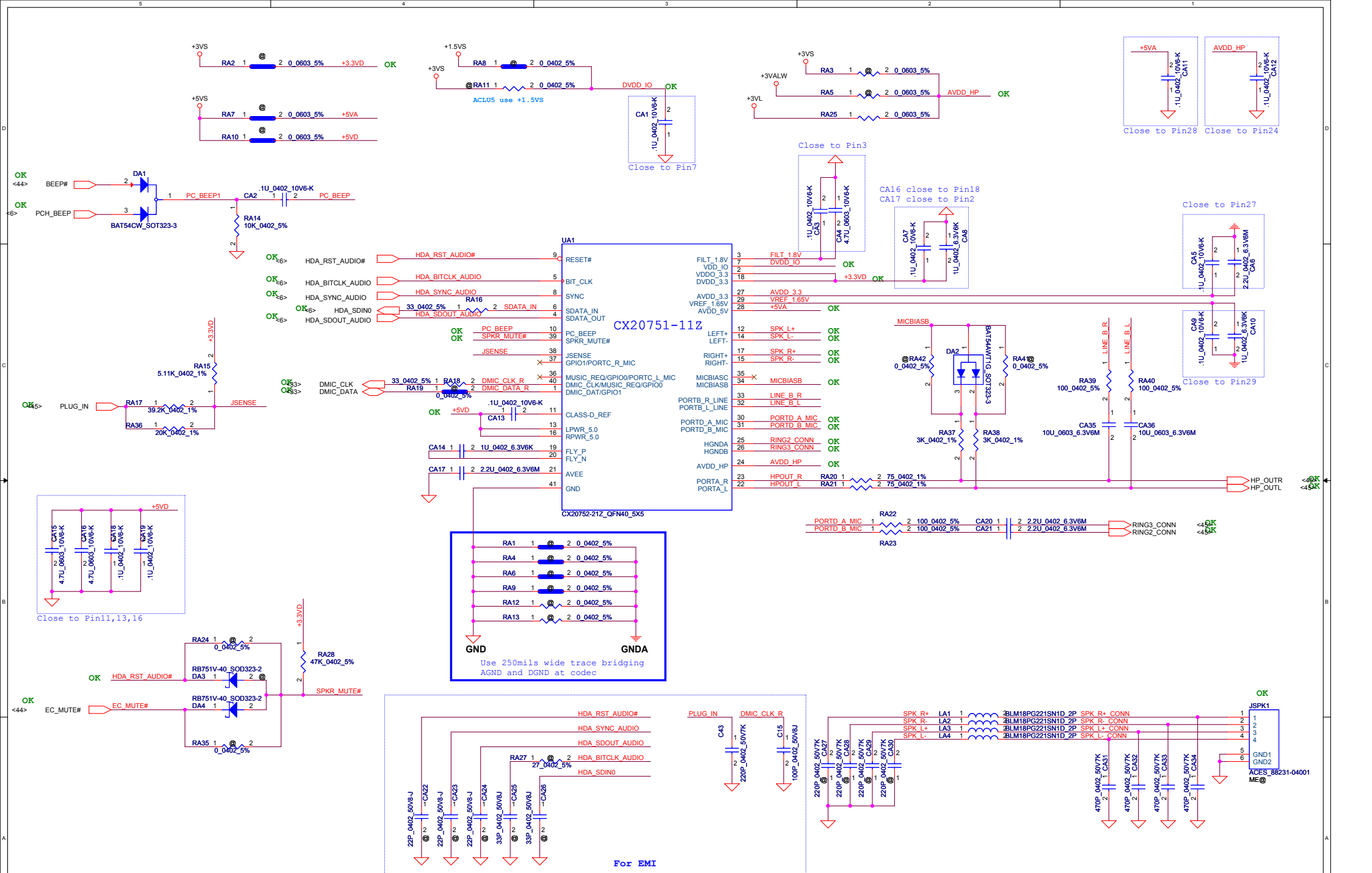
### FOR 15" SATA ODD FFC Conn



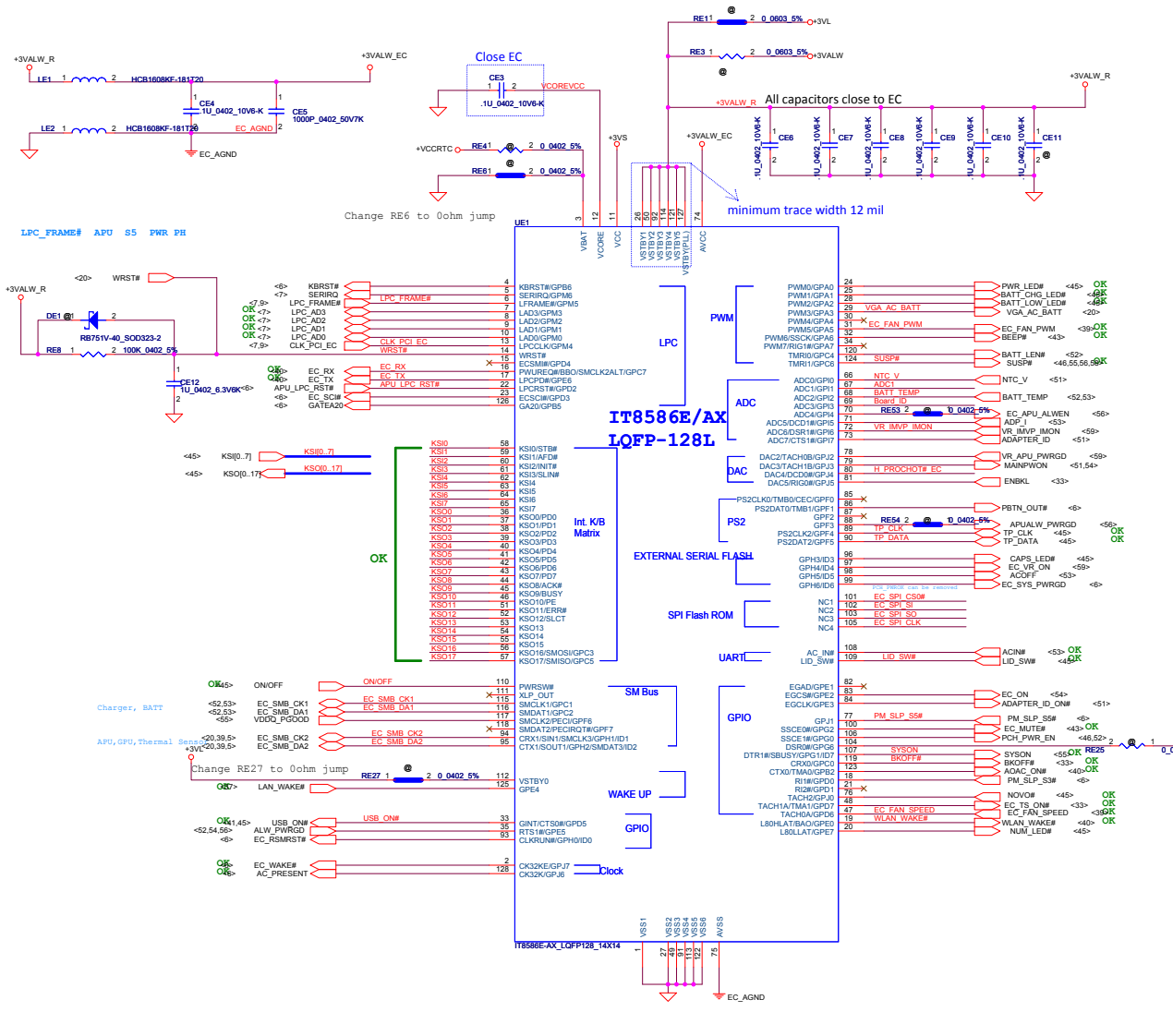
### +5VS to +5V\_ODD OK



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				Custom		NM-A281		0.4	
Date:				Thursday, February 20, 2014		Sheet		42 of 60	



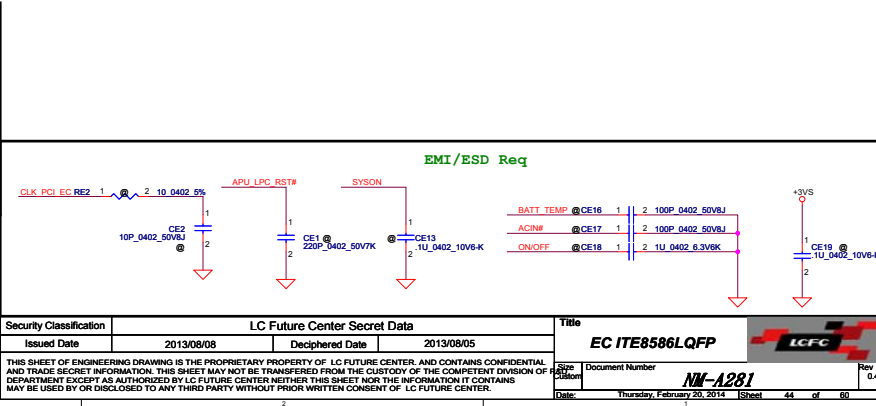
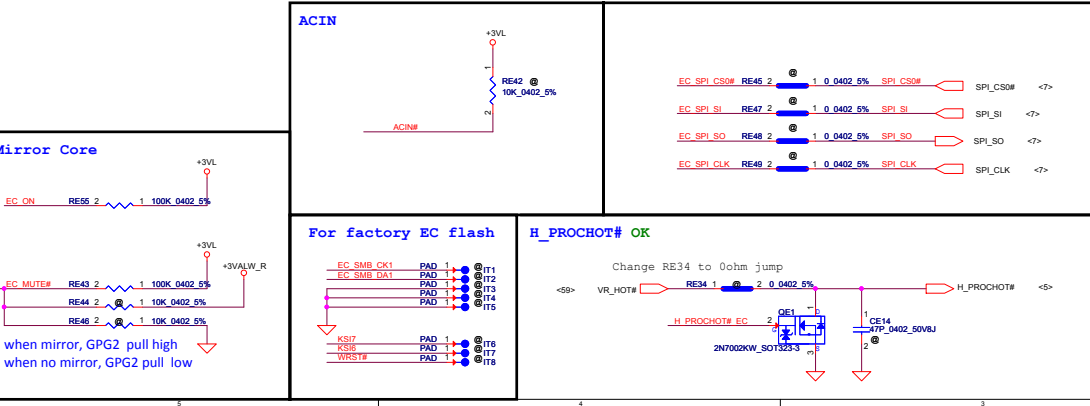
Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Size	Document Number	Rev	
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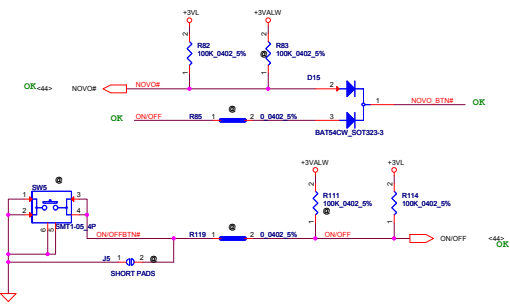
**BORAD ID Config**

Vcc	3.3V +/- 5%
RE33	100K +/- 1%

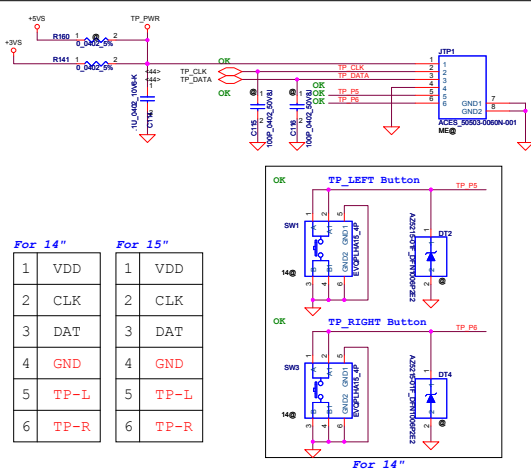
Board ID	RE34	V <sub>AD_BTD</sub> min	V <sub>AD_BTD</sub> typ	V <sub>AD_BTD</sub> max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



### ON/OFF switch



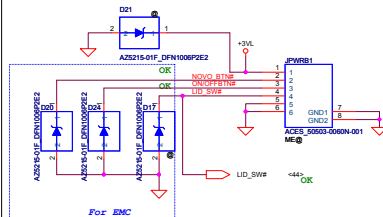
### TP/B Connector



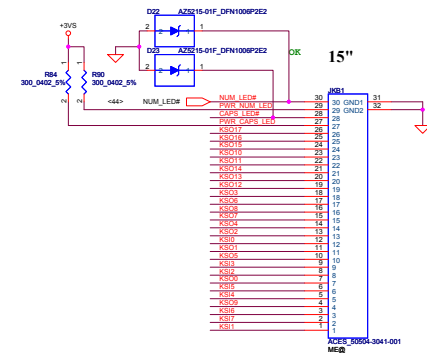
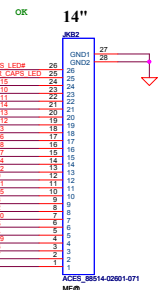
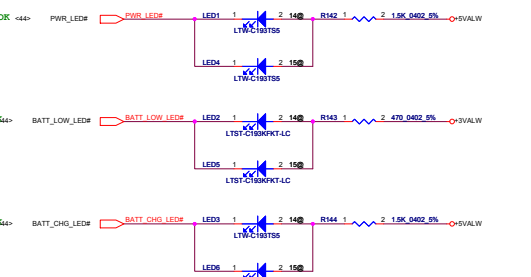
### K/B Connector



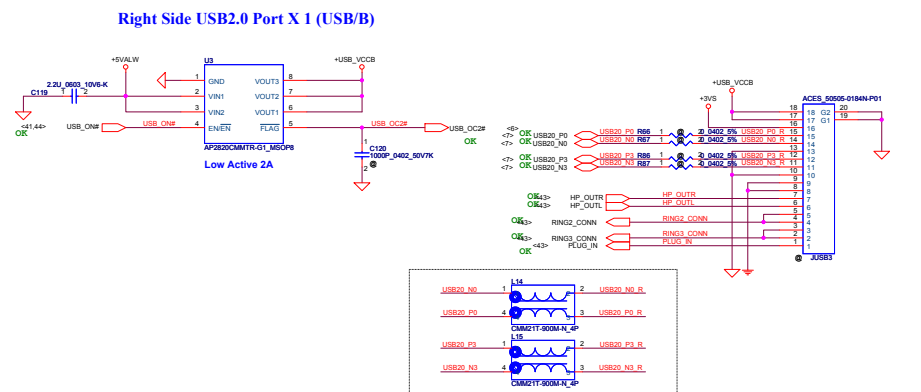
### PWR/B Connector



### LED

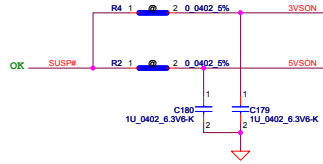


### USB I/O Connector

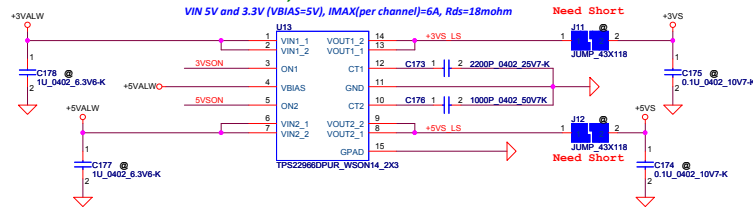


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Issued Date				Deciphered Date				KBD/PWR/LED/TP Conn.	
2013/08/08				2013/08/05				LCFC	
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11x17		NW-A281		February 21, 2014		45		04	

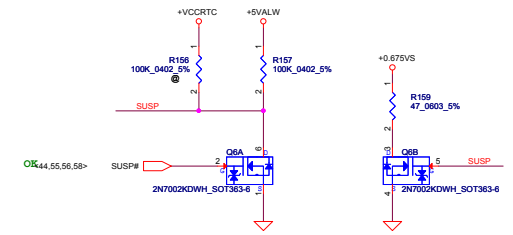
**Load Switch**  
**+5VALW To +5VS OK**  
**+3VALW To +3VS**



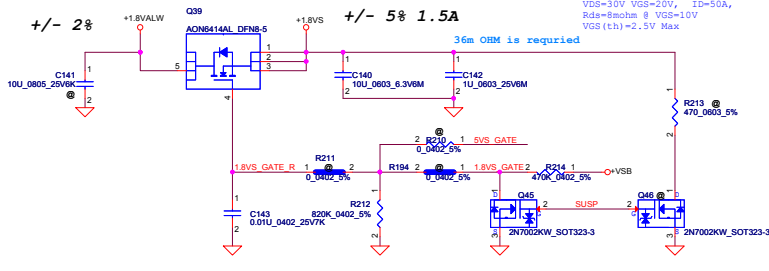
**+5VS, C159 --> 1.5ms**  
**+3VS, C160 --> 2.5ms**



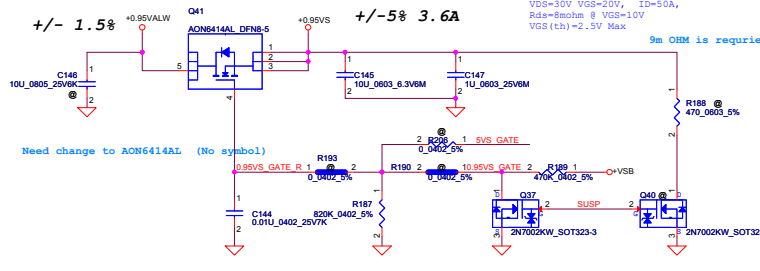
**For DisCharge**



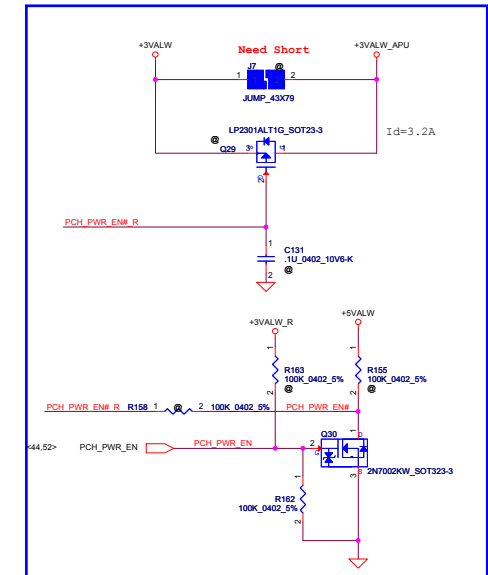
**+1.8VALW to +1.8VS**



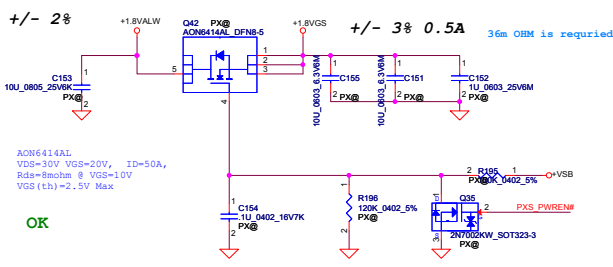
**+0.95VALW to +0.95VS**



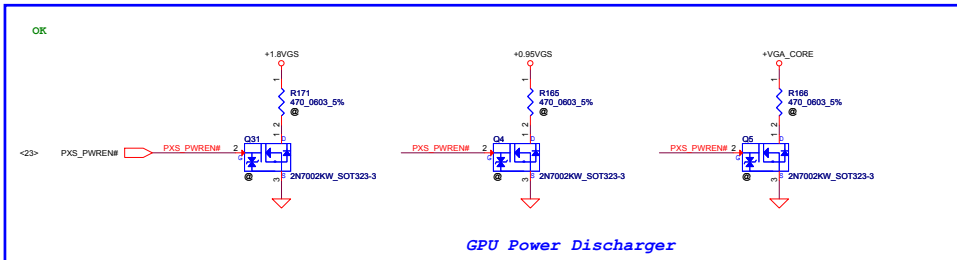
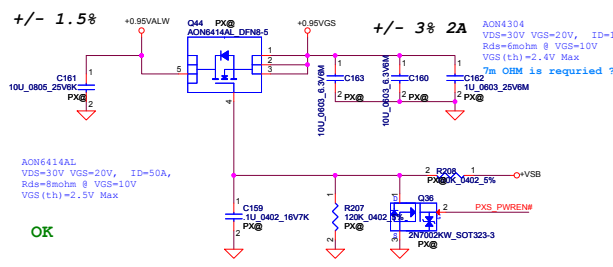
**Need check all the EN pin and PWR Sequence.**



**+1.8VALW to +1.8VGS Reserve for GPU/APU share +1.8V**



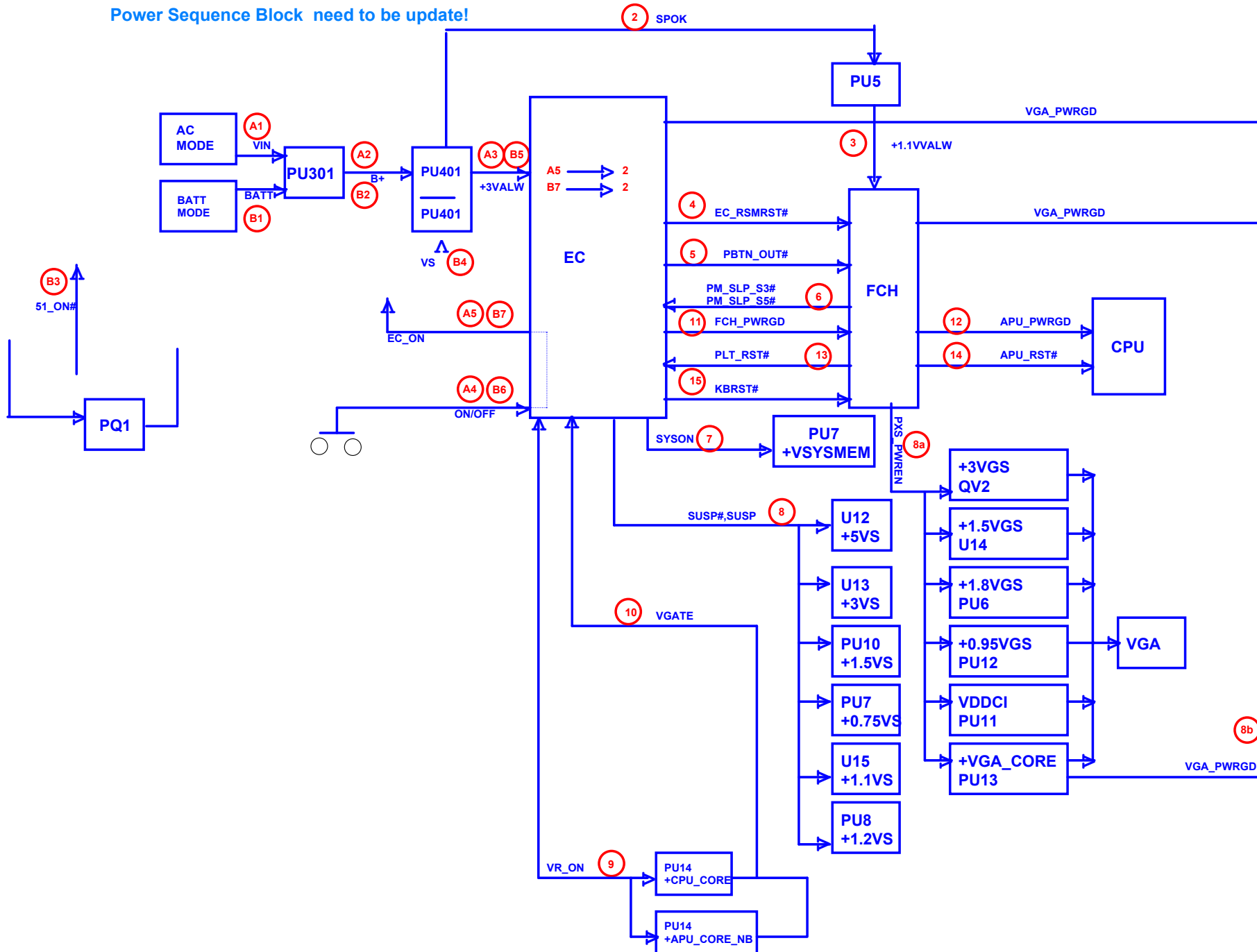
**+0.95VALW to +0.95VGS Reserve for GPU/APU share +0.95V**



**GPU Power Discharge**

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Customer:				Rev 0.4
Date: Thursday, February 20, 2014 1:58:48 PM				Sheet 46 of 60

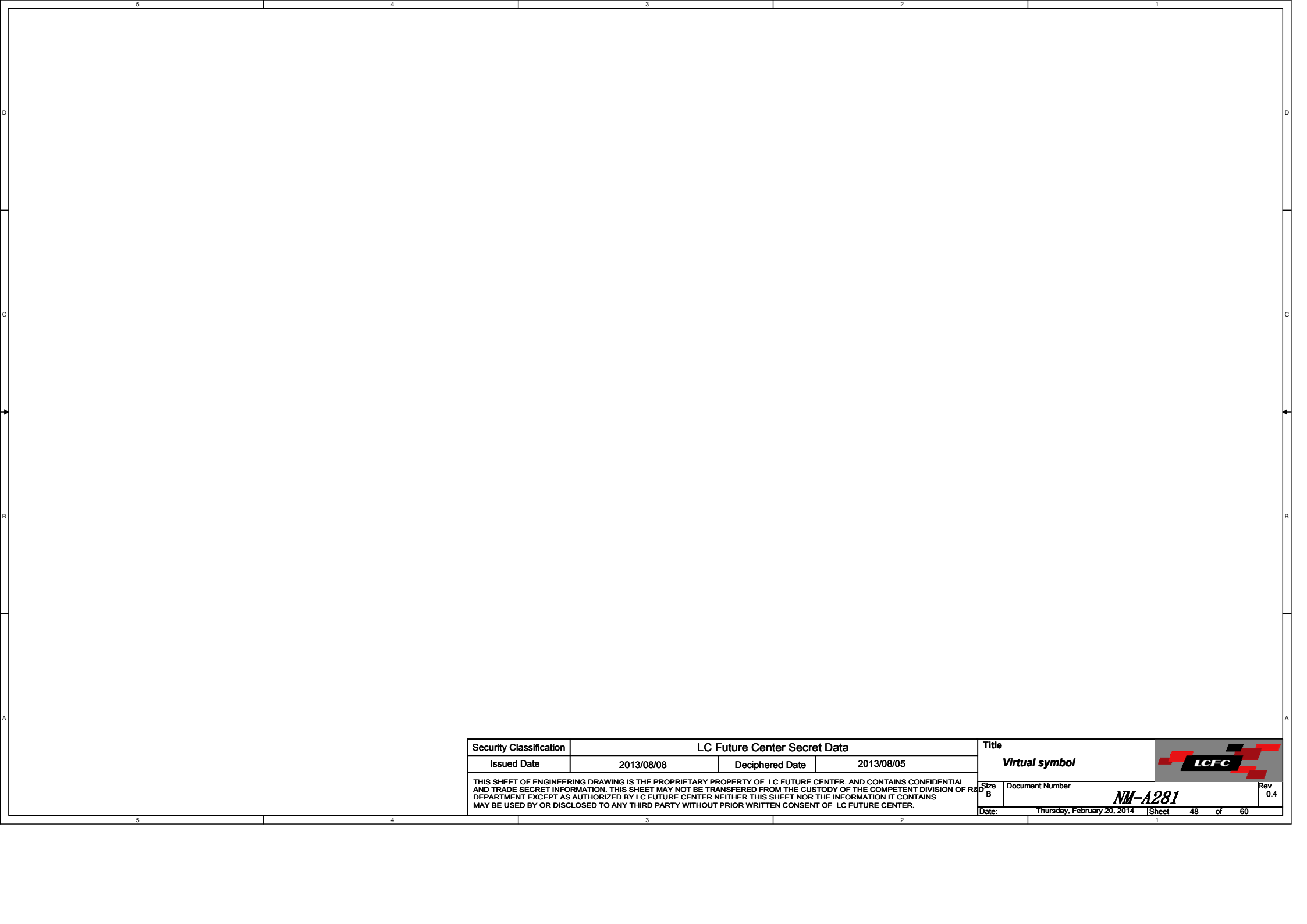
Power Sequence Block need to be update!




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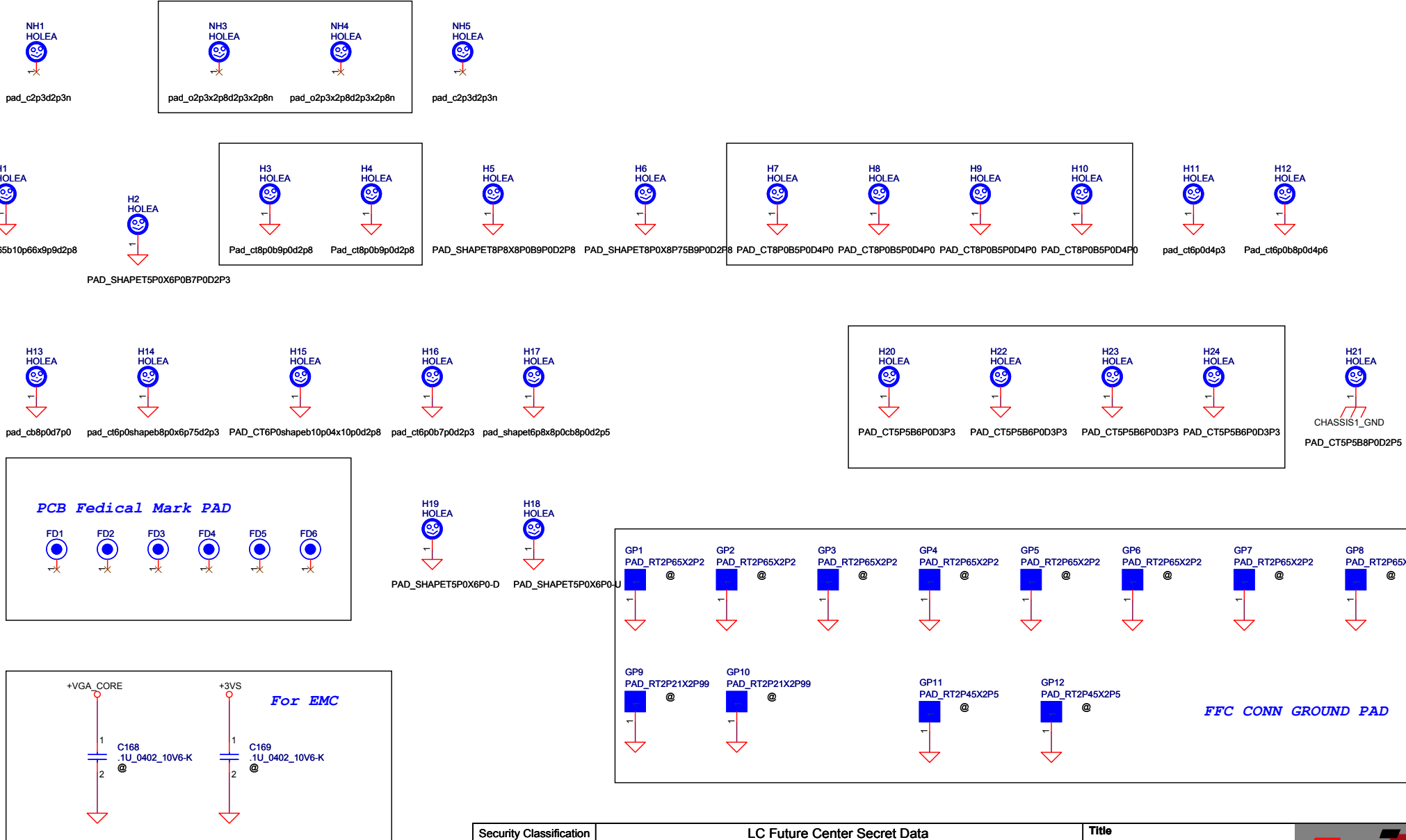
Size	Document Number	Rev
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Date:	Thursday, February 20, 2014	Sheet 47 of 60




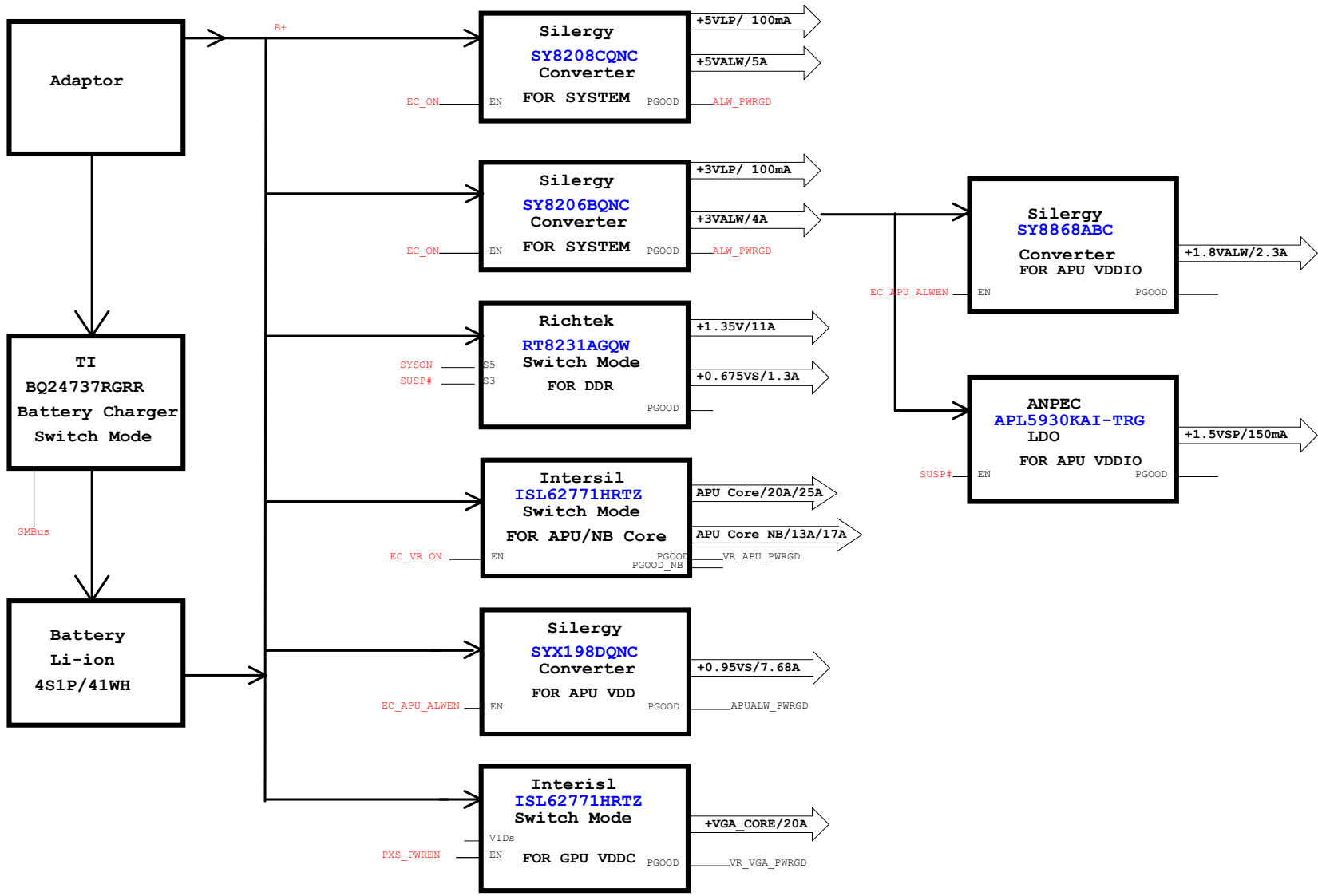


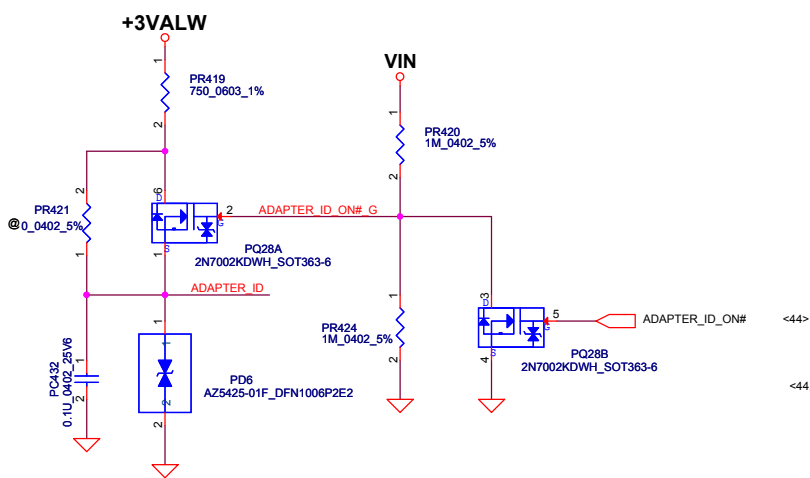
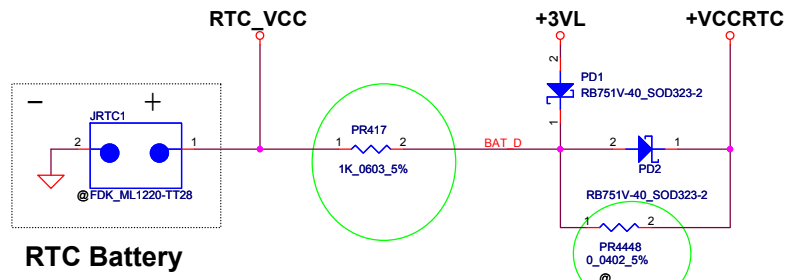
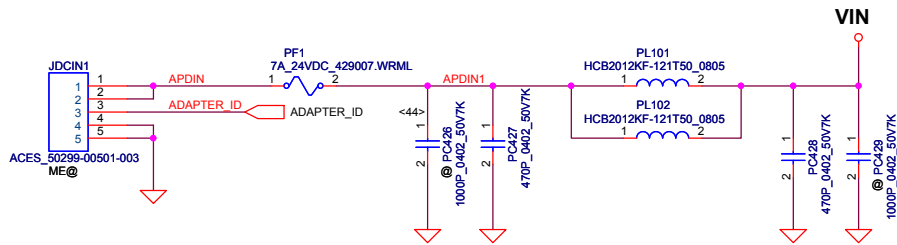
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	<b>Virtual symbol</b>		
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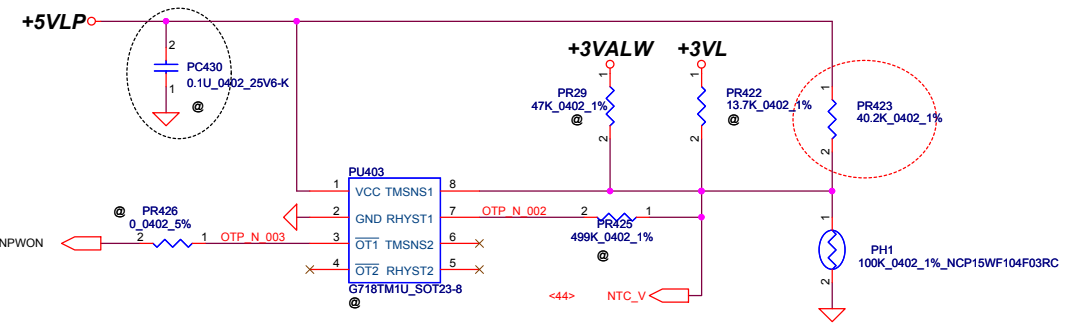


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				<b>NM-A281</b> Date: Thursday, February 20, 2014 Sheet 49 of 60	

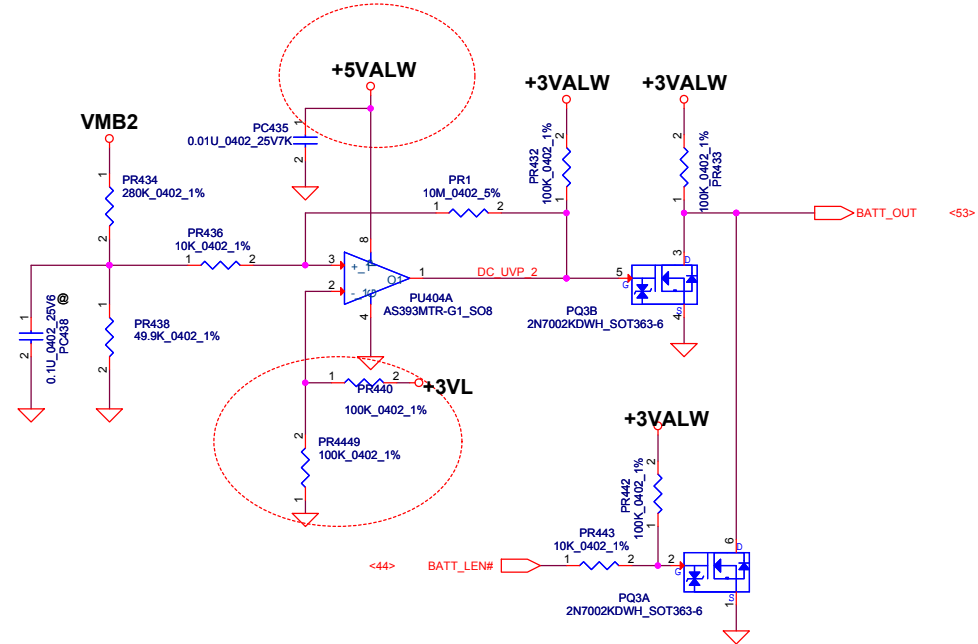
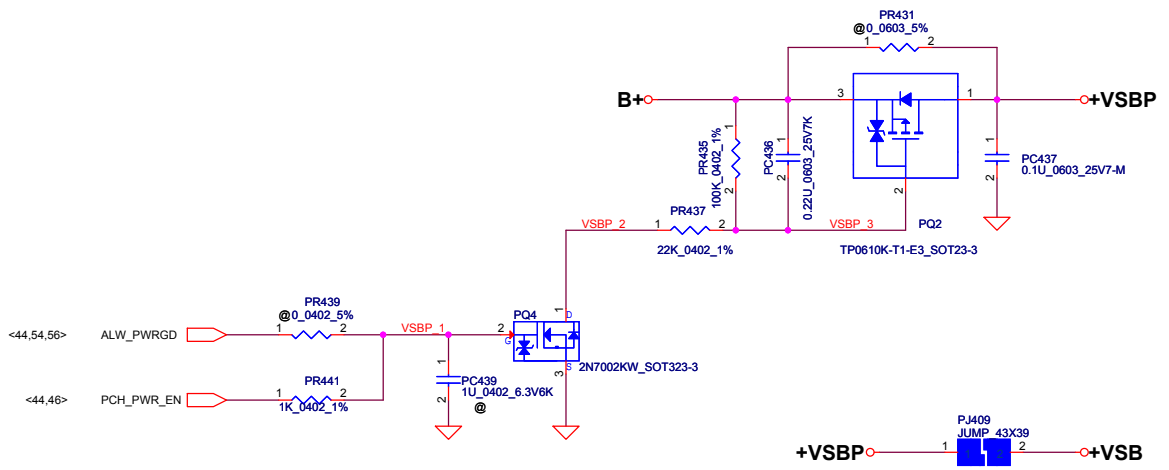
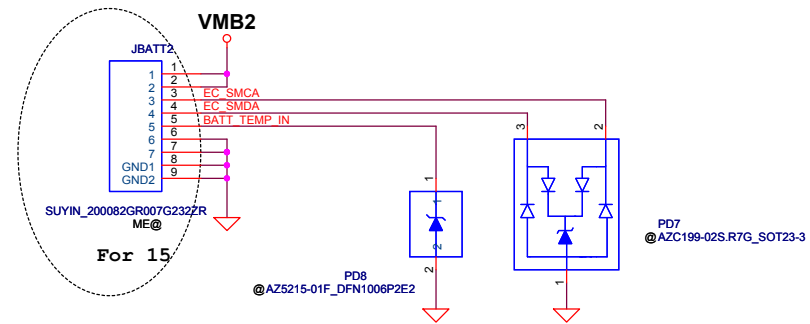
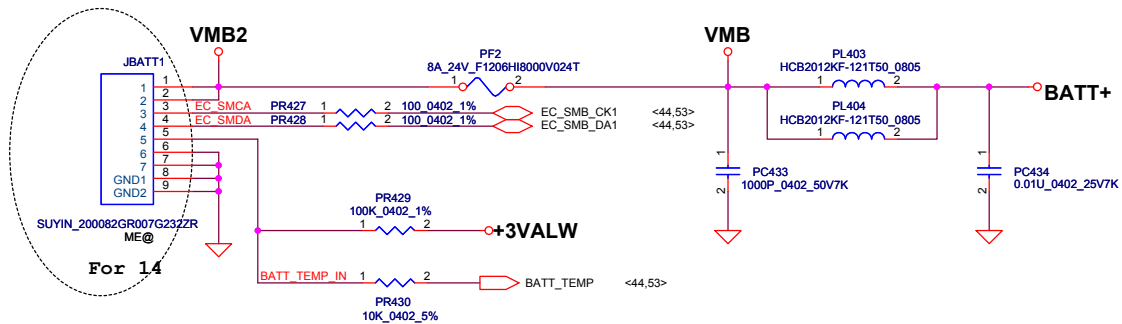




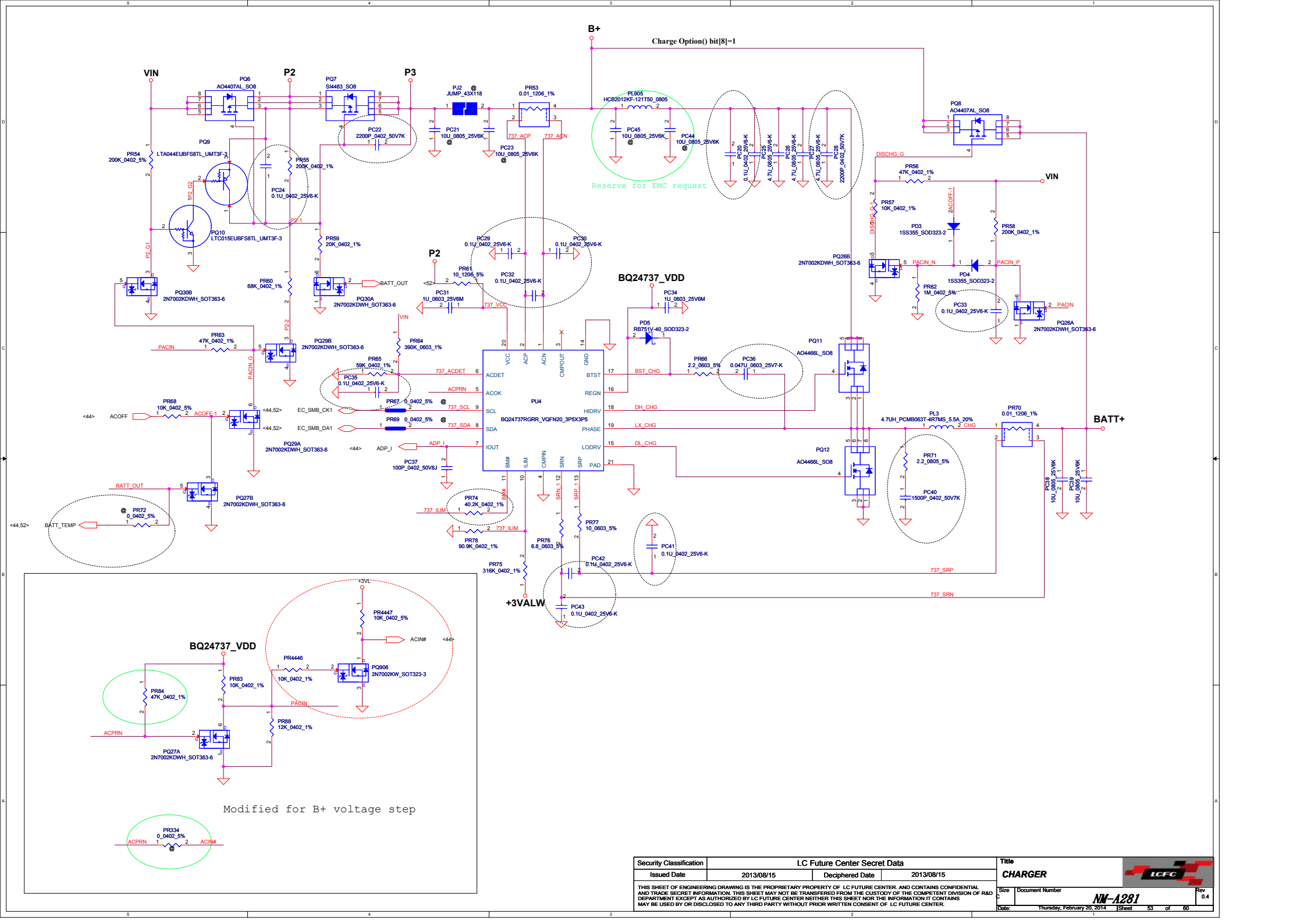
**PH1 under CPU bottom side :**  
**CPU thermal protection at 92+3 degree C**  
**Recovery at 56 +3 degree C**



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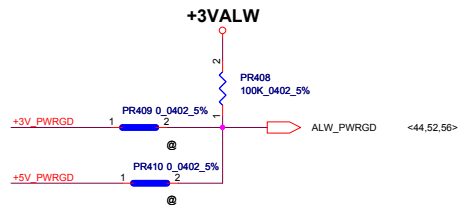
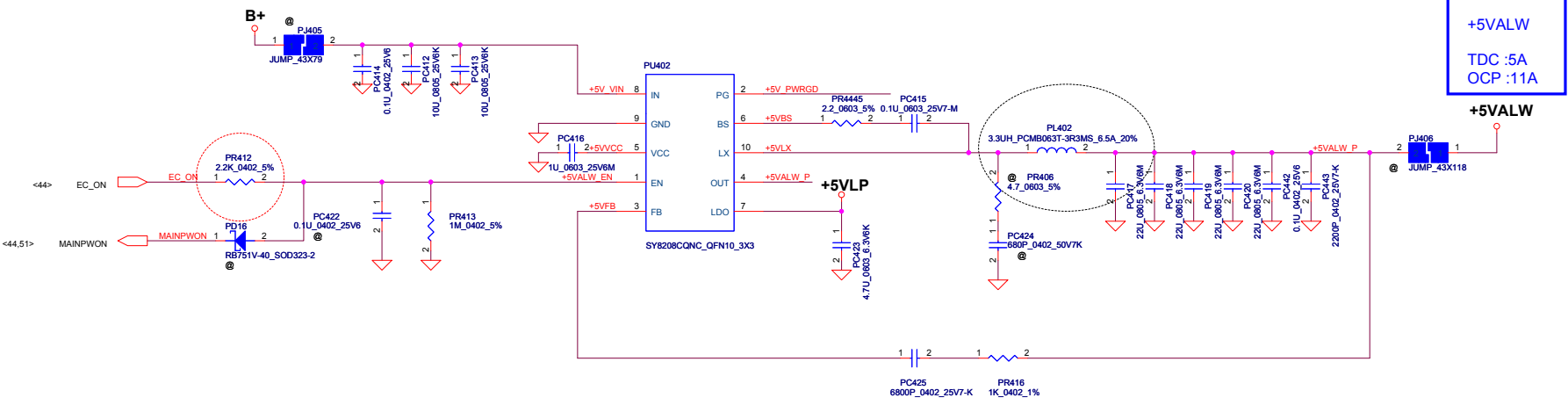
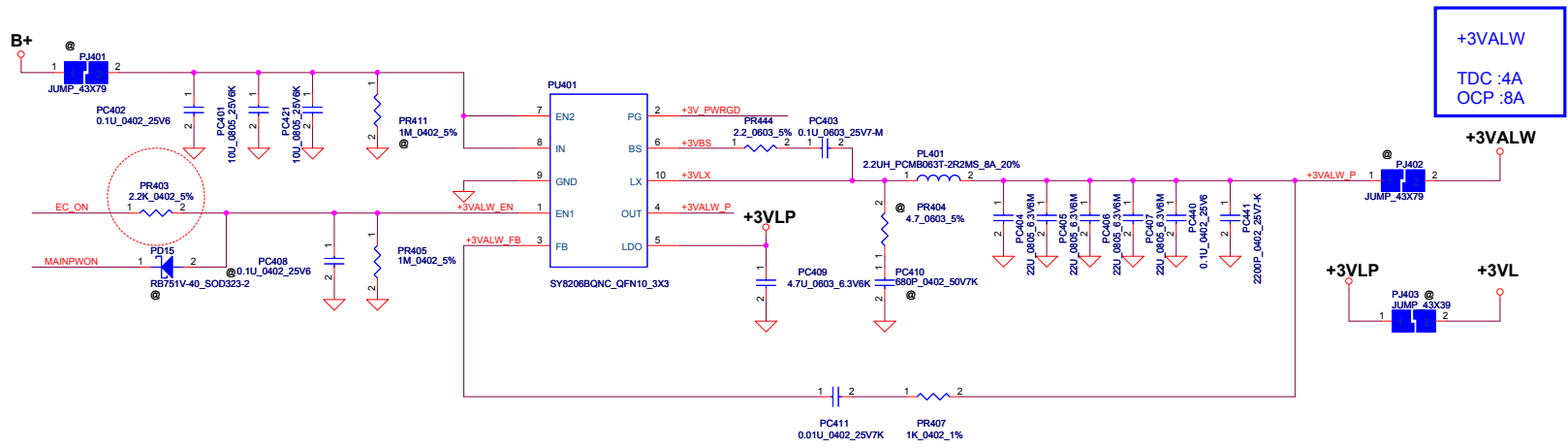


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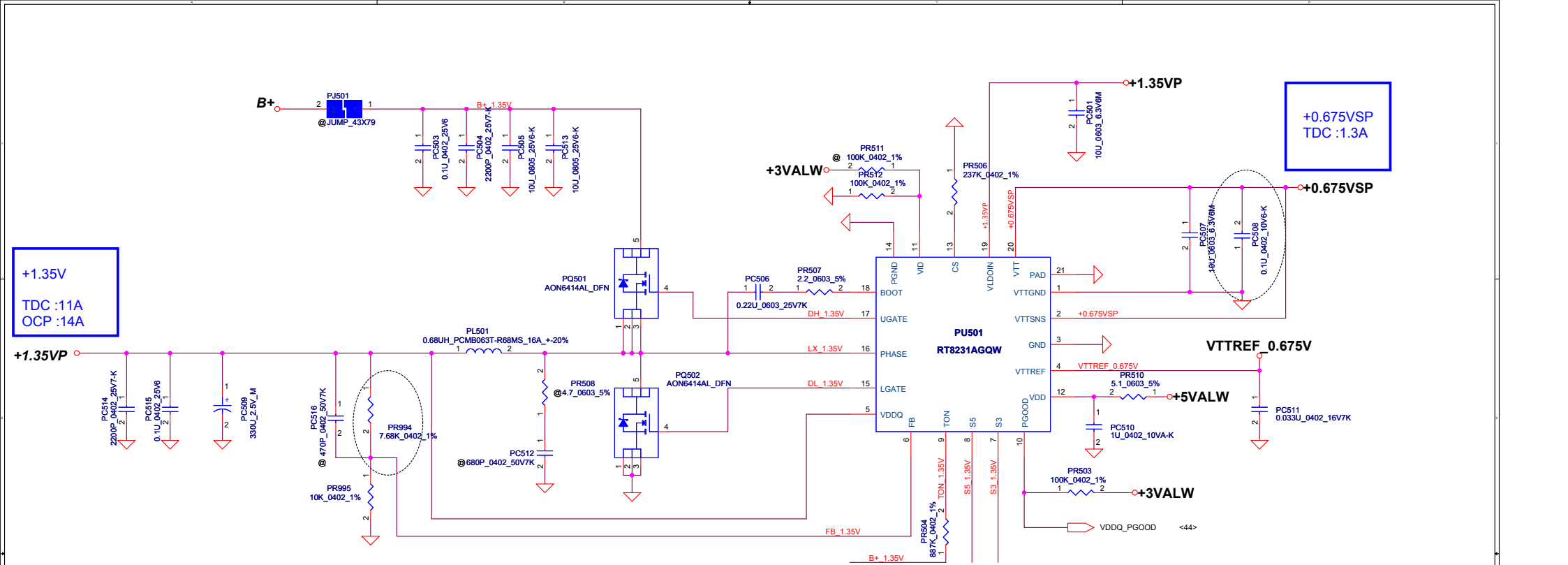
Modified for B+ voltage step

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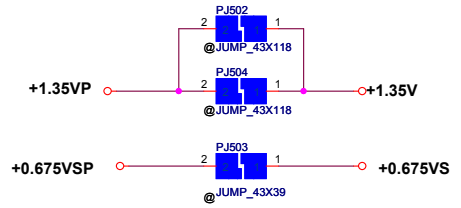
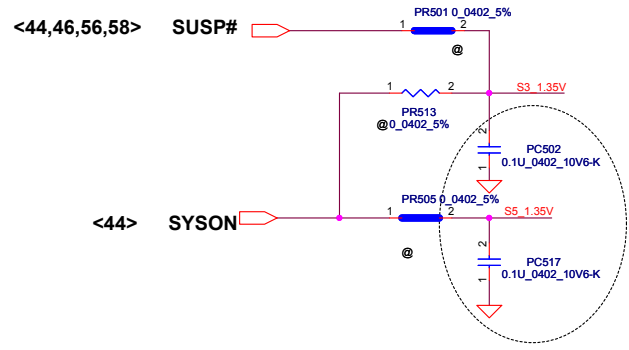
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+1.35V  
TDC :11A  
OCP :14A

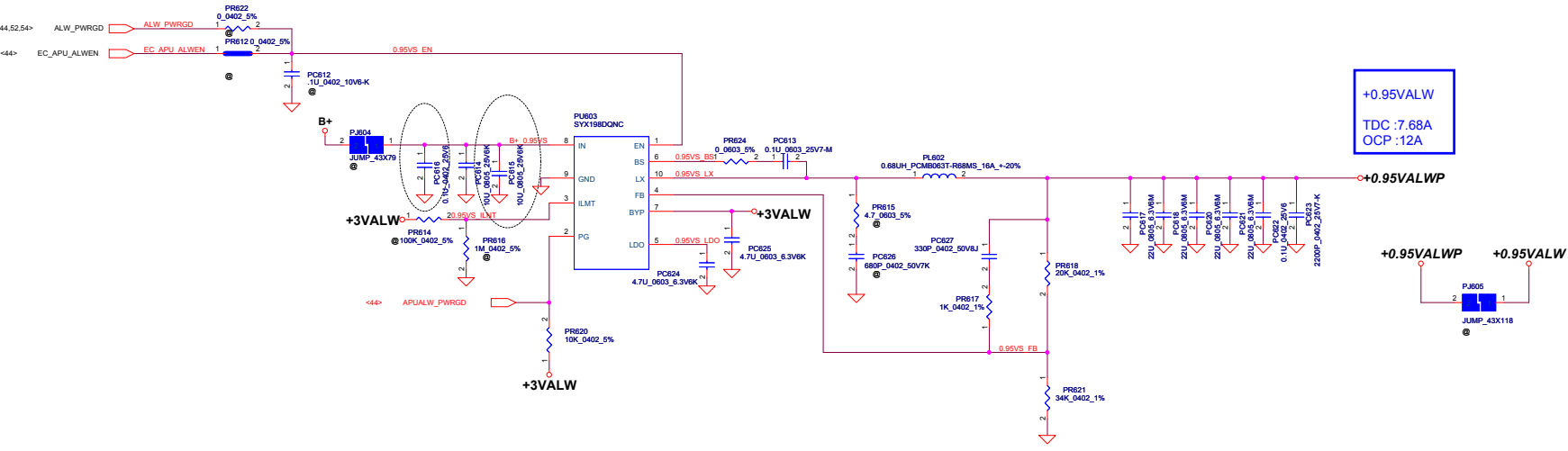
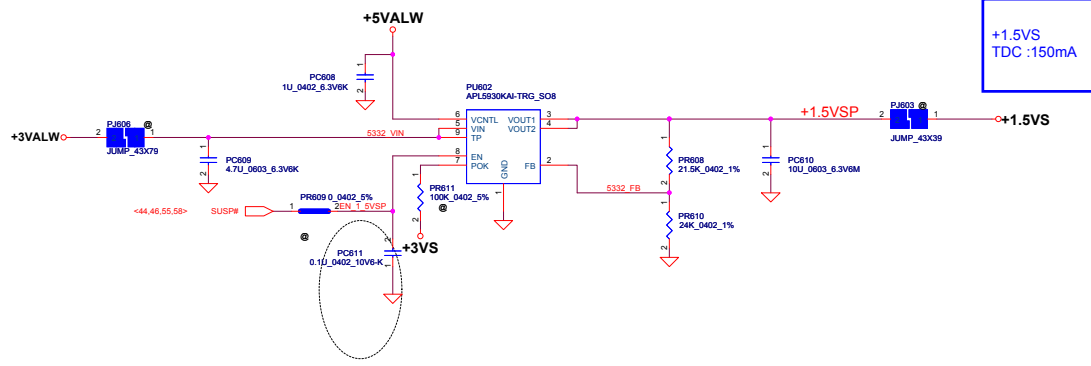
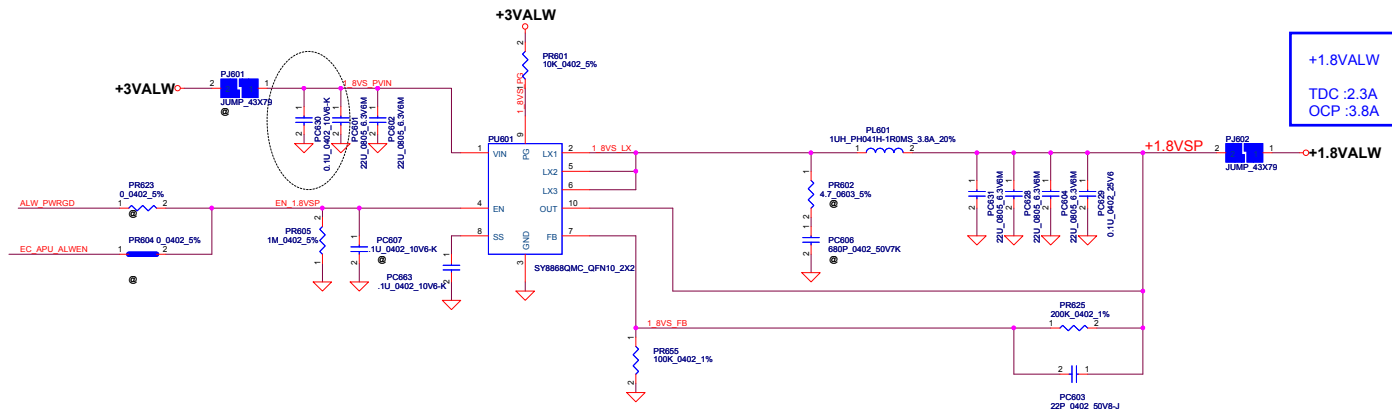
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TDC :1.3A



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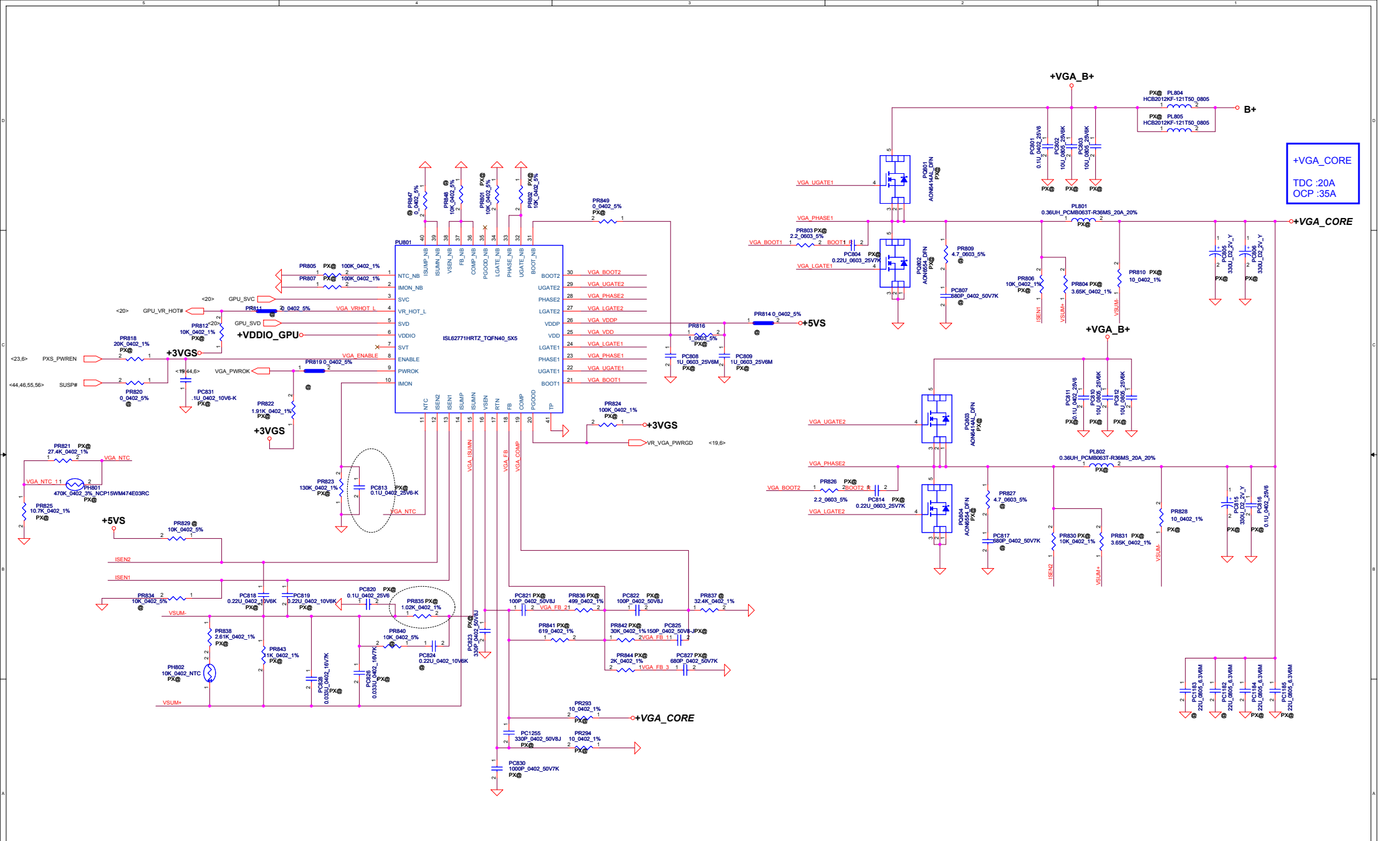








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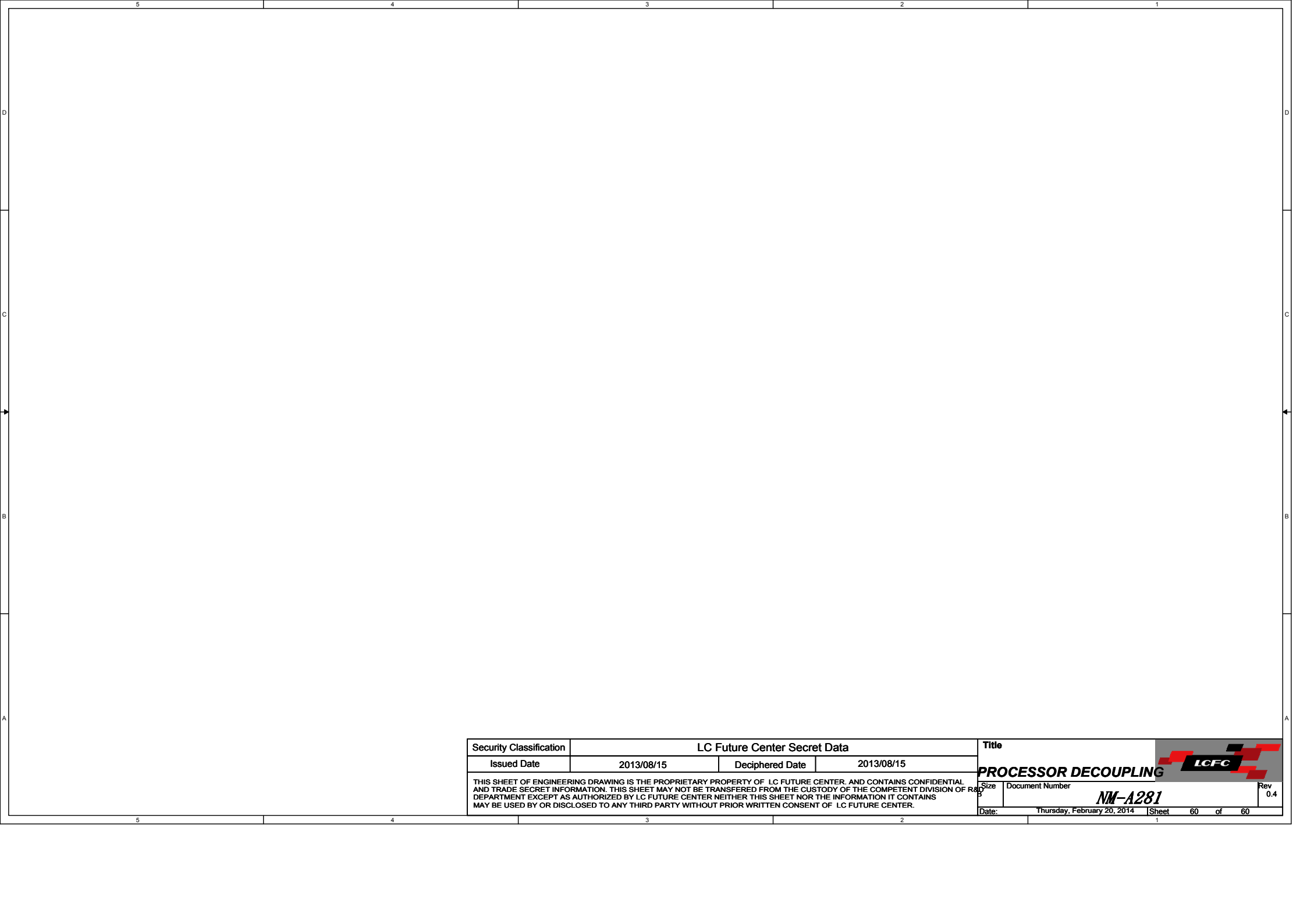



**+VGA\_CORE**  
TDC:20A  
OCP:35A

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