

QUANTA COMPUTER

CPU HT/CONTROL(1/3)

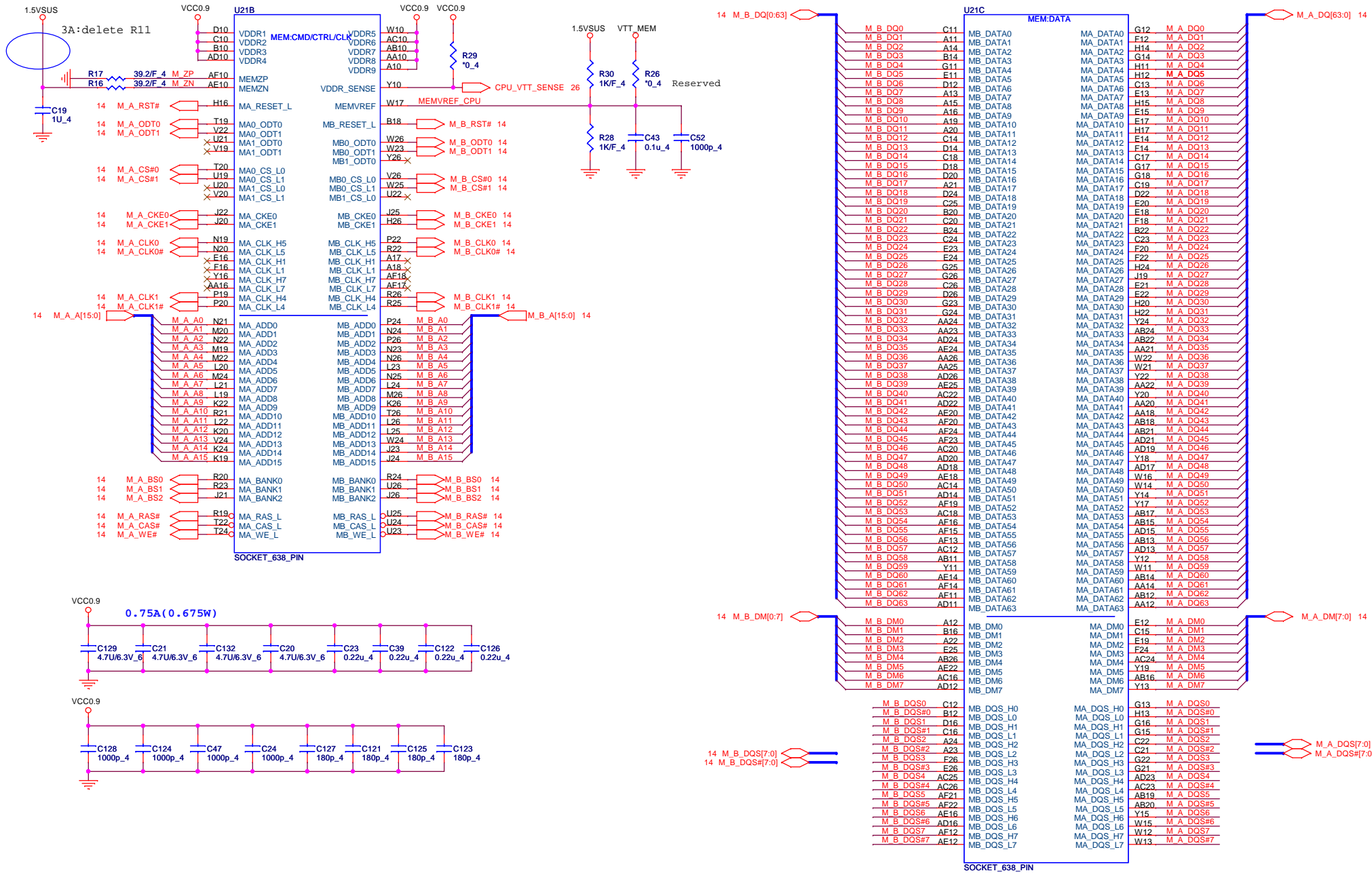
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Size: Custom | Document Number: AMD | Rev: 3A
 Date: Saturday, March 20, 2010 | Sheet: 3 of 34

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

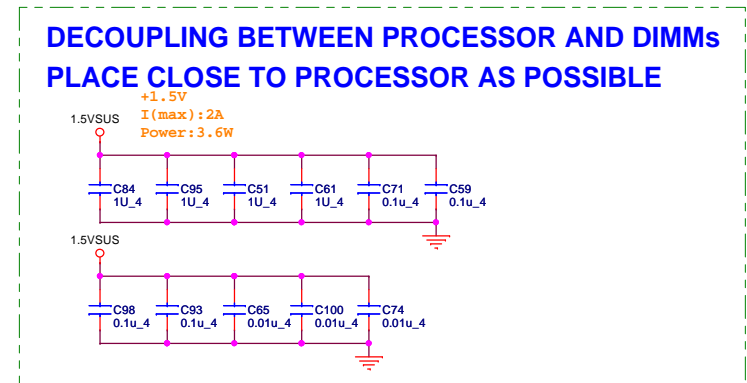
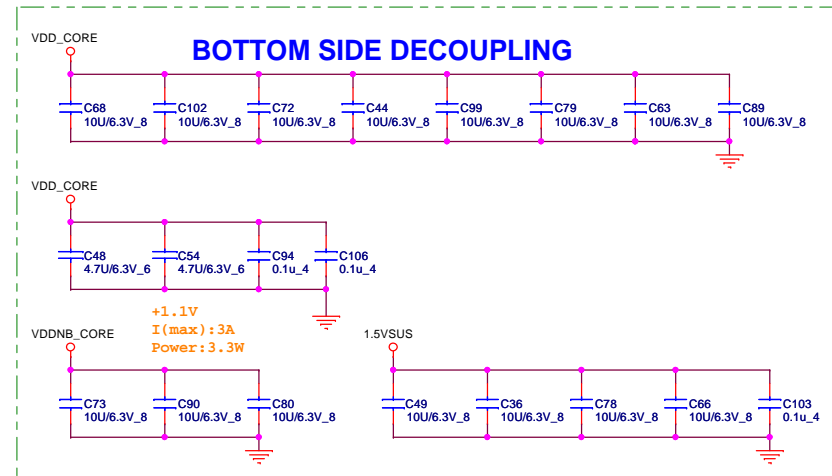
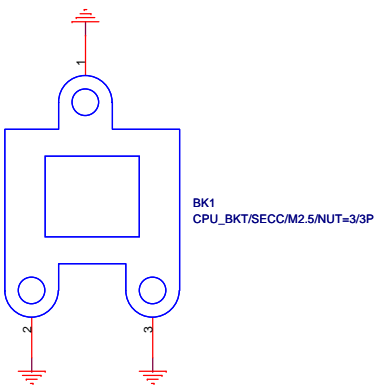
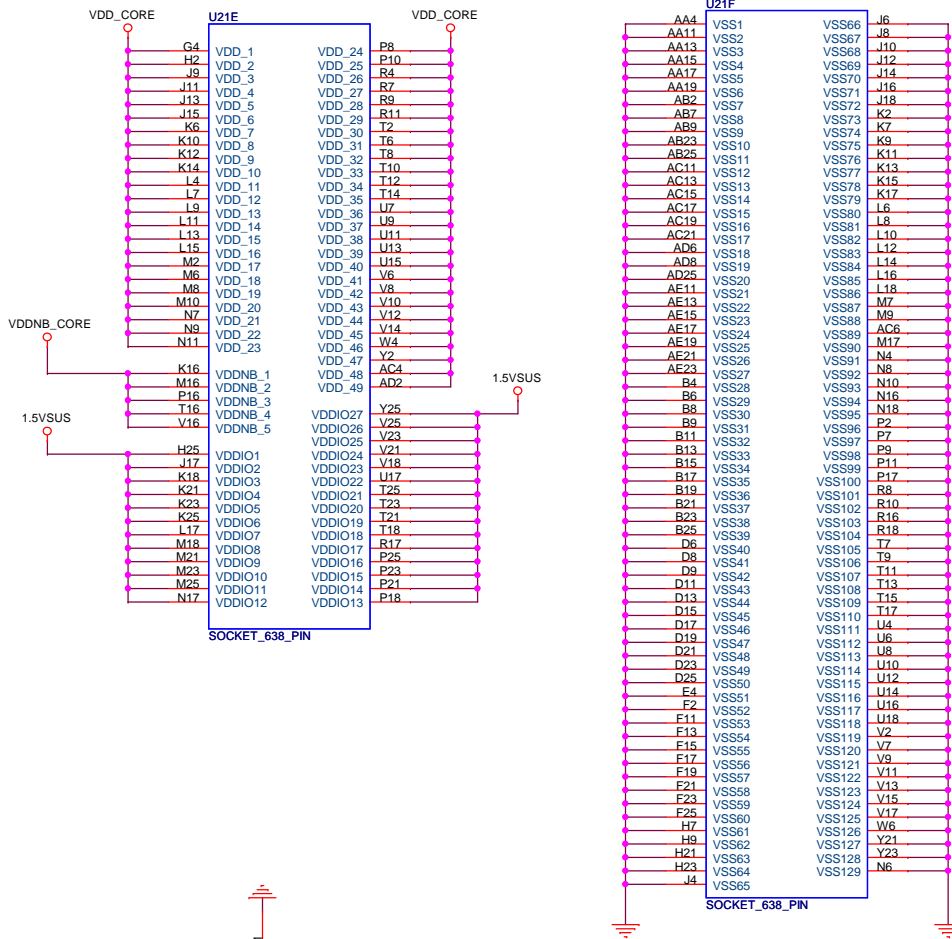
CPU_VDDR : 35W->0.9V
45W->1.05V

Processor Memory Interface

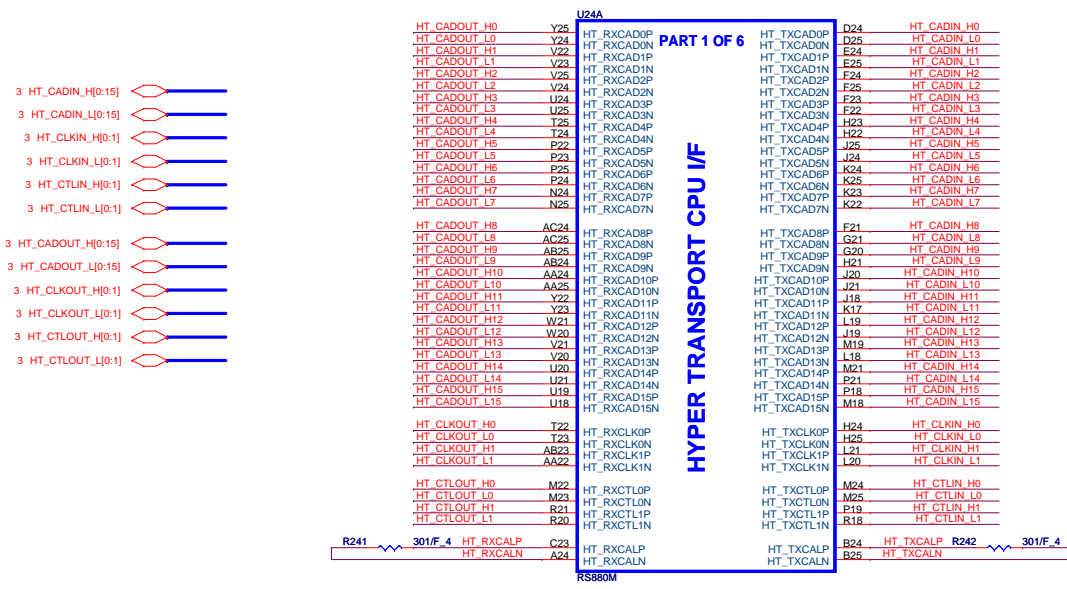


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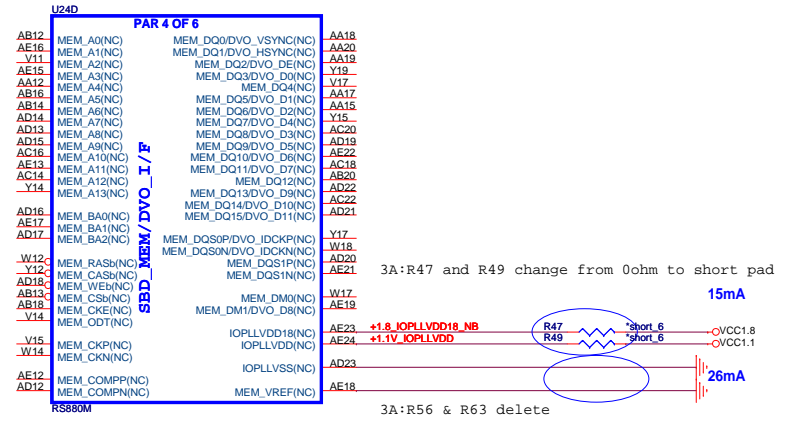
Socket Type	QCI P/N
Normal	DG0^8000018
90 degree	DG0^8000023



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This block is for UMA RS880M only , RX881 can remove all component



QUANTA COMPUTER

File: **RS880M HT/SPMEM(1/4)**

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Rev 3A

1. Level 1 Environment-related Substances should NEVER be Used.
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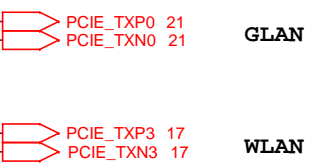
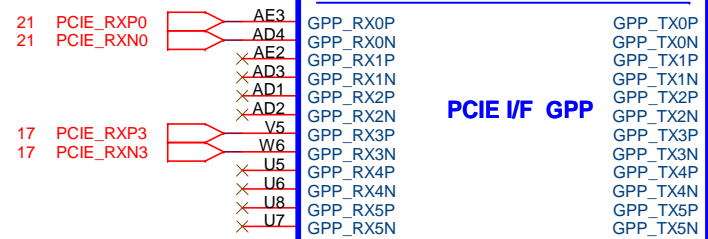
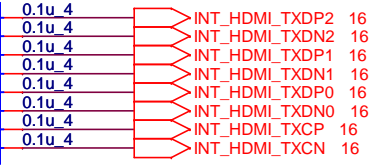
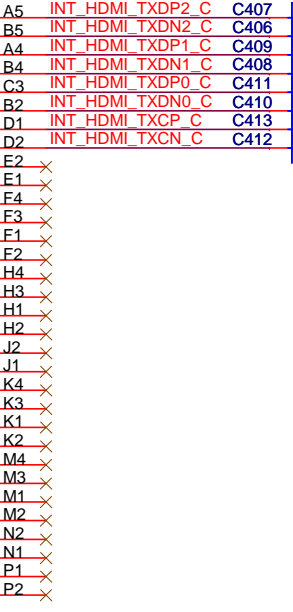
U24B

PART 2 OF 6

PCIE I/F GFX

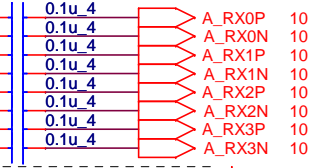
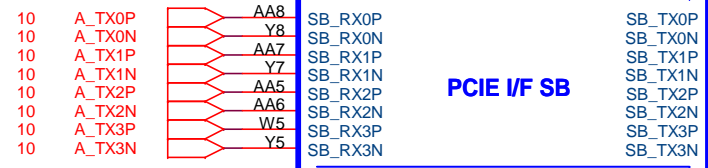
PCIE I/F GPP

PCIE I/F SB

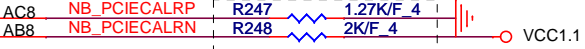


GLAN

WLAN



PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)



Close NB within 1"

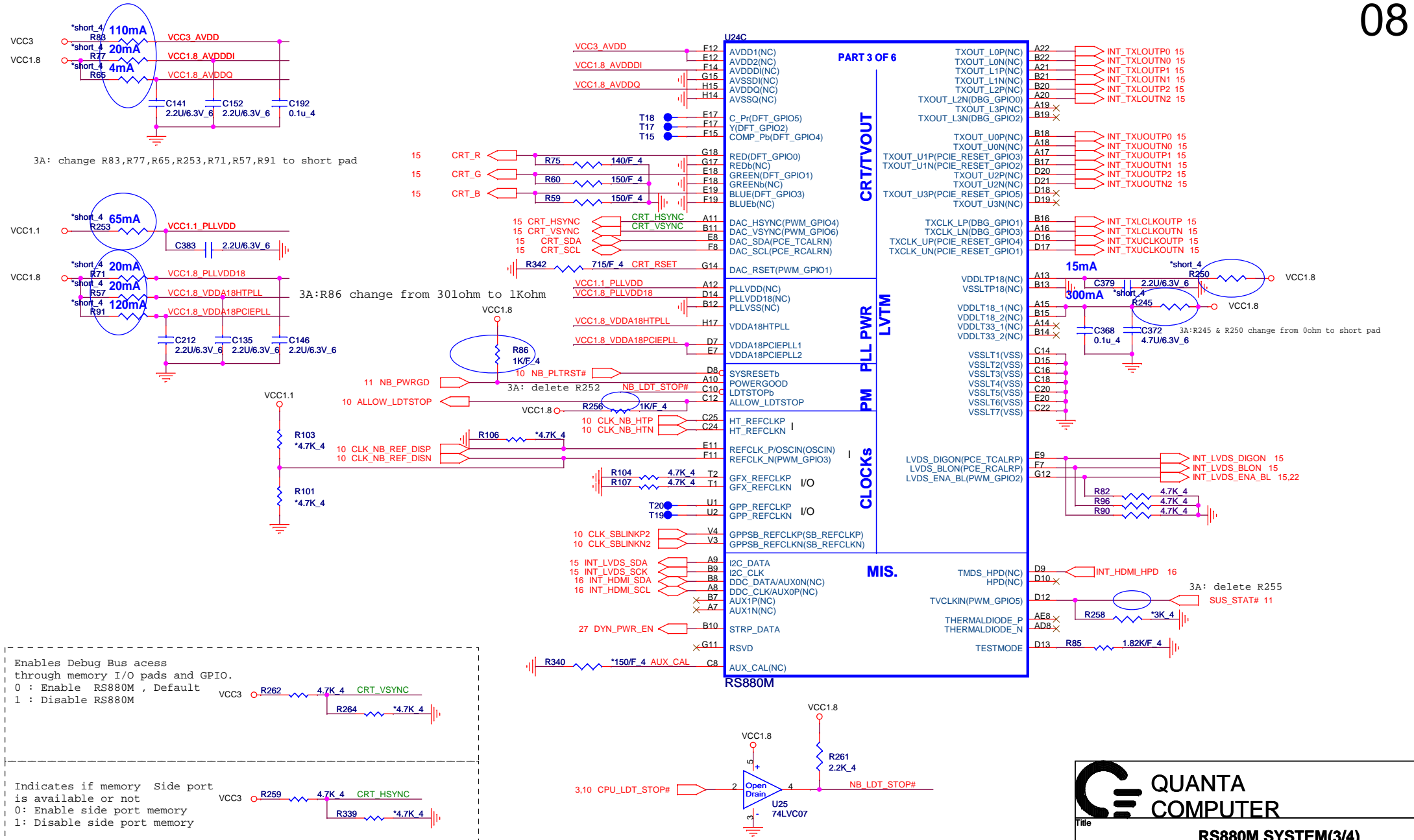
VCC1.1

RS880M



Title			RS880M GFX/PCIE(2/4)		
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1.Level 1 Environment-related Substances Should NEVER be Used.
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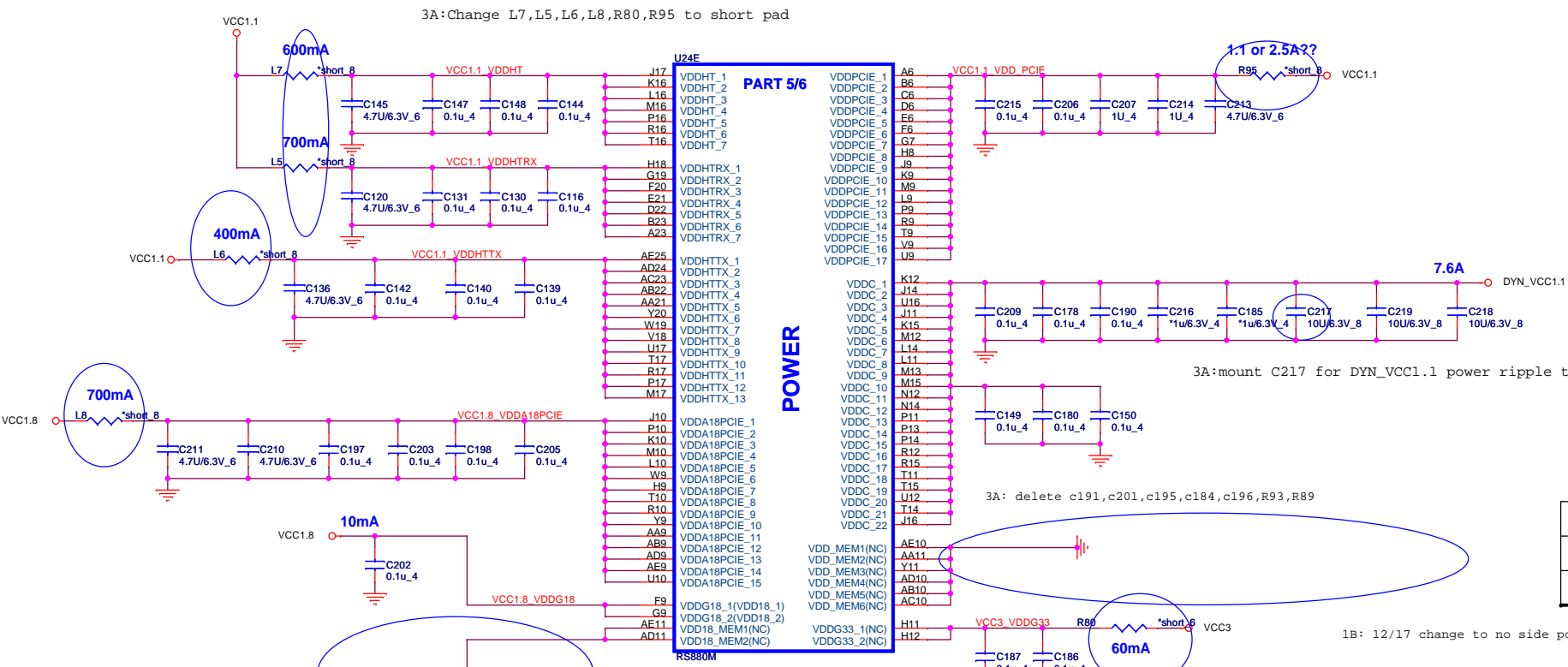
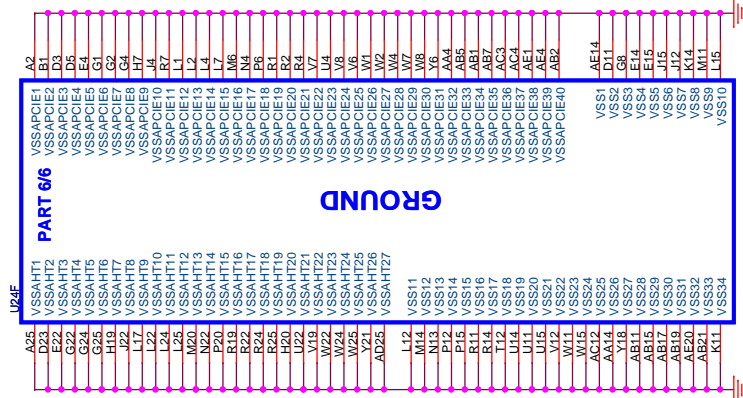


QUANTA COMPUTER

Title: **RS880M SYSTEM(3/4)**

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	AMD	

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3A: Change L7, L5, L6, L8, R80, R95 to short pad

1.1 or 2.5A??

3A: mount C217 for DYN_VCC1.1 power ripple too large

3A: delete c191, c201, c195, c184, c196, r93, r89

1B: 12/17 change to no side port setting

VDD18_MEM	
Side-Port	VCC1.8
No Side-Port	GND

1B: 12/17 change to no side port setting

3A: delete R251, R249, C377

	VDD_MEM
Side-Port	VCC1.5
No Side-Port	GND

QUANTA COMPUTER

Title: **RS880M POWER(4/4)**

Size: Custom	Document Number: AMD	Rev: 3A
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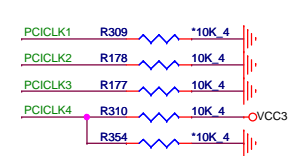
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Strap Table

1221,AMD suggest R309 unimpunt

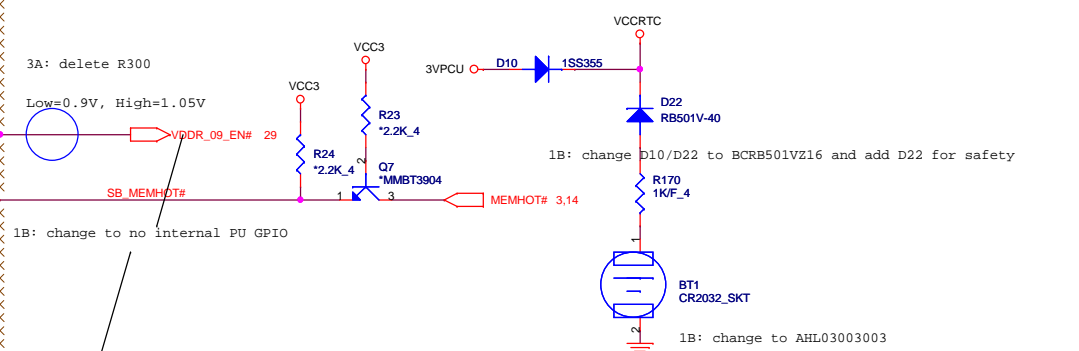
PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4
ALLOW PCIe Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE
FORCE PCIe Gen1	Watchdog Timer Disable	IGNORE DEBUG STRAPS	Fusion CLOCK MODE

PCI Strap

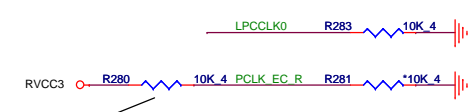


1B: delete no need PU R128/R161/R272/R155, add R354 for optional

RTC

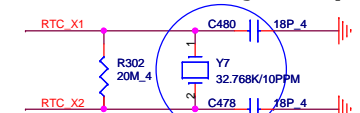


LPCLK0	LPCLK1
H=Enable embedded EC	H=Enable Internal CLK Gen.
L=Disable embedded EC	L=Disable Internal CLK Gen.



1B: change to INT CLK Gen.

3A: 1/22 change Y7 P/N(BG332768909) and C478=18PF for timing accuracy

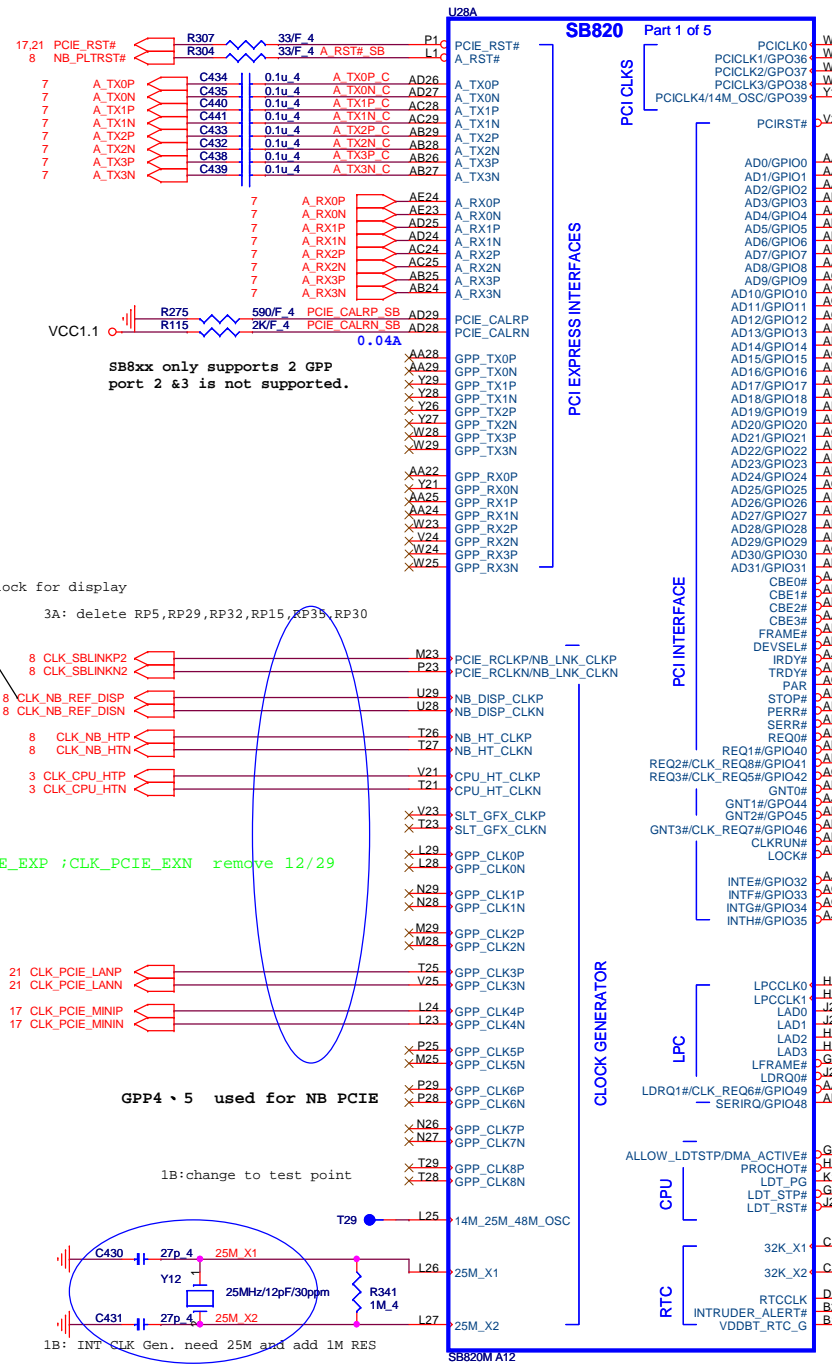


QUANTA COMPUTER

Title: **SB8X0 PCI/CLK/LPC(1/4)**

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1B: modify INT clock for display
3A: delete RP5,RP29,RP32,RP15,RP35,RP30

CLK_PCIE_EXP ;CLK_PCIE_EXN remove 12/29

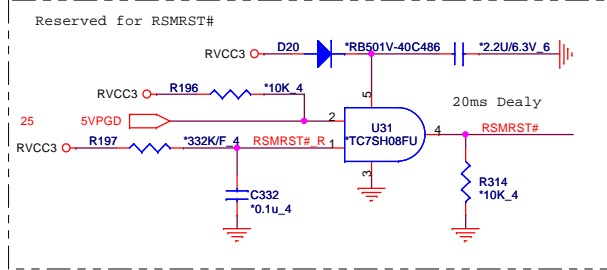
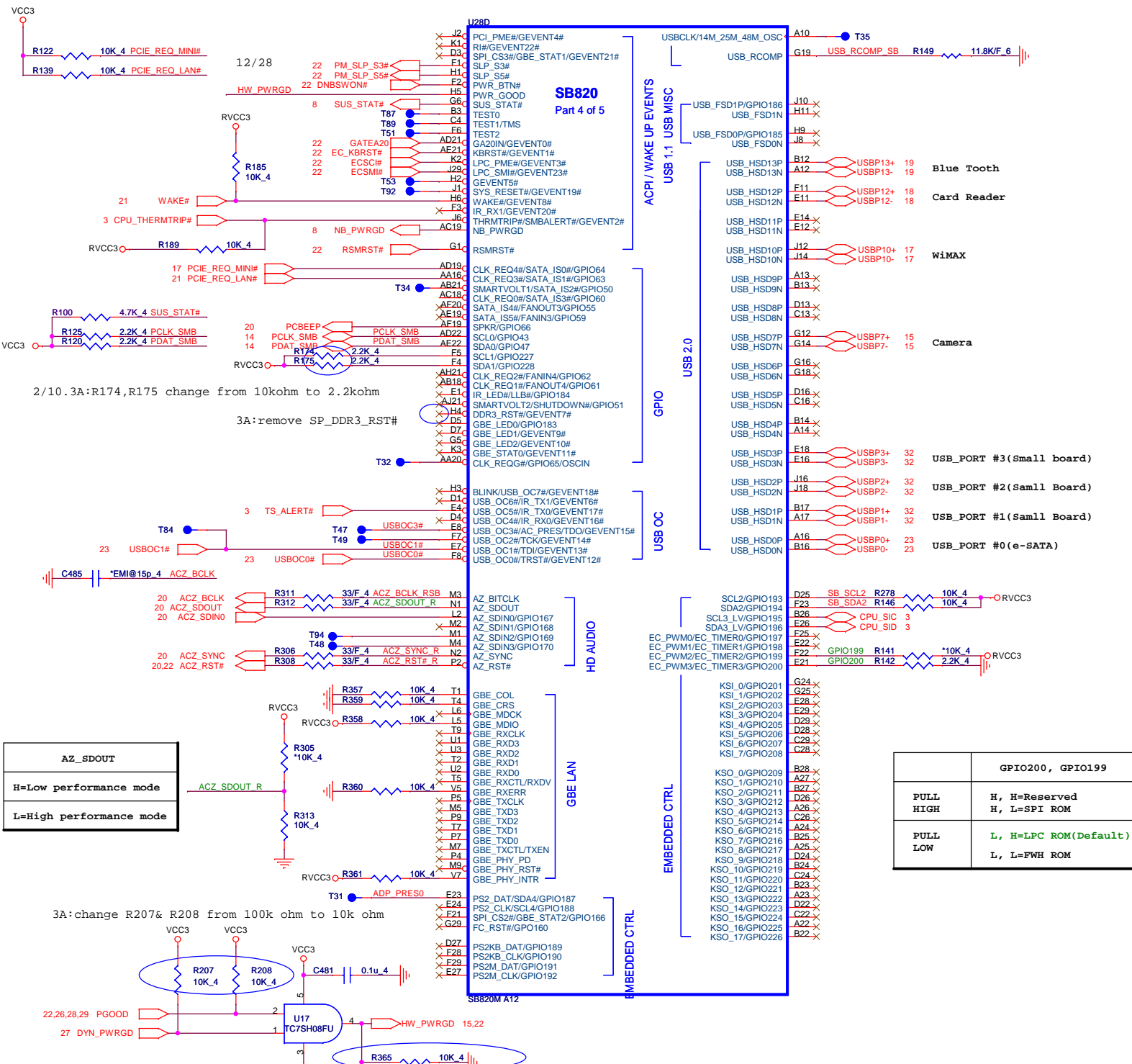
GPP4 * 5 used for NB PCIE

1B: change to test point

1B: INT CLK Gen. need 25M and add 1M RES

3A: 1/22 change Y12 P/N: BG625000486 and C430=C431 27PF for timing accuracy

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3A Remove Panel ID 3A :delete RP27,SW1,RP25

GPIO200, GPIO199	
PULL HIGH	H, H=Reserved H, L=SPI ROM
PULL LOW	L, H=LPC ROM(Default) L, L=FWH ROM

AZ_SDOUT	
H=Low performance mode	
L=High performance mode	

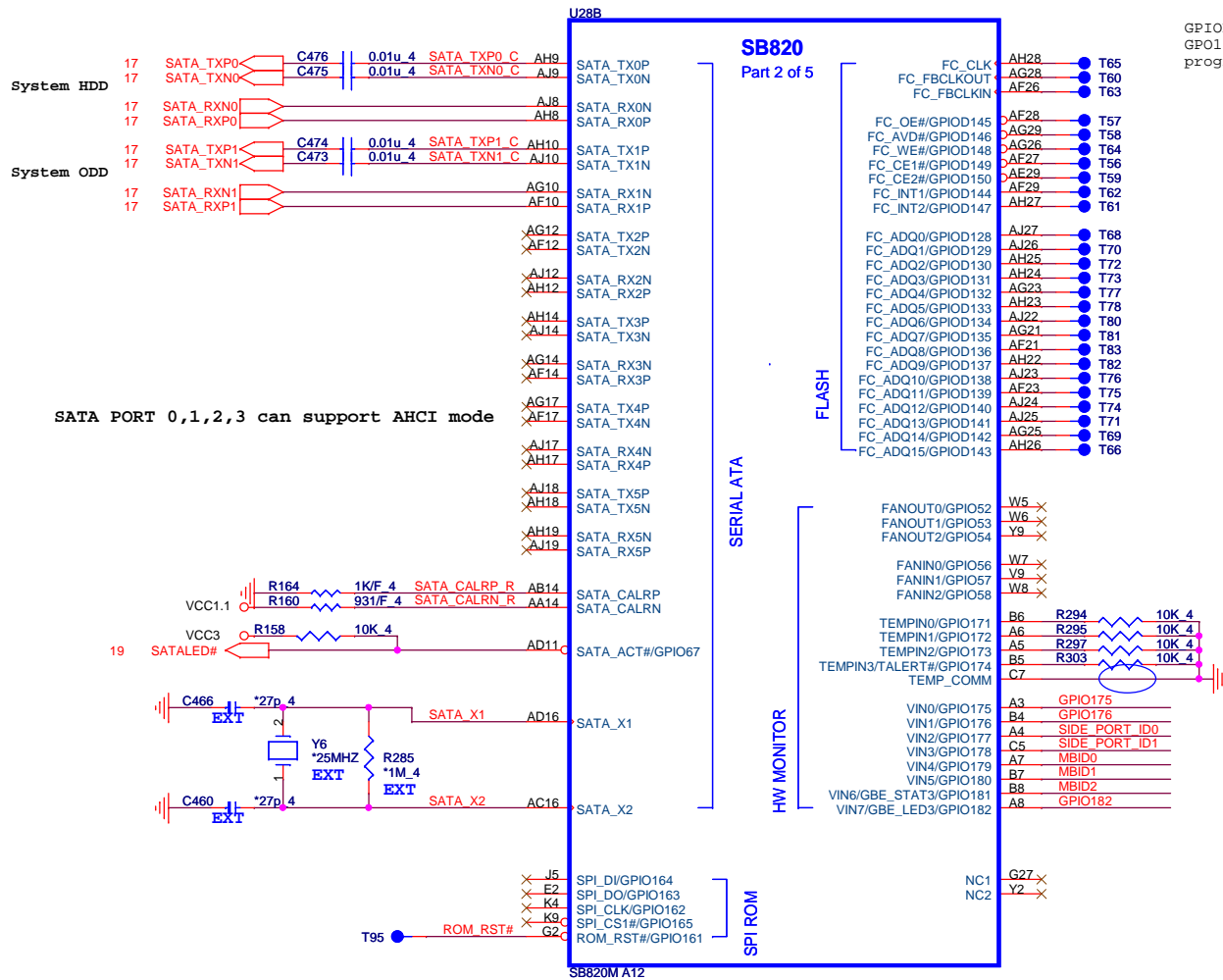
1.Level 1 Environment-related Substances should NEVER be Used.
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QUANTA COMPUTER

Title: **SB8X0 AUDIO/USB(3/4)**

Size: Custom Document Number: AMD Rev: 3A

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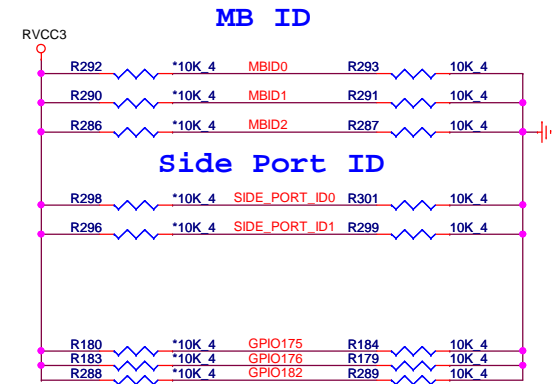


GPIO[150:128] are open drain GPIO pins where as GPIO160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

ID2	ID1	ID0	
0	0	0	Danube UMA
0	0	1	Danube UMA+Side port
0	1	0	Danube+Park XT
0	1	1	Danube+Madison LP
1	0	0	Danube+M92 XTX
1	0	1	
1	1	0	
1	1	1	

	NON	SAMSUNG	HYNIX	
SP ID0	0	1	0	1
SP ID1	0	0	1	1

3A:delete R176



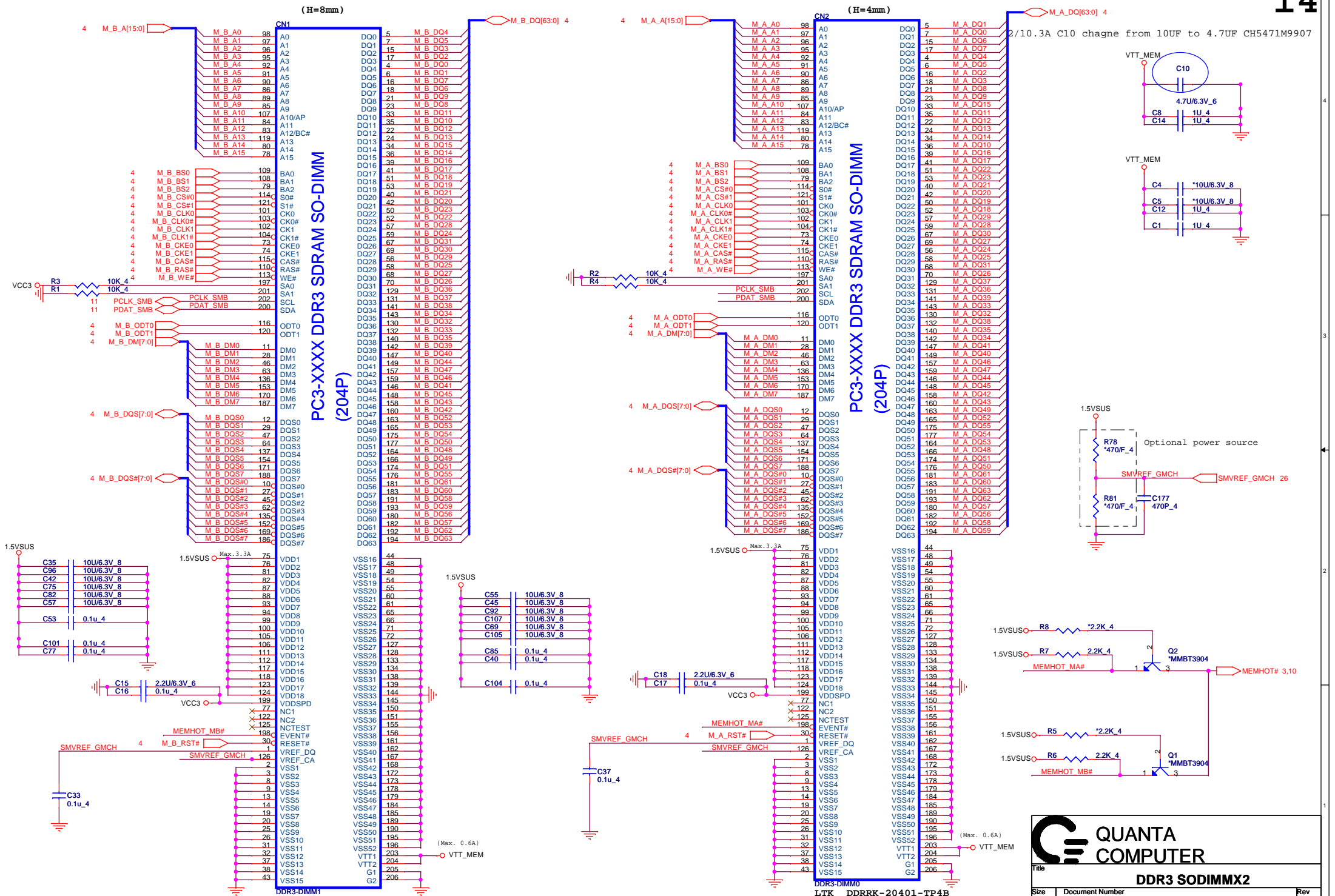
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QUANTA COMPUTER

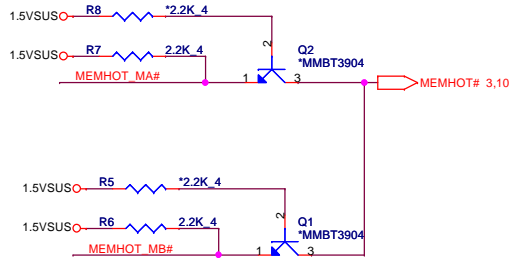
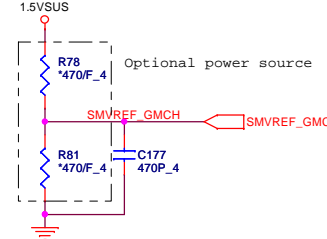
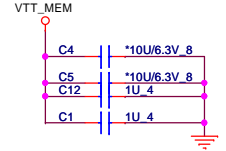
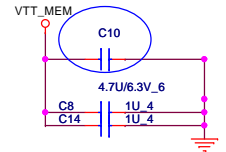
Title: **SB8X0 SATA(2/4)**

Size B Document Number: **AMD** Rev 3A

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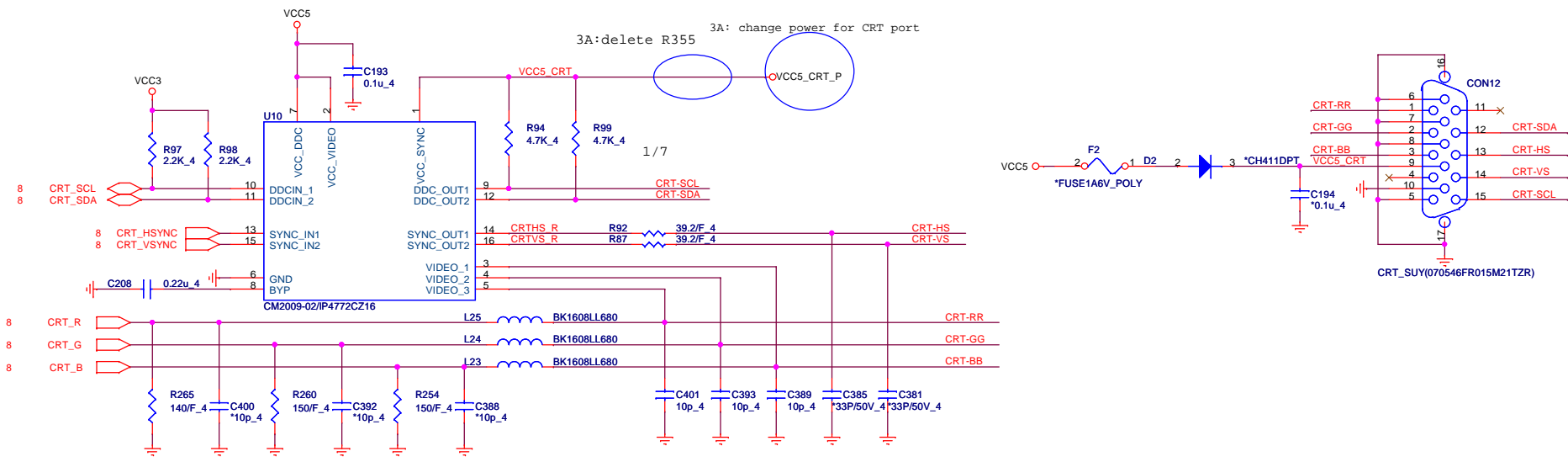


2/10.3A C10 change from 10UF to 4.7UF CH5471M9907

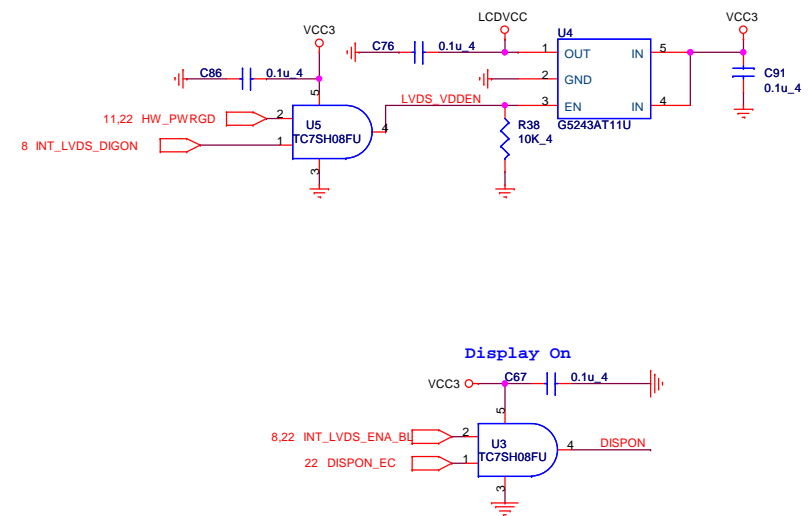
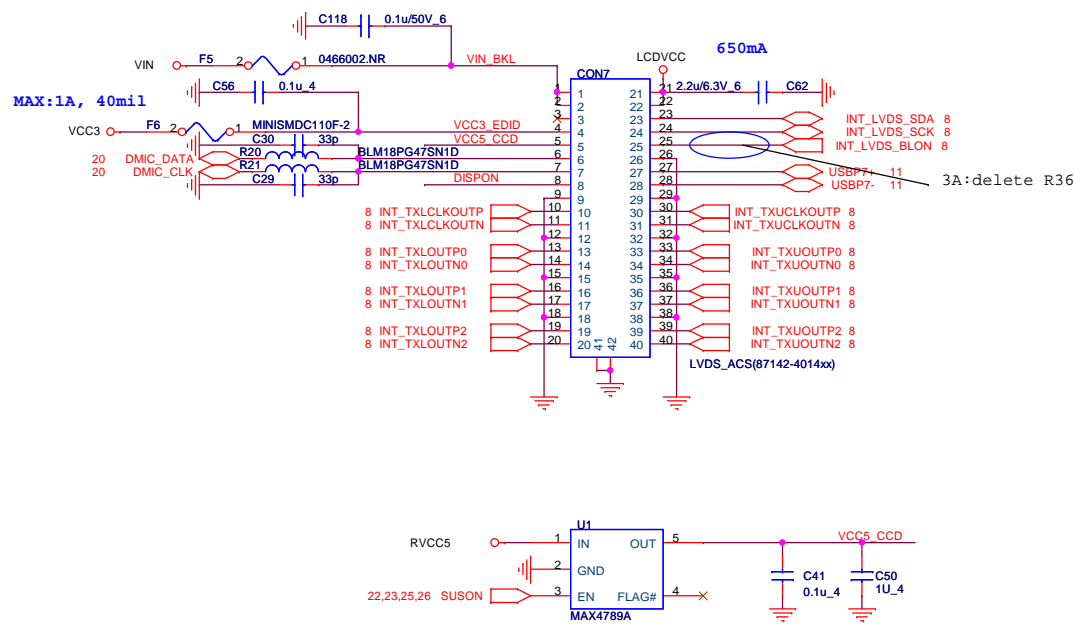


Title			DDR3 SODIMMX2		
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LVDS



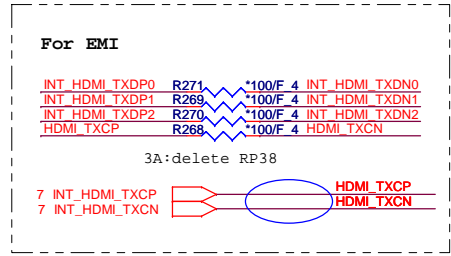
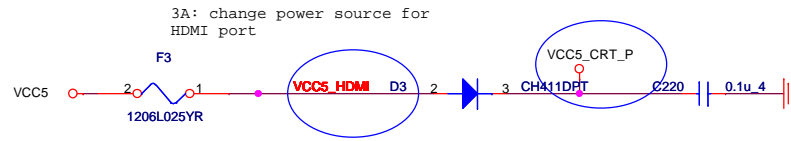
QUANTA COMPUTER

Title: **CRT/LVDS**

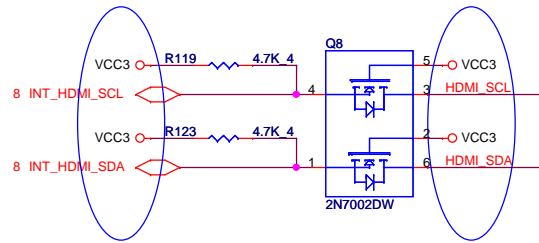
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1.Level 1 Environment-related Substances Should NEVER be Used.
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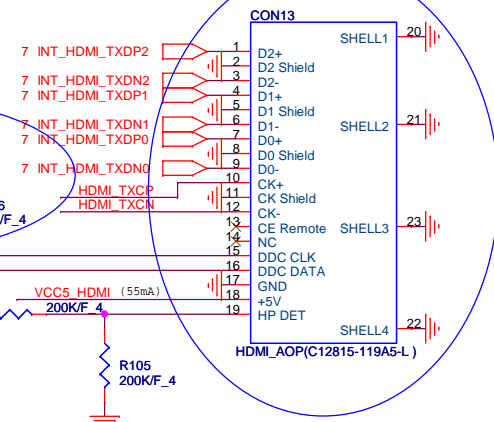
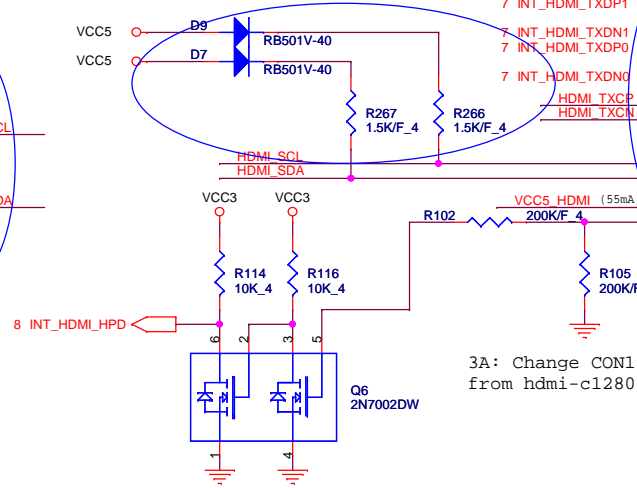
3A: change power source for CRT port



3A : VCC5 -> VCC3

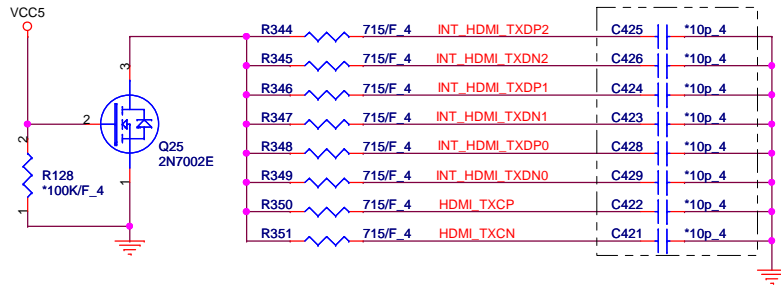


3A:Prevent incorrect voltage level



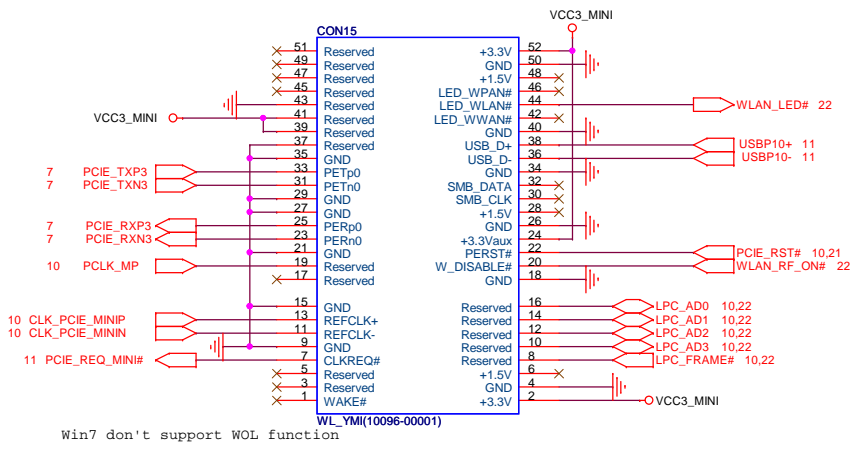
3A: Change CON13 footprint:
from hdmi-c12806-11908-1-19p-v to Hdmi-c12825-11908-1-19p-v

For ESD



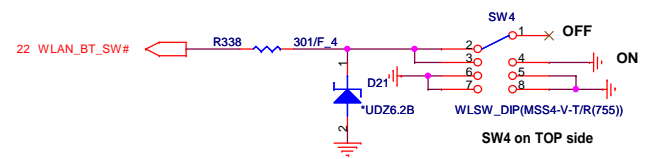
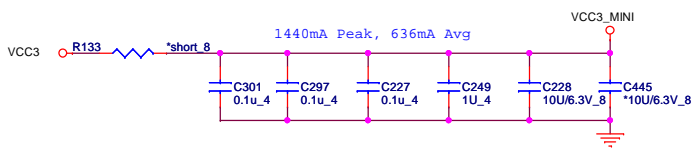
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		QUANTA COMPUTER
Title HDMI		
Size B	Document Number AMD	Rev 3A
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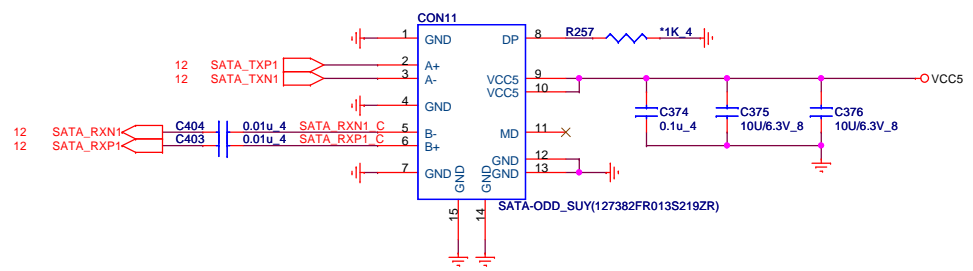


Win7 don't support WOL function

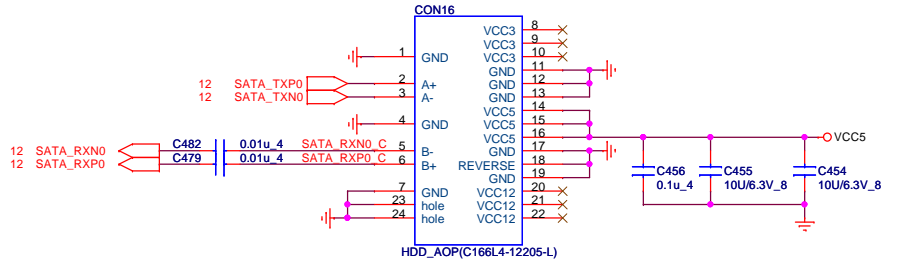
WLAN_BT_S/W



SATA ODD



SATA HDD



QUANTA COMPUTER

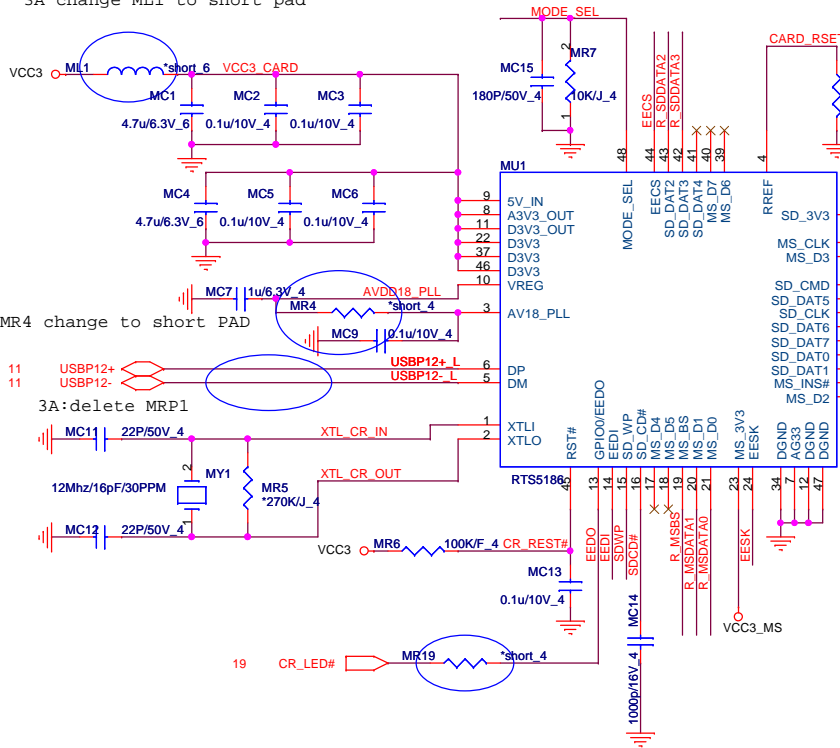
Title: **WLAN/HDD/ODD**

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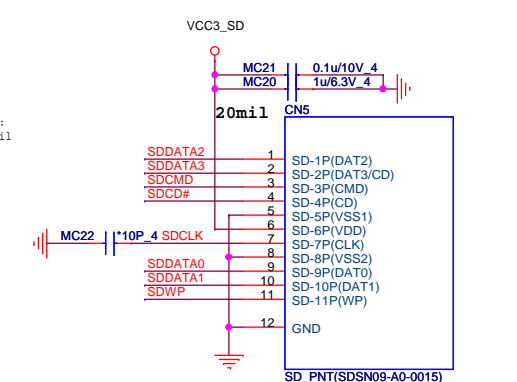
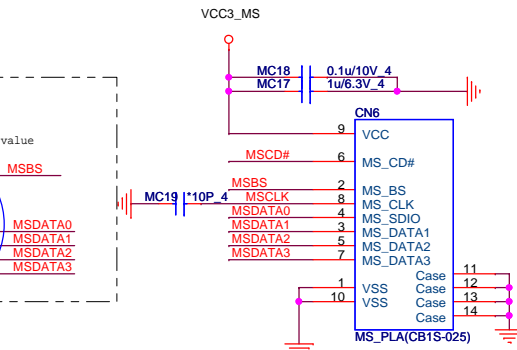
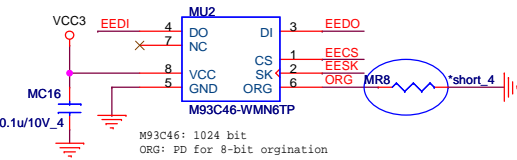
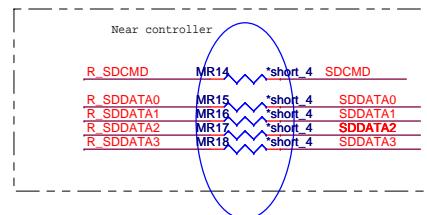
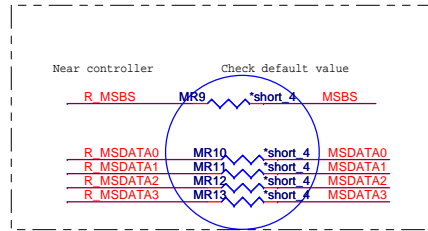
3A:Change MR19,MR3,MR2,MR9,MR10,MR11,MR12,MR13,MR14,MR15,MR16,MR17,MR18,MR8 to short pad

3A change ML1 to short pad



3A:MR4 change to short PAD

3A:delete MRP1



QUANTA COMPUTER

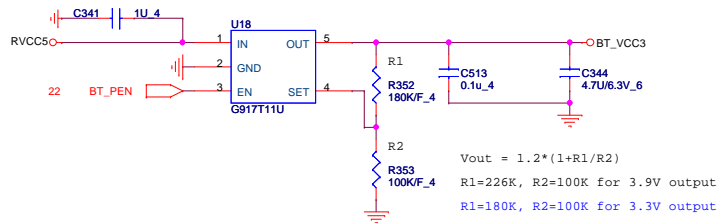
Title: **CARD READER(RTS5186)**

Size: Custom Document Number: **AMD** Rev: 3A

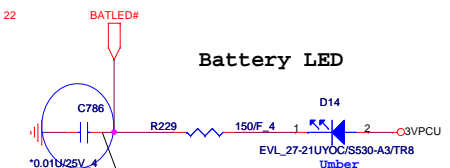
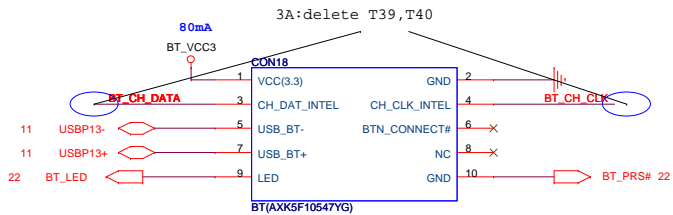
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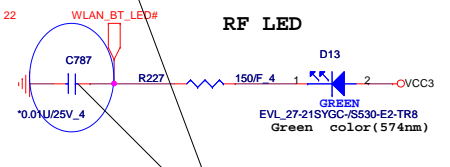
Bluetooth



$V_{out} = 1.2 * (1 + R1/R2)$
 R1=226K, R2=100K for 3.9V output
 R1=180K, R2=100K for 3.3V output



Battery LED

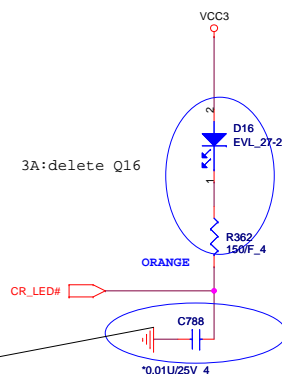


RF LED

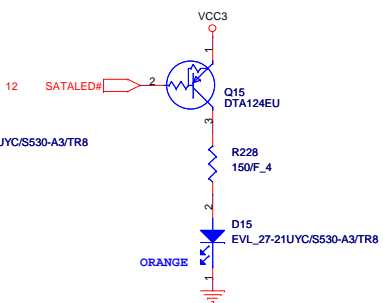
3A : Reverse C786, C787, C788 FP for ESD

Two Color :
 everlight : 19-22UYOSYGC (BEAG0028ZA0_
 liteon : LTST-C195KGFKT (BEAG0032ZA0)
 Amber :
 everlight : 19-21UYOC/S530-A6/TR8 (BEAB0015Z06)
 liteon : LTST-C190KFKT (BEAB0006Z07)
 Green :
 everlight : 19-21SYGC/S530-E2/TR8 (BEYG0053ZA2)
 liteon : LTST-C190KFKT (BEGR0080Z07)
 Yellow :
 everlight : 19-21UYC/S530-A2/TR8 (BEYL0016Z08)
 liteon : LTST-C190KSKT (BEYL0024Z01)

CR LED



HDD LED



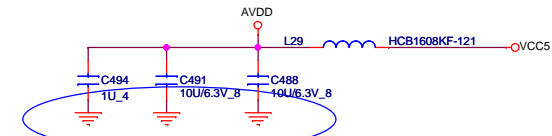
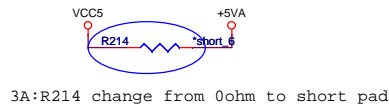
QUANTA COMPUTER

Title: **Express Card/LED/BT**

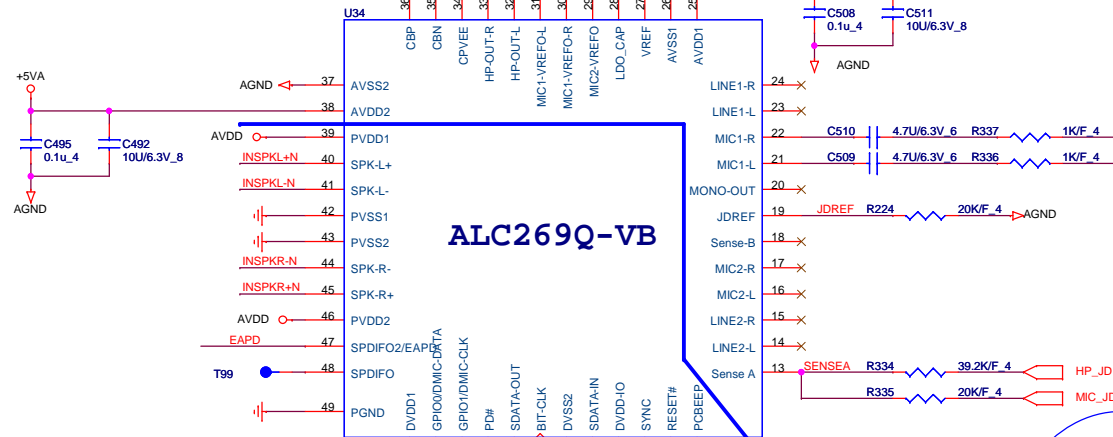
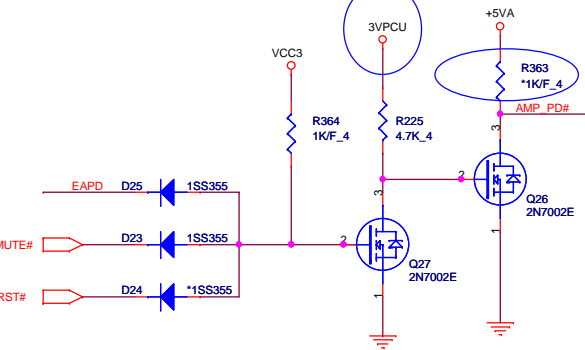
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1.Level 1 Environment-related Substances should NEVER be Used.
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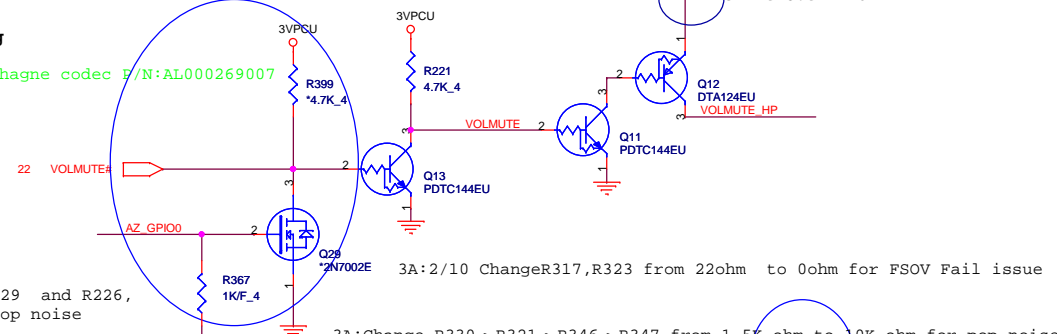
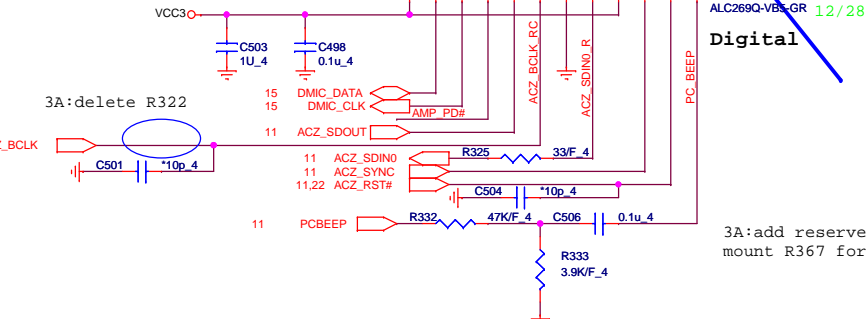


3A:Change from +5VA to 3VPCU
3A:R363 unmount

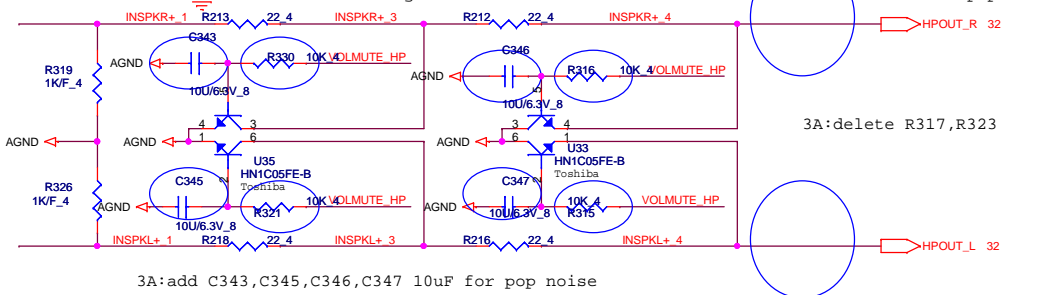
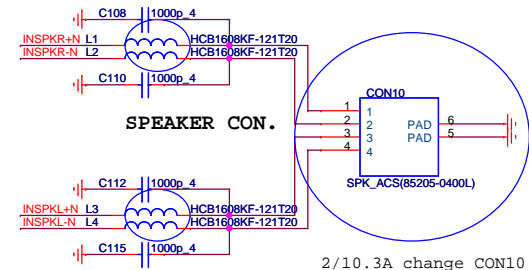
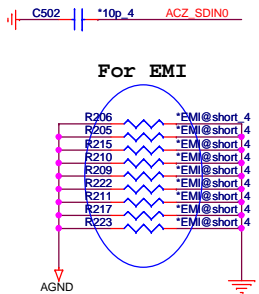


Analog
ALC269Q-VB-GR 12/28 chagne codec E/N:AL000269007

Digital



3A:Change L1-L4 to bead CX121T20100



For EMI : 12/23 add 3 pcs 0ohm
3A:R206, R205, R215, R210, R209, R222, R211, R217, R223 change to short pad

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Welding resins only from the business Partners that Sony approves as Green Partners.

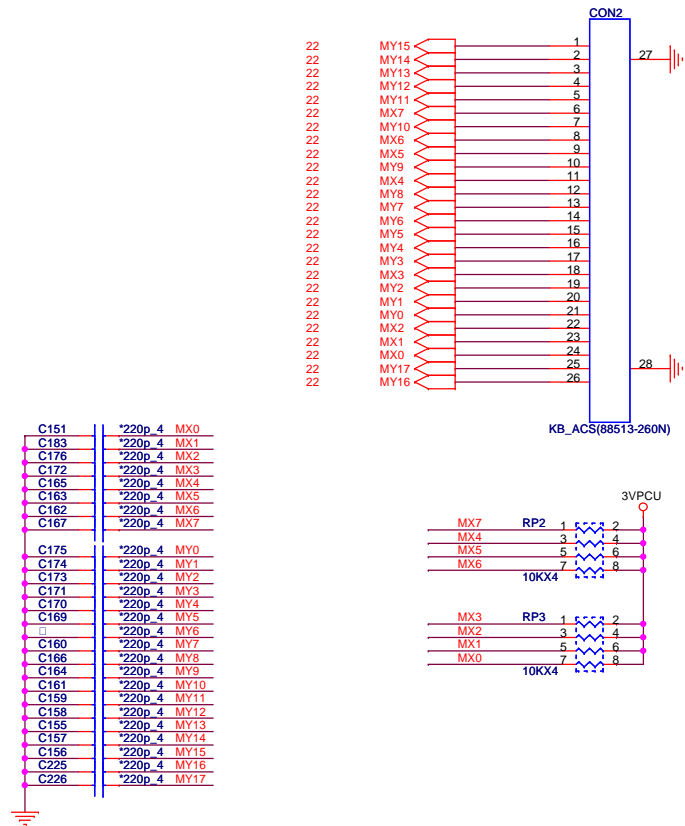
QUANTA COMPUTER

Title: **Codec ALC269Q**

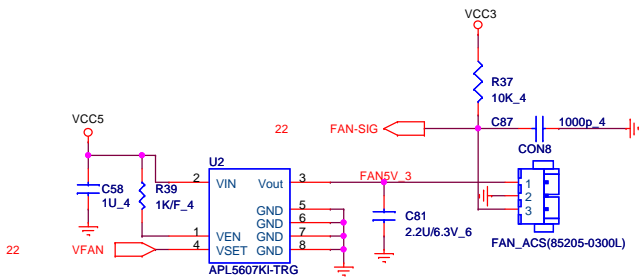
Size	Document Number	Rev
Custom	AMD	3A

Date: Saturday, March 20, 2010 Sheet 20 of 34

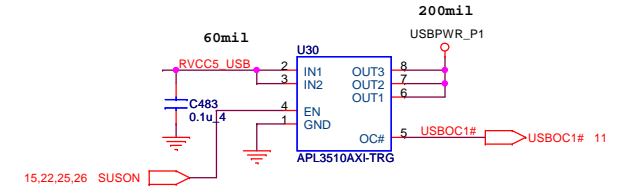
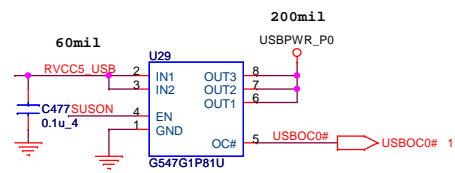
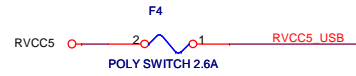
KEYBOARD



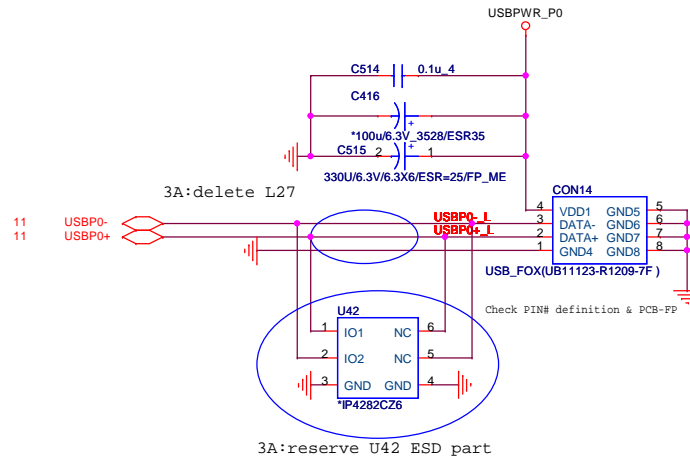
FAN



USB Port



USB Port on MB



QUANTA COMPUTER

Title **KB/USB/FAN/PS**

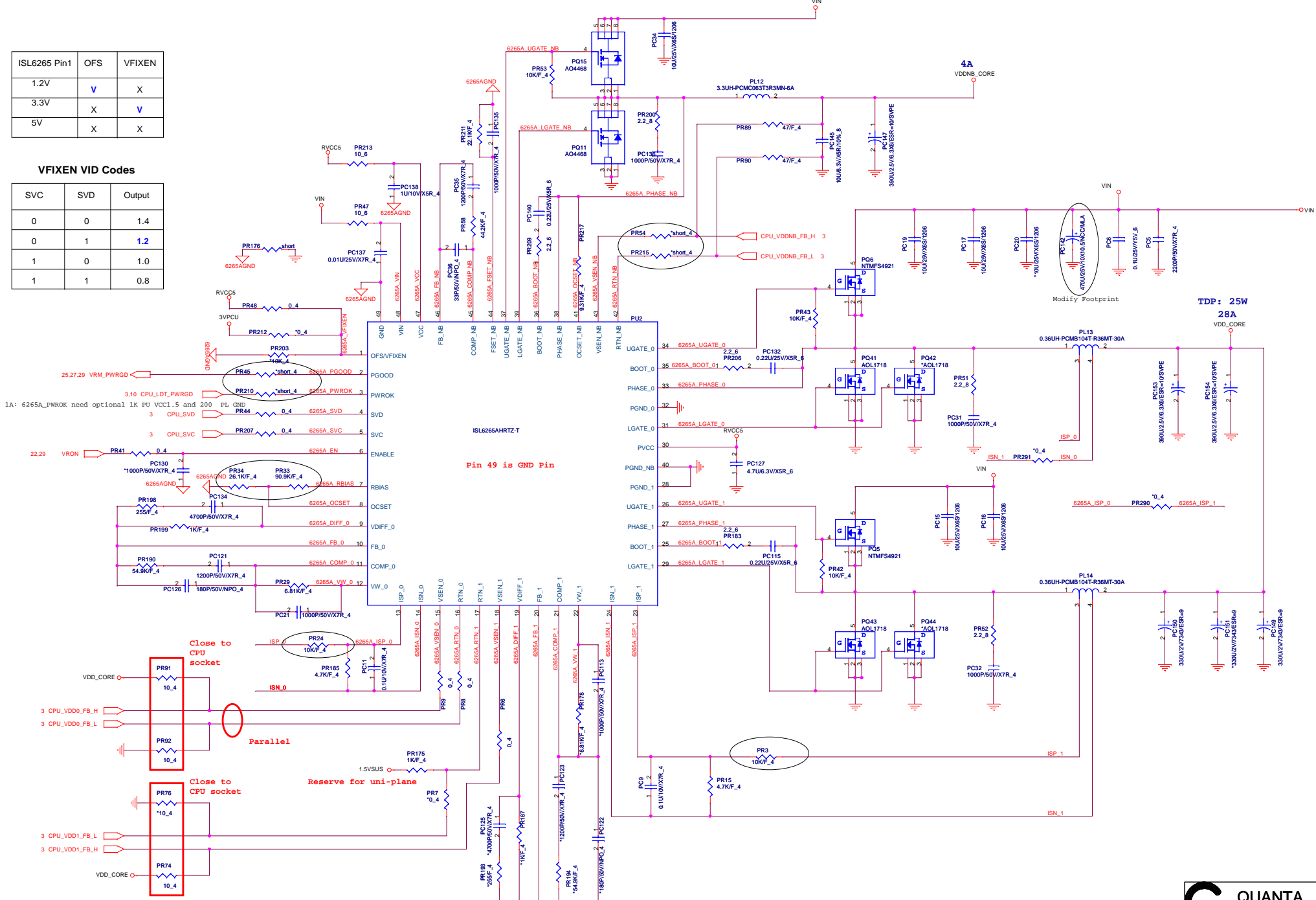
Size Custom	Document Number AMD	Rev 3A
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1.Level 1 Environment-related Substances Should NEVER be Used.
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

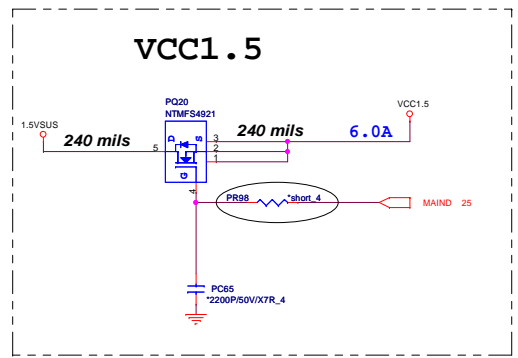
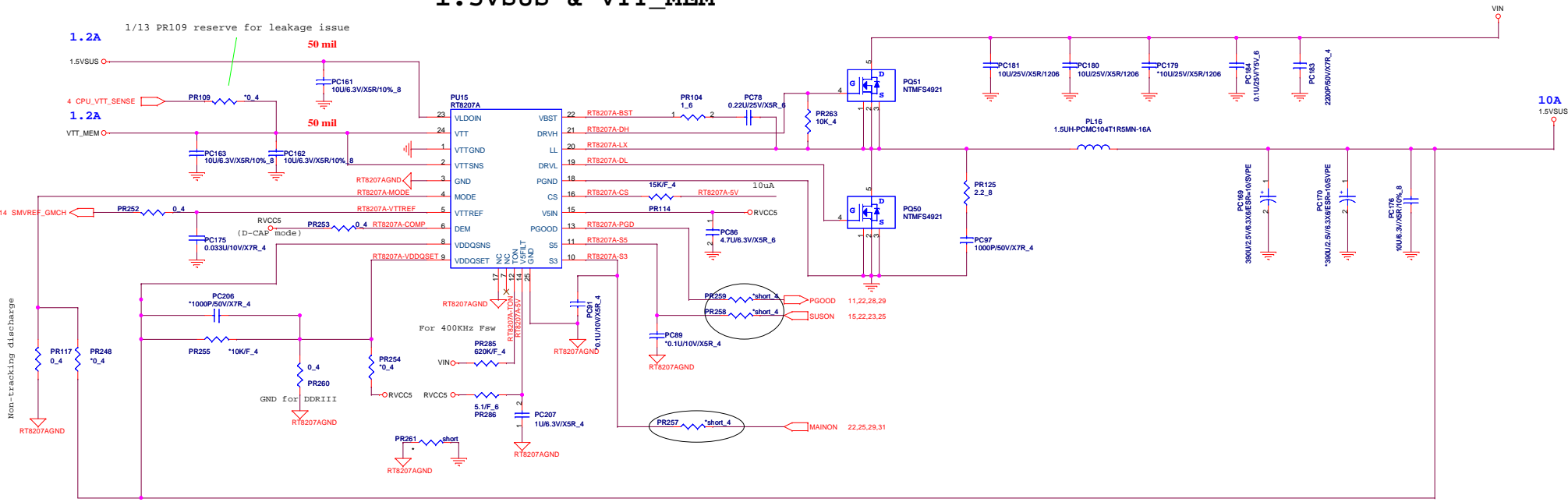


TDP: 25W
28A
VDD_CORE

QUANTA COMPUTER
VCORE(ISL6265A)
Date: Saturday, March 20, 2010 Sheet 24 of 8

1.Level 1 Environment-related Substances Should NEVER be Used.
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1.5VSUS & VTT_MEM



MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VITREF & VIT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

VIT = VITREF = VDDQSNS/2 = 0.75V

STATE	S3	S5	1.5VSUS	VITREF	VIT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

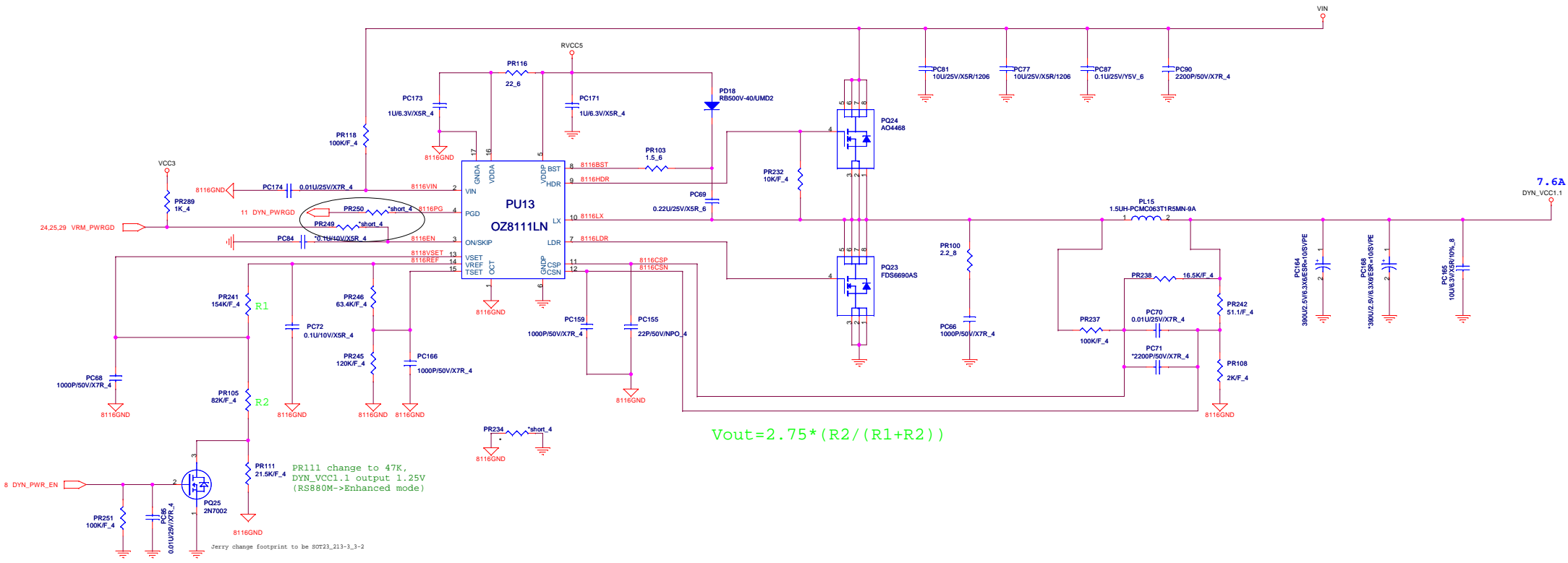
**QUANTA
COMPUTER**

File: **1.5VSUS/VTT_MEM**

Size: Custom Document Number: AMD Row: 3A

Date: Saturday, March 20, 2010 Sheet: 26 of 8

1. Level 1 Environment-related Substances Should NEVER be Used.
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DYN_PWR_EN	High	Low
DYN_VCC1.1	0.95V	1.1V

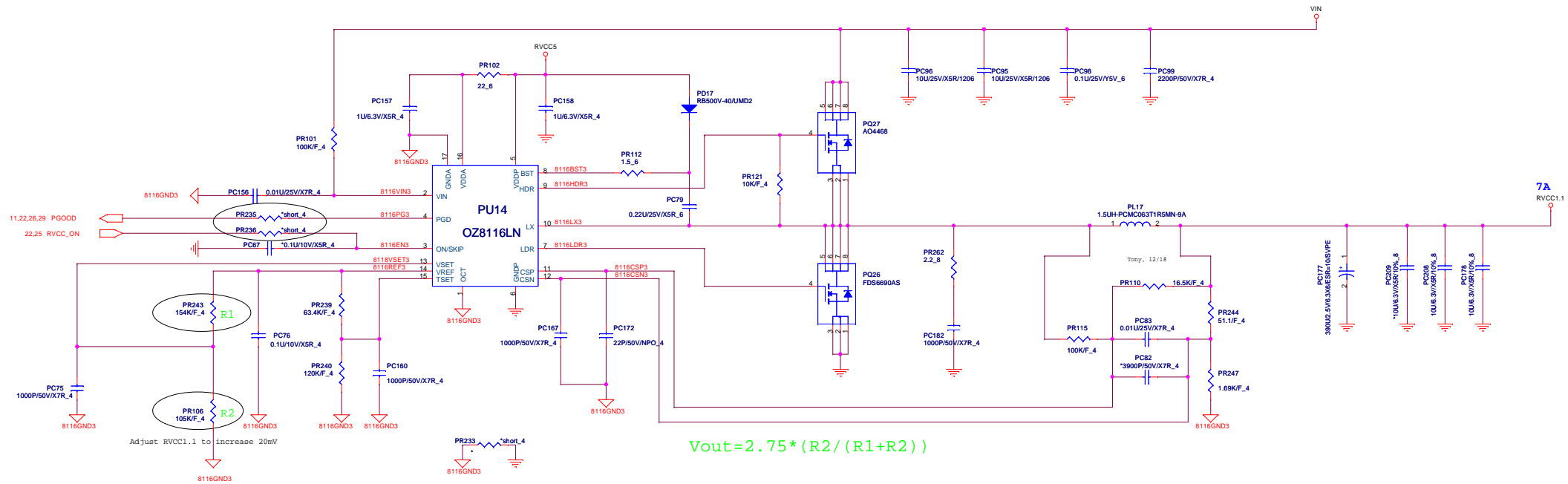
QUANTA COMPUTER

File: **DYN_VCC1.1(OZ8116LN)**

Size: Custom Document Number: AMD

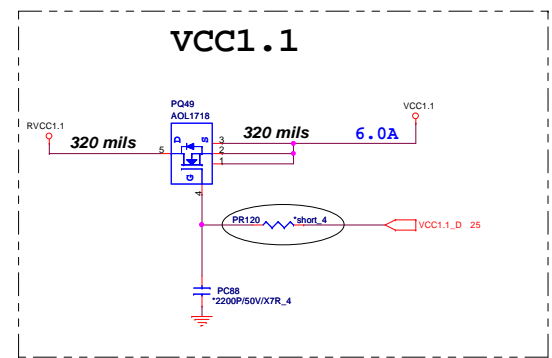
Date: Saturday, March 20, 2010 Sheet: 27 of 8 Row: 3A

1. Level 1 Environment-related Substances Should NEVER be Used.
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$V_{out} = 2.75 * (R2 / (R1 + R2))$

Adjust RVCC1.1 to increase 20mV



QUANTA COMPUTER

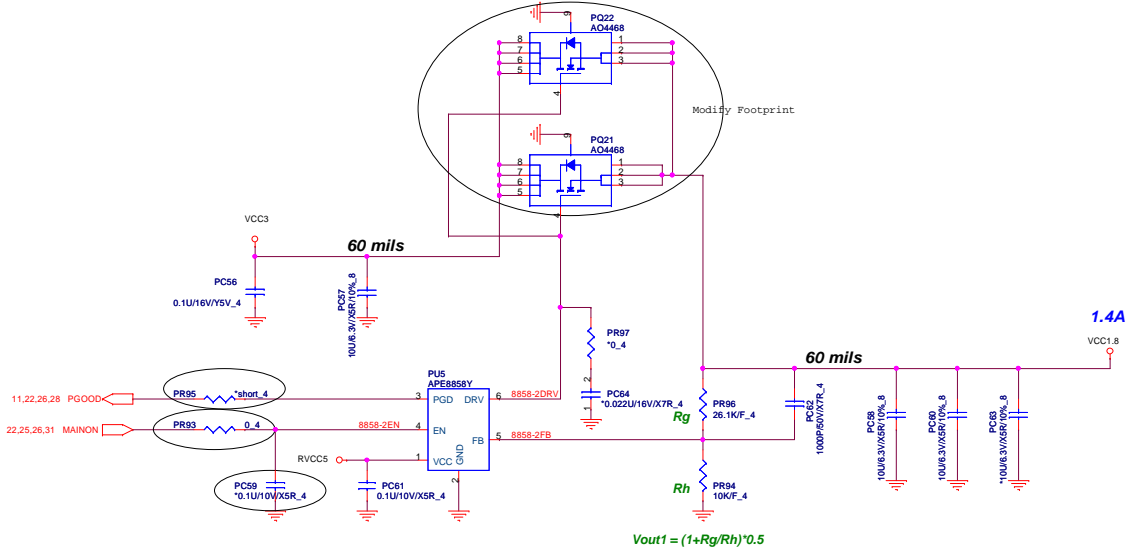
File: **VCC1.1(OZ8116LN)-7A**

Size: Custom Document Number: **AMD** Row: **3A**

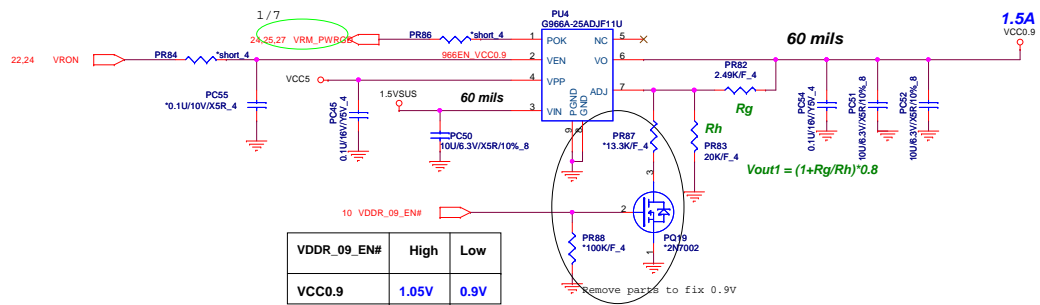
Date: Saturday, March 20, 2010 Sheet: 28 of 8

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

VCC1.8

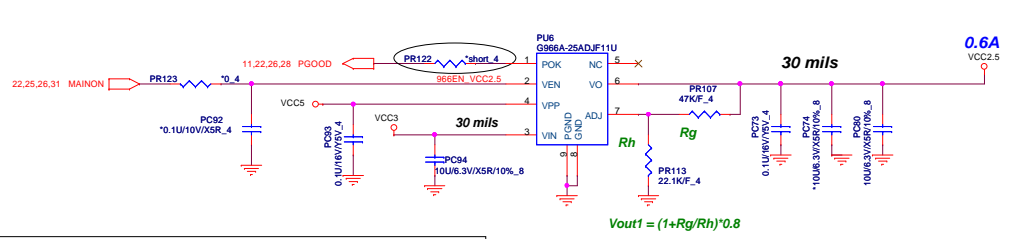


VCC0.9

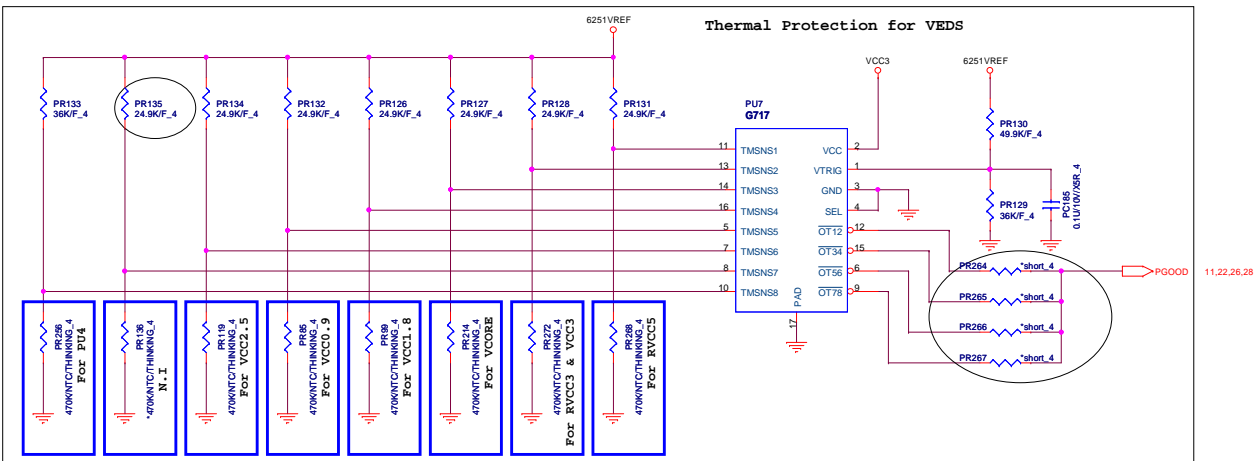


VDDR_09_EN#	High	Low
VCC0.9	1.05V	0.9V

VCC2.5



Thermal Protection for VEDS



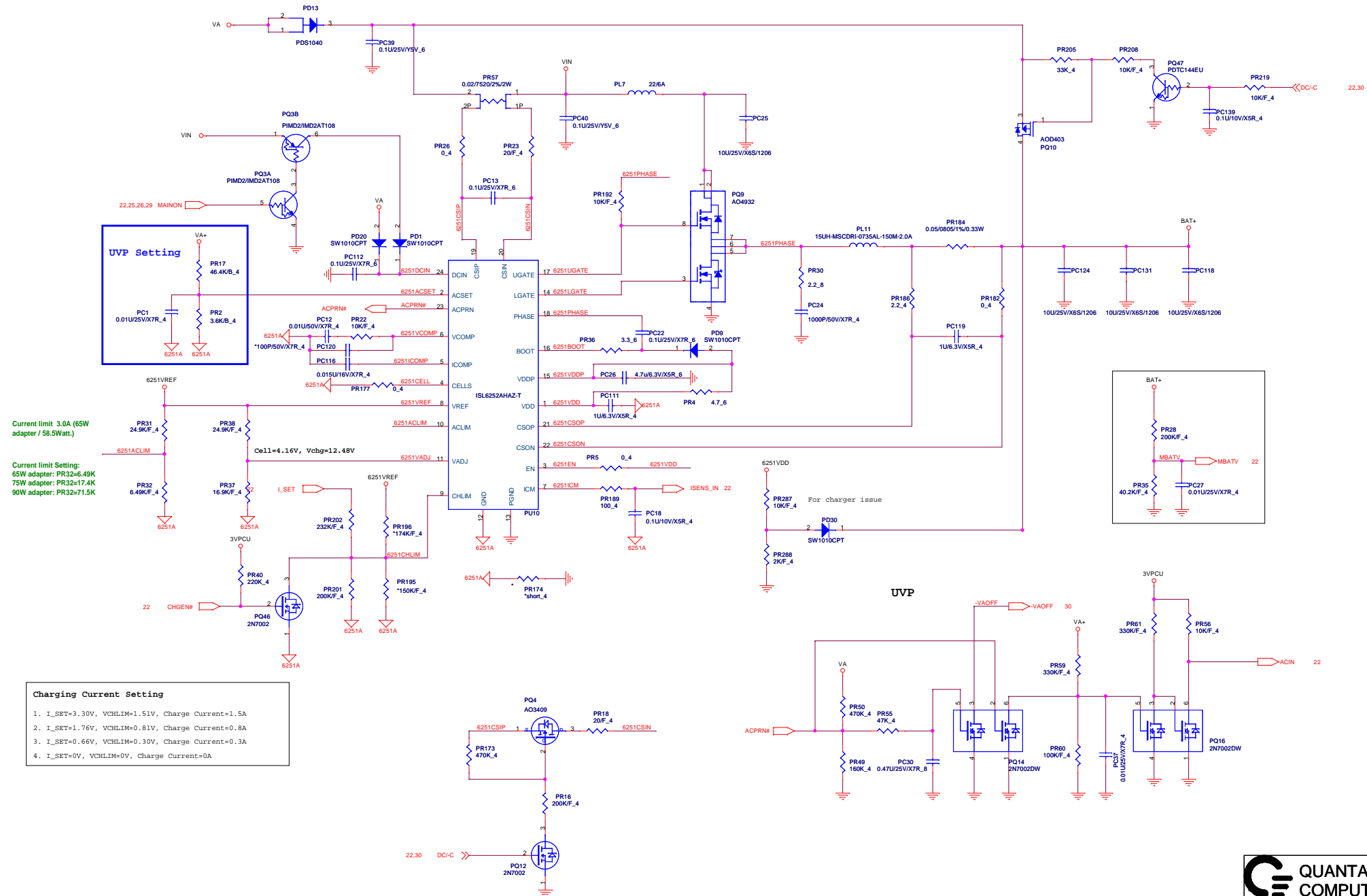
1. Level 1 Environment-related Substances should NEVER be used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

File: **VCC1.8/0.9/2.5**

Size: Custom Document Number: **AMD** Row: 3A

Date: Saturday, March 20, 2010 Sheet: 29 of 8



UVP Setting

VA+
PR17 46.4K_{B_4}
PR2 3.6K_{B_4}
PC1 0.01U/25V/X7R_4

Current limit 3.0A (65W adapter / 58.5Watt.)

Current limit Setting:
65W adapter: PR32=6.49K
75W adapter: PR32=17.4K
90W adapter: PR32=71.5K

Charging Current Setting

- I_SET=3.30V, VCHLIM=1.51V, Charge Current=1.5A
- I_SET=1.76V, VCHLIM=0.81V, Charge Current=0.8A
- I_SET=0.66V, VCHLIM=0.30V, Charge Current=0.3A
- I_SET=0V, VCHLIM=0V, Charge Current=0A

BAT+
PR28 200K_{F_4}
MBATV
PR35 40.2K_{F_4}
PC27 0.01U/25V/X7R_4

QUANTA COMPUTER

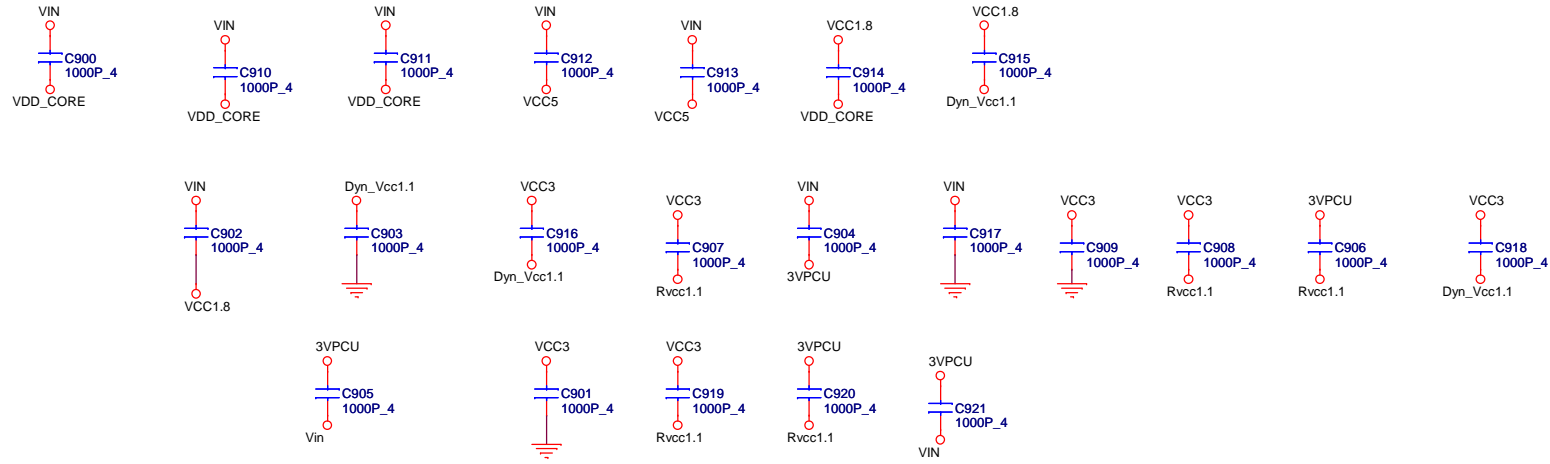
CHARGER(ISL6252A)

AMD

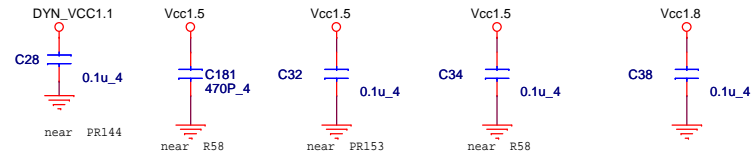
Date: Saturday, March 20, 2010 Sheet 31 of 8

1.Level 1 Environment-related Substances Should NEVER be Used.
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Decoupling Cap



Power ripple



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Title		
Decoupling Cap		
Size	Document Number	Rev
B	AMD	3A
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Power on Sequence required:

- SB800:**
 1. +3.3VDUAL ramp before +1.1VDUAL
 2. +3.3V ramp before +1.8V
 3. +1.8V ramp before +1.1V
 4. +3.3V ramp before +1.1V
 5. +3.3VALW_R ramping down time > 300us
 6. 50uS <= All power rails except +3.3VALW_R <= 40mS
 7. 100uS <= +3.3VALW_R <= 40mS

- RS880:**
 1. 0 <(+3.3V) - (-1.8V) < 2.1
 2. +1.8V ramp before +1.1V
 3. +1.1V ramp before VCC_NB

SB OUTPUT - - - - -NB_PWRGD
 NB_PWRGD_IN
 SB INPUT - - - - -SB_PWRGD

GROUP B
 PGOOD(DYN)
 DYN_VCC1.1
 VLDT(VCC1.1)
 VCC1.1
 VRM_PWRGD
 VCC0.9
 VDD_CORE (VRON)
 VDDNB_CORE

GROUP A
 PGOOD(2.5)
 VCC2.5 (CPU_VDDA_2.5_RUN)
 VCC1.5
 PGOOD(1.8)
 VCC1.8
 VCC3, VCC5
 MAINON
 SUSON
 PM_SLP_S3#

CPU MEM CTL & DDR3 SODIMM PWRs
 PGOOD(1.5)
 MEM_VTT

1.5VSUS

CPU_THM/SB/SB_SCL1/2
 SB_KB/SPI/LPC ROM PWRs
 EC_DNBSWON#
 RSMRST#

RVCC5, RVCC3, RVCC1.1

VDD_DUAL_EN

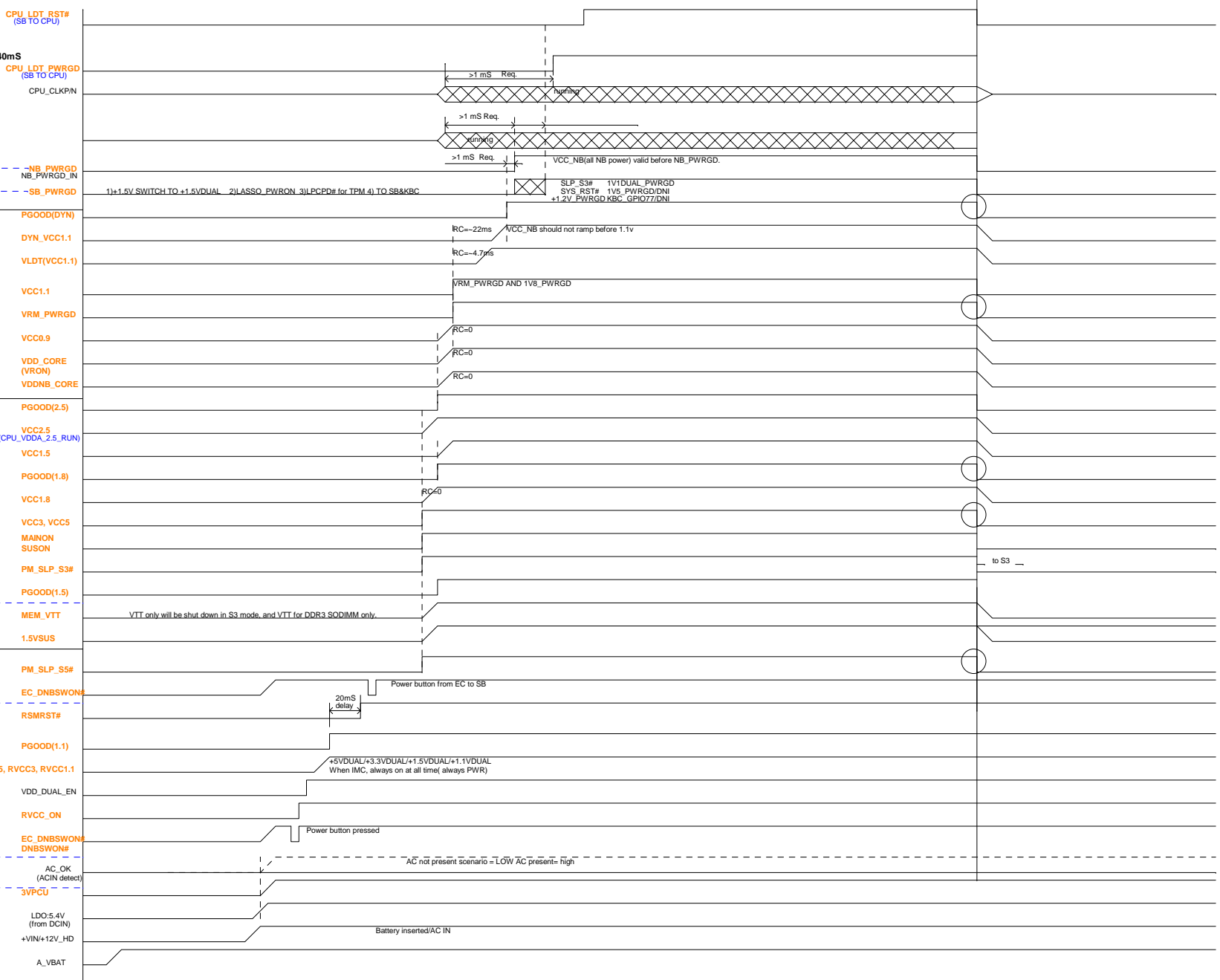
RVCC_ON

KBC is ready
 EC_DNBSWON#
 DNBSWON#

KBC is powered by A_VBAT & +3.3VALW
 AC_OK (ACIN detect)
 3VPCU

LDO:5.4V (from DCIN)
 +VIN/+12V_HD

A_VBAT



QUANTA COMPUTER

Change History

File			Rev	3A
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1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Welding resins only from the business Partners that Sony approves as Green Partners.

12/21

Page 10--R309 unmount
Page 8--R252 mount(CS00002JB38)RESISTOR CHIP 0 1/16W +-5%(0402)
Page 8--R101 & R106 unmount
Page 12--mount R184,R179,R289(CS31002FB26) RC0402,RC0402-C,0402-CNXT
Page 11--change R174,R175,R278,R146 to 10Kohm(CS31002JB28; RES CHIP 10K 1/16W +-5% (0402))
Page 21--LU1 change AL008111001 to AL008111002
Page 20--C29,C30 Mount 33PF CH03306JB04
Page 10--R20,R21 change CS00003J951 to bead CX8PG471000

12/22

Page 16--RP38 pin2 & pin 4 change net name :HDMI_TCXP & HDMI_TXCN
Page 16--C422 & C421 change net name :HDMI_TCXP & HDMI_TXCN
Page 32--H12 need change footprint

Page 32--H22 need change footprint

Page 32--remove H19

Page 32--Add H23 & H24

Page 10-- modify net name as NB_DISP_CLKN

12/23

Page 32--PU VCC5 TBDATA & TBCLK
Page 20--add 3 pcs 0ohm for EMI
Page 32--Add H23 footprint H-E315X315D102P2 & H24 footprint H-E315X315D102P2

Page 32--change footprint
H1 : H-E315X315D102P2-4
H2 : H-E315X630D102P2
H5 : H-E494X248D102P2
H6 : H-E217X358D102P2
H7 : H-E343X276D102P2
H12 : H-C236D102P2
H18 : H-E315X315D102P2-5
H22 : H-E315X198D102P2

12/24

Page 21 -- change 25MHz XTAL P/N:BG625000737
LC20 & LC21 change to CH03306JB04

12/25

Page 15 --camera power source 從USB power 改成RVCC5

12/28

Page 22 --U11(35001) ID pin 漏電問題, 請參考GD3加上diode, R108,R110,100 ohm PU改成2.2K;R272 10k ohm PU改成4.7k ohm
Page 22 --slp_s5#從EC pin 26改成106, 相當於Intel的slp_s4#, pin 26到106中間留一顆0 ohm接起來先不上
Page 11,15,22 --SB_PWRGD接到EC pin 16, 並改名為HW_PWRGD, 以方便辨識
Page 20 --change codec U34 P/N:AL000269007

12/29

Page 19 --remove Express card

1/15

1/13

Page18: MC8 unmount for MS card recognize issue
Page4 : Reverse CPU_VTT_SENSE PU VCC0.9
Page26: PR109 reserve for leakage issue

Page 3:con20 CPU_LDT_RST# add C31(reserve)
Page 21: LU1 pin 30 add LR4 10Kohm
Page 29: mount PR86
AJ069700T08-->IC CTRL(605P)SB820M
AJ075200T16--> IC CTRL(528P)RS880M
Page 16: Change CON13 footprint -->hdmi-c12806-11908-1-19p-v

1/19

Page 32: H19 add Spad-NE7-1-NP
Page 32 :H14 change footprint H-E315X315D110P2
Page 21: LU2 Change P/N DBBL5MLAN01

1/18

Page 3: T10 & T11 change footprint TP3050

1/4 Change footprint for layout

Page 20--U34 QFN48-7X7-5-49P-SMT
Page 26,25,25--PL16,PL19,PL20 CHOKE-ETQP4LR36WFC-4P-SMT
Page 30--PU9 HVSOF5-1_6-5-5P-SMT
Page 23--CON2 88513-2641-26P-L-SMT
Page 32--CON3 88513-0601-6P-L-SMT
Page 32
H2 O-NE7-2
H22 O-NE7-1
H6 O-NE7-3
H12 H-C236D102P2
H16 O-NE7-4
H1 H-TE295X295BE276X276D102P2
H18 H-E315X315D102P2-1
H5 H-E494X248D102P2-1
H7 H-E315X272D102P2

Page 21-- LU2 TRF-10-1-24P-SMT 加入-SMT
Page 18-- CN6 CARD-JBS010-2601-0-10P 移除-NB3
Page 24--PC142 ECAP10X6S 移除-Z01
Page 24--PL13,PL14 CHOKE-PCMB104T-R45MN-4P 移除-WK1

Add test point

Page3--U21 AF9 , AE9 , AC9 , AA9
Page11--U28 C4 , E7 , F7 , E8
Page22--U13 Pin21 , 25 , 17 , 20 , 48 , 50 , 51 , 52 , 110 , 111 , 112 , 35

*For screen will be clone mode bug
Page15--R265 change from 75 ohm to 140 ohm
R260 change from 75 ohm to 150 ohm
R254 change from 75 ohm to 150 ohm

*For Power on issue
Page28--PQ49 pin4 pin name change from VRM_PWRGD to MAIN0

1/5

*Avoid system shutdown
Page11--CPU_THERMTRIP#上加一顆10K pull high到RVCC3

*For overload fail issue
Page 32--R130 change from 22ohm to F7 FUSE SMD 0.12A 48V
1/7

Page 15: R94, R99 change from 2.2k to 4.7K ohm for VEDS ARGB(4-5).

Page 14: remove no need cap for cost down
Page 11: R174;R175 PU power change from VCC3 to RVCC3
Page 11: RSMRST# schematic unmount

Page 6: Side port memory vref voltage PU low
Page 29: PU4 pin1 change pin name from PGOOD to VRM_PWRGD

Page 17: remove WLAN VCC1.5_MINI
Page 5: remove C34, C28
Page 32: Touch Pad CON3 pin reverse
Page 32: USB CON4 add GND Pin from 27~30

1/11
Page 18:CN6 change footprint mscard-cb1s-025-10p-1 for SMT request
Page 14:Add C37

Page 10:change Y7 P/N(BG332768542) and C480=18PF for timing accuracy

1/12
Page 15:CON7.10-->INT_LVDS_BLON: it is the PWM output to adjust the brightness.
U3.2-->INT_LVDS_ENA_BL: Enables Backlight for CPIS compliant LCD panels

Page 17:chang WLAN SW4 the same as SY2

Page 19:change BT con footprint AXK5F10537YG-10P-RUV --> add fix hole for SMT request

1/14

Page 20 --Add AMP_PD# schematic
Page 11:SUS_STAT# signal, it is OD; need pull up


QUANTA COMPUTER logo and Change History table with columns for Title, Size, Document Number, Date, Sheet, and Rev.

1.Level 1 Environment-related Substances Should NEVER be Used.
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1/21--->改版PVT
 Page 21:L1 pin26 ISOLATE# add 15kohm PD
1/22
 Page 10: Y7 change P/N:BG332768909
 C478 change to 18PF
 Page 10: change Y12 P/N: BG625000486
 and C430=C431 27PF for timing accuracy
 Page 21:L1Y1 Change 25MHz XTAL P/N:BG625000486(2nd:BG625000737)
2/10
 Page11: HW_PWRGD PD 10Kohm ---decrease impact on switch issue
 Page 20: ChangeR317,R323 from 22ohm to 0ohm for FSOV Fail issue
 Page 20: AMP_PD# power change from +5VA to 3VPCU
 Page 22: add INT_LVDS_ENA_BL pin for EC control backlight
 Page11: R174,R175 change from 10kohm to 2.2kohm
 Page14: C10 chagne from 10UF to 4.7UF
 Page15: chagne CON7 LVDS con
 Page19: chagne CON18 BT con
 Page17: chagne WLAN switch SW4
 Page20: chagne spk con CON10
 Page3: CPU_LDT_RST# add R69 short pad for debug
3/5
 Page16: change power source for CRT port
 Page16: change D9,D7 P/N and mount R266,R267
 Page21: LR8 umount
 Page22: R68 mount
3/8
 Page 24: Change PC 142 footprint ECAP10X6S-Z01
 Page 16: Change CON13 footprint & P/N:
 from hdmi-c12806-11908-1-19p-v to Hdmi-c12825-11908-1-19p-v
3/9
 Page 23: delete L27
 Page6 & Page11: remove all side port component
3/10
 Page 3:add C291 & C137(mount) change from 0.1u(CH4102M9B13) to
 180pf (CH11806JB09)
 for power noise
 Page 3:C31(mount) change from 33pf to 180pf (CH11806JB09)
 for power noise
3/11
 Page6 :R47 and R49 change from 0ohm to short pad
 Page8 :R245 change from 0ohm to short pad
 Page20 :remove R220
 Page20 :change C488,C491,C494 from AGND to GND
 Page 3 & 22 & 10: Change CPU Prochot schematic controlled by EC
 Page 3 mount R267
 Page 6:delete R56 & R63
 Page 8: change R83,R77,R65,R253,R71,R57,R91,R245 & R250 to short pad
 Page 8: delete R255,R252
3/12
 Page 9: delete R251,R249,C377,c191,c201,c195,c184,c196,R93,R89 for no side port
 Page 10: delete RP5,RP29,RP32,RP15,RP35,RP30
 Page 10: delete R300
 Page 11:delete RP27,SW1,RP25 (remove Panel ID set)
 Page 18:Change MR19,MR3,MR2,MR9,MR10,MR11,MR12,MR13,MR14,MR15,MR16,MR17,MR18,MR8 to short pad
 Page 24:Change PC142 footprint Ecap10x6s-SMT
 Page20 :delete R322,R329,R328
 Page21 :delete LR14
 Page21 :change LR6 to short pad
 Page 9: Change L7,L5,L6,L8,R80,R95 to short pad
 Page 13: Change R187,L10,L9,L15,L13,L28,L18,R169,L12,L11,L19,L14,L17,R127,R284,L26,R145 to short pad

3/15
 Page 20: reserve Q29 and R399,
 mount R367 for pop noise
 Page 20:Change R330、R321、R346、R347 from 1.5K ohm to 10K ohm for pop noise
 Page 20:add C343,C345,C346,C347 10uF for pop noise
 Page 8:R86 change from 30lohm to 1Kohm
 Page 11:R207& R208 from 100k ohm to 10k ohm
 Page 20:R363 umount
 Page 18:ML1 & MR4 change to short pad
 Page 19:delete Q16
 Page21:change con9 from DFTJ08FR085 to DFTJ08FR167
 Page22:U13 GPIO66 PL 10kohm(R159)
 Page 12:delete R176
 Page 15:delete R36
 Page 19:con18 delete T39,T40
 Page 20:delete R317,R323
 Page 20:R214 change from 0ohm to short pad
 Page 22:delete R68
 Page 3:delete con20 & C31 & C267
 Page 3:reserve C182 0.1uF
 Page 3:R69 change to short pad
3/16
 Page 23:reserve U42 ESD part
 Page 32:change con4 抽屜式
 Page 32:change H13,H15,H17,and add H23,H24 NUT
 Page 19:Reverse C786, C787, C788 FP for ESD
 Page 20:C342 umount
 Page 20:CPU_PROCHOT# add C312
 Page 9:mount C217 for DYN_VCC1.1 power ripple too large
3/17
 Page20:R206,R205,R215,R210,R209,R222,R211,R217,R223 change to short pad
 Page 3:reserve C184 0.1uF
 Page21:change LC23 from 1000P/2KV to 1000P/3KV
 Page 3:delete R51,R50
 Page 4:delete R11
 Page20:L1-L4 change P/N to CX121T20100
 Page 16:delete RP38
 Page 18:delete MRP1
 Page 22:delete R155
 Page 3:delete R238
 Page 15:delete R355
 Page 15: R273 change from CS41002JB20 to CS41002FB28
3/20
 Page 32: change R236,R237 from 150 ohm to 75ohm for two color LED

1.Level 1 Environment-related Substances Should NEVER be Used.
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 Quanta Computer Inc. PROJECT : NE8		Rev
		3A
CHANGE LIST 2		
Date:	Saturday, March 20, 2010	Sheet 36 of 42