

Compal Confidential

NEW50/70/80/90 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ixex Peak-M
ATI Madision/Park

2010-01-07

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	Cover Page
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				NEW70 M/B LA-5891P Schematic	1.0
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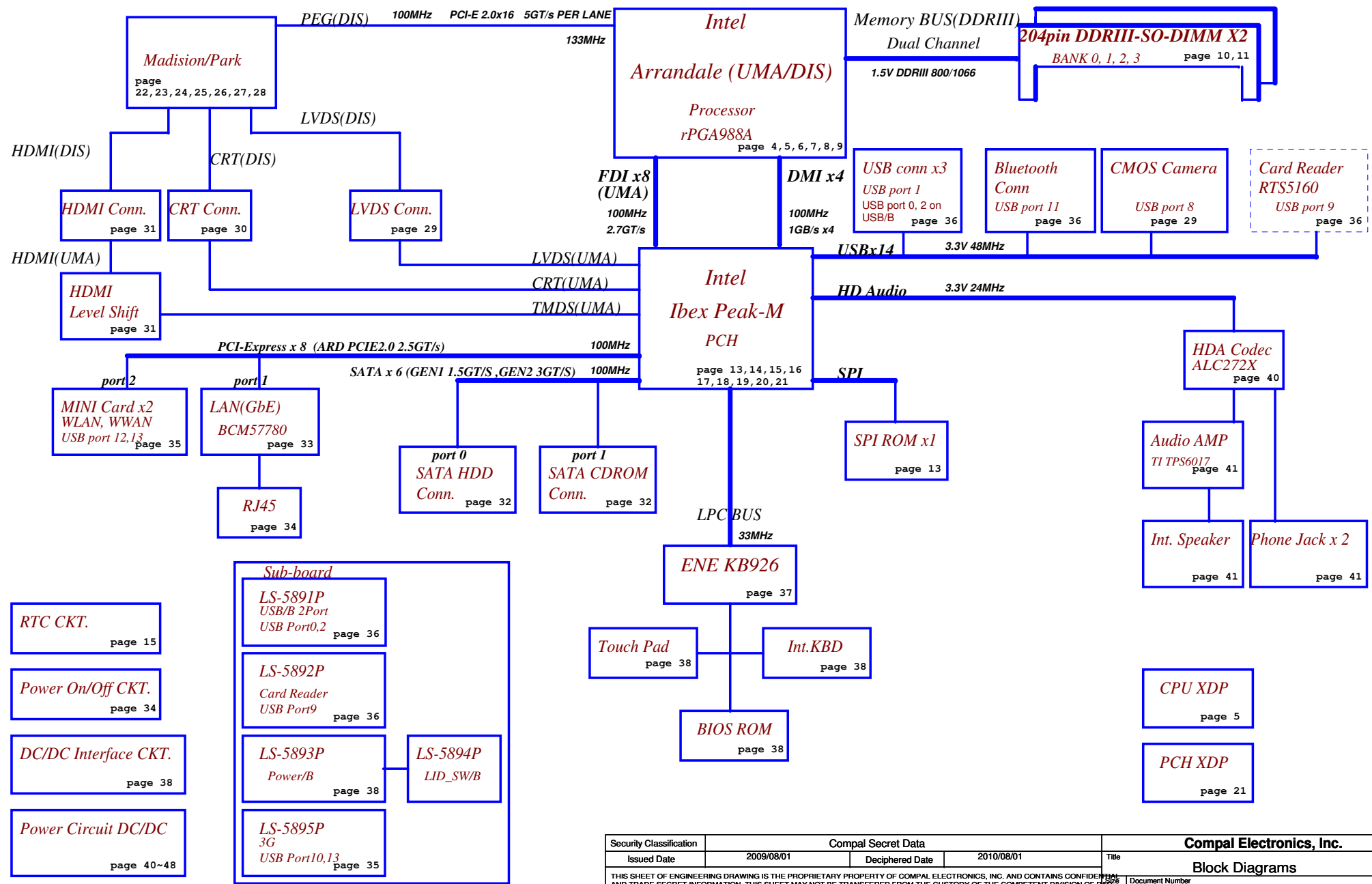
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Model Name : NEW50/70/80/90

File Name : LA5891P

Fan Control
page 38

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-VB-GRT
133/120/100/96/14.318MHZ to PCH
page 12



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011Xb		

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Option	UMAHD@	VGAMD@	HDMI@	@	SG@
UMA	V	X	V	X	X
VGA	X	V	V	X	X
SG	X	V	V	X	V
NO HDMI	X	X	X	X	X

3G & BT Config
3G SKU: 3G@
BT SKU: BT@

GPU BOM Config
Madison SKU: MADI@
Park SKU: PARK@

VRAM BOM Config
X761@: X76198BOL01 Park Samsung 512MB
X762@: X76198BOL02 Park Hynix 512MB
X763@: X76198BOL03 Madison Samsung 1024MB
X764@: X76198BOL04 Madison Hynix 1024MB
X765@: X76198BOL05 Park AMD 512MB
X766@: X76198BOL06 Madison AMD 1024MB

LED BOM config
NEW70,80 SKU: 7080@
NEW50,90 SKU: 5090@

BOM Config
UMA W/O HDMI SKU: BT@/3G@/UMA@/UMAO@
UMA W/ HDMI SKU: BT@/3G@/UMA@/UMAO@/HDMI@/UMAHD@
Discrete W/O HDMI SKU: BT@/3G@/DIS@/DISO@/VGA@
Discrete W/ HDMI SKU: BT@/3G@/DIS@/DISO@/VGA@/HDMI@/VGAMD@
Switchable W/O HDMI SKU: BT@/3G@/DIS@/UMA@/VGA@/SG@
Switchable W HDMI SKU: BT@/3G@/DIS@/UMA@/VGA@/SG@/HDMI@/VGAMD@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMAO@
Discrete	DIS@
Discrete Only	DISO@
GPU ALL Components	VGA@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
UMA HDMI	UMAHD@
Discrete HDMI	VGAMD@
UMA & DIS POP HDMI	HDMI@
GPU Madison	MADI@
GPU Park	PARK@
NEW70,80 LED	7080@
NEW50,90 LED	5090@

X76@

ID3, ID1 : VRAM Vender

Location	VRAM_ID3	VRAM_ID1
Samsung	0 R492	0 R474
HYNIX	1 R491	0 R474
AMD	1 R491	1 R473

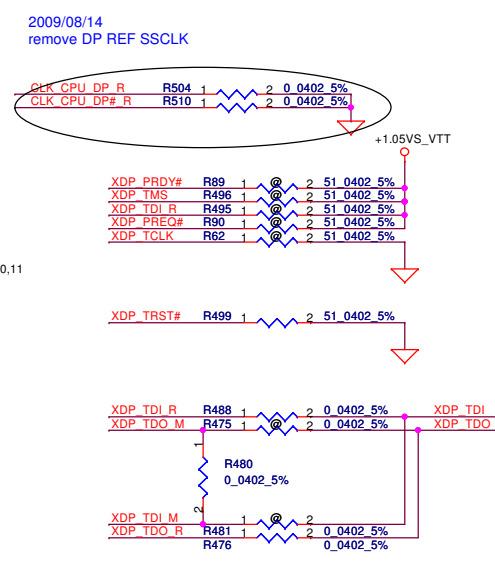
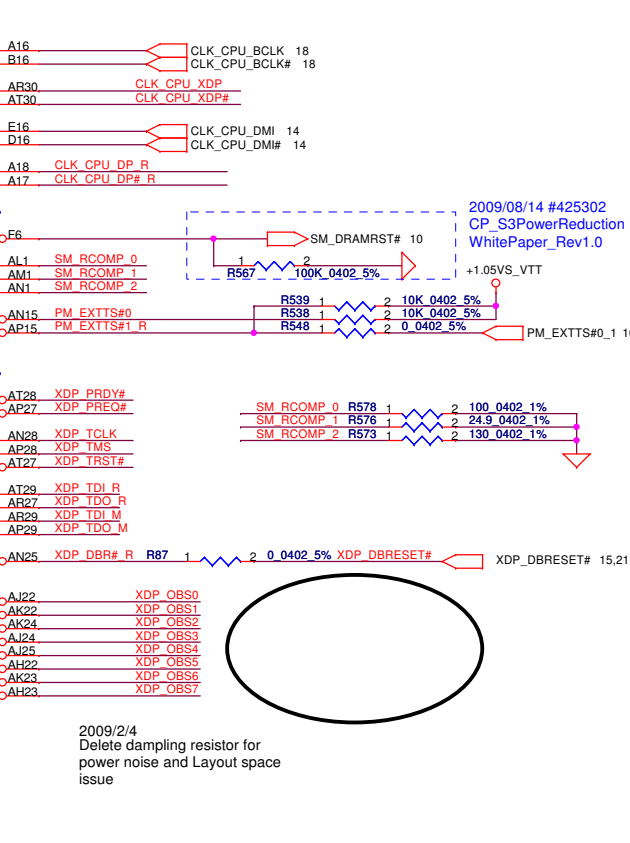
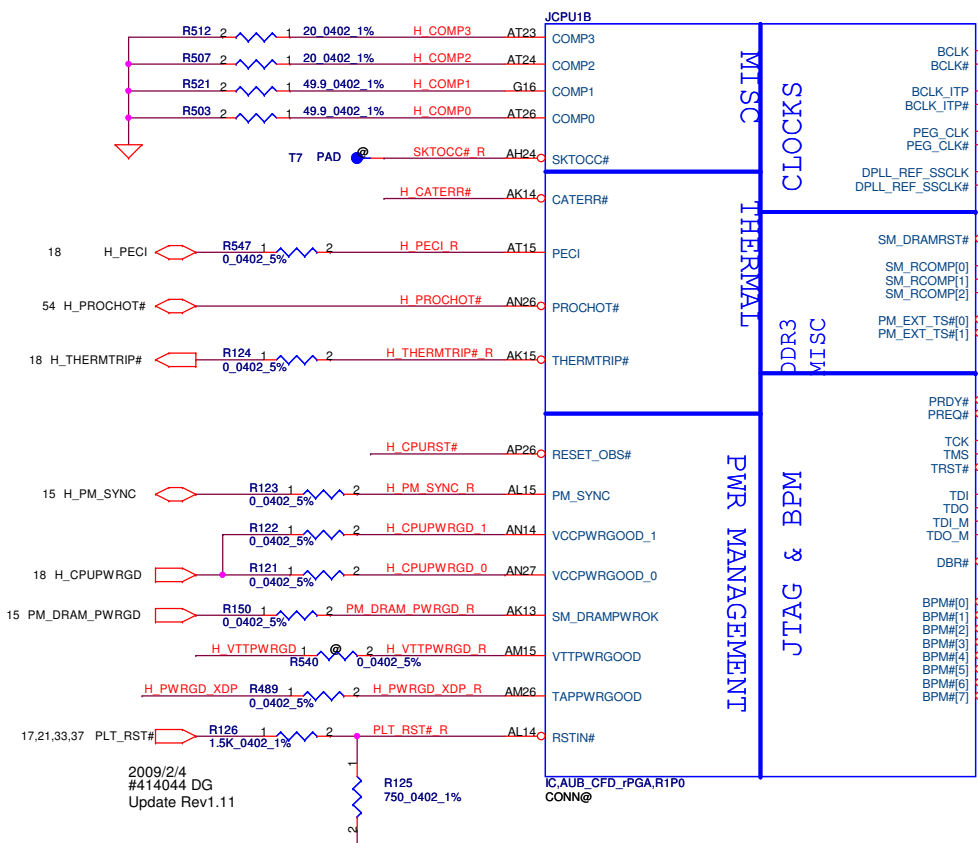
ID2: VRAM Size

VRAM	Location	VRAM_ID2
8PCS 64Mx16		0
4PCS 64Mx16		1

VRAM P/N :

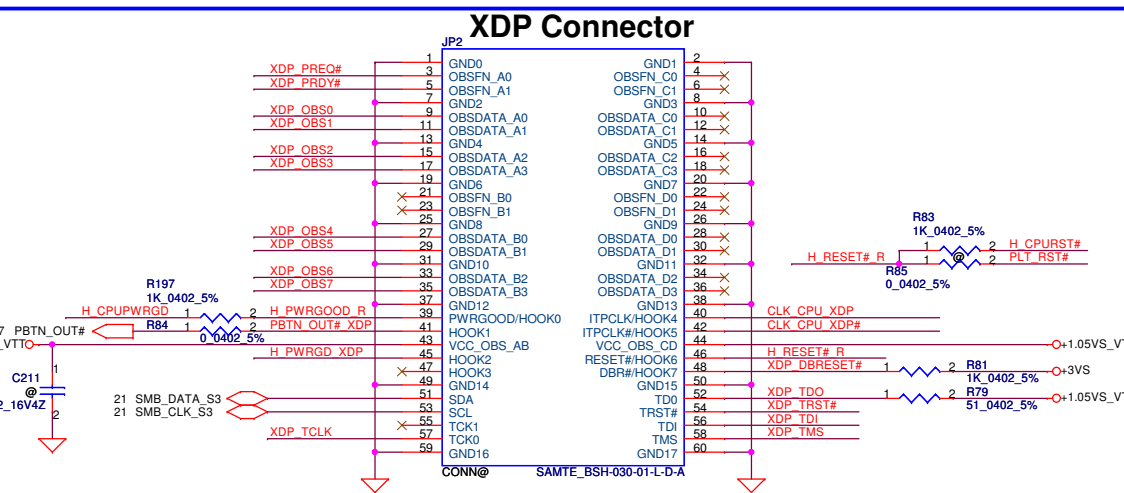
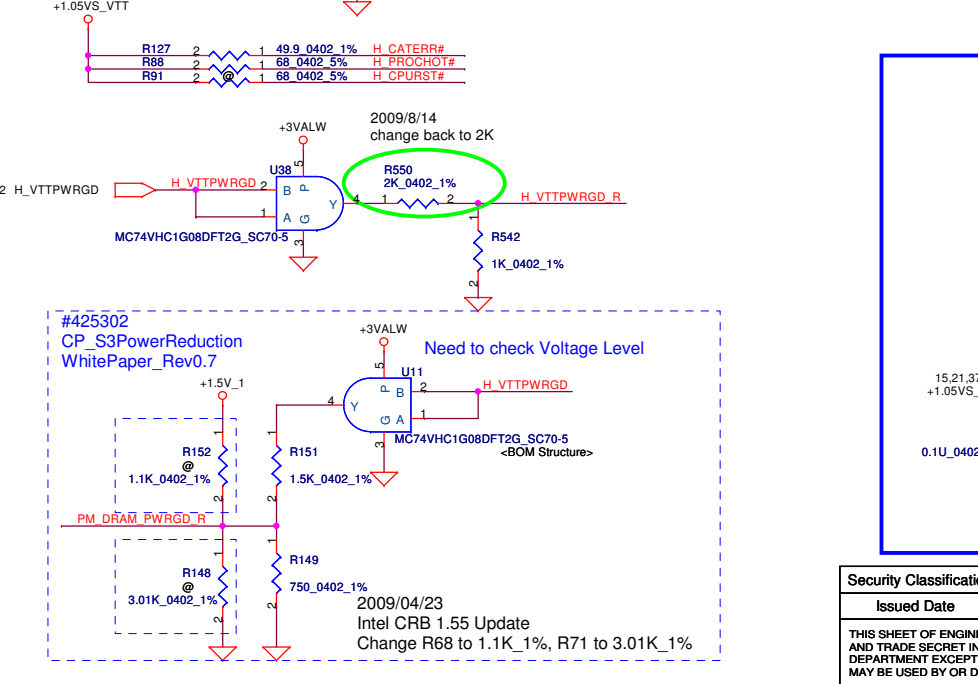
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
 AMD : SA00003PF20 (S IC D3 23EY2387MB-12)

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JTAG MAPPING 2009/09/16 update

Scan Chain (Default)	STUFF -> R488, R476 NO STUFF -> R475, R481
CPU Only	STUFF -> R488, R475 NO STUFF -> R480, R481, R476
GMCH Only	STUFF -> R481, R476 NO STUFF -> R488, R475, R480



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10 DDR_A_D[0..63]
 10 DDR_A_DM[0..7]
 10 DDR_A_DQS[0..7]
 10 DDR_A_DOS[0..7]
 10 DDR_A_MA[0..15]

JCPU1C

DDR A D0 A10
 DDR A D1 C10
 DDR A D2 C7
 DDR A D3 A7
 DDR A D4 B10
 DDR A D5 D10
 DDR A D6 E10
 DDR A D7 A8
 DDR A D8 D8
 DDR A D9 F10
 DDR A D10 E6
 DDR A D11 E2
 DDR A D12 E9
 DDR A D13 B7
 DDR A D14 E7
 DDR A D15 C6
 DDR A D16 H8
 DDR A D17 G8
 DDR A D18 K7
 DDR A D19 J8
 DDR A D20 G7
 DDR A D21 G10
 DDR A D22 J7
 DDR A D23 J10
 DDR A D24 L7
 DDR A D25 M6
 DDR A D26 M8
 DDR A D27 L9
 DDR A D28 L6
 DDR A D29 K8
 DDR A D30 N8
 DDR A D31 P9
 DDR A D32 AH5
 DDR A D33 AF5
 DDR A D34 AK6
 DDR A D35 AK7
 DDR A D36 AF6
 DDR A D37 AG5
 DDR A D38 AI7
 DDR A D39 AI6
 DDR A D40 AJ10
 DDR A D41 AI9
 DDR A D42 AL10
 DDR A D43 AK12
 DDR A D44 AK8
 DDR A D45 AL7
 DDR A D46 AK11
 DDR A D47 AL8
 DDR A D48 AN8
 DDR A D49 AM10
 DDR A D50 AR11
 DDR A D51 AL11
 DDR A D52 AM9
 DDR A D53 AN9
 DDR A D54 AT11
 DDR A D55 AP12
 DDR A D56 AM12
 DDR A D57 AN12
 DDR A D58 AM13
 DDR A D59 AT14
 DDR A D60 AT12
 DDR A D61 AL13
 DDR A D62 AR14
 DDR A D63 AP14
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 SA_DQ[57]
 SA_DQ[58]
 SA_DQ[59]
 SA_DQ[60]
 SA_DQ[61]
 SA_DQ[62]
 SA_DQ[63]

DDR SYSTEM MEMORY A

SA_CK[0] AA6
 SA_CK#0 AA7
 SA_CKE[0] P7
 SA_CK[1] Y6
 SA_CK#1 Y5
 SA_CKE[1] P6
 SA_CS#0 CAE2
 SA_CS#1 CAE8
 SA_ODT[0] AD8
 SA_ODT[1] AF9
 SA_DM[0] B9
 SA_DM[1] D7
 SA_DM[2] LH7
 SA_DM[3] M7
 SA_DM[4] AG6
 SA_DM[5] AM7
 SA_DM[6] AN10
 SA_DM[7] AN13
 SA_DQS#0 C9
 SA_DQS#1 CE8
 SA_DQS#2 CJ9
 SA_DQS#3 CAH7
 SA_DQS#4 CAK9
 SA_DQS#5 CAP11
 SA_DQS#6 CAT13
 SA_DQS#7
 SA_DOS[0] C8
 SA_DOS[1] F9
 SA_DOS[2] LH9
 SA_DOS[3] AH8
 SA_DOS[4] AK10
 SA_DOS[5] AN11
 SA_DOS[6] AR13
 SA_DOS[7]
 SA_MA[0] Y3
 SA_MA[1] W1
 SA_MA[2] AA8
 SA_MA[3] AA3
 SA_MA[4] V1
 SA_MA[5] AA9
 SA_MA[6] V8
 SA_MA[7] T1
 SA_MA[8] Y9
 SA_MA[9] U6
 SA_MA[10] AD4
 SA_MA[11] T2
 SA_MA[12] U3
 SA_MA[13] AG8
 SA_MA[14] T3
 SA_MA[15] V9
 DDR A D0 M0
 DDR A D1 M1
 DDR A D2 M2
 DDR A D3 M3
 DDR A D4 M4
 DDR A D5 M5
 DDR A D6 M6
 DDR A D7 M7
 DDR A DQS#0 DQS#0
 DDR A DQS#1 DQS#1
 DDR A DQS#2 DQS#2
 DDR A DQS#3 DQS#3
 DDR A DQS#4 DQS#4
 DDR A DQS#5 DQS#5
 DDR A DQS#6 DQS#6
 DDR A DQS#7 DQS#7
 DDR A DOS#0 DOS#0
 DDR A DOS#1 DOS#1
 DDR A DOS#2 DOS#2
 DDR A DOS#3 DOS#3
 DDR A DOS#4 DOS#4
 DDR A DOS#5 DOS#5
 DDR A DOS#6 DOS#6
 DDR A DOS#7 DOS#7
 DDR A MA0 MA0
 DDR A MA1 MA1
 DDR A MA2 MA2
 DDR A MA3 MA3
 DDR A MA4 MA4
 DDR A MA5 MA5
 DDR A MA6 MA6
 DDR A MA7 MA7
 DDR A MA8 MA8
 DDR A MA9 MA9
 DDR A MA10 MA10
 DDR A MA11 MA11
 DDR A MA12 MA12
 DDR A MA13 MA13
 DDR A MA14 MA14
 DDR A MA15 MA15

IC_AUB_CFD_rPGA,R1P0
 CONN@

11 DDR_B_D[0..63]
 11 DDR_B_DM[0..7]
 11 DDR_B_DQS[0..7]
 11 DDR_B_DS[0..7]
 11 DDR_B_MA[0..15]

JCPU1D

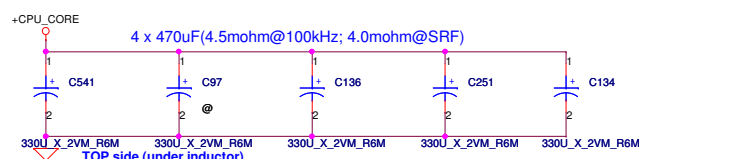
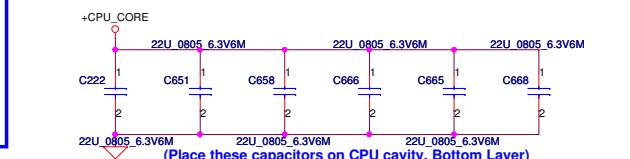
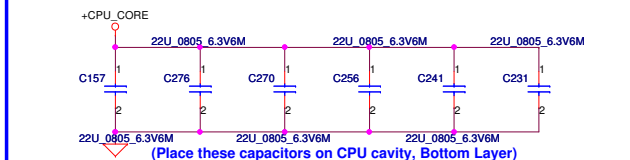
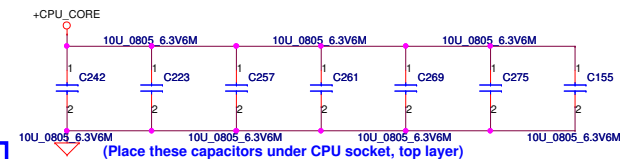
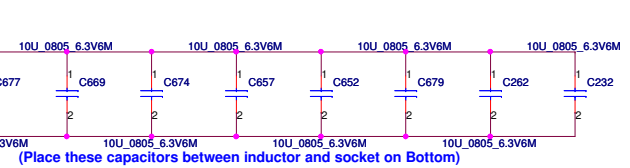
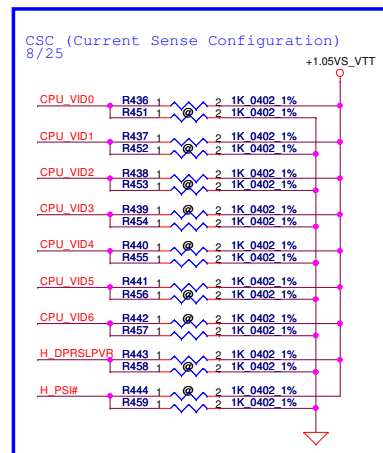
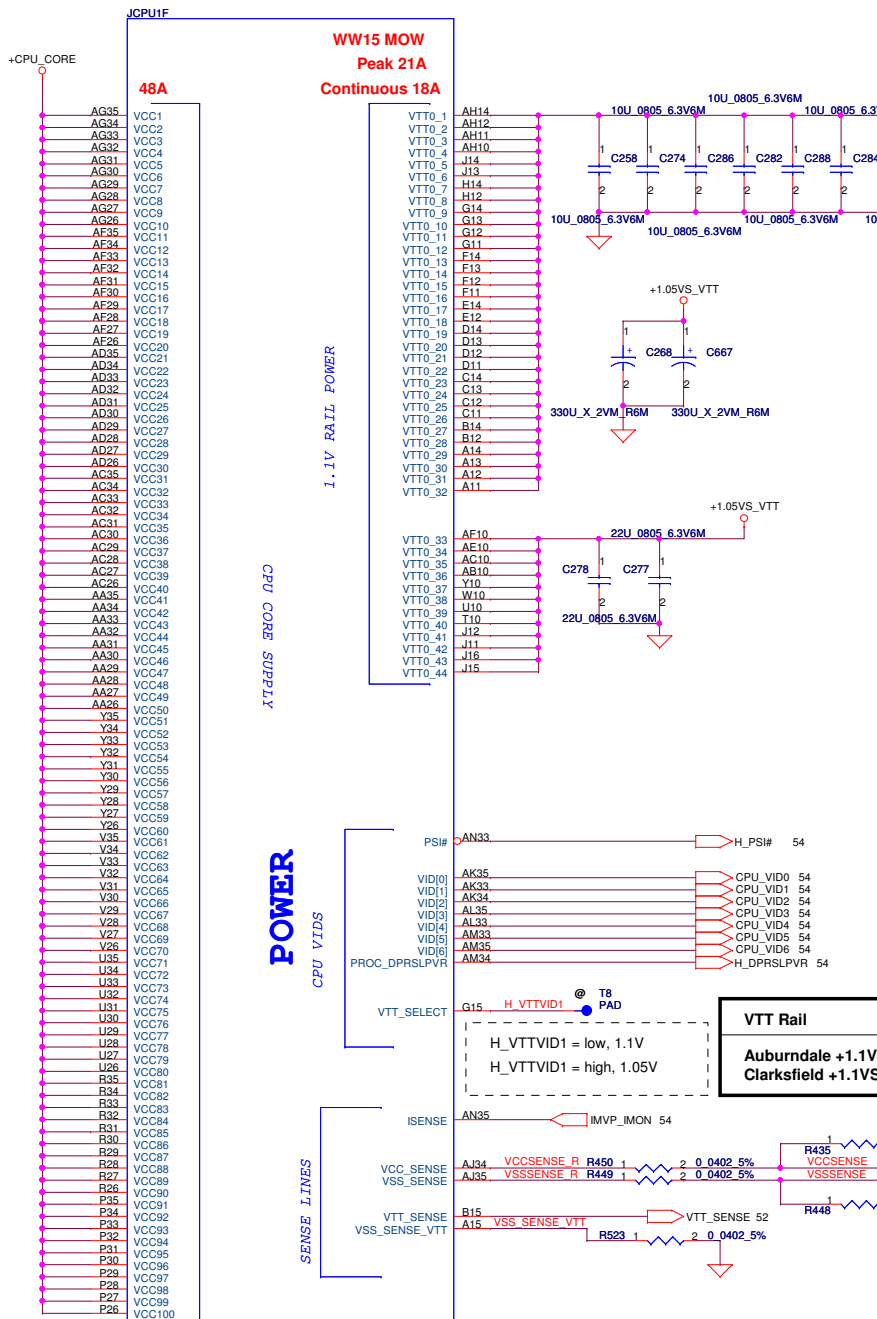
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 DDR B D1 A5
 DDR B D2 C3
 DDR B D3 B3
 DDR B D4 E4
 DDR B D5 A6
 DDR B D6 C4
 DDR B D7 D4
 DDR B D8 D1
 DDR B D9 D2
 DDR B D10 F2
 DDR B D11 F1
 DDR B D12 C2
 DDR B D13 F5
 DDR B D14 F3
 DDR B D15 G4
 DDR B D16 H6
 DDR B D17 G2
 DDR B D18 J6
 DDR B D19 J3
 DDR B D20 G1
 DDR B D21 G5
 DDR B D22 J2
 DDR B D23 J1
 DDR B D24 J5
 DDR B D25 L3
 DDR B D26 K2
 DDR B D27 M1
 DDR B D28 K5
 DDR B D29 K4
 DDR B D30 M4
 DDR B D31 N5
 DDR B D32 AG1
 DDR B D33 AG1
 DDR B D34 AG1
 DDR B D35 AK1
 DDR B D36 AG4
 DDR B D37 AG3
 DDR B D38 AJ4
 DDR B D39 AH4
 DDR B D40 AK3
 DDR B D41 AK4
 DDR B D42 AM6
 DDR B D43 AN2
 DDR B D44 AK5
 DDR B D45 AK2
 DDR B D46 AM4
 DDR B D47 AM3
 DDR B D48 AP3
 DDR B D49 AN5
 DDR B D50 AT4
 DDR B D51 AN6
 DDR B D52 AN4
 DDR B D53 AN5
 DDR B D54 AT5
 DDR B D55 AT6
 DDR B D56 AN7
 DDR B D57 AP6
 DDR B D58 AP8
 DDR B D59 AT9
 DDR B D60 AT7
 DDR B D61 AP9
 DDR B D62 AR10
 DDR B D63 AT10

DDR SYSTEM MEMORY - B

SB_CK[0] W8
 SB_CK#0 W9
 SB_CKE[0] M3
 SB_CK[1] V7
 SB_CK#1 V6
 SB_CKE[1] M2
 SB_CS#0 AB8
 SB_CS#1 AD6
 SB_ODT[0] AC7
 SB_ODT[1] AD1
 SB_DM[0] D4
 SB_DM[1] E1
 SB_DM[2] H3
 SB_DM[3] K1
 SB_DM[4] AH1
 SB_DM[5] AL2
 SB_DM[6] AR4
 SB_DM[7] AT8
 SB_DQS#0 D5
 SB_DQS#1 E4
 SB_DQS#2 D4
 SB_DQS#3 L4
 SB_DQS#4 AH2
 SB_DQS#5 AR5
 SB_DQS#6 AR8
 SB_DQS#7
 SB_DOS#0 C5
 SB_DOS#1 E3
 SB_DOS#2 H4
 SB_DOS#3 M5
 SB_DOS#4 AG2
 SB_DOS#5 AP5
 SB_DOS#6 AR7
 SB_DOS#7
 SB_MA[0] U5
 SB_MA[1] V2
 SB_MA[2] T6
 SB_MA[3] V3
 SB_MA[4] B1
 SB_MA[5] TR
 SB_MA[6] R2
 SB_MA[7] R6
 SB_MA[8] R4
 SB_MA[9] R5
 SB_MA[10] AB5
 SB_MA[11] P3
 SB_MA[12] R3
 SB_MA[13] AF7
 SB_MA[14] P5
 SB_MA[15] N1
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 DDR B D1 A5
 DDR B D2 C3
 DDR B D3 B3
 DDR B D4 E4
 DDR B D5 A6
 DDR B D6 C4
 DDR B D7 D4
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 DDR B D63 AT10
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 DDR B BS1 W5
 DDR B BS2 R7
 DDR B CAS# AC5
 DDR B RAS# Y7
 DDR B WE# AC6

IC_AUB_CFD_rPGA,R1P0
 CONN@

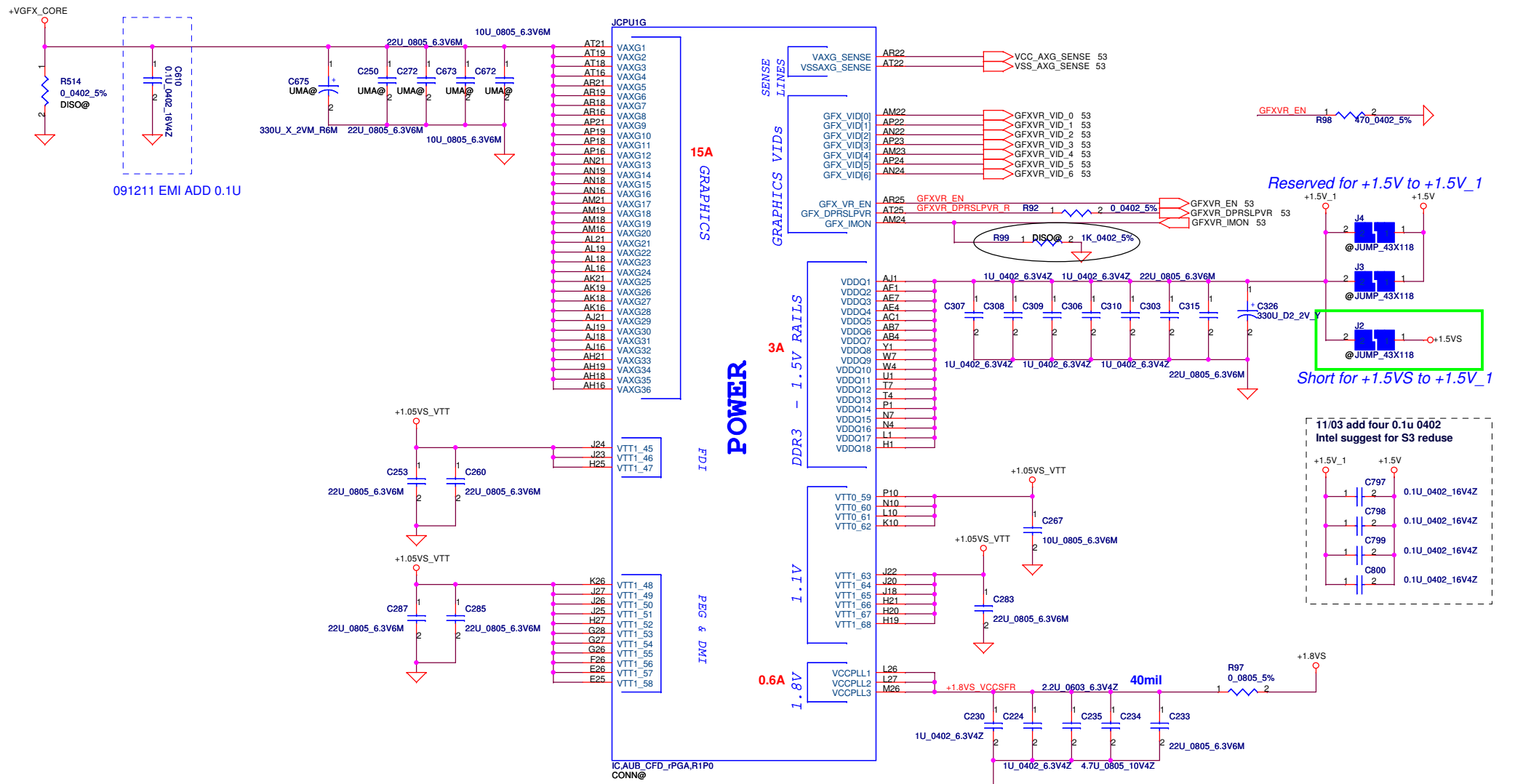
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Date		Sheet	Rev
B	NEW70 M/B LA-5891P Schematic	Tuesday, December 29, 2009		6	1.0
				of	59



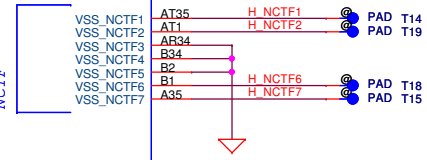
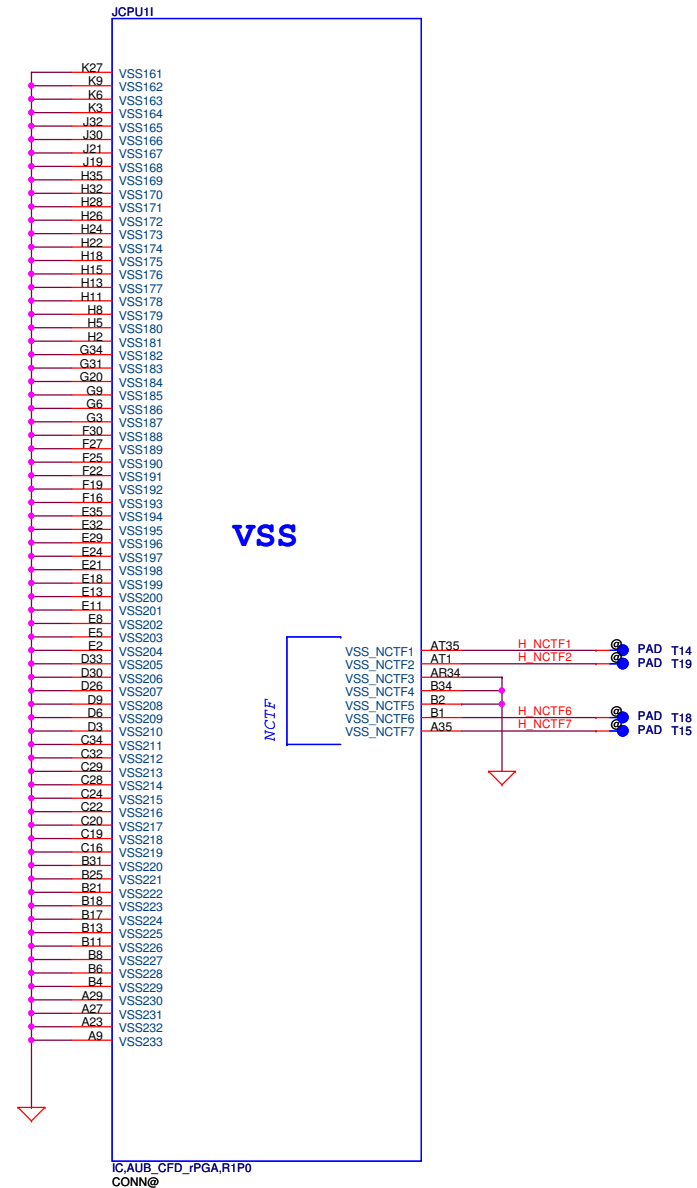
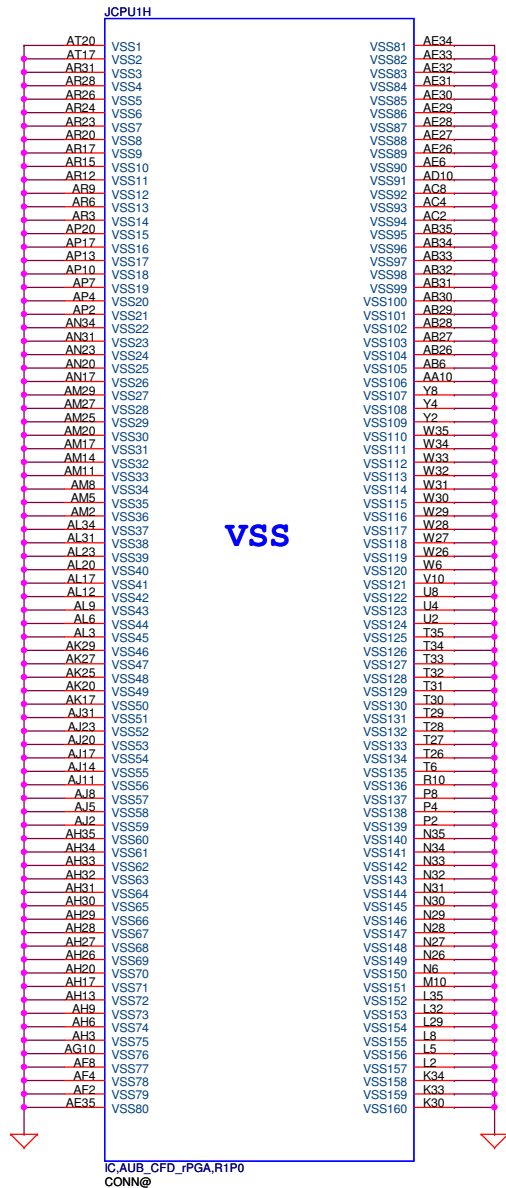
	C, uF	ESR, mohm	Stuffing Option
+CPU-CORE Decoupling	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

IC_AUB_CFD_PGA_R1P0
CONN@

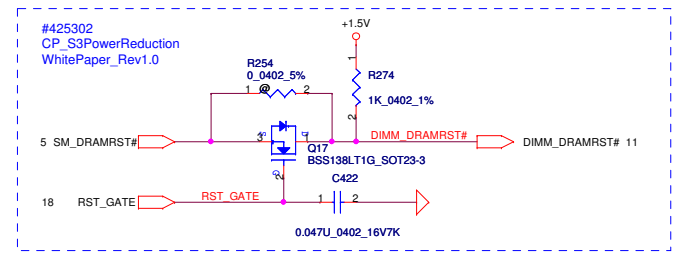
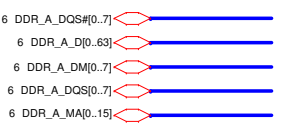
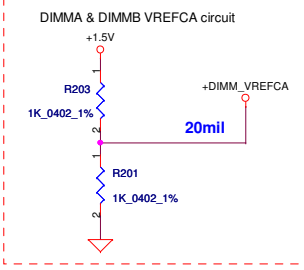
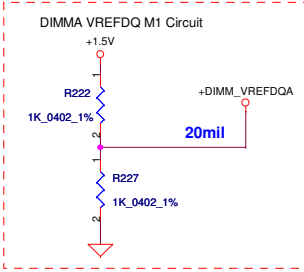
Security Classification	Compal Secret Data		Title	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	PROCESSOR (4/6) PWR, Bypass
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Customer: NEW70 M/B LA-5891P Schematic				Rev 1.0
Date: Tuesday, December 29, 2009				Sheet 7 of 59



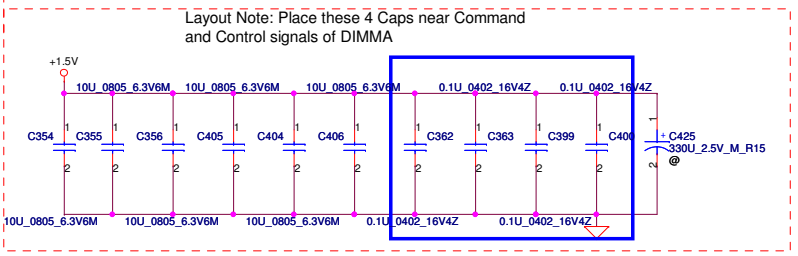
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Customer		Rev	
	NEW70 M/B LA-5891P Schematic			1.0	
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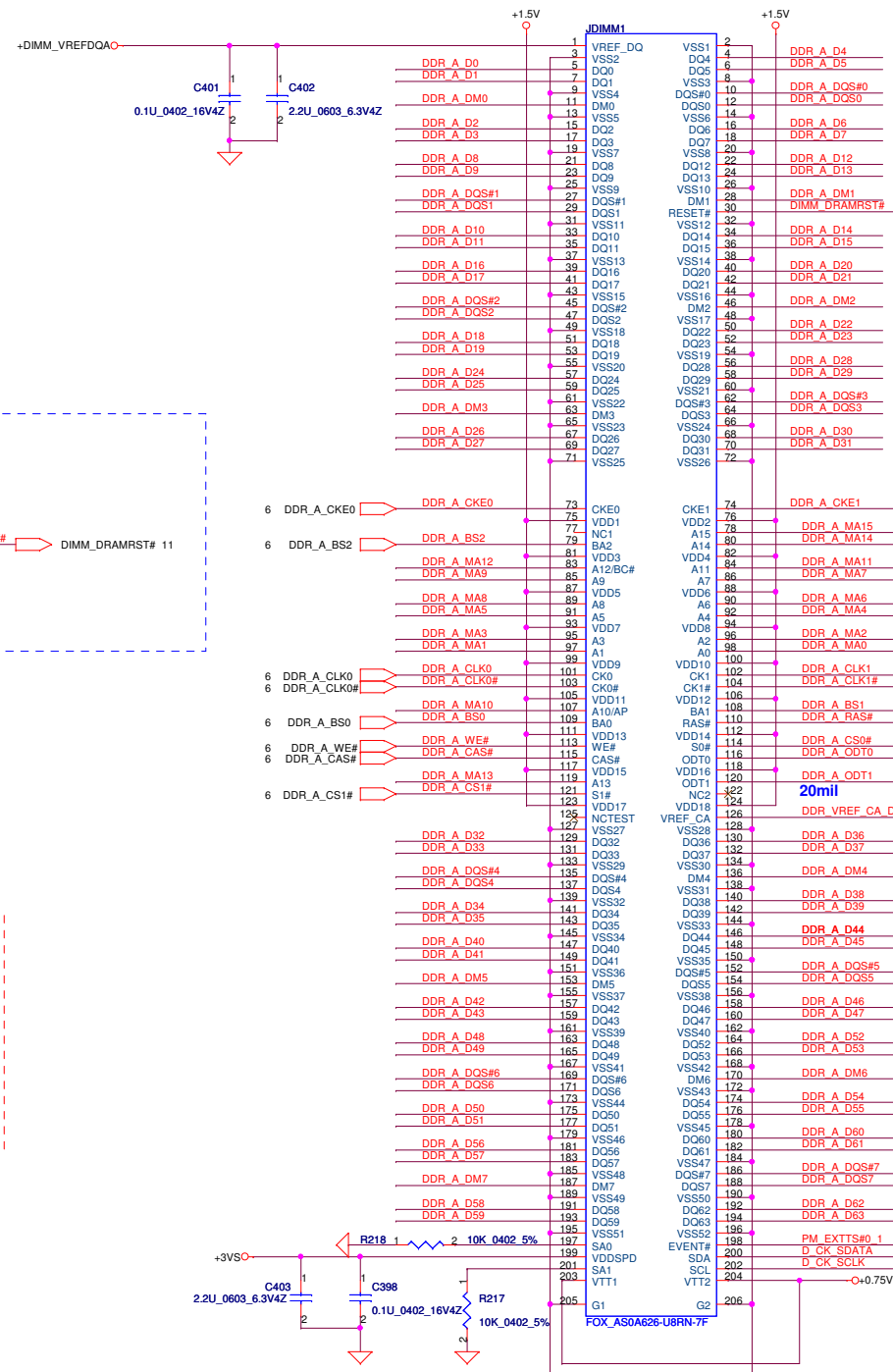
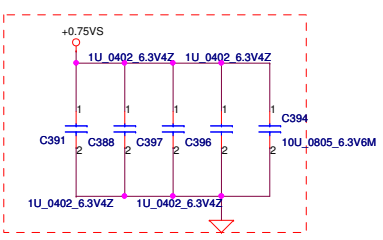
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Date		Sheet	Rev
Customer	NEW70 M/B LA-5891P Schematic	Tuesday, December 29, 2009		9	1.0
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Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



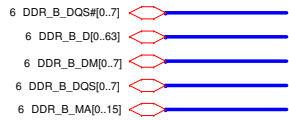
DDR3 SO-DIMM A H=8mm

Compal Electronics, Inc.

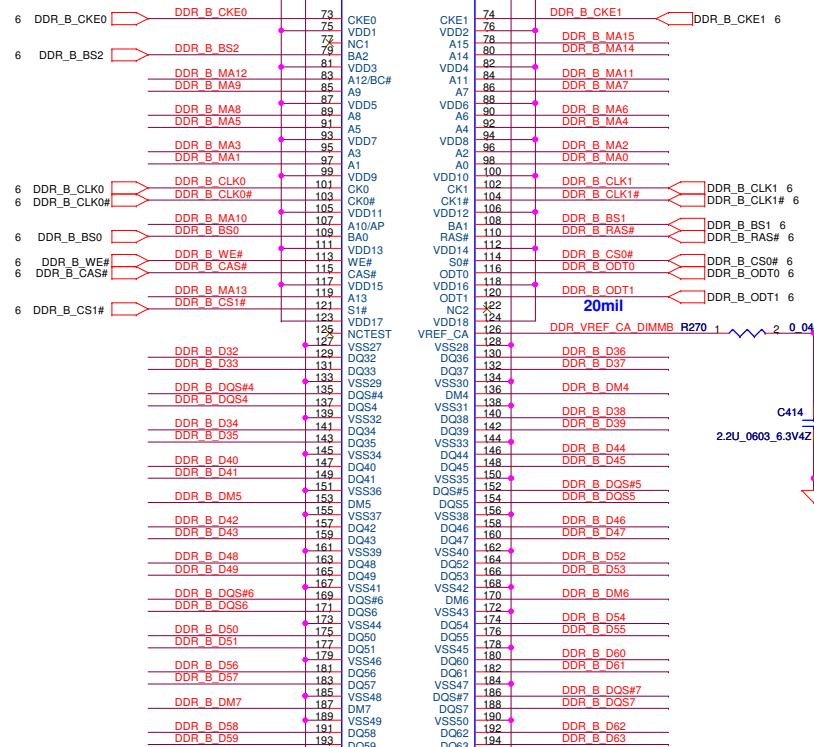
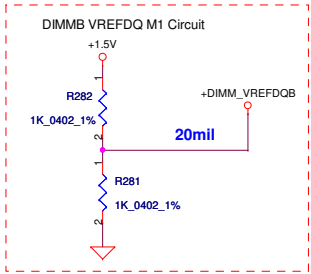
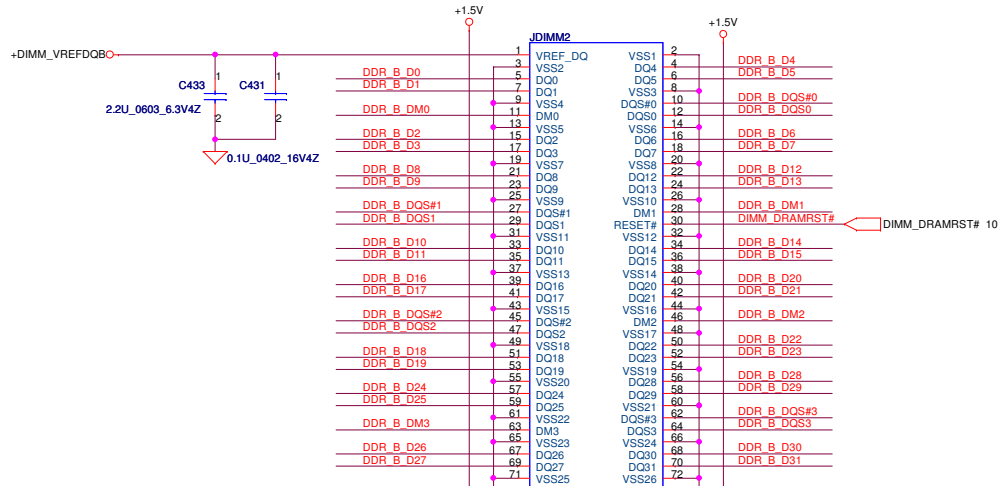
Security Classification	Compal Secret Data	
Issued Date	2009/08/01	Deciphered Date
		2010/08/01

Title	Document Number	Rev
DDRIII-SODIMM SLOT1	NEW70 M/B LA-5891P Schematic	1.0

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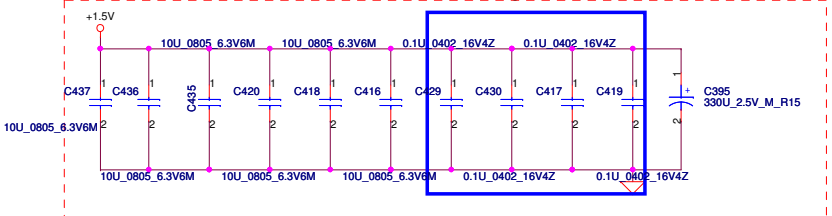


2008/9/8 #400755
 Calpella Clarkfield
 DDR3 SO-DIMM
 VREFDQ Platform
 Design Guide Change Details

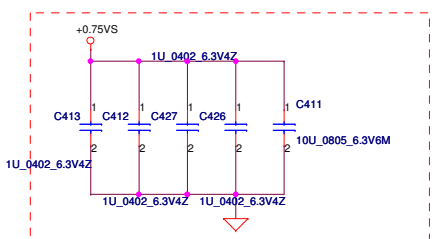


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



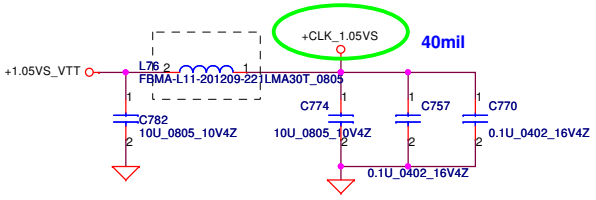
Layout Note:
Place near JDIMM2.203 & JDIMM2.204



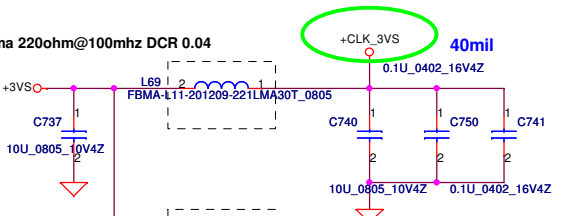
DDR3 SO-DIMM B
H=4mm

Security Classification	Compal Secret Data		Title	DDRIII-SODIMM SLOT2
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Document Number
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			Date:	Tuesday, December 29, 2009
			Sheet	11 of 59

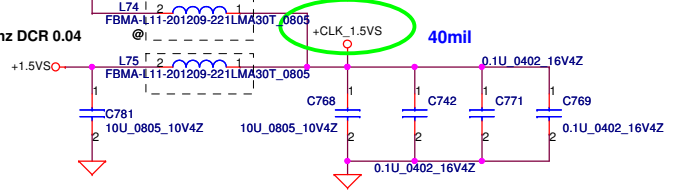
SM010014520 3000ma 220ohm@100mhz DCR 0.04



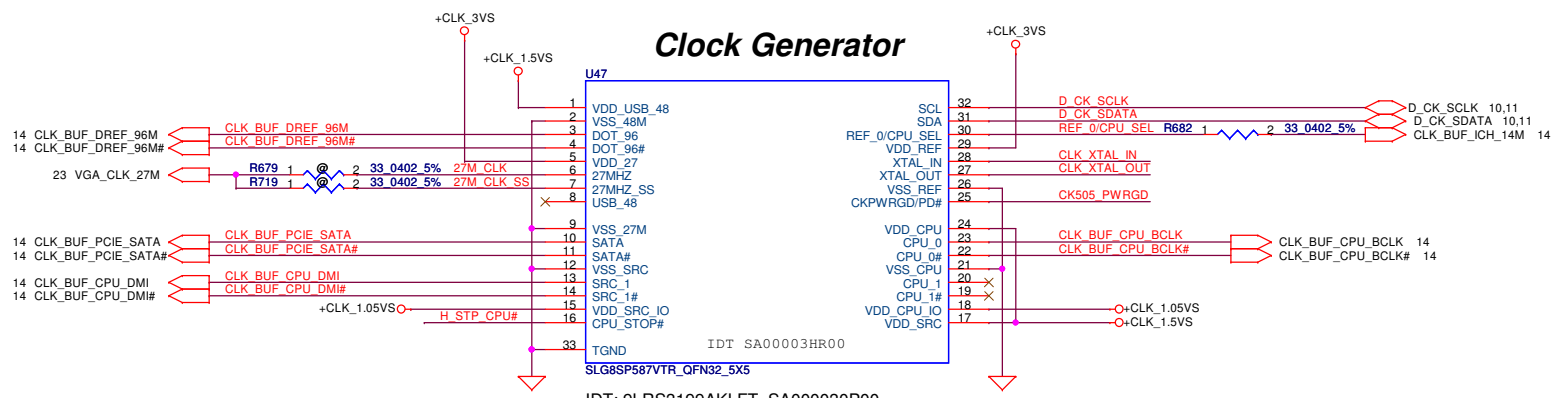
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04

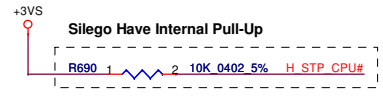


Clock Generator

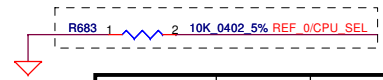


IDT: 9LRS3199AKLFT, SA00003P00
 SILEGO: SLG8SP587V(WF), SA00002XY10
 Low Power:
 IDT: 9LVS3199AKLFT, SA00003HR00
 Realtek: RTM890N-631-VB-GRT, SA00003HQ10

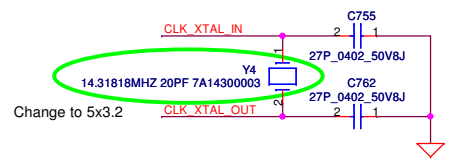
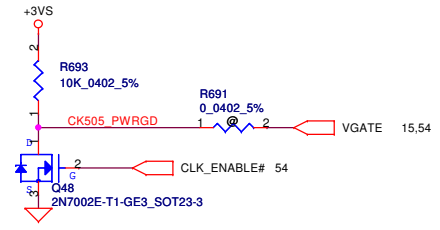
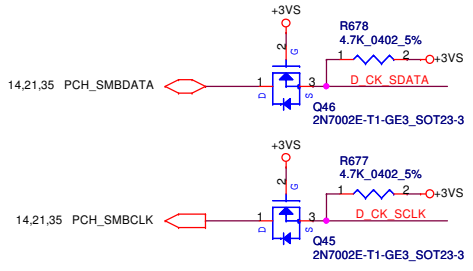
IDT 9LVS3199AKLFT NC



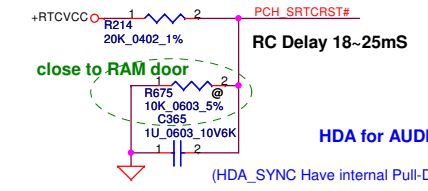
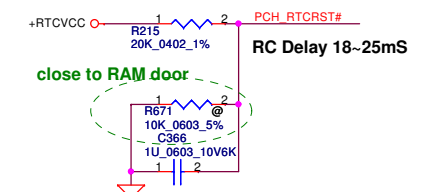
IDT Have Internal Pull-Down FOR Realtek



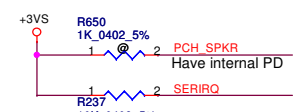
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



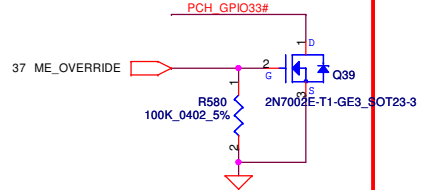
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Size	Document Number	Customer		Rev	
	NEW70 M/B LA-5891P Schematic			1.0	
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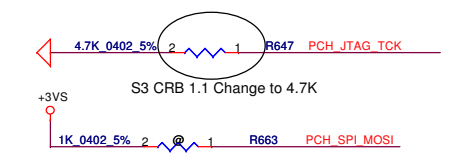
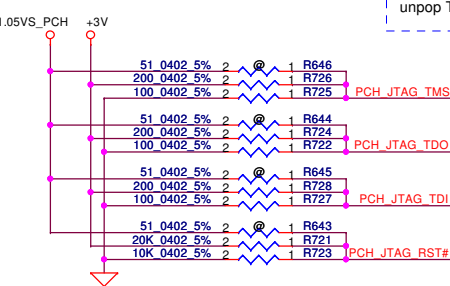
HDA_SYNC
On Die PLL VR is supplied by 1.5V when sampled High, 1.8V when sampled Low.



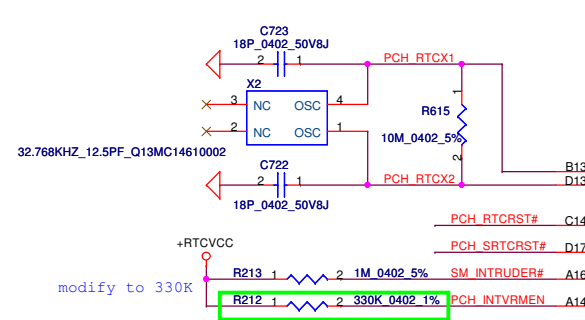
If GPIO33 pull down, ME will not working. For factory update ME, pull down resistor pull under door.



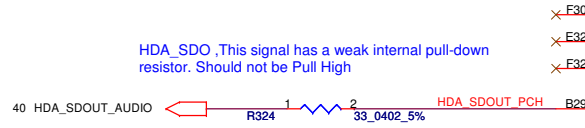
GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.



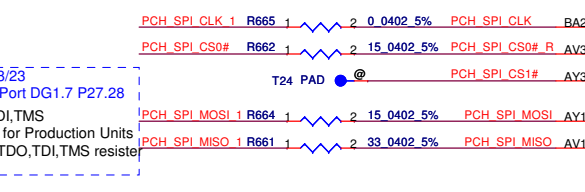
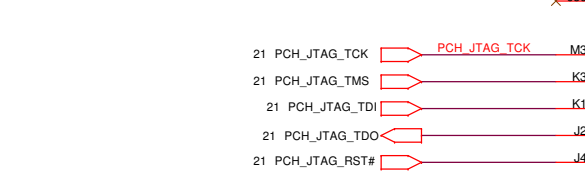
enable iTPM: SPI_MOSI High
MOSI This signal has a weak internal pull-down resistor. This signal must be sampled low.



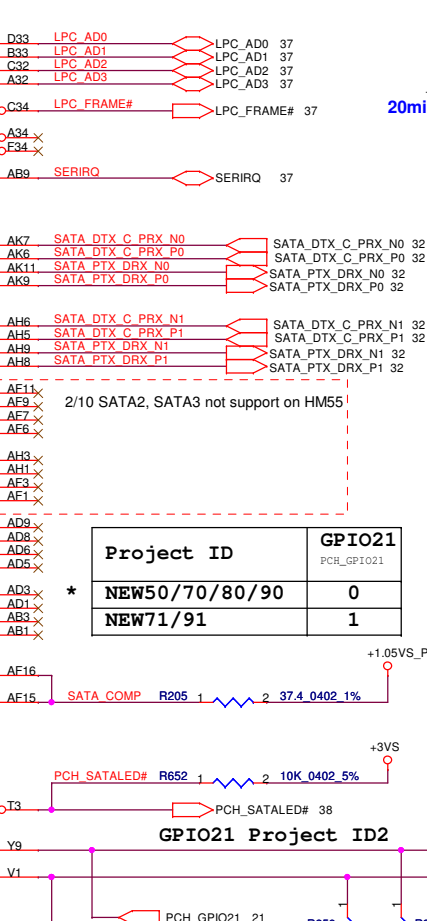
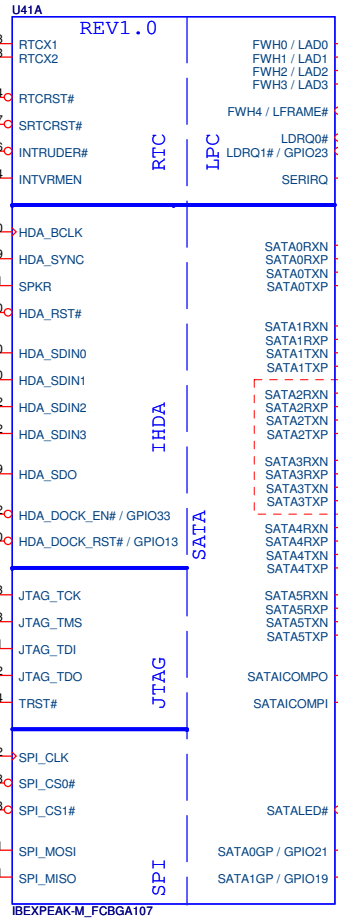
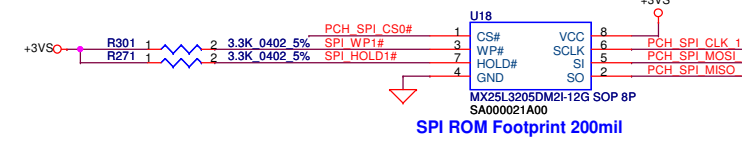
INTVRMEN - Integrated SUS 1.05V VRM Enable High - Enable Internal VRs
modify to 330K
R212 1 2 330K 0402 1%
PCH_INTRUDER# A16
PCH_INTVRMEN A14



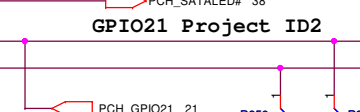
HDA_SDO ,This signal has a weak internal pull-down resistor. Should not be Pull High
GPIO33 can not pull down (manufacturing environments)



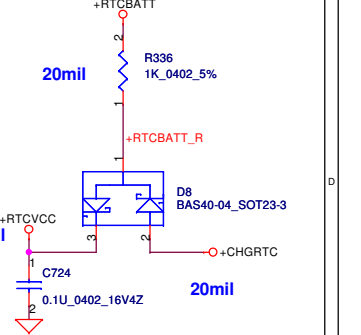
2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R724, R722 on ES2 Sample
MP mount R646, R644, R645, R643 and remove others



Project ID	GPIO21
NEW50/70/80/90	0
NEW71/91	1



	GPIO19	GPIO37
dGPU	0	0
iGPU	0	1
SG	1	X



For PCIE LAN

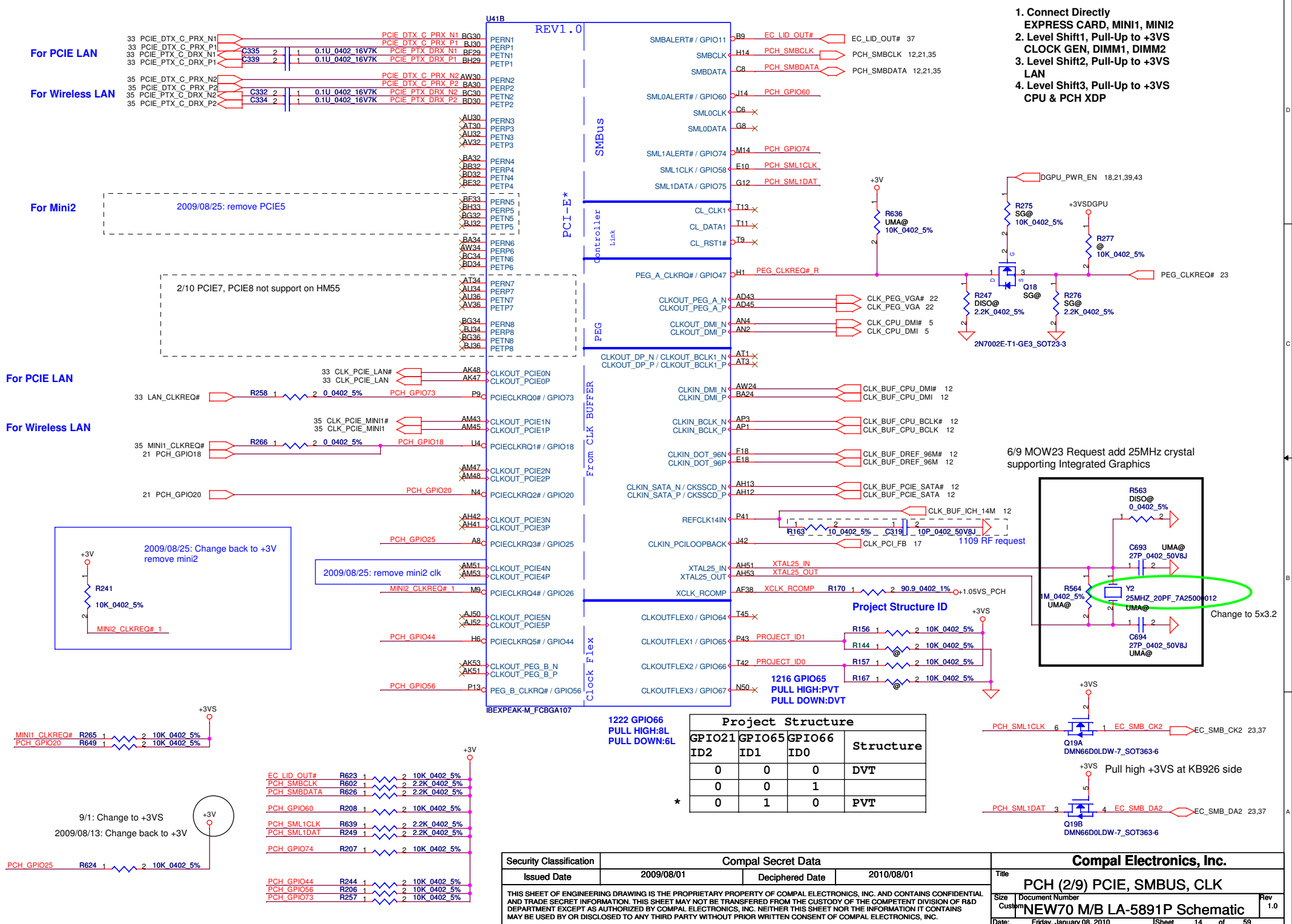
For Wireless LAN

For Mini2

For PCIE LAN

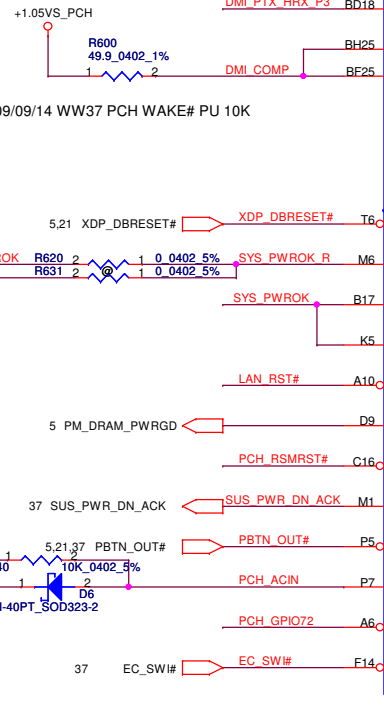
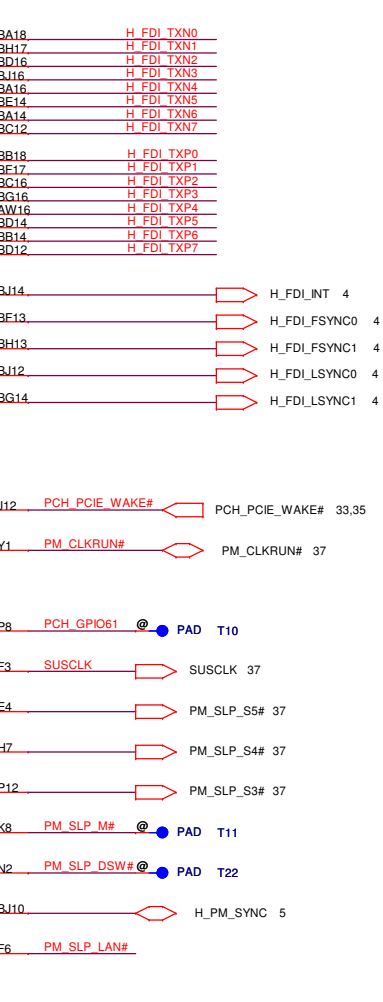
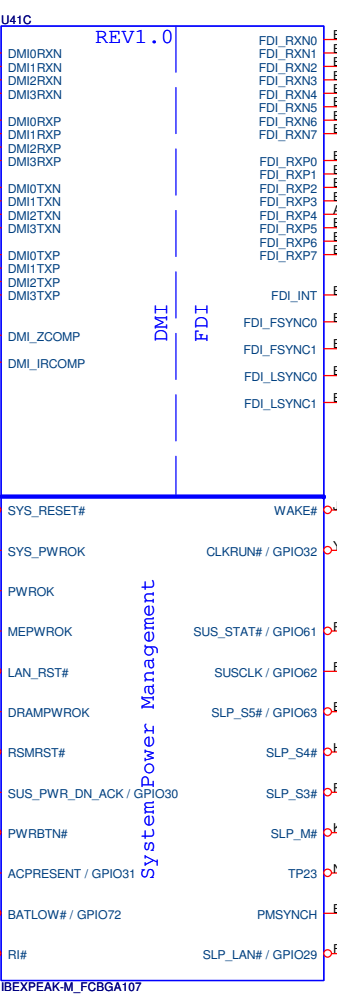
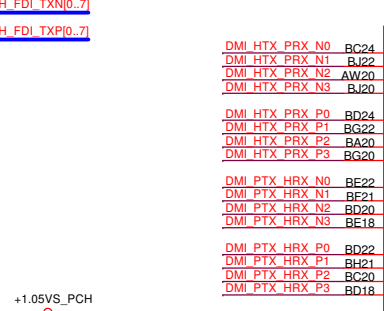
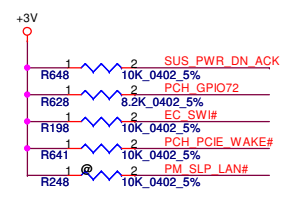
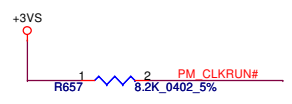
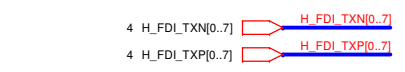
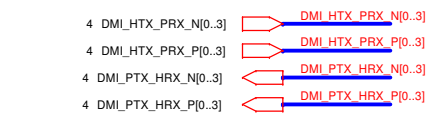
For Wireless LAN

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

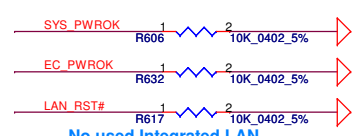
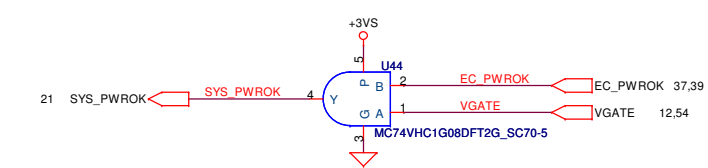


Project Structure			
GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	DVT
0	0	1	PVT
0	1	0	PVT

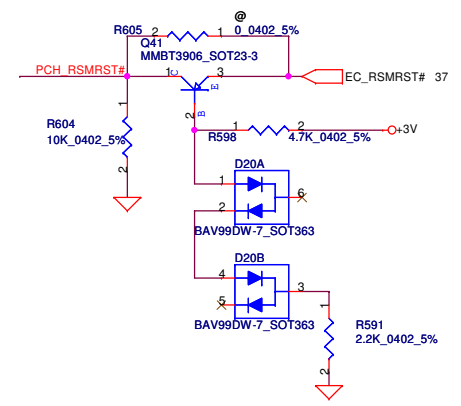
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Size	Document Number	Customer		Date		Rev	
	NEW70 M/B LA-5891P Schematic	Friday, January 08, 2010		Sheet 14 of 59		1.0	



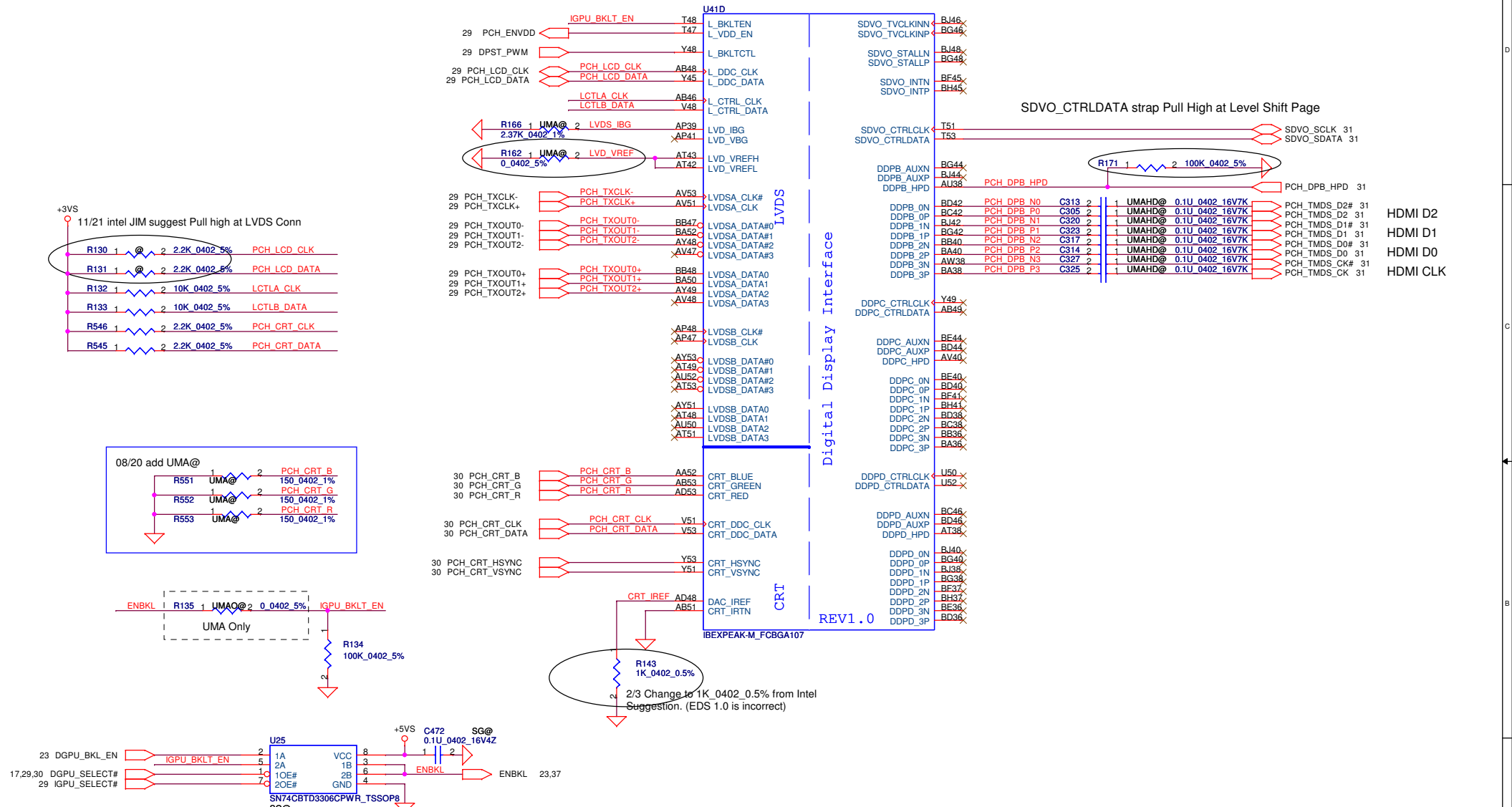
System Power Management



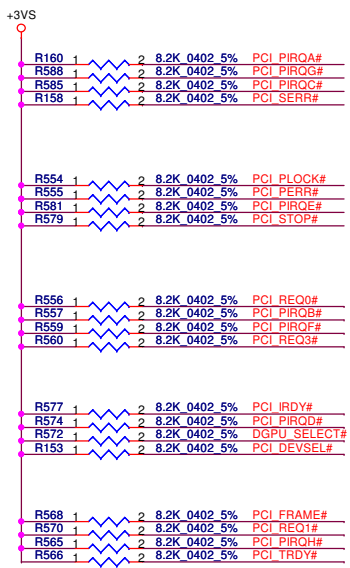
No used Integrated LAN,
 connecting LAN_RST# to GND



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	NEW70 M/B LA-5891P Schematic			1.0	
Date:	Tuesday, December 29, 2009	Sheet	16	of 59	



PCI_GNT0#, PCI_GNT1#, PCI_GNT2#, PCI_GNT3# has a weak internal pull-up

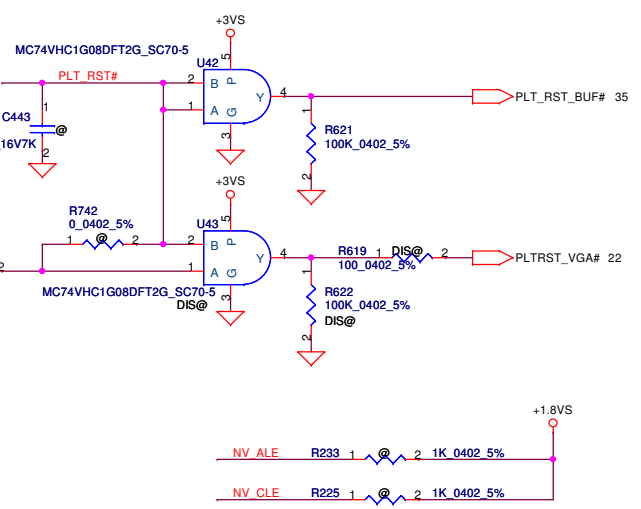
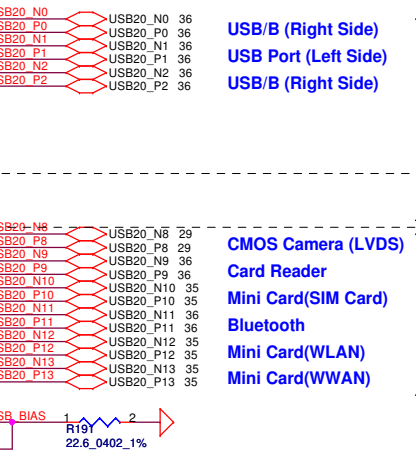
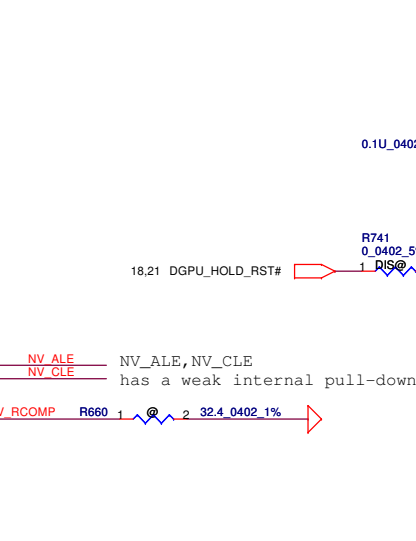
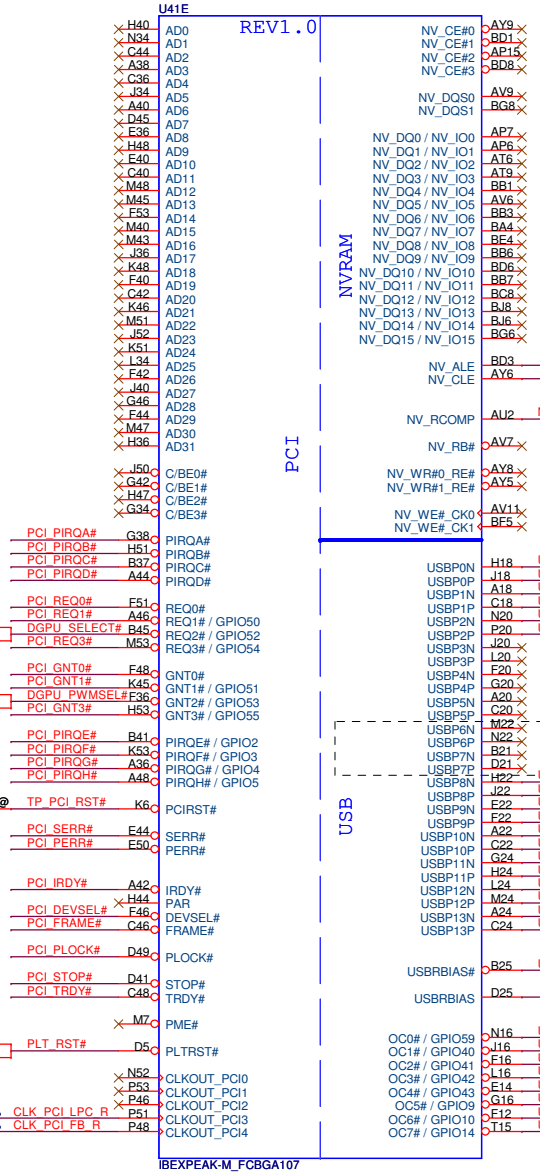
PCI_GNT2# ESI Strap (Server Only) this signal should not be pulled low

2008/1/6 2009MOW01 change to 22 ohm

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

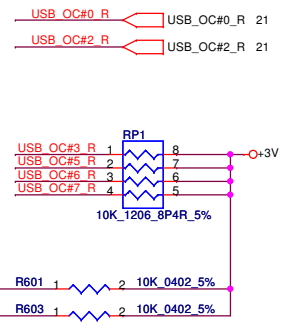
A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled
High=Default *



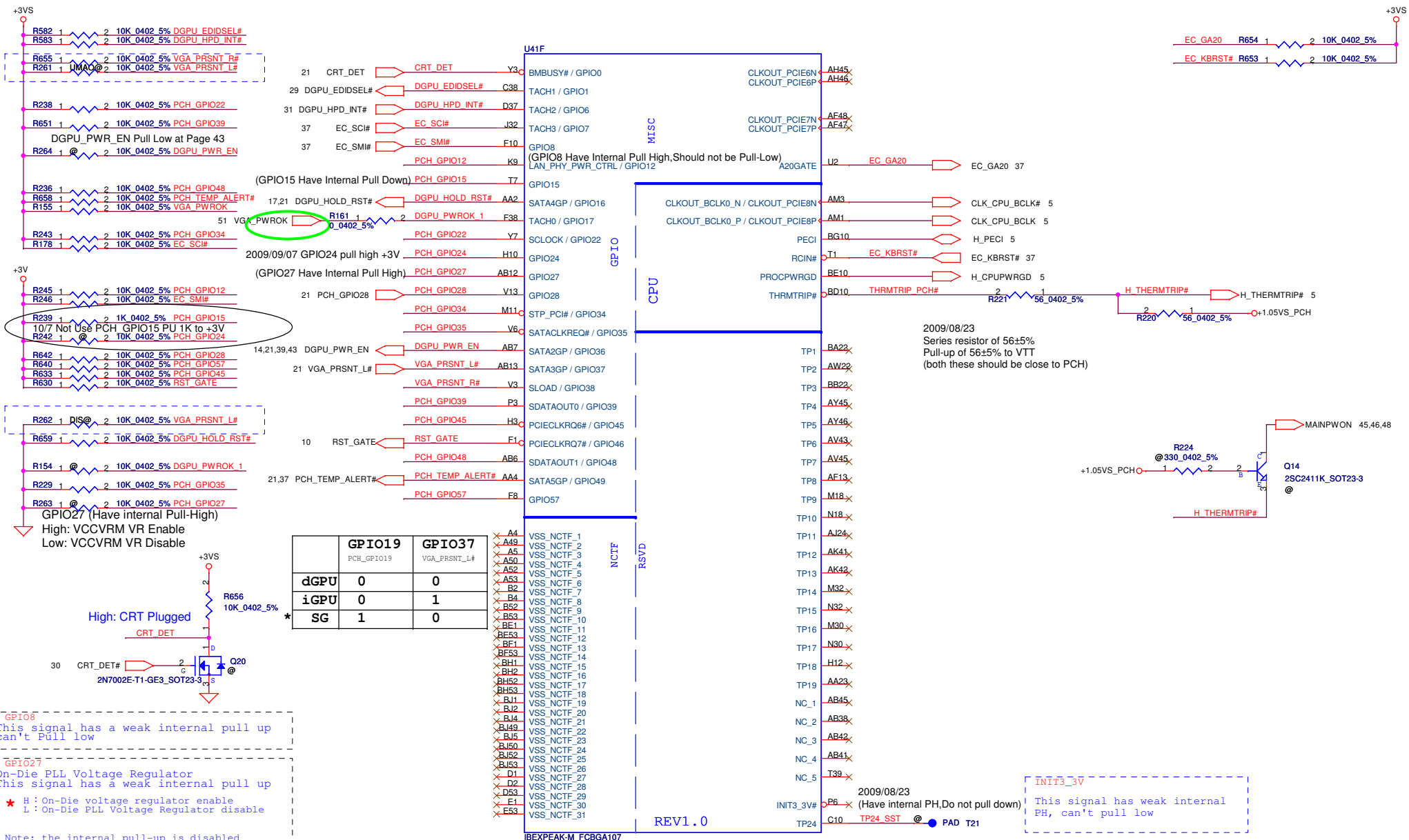
Intel Anti-Theft Technology	
NV_ALE	High=Enabled Low=Disable(floating) *
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH Set to Vss when LOW

NV_ALE Enable Intel Anti-Theft Technology : 8.2K PU to +3VS
Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE DMI termination voltage. weak internal PU, don't PD



OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	PCH (5/9) PCI, USB, VRAM	
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	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSN_T_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO8
This signal has a weak internal pull up can't Pull low

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

- H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts.
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

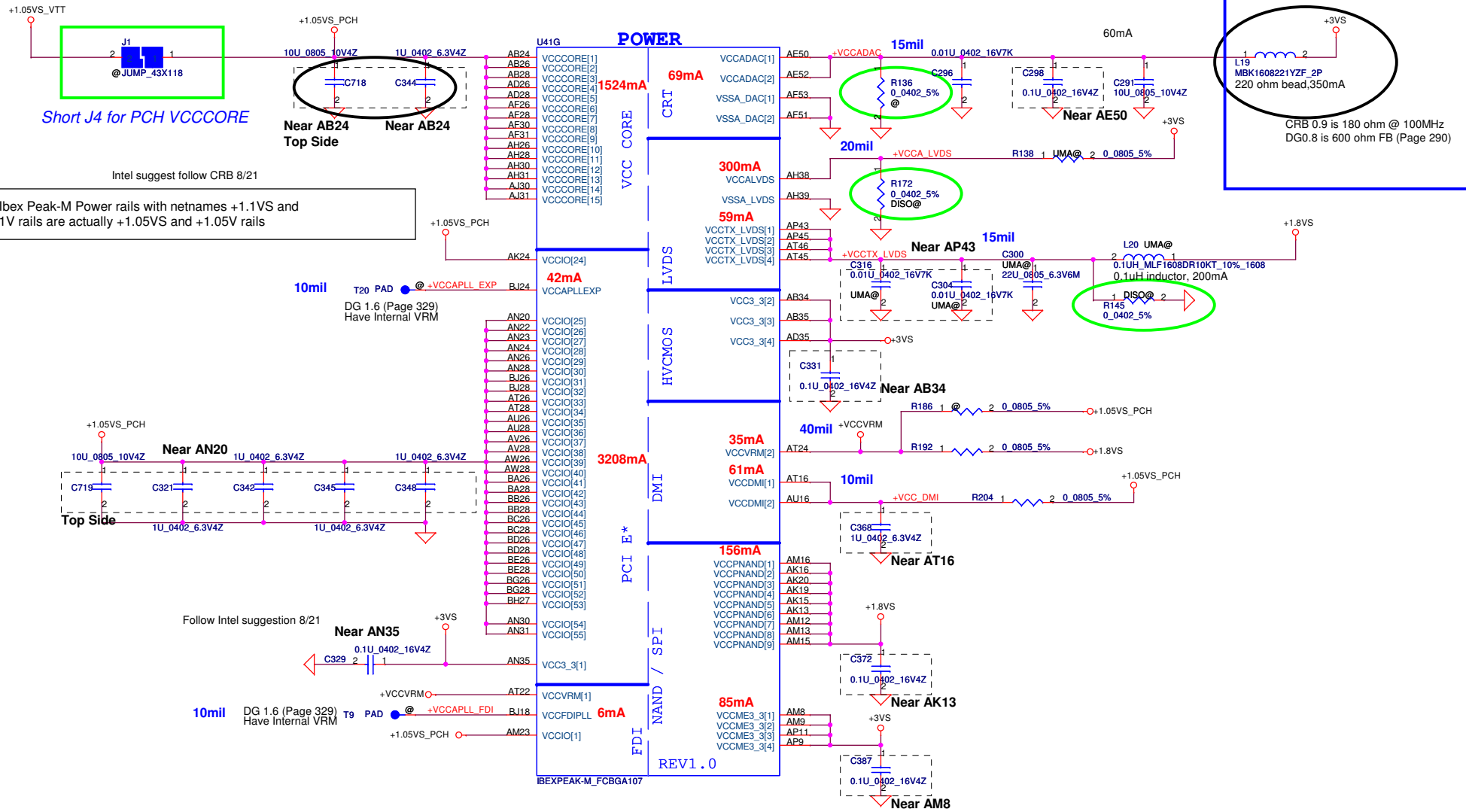
GPIO15

- L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
- H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

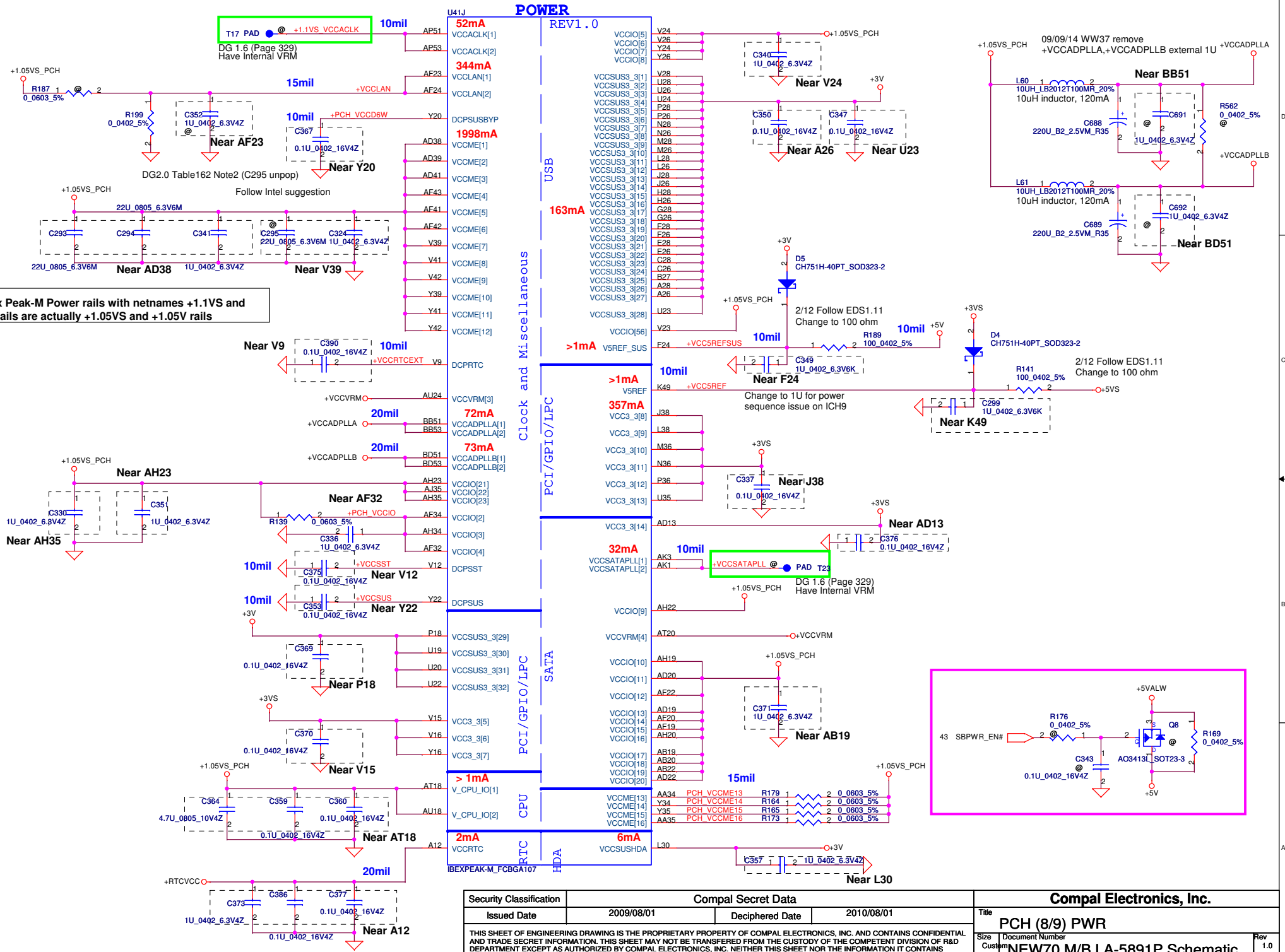
INIT3_3V
This signal has weak internal PH, can't pull low

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	PCH (6/9) GPIO, CPU, MISC	
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Size	Document Number	Date		Sheet	Rev
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				Sheet	of
				18	59







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Date:	Tuesday, December 29, 2009	Sheet	19	of	59

All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

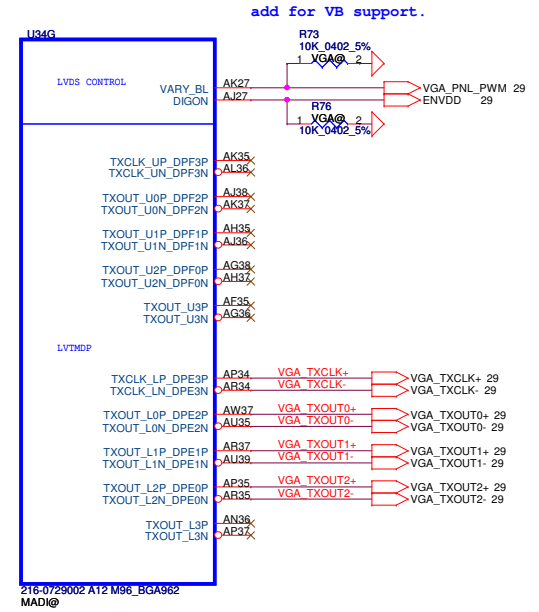
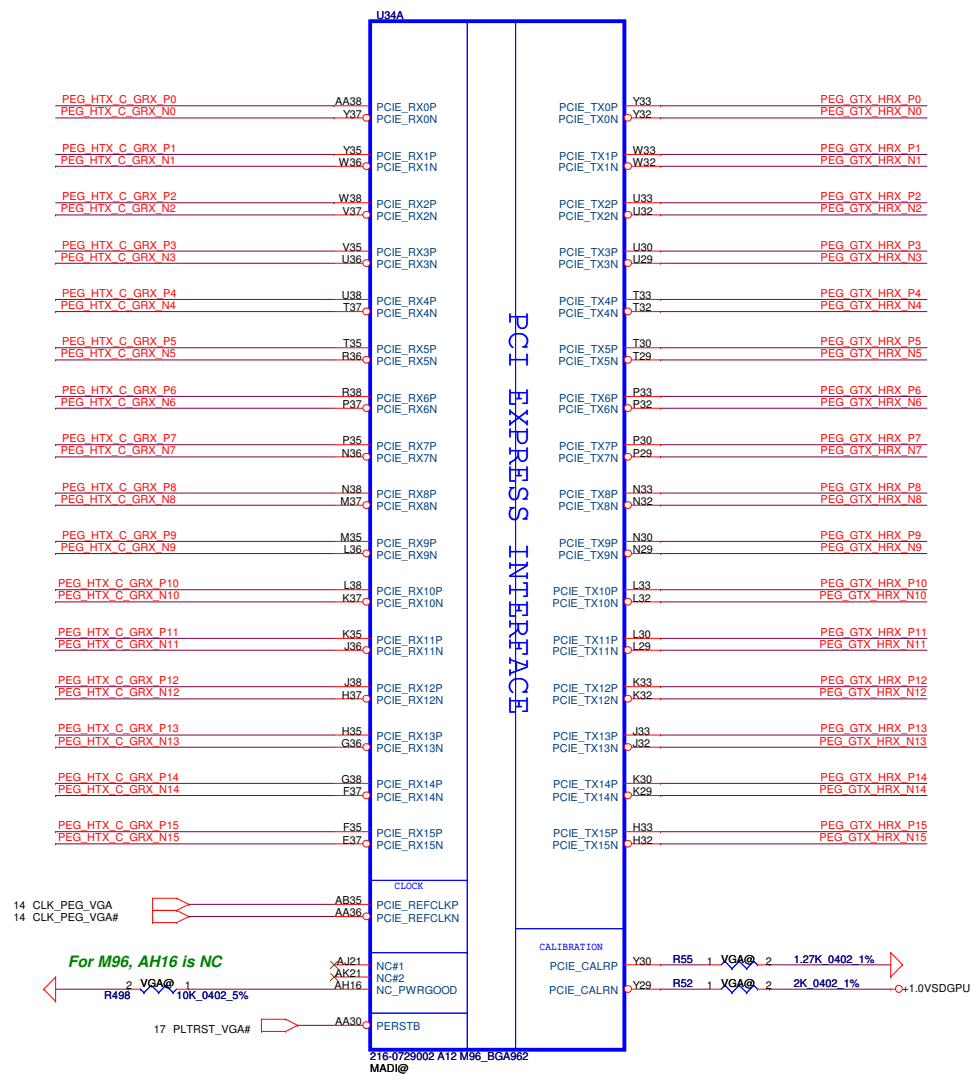


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Title: PCH (8/9) PWR			
Size	Document Number	Rev	
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4 PEG_GTX_HRX_N[0..15] 
 4 PEG_GTX_HRX_P[0..15] 
 4 PEG_HTX_C_GRX_N[0..15] 
 4 PEG_HTX_C_GRX_P[0..15] 

GFX PCIE LANE REVERSAL

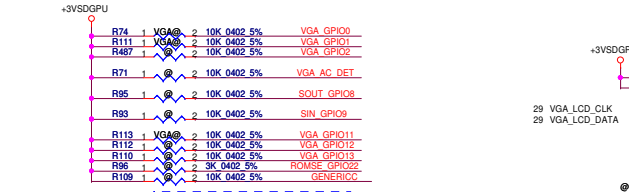


add for VB support.

Park XT P/N : SA00003M500 (S IC 216-0774009 A11 PARK XT S3 631P C38)
 Madison Pro P/N : SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)

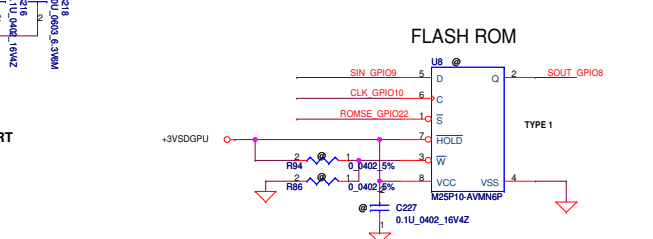
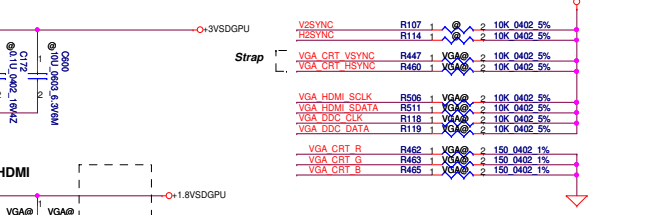
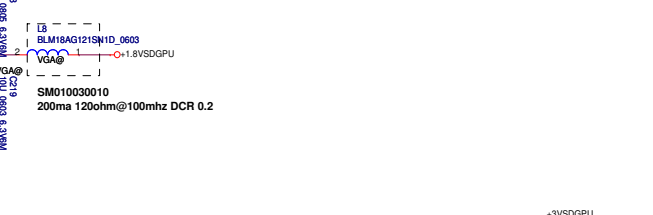
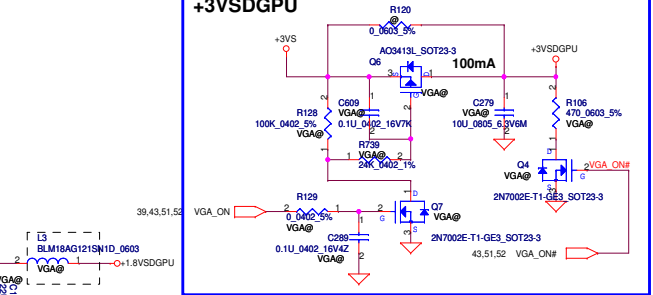
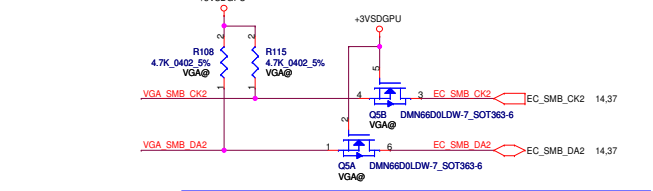
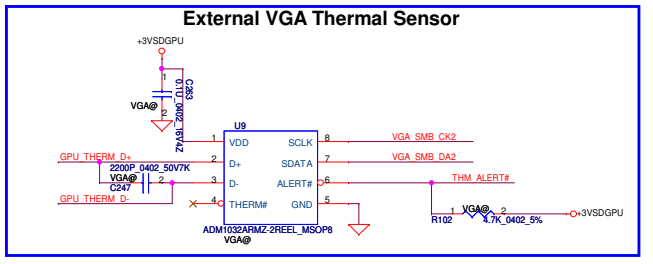
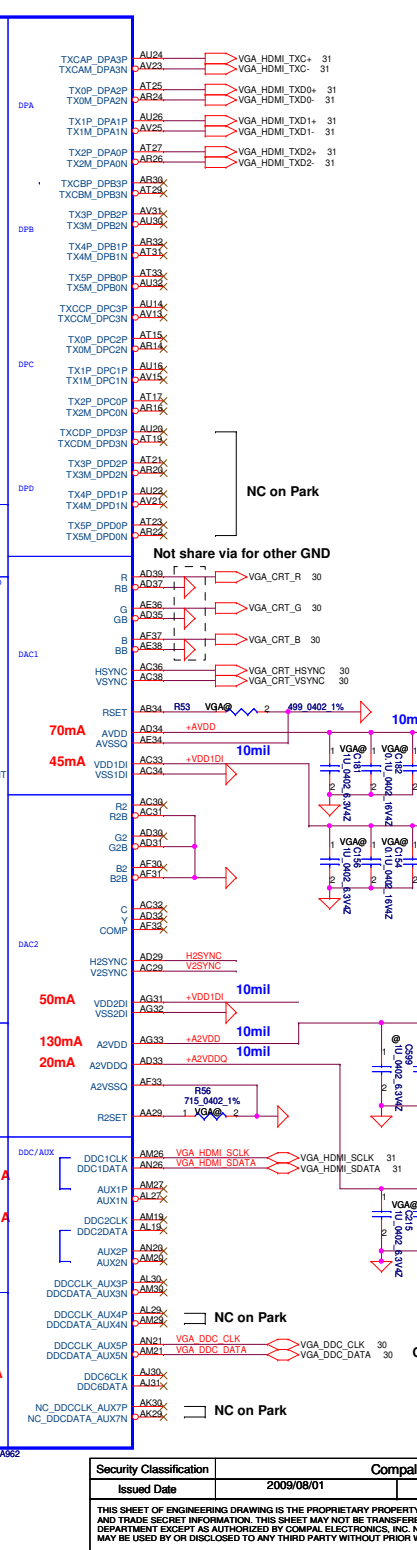
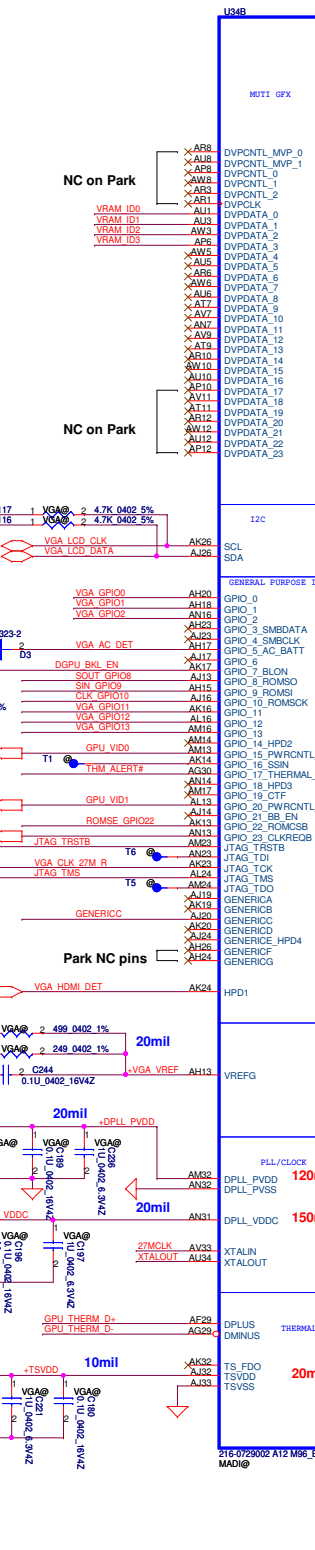
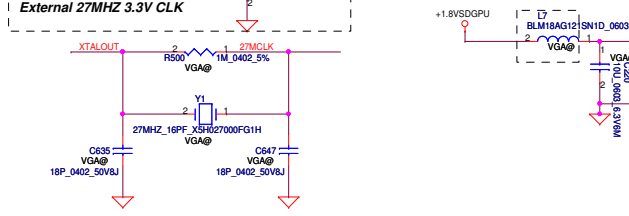
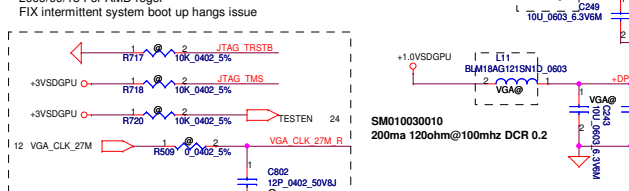
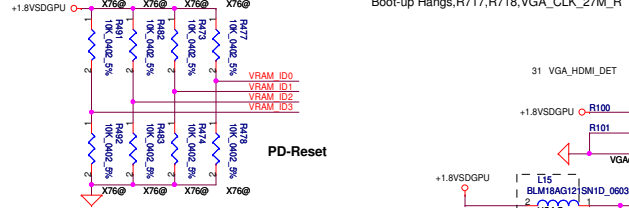
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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 [config 2,1,0]: a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. memory apertures CONFIG[2:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	



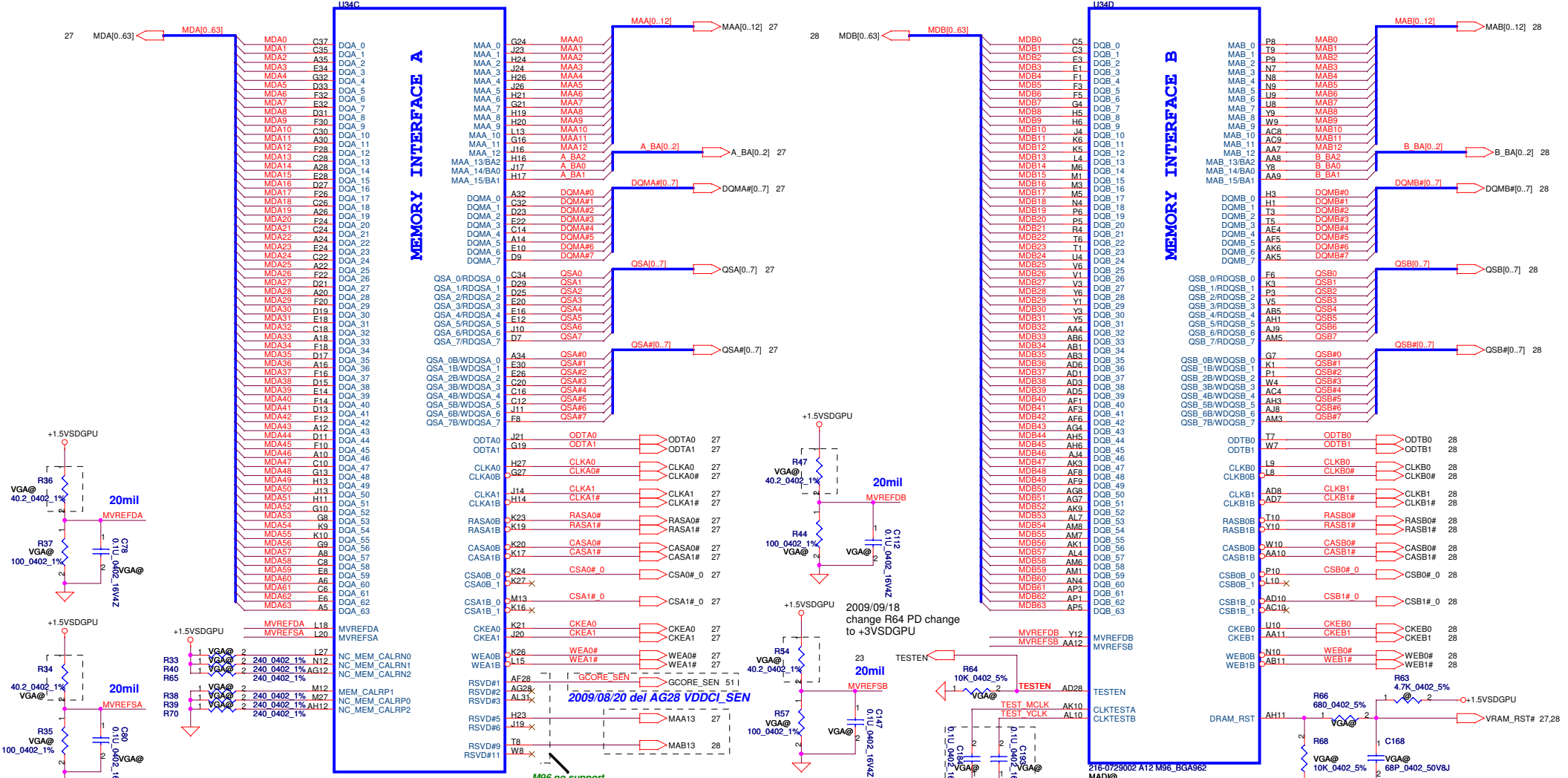
Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM	64Mx16	64Mx16	0	0
Samsung	<4PCS>			
HYNIX	1	<4PCS>	0	0
AMD		<4PCS>	1	0

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM	64Mx16	64Mx16	0	0
Samsung	0	<8PCS>	0	0
HYNIX	1	<8PCS>	0	0
AMD		<8PCS>	1	0



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Compal Electronics, Inc.		NEW70 M/B LA-5891P Schematic	
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Park is single channel for memory (channel B only)



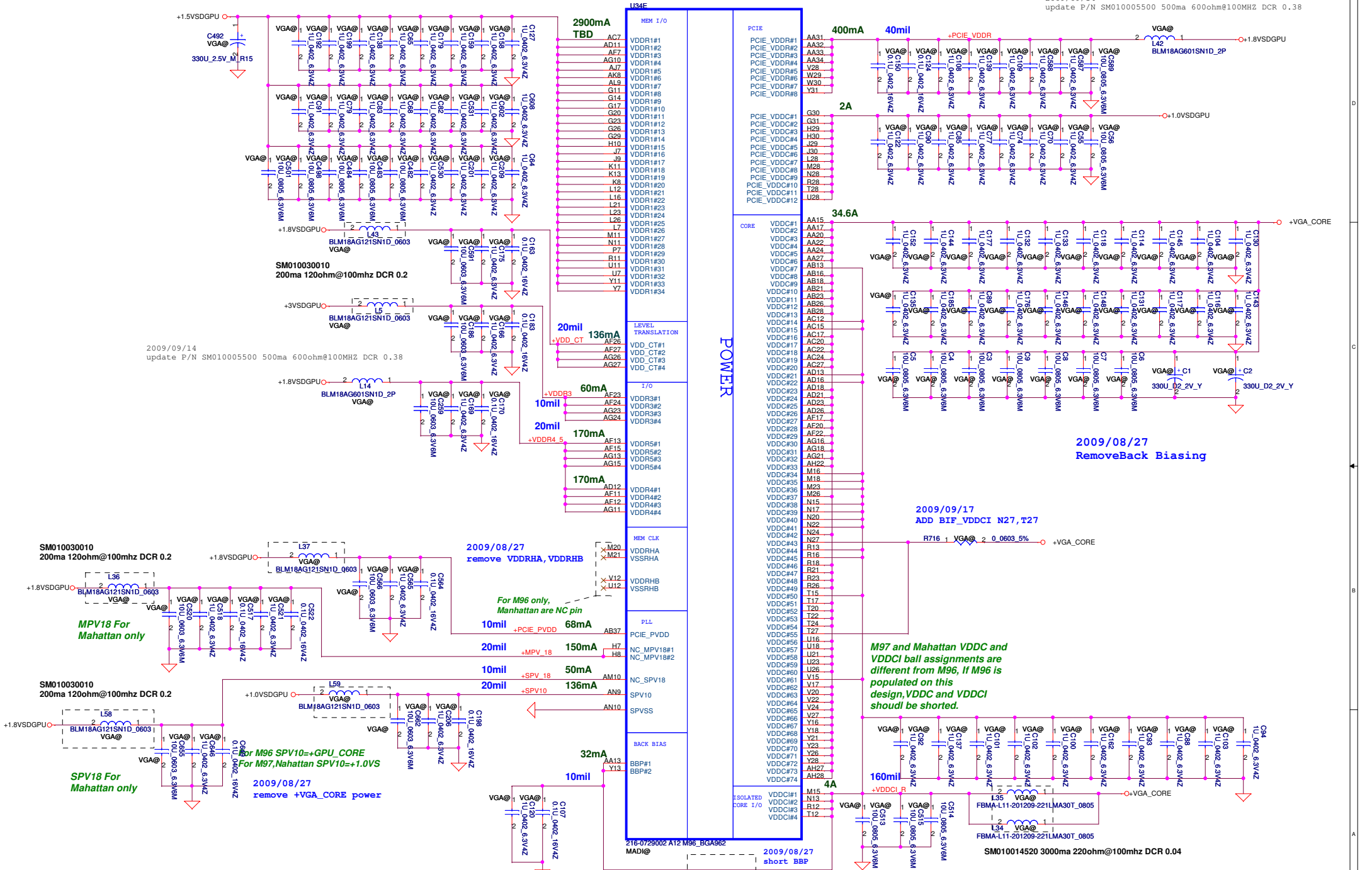
If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

In M97, Medison and Park, AF28 is FB_VDDC, AG28 is FB_VDDCI, AH29 is FB_GND. GCORE_SEN and FB_GND should route as differential pair Same as VDDCI_SEN and FB_GND

If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

M96 use 4.7K to PD directly.

	M96	Broadway
R228	4.7k Ohm	10k Ohm
	0 Ohm	SD028100280
R159	0 Ohm	SD02860080
	4.7k Ohm	SD02860080
R159	4.7k Ohm	DNI
	1000 pF	68 pF
C659	SE074102K80	SE071680J80



2009/09/14
update P/N SM01005500 500ma 600ohm@100MHZ DCR 0.38

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

Back Bias is not supported on M97, Broadway, Madison and Park Connect to VDDCI directly

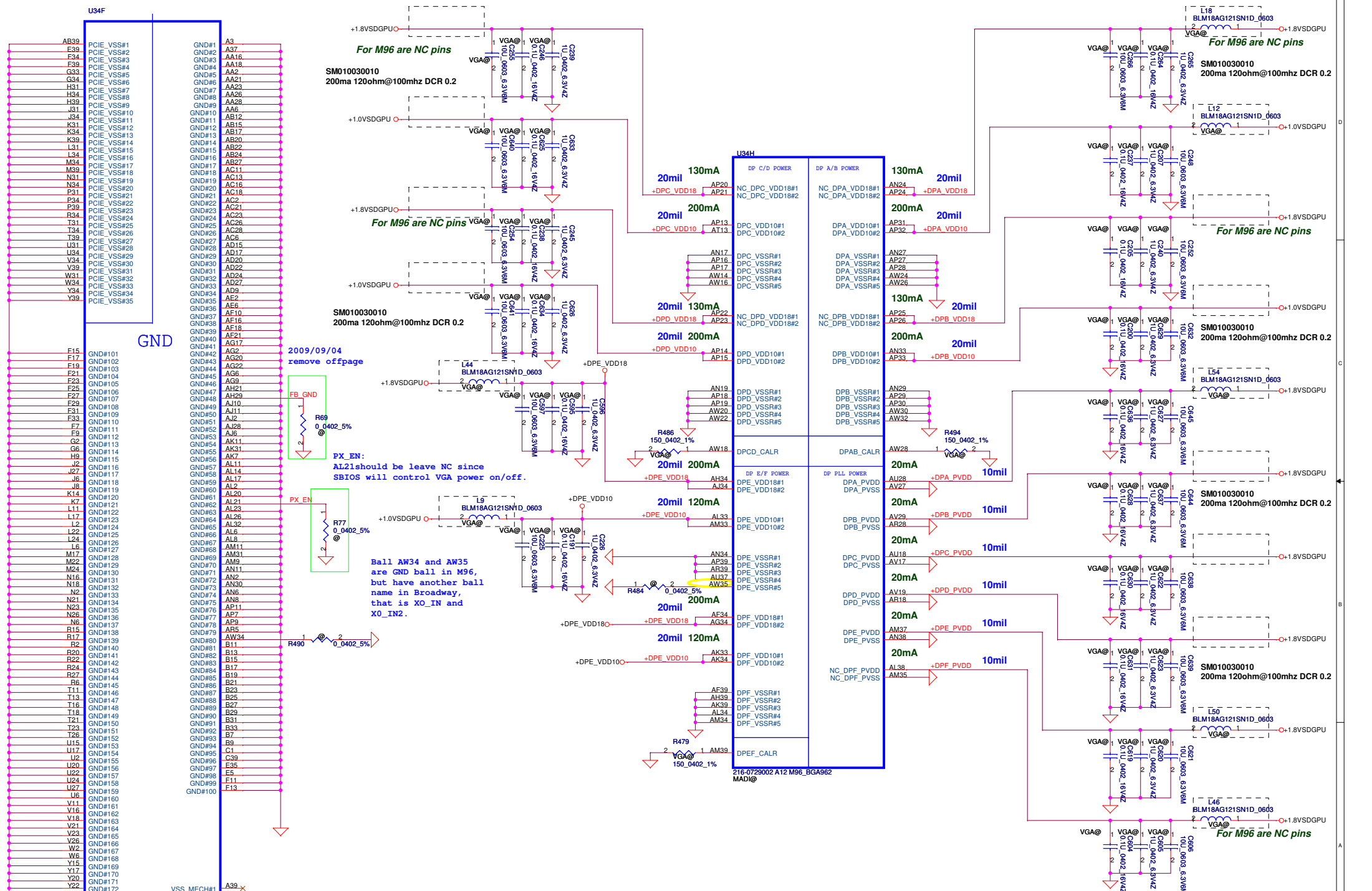
M97 and Mahattan VDDC and VDDCI ball assignments are different from M96, if M96 is populated on this design, VDDC and VDDCI should be shorted.

2009/08/27
RemoveBack Biasing

2009/09/17
ADD BIF_VDDCI N27, T27

2009/08/27
short BBP

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				M96 Power/GND	
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				Customer	Rev
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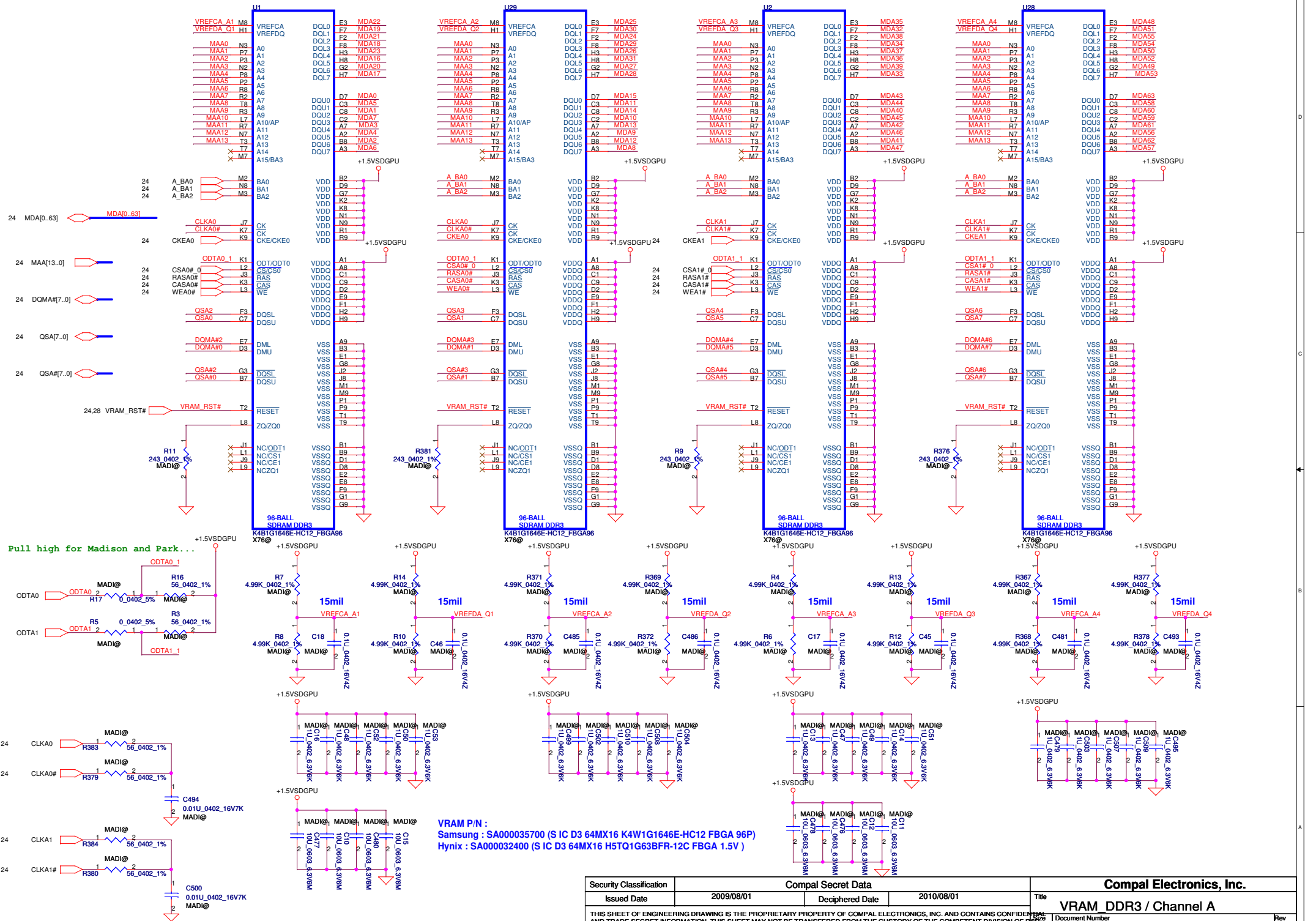


2009/09/04
remove offpage
FB GND

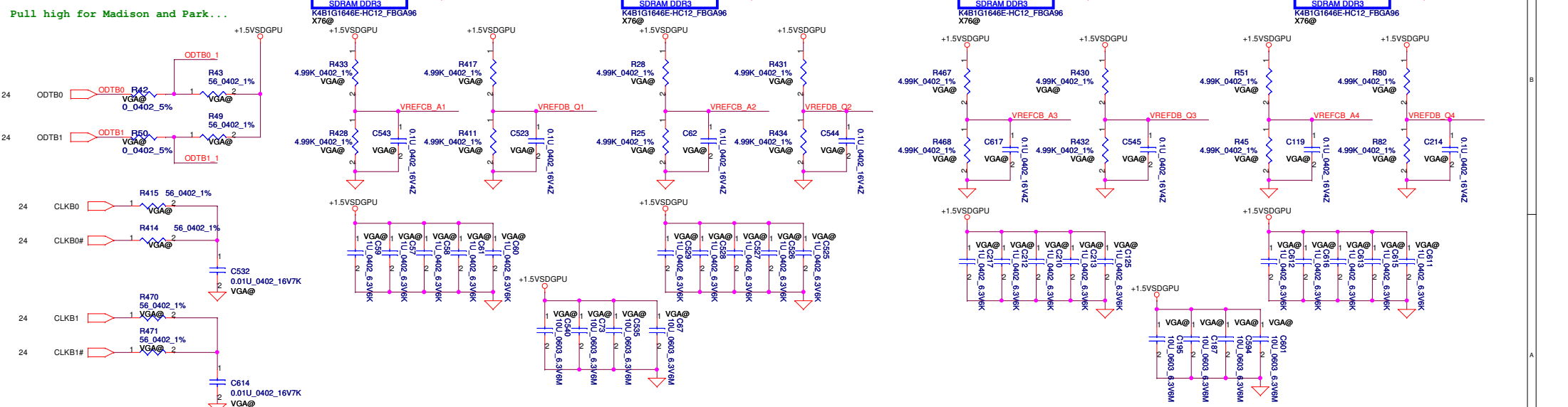
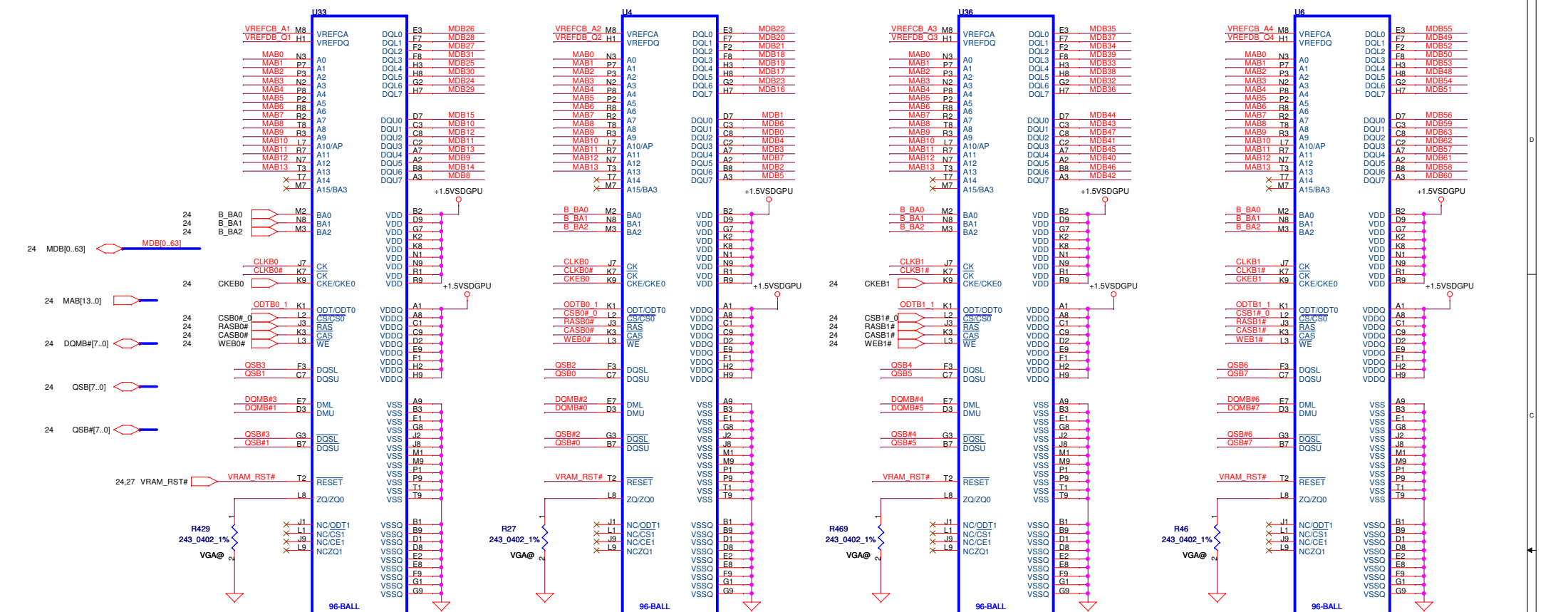
PX EN:
AL21 should leave NC since
SBIOS will control VGA power on/off.

Ball AW34 and AW35
are GND ball in M96,
but have another ball
name in Broadway,
that is XO_IN and
XO_IN2.

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				M96 Power/GND	
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Customer				Document Number	Rev
NEW70 M/B LA-5891P Schematic				1.0	
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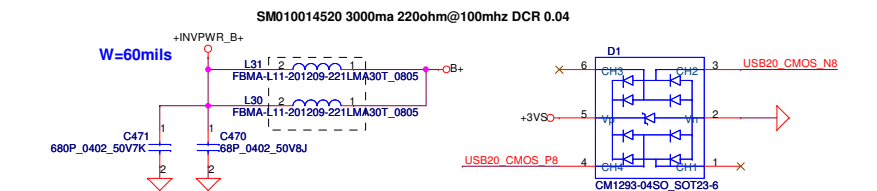
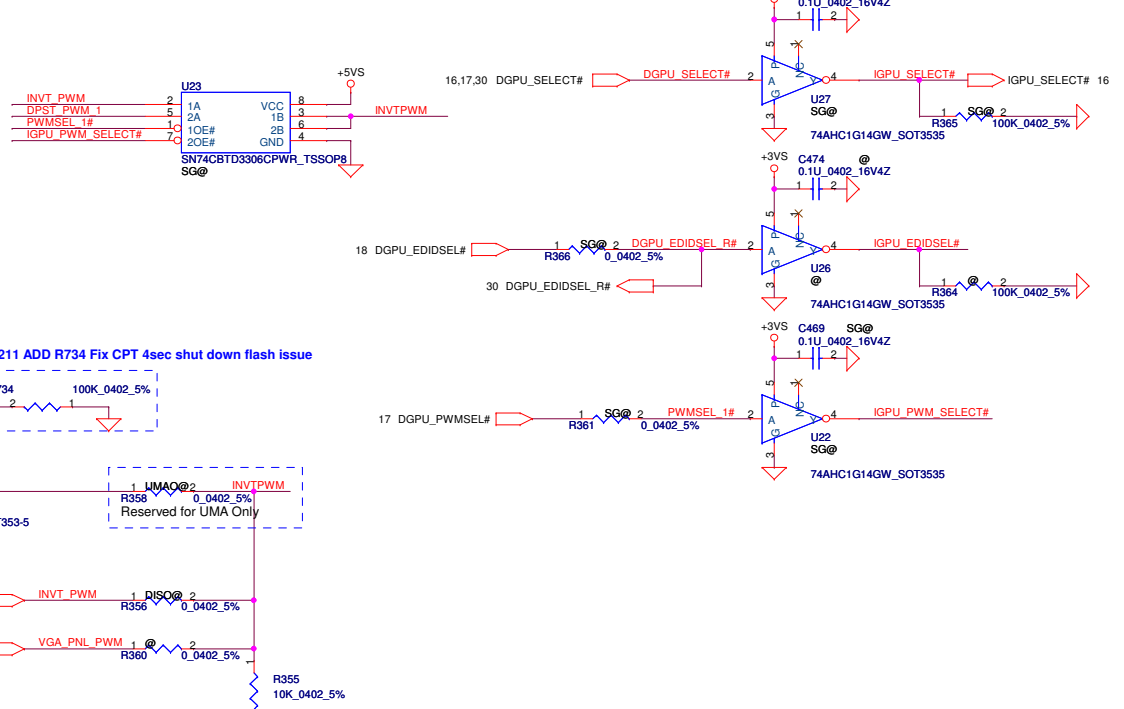
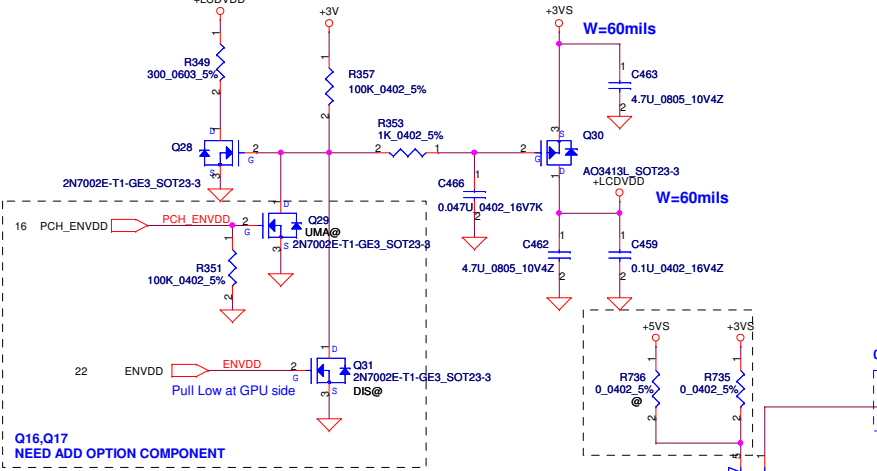
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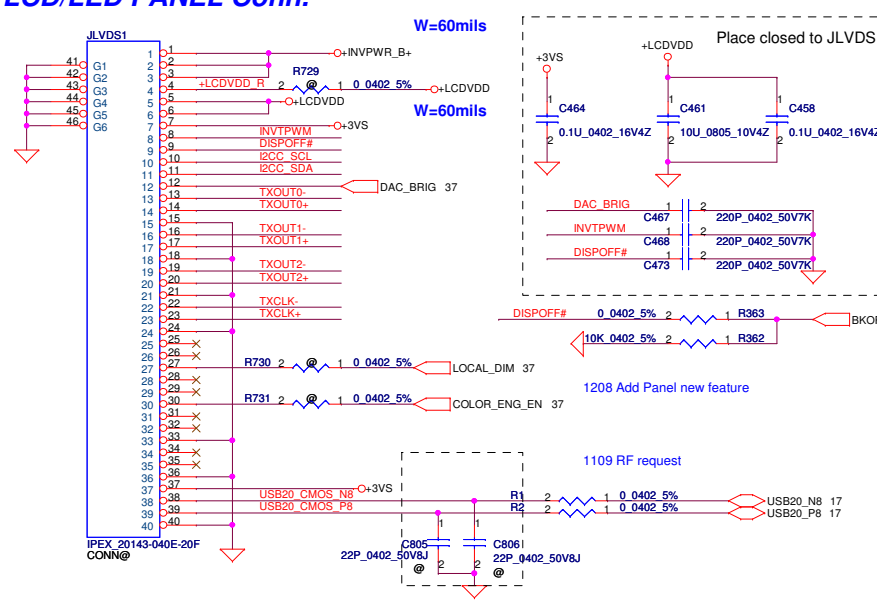
Pull high for Madison and Park...

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Customer: NEW70 M/B LA-5891P Schematic				Rev 1.0
Date: Tuesday, December 29, 2009				Sheet 28 of 59

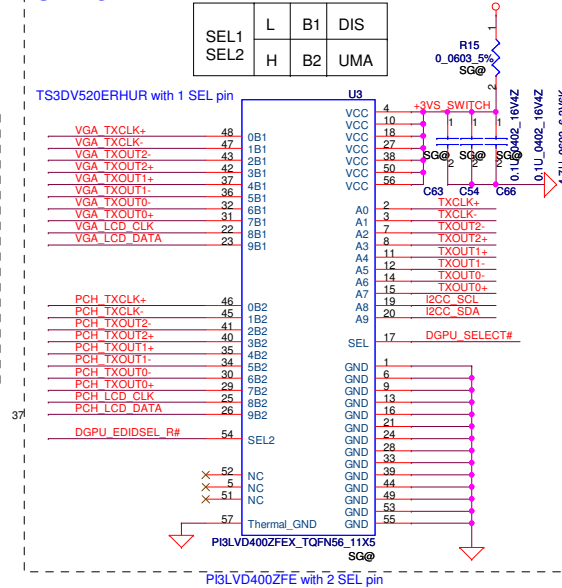
LCD POWER CIRCUIT



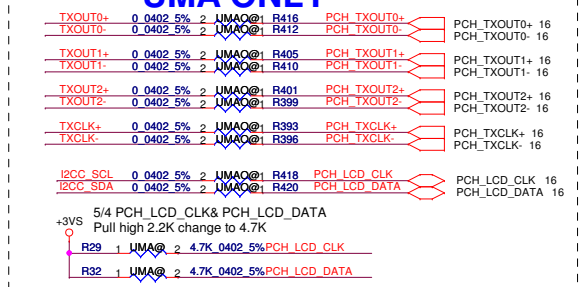
LCD/LED PANEL Conn.



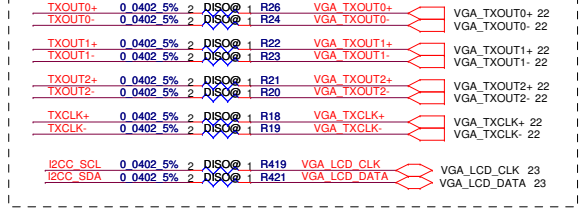
SWITCHABLE



UMA ONLY

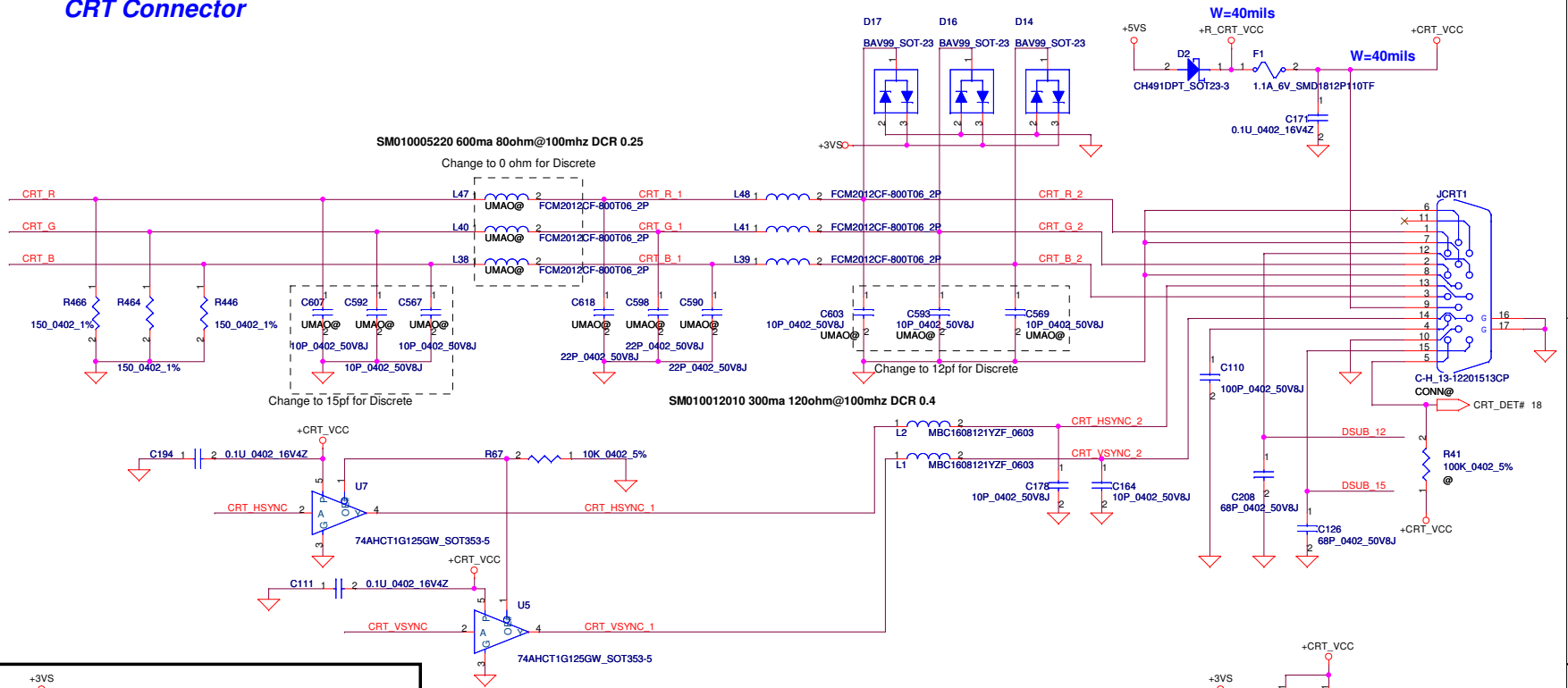


Discrete ONLY



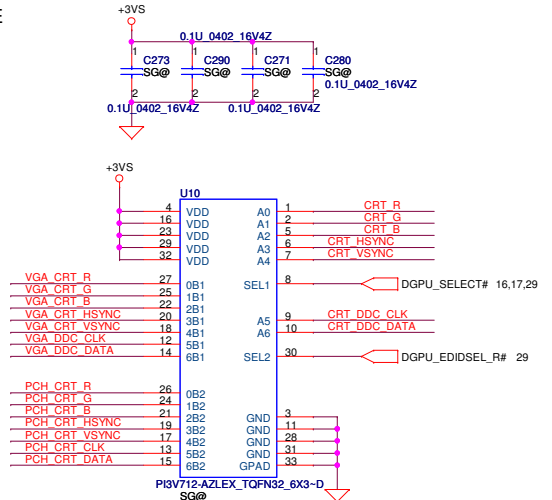
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	LVDS Connector	
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CRT Connector



SWITCHABLE

2009/08/27



L	B1	DIS
H	E2	UMA

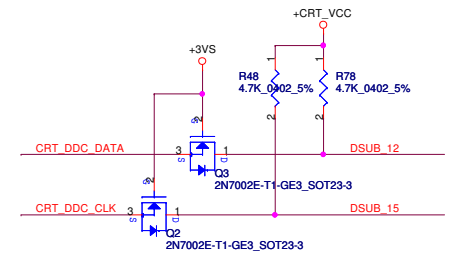
UMA only

16	PCH_CRT_R	PCH_CRT_R	R536	2	UMA0@	1	0.0402 5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R534	2	UMA0@	1	0.0402 5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R532	2	UMA0@	1	0.0402 5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R530	2	UMA0@	1	0.0402 5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R528	2	UMA0@	1	0.0402 5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R544	2	UMA0@	1	0.0402 5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R543	2	UMA0@	1	0.0402 5%	CRT_DDC_DATA

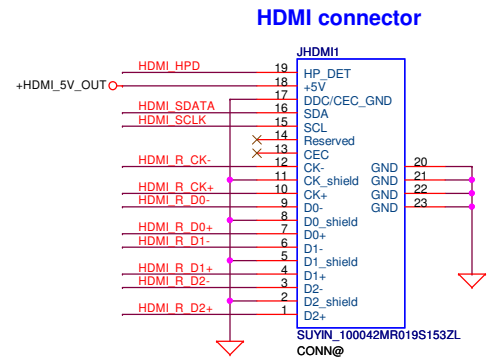
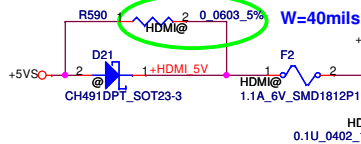
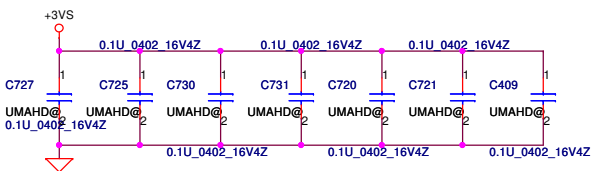
PCH DDC PU 2.2K on Page 17

Discrete only

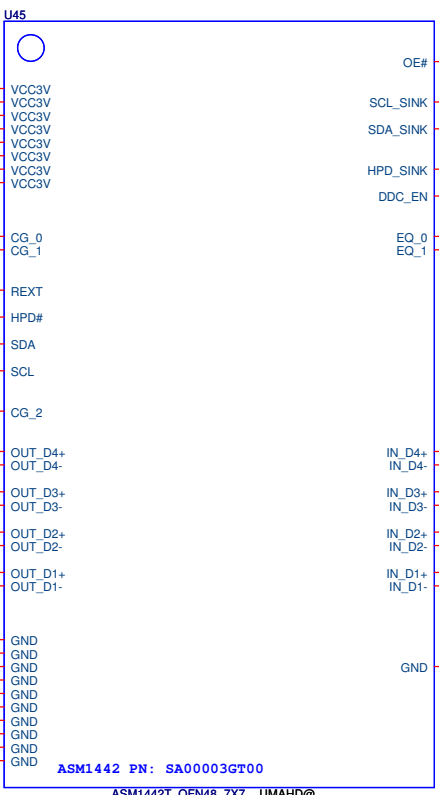
23	VGA_CRT_R	VGA_CRT_R	R537	2	DIS0@	1	0.0402 5%	CRT_R
23	VGA_CRT_G	VGA_CRT_G	R535	2	DIS0@	1	0.0402 5%	CRT_G
23	VGA_CRT_B	VGA_CRT_B	R533	2	DIS0@	1	0.0402 5%	CRT_B
23	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R531	2	DIS0@	1	0.0402 5%	CRT_HSYNC
23	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R529	2	DIS0@	1	0.0402 5%	CRT_VSYNC
23	VGA_DDC_CLK	VGA_DDC_CLK	R527	2	DIS0@	1	0.0402 5%	CRT_DDC_CLK
23	VGA_DDC_DATA	VGA_DDC_DATA	R526	2	DIS0@	1	0.0402 5%	CRT_DDC_DATA



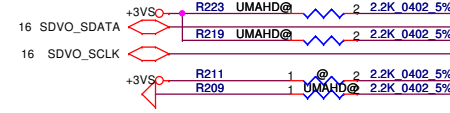
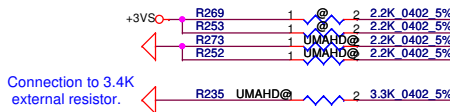
Security Classification	Compal Secret Data		Title	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Compal Electronics, Inc.
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				Rev 1.0
				Date: Tuesday, December 29, 2009 E Sheet 30 of 59



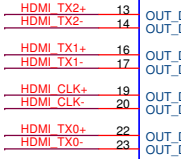
Option	UMAHD@	VGAHD@	HDMI@	@	SG@
UMA	V	X	V	X	X
VGA	X	V	V	X	X
SG	X	V	V	X	V
NO HDM	X	X	X	X	X



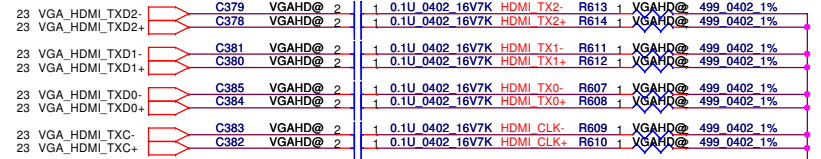
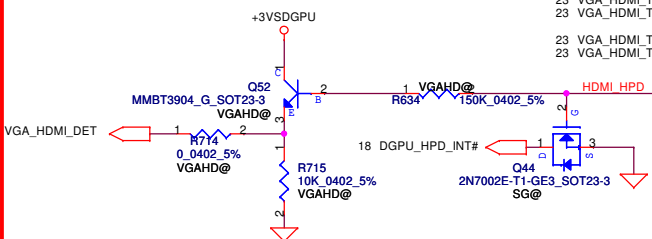
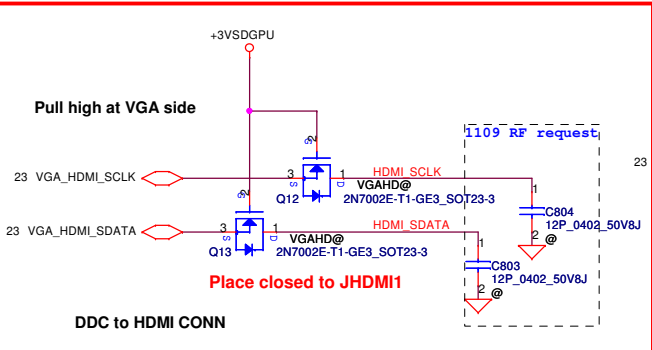
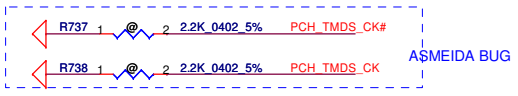
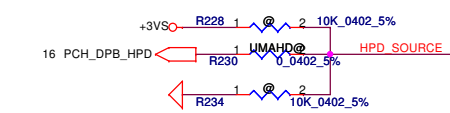
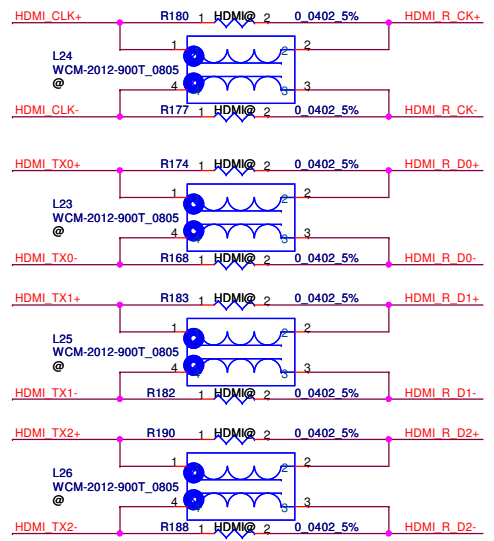
EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)



CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

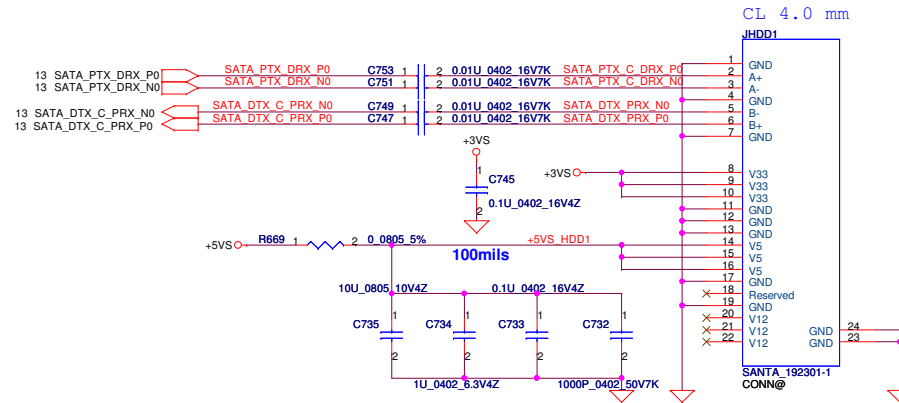


SM070001310 400ma 90ohm@100mhz DCR 0.3

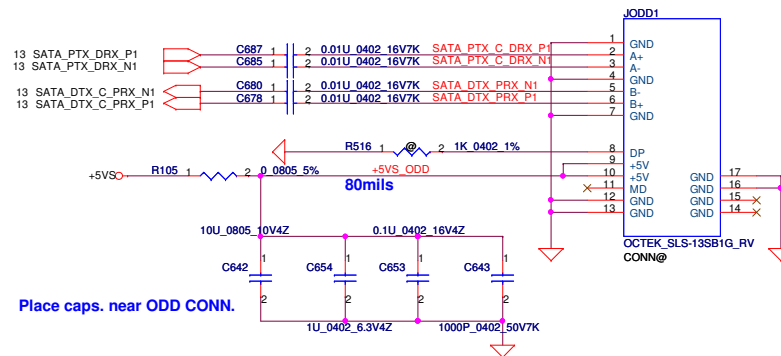


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Size	Document Number	Date		Rev	
Custom	NEW70 M/B LA-5891P Schematic	Tuesday, December 29, 2009		1 of 59	

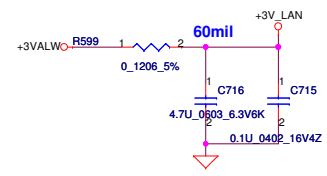
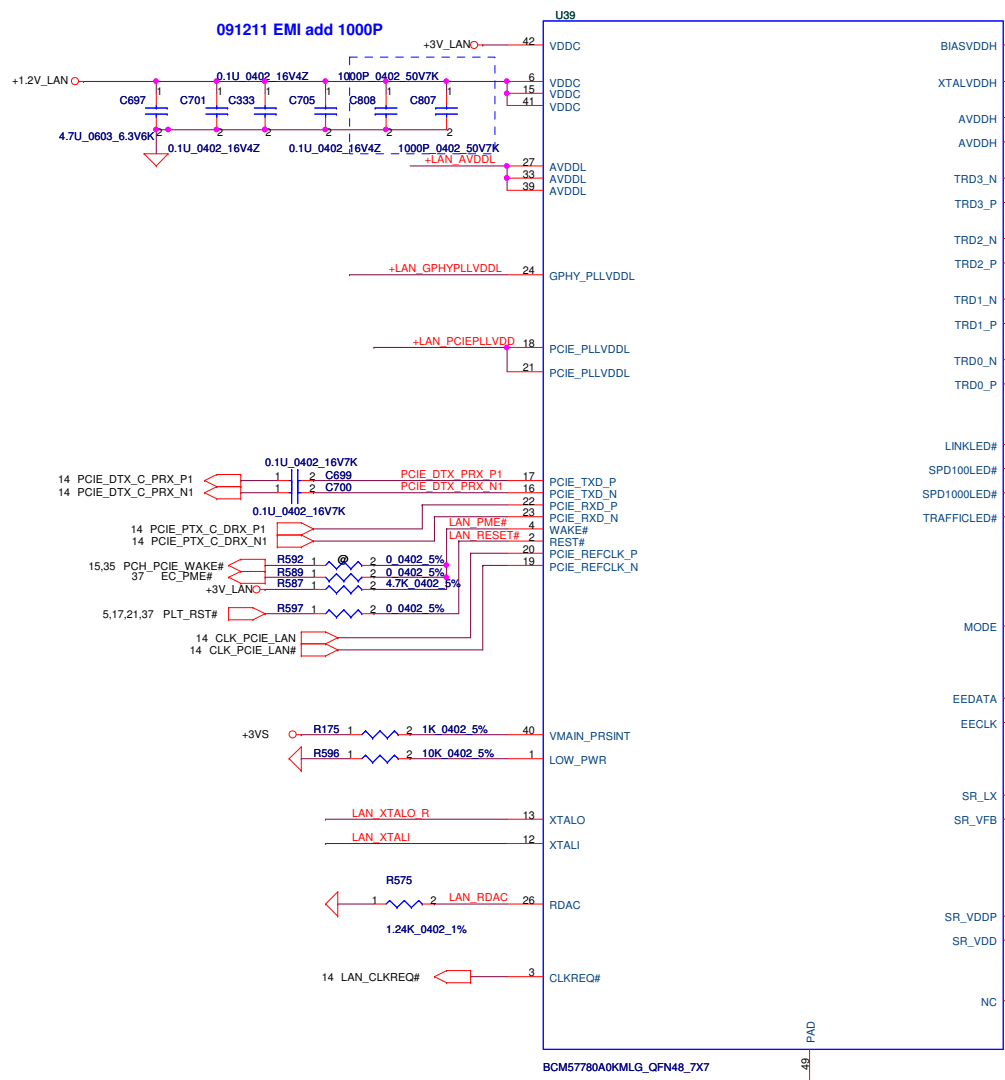
SATA HDD1 Conn.



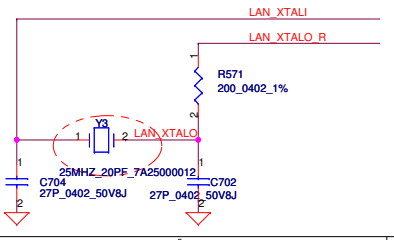
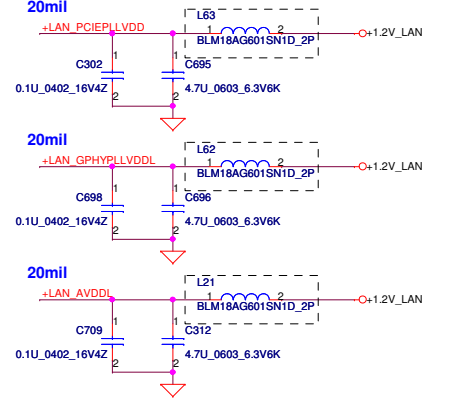
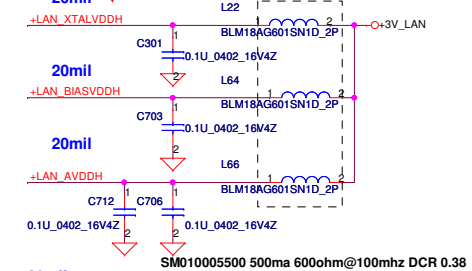
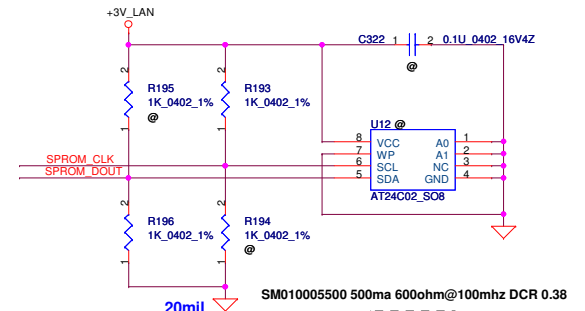
SATA ODD Conn.



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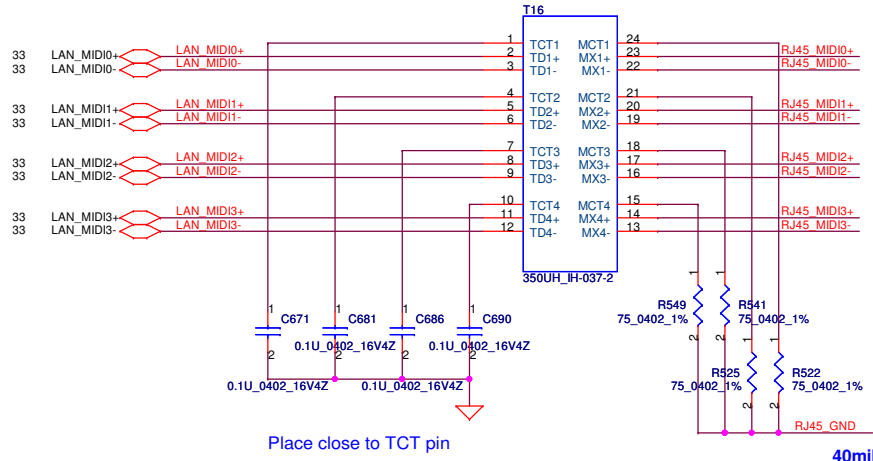


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

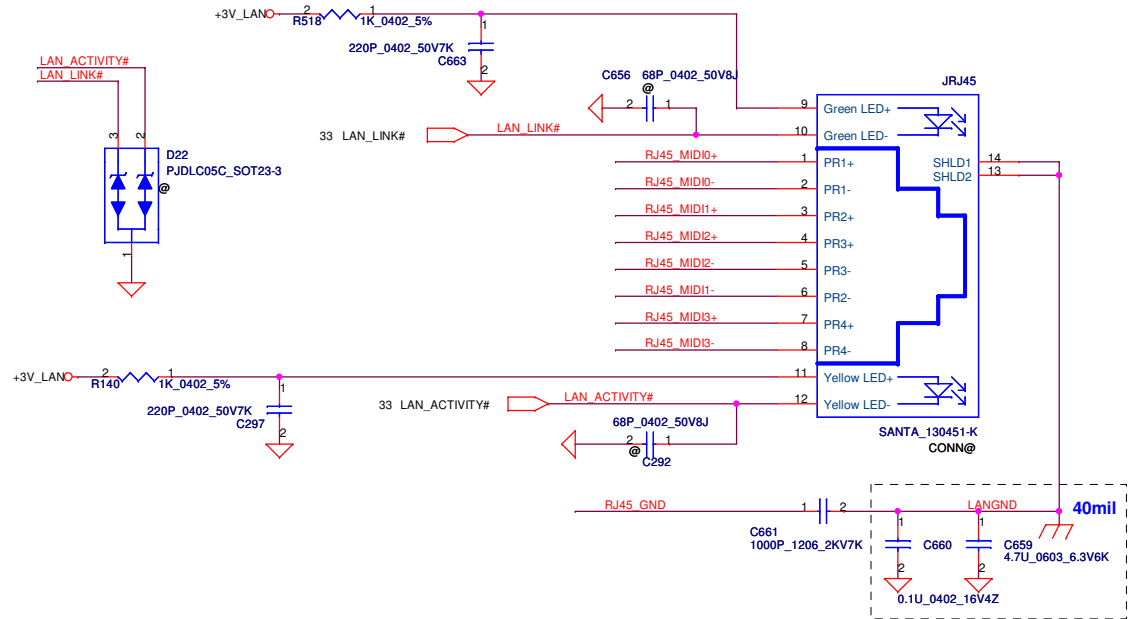


Security Classification	Compal Secret Data		Title	
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LAN Connector

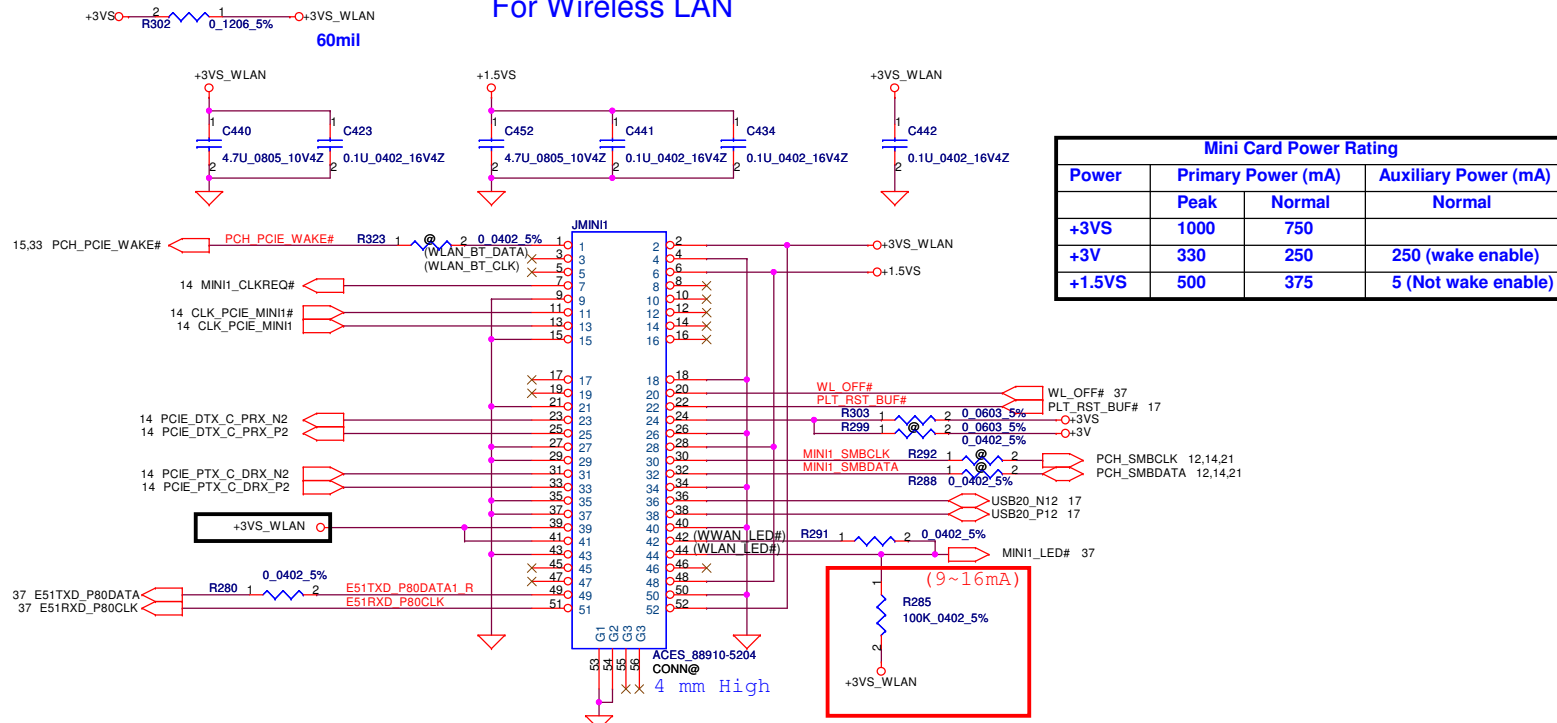


BOTHHAND: S X'FORM_GST5009-D LF LAN, SP050006B00
 TIMAG:S X'FORM_IH-160 LAN , SP050006F00



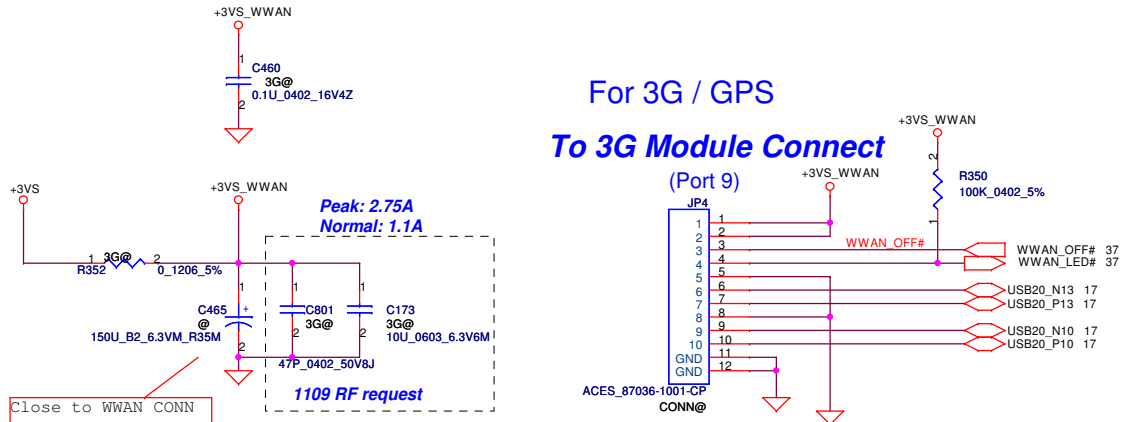
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Date		Sheet	Rev
Customer	NEW70 M/B LA-5891P Schematic	Tuesday, December 29, 2009		34	1.0
				of	59

For Wireless LAN

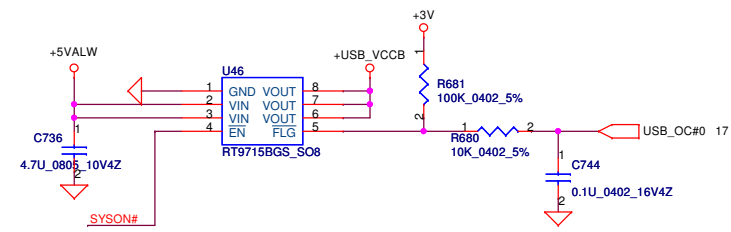
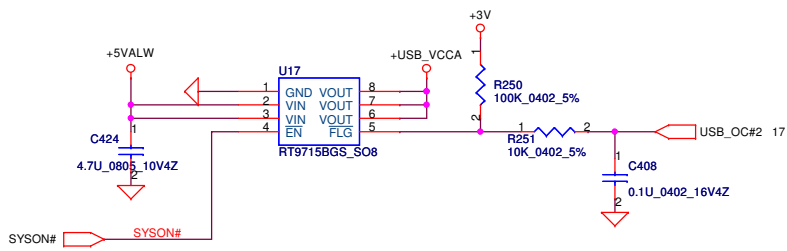


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

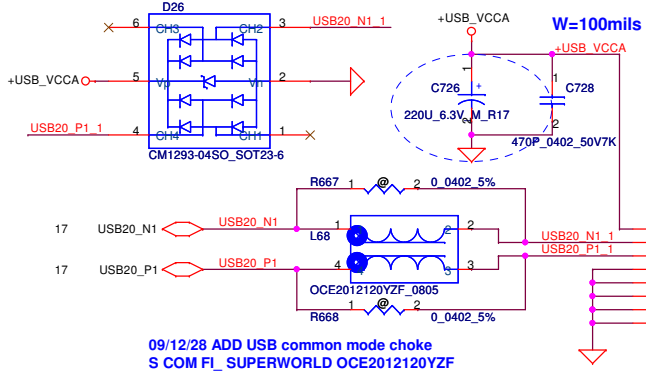
For 3G / GPS To 3G Module Connect



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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title MINI CARD (WLAN & TV-Tuner)				
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Date:	Monday, January 04, 2010	Sheet	35	of		59		



2009/08/14 CHANGE cap



2009/08/25 Update Footprint(follow NAL00)

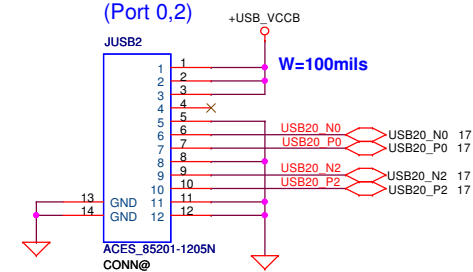
USB Conn.

(Port 1)

09/12/28 ADD USB common mode choke
S COM FL SUPERWORLD OCE2012120VZF

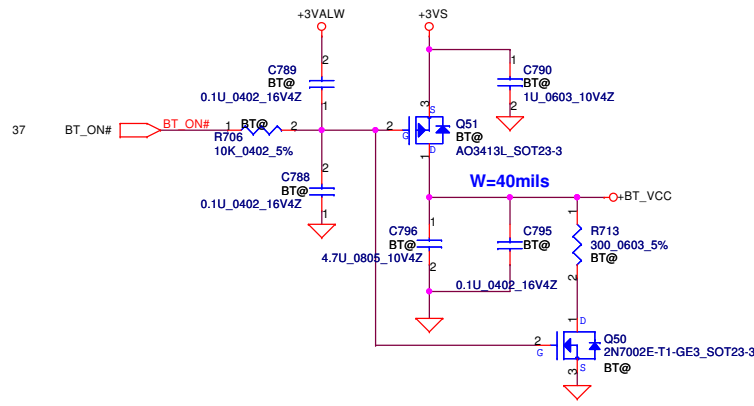
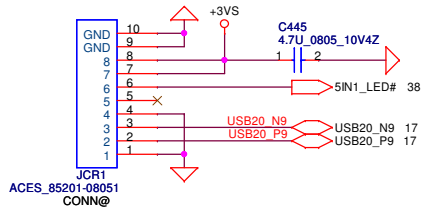
USB/B Conn.

(Port 0,2)



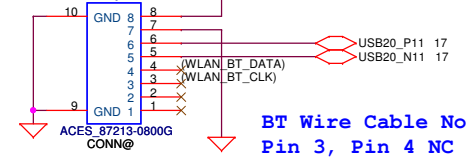
2009/08/24 CHANGE Conn to FFC Type

Card Reader Conn.



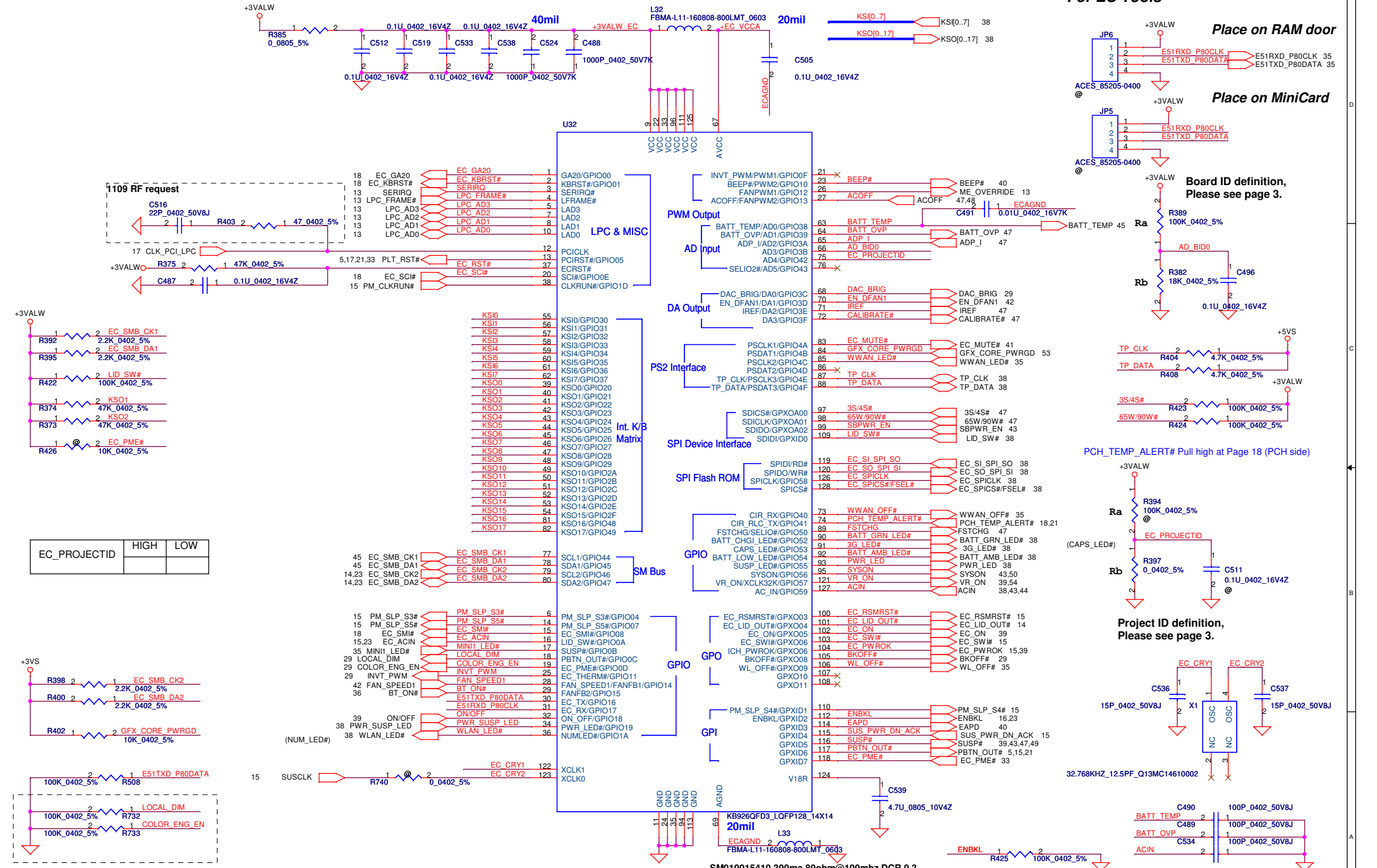
BT Conn.

(Port 11)

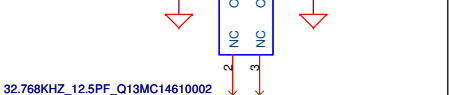
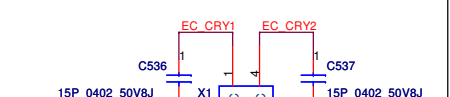
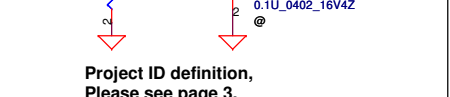
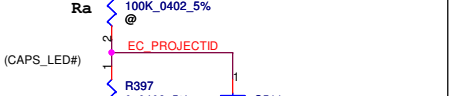
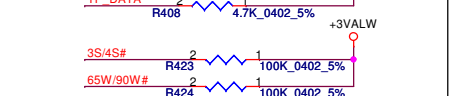
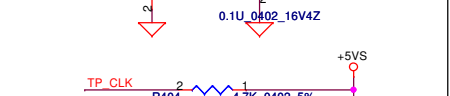
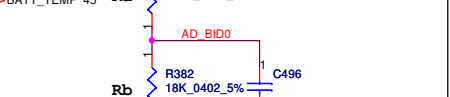
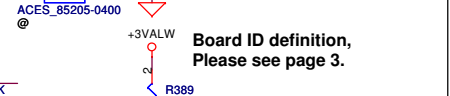
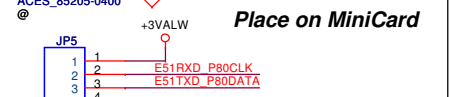
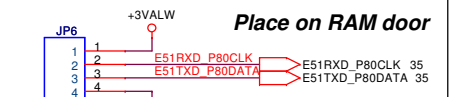


BT Wire Cable Note:
Pin 3, Pin 4 NC

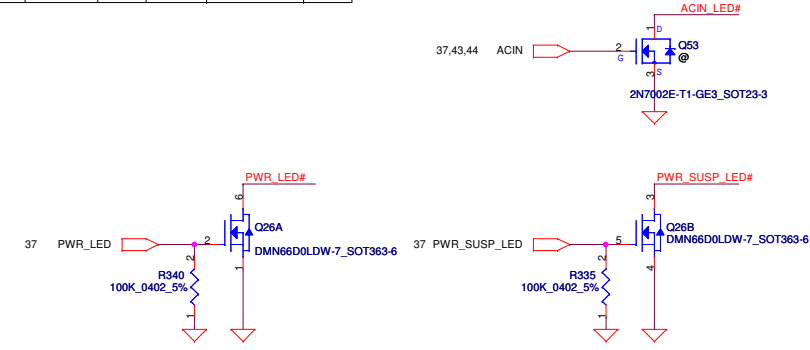
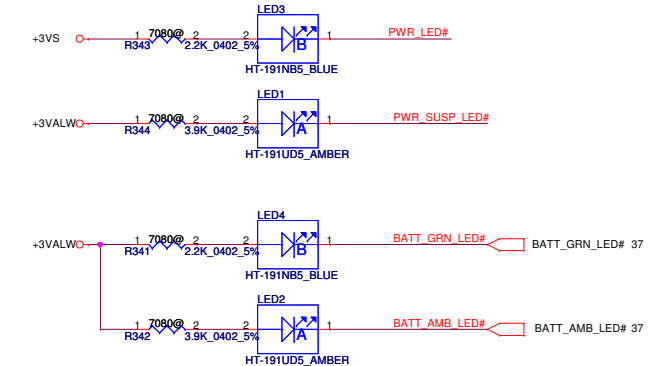
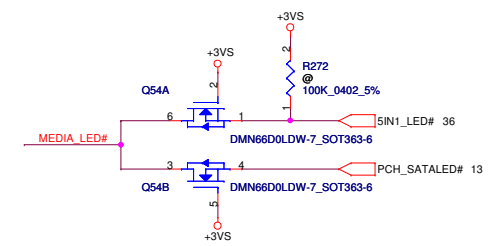
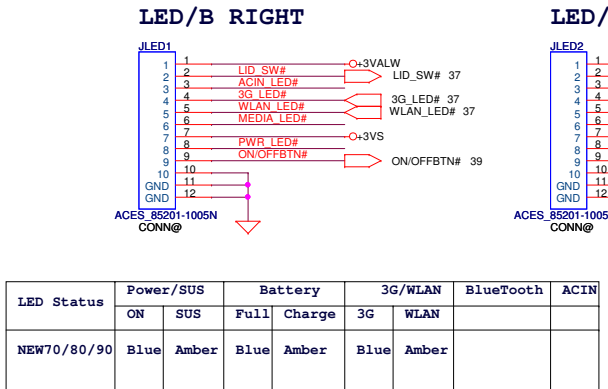
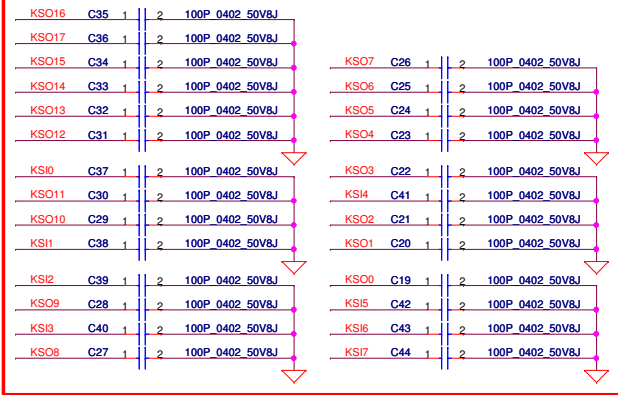
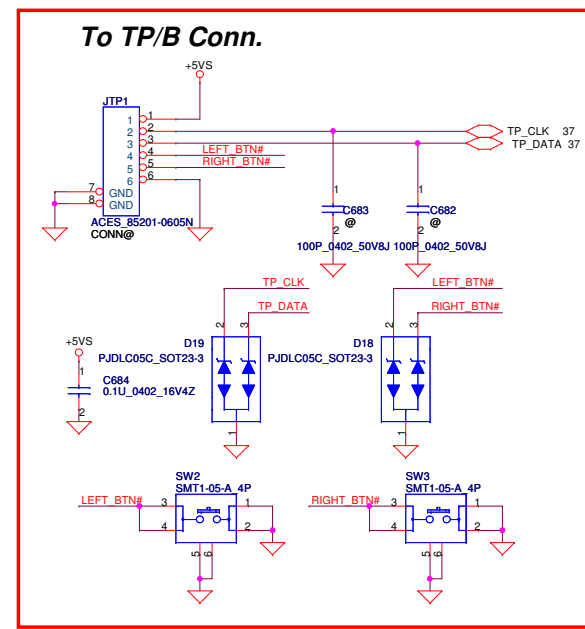
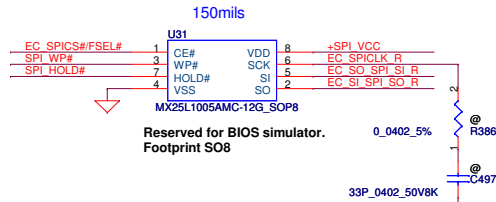
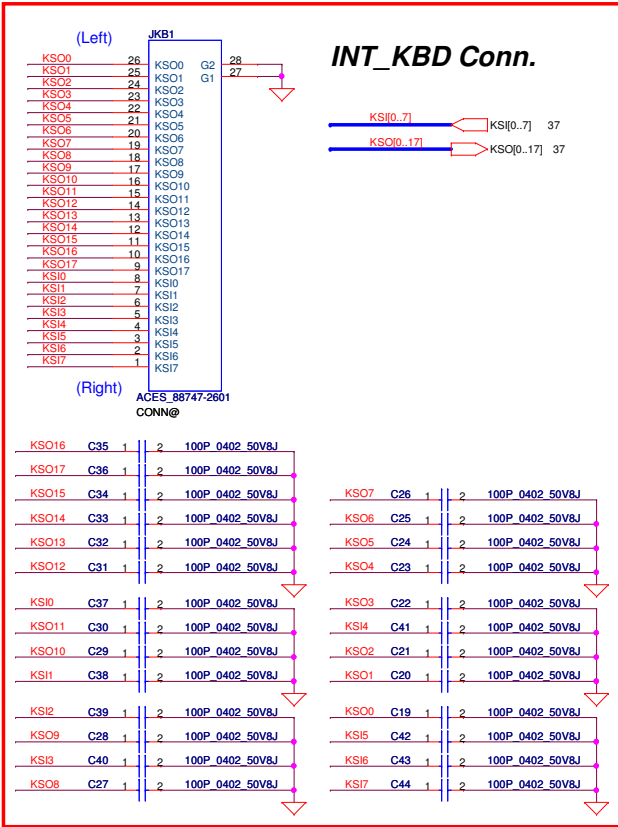
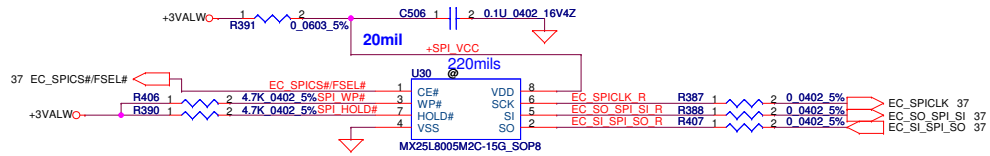
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EC_PROJECTID	HIGH	LOW



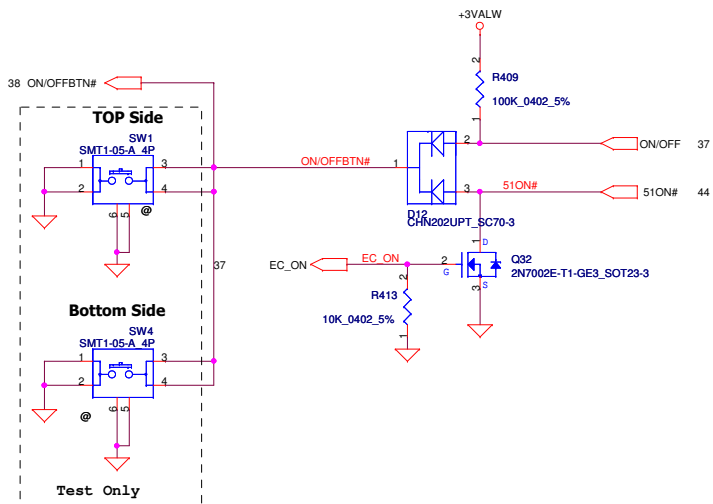
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	NEW70 M/B LA-5891P Schematic		Rev	1.0
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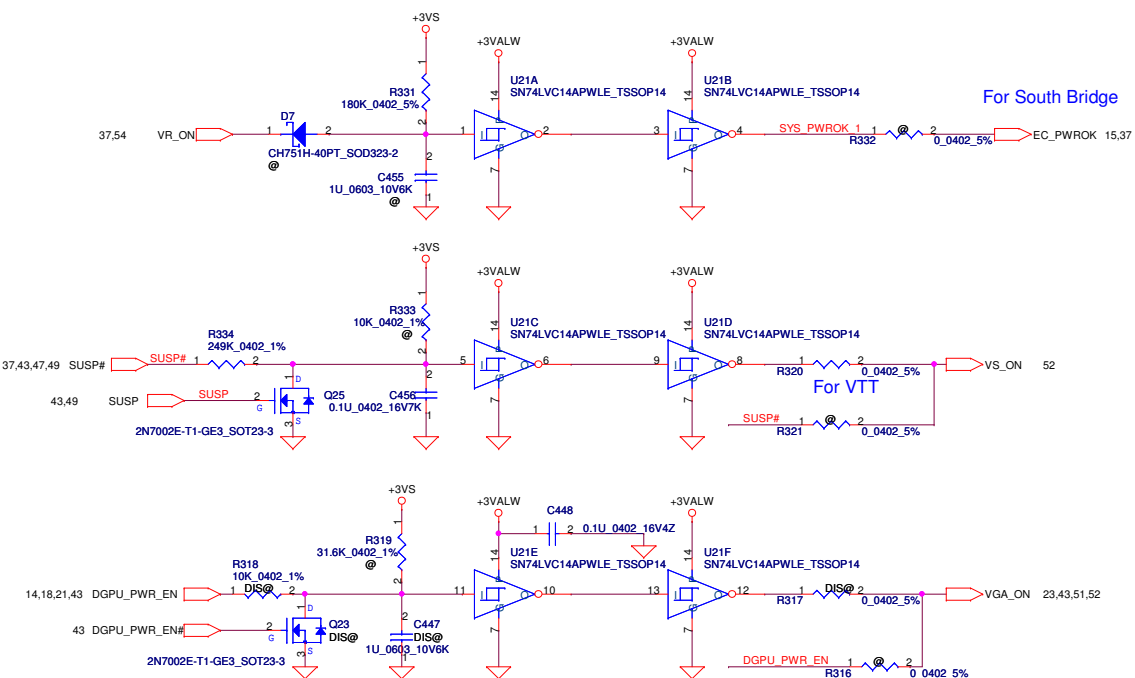
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

Power Button

ON/OFF switch

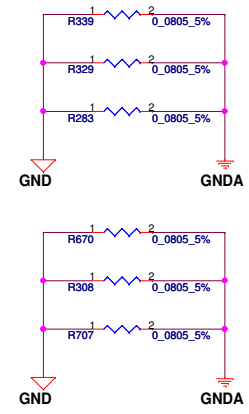
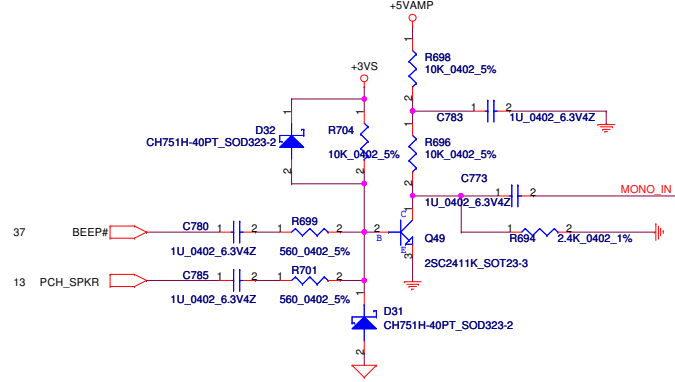
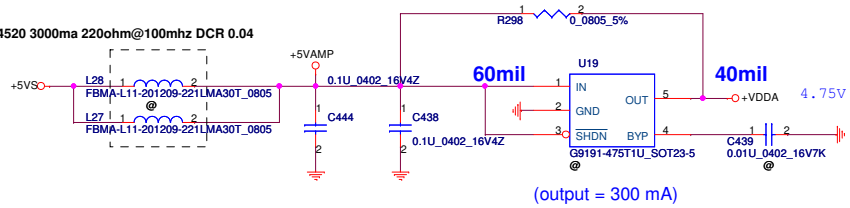


Power ON Circuit



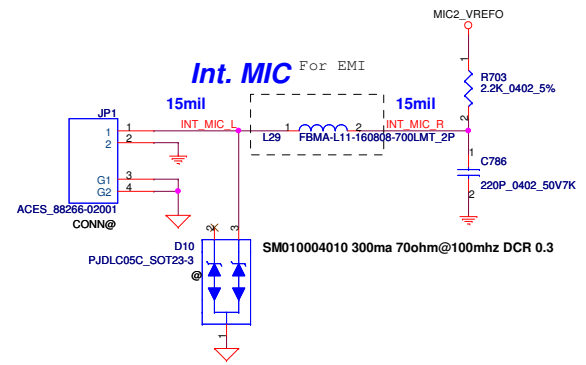
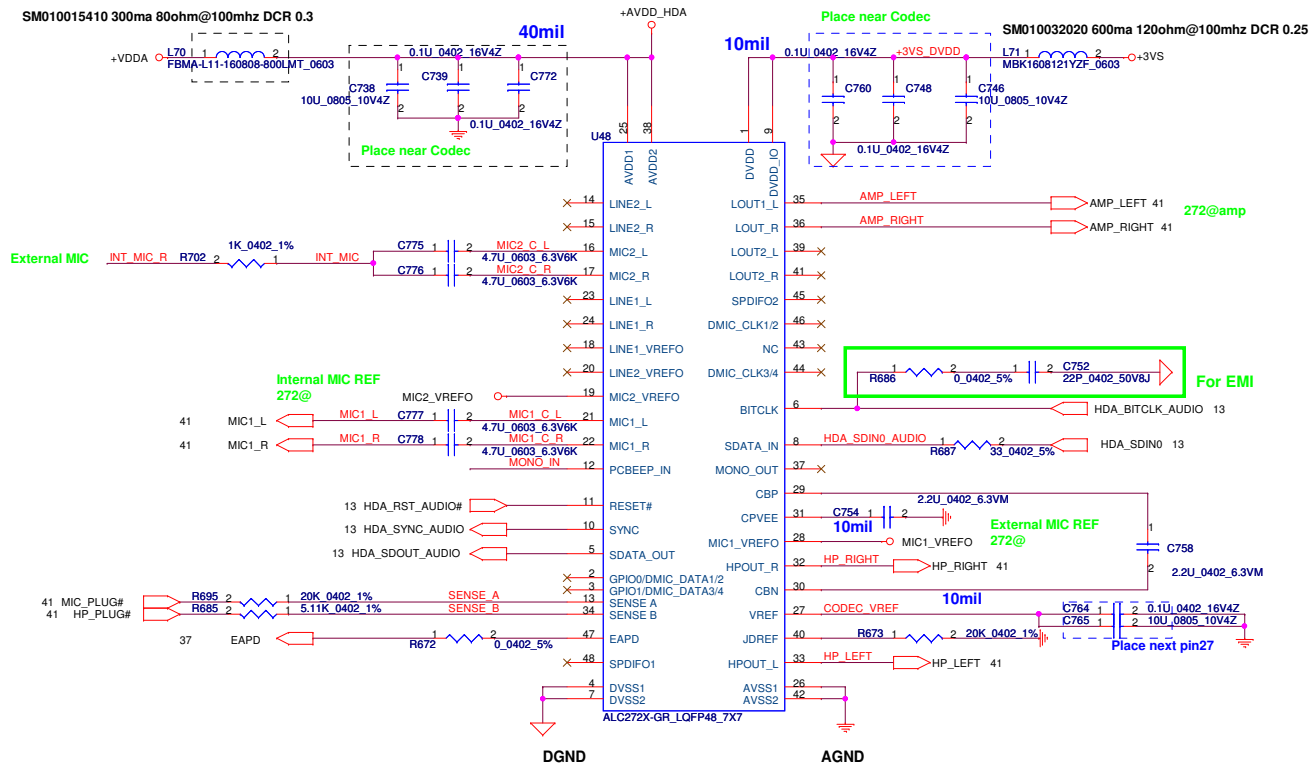
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				NEW70 M/B LA-5891P Schematic	1.0
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SM010014520 3000ma 220ohm@100mhz DCR 0.04



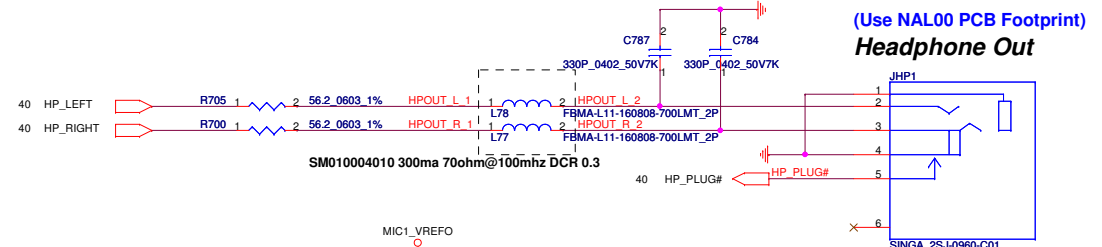
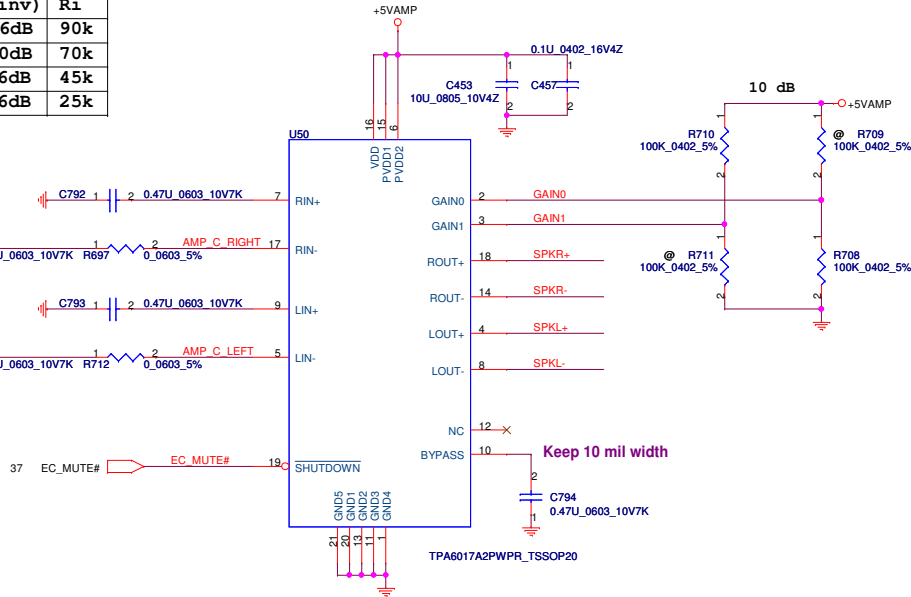
HD Audio Codec

SM010015410 300ma 80ohm@100mhz DCR 0.3

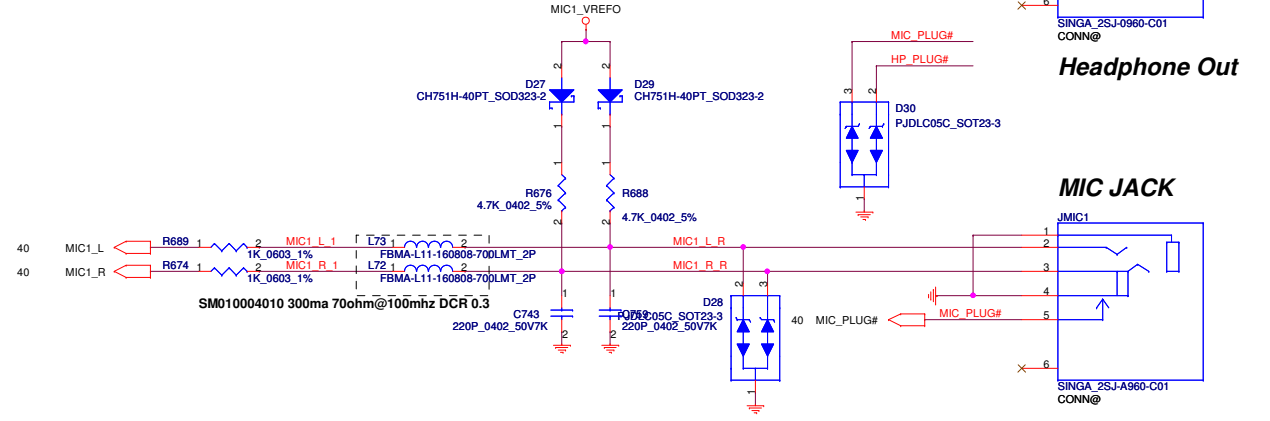
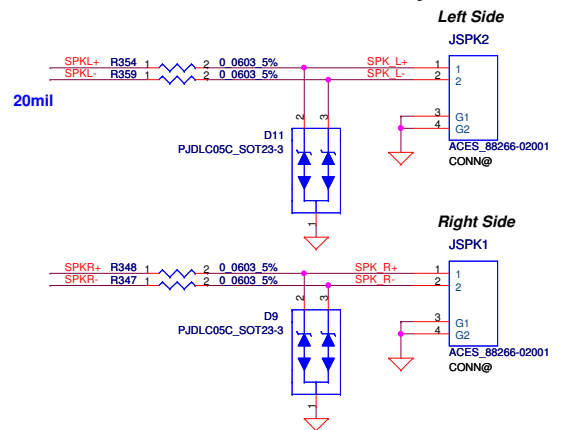


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GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

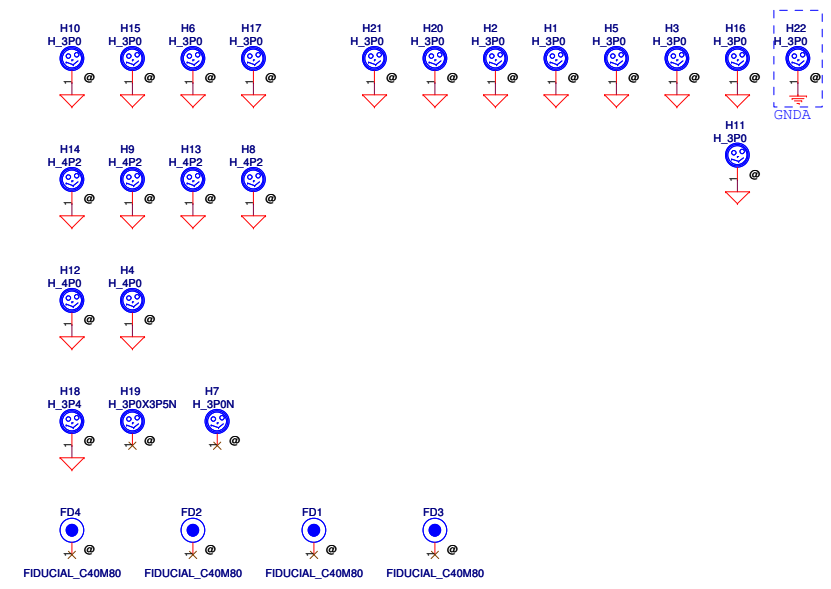
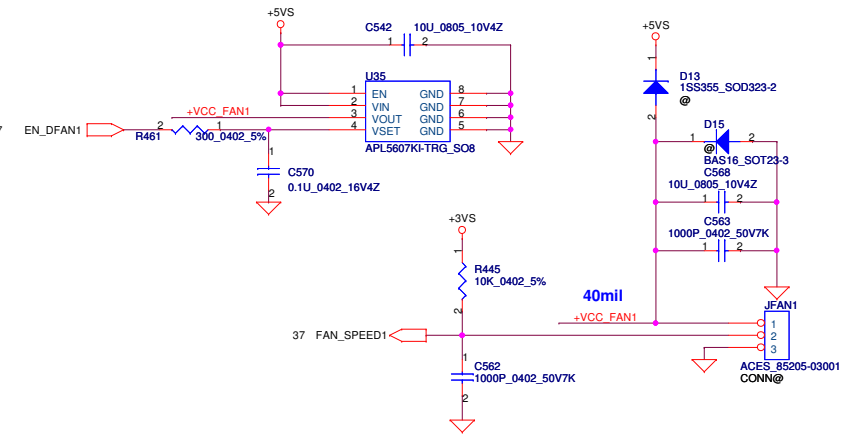


Int. Speaker Conn.

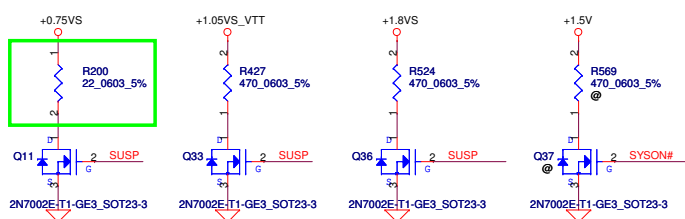
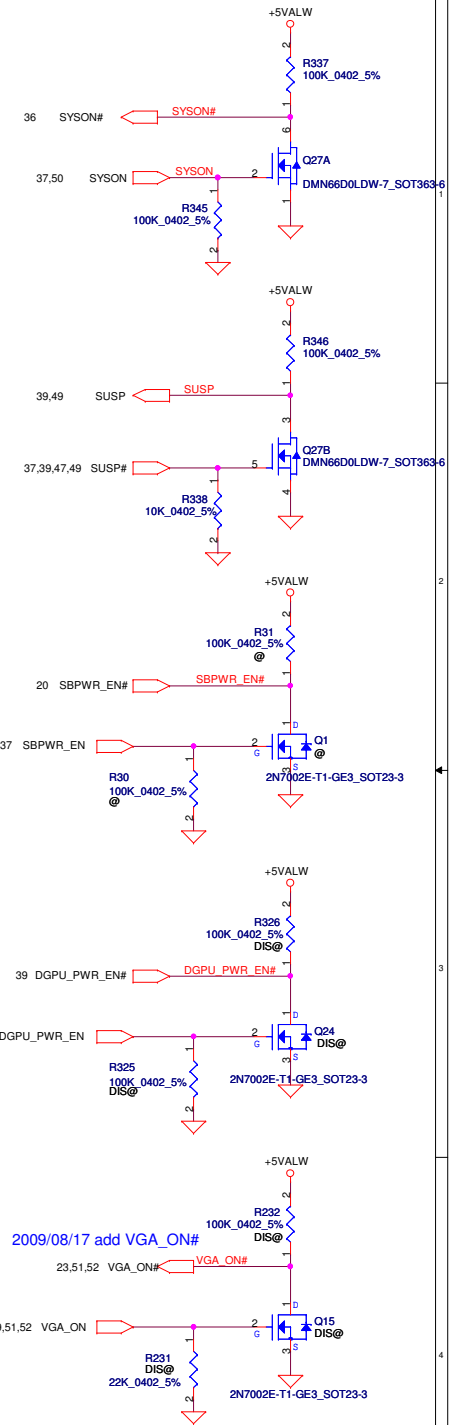
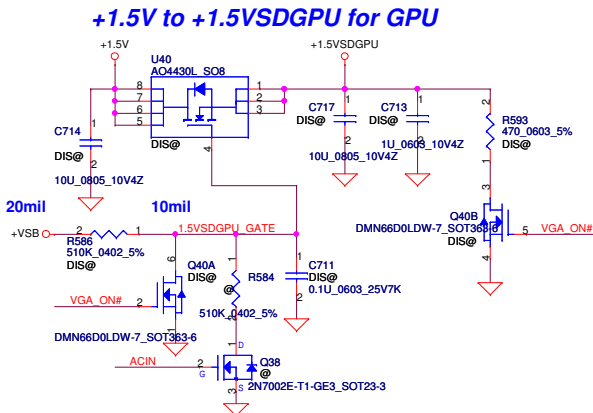
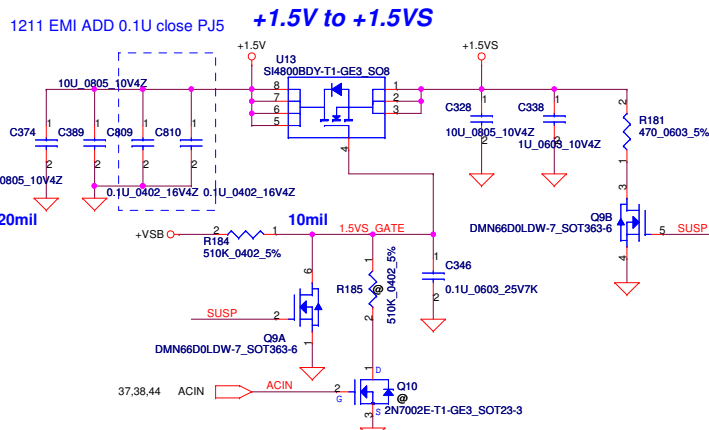
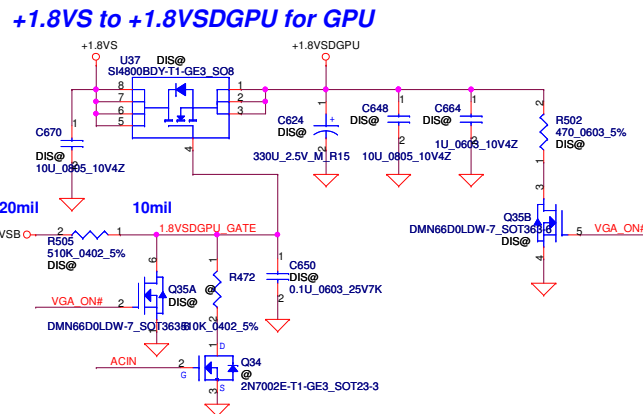
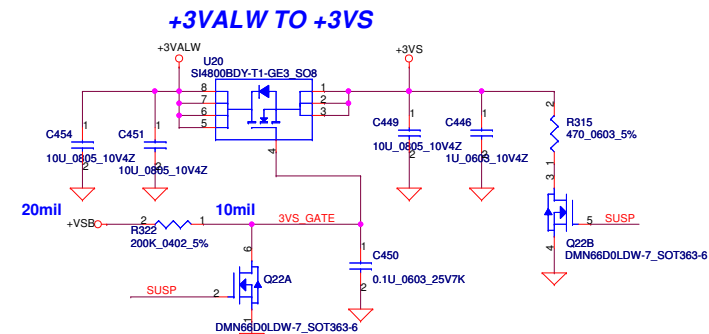
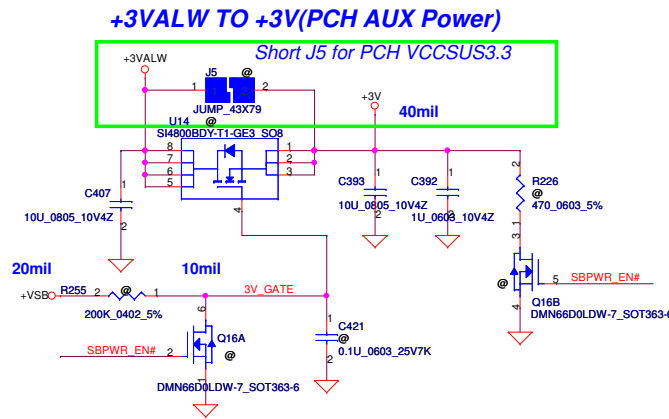
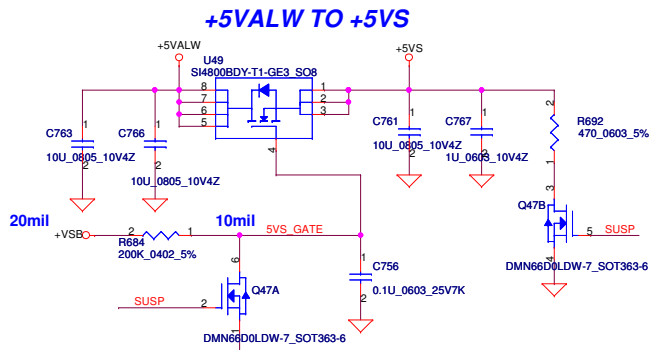


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FAN1 Conn

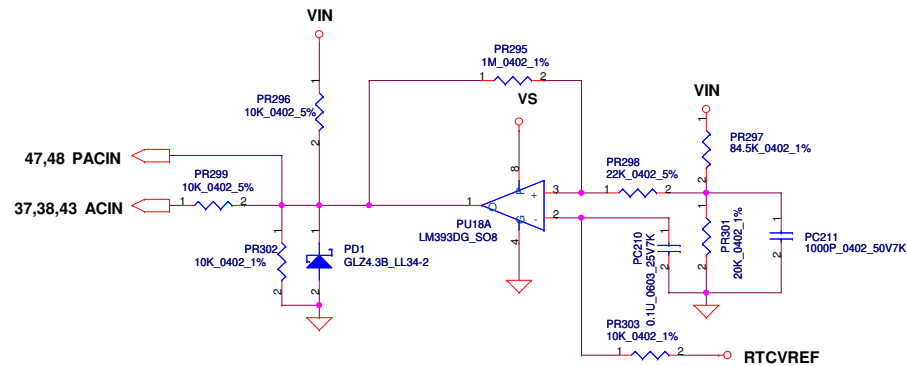
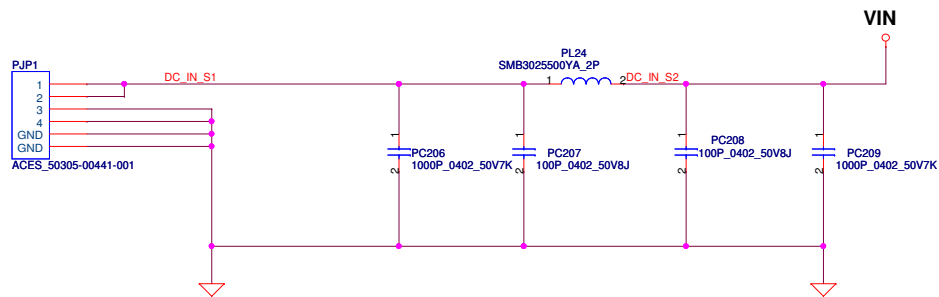


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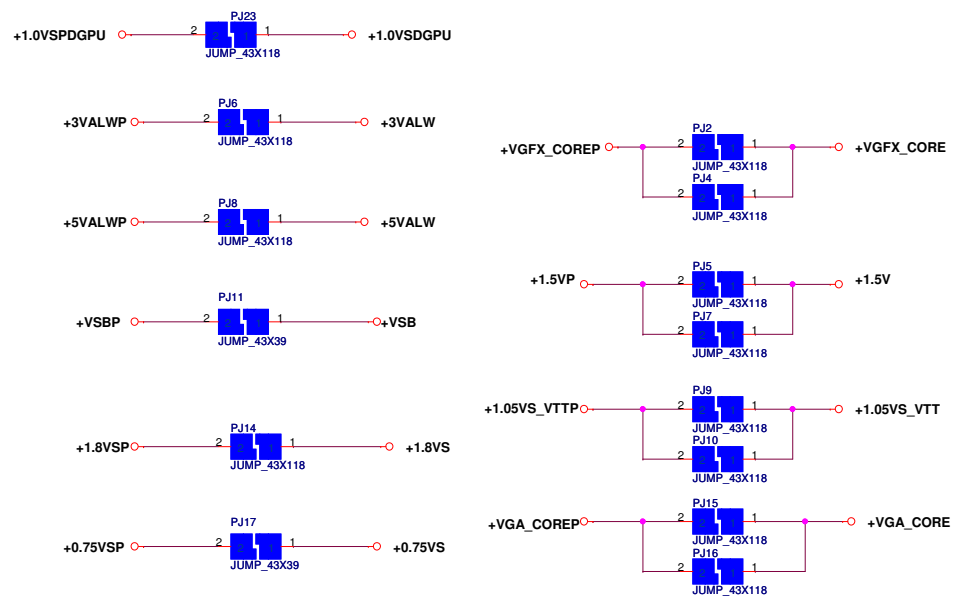
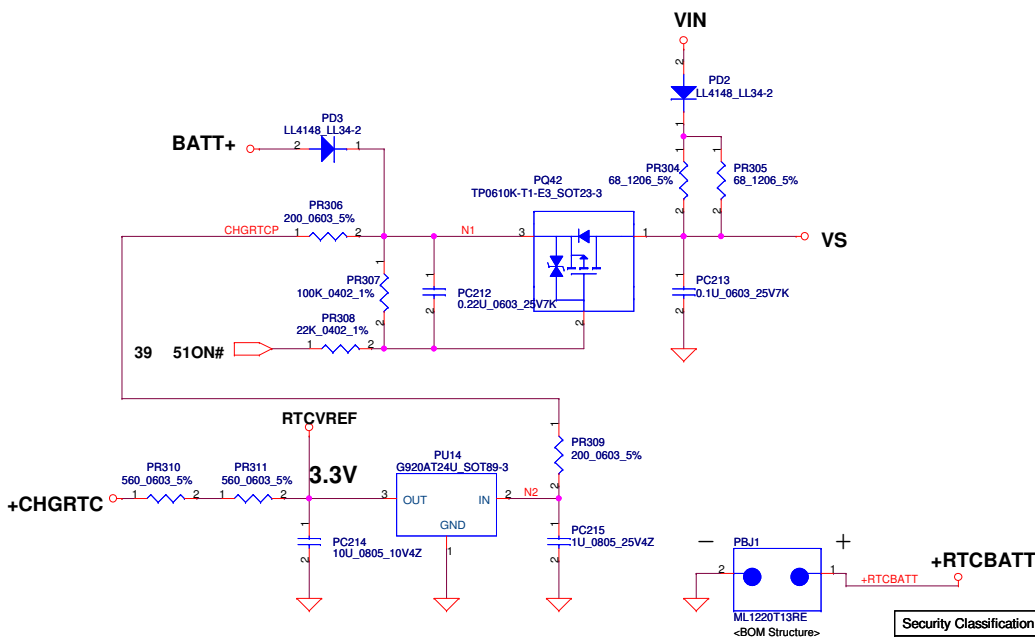


2009/08/14
 CP_S3PowerReduction
 WhitePaper_Rev0.9
 0.75VS speed up discharge

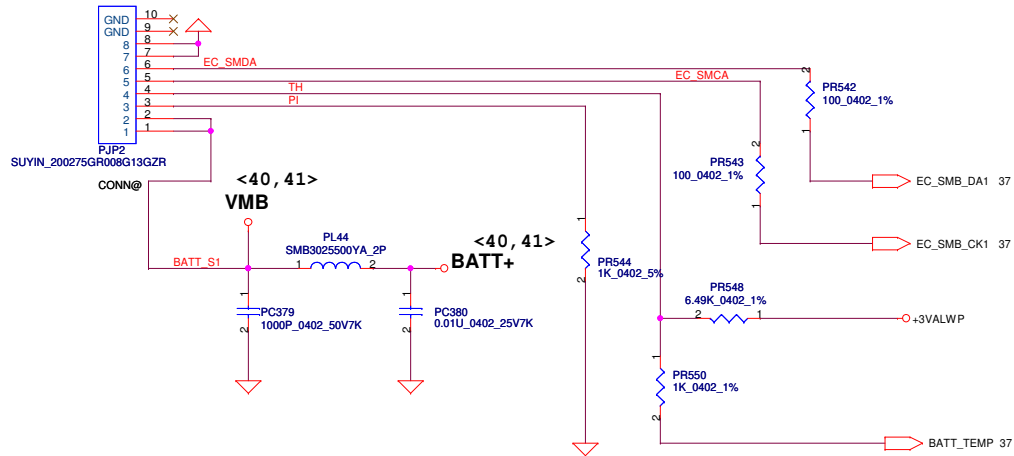
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	DC Interface
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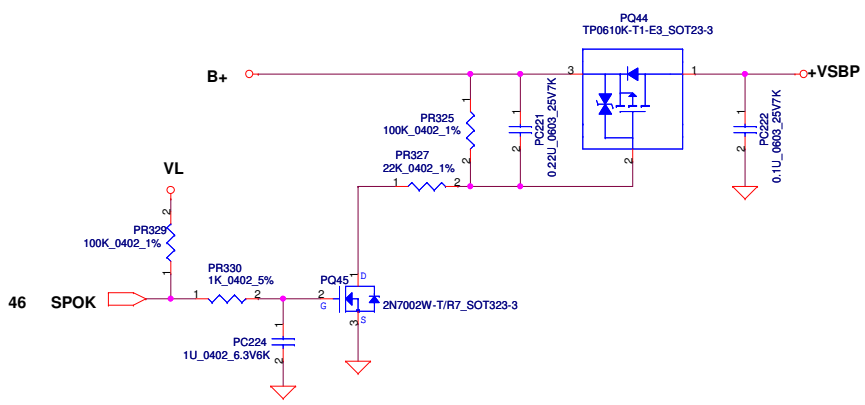
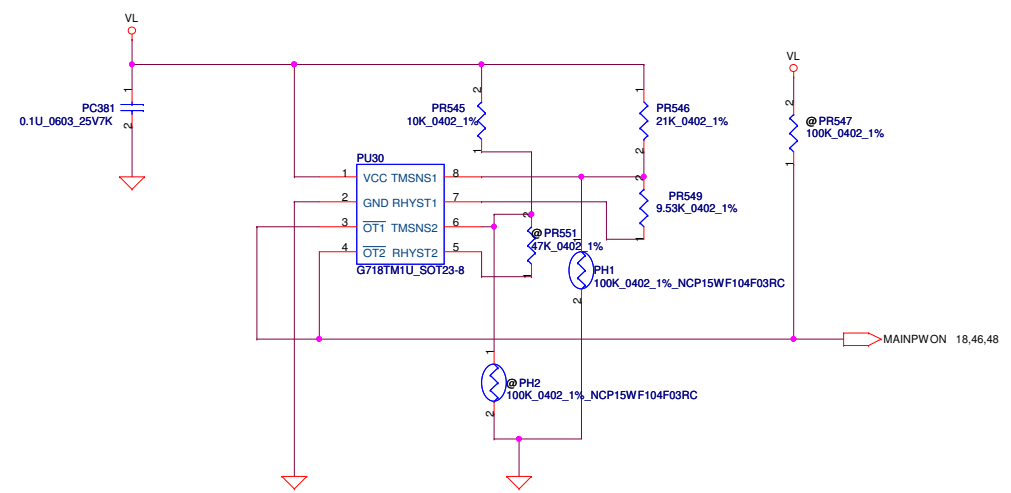
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



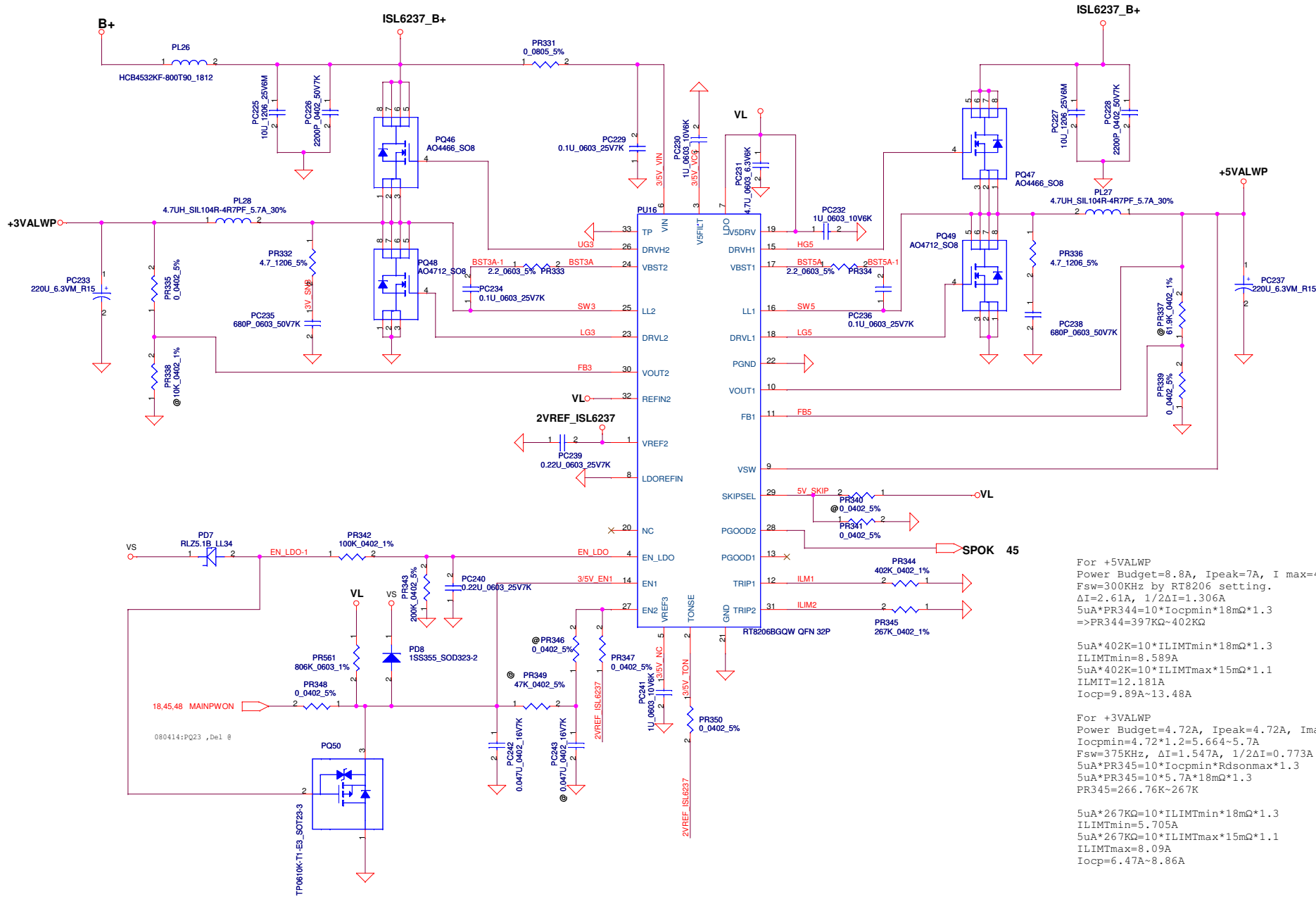
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PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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For +5VALWP
 Power Budget=8.8A, Ipeak=7A, I max=4.9A
 Fsw=300KHz by RT8206 setting.
 $\Delta I=2.61A$, $1/2\Delta I=1.306A$
 $5uA*PR344=10*Iocpmin*18m\Omega*1.3$
 $\Rightarrow PR344=397K\Omega-402K\Omega$

$5uA*402K=10*ILIMITmin*18m\Omega*1.3$
 $ILIMITmin=8.589A$
 $5uA*402K=10*ILIMITmax*15m\Omega*1.1$
 $ILIMIT=12.181A$
 $Iocp=9.89A-13.48A$

For +3VALWP
 Power Budget=4.72A, Ipeak=4.72A, I max=4A
 $Iocpmin=4.72*1.2=5.664\sim 5.7A$
 $Fsw=375KHz$, $\Delta I=1.547A$, $1/2\Delta I=0.773A$
 $5uA*PR345=10*Iocpmin*18m\Omega*1.3$
 $5uA*PR345=10*5.7A*18m\Omega*1.3$
 $PR345=266.76K\sim 267K$

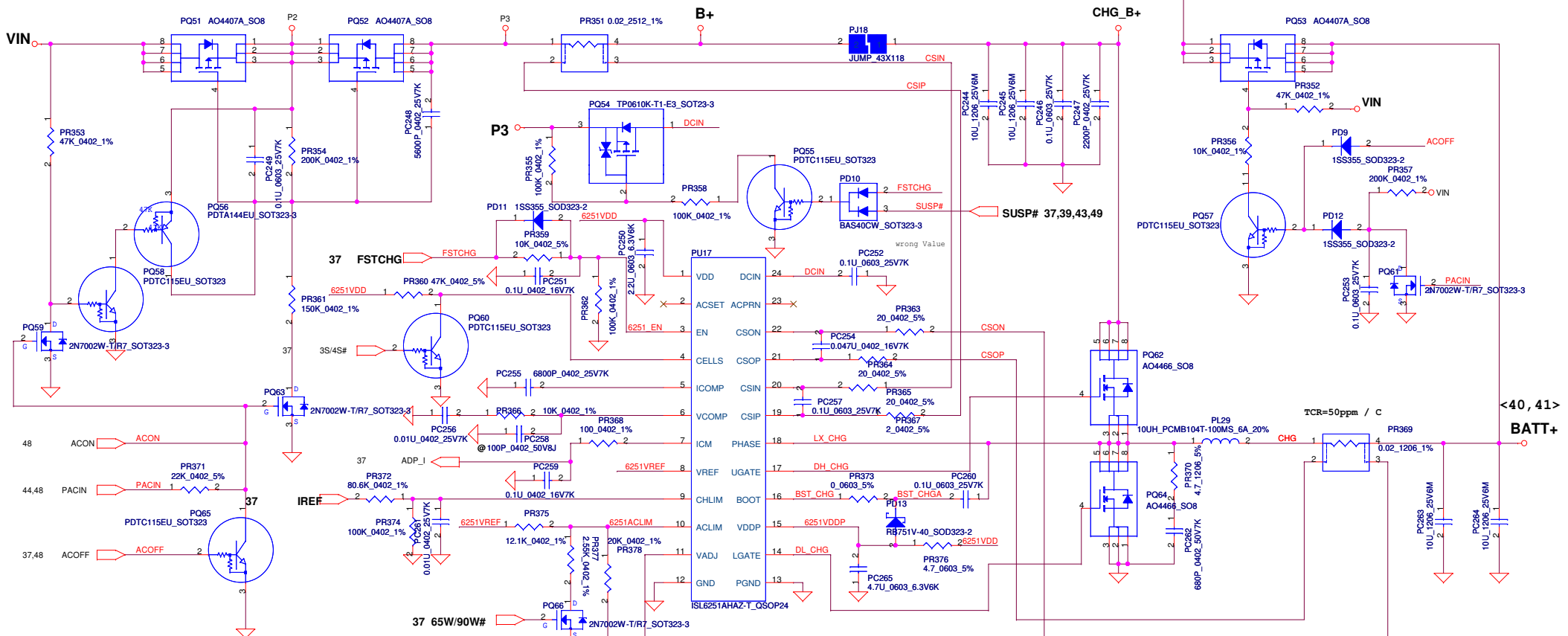
$5uA*267K=10*ILIMITmin*18m\Omega*1.3$
 $ILIMITmin=5.705A$
 $5uA*267K=10*ILIMITmax*15m\Omega*1.1$
 $ILIMITmax=8.09A$
 $Iocp=6.47A-8.86A$

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Iada=0~4.74A (90W/19V=4.736A)
 Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
 CP = 85%*Iada ; CP = 2.91A



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

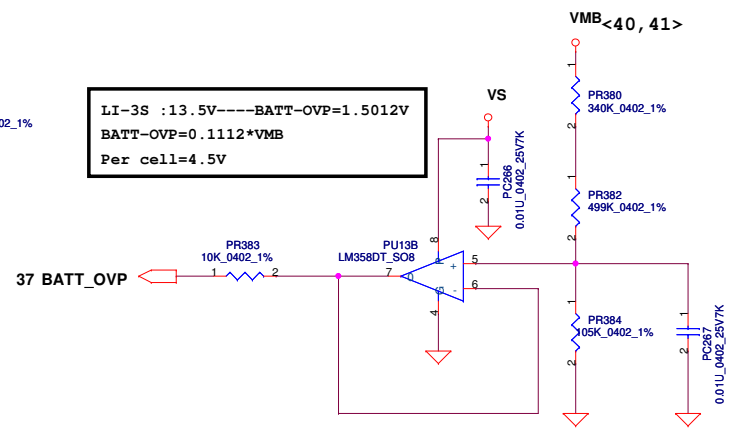
CC=0.6-4.48A
 $I_{ref} = 0.7224 * I_{charge}$
 $k_I = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

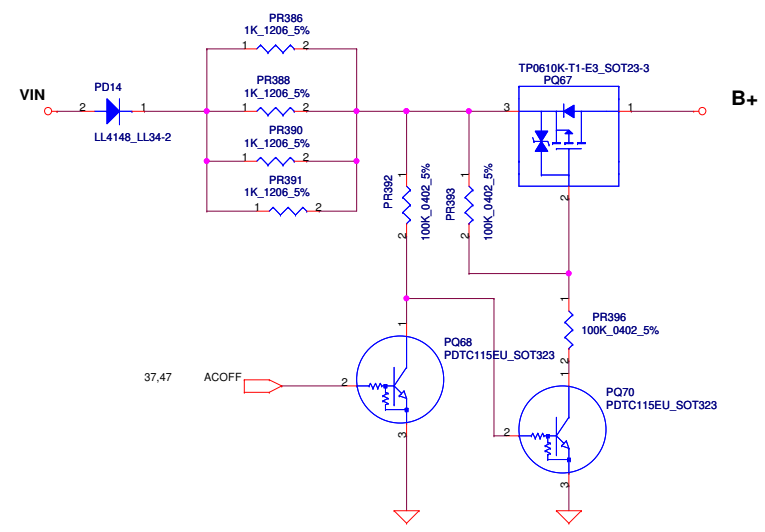
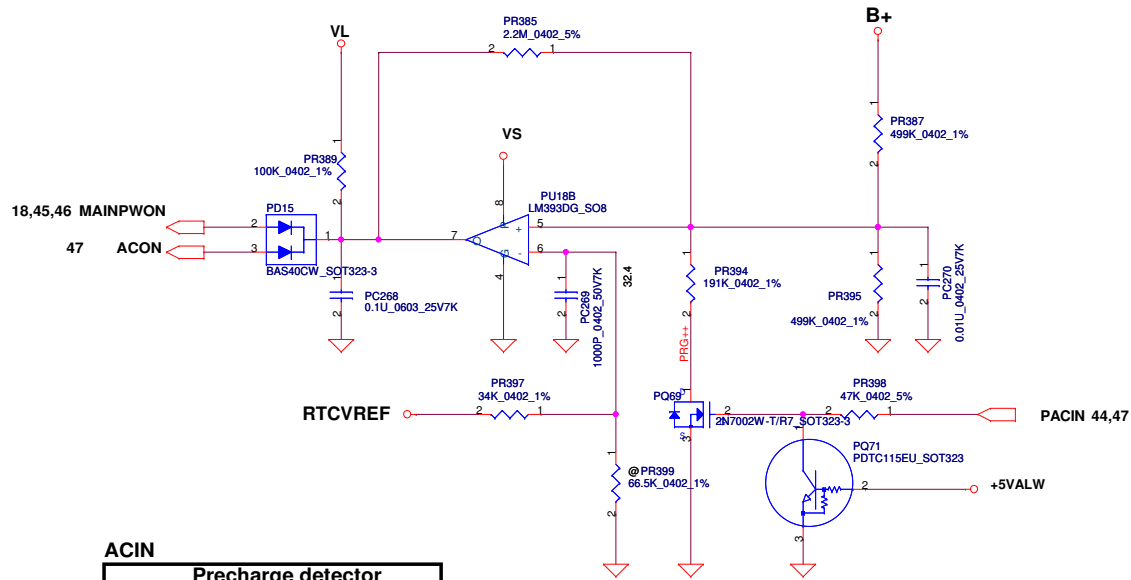
K1
 $V_{ch1m} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{ch1m} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow k_I = 0.7224$

Kv
 $R_{internal} = 514K$, $R_{ec} = 3K$, $R_1 = PR379 = 15.4K$, $R_2 = PR381 = 31.6K$
 $r = 514K / (514K // 31.6K // (15.4K + 3K)) = 1.372K$
 $r = 514K // (514K // 31.6K // 28.14K)$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R_1 / (R_1 + 514K)) = CALIBRATE * (r / (r + 514K))$
 $1.1463 = CALIBRATE * 0.6048 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R_1 / (R_1 + 514K)) = 0.052$
 $Kv = 9.451$

LI-3S : 1.3.5V --- BATT-OVP=1.5012V
 $BATT-OVP = 0.1112 * V_{MB}$
 Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V





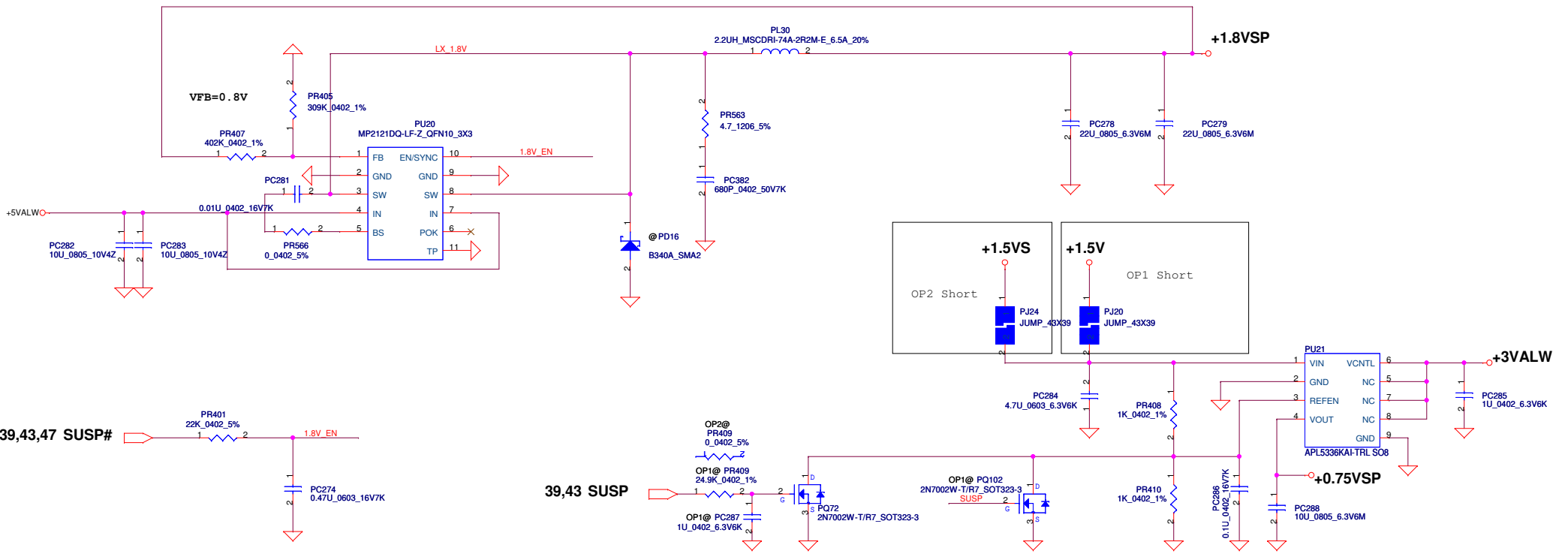
ACIN

Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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7,39,43,47 SUSP#

39,43 SUSP

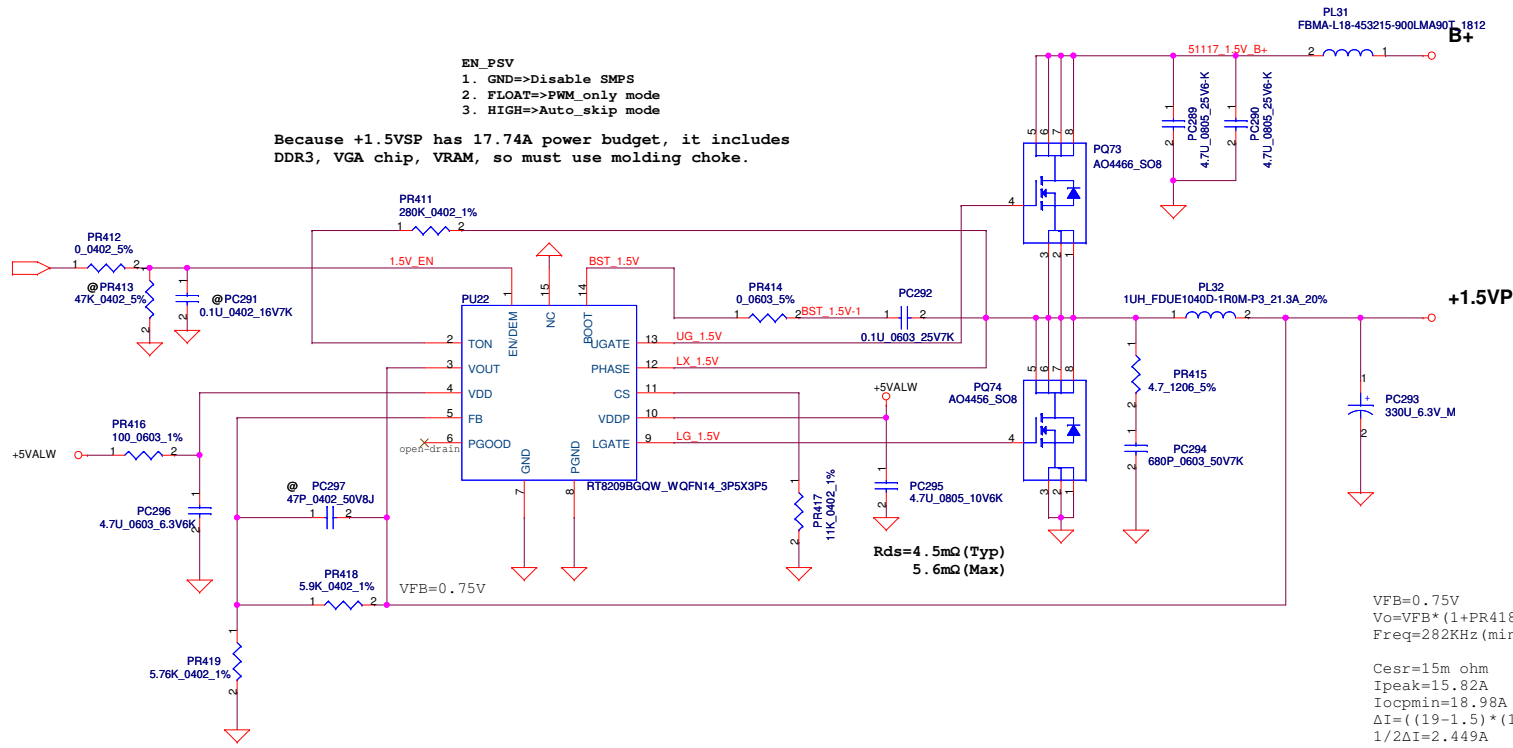
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+1.8VSP/+0.75VSP
 NEW70 M/B LA-5891P Schematic
 1.0
 Tuesday, December 29, 2009

- EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.

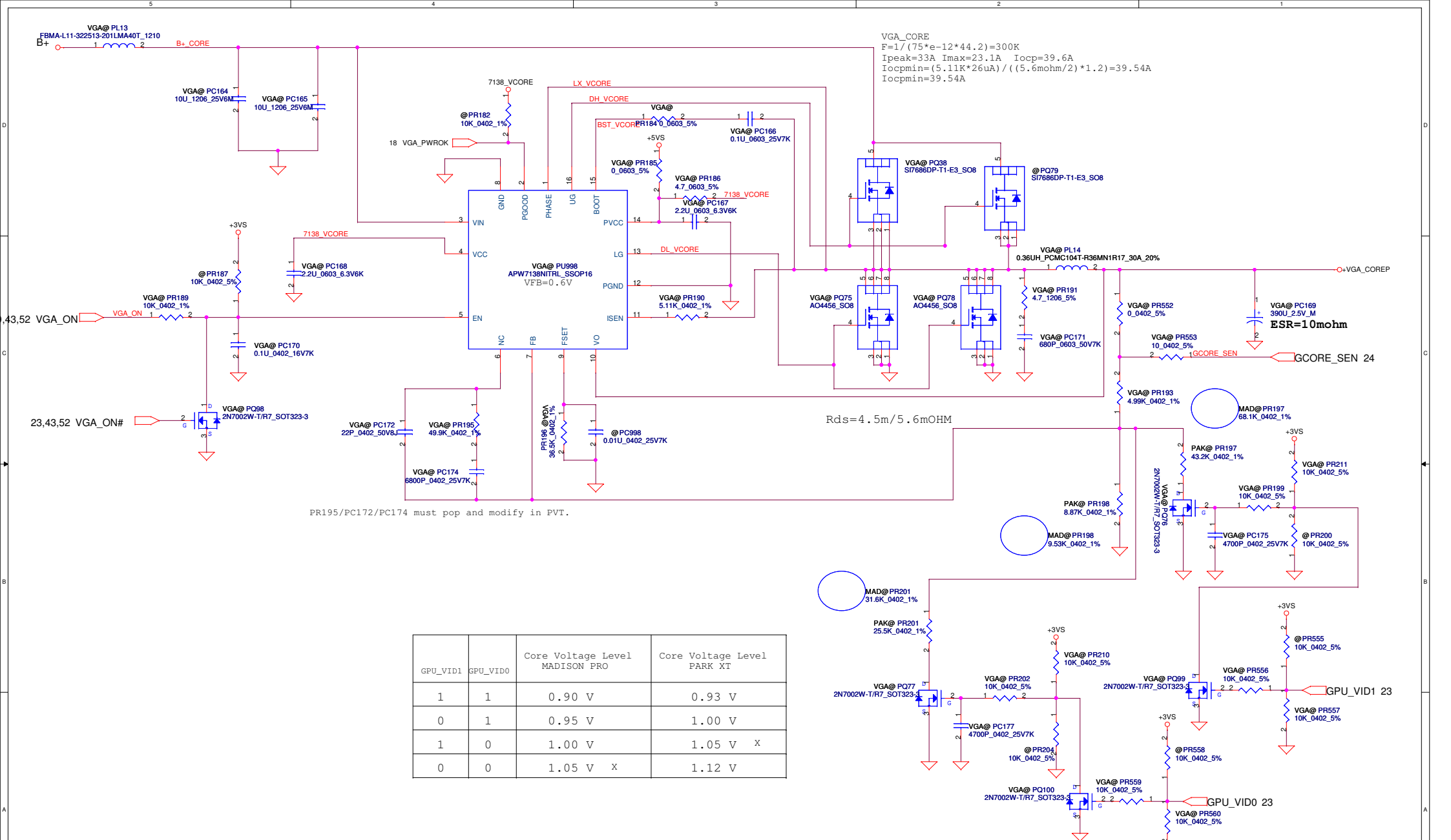
37,43 SYSON



VFB=0.75V
 $V_o = VFB * (1 + PR418 / PR419) = 1.52V$
 Freq=282KHz(min) , 300KHz(typ)

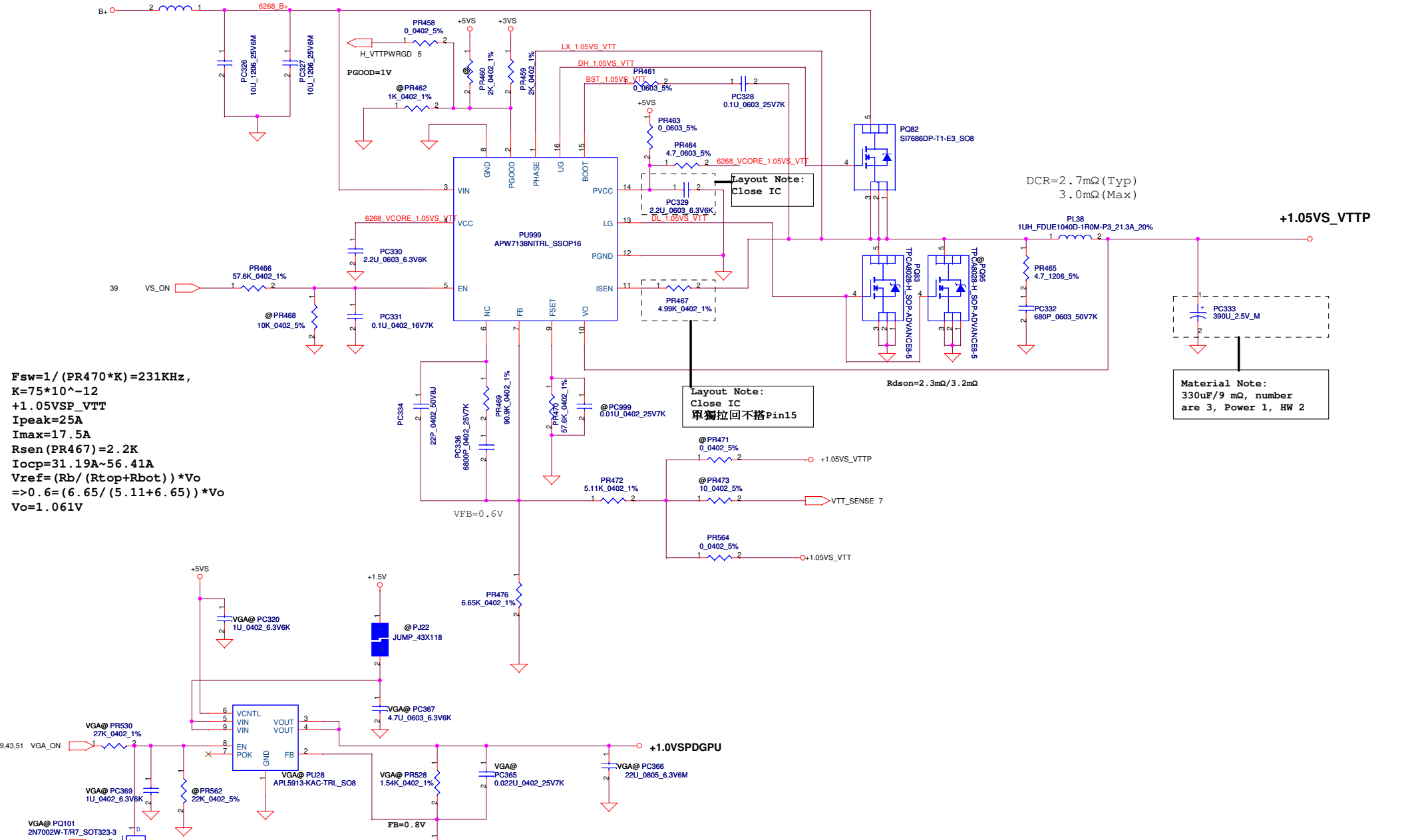
Cesr=15m ohm
 Ipeak=15.82A
 Iocpmin=18.98A
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Freq) = 4.899A$
 $1/2 \Delta I = 2.449A$
 Iocp=18.09A~29.13A

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GPU_VID1	GPU_VID0	Core Voltage Level MADISON PRO	Core Voltage Level PARK XT
1	1	0.90 V	0.93 V
0	1	0.95 V	1.00 V
1	0	1.00 V	1.05 V X
0	0	1.05 V X	1.12 V

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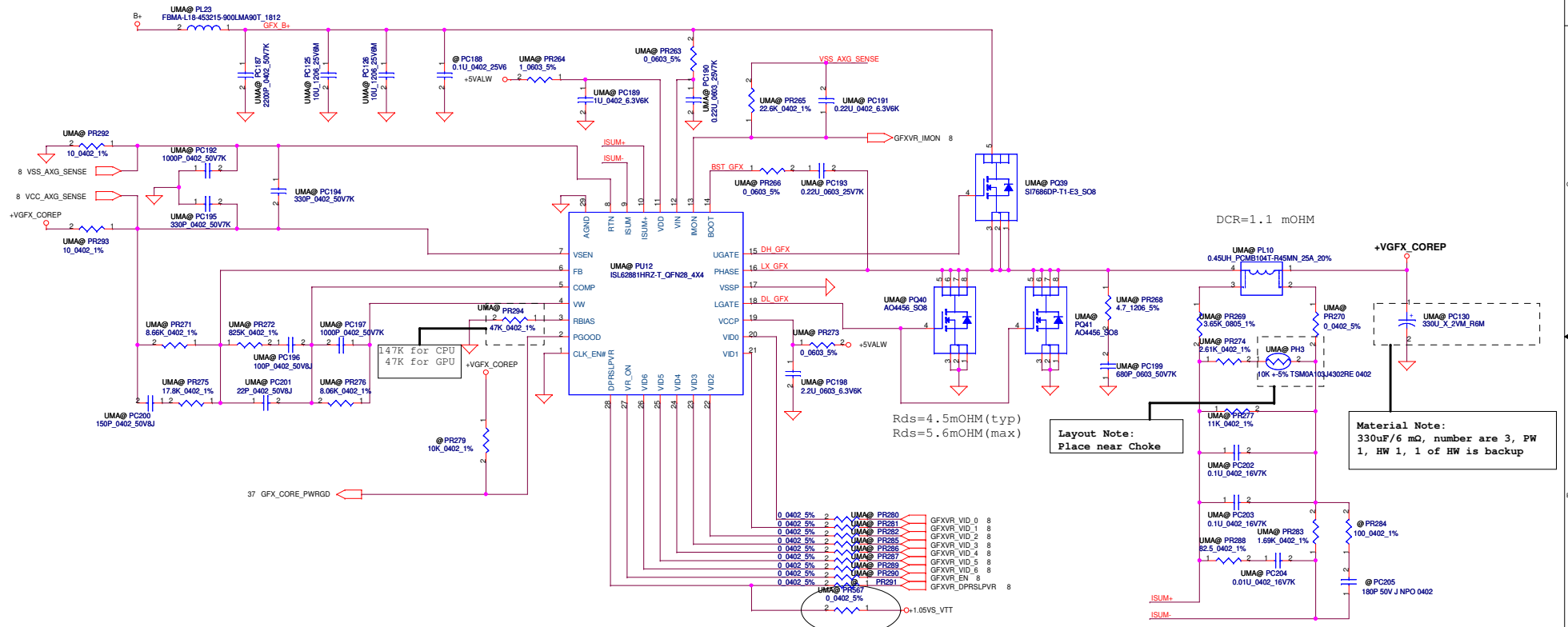
$F_{sw} = 1 / (PR470 * K) = 231KHz,$
 $K = 75 * 10^{-12}$
 $+1.05VSP_VTT$
 $I_{peak} = 25A$
 $I_{max} = 17.5A$
 $R_{sen} (PR467) = 2.2K$
 $I_{ocp} = 31.19A \sim 56.41A$
 $V_{ref} = (R_b / (R_{top} + R_{bot})) * V_o$
 $\Rightarrow 0.6 = (6.65 / (5.11 + 6.65)) * V_o$
 $V_o = 1.061V$

Layout Note:
 Close IC
 單獨拉回不搭Pin15

Material Note:
 330uF/9 mΩ, number
 are 3, Power 1, HW 2

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Intel Aburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum)=0.617$
 where $Rn=PR277 // (PR274+PH3)=5.875k\ ohm$
 $Rsum=PR269=3.65k\ ohm$
 $LL=2*Rdroop*G1*DCR/Ri=6.96m\ V/A$
 where $Rdroop=PR271=8.66k\ ohm$, $Ri=PR283=1.69k\ ohm$
 $Iocp=OCP\ Threshold*Rdroop/LL=24.89A$



Layout Note:
Place near Choke

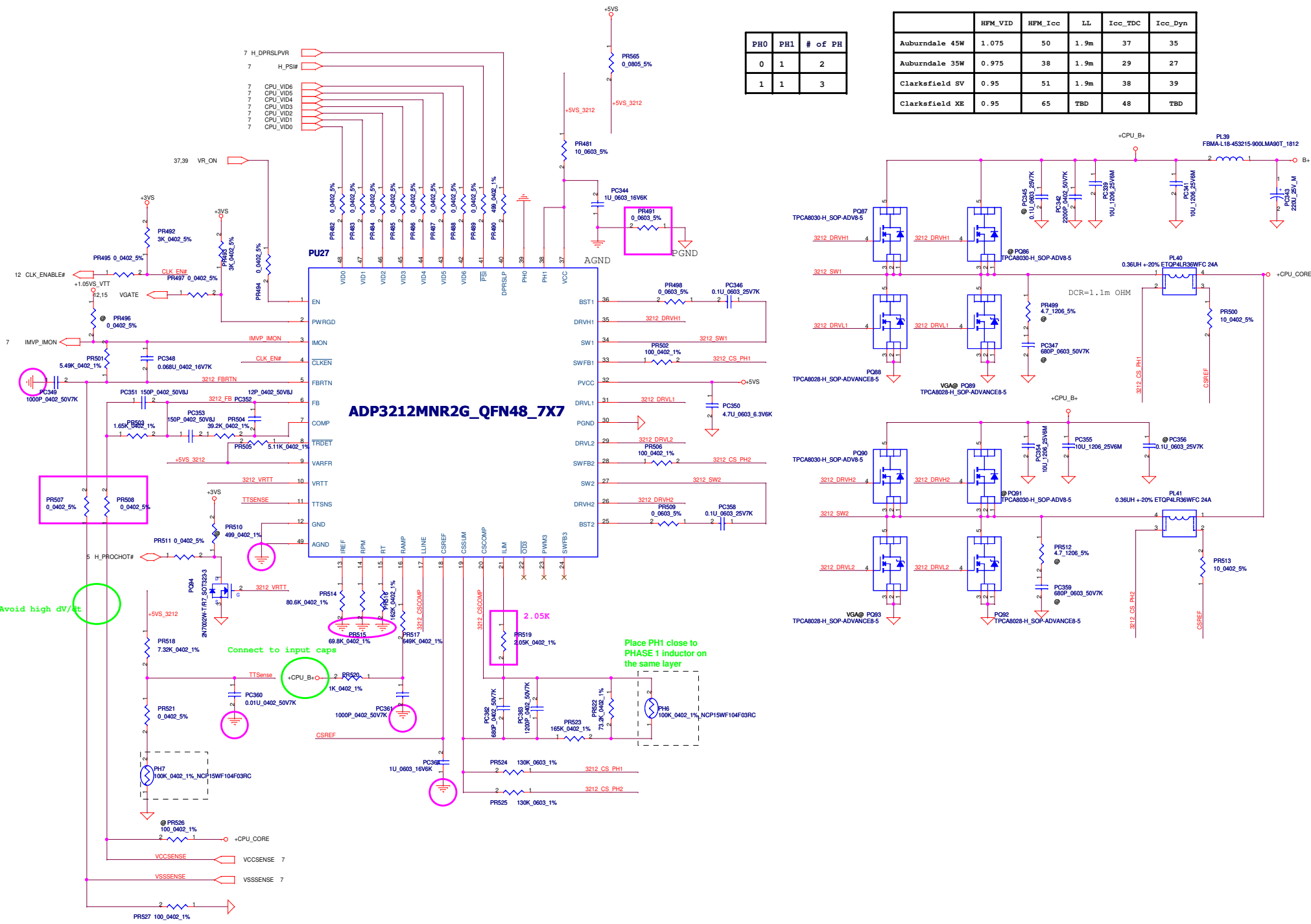
Material Note:
330uF/6 mΩ, number are 3, PW
1, HW 1, 1 of HW is backup

2009-1214 common circuit modify.

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Size	C	Rev	1.0	

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_FDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Avoid high dV/dt

Connect to input caps

Place PH1 close to PHASE 1 inductor on the same layer

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
13	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004080(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
14	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280.	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC273 SE075103K80 PC275 SE000000I10 Delete PC272 SE107475K80, PC271 SE107105M80	2009-1029	to DVT
17	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Change PR196 from SD034442280 to SD034365280. Change PL14 from SL200000V00 to SH000005680	2009-1029	to DVT
18	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
19	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N S08)	2009-1029	to DVT
20	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7866DP-T1-E3 1N POWERPAK S08)	2009-1029	to DVT
21	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000200 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
22	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU choke TOHO quality issue.	Because TOHO has quality issue before, change to Panasonic choke.	0.2	54	Change PL40/PL41 from SHSH00000F000 S COIL 0.36UH +-20% SF-1104-R36 23A to SH000005680 S COIL 0.36UH +-20% PCMC104T-R36MN1R17	2009-1029	to DVT
2	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Change PR197 from SD034649280 to SD034432280.	2009-1029	to DVT
3	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Chnage PR198 from SD034953180 to SD034887180.	2009-1029	to DVT
4	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	CHange PR201 from SD034316280 to SD034255280.	2009-1029	to DVT
5	+VGA_COREP, initial state unknow.	When VGA_CORE start up, but VBIOS doesn't ready, the VID is unknow, add pull down R.	0.2	51	Add PR557/PR560 SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
6	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PC369 from SE076104K80 to SE000000K80 (S CER CAP 1U 0402 X7R)	2009-1029	to DVT
7	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PR530 from SD028150380 to SD034270280 (S RES 1/16W 27K 0402 1%)	2009-1029	to DVT
8	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Delete PR562 SD028220280 (S RES 1/16W 22K +-5% 0402)	2009-1029	to DVT
9	+0.75VSP,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	49	Change PR409 SD028000080 to SD034249280 (24.9K 0402 1%)	2009-1029	to DVT
10	=1.8VSP, voltage too small.	Because +1.8VSP drop in HW side, increase +1.8VSP.	0.2	49	Change PC287 from SE076104K80 to SE000000K80 Change PR405 from SD034316380(S RES 1/16W 316K +-1% 0402) to SD034309380(S RES 1/16W 309K 0402 1%)	2009-1029	to DVT
11	+GFX_COREP, spike voltage issue.	Because GFX_COREP has spike voltage issue, originally we add a schottcky diode to solve it, but Intel's command is that do not add it, because of overdriving, so delete it now.	0.3	53	Delete PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1104	to DVT
12	+GFX_COREP, EMI request.	EMI request to add snubber.	0.3	53	Add PR268 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC199 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
13	+1.05VSV_VTTP, EMI request.	EMI request to add snubber.	0.3	52	Add PR465 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC332 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
14	+VGA_COREP, EMI request.	EMI request to add snubber.	0.3	51	Add PR191 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC171 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
15	+1.5VP, EMI request.	EMI request to add snubber.	0.3	50	Add PR415 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC294 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
16	Charger, EMI request.	EMI request to add snubber.	0.3	47	Add PR370 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC262 SE074681K80 (S CER CAP 680P 50V K X7R 0402)	2009-1104	to DVT
17	CPU_COREP, transient, load line modify.	CPU_COREP, transient, load line modify.	0.3	54	Change PR524/PR525 from SD014120380 to SD014130380. Change PR501 from SD034536180 to SD034549180 Change PC362 from SE074391K80 to SE074681K80	2009-1104	to DVT
18	+VSBP, EMI request.	EMI request to add cap to reduce EMI noise on B+	0.3	45	Change PL40/PL41 from SH000005680 to SH12036BM00. Add PC221 SE000005280 S CER CAP .22U 25V K X7R 0603. Add PC222 SE042104K80 S CER CAP .1U 25V K X7R 0603	2009-1104	to DVT
19	+1.8VSP BOM error.	Loss +1.8VSP enable circiut.	0.3	49	Add PR401 SD014220280 S RES 1/16W 22K 0402 5% Add PC274 SE026474K80 S CER CAP 0.47U 16V K X7R 0603	2009-1104	to DVT
20	+VGA_COREP, output voltage change.	Because ATI change Park output voltage, we saperate Park and Madison by PAK@ and MAD@. And Change Madison X63 BOM.	0.4	51	Change PR197 from SD034432280 to SD034681280. Chnage PR198 from SD034887180 to SD034953180. Change PR201 SD034255280 to SD034316280.	2009-1113	to DVT
21	+CPU_COREP, power measure.	Because HW want to measure CPU_CORE IC power loss, Add 0805 R to saperate +5VS.	0.4	54	Add PR565 SD002000080 S RES 1/8W 0 +-5% 0805	2009-1113	to DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	+CPU_COREP, IMON design change.	Intel release IMON RC time constant new request, change PC348 to 0.068u to meet spec.	0.4	54	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
2	+CPU_COREP, cost issue.	SF000000G80 will cost up, change to SF22004M210.	0.4	54	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
3	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.5	46	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC ESR15	2009-1118	to DVT
4	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.5	52	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0M20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M-P3 21.3A	2009-1118	to DVT
5	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 requirement.	0.6	51	Add PC172 SE071220J80 S CER CAP 22P 50V J NPO 0402 Add PC174 SE075682K80 S CER CAP 6800P 25V K X7R 0402 Add PR195 SD034909280 S RES 1/16W 90.9K 0402 1%	2009-1208	to PVT
6	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 requirement.	0.6	51	Change location PU23 to PU998.	2009-1208	to PVT
7	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.6	52	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA000020600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
8	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.6	52	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
9	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.6	45	Add PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2009-1208	to PVT
10	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1K to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.6	45	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
11	BOM error.	+1.8VSP choke use wrong material.	0.6	49	Change PL30 from SH000006I80 S COIL 2.2UH +-20% PCMC063T-2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2009-1208	to PVT
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A --> B Change List

1012:-----
Page 29,30 Update F1,F2 symbol to SP04301P120(F_SMD1812P110TF)
Page 36,38 C789,C788,C684 symbol update (have pin define)
Page 31, U3 P/N change from SA00001RM00 to SA00003O900
1102:-----
Page 7,8 C97,C675,C134,C136,C251,C268,C541,C667 symbol update from SGA00002380 to SGA00002U00
Page 23. Add C609 0.1u_0402(SE076104K80) R739 24K_0402(SD034240280) fix +3VSDGPU Ramp up issue
Page 17,35 Add 1 more USB trace to 3G/B connector from PCH USB20_P10 & USB20_N10
1103:-----
Page 43 R200 change symbol from 22_0402_5% to 22_0603_5%
Page 39 SW1,SW4 BOM structure change to @
Page 36 C789.2 power source +3VS change to +3VALW
1104:-----
Page 8, Add C797,C798,C799,C800 0.1u_0402 at between +1.5V&+1.5V_1(Intel suggest)
Page 15,37 U41.F3 modify net from GPIO62 to susclk
Page 37 Add R740(@) close U32.123
1105:-----
Page 8 R98 change from 4.7K_0402_5% to 330ohm_0402_5% (Intel feekback VGFX_CORE issue solution)
1109:-----
Page 23 Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
Page 24 Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Page 23 Remove and short R729 (A2VDD)
Page 23 Change C600,C172,C599 BOM structure from VGA@ to @ (+A2VDD)
Page 23 Remove and short L6 (+A2VDDQ)
Page 26 Remove and short R730,R731,R732,R733,R734,R735,R736,R737,R738, (DPB,DPC,DPD power source)
Page 37 Add R508 100K_0402 Pull down to GND(EC E51TXD_P80DATA)(fix Intel WLAN Card reset issue)
RF request:-----
Page 35 Add C801 (SE071470J80 47P_0402) and C173(SE000005T80 10U_0603)(+3VS_WWAN)
Page 23 Remove R508 (100_0402) change to C802(@) (12P_0402_50V8J)(SE071120J80) (VGA_CLK_27M)
Page 29 Add two shunt C804,C803 12P_0402_50V8J(SE071120J80)(P31.DDC to HDMI conn)
Page 29 Add two shunt C805,C806 22P_0402_50V8J(SE071220J80)(P29.LCD Conn)
pop R403(47_0402) and C516 (22P_0402)(CLK_PCI_LPC)
pop R163 (10_0402)and C319 (10P_0402) (CLK_BUF_ICH_14M)
EMI request:-----
Page 36 POP D26, CM1293-04SO(SC300000O00)
Page 38,40,41 POP D18,D19,D10,D9,D11,D28,D30 PJDLC05C(SCA00001100)
1110:-----
Page 38 Add Q53(ACIN_LED#)
1111:-----
Page 40 C775,C776,C777,C778 change Symbol from SE093475K80(4.7U_0805) to SE107475M80(4.7U_0603)
Page 38 R341,R343 100_0402_5% change to 680_0402_5%(BLUE LED Bright)
Page 38 R342,R344 300_0402_5% change to 3.9K_0402_5%(Orange LED Bright)
1113:-----
Page 8 R98 change from 330_0402_5% to 470_0402_5%(SD028470080)
Page 23 Change back R717,R718,R720,R509 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Page 24 Change back R64 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
1116:-----
Page 13 U41 change P/N from SA00003N700 to SA00003N7B0
Page 34 T16 change P/N from SP050006C00 to SP050006B00
1117:-----
Page 58 Add HW PIR

B --> C Change List

1209:-----
R679 change BOM structure to @
D13,D15 change BOM structure to @
Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Add R729 0_0402(SD028000080,@)
Add R730 0_0402(SD028000080,@) LOCAL_DIM for Panel new feature
Add R731 0_0402(SD028000080,@) COLOR_ENG_EN for Panel new feature
Add R732 100K_0402(SD028100380)LOCAL_DIM PD to GND
Add R733 100K_0402(SD028100380)COLOR_ENG_EN PD to GND
Q53 change BOM structure to @
ADD Q54 2N7002DWH_SOT363-6(SB00000AR10) for AC PLUG HDD LED flash issue
DEL U16 for AC PLUG HDD LED flash issue
C97,C134,C136,C251,C541,C268,C675,C667 symbol update from SGA00002U00 to SGA00001Q80
C775,C776,C777,C778 change P/N SE107475M80 to SE107475K80(4.7U_0603_6.3V6K)
R272(100K PU +3VS) change BOM structure to @
Add U32.85 WWAN_LED# (input)
Add U32.17 MINI1_LED# (input)
ADD R734 PD to GND (fix CPT Panel Flash issue)

1211:-----
ADD C807,C808 1000P_0402(SE074102K80) LAN EMI
ADD C610 0.1U_0402 Y5V(SE070104Z80) VGFX_CORE EMI
ADD C809 C810 0.1U_0402 Y5V(SE070104Z80) +1.5V EMI
1211B:-----
Add U32.36 WLAN_LED# (output)
Add U32.91 3G_LED# (output)
Add U32.85 WWAN_LED# (input)
1214:-----
ADD R735 For U24 power source +3VS (POP)
ADD R736 For U24 power source +5VS (@)
1215:-----
ADD R737 asmedia CLK-
ADD R738 asmedia CLK+
U24 PN change to SA00000U500 (74AHC1G125GW_SOT353-5)
1216:-----
C465 change BOM structure to @(3G 150U)
R41 change BOM structure to @(CRT DET)
Q20 change BOM structure to @(CRT DET)
R343,R341 change to 2.2K_0402_5%(SD028220180) (LED)
R334 change to 249K_0402_1%(SD034249380)
1217:-----
R253 2.2K_0402_5% change to @
R252 2.2K_0402_5% change to UMAHD@
R343 change to 2.2K_0402_5%(7080@) 680_0402_5%(90@)
R344 change to 3.9K_0402_5%(7080@) 680_0402_5%(90@)
R341 change to 2.2K_0402_5%(7080@) 680_0402_5%(90@)
R342 change to 3.9K_0402_5%(7080@) 680_0402_5%(90@)
1219:
R382 change to 18K_0402(SD028180280)(Board ID)
R389 ADD 100K_0402_5%(SD028100380) PH +3VALW(Board ID)
1223:
R157 change to R167 10K_0402_5% (GPIO66: L:6L H:8L)
GPIO21 define to Project ID (L:NEW50/70/80/90 H:NEW71/91)


C --> MP Change List

1228:
MB PCB P/N (DA80000H700)change to (DAZ0C900100)
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000AR10 to SB00000D900
DEL D10 (Int. MIC ESD Diode PASS Can remove)
R382 change to 18K_0402_5%(SD028180280 Board ID rev0.3)
DEL R667,R668(SD028000080) USb common mode choke
DEL R167,(SD028100280)(GPIO66 PH 8L,PD 6L) 10K_0402_5%
ADD R157 (SD028100280)(GPIO66 PH 8L,PD 6L) 10K_0402_5%
ADD R389 (SD028100380)(Board ID)100K_0402_5%
ADD L68(SM070001600 12ohm bead) USB common mode choke
Modify U24 Symbol


0104:
ADD R350 100K_0402_5%(SD028100380)(3G PH +3VS_WWAN)
0107:
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000D900 to SB00000DH00

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				Date:	Friday, January 08, 2010	Sheet 58 of 59


VGA


U34
 PARK XT M2 A11: SA00003MC10
 216-0774007 A11 PARK XT M2


PCB


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 LA-5891P MB Rev0: DA80000H700
 LA-5891P MB Rev1: DA80000H710
 LA-5891P MB with Small Board Rev1: DAZ0C900100
 LA-5891P REV1 M/B


X76


ZZZ

 X76198BOL01 VRAM 512M SAM NEW70
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ

 X76198BOL02 VRAM 512M HYN NEW70
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

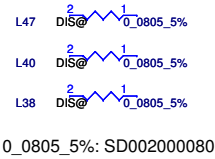
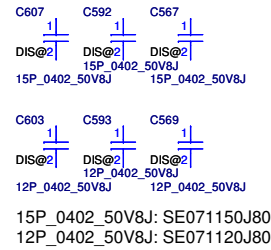
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 X76198BOL03 VRAM 1G SAM NEW70
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

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 X76198BOL04 VRAM 1G HYN NEW70
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

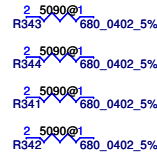
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 X76198BOL05 VRAM 512M AMD NEW70
 AMD :SA00003PF10
 (S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

ZZZ

 X76198BOL06 VRAM 1G AMD NEW70
 AMD :SA00003PF10
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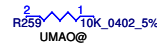
CRT Option Components



NEW90 LED Option



PCH SKU Option



GPIO19

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