

MS-7788 Ver: 1.0 u-ATX : 226 * 173 mm

CPU:

Intel - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:ALC887VD / VT1708SCE

LAN:RTL 8105E 10/100 , Co-lay 8111E 10/100/1000

SIO:FIN71868AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PWM:

Controller: UT501 3+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: UP1504

CPU SA : OP+MOS

DDR: UP1504

PCH: OP+MOS

ACPI:

UPI

Other:

SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x4

D-SUB/DVI*1

TPM Header *1

Speaker Pin Header

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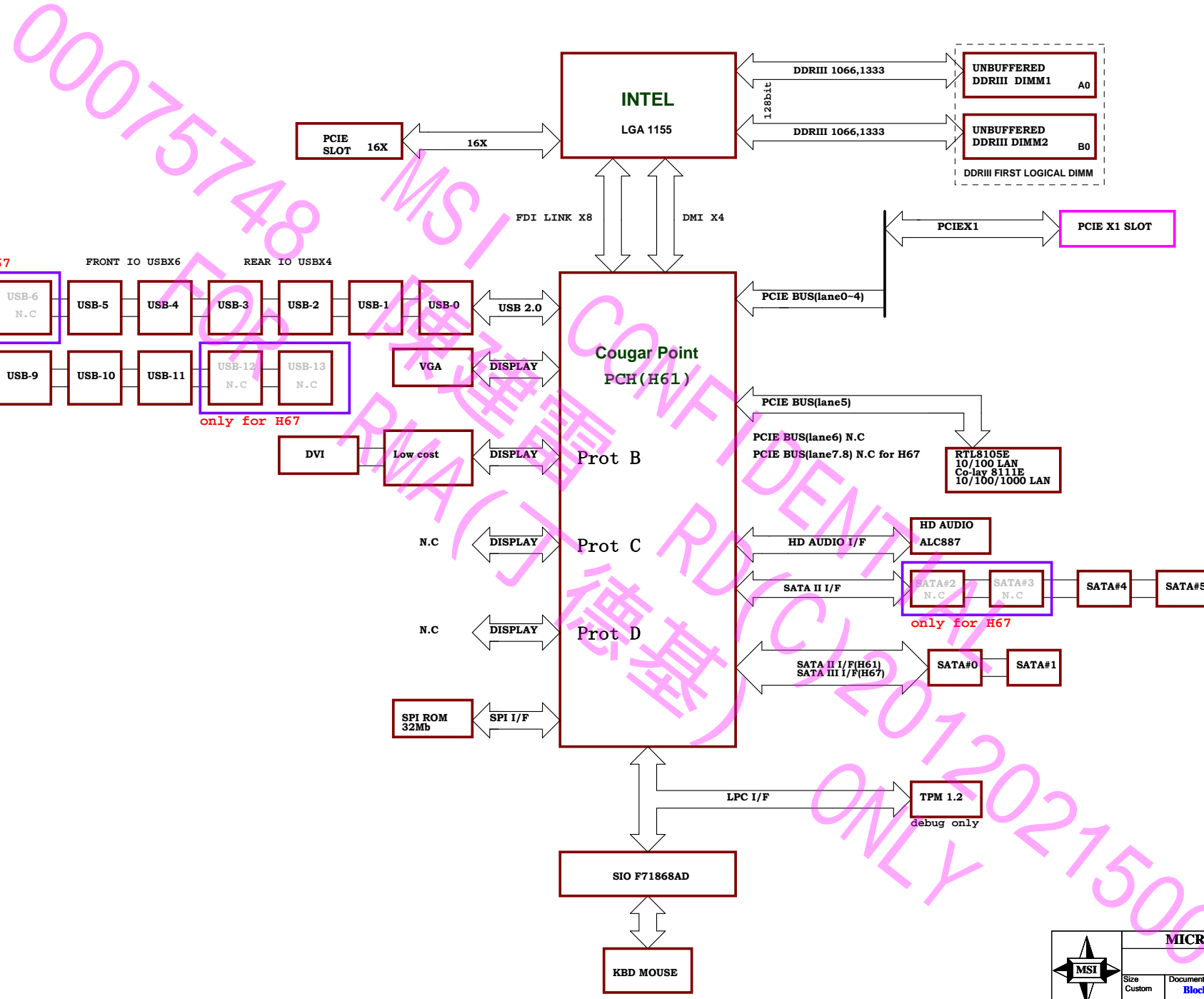


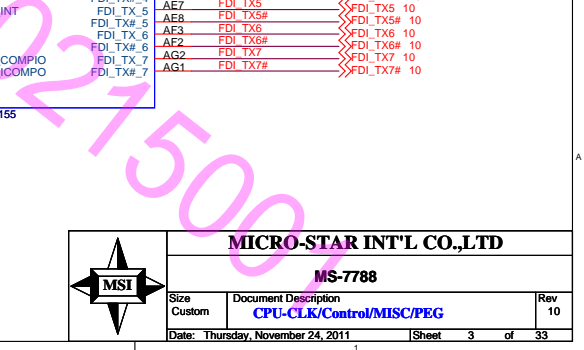
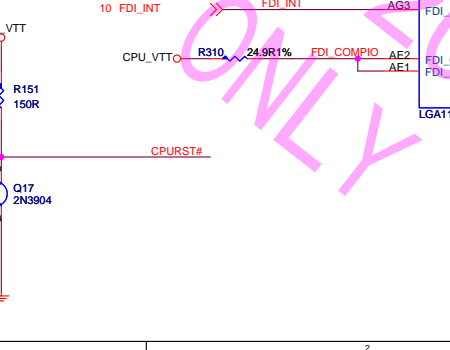
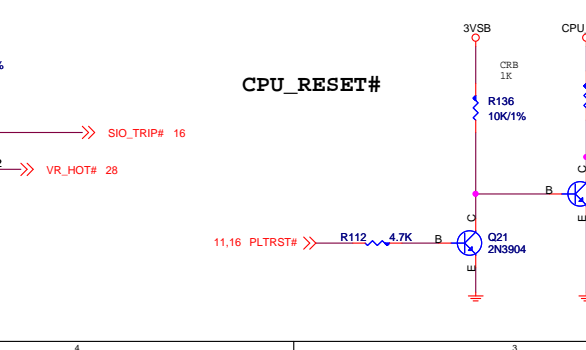
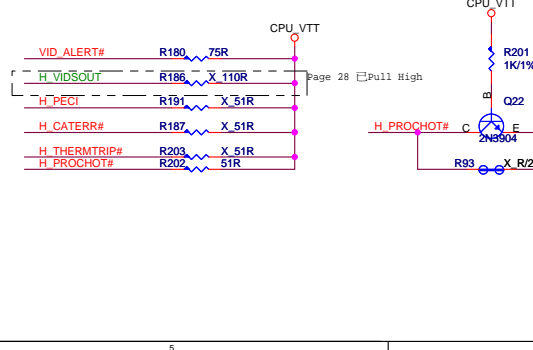
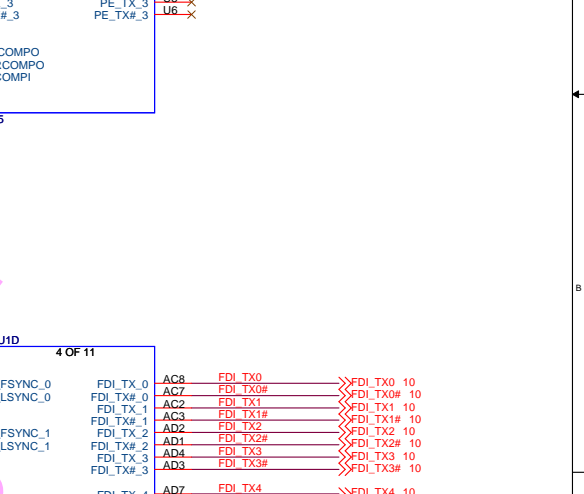
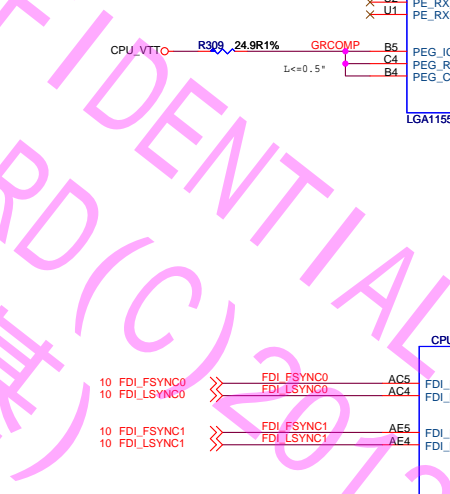
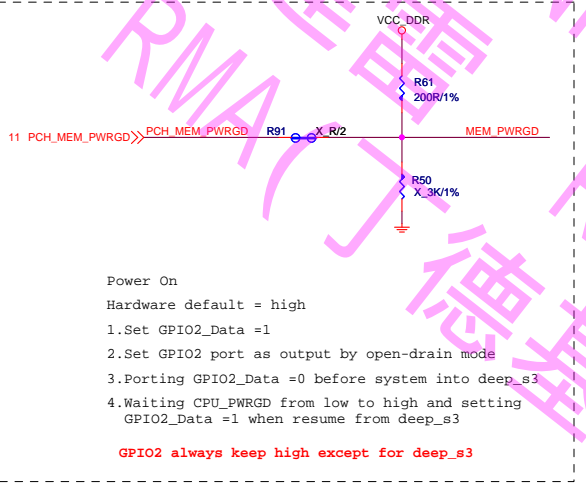
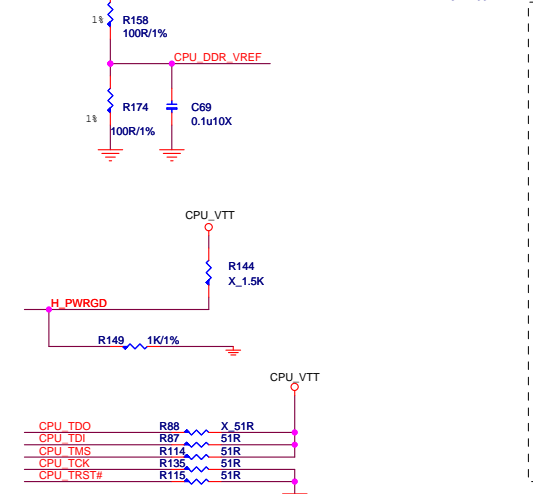
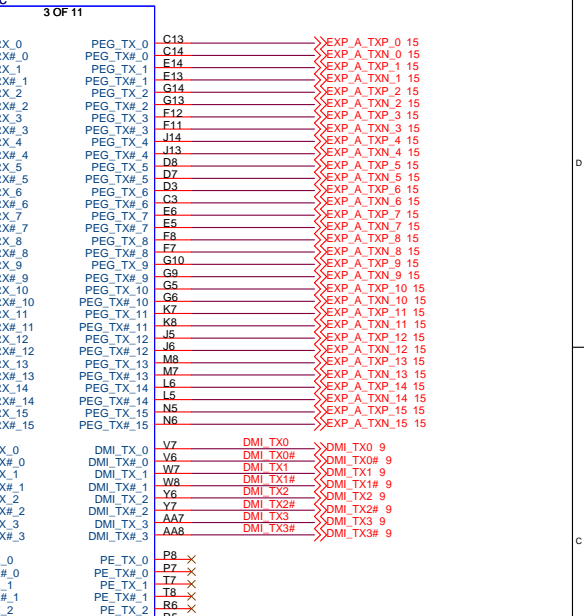
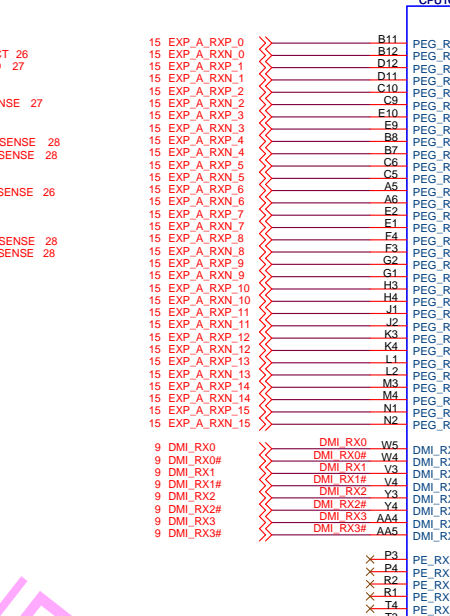
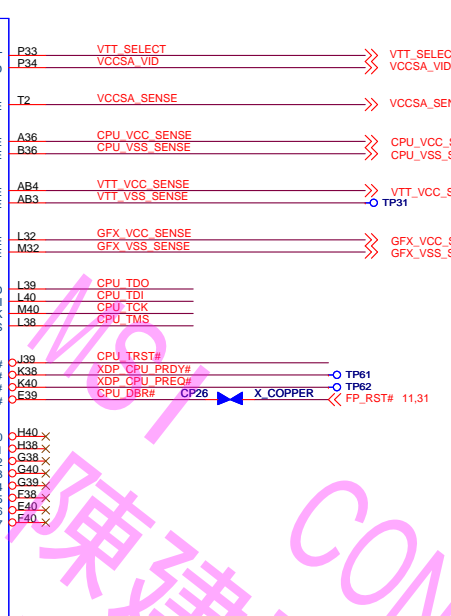
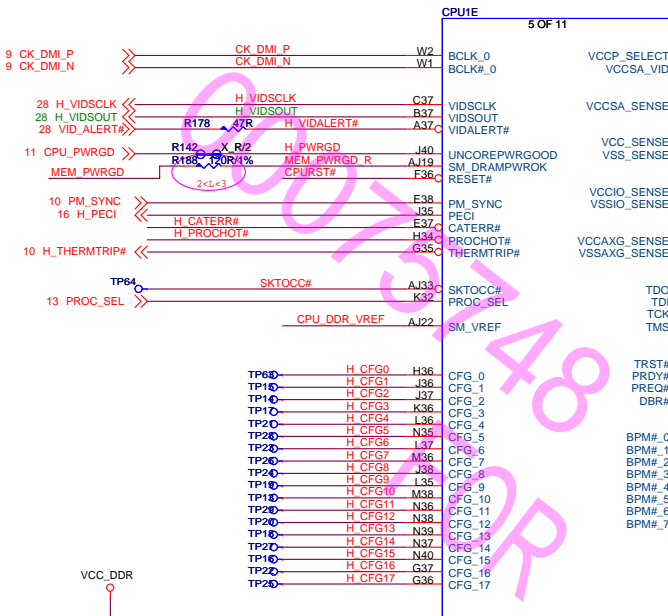
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Power On
Hardware default = high

1. Set GPIO2_Data = 1
2. Set GPIO2 port as output by open-drain mode
3. Porting GPIO2_Data = 0 before system into deep_s3
4. Waiting CPU_PWRGD from low to high and setting GPIO2_Data = 1 when resume from deep_s3

GPIO2 always keep high except for deep_s3

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7 MEM_MA_ADD[15..0]

MEM_MA_ADD0 AV27
MEM_MA_ADD1 AV24
MEM_MA_ADD2 AW24
MEM_MA_ADD3 AW23
MEM_MA_ADD4 AV23
MEM_MA_ADD5 AT24
MEM_MA_ADD6 AT23
MEM_MA_ADD7 AU22
MEM_MA_ADD8 AV22
MEM_MA_ADD9 AT22
MEM_MA_ADD10 AV20
MEM_MA_ADD11 AU21
MEM_MA_ADD12 AT21
MEM_MA_ADD13 AW20
MEM_MA_ADD14 AU20
MEM_MA_ADD15 AT20

CPU1A 1 OF 11

SA_MA_0 SA_DQ_0
SA_MA_1 SA_DQ_1
SA_MA_2 SA_DQ_2
SA_MA_3 SA_DQ_3
SA_MA_4 SA_DQ_4
SA_MA_5 SA_DQ_5
SA_MA_6 SA_DQ_6
SA_MA_7 SA_DQ_7
SA_MA_8 SA_DQ_8
SA_MA_9 SA_DQ_9
SA_MA_10 SA_DQ_10
SA_MA_11 SA_DQ_11
SA_MA_12 SA_DQ_12
SA_MA_13 SA_DQ_13
SA_MA_14 SA_DQ_14
SA_MA_15 SA_DQ_15

AJ3 MEM_MA_DATA0
AJ4 MEM_MA_DATA1
AL3 MEM_MA_DATA2
AL4 MEM_MA_DATA3
AJ2 MEM_MA_DATA4
AJ1 MEM_MA_DATA5
AL2 MEM_MA_DATA6
AL1 MEM_MA_DATA7
AN1 MEM_MA_DATA8
AN4 MEM_MA_DATA9
AR3 MEM_MA_DATA10
AR4 MEM_MA_DATA11
AN2 MEM_MA_DATA12
AN3 MEM_MA_DATA13
AR2 MEM_MA_DATA14
AR1 MEM_MA_DATA15
AV2 MEM_MA_DATA16

MEM_MA_DATA[63..0] 7

SA_WE# MEM_MA_DATA17
AV5 MEM_MA_DATA18
AW5 MEM_MA_DATA19
AU2 MEM_MA_DATA20
AU3 MEM_MA_DATA21
AV5 MEM_MA_DATA22
AV5 MEM_MA_DATA23
AV7 MEM_MA_DATA24
AV9 MEM_MA_DATA25
AU9 MEM_MA_DATA27
AV7 MEM_MA_DATA28
AW7 MEM_MA_DATA29
AW9 MEM_MA_DATA30
AW9 MEM_MA_DATA31
AU35 MEM_MA_DATA32
AW32 MEM_MA_DATA33
AU39 MEM_MA_DATA34
AU36 MEM_MA_DATA35
AW35 MEM_MA_DATA36
AY36 MEM_MA_DATA37
AU38 MEM_MA_DATA38
AU37 MEM_MA_DATA39
AR40 MEM_MA_DATA40
AR37 MEM_MA_DATA41
AN37 MEM_MA_DATA42
AR39 MEM_MA_DATA43
AR39 MEM_MA_DATA44
AR38 MEM_MA_DATA45
AN39 MEM_MA_DATA46
AN40 MEM_MA_DATA47
AL40 MEM_MA_DATA48
AL37 MEM_MA_DATA49
AJ38 MEM_MA_DATA50
AJ37 MEM_MA_DATA51
AL39 MEM_MA_DATA52
AL38 MEM_MA_DATA53
AJ39 MEM_MA_DATA54
AJ40 MEM_MA_DATA55
AG40 MEM_MA_DATA56
AG37 MEM_MA_DATA57
AE38 MEM_MA_DATA58
AE37 MEM_MA_DATA59
AG39 MEM_MA_DATA60
AG38 MEM_MA_DATA61
AE39 MEM_MA_DATA62
AE40 MEM_MA_DATA63

SA_WE# MEM_MA_DATA17
SA_CAS# MEM_MA_DATA18
SA_RAS# MEM_MA_DATA19
SA_BS_0 MEM_MA_BANK0
SA_BS_1 MEM_MA_BANK1
SA_BS_2 MEM_MA_BANK2

MEM_MA_CS_L0 MEM_MA_CS_L0
MEM_MA_CS_L1 MEM_MA_CS_L1
MEM_MA_CS_1 MEM_MA_CS_1
MEM_MA_CS_2 MEM_MA_CS_2
MEM_MA_CS_3 MEM_MA_CS_3

MEM_MA_CKE0 MEM_MA_CKE0
MEM_MA_CKE1 MEM_MA_CKE1

MEM_MA_ODT0 MEM_MA_ODT0
MEM_MA_ODT1 MEM_MA_ODT1

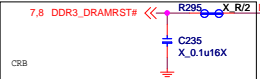
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MEM_MA_CLK_H1 MEM_MA_CLK_H1
MEM_MA_CLK_L1 MEM_MA_CLK_L1

MEM_MA_DRAMRST# MEM_MA_DRAMRST#

MEM_MA_DQS_8 MEM_MA_DQS_8
MEM_MA_DQS_H0 MEM_MA_DQS_H0
MEM_MA_DQS_H1 MEM_MA_DQS_H1
MEM_MA_DQS_H2 MEM_MA_DQS_H2
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MEM_MA_DQS_H4 MEM_MA_DQS_H4
MEM_MA_DQS_H5 MEM_MA_DQS_H5
MEM_MA_DQS_H6 MEM_MA_DQS_H6
MEM_MA_DQS_H7 MEM_MA_DQS_H7

MEM_MA_DQS_L0 MEM_MA_DQS_L0
MEM_MA_DQS_L1 MEM_MA_DQS_L1
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MEM_MA_DQS_L6 MEM_MA_DQS_L6
MEM_MA_DQS_L7 MEM_MA_DQS_L7

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MEM_MA_ECC_CB_5 MEM_MA_ECC_CB_5
MEM_MA_ECC_CB_6 MEM_MA_ECC_CB_6
MEM_MA_ECC_CB_7 MEM_MA_ECC_CB_7



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8 MEM_MB_ADD[15..0]

MEM_MB_ADD0 AK24
MEM_MB_ADD1 AM20
MEM_MB_ADD2 AM19
MEM_MB_ADD3 AK18
MEM_MB_ADD4 AP19
MEM_MB_ADD5 AP18
MEM_MB_ADD6 AM18
MEM_MB_ADD7 AL18
MEM_MB_ADD8 AN18
MEM_MB_ADD9 AY17
MEM_MB_ADD10 AN23
MEM_MB_ADD11 AU17
MEM_MB_ADD12 AT18
MEM_MB_ADD13 AR08
MEM_MB_ADD14 AY16
MEM_MB_ADD15 AV16

CPU1B 2 OF 11

SB_MA_0 SB_DQ_0
SB_MA_1 SB_DQ_1
SB_MA_2 SB_DQ_2
SB_MA_3 SB_DQ_3
SB_MA_4 SB_DQ_4
SB_MA_5 SB_DQ_5
SB_MA_6 SB_DQ_6
SB_MA_7 SB_DQ_7
SB_MA_8 SB_DQ_8
SB_MA_9 SB_DQ_9
SB_MA_10 SB_DQ_10
SB_MA_11 SB_DQ_11
SB_MA_12 SB_DQ_12
SB_MA_13 SB_DQ_13
SB_MA_14 SB_DQ_14
SB_MA_15 SB_DQ_15

AG7 MEM_MB_DATA0
AG8 MEM_MB_DATA1
AJ8 MEM_MB_DATA2
AJ9 MEM_MB_DATA3
AG6 MEM_MB_DATA4
AJ6 MEM_MB_DATA5
AJ7 MEM_MB_DATA7
AJ7 MEM_MB_DATA8
AM7 MEM_MB_DATA9
AM10 MEM_MB_DATA10
AL10 MEM_MB_DATA11
AL10 MEM_MB_DATA12
AL6 MEM_MB_DATA13
AL9 MEM_MB_DATA14
AM9 MEM_MB_DATA15
AF7 MEM_MB_DATA16
AR7 MEM_MB_DATA17
AP10 MEM_MB_DATA18
AR10 MEM_MB_DATA19
AP6 MEM_MB_DATA20
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AR9 MEM_MB_DATA22
AP9 MEM_MB_DATA23
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AM13 MEM_MB_DATA25
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AL12 MEM_MB_DATA28
AL13 MEM_MB_DATA29
AR12 MEM_MB_DATA30
AP12 MEM_MB_DATA31
AR28 MEM_MB_DATA32
AR29 MEM_MB_DATA33
AL28 MEM_MB_DATA34
AL29 MEM_MB_DATA35
AP28 MEM_MB_DATA36
AP29 MEM_MB_DATA37
AM28 MEM_MB_DATA38
AM28 MEM_MB_DATA39
AP32 MEM_MB_DATA40
AP31 MEM_MB_DATA41
AR32 MEM_MB_DATA42
AR32 MEM_MB_DATA43
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AL31 MEM_MB_DATA53
AL34 MEM_MB_DATA55
AH35 MEM_MB_DATA56
AH34 MEM_MB_DATA57
AE34 MEM_MB_DATA58
AE35 MEM_MB_DATA59
AJ34 MEM_MB_DATA61
AE36 MEM_MB_DATA62
AE33 MEM_MB_DATA63

SB_WE# MEM_MB_DATA17
SB_CAS# MEM_MB_DATA18
SB_RAS# MEM_MB_DATA19
SB_BS_0 MEM_MB_BANK0
SB_BS_1 MEM_MB_BANK1
SB_BS_2 MEM_MB_BANK2

MEM_MB_CS_L0 MEM_MB_CS_L0
MEM_MB_CS_L1 MEM_MB_CS_L1
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MEM_MB_CS_2 MEM_MB_CS_2
MEM_MB_CS_3 MEM_MB_CS_3

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MEM_MB_ODT0 MEM_MB_ODT0
MEM_MB_ODT1 MEM_MB_ODT1

MEM_MB_CLK_H0 MEM_MB_CLK_H0
MEM_MB_CLK_L0 MEM_MB_CLK_L0
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MEM_MB_CLK_L1 MEM_MB_CLK_L1

MEM_MB_DRAMRST# MEM_MB_DRAMRST#

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LGA1155

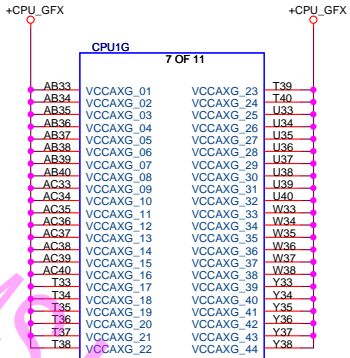
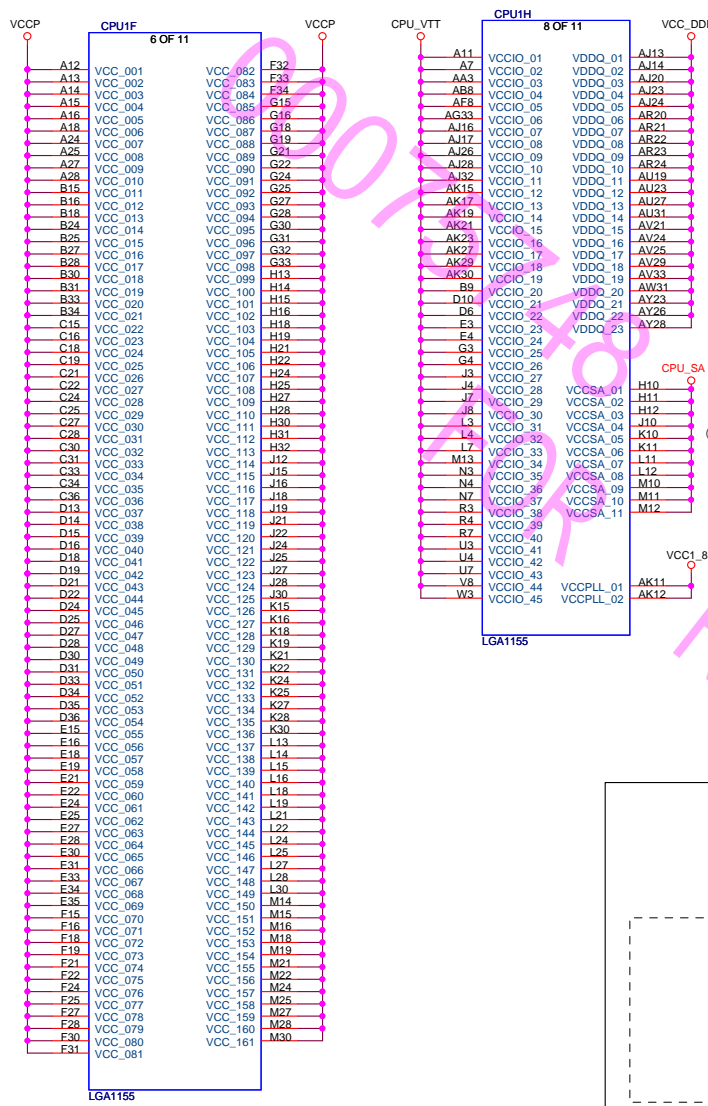


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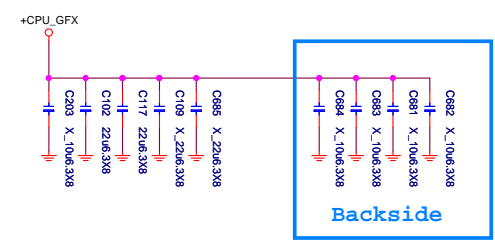
(1.05V / 1.00V)



VCCP: 112A
 CPU_VTT: 8.2A
 CPU_SA: 8.8A
 VCC_DDR: 4.5A
 VCC1_8: 1.6A

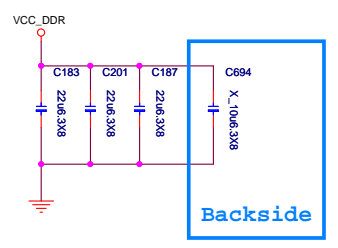
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+CPU_GFX Decoupling



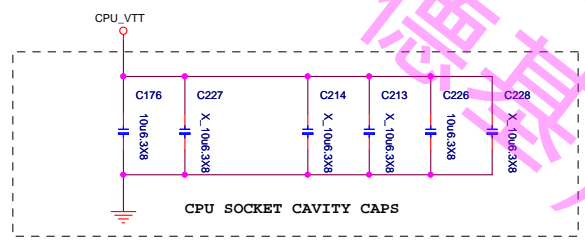
CPU SOCKET CAVITY CAPS

+1.5V_DDR3-Decoupling

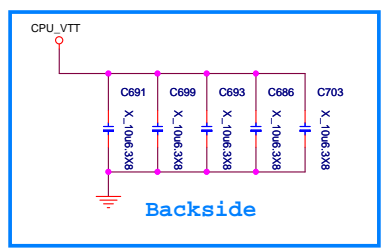


CPU SOCKET CAVITY CAPS

+CPU_VTT Decoupling

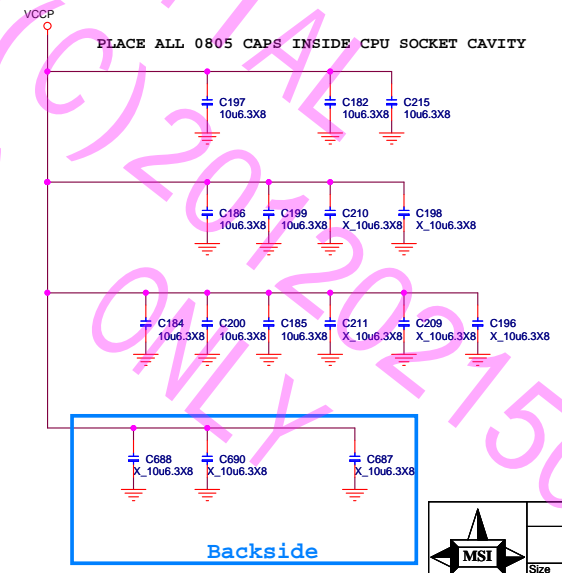


CPU SOCKET CAVITY CAPS



Backside

+CPU_VCCP-Decoupling



Backside

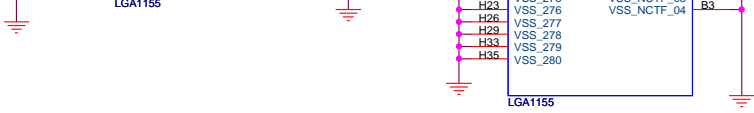
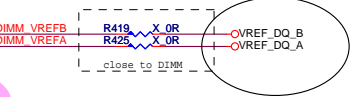


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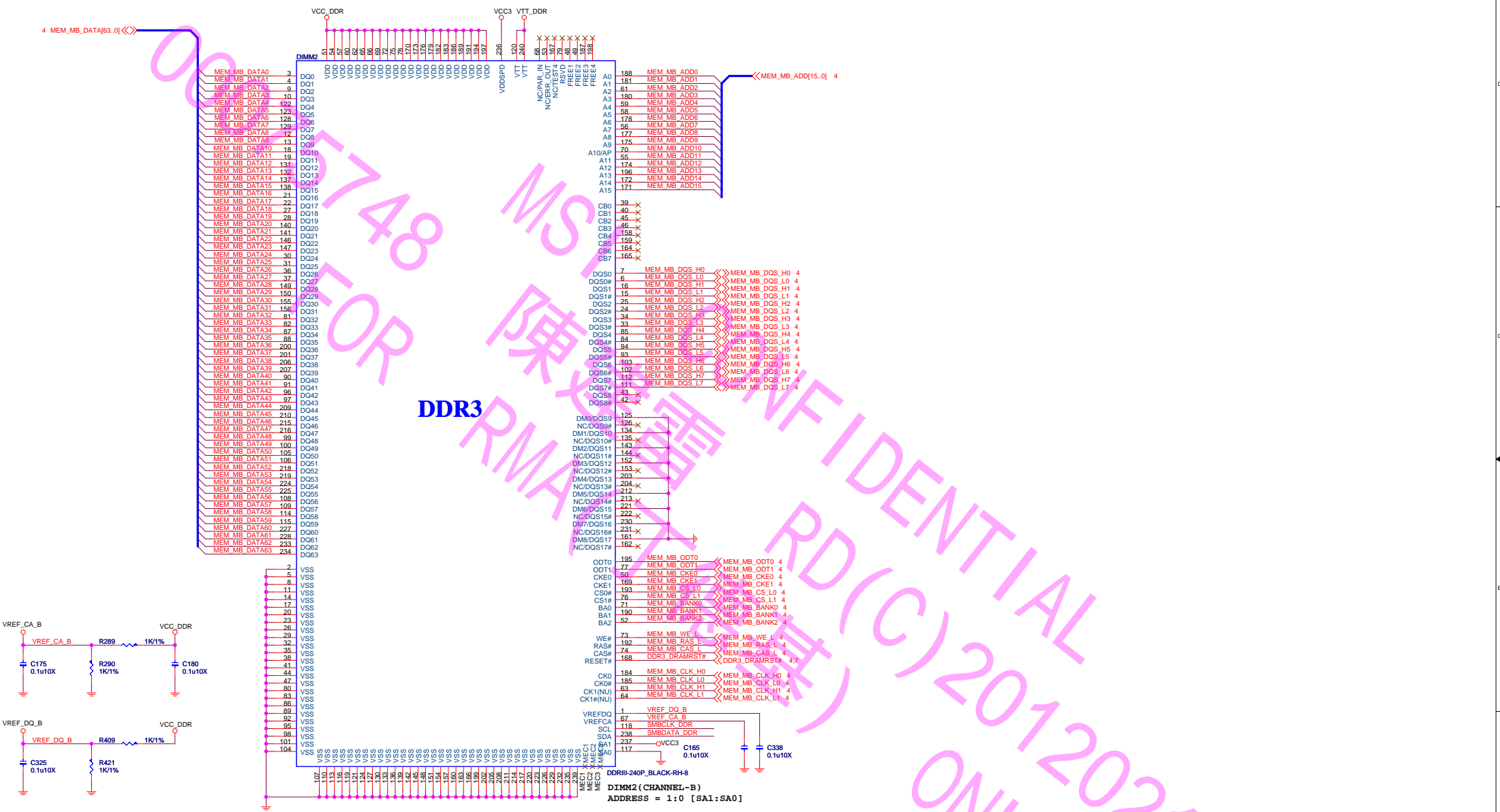
CPU1I 9 OF 11		
A17	VSS_001	VSS_091
A23	VSS_002	VSS_092
A26	VSS_003	VSS_093
A29	VSS_004	VSS_094
A35	VSS_005	VSS_095
AA33	VSS_006	VSS_096
AA34	VSS_007	VSS_097
AA35	VSS_008	VSS_098
AA36	VSS_009	VSS_099
AA37	VSS_010	VSS_100
AA38	VSS_011	VSS_101
AA6	VSS_012	VSS_102
AB5	VSS_013	VSS_103
AC1	VSS_014	VSS_104
AC6	VSS_015	VSS_105
AD33	VSS_016	VSS_106
AD36	VSS_017	VSS_107
AD38	VSS_018	VSS_108
AD39	VSS_019	VSS_109
AD40	VSS_020	VSS_110
AD5	VSS_021	VSS_111
AD8	VSS_022	VSS_112
AE3	VSS_023	VSS_113
AE33	VSS_024	VSS_114
AE36	VSS_025	VSS_115
AF1	VSS_026	VSS_116
AF34	VSS_027	VSS_117
AF36	VSS_028	VSS_118
AF37	VSS_029	VSS_119
AF40	VSS_030	VSS_120
AF5	VSS_031	VSS_121
AF6	VSS_032	VSS_122
AF7	VSS_033	VSS_123
AG36	VSS_034	VSS_124
AH2	VSS_035	VSS_125
AH3	VSS_036	VSS_126
AH33	VSS_037	VSS_127
AH36	VSS_038	VSS_128
AH37	VSS_039	VSS_129
AH38	VSS_040	VSS_130
AH39	VSS_041	VSS_131
AH40	VSS_042	VSS_132
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AH8	VSS_044	VSS_134
AJ12	VSS_045	VSS_135
AJ15	VSS_046	VSS_136
AJ18	VSS_047	VSS_137
AJ21	VSS_048	VSS_138
AJ25	VSS_049	VSS_139
AJ27	VSS_050	VSS_140
AJ36	VSS_051	VSS_141
AJ5	VSS_052	VSS_142
AK1	VSS_053	VSS_143
AK10	VSS_054	VSS_144
AK13	VSS_055	VSS_145
AK14	VSS_056	VSS_146
AK16	VSS_057	VSS_147
AK22	VSS_058	VSS_148
AK28	VSS_059	VSS_149
AK31	VSS_060	VSS_150
AK32	VSS_061	VSS_151
AK33	VSS_062	VSS_152
AK34	VSS_063	VSS_153
AK35	VSS_064	VSS_154
AK36	VSS_065	VSS_155
AK37	VSS_066	VSS_156
AK4	VSS_067	VSS_157
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AK7	VSS_071	VSS_161
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AL17	VSS_076	VSS_166
AL19	VSS_077	VSS_167
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AM14	VSS_085	VSS_175
AM17	VSS_086	VSS_176
AM2	VSS_087	VSS_177
AM21	VSS_088	VSS_178
AM23	VSS_089	VSS_179
AM25	VSS_090	VSS_180

CPU1J 10 OF 11		
AV11	VSS_181	VSS_281
AV14	VSS_182	VSS_282
AV17	VSS_183	VSS_283
AV3	VSS_184	VSS_284
AV35	VSS_185	VSS_285
AV38	VSS_186	VSS_286
AV6	VSS_187	VSS_287
AW10	VSS_188	VSS_288
AW11	VSS_189	VSS_289
AW14	VSS_190	VSS_290
AW16	VSS_191	VSS_291
AW36	VSS_192	VSS_292
AW6	VSS_193	VSS_293
AY11	VSS_194	VSS_294
AY14	VSS_195	VSS_295
AY17	VSS_196	VSS_296
AY35	VSS_197	VSS_297
AY4	VSS_198	VSS_298
AY6	VSS_199	VSS_299
AY8	VSS_200	VSS_300
B10	VSS_201	VSS_301
B13	VSS_202	VSS_302
B14	VSS_203	VSS_303
B17	VSS_204	VSS_304
B23	VSS_205	VSS_305
B26	VSS_206	VSS_306
B29	VSS_207	VSS_307
B32	VSS_208	VSS_308
B35	VSS_209	VSS_309
B38	VSS_210	VSS_310
B6	VSS_211	VSS_311
C11	VSS_212	VSS_312
C12	VSS_213	VSS_313
C17	VSS_214	VSS_314
C14	VSS_215	VSS_315
C23	VSS_216	VSS_316
C26	VSS_217	VSS_317
C29	VSS_218	VSS_318
C32	VSS_219	VSS_319
C35	VSS_220	VSS_320
C7	VSS_221	VSS_321
C8	VSS_222	VSS_322
D17	VSS_223	VSS_323
D2	VSS_224	VSS_324
D20	VSS_225	VSS_325
D23	VSS_226	VSS_326
D26	VSS_227	VSS_327
D29	VSS_228	VSS_328
D32	VSS_229	VSS_329
D37	VSS_230	VSS_330
D39	VSS_231	VSS_331
D4	VSS_232	VSS_332
D9	VSS_233	VSS_333
D9	VSS_234	VSS_334
E11	VSS_235	VSS_335
E12	VSS_236	VSS_336
E17	VSS_237	VSS_337
E12	VSS_238	VSS_338
E20	VSS_239	VSS_339
E23	VSS_240	VSS_340
E26	VSS_241	VSS_341
E29	VSS_242	VSS_342
E32	VSS_243	VSS_343
E36	VSS_244	VSS_344
E7	VSS_245	VSS_345
E8	VSS_246	VSS_346
F11	VSS_247	VSS_347
F10	VSS_248	VSS_348
F13	VSS_249	VSS_349
F14	VSS_250	VSS_350
F17	VSS_251	VSS_351
F2	VSS_252	VSS_352
F20	VSS_253	VSS_353
F23	VSS_254	VSS_354
F26	VSS_255	VSS_355
F29	VSS_256	VSS_356
F35	VSS_257	VSS_357
F37	VSS_258	VSS_358
F39	VSS_259	VSS_359
F5	VSS_260	VSS_360
F6	VSS_261	VSS_361
F9	VSS_262	VSS_362
G11	VSS_263	VSS_363
G12	VSS_264	VSS_364
G20	VSS_265	VSS_365
G23	VSS_266	VSS_366
G26	VSS_267	VSS_367
G29	VSS_268	VSS_368
G34	VSS_269	VSS_369
G7	VSS_270	VSS_370
G8	VSS_271	VSS_371
H1	VSS_272	VSS_372
H17	VSS_273	VSS_373
H2	VSS_274	VSS_374
H20	VSS_275	VSS_375
H23	VSS_276	VSS_376
H26	VSS_277	VSS_377
H29	VSS_278	VSS_378
H33	VSS_279	VSS_379
H35	VSS_280	VSS_380

CPU1K 11 OF 11		
C40	RSVD_001	RSVD_036
D40	RSVD_002	RSVD_037
A86	RSVD_003	RSVD_038
AB7	RSVD_004	RSVD_039
AD37	RSVD_005	RSVD_040
A86	RSVD_006	RSVD_041
AF4	RSVD_007	RSVD_043
AG4	RSVD_008	RSVD_044
AJ11	RSVD_009	RSVD_045
AJ29	RSVD_010	RSVD_046
AJ30	RSVD_011	RSVD_047
AJ31	RSVD_012	RSVD_048
AN20	RSVD_013	RSVD_049
AP20	RSVD_014	RSVD_050
AT11	RSVD_015	RSVD_051
AT14	RSVD_016	RSVD_052
AU10	RSVD_017	RSVD_053
AV1	RSVD_018	RSVD_054
AV34	RSVD_019	RSVD_055
AW2	RSVD_020	RSVD_056
AW34	RSVD_021	RSVD_057
AY3	RSVD_022	RSVD_058
B39	RSVD_023	RSVD_059
C38	RSVD_024	RSVD_060
C39	RSVD_025	RSVD_061
D38	RSVD_026	RSVD_062
H7	RSVD_027	RSVD_063
H8	RSVD_028	RSVD_064
J33	RSVD_029	RSVD_065
J34	RSVD_030	RSVD_066
J9	RSVD_031	RSVD_067
K34	RSVD_032	RSVD_068
K9	RSVD_033	RSVD_069
L31	RSVD_034	RSVD_070
	NCTF_01	A38
	NCTF_02	AU40
	NCTF_03	AW36
	NCTF_04	C2
	NCTF_05	D1



DDRIII DIMM_B0

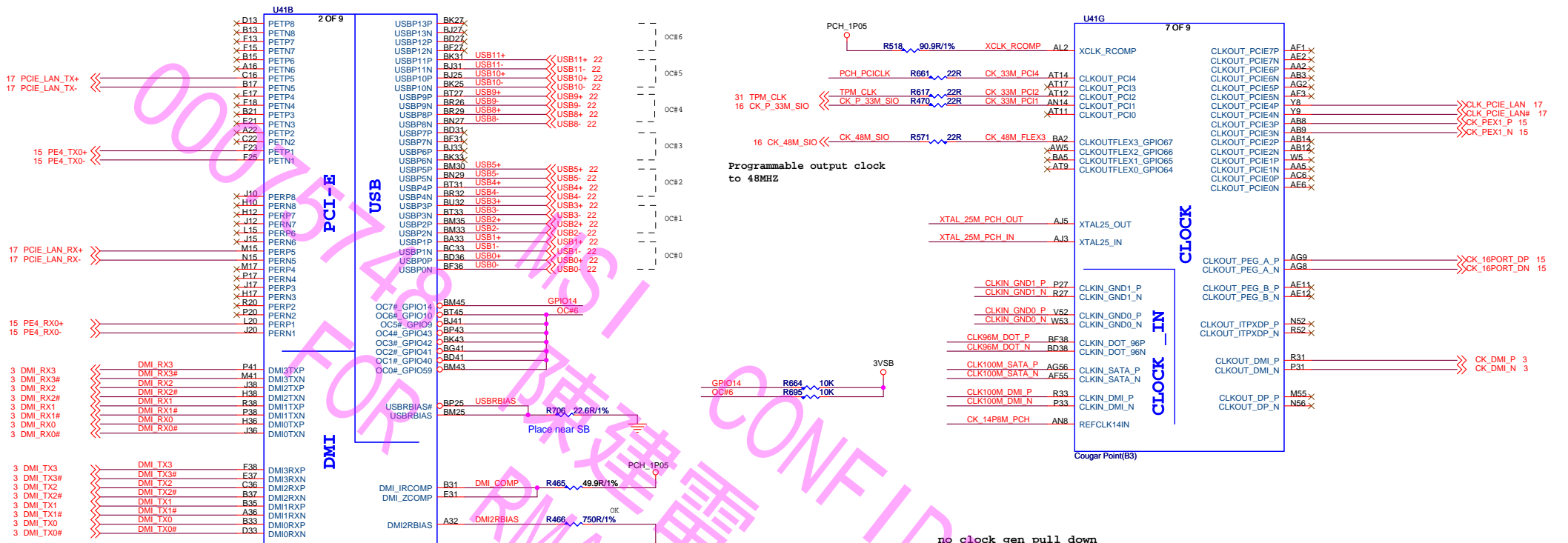


DDR3

DDRIII-240P_BLACK-RH-8
DIMM2 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

— SMBCLK_DDR << SMBCLK_DDR 7
— SMBDATA_DDR << SMBDATA_DDR 7

		MICRO-STAR INT'L CO.,LTD	
		MS-7788	
Size Custom	Document Description DDR III DIMM 2	Rev 10	
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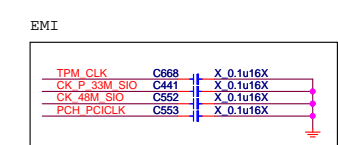
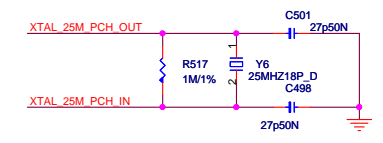
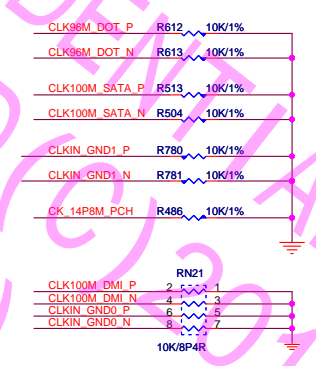
Programmable output clock to 48MHZ

- XTAL 25M PCH OUT AJ5
- XTAL 25M PCH IN AJ3
- CLIN_GND1_P P27
- CLIN_GND1_N R27
- CLIN_GND0_P V52
- CLIN_GND0_N W53
- CLK96M DOT P BF38
- CLK96M DOT N BD38
- CLK100M SATA P AG56
- CLK100M SATA N AE55
- CLK100M DMI P R33
- CLK100M DMI N P33
- CK 14P8M PCH AN8

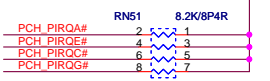
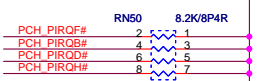
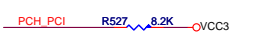
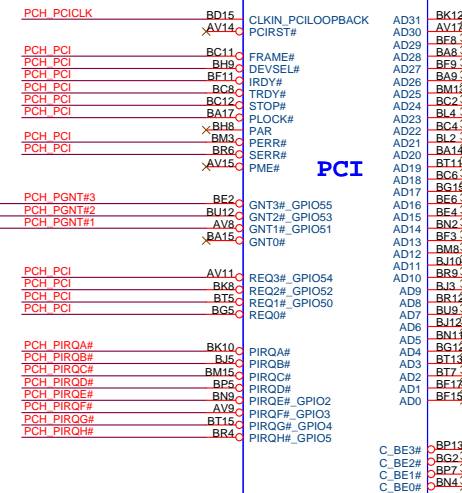
CLOCK _IN

CLOCK

no clock gen pull down



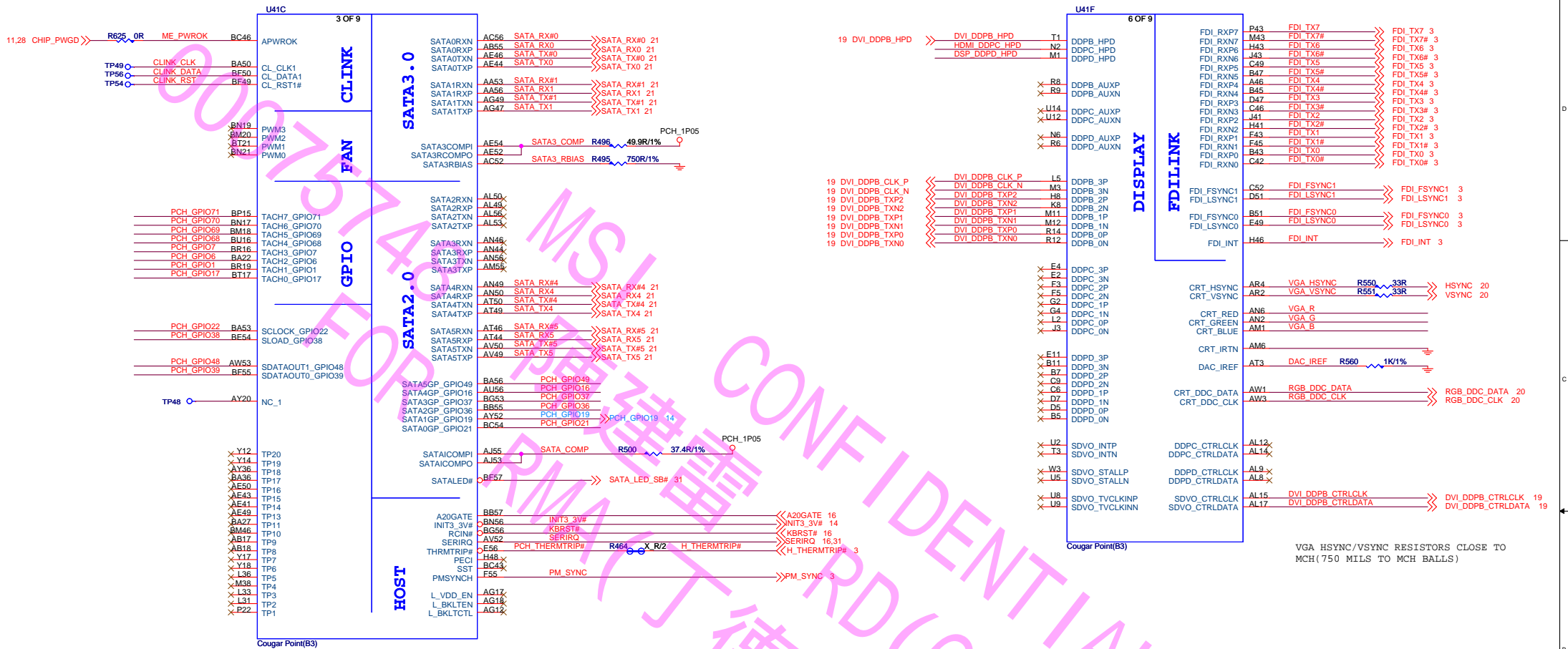
PCICLK LOOPBACK



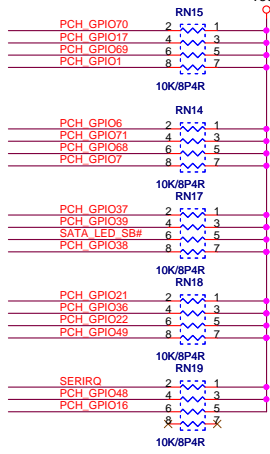
MICRO-STAR INT'L CO.,LTD

MS-7788

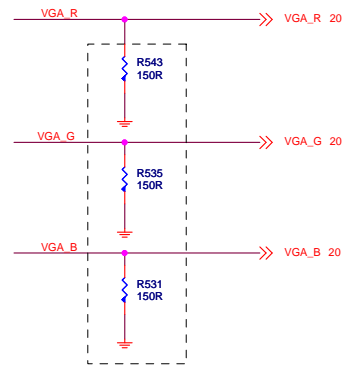
Size Custom	Document Description CP-PCI/E/DMI/USB/CLK	Rev 10
Date: Thursday, November 24, 2011	Sheet 9 of 33	



Pull HIGH for PCH



No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)

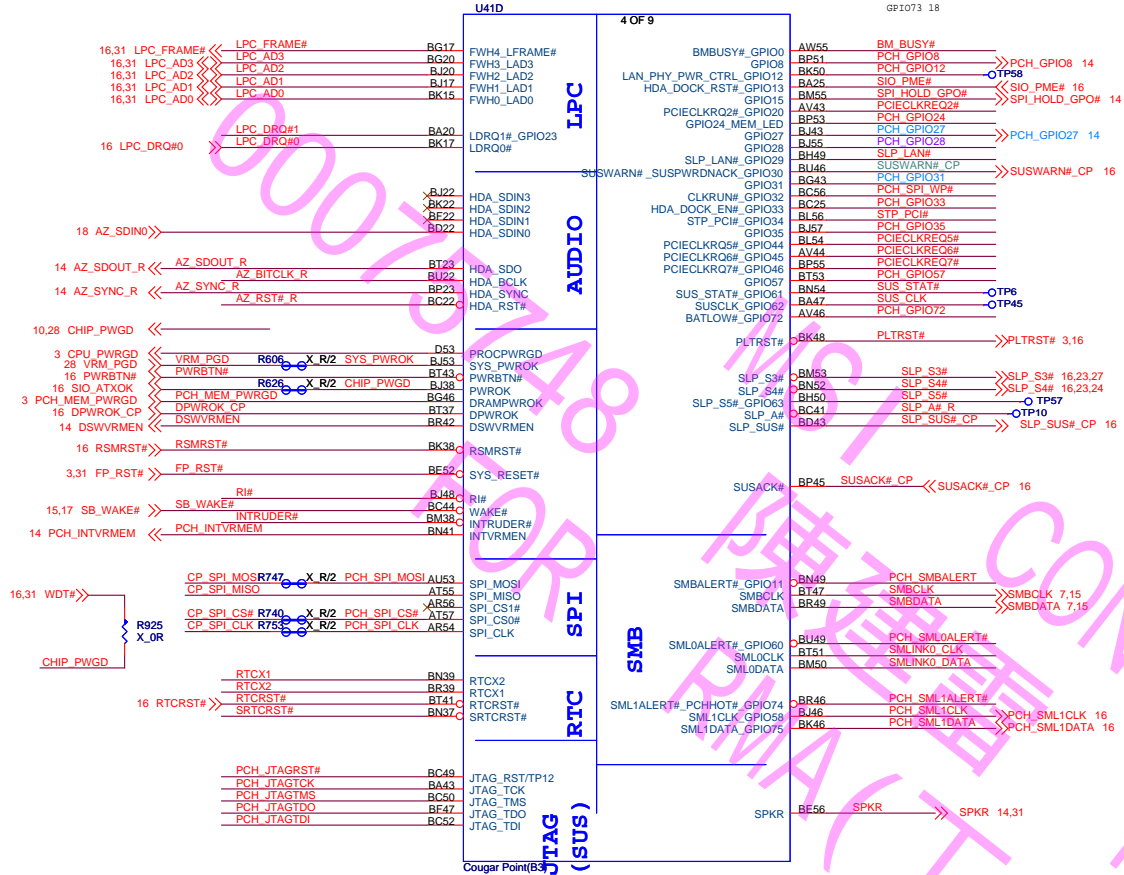


MICRO-STAR INT'L CO.,LTD

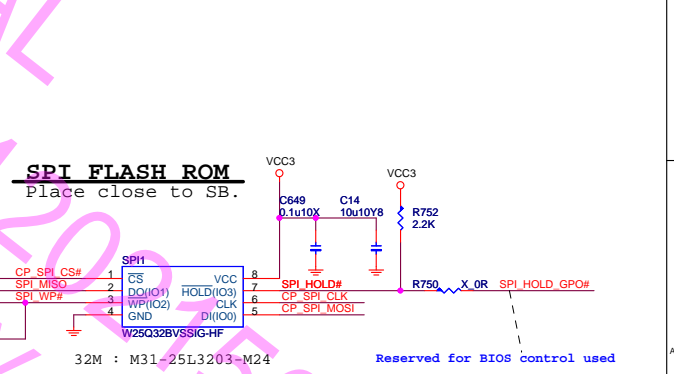
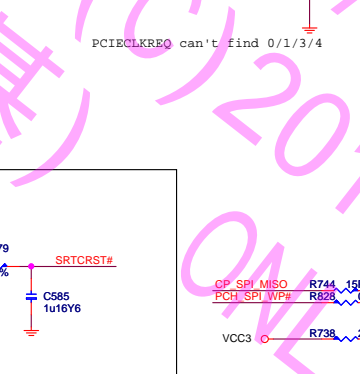
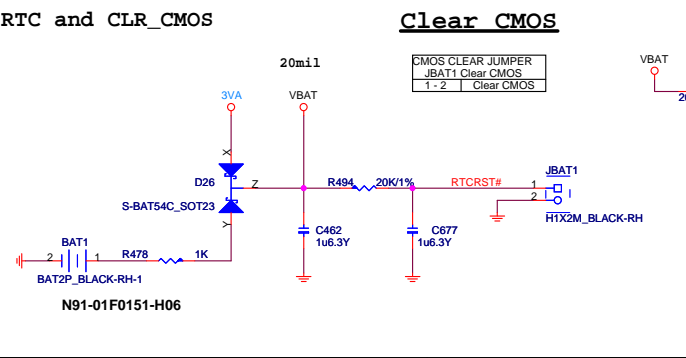
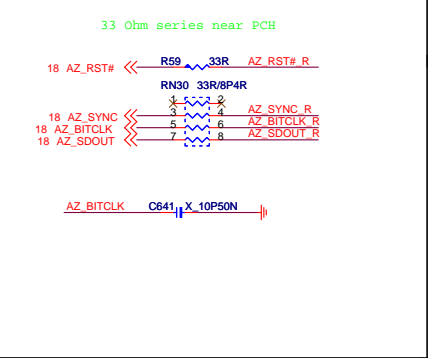
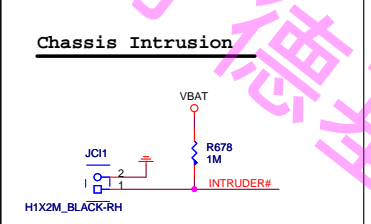
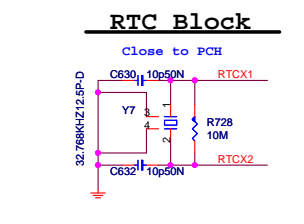
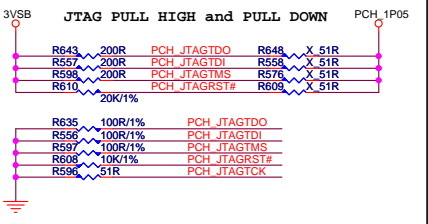
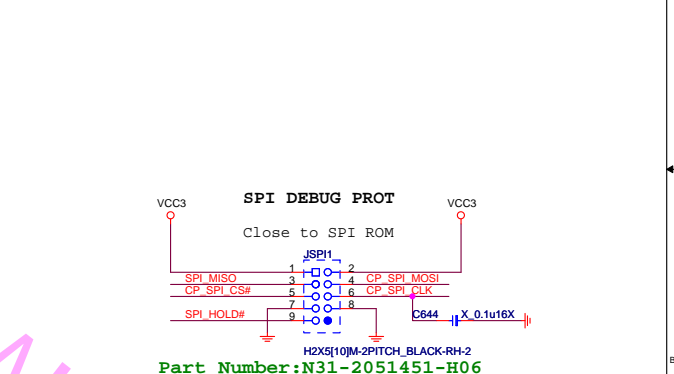
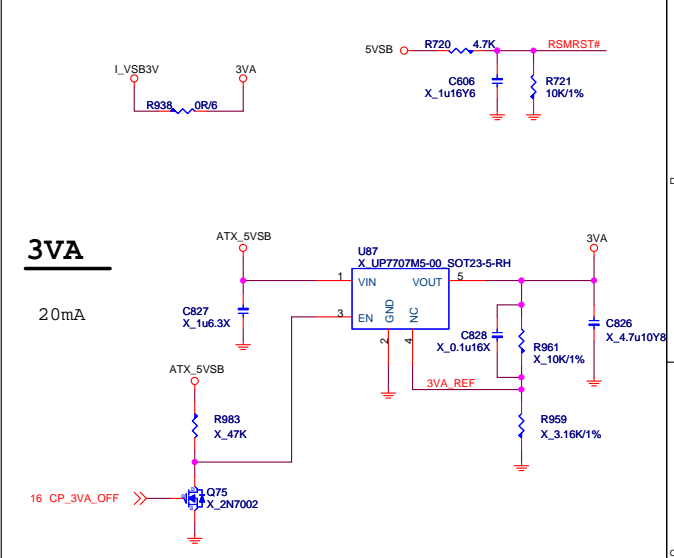
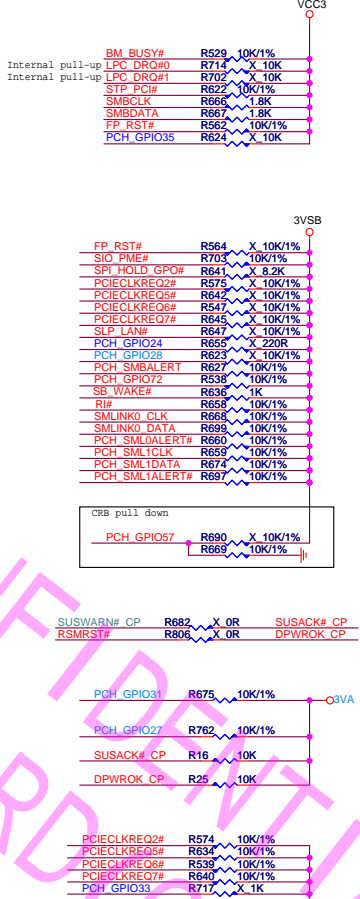
MS-7788

Size: Custom | Document Description: CP-SATA/HOST/FAN/GPIO/VGA | Rev: 10

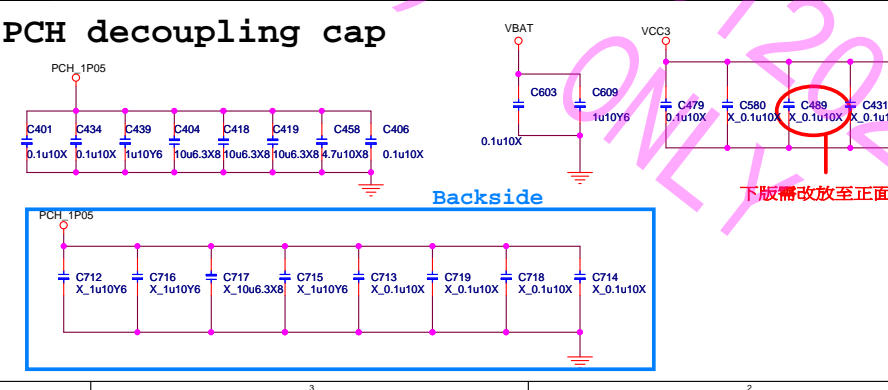
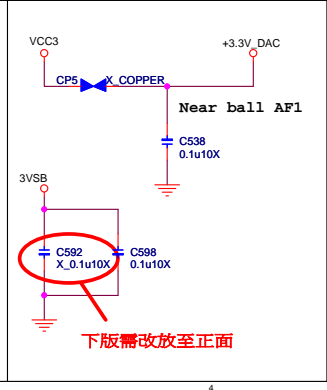
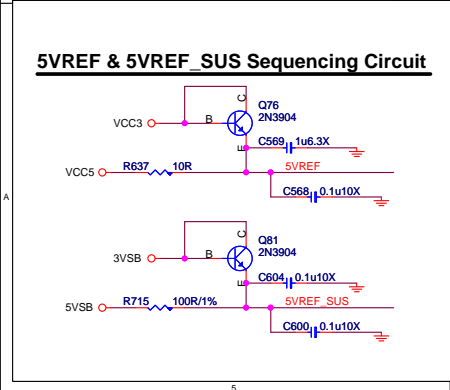
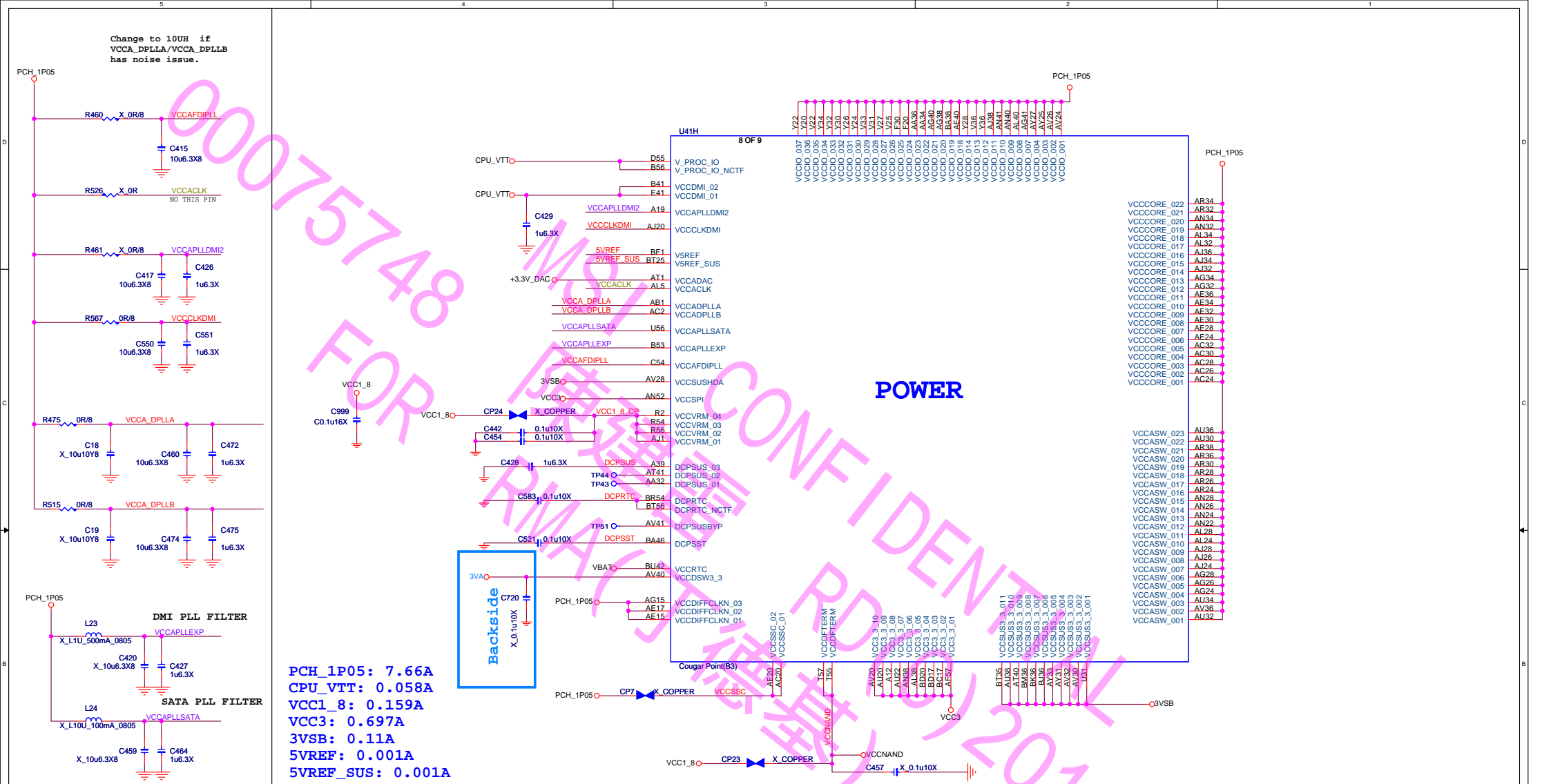
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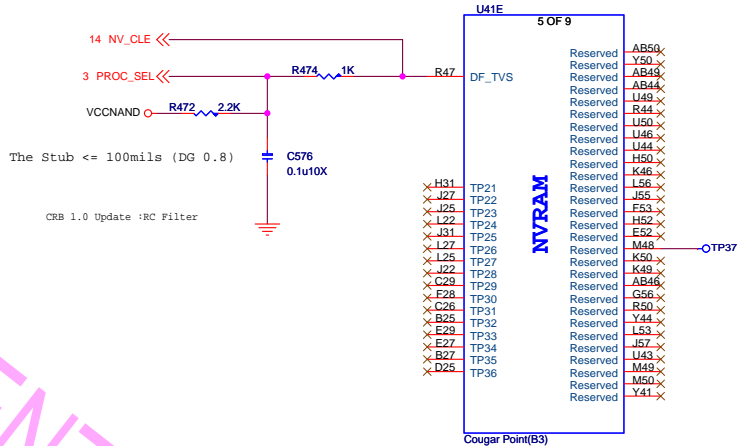
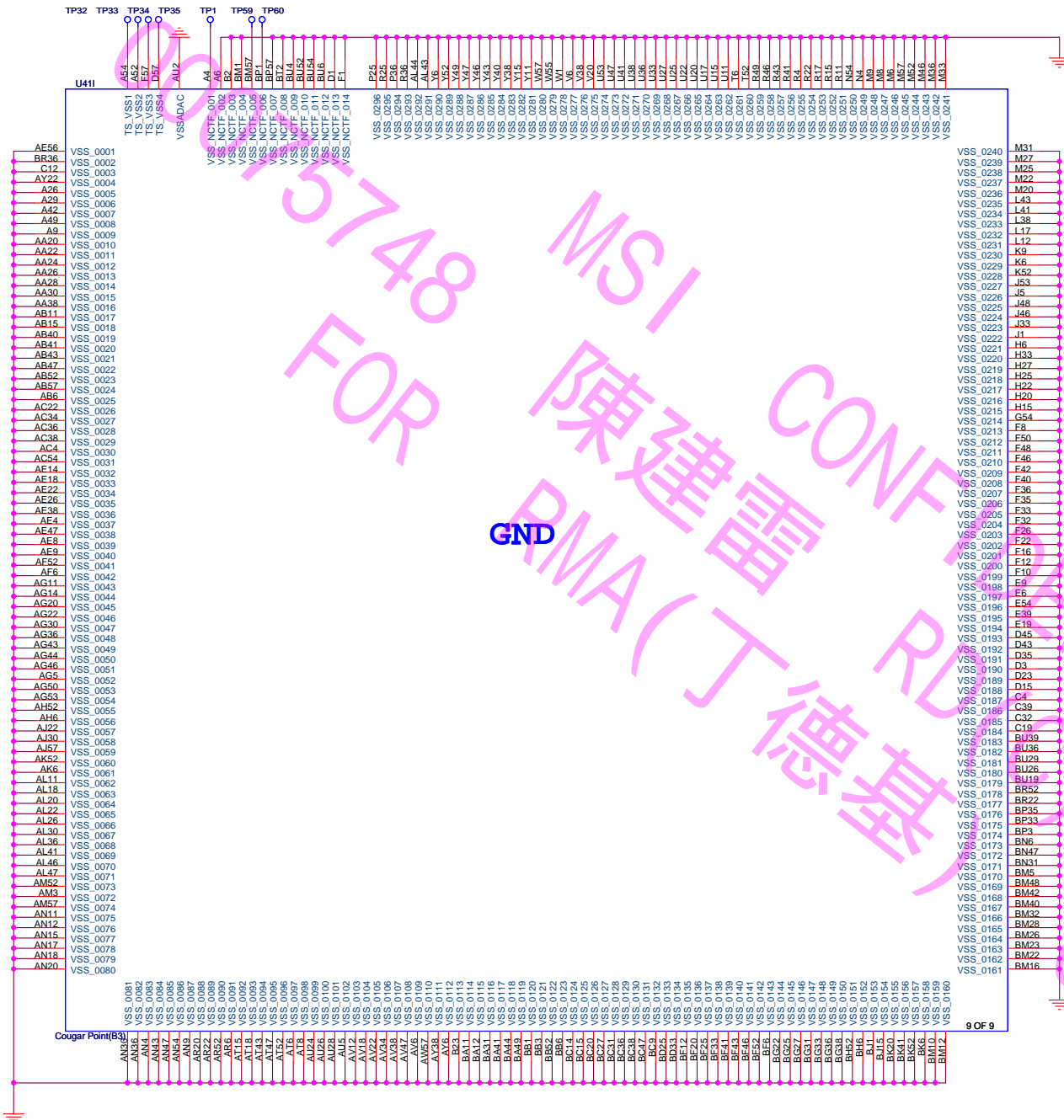
REQUIRED STRAPS



MICRO-STAR INT'L CO.,LTD	
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MSI		
MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description CP-POWER	Rev 10
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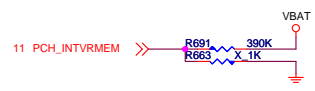
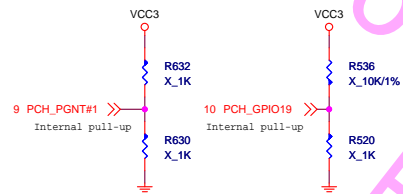


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MICRO-STAR INT'L CO.,LTD		
MS-7788		
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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



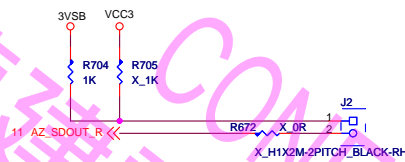
INTVRMEN
 0: DISABLE INTERNAL VRM
 1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



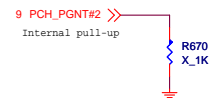
DSWVRMEN
 0 : Disable Internal Deep Sleep 1.05 V regulators.
 1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

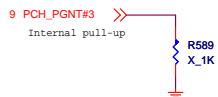


HDA_SDO
 Disable ME in Manufacturing Mode when pull LOW ????

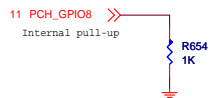
HDA_SDO has internal pull down. Default should be connected to SDIN of codec, no pull up/down. To Disable ME need to have a jumper to pull high



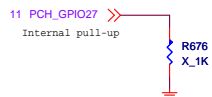
DMI AC/DC MODE
 0 : AC
 1 : DC *



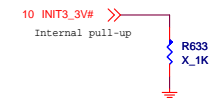
Topblock swap override when pull-low
 Signal has a weak internal pull-up



GPIO8
 0 : Integrated Clocking Enable (FCIM) *
 1 : Buffer Through Mode Enable (BTM)



GPIO28
 0 : OD PLL VR disabled
 1 : OD PLL VR enabled *
 Signal has a weak internal pull-up



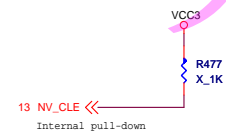
INIT3_3V#
 0 : ??????????????????
 1 : ?????????????????? *



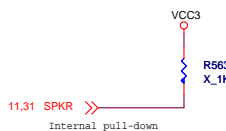
HDA_SYNC
 OD PLL VR SUPPLY SEL
 0: 1.8V SUPPLY *
 1: 1.5V SUPPLY



GPIO15
 0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
 1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
 0 : EN TCO REBOOT *
 1 : DIS TCO REBOOT

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
 0: Can not to reset the processor.

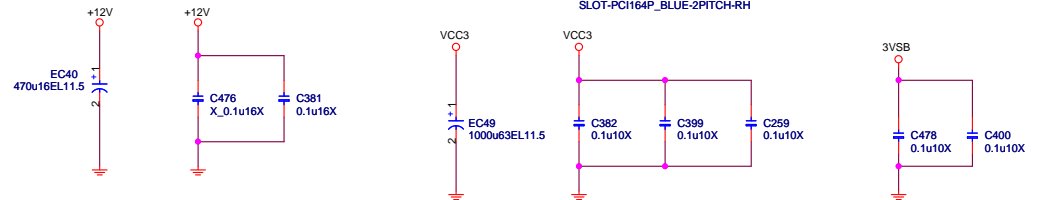
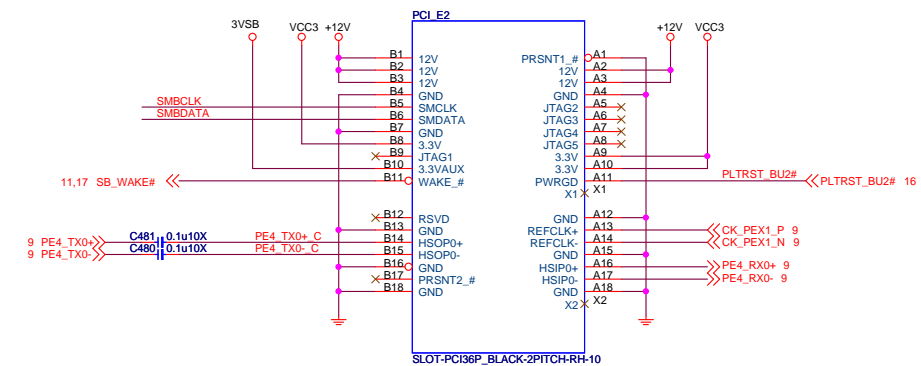
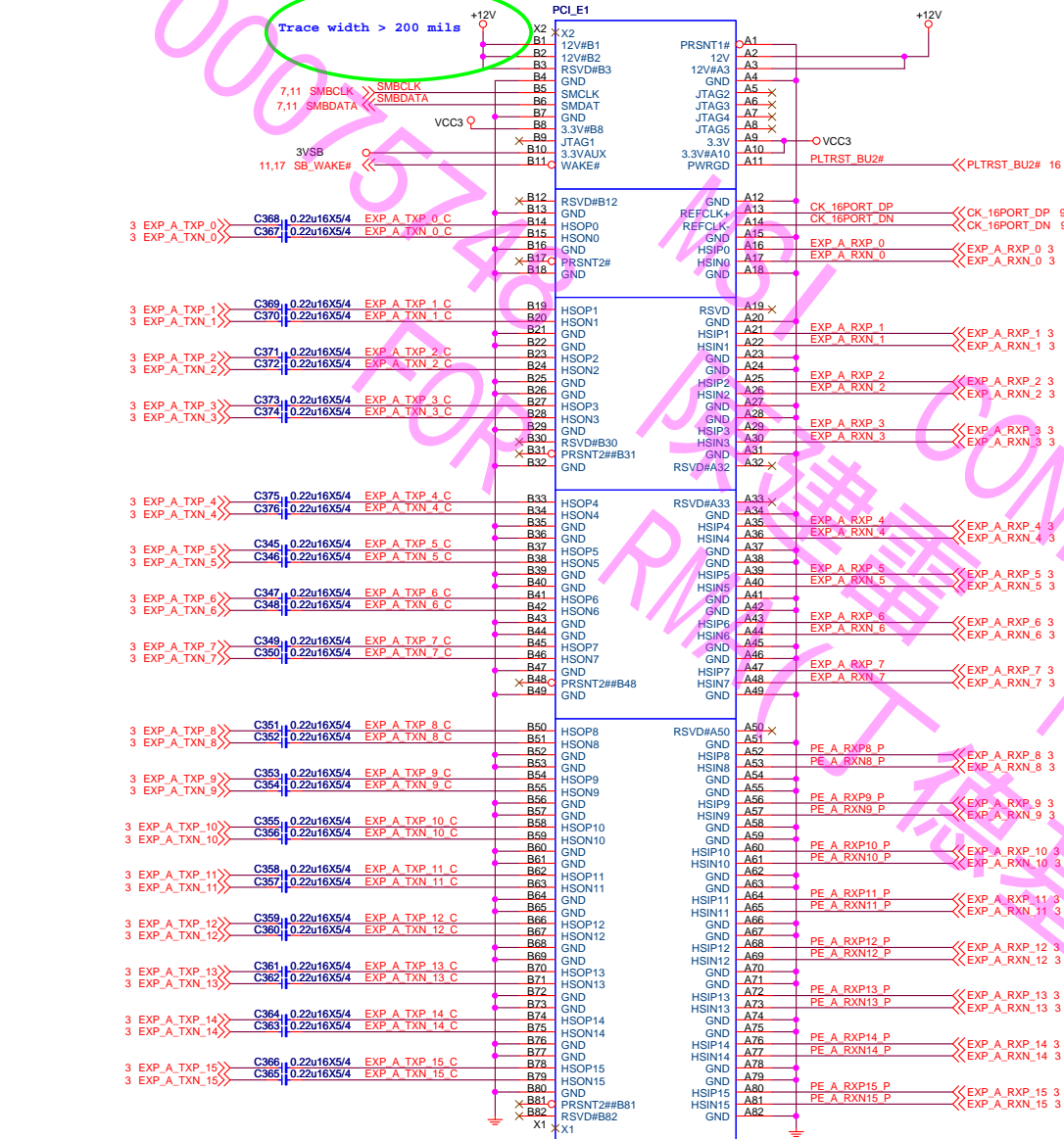
	MICRO-STAR INT'L CO.,LTD	
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PCI_Express X16 slot

N11-1640971-K06

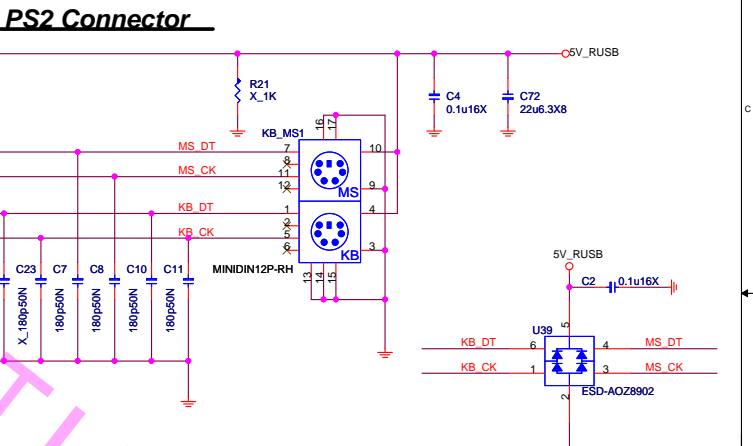
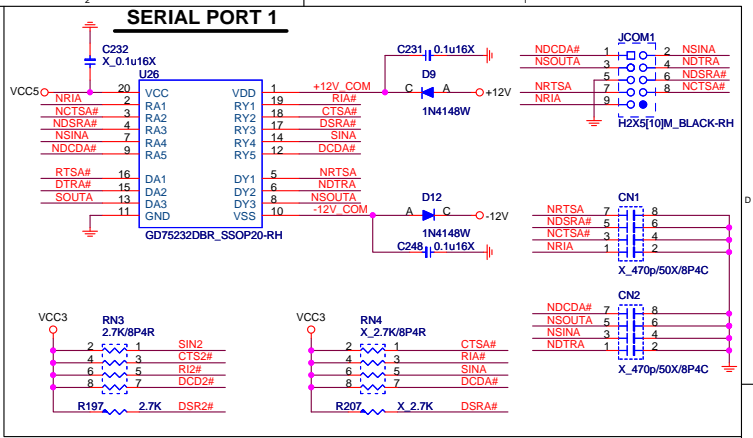
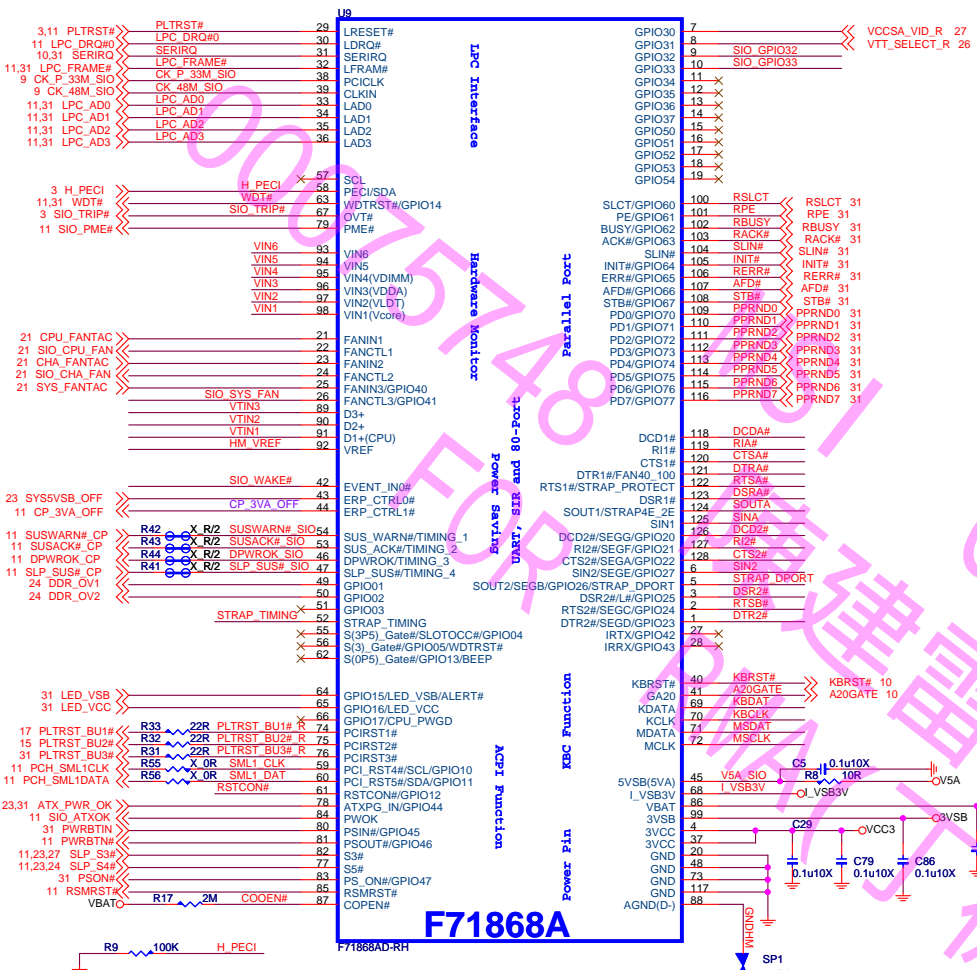
Trace width > 200 mils

PCI EXPRESS x1-PORT



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MICRO-STAR INT'L CO.,LTD		
MS-7788		
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Custom	PCIe x16/x1	10
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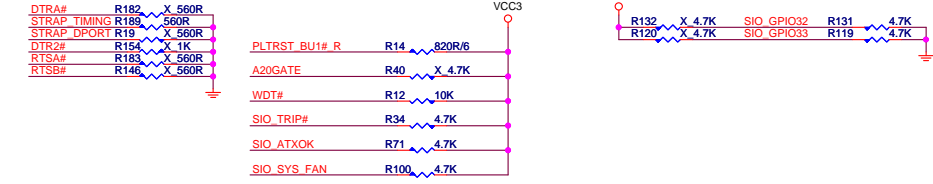


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

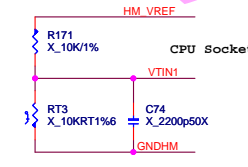
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Couragar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
Strap_Peotect (RTSA#)	Alarm mode	Force mode

MB ID	GPIO 32	33
SKU_A	0	0
	0	1
	1	0
	1	1

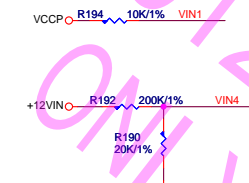
OPT BOM



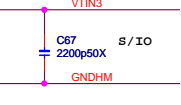
HW Monitor - Thermal



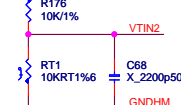
HW Monitor - Voltage



Close to Hot point



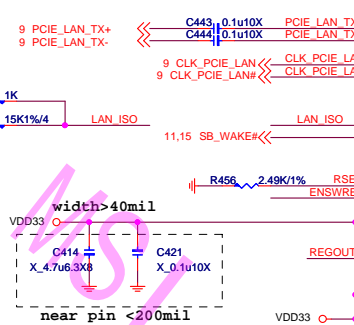
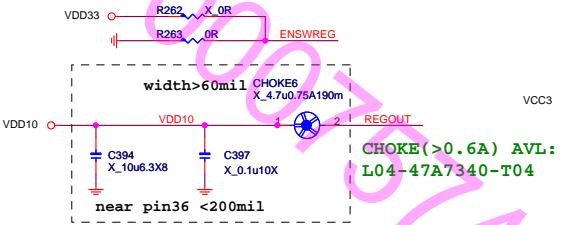
Close to Hot point



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Power Regulator Option

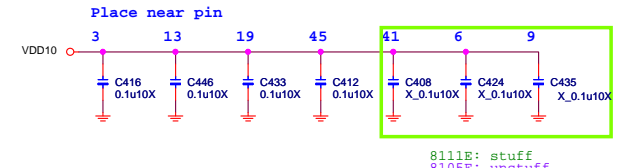
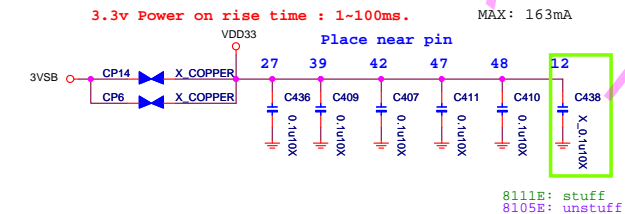
	Mode	Choke6	C394	C397	C414	C421	R262	R263
8111E Series & 8105E Series	SWR mode							
8105E Series	LDO mode							



For RTL8111E Series EEPROM / ASF / Efuse Function

	EEPROM 93C46	EEPROM 93C56/6	EEPROM 603C46	EFuse
SMBCLK	X	X	L	X
SMBDATA	L	H	H	L
GPO	H	H	H	H

Note: For RTL8111E-VL, R17 must be 1K.



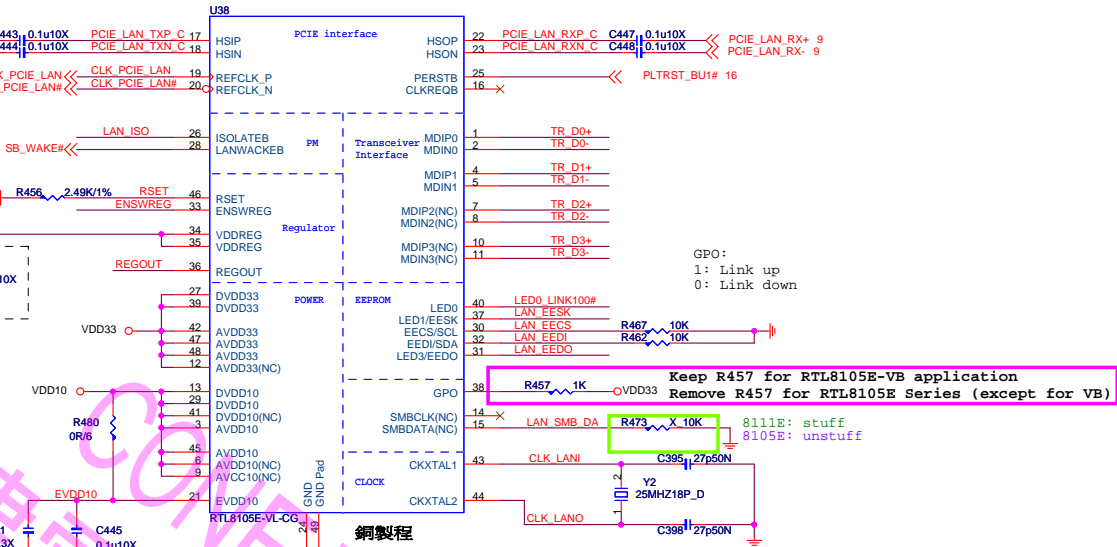
8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

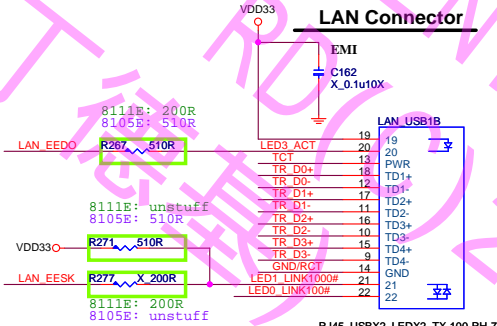
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

RTL8105E 10/100M LAN
co-lay RTL8111E Giga LAN

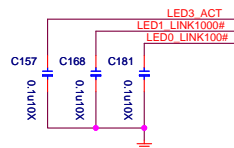


Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

LAN Connector



only support LED0+LED1+LED1+LED3 dual color LED combinations when using EEPROM



Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0771	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20		20	
21		21	
22		22	

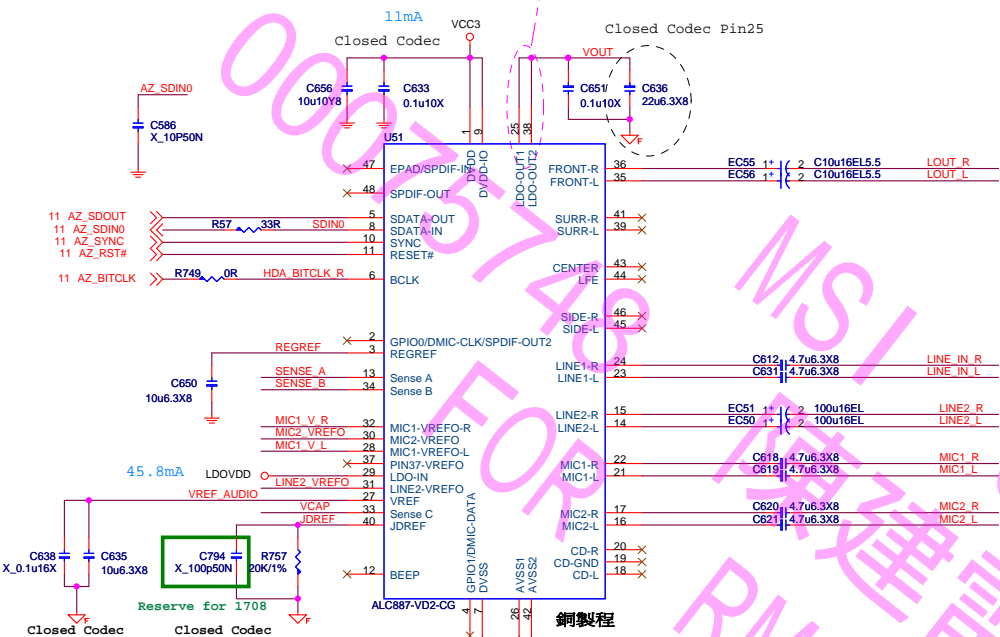


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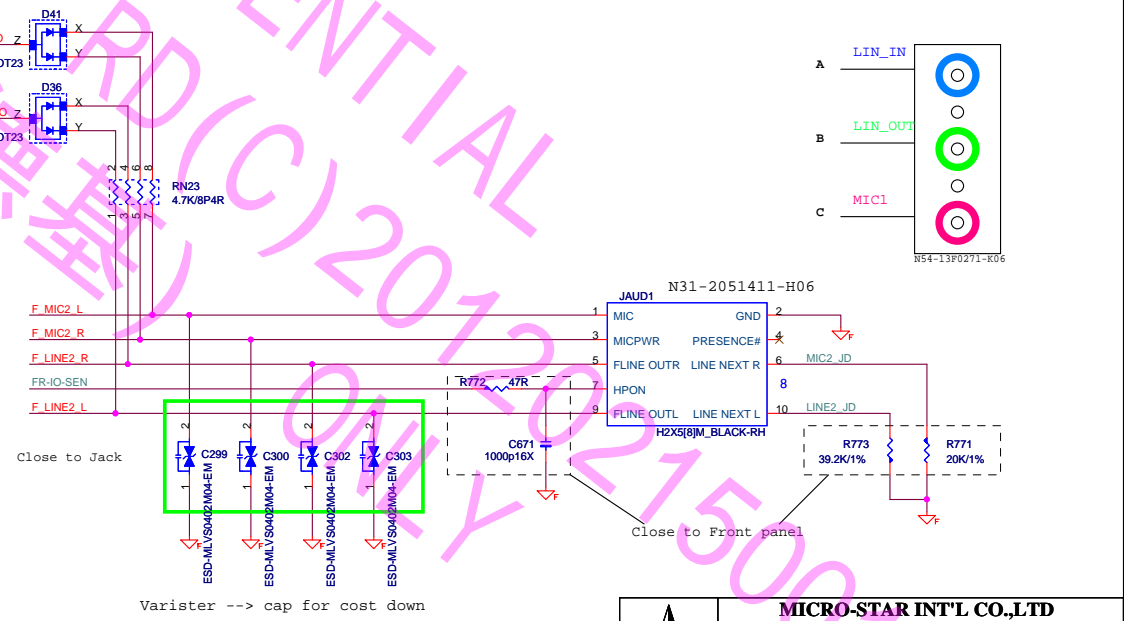
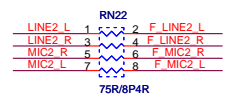
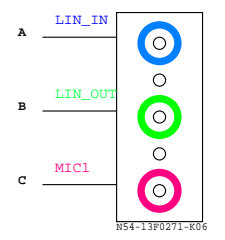
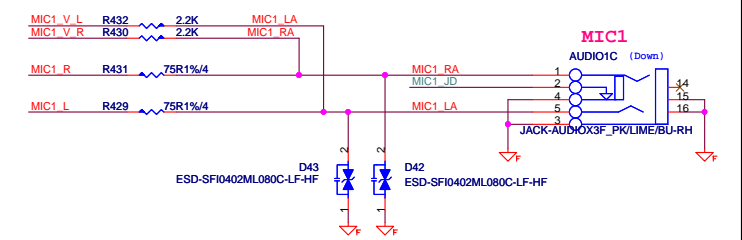
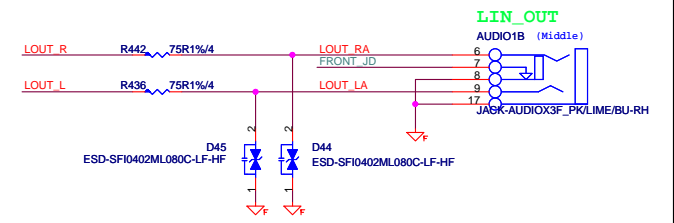
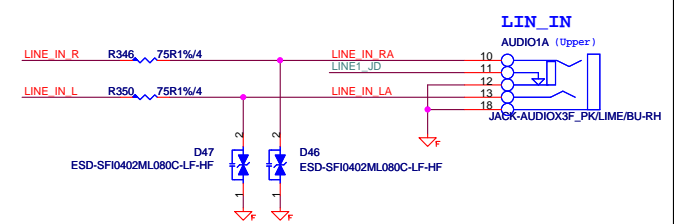
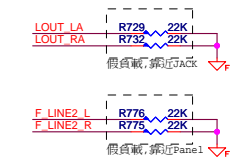
Size	Document Description	Rev
Custom	LAN - RTL8105E / 8111E	10
Date:	Thursday, November 24, 2011	Sheet 17 of 33

Codec Pin25 & 38連接的Layout，以最短路徑，至少40mils線寬連接。

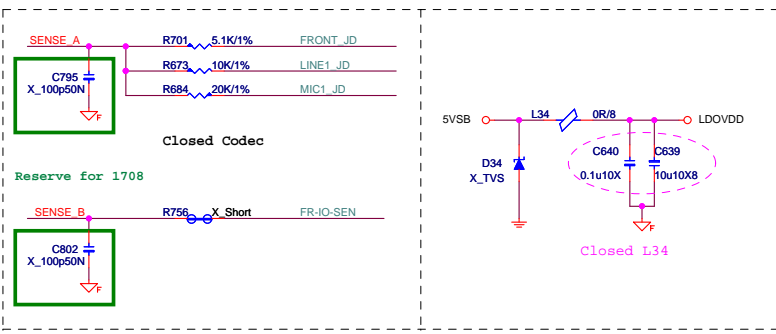
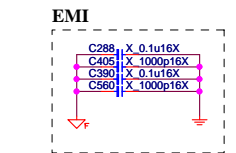


銅製程

當串接電容有極性時，需上對地電阻

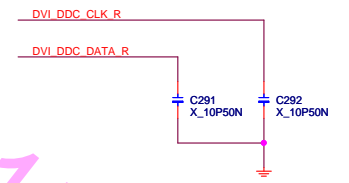
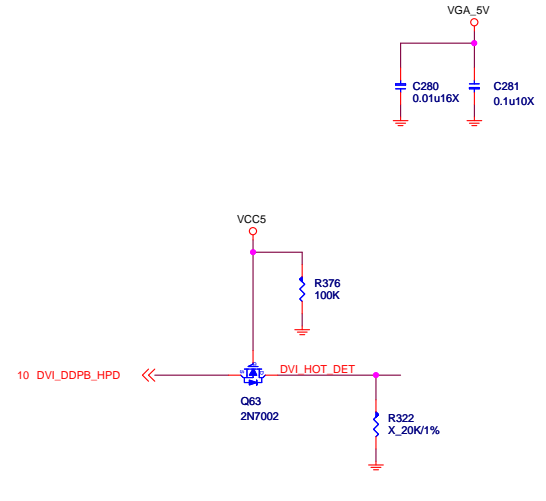
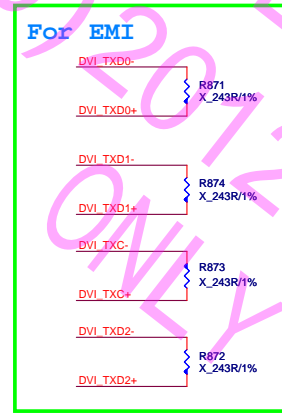
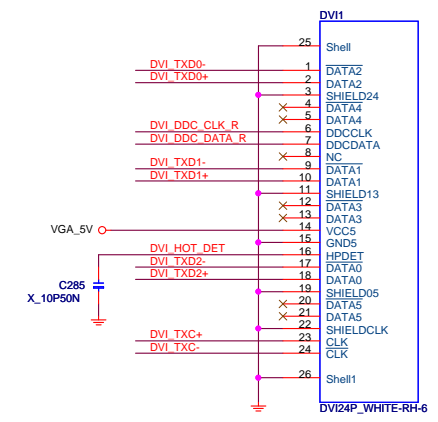
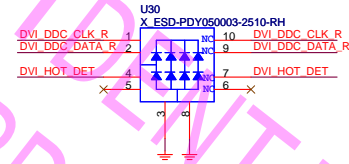
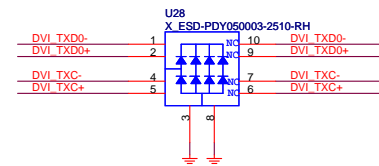
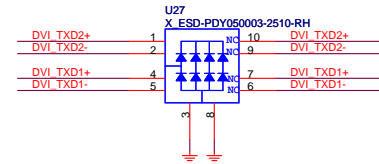
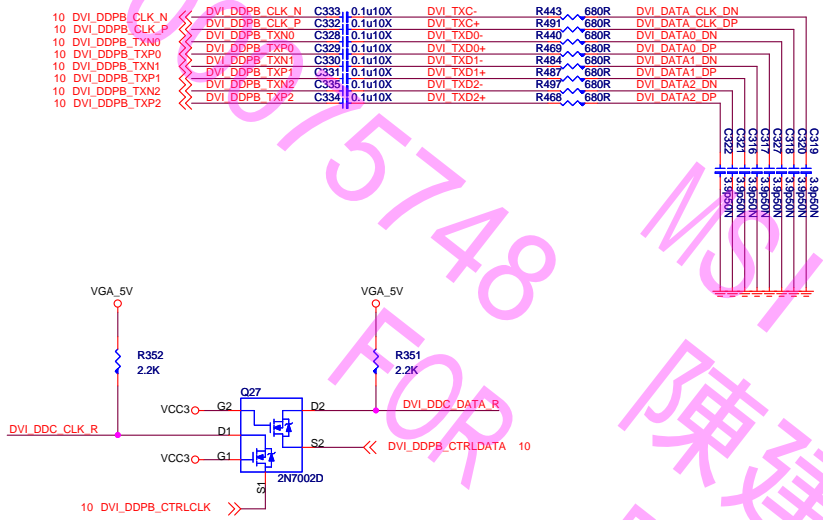


Varister --> cap for cost down



DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

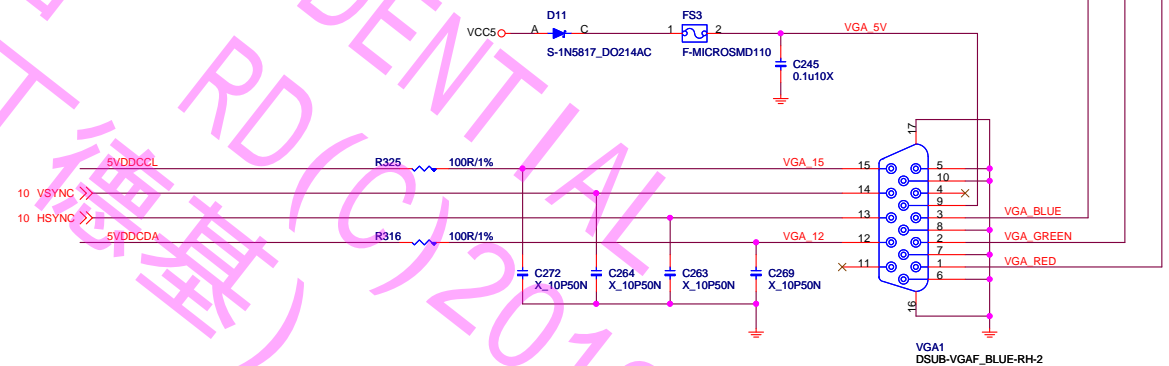
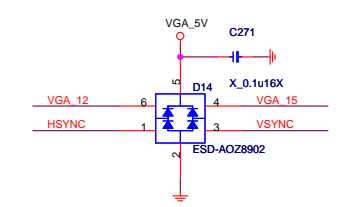
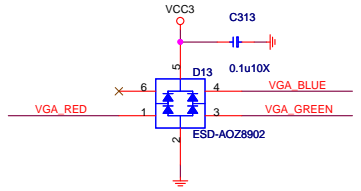
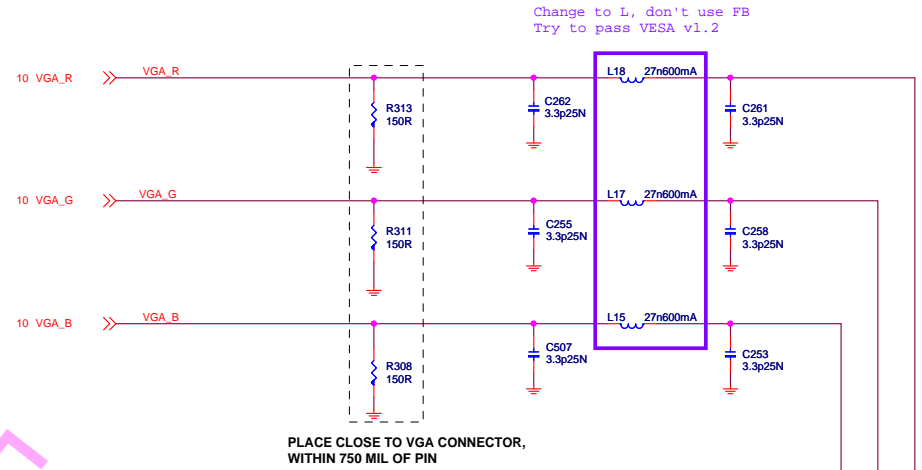
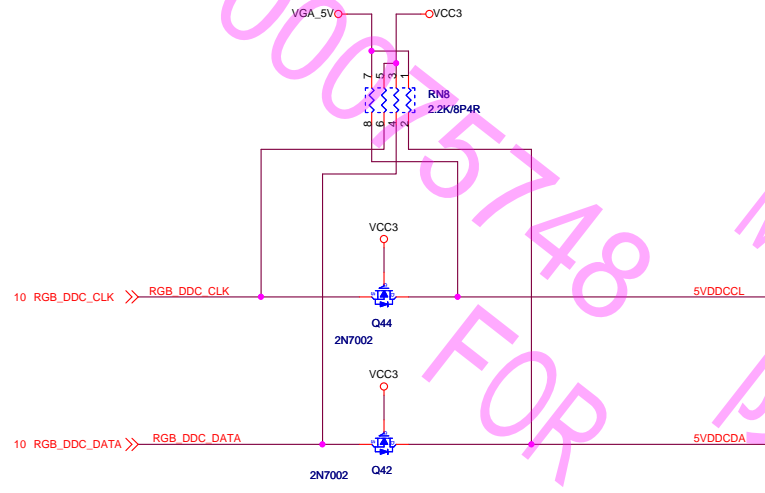


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D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



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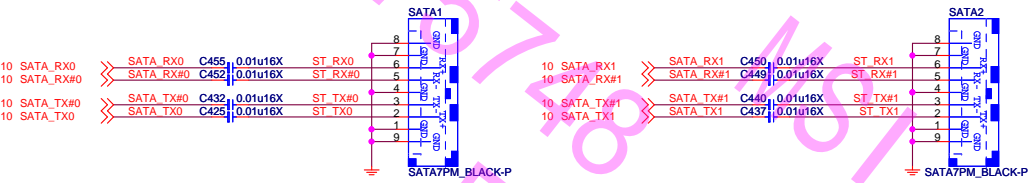
MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description VGA	Rev 10
Date: Thursday, November 24, 2011		Sheet 20 of 33

Table 1-3. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)					
	Q67	Q65	B65	H67	P67	H61
Total number of SATA ports	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 ⁴	1 ⁵	1 ⁵	2 ⁴	2 ⁴	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4 ⁸

NOTES:
8. SATA ports 2 and 3 are disabled.

SATA 3G PORT 0,1

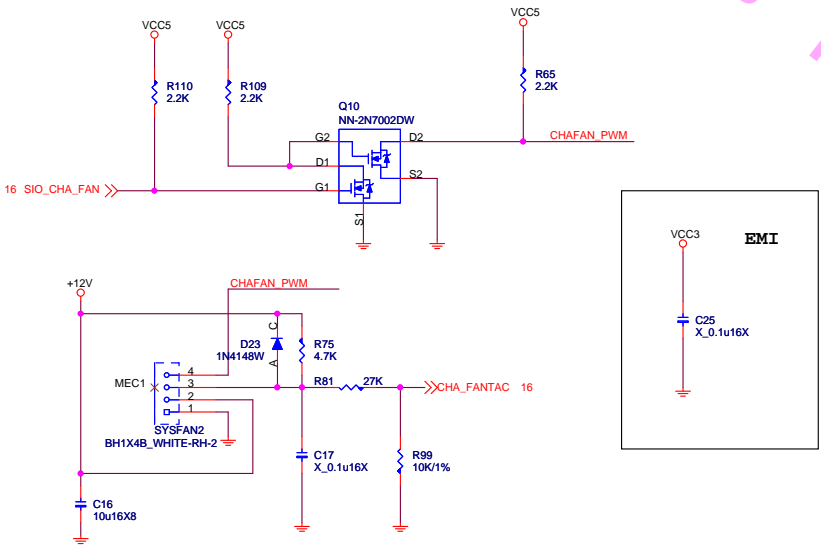


SATA 3G PORT 4,5



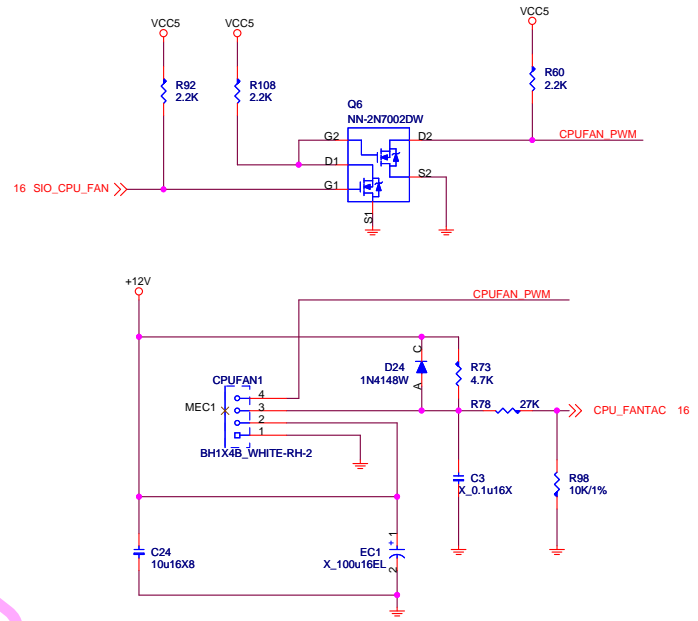
CHASSIS FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN2



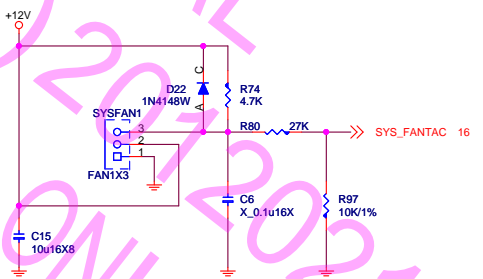
CPU FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN1



SYSTEM FAN3-COUNTROL CIRCUIT

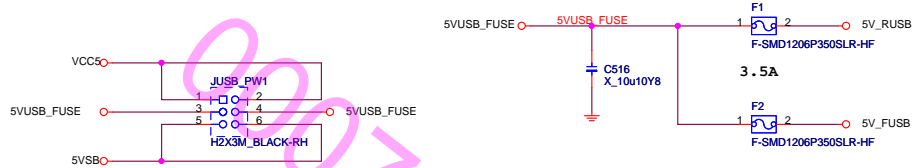
From SIO SYSTEM FAN3



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5V_USB Switch

5V_USB must 120mm

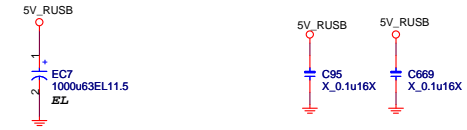


Default VCC5 (PIN1-3,2-4)

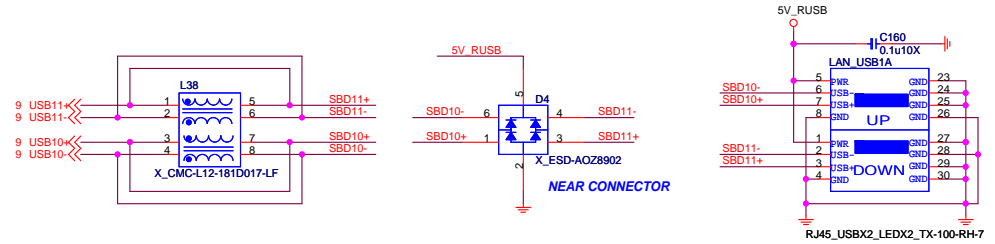
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	Not support
3-5,4-6	EUP Enable	Not support
	EUP Disable	support

Rear USB Connector

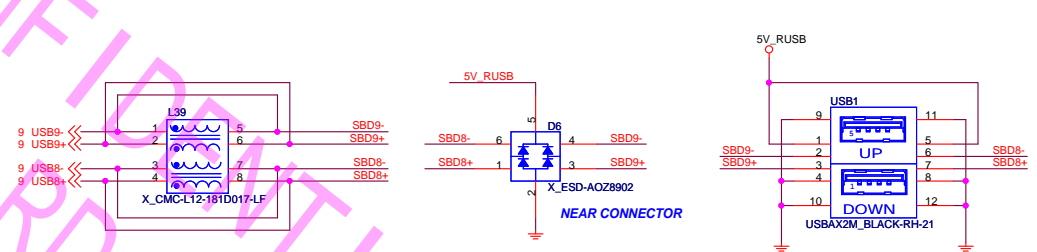
NEAR USB REAR CONNECTOR



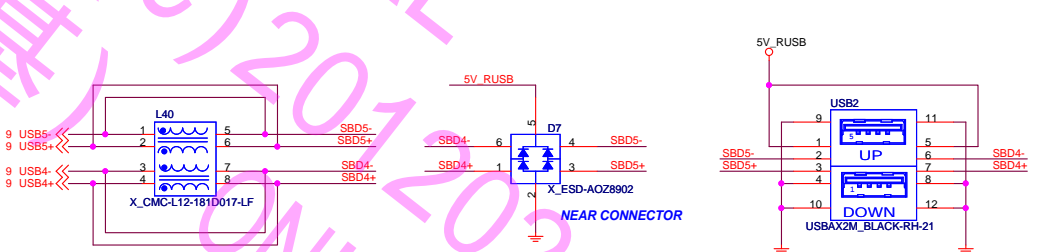
REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9



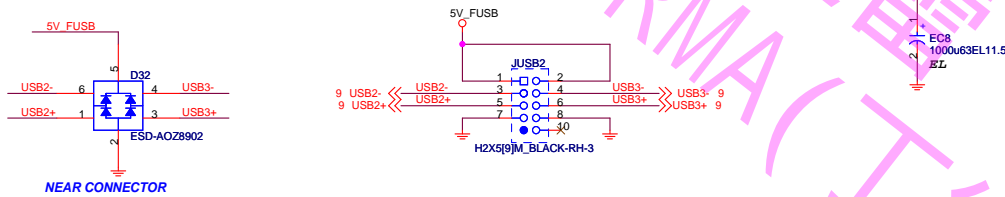
REAL USB PORT 4,5



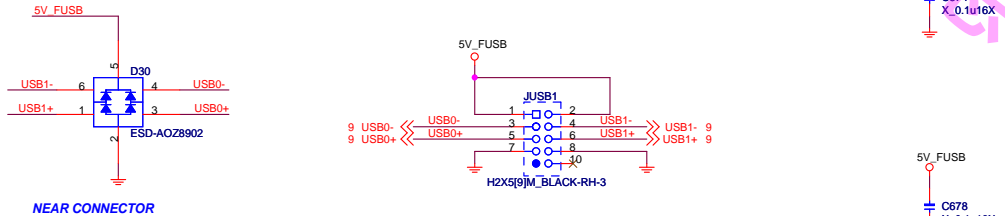
Front USB Connector


For H61 6,7,12,13 Port should be remove

FRONT USB PORT 2,3



FRONT USB PORT 0,1



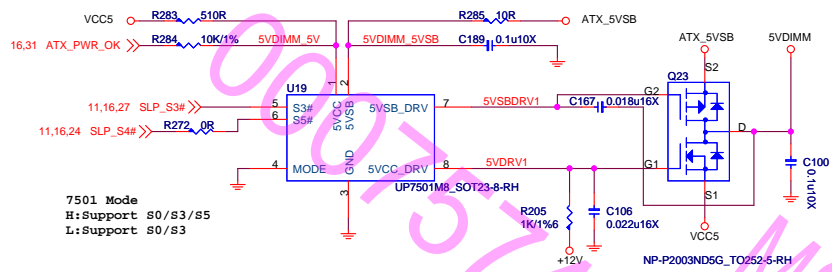


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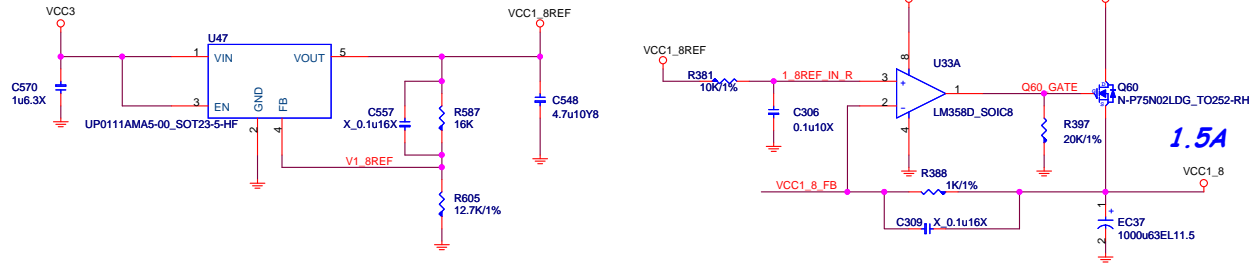
MS-7788

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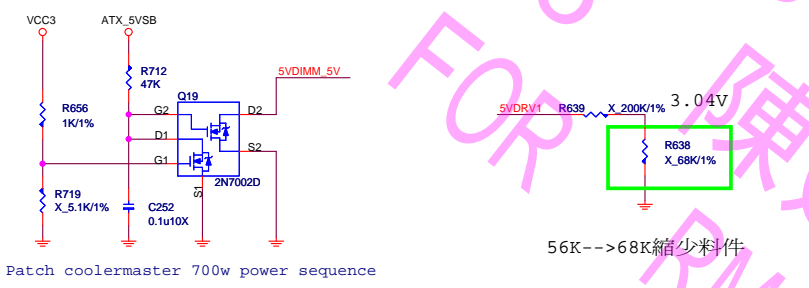
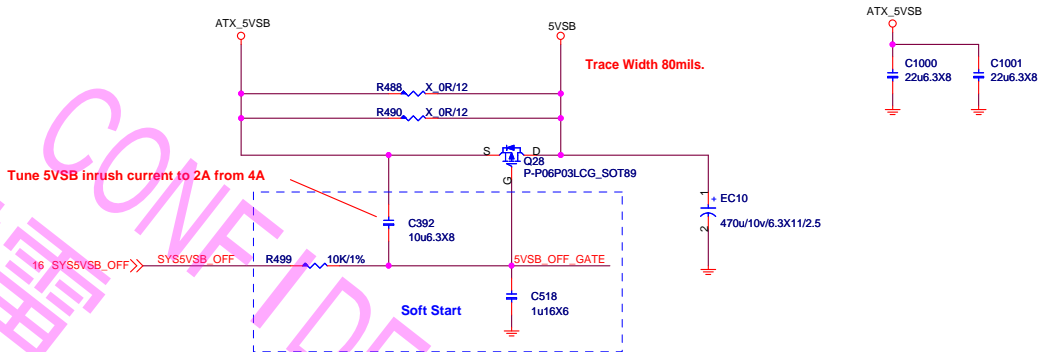
5VDIMM FOR DDR



VCC1_8REF

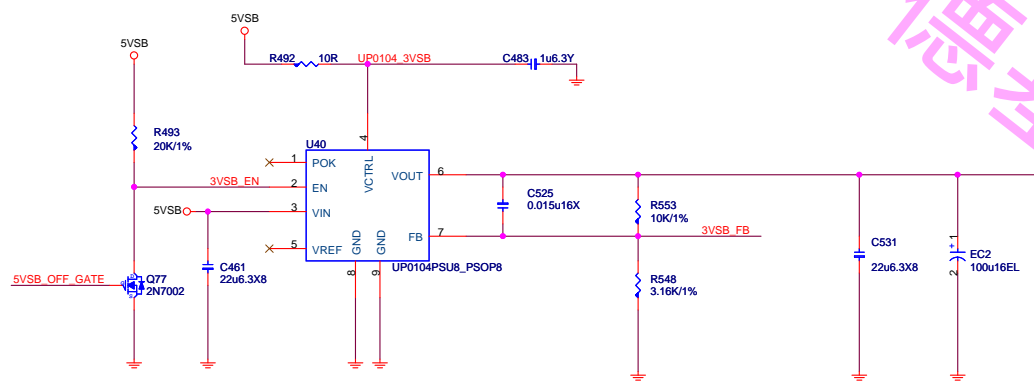


5VSB Power Switch



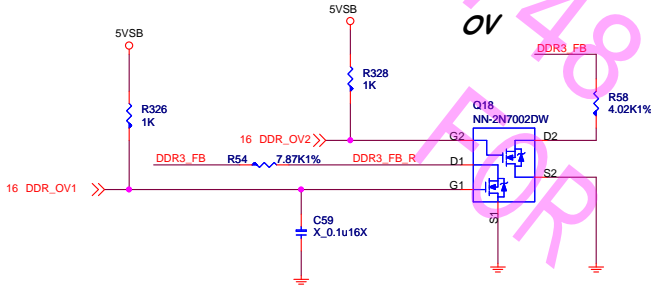
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



DDR3_1.5V 4.5A+6A+1A+8A=19.5A

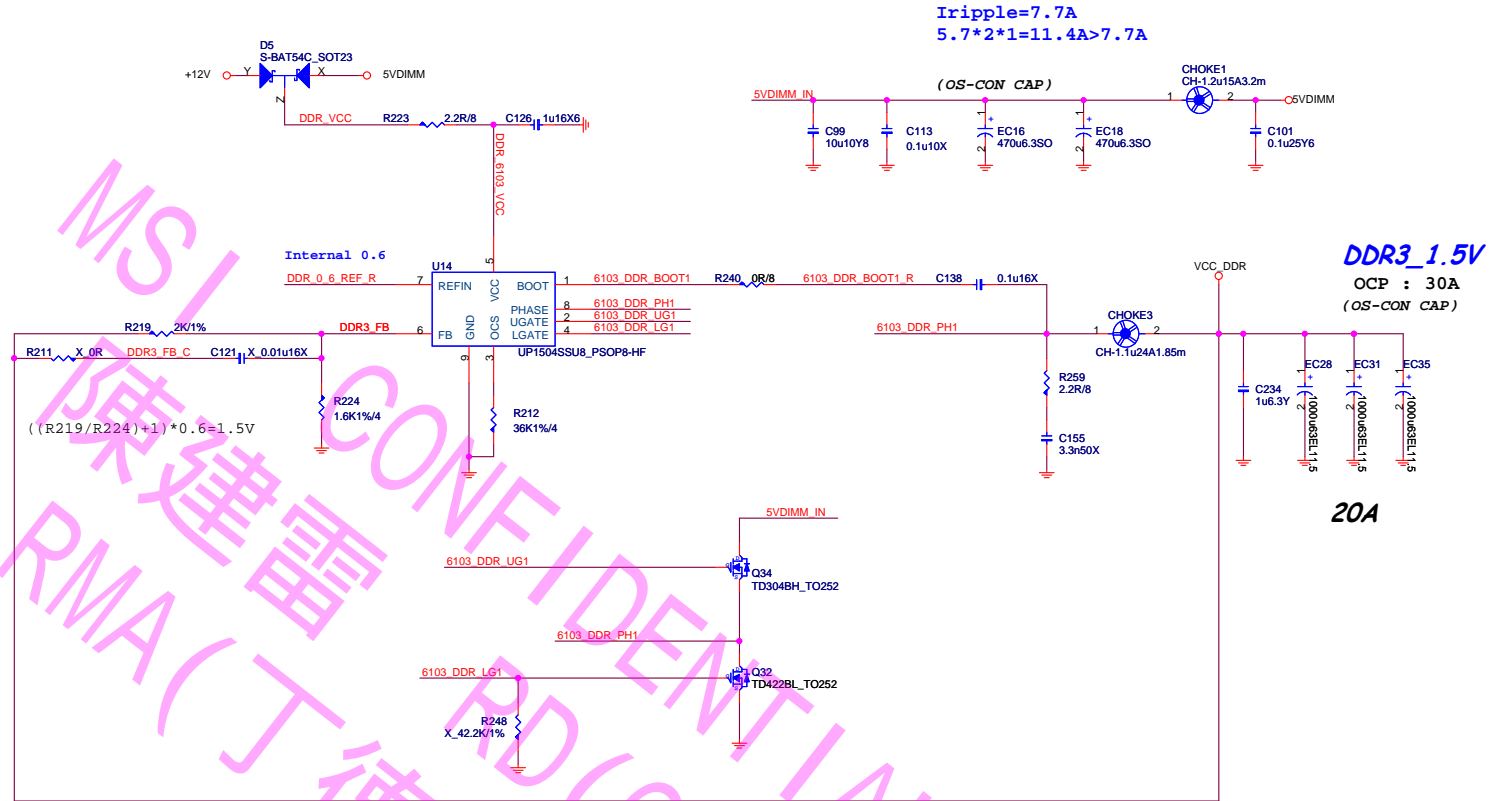
4.5A FOR CPU
6A FOR 2DIMM
1A FOR DDR VTT
8A FOR PCH



*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

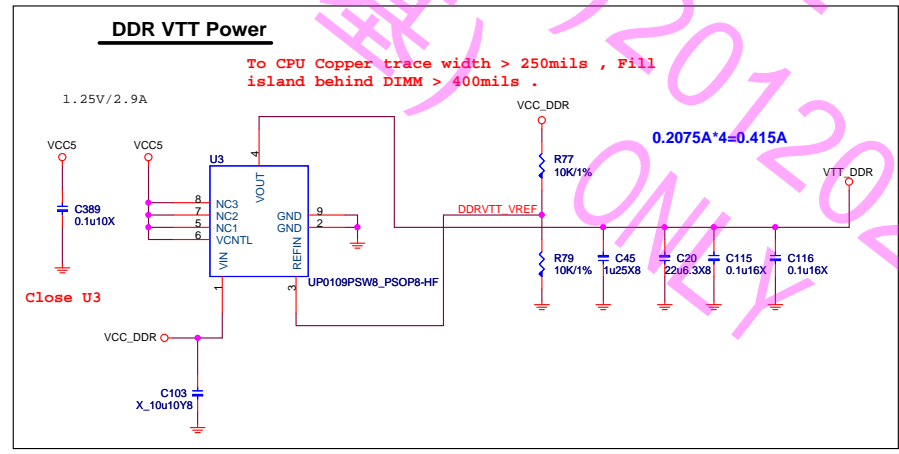
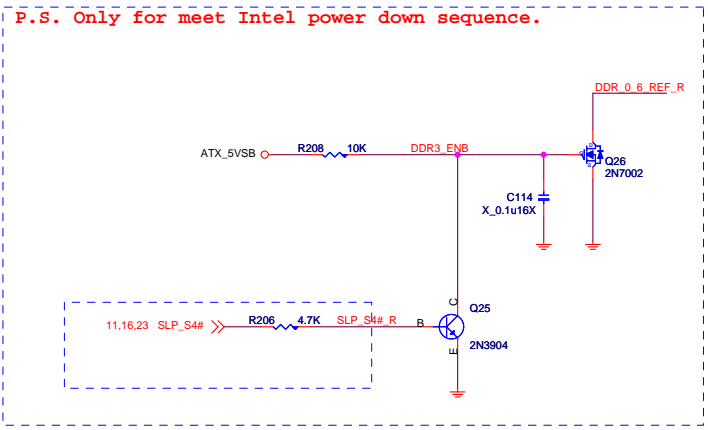
DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)



Ripple=7.7A
5.7*2*1=11.4A>7.7A

DDR3_1.5V
OCP : 30A
(OS-CON CAP)

20A



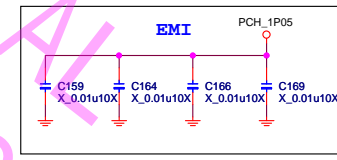
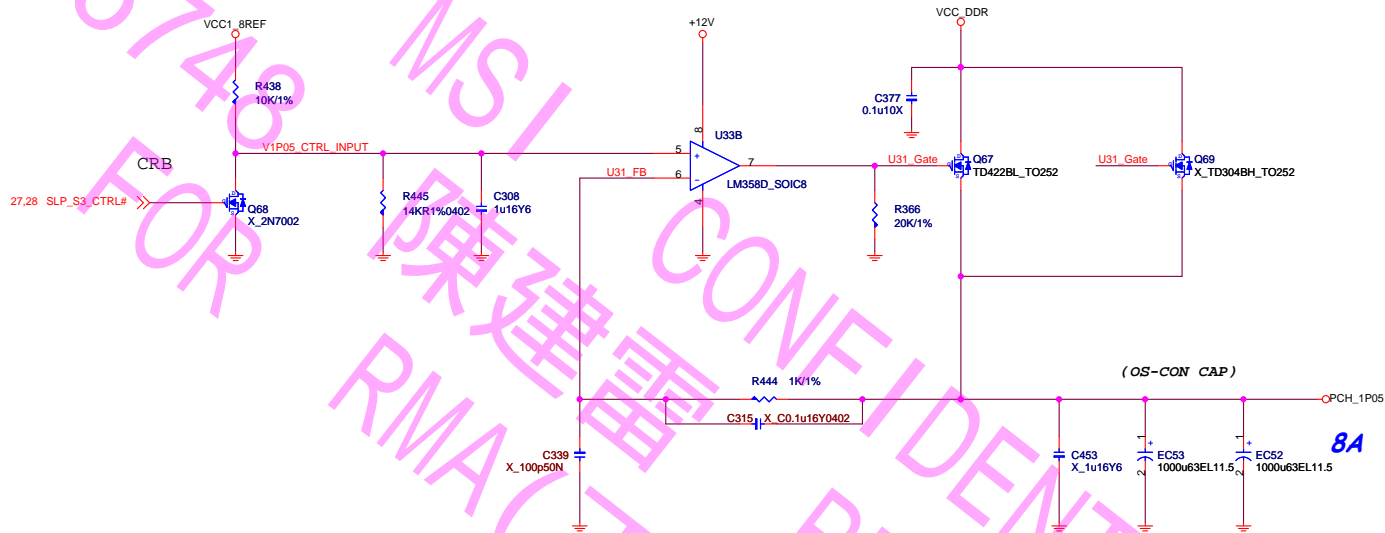
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Size: Custom | Document Description: DDR Power - UPI504-1-Phase | Rev: 10

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PCH Power:1.05V

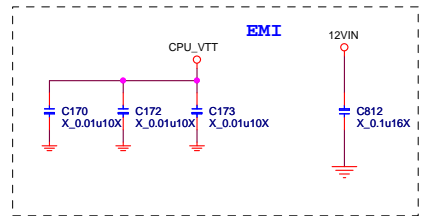
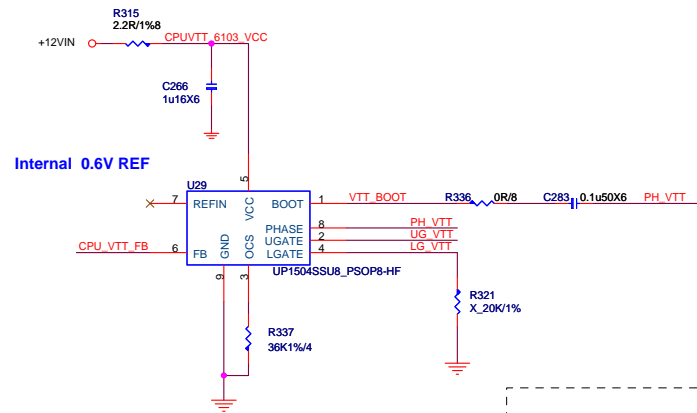


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CPU_VTT:1.05/1.00

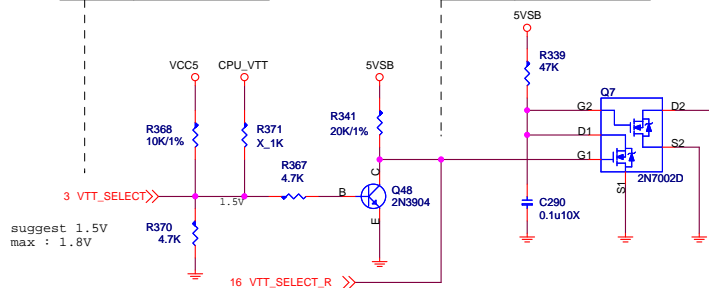
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$

$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5 * 1 = 5A > 3.8A$

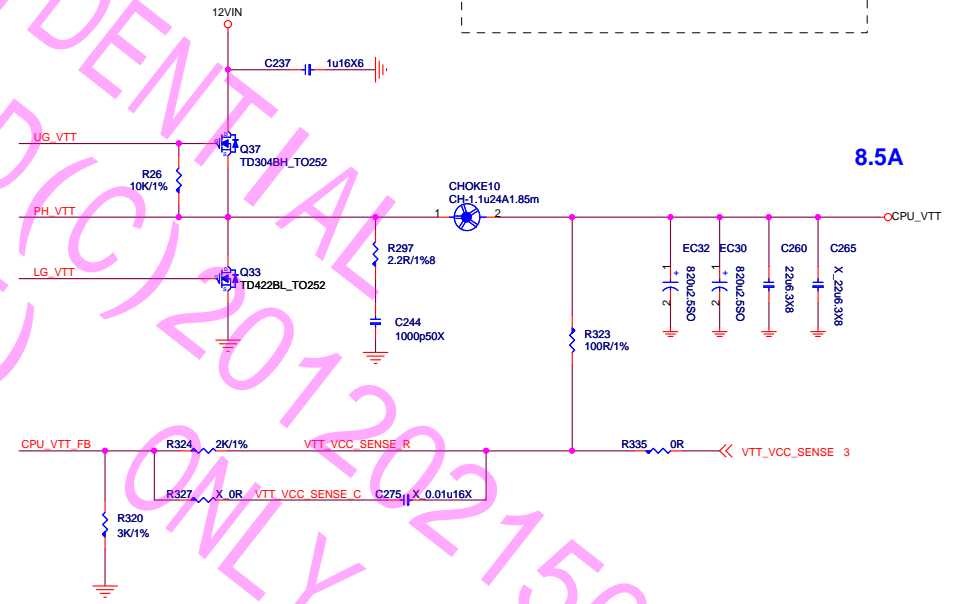


VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



suggest 1.5V
max : 1.8V

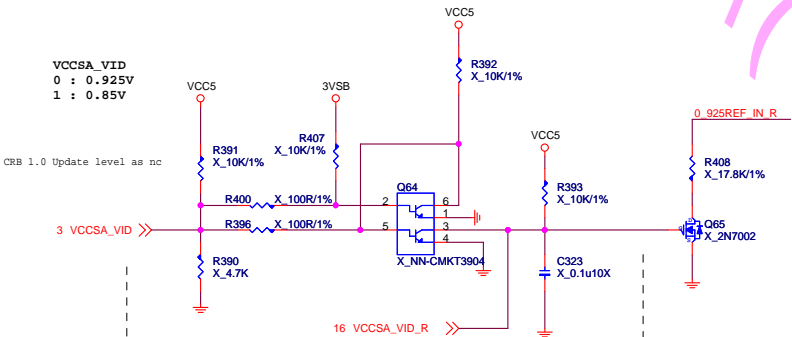
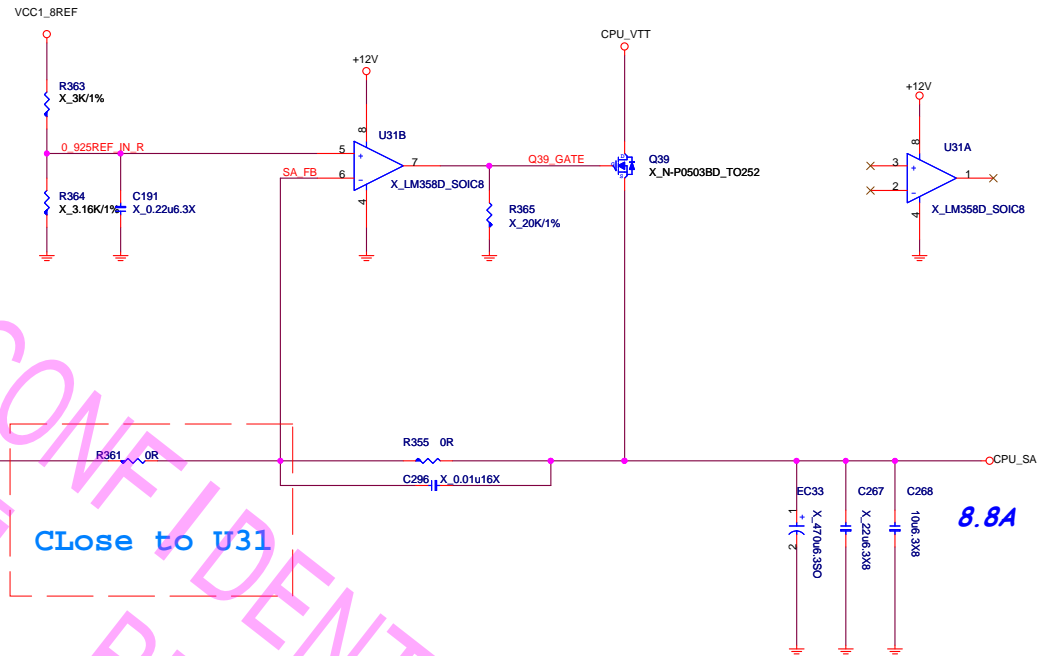
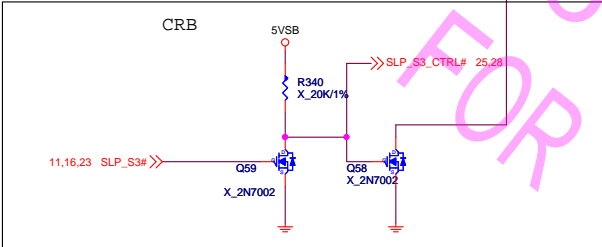
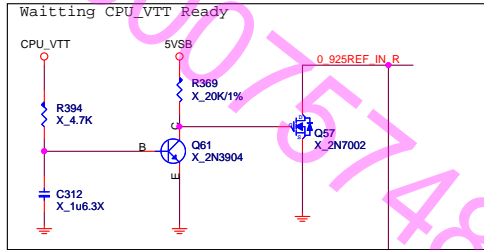


8.5A

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	MS-7788	
Size Custom	Document Description CPU_VTT - UP1504 1-Phase	Rev 10
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CPU_SA:0.925/0.85

SA Core = 8.8A

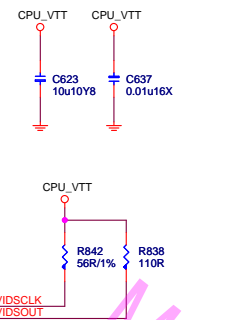
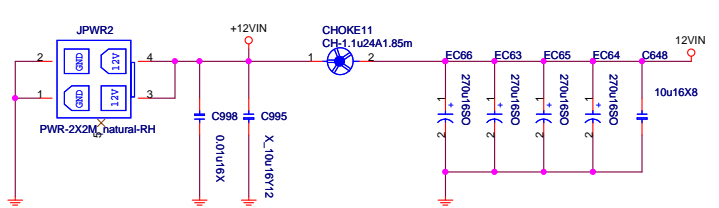
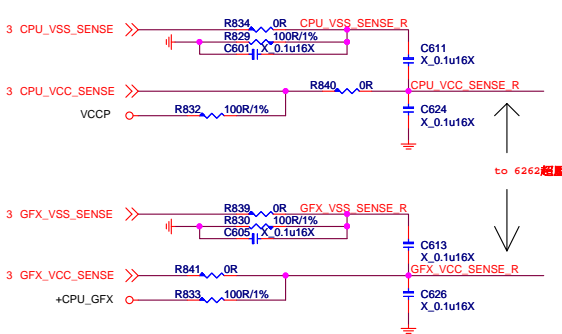
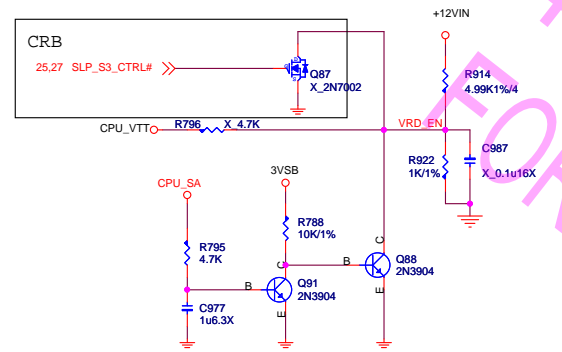
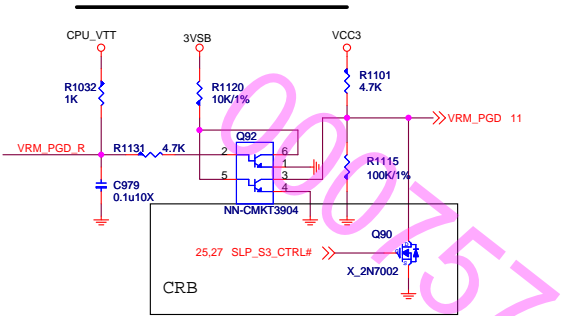


VCCSA_VID	
Low	0.925V
High	0.85V

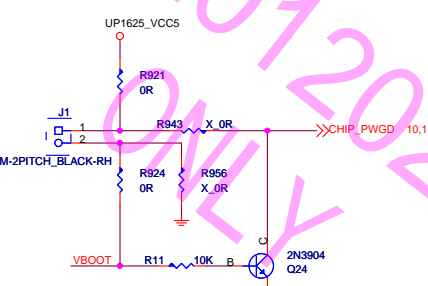
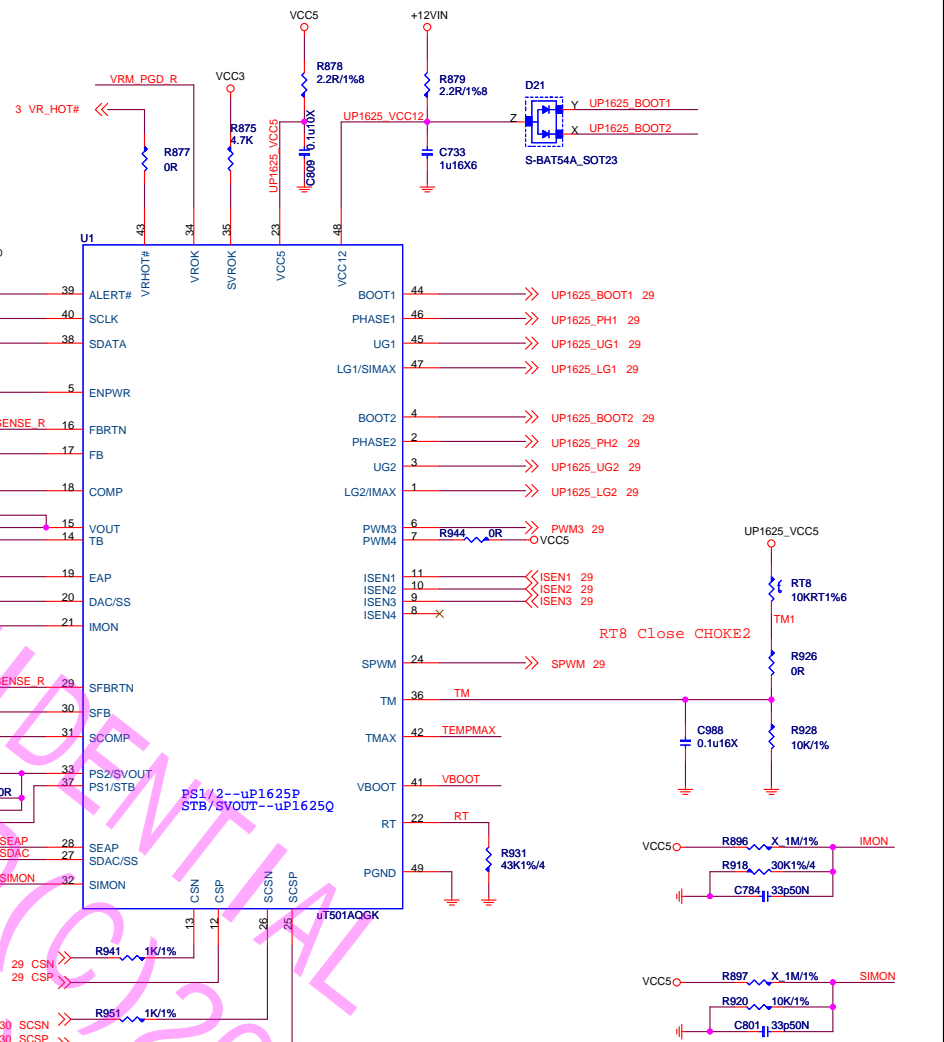
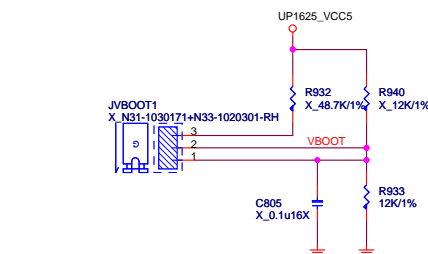
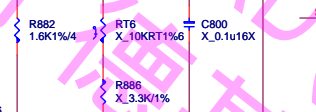
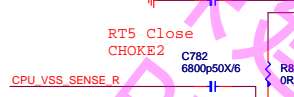
VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

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 2012021500

VRMPWRGD LEVEL SHIFT



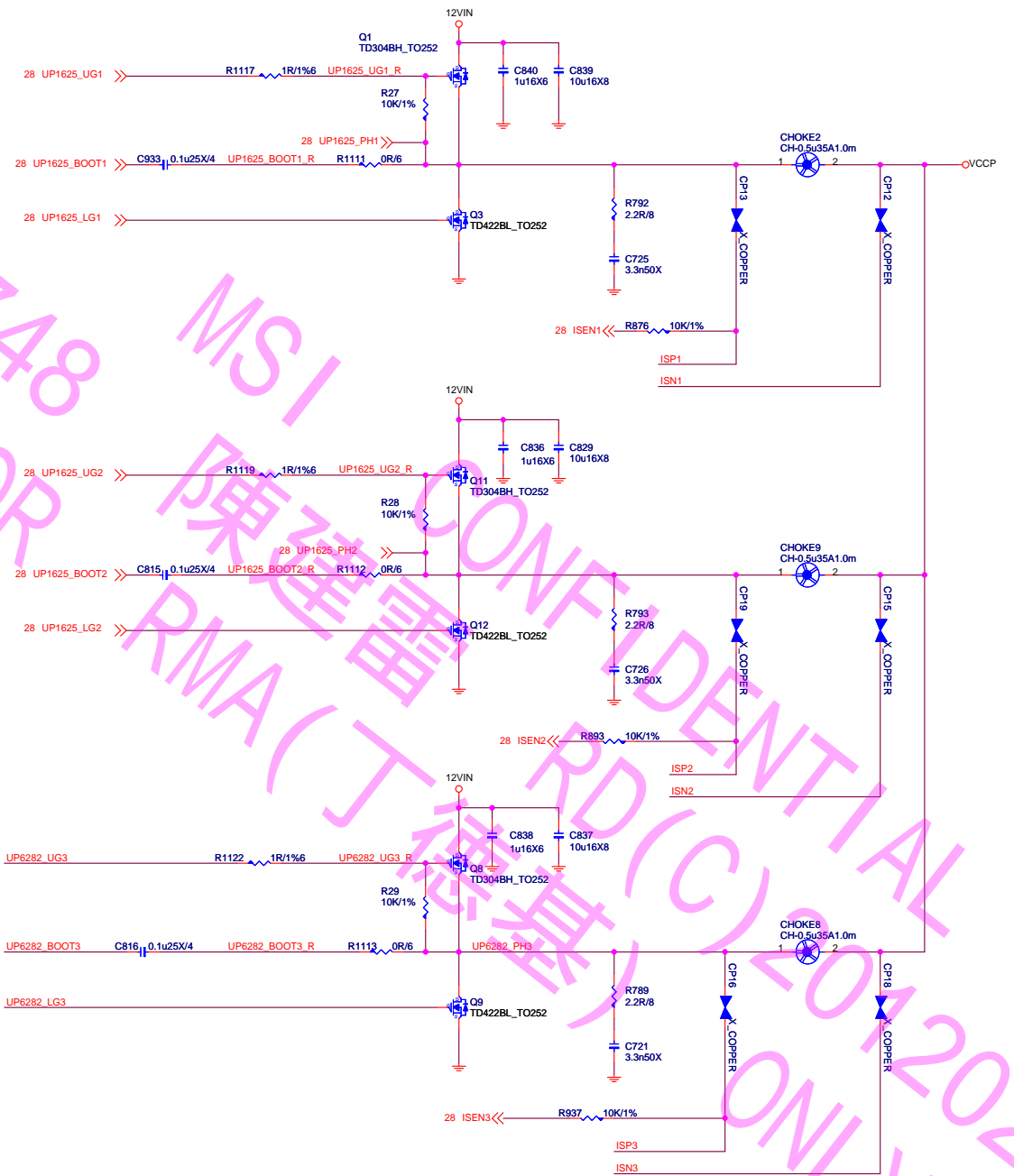
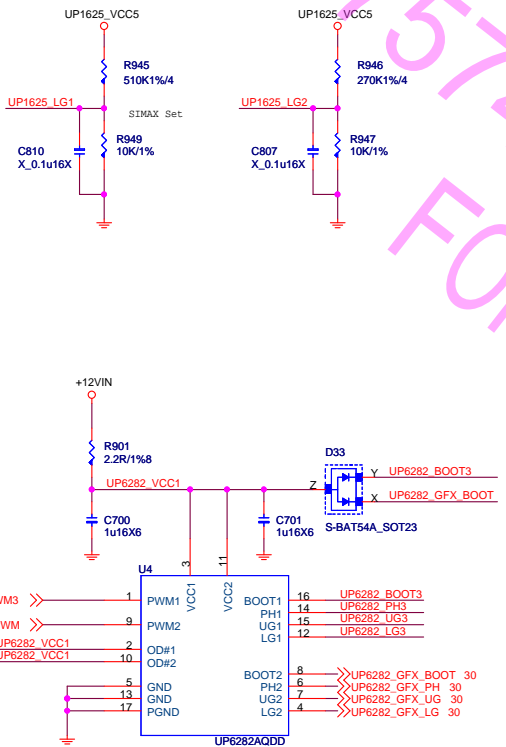
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND



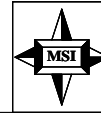
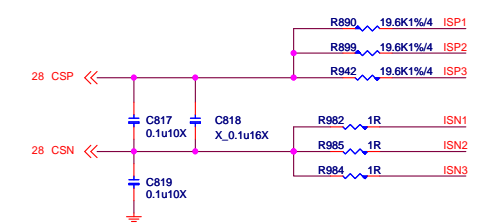
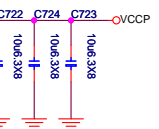
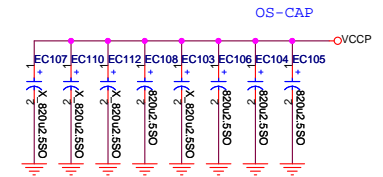
MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description VRD12 - UT501 3+1-Phase	Rev 10
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Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24

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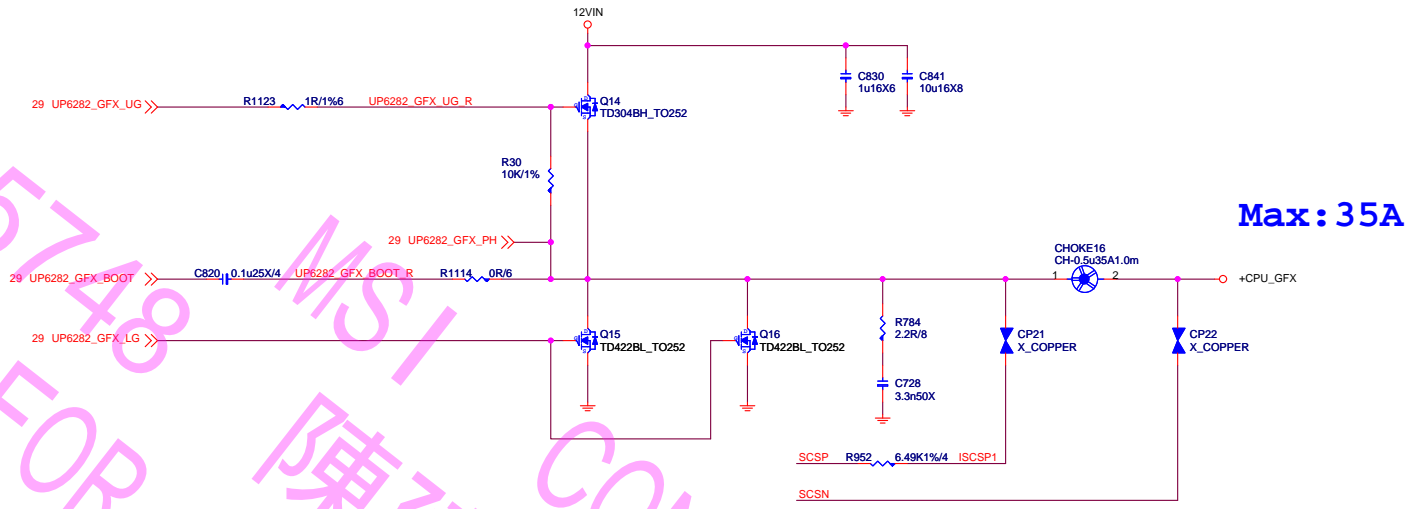


0.5V~1.6V/110A
VCORE 75A TDC:55A
LL:1.7m ohm

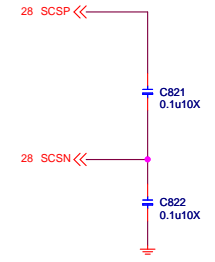
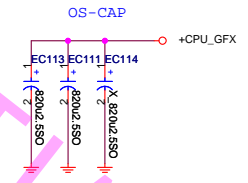


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Size	Document Description	Rev
Custom	UP6234 3-Phase CPU	10
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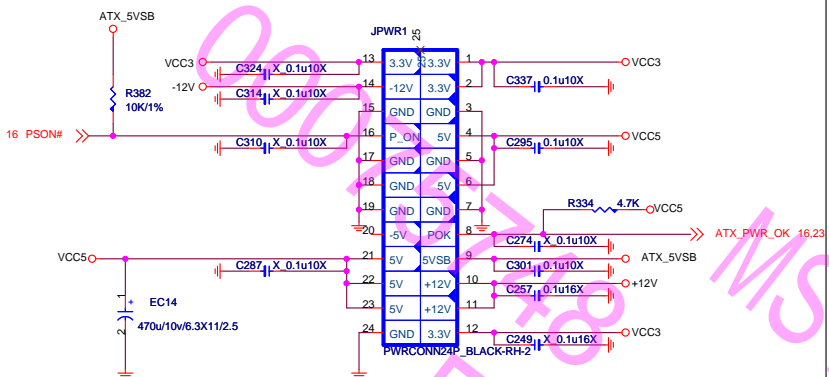


Max: 35A



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Size	Document Description	Rev
Custom	UP6234 1-Phase GPU	10
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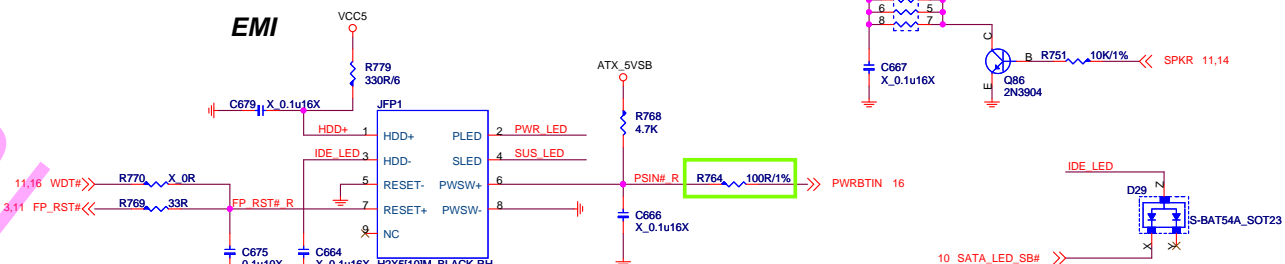
ATX POWER CONNECTOR



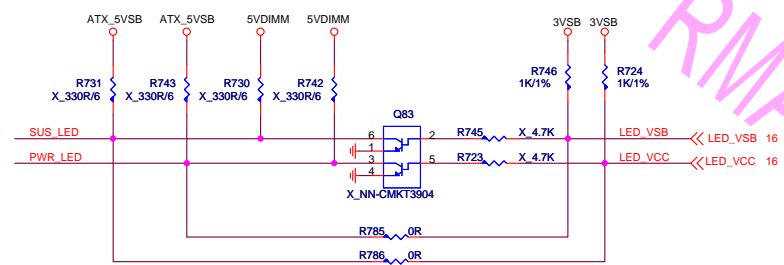
FRONT PANEL

Speaker Pin Header

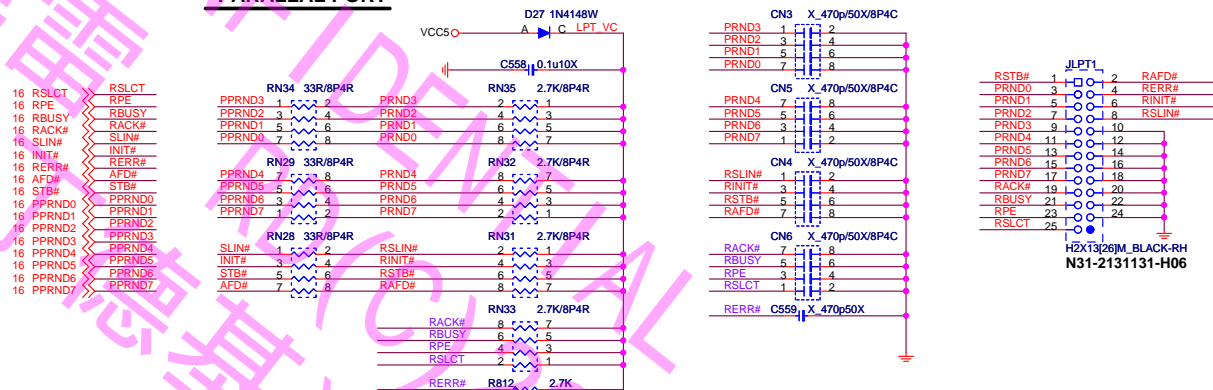
EMI



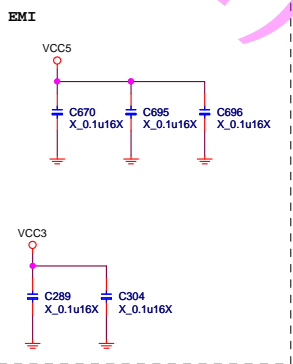
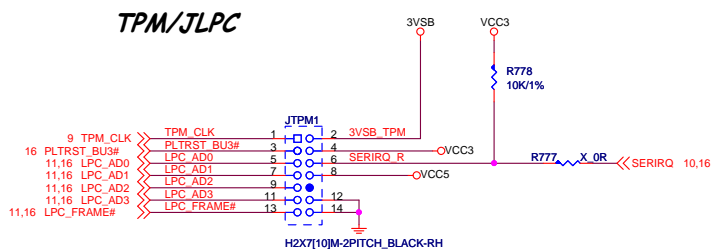
LED (for Fintek 71868)



PARALLAL PORT



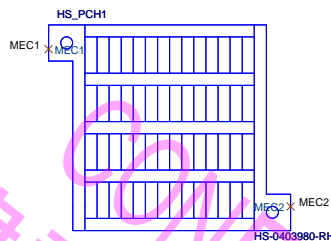
TPM/JLPC



		MICRO-STAR INT'L CO.,LTD	
		MS-7788	
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Custom	ATX PWR-Connector & Front Panel & EMI		10
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OPT	Configure	BOM	Function
A	H61M-P30 (B3)	601-7680-300	H61M-P30 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, Gb Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio, DVI/D-sub, All Solid Cap, EuP, RoHS
B	H61M-P20 (B3)	601-7680-20S	H61M-P22 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, 10/100 Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio(3 hole), DVI/D-sub, Half Solid Cap, EuP, RoHS
C	H61M-P25 (B3)	601-7680-310	H61M-P25 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, Gb Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio(3 hole), DVI/D-sub, Half Solid Cap, EuP, RoHS
D	H61M-P22 (B3)	601-7680-320	H61M-P22 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, 10/100 Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio(3 hole), DVI/D-sub, Half Solid Cap, EuP, RoHS

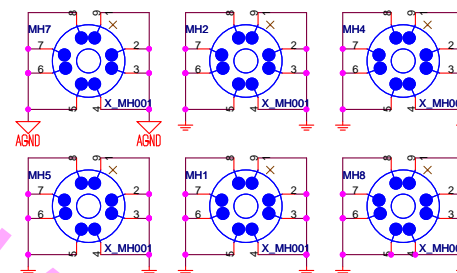
PCH XDP PWRGD/RESET



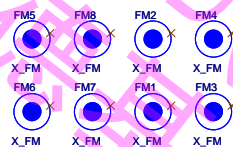
Simulation



Mounting Holes



Optical Fiducial Marks-120



PCB1

7788-10

PK0-0768051-E36, E&E, 23, 寶安恩斯邁廠 (MSIS), 4, Coffee
 PK0-0768051-E36, E&E, 27, 寶安恩斯邁廠 (MSIS), 4, Coffee
 PK0-0768051-G37, 精成, 23, 寶安恩斯邁廠 (MSIS), 4, Coffee
 PK0-0768051-G37, 精成, 27, 寶安恩斯邁廠 (MSIS), 4, Coffee



BAT1_X1

BAT-BCR2032P-RH



RUB1

USB



RUB2

USB



CPU_H1

CPU 鐵座
E21-7557050-L06

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	MS-7788	
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MS-7680 5.1 Change to MS-7778 0A

1. 7.1-Channel Audio out change to 5.1-Channel Audio out.
2. Remove PCIe X1 slot (PCI_E3).
3. Remove SPIDF out.
4. Remove Front USB port*2 (JUSB3).
5. JLPT1 2mm pitch change to 2.54mm pitch.

MS-7788 0A Change to MS-7788 1.0

1. modify VT501 COMP & SCOMP not connection to GND.
2. Vcore : E110 、EC112 、EC103 、EC107 >> N.C
C196 、C198 、C209 、C210 、C211 >> N.C
Vtt : C213 、C214 、C227 、C228 、C265 >> N.C
Vgfx : C109 、C203 、EC114 >> N.C
PWM : C782 、C786 Chang to 6.8nF ; R928 Change to 10K1%
By Power Solution.
3. Add C634 、C642 、C794 、C795 、C802 Empty By Audio codec ALC887 co-lay VT1708S CE.
4. Add C25 Empty By EMI Solution.
5. EC55 & EC56 DIP Footprint Change to SMD DIP Footprint (MSI P/N:C96-1001630-N07) By PM Request.

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