

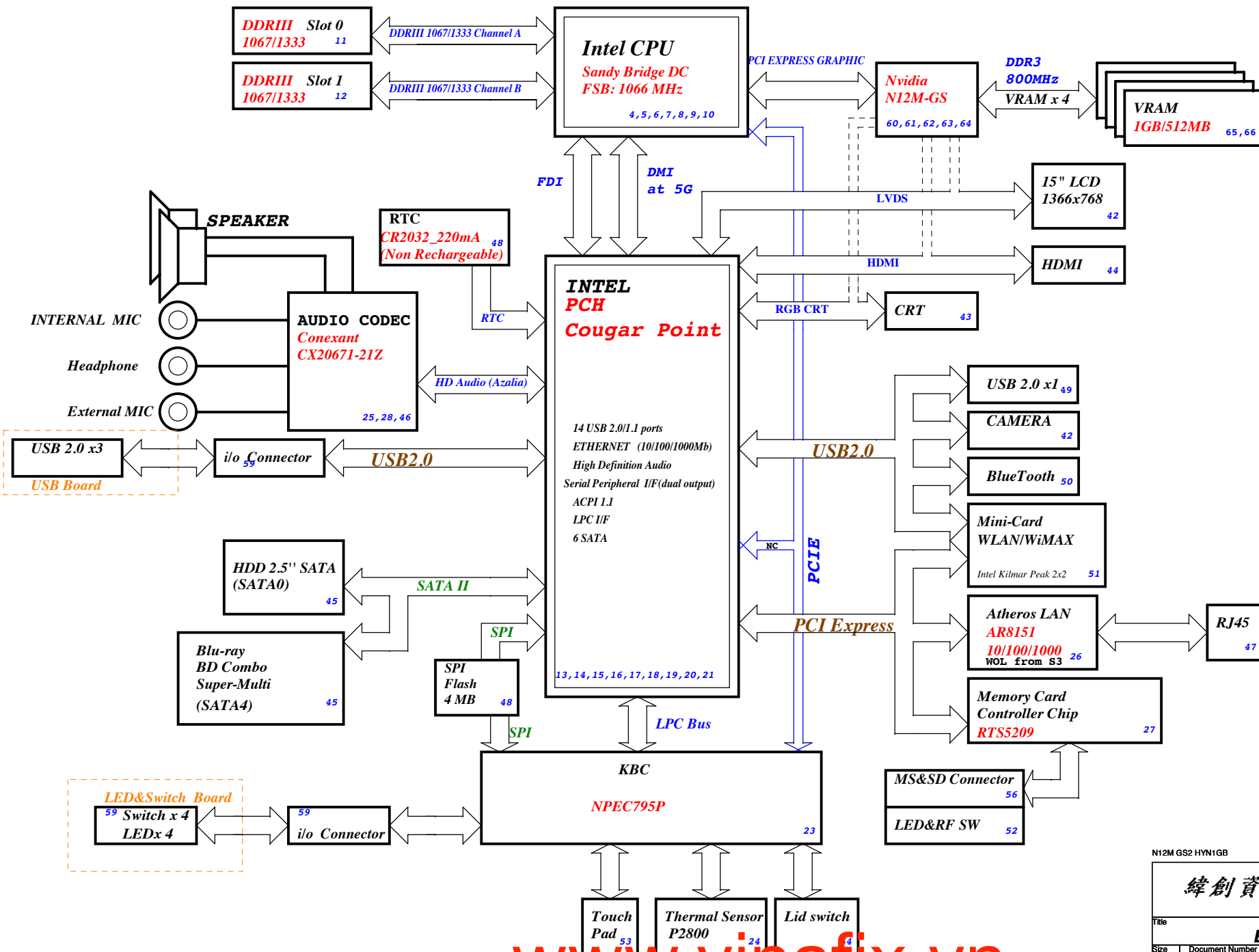
Z50-HR(S204-SC) Schematics Document
Sandy Bridge
Intel PCH
2011-02-14
REV :-1

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N12M GS2 HYN1GB

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Cover Page			
Size	Document Number	Rev	
A3	Z50-HR { Huron River Platform}	-1	
Date:	Wednesday, March 02, 2011	Sheet	1 of 74

Z50-HR Block Diagram



CPU DC/DC ISL95831 35, 36, 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51218D 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC RT8223 34	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC RT8207 39	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
SYSTEM DC/DC ISL95831HRTZ 37	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE
VGA RT8208A 67	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
TI CHARGER BQ24725 33	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC RT9025 40	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
SYSTEM DC/DC APL5916KAI-TRL-GP 41	
INPUTS	OUTPUTS
3D3V_S0	0D85V_S0
Switches 29	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title: **Block Diagram**

Size A3 Document Number: **Z50-HR { Huron River Platform}** Rev: -1

Date: Wednesday, March 02, 2011 Sheet 2 of 74

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port 0:	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following XXRESETB de assertion 0: PEG Wait for BIOS for training	1

PCIE Routing

LANE1	Mini Card1(WLAN)
LANE2	Card Reader
LANE3	N/A
LANE4	GIGA LAN
LANE5	N/A
LANE6	N/A
LANE7	N/A
LANE8	N/A

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	USB Ext. port 2 OC#0
1	USB Ext. port 1 OC#1
2	USB Ext. port 4 OC#2
3	
4	USB Ext. port 3 OC#3
5	X
6	X
7	X
8	X
9	CAMERA OC#5
10	X
11	X
12	Mini Card (LAN)
13	Bluetooth OC#7

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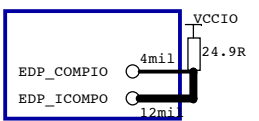
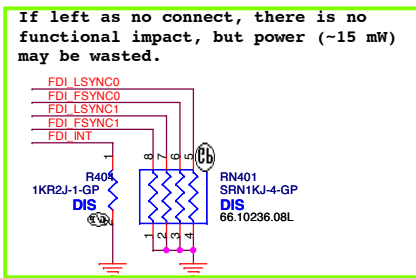
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Table of Content			
Size A3	Document Number	Rev	
Z50-HR { Huron River Platform}		-1	
Date:	Wednesday, March 02, 2011	Sheet	3 of 74

SSID = CPU

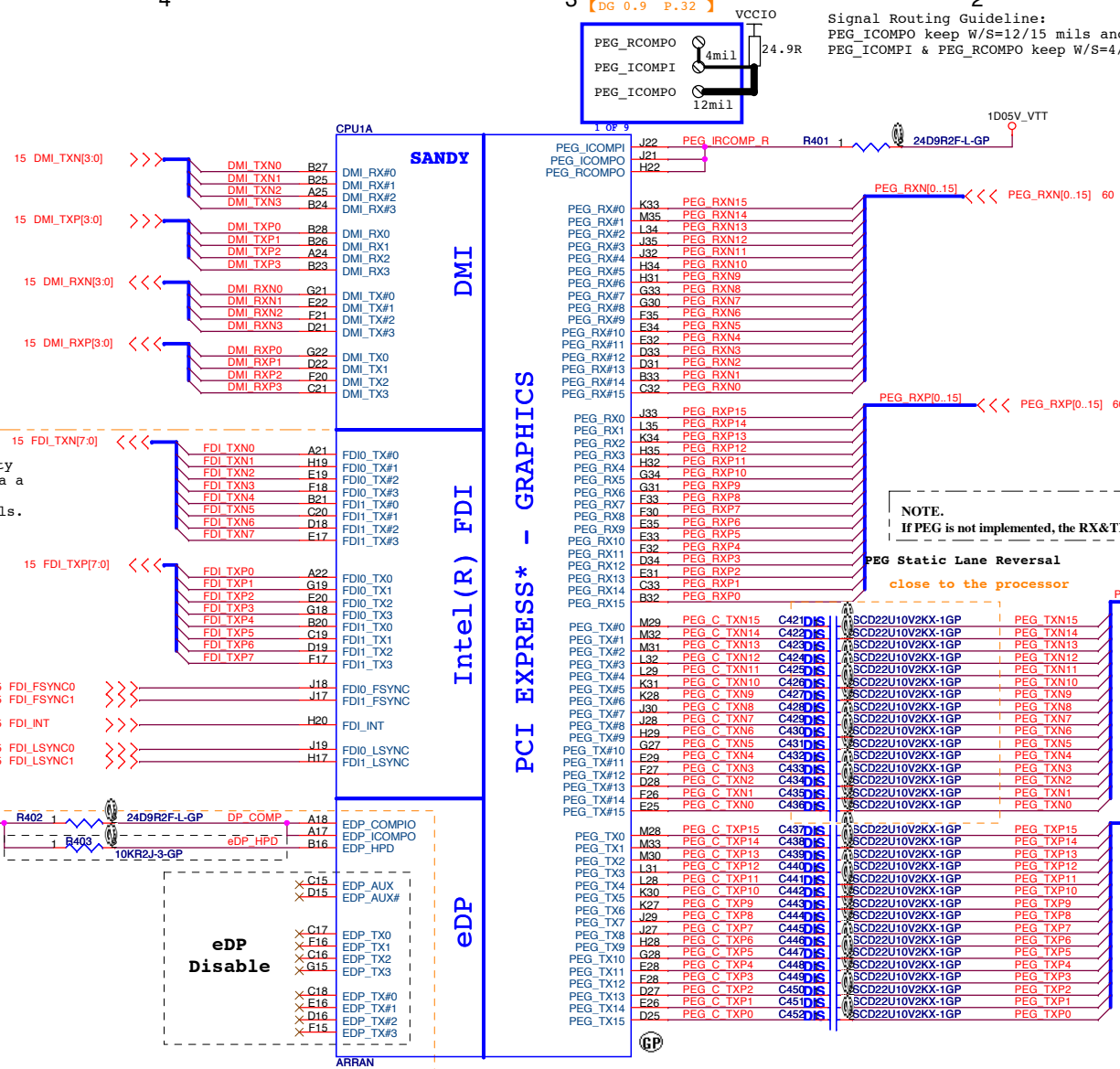
Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap. Lane reversal does not apply to FDI sideband signals.



【DG 0.9 P.54】
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

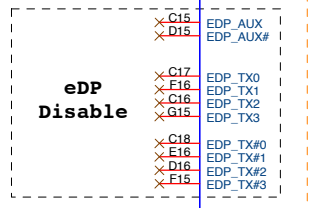
Port	Strap	Enable	Disable
eDP	CFG[4]	Pull down to GND through a 1K ± 5% resistor	No Connect
	EDP_HDP	Pull down to GND through a 1K ± 5% resistor	Pull high to CPU VCCIO through a 10K ± 5% resistor



Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_ROMPO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
IF PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal
close to the processor



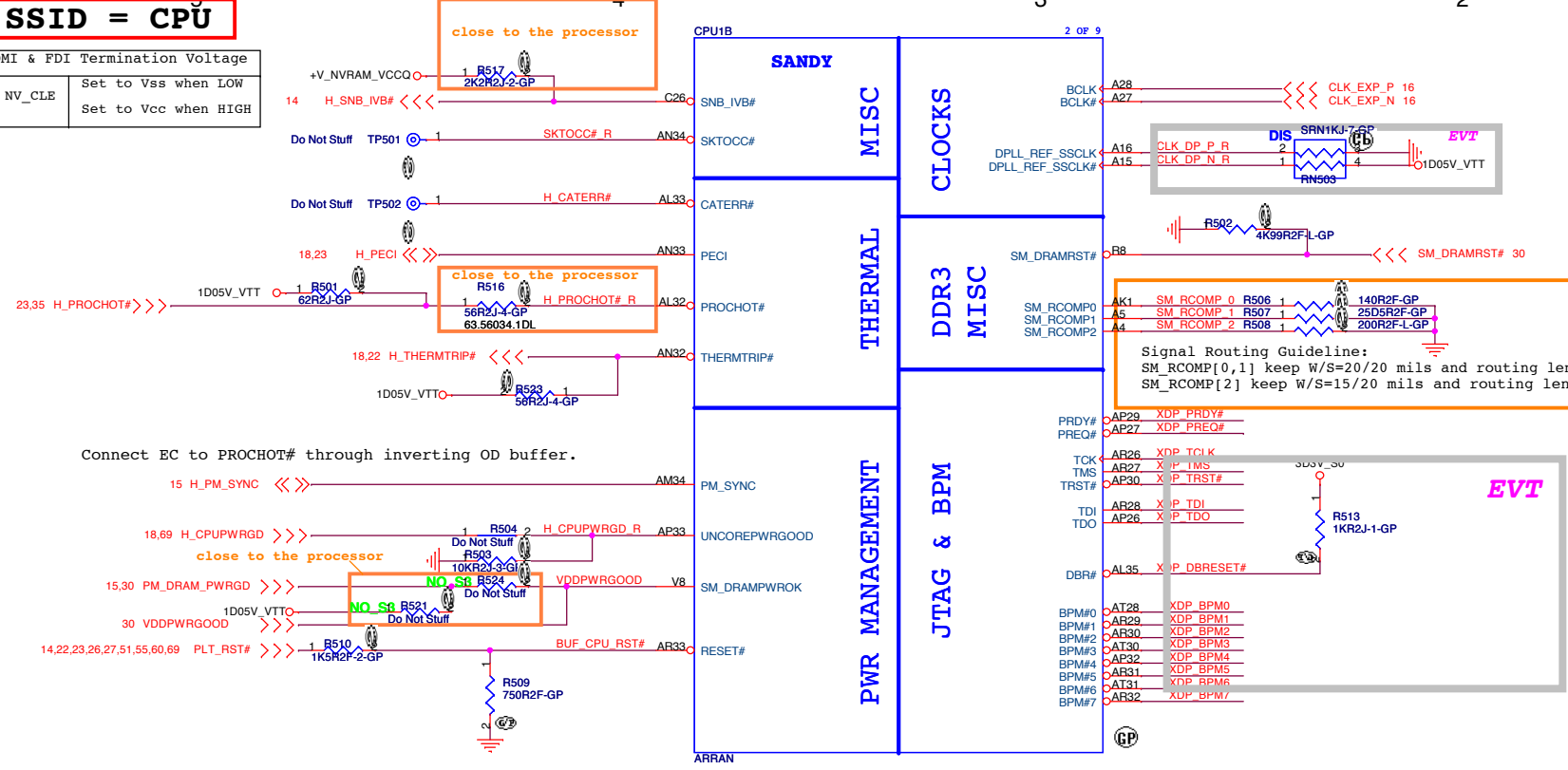
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Title CPU (PCIe/DMI/FDI)		
Size A3	Document Number Z50-HR {Huron River Platform}	Rev -1
Date: Wednesday, March 02, 2011	Sheet 4	of 74

SSID = CPU

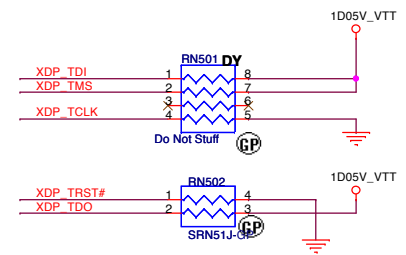
DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH



62.10055.321

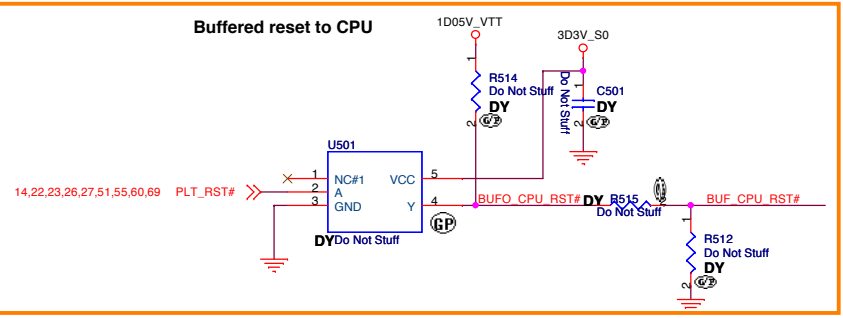
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor (power (~15 mW) may be wasted).

Signal Routing Guideline:
SM_RCOMP[0,1] keep W/S=20/20 mils and routing length less than 500 mils.
SM_RCOMP[2] keep W/S=15/20 mils and routing length less than 500 mils.



XDP Test Point

XDP PRDY#	TP12	Do Not Stuff
XDP PREG#	TP13	Do Not Stuff
XDP_BPM0	TP14	Do Not Stuff
XDP_BPM1	TP15	Do Not Stuff
XDP_BPM2	TP18	Do Not Stuff
XDP_BPM3	TP16	Do Not Stuff
XDP_BPM4	TP19	Do Not Stuff
XDP_BPM5	TP20	Do Not Stuff
XDP_BPM6	TP21	Do Not Stuff
XDP_BPM7	TP22	Do Not Stuff



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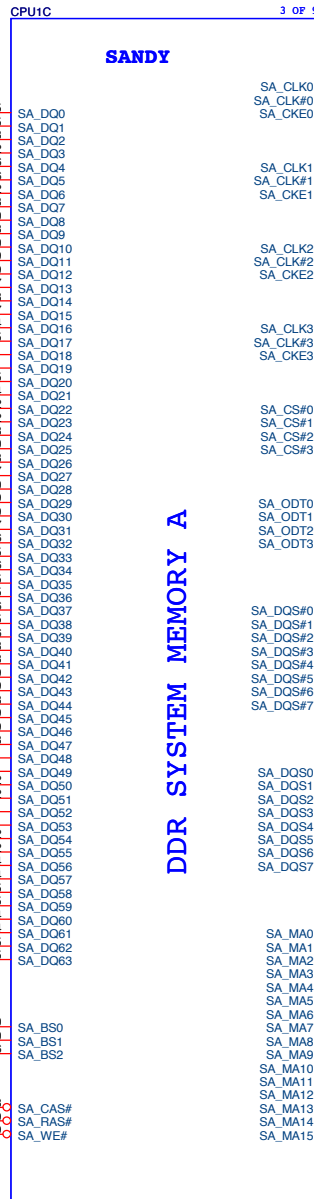
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Title: **CPU (THERMAL/CLOCK/PM)**

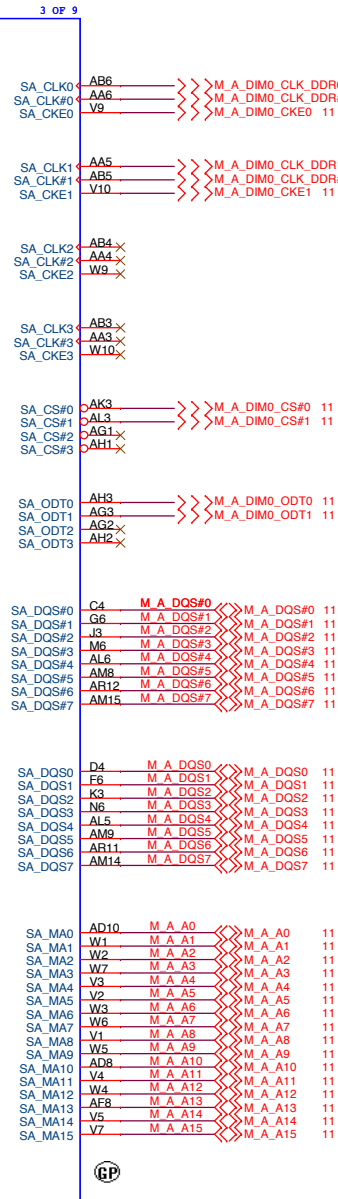
Size A3 Document Number **Z50-HR { Huron River Platform}** Rev -1

Date: Wednesday, March 02, 2011 Sheet 5 of 74

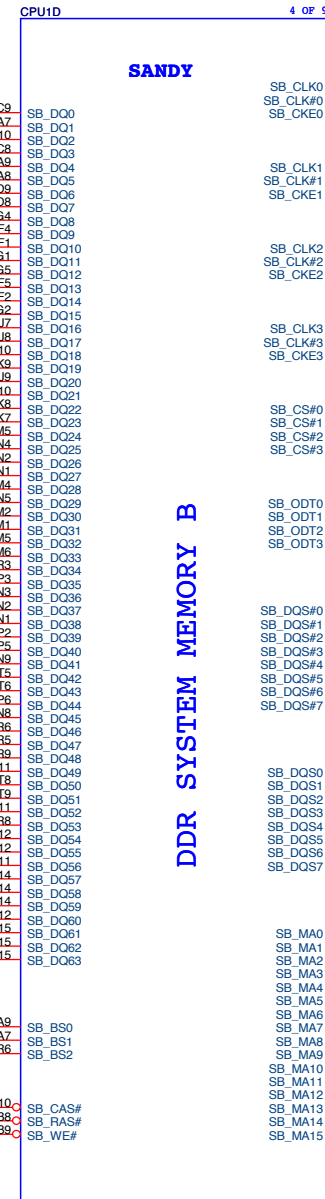
SSID = CPU



DDR SYSTEM MEMORY A



12 M_B_DQ[63:0] <<< M_B_DQ[63:0]



DDR SYSTEM MEMORY B

N12M GS2 HYN1GB

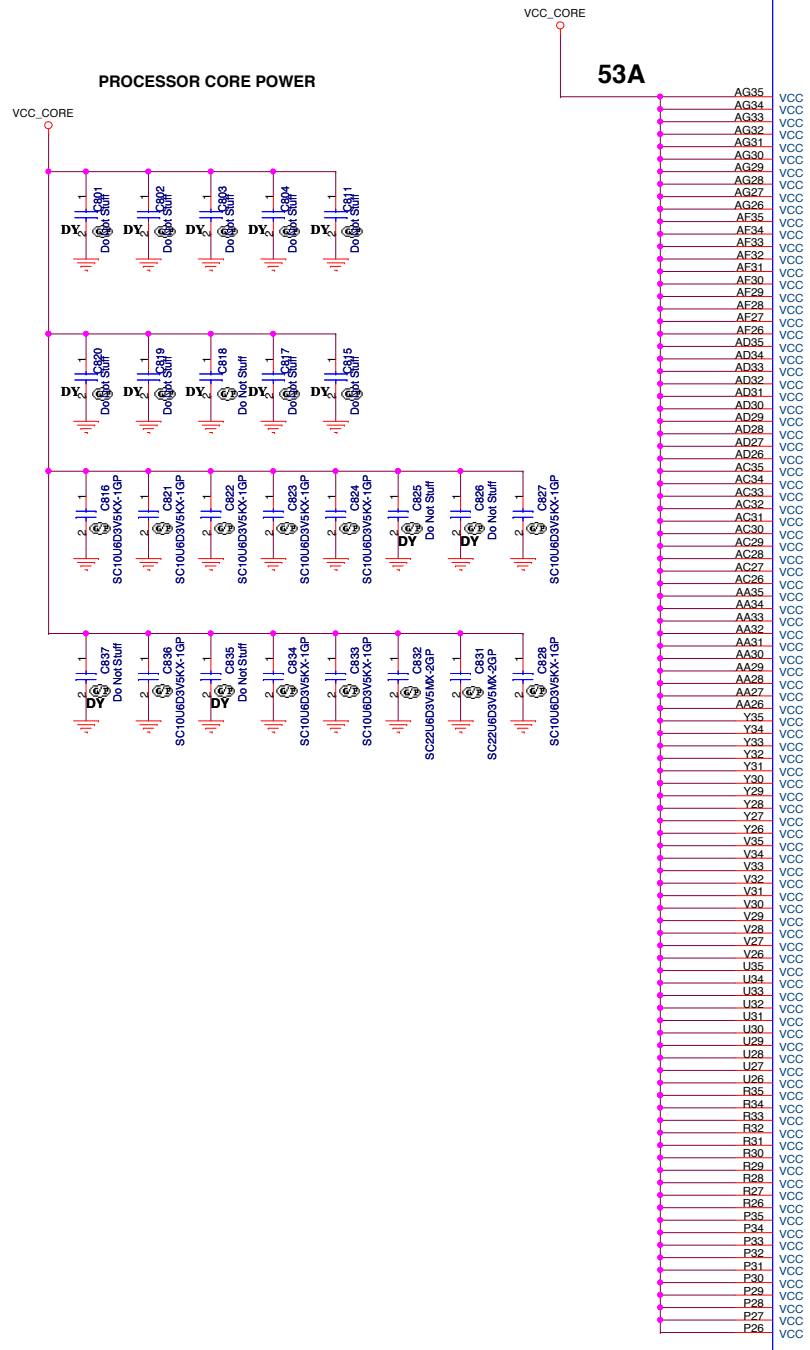
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Title: **CPU (DDR)**

Size A3 Document Number: **Z50-HR { Huron River Platform}** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 6 of 74

SANDY

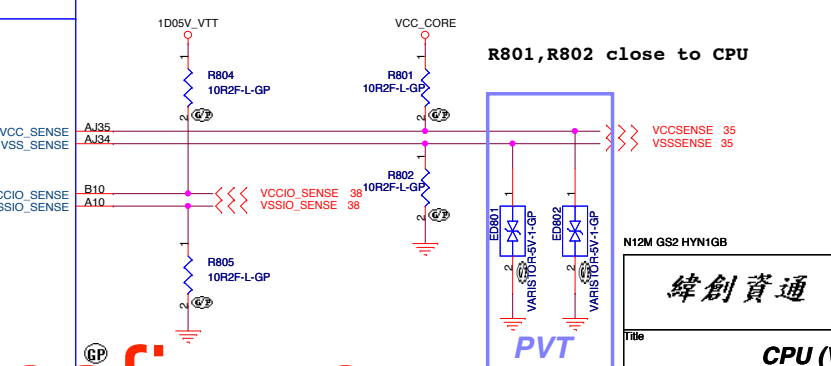
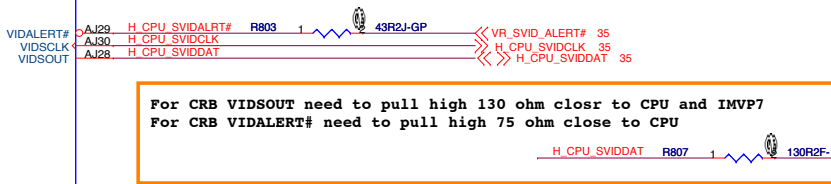
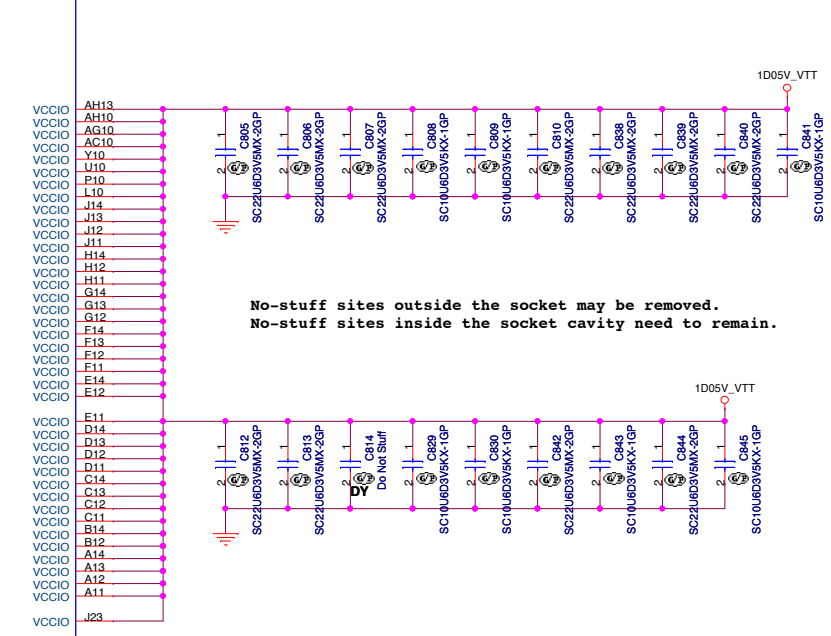


CORE SUPPLY

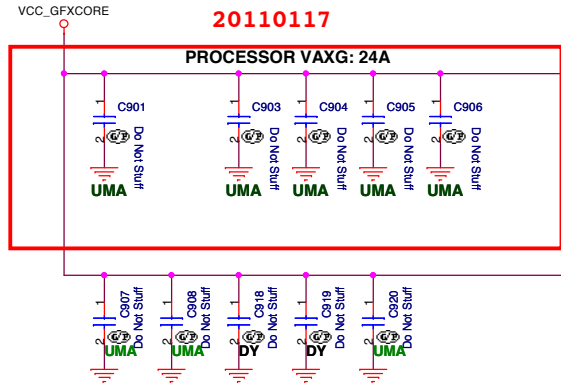
SVID

SENSE LINES

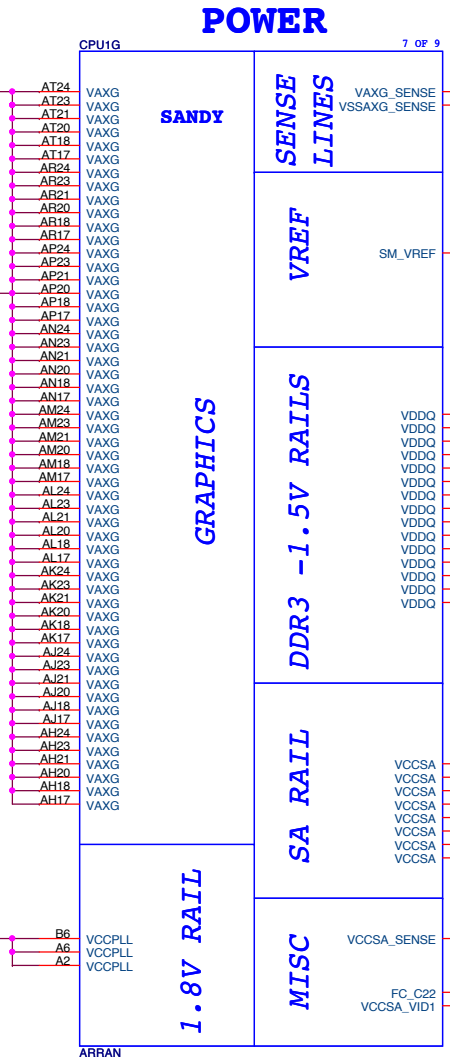
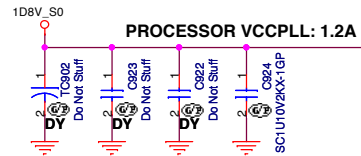
PEG AND DDR



SSID = CPU



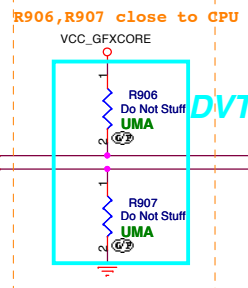
Disabling Guidelines for External Graphics Designs:
 Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
 Can be left floating (Gfx VR keeps VauxG rail from floating) if the VR is stuffed



POWER

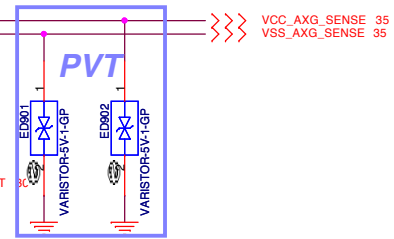
GRAPHICS

1.8V RAIL



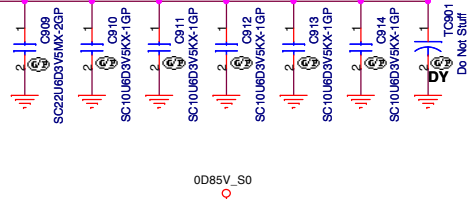
Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

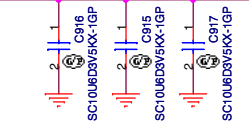


Routing Guideline:
 Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

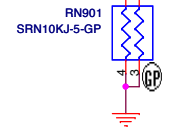
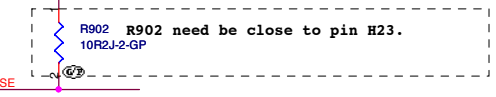
PROCESSOR VDDQ: 10A



PROCESSOR VCCSA: 6A

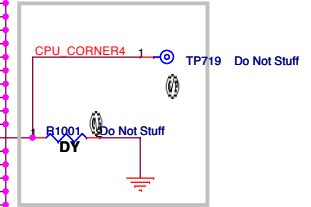
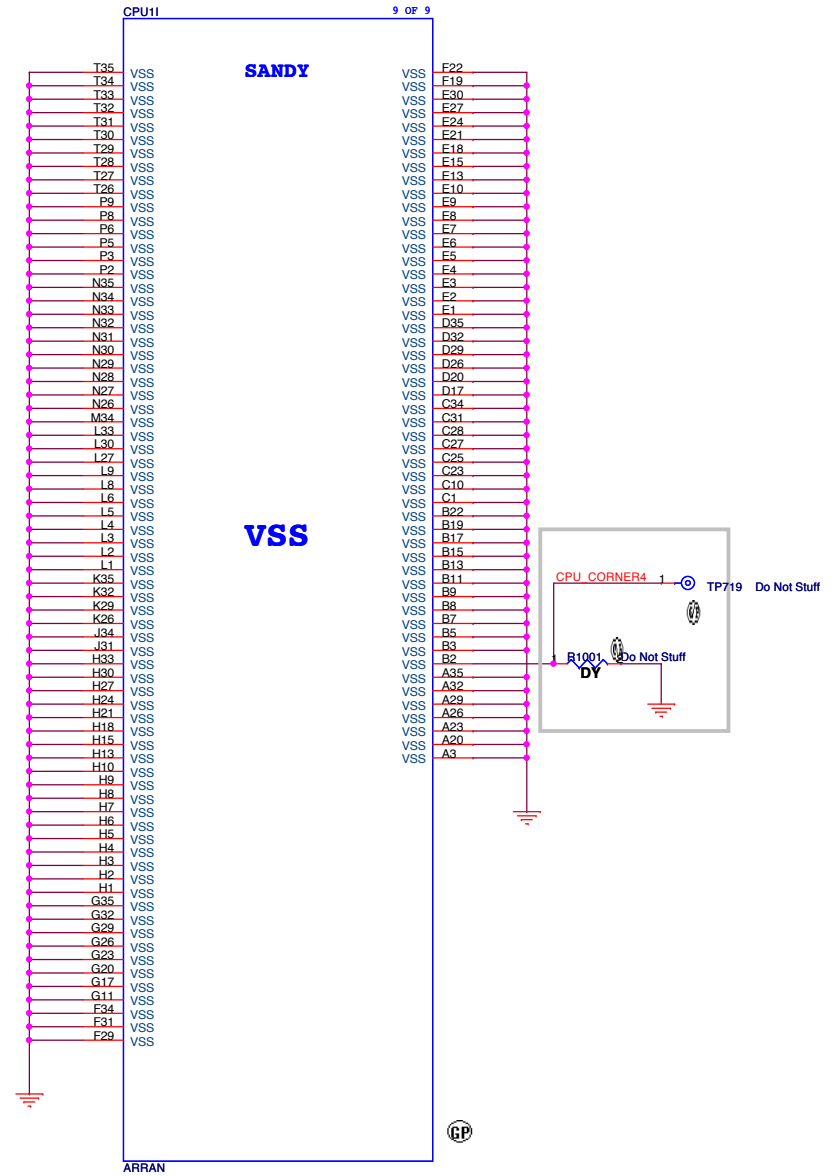
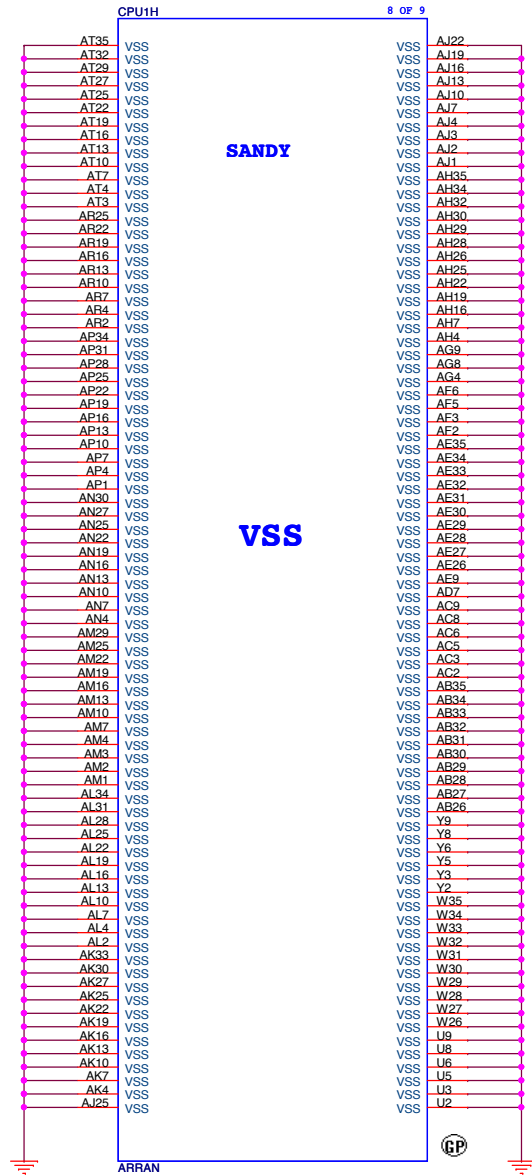


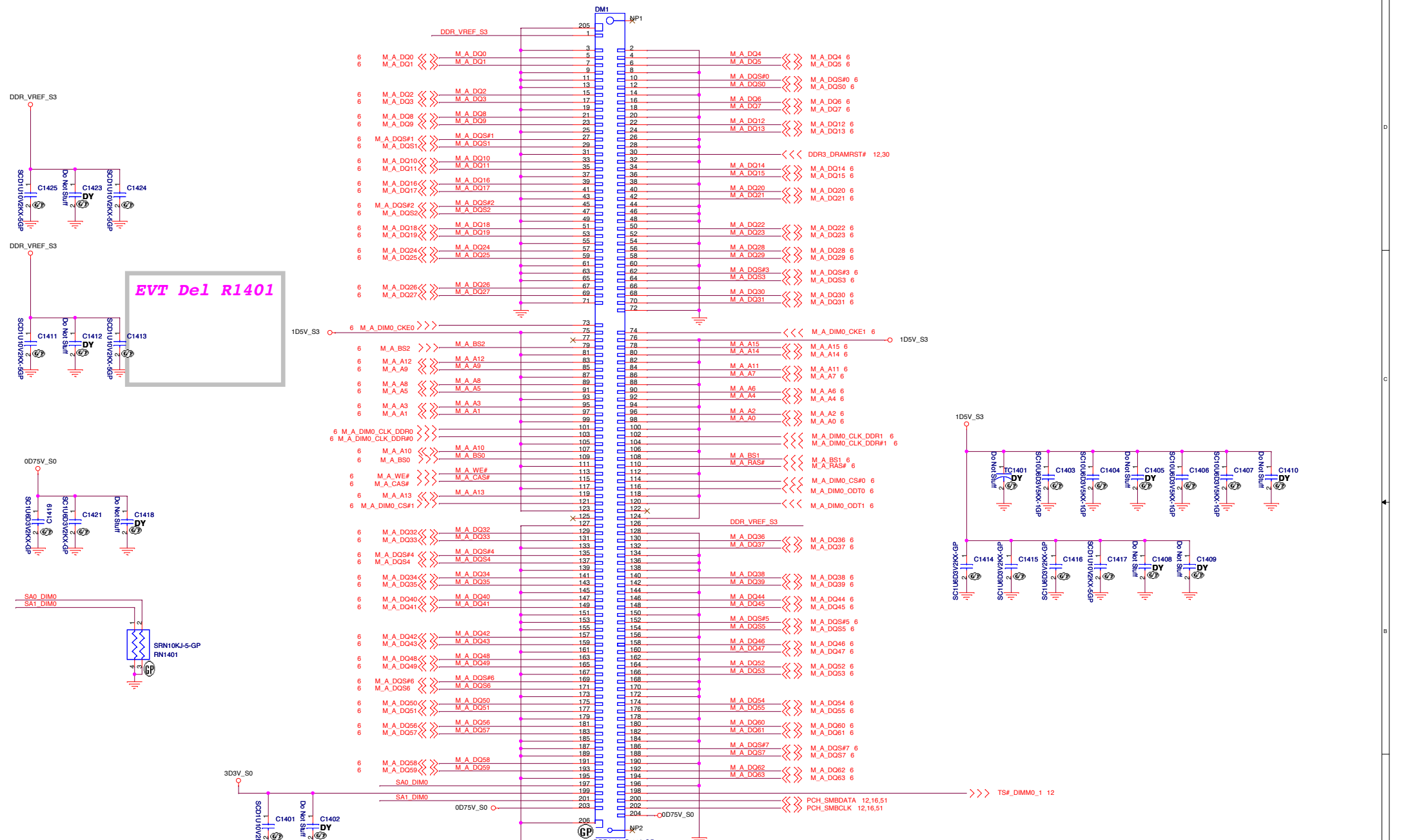
VCCSA Output Decoupling Recommendation:
 1 x 330 uF
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge



H_FC_C22 1 TP901 Do Not Stuff
 VCCSA_Sense TP902 Do Not Stuff

SSID = CPU





EVT Del R1401

62.10017.Z81
 2nd = 62.10017.N41
 3rd = 62.10017.P41

DIMM main = 62.10017.N41
2nd = 62.10017.P41

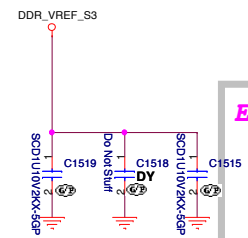
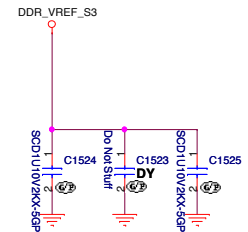
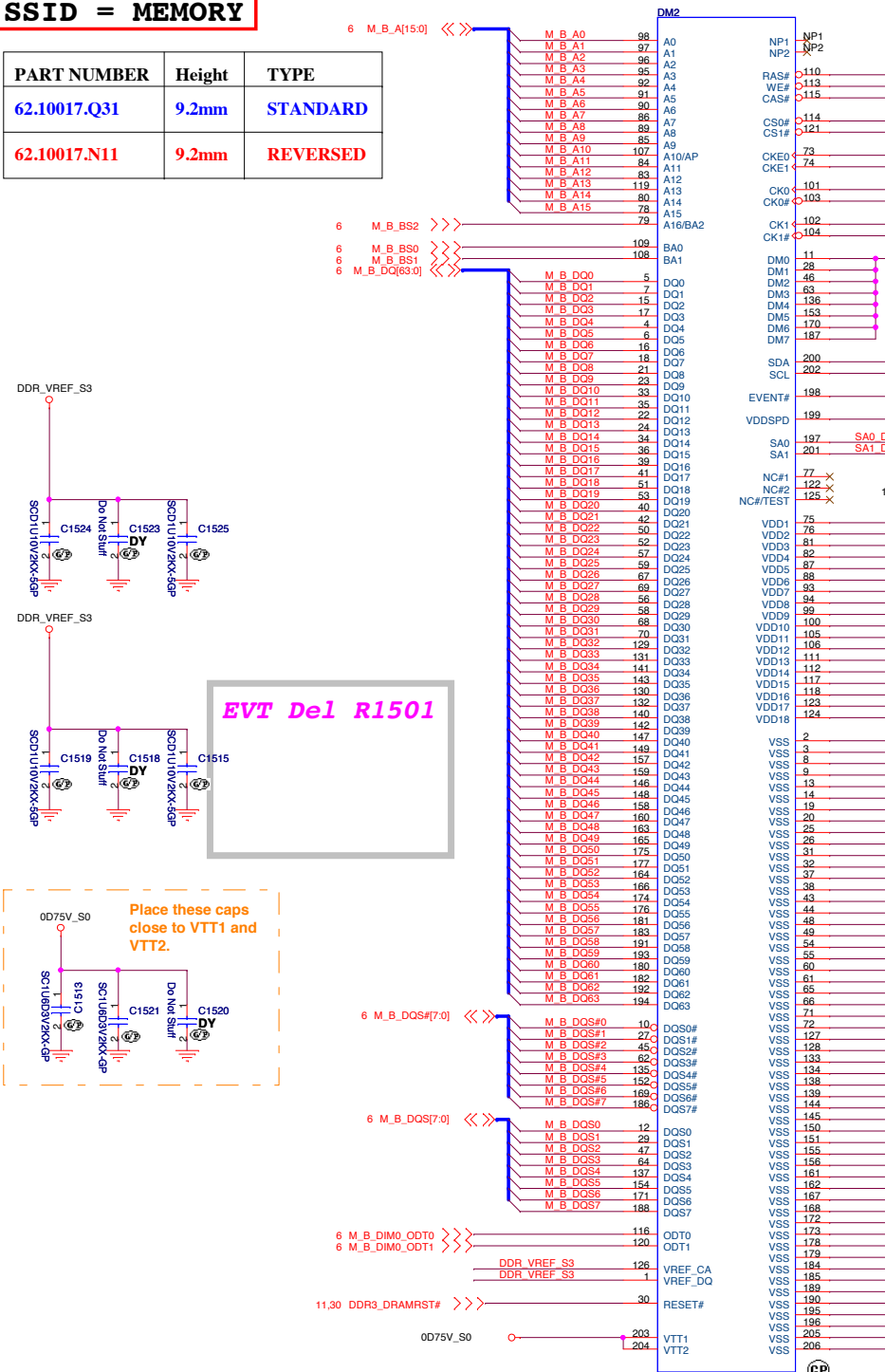
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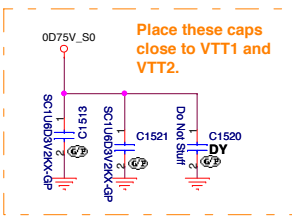
Title DDR3-SODIMM1		
Size Custom	Document Number Z50-HR { Huron River Platform }	Rev -1
Date: Wednesday, March 02, 2011	Sheet 11	of 74

SSID = MEMORY

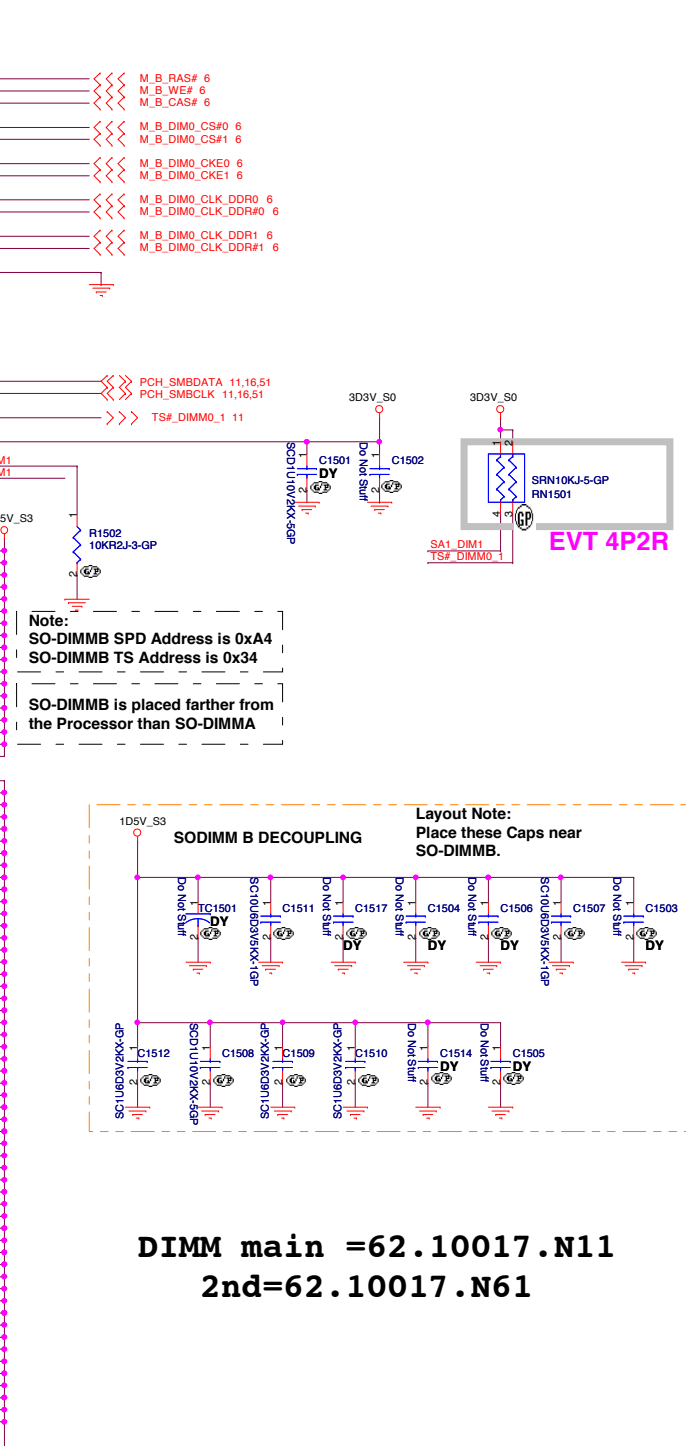
PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED



EVT Del R1501

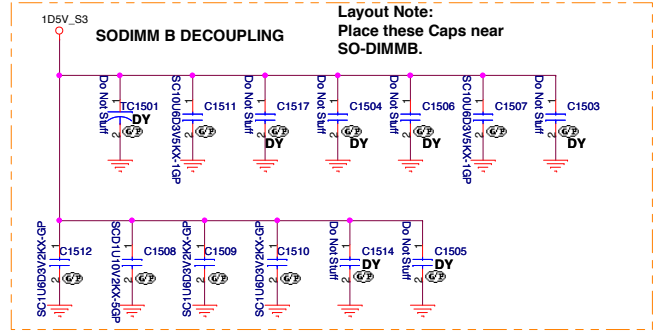


Place these caps close to VTT1 and VTT2.



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



DIMM main =62.10017.N11
2nd=62.10017.N61

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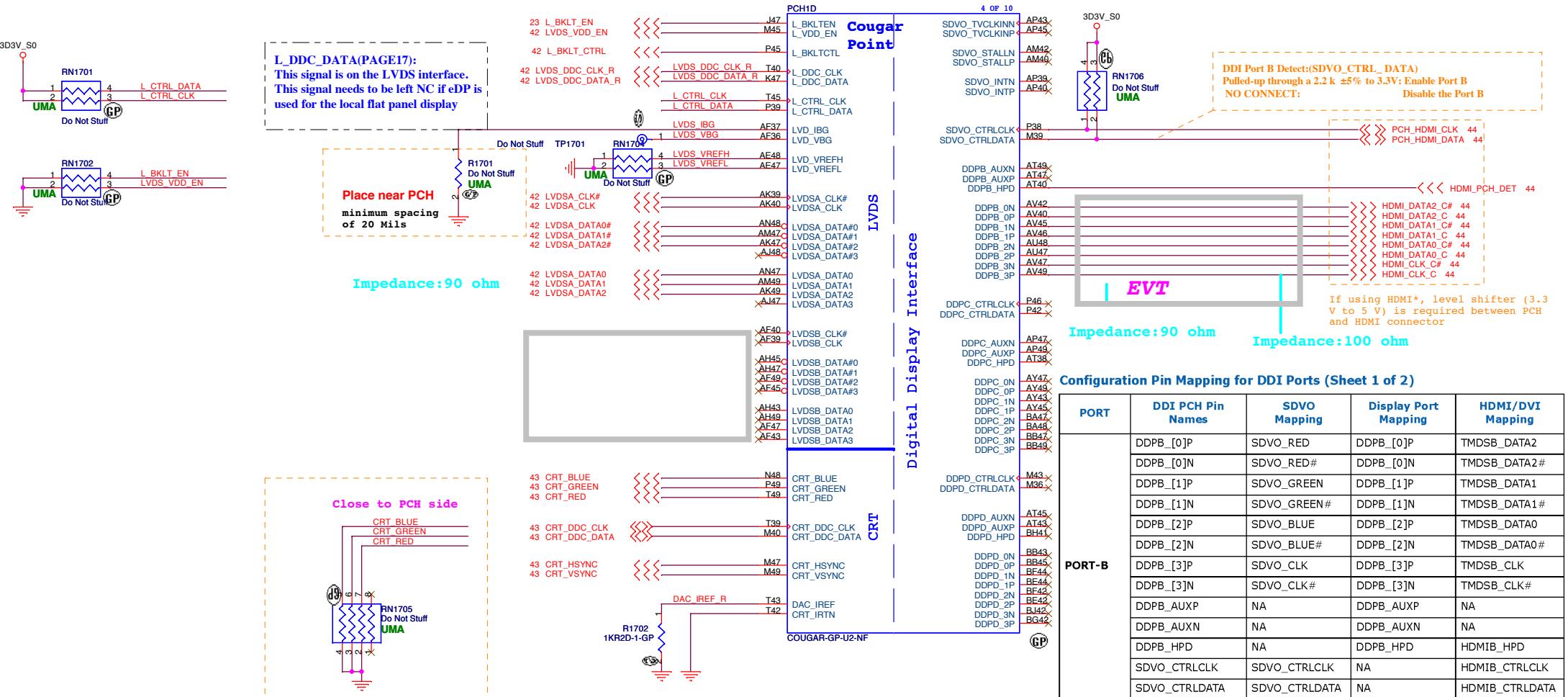
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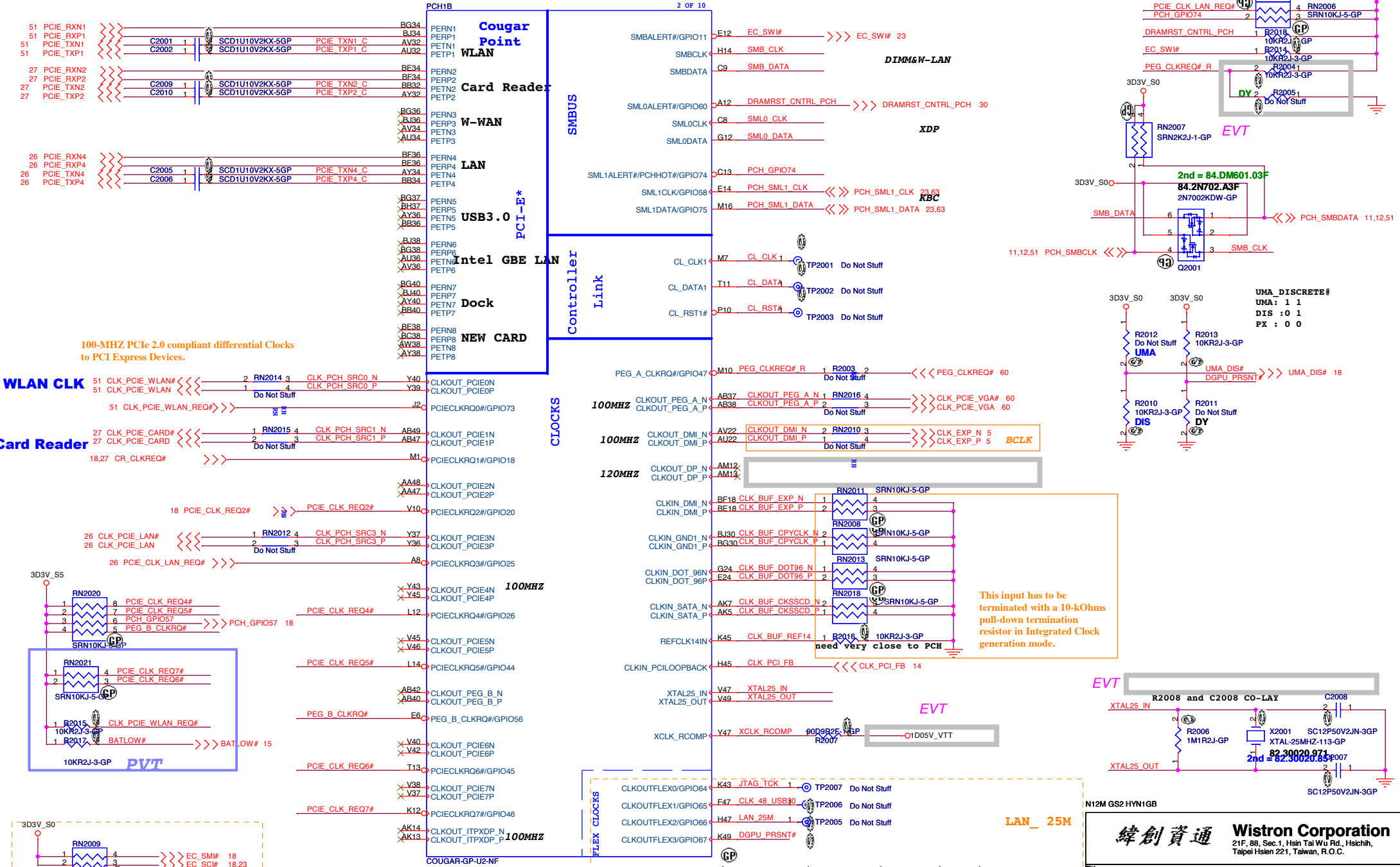
Title: **DDR3-SODIMM2**

Size	Document Number	Rev
Custom	Z50-HR { Huron River Platform}	-1
Date:	Wednesday, March 02, 2011	Sheet 12 of 74

CHANGE TO 71.0HM65.00U



SSID = PCH

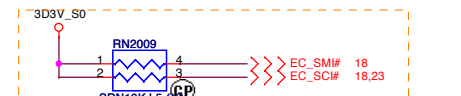
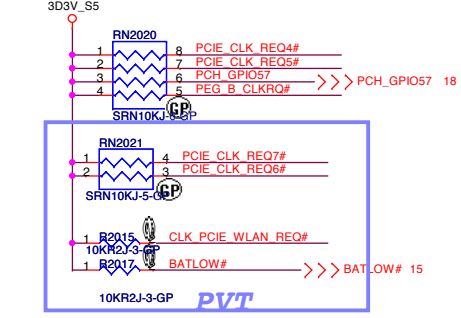


100-MHz PCIe 2.0 compliant differential Clocks to PCI Express Devices.

WLAN CLK
51 CLK_PCIE_WLAN# <<<< 2 RN2014 3 CLK_PCH_SRC0_N Y40
51 CLK_PCIE_WLAN# <<<< 1 Do Not Stuff
51 CLK_PCIE_WLAN_REQ# >>>> J2

Card Reader
27 CLK_PCIE_CARD# <<<< 1 RN2015 4 CLK_PCH_SRC1_N AB49
27 CLK_PCIE_CARD# <<<< 2 Do Not Stuff
18,27 CR_CLKREQ# >>>> M1

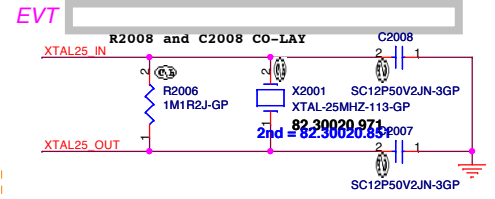
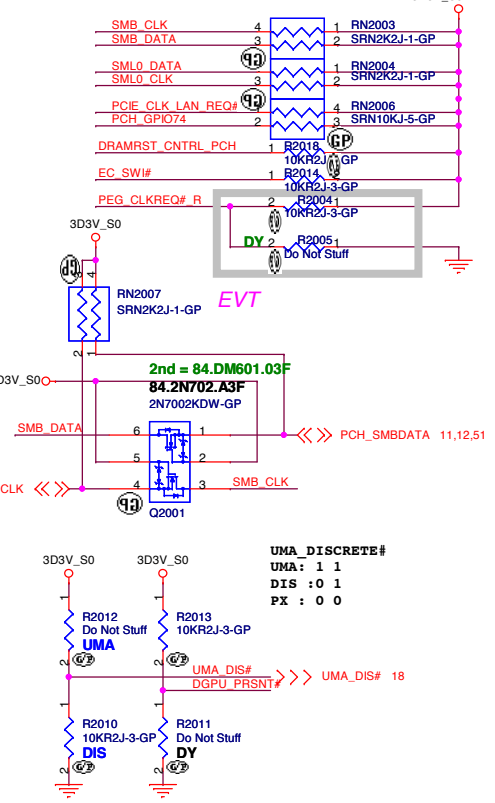
26 CLK_PCIE_LAN# <<<< 1 RN2012 4 CLK_PCH_SRC3_N Y37
26 CLK_PCIE_LAN# <<<< 2 Do Not Stuff
26 CLK_PCIE_LAN_REQ# >>>> A8



PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

CLKOUTFLEX0-33 MHz/14.31818 MHz/27MHz (SSC/non-SSC)/48MHz/24MHz
CLKOUTFLEX1,3-14.31818 MHz/27MHz (SSC/non-SSC)/48MHz/24MHz
CLKOUTFLEX2-3 MHz/15MHz/14.31818 MHz/27MHz (SSC/non-SSC)/48MHz/24MHz

This input has to be terminated with a 10-Kohms pull-down termination resistor in Integrated Clock generation mode.

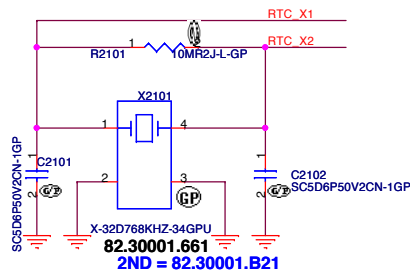


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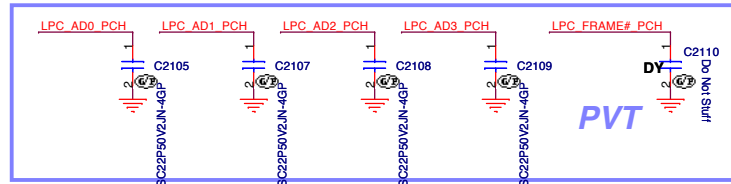
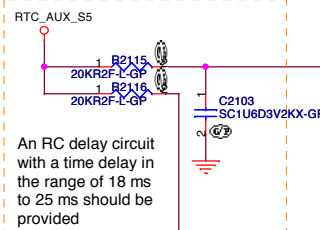
SSID = PCH

Functional Strap Definitions

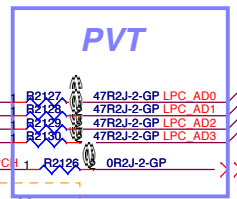
[EDS 1.0 P.89]



Intruder Detect: [EDS 1.0 P.195]
 This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.

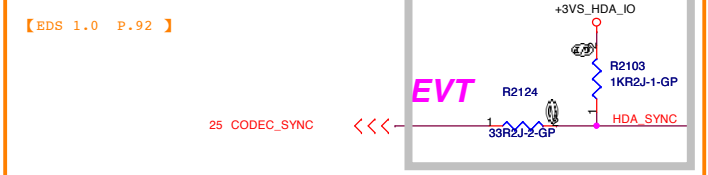


INTVRMEN- Integrated SUS [EDS 1.0 P.90]
 1.05V VRM Enable
 High - Enable internal 1.05 V regulators.
 Low - Enable external 1.05 V regulators.
 NOTE: This signal should always be pulled high



GPI033
 Pull-down with 1K is recommended for manufacturing environment. There is an internal pull-up of 20 k for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.

- HDA_SDO and HDA_BCLK must be length matched to within 500 mils
- HDA_DOCK_EN# length matched of 500 mils with HDA_BCLK.



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

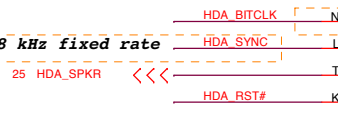
This signal has a weak internal pull down.
 On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
 Needs to be pulled High for Huron River platform. co-operate with R2310

On-Die PLL Voltage Regulator Voltage Select	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

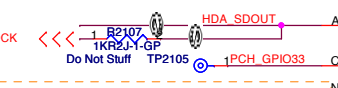
NO REBOOT STRAP [EDS 1.0 P.89]
 Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature)

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

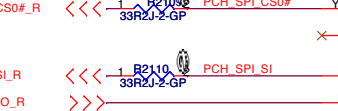
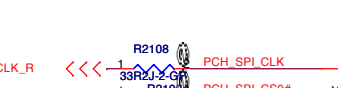
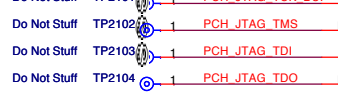
Flash Descriptor Security Override/ ME Debug Mode
 HDA_SDOUIT Low = Default
 High = Enable [EDS 1.0 P.92]



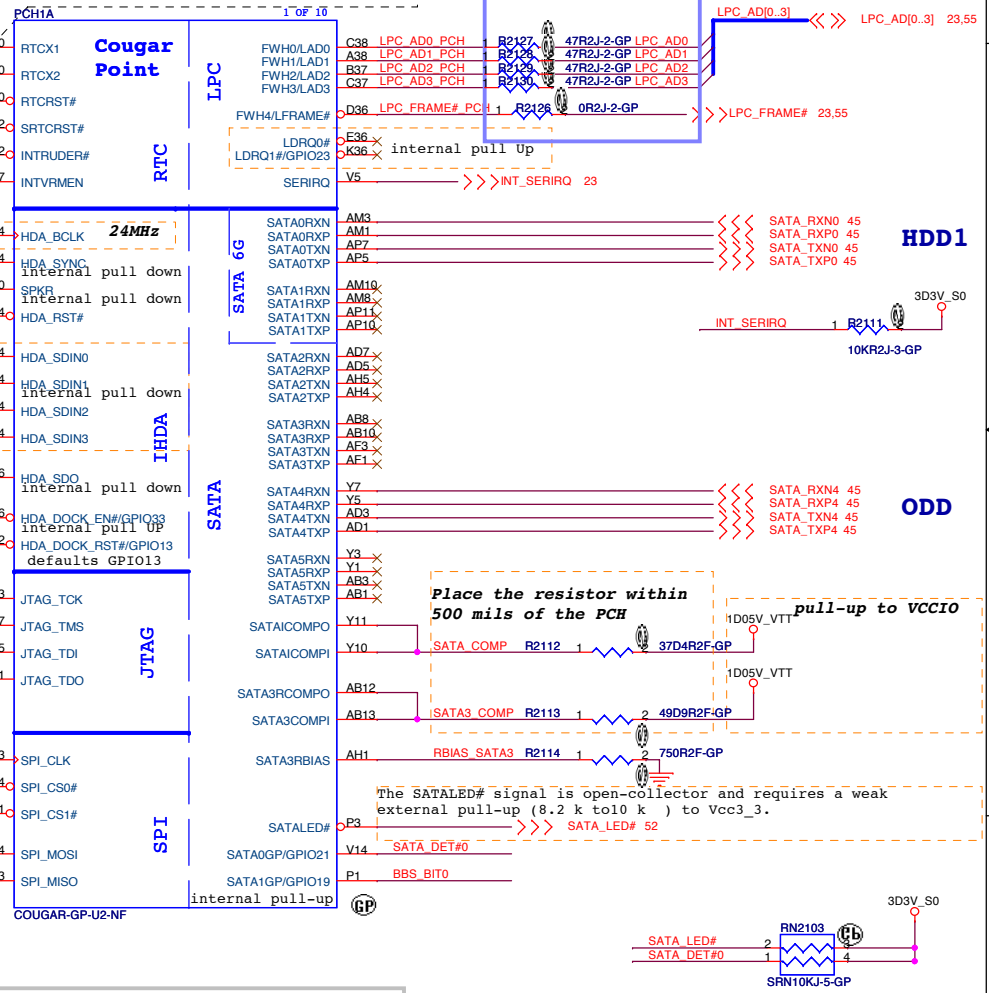
Can be left NO CONNECT if not used (internal pull-down resistors that are always enabled).



This can be left unconnected when not in use.



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	Reserved



Place the resistor within 500 mils of the PCH pull-up to VCCIO

The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to Vcc3_3.

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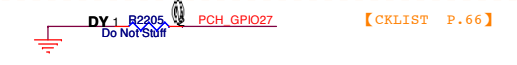
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size A3 Document Number: **750-HR (Huron River Platform)** Rev -1

Date: Wednesday, March 02, 2011 Sheet 17 of 74

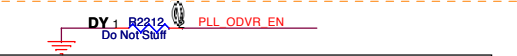
Integrated Clock Chip Enable	
HIGH (R2211 DY)- DISABLED [DEFAULT]	
ICC_EN#	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up. Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

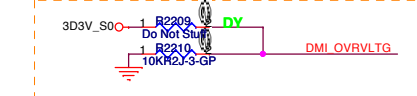
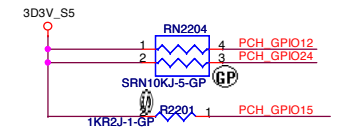
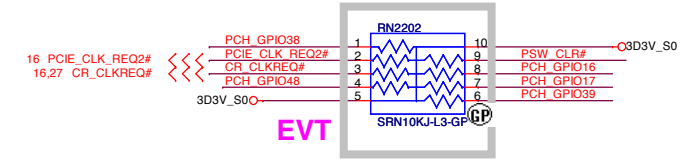


Deep Sleep	
HIGH (R2019 DY)- ENABLED [DEFAULT]	
GPIO27	LOW (R2019) - DISABLED

GPIO27 has a weak[20K] internal pull up. If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

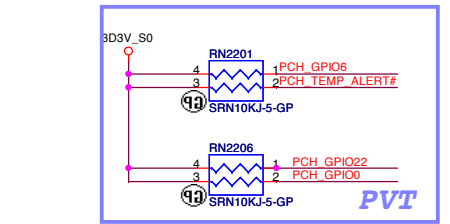


The On-Die PLL voltage regulator
NOTE: This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)
If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.



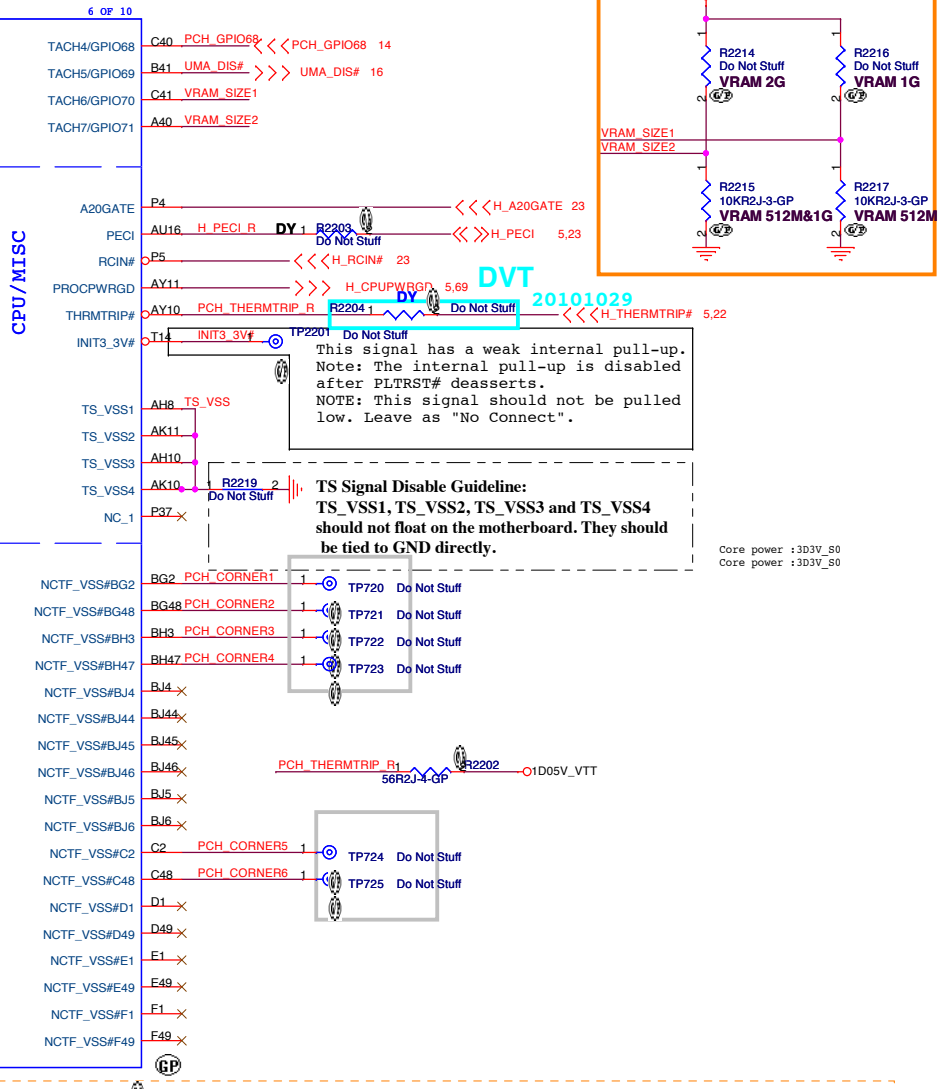
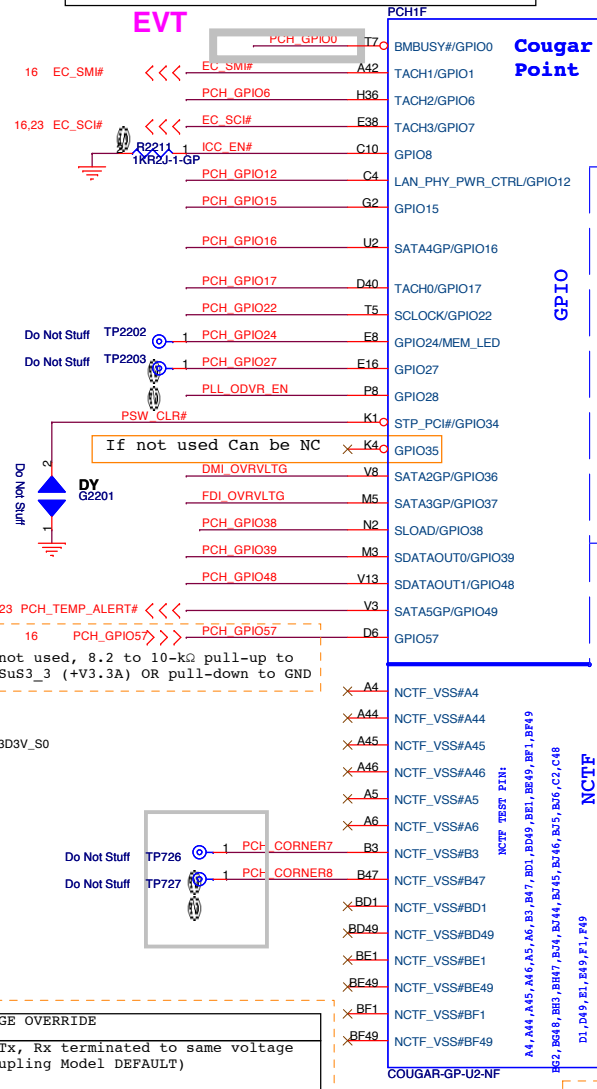
DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.
This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

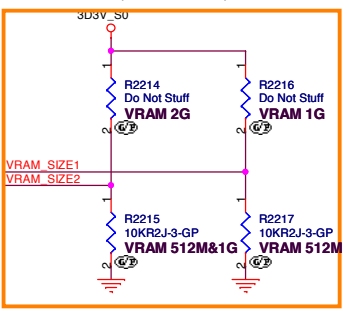


SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218



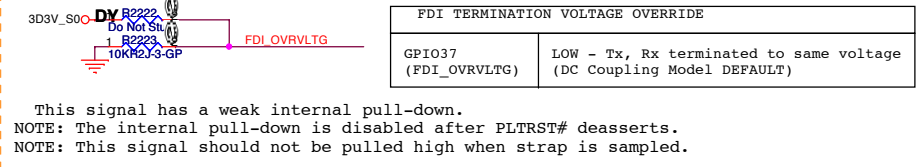
[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G



DVT 20101029
This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".

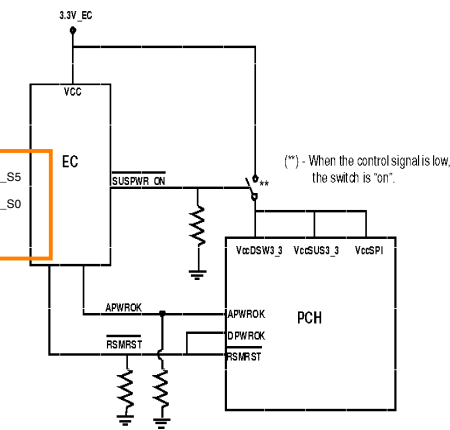
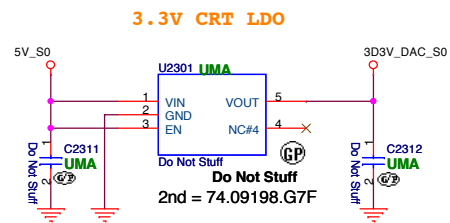
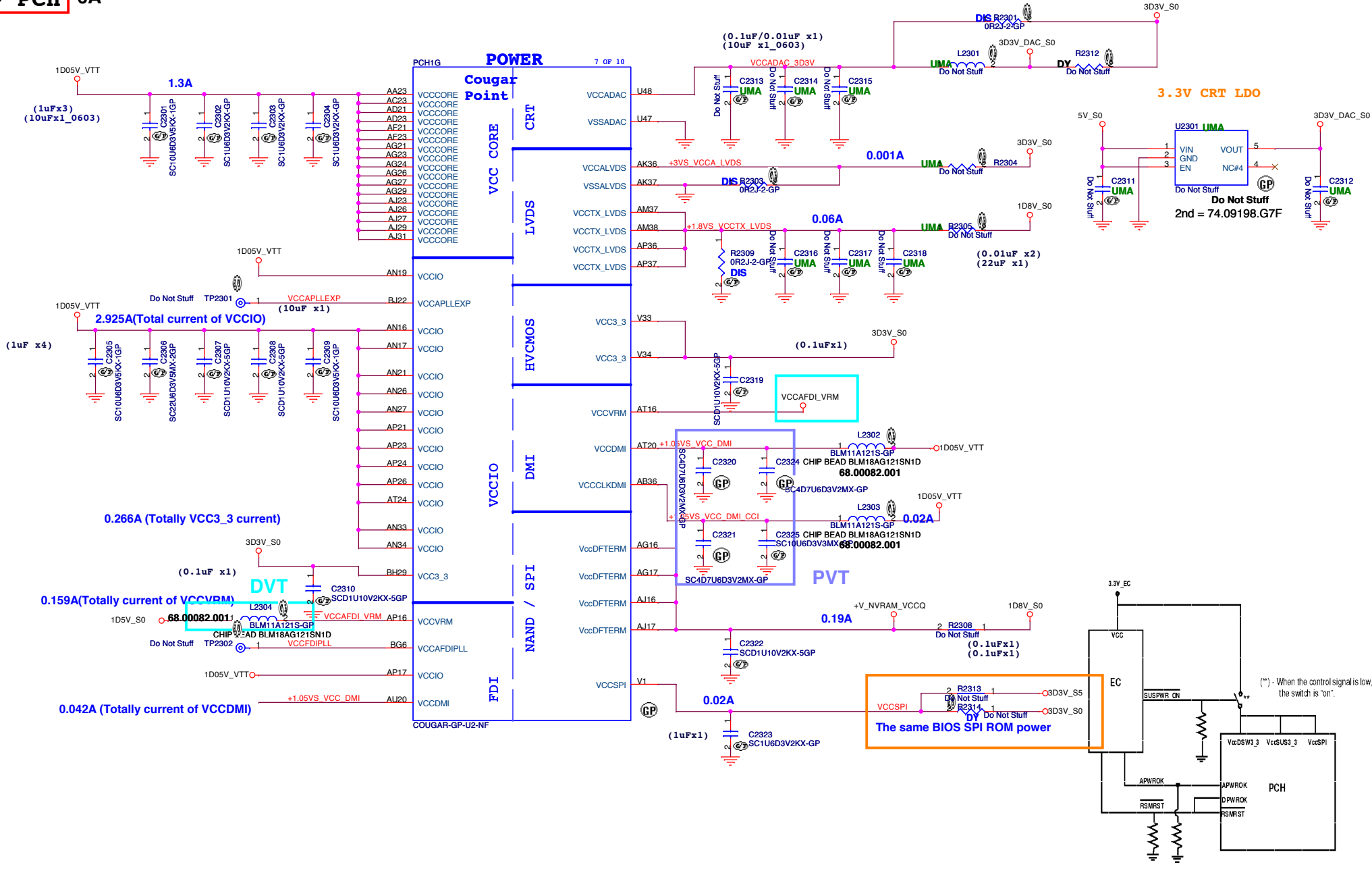
TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

Core power : 3D3V_S0
Core power : 3D3V_S0

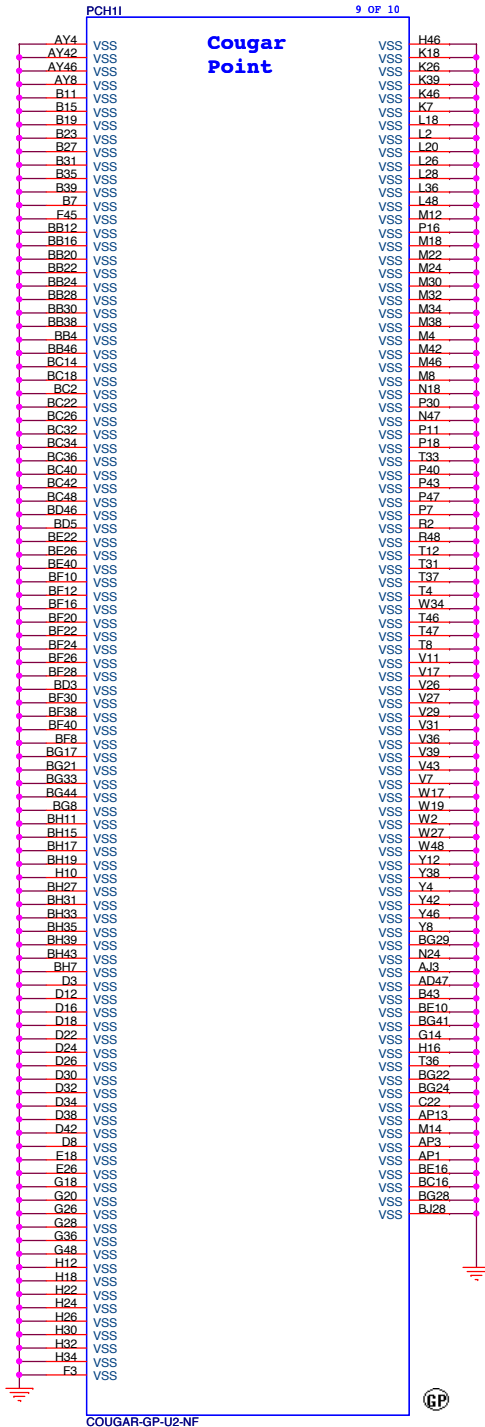
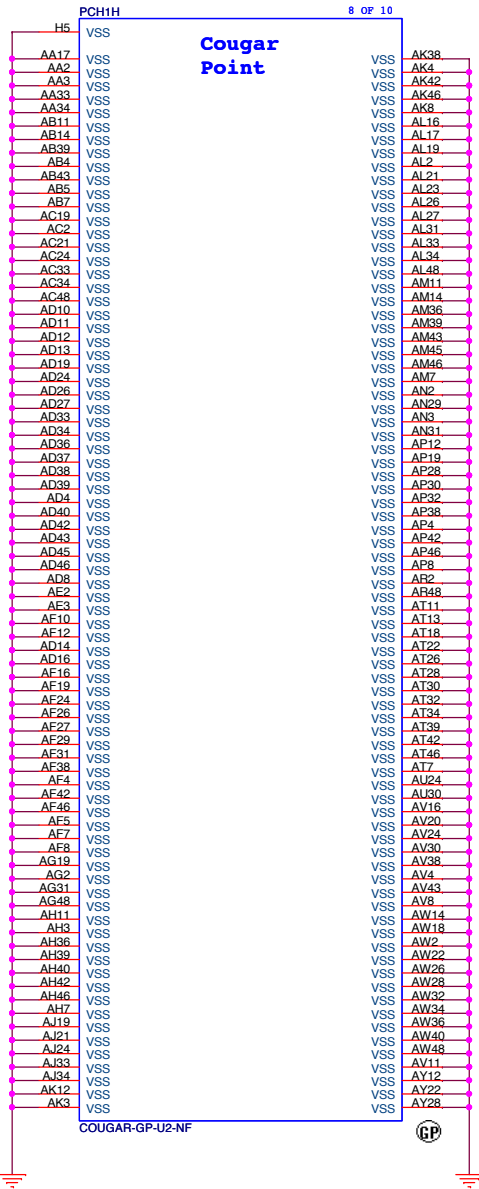


FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.



SSID = PCH



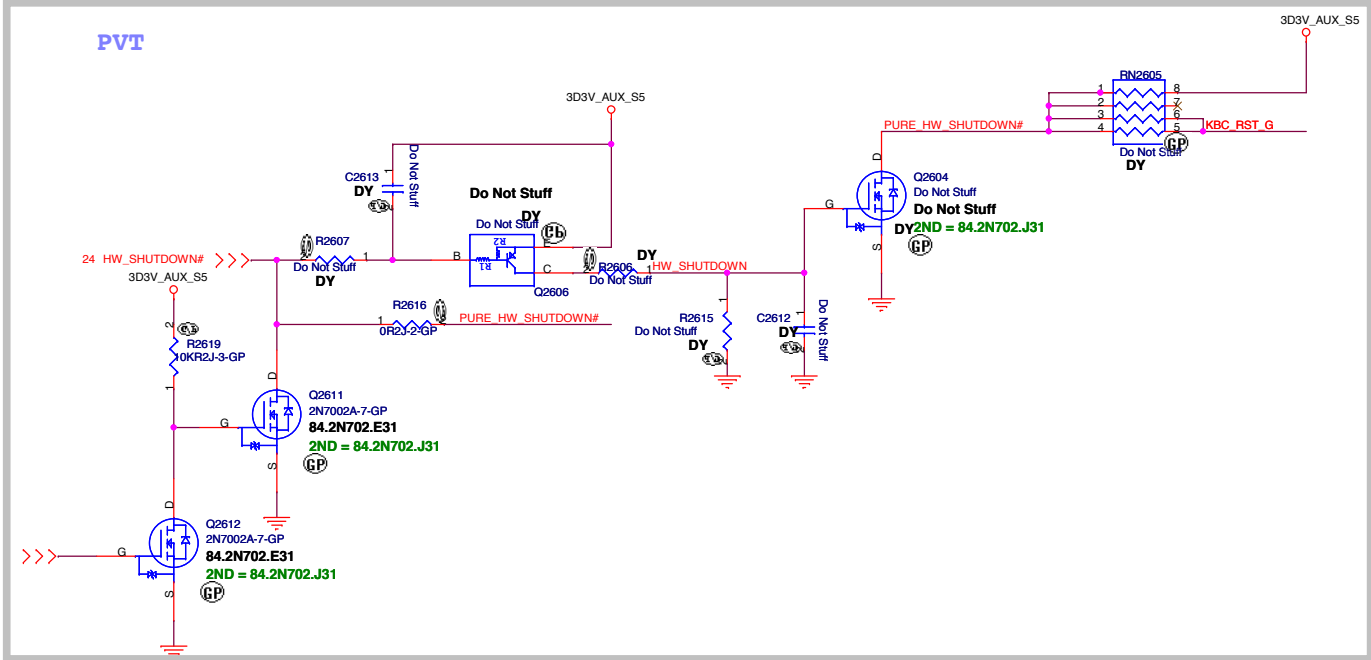
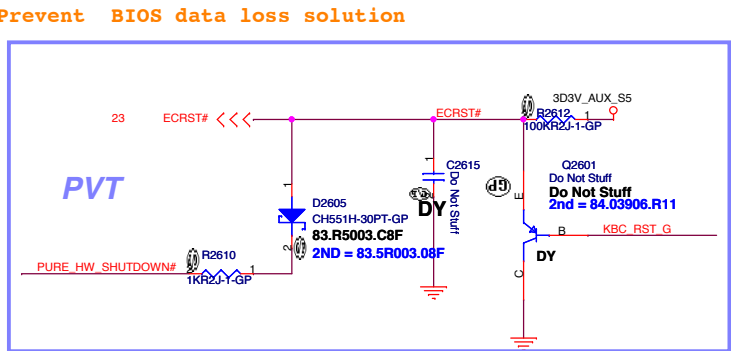
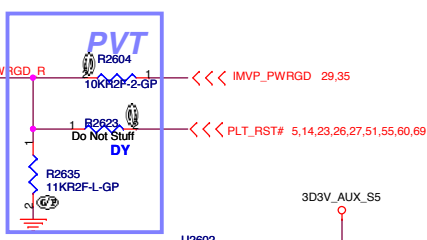
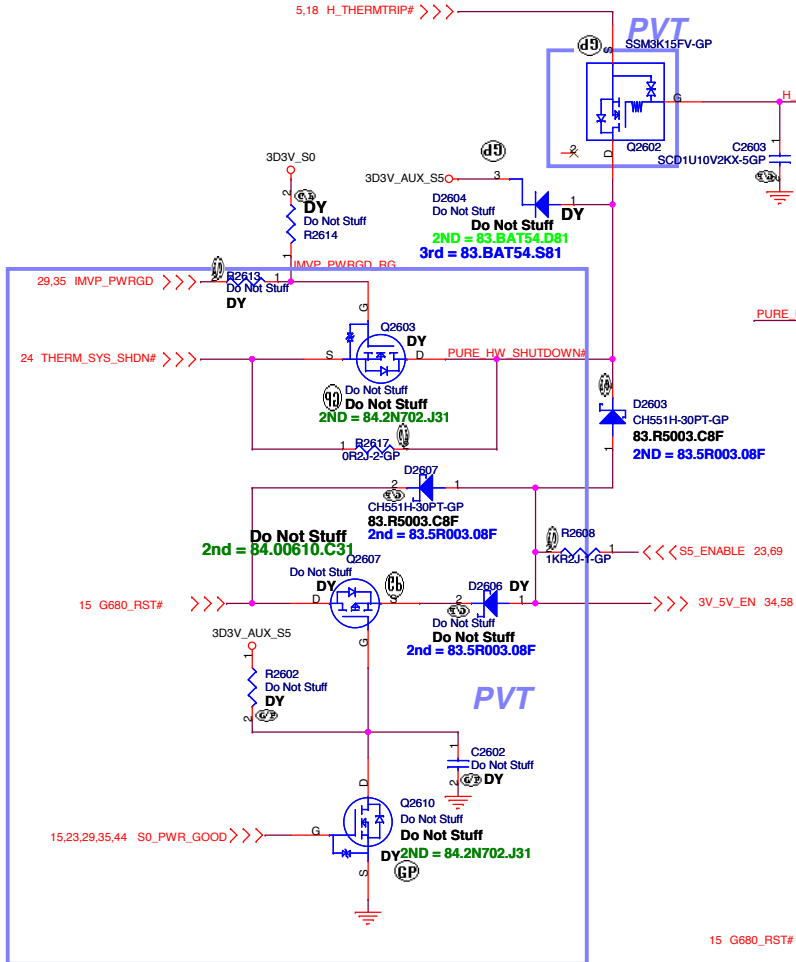
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Title: **PCH (VSS)**

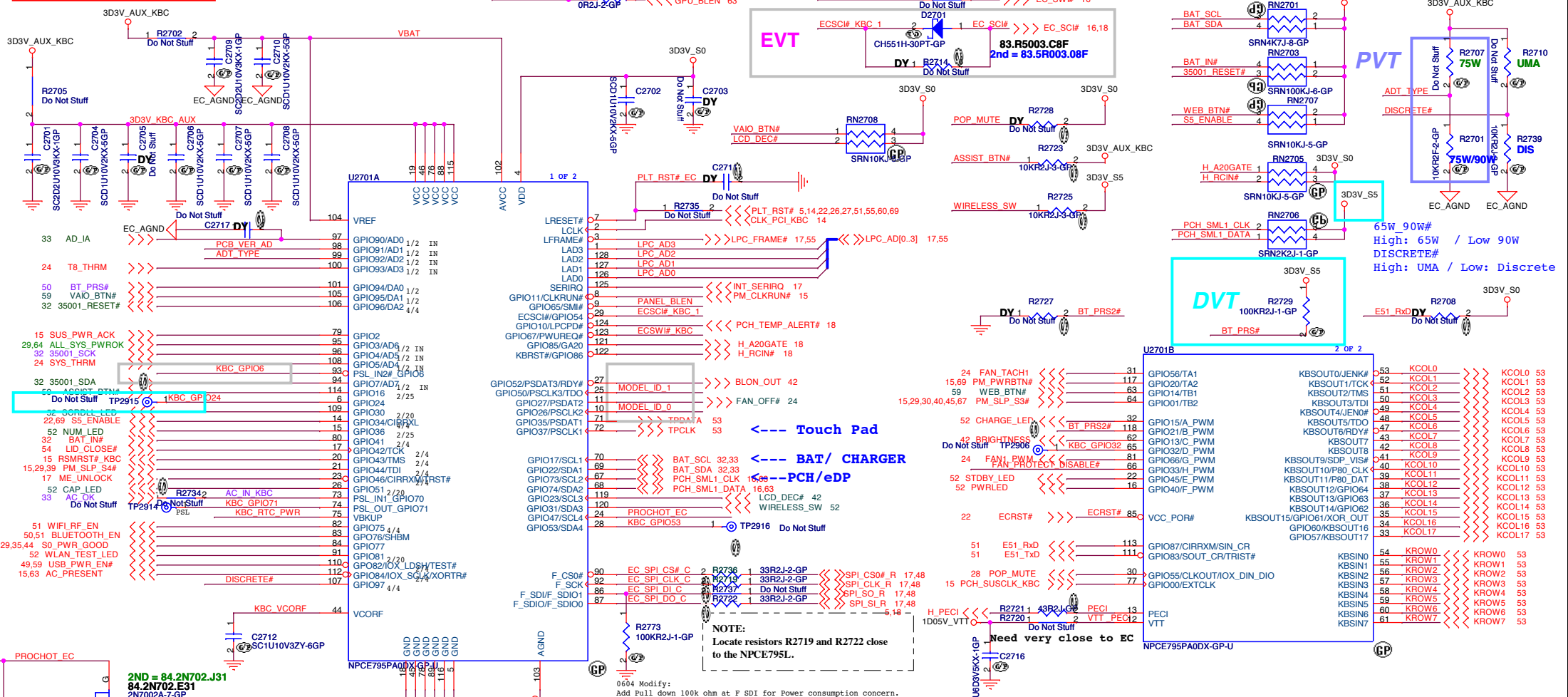
Size A3	Document Number	Rev
Date: Wednesday, March 02, 2011	Z50-HR { Huron River Platform }	-1
	Sheet 21 of 74	



N12M GS2 HYN1GB

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KBC Reset			
Title			
Size	Document Number		Rev
Custom	Z50-HR { Huron River Platform}		-1
Date	Wednesday, March 02, 2011	Sheet 22	of 74

SSID = KBC



Touch Pad

BAT/ CHARGER

PCH/eDP

NOTE:
Locate resistors R2719 and R2722 close to the NPCE795L.

EC GPIO standard PH/PL

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

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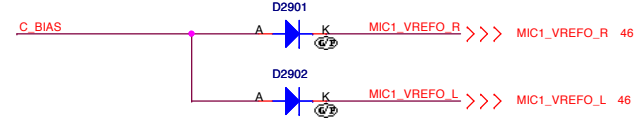
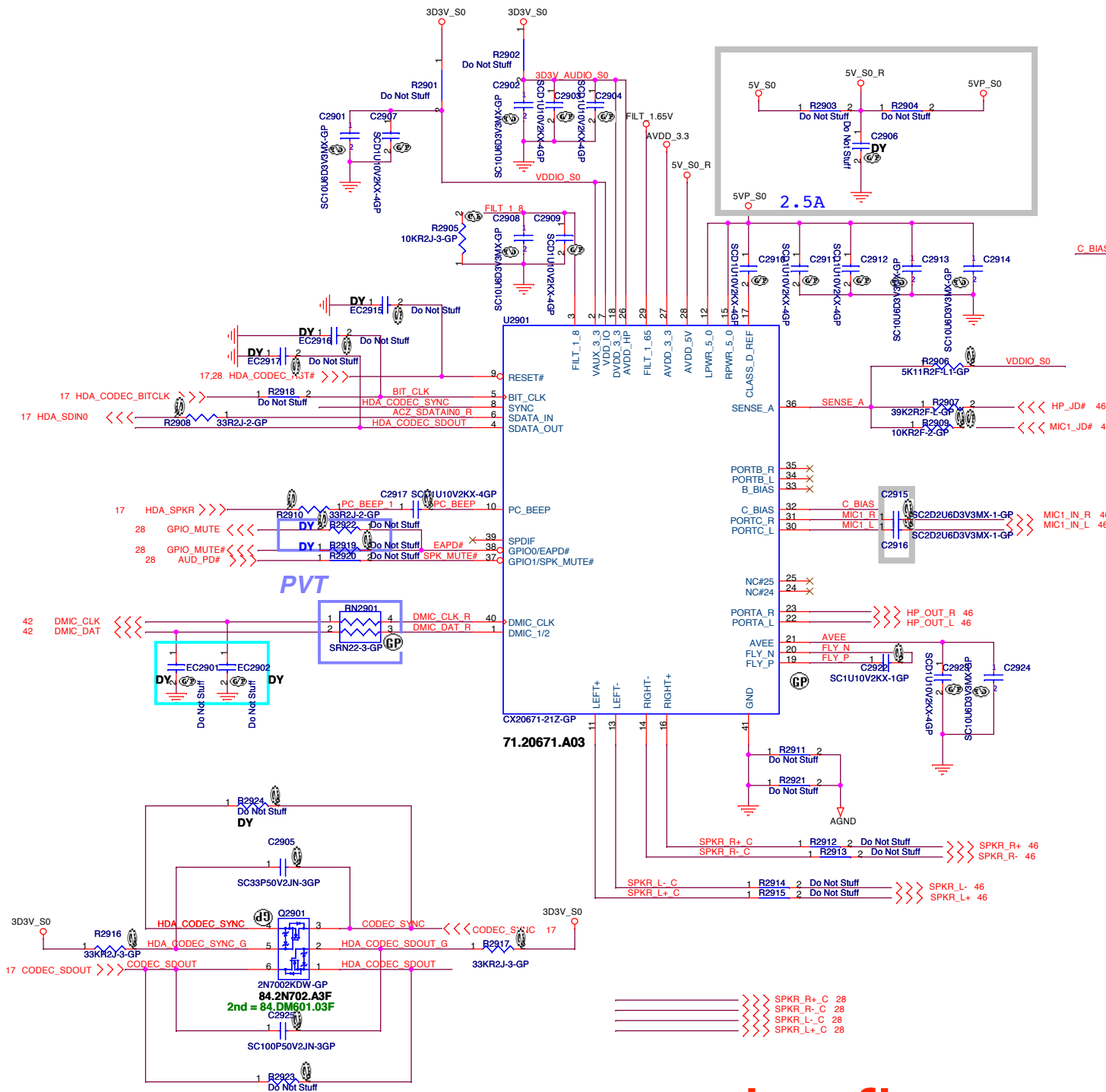
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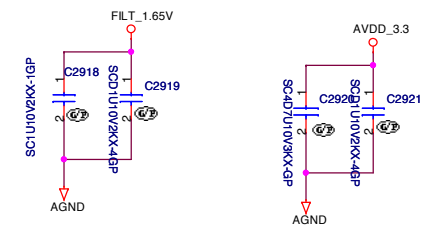
Title: **KBC Nuvoton NPCE795**

Size: A3 Document Number: **Z50-HR (Huron River Platform)** Rev: -1

Date: Thursday, March 03, 2011 Sheet: 23 of 74



RB751V-40-2-GP
 83.R2004.B8F
 2ND = 83.R0304.LD8F
 3RD = 83.R2004.C8F



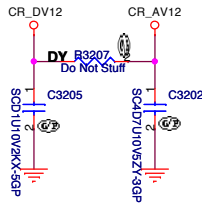
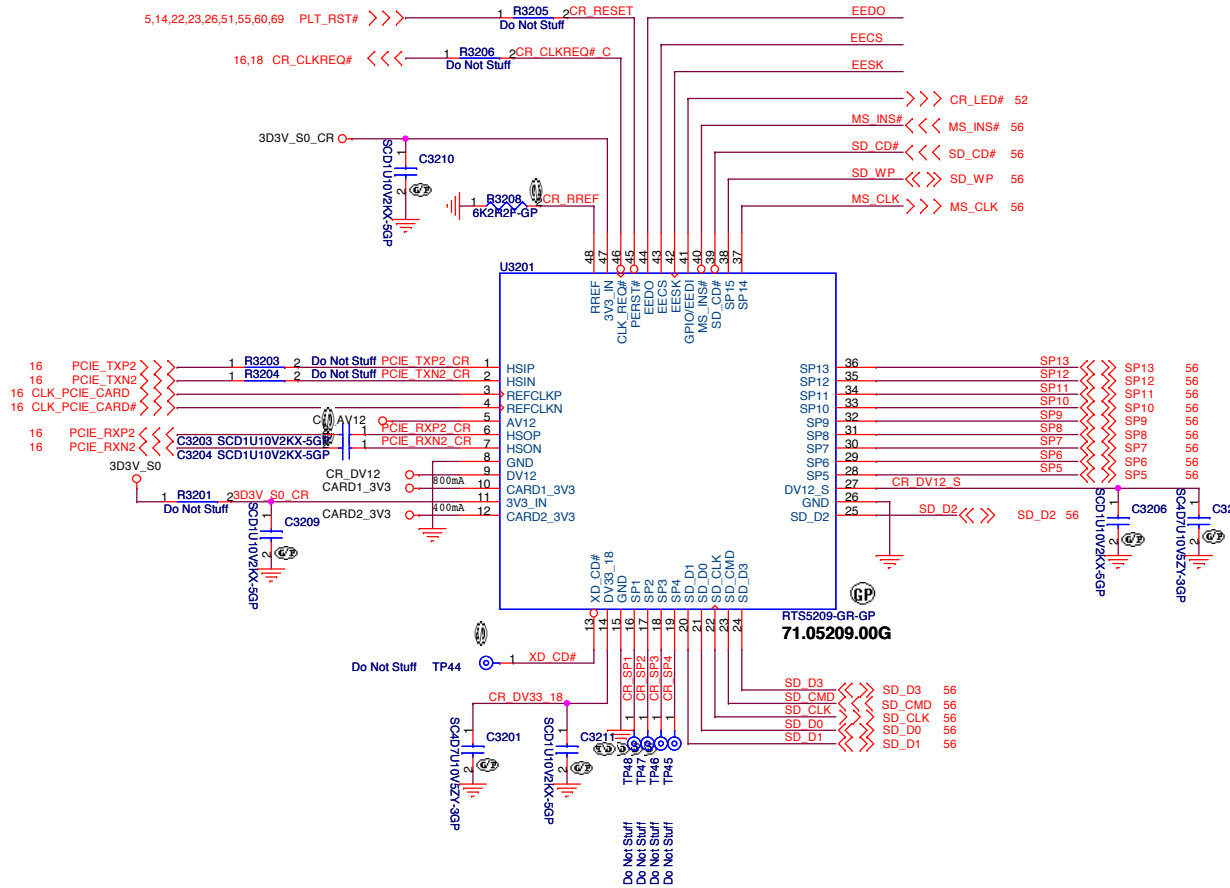
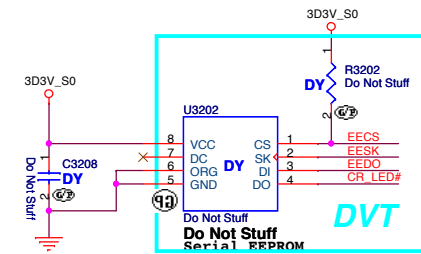
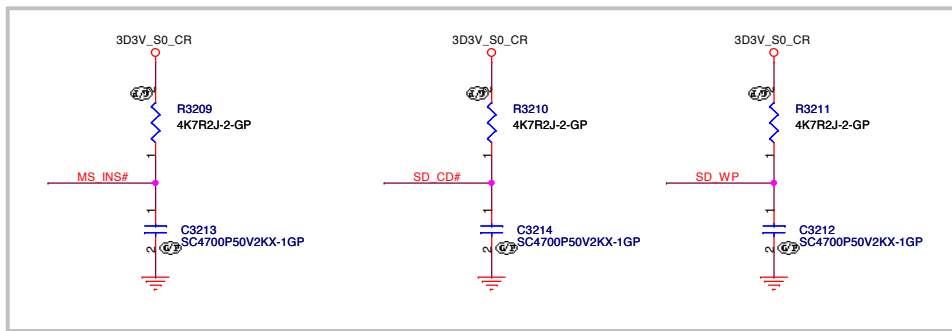
- ===== SPKR_R+_C 28
- ===== SPKR_R-_C 28
- ===== SPKR_L+_C 28
- ===== SPKR_L-_C 28

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Title: **Audio Codec**

Size A3	Document Number: Z50-HR { Huron River Platform}	Rev: -1
Date: Wednesday, March 02, 2011	Sheet 25 of 74	



N12M GS2 HYN1GB

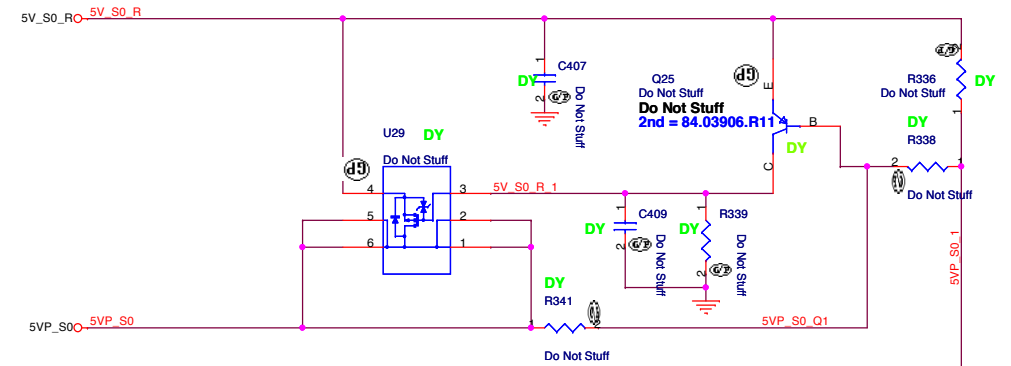
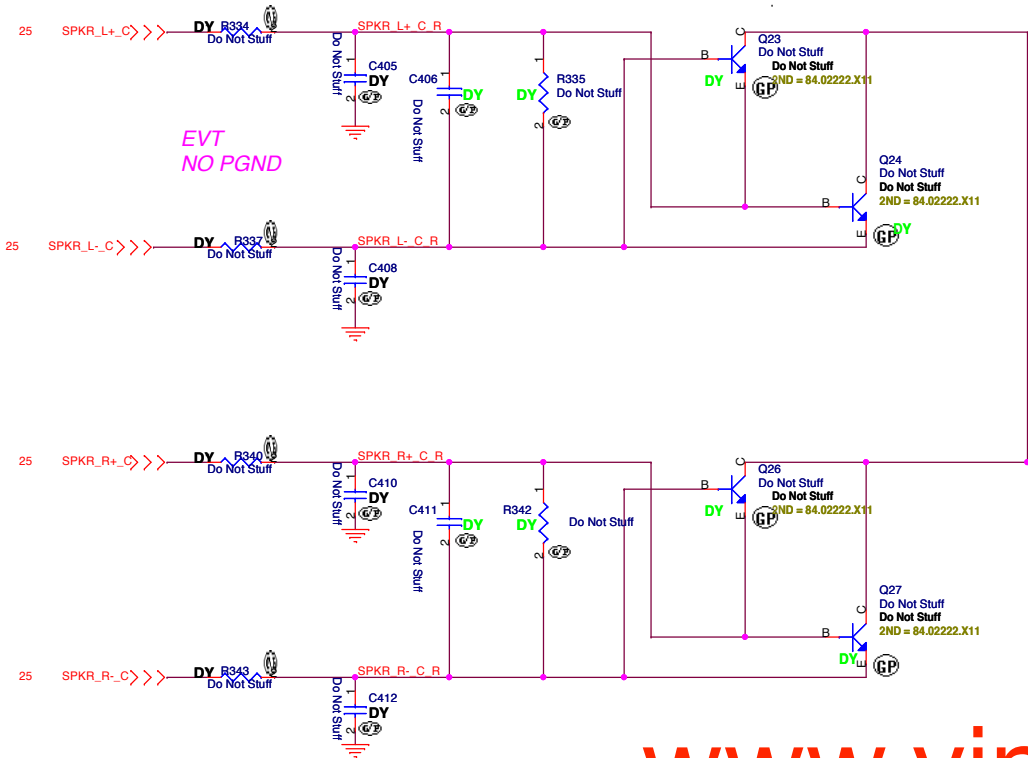
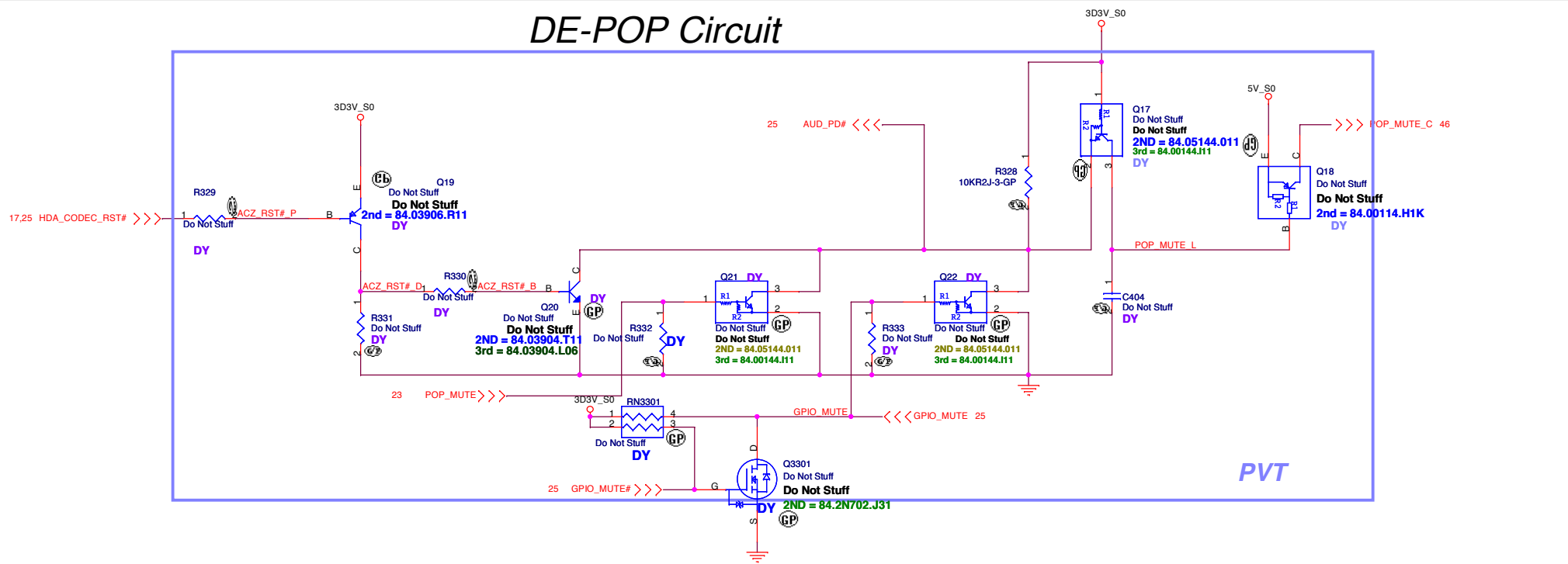
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTS5209 (CARD READER)**

Size A3 Document Number: **750-HR { Huron River Platform }** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 27 of 74

DE-POP Circuit



N12M GS2 HYN1GB

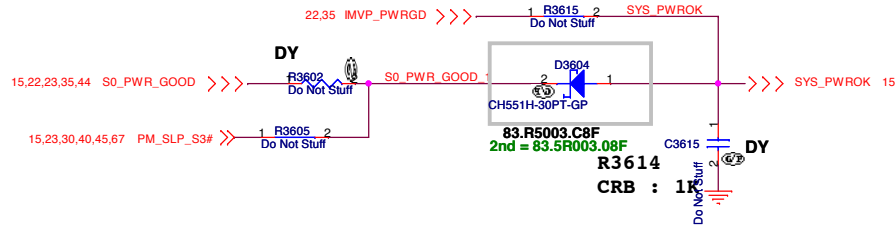
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			Audio DE-POP Circuit		
Size	Document Number		Rev		-1
Z50-HR {Huron River Platform}					
Date:	Wednesday, March 02, 2011	Sheet	28	of	74

Power Sequence

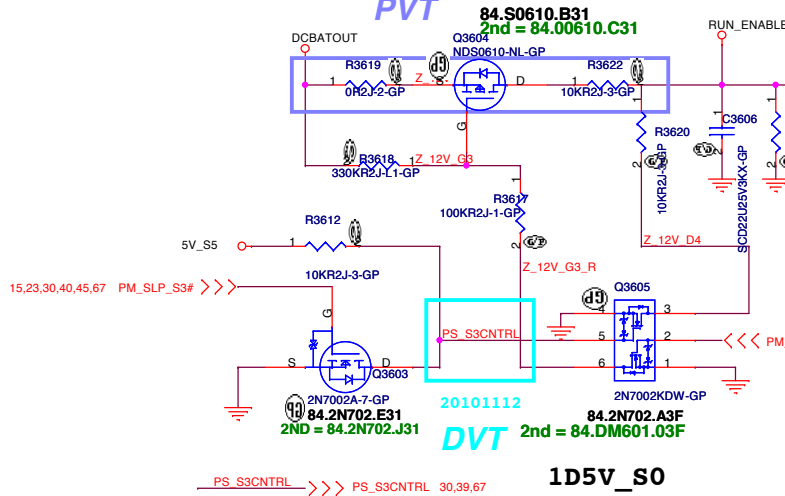
EVT
DEL U3608

1 R3604 2 >>> ALL_SYS_PWROK 23.64
Do Not Stuff <<< PWR_VCCSA_PWRGD 15.35.41



Run Power

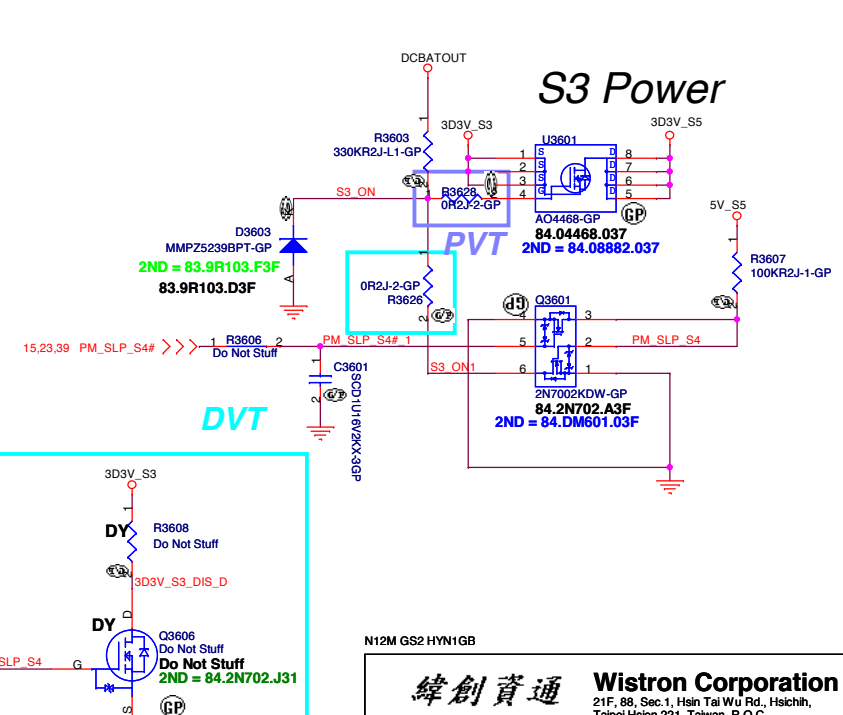
PVT



1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total = 11.39A

S3 Power

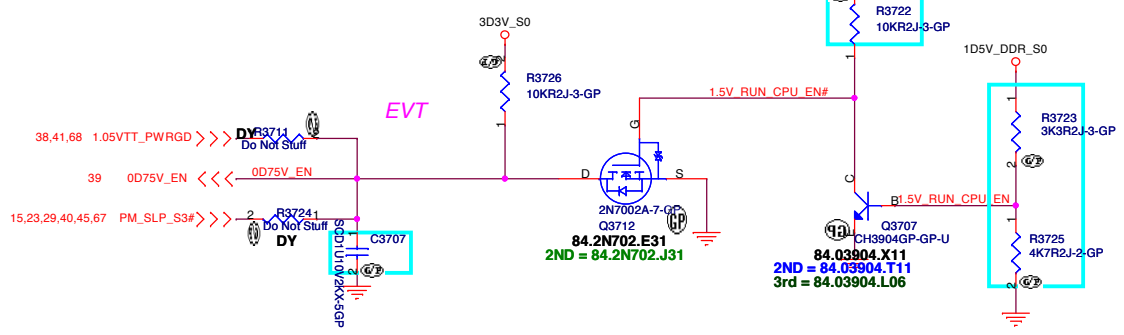
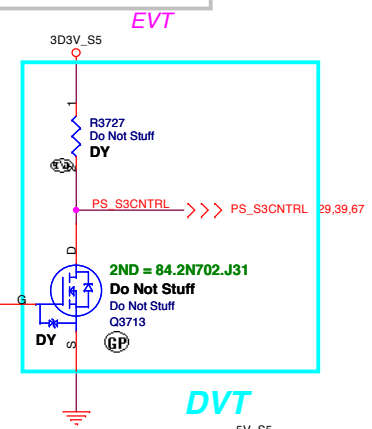
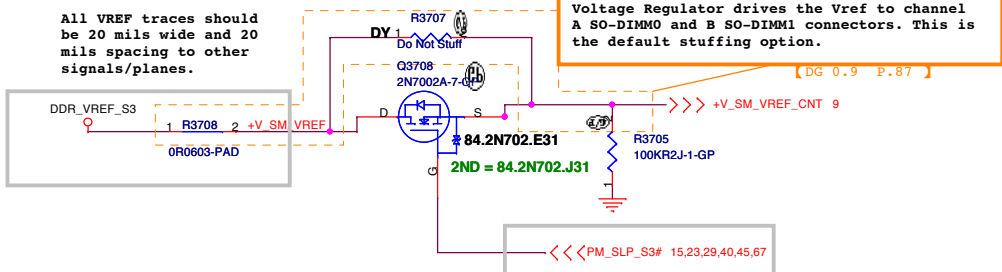


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Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

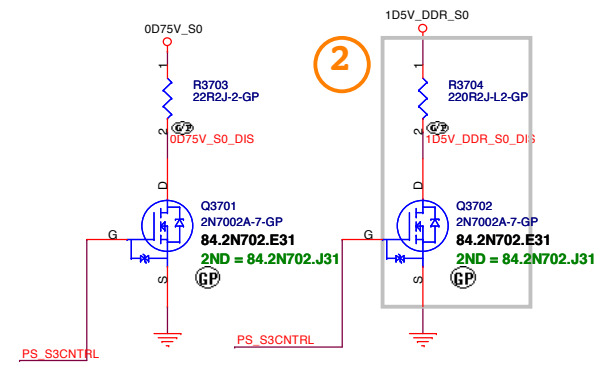
All VREF traces should be 20 mils wide and 20 mils spacing to other signals/planes.

M1 :Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref to channel A SO-DIMM and B SO-DIMM1 connectors. This is the default stuffing option.

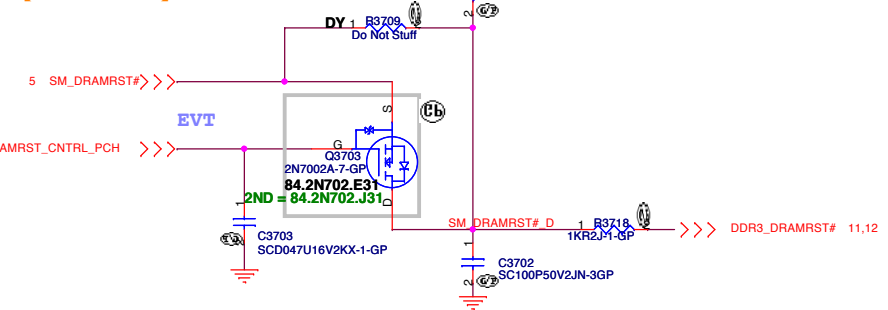


S3 Power Reduction Circuit

Close to DIMM
 S3 Power Reduction Circuit RamPower discharge

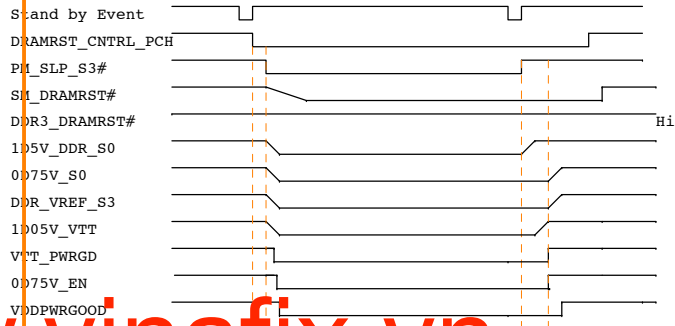
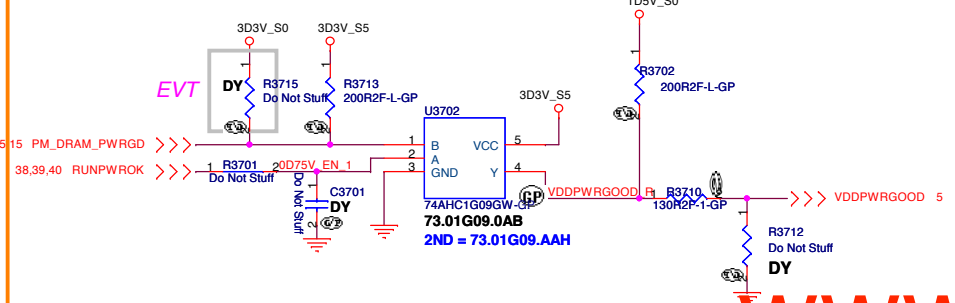


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

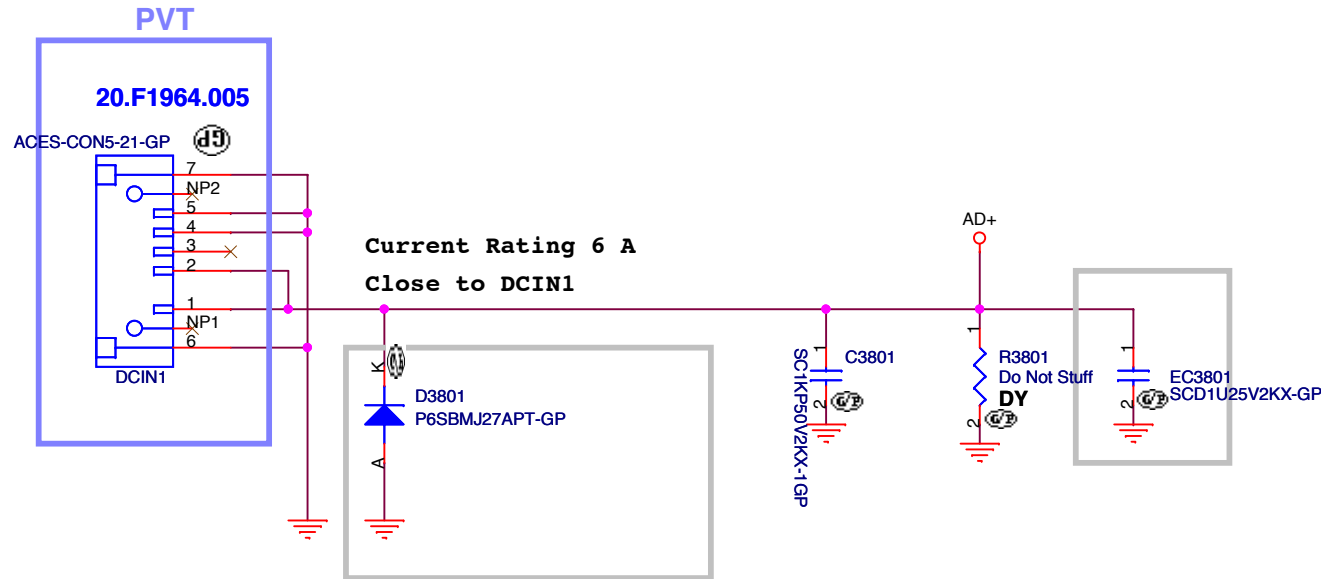


Signal Routing Guideline:
 1. Maximal trace length from R_iso to any DRAM (on the S0 DIMM) is 6".
 2. FET's Ron must be lower than 6 Ohms and pad capacitance lower than 30pF.

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Adaptor in to generate DCBATOUT



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Title

DCIN JACK

Size

Document Number

A4

Z50-HR { Huron River Platform}

Rev

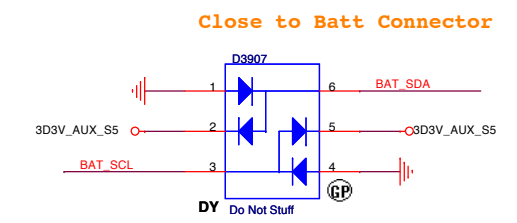
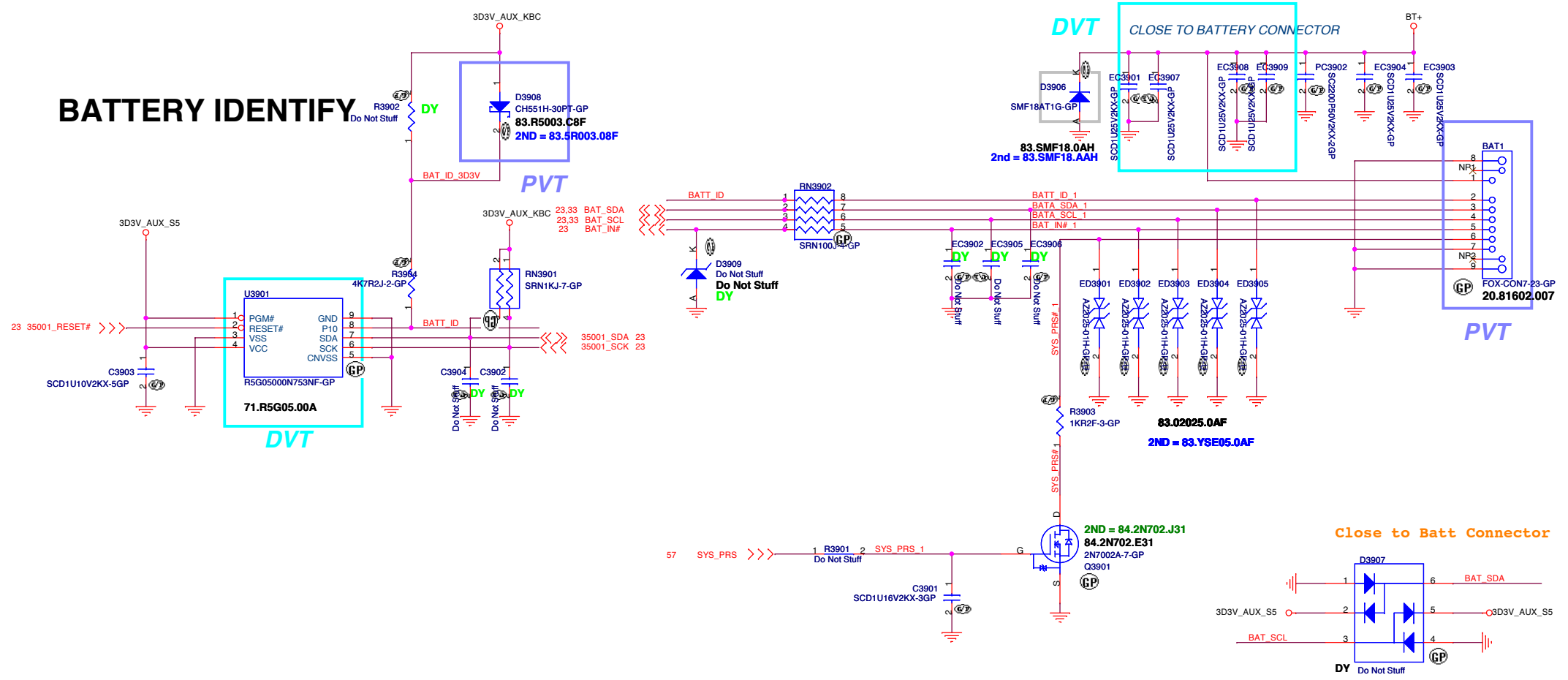
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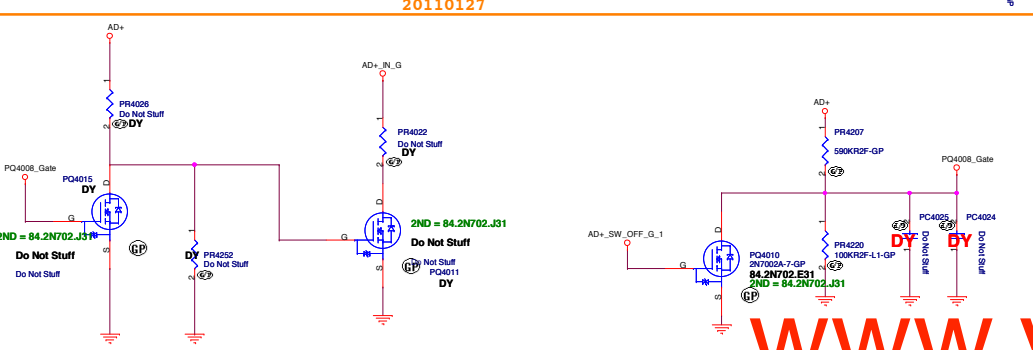
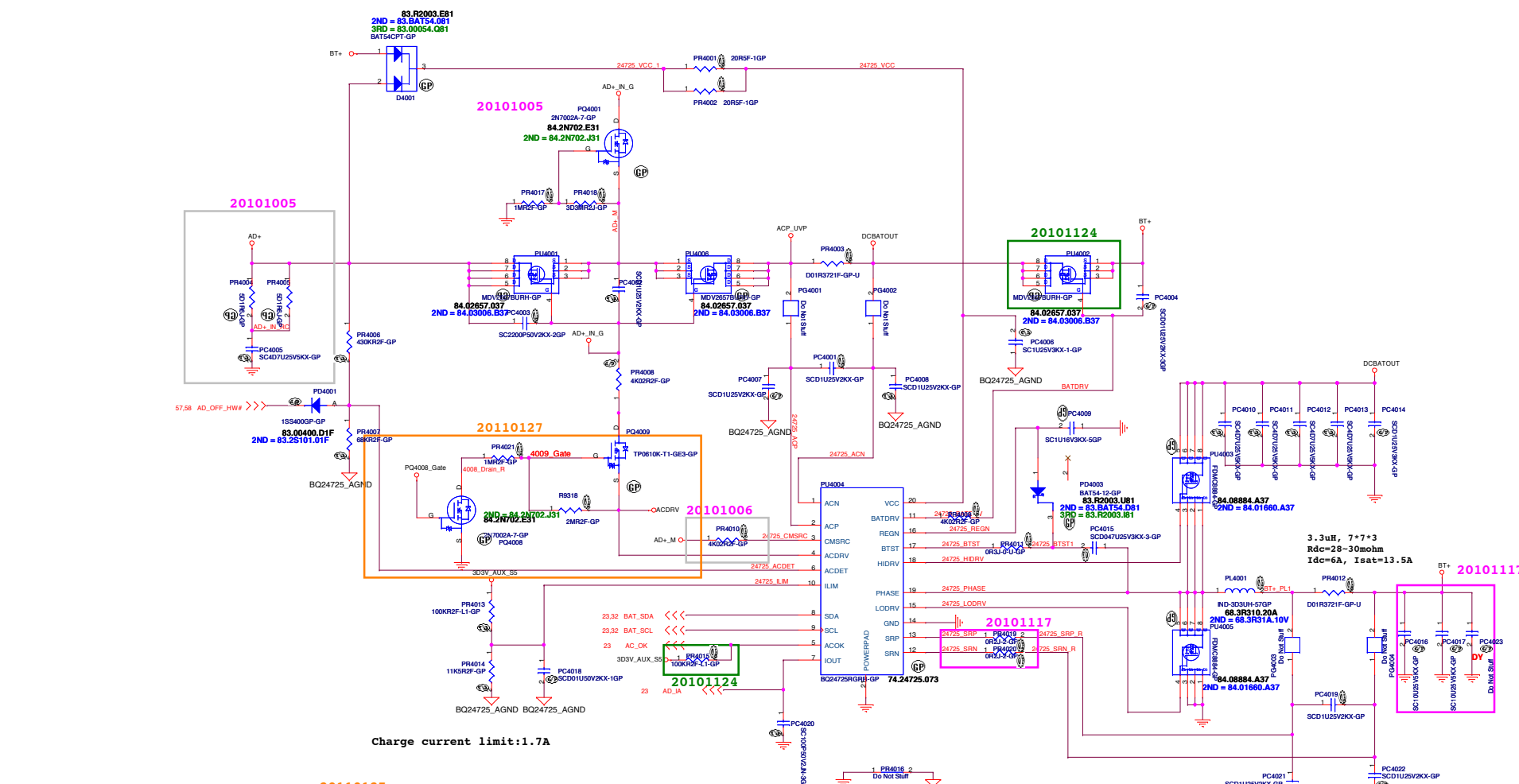
Date: Wednesday, March 02, 2011

Sheet 31 of 74

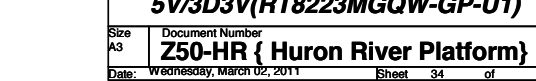
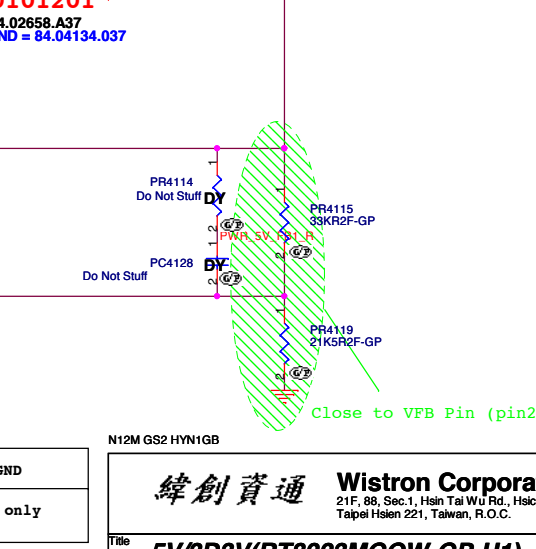
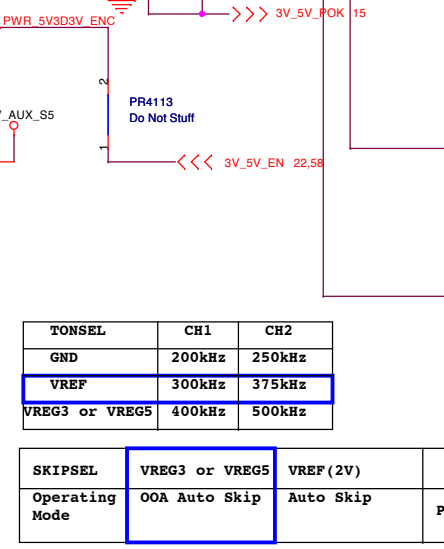
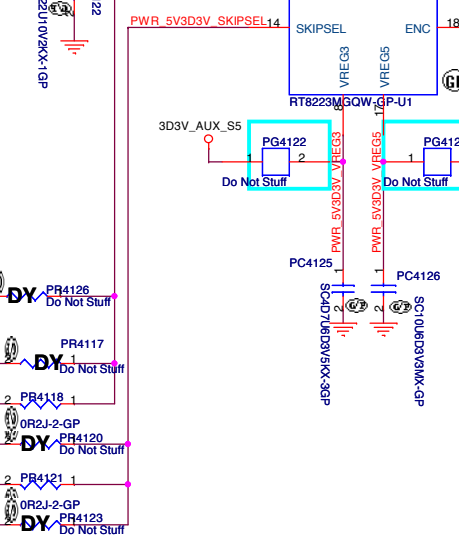
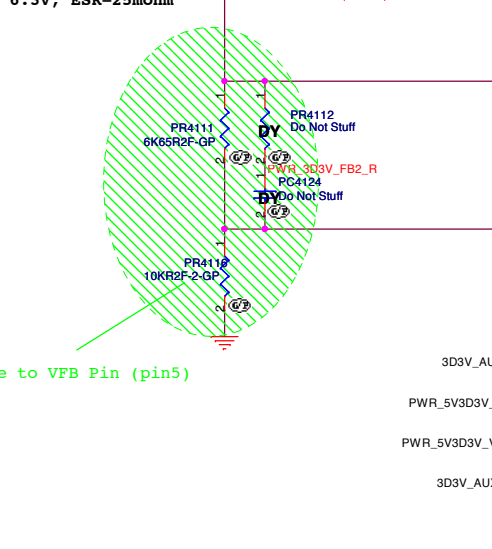
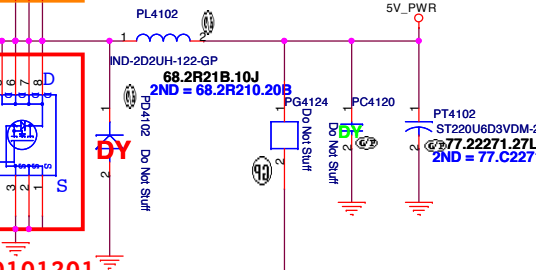
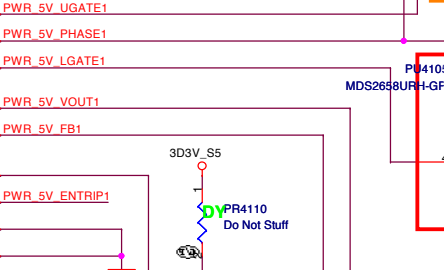
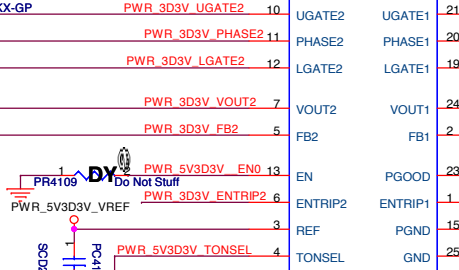
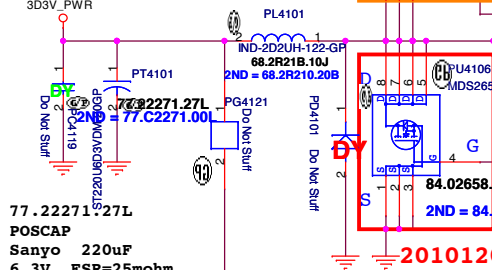
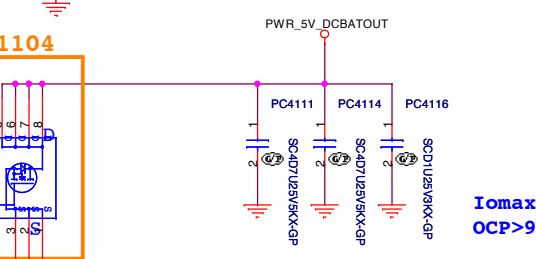
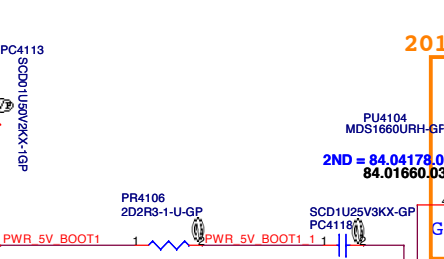
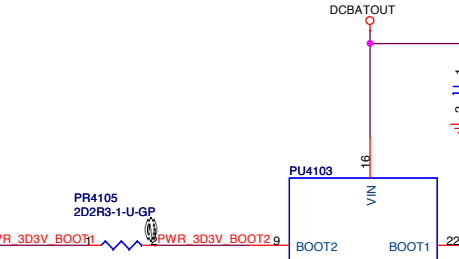
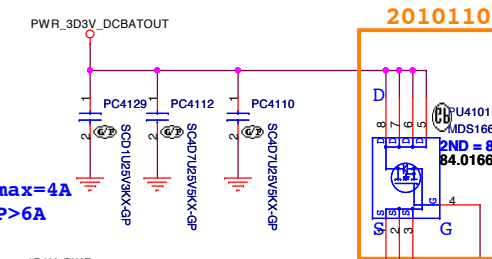
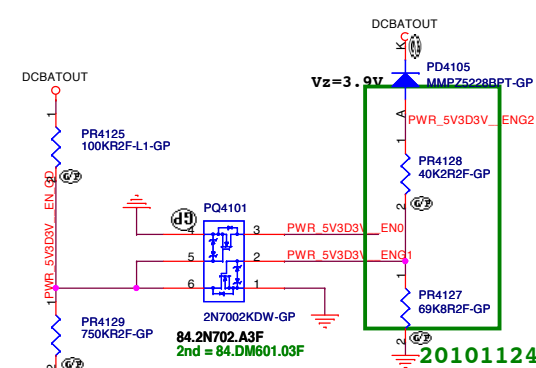
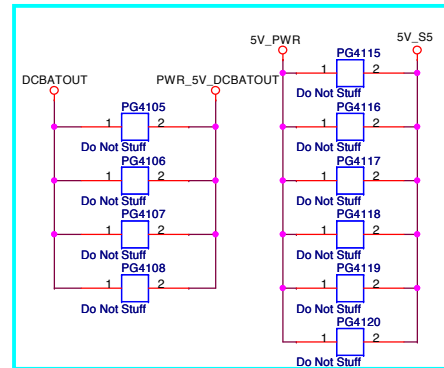
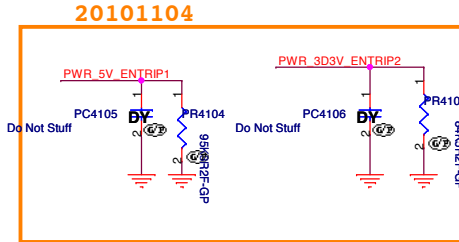
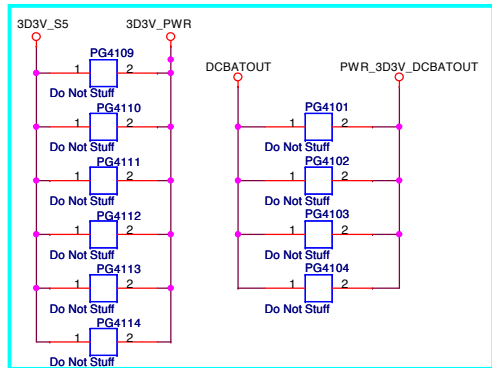
www.vinafix.vn

BATTERY IDENTIFY





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Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

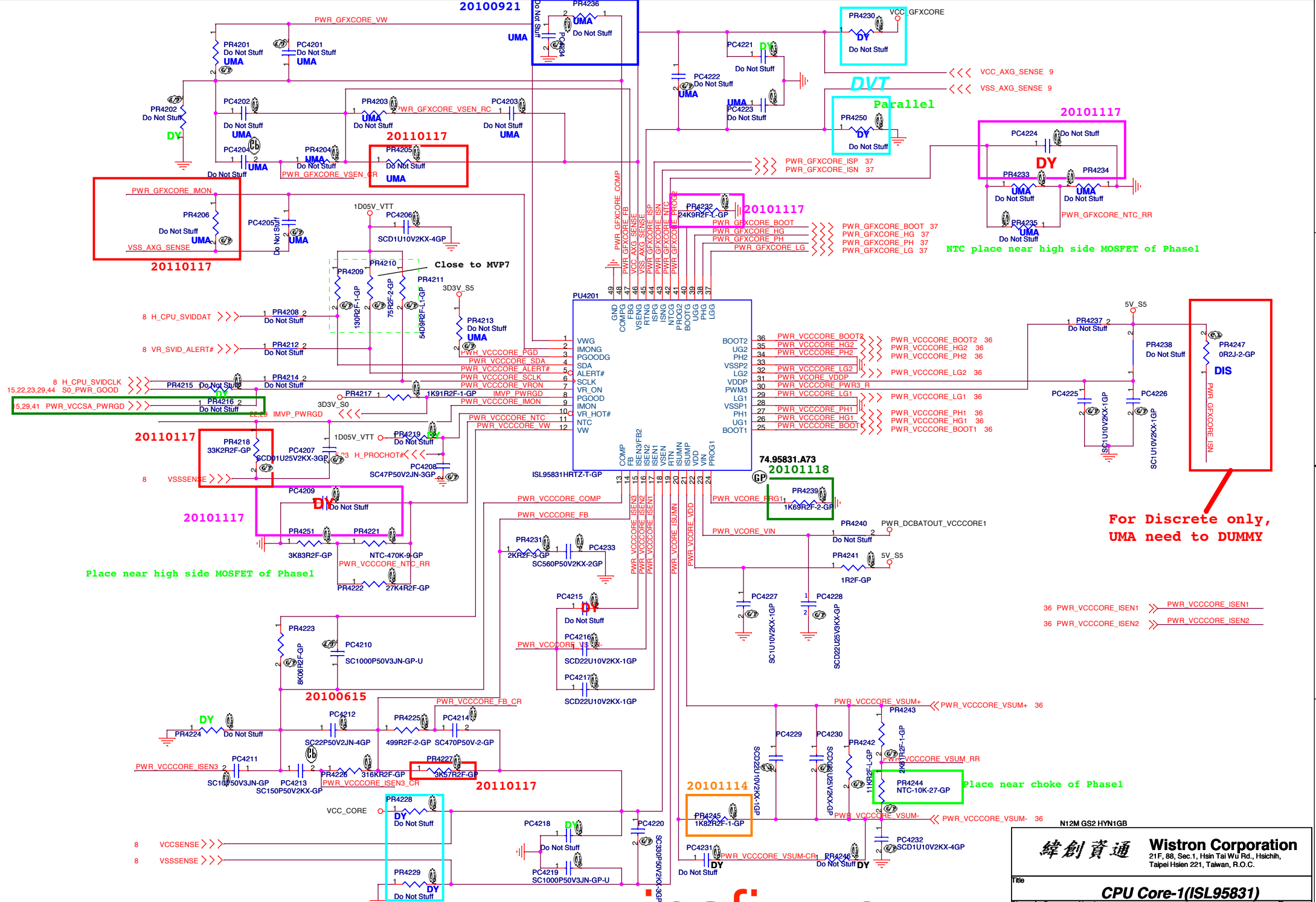
N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.

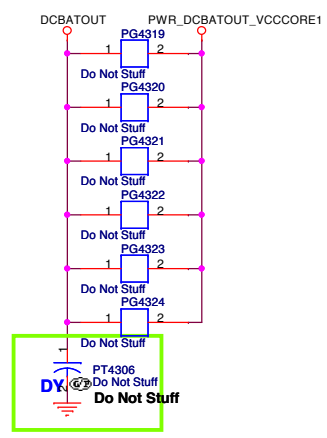
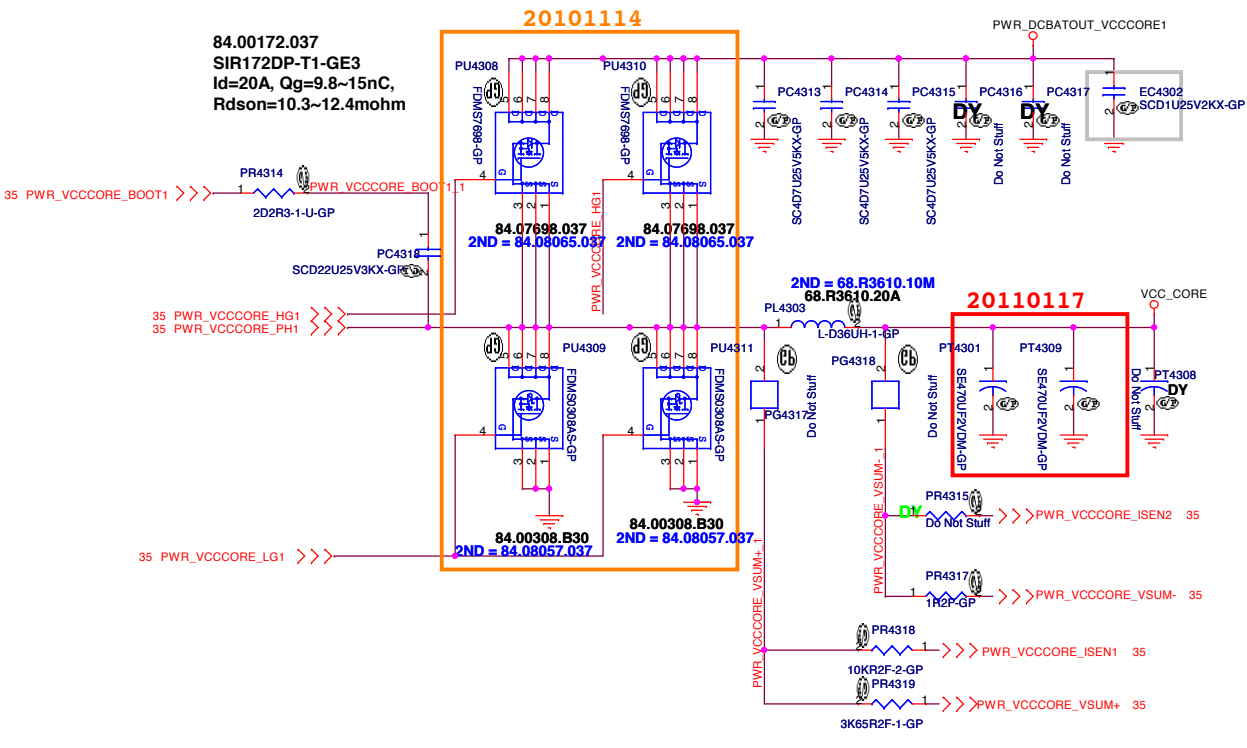
Title: **5V/3D3V(RT8223MGQW-GP-U1)**

Size A3 Document Number **Z50-HR {Huron River Platform}** Rev -1

Date: Wednesday, March 02, 2011 Sheet 34 of 74

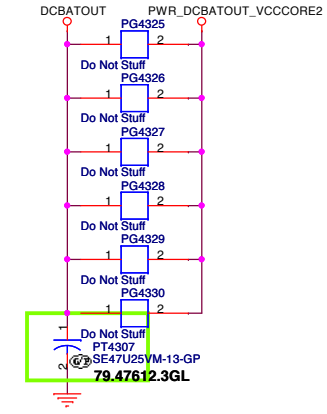
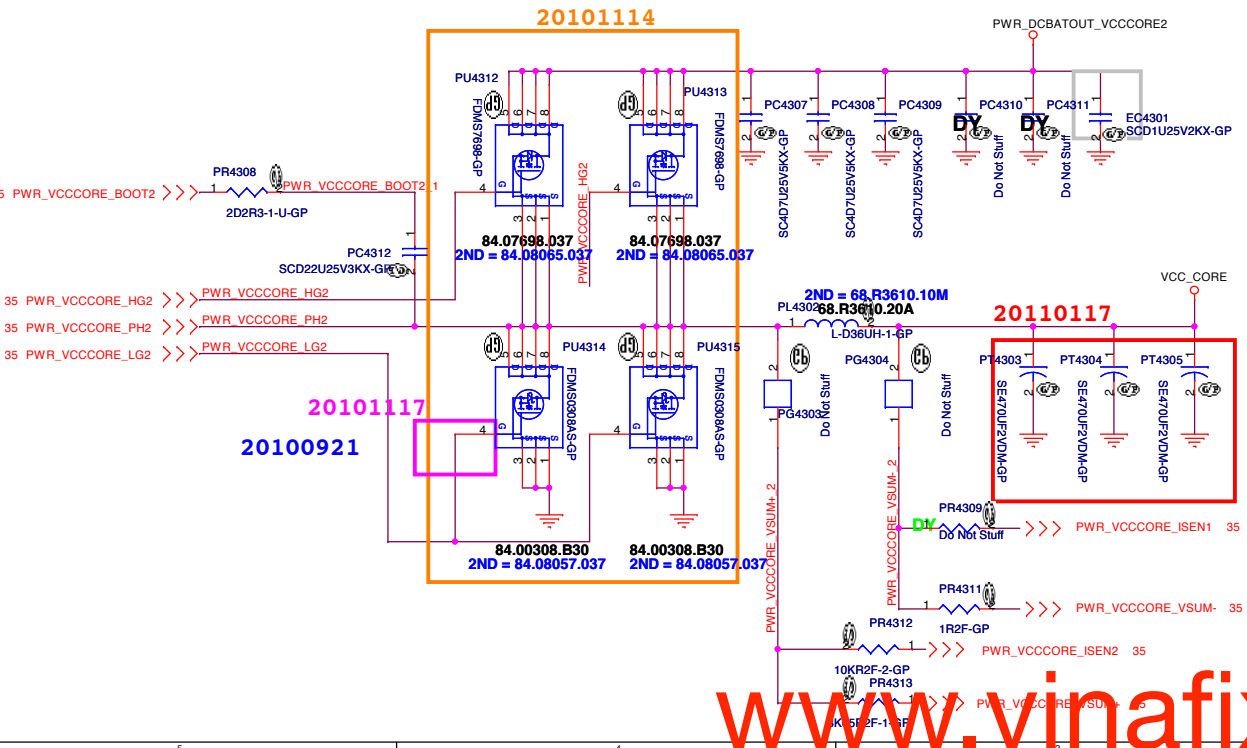


84.00172.037
SIR172DP-T1-GE3
Id=20A, Qg=9.8~15nC,
Rdson=10.3~12.4mohm



79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA

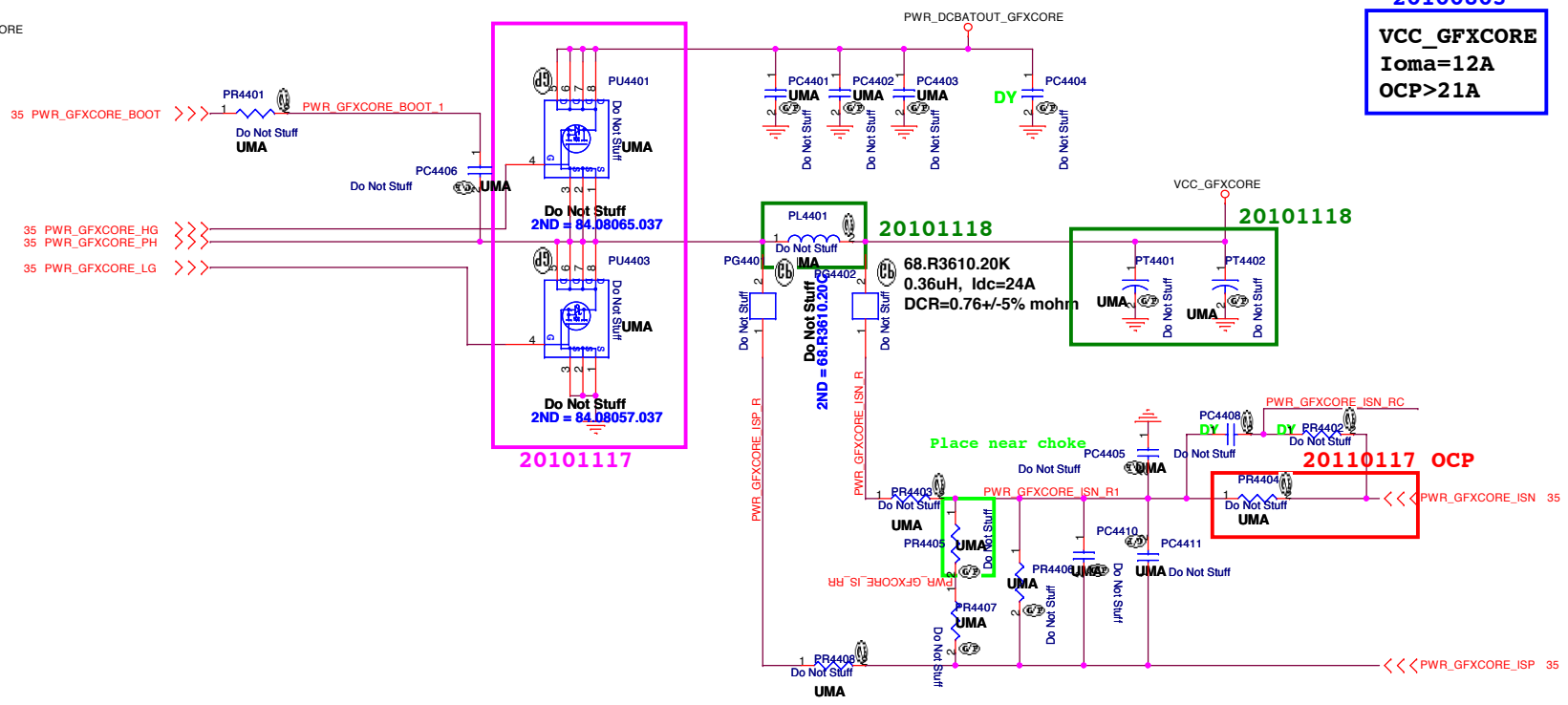
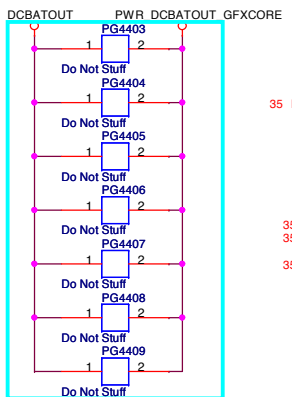
Vcc_core
Iomax=53A
OCP>80A



79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA

N12M GS2 HYN1GB

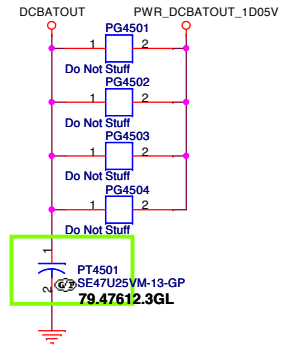
緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
CPU Core-2(ISL9581)		
Title		
Size A3	Document Number	Rev
Date: Wednesday, March 02, 2011	Z50-HR (Huron River Platform)	-1
	Sheet 36 of 74	



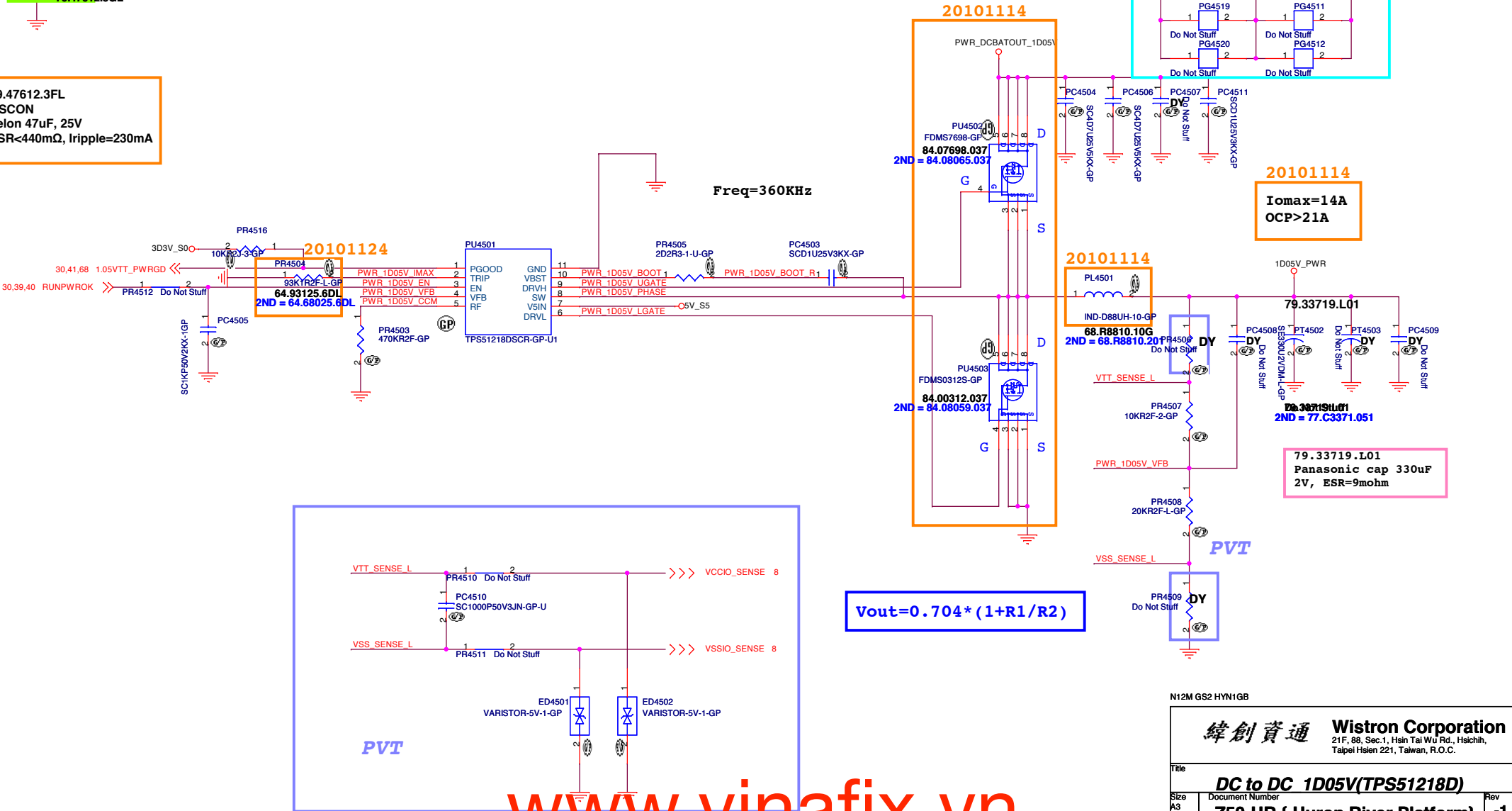
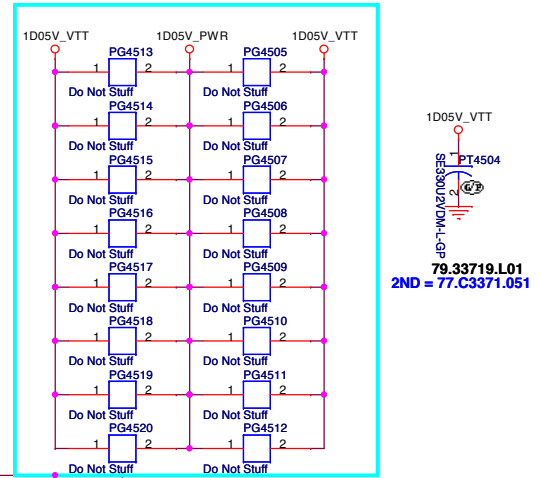
www.vinafix.vn

N12M GS2 HYN1GB		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
CPU Core-3 (ISL95831)		
Title	Document Number	Rev
	Z50-HR (Huron River Platform)	-1
Date: Wednesday, March 02, 2011	Sheet 37 of 74	

TPS51218D for 1D05V



79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA



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N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

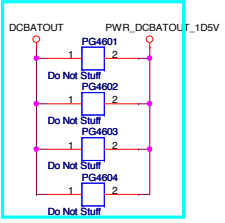
Title DC to DC 1D05V(TPS51218D)

Size Document Number 750-HR { Huron River Platform} -1

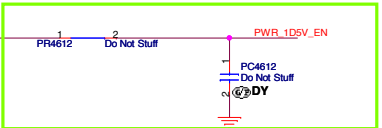
Date: Wednesday, March 02, 2011 Sheet 38 of 74

SSID = PWR.Plane.Regulator_1p5v0p75v

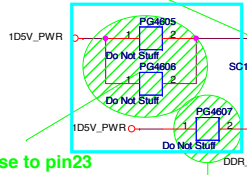
RT8207 for 1D5V and 0D75V



79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR=440mΩ, Irripple=230mA



Close to pin23

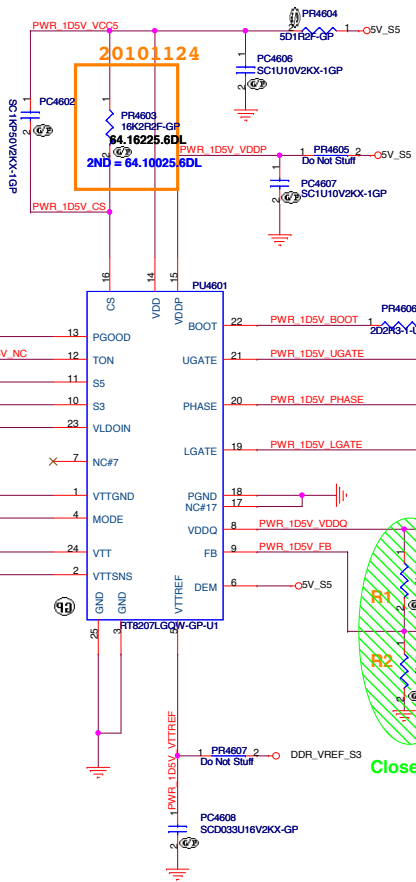
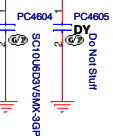
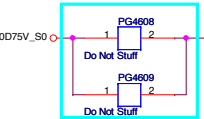


Close to pin23

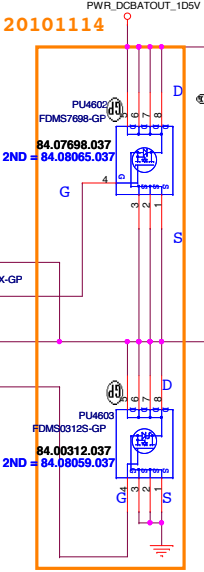
I_omax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

+0.75VS
I_omax: 1.2A

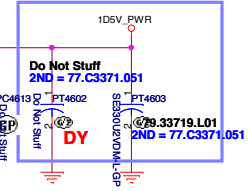


Close to PIN9

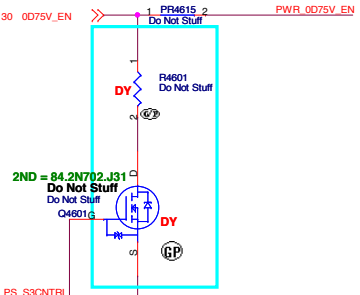


Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
I_dc=18A, Isat=36A

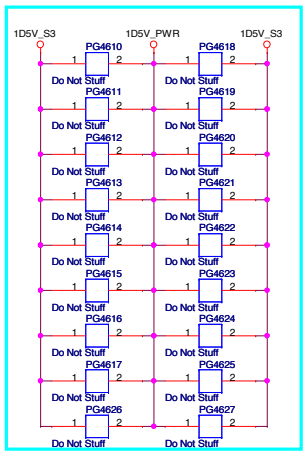
IND-1U4-83-GP
68.1R01B.10J
2ND = 68.1R01A.20A



79.33719.L01
Panasonic cap 330uF
2V, ESR=9mohm



2ND = 84.2N702.J31
Do Not Stuff
Q4601G



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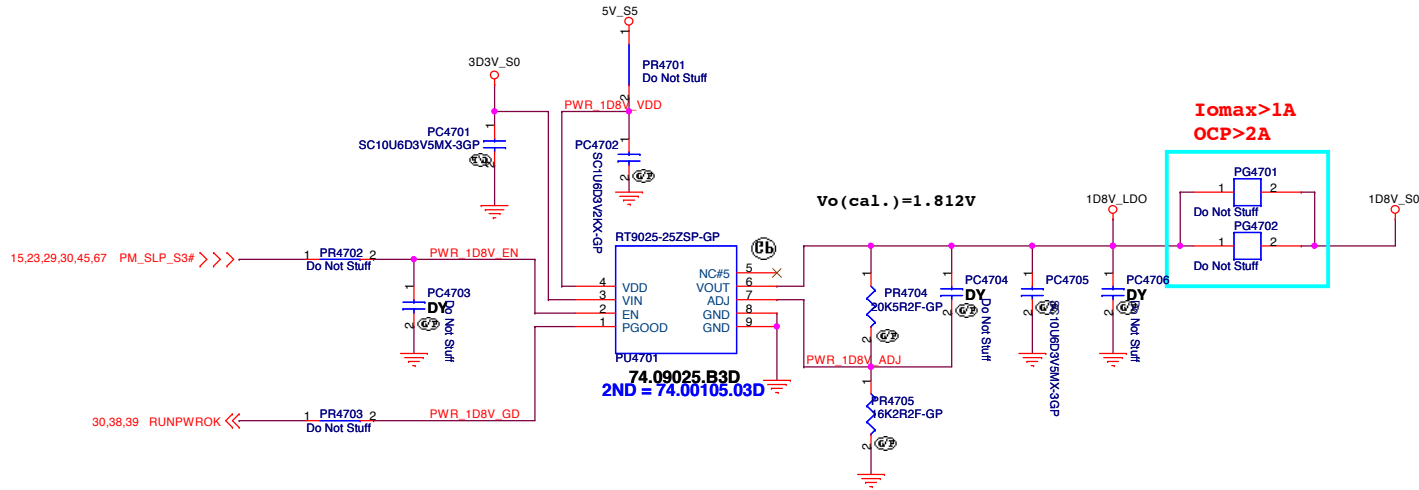
Title: RT8207

Size	Document Number	Rev
Custom	Z50-HR (Huron River Platform)	-1

Date: Wednesday, March 02, 2011 Sheet 39 of 74

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



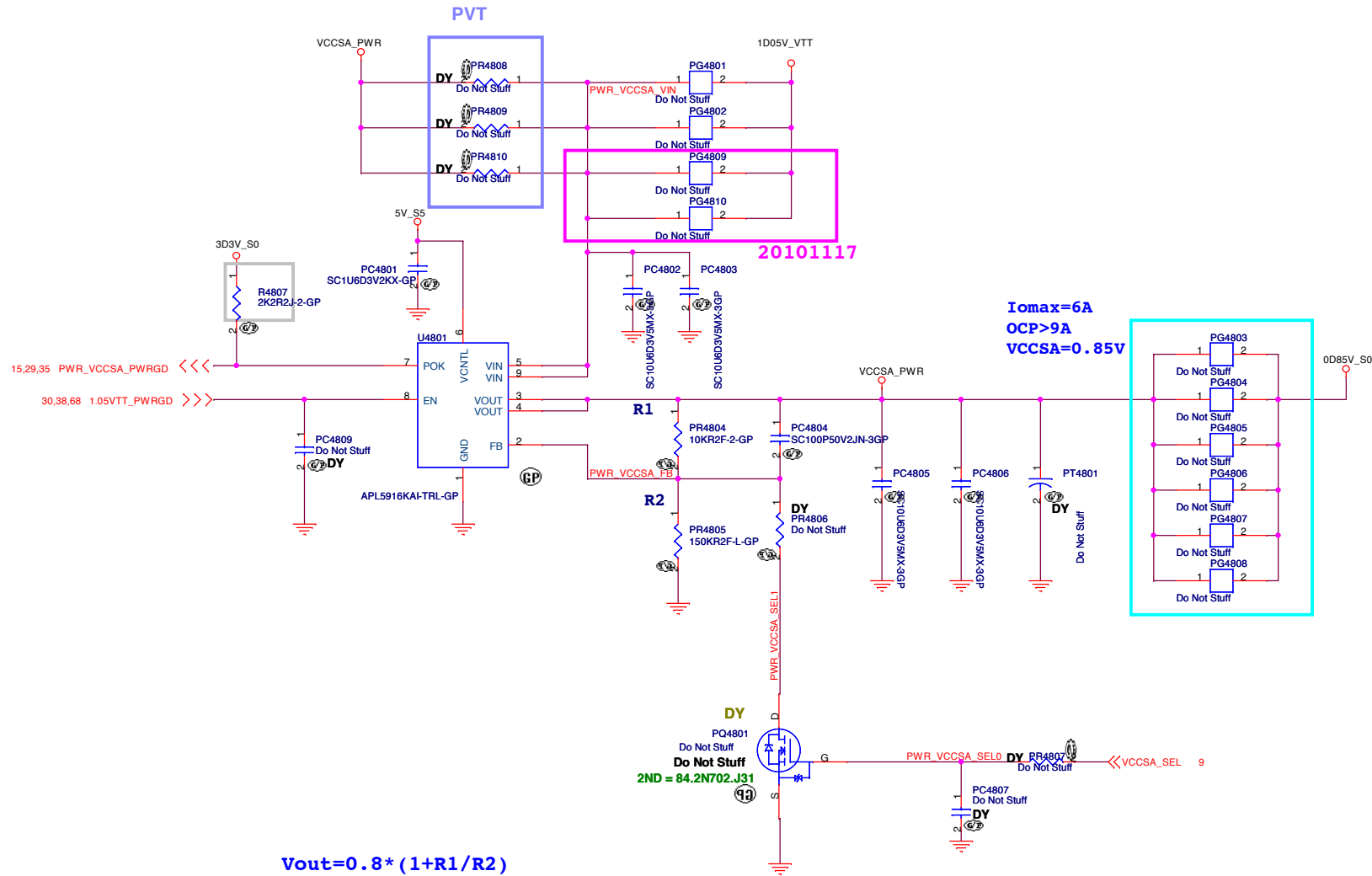
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
LDO 1D8V(RT9025)		
Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1
Date:	Wednesday, March 02, 2011	Sheet 40 of 74

APL5916 for VCCSA



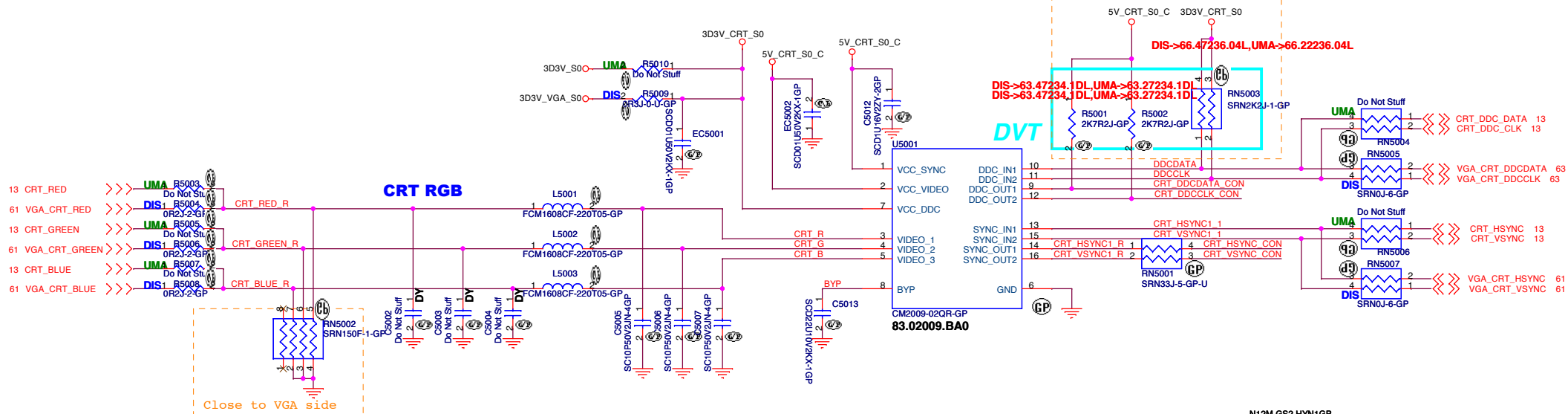
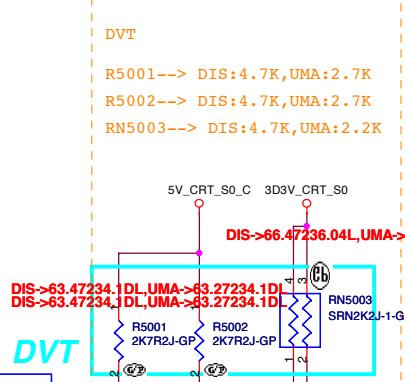
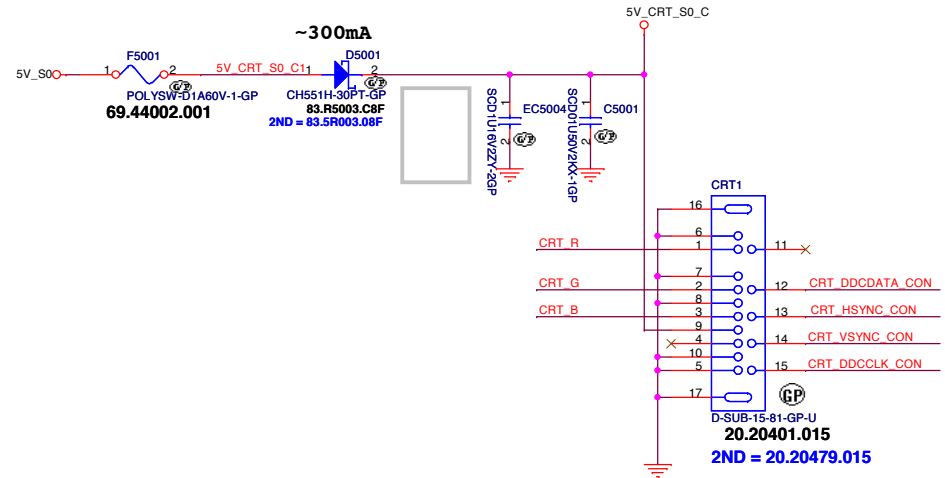
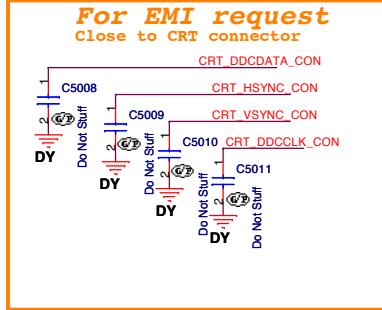
VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

N12M GS2 HYN1GB

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LDO VCCSA(APL5916)		
Size	Document Number	Rev
A3	Z50-HR { Huron River Platform }	-1
Date:	Wednesday, March 02, 2011	Sheet 41 of 74

CRT I/F & CONNECTOR



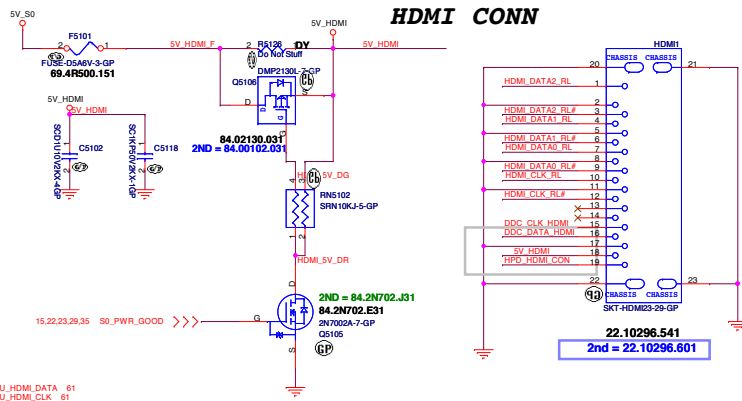
N12M GS2 HYH1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

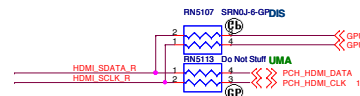
Title: **CRT Connector**

Size A3 Document Number: **250-HR {Huron River Platform}** Rev: **-1**

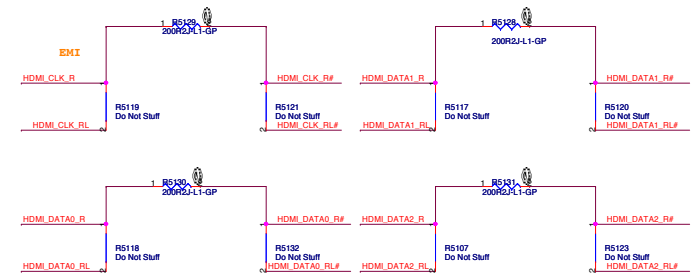
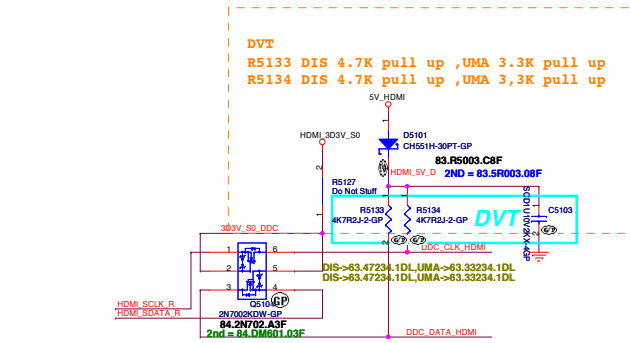
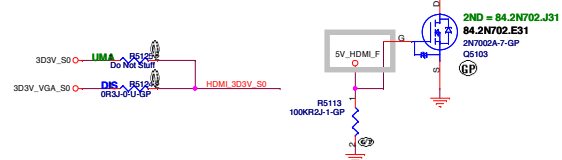
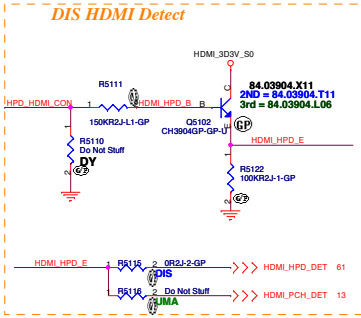
Date: Friday, March 18, 2011 Sheet: 43 of 74



13	HDMI_DATA2_C	>>>	C5119	1	UMA	Do Not Stuff	HDMI_DATA2_B
13	HDMI_DATA2_C#F	>>>	C5120	1	UMA	Do Not Stuff	HDMI_DATA2_R#F
13	HDMI_DATA1_C	>>>	C5121	1	UMA	Do Not Stuff	HDMI_DATA1_R
13	HDMI_DATA1_C#F	>>>	C5122	1	UMA	Do Not Stuff	HDMI_DATA1_R#F
13	HDMI_DATA0_C	>>>	C5123	1	UMA	Do Not Stuff	HDMI_DATA0_R
13	HDMI_DATA0_C#F	>>>	C5124	1	UMA	Do Not Stuff	HDMI_DATA0_R#F
13	HDMI_CLK_C	>>>	C5125	1	UMA	Do Not Stuff	HDMI_CLK_R
13	HDMI_CLK_C#F	>>>	C5126	1	UMA	Do Not Stuff	HDMI_CLK_R#F

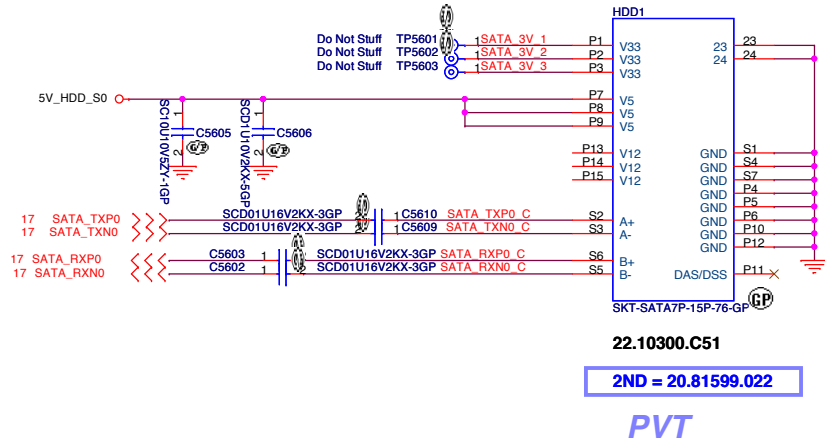


RN5103, RN5104
For Intel SPEC the resistor need stuff 680 ohm
For VGA SPEC the resistor need stuff 499 ohm

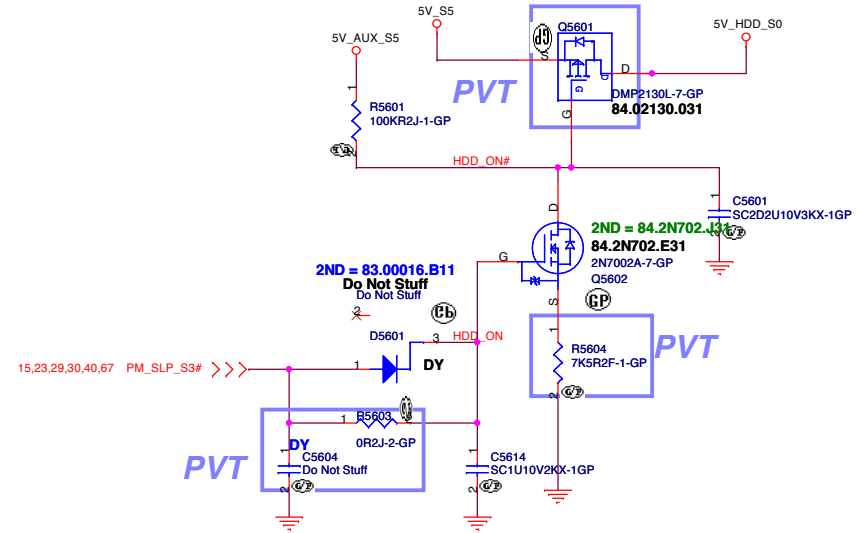


SSID = SATA

SATA HDD Connector



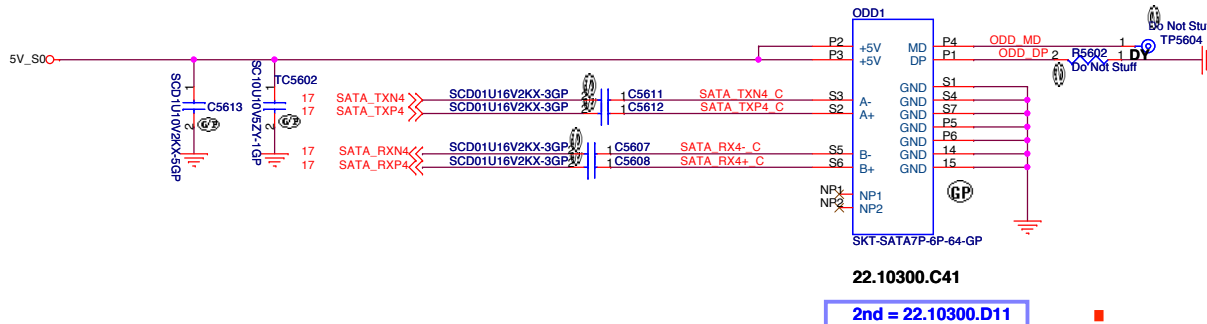
Delay HDD power



Delay HDD power off timing for 400ms after SATA controller shut down. Control the C5601 and R5601 to finally tune delay timing between 500ms and 400ms.

ODD Connector

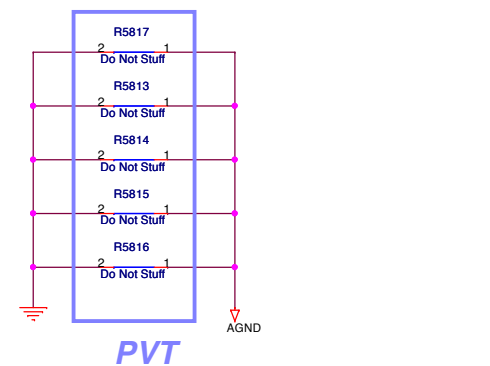
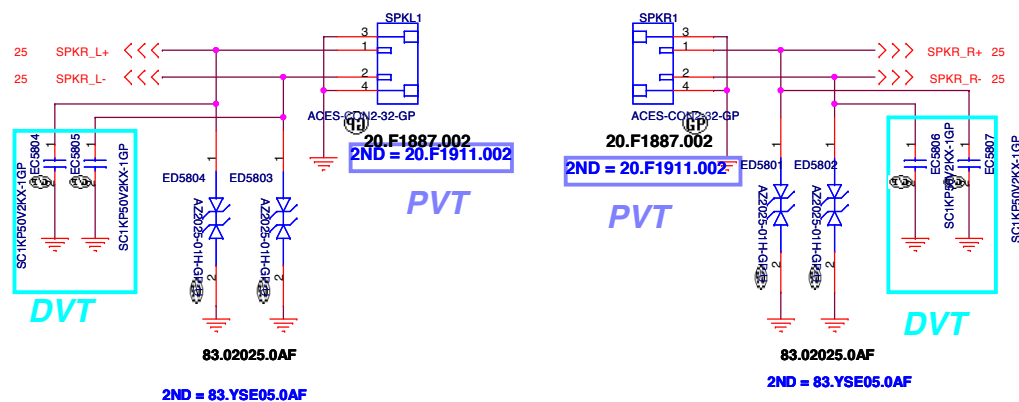
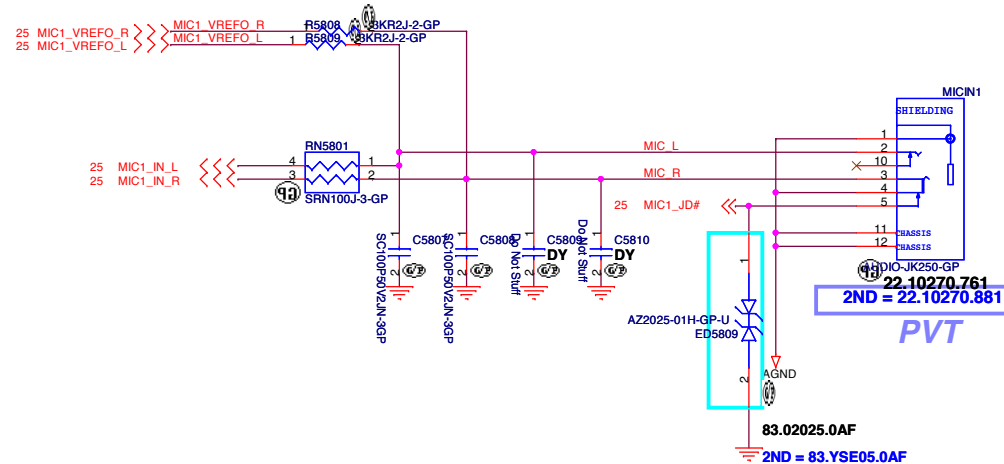
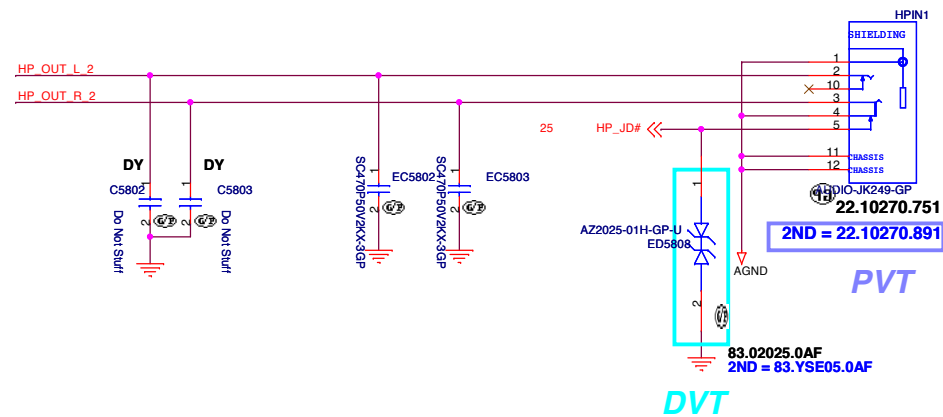
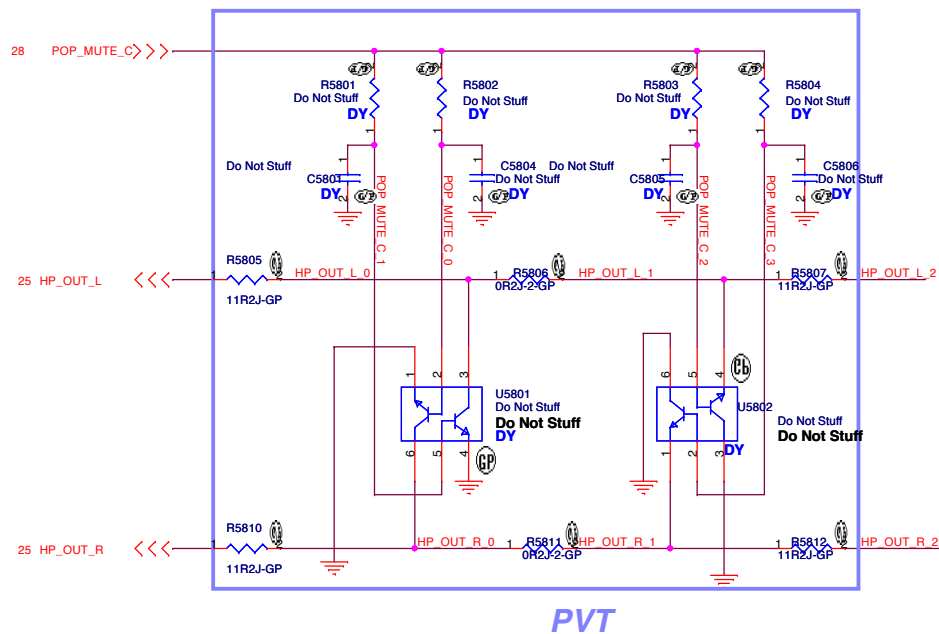
SATA RX- and SATA RX+ Trace
Length match within 20 mil



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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDD/ODD			
Size A3	Document Number Z50-HR { Huron River Platform}	Rev -1	
Date: Wednesday, March 02, 2011	Sheet 45	of	74



N12M GS2 HYN1GB

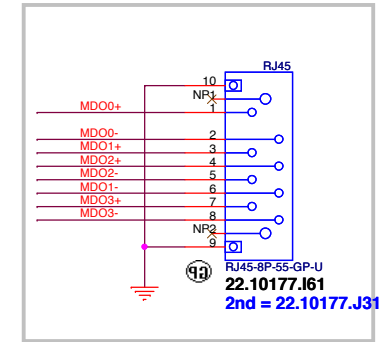
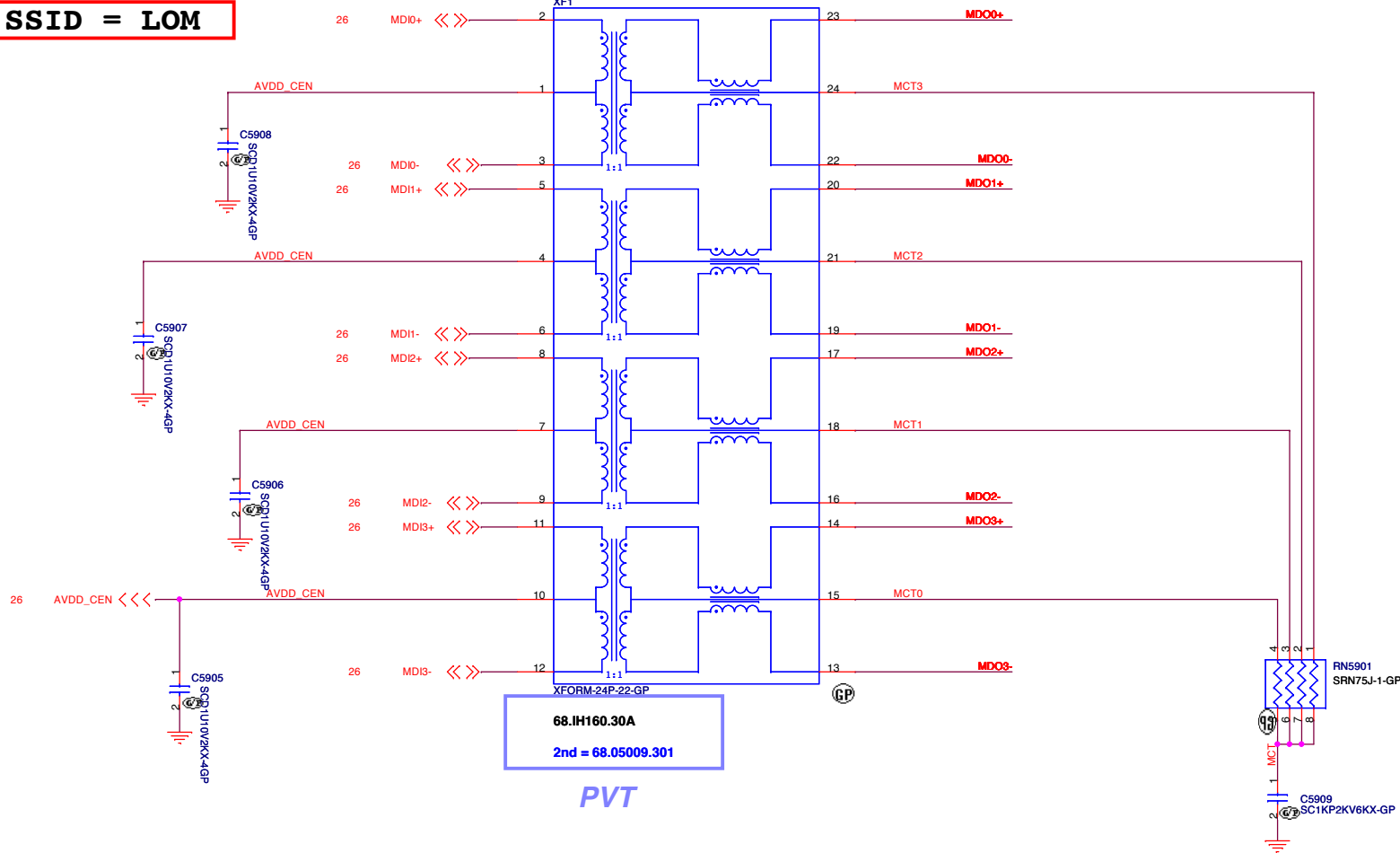
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

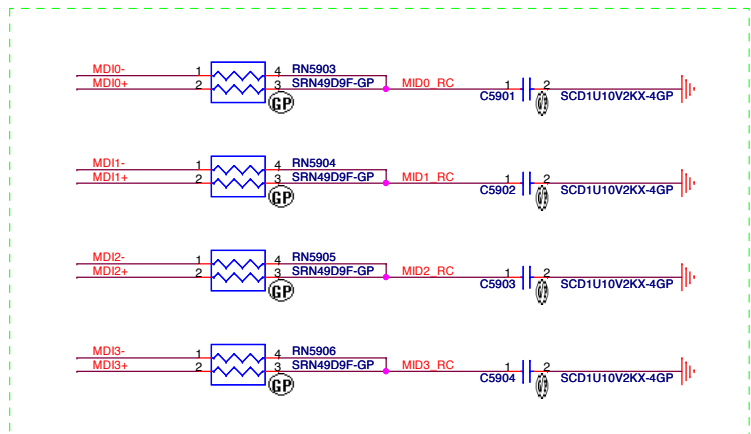
Size A3 Document Number: **Z50-HR (Huron River Platform)** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 46 of 74

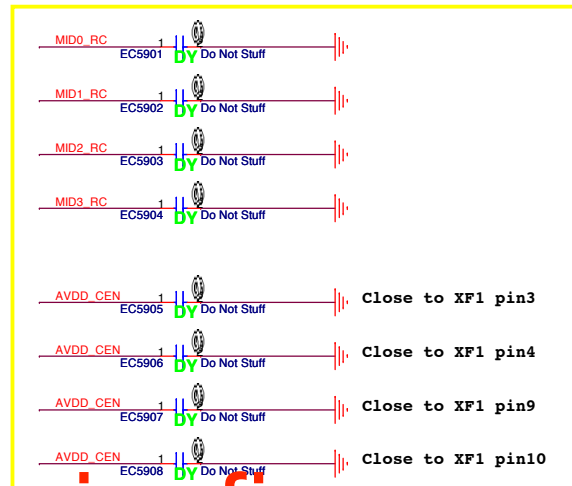
SSID = LOM



Close to LAN AR8151



EMI



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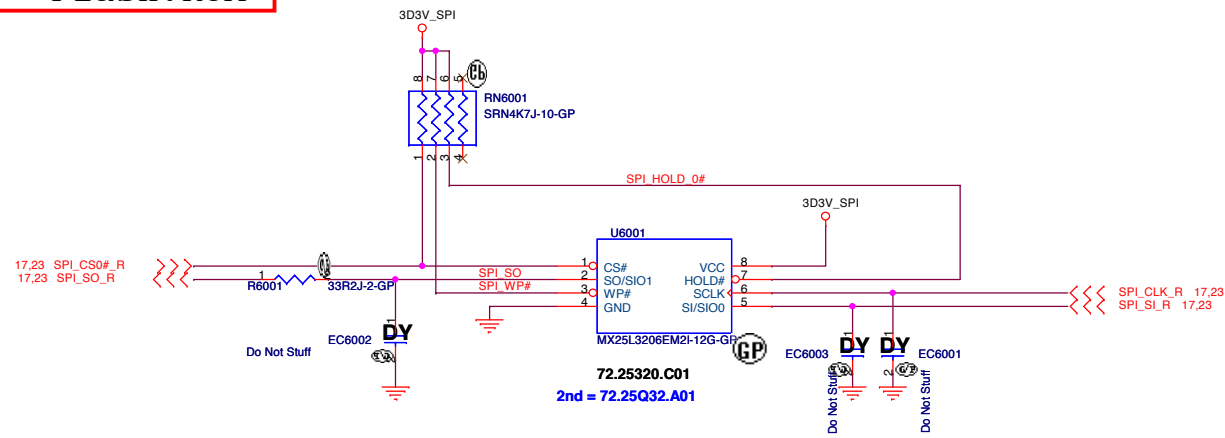
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

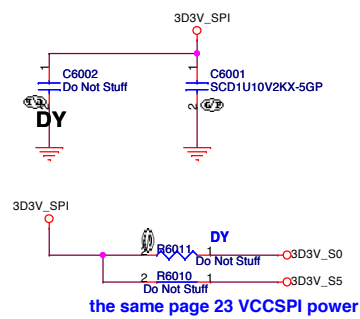
Size A3 Document Number: **Z50-HR { Huron River Platform}** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 47 of 74

SSID = Flash.ROM

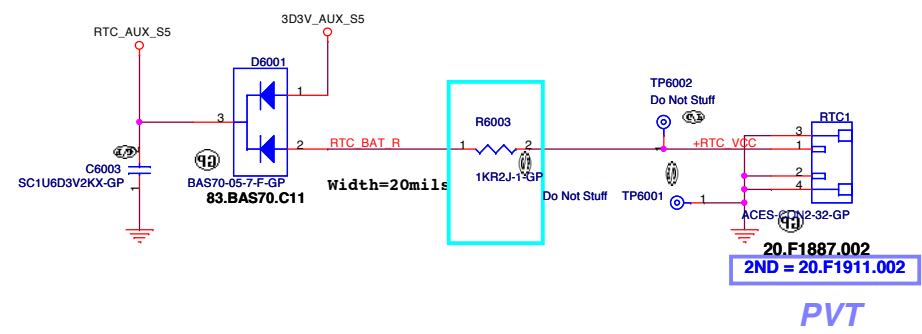
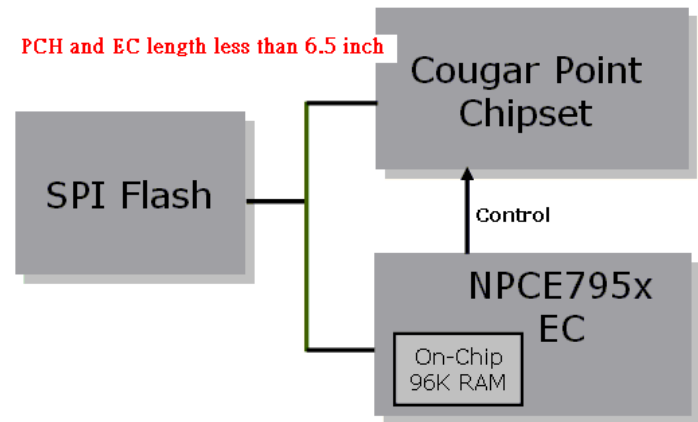


SYSTEM SPI ROM
Socket : 62.10089.001



SPI ROM Equal length need to less than 500mil

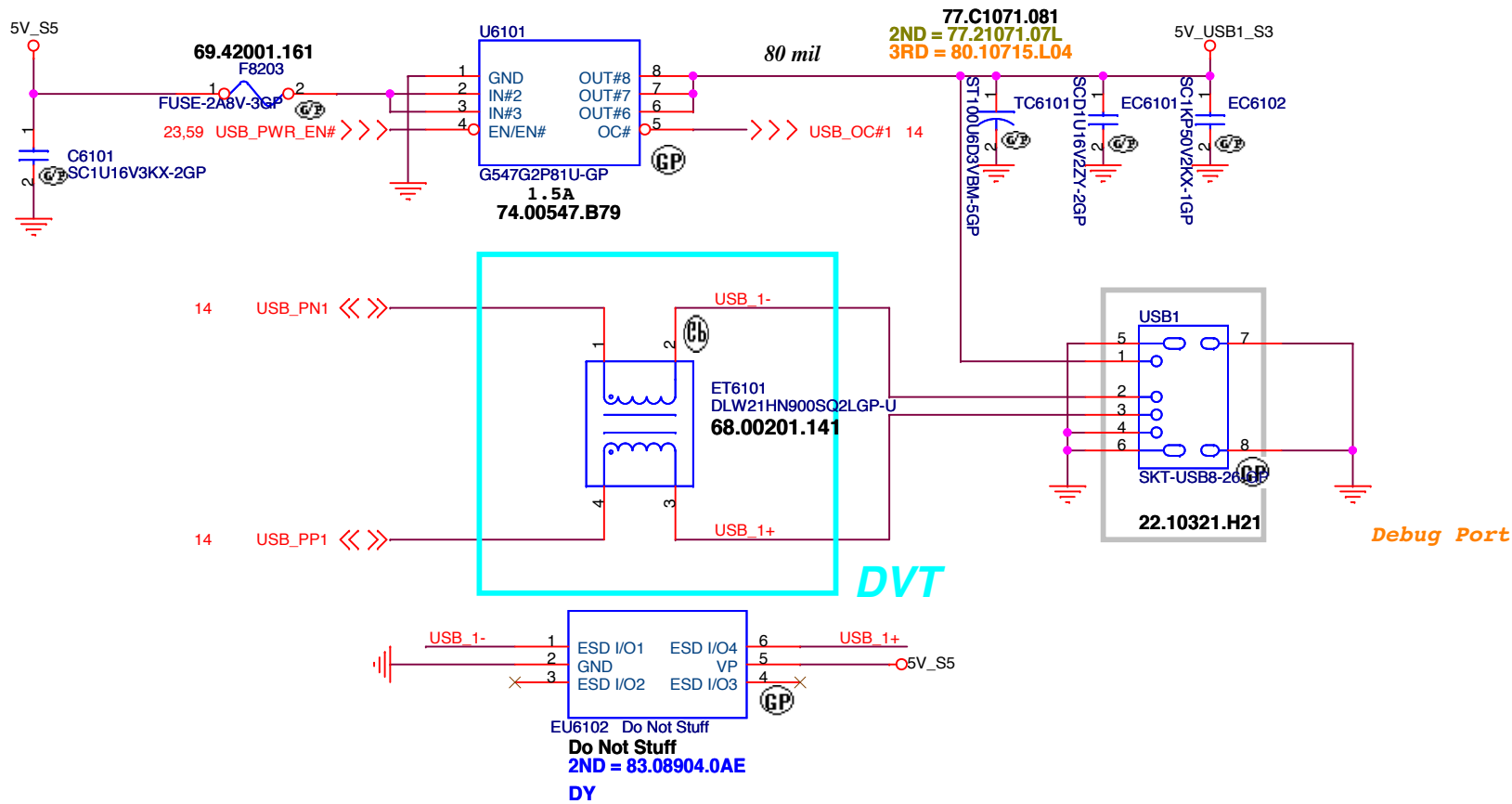
PCH and EC length less than 6.5 inch



PVT

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緯創資通 Wistron Corporation		
<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		
Title	Flash(KBC+PCH)/RTC CONN	
Size A3	Document Number	Rev
	Z50-HR { Huron River Platform}	-1
Date: Wednesday, March 02, 2011	Sheet 48	of 74



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size

Document Number

Rev

A4

Z50-HR { Huron River Platform}

-1

Date:

Wednesday, March 02, 2011

Sheet

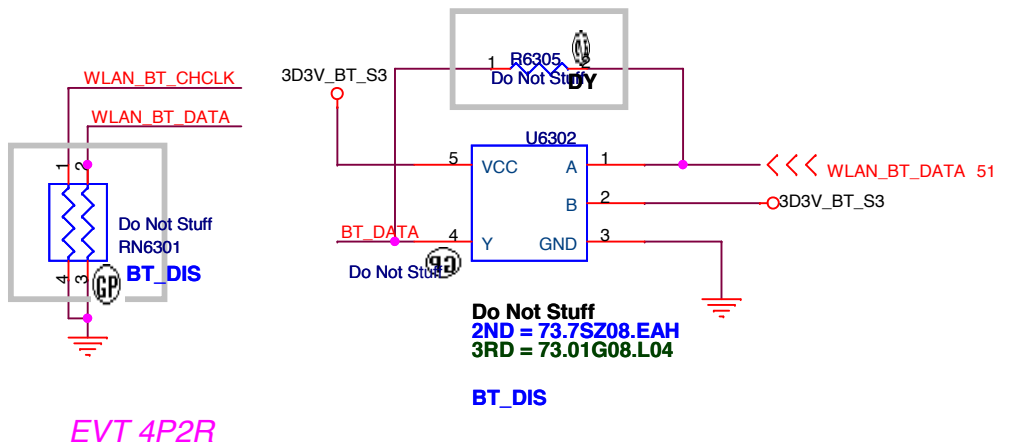
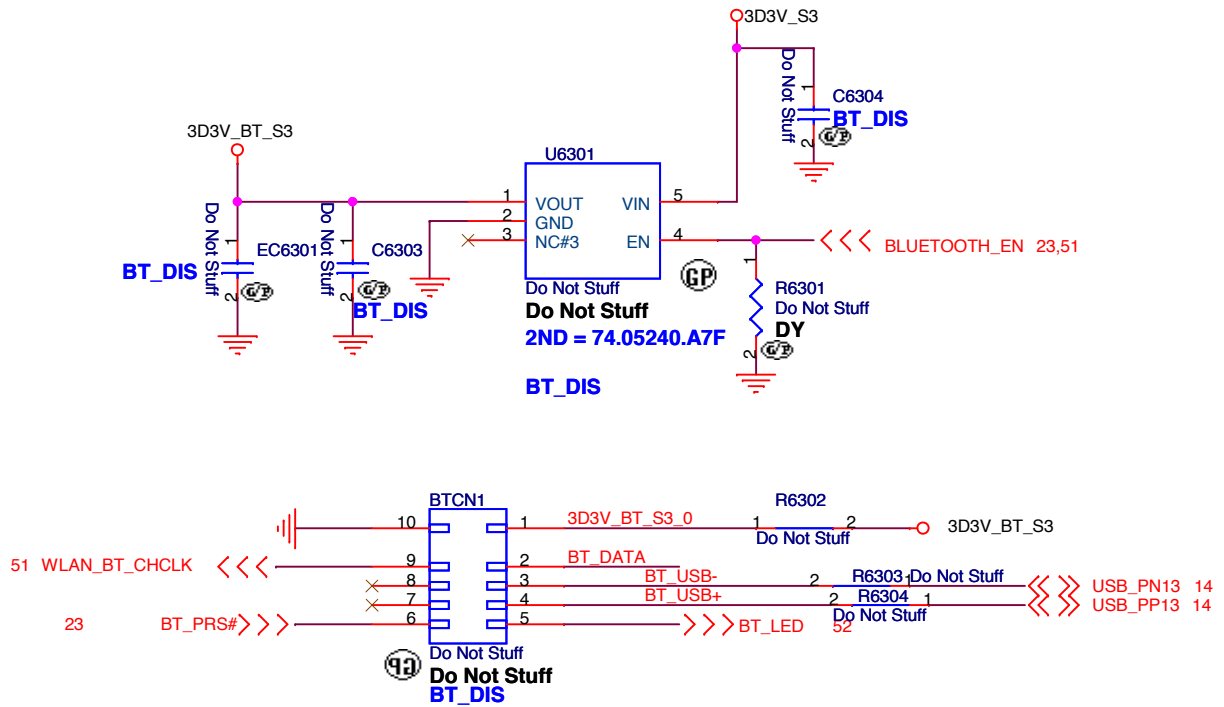
49

of

74

SSID = User.Interface
Bluetooth Module conn.

Bluetooth



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

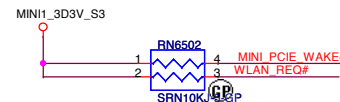
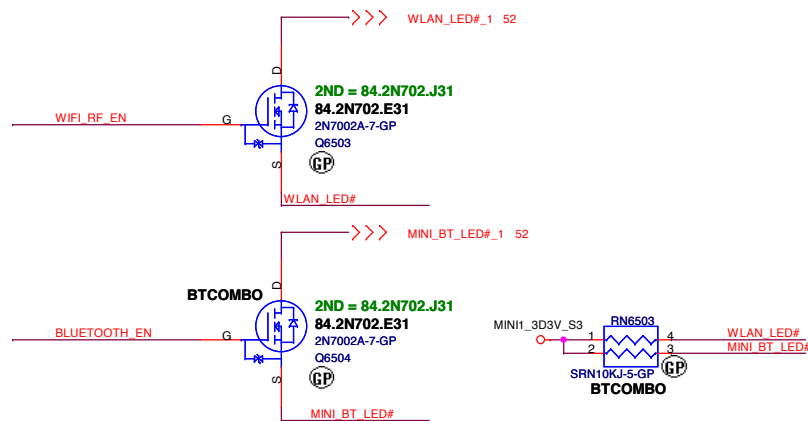
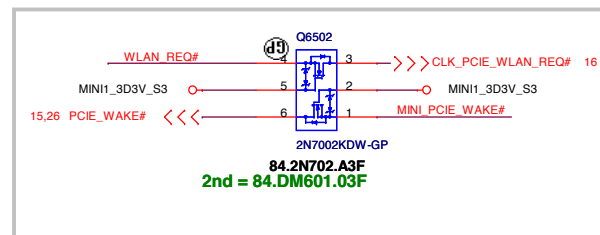
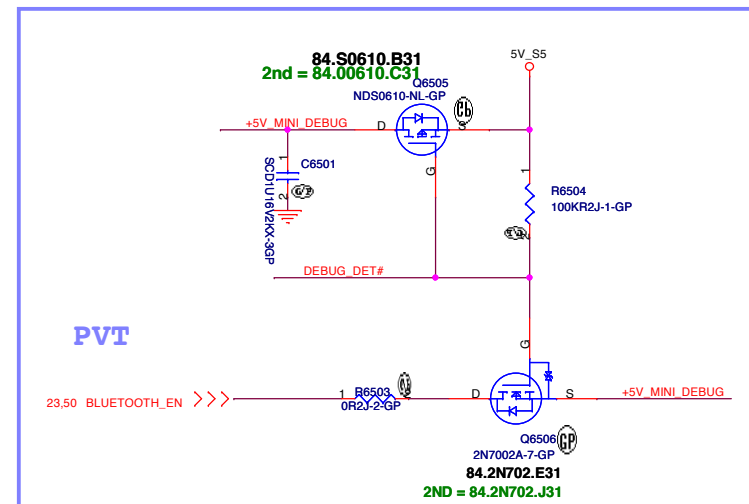
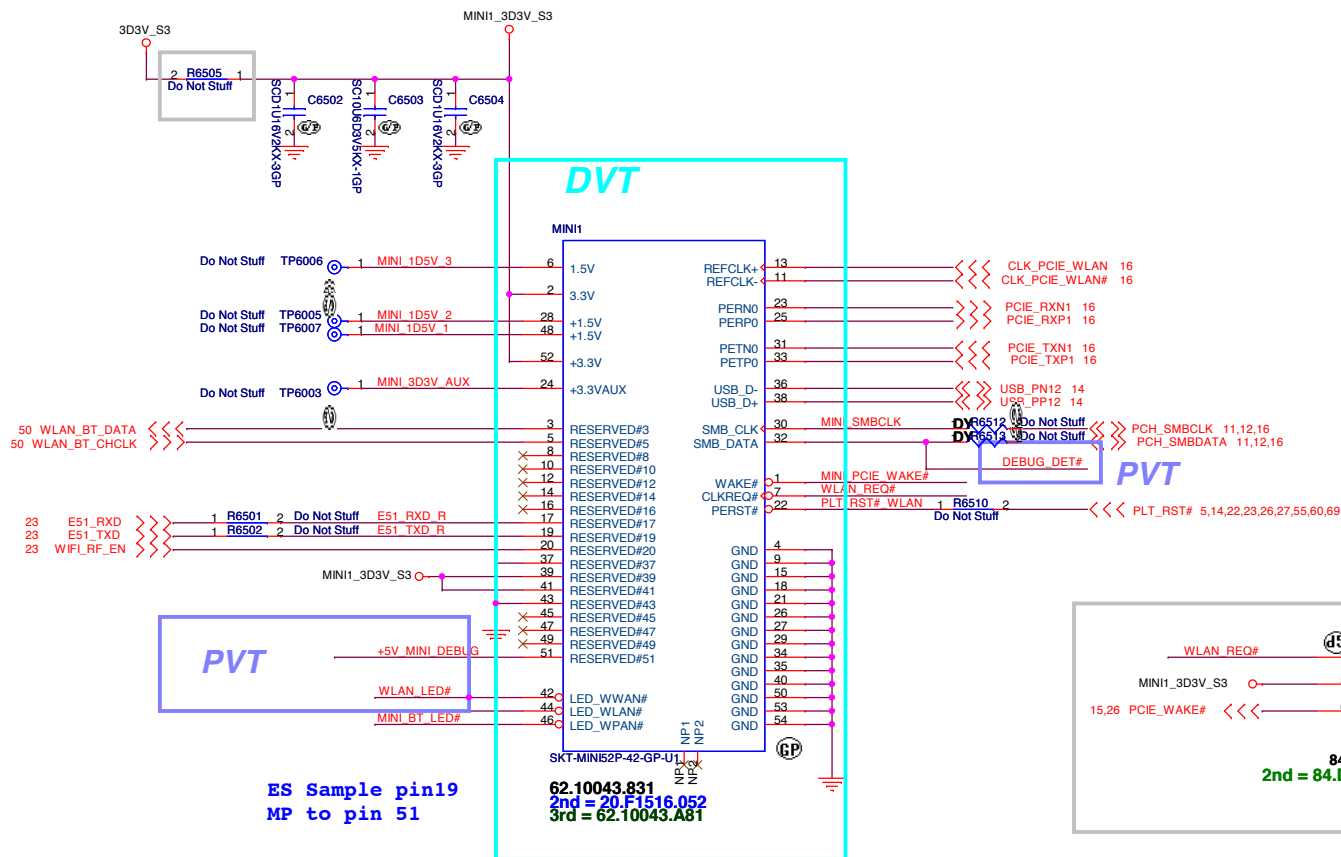
Title **Bluetooth**

Size A4 Document Number **250-HR { Huron River Platform}** Rev **-1**

Date: Wednesday, March 02, 2011 Sheet 50 of 74

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

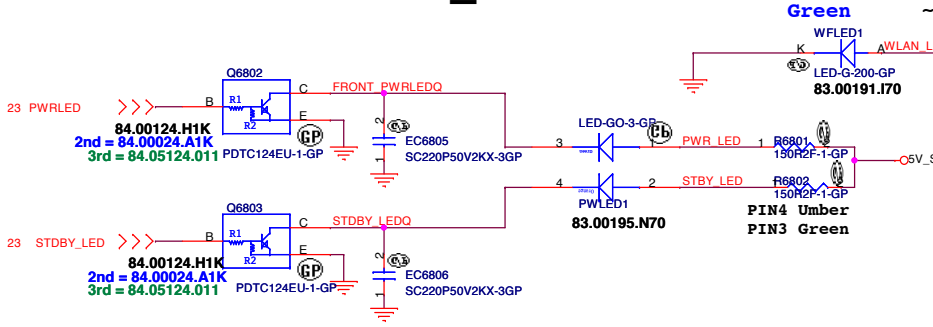


N12M GS2 HYN1GB

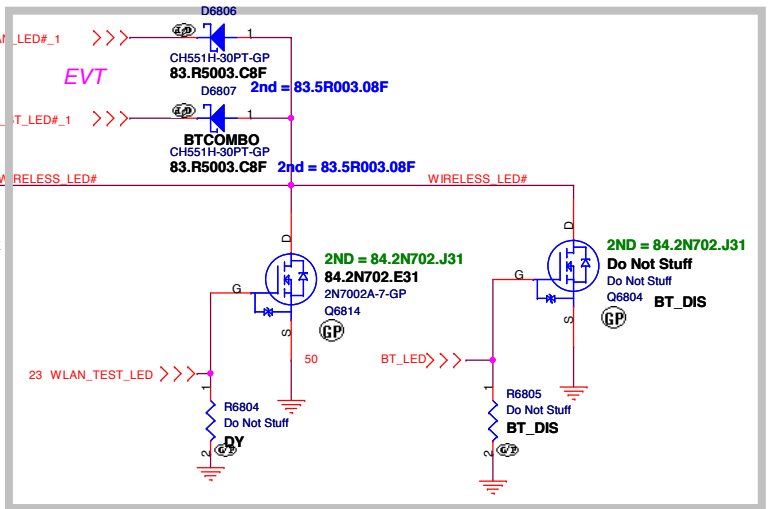
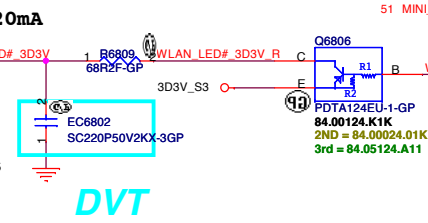
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title MINICARD(WLAN&WMAX)		
Size A3	Document Number Z50-HR (Huron River Platform)	Rev -1
Date: Wednesday, March 02, 2011	Sheet 51 of 74	

**Power button LED
Power STDBY_LED**



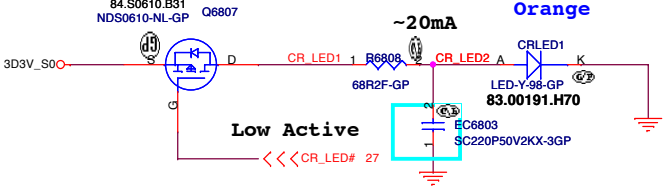
WLAN_LED



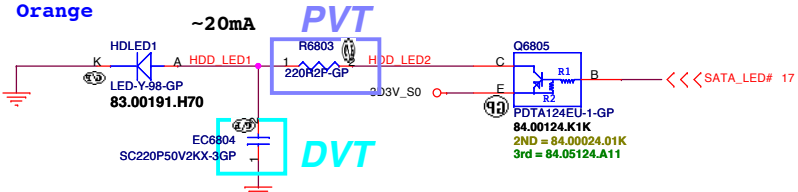
Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

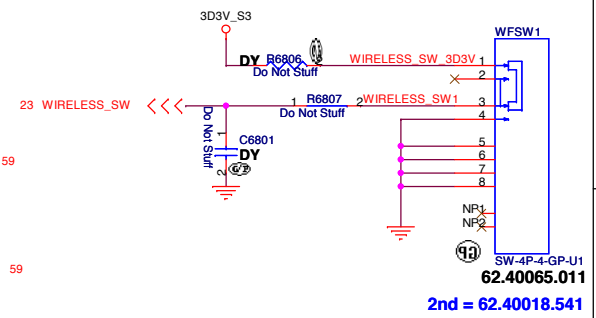
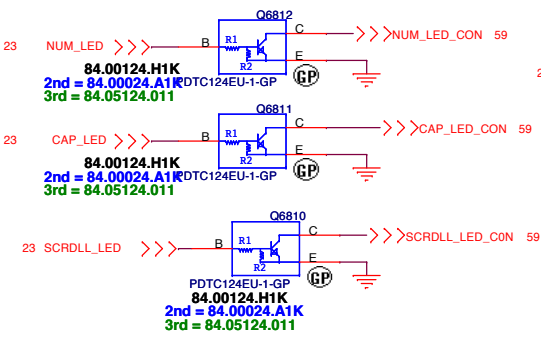
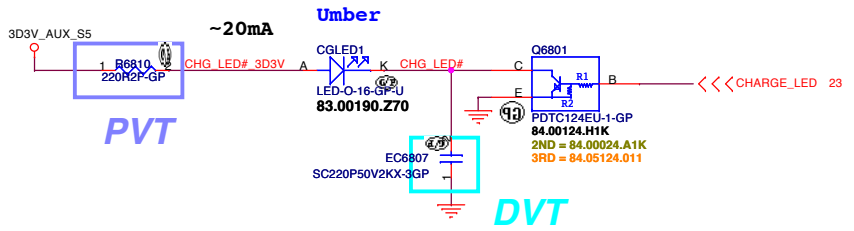
SD/MS LED



SATA HDD LED



Battery LED1 (CHARGE)



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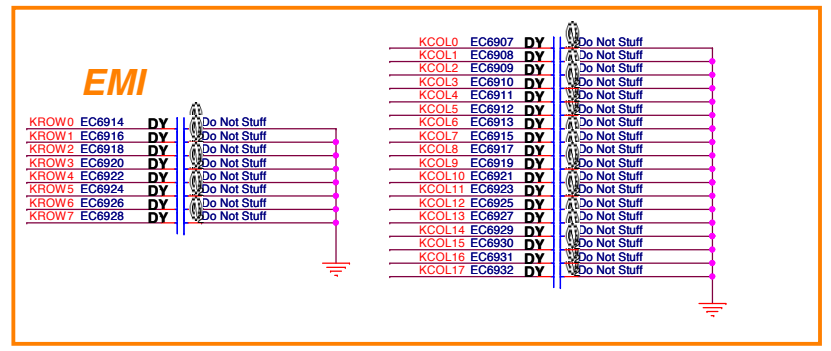
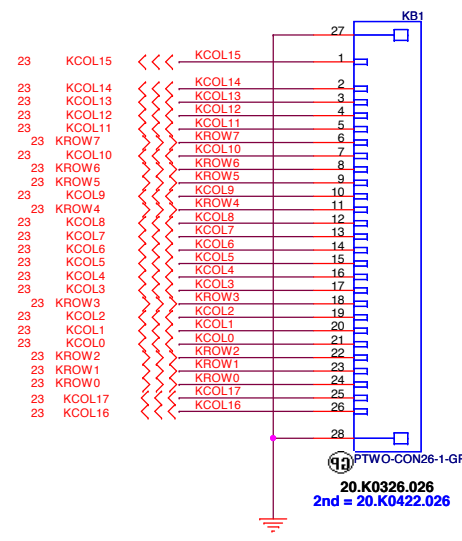
Title: **LED/Wireless Switch**

Size A3 Document Number: **Z50-HR (Huron River Platform)** Rev: **-1**

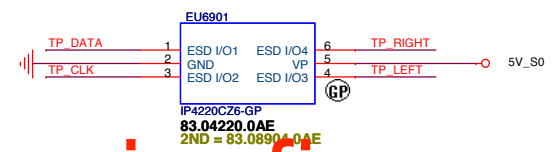
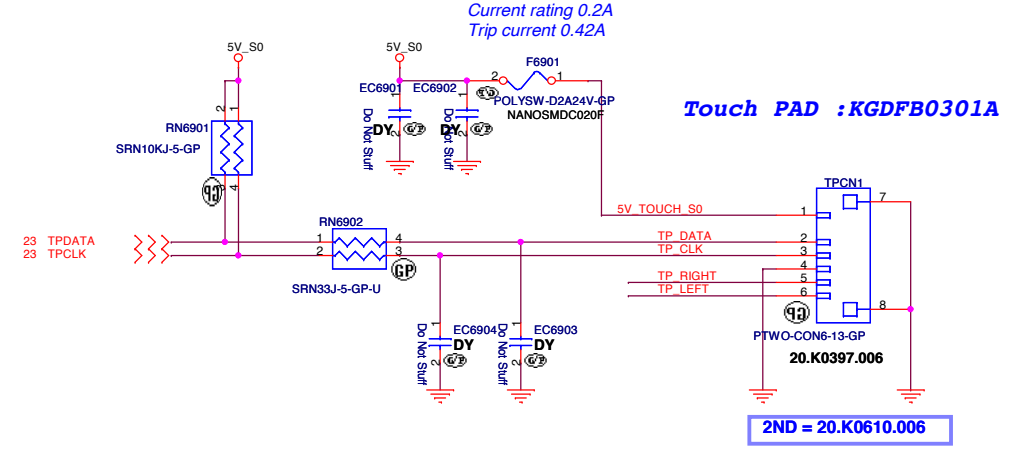
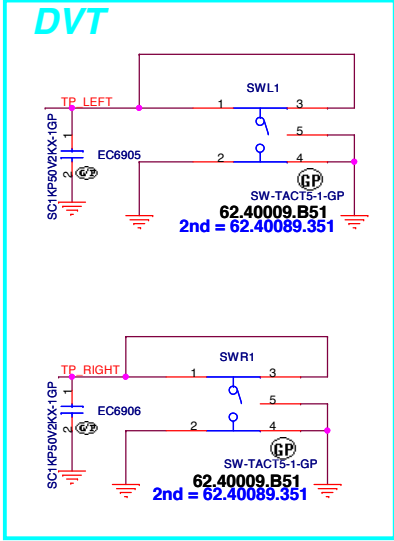
Date: Wednesday, March 02, 2011 Sheet 52 of 74

SSID = KBC

Internal KeyBoard Connector



TOUCH PAD



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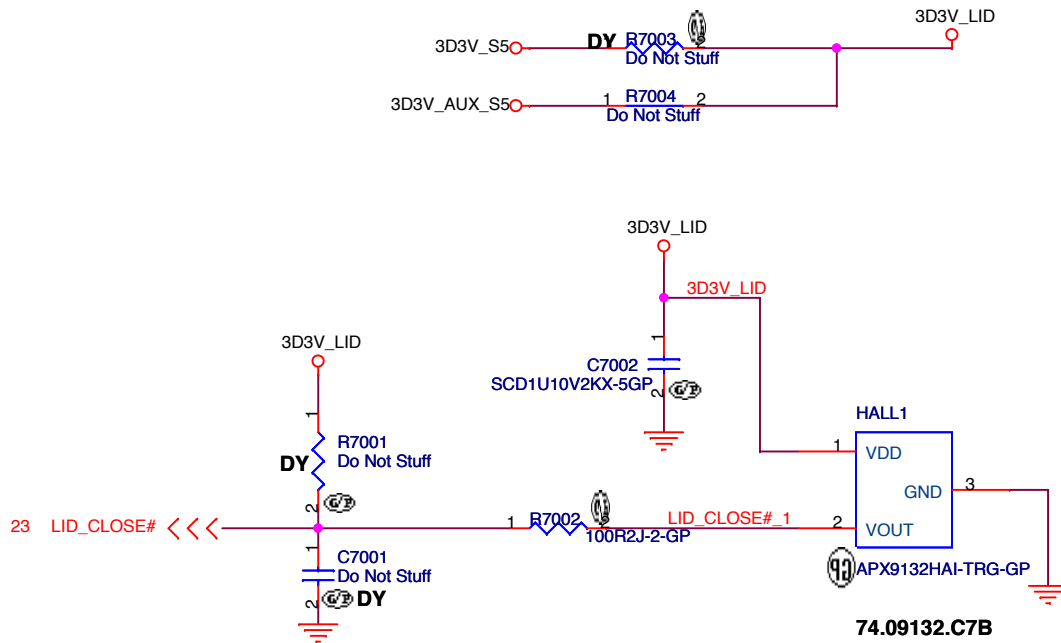
N12M GS2 HYN1GB

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size A3 Document Number: **Z50-HR (Huron River Platform)** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 53 of 74



N12M GS2 HYN1GB

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Title

Hall Sensor

Size

A4

Document Number

Z50-HR { Huron River Platform}

Rev

-1

Date:

Wednesday, March 02, 2011

Sheet

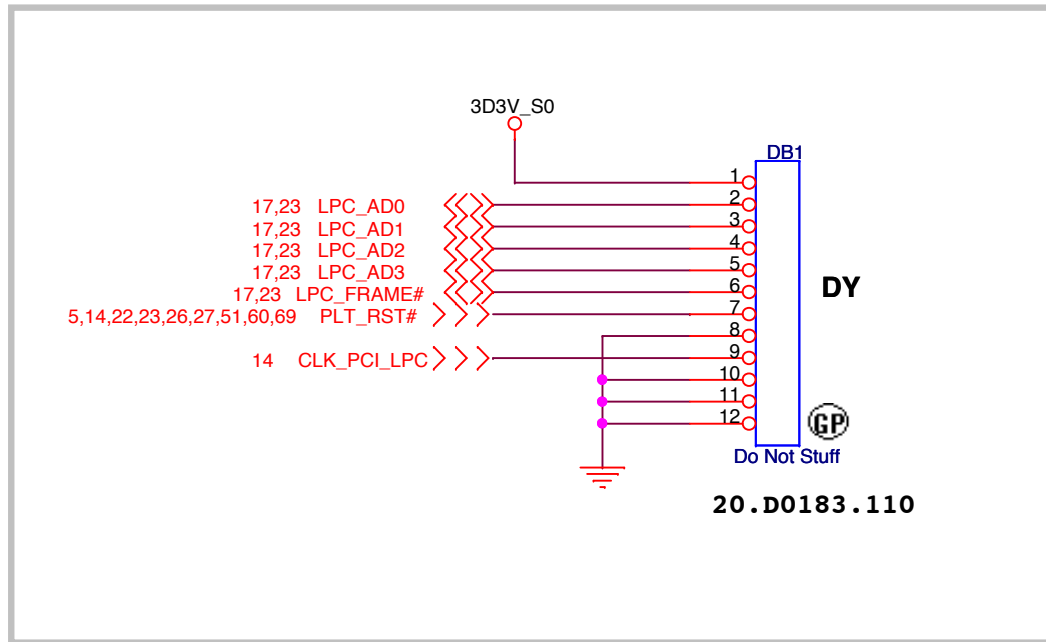
54

of

74

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EVT



N12M GS2 HYN1GB

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size

Document Number

Rev

A

750-HR { Huron River Platform}

-1

Date

Wednesday, March 02, 2011

Sheet

55

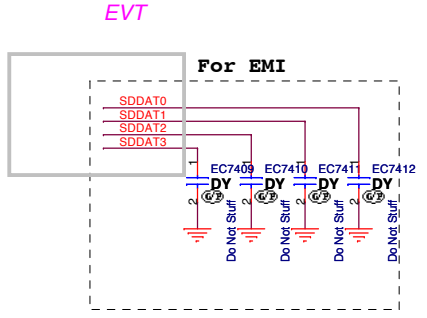
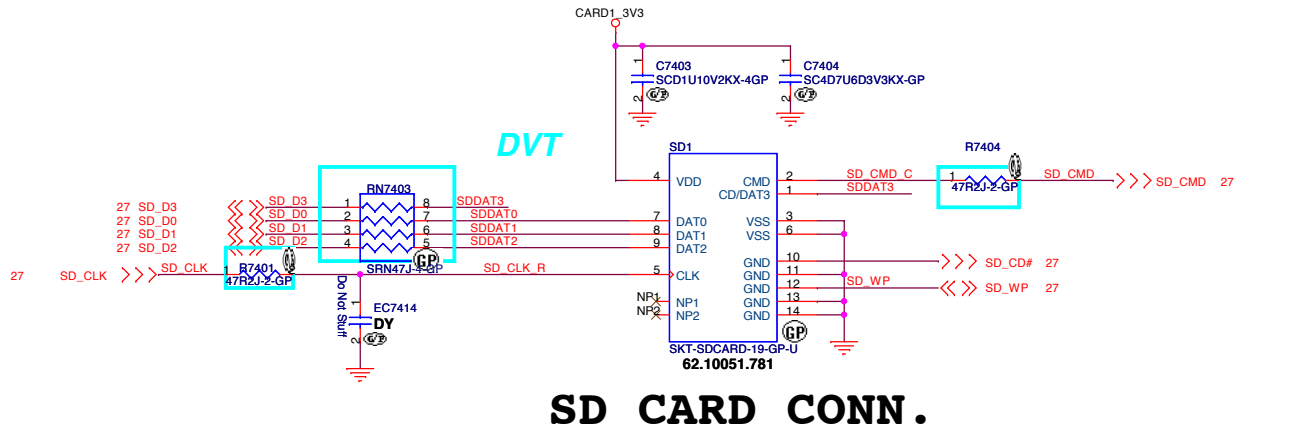
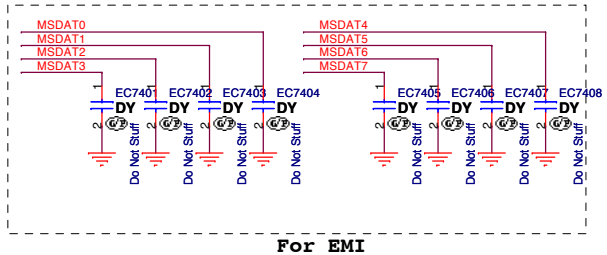
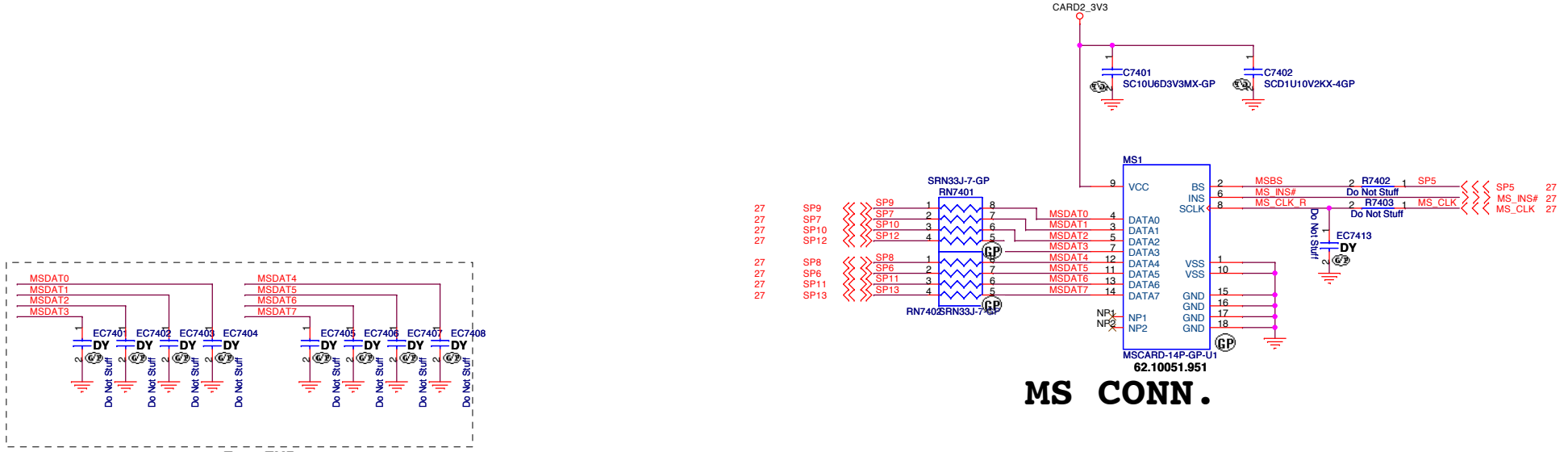
of

74

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SD/MS Card Reader

SSID = SDIO



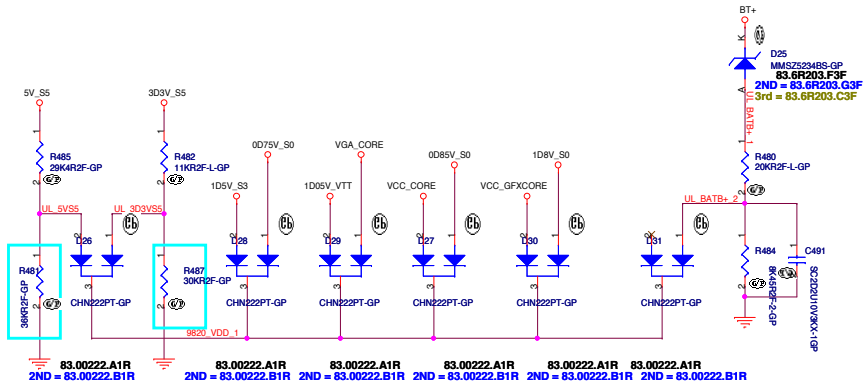
N12M GS2 HYN1GB

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

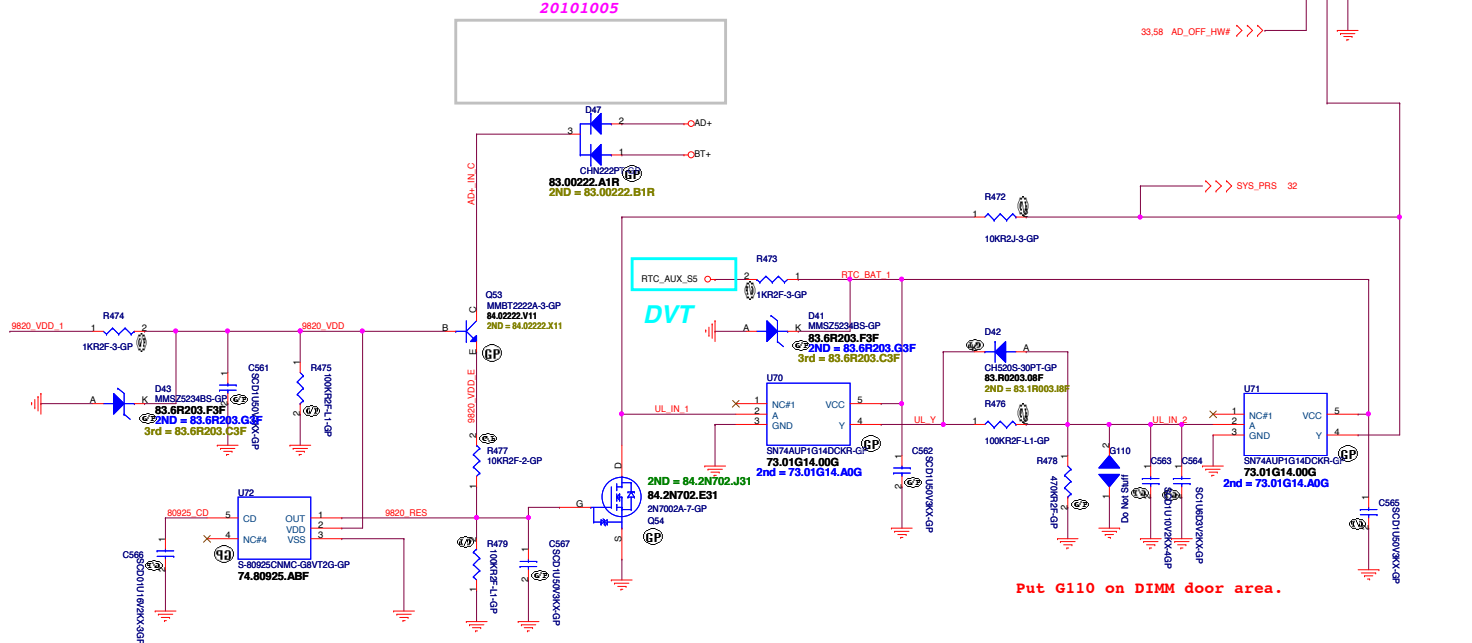
Title: **CARD Reader CONN**

Size: A3 Document Number: **Z50-HR (Huron River Platform)** Rev: **-1**

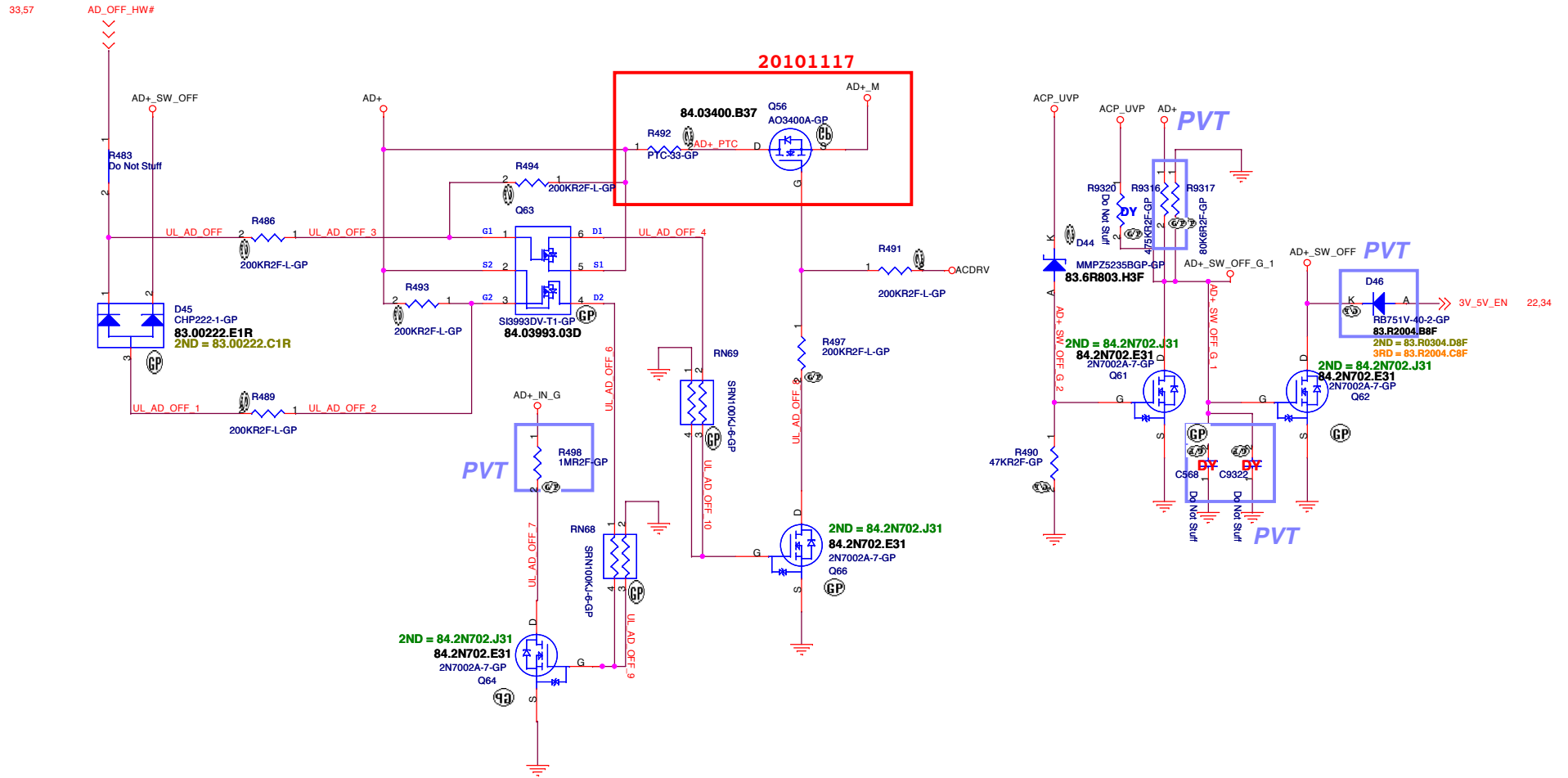
Date: Wednesday, March 02, 2011 Sheet 56 of 74



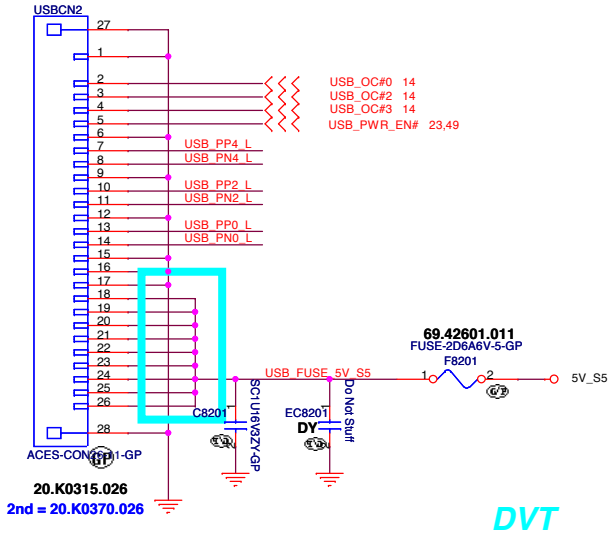
DVT



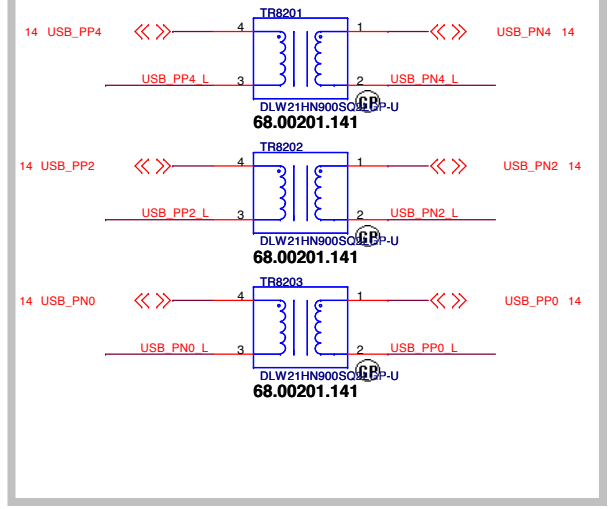
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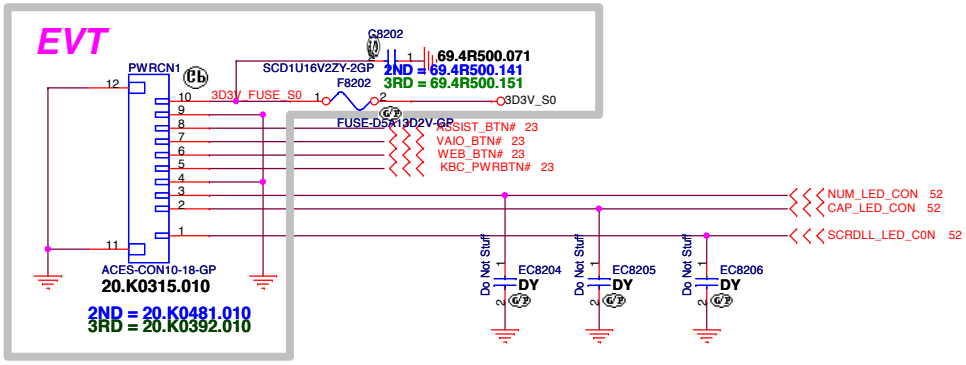
USB BTB CONN



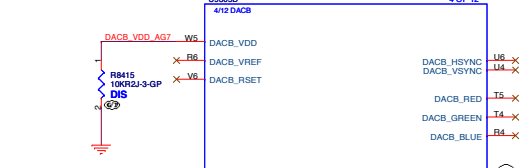
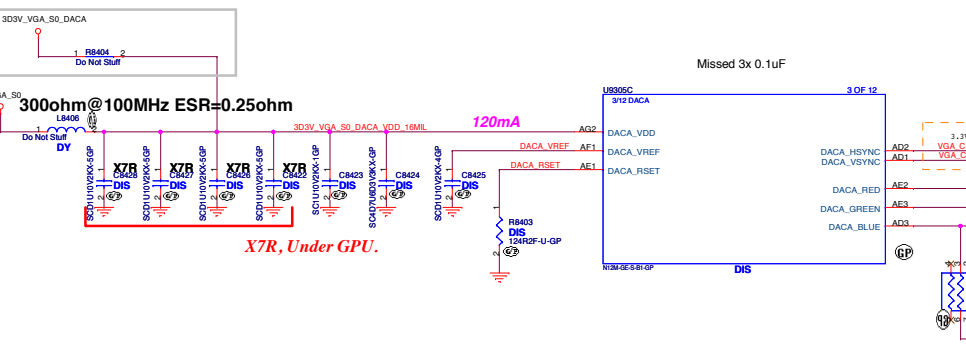
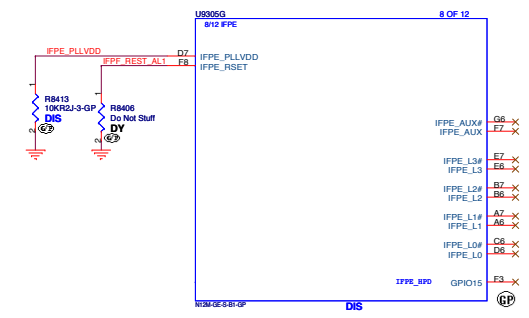
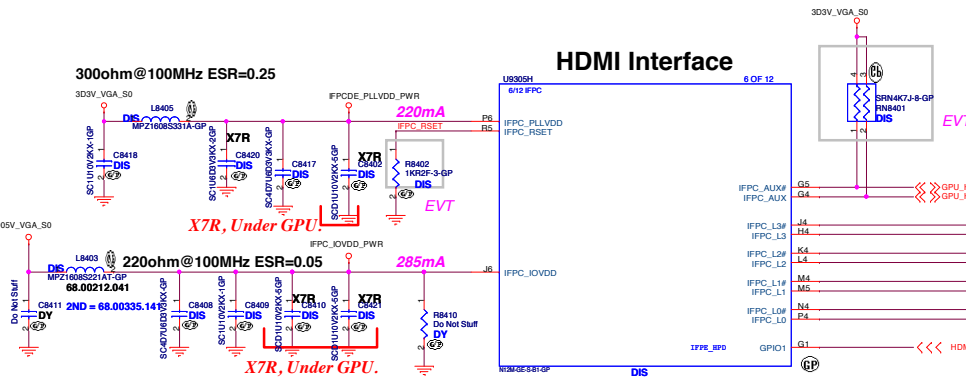
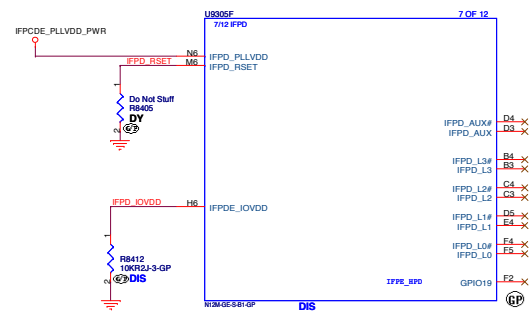
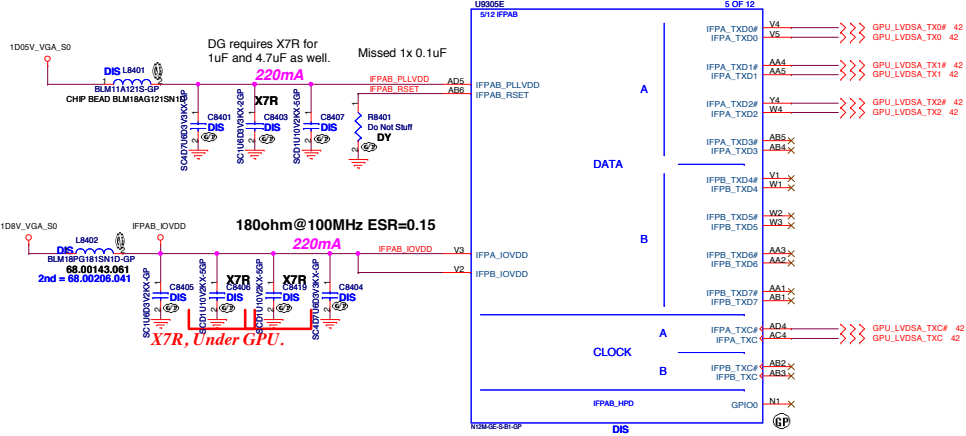
EVT



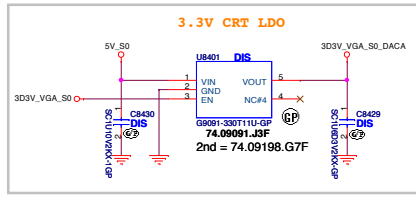
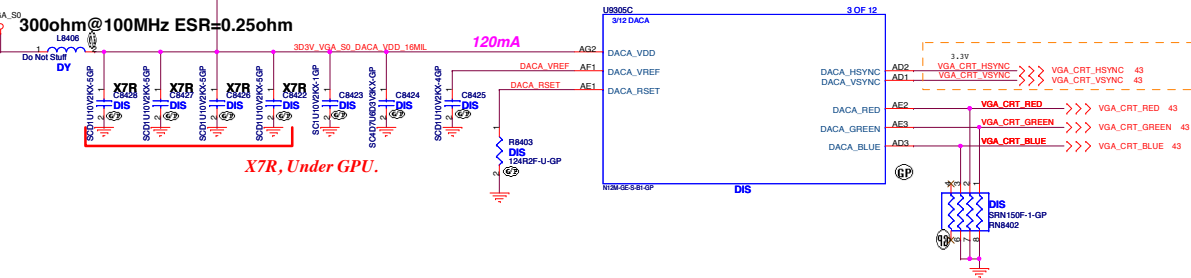
LED BTB CONN

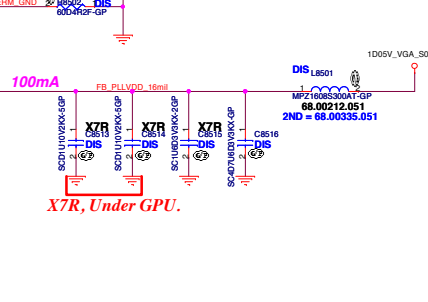
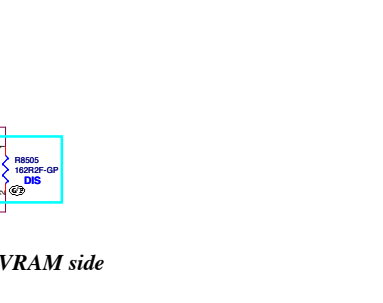
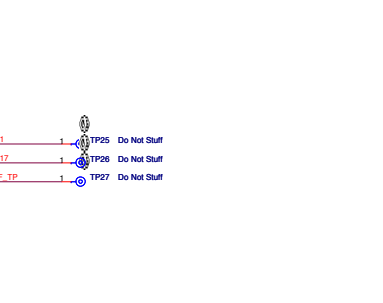
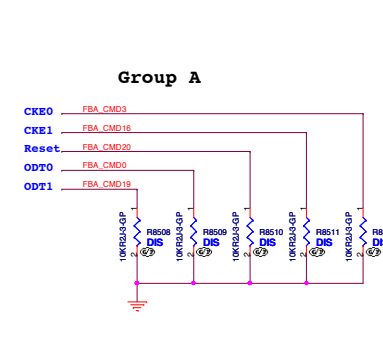
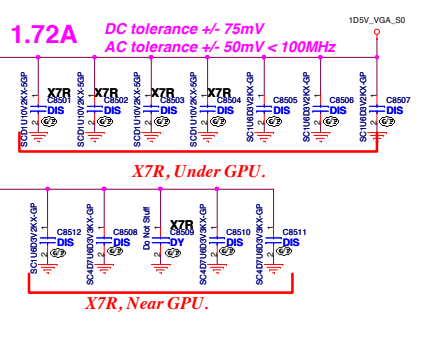
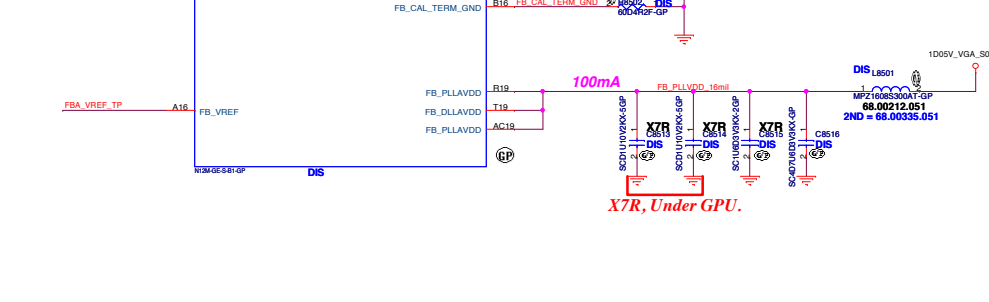
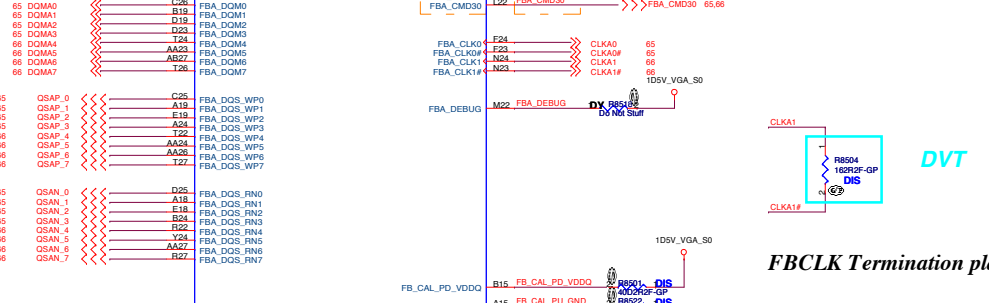
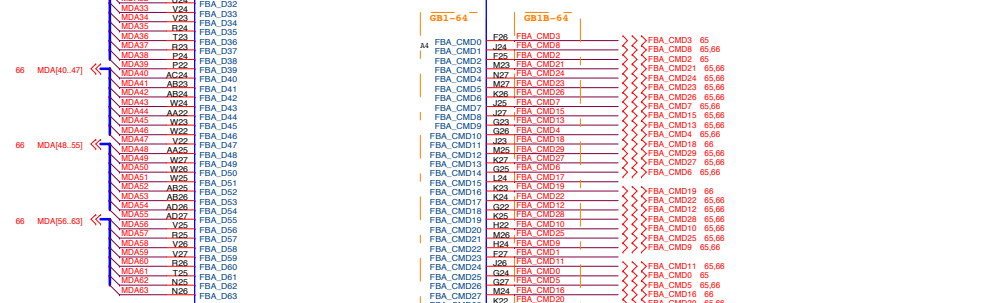
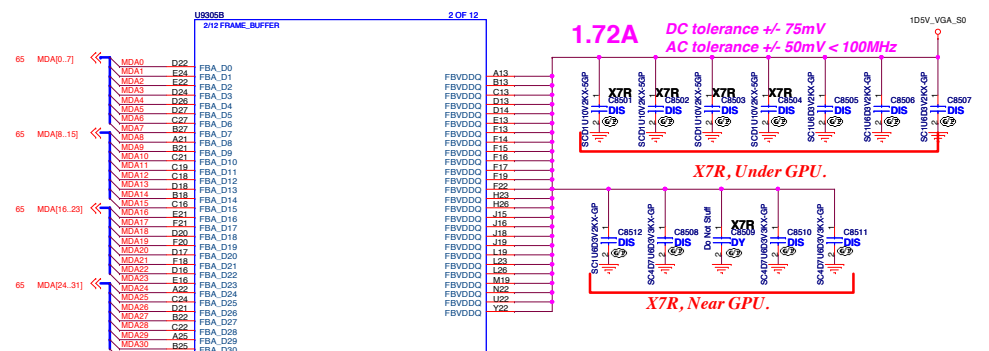


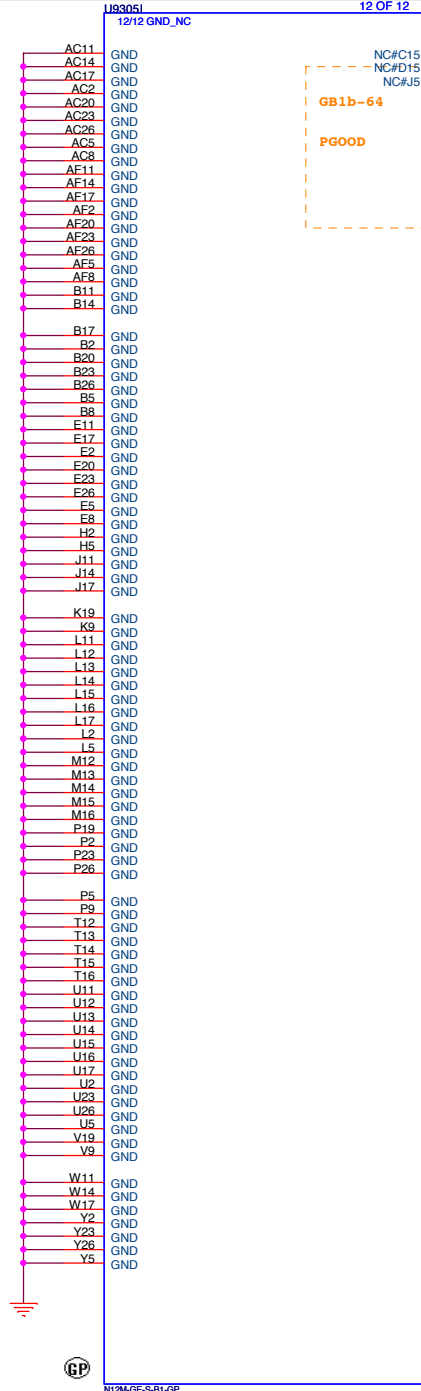
LVDS Interface



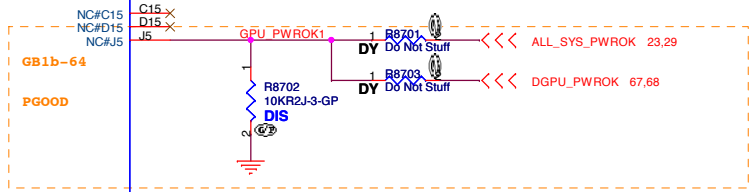
12CA=>CRT, 12CC=>LVDS.







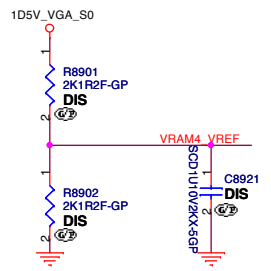
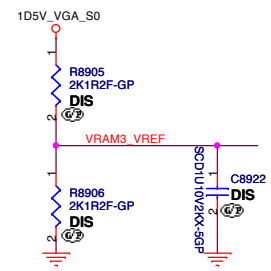
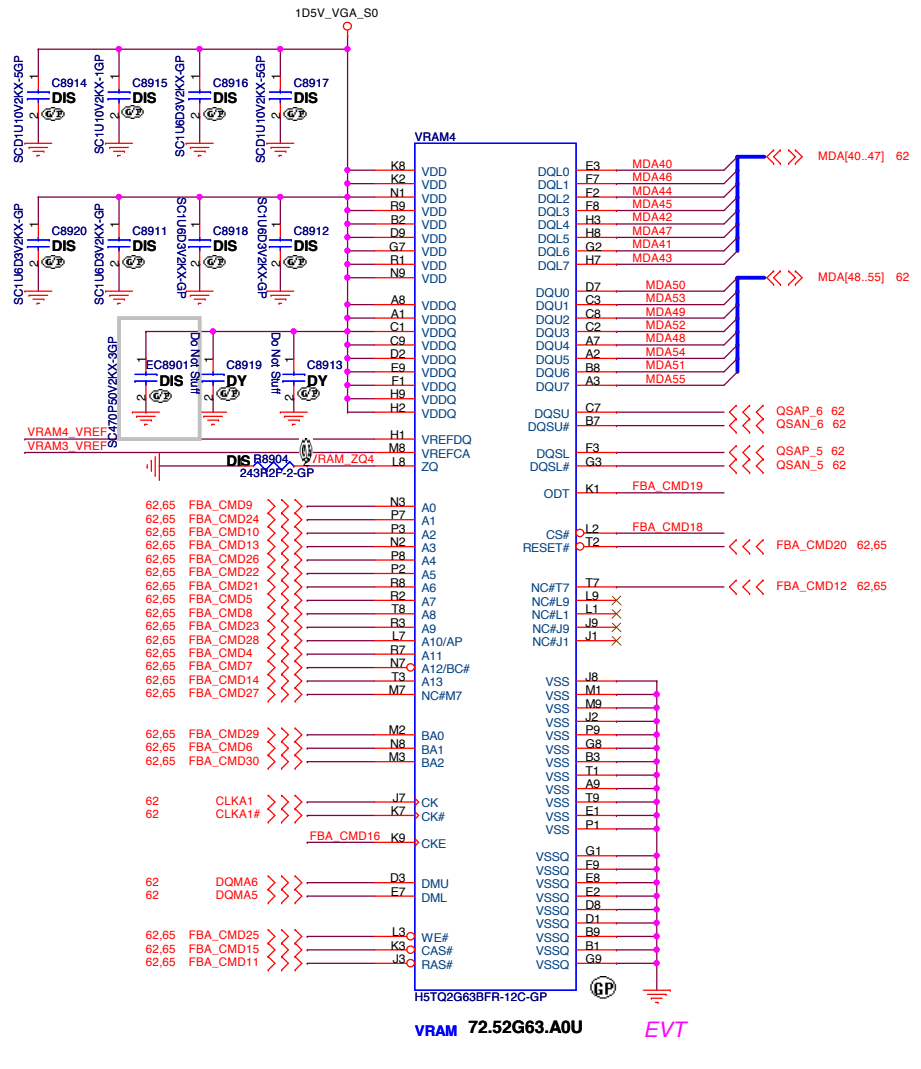
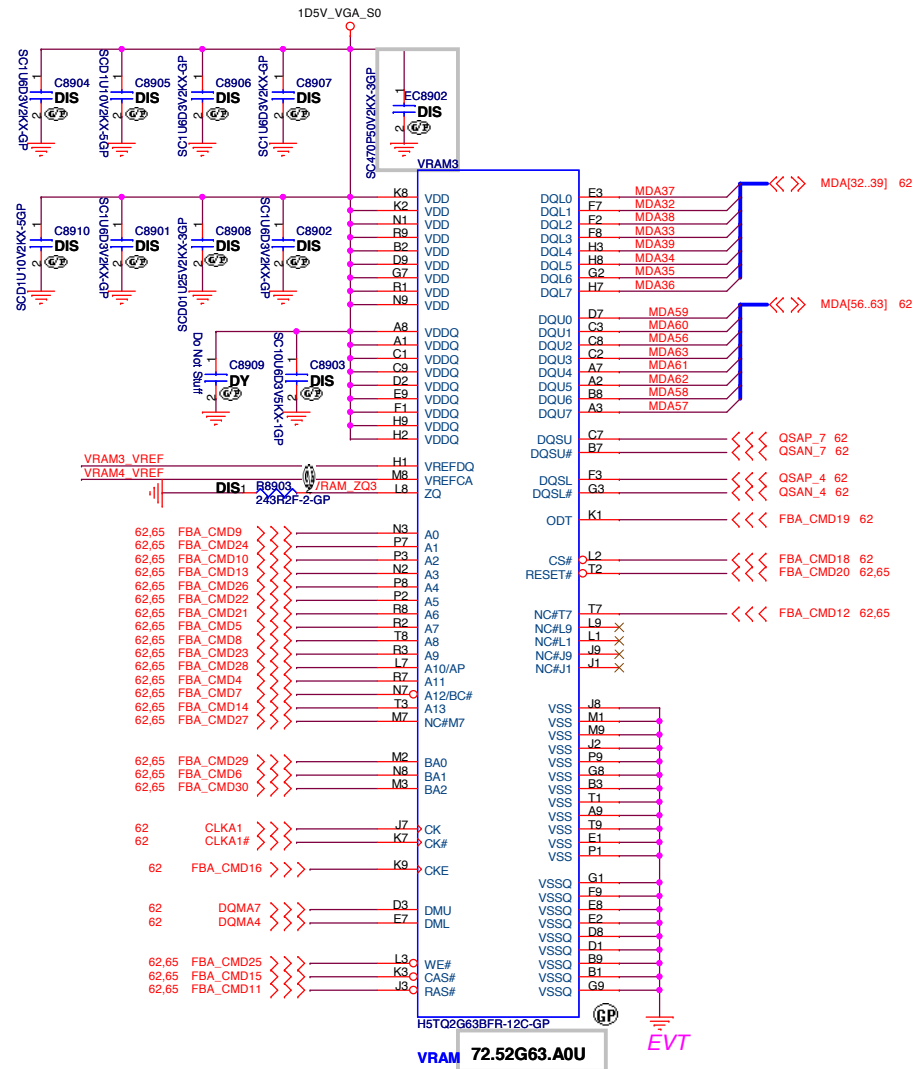
N12M-GE-S-B1-GP



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Title	
GPU GND(5/5)	
Size	Document Number
A3	Z50-HR { Huron River Platform }
Date:	Rev
Wednesday, March 02, 2011	-1
Sheet	of
64	74



- 72.41646.Q0U K4W1G1646G-BC11 Samsung 1Gb
- 72.42164.D0U K4W2G1646C-HC11 Samsung 2Gb
- 72.51G63.H0U H5TQ1G63DFR-11C Hynix 1Gb
- 72.52G63.A0U H5TQ2G63BFR-11C Hynix 2Gb

N12M GS2 HYN1GB

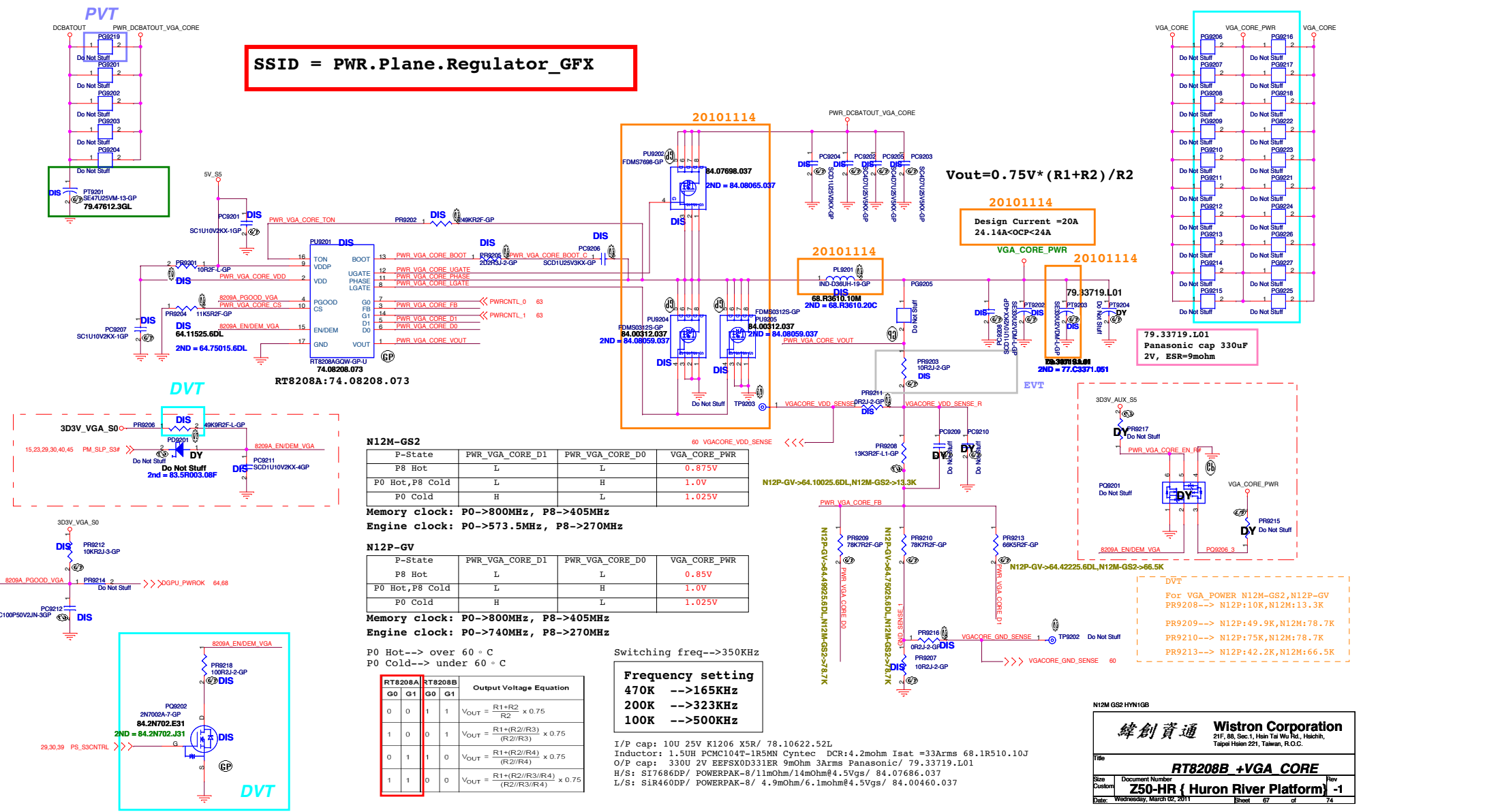
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM3,4 (2/2)**

Size A3 Document Number: **750-HR (Huron River Platform)** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 66 of 74

SSID = PWR.Plane.Regulator_GFX



N12M-GS2

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 Hot	L	L	0.875V
P0 Hot,P8 Cold	L	H	1.0V
P0 Cold	H	L	1.025V

Memory clock: P0->800MHz, P8->405MHz
 Engine clock: P0->573.5MHz, P8->270MHz

N12P-GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 Hot	L	L	0.85V
P0 Hot,P8 Cold	L	H	1.0V
P0 Cold	H	L	1.025V

Memory clock: P0->800MHz, P8->405MHz
 Engine clock: P0->740MHz, P8->270MHz

P0 Hot--> over 60 °C
 P0 Cold--> under 60 °C

Switching freq-->350KHz

Frequency setting
 470K -->165KHz
 200K -->323KHz
 100K -->500KHz

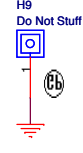
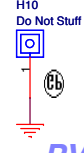
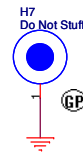
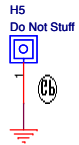
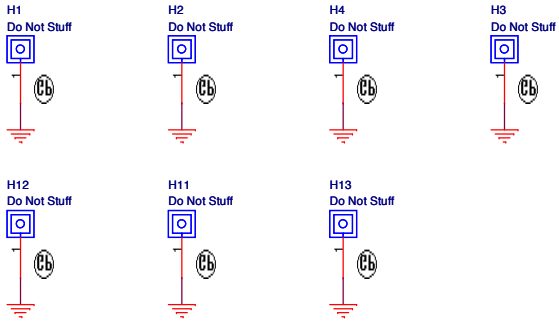
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH PCMC104T-1R5M Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
 O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
 H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

RT8208A	RT8208B	Output Voltage Equation	
G0	G1	G0 G1	
0	0	1 1	$V_{out} = \frac{R1+R2}{R2} \times 0.75$
1	0	0 1	$V_{out} = \frac{R1+(R2/R3)}{R2/R3} \times 0.75$
0	1	1 0	$V_{out} = \frac{R1+(R2/R4)}{R2/R4} \times 0.75$
1	1	0 0	$V_{out} = \frac{R1+(R2/R3/R4)}{(R2/R3/R4)} \times 0.75$

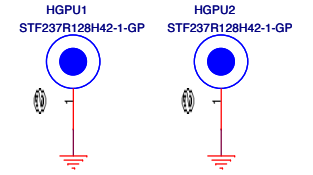
Wistron Corporation
 21F, 6B, Sec.1, Hsin-Tai Wu, Hsueh,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **RT8208B +VGA CORE**

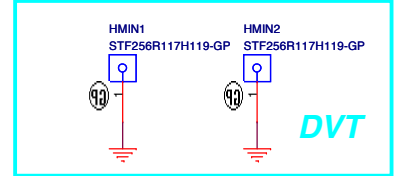
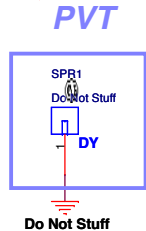
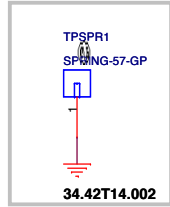
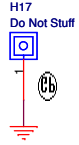
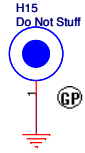
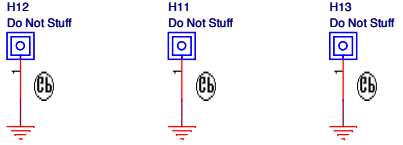
Size: Document Number
 Custom: **Z50-HR { Huron River Platform} -1**
 Date: Wednesday, March 02, 2011 Sheet: 67 of 74



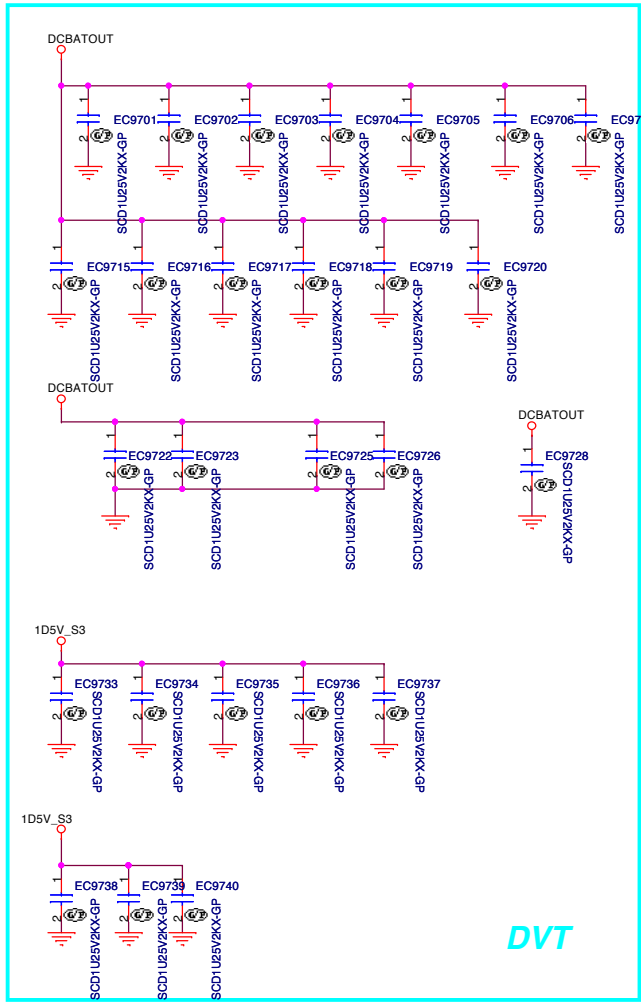
GPU Thermal module hole



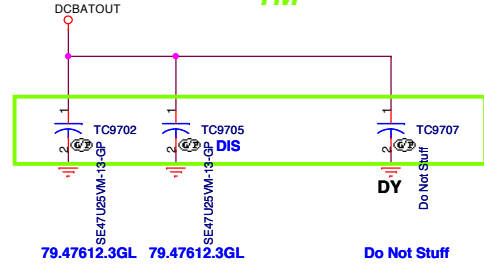
stand off



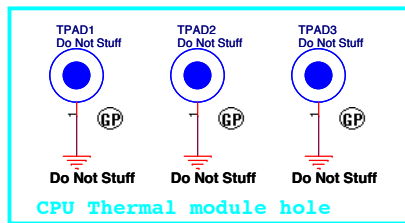
DVT



-1M

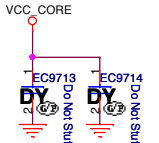
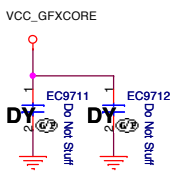
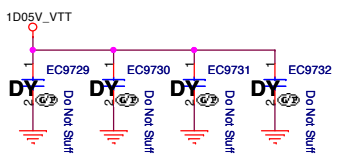
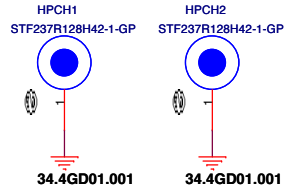


DVT



CPU Thermal module hole

change footprint



Check test point

- 3D3V_S0 1 AFTP1
- 3D3V_AUX_S5 1 AFTP7
- 3D3V_S5 1 AFTP8
- 5V_S5 1 AFTP9
- 15,23 PM_PWRBTN# <<< 1 AFTP10
- 5,18 H_CPOPWRGD >>> 1 AFTP11
- 22,23 S5_ENABLE <<< 1 AFTP12
- 5,14,22,23,26,27,51,55,60 PLT_RST# >>> 1 AFTP13

DVT

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N12M GS2 HYN1GB

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

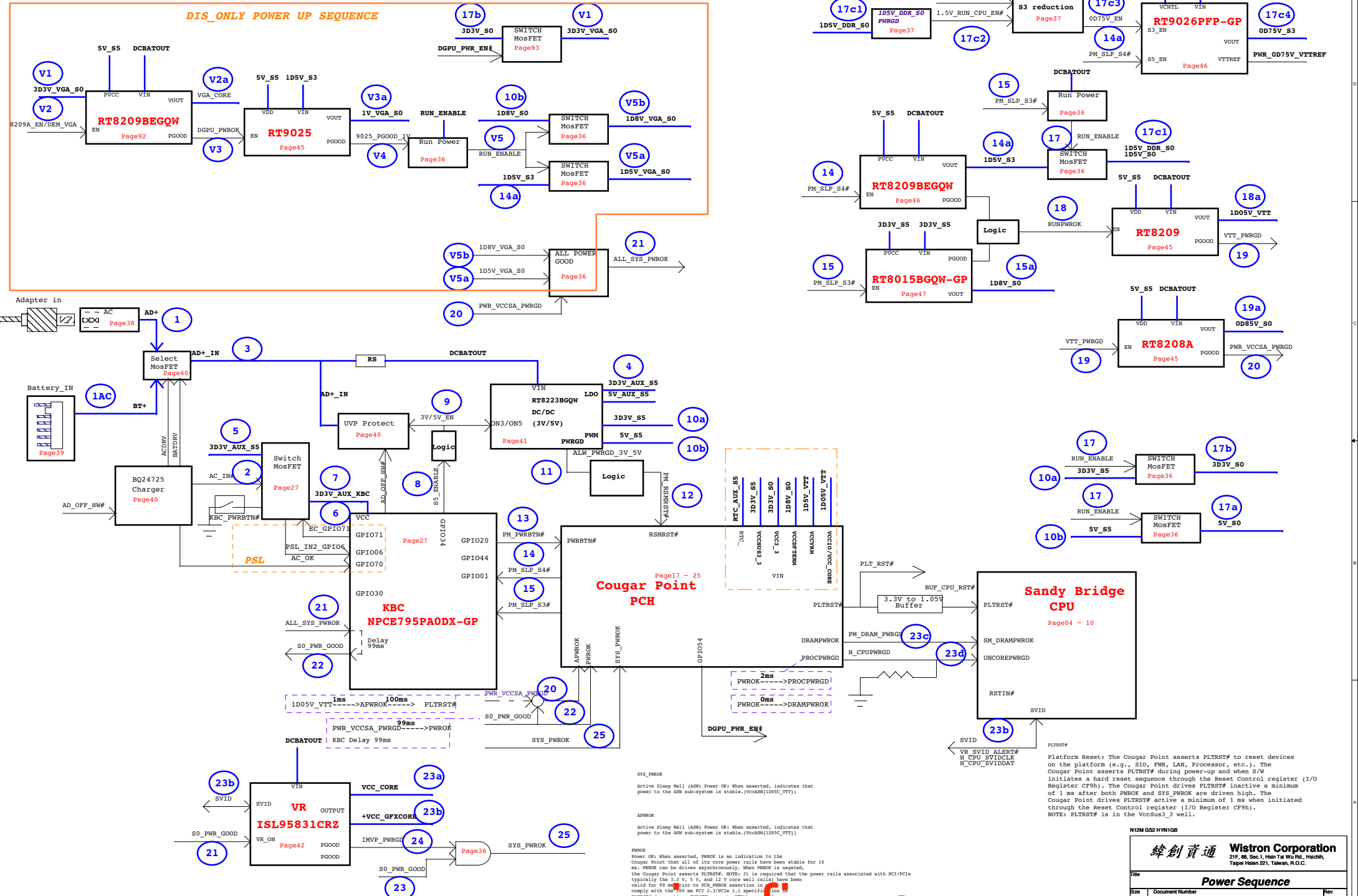
Title: **UNUSED PARTS/EMI Capacitors**

Size A3 Document Number: **Z50-HR { Huron River Platform}** Rev: **-1**

Date: Wednesday, March 02, 2011 Sheet 69 of 74

Z15-HR POWER UP SEQUENCE DIAGRAM

DIS_ONLY POWER UP SEQUENCE



Reversion History

EVT

(2010/09/28)

- P.5 CPU (THERMAL/CLOCK/PM)
- P.7 CPU (RESERVED)
- P.9 CPU (VCC_GFXCORE)
- P.13 PCH (LVDS/CRT/DDI)
- P.14 PCH (PCI/USB/NVRAM)
- P.15 PCH (DM I/FDI/PM)
- P.16 PCH (PCI-E/SMBUS/CLOCK/CL)
- P.17 PCH (SPI/RTC/LPC/SATA/IHDA)
- P.18 PCH (GPIO/CPU)
- P.22 KBC_Reset
- P.23 KBC Nuvoton NPCE795

DUMMY RN501 pull high 1D05V_VTT for intel bebug use
 Delete R706~R709 for no M3 function
 Delete R904,R905,R901 , because R902 has pull low
 Delete LVBS B channel for Z70
 Reserved EC1803 for EMI
 1.DUMMY R1922 ,internal already pull high,2 Del R1925 for intel debug.
 1.Delete RN2017 for no display port,2 R2005 dummy, R2004 mount for PEG_CLKREQ# need pull high
 DEL R2115~R2120,for intel JTAG no use
 Add PCH_GPIO22 for VRAM Frequency 800MHZ ro 900MHZ
 Add VEDS_VEVS_Thermal_System_Protection_Rev1.0.0
 1.ADD GPIO:FAN_PROTECT_DISABLE#,
 2.ADD MODEL_ID for Z40,Z50 model,
 3.ADD R2757 for vendor suggest ,
 4.R2724 CHANGE TO 20K for SB Ver.
 5.ADD BT_PRS2# for BT present.

P.24 Thermal P2800

1.CHANGE FAN PIN DEFINE,2.MOUNT D2802 for Vbemf(back emf),
 3.U2802~U2806 pin4 connector to pin5 pull high follow Thermal_System_Protection_Rev1.0.0

- P.21 Audio Codec_CX20671-21Z
- P.22 Atheros 8151
- P.27 RTS5209 (CARD READER)
- P.28 Audio DE-POP Circuit
- P.29 Power Plane Enable
- P.30 S3 reduction

CHANGE Codec to CX20671
 CHANGE LAN to Atheros 8151
 DUMMY R3202 for use external EEPROM
 Add Q3301,R333 for CODEC multi-function
 Change r3626 to 20k for 3D3V_S3 Leakage

- P.32 BATT CONN
- P.34 CPU Core-1(1SL95831)

1.Del R577 for double pull low,2.Change Q3708_G net to PM_SLP_S3# for Sequence
 3.DUMMY R3724 mount Q3712,R3726,R3722,R3723,Q3707,C3706 for 0D75_EN timing.
 1.ADD D3906 for battery Protection,2.MOUNT D3901~D3905 for EMI
 1.ADD PR4231,PC4233,PR4236,PC4234,MOUNT PR4221,PR4222,PR4420 ,Intel spec update for feedback compensat.
 2.mount PR4221,PR4222,PR4420,PR4233~PR4235 for sensor MOS temperature.

- P.42 [LCD Connector]
- P.44 [HDMI Level Shifter/Conn]
- P.45 [HDD/ODD]
- P.46 [Audio Jack]
- P.47 [LAN Connector]
- P.51 [MINICARD]
- P.52 [LED Board/Power Button]
- P.52 [LED Board/Power Button]
- P.52 [Key Board/Touch Pad]

Change LCD1 to 30pin and pin define
 Add TR4901 for EMI
 F5101 change to 69.4R500.151 POLYSWITCH
 Change R5601 to 147K for delay timing
 Add SPKR1 small board move to MB
 R5808 and R5809 change to 3.0K for Conexant FAE suggestion
 XF1 change to 68.89246.301 common part
 Add WLAN/BT COMBO function

- P.55 [Debug connector]
- P.58 [UVP Protect]
- P.58 [UVP Protect]
- P.58 [UVP Protect]
- P.59 [IO Board Connector]
- P.59 [IO Board Connector]
- P.59 [IO Board Connector]
- P.59 [IO Board Connector]

1.PWRLED1 change to 83.00195.N70 for green color
 Add WLAN/BT COMBO LED signal pin
 Delete Q86 and Q85 for function board no PWR/STDBY LED
 Add EC6905 and EC6906 for EMI
 Add DB1 for SW debug
 Change net from UL_AD_OFF_4 to UL_AD_OFF_41 net name wrong
 RN67 separate to R7816 1Mohm and R7817 80Kohm for change shutdown voltage detect
 Add C7801 10UF/25V for change shutdown voltage detect
 USBCN2 change to 26pin for USB board add G709 thermal sensor
 Add F8201, F8202 and F8203 POLYSWITCH for comtmer request
 Add TR8201, TR8202 and TR8203 for EMI
 PWRCN1 change to 10pin for function board no SPKR1 and PWR/STDBY LED

- P.61 [GPU HDMI/LVDS/CRT(2/5)]
- P.61 [GPU HDMI/LVDS/CRT(2/5)]
- P.63 [GPU_GPIO/MIC(4/5)]
- P.63 [GPU_GPIO/MIC(4/5)]
- P.67 [RT8208B_+VGA_CORE]
- P.69 [UNUSED PARTS/EMI Capacitors]
- P.69 [UNUSED PARTS/EMI Capacitors]

Add LDO 3D3V_VGA_S0_DACA power for INCREASE POWER
 Mount R8402 BOM error because HDMI no display
 R8630 change to 45K for N12P-GV Device ID 0x107F
 R8627 change to 45K for Samsung VRAM 2Gbit size
 Add PU9205 low-side mosfet for N12P-GV NVVDD 20.02A
 Add TPSPR1 for EMI
 Mount EC9740 for EMI

- (2010/09/29)
- P.15 PCH (DMI/FDI/PM)

Add U1901, D1901, D1902, C1901, R1929~R1931 for RSMRST#. PWROK must be "low" earlier than PCH power down. D2603 change to 83.R5003.C8F

- P.22 KBC_Reset
- P.60 [RTC Connector]
- P.11(DDR3-SODIMM1)
- P.12 (DDR3-SODIMM2)
- P.31 DCIN JACK

D6001 change to 83.BAS70.011 for customer request
 Del R1401 for use DDR_VREF_S3 POWER
 Del R1501 for use DDR_VREF_S3 POWER
 Change D3801(TVS) for surge voltage

- (2010/09/30)
- P.29 Power Plane Enable
- P.25 Audio Codec_CX20671-21Z
- P.67 [RT8208B_+VGA_CORE]
- P.68 [DISCRETE VGA POWER]

Add D3603 for protect FET AO4468
 Add C2905, C2925 and R2923(DY), R2924(DY) for vendor request
 PR9203 change to 10R, PR9208 change to 15K for VGA_CORE keep 0.9V
 R9302 change to 20K for 1D05V_VTT enable timing

- (2010/10/01)
- P.20 [PCH (POWER2)]
- P.22 [KBC_Reset]
- P.24 Thermal P8200
- P.25 Audio Codec_CX20671-21Z
- P.28 Audio DE-POP Circuit

D2401, D2402 change to 83.R2004.B8F for common part
 Q2602 change to 84.02222.V11, Q2601 change to 84.C3906.A11 for common part
 Q2801 change to 84.03904.X11 for common part
 D2901, D2902 change to 83.R2004.B8F for common part
 Q19 change to 84.C3906.A11, Q20 change to 84.03904.X11
 Q18 change to 84.09114.A11, Q25 change to 84.C3906.A11 for common part
 Q3707 change to 84.03904.X11, U3702 change to 73.01G09.0AB for common part
 D3908 change to 83.00016.F11 for common part
 U6001 change to 72.25320.C01 for common part
 U6301 change to 74.07534.A7F, U6302 change to 73.01G08.EHG for common part
 X8601 change to 82.30034.641 for common part

- P.30 S3 reduction
- P.32 BATT CONN
- P.48 Flash(KBC+PCH)
- P.50 BLUETOOTH
- P.63 [GPU_GPIO/MIC(4/5)]

Mount R1920, GPIO pin need to Pull Hi for PCH GPIO multi-function
 Add R3209~R3211,C3212~C3214 for customer request
 D3604 change to schottky for customer request
 PD4002 change to 83.10004.08M for common part
 Change R6505 to 0805 size for meet PCIE MINI card max power spec
 Mount R3704,Q3702 for Huron River S3 reduction Desing Guide

- (2010/10/04)
- P.15 PCH (DMI/FDI/PM)
- P.27 RTS5209 (CARD READER)
- P.29 Power Plane Enable
- P.33 CHARGER BQ24725
- P.51 [MINICARD]
- P.30 S3 reduction

ADD corner test point for CPU
 ADD corner test point for PCH
 ADD PU4006,PR4017,PR4018,PQ4001
 ADD PU4006,PR4017,PR4018,PQ4001
 (Q56 pin D connect to AD+)
 (R9316 pin 1 connect to AD+)
 add R9320 and DUMMY it. (Part number 64.10045.6DL)
 connect R9320 pin 1 to ACP_UVP.
 change C568 to the part number 78.10620.51L
 add C9322 component.(part number 78.10620.51L)
 HDMI CONN pin17 connect to GND
 PR9208 change to 17.8k
 P8603 change to 15k
 R8617 DUMMY, R8625 PU 10K for vendor suggest

- (2010/10/05)
- P.7 CPU (RESERVED)
- P.18 PCH (GPIO/CPU)
- P.33 CHARGER BQ24725
- P.57 [UVP Protect]
- P.58 [UVP Protect]

ADD F6101 POLYSWISH 2A for USB power
 Change net name from "+3VS_+1.5VS_HDA_IO" to "+3VS_HDA_IO"
 Del HDMI Level Shifter

- P.44 [HDMI Level Shifter/Conn]
- P.67 [RT8208B_+VGA_CORE]
- P.63 [GPU_GPIO/MIC(4/5)]
- P.63 [GPU_GPIO/MIC(4/5)]

- (2010/10/07)
- P.49 USB Power SW
- P.17 PCH /P.24
- P.44 [HDMI Level Shifter/Conn]

Change net name from "+3VS_+1.5VS_HDA_IO" to "+3VS_HDA_IO"
 Del HDMI Level Shifter

- (2010/10/14)
- P.18 PCH (GPIO/CPU)

R2204 BOM change to 390ohm for intel spec

N12M GS2 HYN1GB

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Title: **Change History**

Size: Custom
 Document Number: **750-HR (Huron River Platform)**
 Date: Wednesday, March 02, 2011
 Sheet: 71 of 74
 Rev: -1

Reversion History

DVT

(2010/11/16~2010/11/17)

P17--C2101, C2102 change to 6pF
Reason: Crystal vendor suggestion (32.768K)
Possible Risk: Rework OK

P17--Add R2126 ~ R2130 and C2105~C2110
Reason: Reserver for LPC debug by EC VEVS
Possible Risk:

P18--DUMMY R2204
Reason: For customer request THERMTRIP# Shutdown Policy
Possible Risk: Rework OK

P22--R2604 stuff to IMVP_PWRGD, Q2602 change to 2N7002
Reason: For customer request THERMTRIP# Shutdown Policy
Possible Risk: Rework OK

P23--BT_PRS# add R2729 pull-up to 3D3V_S5
Reason: The VEVS request BT_PRS# signal be high when Module is not present so we add it.
Possible Risk:We already rework to finish BT VEVS report.

P23-- R2724 change to 33K
Reason: For SC version
Possible Risk:

P23--PCH_SML1_CLK,PCH_SML1_DATA Change power source to 3D3V_S5
Reason: If PH 3D3V_AUX_S5. When DC mode will cause leakage Problem
Possible Risk: Rework OK.

P24-- Add C2803=0.1uF
Reason: 5V has drop when fan power on so add a cap for soft start
Possible Risk: Rework OK.

P25--Stuff EC2901,EC2902
Reason:FOR EMI request
Possible Risk:

P25--DUMMY R2919 ,stuff R2922
Reason: "codec verb table" set mute functio is high active so we change it..
Possible Risk: Rework OK.

P26--DUMMY Q3101 R3104,R3110,ADD R3112,R3111
Reason:LAN_CLK_REQ# and PCIE_WAKE# no leakage on S3.
Possible Risk: Rework OK.

P26--Change C3126, C3127 to 18pF
Reason: Crystal vendor suggestion (25MHz for LAN)
Possible Risk: Rework OK.

P27--Dummy U3202, mount R3202
Reason: Use card reader IC internal EFUSE
Possible Risk: Rework OK

P29--R3626 change to 0ohm
Reason:First we use resistor to do voltage divider for protecting U3601 (let gate voltage < spec) but it is not safty so we add Zener diode D3603 to protect U3601.So Voltage divider do not need.
Possible Risk: Rework OK.

P29--Add Q3606, R3608 (DY)
Reason: Reserve 3D3V_S3 discharge circuit
Possible Risk: Rework OK

P30--DUMMY R3714,Q3704
Reason:When enter S3, DDR_VREF_S3 still have power. So it cannot do discharge when enter S3.
Possible Risk:

P30--DUMMY R3727,Q3713 ,replace PM_SLP_S3 net by PS_S3CNTRL .
Reason:PS_S3CNTRL control S3 discharge can instead of R3612,Q3603
Possible Risk:

P30--R3722 change to 10k,R3723 change to 3.3k,C3706 change to 4.7kohm, stuff C3707.
Reason:for S3 resume issue and sequence timing(ID 0547)
Possible Risk:Rework OK.

P32--add EC3901,EC3907,EC3908,EC3909
Reason:for EMI request
Possible Risk:

P43--R5001, R5002, RN5003 change to 4.7K for DIS SKU
R5001, R5002=2.7K, RN5003=2.2K for UMA SKU
Reason: For CRT DDC signal VEVS report
Possible Risk: Rework OK

P44-- R5133,R5134 change 3.3K for UMA sku, 4.7K for DIS SKU
Reason: For HDMI DDC signal VEVS report
Possible Risk: Rework OK

P45--R5601 change to 100k,R5603 change to 220k,C5614,C5604 change to 1u
Reason:for delay HDD power off timing
Possible Risk:Rework OK

P46--R5805,R5806,R5807,R5810,R5811,R5812 change to 11ohm.
Reason:For VEVS audio full scale output vottage(FSOV) report
Possible Risk:Rework OK.

P46--Add EC5804,EC5805,EC5806,EC5807,ED5808,ED5809
Reason:for EMI request (ED is mean diode)
Possible Risk:

P49--Add TR6101
Reason:for EMI request
Possible Risk:Rework OK and USB eye diagram pass.

P56--Add SD DATA, CLK, CMD 47 ohm damping(RN7403,R7401,R7404)
Reason:For cardreader VEVS report overshoot and undershoot
Possible Risk: Rework OK.

P57--RTC_PWR change to RTC_AUX_S5 power
Reason: Unplug AC will auto shut down after Remove RTC battery
Possible Risk: Rework OK

P59--Change USB BD FFC CONN pin define
Reason:del G709 on USB BD then add one usb power and ground pin for USB voltage drop issue. (ID 0583)
Possible Risk:

P62--R8504, R8505 change to 162ohm
Reason: NV FAE suggestion
Possible Risk:

P63--Change GPU GPIO strap pin R8626 to 4.99K, R8619 to 10K, R8629 to 4.99K for N12P-GV, R8629 to 25K for N12M-GS2, Dummy R8630 Dummy R8632, mount R8633~35K
Reason: NV FAE suggestion for GPU HW strap pin
Possible Risk:

P63--R8607 change to 470ohm
Reason: Crystal vendor suggestion (27MHz)
Possible Risk:Rework OK

P63--R8639 change to15K ohm
Reason: Resolve ID 0617 no HDMI audio output
Possible Risk:Rework OK

P67--Change PR9206 to 49.9K; add PR9218,PQ9202 for VGA_CORE discharge circuit.
Reason:For GPU VEVS Sequence Issue (ID 01019)
Possible Risk: Rework ok.

P68--Change R9303 to 0ohm ,R9315 to 2.2K, C9309 to 1uF; Dummy C9304
Reason:For GPU VEVS Sequence Issue (ID 01019)
Possible Risk: Rework ok.

P69--add DCBATOUT and 1D5V_S3 POWER plane capacitance
Reason:For EMI request
Possible Risk:

(2010/11/22)

P18--Delete R2220, R2221
Reason: Only use 900MHz VRAM frequency
Possible Risk: Rework OK

P22--Add Q2610,Q2607,D2606,R2608,R2602,C2602
Reason: For UVP circuit Simplification and Verification by 3V_5V_EN
Possible Risk: Rework OK

P44--add C5103 0.1uF.
Reason: Resolve HDMI DDC/CEC Capacitance fail (Issue ID 1106)
Possible Risk: Rework OK

P69--Add SPR1
Reason: For EMI request
Possible Risk:

(2010/11/24)

P17--Add C2105,C2107 ~ C2110
Reason: Reserver for LPC debug by EC VEVS
Possible Risk:

P19--Add C2324,C2325,L2302,L2303,L2304
Reason: Improve DMI eye diagram
Possible Risk: Under Verify (ZM and ZG-I different)

P48--DelR6004,R6003 change to 1k
Reason: customer request,do not need "RCT_PWR"net
Possible Risk: Rework OK

P60--PEX_SVDD_3V3 power rail from 1.05V change to 3.3V
Reason: NV FAE suggution for N12M-GS2/N12P-GV GPU
Possible Risk:

(2010/11/25)

P9--R906, R907 change to 10ohm
Reason: Customer requirement
Possible Risk:

P24-- Add F2801
Reason: 0.5A POLYSWITCH for FAN by Customer requirement
Possible Risk:

P35--Dummy PR4230, PR4250, PR4228, PR4229
Reason: Customer requirement
Possible Risk:

(2010/11/26)

P32--Change U3901 to R5G05000N753NF
Reason: Battery authentication IC package is shrunk and renamed as R5G05000N753NF.
Possible Risk:

(2010/11/29)

P58--dummy R9320
Reason: customer request
Possible Risk:

P58--R8629 change to 30k for N12M
Reason: N12M GPU change new device ID
Possible Risk:

N12M GS2 HW1GB

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Change History
750-HB (Huron River Platform) -1
Date: Wednesday, March 02, 2011 Sheet 72 of 74

(POWER modify)

P8--R801, R802 change to 10ohm, reserve R804, R805=10ohm
Reason: Vendor suggestion
Possible Risk:

P33--Add PR4019, PR4020
Reason: Vendor TI suggestion reserve
Possible Risk:

P33--PU4001, PU4002, PU4006 change to 84.02657.037
Reason: Low Rds(on), decrease consumption
Possible Risk:

P34--Change PU4101 PU4106 PU4104 PU4105
Reason: Material shortage issue
Possible Risk:

P34--PR4104 change to 95.3K, PR4103 change to 84.5K
Reason: OCP modify
Possible Risk:

P35--Change PR4205 to 2.26K, PR4227 to 3.74K
Reason: Load line
Possible Risk:

P35--Change PR4206 to 21.5K, PC4205 to 0.01uF, PR4218 to 36K
PC4207 to 0.01uF
Reason: Vendor Intersil suggestion for Imon=2.7V
Possible Risk:

P35--Dummy PC4224, PC4209
Reason: FAE suggestion for delay issue
Possible Risk:

P35--Change PR4239 to 1.69K
Reason: For Intel spec increase efficiency
Possible Risk:

P36--Delete PU4308, PU4311, PU4312, PU4314
change PL4303, PL4302 to 68.R3610.10X
Reason: Thermal issue, use low DCR
Possible Risk:

P36--Change PU4308~ PU4315
Reason: Material shortage issue
Possible Risk:

P37--Change PU4401 to 84.07698.037, PU4403 to 84.00308.B03
PL4401 to 68.R3610.10M
Reason: Material shortage issue
Possible Risk:

P37--Change PR4404 to 536ohm
Reason: OCP modify
Possible Risk:

P37--Change PC4405 TO 10K
Reason: Transient
Possible Risk:

P38--Change PR4504 to 93.1K
Reason: OCP modify
Possible Risk:

P38--Change PU4502 to 84.07698.037, PU4503 to 84.00312.037
Reason: Material shortage issue
Possible Risk:

P38--Change PL4501 to 68.R8810.10G
Reason: Increase ripple
Possible Risk:

P39--Change PR4603 to 32.4K
Reason: OCP modify
Possible Risk:

P39--Change PU4602 to 84.07698.037, PU4603 to 84.00312.037
Reason: Material shortage issue
Possible Risk:

P41--Add PG4810, PG4809
Reason: Increase input current
Possible Risk:

P67--Change PU9202, PU9304, PU9205 PL9201
Reason: Material shortage issue
Possible Risk:

P67--Mount PTC9203
Reason: Decrease output ripple
Possible Risk:

P58--Dummy D46
Reason: For UVP circuit by Customer requirement
Possible Risk:

P58--Add Q57
Reason: Prevent battery only, voltage through body diode return back
to adaptor, induce unknow risk
Possible Risk:

P67--Add PG9218~PG9220, PG9222~PG9224
Reason: Increase input current
Possible Risk:

P67--PR9208=13.3k, PR9210=78.7k, PR9209=78.7k, PR9213=66.5K for N12M-GS2
PR9208=10k, PR9210=75k, PR9209=49.9k, PR9213=42.2K for N12P-GV
Reason: Tune GPU P-State voltage
Possible Risk:

(ME Connector change)

1. Mini Card CONN: (MINI1)
Issue: The ANT cable's tube might
has risk to overlap with Low-case's shielding

Action: Changed the CONN height from 8.0 to 5.3mm

2. RTC & SPK & Fan CONN: (RTC1,SPK1,SPKR1,FAN1)
Issue: Follow Sandra's request to
change the terminal with Gold plating

Action: change the CONN's terminal from Tin to Gold terminal

3. ODD & HDD CONN: (ODD1,HDD1)
Issue: Follow WKS's request to change
from SMT to DIP type for prevent Empty solder,
Floating solder Excess solder

Action: Changed the CONN from SMT to DIP type

4. TP Switch: (SWL1,SWR1)
Issue: Issue: Follow WKS's request to change
new Switch for prevent Empty solder,
Floating solder and Excess solder ect.

Action: Changed new switch.

5. WLA: (MINI1)
Issue: Issue: cost too high
Action: Changed size the same new connector.

N12M GS2 HYN1GB

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Change History			
Title	Document Number		Rev
	750-HB (Huron River Platform)		-1
Date:	Wednesday, March 02, 2011	Sheet	73 of 74

Reversion History

PVT

(2010/10/28~2011/01/05)

P63_ Dummy RN8606
Reason: for double pull high
Possible Risk: Rework ok

P30_ Delete R3714,Q3704(Q00008)
Reason:customer request delete S3 error circuit
Possible Risk: Rework ok

P32_change D3908 to Schottky diode(Q-00009)
Reason:customer request
Possible Risk: Rework ok

P58_UVP R9316 change to 475K
Reason: customer request
Possible Risk: Rework ok

(2011/01/11~01/18)

P8_Add R805,R804(Q00002)
Reason: customer request
Possible Risk: Rework ok

P15_G680 reset_change D1901 to schottky diode(Q00003)
Reason: customer request
Possible Risk: Rework ok

P15_ Delete R1928
Reason: Customer request for DeepSleep issue
Possible Risk: Rework ok

P20_ Delete R2415
Reason: Customer request for DeepSleep issue
Possible Risk: Rework ok

P22_R2604 change to 10.5K, R2635 change to 8.87K, Q2602 change to transistor
84.02222.V11, R2612 change to 100K, Mount R2616
Dummy Q2607, R2602, C2602, R2607, C2613, Q2606, R2606,
R2615, C2612, Q2604, RN2605, Q2601, R2613, Q2603,
Add R2619, Q2611, Q2612, D2605, R2611,R2617(Q00004)
Reason: Customer request
Possible Risk: Rework OK

P8, 9, 37_ Add ED801, ED802, ED901, ED902, ED4501, ED4502 Varistor
Reason: EMI request for ESD protect
Possible Risk: Rework OK

P24_ U2801 power plane change to 3D3V_AUX_S5
Dummy R2809, (Q-00035)
Reason: Customer request for Thermal Sensor P2800 Issue
Possible Risk: Rework OK

P24_ R2811&R2812 change to 29.4K, R2810 change to 44.2K
R2824 change to 33.2K, R2833 change to 36.5K(Q-00006)
Reason: Thermal request for G709 temperature protect
Possible Risk: Rework OK

P37_ Mount PR4510, PR4511,PC4510
Reason: Customer request for VCCIO sense function (Q00013)
Possible Risk: Rework OK

P42_ Change LCD1 connector and pin define
Reason: Fool-proof is not good (ME)
Possible Risk:

P44_ Delete U5102~U5105
Reason: Manufacturing request can not co-layer
Possible Risk:

P50_ R6803, R6810 change to 220 ohm
Reason: Adjust LED brightness
Possible Risk: Rework OK

P51_ Delete D6501, R6517, R6516; Add Q6505, Q6506, R6504,R6503
Reason: Manufacturing request can direct use debug card
Possible Risk: Rework OK

P58_ Mount D46 schottky diode(Q00033)
Reason: Customer request
Possible Risk: Rework OK

P68_ R9303 change to 4.7K, R9315 change to 7.5K
C9309 cchange to 0.47uF
Reason: For VEVs report GPU sequence timing
Possible Risk: Rework OK

(2011/01/17~01/25)

P32_ Change BAT1 connector to 20.81602.007
Reason: Solve hitting L-case or battery shutdown issue (ME)
Possible Risk:

P58_ D46 change to Schottky diode 83.R2004.B8F(Q00033)
Reason: Customer request
Possible Risk: Rework OK

P33_ 58_Delete Q57, Add PR4021~PR4023, PQ4008, PQ4009, PQ4011
Reason: Provide DCBATOUT short surge current (power team)
Possible Risk: Rework OK

P9_C901, C903, C904, C905 and C906 change to 22uF
Reason: For GFX power ripple
Possible Risk: Rework OK

P23_R2707 change to 47K
Reason: For UMA 75W setting
Possible Risk:

P23_R2724 change to 47K
Reason: For -1 version
Possible Risk:

P17_R2127~R2130 change to 47 ohm,R2130 change to 0 ohm
C2105, C2107, C2108, C2109 change to 22pF
Reason: For VEVs LPC report
Possible Risk:

P15_ D1901 change to dual schottky , dummy Q1904,
R1911 change to 1K, R1910 change to 10K ,add R1924(Q00003)
Reason: Customer request
Possible Risk: Rework OK

P29_R3619 change to 0 ohm, add R3622=10K
R3623, R3624, R3627, R3628=0 ohm, Dummy C3614
Reason: Customer request
Possible Risk: Rework OK

P25_P28_ 46_Dummy R2922 ,Q17~Q22, R329 R331 , R330, R333,C404,
R5801~R5804, C5801, C5804, C5805, C5806, U5801, U5802(Q00042)
Reason: Customer request for External De-pop Circuit Eliminating Trial
(Q00043)
Possible Risk: Rework OK

P22_ Q2602 change to FET MOS
Reason: Customer request
Possible Risk: Rework OK

P33_ PR4404 change to 715
Reason: For VCC_GFXCORE OCP protect (power team)
Possible Risk:

P36_ PT4301,PT4303,PT4304,PT4305,PT4309, Dummy PT4308
Reason: For CPU transient (power team)
Possible Risk:

P35_ PR4227 change to 3.57K
Reason: For CPU load line (power team)
Possible Risk:

P35_ PR4218 change to 33.2K
Reason: For CPU lmon setting (power team)
Possible Risk:

P37_PR4404 change to 715 ohm
Reason: For 3/5V OCP protect (power team)
Possible Risk: Rework OK

P35_ PR4205 change to 2.74K
Reason: For CPU load line (power team)
Possible Risk: Rework OK

P35_ PR4206 change to 17.8K
Reason: For CPU lmon setting (power team)
Possible Risk: Rework OK

P45_Dummy C5604 ,R5603 change
to 0 ohm,add R5604_7.5 ohm ,change Q5601(Q00011)
Reason: Customer request
Possible Risk: Rework OK

(2011/01/17~01/26)

P22_ R2635 change to 11K
Reason: Customer request
Possible Risk: Rework OK

P39_ PR4603 change to 16.2K
Reason: For 1.5V OCP protect (power team)
Possible Risk: Rework OK

P38_ PR4504 change to 93.1K
Reason: For 1.05V OCP protect (power team)
Possible Risk: Rework OK

P42_ Add EC4901
Reason:LDC connector DCBATOUT (EMI team)
Possible Risk: Rework OK

P58_ Add R496,R505,R499,C569,R495,R500,R518,R511
Reason:UVP protect(Customer request)
Possible Risk:

(2011/01/27)

P15_ DUMMY R1925(SUSPWRDNACK)
Reason:intel HR schematic check list
Possible Risk:Rework OK

P15_ Q1904 change to 84.03k15.A31
Reason:Low VGS
Possible Risk:Rework OK

P58_ Del R496,R505,R499,C569,R495,R500,R518,R511
Dummy:C568, C9322 and D46
Reason:UVP protect(Customer request)
Possible Risk:

P33_ add PC4025,PC4024,PR4207,PR4220,PQ4010,PR4552,PR4026,PQ4015
Reason:UVP protect(Customer request)
Possible Risk:

(2011/01/31)

P38_ Dummy PR4509,PR4506
Reason:For 1.05v VCCIO_SENSE ,dummy 1.05v is better
Possible Risk:Rework OK

(2011/02/08)

P41_ Add PR4808, PR4809, PR4810(DUMMY)
Reason: for intel released
new spec of Celeron and Pentium CPU VCCSA_PWR
Possible Risk:

(2011/02/09)

Add Aluminum Solid Capacitors 2ND source
Reason: Material shortage issue
Possible Risk:

P58_ Add D46
Reason:
Possible Risk:

(2011/02/11)

P25_ Change RN2901 to 22 ohm
Reason: DMIC VEVs report
Possible Risk:

(2011/02/14)

P69_DUMMY SPR1
Reason: factory damage issue
Possible Risk:

P40_change PU4701 new version
Reason: old will EOL
Possible Risk:

P58_ ADD D46,R498 change to 1M ohm
Reason:UVP protect
Possible Risk:Rework ok

P33_ DUMMY PR4026,PQ4015,PR4252,PR4022,PQ4011
Reason:UVP protect
Possible Risk:Rework ok

P25_ Delete EC2901 and EC2902
Reason: For D-MIC record sound quietly
Possible Risk: Rework OK

Reversion History

-1M

(2011/03/02)

P23_R2724 change to 64.9K
Reason: For -1M version
Possible Risk:

MATSUKI capacitance 47U/ 25V change to NCC
Reason:MATSUKI test failure issue
Possible Risk: