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Project Code & Schematics Subject: M790 Main Board 6L

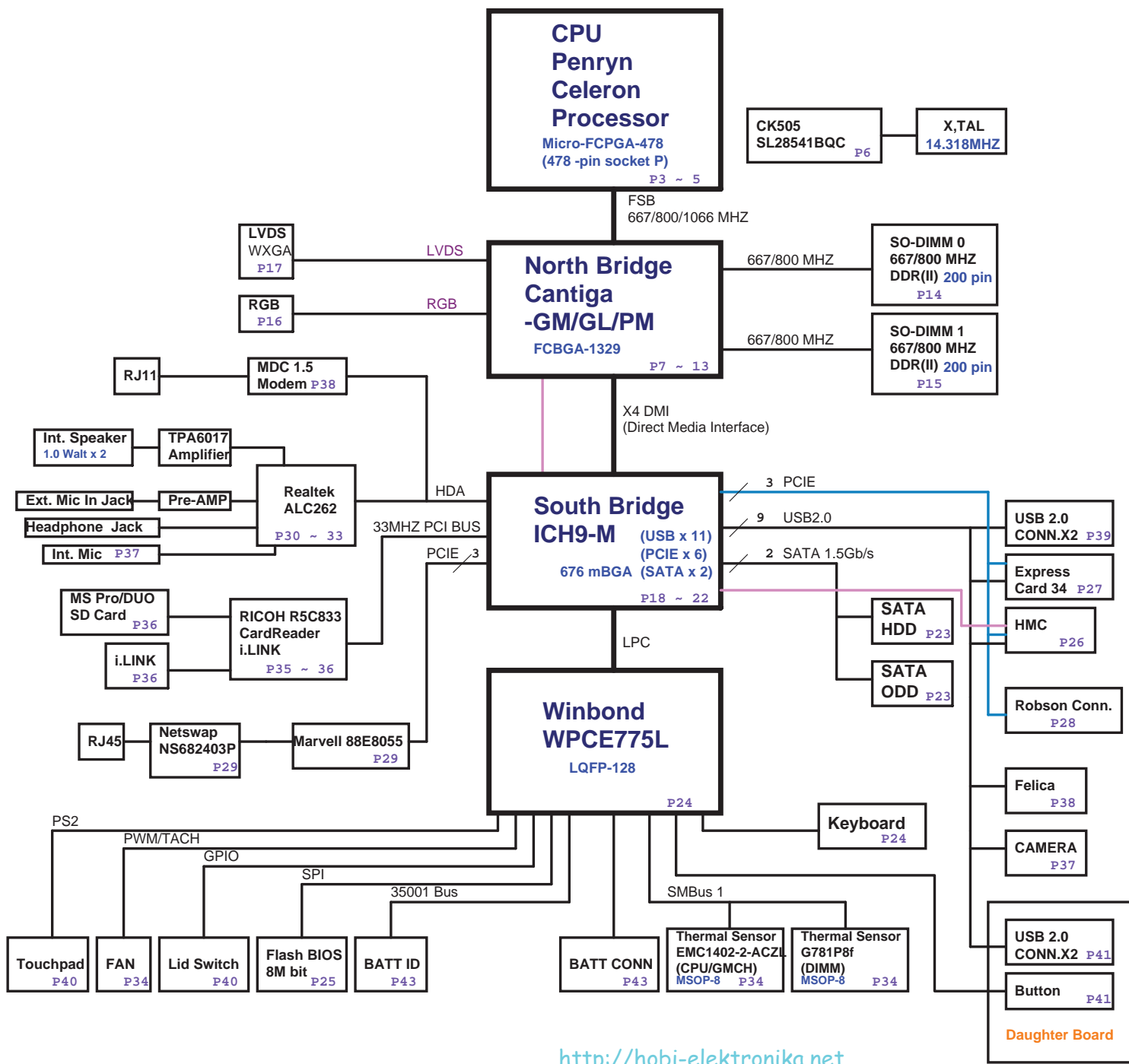
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P/B P/N:	1P-1086J03-6010(IRIS)
R/B P/N:	1P-1086J01-6010(IRIS)

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EC+KBC (WPC8763L)

M790(Montevina)

TI CHARGER BQ24751 P.63	
INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT
SYSTEM DC/DC TPS51125RGER P.64	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW
SYSTEM DC/DC SC411 P.65	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM
SYSTEM DC/DC TPS51116RGER P.66	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS +0_9VSUS
CPU DC/DC ISL6262A P.67	
INPUTS	OUTPUTS
DCBATOUT	VHORE
SYSTEM DC/DC APL5912 P.70	
INPUTS	OUTPUTS
+1_5VRUN	PEX_VDD
SYSTEM DC/DC TPS51117 P.70	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD
SYSTEM DC/DC MAX8776 P.71	
INPUTS	OUTPUTS
DCBATOUT	+VGF_X_CORE



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7 H_AA#[3..35]

7 H_ADSTB#0
7 H_REQ#[4..0]

7 H_ADSTB#1
19 H_A20M#
19 H_FERR#
19 H_IGNNE#
19 H_STPCLK#
19 H_INTR#
19 H_NMI#
19 H_SMI#

TP15 20MIL 1 TP CPU RSVD01 M4
TP18 20MIL 1 TP CPU RSVD02 N5
TP7 20MIL 1 TP CPU RSVD03 T2
TP11 20MIL 1 TP CPU RSVD04 V3
TP5 20MIL 1 TP CPU RSVD05 B2
TP14 20MIL 1 CPU TEST7 C3
TP6 20MIL 1 TP CPU RSVD07 D2
TP25 20MIL 1 TP CPU RSVD08 D22
TP10 20MIL 1 TP CPU RSVD09 D3
TP19 20MIL 1 TP CPU RSVD10 F6

H_A#3 J4
H_A#4 L5
H_A#5 L4
H_A#6 K5
H_A#7 M3
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P2
H_A#12 P2
H_A#13 L2
H_A#14 P4
H_A#15 P1
H_A#16 R1
M1

H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L1
REQ[0]#
REQ[1]#
REQ[2]#
REQ[3]#
REQ[4]#

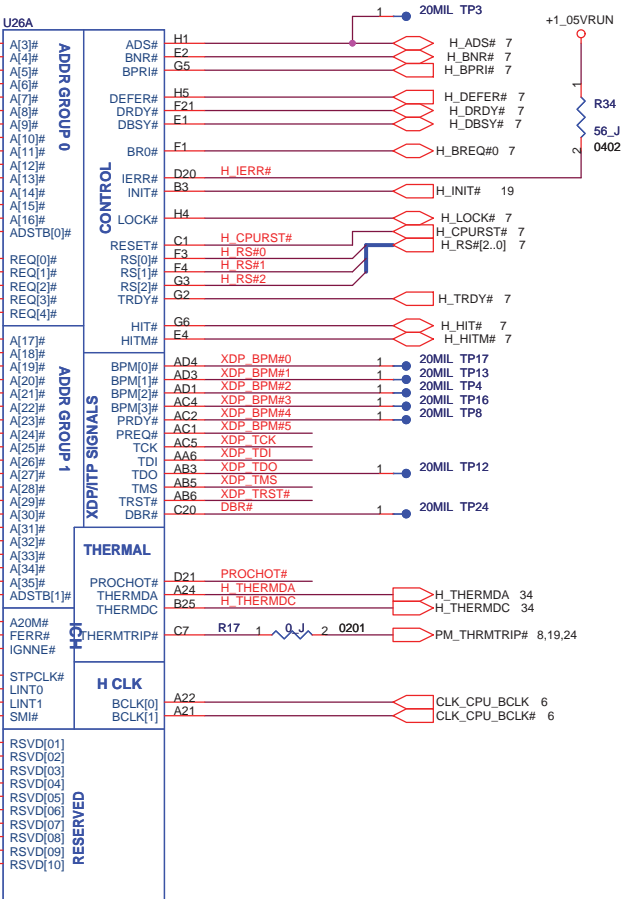
H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U1
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W2
H_A#28 W5
H_A#29 Y4
H_A#30 U2
H_A#31 V4
H_A#32 W3
H_A#33 AA4
H_A#34 AB2
H_A#35 AA3
V1

A6 A20M#
A5 FERR#
C4 IGNNE#
D5 H_STPCLK# R
C6 H_INTR#
B4 H_NMI#
A3 H_SMI#

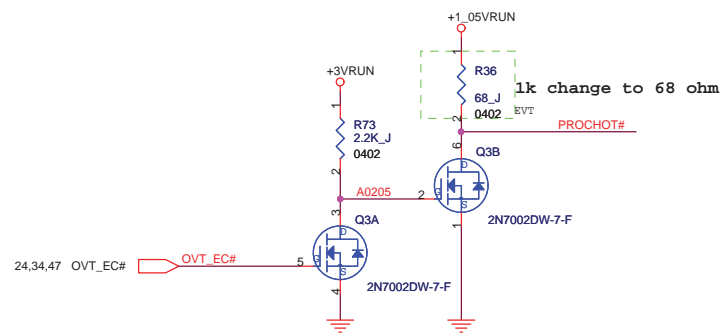
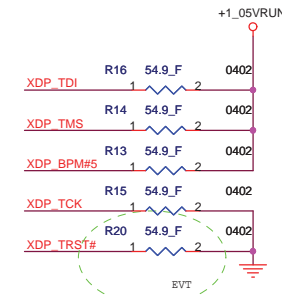
A20M#
FERR#
IGNNE#
H_STPCLK# R
LINT0
LINT1
SMI#

RSVD[0]# M4
RSVD[01]# N5
RSVD[02]# T2
RSVD[03]# V3
RSVD[04]# B2
RSVD[05]# C3
RSVD[06]# D2
RSVD[07]# D22
RSVD[08]# D3
RSVD[09]# F6
RSVD[10]#

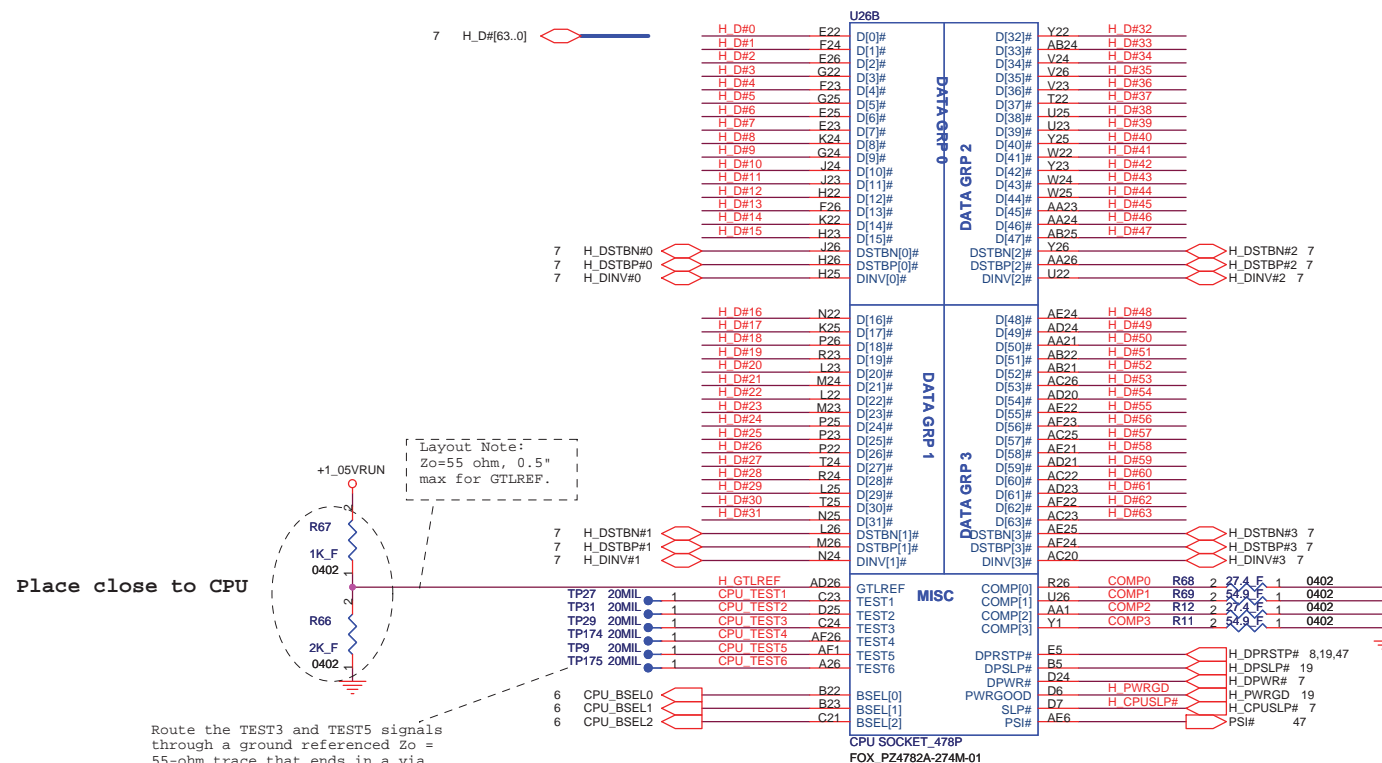
CPU SOCKET_478P
FOX_PZ4782A-274M-01



H_CPURST# 1 20MIL TP2



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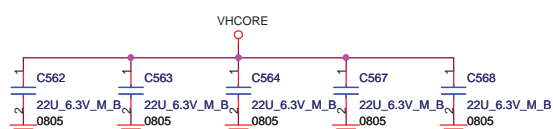
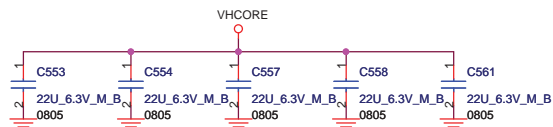
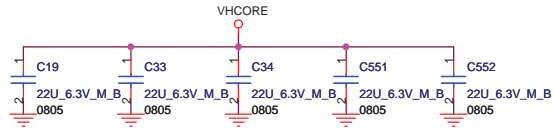
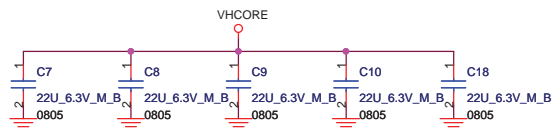


Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

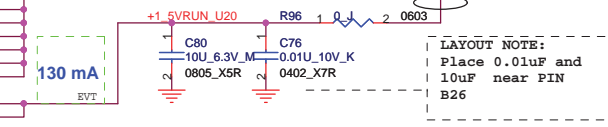
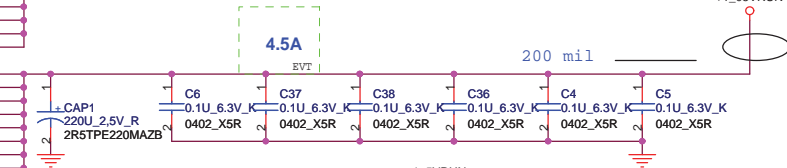
Place close to CPU

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		CCPBG - R&D Division	
Title Penryn (HOST BUS) 2/3			
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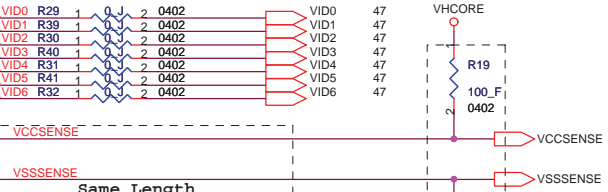


Pin	Signal	Value	Pin	Signal	Value
A7	VCC[001]	VCC[068]	AB20		
A9	VCC[002]	VCC[069]	AB7		
A10	VCC[003]	VCC[070]	AC7		
A12	VCC[004]	VCC[071]	AC9		
A13	VCC[005]	VCC[072]	AC12		
A15	VCC[006]	VCC[073]	AC13		
A17	VCC[007]	VCC[074]	AC15		
A18	VCC[008]	VCC[075]	AC17		
A20	VCC[009]	VCC[076]	AC18		
B7	VCC[010]	VCC[077]	AD7		
B9	VCC[011]	VCC[078]	AD9		
B10	VCC[012]	VCC[079]	AD10		
B12	VCC[013]	VCC[080]	AD12		
B14	VCC[014]	VCC[081]	AD14		
B15	VCC[015]	VCC[082]	AD15		
B17	VCC[016]	VCC[083]	AD17		
B18	VCC[017]	VCC[084]	AD18		
B20	VCC[018]	VCC[085]	AE9		
C9	VCC[019]	VCC[086]	AE10		
C10	VCC[020]	VCC[087]	AE12		
C12	VCC[021]	VCC[088]	AE13		
C13	VCC[022]	VCC[089]	AE15		
C15	VCC[023]	VCC[090]	AE17		
C17	VCC[024]	VCC[091]	AE18		
C18	VCC[025]	VCC[092]	AE20		
D9	VCC[026]	VCC[093]	AF9		
D10	VCC[027]	VCC[094]	AF10		
D12	VCC[028]	VCC[095]	AF12		
D14	VCC[029]	VCC[096]	AF14		
D15	VCC[030]	VCC[097]	AF17		
D17	VCC[031]	VCC[098]	AF18		
D18	VCC[032]	VCC[099]	AF20		
E7	VCC[033]	VCC[100]			
E9	VCC[034]				
E10	VCC[035]	VCCP[01]	G21		
E12	VCC[036]	VCCP[02]	V6		
E13	VCC[037]	VCCP[03]	J6		
E15	VCC[038]	VCCP[04]	K6		
E17	VCC[039]	VCCP[05]	M6		
E18	VCC[040]	VCCP[06]	J21		
E20	VCC[041]	VCCP[07]	K21		
F7	VCC[042]	VCCP[08]	M21		
F9	VCC[043]	VCCP[09]	N21		
F10	VCC[044]	VCCP[10]	N6		
F12	VCC[045]	VCCP[11]	R21		
F14	VCC[046]	VCCP[12]	R6		
F15	VCC[047]	VCCP[13]	T21		
F17	VCC[048]	VCCP[14]	T6		
F18	VCC[049]	VCCP[15]	V21		
F20	VCC[050]	VCCP[16]	W21		
AA7	VCC[051]				
AA9	VCC[052]	VCCA[01]	B26		
AA10	VCC[053]	VCCA[02]	C26		
AA12	VCC[054]				
AA13	VCC[055]				
AA15	VCC[056]				
AA17	VCC[057]				
AA18	VCC[058]				
AA20	VCC[059]				
AB9	VCC[060]				
AC10	VCC[061]				
AB10	VCC[062]				
AB12	VCC[063]				
AB15	VCC[064]				
AB16	VCC[065]				
AB17	VCC[066]				
AB18	VCC[067]				

CPU_VCCA---->0.13A
 CPU_VCCP---->4.5A
 CPU_VCC---->47A



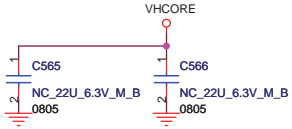
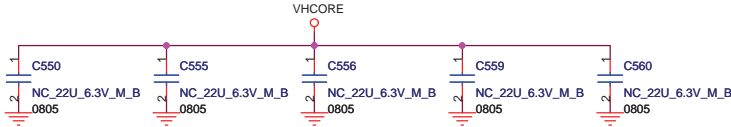
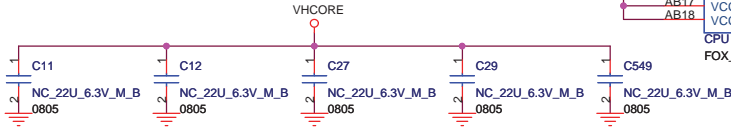
LAYOUT NOTE:
 Place 0.01uF and 10uF near PIN B26

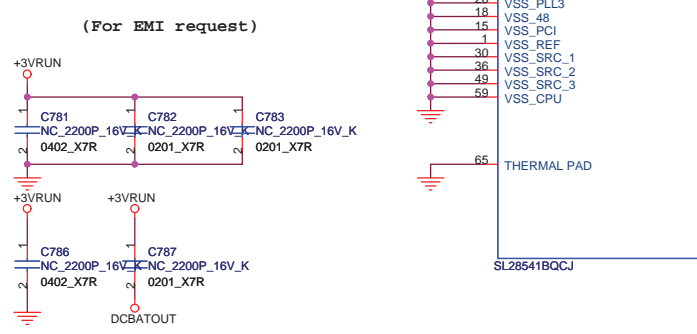
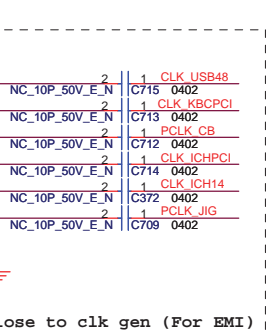
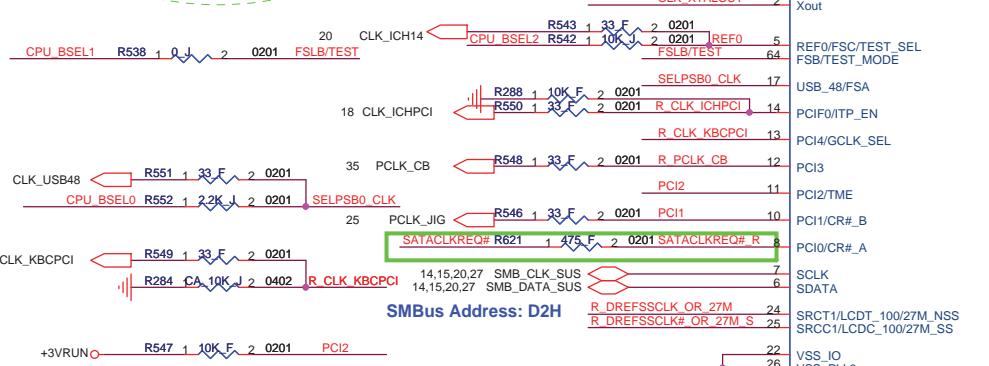
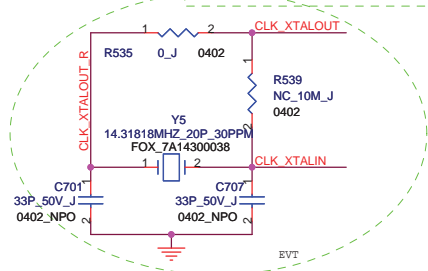
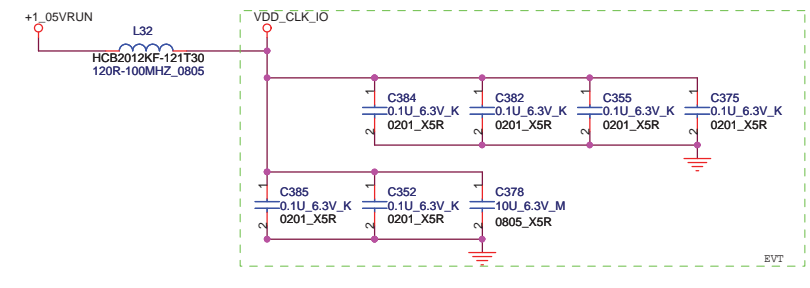
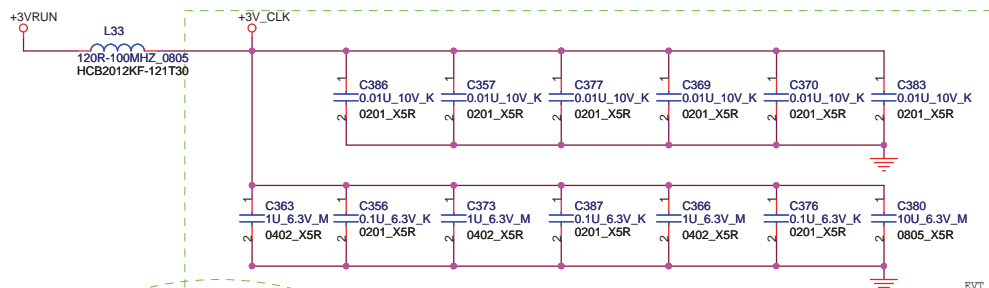


Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.

Outer width=18 mil spacing=7 mil
 Inner width=14 mil spacing=7 mil
 Length match < 25 mil

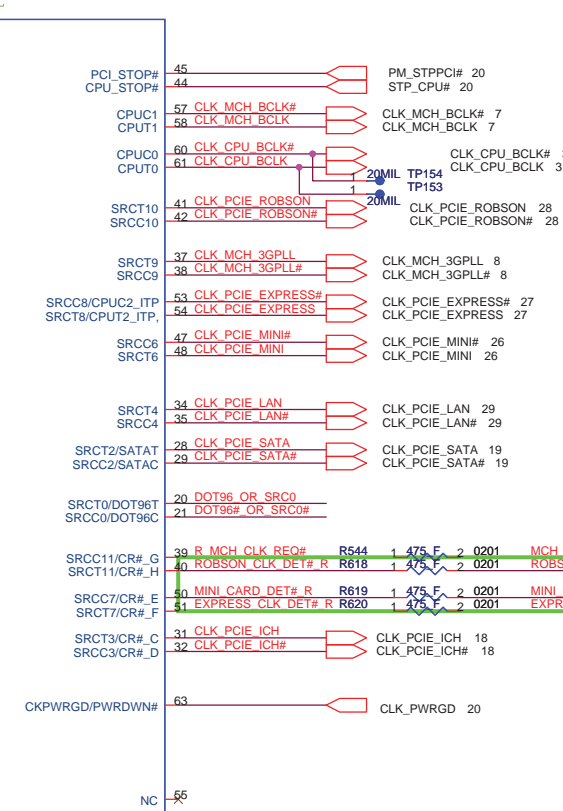
Pin	Signal	Pin	Signal
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V22
C9	VSS[018]	VSS[099]	V25
C14	VSS[019]	VSS[100]	W1
C16	VSS[020]	VSS[101]	W4
C19	VSS[021]	VSS[102]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y6
C25	VSS[025]	VSS[106]	Y21
D1	VSS[026]	VSS[107]	Y24
D4	VSS[027]	VSS[108]	AA2
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D19	VSS[032]	VSS[113]	AA16
D23	VSS[033]	VSS[114]	AA19
D26	VSS[034]	VSS[115]	AA22
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB4
E11	VSS[038]	VSS[119]	AB8
E14	VSS[039]	VSS[120]	AB11
E16	VSS[040]	VSS[121]	AB13
E19	VSS[041]	VSS[122]	AB16
E21	VSS[042]	VSS[123]	AB19
E24	VSS[043]	VSS[124]	AB23
F5	VSS[044]	VSS[125]	AB26
F8	VSS[045]	VSS[126]	AC3
F11	VSS[046]	VSS[127]	AC6
F13	VSS[047]	VSS[128]	AC8
F16	VSS[048]	VSS[129]	AC11
F19	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G1	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD9
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE23
L21	VSS[070]	VSS[151]	AE26
L24	VSS[071]	VSS[152]	A2
M2	VSS[072]	VSS[153]	AF6
M5	VSS[073]	VSS[154]	AF8
M22	VSS[074]	VSS[155]	AF11
M25	VSS[075]	VSS[156]	AF13
N1	VSS[076]	VSS[157]	AF16
N4	VSS[077]	VSS[158]	AF19
N23	VSS[078]	VSS[159]	AF21
N26	VSS[079]	VSS[160]	A25
P3	VSS[080]	VSS[161]	AF25
	VSS[081]	VSS[162]	
	VSS[163]		



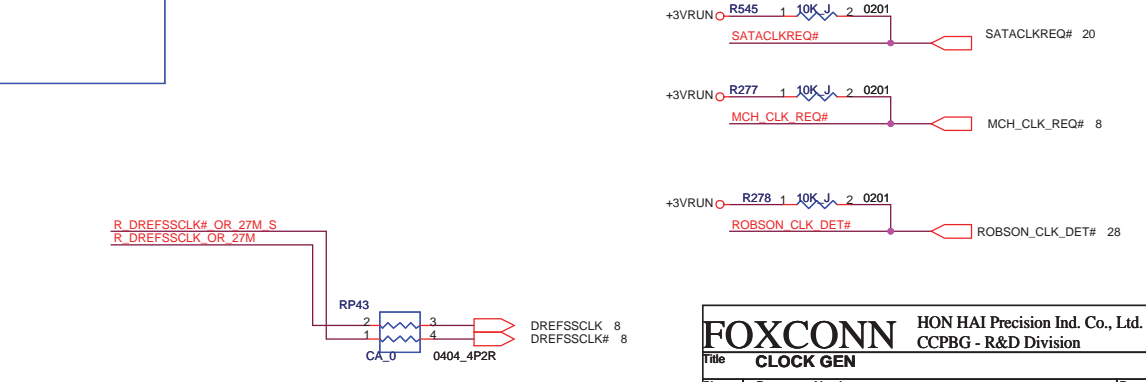
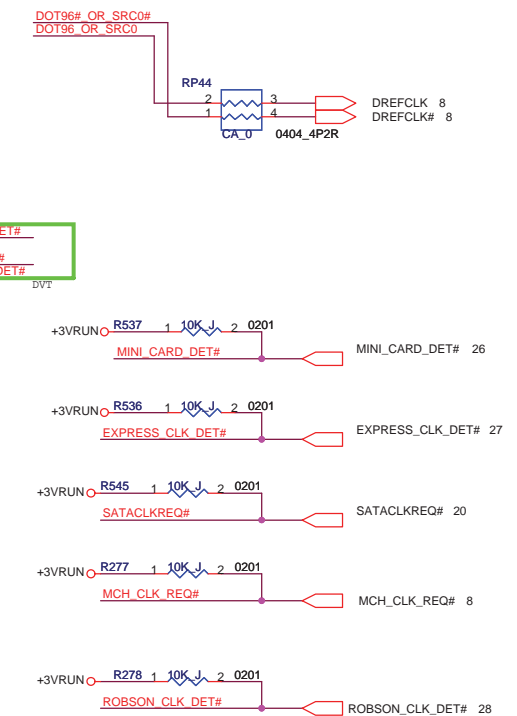


FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33



Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	NC
CR#C	NC
CR#D	NC
CR#E	MINI_CARD_DET#
CR#F	EXPRESS_CLK_DET#
CR#G	MCH_CLK_REQ#
CR#H	ROBSON_CLK_DET#



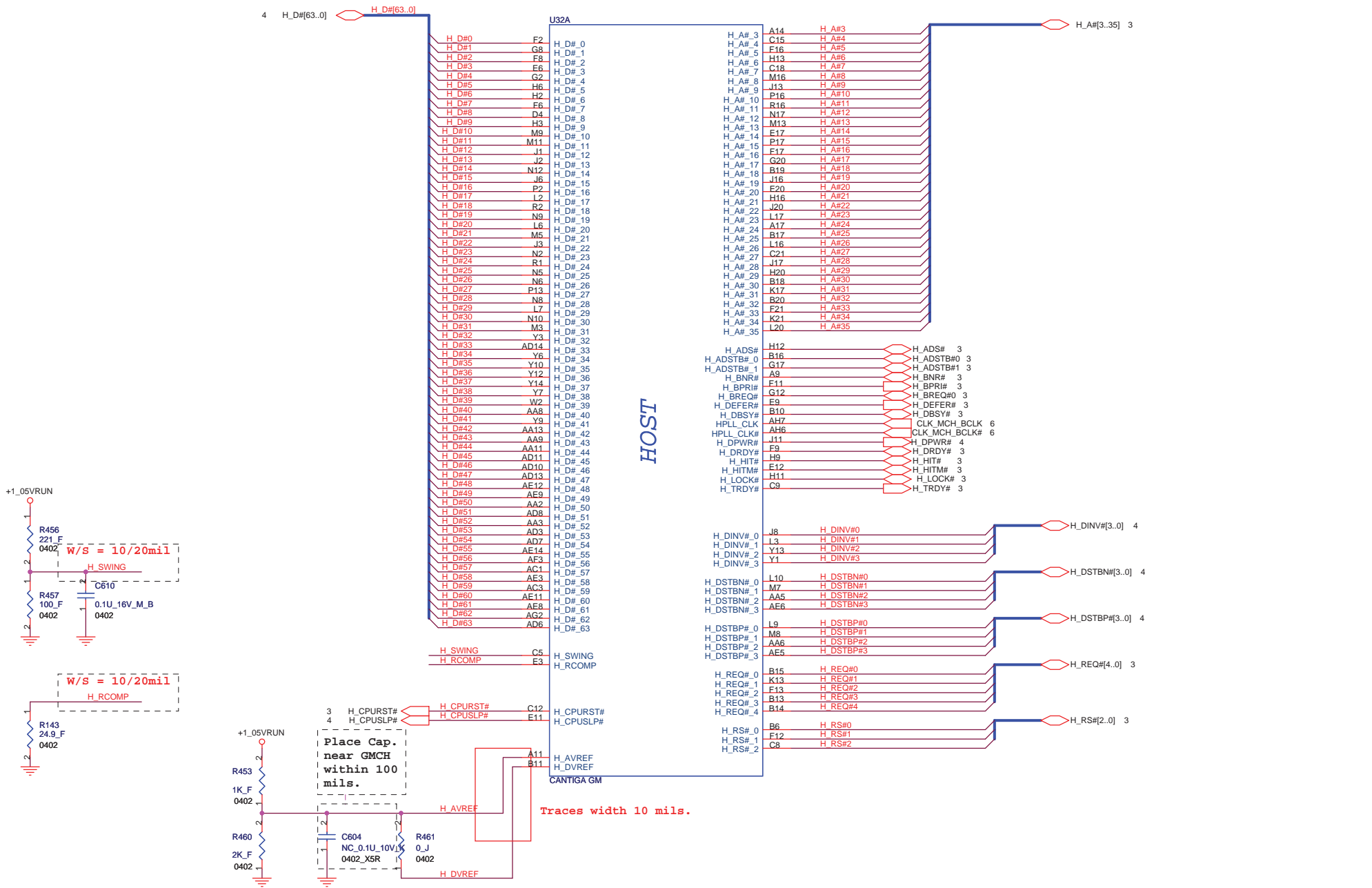
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CCPBG - R&D Division

Title: **CLOCK GEN**

Size: A3 | Document Number: M790-1-01 | Rev: 1.0

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Title Cantiga (HOST) 1/7			
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MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

M36	M36	RESERVED_7
N36	N36	RESERVED_10
R33	R33	RESERVED_12
T33	T33	RESERVED_17
AH9	AH9	RESERVED_17
AH10	AH10	RESERVED_5
AH12	AH12	RESERVED_9
AH13	AH13	RESERVED_8
K12	K12	RESERVED_2
AL34	AL34	RESERVED_18
AK34	AK34	RESERVED_14
AN35	AN35	RESERVED_19
AM35	AM35	RESERVED_13
T24	T24	RESERVED_21
B31	B31	RESERVED_4
B2	B2	RESERVED_3
M1	M1	RESERVED_6
AY21	AY21	RESERVED_1
BG23	BG23	RESERVED_20
BF23	BF23	RESERVED_16
BH18	BH18	RESERVED_22
BF18	BF18	RESERVED_15

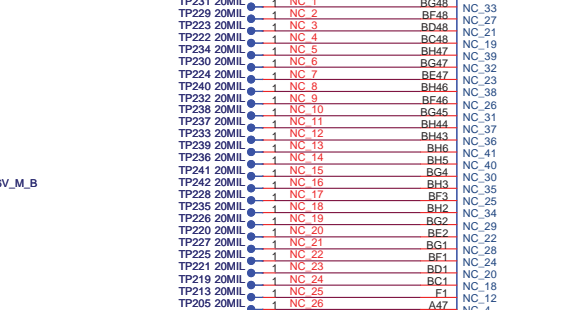
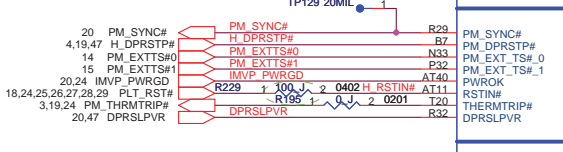
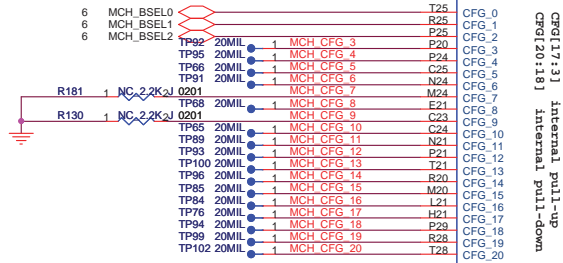
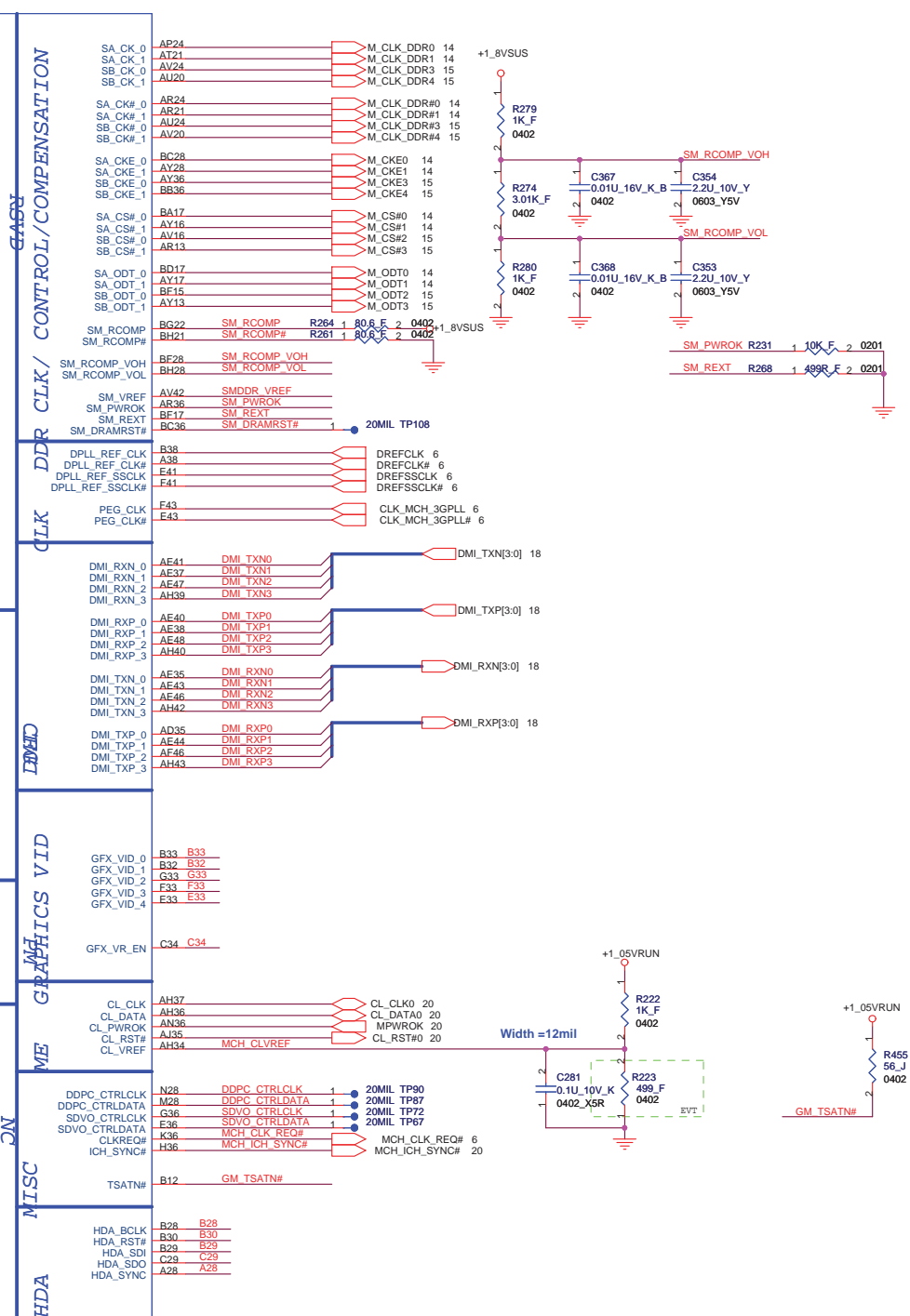
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BF23	BF23	RESERVED_16
BH18	BH18	RESERVED_22
BF18	BF18	RESERVED_15

T25	CFG_0
R25	CFG_1
P25	CFG_2
P20	CFG_3
P24	CFG_4
C25	CFG_5
N24	CFG_6
M24	CFG_7
E21	CFG_8
C23	CFG_9
C24	CFG_10
N21	CFG_11
P21	CFG_12
T21	CFG_13
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M20	CFG_15
H21	CFG_16
H21	CFG_17
P29	CFG_18
R28	CFG_19
T28	CFG_20

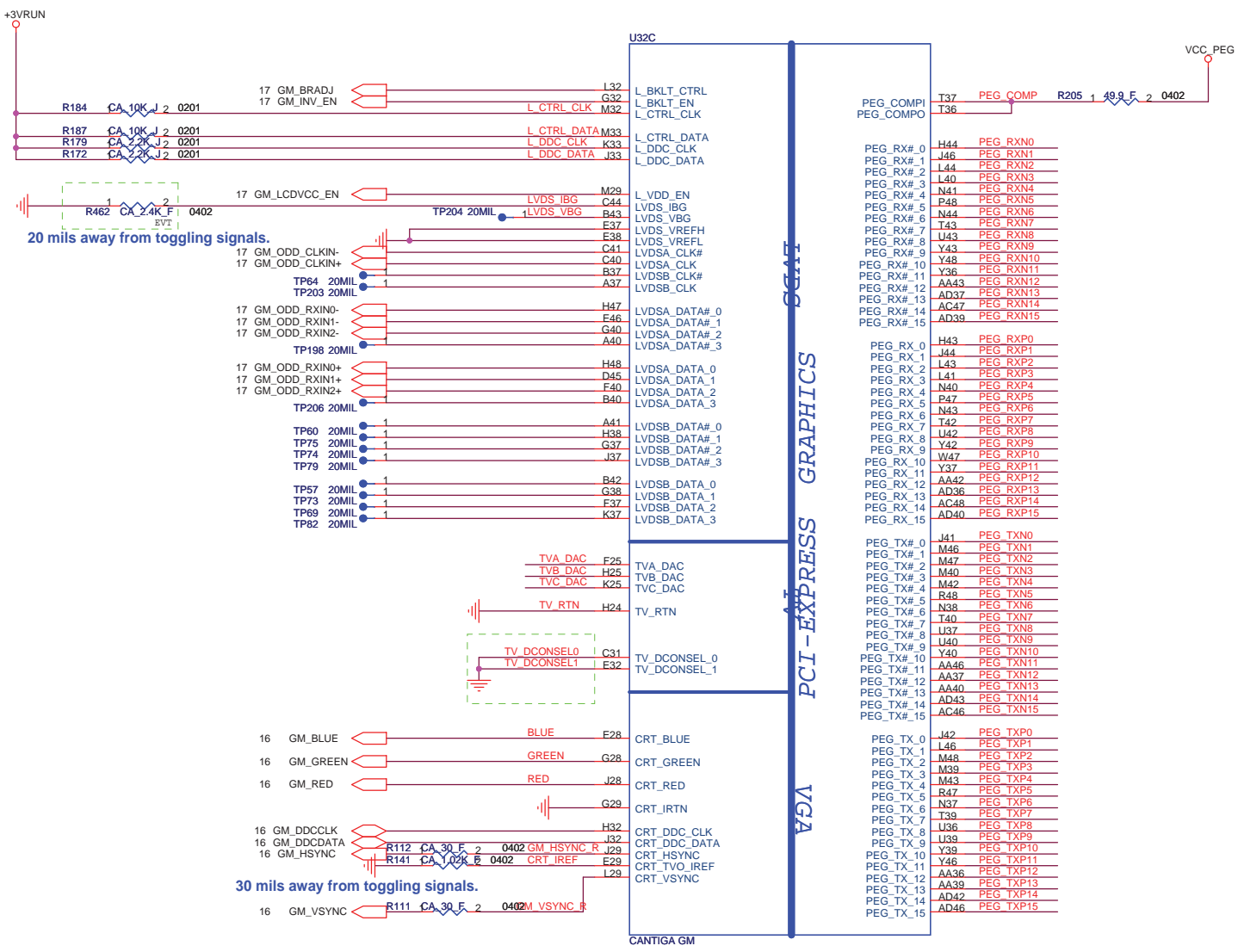
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N33	PM_DPRSTP#
P32	PM_EXT_TSH#_0
AT40	PM_EXT_TSH#_1
T20	PWROK
T20	RSTIN#
T20	THERMTRIP#
R32	DPRSPLVR

BG48	NC_33
BF48	NC_27
BD48	NC_21
BC48	NC_19
BH47	NC_39
BG47	NC_32
BE47	NC_23
BH46	NC_38
BF46	NC_28
BG45	NC_31
BH44	NC_37
BF43	NC_36
BH6	NC_41
BH5	NC_40
BG4	NC_30
BH3	NC_35
BF3	NC_25
BH2	NC_34
BG2	NC_29
BE2	NC_22
BC1	NC_28
BF1	NC_24
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F1	NC_12
A47	NC_4

CANTIGA GM

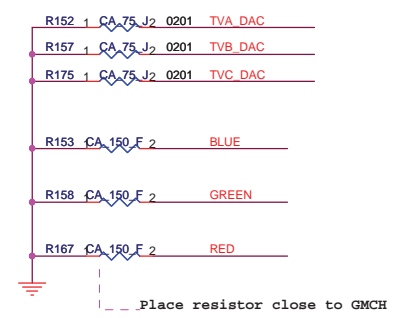


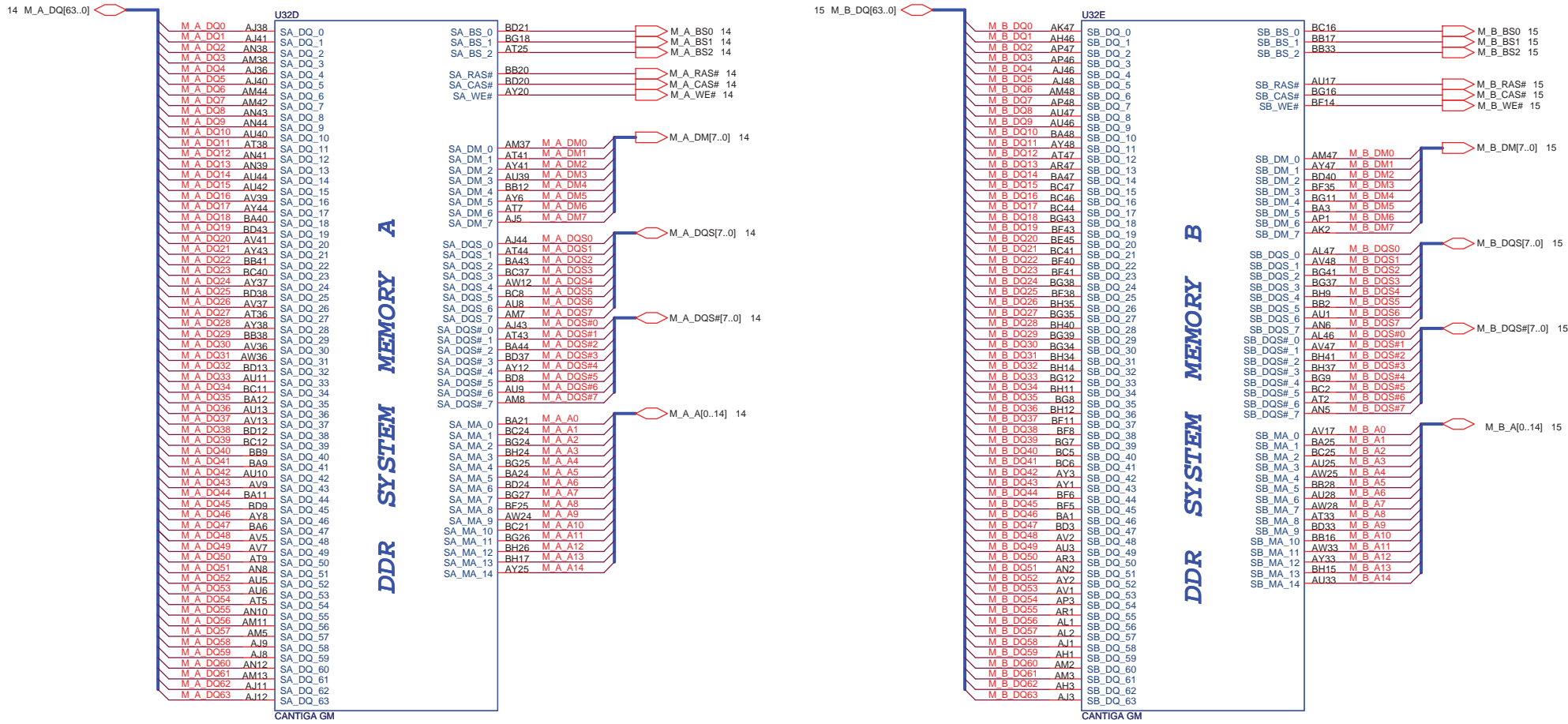
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Cantiga (DMI) 2/7		CCPBG - R&D Division	
Title	Document Number	Rev	
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Custom			
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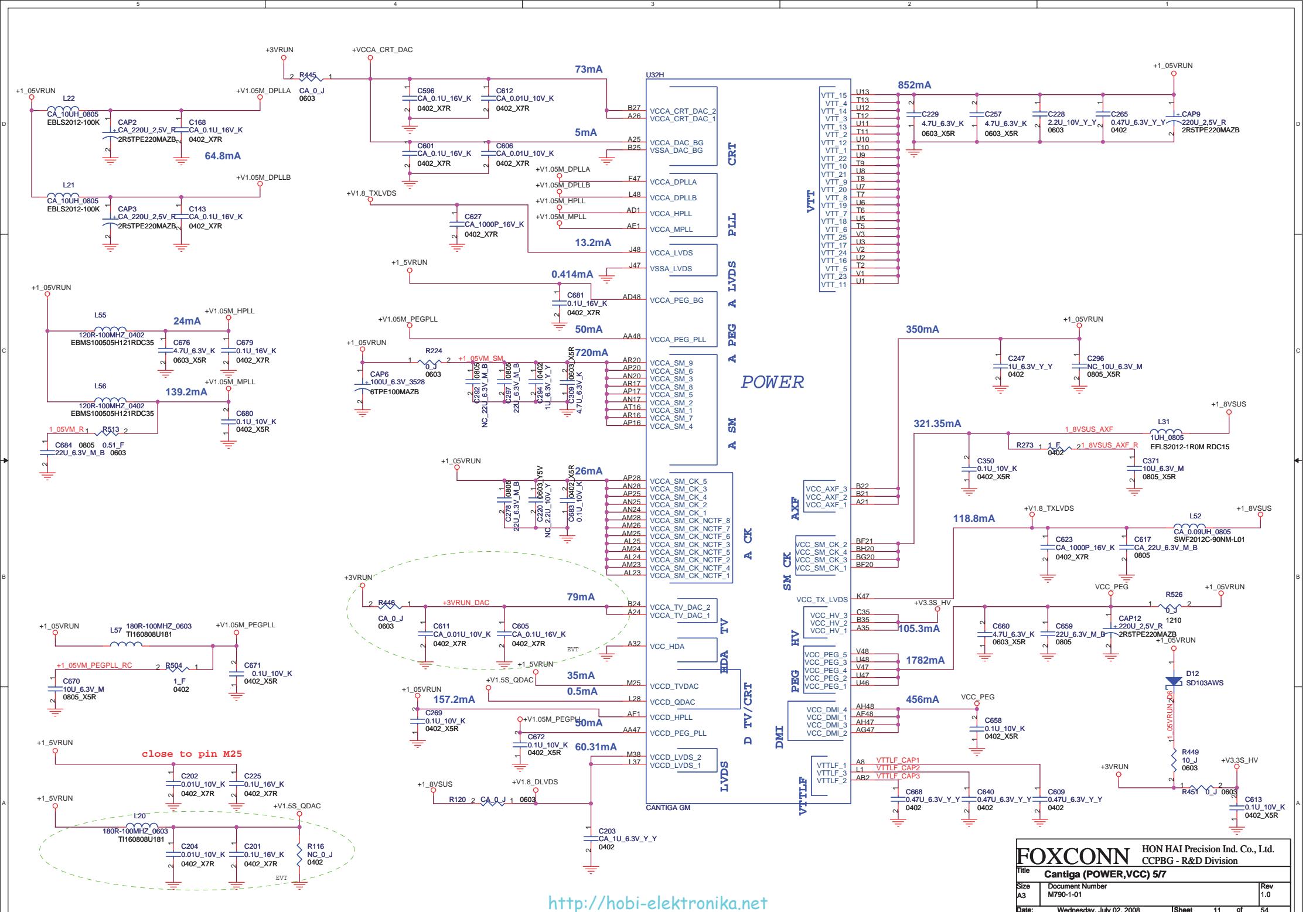


SERIAL
 PCI-EXPRESS
 VGA

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PEG_RX#_3	L40	PEG_RXN3
PEG_RX#_4	N41	PEG_RXN4
PEG_RX#_5	P48	PEG_RXN5
PEG_RX#_6	N44	PEG_RXN6
PEG_RX#_7	T43	PEG_RXN7
PEG_RX#_8	U43	PEG_RXN8
PEG_RX#_9	Y43	PEG_RXN9
PEG_RX#_10	Y48	PEG_RXN10
PEG_RX#_11	Y36	PEG_RXN11
PEG_RX#_12	AA43	PEG_RXN12
PEG_RX#_13	AD37	PEG_RXN13
PEG_RX#_14	AC47	PEG_RXN14
PEG_RX#_15	AD39	PEG_RXN15
PEG_RX#_0	H43	PEG_RXP0
PEG_RX#_1	J44	PEG_RXP1
PEG_RX#_2	L43	PEG_RXP2
PEG_RX#_3	L41	PEG_RXP3
PEG_RX#_4	N40	PEG_RXP4
PEG_RX#_5	P47	PEG_RXP5
PEG_RX#_6	N43	PEG_RXP6
PEG_RX#_7	T42	PEG_RXP7
PEG_RX#_8	U42	PEG_RXP8
PEG_RX#_9	Y42	PEG_RXP9
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PEG_RX#_14	AC48	PEG_RXP14
PEG_RX#_15	AD40	PEG_RXP15
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PEG_TX#_3	M40	PEG_TXN3
PEG_TX#_4	M42	PEG_TXN4
PEG_TX#_5	R48	PEG_TXN5
PEG_TX#_6	N38	PEG_TXN6
PEG_TX#_7	T40	PEG_TXN7
PEG_TX#_8	U37	PEG_TXN8
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PEG_TX#_10	Y40	PEG_TXN10
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PEG_TX#_15	AC46	PEG_TXN15
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PEG_TX#_1	L46	PEG_TXP1
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PEG_TX#_4	M43	PEG_TXP4
PEG_TX#_5	R47	PEG_TXP5
PEG_TX#_6	N37	PEG_TXP6
PEG_TX#_7	T39	PEG_TXP7
PEG_TX#_8	U36	PEG_TXP8
PEG_TX#_9	U39	PEG_TXP9
PEG_TX#_10	Y39	PEG_TXP10
PEG_TX#_11	Y48	PEG_TXP11
PEG_TX#_12	AA36	PEG_TXP12
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PEG_TX#_15	AD46	PEG_TXP15



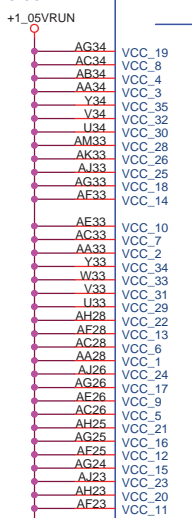




<http://hobi-elektronika.net>

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3.06A



VCC CORE

POWER

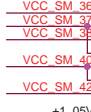
VCC NCTF

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- VCC_NCTF_19 AJ32
- VCC_NCTF_17 AH32
- VCC_NCTF_14 AG32
- VCC_NCTF_10 AE32
- VCC_NCTF_7 AC32
- VCC_NCTF_3 Y32
- VCC_NCTF_41 U32
- VCC_NCTF_33 AL30
- VCC_NCTF_31 AK30
- VCC_NCTF_28 AH30
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- VCC_NCTF_25 AK29
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- VCC_NCTF_1 Y29
- VCC_NCTF_42 W29
- VCC_NCTF_38 V29
- VCC_NCTF_37 U29
- VCC_NCTF_29 AL28
- VCC_NCTF_24 AK28
- VCC_NCTF_28 AH28
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- VCC_NCTF_31 AK30
- VCC_NCTF_28 AH30
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- VCC_NCTF_1 Y28

+1_05VRUN



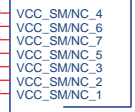
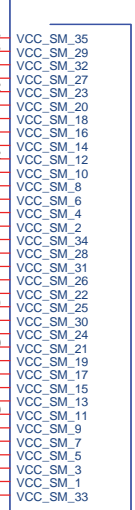
3A +1_8VSUS



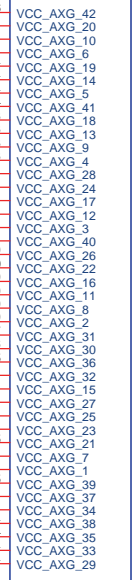
+1_05VRUN



U32G



+1_05VRUN



POWER

VCC GFX NCTF

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- VCC_SM_29
- VCC_SM_32
- VCC_SM_27
- VCC_SM_23
- VCC_SM_20
- VCC_SM_18
- VCC_SM_16
- VCC_SM_14
- VCC_SM_12
- VCC_SM_10
- VCC_SM_8
- VCC_SM_6
- VCC_SM_4
- VCC_SM_2
- VCC_SM_34
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- VCC_SM_26
- VCC_SM_25
- VCC_SM_24
- VCC_SM_21
- VCC_SM_19
- VCC_SM_17
- VCC_SM_15
- VCC_SM_13
- VCC_SM_11
- VCC_SM_9
- VCC_SM_7
- VCC_SM_5
- VCC_SM_3
- VCC_SM_1
- VCC_SM_33
- VCC_SM_36 BA36
- VCC_SM_37 BB24
- VCC_SM_38 BD16
- VCC_SM_40 AW16
- VCC_SM_42 AT13
- VCC_SM/NC_4
- VCC_SM/NC_6
- VCC_SM/NC_7
- VCC_SM/NC_5
- VCC_SM/NC_3
- VCC_SM/NC_2
- VCC_SM/NC_1
- VCC_AXG_42
- VCC_AXG_20
- VCC_AXG_10
- VCC_AXG_6
- VCC_AXG_19
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VCC GFX

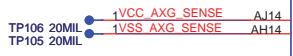
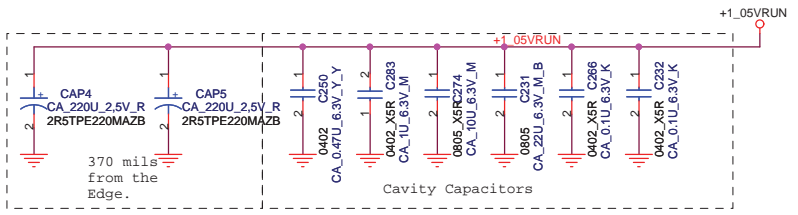
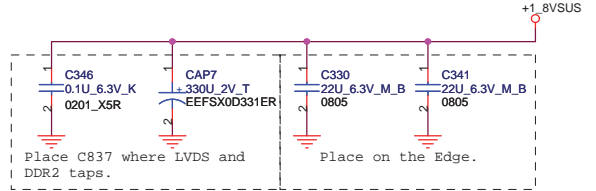
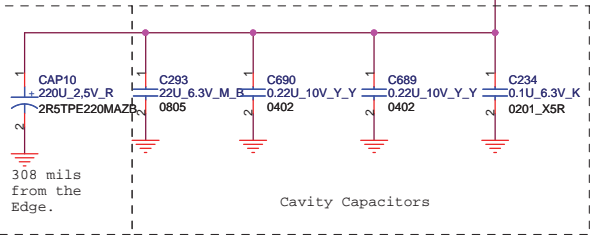
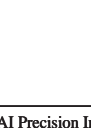
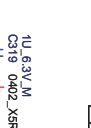
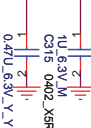
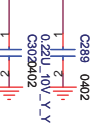
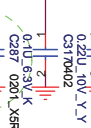
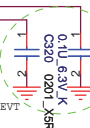
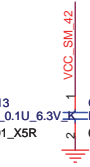
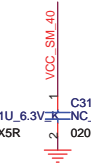
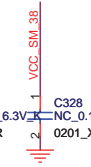
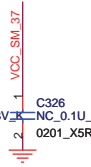
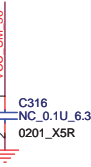
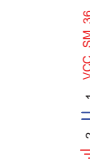
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- VCC_SM_LF_5 AM10
- VCC_SM_LF_6 BB13
- VCC_SM_LF_7 VCC_SM_LF7
- VCC_SM_LF1
- VCC_SM_LF2
- VCC_SM_LF3
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- VCC_SM_LF6
- VCC_SM_LF7



+1_05VRUN



8.7A

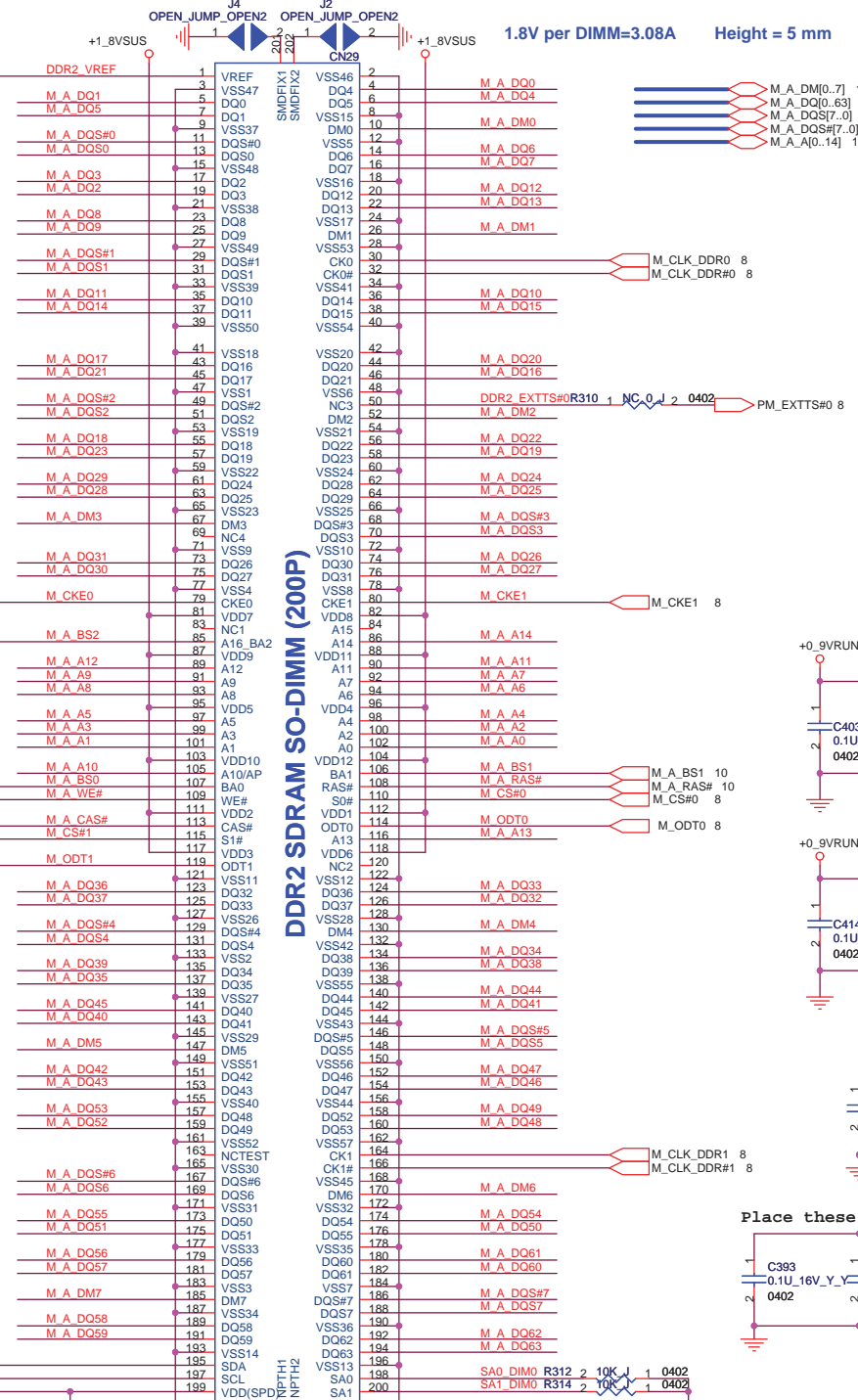
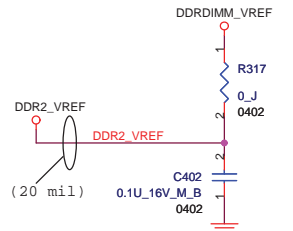


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **Cantiga (VCC CORE) 6/7**

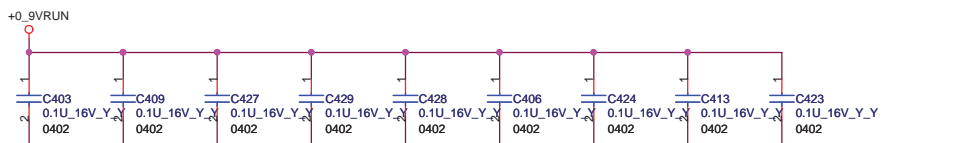
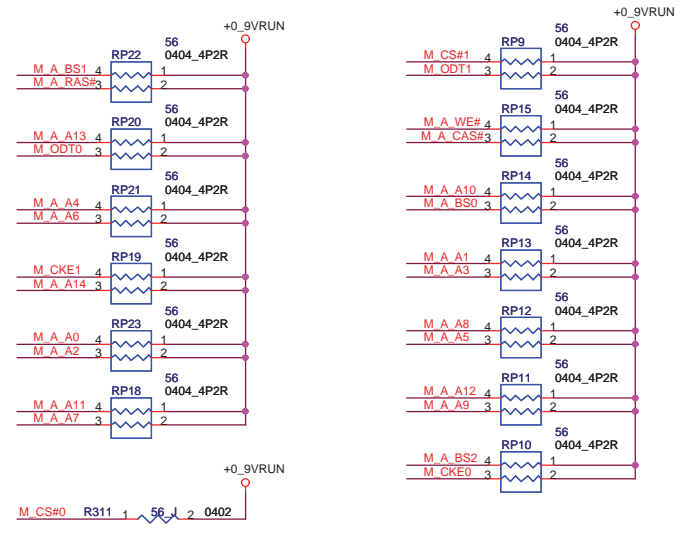
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0.1 μ F and 2.2 μ F placed close to VREF pins



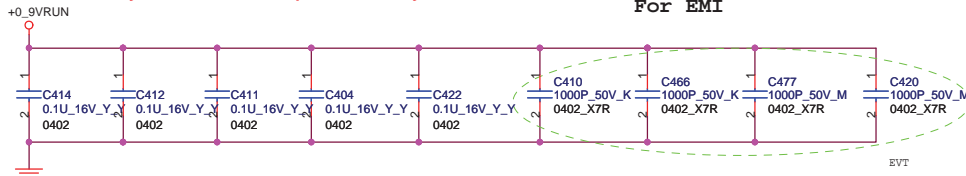
DDR2 SDRAM SO-DIMM (200P)

1.8V per DIMM=3.08A Height = 5 mm



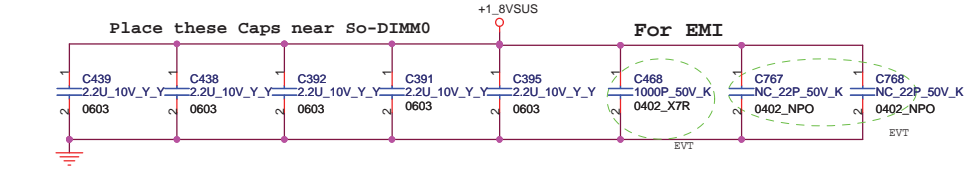
Layout note: Place 1 cap close to every 2 Rtt to +0.9VRUN

For EMI



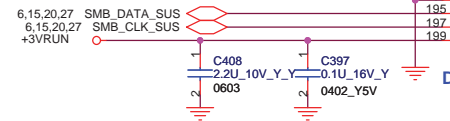
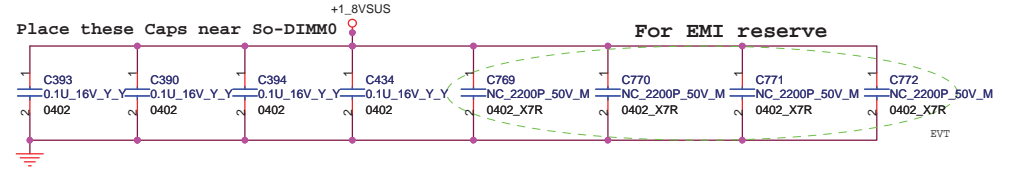
Place these Caps near So-DIMM0

For EMI



Place these Caps near So-DIMM0

For EMI reserve

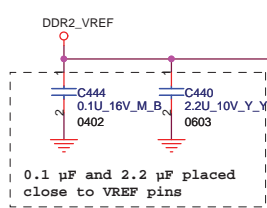


DIMM 0
DDR2 SO-DIMM 200P
FOX_AS0A426_N4RC_4F

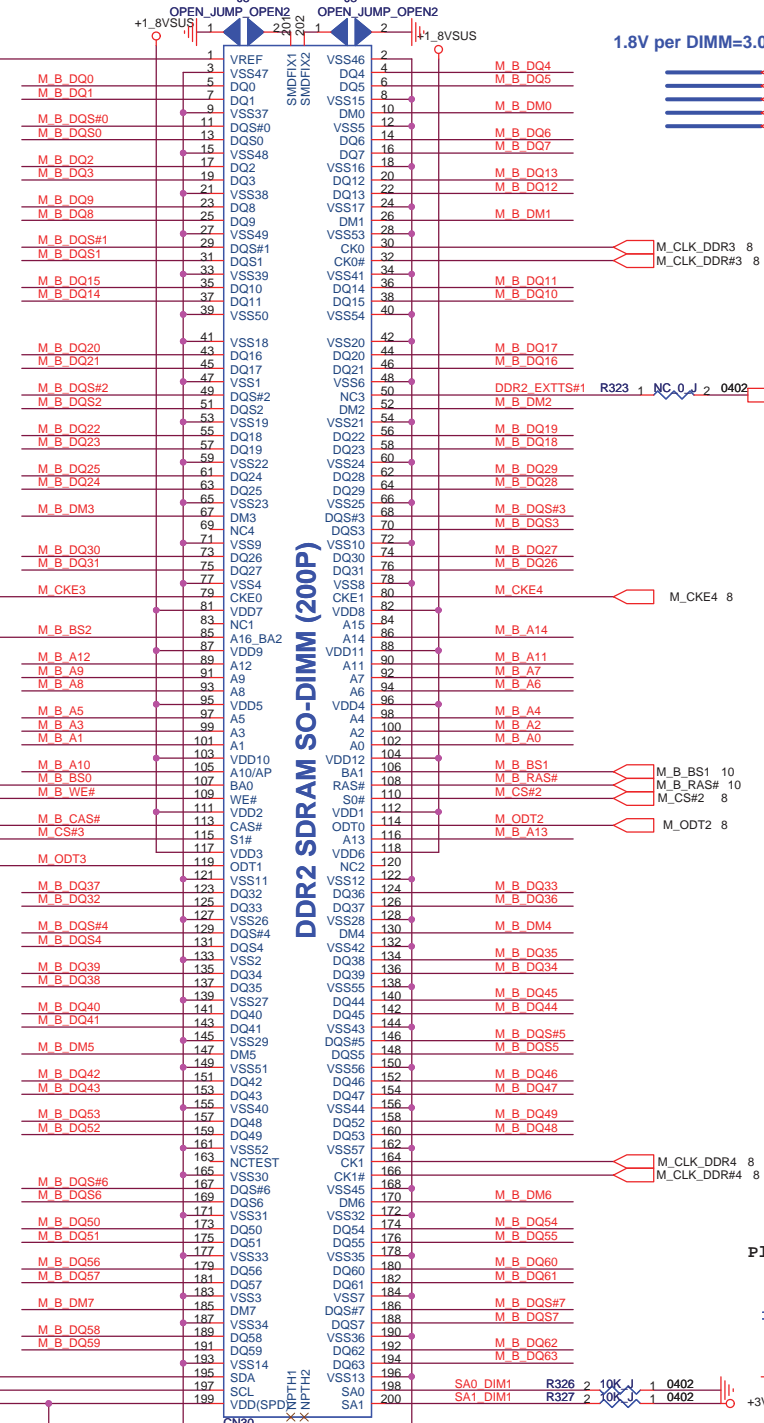
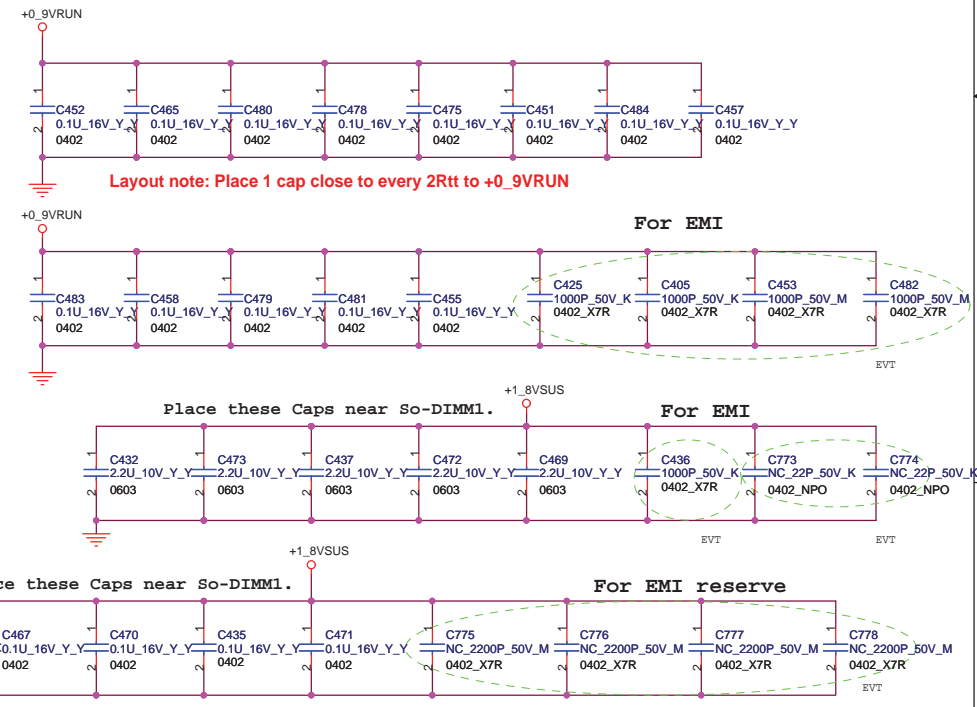
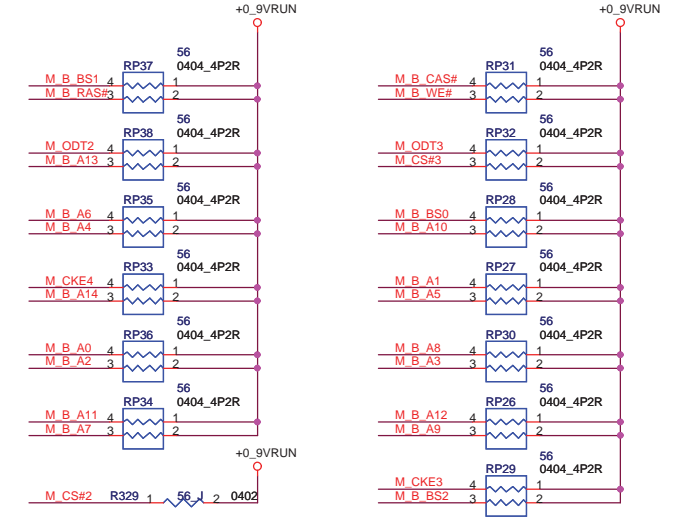
SMBus Address: A0H(W)/A1H(R)

Place DIMM 0 near C402

FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title DDR(H)SO-DIMM_0	
Size A3	Document Number M790-1-01
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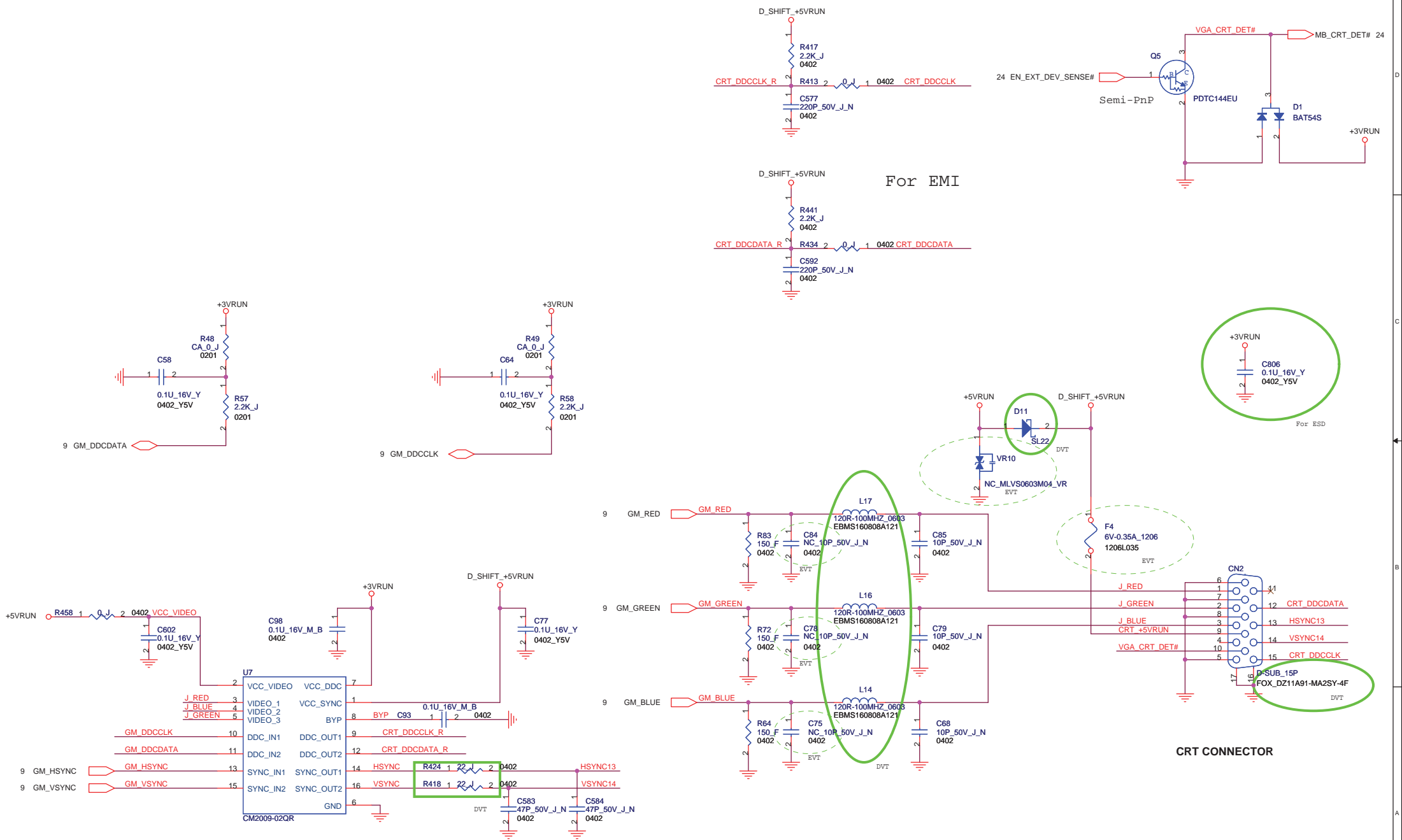
1.8V per DIMM=3.08A Height = 4 mm



DDR2 SDRAM SO-DIMM (200P)

SMBus Address: A4(W)/A5(R)
DIMM_1 is placed farther from the GMCH than DIMM_0
<http://hob-elektronika.net>

FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title DDR(H)SO-DIMM_1	
Size A3	Document Number M790-1-01
Date: Wednesday, July 02, 2008	Sheet 15 of 54

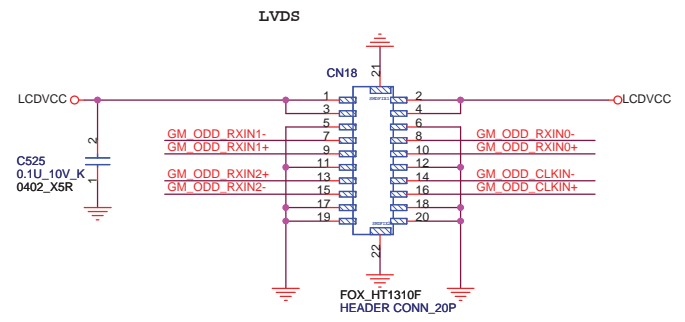
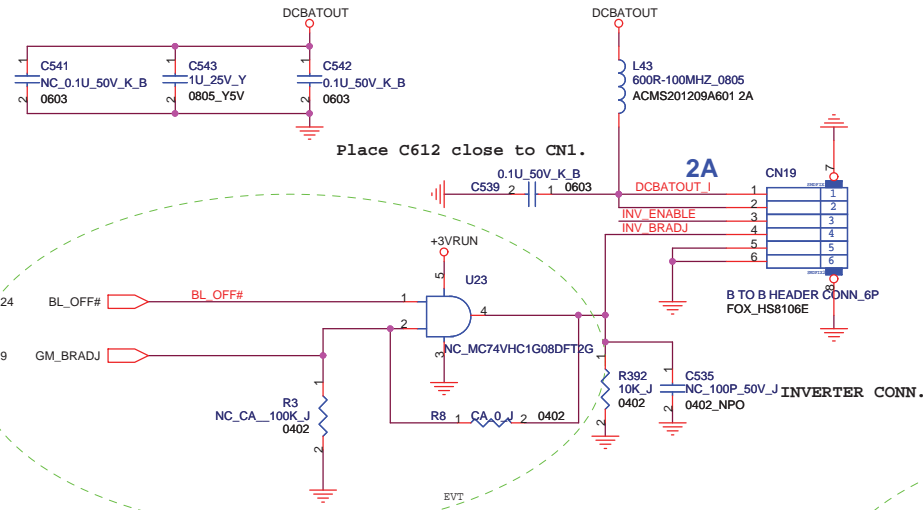


For EMI

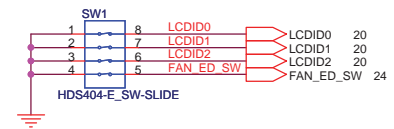
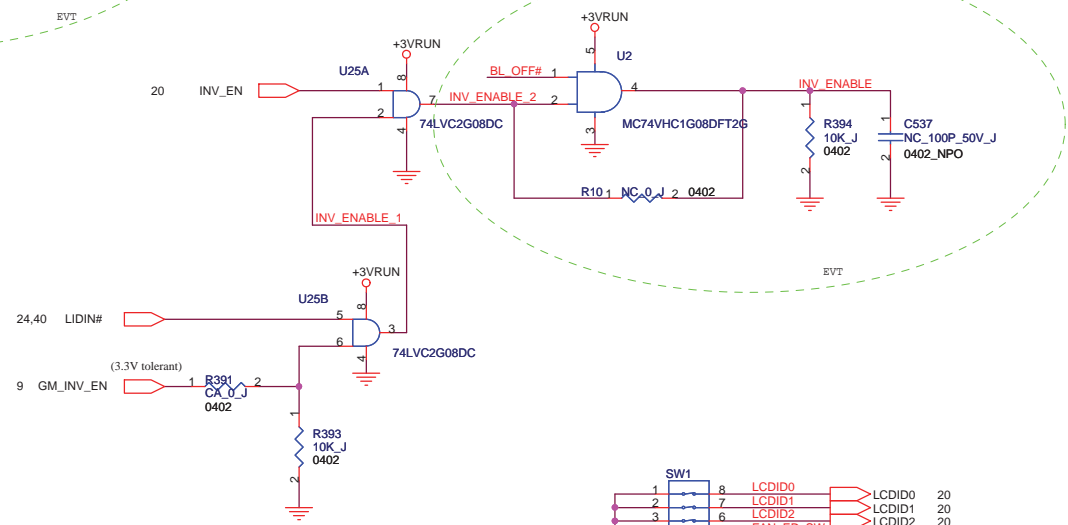
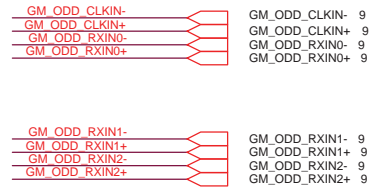
For ESD

CRT CONNECTOR

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	CRT		
Size	Document Number	Rev	
A3	M790-1-01	1.0	
Date:	Wednesday, July 02, 2008	Sheet	16 of 54

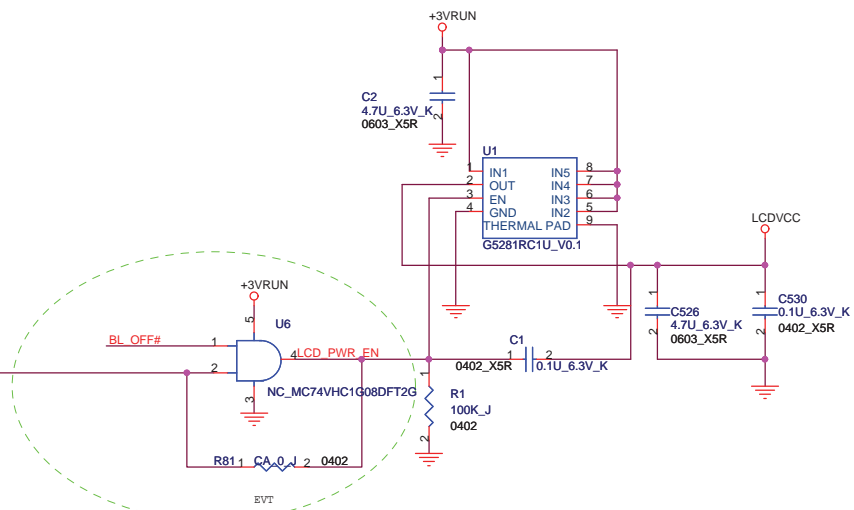


LVDS



PANEL ID

Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vendor	AUO	CPI	LPL	LPL
Device Name	B154EW02V7	CLAA154WB03	LP154WX4-TLC5	LP154WX5-TLA1
Panel ID [3..0]	001	010	011	100

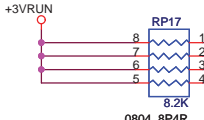
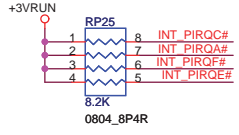
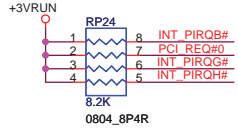
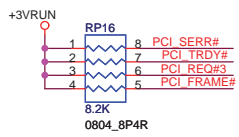
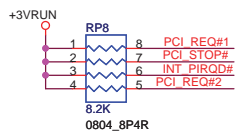


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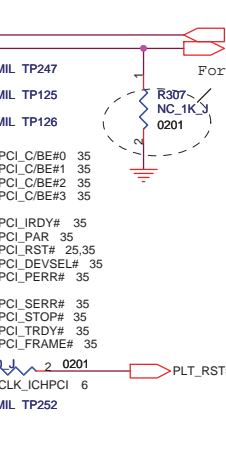
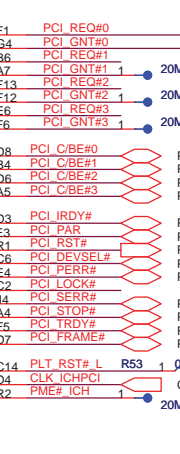
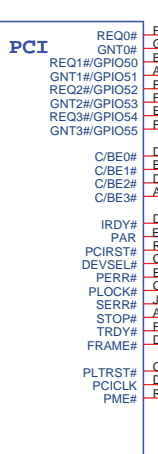
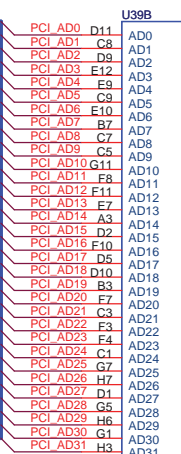
Title **LVDS**

Size A3	Document Number M790-1-01	Rev 1.0
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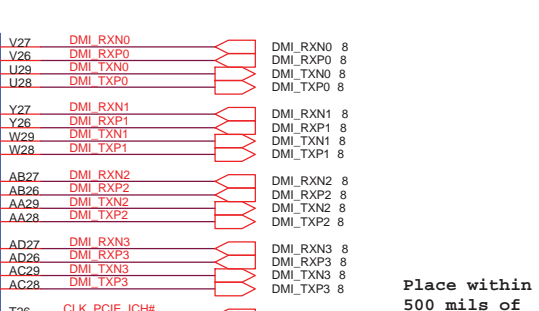
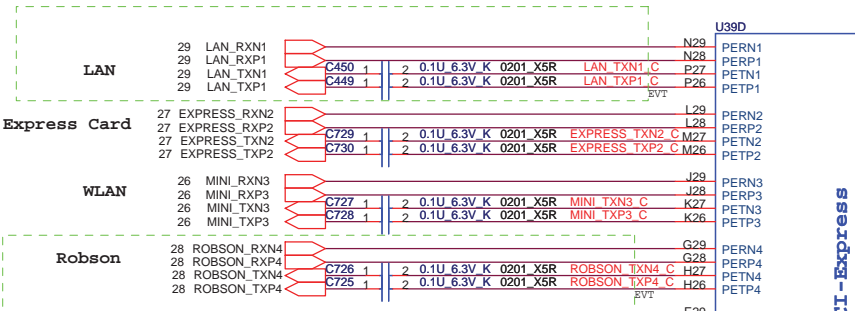
PCI Pullups



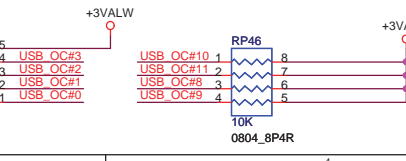
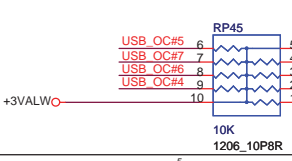
For Boot BIOS Selection.

Strap for Boot-BIOS

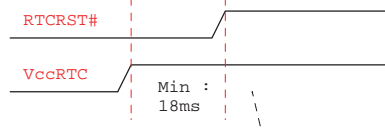
	GNT#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi



USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	Ext. Port
PORT-3	Ext. Port
PORT-4	
PORT-5	EXPRESS CARD
PORT-6	
PORT-7	Camera
PORT-8	Felica
PORT-9	
PORT-10	Wi-MAX
PORT-11	

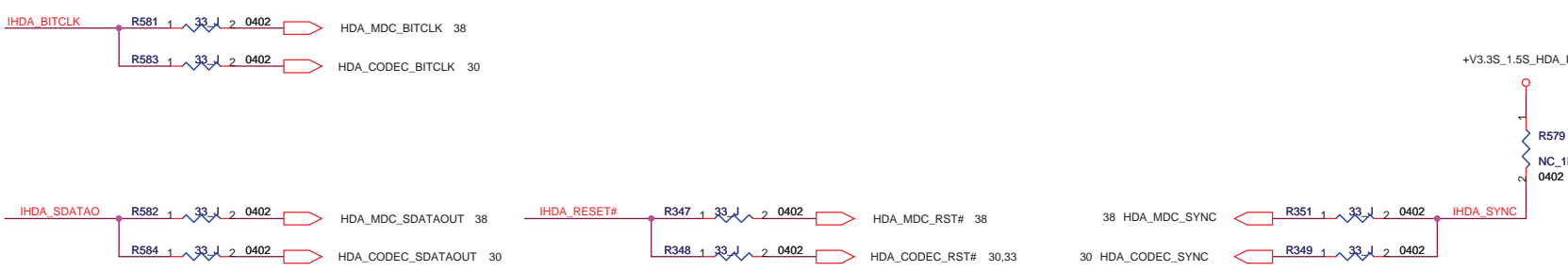
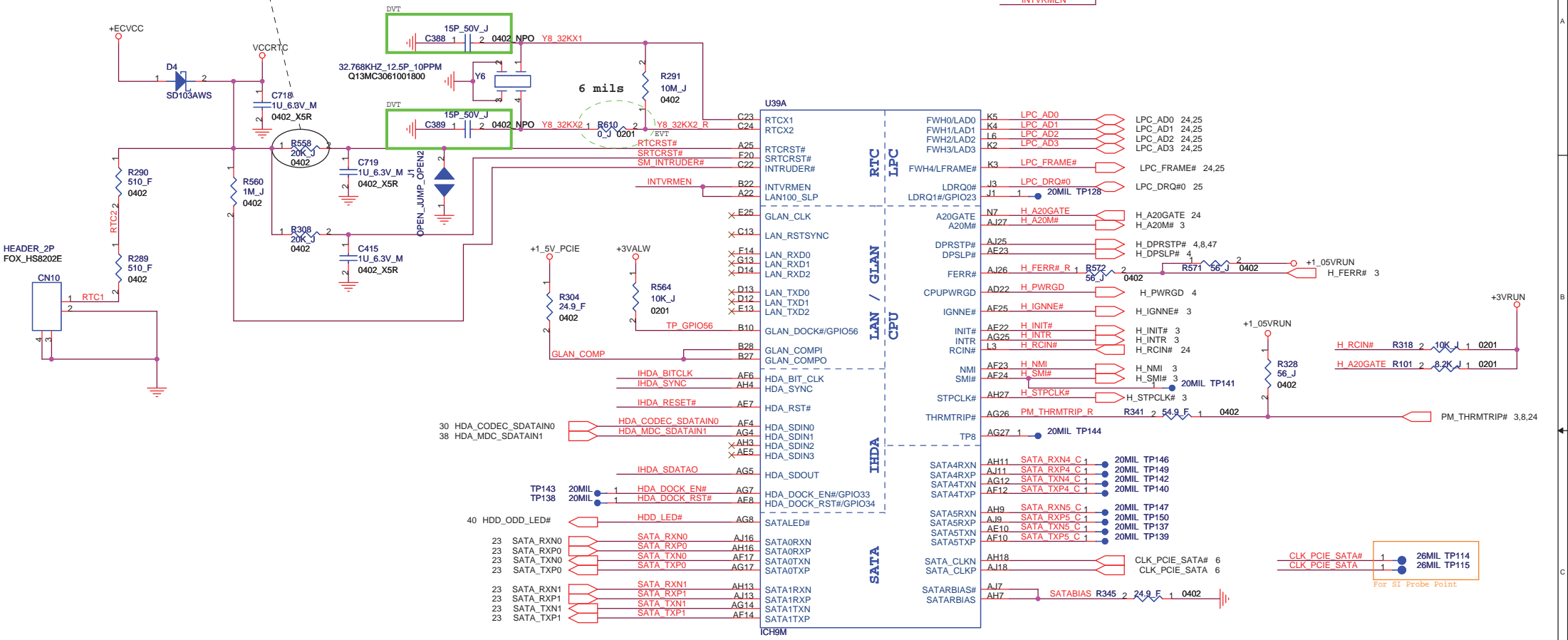


Place within 500 mils of ICH and don't routing next to high speed signals

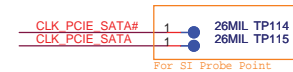


The traces inside this block should be wider.

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCt1_5, VccLAN1_05 and VccCt1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)



FWH0/LAD0	K5	LPC_AD0	LPC_AD0	24,25
FWH1/LAD1	K4	LPC_AD1	LPC_AD1	24,25
FWH2/LAD2	L6	LPC_AD2	LPC_AD2	24,25
FWH3/LAD3	K2	LPC_AD3	LPC_AD3	24,25
FWH4/LFRAME#	K3	LPC_FRAME#	LPC_FRAME#	24,25
LDRQ0#	J3	LPC_DRQ#0	LPC_DRQ#0	25
LDRQ1#/GPIO23	J1	20MIL TP128		
A20GATE	N7	H_A20GATE	H_A20GATE	24
A20M#	AJ27	H_A20M#	H_A20M#	3
DPRSTP#	AJ25	H_DPRSTP#	H_DPRSTP#	4,8,47
DPSP#	AE23	H_DPSP#	H_DPSP#	4
FERR#	AJ26	H_FERR#	H_FERR#	3
CPUPWRGD	AD22	H_PWRGD	H_PWRGD	4
IGNNE#	AE25	H_IGNNE#	H_IGNNE#	3
INIT#	AE22	H_INIT#	H_INIT#	3
INTR	AG25	H_INTR	H_INTR	3
RCIN#	L3	H_RCIN#	H_RCIN#	24
NMI	AE23	H_NMI	H_NMI	3
SMI#	AE24	H_SMI#	H_SMI#	3
STPCLK#	AH27	H_STPCLK#	H_STPCLK#	3
THRMTRIP#	AG26	PM_THRMTRIP#	PM_THRMTRIP#	3,8,24
TP8	AG27	20MIL TP144		
SATA4RXN	AH11	SATA_RXN4	20MIL TP146	
SATA4RXP	AJ11	SATA_RXP4	20MIL TP149	
SATA4TXN	AG12	SATA_TXN4	20MIL TP142	
SATA4TXP	AE12	SATA_TXP4	20MIL TP140	
SATA5RXN	AH9	SATA_RXN5	20MIL TP147	
SATA5RXP	AJ9	SATA_RXP5	20MIL TP150	
SATA5TXN	AE10	SATA_TXN5	20MIL TP137	
SATA5TXP	AE10	SATA_TXP5	20MIL TP139	
SATA_CLKN	AH18	CLK_PCIE_SATA#	6	
SATA_CLKP	AJ18	CLK_PCIE_SATA	6	
SATARBIAS#	AJ7	SATARBIAS	R345	24,9
SATARBIAS	AH7	SATARBIAS	R345	24,9

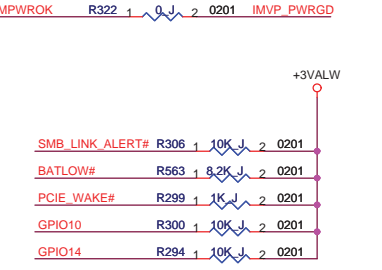
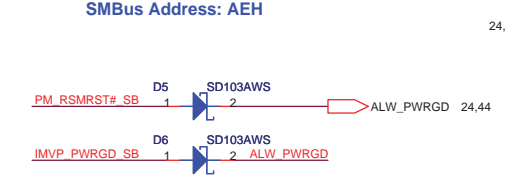
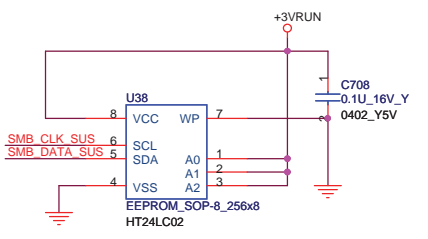
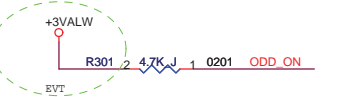
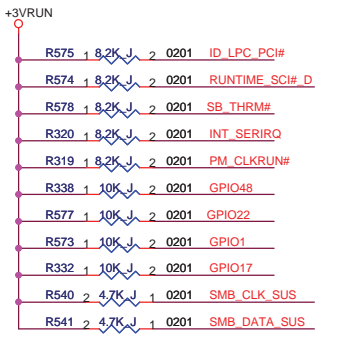
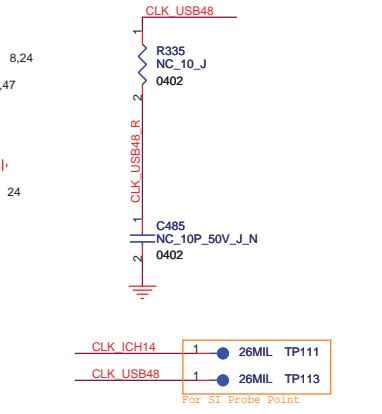
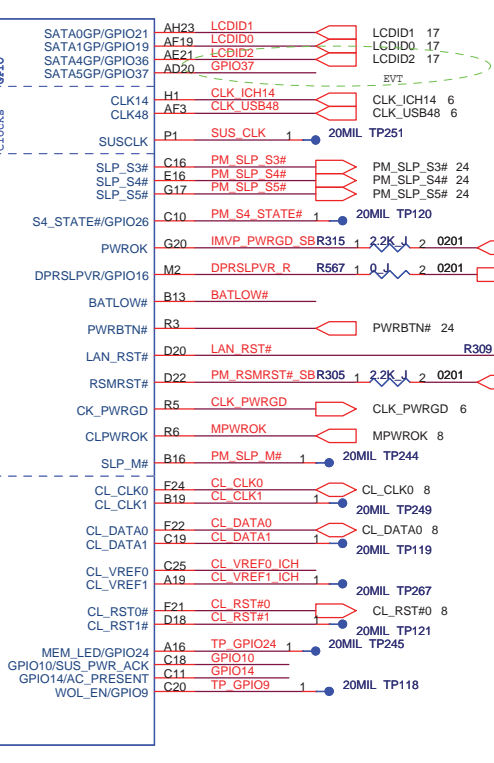
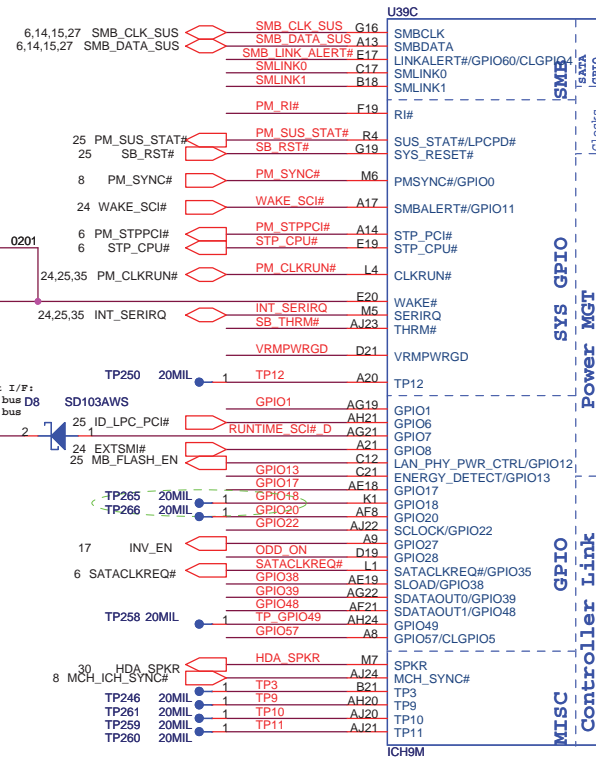
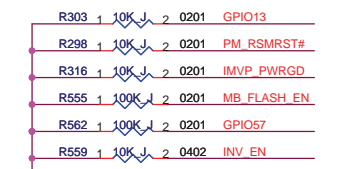
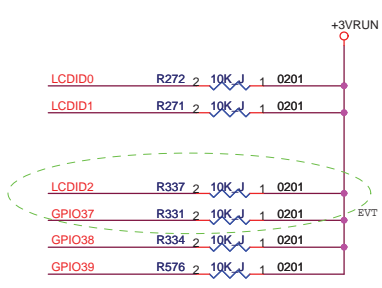
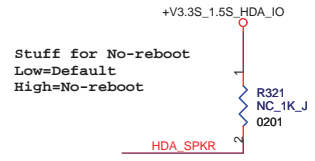
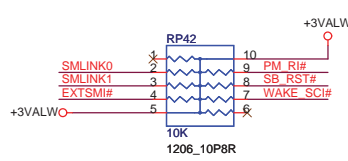


FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **ICH9-M (LPC,IDE,SATA) 2/5**

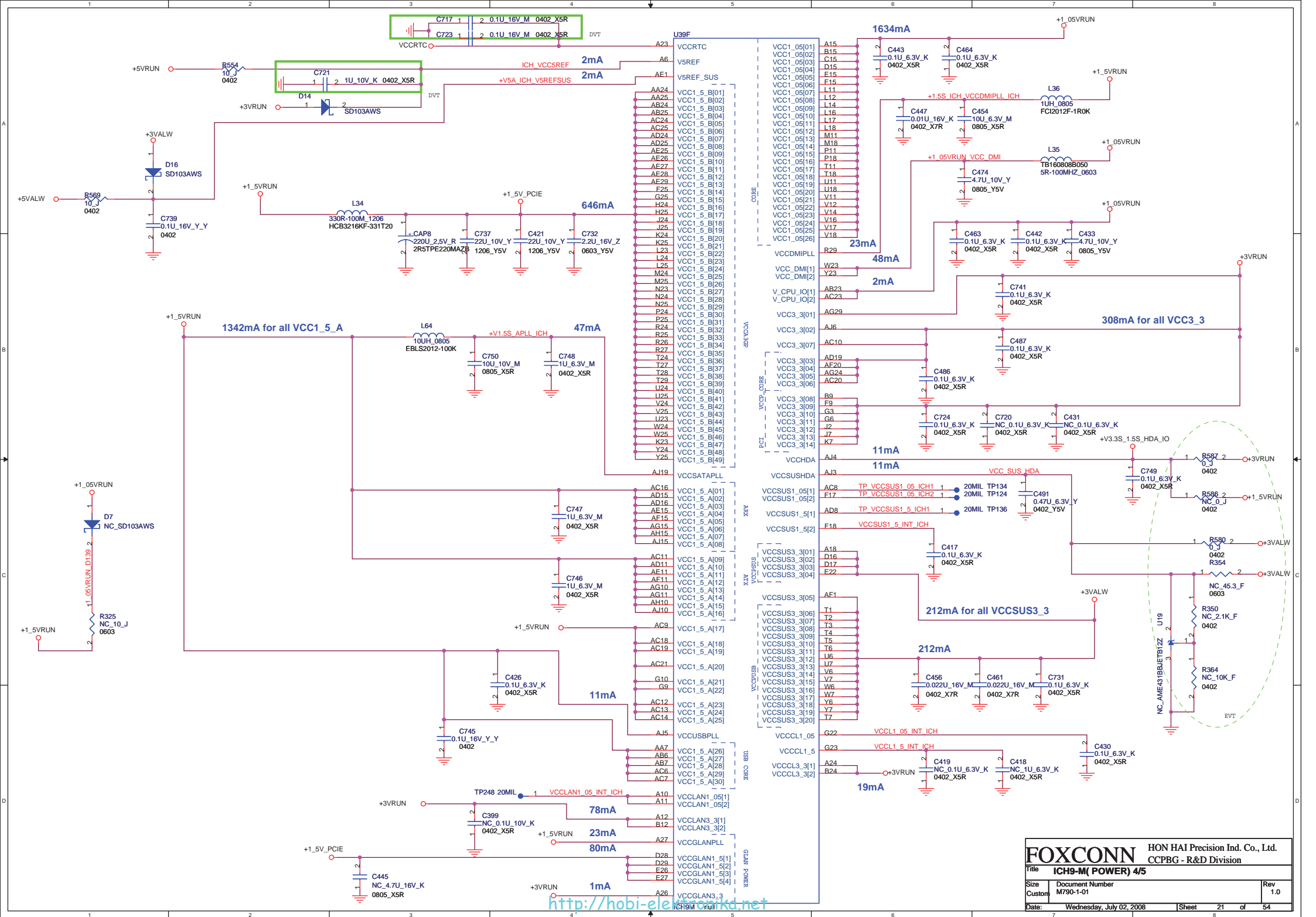
Size A3 Document Number M790-1-01 Rev 1.0

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FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division
 Title: ICH9-M(GPIO) 3/5
 Size: A3 Document Number: M790-1-01 Rev: 1.0
 Date: Wednesday, July 02, 2008 Sheet: 20 of 54



FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **ICH9-M (POWER) 4/5**

Size	Document Number	Rev
Custom	M790-1-01	1.0

Date: Wednesday, July 02, 2008 | Sheet 21 of 54

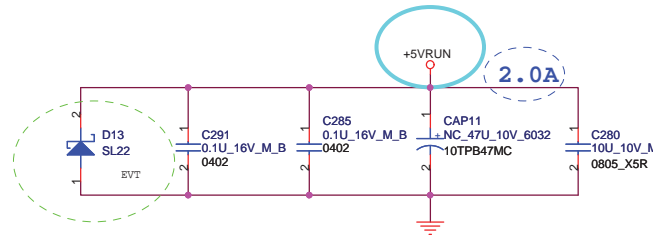
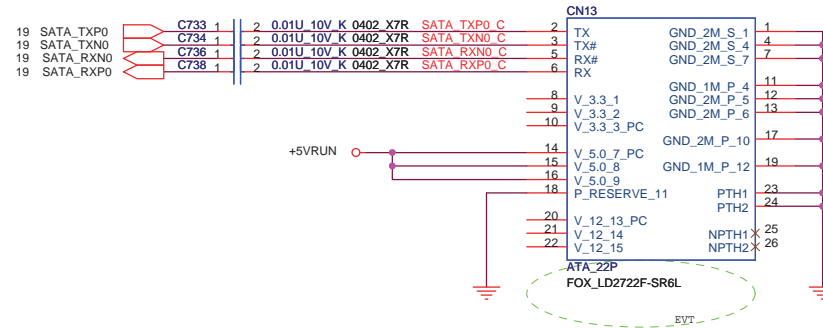
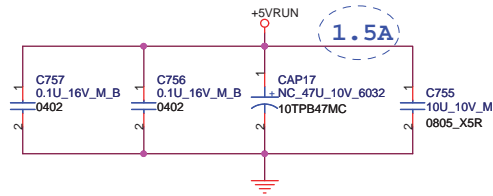
<http://hobi-electronics.com>

U39E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB23	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD5	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AE13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF26	VSS[047]	VSS[153]	R13
AF27	VSS[048]	VSS[154]	R14
AF5	VSS[049]	VSS[155]	R15
AF7	VSS[050]	VSS[156]	R16
AF9	VSS[051]	VSS[157]	R17
AG13	VSS[052]	VSS[158]	R18
AG16	VSS[053]	VSS[159]	R28
AG18	VSS[054]	VSS[160]	T12
AG20	VSS[055]	VSS[161]	T13
AG23	VSS[056]	VSS[162]	T14
AG3	VSS[057]	VSS[163]	T15
AG6	VSS[058]	VSS[164]	T16
AG9	VSS[059]	VSS[165]	T17
AH12	VSS[060]	VSS[166]	T23
AH14	VSS[061]	VSS[167]	B26
AH17	VSS[062]	VSS[168]	U12
AH19	VSS[063]	VSS[169]	U13
AH2	VSS[064]	VSS[170]	U14
AH22	VSS[065]	VSS[171]	U15
AH25	VSS[066]	VSS[172]	U16
AH28	VSS[067]	VSS[173]	U17
AH5	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AJ12	VSS[070]	VSS[176]	U27
AJ14	VSS[071]	VSS[177]	U3
AJ17	VSS[072]	VSS[178]	V1
AJ8	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B14	VSS[075]	VSS[181]	V23
B17	VSS[076]	VSS[182]	V28
B2	VSS[077]	VSS[183]	V29
B20	VSS[078]	VSS[184]	V4
B23	VSS[079]	VSS[185]	V5
B5	VSS[080]	VSS[186]	W26
B8	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	W3
C27	VSS[083]	VSS[189]	Y1
E11	VSS[084]	VSS[190]	Y28
E14	VSS[085]	VSS[191]	Y29
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	AG28
E24	VSS[089]	VSS[195]	AH6
E5	VSS[090]	VSS[196]	AF2
E8	VSS[091]	VSS[197]	B25
F16	VSS[092]	VSS[198]	
F28	VSS[093]		
F29	VSS[094]	VSS_NCTF[01]	A1
G12	VSS[095]	VSS_NCTF[02]	A2
G14	VSS[096]	VSS_NCTF[03]	A28
G18	VSS[097]	VSS_NCTF[04]	A29
G21	VSS[098]	VSS_NCTF[05]	AH1
G24	VSS[099]	VSS_NCTF[06]	AH29
G26	VSS[100]	VSS_NCTF[07]	AJ1
G27	VSS[101]	VSS_NCTF[08]	AJ2
G8	VSS[102]	VSS_NCTF[09]	AJ28
H2	VSS[103]	VSS_NCTF[10]	AJ29
H23	VSS[104]	VSS_NCTF[11]	B1
H28	VSS[105]	VSS_NCTF[12]	B29
H29	VSS[106]		

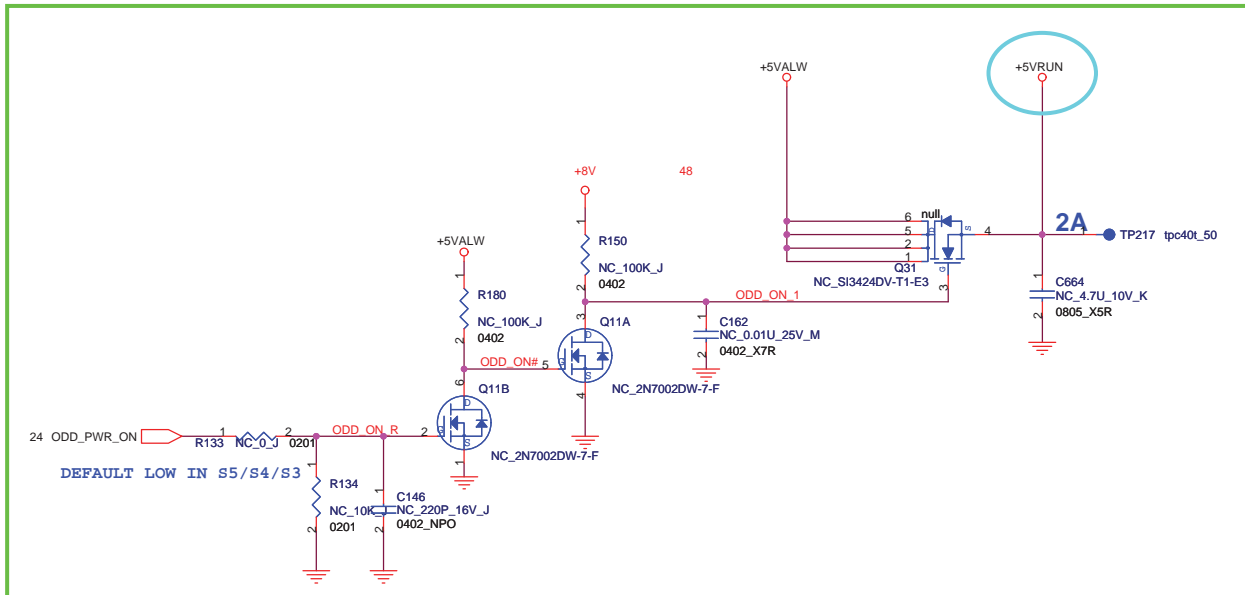
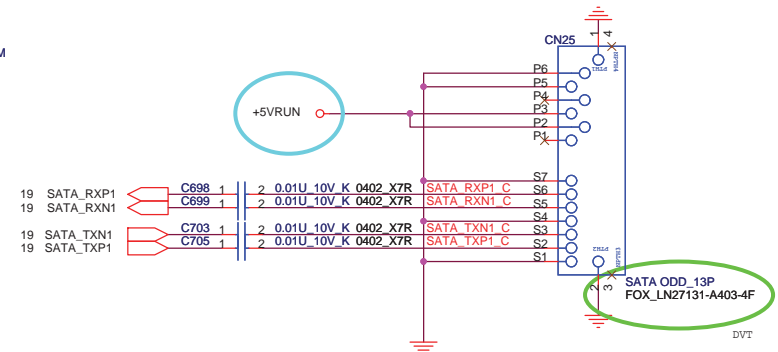
ICH9M

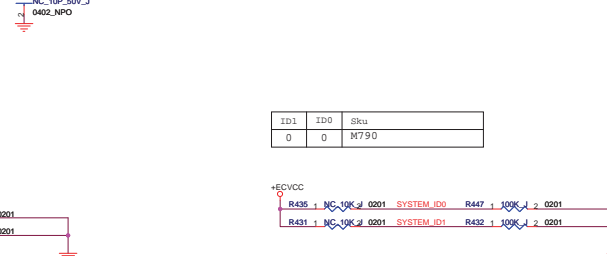
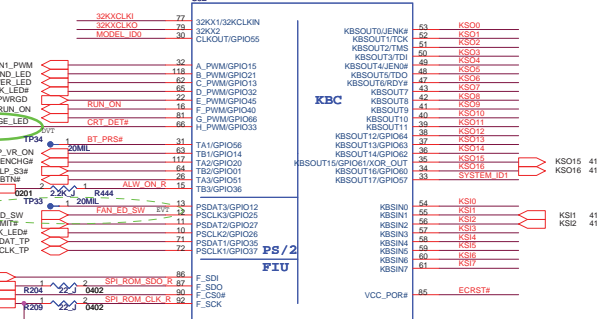
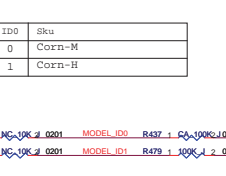
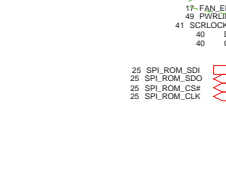
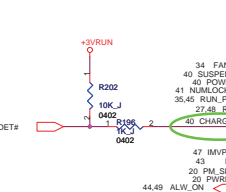
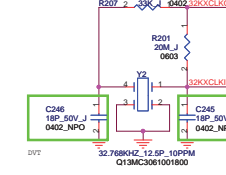
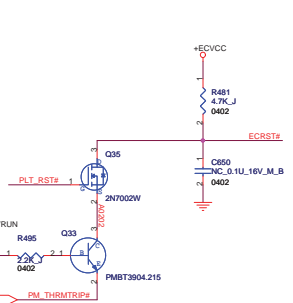
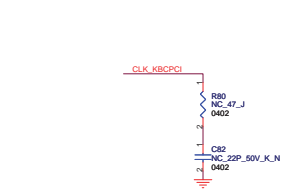
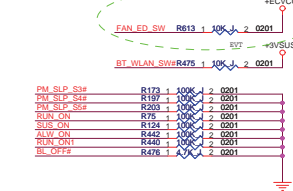
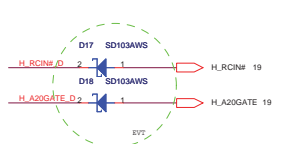
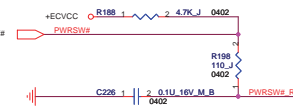
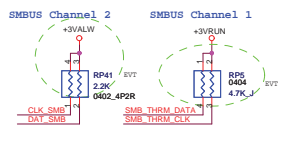
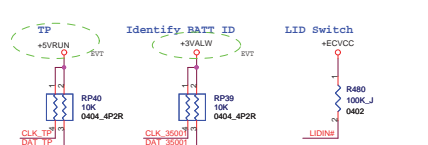
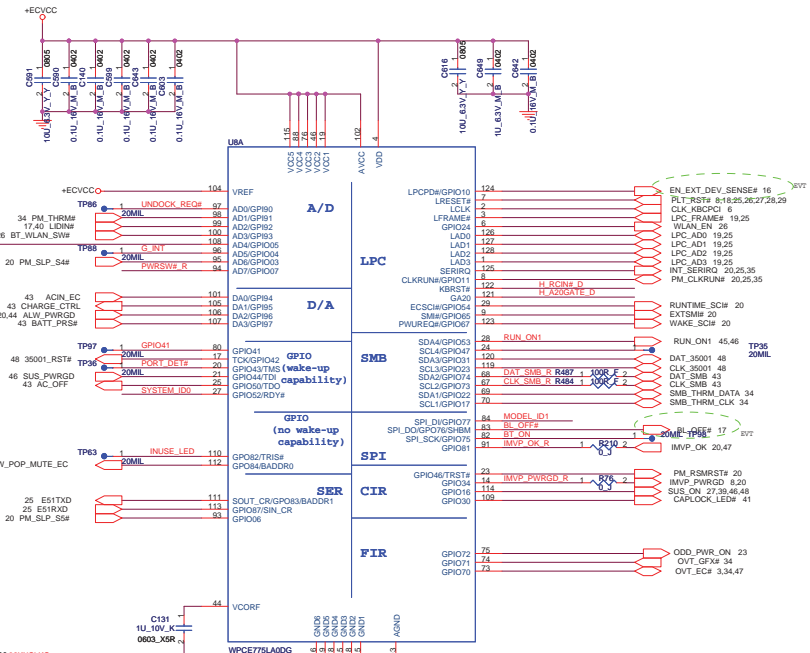
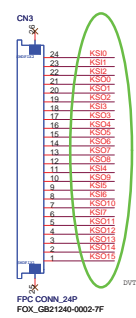
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ICH9-M (GND) 5/5		
Size	Document Number	Rev	
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Date:	Wednesday, July 02, 2008	Sheet	22 of 54

SATA HDD CONN



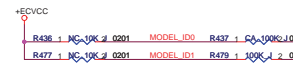
SATA ODD CONN

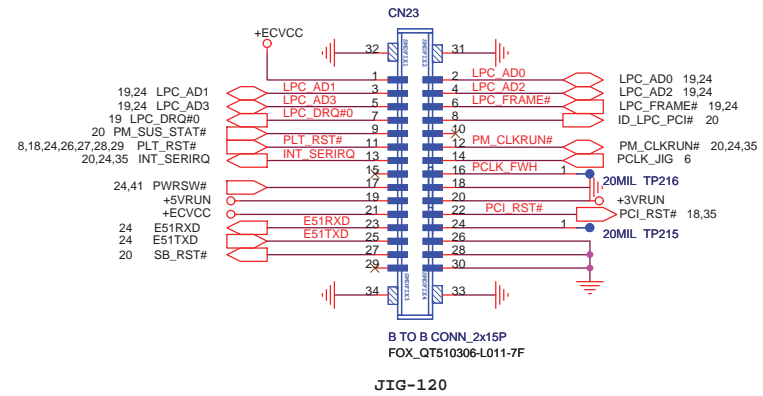
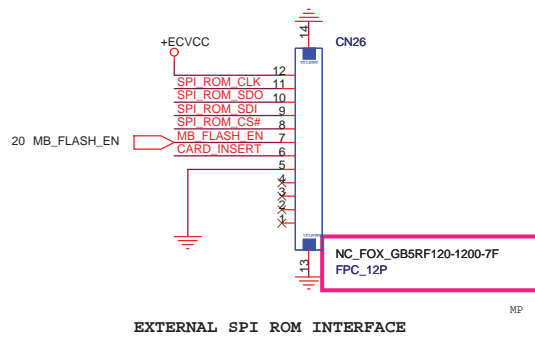
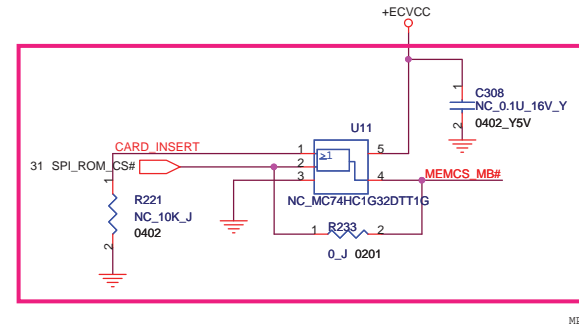
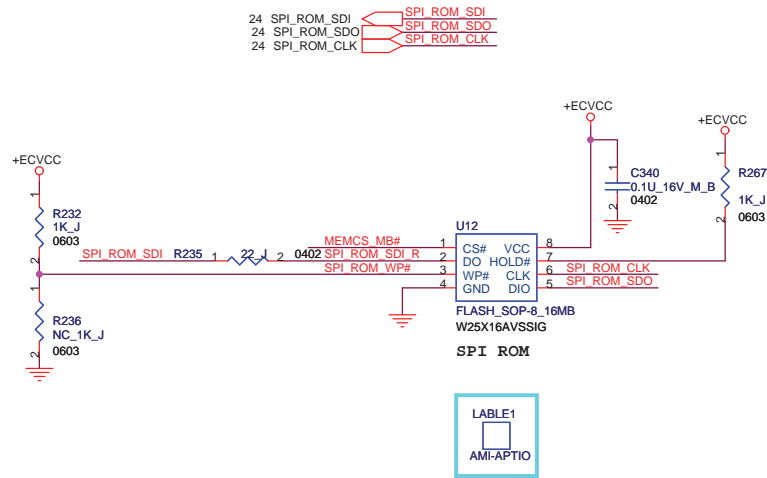


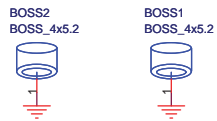


ID1	ID0	Sku
0	0	CoIn-M
0	1	CoIn-H

ID1	ID0	Sku
0	0	M790



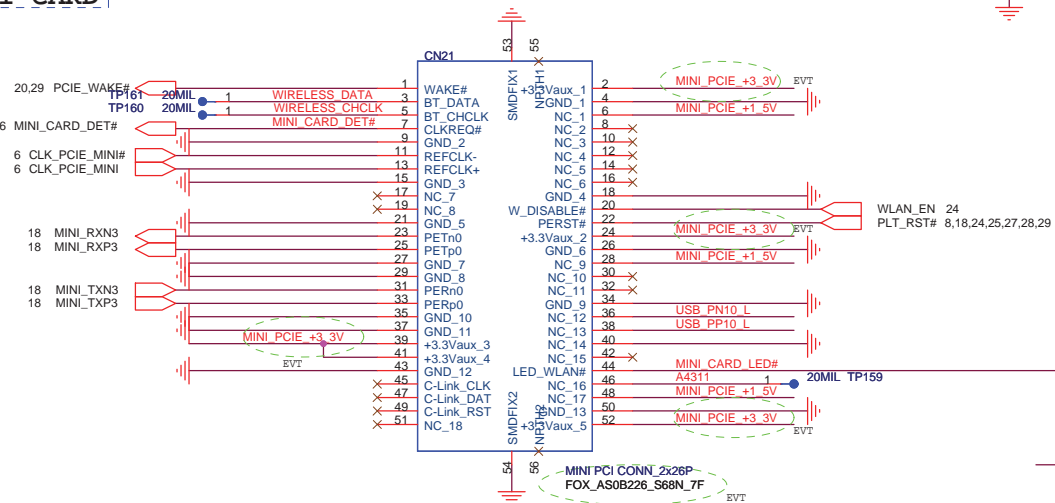
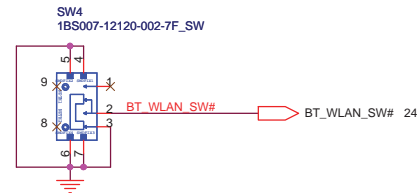




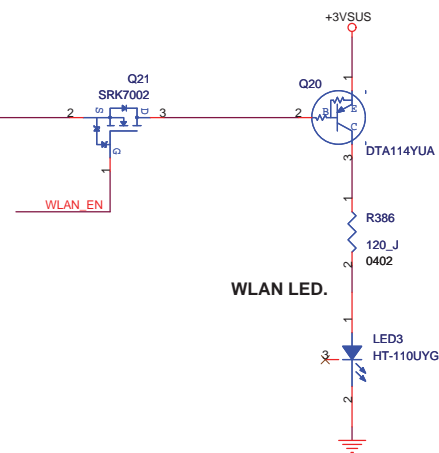
MINI CARD

+1.5V=>0.5A Peak/0.375A Normal
 +3.3VAux=>2.75A Peak/1.1A Normal

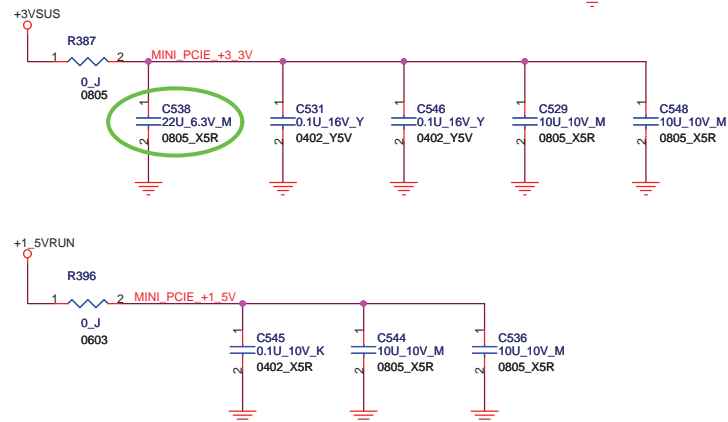
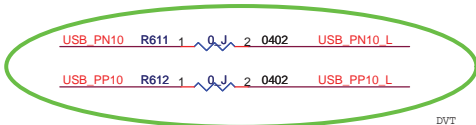
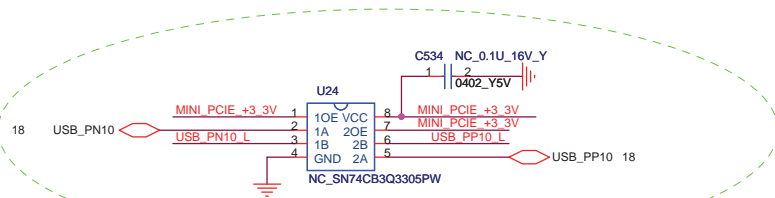
WLAN ON/OFF Switch



**Mini Card.
WLAN**



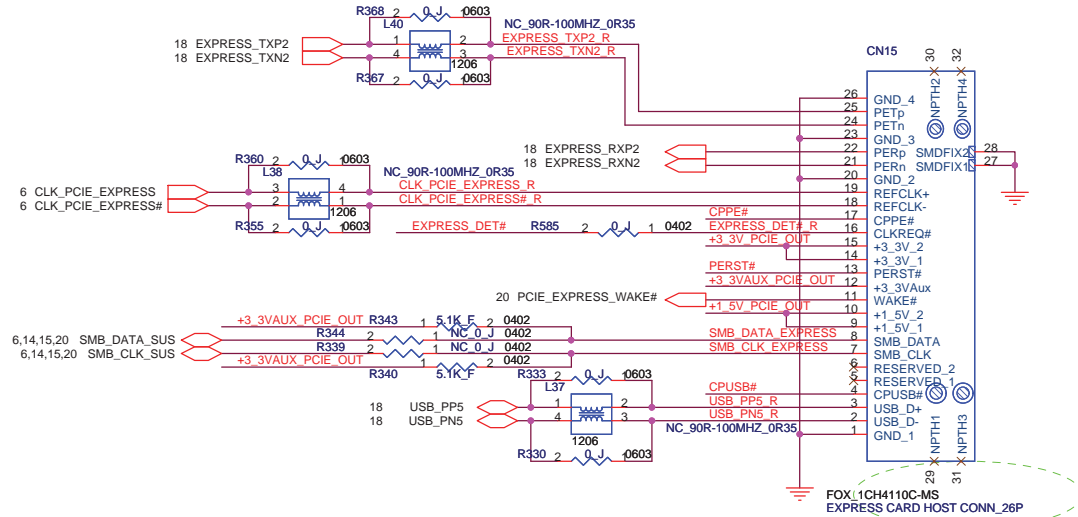
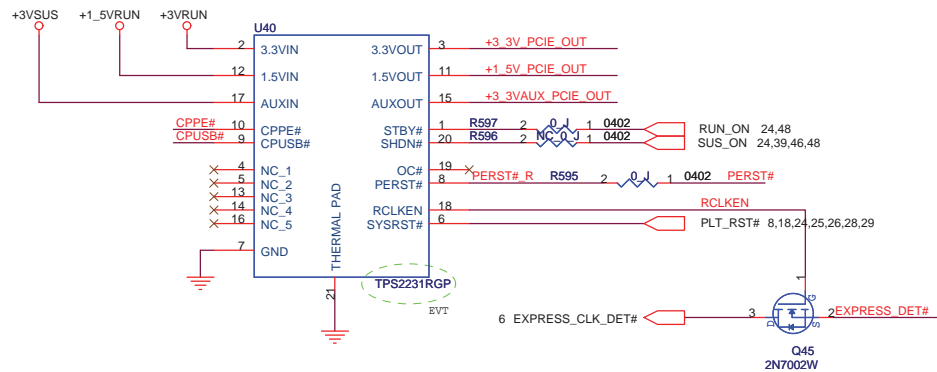
WLAN LED.



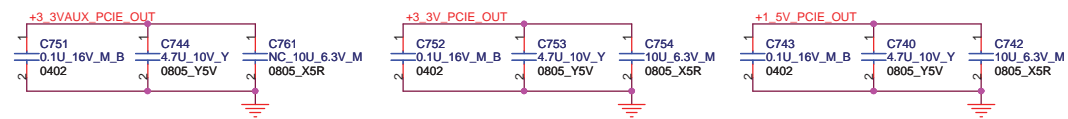
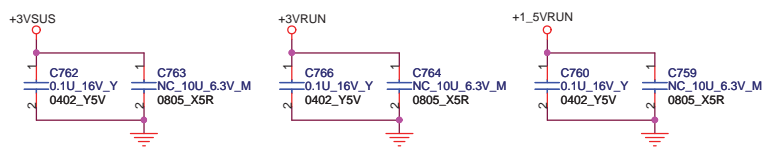
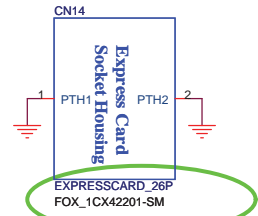
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Mini-PCIE Card			
Size A3	Document Number M790-1-01	Rev 1.0	
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+1.5V=>1.3A
+3.3VAux=>0.6A
+3.3V=>2.5A

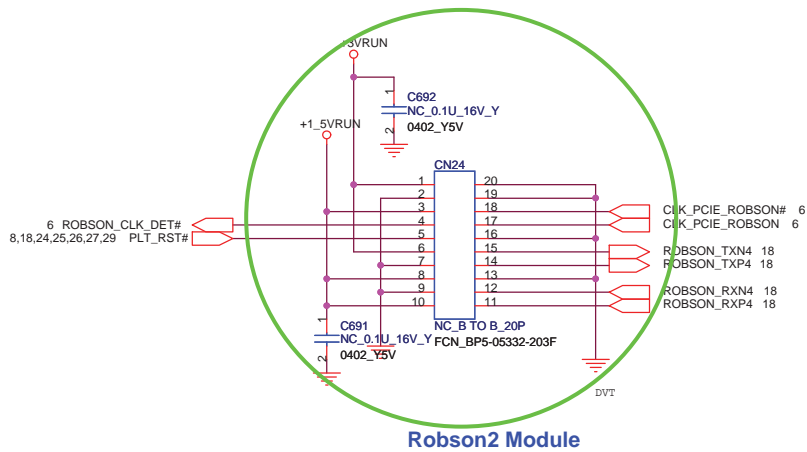
Express Card Power Switch



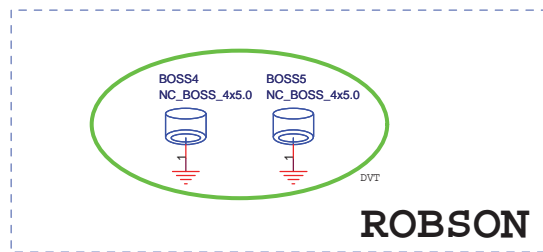
Express Card Slot.

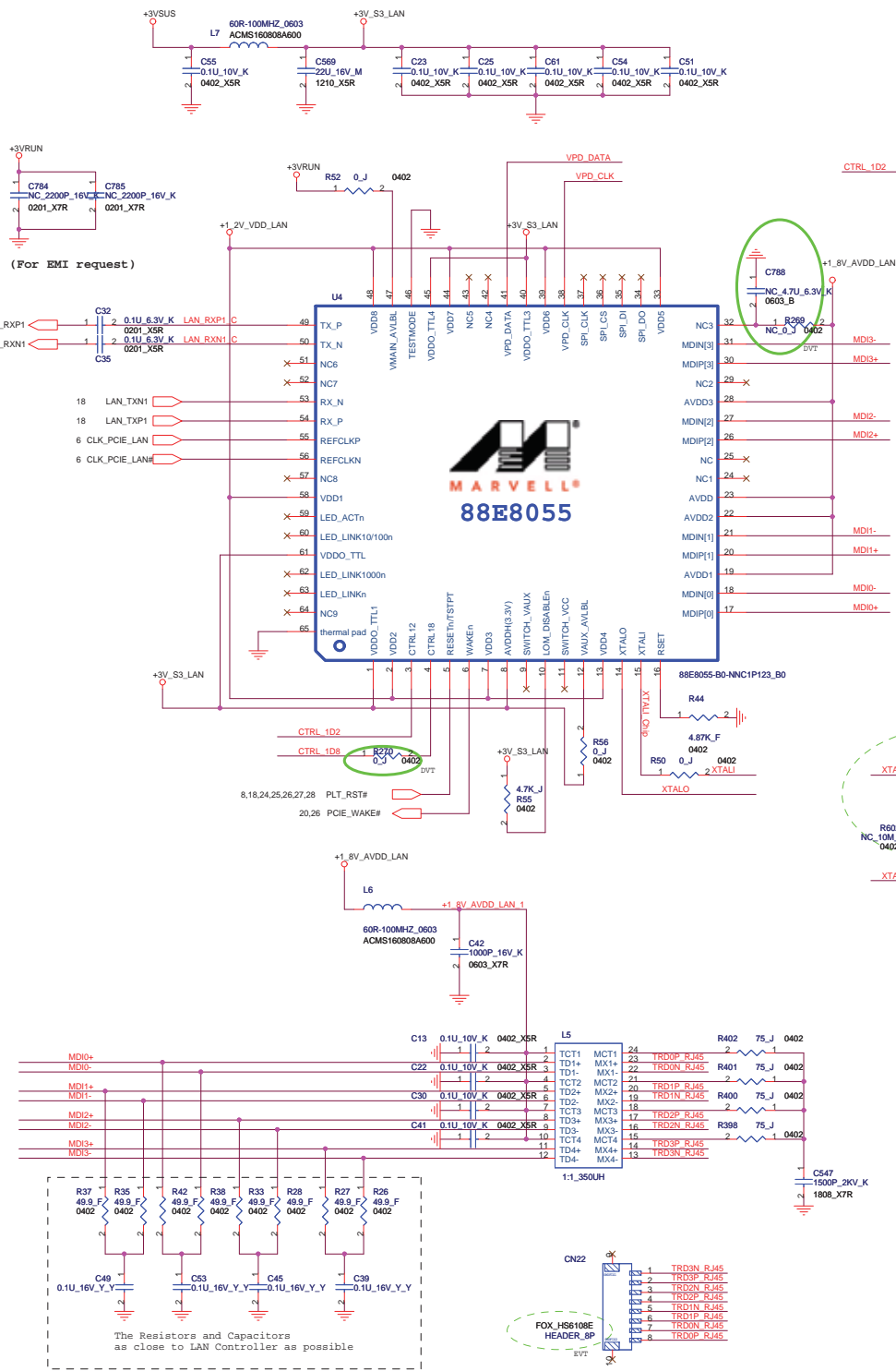


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title EXPRESS CARD		CCPBG - R&D Division	
Size A3	Document Number M790-1-01	Rev 1.0	
Date: Wednesday, July 02, 2008	Sheet 27	of 54	

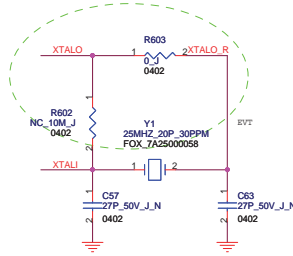
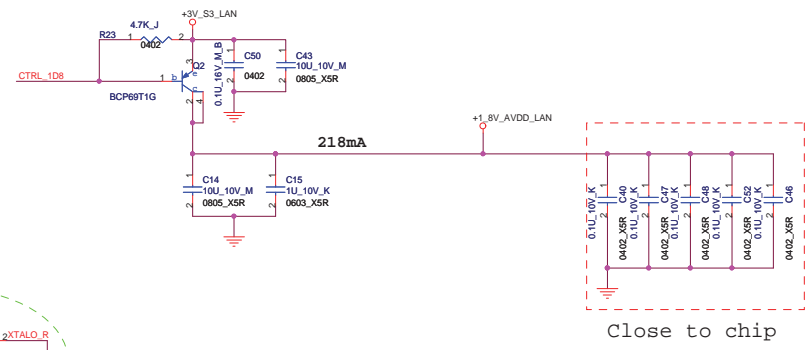
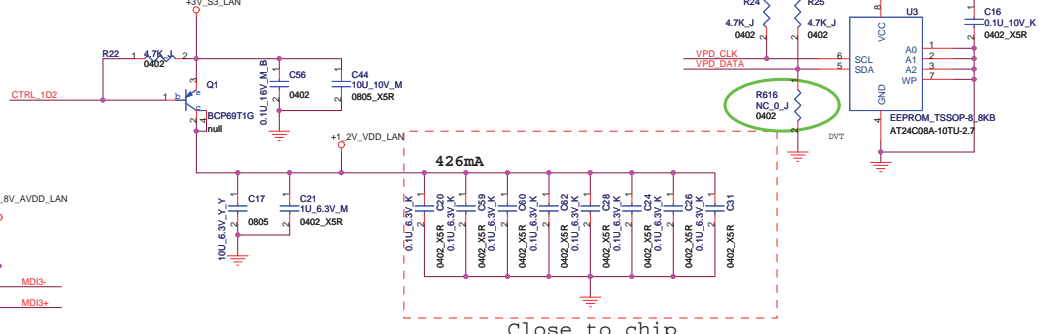


EVT2 11/6 Need to update new connector.





Used EEPROM R616 need NC.
No used EEPROM R25/U3/C16 need NC.

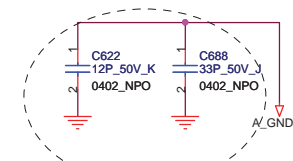
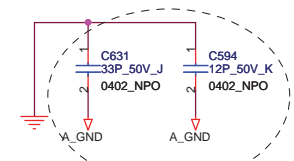
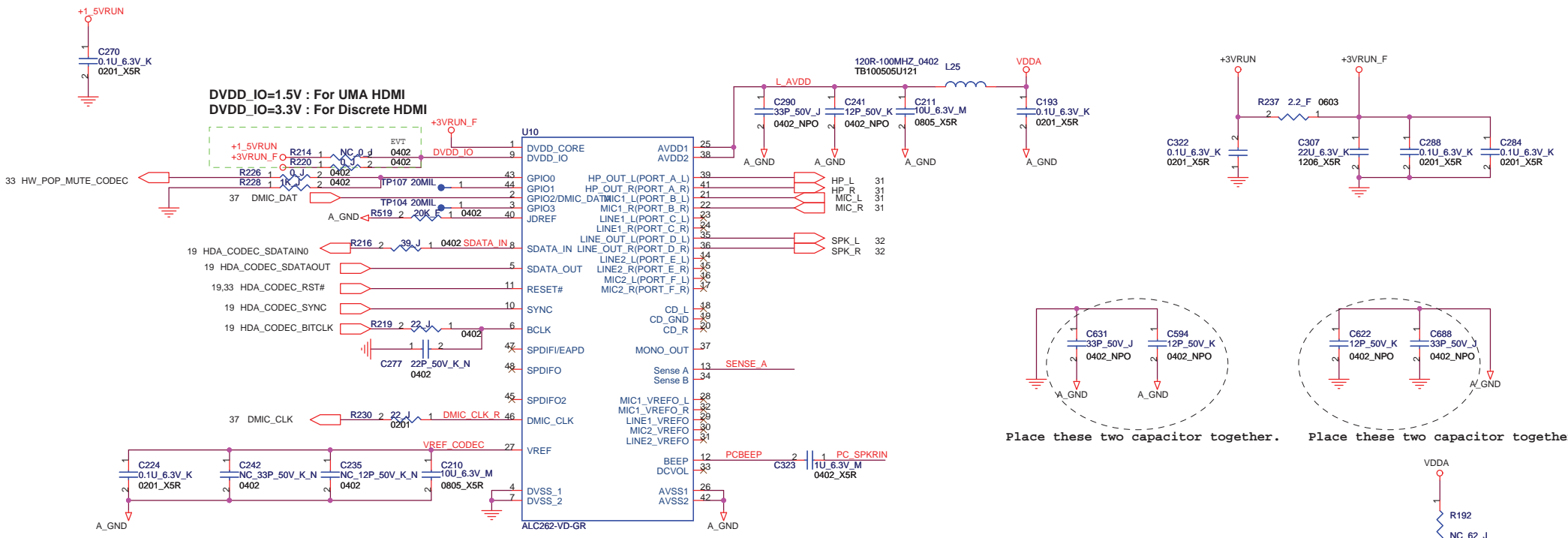


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

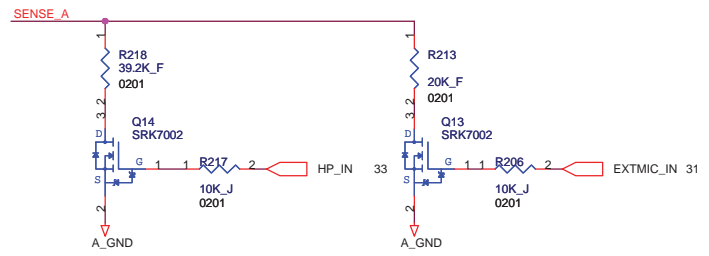
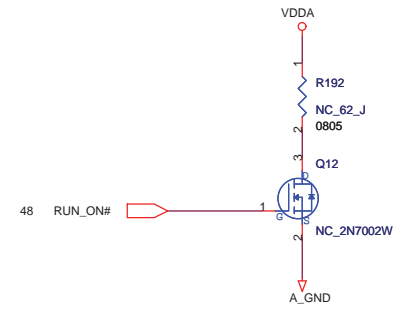
File: LAN (88E8055)

Size C	Document Number M790-1-01	Rev 1.0
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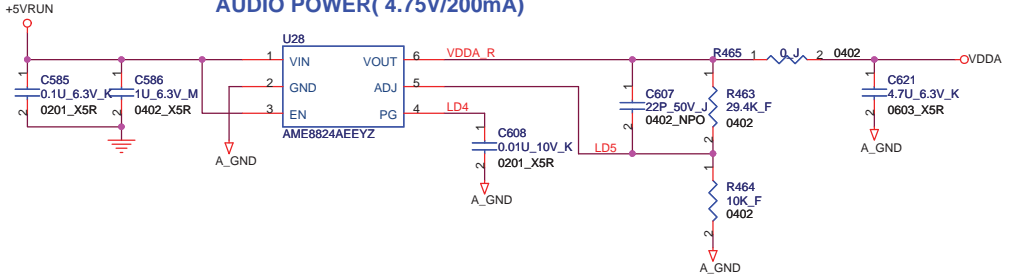
DVDD_IO=1.5V : For UMA HDMI
 DVDD_IO=3.3V : For Discrete HDMI



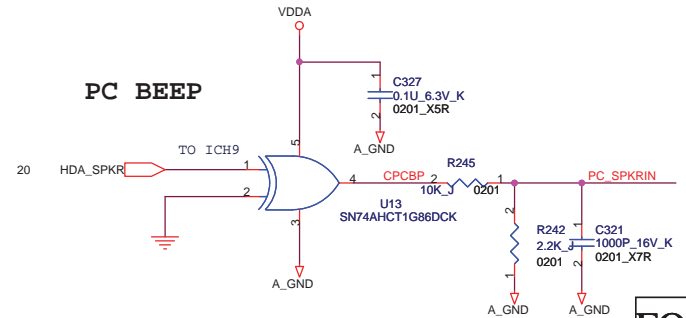
Place these two capacitor together. Place these two capacitor together.

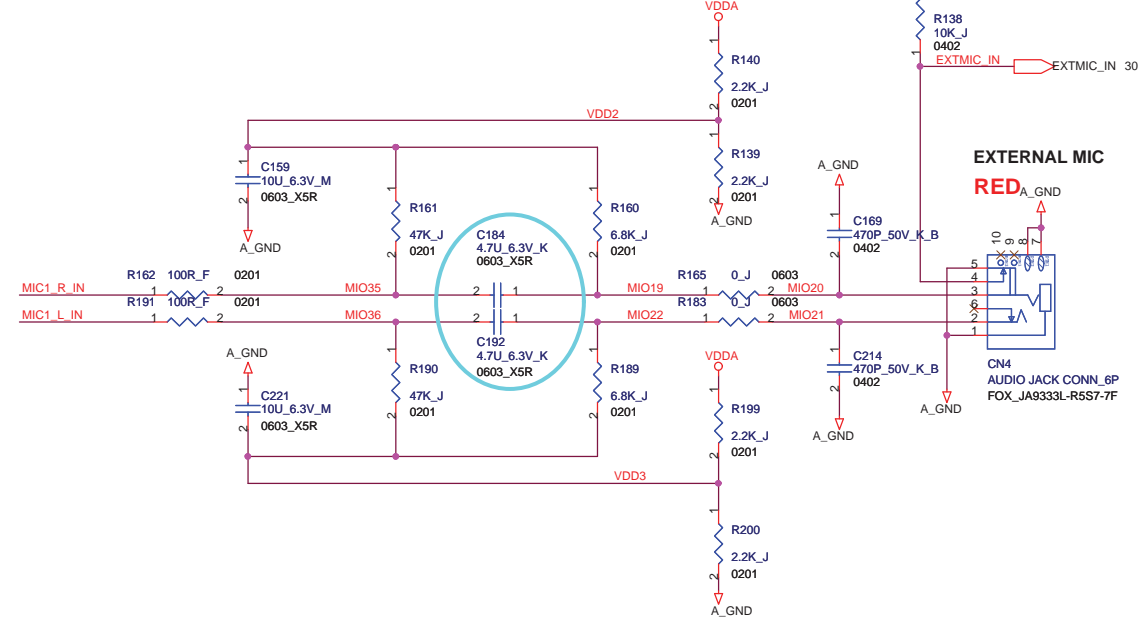
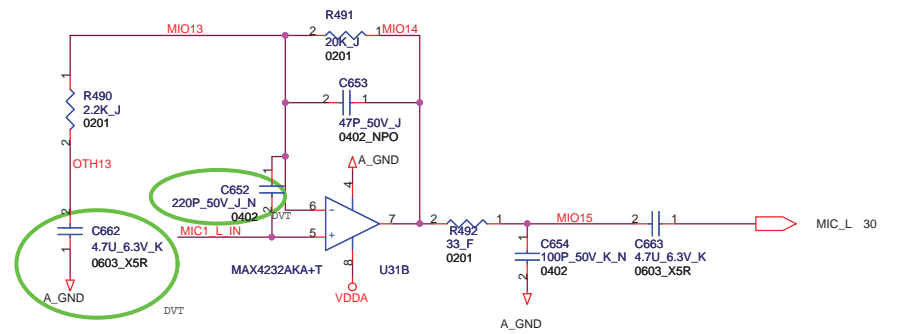
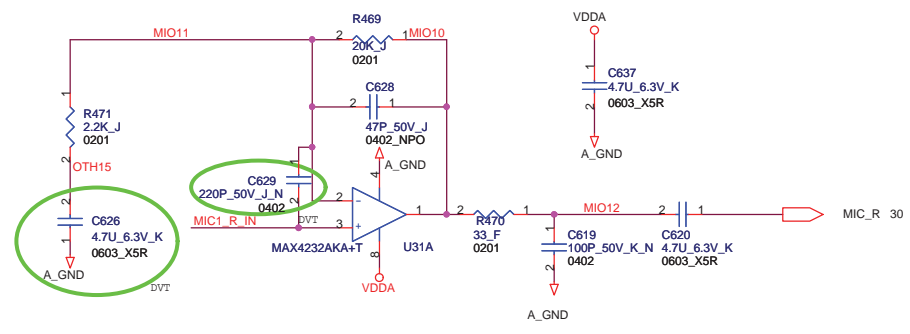
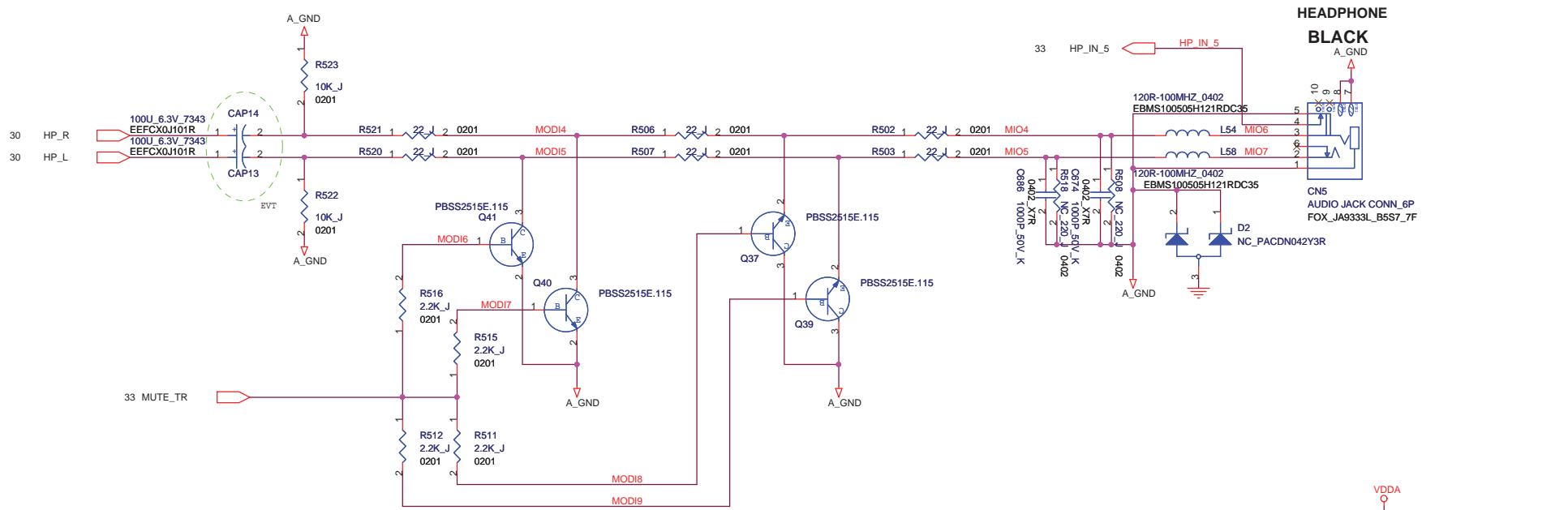


AUDIO POWER (4.75V/200mA)

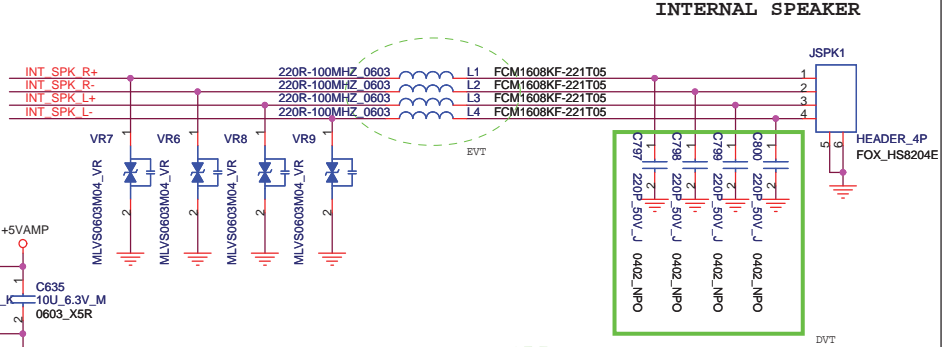
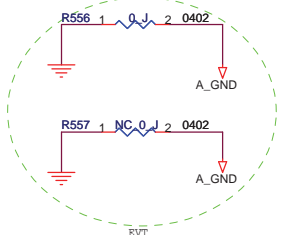
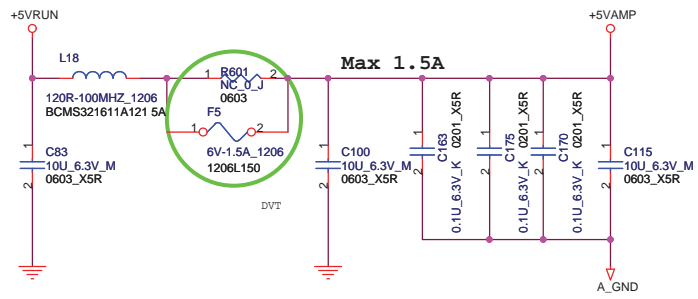


PC BEEP

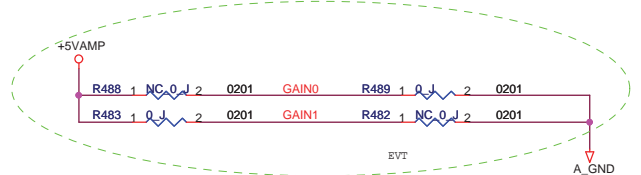
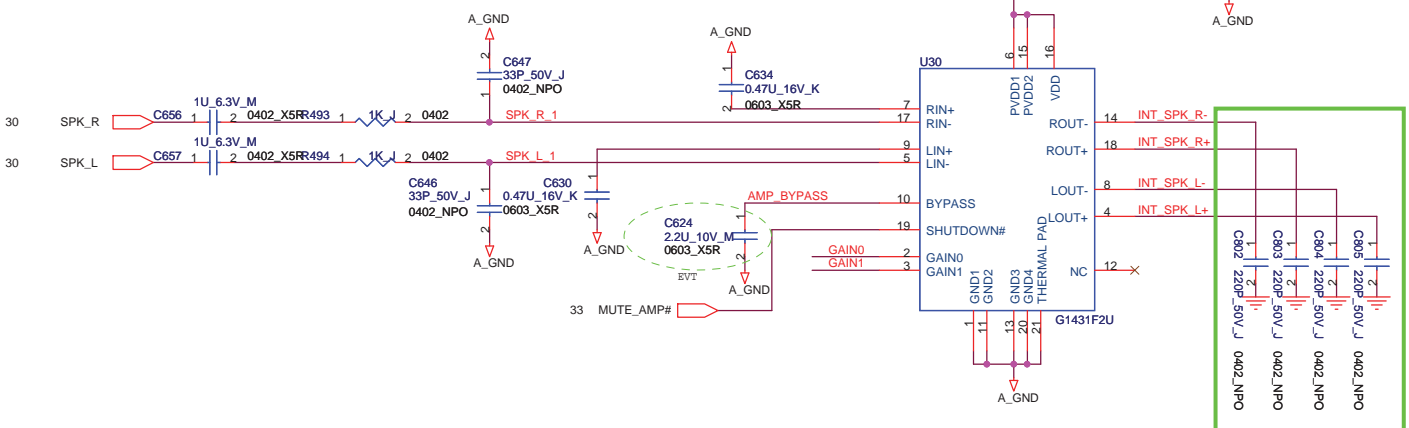




<http://hobi-elektronika.net>

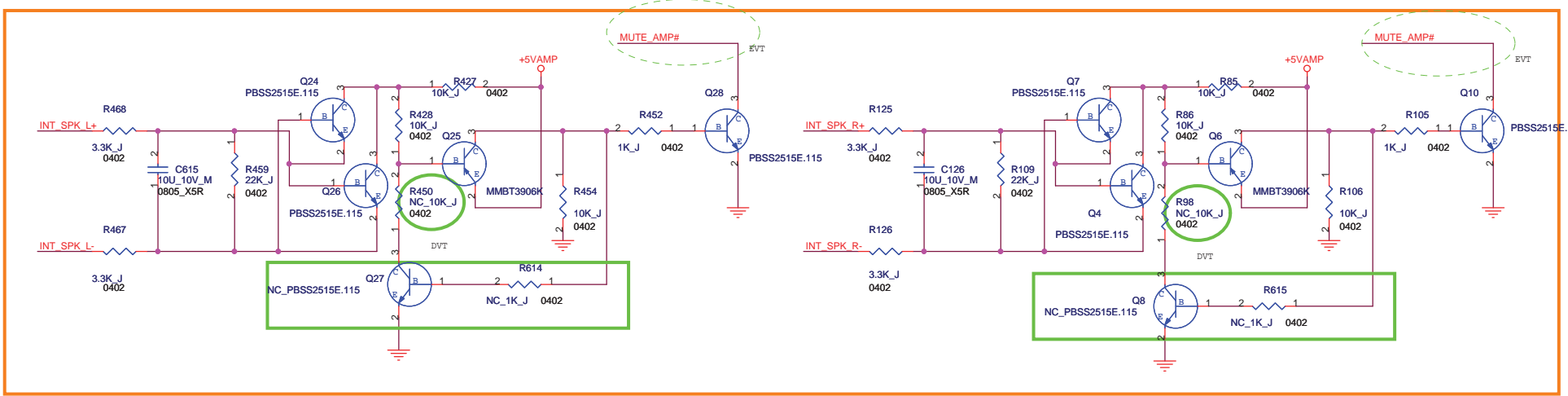


SPEAKER AMP

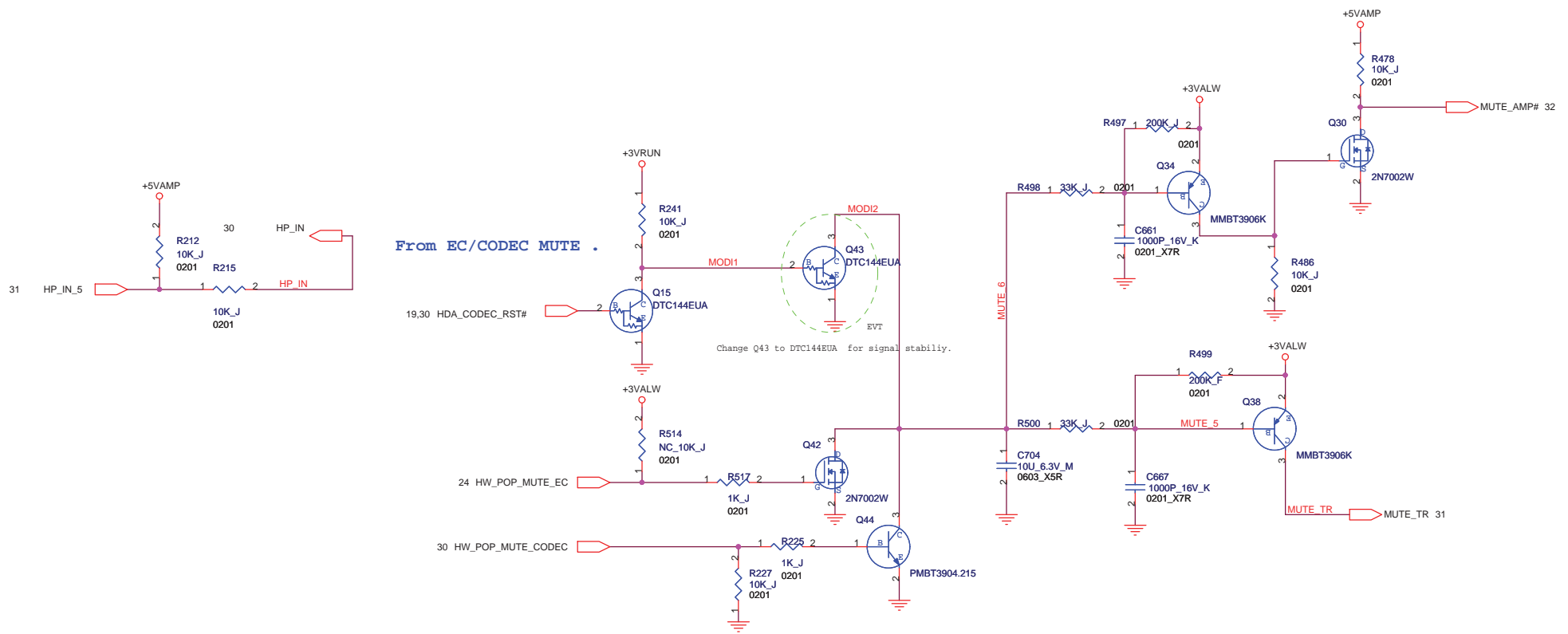


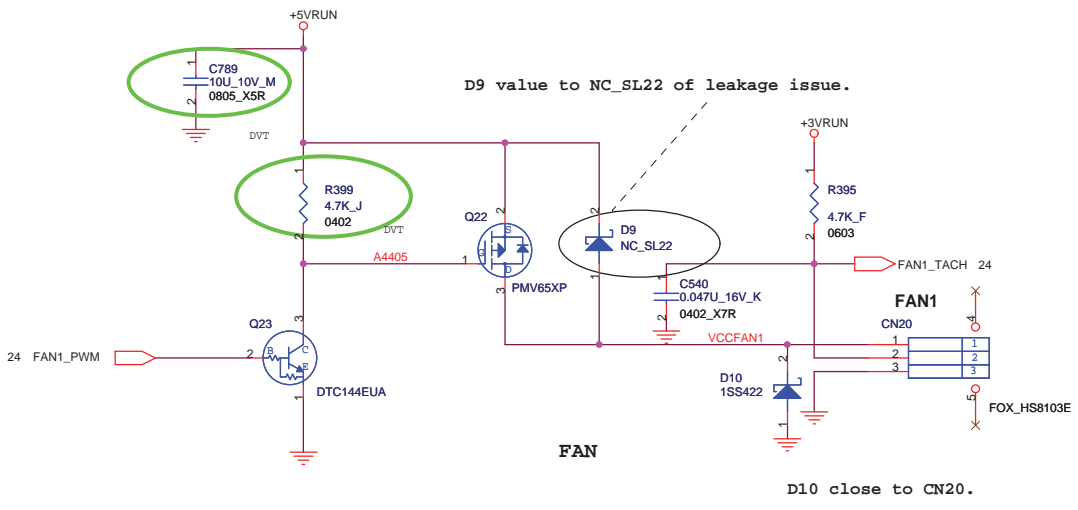
SPEAKER AMP

	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

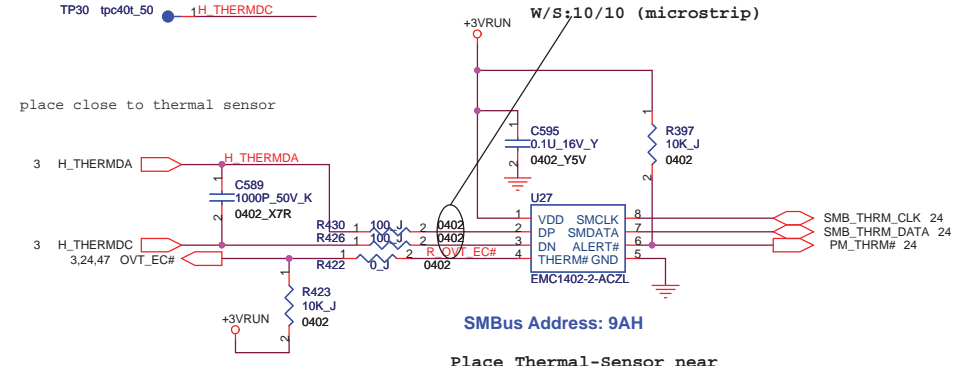


For Mor request, add the speaker cable short protection circuit

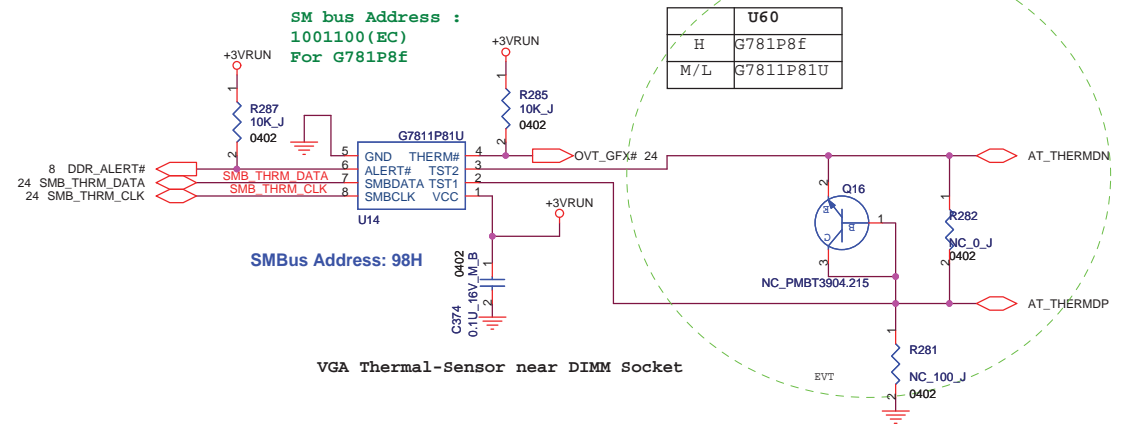


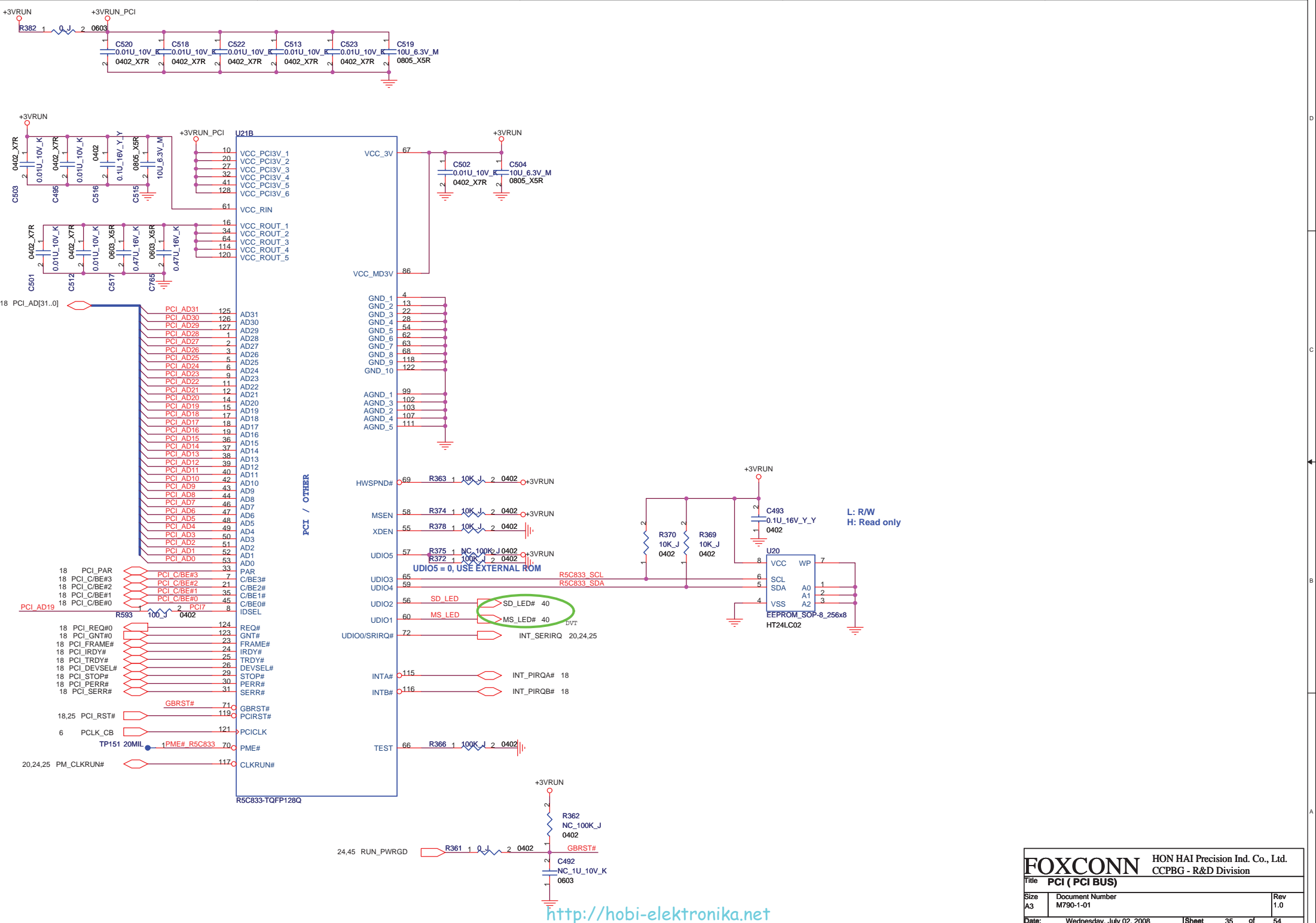


TP28 tpc40t_50 1H_THERMDA
 TP30 tpc40t_50 1H_THERMDC



CPU Thermal-Sensor



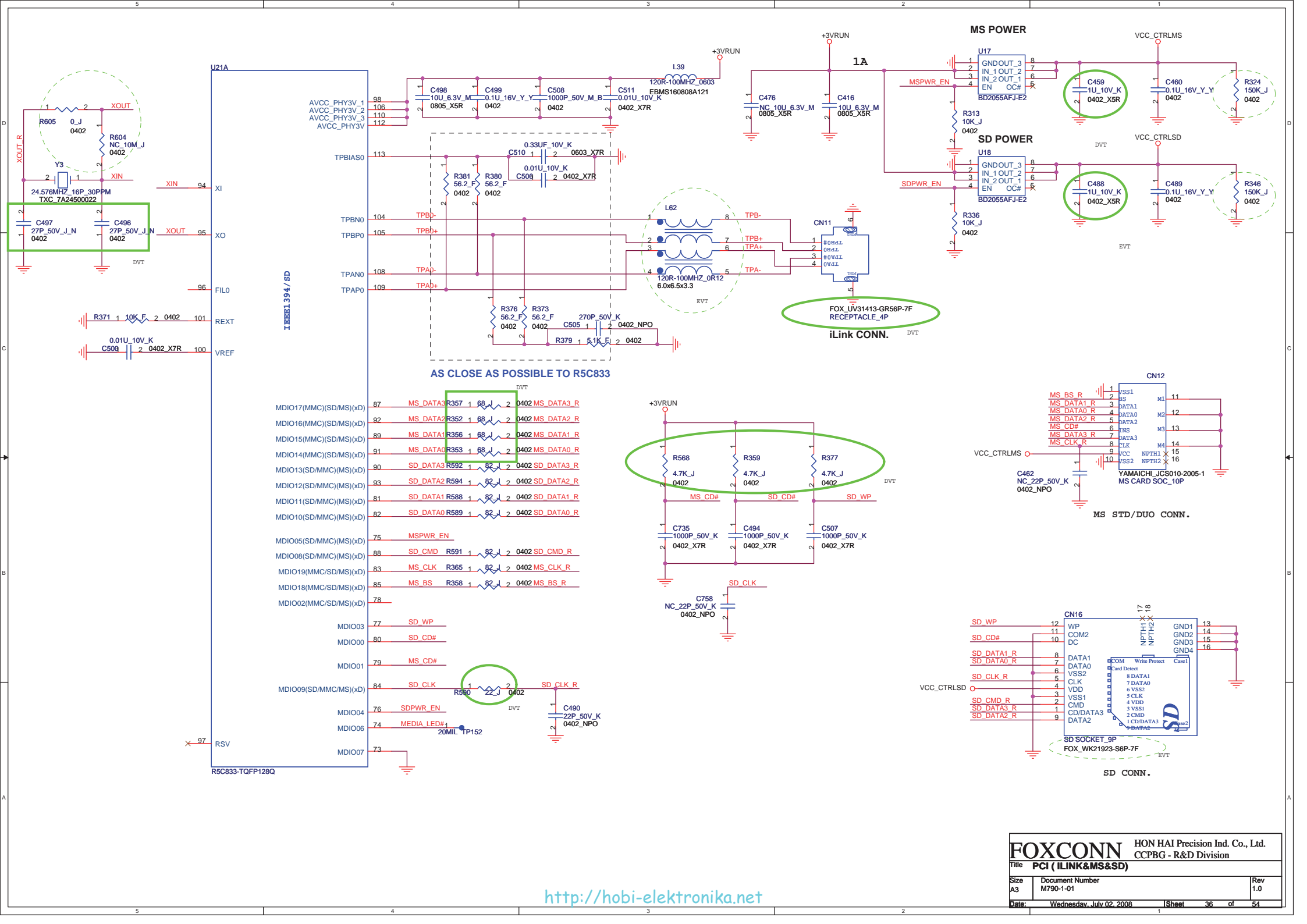


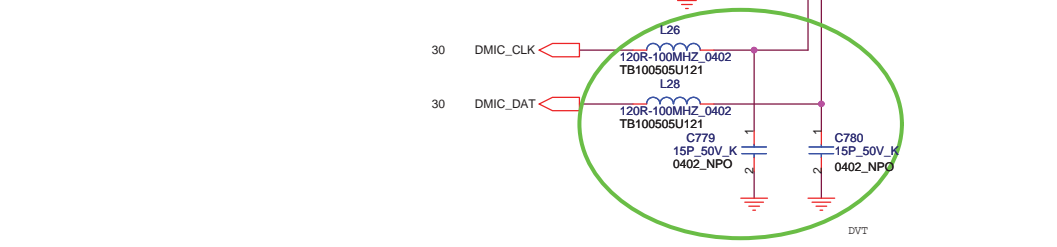
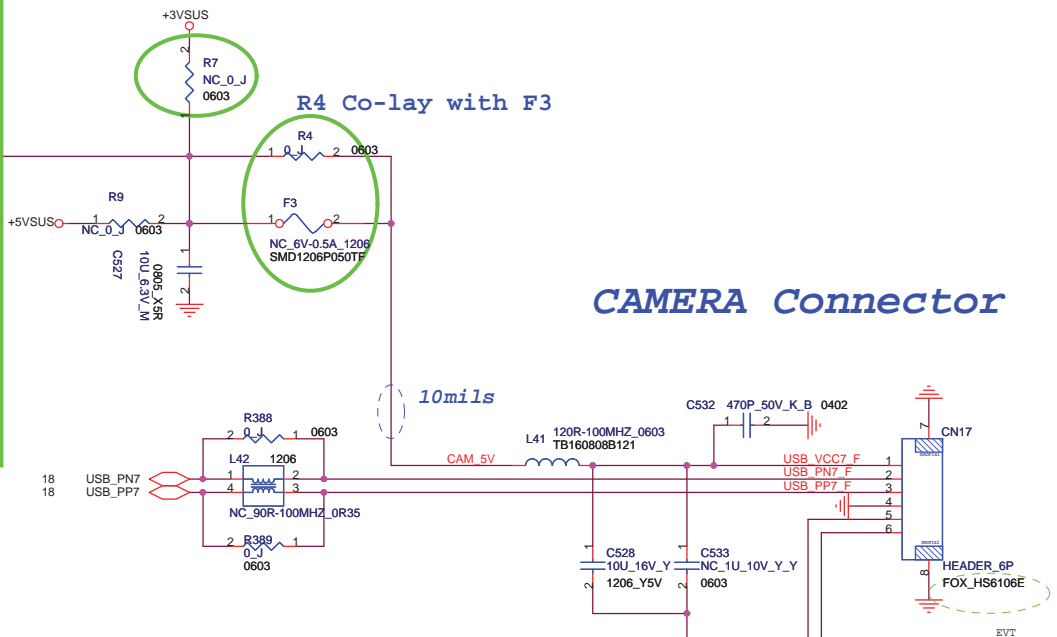
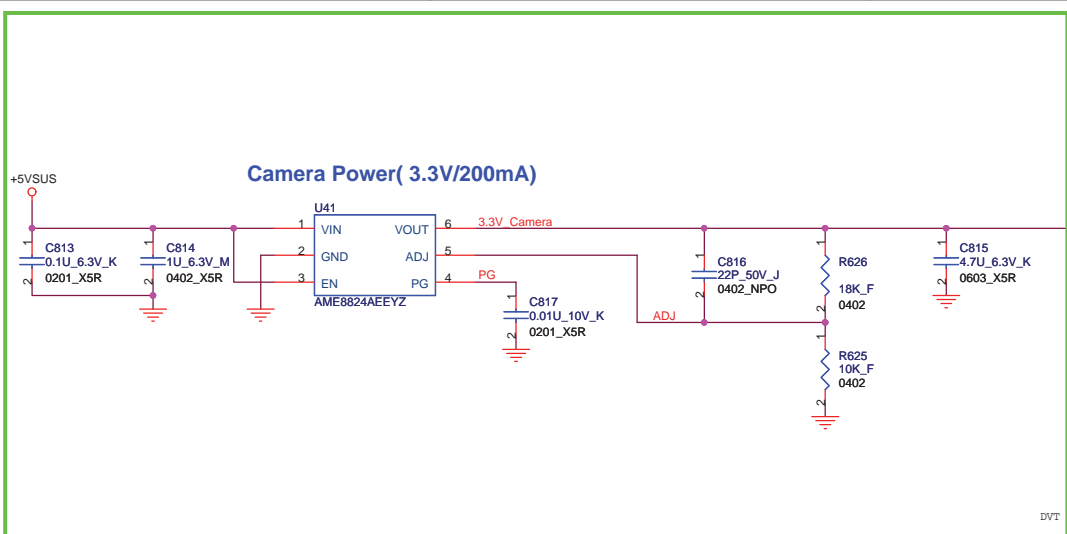
PCI / OTHER

L: R/W
H: Read only

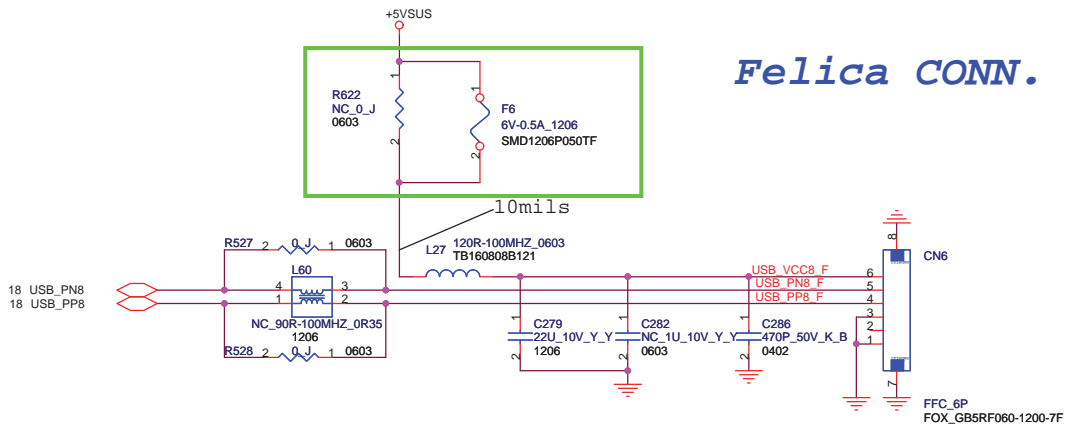
<http://hobi-elektronika.net>

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title PCI (PCI BUS)		
Size A3	Document Number M790-1-01	Rev 1.0
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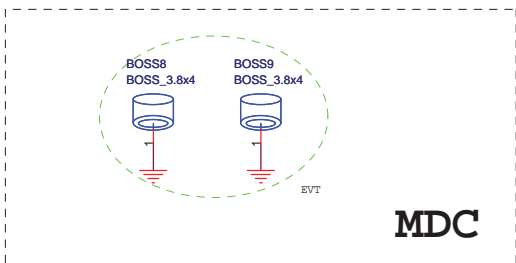
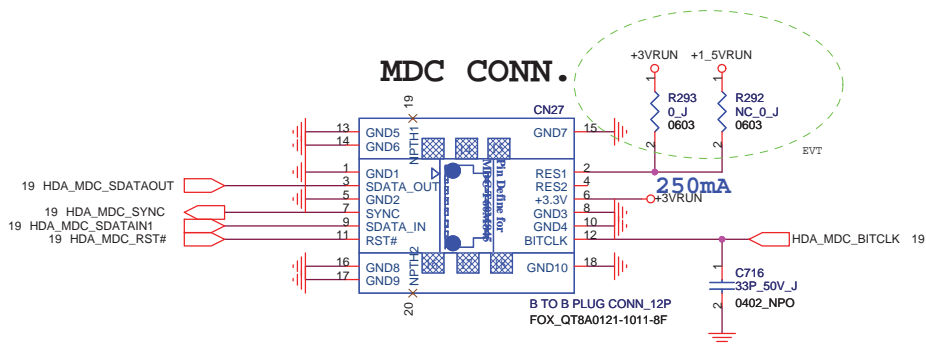


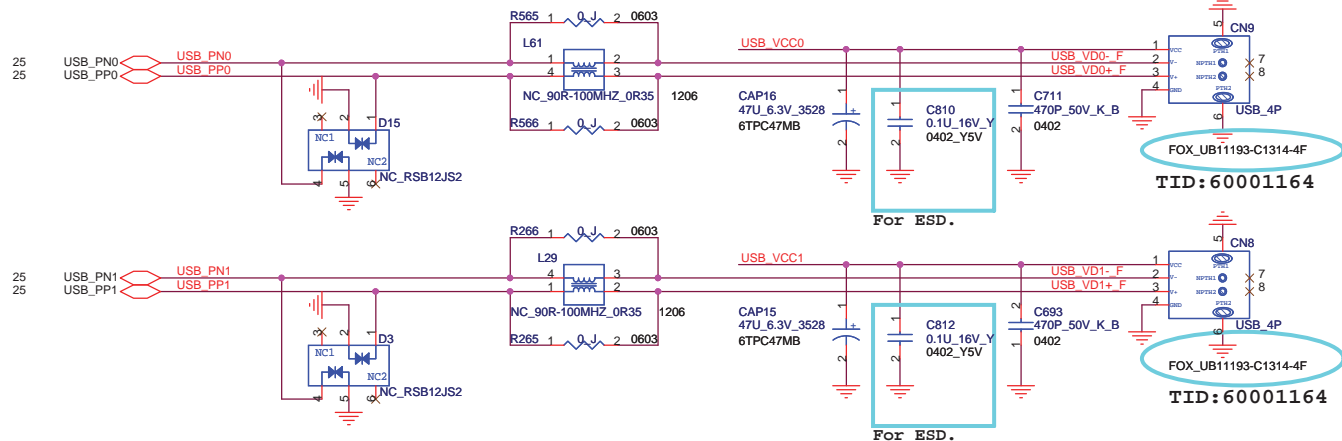
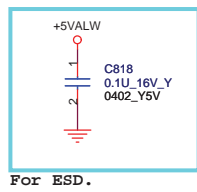
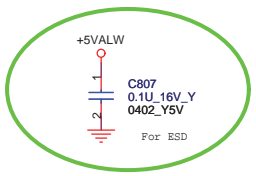
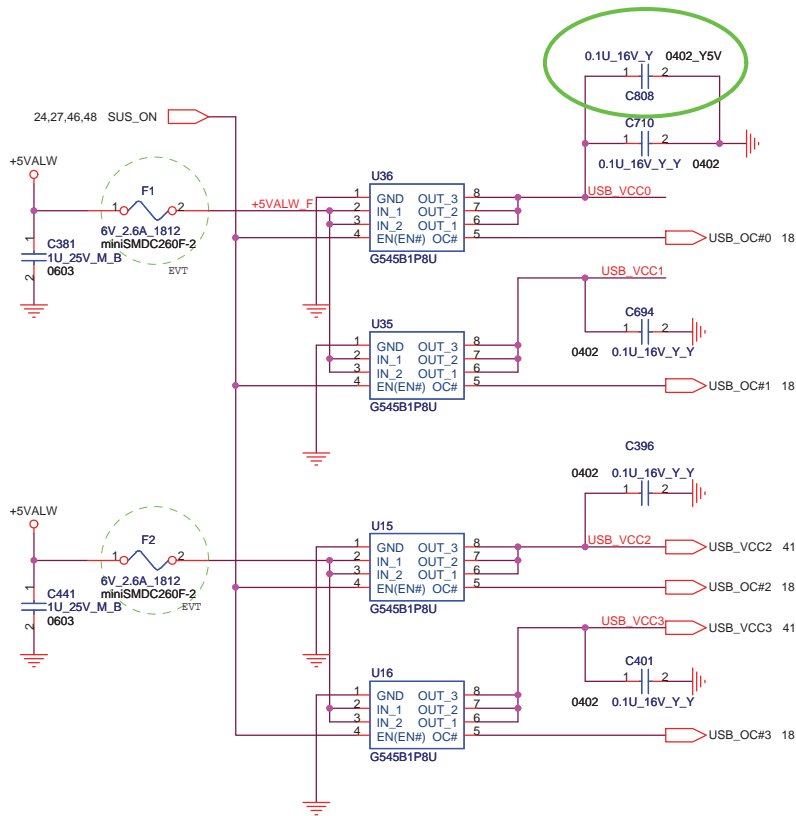


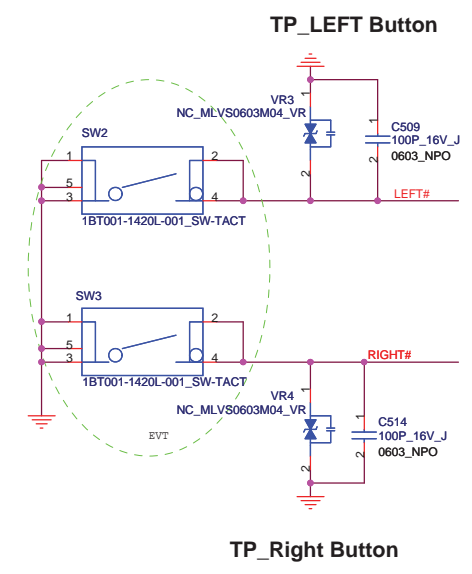
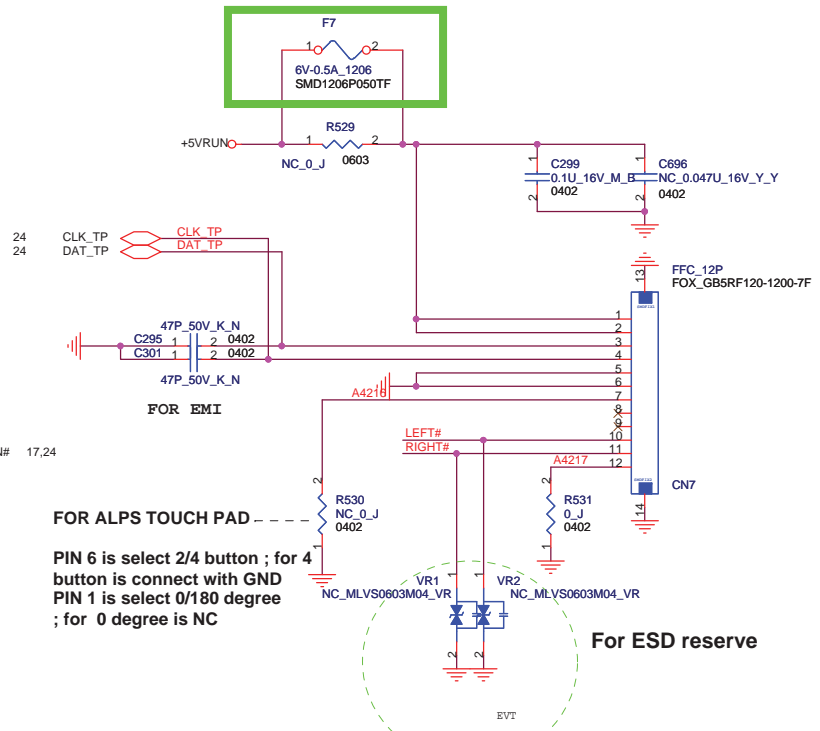
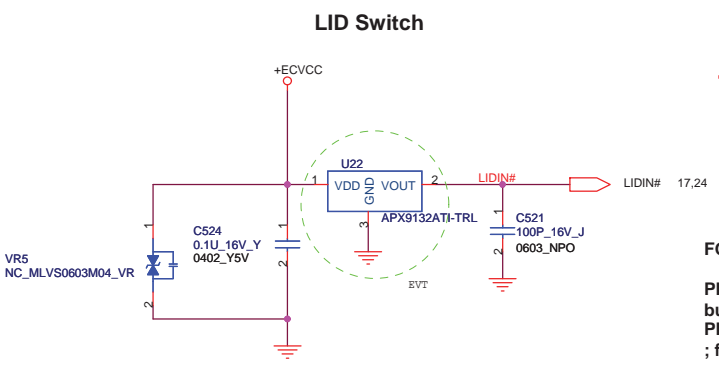
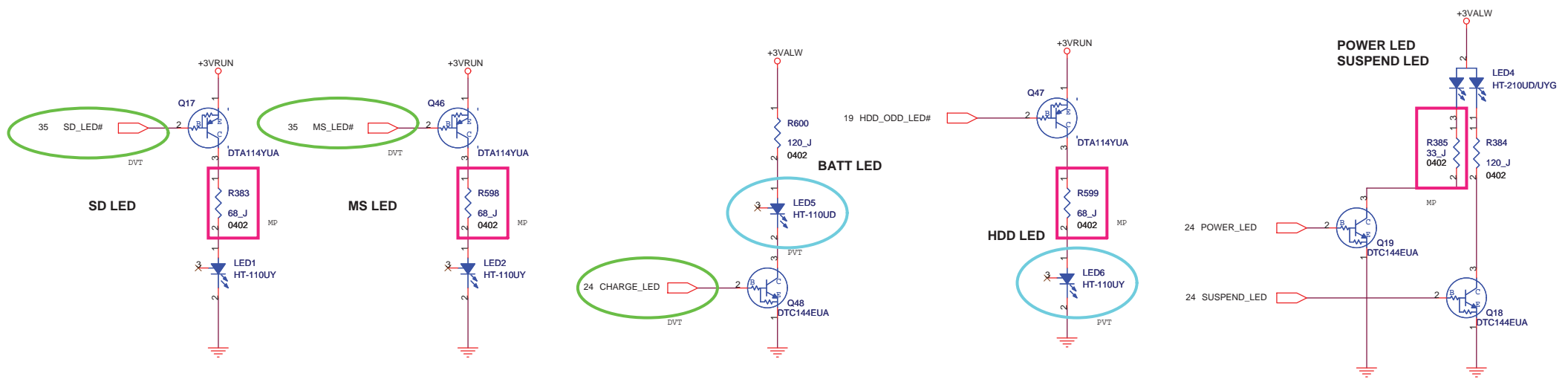
Felica CONN.



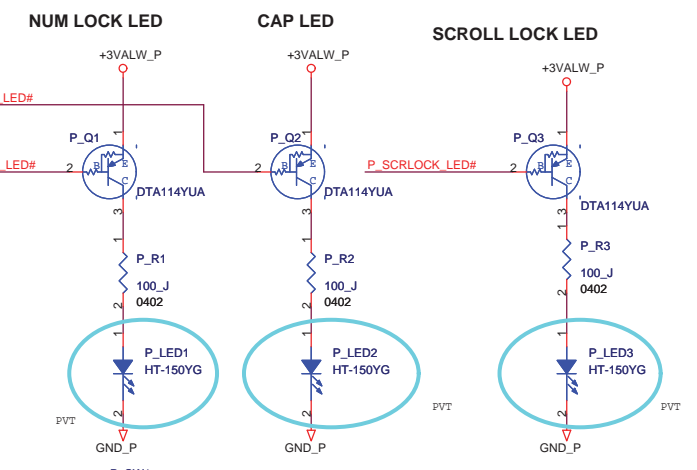
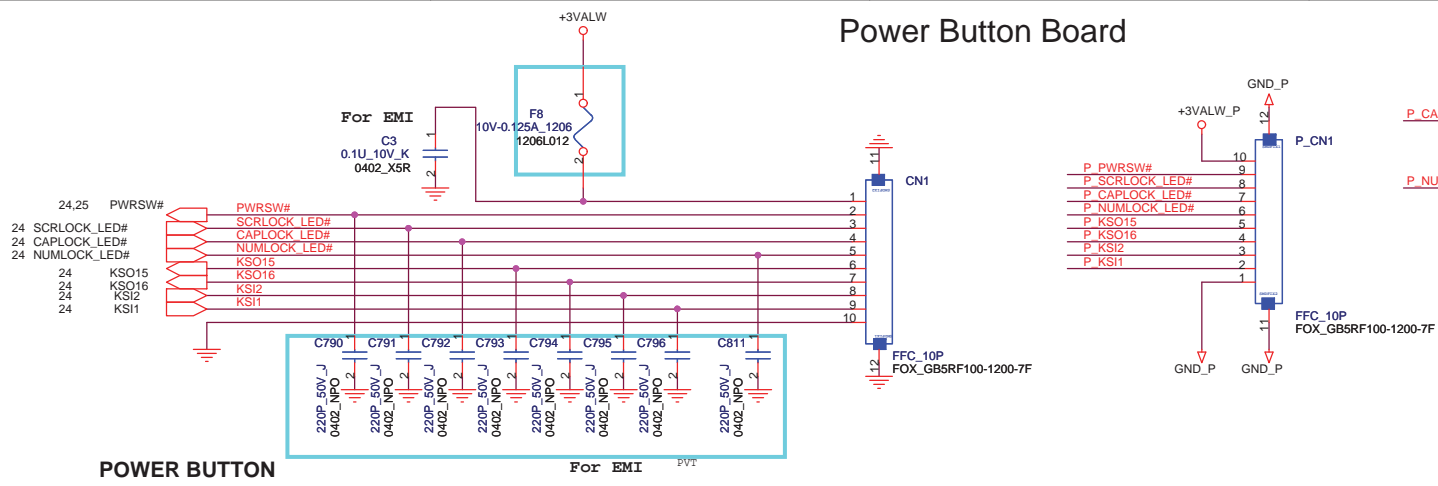
MDC CONN.



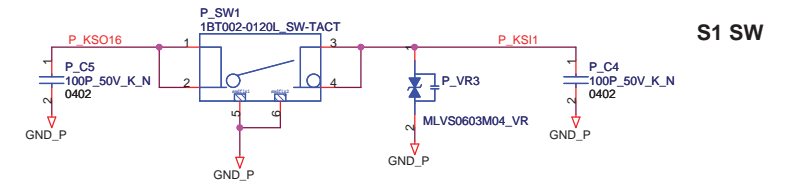
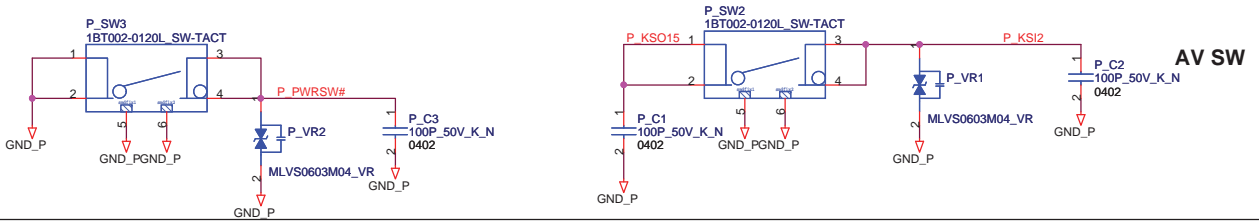




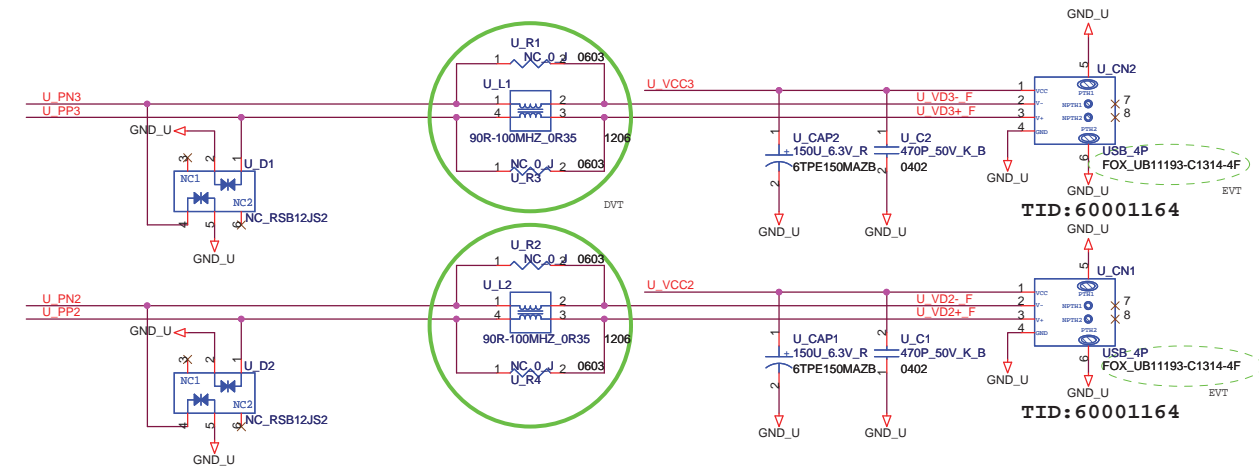
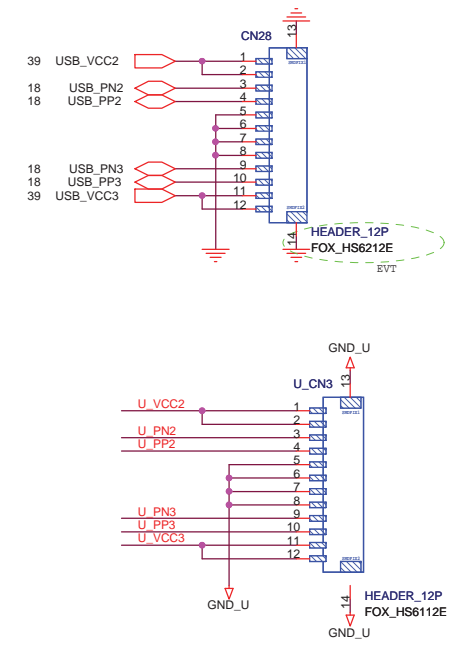
Power Button Board

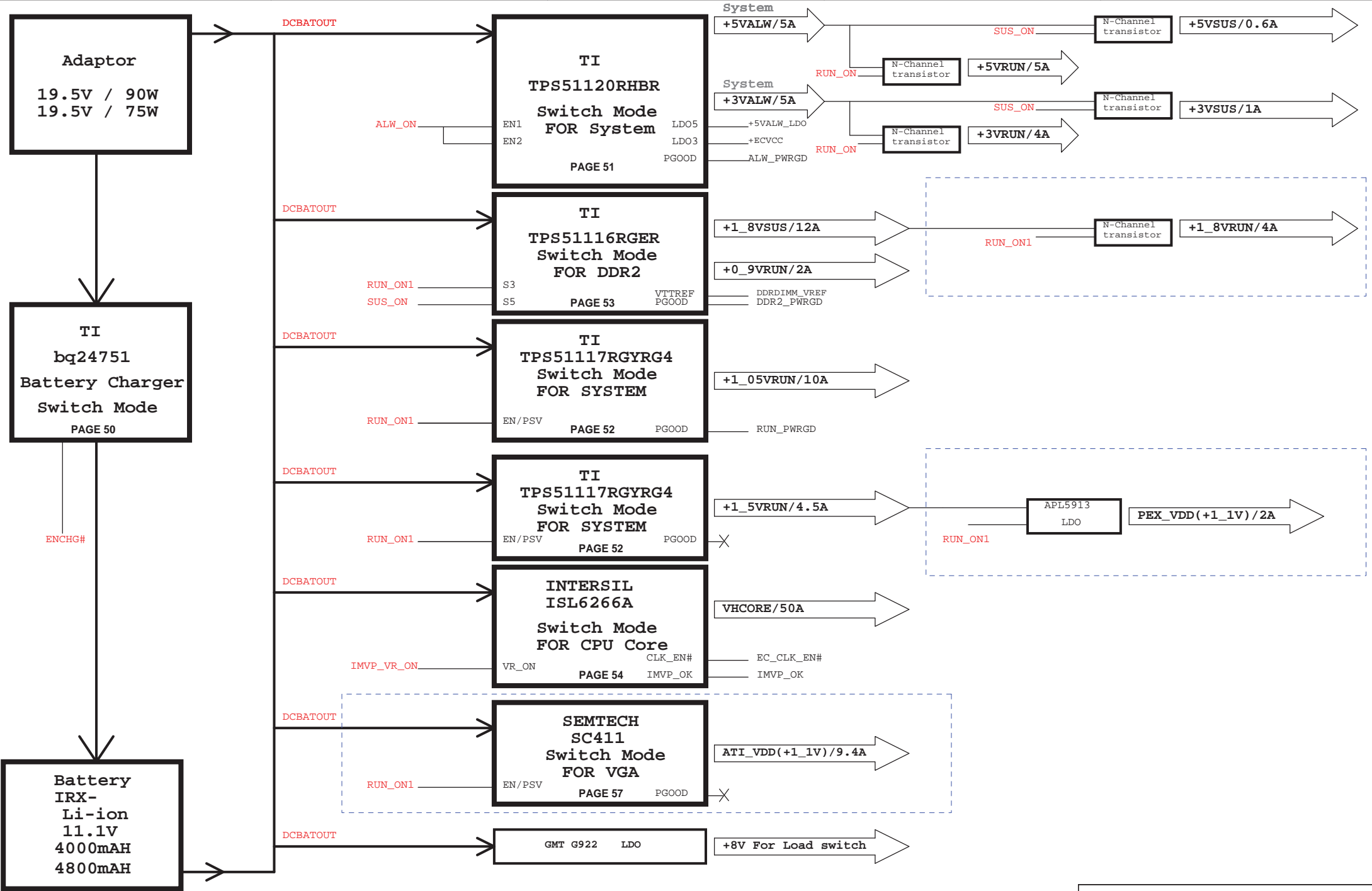


POWER BUTTON

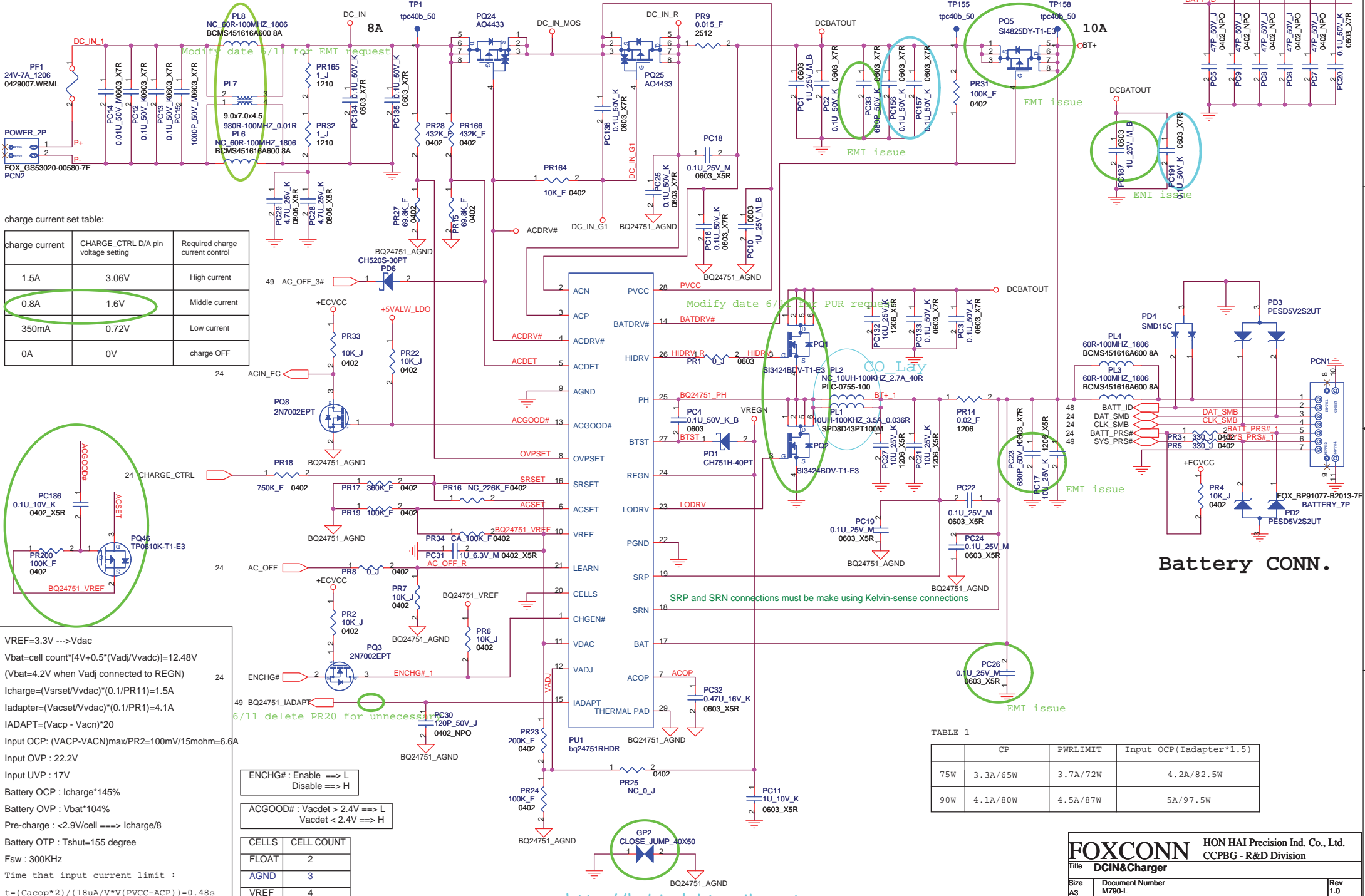


USB Board





ACP and ACN connections must be make using Kelvin-sense connections



charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V --->Vdac
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{dac})] = 12.48V$
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to } REGN)$
 $I_{charge} = (V_{srset} / V_{dac}) * (0.1 / PR11) = 1.5A$
 $I_{adapter} = (V_{acset} / V_{dac}) * (0.1 / PR1) = 4.1A$
 $IADAPT = (V_{acp} - V_{vacn}) * 20$
 Input OCP: $(V_{acp} - V_{vacn})_{max} / PR2 = 100mV / 15mohm = 6.6A$
 Input OVP: 22.2V
 Input UVP: 17V
 Battery OCP: $I_{charge} * 145\%$
 Battery OVP: $V_{bat} * 104\%$
 Pre-charge: $< 2.9V / \text{cell} \implies I_{charge} / 8$
 Battery OTP: $T_{shut} = 155 \text{ degree}$
 $F_{sw} = 300KHz$
 Time that input current limit :
 $t = (C_{acop} * 2) / (18uA * V * (PVCC - ACP)) = 0.48s$

ENCHG# : Enable ==> L Disable ==> H	
ACGOOD# : Vacdet > 2.4V ==> L Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

TABLE 1

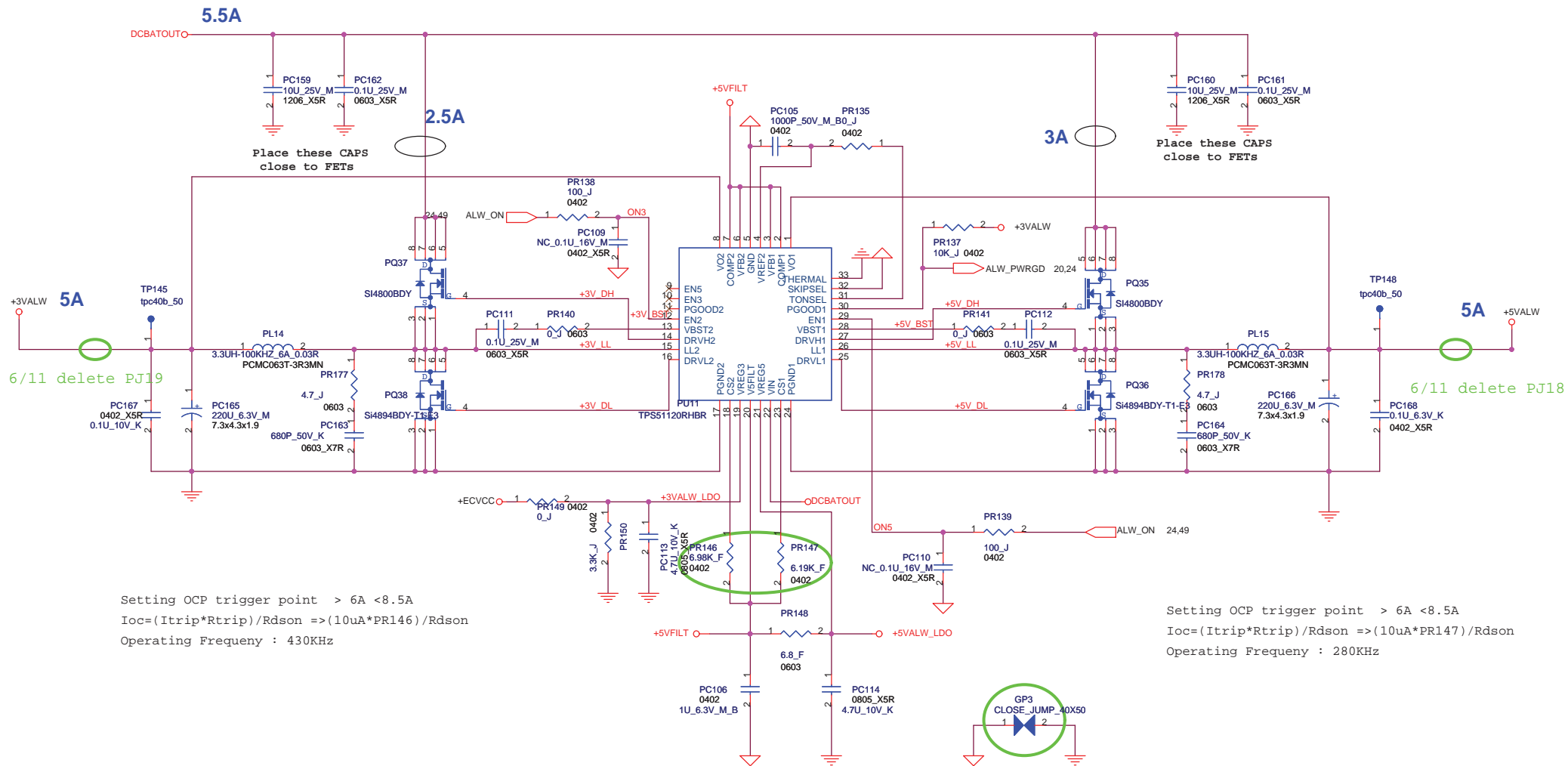
	CP	PWRLIMIT	Input OCP(Iadapter*1.5)
75W	3.3A/65W	3.7A/72W	4.2A/82.5W
90W	4.1A/80W	4.5A/87W	5A/97.5W

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **DCIN&Charger**

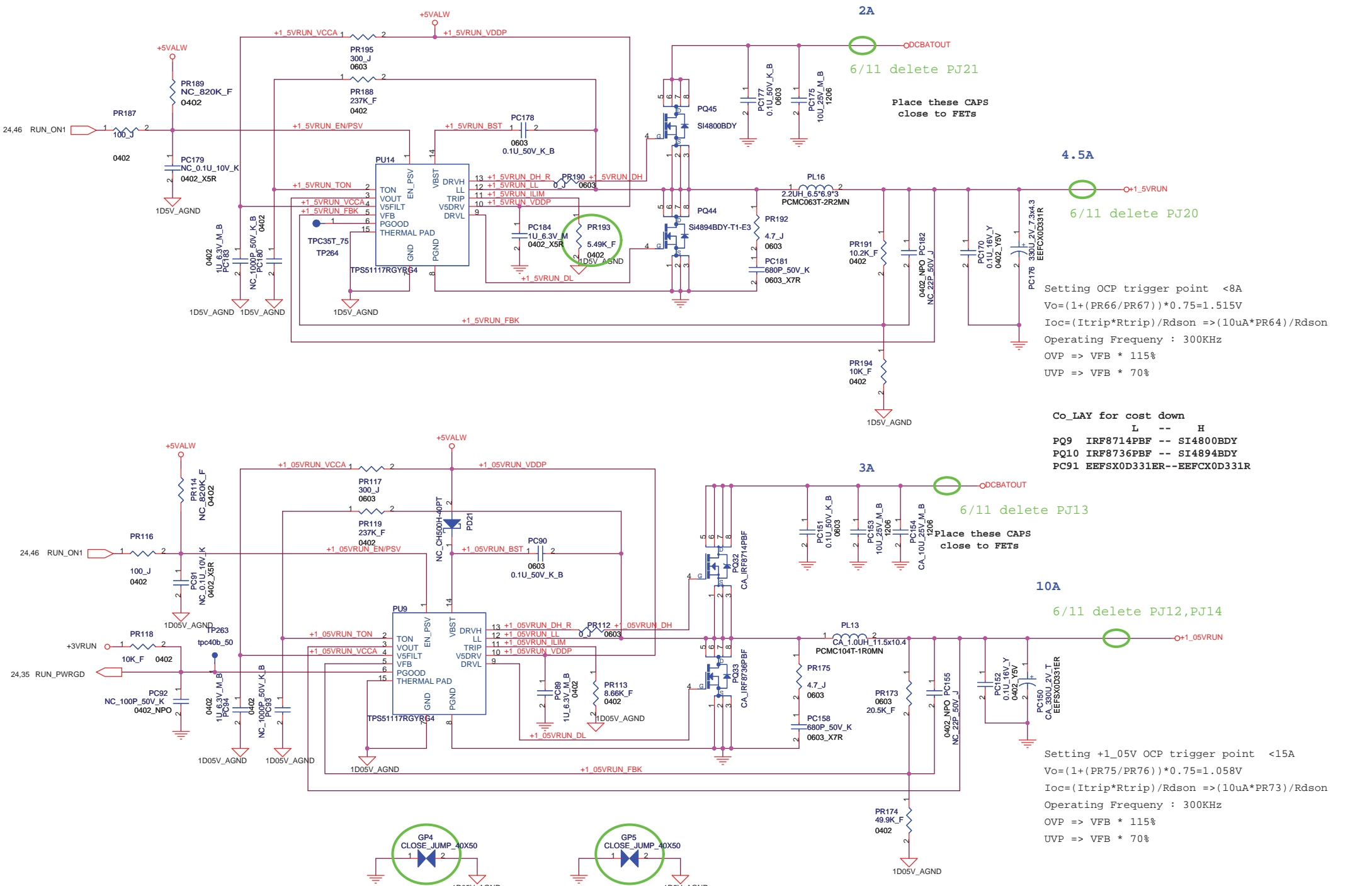
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Setting OCP trigger point > 6A < 8.5A
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR146) / R_{dson}$
 Operating Frequency : 430KHz

Setting OCP trigger point > 6A < 8.5A
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR147) / R_{dson}$
 Operating Frequency : 280KHz

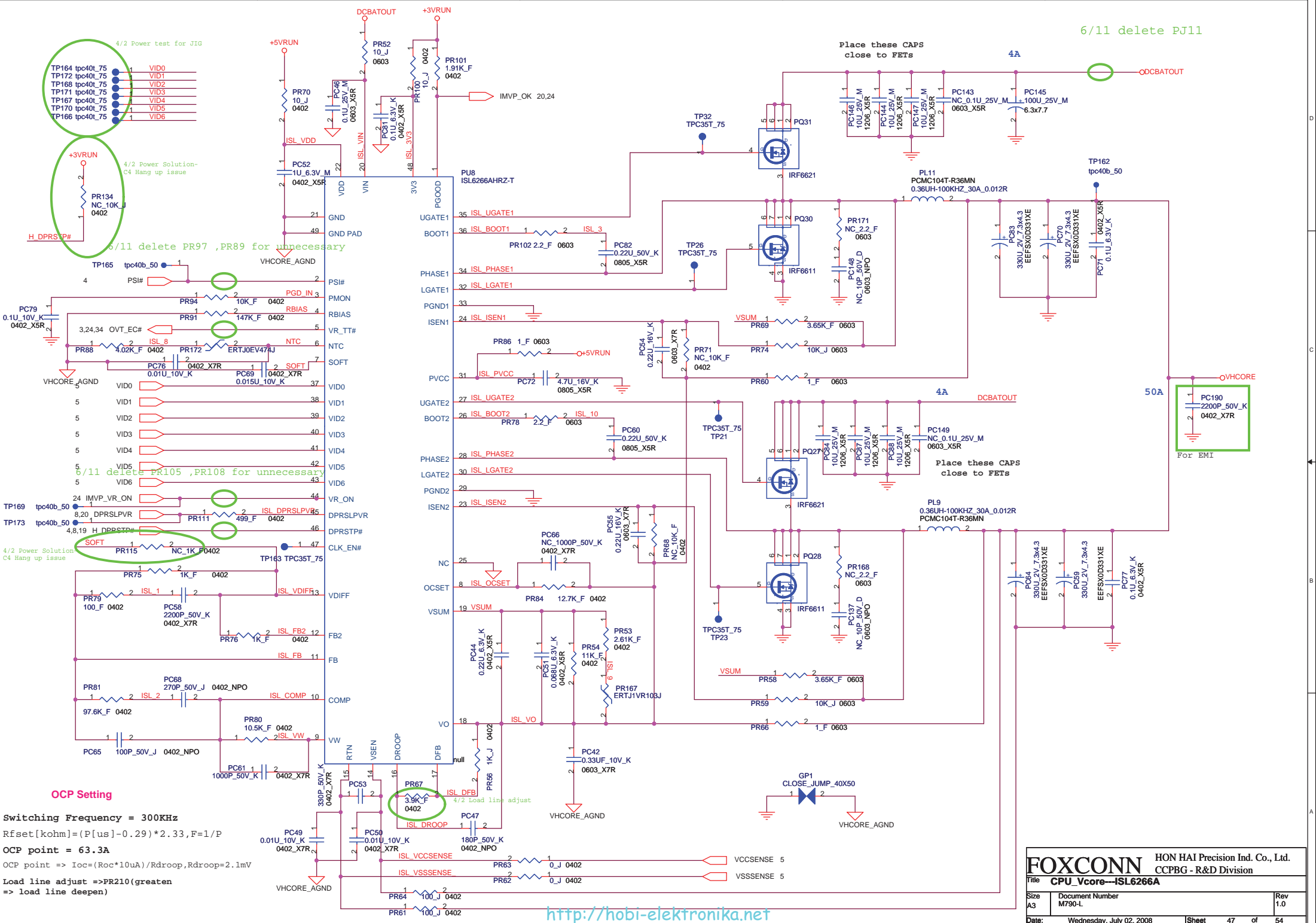


Setting OCP trigger point <8A
 $V_o = (1 + (PR66/PR67)) * 0.75 = 1.515V$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR64) / R_{dson}$
 Operating Frequency : 300KHz
 OVP => VFB * 115%
 UVP => VFB * 70%

Co_LAY for cost down
 L -- H
 PQ9 IRF8714PBF -- SI4800BDY
 PQ10 IRF8736PBF -- SI4894BDY
 PC91 EEFSX0D331ER--EEFCX0D331R

Setting +1_05V OCP trigger point <15A
 $V_o = (1 + (PR75/PR76)) * 0.75 = 1.058V$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR73) / R_{dson}$
 Operating Frequency : 300KHz
 OVP => VFB * 115%
 UVP => VFB * 70%

FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title SYS Power(+1_5V/+1_05V)	
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6/11 delete PJ11

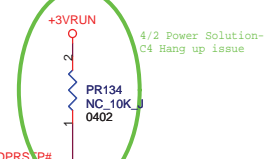
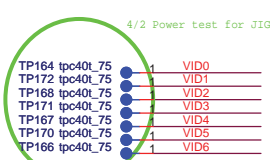
Place these CAPS close to FETs

4A

50A

Place these CAPS close to FETs

For EMI



6/11 delete PR97 ,PR89 for unnecessary

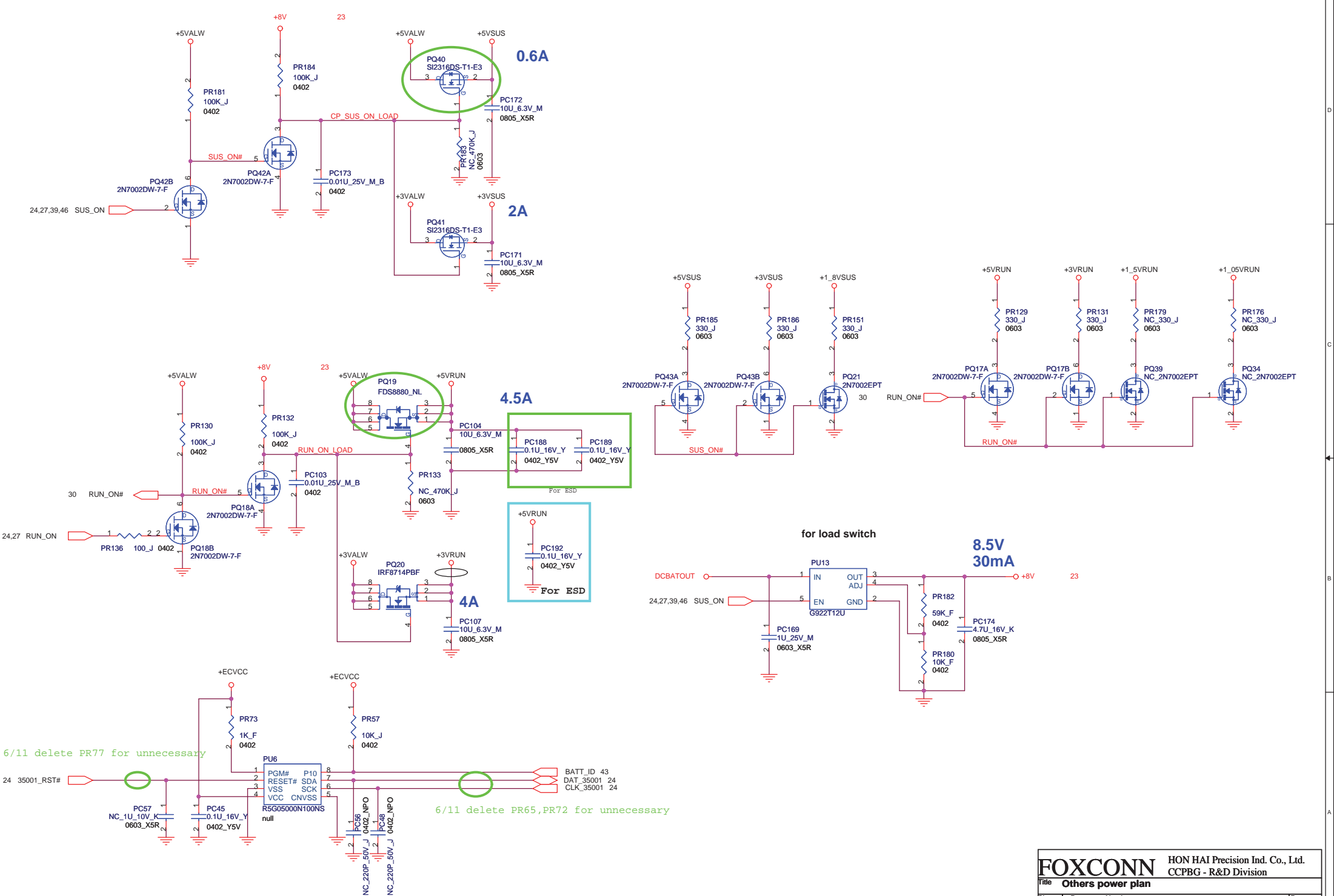
6/11 delete PR105 ,PR108 for unnecessary

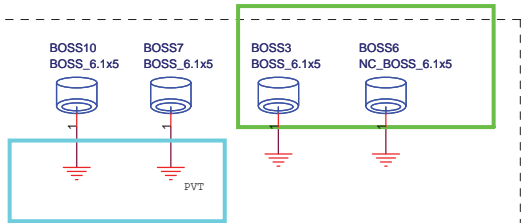
4/2 Power Solution C4 Hang up issue

OCP Setting

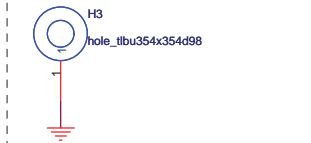
Switching Frequency = 300KHz
 $R_{fset}[\text{kohm}] = (P_{us} - 0.29) * 2.33, F=1/P$
 OCP point = 63.3A
 OCP point => $I_{oc} = (R_{oc} * 10\mu A) / R_{droop}, R_{droop} = 2.1\text{mV}$
 Load line adjust => PR210(greaten => load line deepen)

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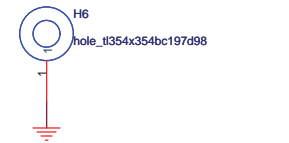




Thermal Module



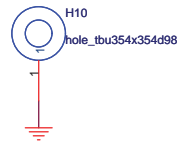
Near CRT



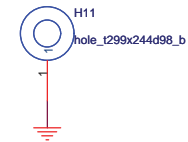
Near AUDIO



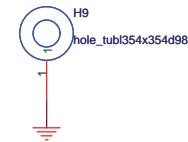
Near USB



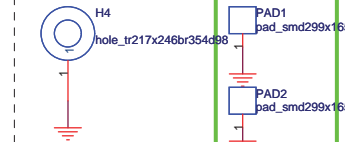
Near Express card



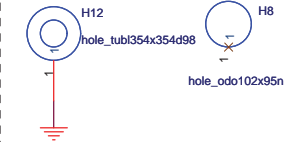
Near SD card



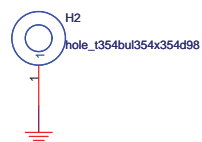
Near MS card



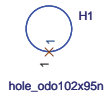
Near ODD



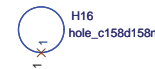
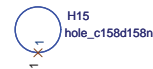
Near DC-IN



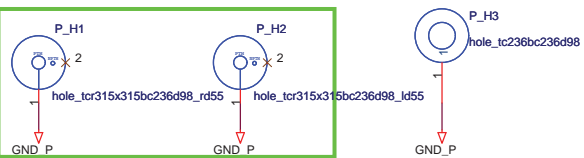
Near Robson



Near HDD

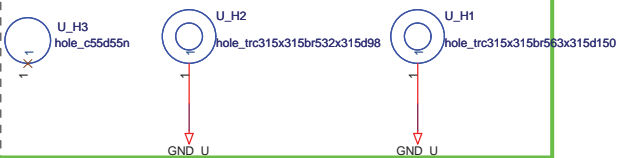
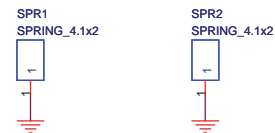


CPU



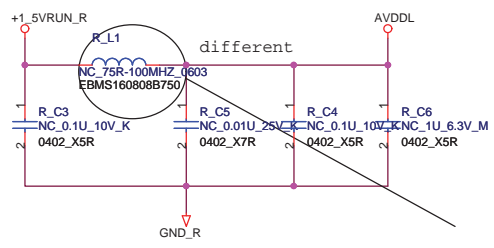
Power board

Finger

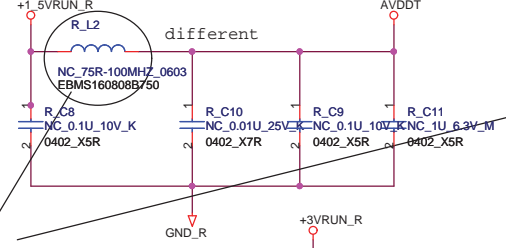


USB board

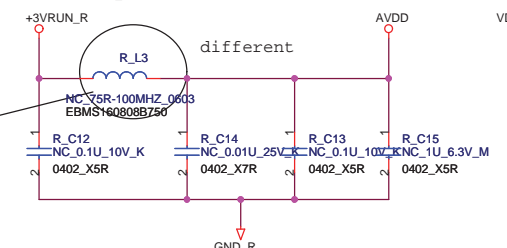
LAYOUT NOTE:
Place as close as possible
to AVDDL pins of Diamond Lake



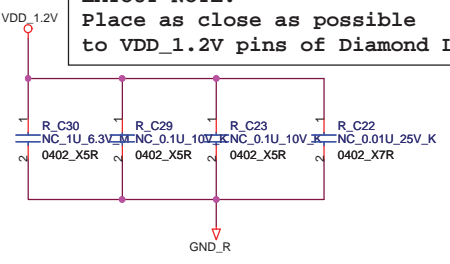
LAYOUT NOTE:
Place as close as possible
to AVDDT pins of Diamond Lake



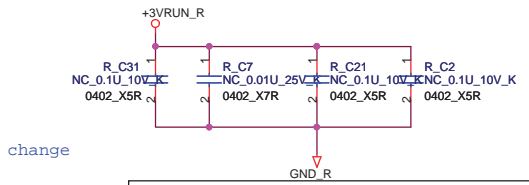
LAYOUT NOTE:
Place as close as possible
to AVDD pins of Diamond Lake



LAYOUT NOTE:
Place as close as possible
to VDD_1.2V pins of Diamond Lake



Intel sch use 70ohm /100MHZ



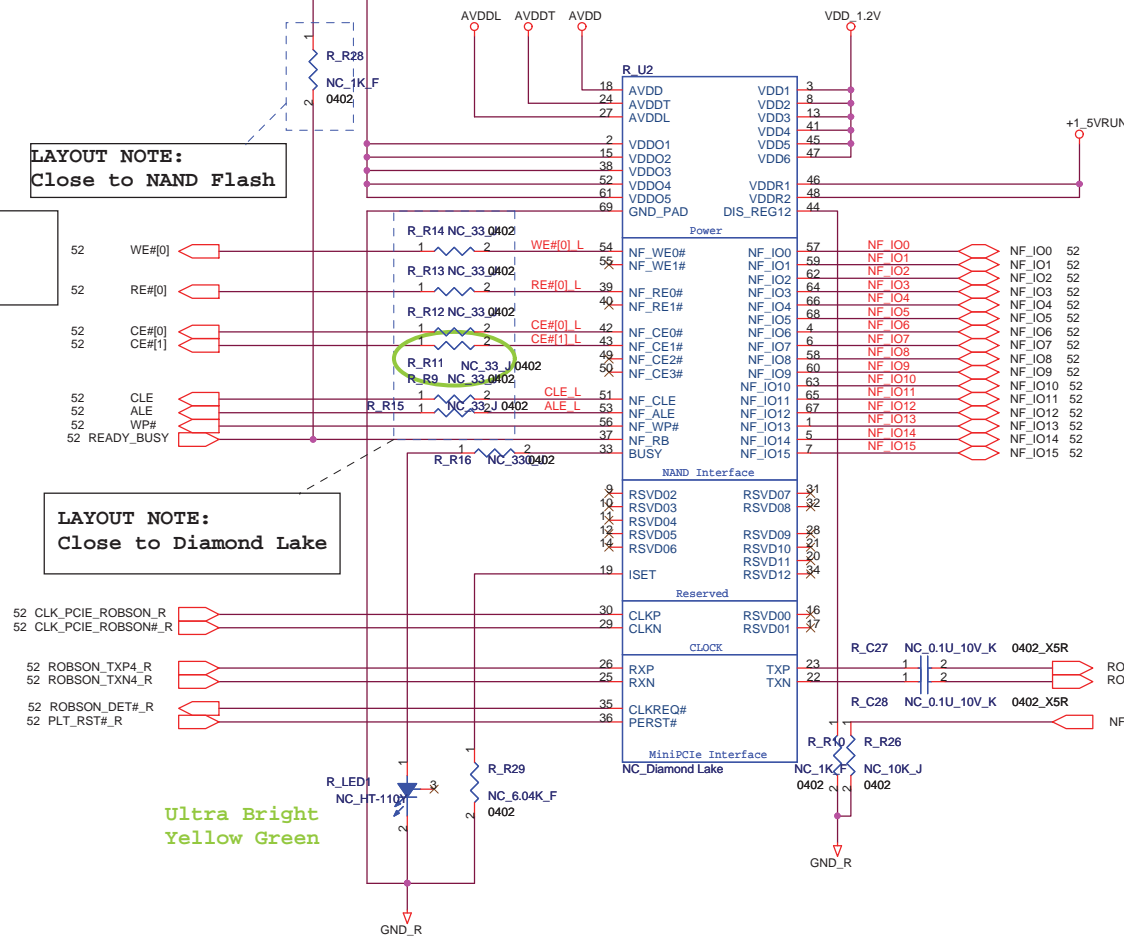
change

LAYOUT NOTE:
Place as close as possible
to +3VRUN pins of Diamond Lake

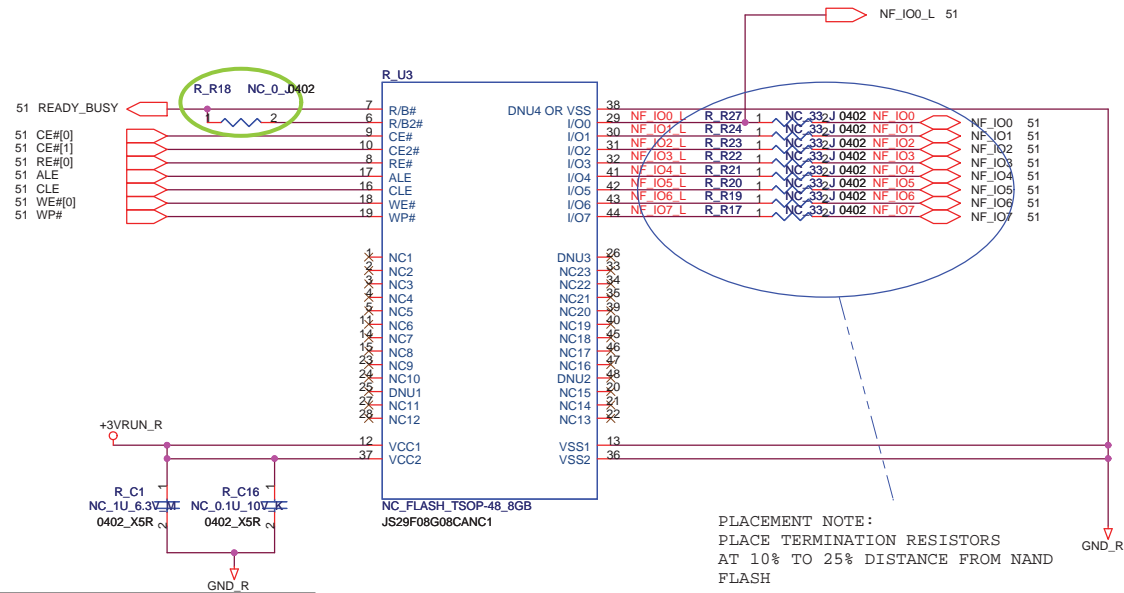
LAYOUT NOTE:
Close to NAND Flash

LAYOUT NOTE:
Close to Diamond Lake

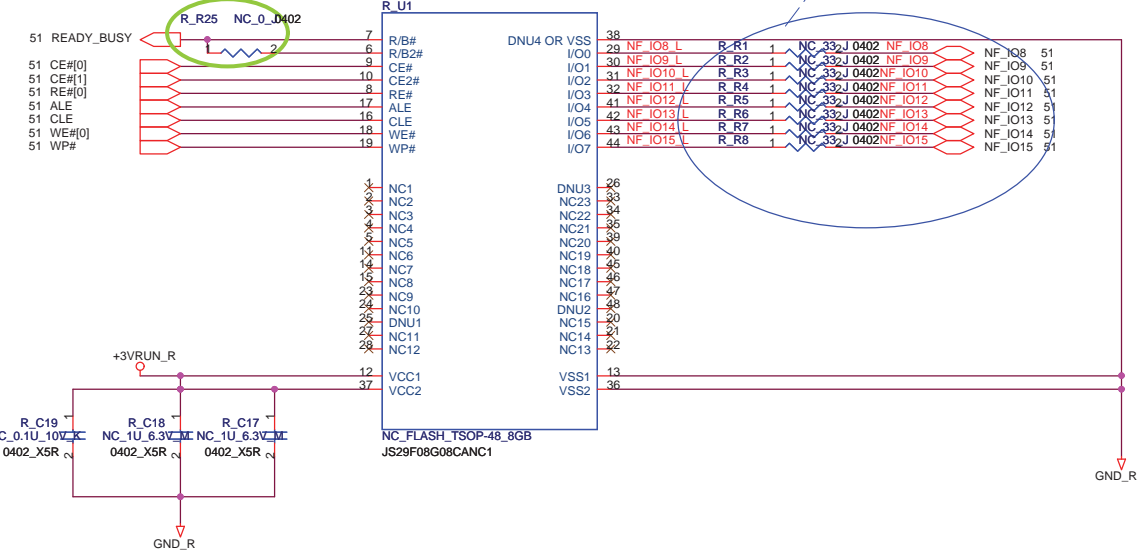
LAYOUT NOTE:
Place as close as possible
to VDDR1 and VDDR2 pins
of Diamond Lake



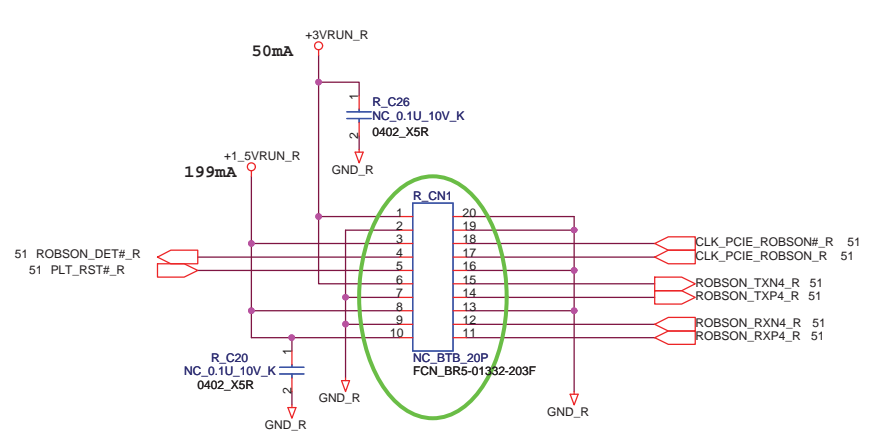
Ultra Bright
Yellow Green



LAYOUT NOTE:
Place as close as possible
to +3VRUN pins of R_U3

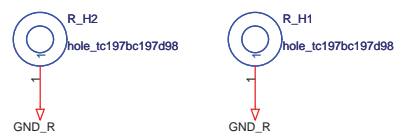


LAYOUT NOTE:
Place as close as possible
to +3VRUN pins of R_U1



will change the connector type to bluetooth connector

ROBSON Board CONN



M790 EVT

(2008/01/23)

Update 8Layer H/L versio to 6Layer L version.

(2008/01/24)

Page 6. Change Clock to B version.

Page 25. Change SPI rom to new version.

Page 36. Change L62,delete L63 same as M760.

(2008/01/28)

Page 14/15. Add C767~C778 for EMI reserve.

Page 19. Add R610 damping resistor for adjustment for MOR request.

Page 20. Change GPIO18,20 to GPIO36,37 and delete R269,R270.

Page 23. Change D13 to mount.

Page 24. Change RP39,RP41 to +3VALW.Add D17,D18 for EC leakage current issue.

Page 29. Add R602,R603 damping resistor for adjustment for MOR request.

Page 32. Add R601 for MOR request.

Page 36. Add R604,R605 damping resistor for adjustment for MOR request.

Page 37. Add R611,R612,C779,C780 for EMI reserve.

Page 48. Change PQ40 from SI2304BDS-T1-E3 to SI2316DS-T1-E3 and Change PQ19 from IRF8714PBF to FDS8880_NL for MOR request.

(2008/01/29)

Page 50. Add H13~H16,P_H3.

(2008/01/30)

Page 50. Update H4,U_H1,U_H2.

(2008/01/31)

Page 20. Not AMT support,so delete R556, R557 and C722.

Page 32. Change GP2,GP3 to R556,R557.

Page 33. Change R486 connect to D_GND.

Page 50. Add Boss10.

(2008/02/01)

Page 49. Change PJ17 from PD13 pin1 to pin2.

(2008/02/02)

Page 17/24. Add FAN error detect function in panel switch pin4.

Page 32. Change C624 to 2.2uF for pop noise issue.

(2008/02/14)

Update some error discription for MOR request.

(2008/02/18)

Page 32. Mount Audio cable short components for EVT test.

(2008/02/20)

Page 32. Change U30 from TI(TPA6017) to GMT(G1431F2U) for pop noise issue.

(2008/02/21)

Page 17. Update Panel ID table.

Page 24. Update R447 CA to Mount,R437 Mount to CA.

Page 46. Add PJ10.

Page 14/15.Add J2/J3 for EMI request.

Page 6. Add reserverve C781,C782,C783 for EMI request.

Page 29. Add reserverve C784,C785 for EMI request.

(2008/02/22)

Page 14/15.Add J4/J5 for EMI request.

Page 6. Add reserverve C786,C787 for EMI request.

(2008/02/26)

Page 5. Change C76 from 6.3V to 10V for PUR request.

Page 11. Change C201,C225,C679,C681,C143,C168,C596,C601,C605 from 10V to 16V for PUR request.

Page 18/29. Change C32,C35,C449,C450,C725,C726,C727,C728,C729,C730 to 0.1uF,6.3V,10% for PUR request.

Page 31. Change R202 for PUR request.

Page 31. Change Q37,Q39,Q40,Q41 to PBSS2515E.115 for PUR request.

Page 32/33. Change Q6,Q25,Q34,Q38 to MMBT3906K for PUR request.

Page 33. Change Q33/Q44 to MMBT3904 for PUR request.

M790 DVT

(2008/02/28)

Page 33. Change Q33/Q44 to PMBT3904.215 for PUR request.

(2008/03/03)

Page 52. Change R_U1,R_U3 to 8Gbit size and change R_R11,R_R18,R_R25 to mount.

(2008/03/05)

Page 24. Mirror CN3 for Int. keyboard issue.

(2008/03/06)

Page 38. Mirror CN6 for easy A'ssy.

Page 44. Change PR146 to 6.8K,PR147 to 5.49K for OCP current adjust.

Page 45. Change PR193 to 5.49K for OCP current adjust.

(2008/03/24)

For PUR request change C624 2.2uF(1.25mm) to (0.8mm),C510/PC42 0.33uF(X5R) to (X7R).

Page 38. SWAP L60 for CN6 mirror issue.

Page 24/40. Change CHARGE_LED# low enable to H enable same as M750/M760.

(2008/03/28)

Page 24. Add C722(1000pF) for FAN speed stable.

(2008/04/02)

Page 28/51/52. Change Robson function to no mount.

(2008/04/07)

Page 23. Del PJ4 Change PJ3 type for JIG.

Page 43. Add for charger ocp improve.

Page 43~46,48. A_GND and P_GND change to GP2~6.

Page 47. Add PR134,PR115 for Power Solution- C4 Hang up issue.

Page 47. tpc40b_50 Change to tpc40t_75 power point part for JIG.

Page 49. Add Battery UVP protect for power issue.

(2008/04/08)

Page 29. Add C733,R269,R270/R616(no mount),Change R44 to 4.99Kohm and NC CTRL_LD8 circuit for 88E8057.

Page 32. Change R98,R450,Q8,Q27 to NC and Add R614,R615 no mount for speaker cable short protection circuit.

Page 35/40. Change MS/SD LED to Low active.

(2008/04/11)

Page 31. Change C182,C194 to 0.1uF for MIC THD+N issue

Page 49.Change PR199 to 215Kohm for Battery UVP adjust.

(2008/04/14)

Page 31. Change C626,C662 to 4.7uF for MIC FSIV issue.

Page 29. Design for 88E8055.

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(2008/04/14)

Page 16. Change L14,L16,L17 to 120ohm/100Mhz bead for CRT EMI issue.
Page 32. Add C797~C800(220pF)for Speaker EMI issue.
Page 37. Change R611,R612 to L26,L28 120ohm/100Mhz bead and C779,C780 to 15pF for Camera EMI issue.
Page 41. Add C790~C79(2200pF)for power board EMI issue.

(2008/04/15)

Page 50. Change Boss7 pin2 connect to RC for EMI reserve and Add Finger SPR1,SPR2 for EMI issue.
Page 32. Add C802~C805(220pF)for Speaker EMI issue.

(2008/04/18)

Page 23. Update ODD connector for MOR request.
Page 26. Add R611,R612 and Change U24,C534 to no mount for MOR request.

(2008/04/21)

Page 19. Change C388,C389 to 15pF for Y6 test fail.
Page 24. Change C245,C246 to 18pF for Y2 test fail.
Page 31. Change C629,C652 to 220pF same as M760.
Page 36. Change C496,C497 to 27pF for Y3 test fail.Change R352,R353,R356,R357 to 100ohm,R590 to 33ohm for MS/SD fail items.

(2008/04/23)

Page 16. Update CN2 VGA connector type.

(2008/04/24)

Page 41. Change U_R1~R4 to NC,U_L1,L2 to mount.
Page 43. Add PC187,and Change PC23,PC33 to 680P for EMI request.

(2008/04/25)

Page 16. Update D11 to SL22 for CRT ripple noise.

(2008/04/28)

Add C806~C808,PC188,PC189(0.1uF) for ESD solution.
Page 27. Change CN14 to FOX_1CX42201-SM for ME request.
Page 36. Change CN11 to Gray color,C459,C488 to X5R and R568,R359,R377 to mount for MOR request.

(2008/04/29)

Page 21. Change C717,C723 to X5R.

(2008/04/30)

Page 26. Change C538 to mount for ripple noise.
Page 37. Change R7/F3 to mount,R9/R4 to NC for 3.3V Camera.
Page 50. Change BOSS3,6,7,10 to 1M-1F50M20-5000 and NC BOSS6.

(2008/05/02)

For MOR request,add F5,F6,F7.
Page 6. Add R618~R621 475ohm for CR# issue.
Page 21. Change C721 to 1uF for Intel design change.

(2008/05/06)

Page 16. Change R418,R424 to 30 ohm for Graphic test fail item.
Page 50. Update PAD1,2 size.

(2008/05/07)

Page 36. Change R590 to 22ohm for SD card clock issue.
Page 37. Add resver regulator IC for Camera power.
Page 41. Add C811 for ESD issue.
Page 50. Add resver C812,R623 for EMI issue.
Page 43. Change PQ5 from AO4433 to SI4825DY-T1-E3 for EMI issue.
Page 47. Add PC190 for EMI issue.

(2008/05/08)

Page 6. Add TP153,TP154 for FSB easy measure.

BOM Change

Change CN25 to LN27131-A403-4F.
Change R352,R353,R356,R357 to 68ohm.
Change R601 to mount,F5 to NC.
Change U41,C813~C817,R626,R625,R4 to mount,R7,F3 to NC.

(2008/05/14)

Page 16. Change R418,R424 to 22ohm for CRT issue.
Page 43. Change PL6,PL8 to no mount,Change PL7 to 1000R-100MHZ_0.015R for EMI issue.
Page 47. Change PR115 to no mount.

M790 PVT

(2008/06/03)

Page 25. Add lable1 for BIOS.
Page 39. Change CN8,CN9 to grey color.

(2008/06/11)

Page 23. Delete PJ3 for unnecessary
Page 43. Change PL7 to 1L-FPWC090-7H01 for EMI request.
Page 43. Change PQ1,PQ2 from17-S134240-VT00 to 17-S13424B-DV00 for PUR request.
Page 43. Delete PR20 for unnecessary
Page 44. Delete PJ18,PJ19 for unnecessary
Page 45. Delete PJ12,PJ13,PJ14,PJ20 ,PJ21for unnecessary
Page 46. Delete PJ6,PJ7,PJ8,PJ9 ,PJ10 for unnecessary
Page 47. Delete PJ11,PR97,PR89,PR105,PR108 for unnecessary
Page 48. Delete PR77,PR72,PR65 for unnecessary
Page 49. Delete PR12,PR38,PR46 for unnecessary

(2008/06/16)

Page 32. Change F5 to 1.5A and to mount for MOR request.

(2008/06/23)

Page 41. Change C790~C796,C811 to 220pF for EMI and Hotkey issue.
Page 41. Add Fuse(F8) in power source on power board for short test.
Page 43. Mount PC156,PC157 and Add PC191 for EMI issue.
Page 50. Change BOSS7,10 connect to GND.

(2008/06/24)

Page 40. Change LED1,LED2,LED6 to HT-110UY,LED5 to HT-110UD.R383,R598 to 120ohm for MOR request.
Page 41. Change P_LED1~P_LED3 to HT-150YG.P_R1~P_R3 to 100 ohm for MOR request.

(2008/07/02)

Page 31. Change C184,C192 to 4.7uf 0603 for MIC THD+N issue this change same as M761.
Add ESD solution C810,C812,C818,PC192(0.1uF).

M790 MP

(2008/07/24)

Page 25. Change CN26,U11,C308,R221 to no mount,R233 to mount.
Page 40. Change R385 to 33ohm,R383,R598,R599 to 68ohm for LED bright issue.

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