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**Project Code & Schematics Subject:** M790 Main Board\_6L

<b>PCB P/N:</b>	1P-0086J01-6010 (IRIS)
<b>U/B P/N:</b>	1P-1086J02-6010 (IRIS)
<b>P/B P/N:</b>	1P-1086J03-6010 (IRIS)
<b>R/B P/N:</b>	1P-1086J01-6010 (IRIS)

P. Leader	Check by	Design by
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>Index Page</b>		
Size Custom	Document Number M790-1-01	Rev 1.0
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# M790(Montevina)

TI CHARGER BQ24751 P.63	
INPUTS	OUTPUTS
DC_IN	BT+
	DCBATOUT

SYSTEM DC/DC TPS51125RGER P.64	
INPUTS	OUTPUTS
DCBATOUT	+5VALW
	+5VALW_LDO
	+3VALW
	+ECVCC
	+15V_ALW

SYSTEM DC/DC SC411 P.65	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN
	+1_05VM

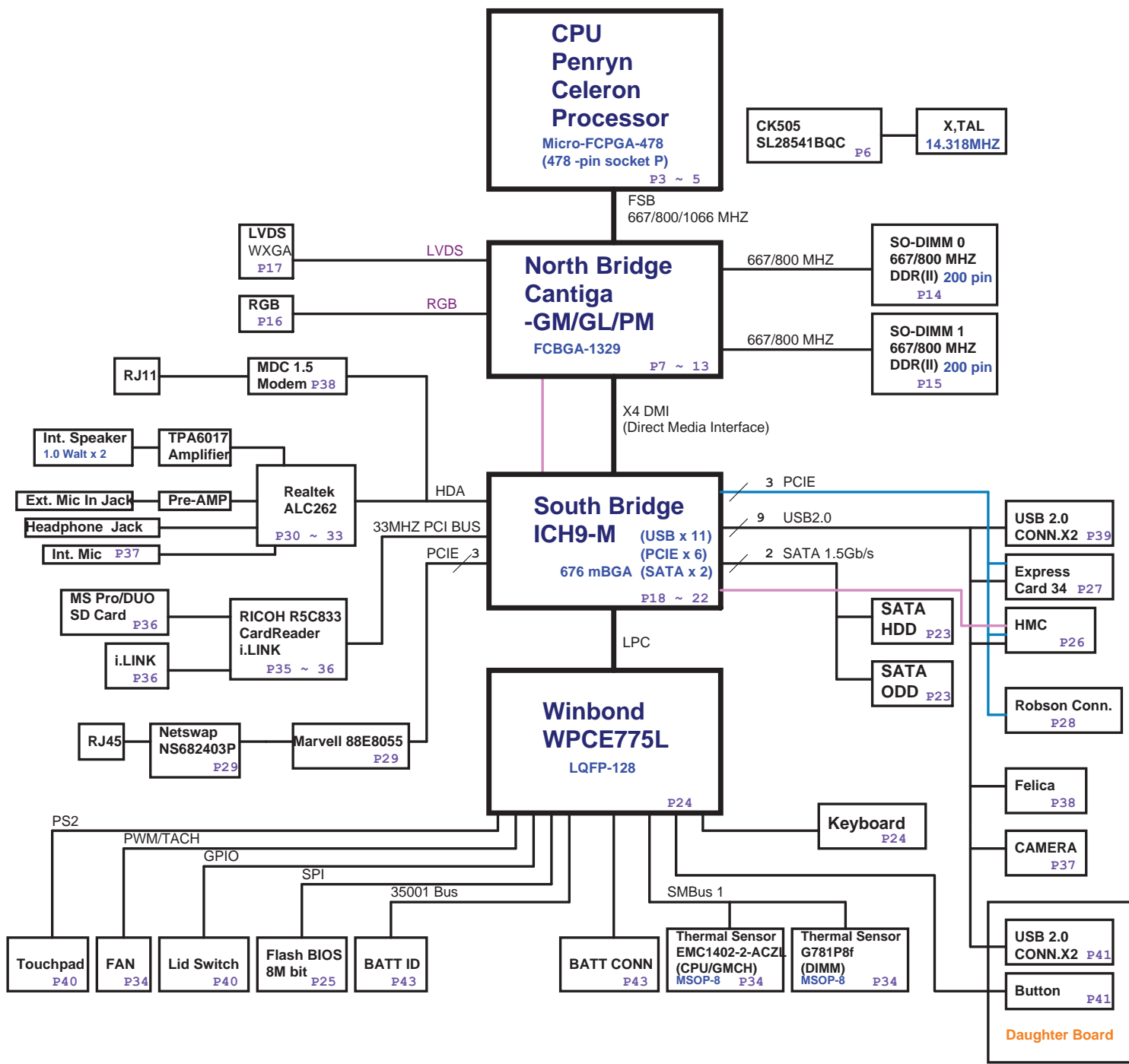
SYSTEM DC/DC TPS51116RGER P.66	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS
	+0_9VSUS

CPU DC/DC ISL6262A P.67	
INPUTS	OUTPUTS
DCBATOUT	VHORE

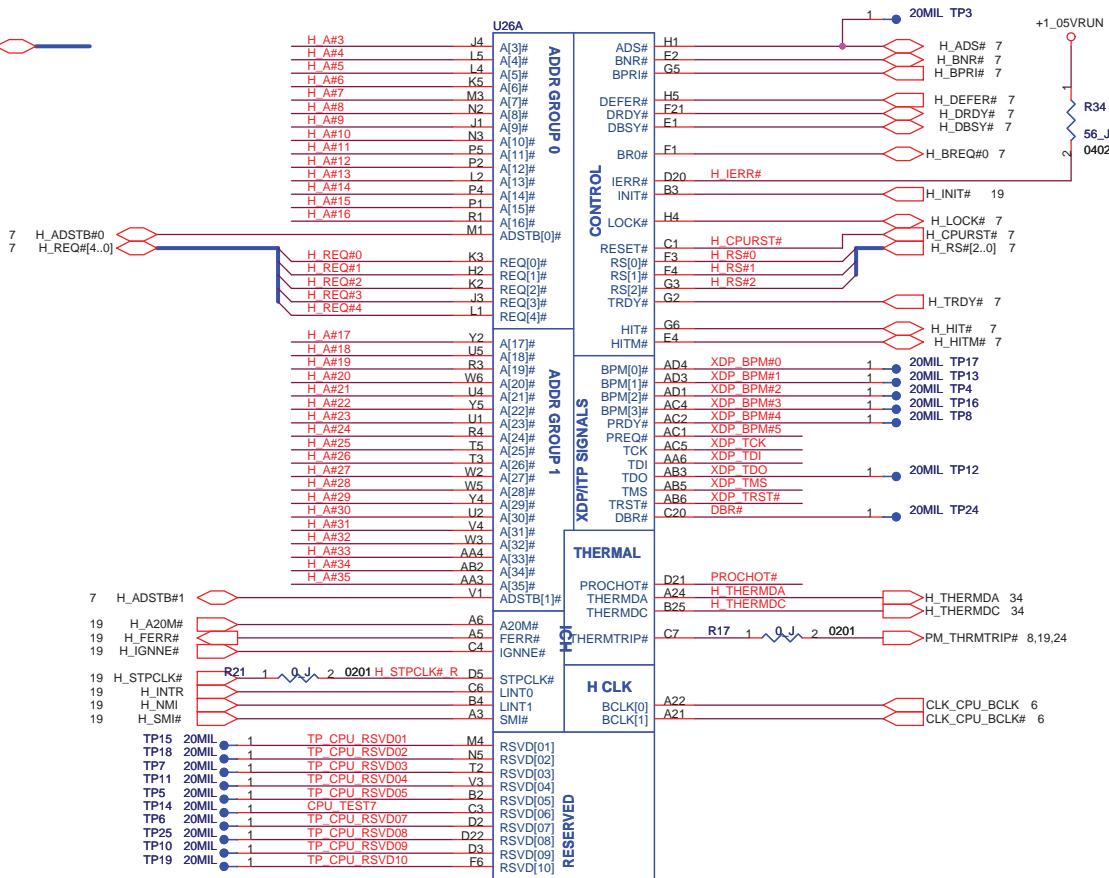
SYSTEM DC/DC APL5912 P.70	
INPUTS	OUTPUTS
+1_5VRUN	PEX_VDD

SYSTEM DC/DC TPS51117 P.70	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

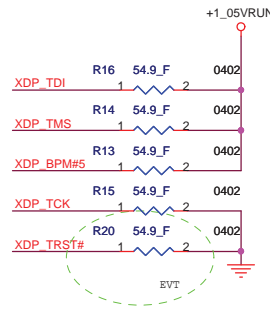
SYSTEM DC/DC MAX8776 P.71	
INPUTS	OUTPUTS
DCBATOUT	+VGFY_CORE



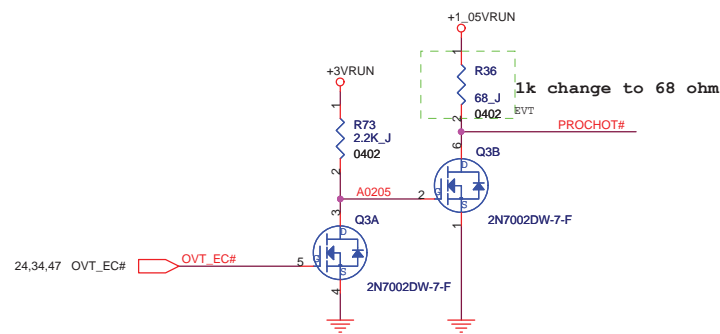
7 H\_AA#[3..35]



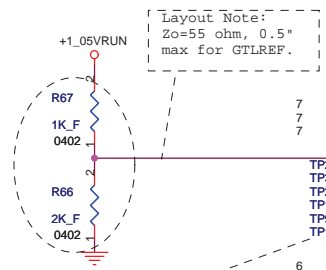
H\_CPURST# 1 20MIL TP2



CPU SOCKET\_478P  
FOX\_PZ4782A-274M-01



Place close to CPU



Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

7 H\_D#[63..0]

7 H\_DSTBN#0  
7 H\_DSTBP#0  
7 H\_DINV#0

7 H\_DSTBN#1  
7 H\_DSTBP#1  
7 H\_DINV#1

6 CPU\_BSEL0  
6 CPU\_BSEL1  
6 CPU\_BSEL2

U26B		
H_D#0	E22	D[0]#
H_D#1	F24	D[1]#
H_D#2	E26	D[2]#
H_D#3	G22	D[3]#
H_D#4	E23	D[4]#
H_D#5	G25	D[5]#
H_D#6	E25	D[6]#
H_D#7	E23	D[7]#
H_D#8	K24	D[8]#
H_D#9	G24	D[9]#
H_D#10	J24	D[10]#
H_D#11	J23	D[11]#
H_D#12	H22	D[12]#
H_D#13	F26	D[13]#
H_D#14	K22	D[14]#
H_D#15	H23	D[15]#
	J26	DSTBN[0]#
	H26	DSTBP[0]#
	H25	DINV[0]#

H_D#16	N22	D[16]#
H_D#17	K25	D[17]#
H_D#18	P28	D[18]#
H_D#19	R23	D[19]#
H_D#20	L23	D[20]#
H_D#21	M24	D[21]#
H_D#22	L22	D[22]#
H_D#23	M23	D[23]#
H_D#24	P25	D[24]#
H_D#25	P23	D[25]#
H_D#26	P22	D[26]#
H_D#27	T24	D[27]#
H_D#28	R24	D[28]#
H_D#29	L25	D[29]#
H_D#30	T25	D[30]#
H_D#31	N25	D[31]#
	L26	DSTBN[1]#
	M26	DSTBP[1]#
	N24	DINV[1]#

MISC		
H_GTLREF	AD26	GTLREF
CPU_TEST1	C23	TEST1
CPU_TEST2	D25	TEST2
CPU_TEST3	C24	TEST3
CPU_TEST4	AF26	TEST4
CPU_TEST5	AF1	TEST5
CPU_TEST6	A26	TEST6
	B22	BSEL[0]
	B23	BSEL[1]
	C21	BSEL[2]

CPU SOCKET\_478P  
FOX\_P24782A-274M-01

DATA GRP 0

DATA GRP 1

DATA GRP 2

DATA GRP 3

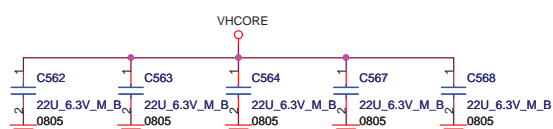
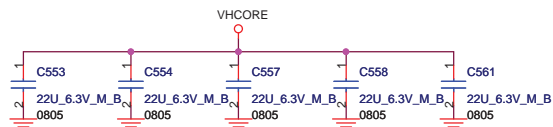
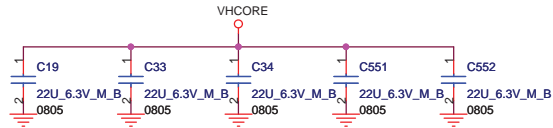
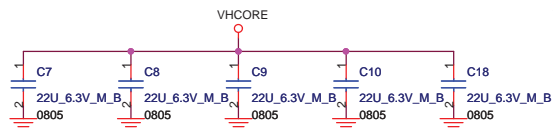
D[32]#	Y22	H_D#32
D[33]#	AB24	H_D#33
D[34]#	V26	H_D#34
D[35]#	V23	H_D#35
D[36]#	T22	H_D#36
D[37]#	U25	H_D#37
D[38]#	U23	H_D#38
D[39]#	Y25	H_D#39
D[40]#	W22	H_D#40
D[41]#	Y23	H_D#41
D[42]#	W24	H_D#42
D[43]#	W25	H_D#43
D[44]#	AA23	H_D#44
D[45]#	AA24	H_D#45
D[46]#	AA24	H_D#46
D[47]#	AB25	H_D#47
Y26	AA26	H_DSTBN#2 7
DSTBN[2]#	U22	H_DSTBP#2 7
DSTBP[2]#		H_DINV#2 7

D[48]#	AE24	H_D#48
D[49]#	AD24	H_D#49
D[50]#	AA21	H_D#50
D[51]#	AB22	H_D#51
D[52]#	AB21	H_D#52
D[53]#	AC26	H_D#53
D[54]#	AD20	H_D#54
D[55]#	AE22	H_D#55
D[56]#	AF23	H_D#56
D[57]#	AC25	H_D#57
D[58]#	AE21	H_D#58
D[59]#	AD21	H_D#59
D[60]#	AC22	H_D#60
D[61]#	AD23	H_D#61
D[62]#	AE22	H_D#62
D[63]#	AC23	H_D#63
D[63]#	AE25	H_DSTBN#3 7
DSTBN[3]#	AE24	H_DSTBP#3 7
DSTBP[3]#	AC20	H_DINV#3 7

COMP[0]	R26	COMP0	R68	2	27.4 F	1	0402
COMP[1]	U26	COMP1	R69	2	54.9 F	1	0402
COMP[2]	AA1	COMP2	R12	2	27.4 F	1	0402
COMP[3]	Y1	COMP3	R11	2	54.9 F	1	0402
DPRSTP#	E5						H DPRSTP# 8.19,47
DPWLR#	B5						H DPWLR# 19
DPWLR#	D24						H DPWLR# 7
PWRGOOD	D5						H PWRGD 19
SLP#	D7						H CPUSLP# 7
PSI#	AE6						PSI# 47

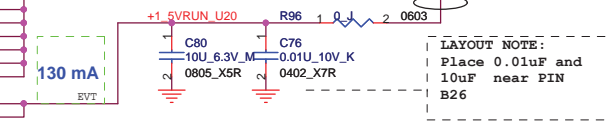
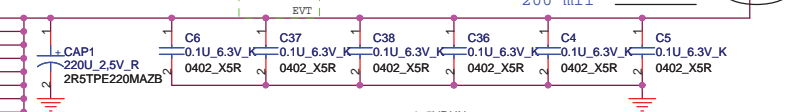
H\_PWRGD 1 20MIL TP135  
H\_CPUSLP# 1 20MIL TP20

Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)  
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)

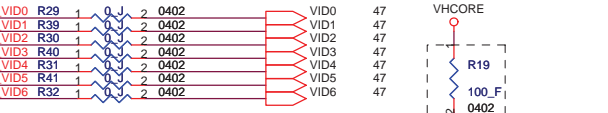


U26C		
A7	VCC[001]	VCC[068]
A9	VCC[002]	VCC[069]
A10	VCC[003]	VCC[070]
A12	VCC[004]	VCC[071]
A13	VCC[005]	VCC[072]
A15	VCC[006]	VCC[073]
A17	VCC[007]	VCC[074]
A18	VCC[008]	VCC[075]
A20	VCC[009]	VCC[076]
B7	VCC[010]	VCC[077]
B9	VCC[011]	VCC[078]
B10	VCC[012]	VCC[079]
B12	VCC[013]	VCC[080]
B14	VCC[014]	VCC[081]
B15	VCC[015]	VCC[082]
B17	VCC[016]	VCC[083]
B18	VCC[017]	VCC[084]
B20	VCC[018]	VCC[085]
C9	VCC[019]	VCC[086]
C10	VCC[020]	VCC[087]
C12	VCC[021]	VCC[088]
C13	VCC[022]	VCC[089]
C15	VCC[023]	VCC[090]
C17	VCC[024]	VCC[091]
C18	VCC[025]	VCC[092]
D9	VCC[026]	VCC[093]
D10	VCC[027]	VCC[094]
D12	VCC[028]	VCC[095]
D14	VCC[029]	VCC[096]
D15	VCC[030]	VCC[097]
D17	VCC[031]	VCC[098]
D18	VCC[032]	VCC[099]
E7	VCC[033]	VCC[100]
E9	VCC[034]	
E10	VCCP[01]	
E12	VCCP[02]	
E13	VCCP[03]	
E15	VCCP[04]	
E17	VCCP[05]	
E18	VCCP[06]	
E20	VCCP[07]	
F7	VCCP[08]	
F9	VCCP[09]	
F10	VCCP[10]	
F12	VCCP[11]	
F14	VCCP[12]	
F15	VCCP[13]	
F17	VCCP[14]	
F18	VCCP[15]	
F20	VCCP[16]	
AA7	VCC[051]	
AA9	VCC[052]	
AA10	VCC[053]	
AA12	VCC[054]	
AA13	VCC[055]	
AA15	VCC[056]	
AA17	VCC[057]	
AA18	VCC[058]	
AA20	VCC[059]	
AB9	VCC[060]	
AC10	VCC[061]	
AB10	VCC[062]	
AB12	VCC[063]	
AB15	VCC[064]	
AB16	VCC[065]	
AB17	VCC[066]	
AB18	VCC[067]	

CPU\_VCCA---->0.13A  
 CPU\_VCCP---->4.5A  
 CPU\_VCC---->47A



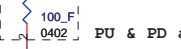
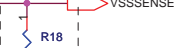
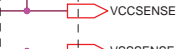
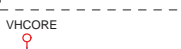
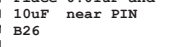
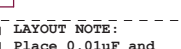
LAYOUT NOTE:  
 Place 0.01uF and 10uF near PIN B26

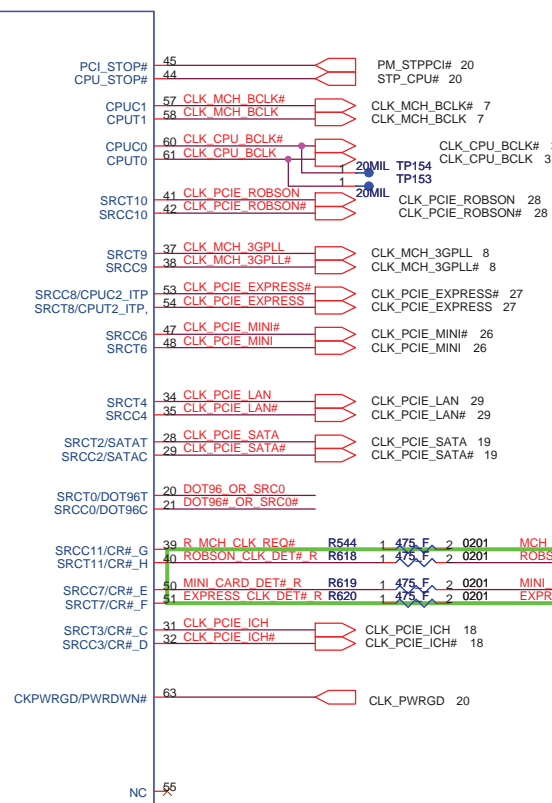
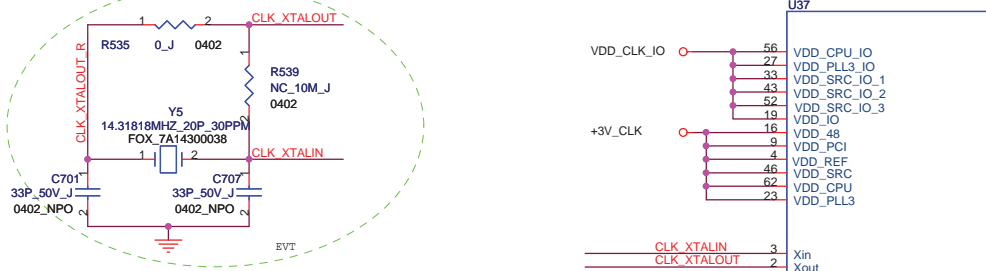
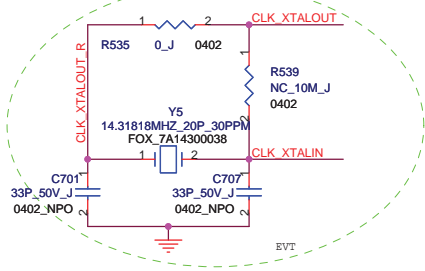
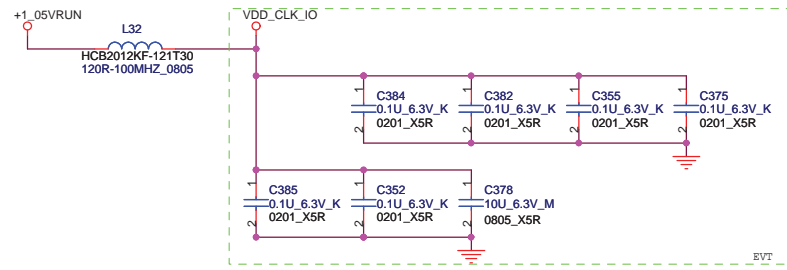
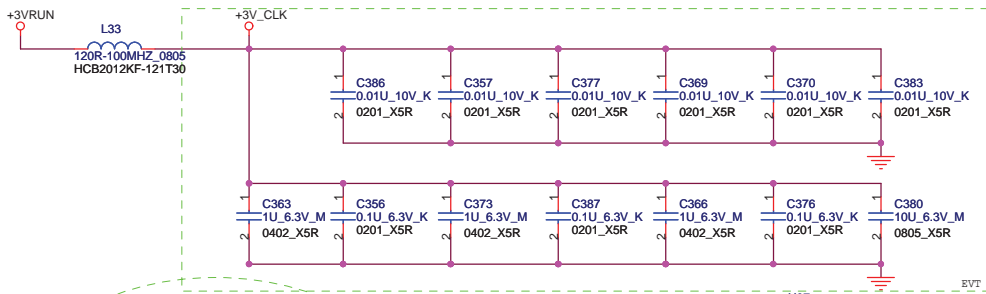


Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.

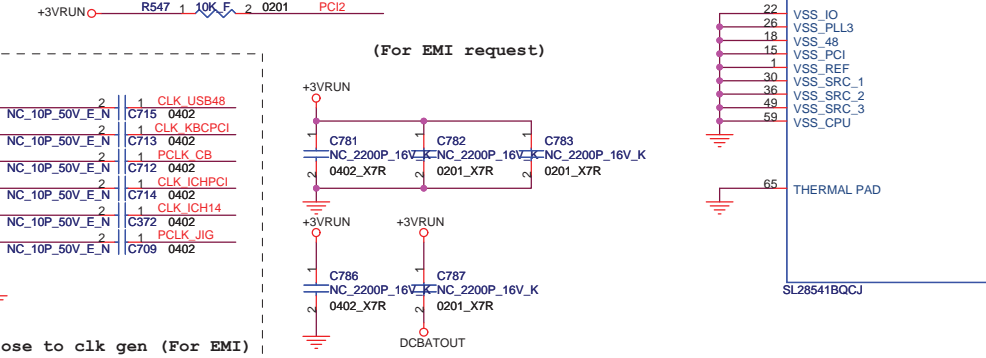
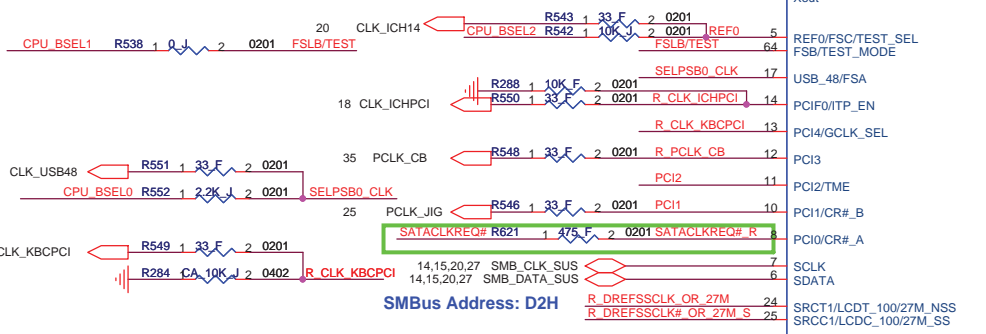
Outer width=18 mil spacing=7 mil  
 Inner width=14 mil spacing=7 mil  
 Length match < 25 mil

U26D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C9	VSS[018]	VSS[099]
C14	VSS[019]	VSS[100]
C16	VSS[020]	VSS[101]
VSS[021]	VSS[102]	
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
	VSS[163]	



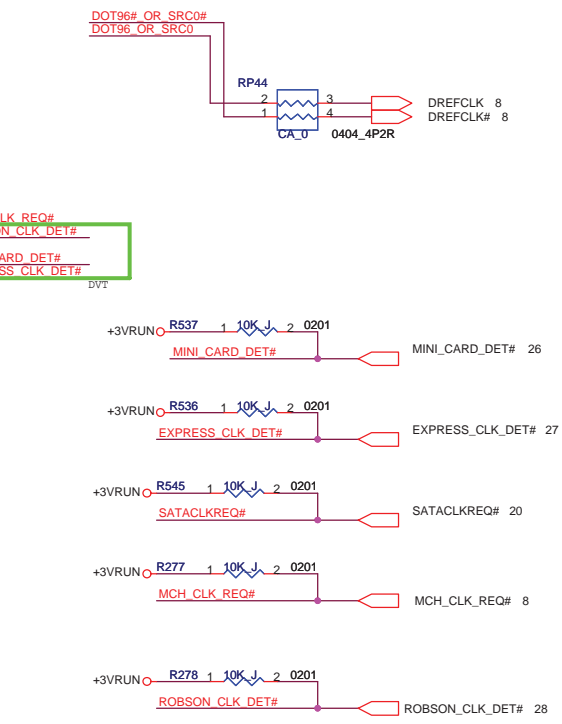


Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	NC
CR#C	NC
CR#D	NC
CR#E	MINI_CARD_DET#
CR#F	EXPRESS_CLK_DET#
CR#G	MCH_CLK_REQ#
CR#H	ROBSON_CLK_DET#



**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

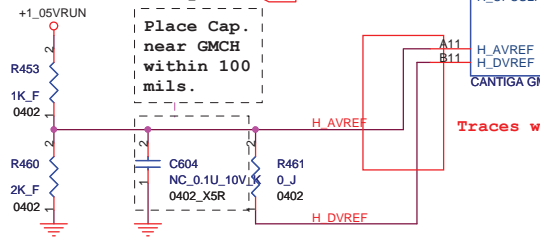
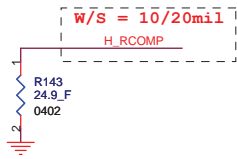
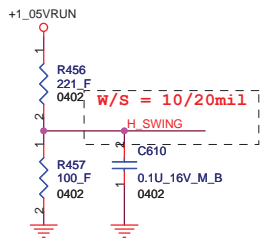
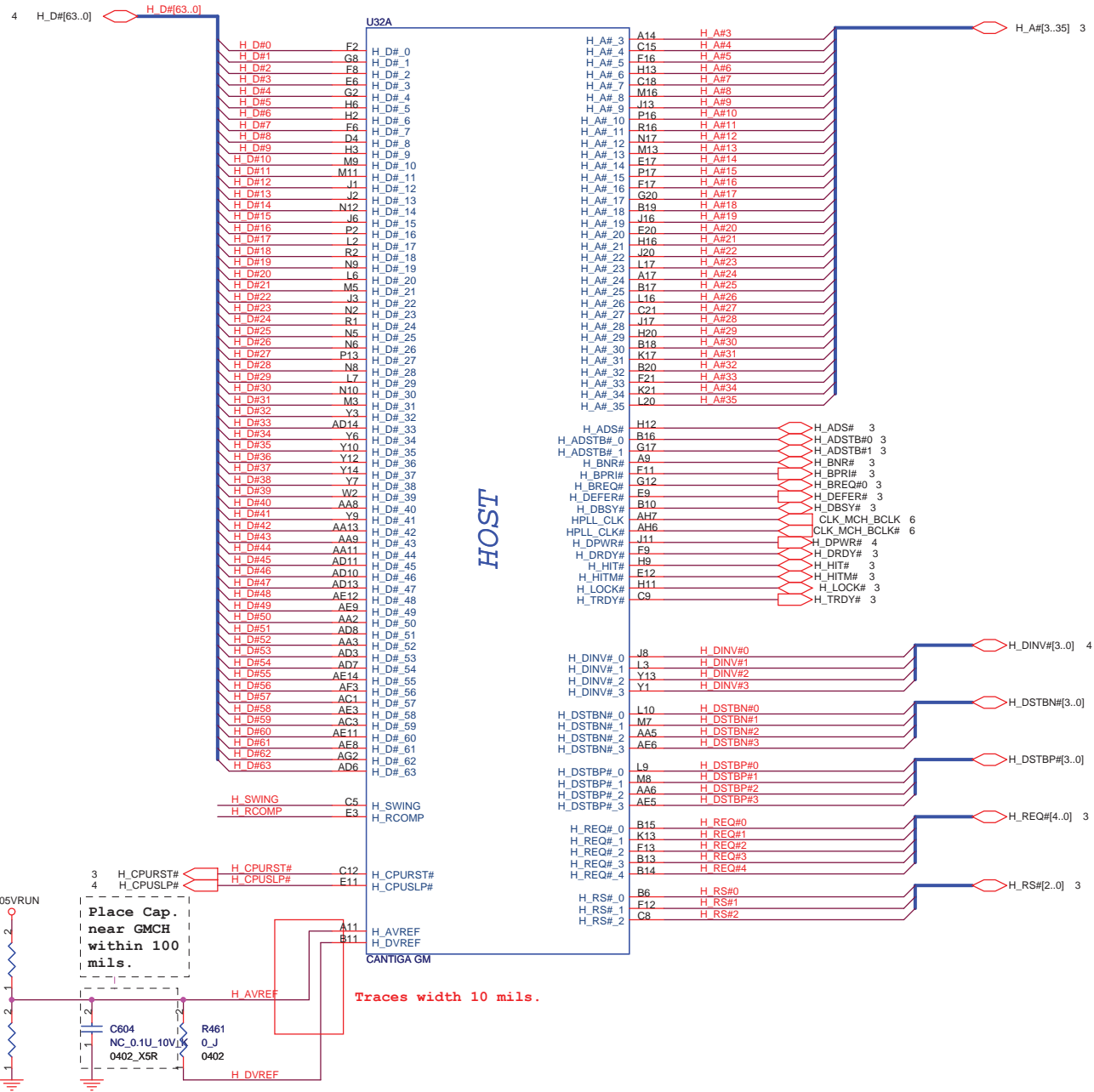


**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **CLOCK GEN**

Size: A3 | Document Number: M790-1-01 | Rev: 1.0

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HOST



MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800 ; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

M36	M36	RESERVED_7
N36	N36	RESERVED_10
R33	R33	RESERVED_12
T33	T33	RESERVED_17
AH9	AH9	RESERVED_17
AH10	AH10	RESERVED_11
AH12	AH12	RESERVED_9
AH13	AH13	RESERVED_8
K12	K12	RESERVED_2
AL34	AL34	RESERVED_18
AK34	AK34	RESERVED_14
AN35	AN35	RESERVED_19
AM35	AM35	RESERVED_21
T24	T24	RESERVED_13
B31	B31	RESERVED_4
B2	B2	RESERVED_3
M1	M1	RESERVED_6
AY21	AY21	RESERVED_1
BG23	BG23	RESERVED_20
BF23	BF23	RESERVED_15
BH18	BH18	RESERVED_22
BF18	BF18	RESERVED_15

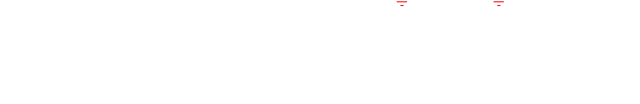
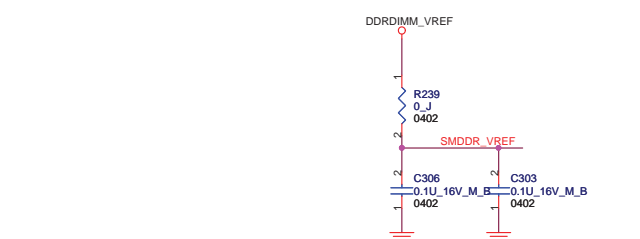
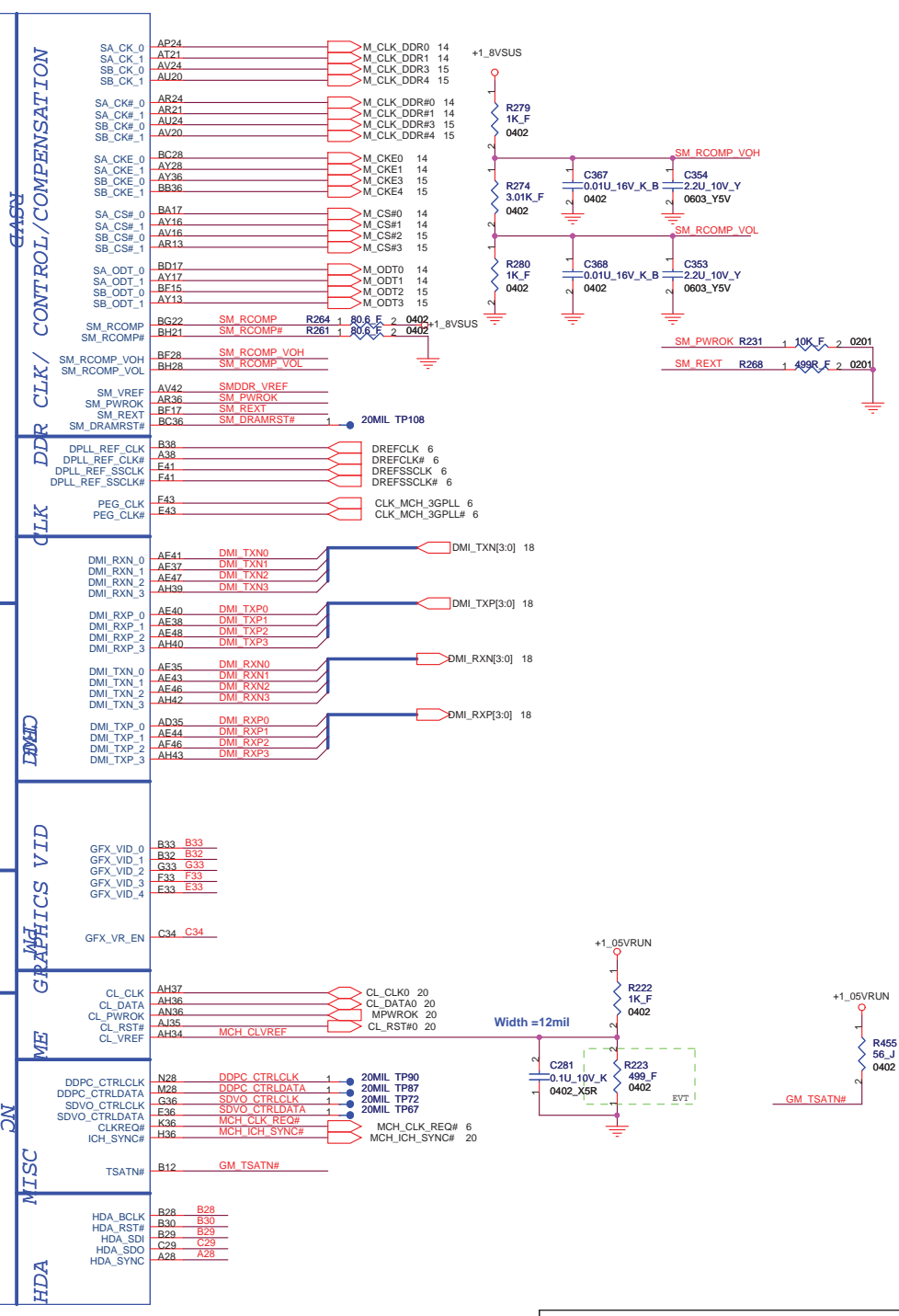
BG22	BG22	RESERVED_20
BF21	BF21	RESERVED_16
BF18	BF18	RESERVED_22
BF18	BF18	RESERVED_15

T25	CFG_0
R25	CFG_1
P25	CFG_2
P20	CFG_3
P24	CFG_4
C25	CFG_5
N24	CFG_6
M24	CFG_7
E21	CFG_8
C23	CFG_9
C24	CFG_10
N21	CFG_11
P21	CFG_12
T21	CFG_13
R20	CFG_14
M20	CFG_15
L21	CFG_16
H21	CFG_17
P21	CFG_18
R28	CFG_19
T28	CFG_20

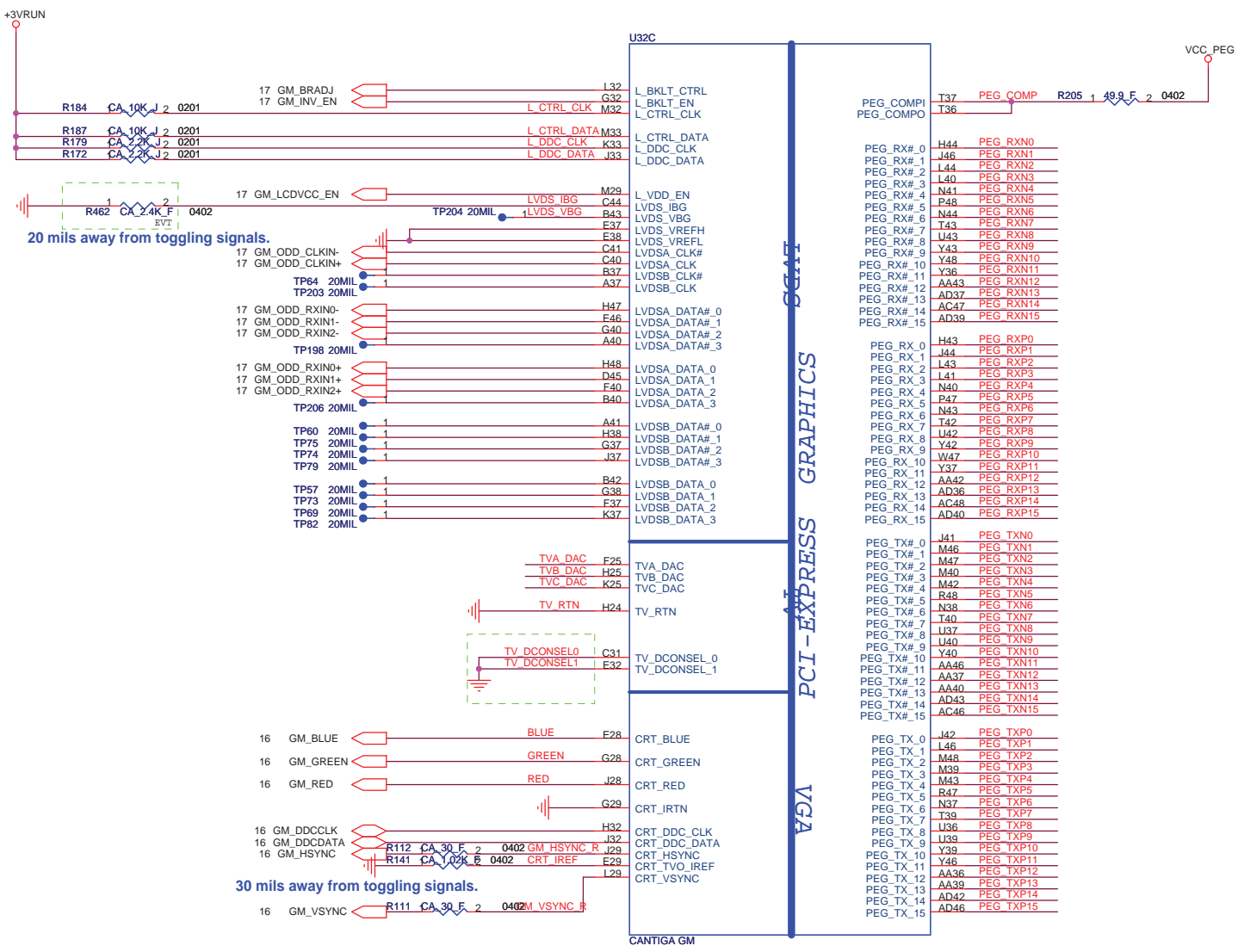
R29	PM_SYNC#
N33	PM_DPRSTP#
P32	PM_EXT_TSH#_0
AT40	PM_EXT_TSH#_1
T20	PWROK
T20	RSTIN#
R32	THERMTRIP#
R32	DPRSLPVR

BG48	NC_33
BF48	NC_27
BD48	NC_21
BC48	NC_19
BH47	NC_39
BG47	NC_32
BE47	NC_32
BH46	NC_38
BF46	NC_28
BG45	NC_36
BH44	NC_37
BF43	NC_31
BH6	NC_36
BH5	NC_41
BG4	NC_40
BH3	NC_30
BF3	NC_35
BH2	NC_25
BG2	NC_29
BE2	NC_22
BC1	NC_28
BF1	NC_20
BD1	NC_20
BC1	NC_18
F1	NC_12
A47	NC_4

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PEG_COMP1	T37	PEG_COMP	R205	49.9	F	2	0402
PEG_COMP0	T36						
PEG_RX#_0	H44	PEG_RXN0					
PEG_RX#_1	J46	PEG_RXN1					
PEG_RX#_2	L44	PEG_RXN2					
PEG_RX#_3	L40	PEG_RXN3					
PEG_RX#_4	N41	PEG_RXN4					
PEG_RX#_5	P48	PEG_RXN5					
PEG_RX#_6	N44	PEG_RXN6					
PEG_RX#_7	T43	PEG_RXN7					
PEG_RX#_8	U43	PEG_RXN8					
PEG_RX#_9	Y43	PEG_RXN9					
PEG_RX#_10	Y48	PEG_RXN10					
PEG_RX#_11	Y36	PEG_RXN11					
PEG_RX#_12	AA43	PEG_RXN12					
PEG_RX#_13	AD37	PEG_RXN13					
PEG_RX#_14	AC47	PEG_RXN14					
PEG_RX#_15	AD39	PEG_RXN15					
PEG_RX_0	H43	PEG_RXP0					
PEG_RX_1	J44	PEG_RXP1					
PEG_RX_2	L43	PEG_RXP2					
PEG_RX_3	L41	PEG_RXP3					
PEG_RX_4	N40	PEG_RXP4					
PEG_RX_5	P47	PEG_RXP5					
PEG_RX_6	N43	PEG_RXP6					
PEG_RX_7	T42	PEG_RXP7					
PEG_RX_8	U42	PEG_RXP8					
PEG_RX_9	Y42	PEG_RXP9					
PEG_RX_10	W47	PEG_RXP10					
PEG_RX_11	Y37	PEG_RXP11					
PEG_RX_12	AA42	PEG_RXP12					
PEG_RX_13	AD36	PEG_RXP13					
PEG_RX_14	AC48	PEG_RXP14					
PEG_RX_15	AD40	PEG_RXP15					
PEG_TX#_0	J41	PEG_TXN0					
PEG_TX#_1	M46	PEG_TXN1					
PEG_TX#_2	M47	PEG_TXN2					
PEG_TX#_3	M40	PEG_TXN3					
PEG_TX#_4	M42	PEG_TXN4					
PEG_TX#_5	R48	PEG_TXN5					
PEG_TX#_6	N38	PEG_TXN6					
PEG_TX#_7	T40	PEG_TXN7					
PEG_TX#_8	U37	PEG_TXN8					
PEG_TX#_9	U40	PEG_TXN9					
PEG_TX#_10	Y40	PEG_TXN10					
PEG_TX#_11	AA46	PEG_TXN11					
PEG_TX#_12	AA37	PEG_TXN12					
PEG_TX#_13	AA40	PEG_TXN13					
PEG_TX#_14	AD43	PEG_TXN14					
PEG_TX#_15	AC46	PEG_TXN15					
PEG_TX_0	J42	PEG_TXP0					
PEG_TX_1	L46	PEG_TXP1					
PEG_TX_2	M48	PEG_TXP2					
PEG_TX_3	M39	PEG_TXP3					
PEG_TX_4	M43	PEG_TXP4					
PEG_TX_5	R47	PEG_TXP5					
PEG_TX_6	N37	PEG_TXP6					
PEG_TX_7	T39	PEG_TXP7					
PEG_TX_8	U36	PEG_TXP8					
PEG_TX_9	U39	PEG_TXP9					
PEG_TX_10	Y39	PEG_TXP10					
PEG_TX_11	Y46	PEG_TXP11					
PEG_TX_12	AA36	PEG_TXP12					
PEG_TX_13	AA39	PEG_TXP13					
PEG_TX_14	AD42	PEG_TXP14					
PEG_TX_15	AD46	PEG_TXP15					

14 M\_A\_DQ[63.0]

M_A DQ0	AJ38	SA DO_0
M_A DQ1	AJ41	SA DO_1
M_A DQ2	AN38	SA DO_2
M_A DQ3	AM38	SA DO_3
M_A DQ4	AJ36	SA DO_4
M_A DQ5	AJ40	SA DO_5
M_A DQ6	AM44	SA DO_6
M_A DQ7	AM42	SA DO_7
M_A DQ8	AN43	SA DO_8
M_A DQ9	AN44	SA DO_9
M_A DQ10	AJ40	SA DO_10
M_A DQ11	AT38	SA DO_11
M_A DQ12	AN41	SA DO_12
M_A DQ13	AN39	SA DO_13
M_A DQ14	AJ44	SA DO_14
M_A DQ15	AJ42	SA DO_15
M_A DQ16	AV39	SA DO_16
M_A DQ17	AY44	SA DO_17
M_A DQ18	BA40	SA DO_18
M_A DQ19	BD43	SA DO_19
M_A DQ20	AV41	SA DO_20
M_A DQ21	AY43	SA DO_21
M_A DQ22	BB41	SA DO_22
M_A DQ23	BC40	SA DO_23
M_A DQ24	AY37	SA DO_24
M_A DQ25	BD38	SA DO_25
M_A DQ26	AV37	SA DO_26
M_A DQ27	AT36	SA DO_27
M_A DQ28	AY38	SA DO_28
M_A DQ29	BB38	SA DO_29
M_A DQ30	AV36	SA DO_30
M_A DQ31	AW36	SA DO_31
M_A DQ32	BD13	SA DO_32
M_A DQ33	AJ11	SA DO_33
M_A DQ34	BC11	SA DO_34
M_A DQ35	BA12	SA DO_35
M_A DQ36	AJ13	SA DO_36
M_A DQ37	AV13	SA DO_37
M_A DQ38	BD12	SA DO_38
M_A DQ39	BC12	SA DO_39
M_A DQ40	BB9	SA DO_40
M_A DQ41	BA9	SA DO_41
M_A DQ42	AJ10	SA DO_42
M_A DQ43	AV9	SA DO_43
M_A DQ44	BA11	SA DO_44
M_A DQ45	BD9	SA DO_45
M_A DQ46	AY8	SA DO_46
M_A DQ47	BA6	SA DO_47
M_A DQ48	AV7	SA DO_48
M_A DQ49	AT9	SA DO_49
M_A DQ50	AT9	SA DO_50
M_A DQ51	AN8	SA DO_51
M_A DQ52	AU5	SA DO_52
M_A DQ53	AU6	SA DO_53
M_A DQ54	AT5	SA DO_54
M_A DQ55	AN10	SA DO_55
M_A DQ56	AM11	SA DO_56
M_A DQ57	AM5	SA DO_57
M_A DQ58	AJ9	SA DO_58
M_A DQ59	AJ8	SA DO_59
M_A DQ60	AN12	SA DO_60
M_A DQ61	AM13	SA DO_61
M_A DQ62	AJ11	SA DO_62
M_A DQ63	AJ12	SA DO_63

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DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	14
SA_BS_1	BG18	M_A_BS1	14
SA_BS_2	AT25	M_A_BS2	14
SA_RAS#	BB20	M_A_RAS#	14
SA_CAS#	BD20	M_A_CAS#	14
SA_WE#	AY20	M_A_WE#	14
SA_DM_0	AM37	M_A_DM0	14
SA_DM_1	AT41	M_A_DM1	14
SA_DM_2	AY41	M_A_DM2	14
SA_DM_3	AJ39	M_A_DM3	14
SA_DM_4	BB12	M_A_DM4	14
SA_DM_5	AY6	M_A_DM5	14
SA_DM_6	AT7	M_A_DM6	14
SA_DM_7	AJ5	M_A_DM7	14
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	AT44	M_A_DQS1	14
SA_DQS_2	BA43	M_A_DQS2	14
SA_DQS_3	BC37	M_A_DQS3	14
SA_DQS_4	AW12	M_A_DQS4	14
SA_DQS_5	BC8	M_A_DQS5	14
SA_DQS_6	AJ8	M_A_DQS6	14
SA_DQS_7	AM7	M_A_DQS7	14
SA_DQS#_0	AJ43	M_A_DQS#0	14
SA_DQS#_1	AT43	M_A_DQS#1	14
SA_DQS#_2	BA44	M_A_DQS#2	14
SA_DQS#_3	BD37	M_A_DQS#3	14
SA_DQS#_4	AY12	M_A_DQS#4	14
SA_DQS#_5	BD8	M_A_DQS#5	14
SA_DQS#_6	AJ9	M_A_DQS#6	14
SA_DQS#_7	AM8	M_A_DQS#7	14
SA_MA_0	BA21	M_A_A0	14
SA_MA_1	BC24	M_A_A1	14
SA_MA_2	BG24	M_A_A2	14
SA_MA_3	BH24	M_A_A3	14
SA_MA_4	BG25	M_A_A4	14
SA_MA_5	BA24	M_A_A5	14
SA_MA_6	BD24	M_A_A6	14
SA_MA_7	BG27	M_A_A7	14
SA_MA_8	BF25	M_A_A8	14
SA_MA_9	AW24	M_A_A9	14
SA_MA_10	BC21	M_A_A10	14
SA_MA_11	BG26	M_A_A11	14
SA_MA_12	BH26	M_A_A12	14
SA_MA_13	BH17	M_A_A13	14
SA_MA_14	AY25	M_A_A14	14

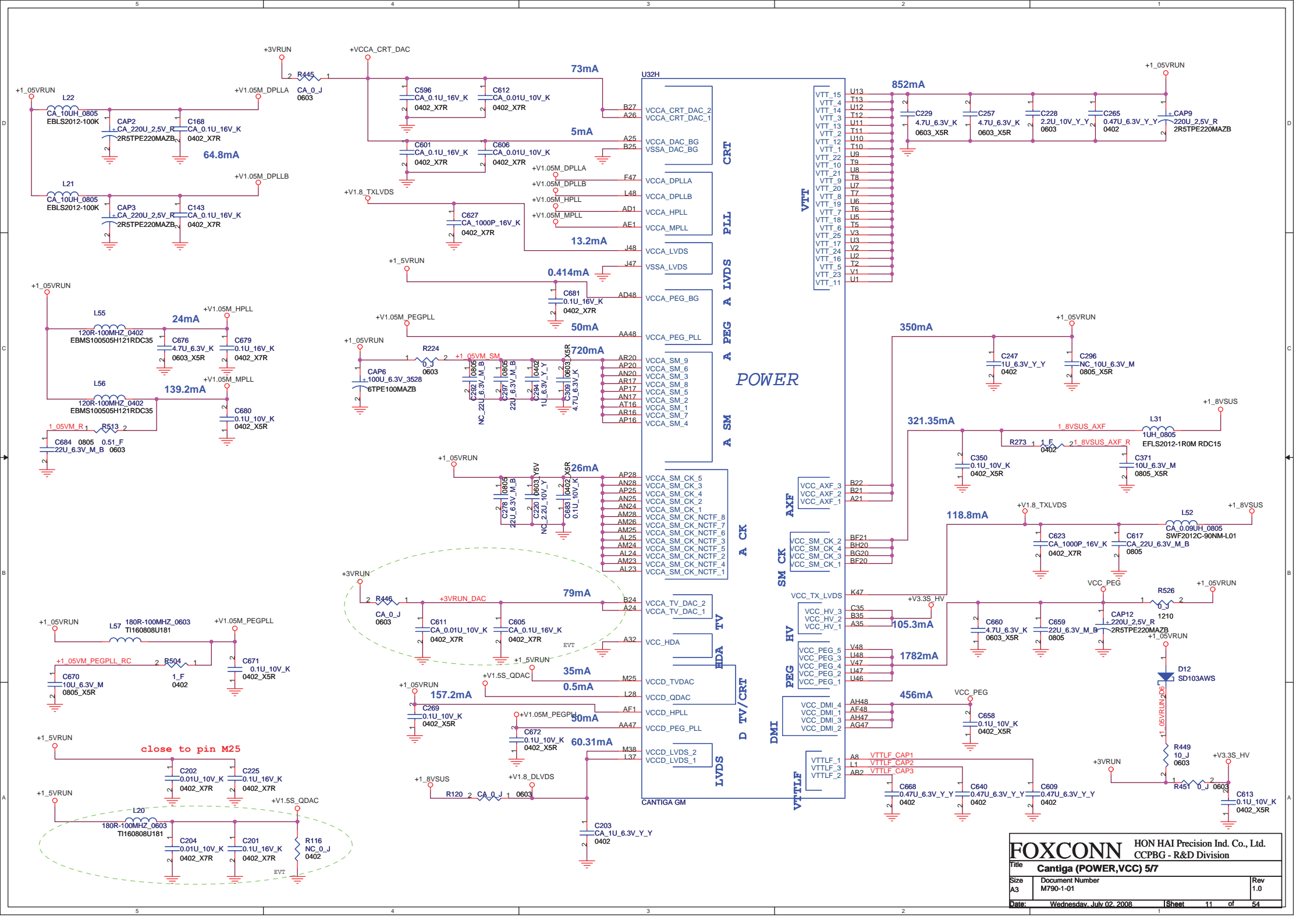
15 M\_B\_DQ[63.0]

M_B DQ0	AK47	SB DO_0
M_B DQ1	AH46	SB DO_1
M_B DQ2	AP47	SB DO_2
M_B DQ3	AP46	SB DO_3
M_B DQ4	AJ46	SB DO_4
M_B DQ5	AJ48	SB DO_5
M_B DQ6	AM48	SB DO_6
M_B DQ7	AP48	SB DO_7
M_B DQ8	AJ47	SB DO_8
M_B DQ9	AJ46	SB DO_9
M_B DQ10	BA48	SB DO_10
M_B DQ11	AY48	SB DO_11
M_B DQ12	AT47	SB DO_12
M_B DQ13	AR47	SB DO_13
M_B DQ14	BA47	SB DO_14
M_B DQ15	BQ47	SB DO_15
M_B DQ16	BC46	SB DO_16
M_B DQ17	BC44	SB DO_17
M_B DQ18	BG43	SB DO_18
M_B DQ19	BF43	SB DO_19
M_B DQ20	BC41	SB DO_20
M_B DQ21	BE40	SB DO_21
M_B DQ22	BF41	SB DO_22
M_B DQ23	BG38	SB DO_23
M_B DQ24	BF38	SB DO_24
M_B DQ25	BH35	SB DO_25
M_B DQ26	BQ35	SB DO_26
M_B DQ27	BH40	SB DO_27
M_B DQ28	BG39	SB DO_28
M_B DQ29	BG34	SB DO_29
M_B DQ30	BH34	SB DO_30
M_B DQ31	BH14	SB DO_31
M_B DQ32	BG12	SB DO_32
M_B DQ33	BH11	SB DO_33
M_B DQ34	BG8	SB DO_34
M_B DQ35	BH12	SB DO_35
M_B DQ36	BF11	SB DO_36
M_B DQ37	BF8	SB DO_37
M_B DQ38	BG7	SB DO_38
M_B DQ39	BC8	SB DO_39
M_B DQ40	BC6	SB DO_40
M_B DQ41	AY3	SB DO_41
M_B DQ42	AY1	SB DO_42
M_B DQ43	BF6	SB DO_43
M_B DQ44	BA1	SB DO_44
M_B DQ45	BA1	SB DO_45
M_B DQ46	AV2	SB DO_46
M_B DQ47	AU3	SB DO_47
M_B DQ48	AR3	SB DO_48
M_B DQ49	AN2	SB DO_49
M_B DQ50	AY2	SB DO_50
M_B DQ51	AV1	SB DO_51
M_B DQ52	AP3	SB DO_52
M_B DQ53	AR1	SB DO_53
M_B DQ54	AL1	SB DO_54
M_B DQ55	AL2	SB DO_55
M_B DQ56	AJ1	SB DO_56
M_B DQ57	AH1	SB DO_57
M_B DQ58	AM2	SB DO_58
M_B DQ59	AM3	SB DO_59
M_B DQ60	AH3	SB DO_60
M_B DQ61	AH3	SB DO_61
M_B DQ62	AJ3	SB DO_62
M_B DQ63	AJ3	SB DO_63

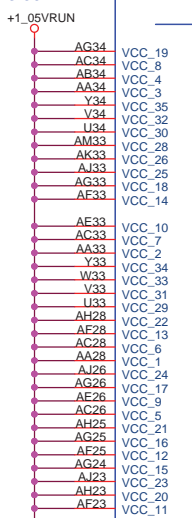
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DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0	15
SB_BS_1	BB17	M_B_BS1	15
SB_BS_2	BB33	M_B_BS2	15
SB_RAS#	AU17	M_B_RAS#	15
SB_CAS#	RG16	M_B_CAS#	15
SB_WE#	BF14	M_B_WE#	15
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	15
SB_DM_2	BD40	M_B_DM2	15
SB_DM_3	BF35	M_B_DM3	15
SB_DM_4	RG11	M_B_DM4	15
SB_DM_5	BA3	M_B_DM5	15
SB_DM_6	AP1	M_B_DM6	15
SB_DM_7	AK2	M_B_DM7	15
SB_DQS_0	AL47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	15
SB_DQS_2	BG41	M_B_DQS2	15
SB_DQS_3	BG37	M_B_DQS3	15
SB_DQS_4	BH9	M_B_DQS4	15
SB_DQS_5	BB2	M_B_DQS5	15
SB_DQS_6	AU1	M_B_DQS6	15
SB_DQS_7	AN6	M_B_DQS7	15
SB_DQS#_0	AL46	M_B_DQS#0	15
SB_DQS#_1	AV47	M_B_DQS#1	15
SB_DQS#_2	BH41	M_B_DQS#2	15
SB_DQS#_3	BH37	M_B_DQS#3	15
SB_DQS#_4	BG9	M_B_DQS#4	15
SB_DQS#_5	PC2	M_B_DQS#5	15
SB_DQS#_6	AT2	M_B_DQS#6	15
SB_DQS#_7	AN5	M_B_DQS#7	15
SB_MA_0	AV17	M_B_A0	15
SB_MA_1	BA25	M_B_A1	15
SB_MA_2	RC25	M_B_A2	15
SB_MA_3	AU25	M_B_A3	15
SB_MA_4	AW25	M_B_A4	15
SB_MA_5	BB28	M_B_A5	15
SB_MA_6	AU28	M_B_A6	15
SB_MA_7	AW28	M_B_A7	15
SB_MA_8	AT33	M_B_A8	15
SB_MA_9	BD33	M_B_A9	15
SB_MA_10	BB16	M_B_A10	15
SB_MA_11	AW33	M_B_A11	15
SB_MA_12	AY33	M_B_A12	15
SB_MA_13	BH15	M_B_A13	15
SB_MA_14	AU33	M_B_A14	15



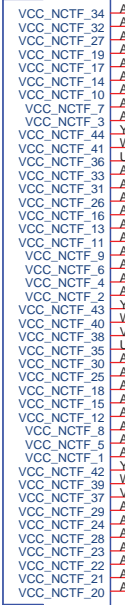
3.06A



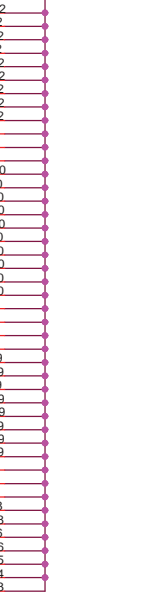
VCC CORE

POWER

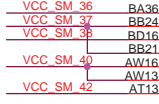
VCC NCTF



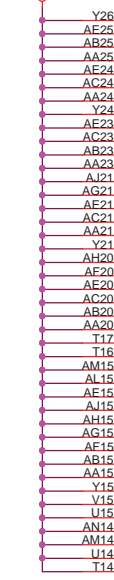
+1\_05VRUN



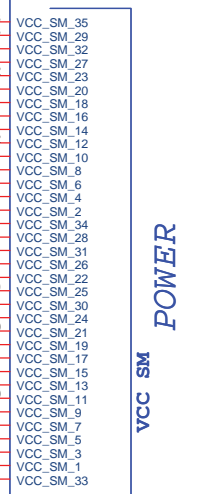
3A +1.8VSUS



+1\_05VRUN

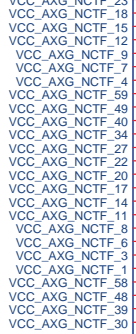


U32G

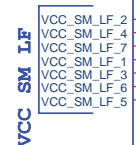


VCC SM POWER

VCC GFX NCTF



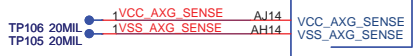
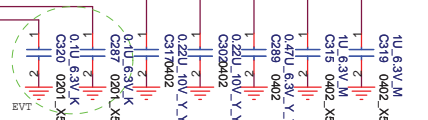
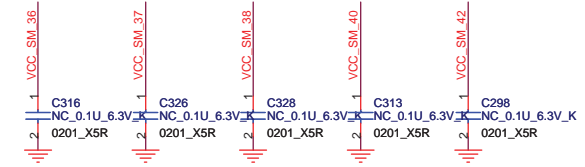
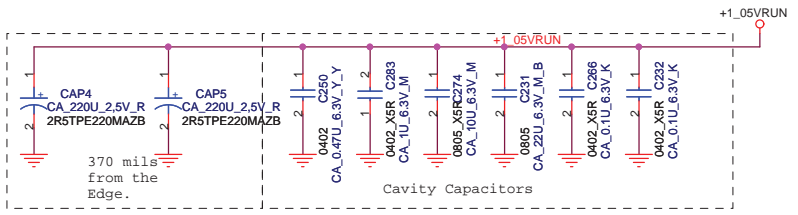
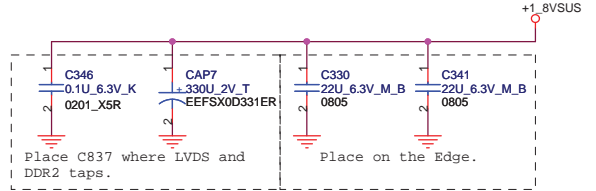
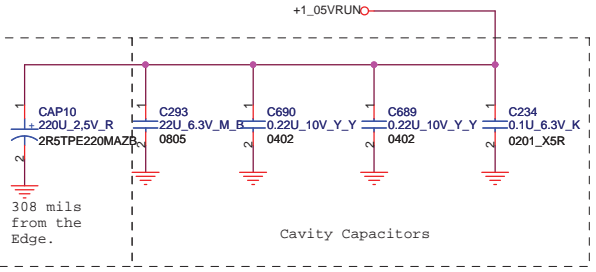
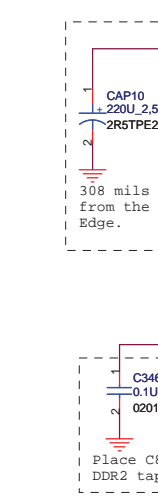
VCC GFX



+1\_05VRUN



8.7A



CANTIGA GM

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Title: **Cantiga (VCC CORE) 6/7**

Size A3	Document Number M790-1-01	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 12	of 54

U32I		VSS		U32J	
ALJ48	VSS_49	VSS_282	AM36	BG21	VSS_200
AR48	VSS_15	VSS_133	AE36	L12	VSS_150
AL48	VSS_278	VSS_248	P36	AW21	VSS_182
BB47	VSS_204	VSS_155	L36	AU21	VSS_44
AW47	VSS_114	VSS_124	J36	AP21	VSS_328
AN47	VSS_313	VSS_57	F36	AN21	VSS_308
AU47	VSS_234	VSS_141	B36	AJ21	VSS_191
AF47	VSS_234	VSS_198	AH35	AB21	VSS_160
AD47	VSS_164	VSS_35	AA35	R21	VSS_66
VSS_106		VSS_343	Y35	M21	VSS_186
AB47	VSS_71	VSS_297	U35	J21	VSS_121
Y47	VSS_347	VSS_269	T35	G21	VSS_121
T47	VSS_273	VSS_263	BF34	BC20	VSS_65
N47	VSS_220	VSS_281	AM34	BA20	VSS_208
L47	VSS_158	VSS_230	AJ34	AW20	VSS_174
G47	VSS_91	VSS_163	AF34	AT20	VSS_111
BD46	VSS_243	VSS_132	AE34	AJ20	VSS_19
BA46	VSS_178	VSS_321	W34	AG20	VSS_226
AY46	VSS_118	VSS_140	A34	Y20	VSS_165
AV46	VSS_83	VSS_8	BG33	N20	VSS_324
AR46	VSS_14	VSS_292	BC33	K20	VSS_214
AM46	VSS_302	VSS_176	BA33	F20	VSS_145
V46	VSS_319	VSS_80	AV33	C20	VSS_51
R46	VSS_254	VSS_13	AR33	A20	VSS_4
P46	VSS_249	VSS_109	AL33	BG19	VSS_289
H46	VSS_100	VSS_277	AH33	AL33	VSS_3
F46	VSS_60	VSS_194	AB33	BG17	VSS_288
BF44	VSS_265	VSS_70	P33	BC17	VSS_207
AH44	VSS_198	VSS_247	L33	AW17	VSS_86
AD44	VSS_105	VSS_154	H33	AT17	VSS_18
AA44	VSS_38	VSS_97	N32	R17	VSS_250
Y44	VSS_346	VSS_217	K32	M17	VSS_184
U44	VSS_300	VSS_149	F32	H17	VSS_184
T44	VSS_272	VSS_56	C32	C17	VSS_94
M44	VSS_188	VSS_336	A31	BA16	VSS_332
F44	VSS_59	VSS_7	AN29	AI16	VSS_172
BC43	VSS_236	VSS_309	T29	AI16	VSS_42
AV43	VSS_82	VSS_268	N29	NI16	VSS_307
AU43	VSS_48	VSS_216	K29	K16	VSS_213
AM43	VSS_301	VSS_148	H29	F29	VSS_129
I43	VSS_126	VSS_96	F29	G16	VSS_64
C43	VSS_339	VSS_54	A29	E16	VSS_27
BG42	VSS_295	VSS_6	BG28	BG15	VSS_27
AY42	VSS_117	VSS_291	BD28	AC15	VSS_287
AT42	VSS_24	VSS_240	BA28	W15	VSS_72
AM42	VSS_312	VSS_175	AV28	A15	VSS_320
AE42	VSS_233	VSS_78	AT28	BG14	VSS_2
N42	VSS_135	VSS_21	AR28	AA14	VSS_286
VSS_219		VSS_12	AJ28	C14	VSS_33
L42	VSS_157	VSS_229	AG28	BG13	VSS_331
BD41	VSS_242	VSS_167	AE28	BC13	VSS_285
AU41	VSS_47	VSS_131	AB28	BA13	VSS_206
AM41	VSS_284	VSS_69	Y28	AN13	VSS_171
AH41	VSS_197	VSS_342	P28	AI13	VSS_306
AD41	VSS_104	VSS_147	K28	AE13	VSS_224
AA41	VSS_37	VSS_53	H28	C28	VSS_110
Y41	VSS_345	VSS_95	F28	N13	VSS_212
U41	VSS_299	VSS_335	BF26	L13	VSS_151
T41	VSS_271	VSS_262	AH26	G13	VSS_63
M41	VSS_187	VSS_162	AF26	E13	VSS_26
G41	VSS_90	VSS_68	AB26	BF12	VSS_260
B41	VSS_143	VSS_34	AA26	AV12	VSS_76
BG40	VSS_294	VSS_334	C26	AT12	VSS_17
BB40	VSS_203	VSS_139	B26	AM12	VSS_280
AV40	VSS_81	VSS_316	BH25	AA12	VSS_32
AM40	VSS_311	VSS_239	BD25	J12	VSS_120
H40	VSS_99	VSS_201	BB25	A12	VSS_1
E40	VSS_30	VSS_77	AV25	BD11	VSS_238
AT39	VSS_23	VSS_11	AR25	BB11	VSS_180
AM39	VSS_283	VSS_228	AC25	AY11	VSS_115
AJ39	VSS_232	VSS_74	Y25	AN11	VSS_305
AE39	VSS_134	VSS_341	N25	AH11	VSS_168
N39	VSS_218	VSS_153	L25	Y11	VSS_322
I39	VSS_156	VSS_123	J25	N11	VSS_211
B39	VSS_142	VSS_89	G11	G25	VSS_62
BH38	VSS_317	VSS_29	E25	C11	VSS_62
BC38	VSS_235	VSS_29	BF24	BG10	VSS_330
BA38	VSS_177	VSS_261	AD12	AV10	VSS_267
AU38	VSS_46	VSS_36	AY24	AT10	VSS_75
AH38	VSS_196	VSS_116	AT24	AI10	VSS_16
AD38	VSS_103	VSS_20	AJ24	AE10	VSS_223
AA38	VSS_36	VSS_227	AH24	AA10	VSS_109
Y38	VSS_344	VSS_192	AF24	M10	VSS_10
U38	VSS_298	VSS_161	AB24	BF9	VSS_183
T38	VSS_270	VSS_97	R24	BC9	VSS_266
I38	VSS_125	VSS_252	L24	AN9	VSS_237
F38	VSS_58	VSS_152	K24	AM9	VSS_326
C38	VSS_338	VSS_146	J24	G9	VSS_304
BF37	VSS_264	VSS_122	G24	B9	VSS_108
BB37	VSS_202	VSS_88	F24	BH8	VSS_92
AW37	VSS_113	VSS_52	E24	BB8	VSS_170
AT37	VSS_22	VSS_315	BH23	AV8	VSS_318
AN37	VSS_310	VSS_166	AG23	AT8	VSS_205
AJ37	VSS_231	VSS_340	Y23		VSS_85
H37	VSS_98	VSS_138	B23		VSS_41
C37	VSS_337	VSS_5	A23		
BG36	VSS_293	VSS_45	AJ6		
BD36	VSS_241				
AK15	VSS_257				
AU36	VSS_45				

CANTIGA GM

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VSS

VSS NCTF

VSS SCB

NC

AH8		VSS		VSS NCTF		VSS SCB		NC	
Y8	VSS_349	VSS_NCTF_6	AF32	VSS_SCB_4	BH48	NC_10	D2	D2	
L8	VSS_182	VSS_NCTF_3	AB32	VSS_SCB_3	BH1	NC_8	C3	C3	
E8	VSS_31	VSS_NCTF_16	V32	VSS_SCB_2	A48	NC_42	B4	B4	
B8	VSS_169	VSS_NCTF_8	AJ30	VSS_SCB_5	C1	NC_14	A5	A5	
AU7	VSS_137	VSS_NCTF_14	AM29	VSS_SCB_1	A3	NC_5	A6	A6	
AN7	VSS_50	VSS_NCTF_5	AF29			NC_6	A43	A43	
AJ7	VSS_325	VSS_NCTF_2	AB29			NC_1	A44	A44	
AE7	VSS_256	VSS_NCTF_13	U26			NC_2	B45	B45	
AA7	VSS_136	VSS_NCTF_12	U23			NC_15	C46	C46	
N7	VSS_39	VSS_NCTF_10	AL20			NC_43	D47	D47	
I7	VSS_221	VSS_NCTF_15	V20			NC_9	B47	B47	
L7	VSS_128	VSS_NCTF_4	AL17			NC_16	A46	A46	
BG6	VSS_314	VSS_NCTF_9	AJ17			NC_3	F48	F48	
BD6	VSS_244	VSS_NCTF_7	AA17			NC_13	E48	E48	
AV6	VSS_111	VSS_NCTF_1	U17			NC_11	C48	C48	
AT6	VSS_40					NC_7	B48	B48	
AM6	VSS_303								
M6	VSS_189								
C6	VSS_25								
BA5	VSS_179								
AH5	VSS_199								
AD5	VSS_107								
Y5	VSS_348								
L5	VSS_181								
J5	VSS_127								
H5	VSS_119								
F5	VSS_61								
BE4	VSS_259								
BC3	VSS_209								
AV3	VSS_79								
AL3	VSS_258								
R3	VSS_184								
P3	VSS_253								
F3	VSS_246								
BA2	VSS_55								
AW2	VSS_173								
AJ2	VSS_87								
AR2	VSS_43								
AP2	VSS_329								
AJ2	VSS_327								
AH2	VSS_225								
AF2	VSS_190								
AE2	VSS_159								
AD2	VSS_130								
AC2	VSS_102								
Y2	VSS_73								
M2	VSS_323								
K2	VSS_185								
AM1	VSS_144								
AA1	VSS_279								
P1	VSS_9								
H1	VSS_222								
U24	VSS_93								
U28	VSS_274								
U25	VSS_276								
U29	VSS_275								
U29	VSS_296								

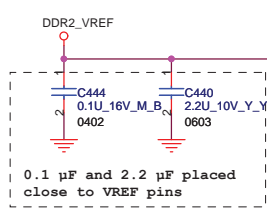
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title <b>Cantiga (VSS) 777</b>		
Size <b>A3</b>	Document Number <b>M790-1-01</b>	Rev <b>1.0</b>
Date <b>Wednesday, July 02, 2008</b>	Sheet <b>13</b>	of <b>54</b>

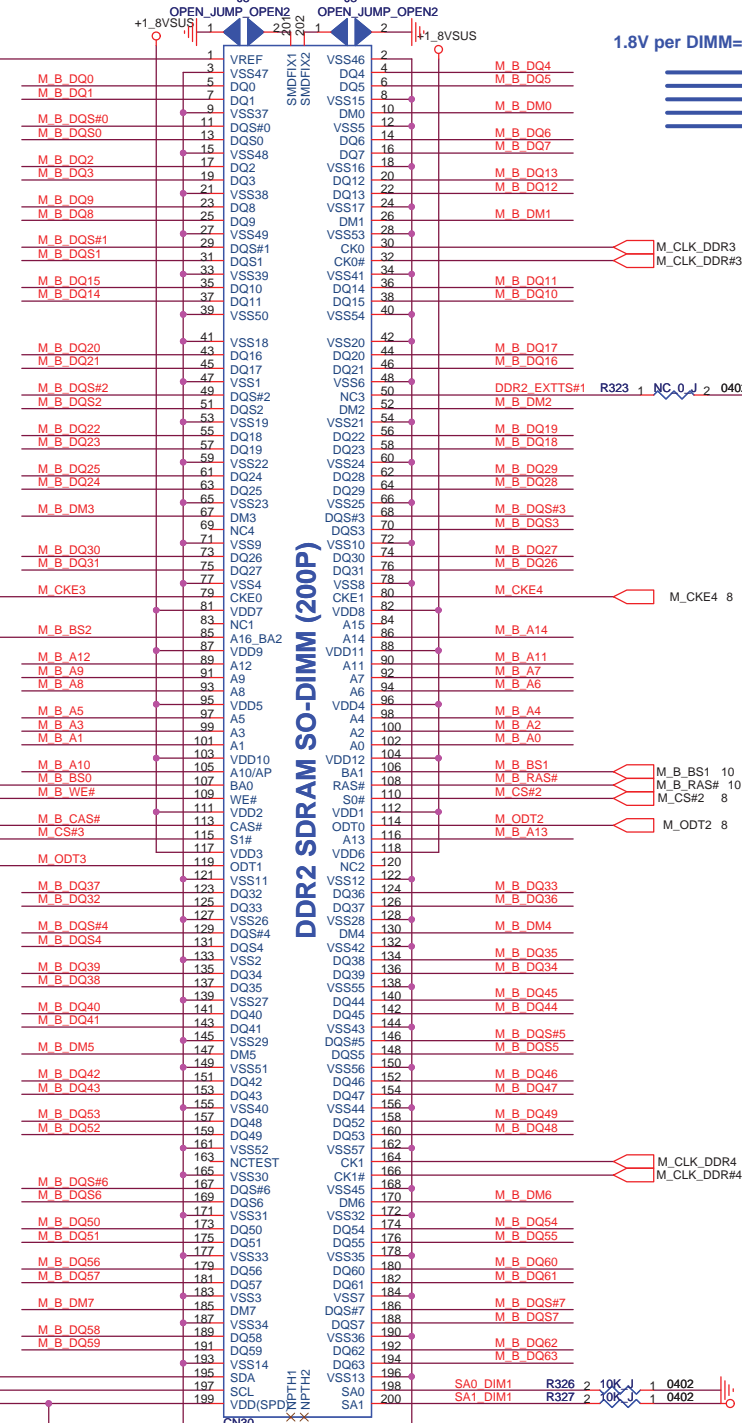








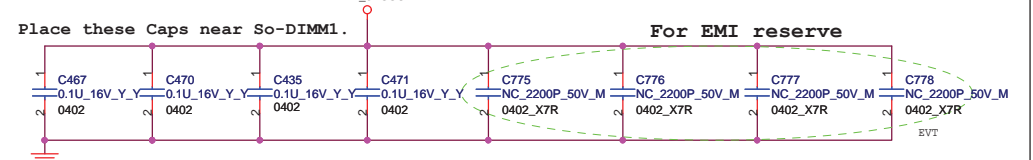
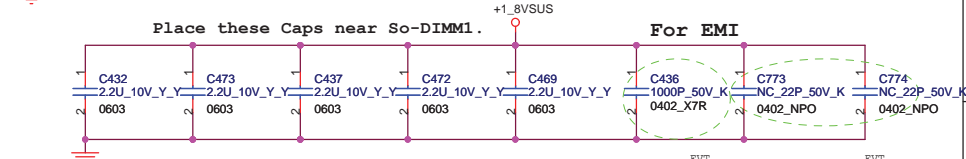
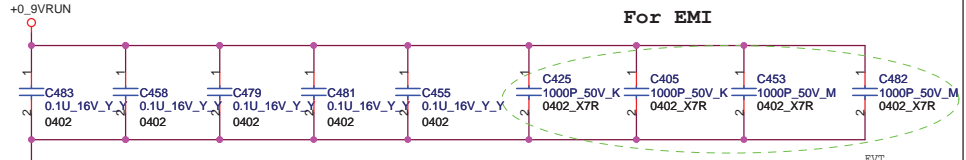
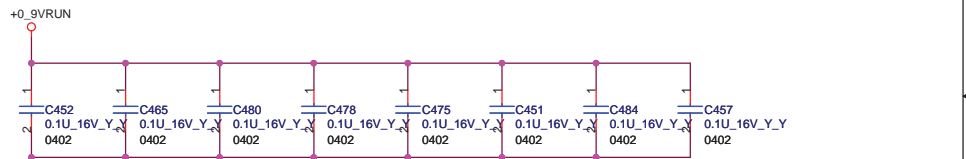
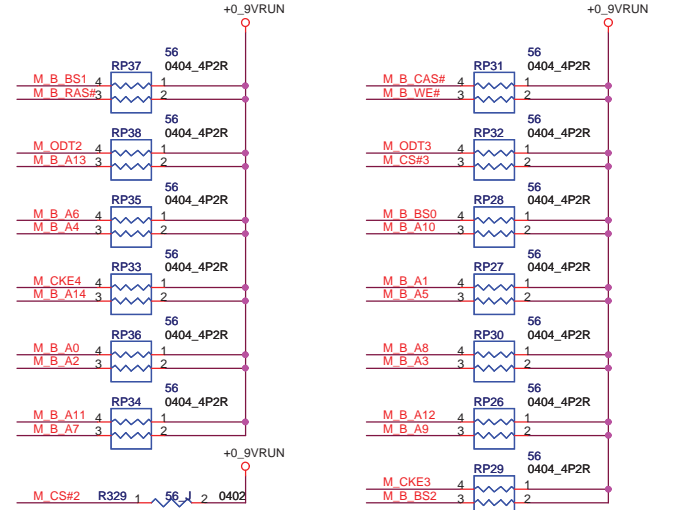
1.8V per DIMM=3.08A Height = 4 mm



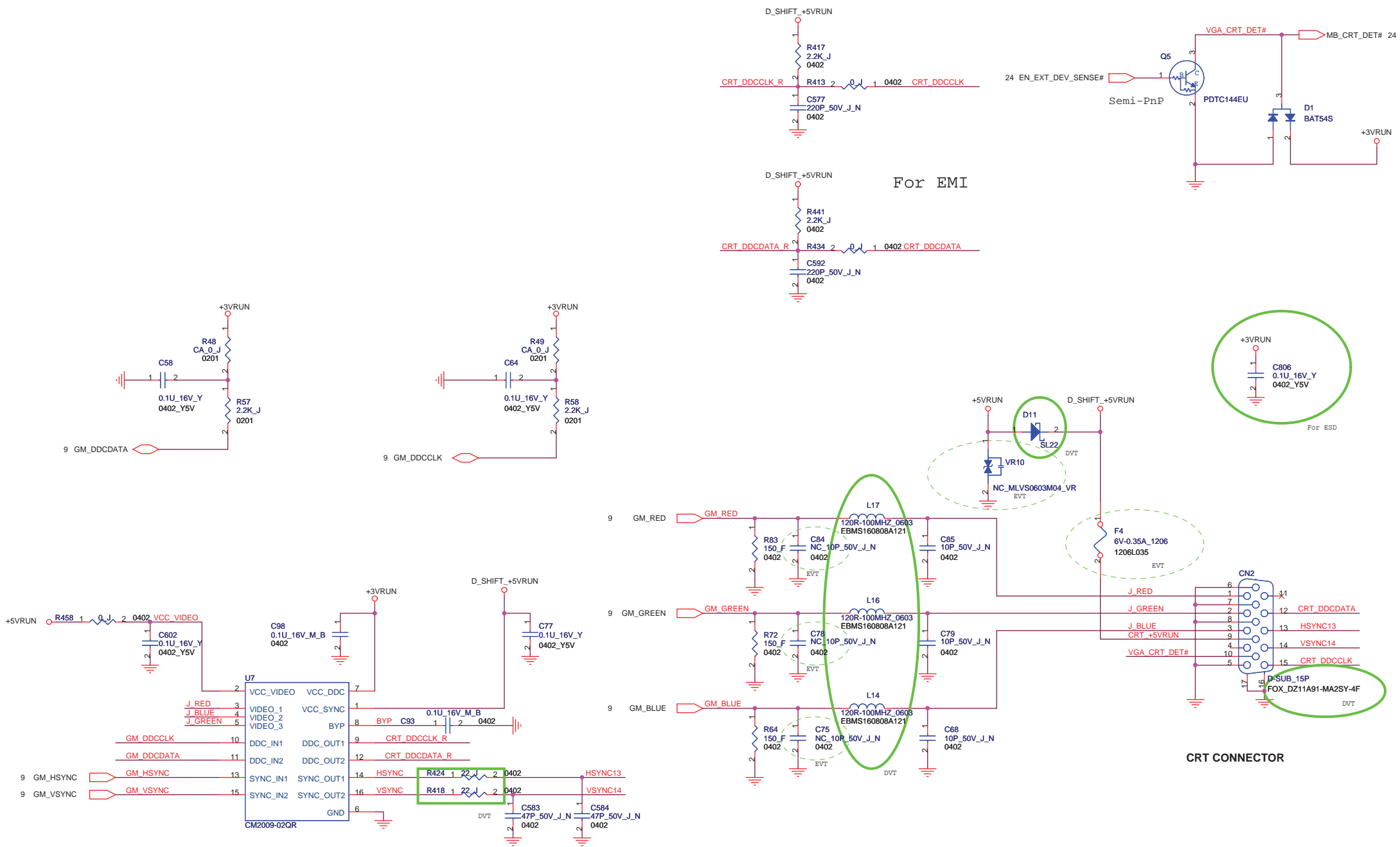
DDR2 SDRAM SO-DIMM (200P)

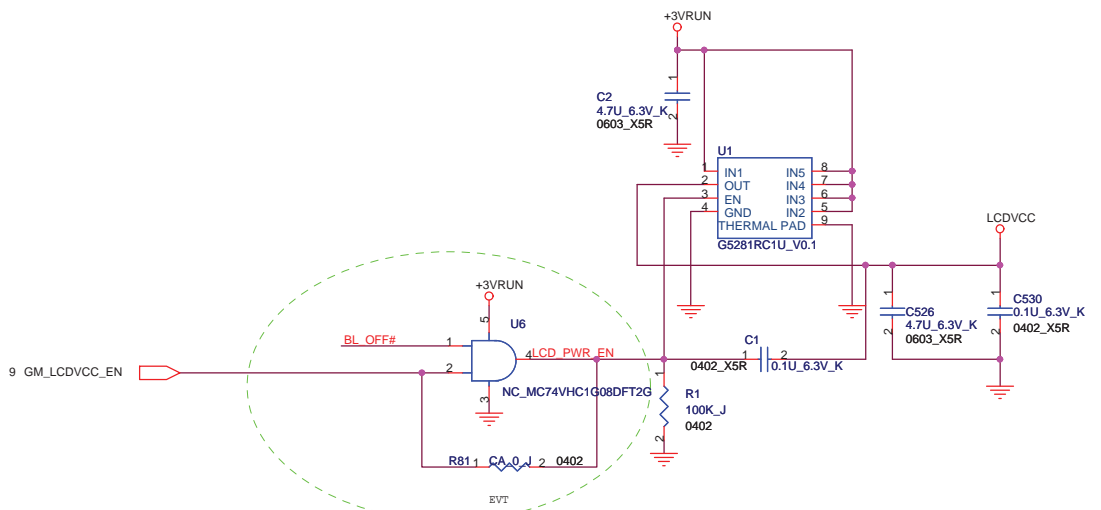
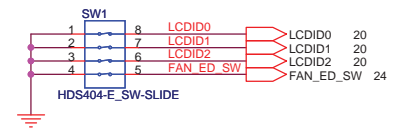
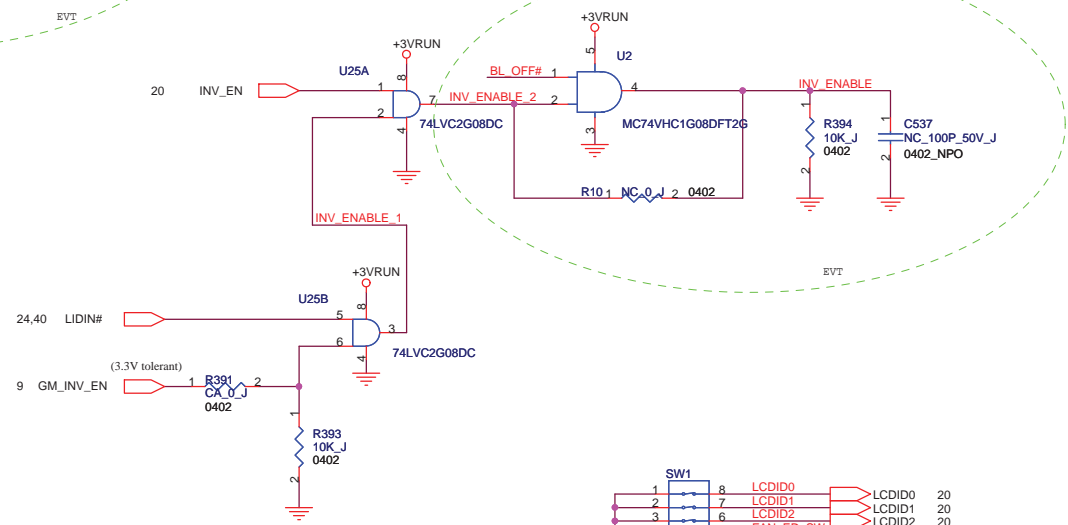
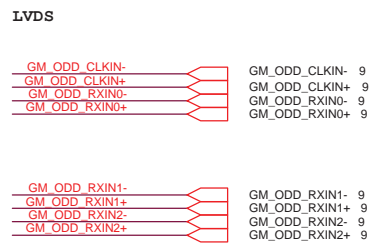
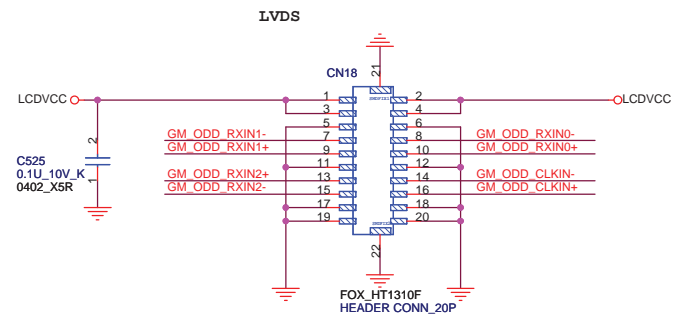
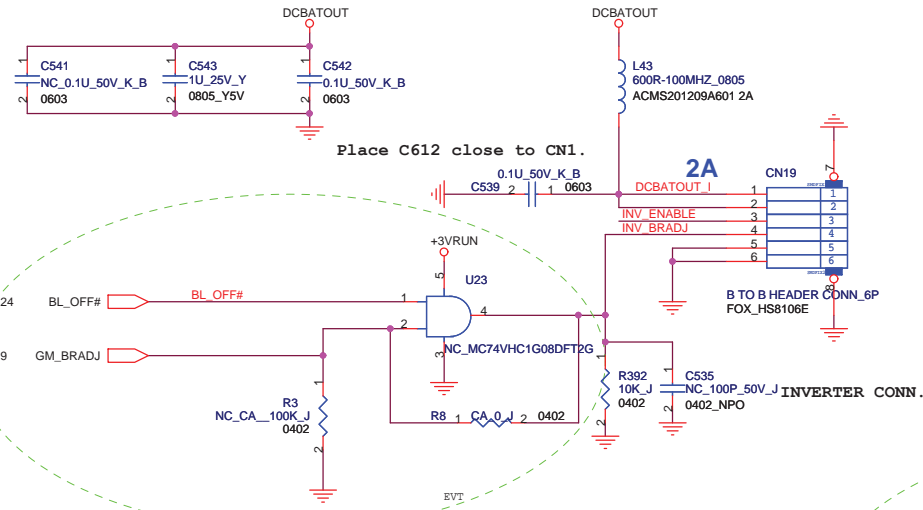
SMBus Address: A4(W)/A5(R)

DIMM\_1 is placed farther from the GMCH than DIMM\_0



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: <b>DDR(H)SO-DIMM_1</b>			
Size: A3	Document Number: M790-1-01	Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet: 15	of 54	





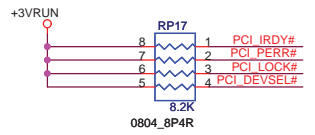
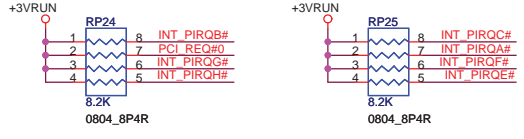
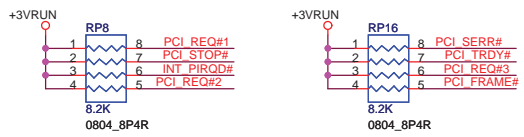
PANEL ID

Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vendor	AUO	CPI	LPL	LPL
Device Name	B154EW02V7	CLAA154WB03	LP154WX4-TLC5	LP154WX5-TLA1
Panel ID [3..0]	001	010	011	100

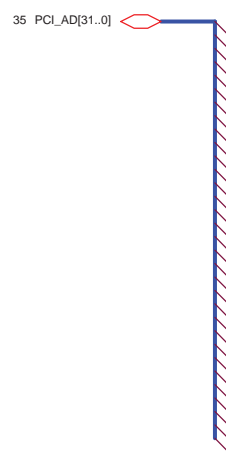
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **LVDS**

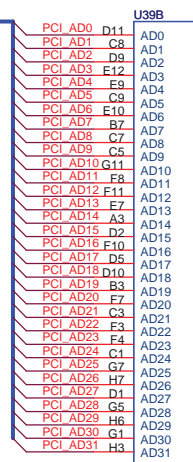
Size A3	Document Number M790-1-01	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 17	of 54



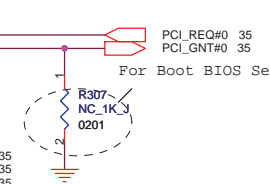
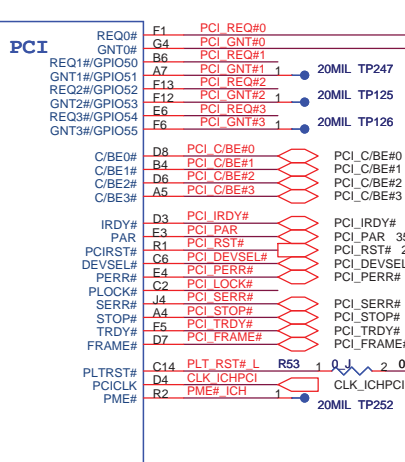
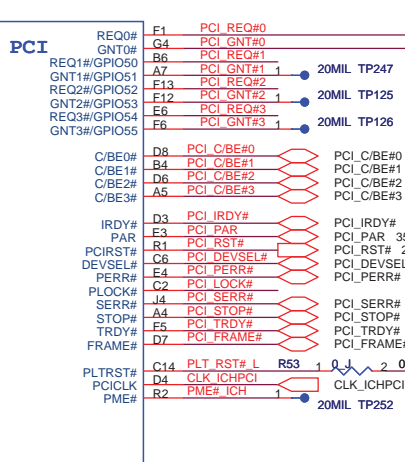
PCI Pullups



U39B



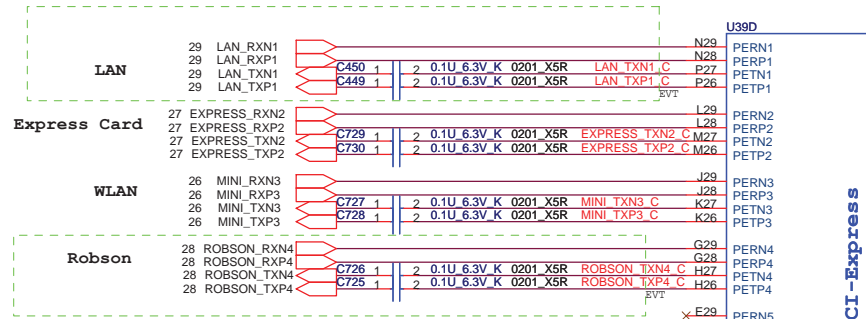
Interrupt I/F



For Boot BIOS Selection.

Strap for Boot-BIOS

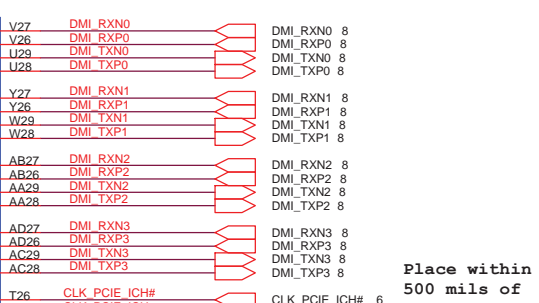
	GNT#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi



U39D

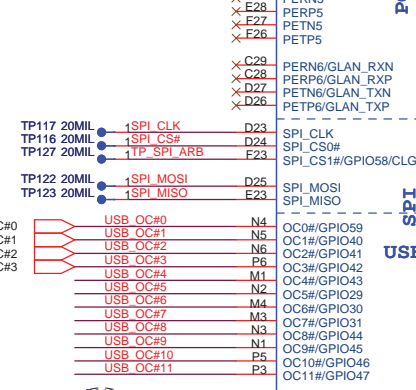


PCI-Express



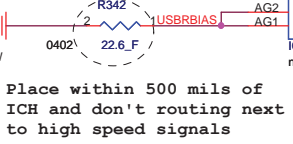
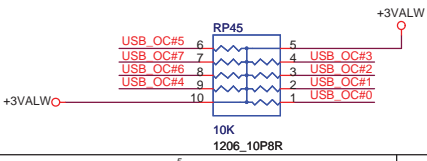
Place within 500 mils of ICH

USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	Ext. Port
PORT-3	Ext. Port
PORT-4	
PORT-5	EXPRESS CARD
PORT-6	
PORT-7	Camera
PORT-8	Felica
PORT-9	
PORT-10	Wi-MAX
PORT-11	



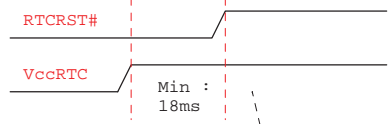
ICH9M

USB



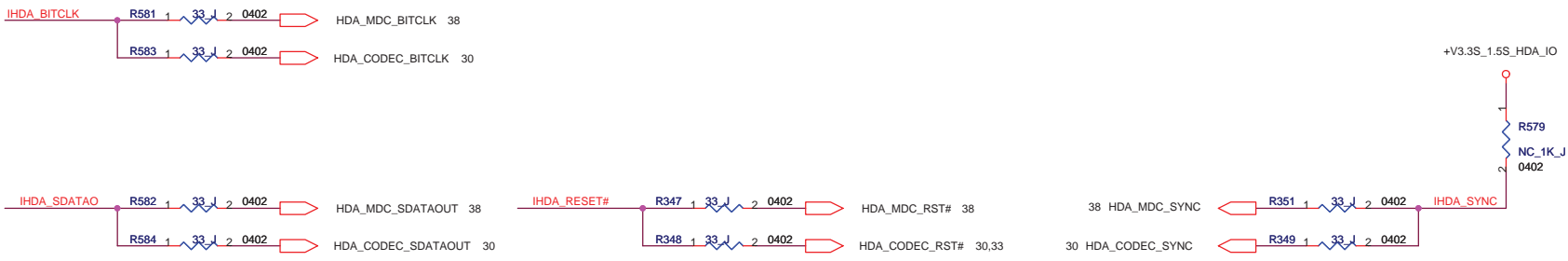
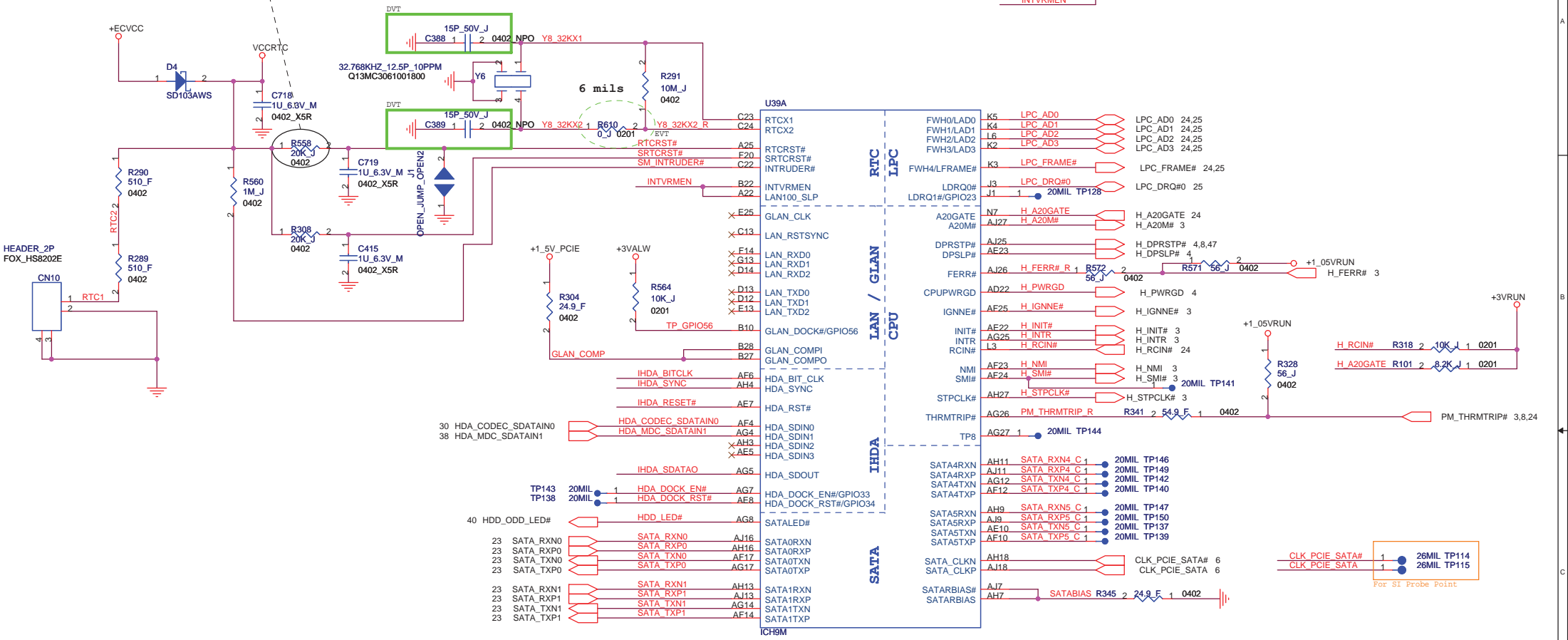
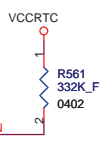
Place within 500 mils of ICH and don't routing next to high speed signals

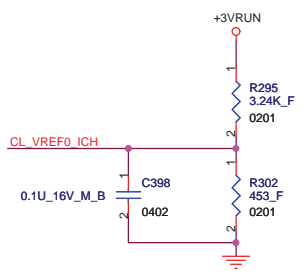
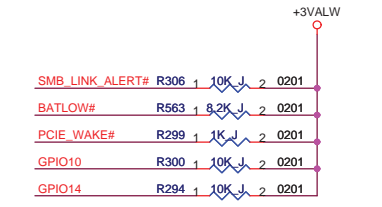
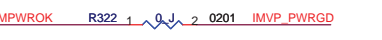
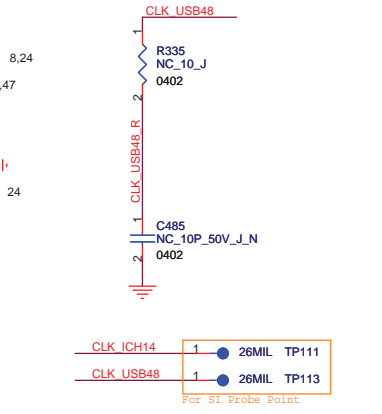
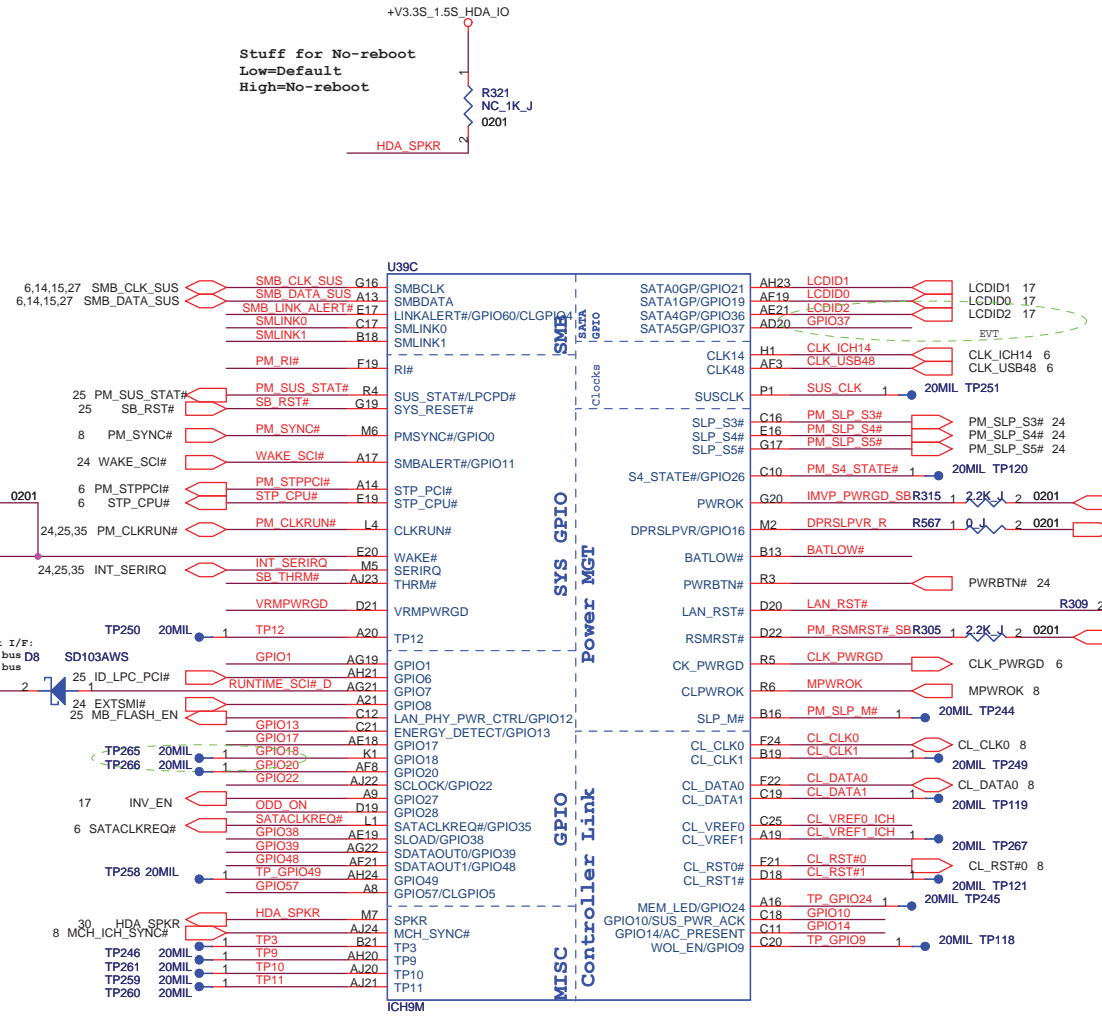
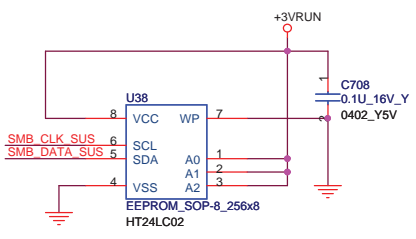
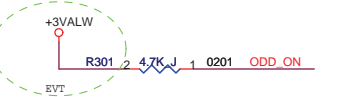
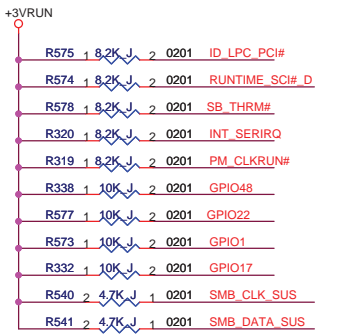
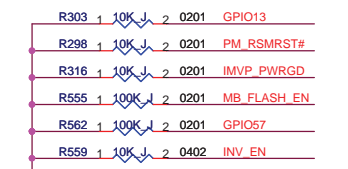
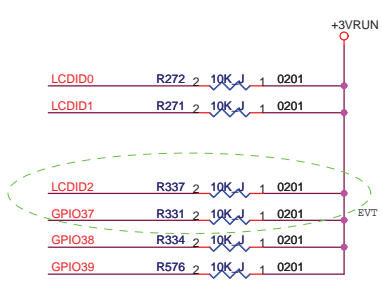
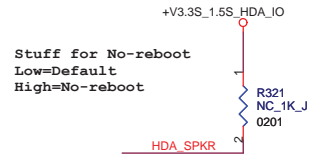
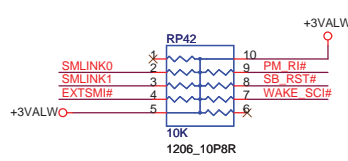
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division  
 Title: **ICH9-M (PCI/DMI/USB/PCIE) 1/5**  
 Size: A3 Document Number: M790-1-01 Rev: 1.0  
 Date: Wednesday, July 02, 2008 Sheet: 18 of 54



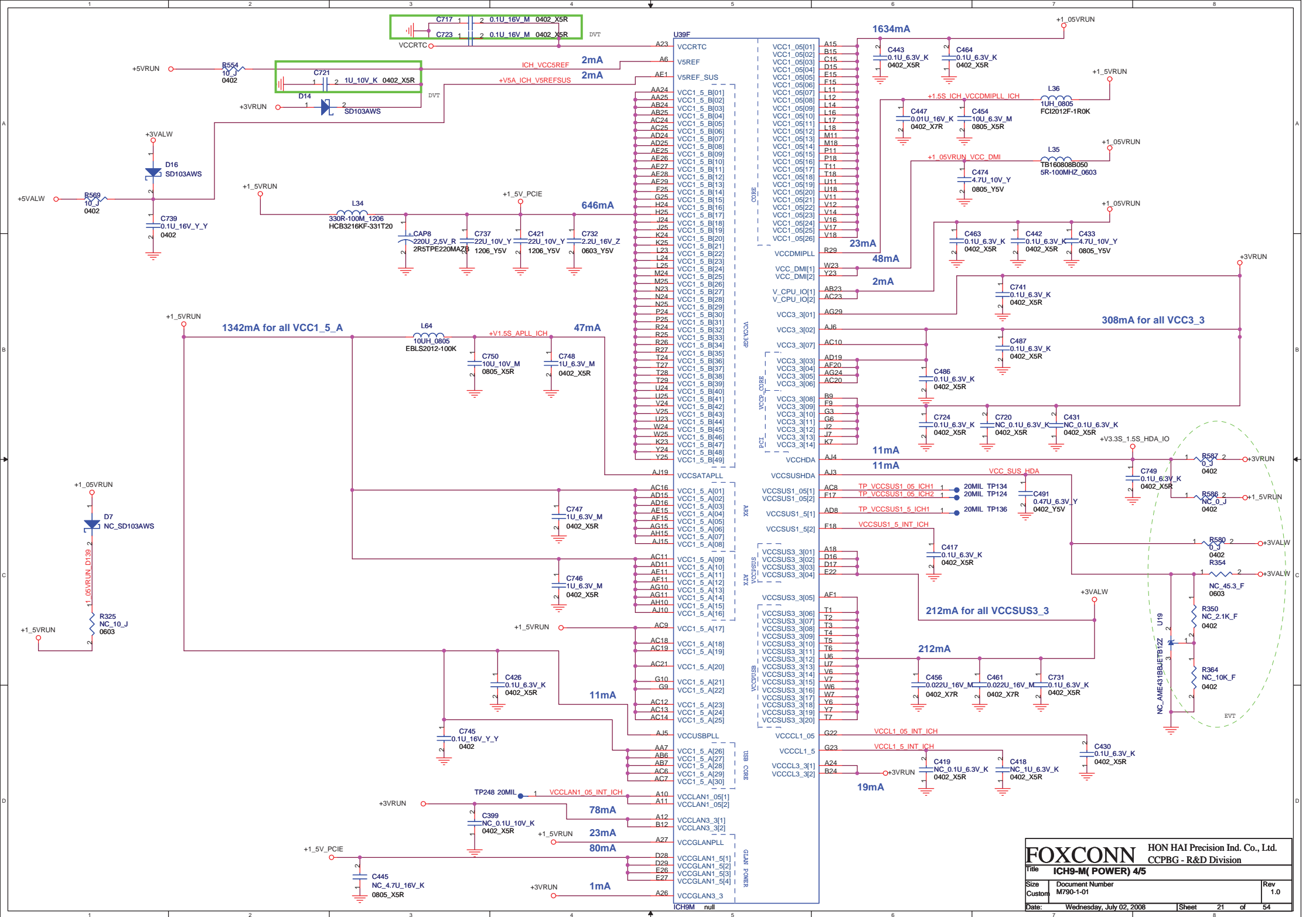
The traces inside this block should be wider.

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCt1_5, VccLAN1_05 and VccCt1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)









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Title: **ICH9-M (POWER) 4/5**

Size	Document Number	Rev
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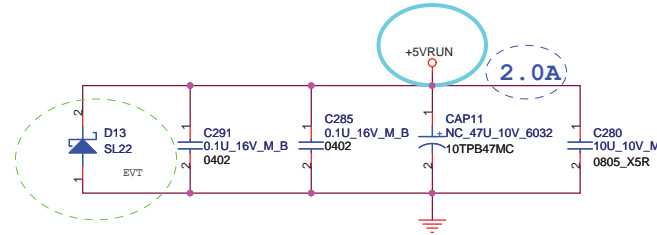
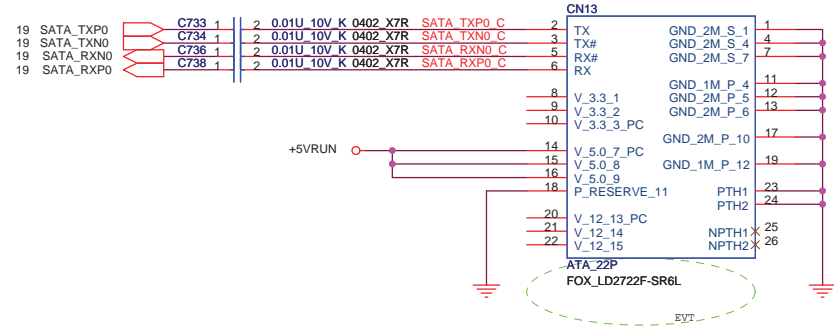
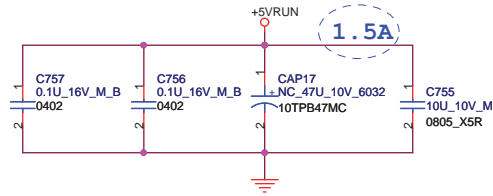
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U39E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB23	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD5	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AE13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF26	VSS[047]	VSS[153]	R13
AF27	VSS[048]	VSS[154]	R14
AF5	VSS[049]	VSS[155]	R15
AF7	VSS[050]	VSS[156]	R16
AF9	VSS[051]	VSS[157]	R17
AG13	VSS[052]	VSS[158]	R18
AG16	VSS[053]	VSS[159]	R28
AG18	VSS[054]	VSS[160]	T12
AG20	VSS[055]	VSS[161]	T13
AG23	VSS[056]	VSS[162]	T14
AG3	VSS[057]	VSS[163]	T15
AG6	VSS[058]	VSS[164]	T16
AG9	VSS[059]	VSS[165]	T17
AH12	VSS[060]	VSS[166]	T23
AH14	VSS[061]	VSS[167]	B26
AH17	VSS[062]	VSS[168]	U12
AH19	VSS[063]	VSS[169]	U13
AH2	VSS[064]	VSS[170]	U14
AH22	VSS[065]	VSS[171]	U15
AH25	VSS[066]	VSS[172]	U16
AH28	VSS[067]	VSS[173]	U17
AH5	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AJ12	VSS[070]	VSS[176]	U27
AJ14	VSS[071]	VSS[177]	U3
AJ17	VSS[072]	VSS[178]	V1
AJ8	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B14	VSS[075]	VSS[181]	V23
B17	VSS[076]	VSS[182]	V28
B2	VSS[077]	VSS[183]	V29
B20	VSS[078]	VSS[184]	V4
B23	VSS[079]	VSS[185]	V5
B5	VSS[080]	VSS[186]	W26
B8	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	W3
C27	VSS[083]	VSS[189]	Y1
E11	VSS[084]	VSS[190]	Y28
E14	VSS[085]	VSS[191]	Y29
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	AG28
E24	VSS[089]	VSS[195]	AH6
E5	VSS[090]	VSS[196]	AF2
E8	VSS[091]	VSS[197]	B25
F16	VSS[092]	VSS[198]	
F28	VSS[093]		
F29	VSS[094]	VSS_NCTF[01]	A1
G12	VSS[095]	VSS_NCTF[02]	A2
G14	VSS[096]	VSS_NCTF[03]	A28
G18	VSS[097]	VSS_NCTF[04]	A29
G21	VSS[098]	VSS_NCTF[05]	AH1
G24	VSS[099]	VSS_NCTF[06]	AH29
G26	VSS[100]	VSS_NCTF[07]	AJ1
G27	VSS[101]	VSS_NCTF[08]	AJ2
G8	VSS[102]	VSS_NCTF[09]	AJ28
H2	VSS[103]	VSS_NCTF[10]	AJ29
H23	VSS[104]	VSS_NCTF[11]	B1
H28	VSS[105]	VSS_NCTF[12]	B29
H29	VSS[106]		

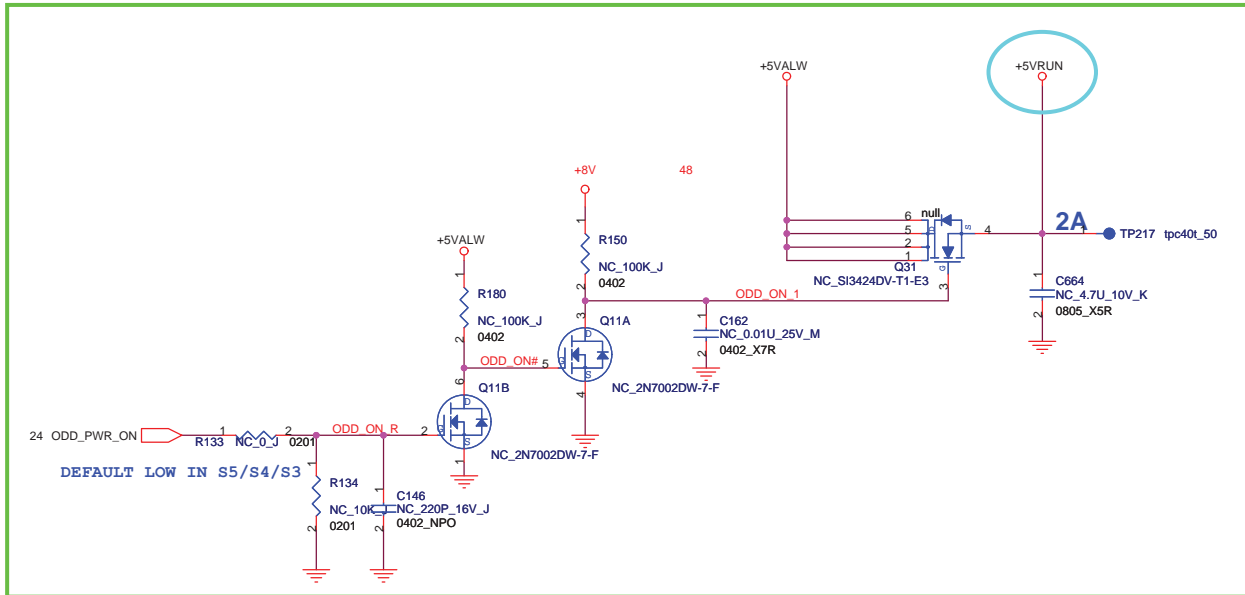
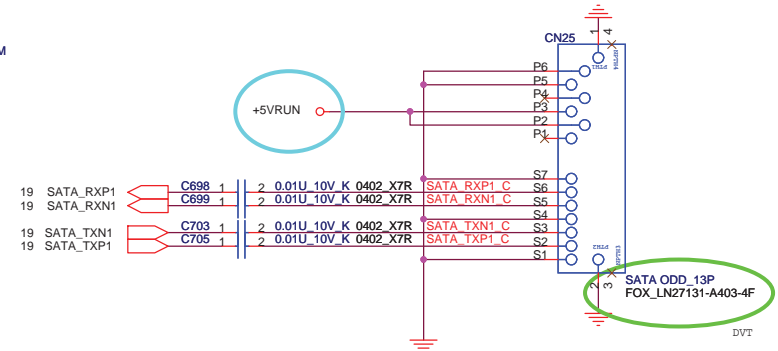
ICH9M

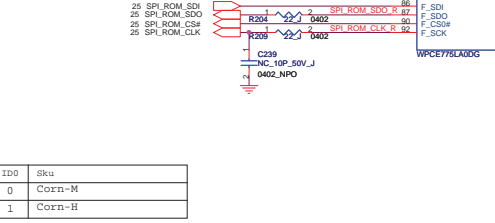
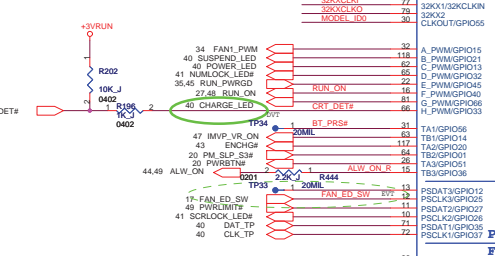
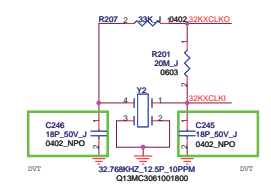
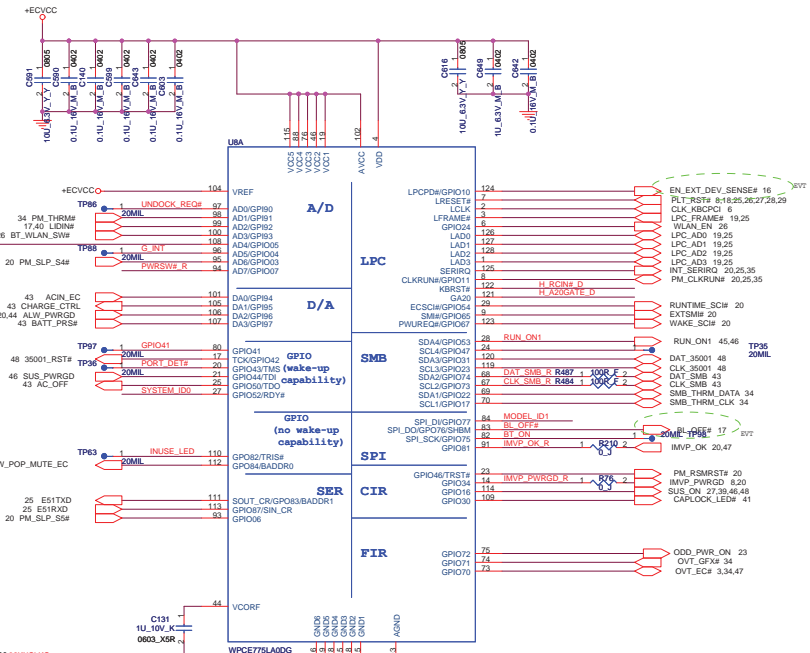
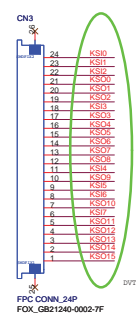
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ICH9-M (GND) 5/5		
Size	Document Number	Rev	
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# SATA HDD CONN



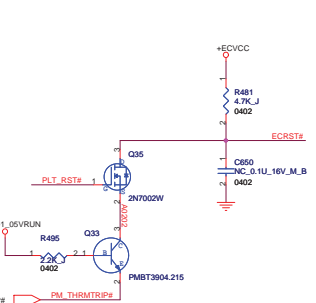
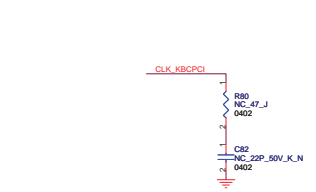
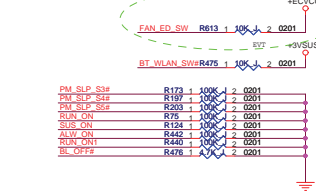
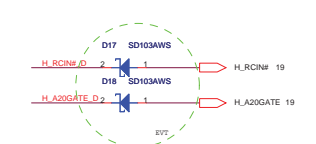
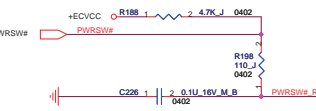
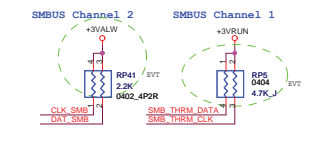
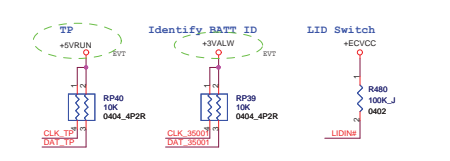
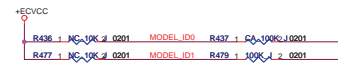
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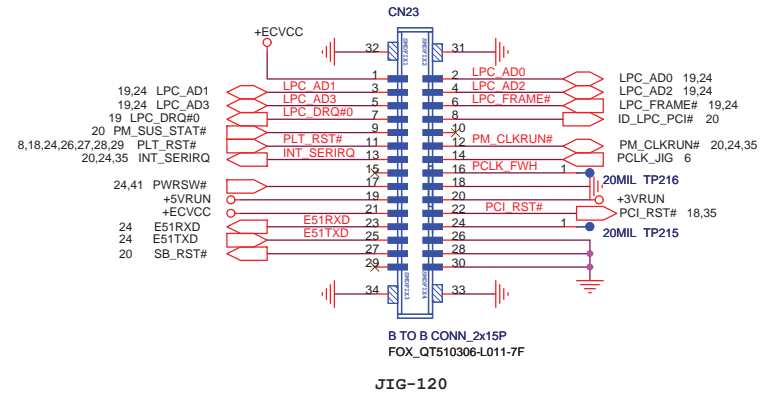
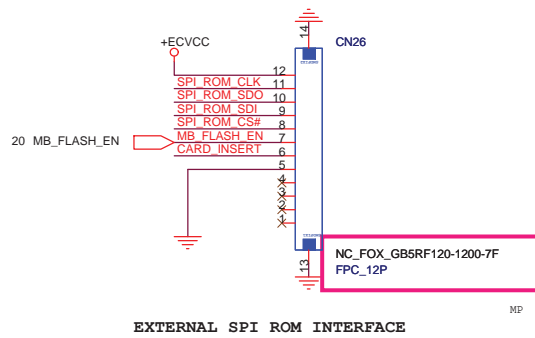
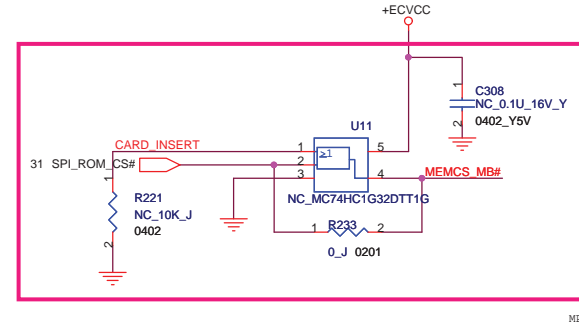
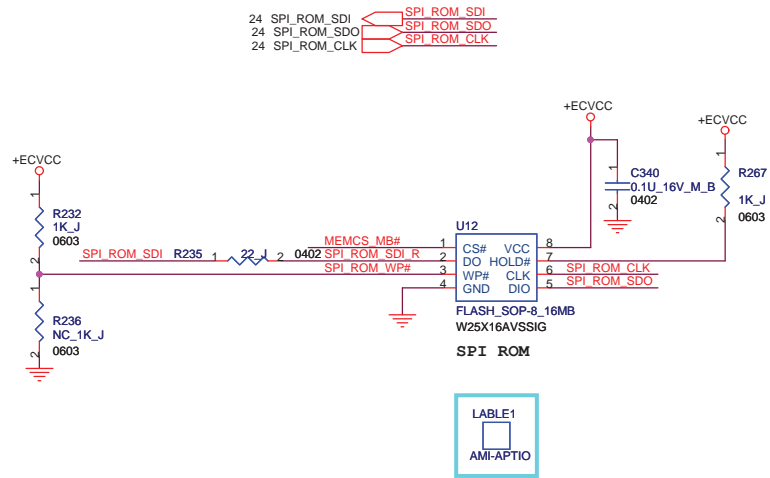




ID1	ID0	SKU
0	0	CoIn-M
0	1	CoIn-H

ID1	ID0	SKU
0	0	M790



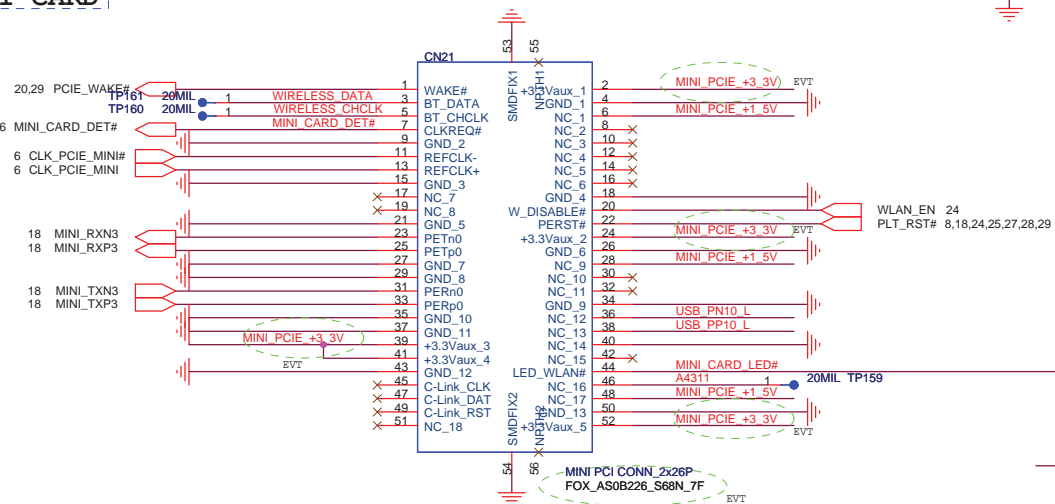
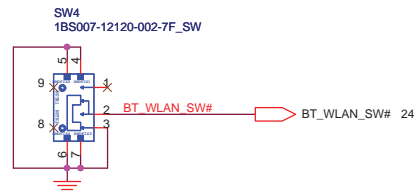




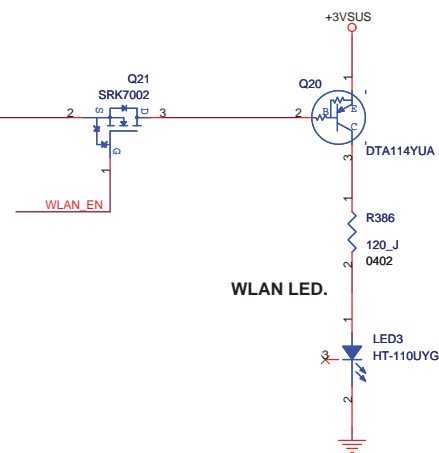
**MINI CARD**

+1\_5V=>0.5A Peak/0.375A Normal  
 +3\_3VAux=>2.75A Peak/1.1A Normal

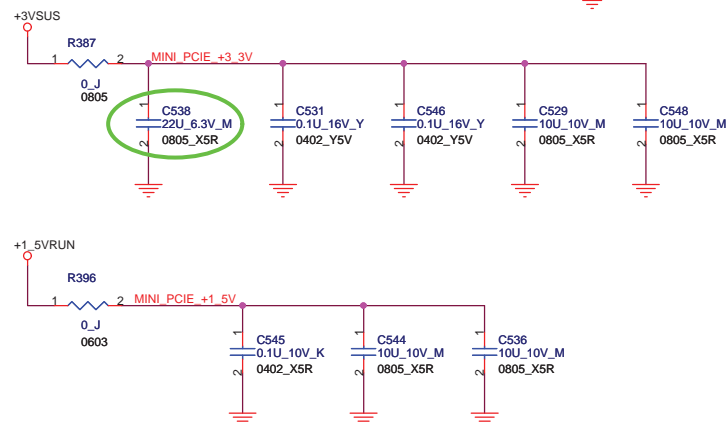
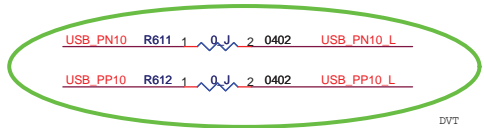
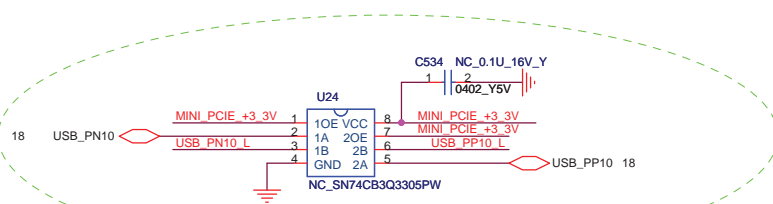
**WLAN ON/OFF Switch**



**Mini Card.  
WLAN**



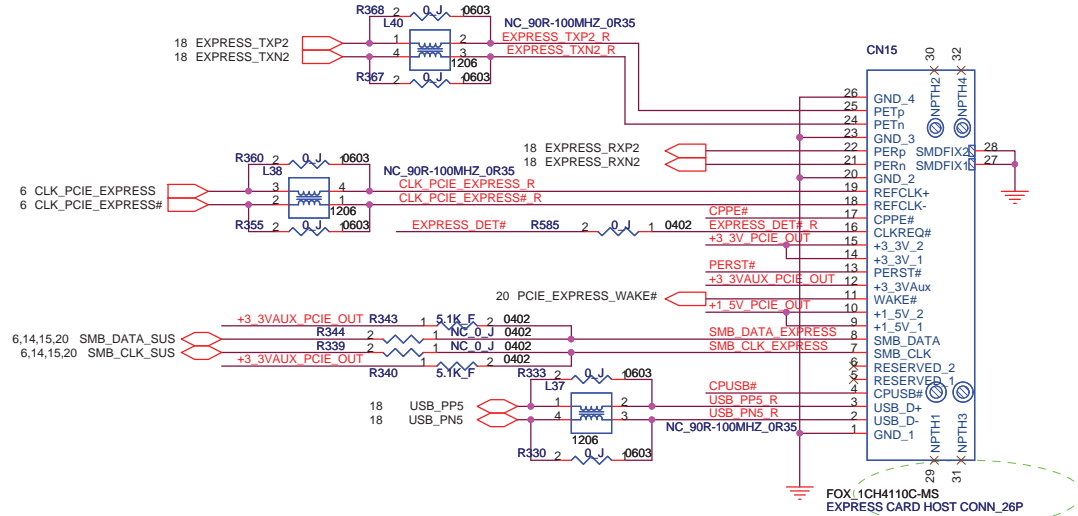
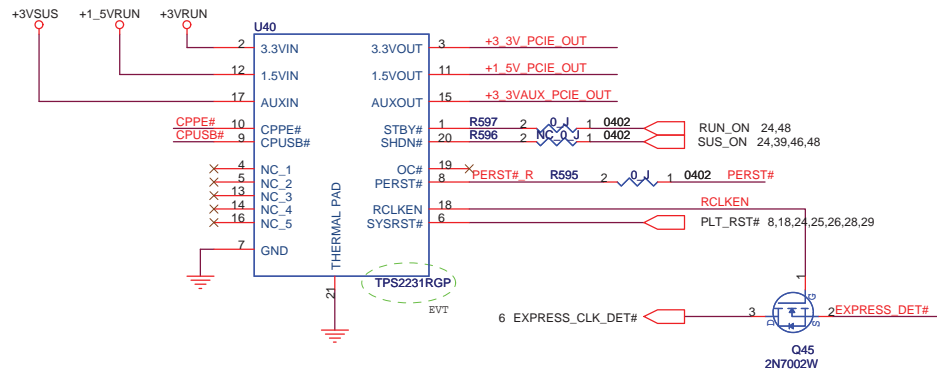
**WLAN LED.**



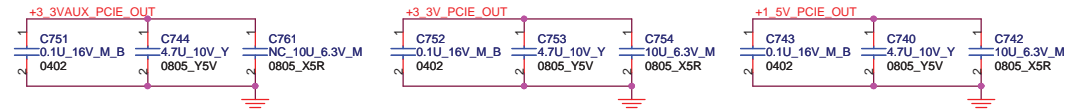
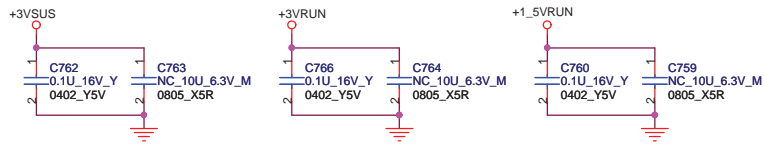
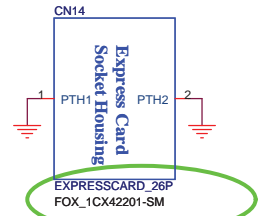


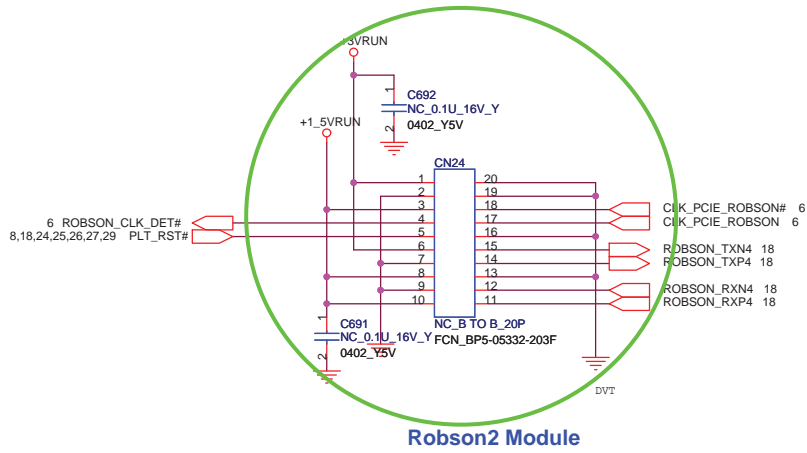
+1\_5V=>1.3A  
 +3\_3VAux=>0.6A  
 +3\_3V=>2.5A

### Express Card Power Switch

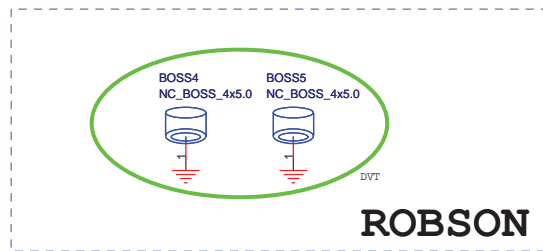


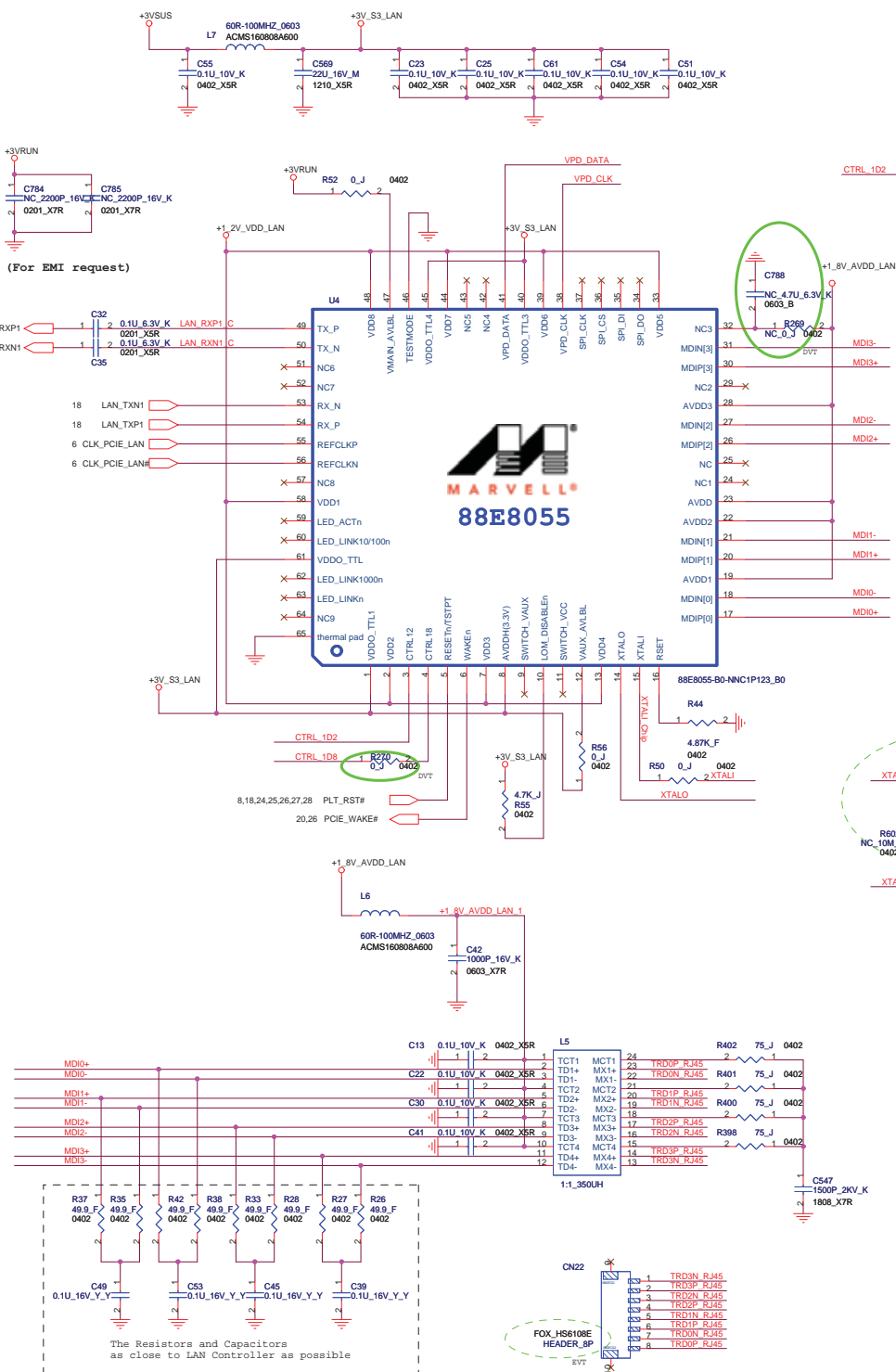
### Express Card Slot.



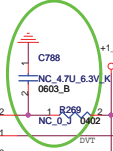


EVT2 11/6 Need to update new connector.

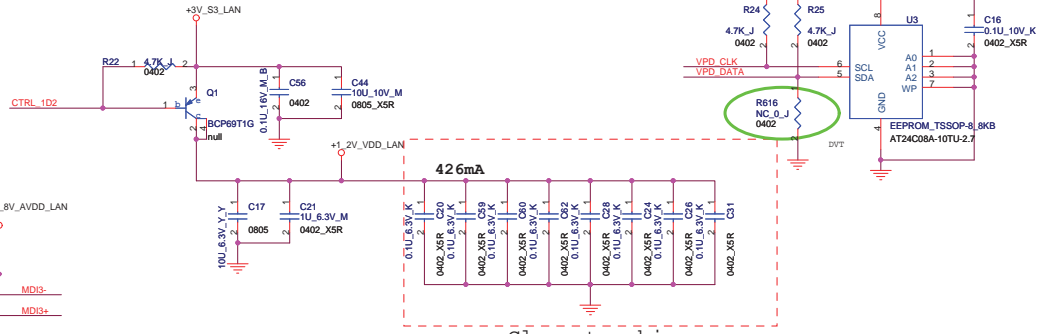




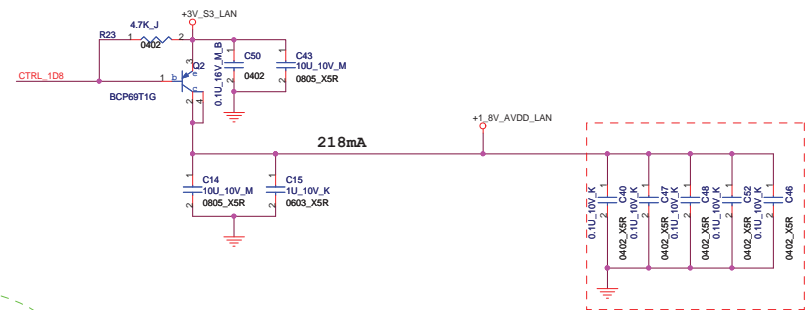
(For EMI request)



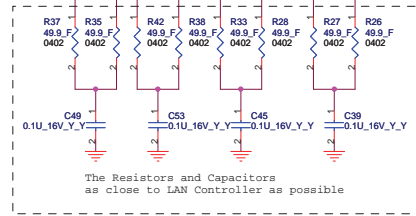
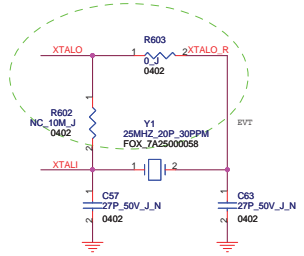
Used EEPROM R616 need NC.  
No used EEPROM R25/U3/C16 need NC.



Close to chip



Close to chip



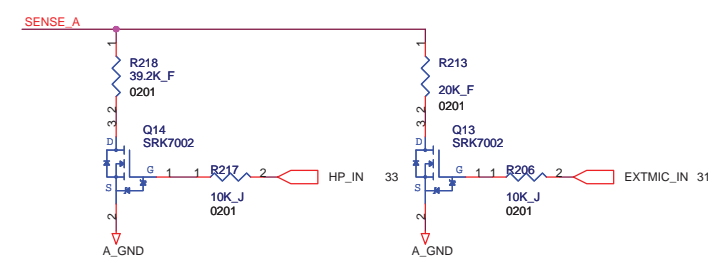
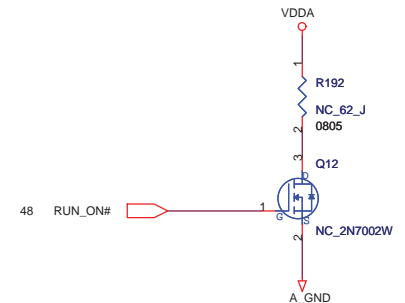
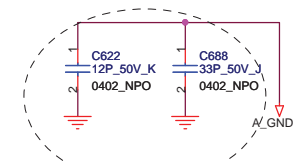
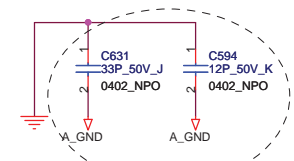
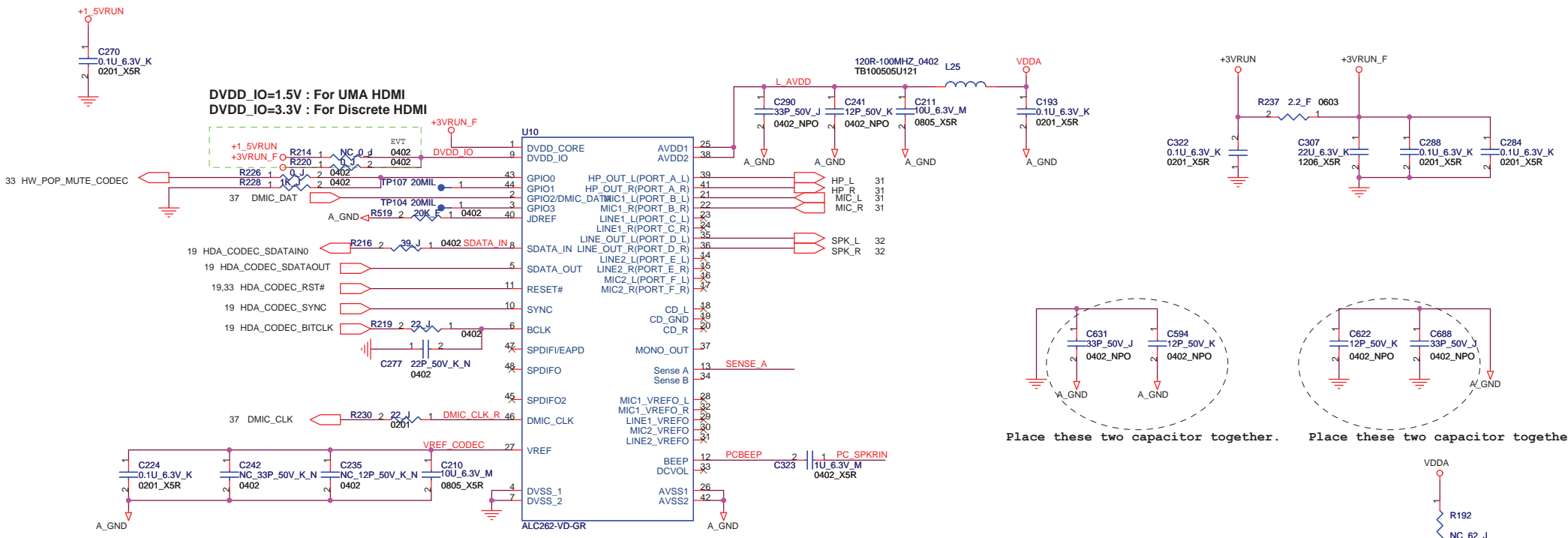
The Resistors and Capacitors as close to LAN Controller as possible

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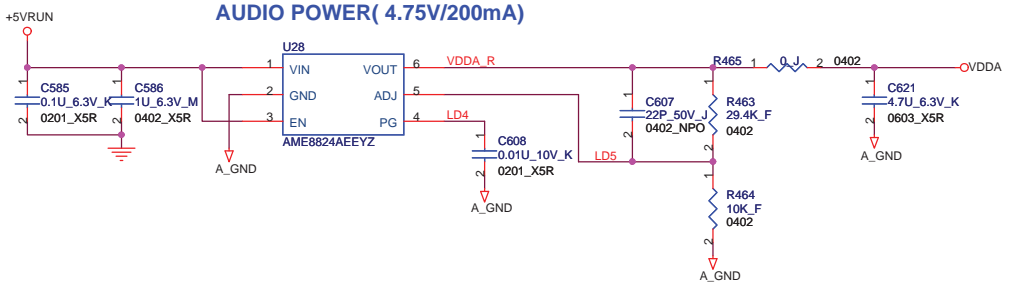
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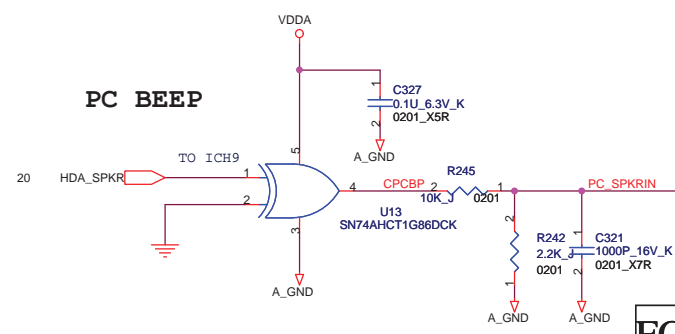
DVDD\_IO=1.5V : For UMA HDMI  
 DVDD\_IO=3.3V : For Discrete HDMI

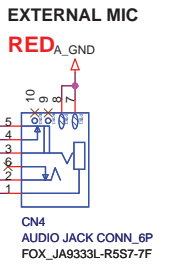
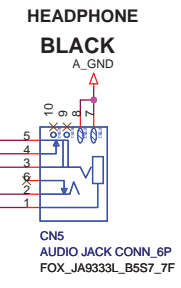
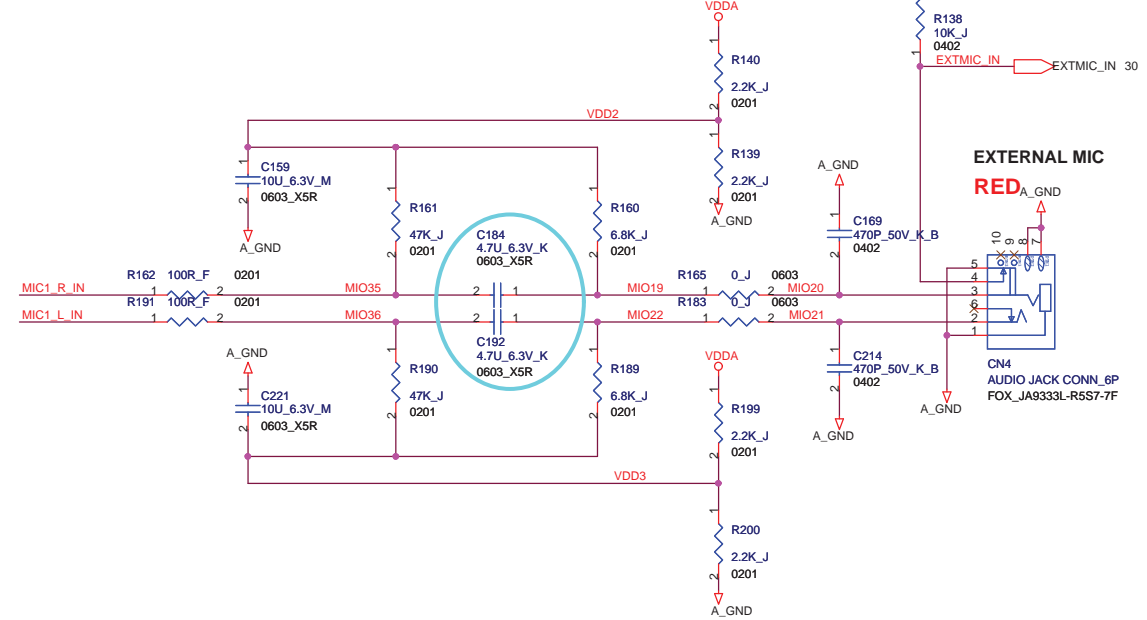
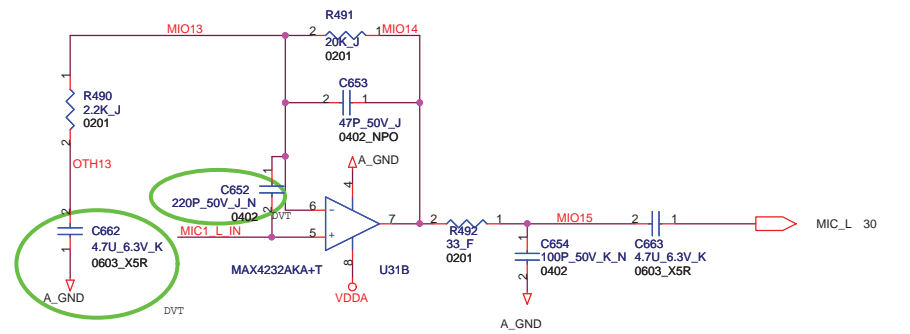
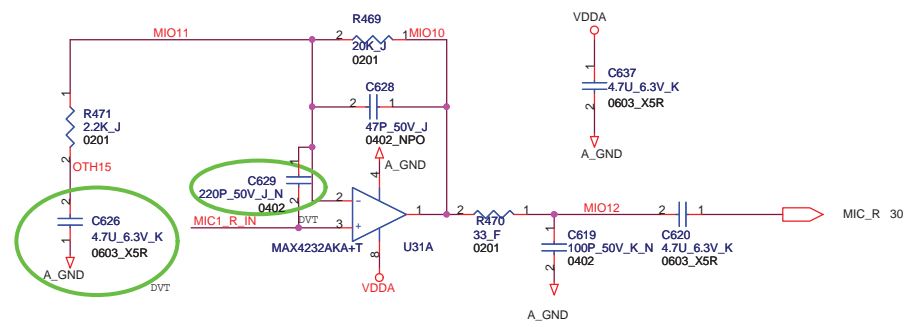
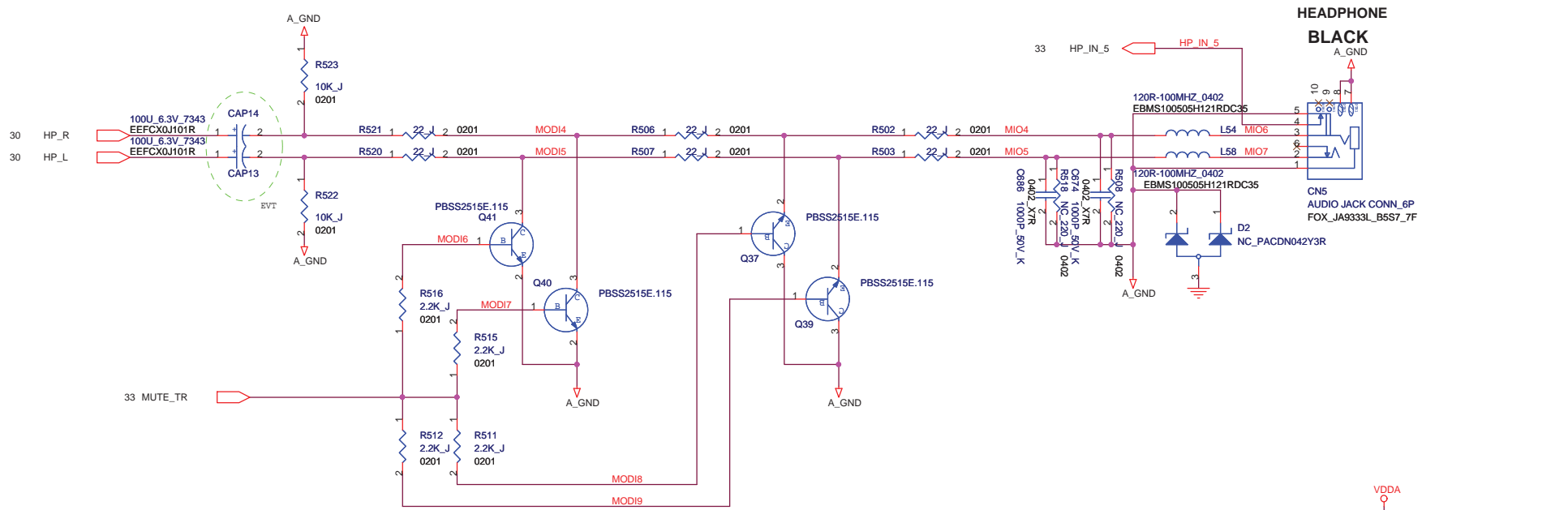


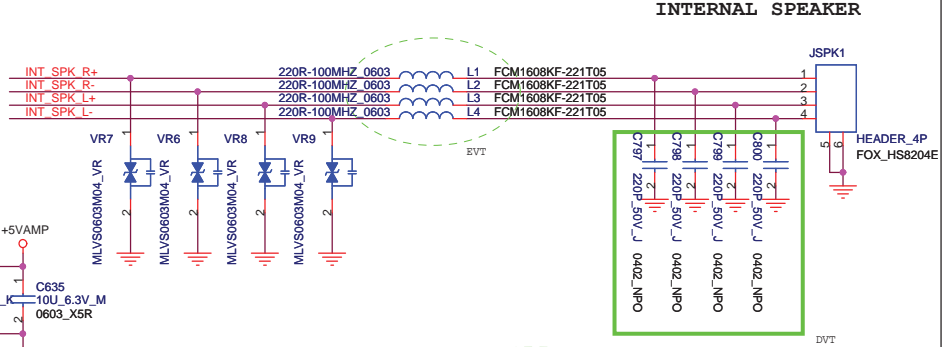
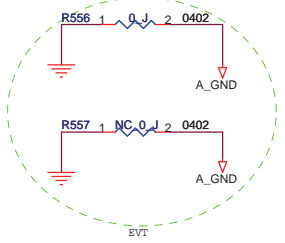
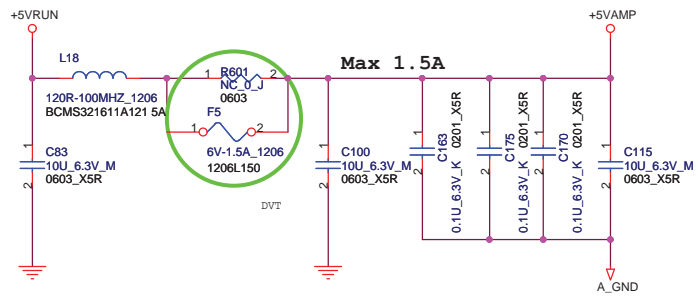
**AUDIO POWER (4.75V/200mA)**



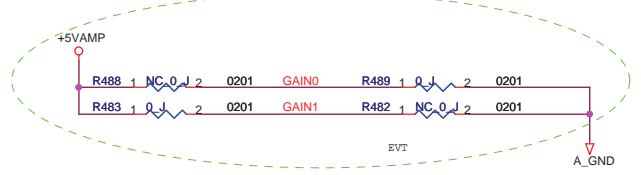
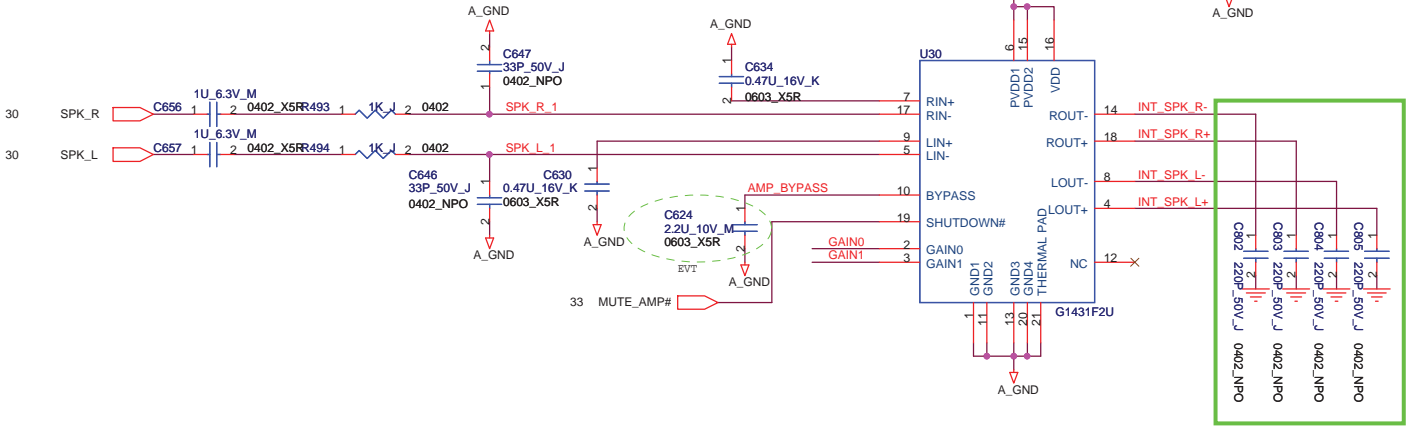
**PC BEEP**





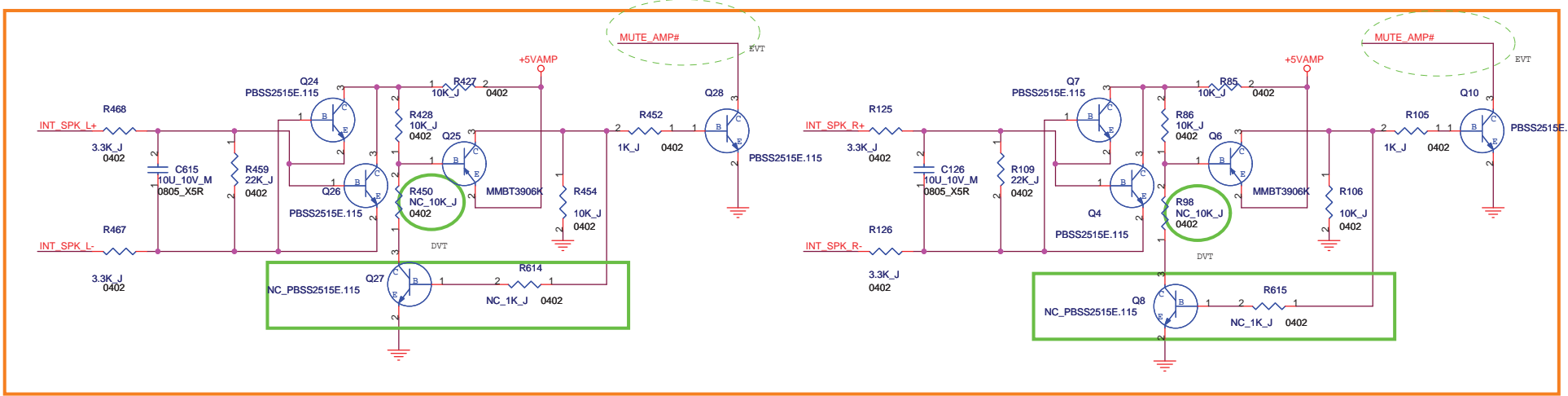


**SPEAKER AMP**

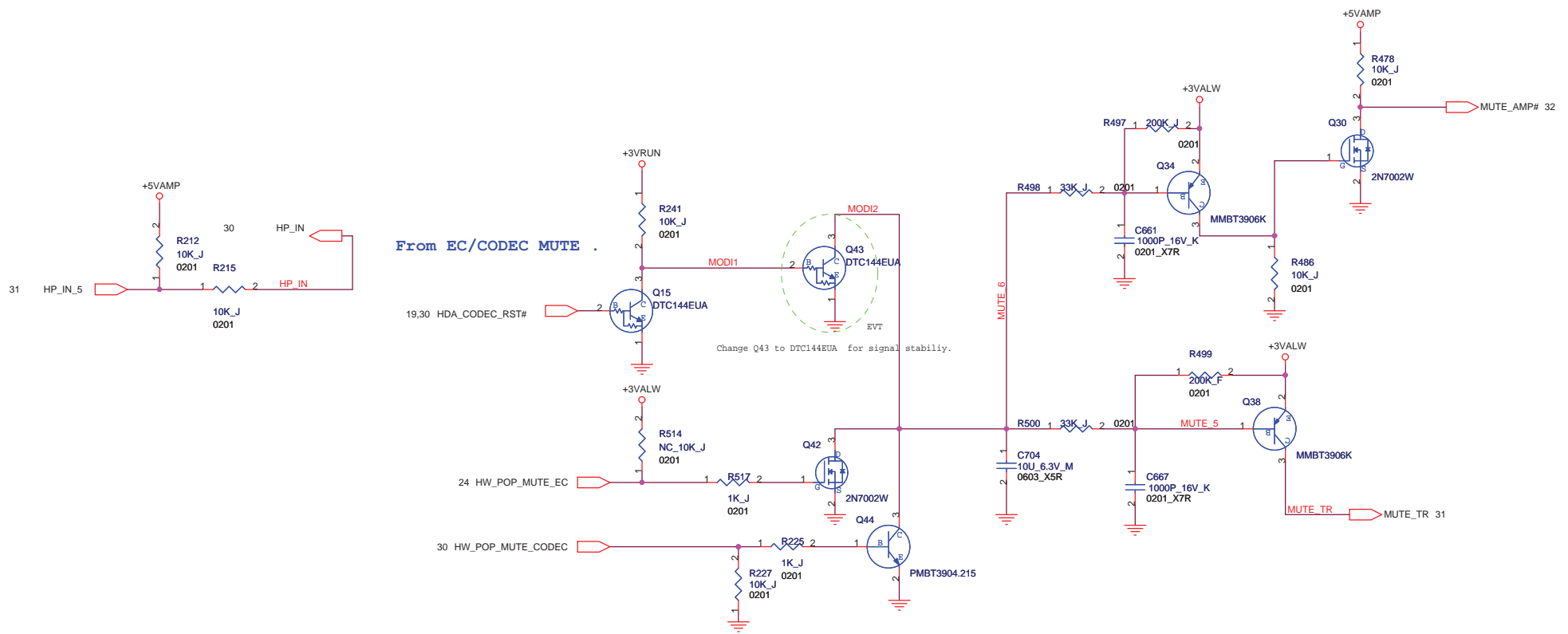


**SPEAKER AMP**

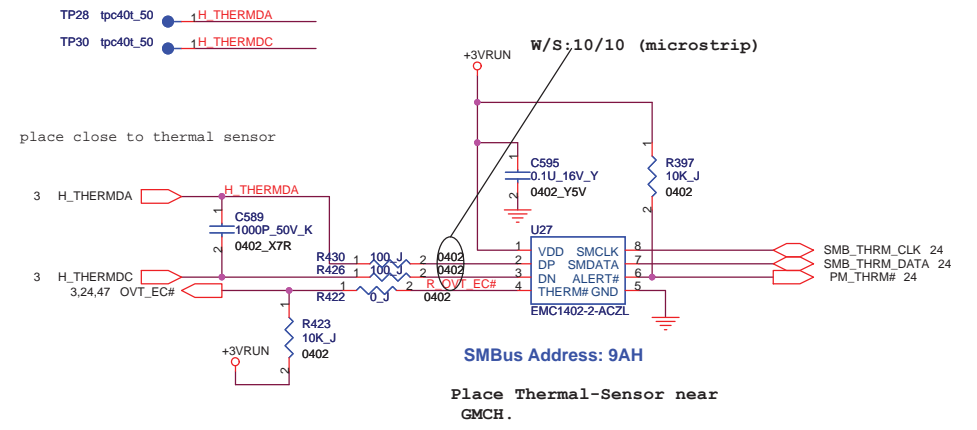
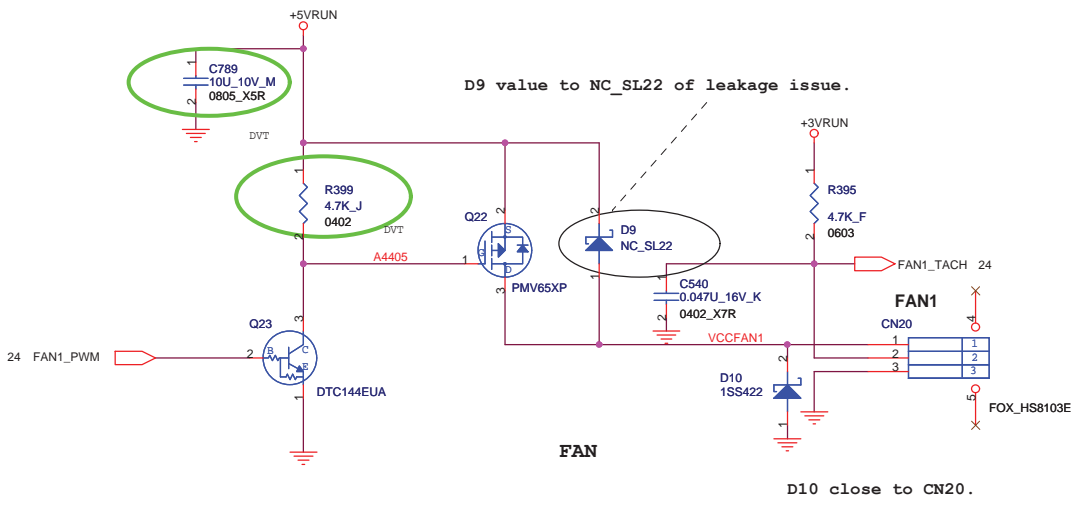
	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1



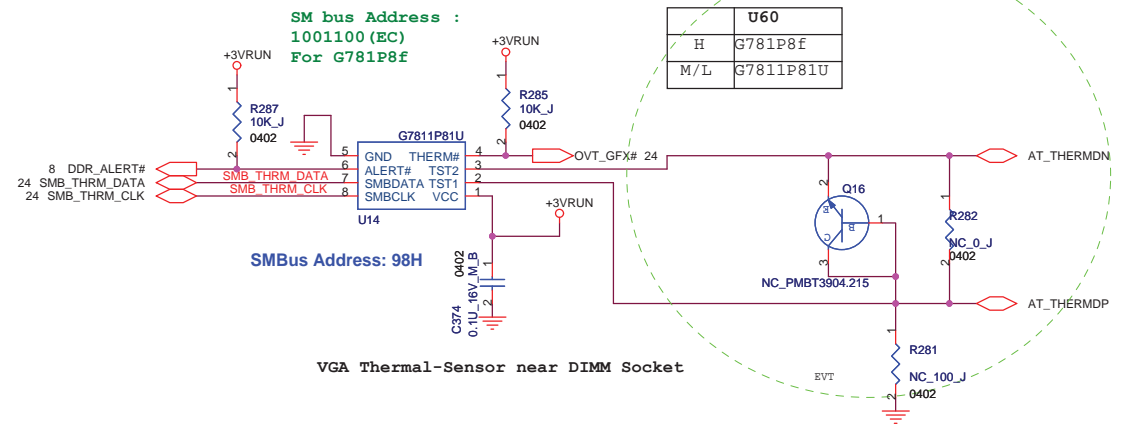
For Mor request, add the speaker cable short protection circuit

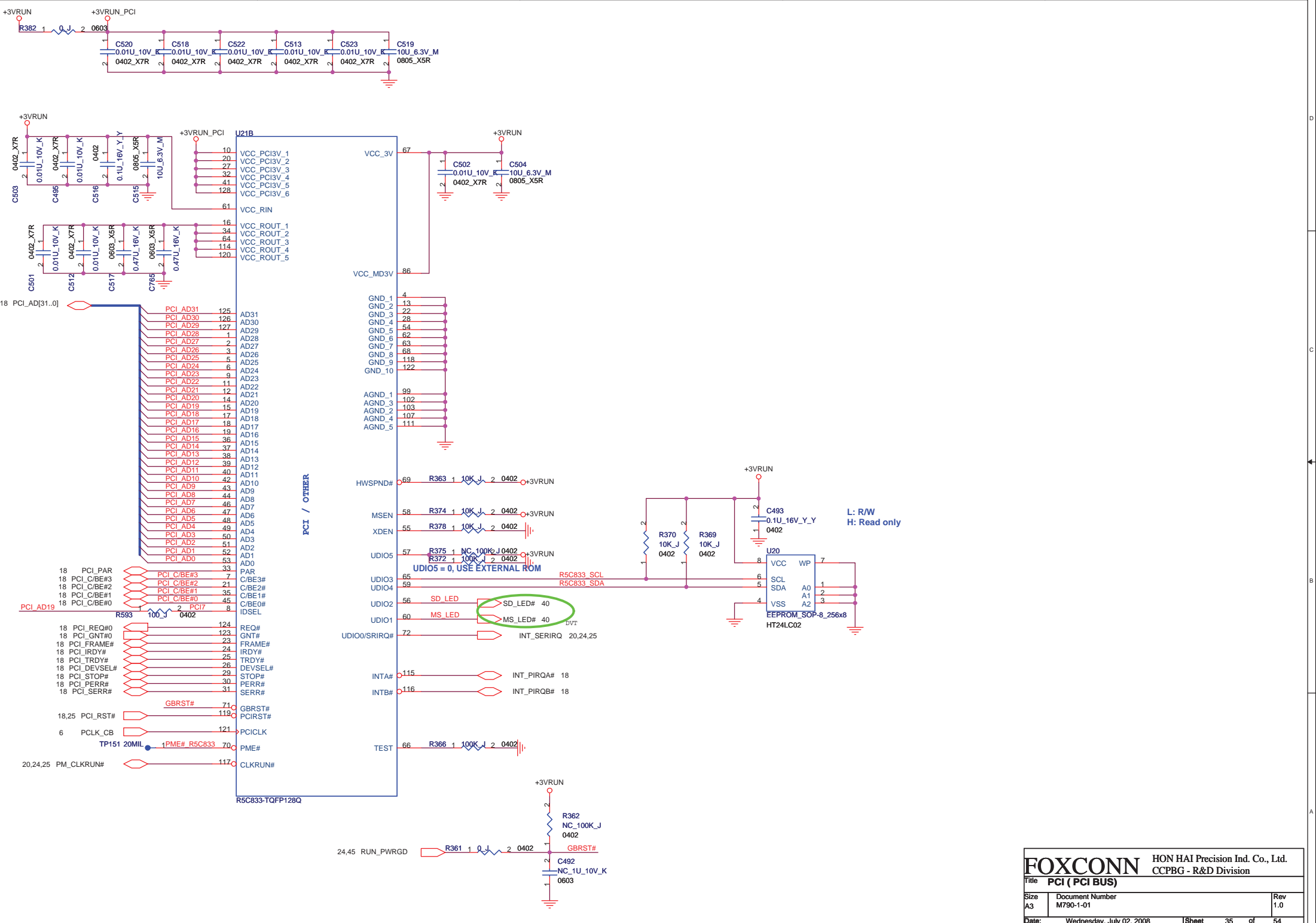






CPU Thermal-Sensor

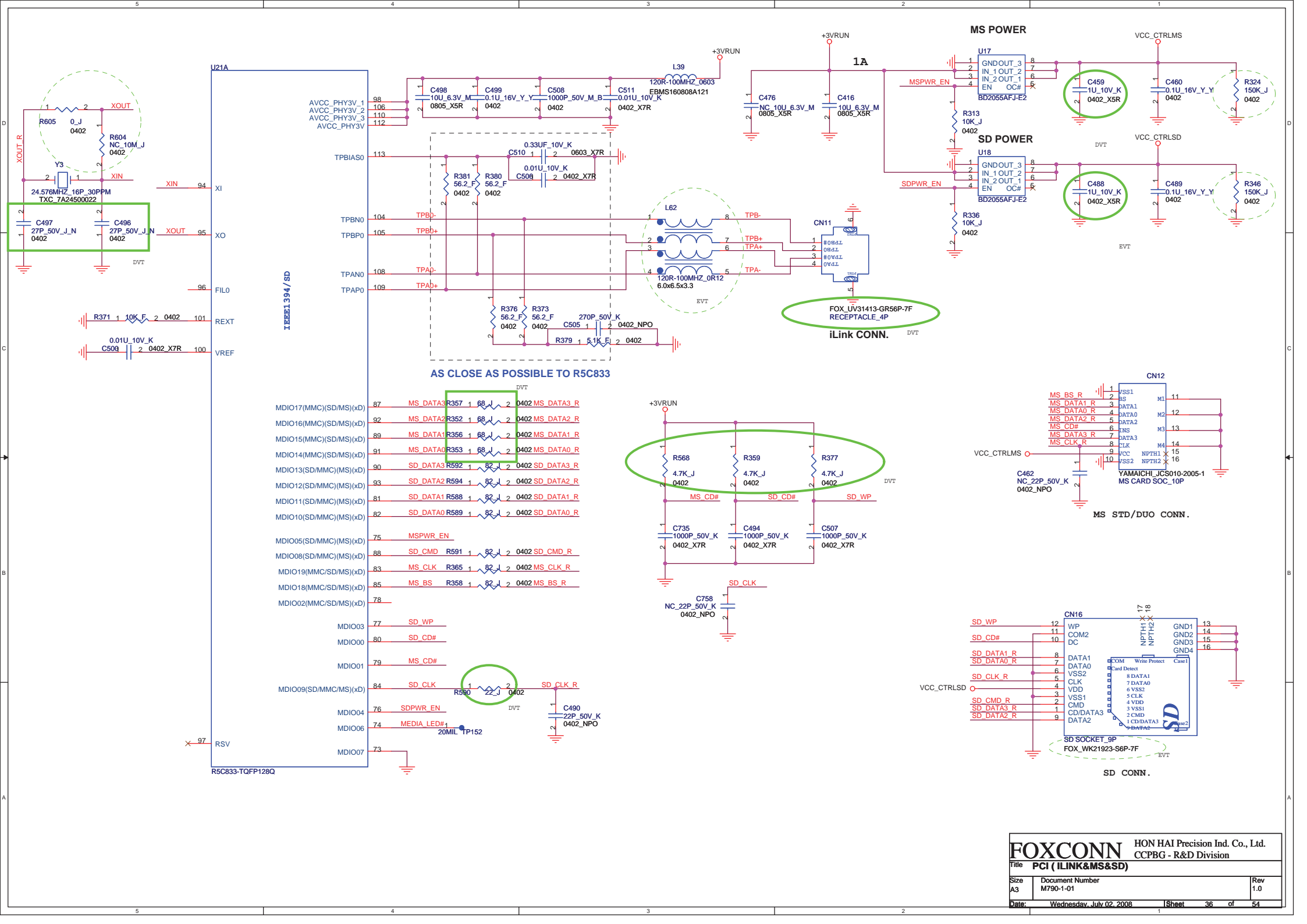




PCI / OTHER

L: R/W  
H: Read only

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Title</b> PCI ( PCI BUS )			
Size	Document Number	Rev	
A3	M790-1-01	1.0	
Date:	Wednesday, July 02, 2008	Sheet	35 of 54



**MS POWER**

**SD POWER**

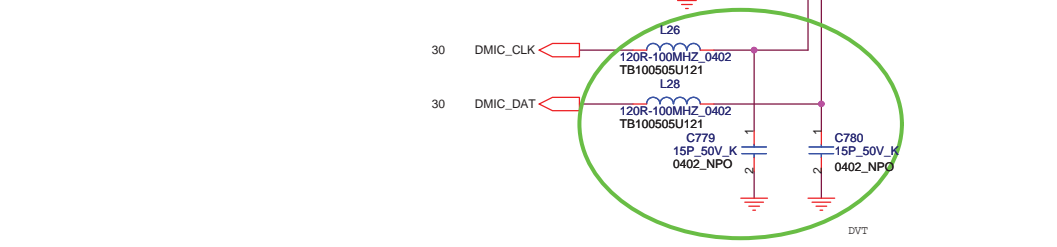
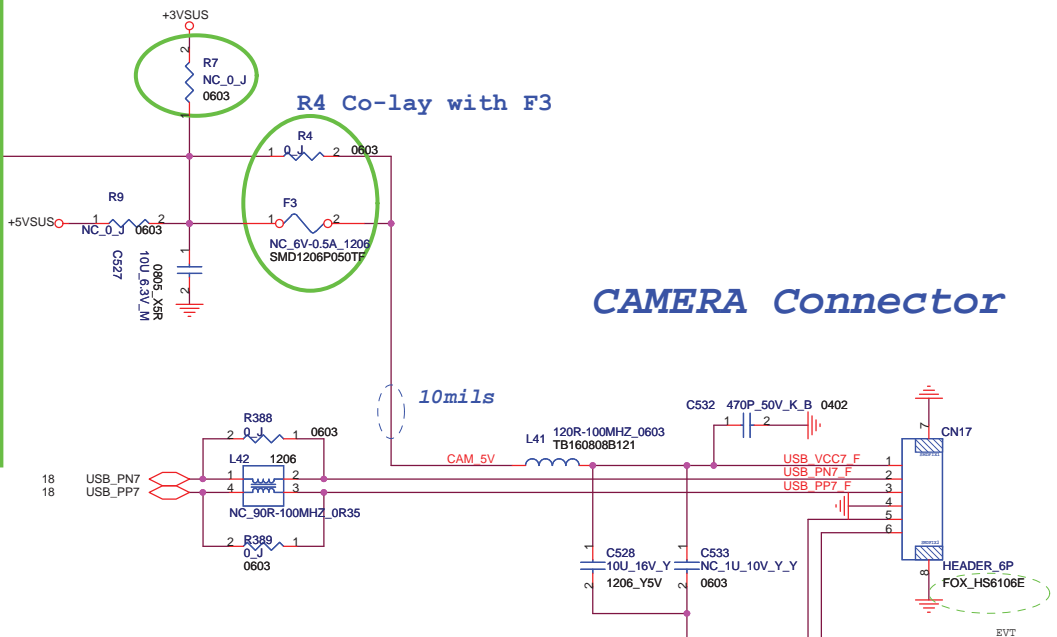
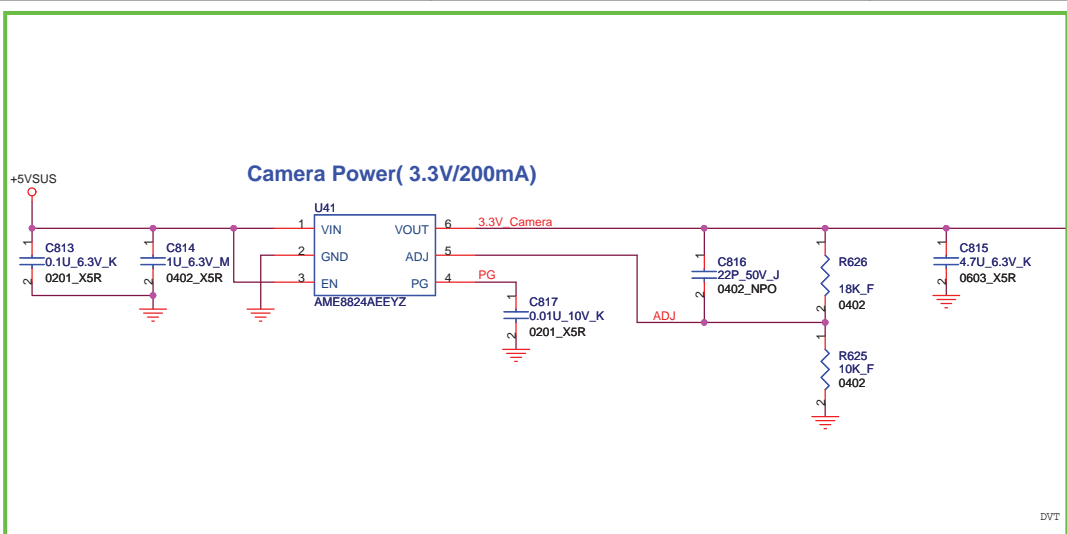
**AS CLOSE AS POSSIBLE TO R5C833**

**MS STD/DUO CONN.**

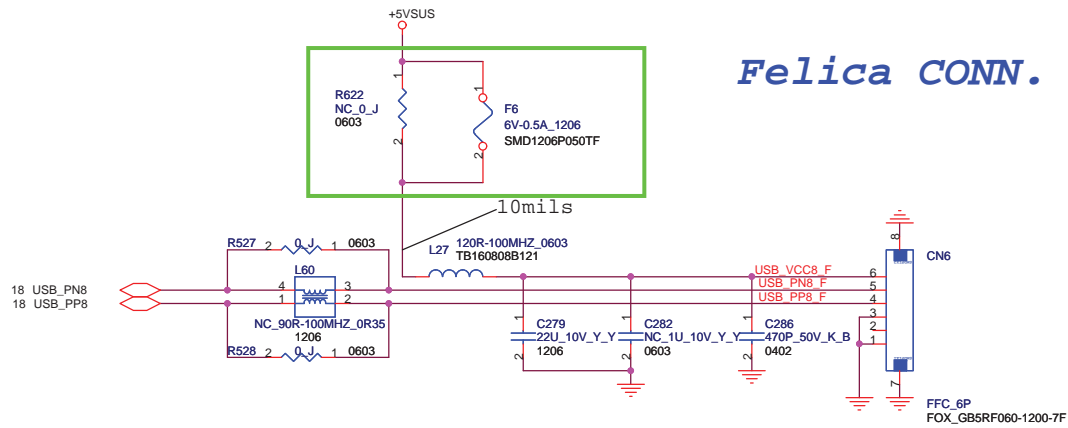
**SD CONN.**

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

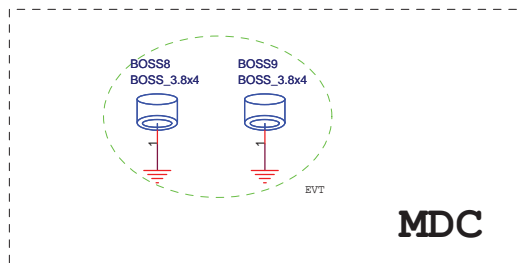
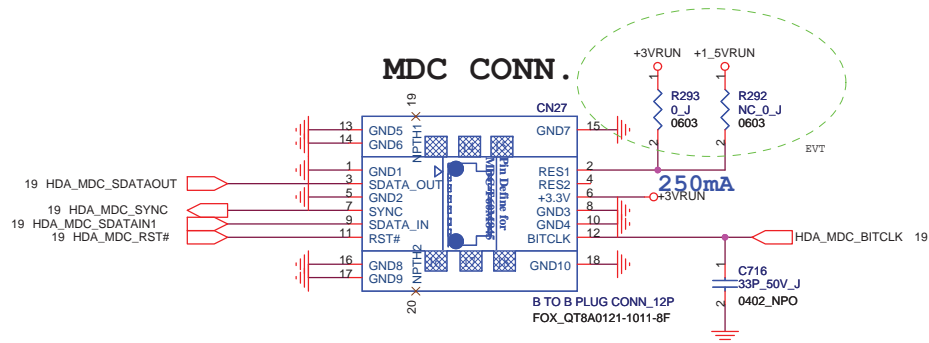
Title <b>PCI ( iLink&amp;MS&amp;SD )</b>		
Size A3	Document Number M790-1-01	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 36	of 54

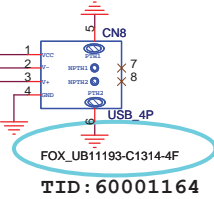
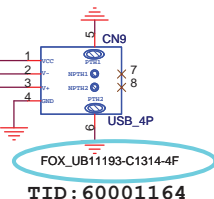
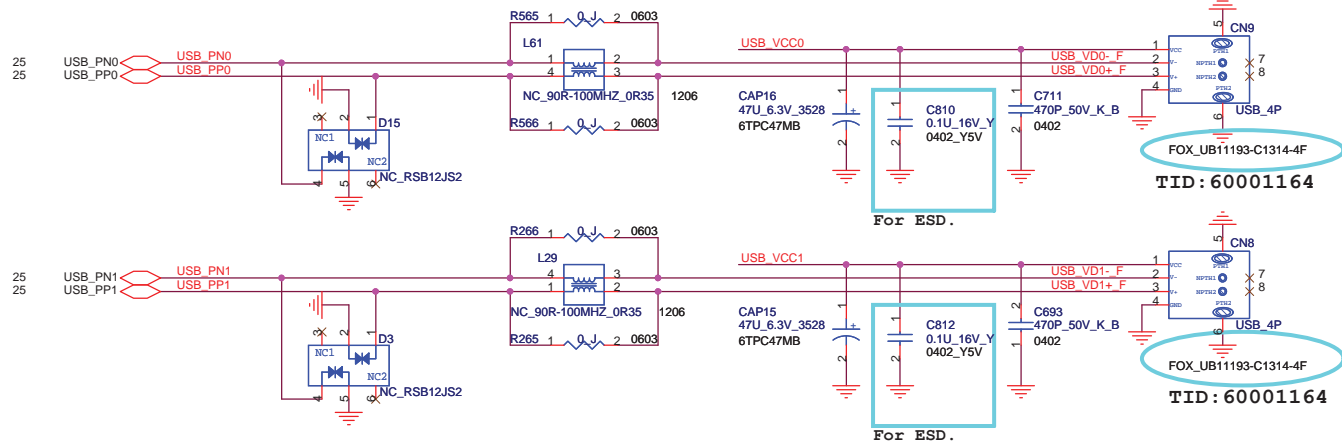
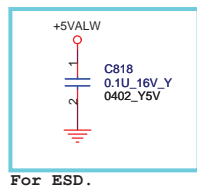
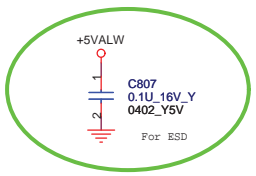
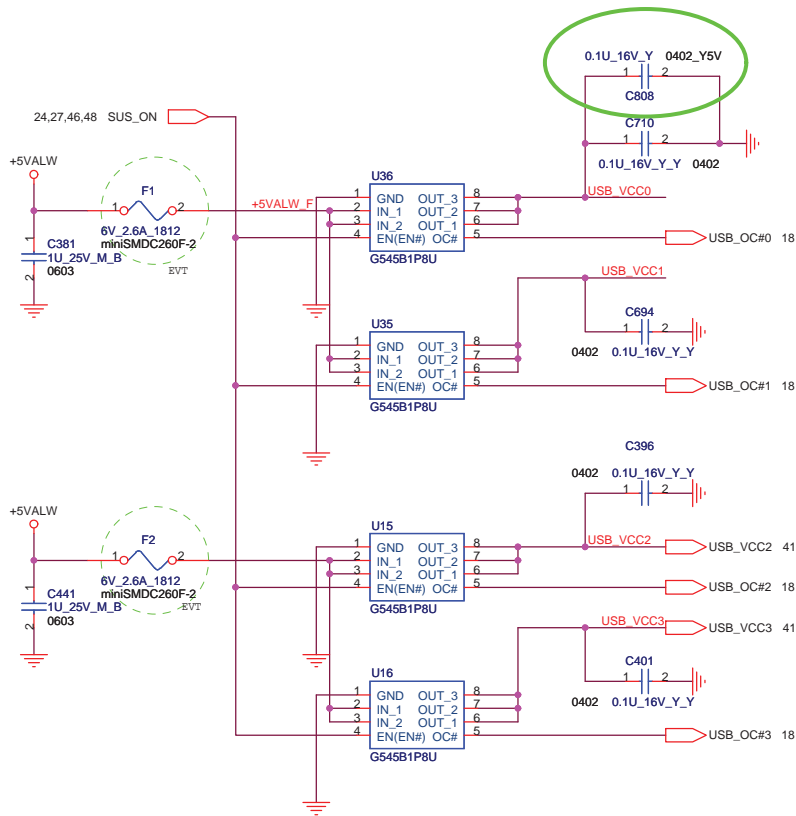


# Felica CONN.

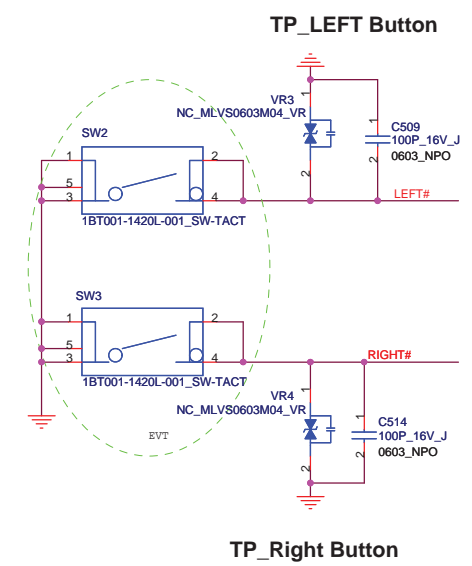
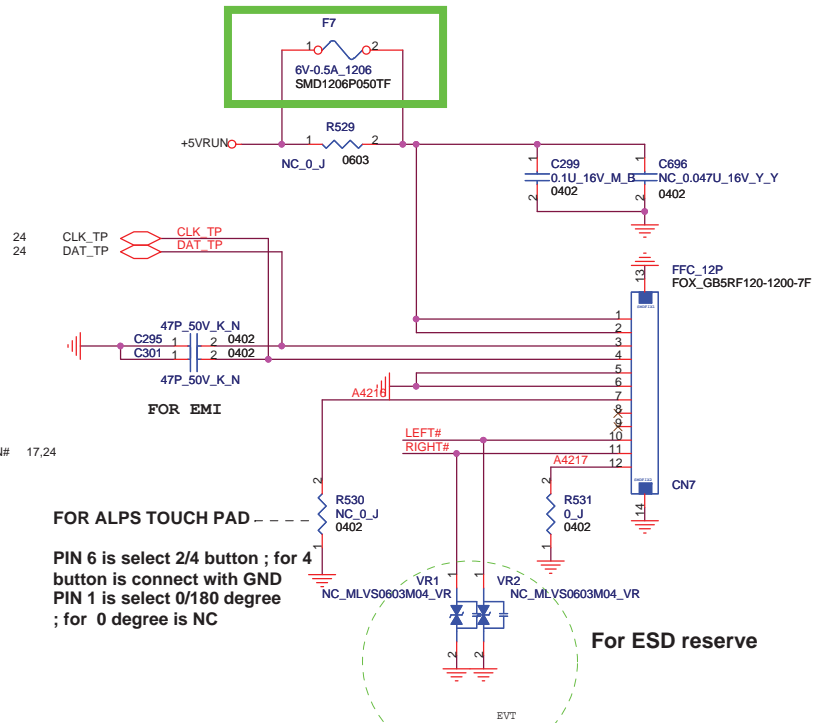
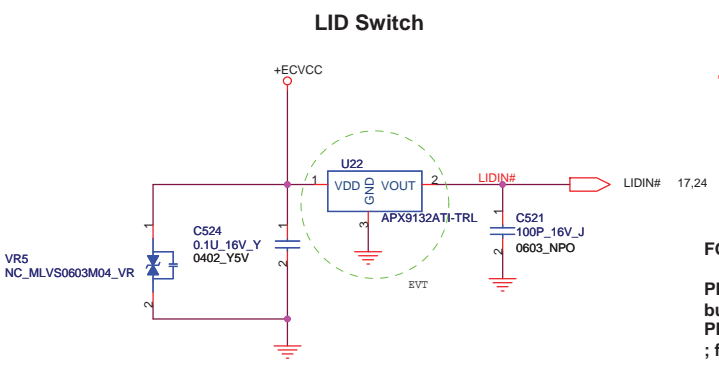
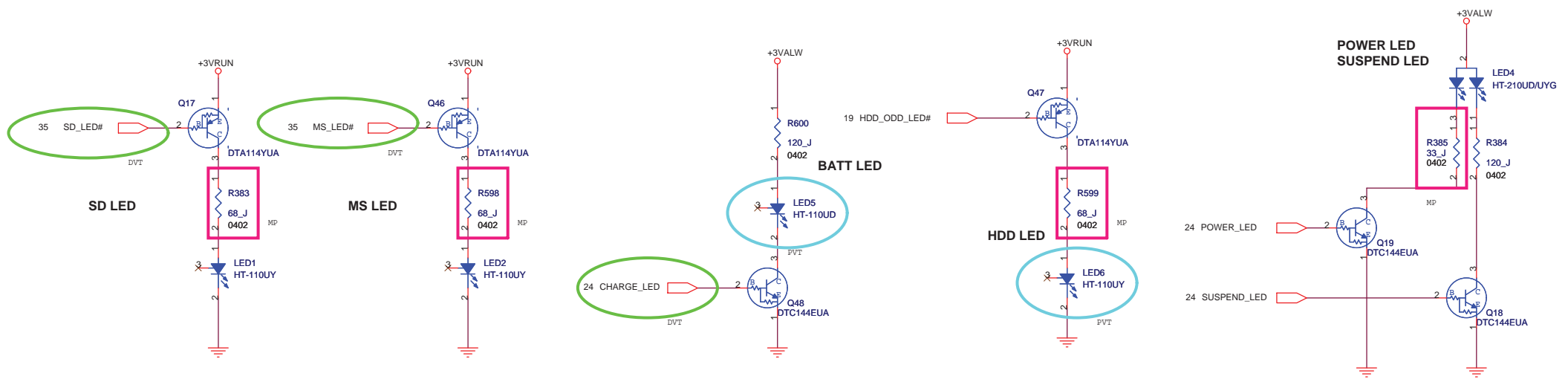


# MDC CONN.

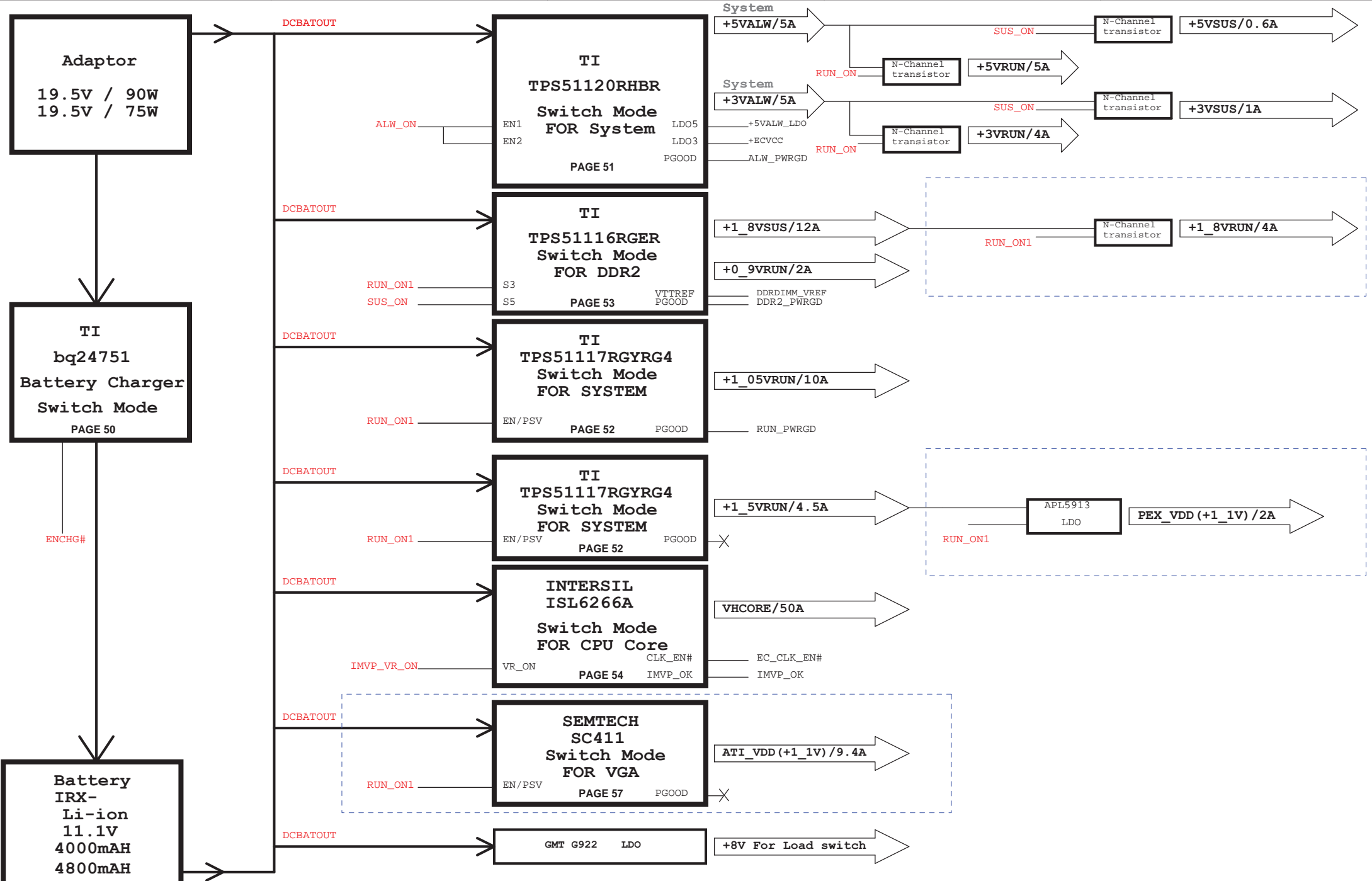




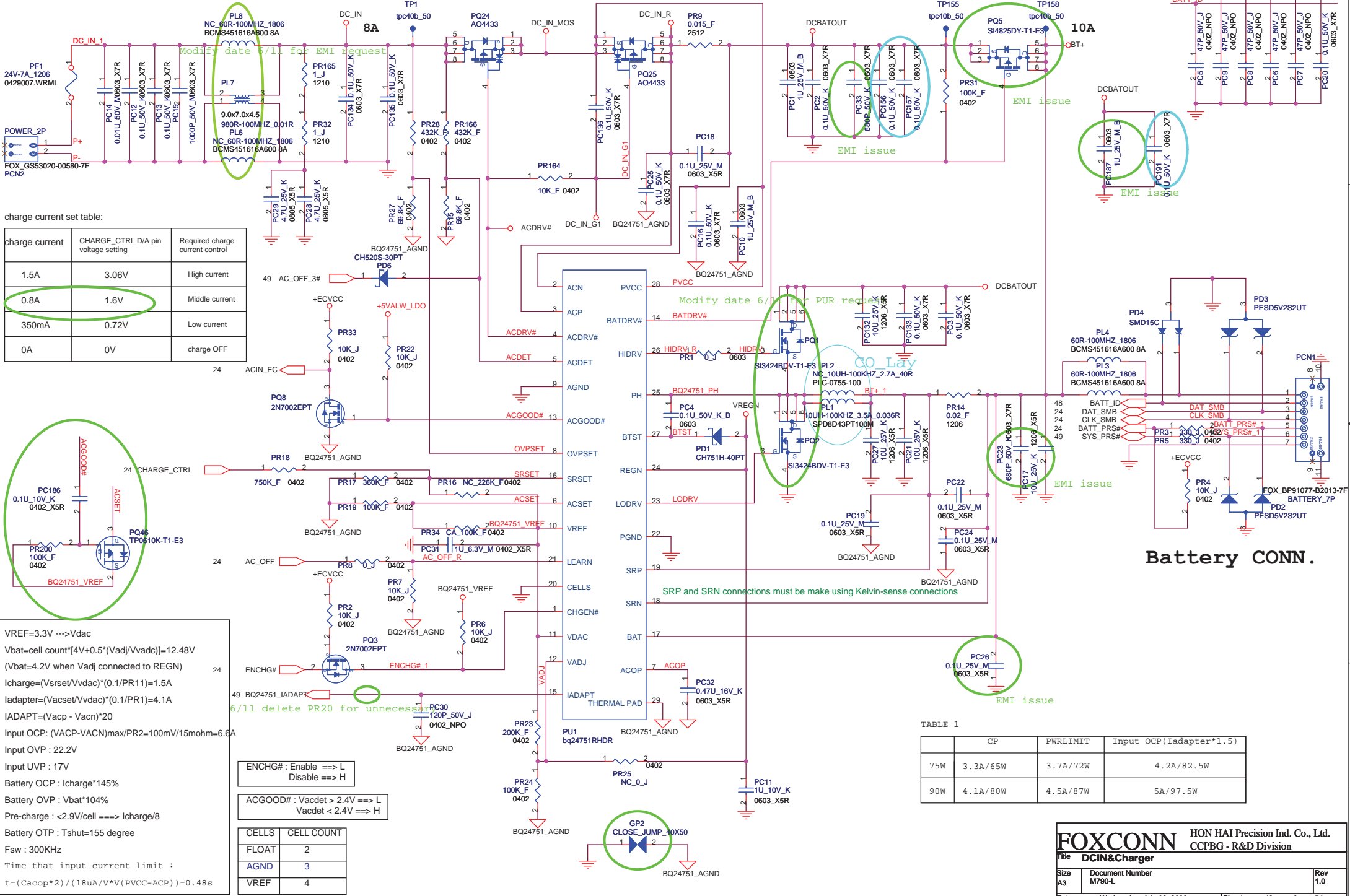






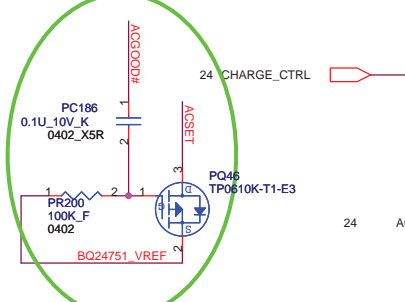


ACP and ACN connections must be make using Kelvin-sense connections



charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF



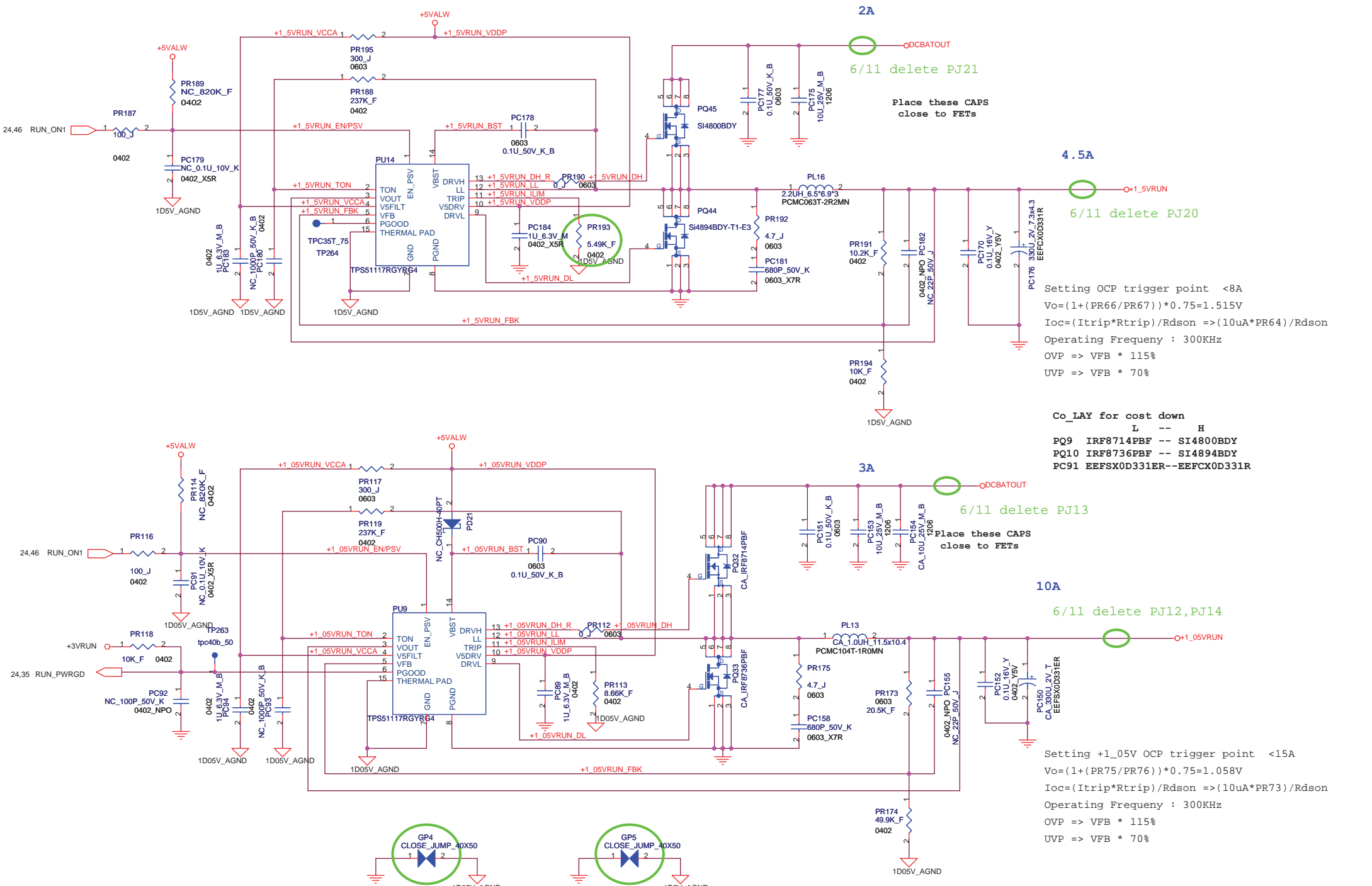
VREF=3.3V --->Vdac  
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})] = 12.48V$   
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to } REGN)$   
 $I_{charge} = (V_{srset} / V_{vdc}) * (0.1 / PR11) = 1.5A$   
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR1) = 4.1A$   
 $IADAPT = (V_{acp} - V_{vacn}) * 20$   
 Input OCP:  $(V_{acp} - V_{vacn})_{max} / PR2 = 100mV / 15mohm = 6.6A$   
 Input OVP: 22.2V  
 Input UVP: 17V  
 Battery OCP:  $I_{charge} * 145\%$   
 Battery OVP:  $V_{bat} * 104\%$   
 Pre-charge:  $< 2.9V / \text{cell} \implies I_{charge} / 8$   
 Battery OTP:  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$   
 Time that input current limit :  
 $t = (C_{acop} * 2) / (18uA / V * (PVCC - ACP)) = 0.48s$

ENCHG# : Enable ==> L	
Disable ==> H	
ACGOOD# : Vacdet > 2.4V ==> L	
Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

TABLE 1

	CP	PWRLIMIT	Input OCP(Iadapter*1.5)
75W	3.3A/65W	3.7A/72W	4.2A/82.5W
90W	4.1A/80W	4.5A/87W	5A/97.5W





2A

6/11 delete PJ21

Place these CAPS close to FETs

4.5A

6/11 delete PJ20

Setting OCP trigger point <8A  
 $V_o = (1 + (PR66/PR67)) * 0.75 = 1.515V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} => (10uA * PR64) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 115%  
 UVP => VFB \* 70%

Co\_LAY for cost down  
 L -- H  
 PQ9 IRF8714PBF -- SI4800BDY  
 PQ10 IRF8736PBF -- SI4894BDY  
 PC91 EEFSX0D331ER--EEFCX0D331R

3A

6/11 delete PJ13

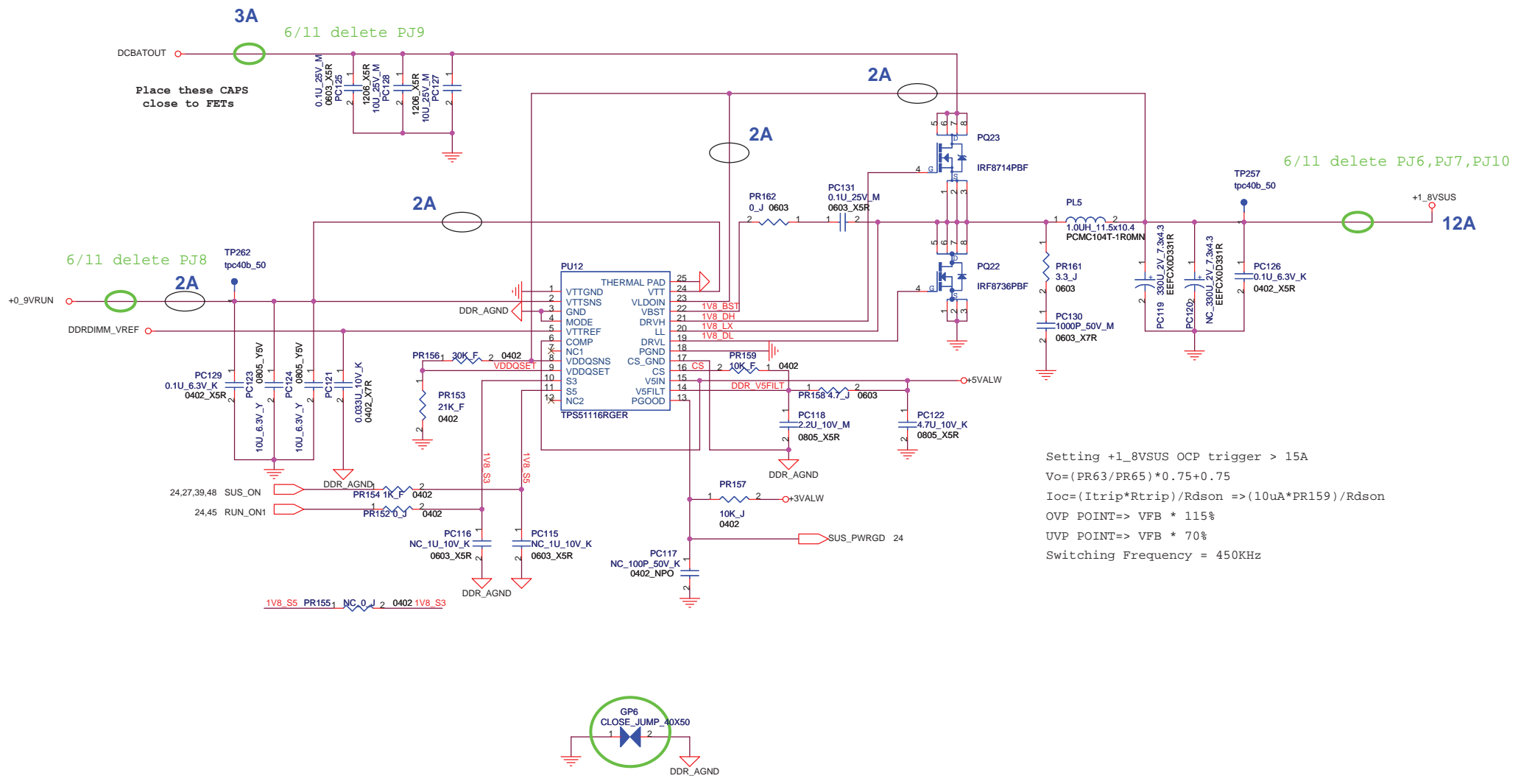
Place these CAPS close to FETs

10A

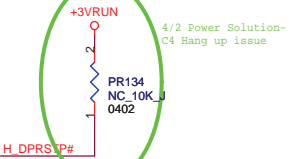
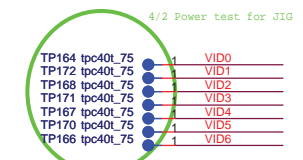
6/11 delete PJ12,PJ14

Setting +1.05V OCP trigger point <15A  
 $V_o = (1 + (PR75/PR76)) * 0.75 = 1.058V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} => (10uA * PR73) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 115%  
 UVP => VFB \* 70%





Setting +1.8VSUS OCP trigger > 15A  
 $V_o = (I_{trip} \cdot R_{trip}) / R_{dson} \Rightarrow (10\mu A \cdot PR159) / R_{dson}$   
 OVP POINT => VFB \* 115%  
 UVP POINT => VFB \* 70%  
 Switching Frequency = 450KHz



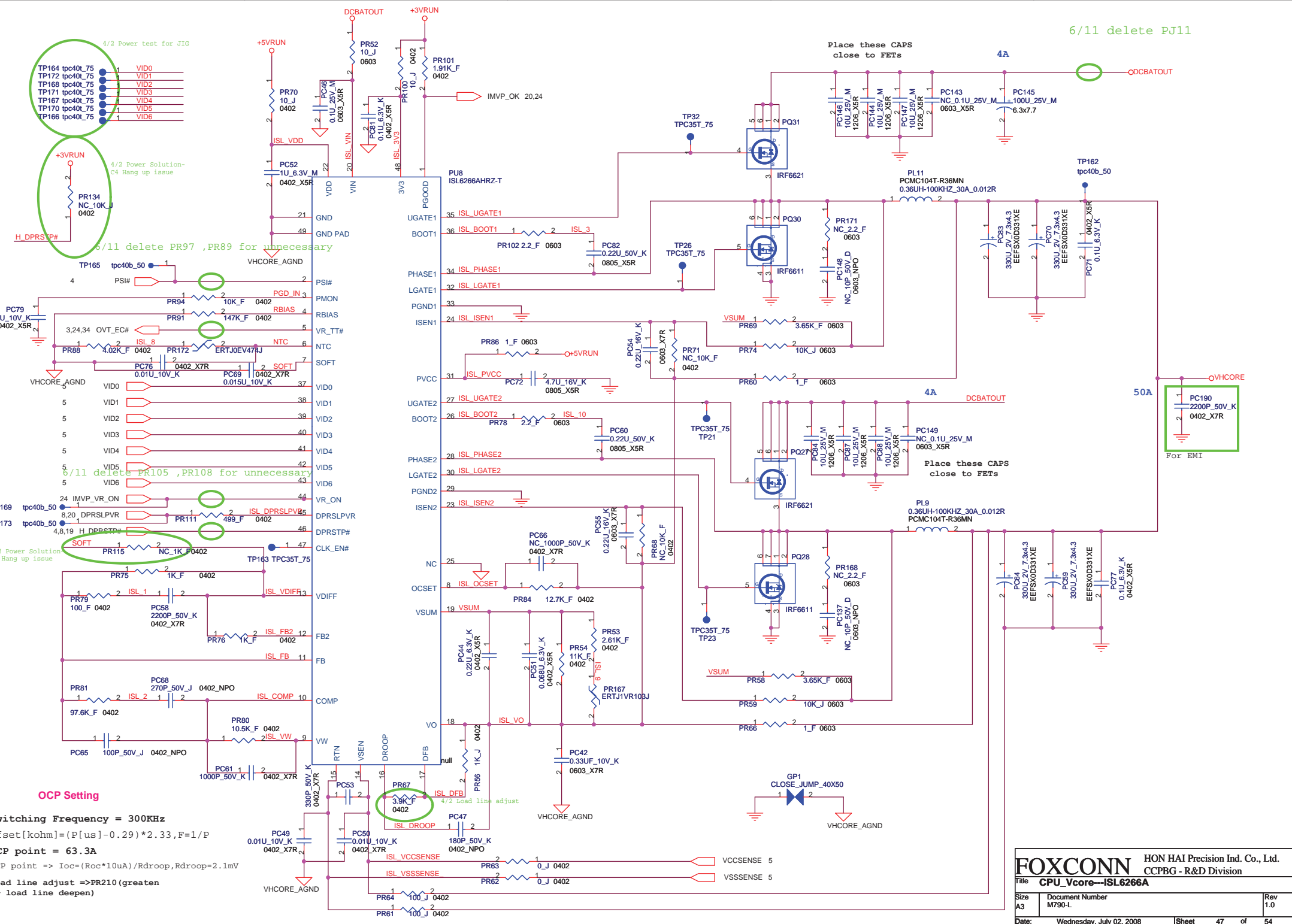
6/11 delete PR97 ,PR89 for unnecessary

6/11 delete PR105 ,PR108 for unnecessary

4/2 Power Solution-C4 Hang up issue

**OCP Setting**

Switching Frequency = 300KHz  
 $Rfset[kohm] = (P[us] - 0.29) * 2.33, F=1/P$   
 OCP point = 63.3A  
 OCP point =>  $Ioc = (Roc * 10uA) / Rdroop, Rdroop = 2.1mV$   
 Load line adjust => PR210 (greaten => load line deepen)



6/11 delete PJ11

Place these CAPS close to FETs

4A

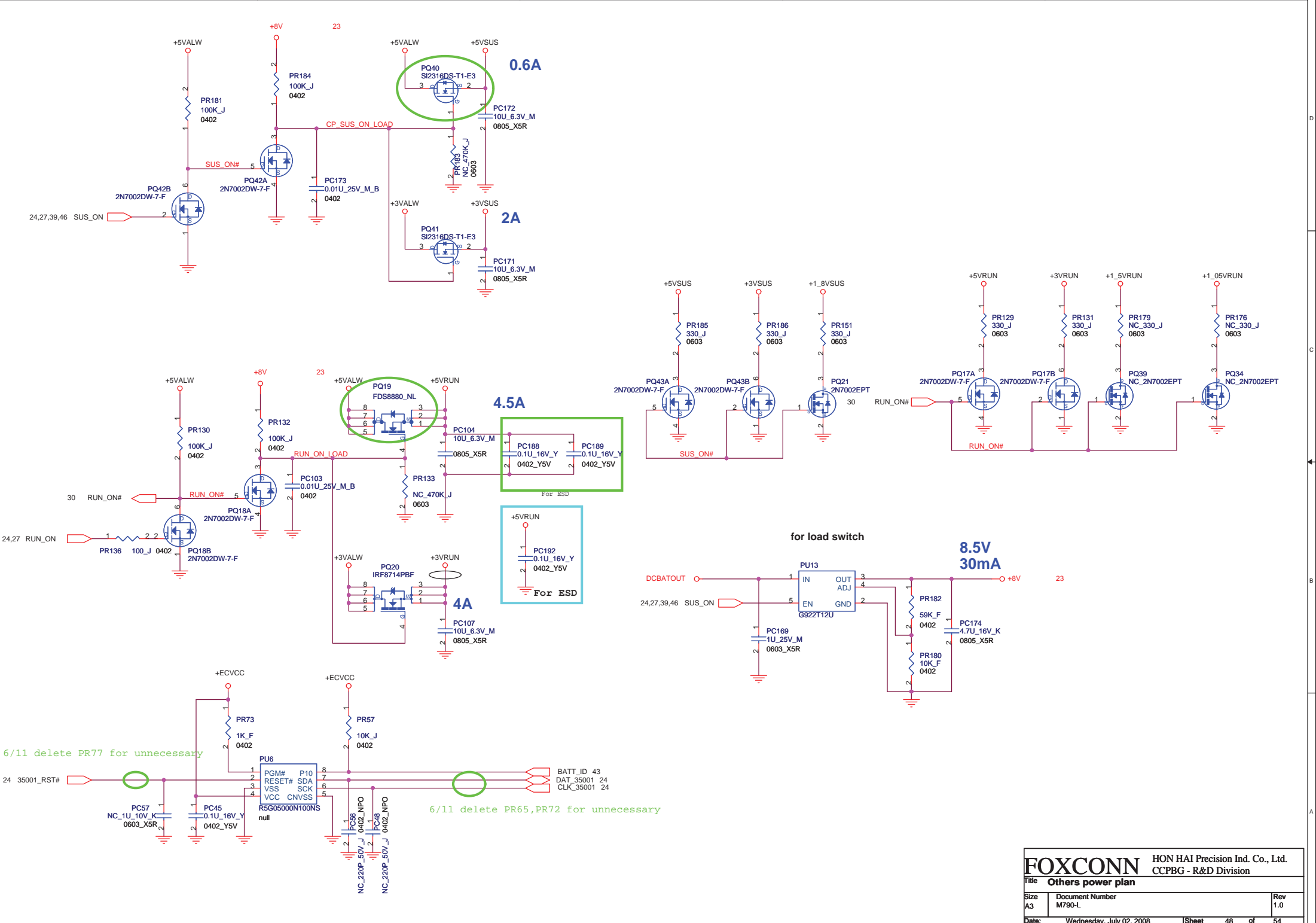
Place these CAPS close to FETs

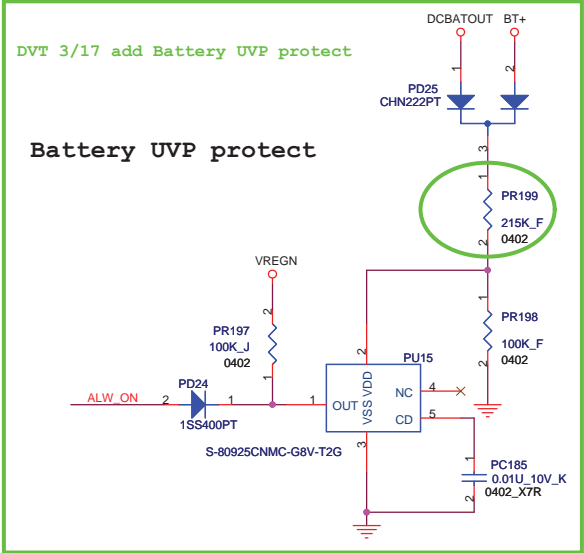
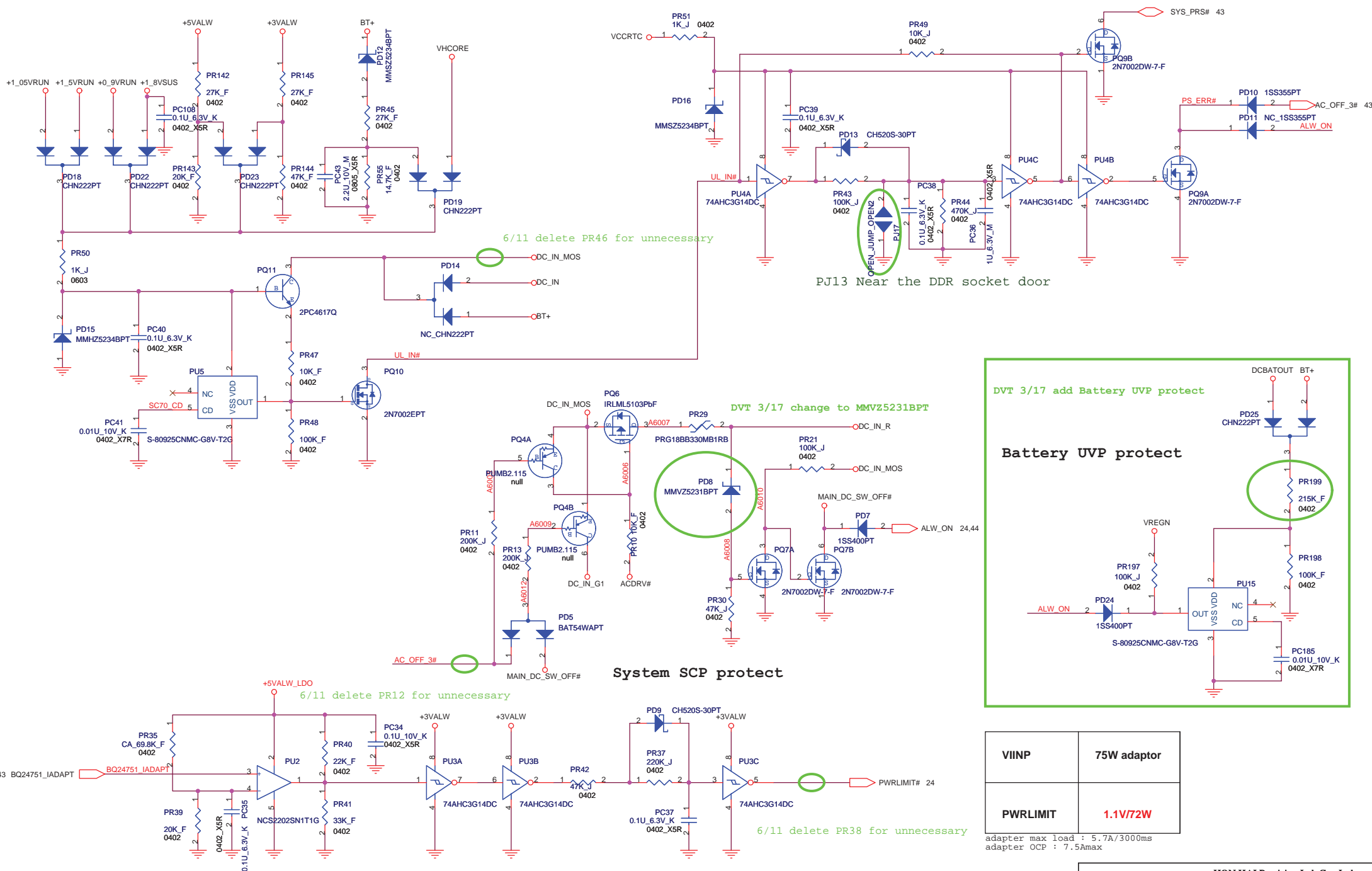
4A

50A

For EMI

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>CPU_Vcore-ISL6266A</b>		
Size A3	Document Number M790-L	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 47	of 54



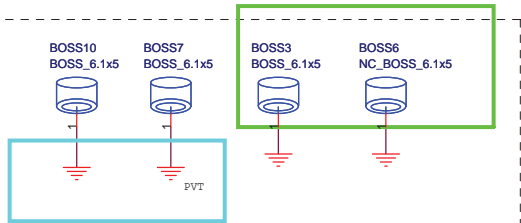


**System SCP protect**

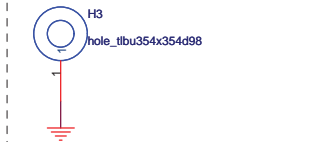
VIINP	75W adaptor
PWRLIMIT	1.1V/72W

adaptor max load : 5.7A/3000ms  
adaptor OCP : 7.5Amax

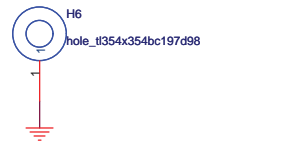
**PWRLIMIT Protect**



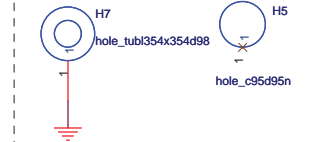
**Thermal Module**



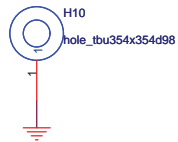
**Near CRT**



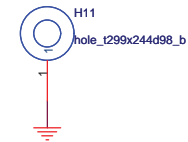
**Near AUDIO**



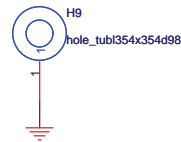
**Near USB**



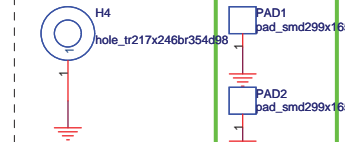
**Near Express card**



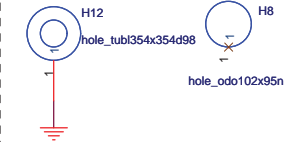
**Near SD card**



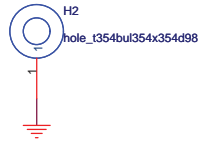
**Near MS card**



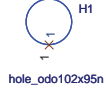
**Near ODD**



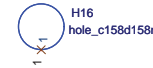
**Near DC-IN**



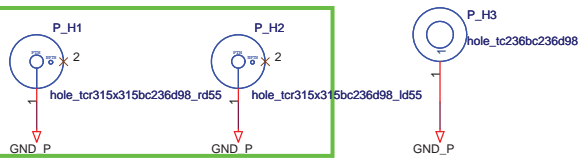
**Near Robson**



**Near HDD**

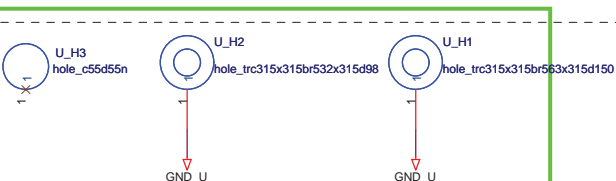
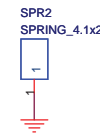
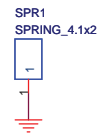


**CPU**



**Power board**

**Finger**



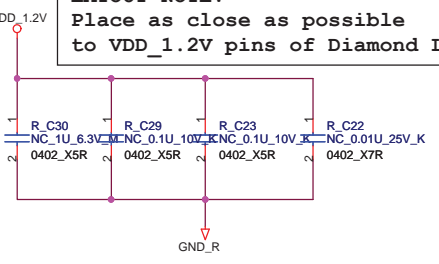
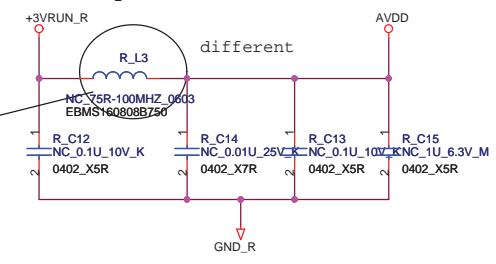
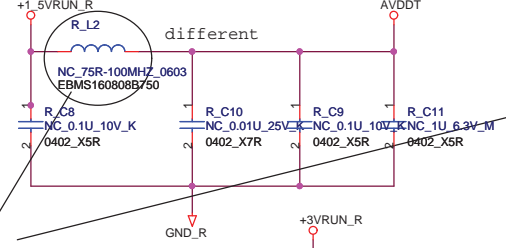
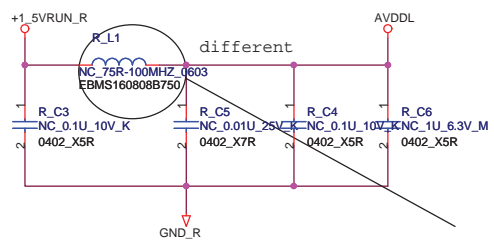
**USB board**

**LAYOUT NOTE:**  
Place as close as possible  
to AVDDL pins of Diamond Lake

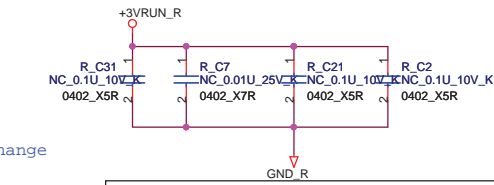
**LAYOUT NOTE:**  
Place as close as possible  
to AVDDT pins of Diamond Lake

**LAYOUT NOTE:**  
Place as close as possible  
to AVDD pins of Diamond Lake

**LAYOUT NOTE:**  
Place as close as possible  
to VDD\_1.2V pins of Diamond Lake



Intel sch use 70ohm /100MHZ



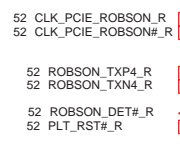
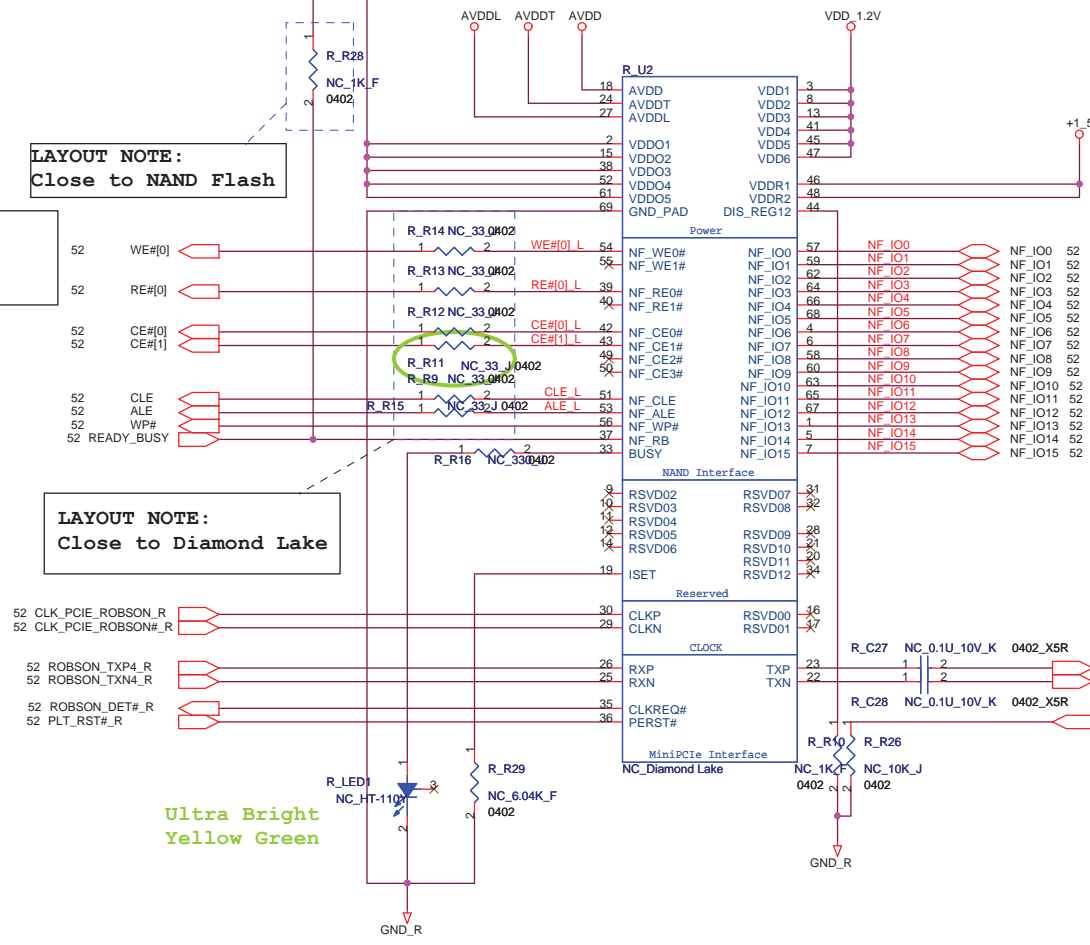
change

**LAYOUT NOTE:**  
Place as close as possible  
to +3VRUN pins of Diamond Lake

**LAYOUT NOTE:**  
Close to NAND Flash

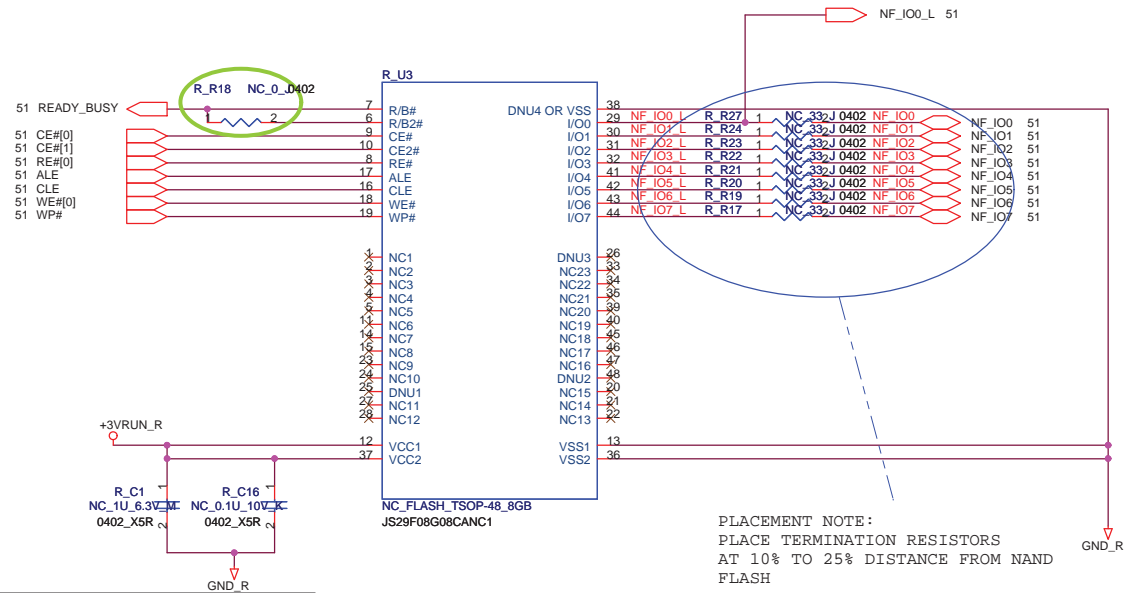
**LAYOUT NOTE:**  
Close to Diamond Lake

**LAYOUT NOTE:**  
Place as close as possible  
to VDDR1 and VDDR2 pins  
of Diamond Lake

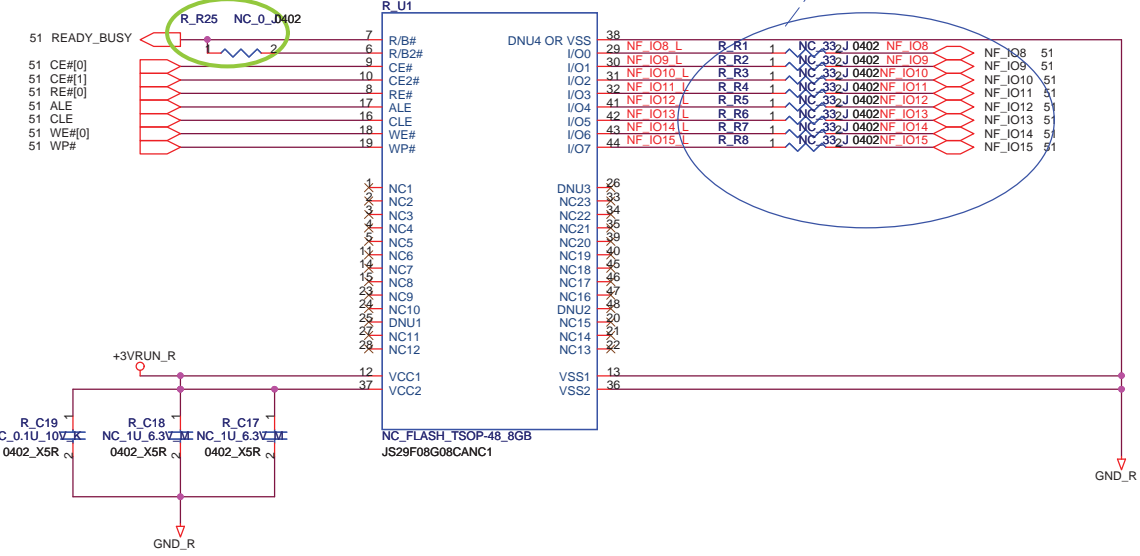


Ultra Bright  
Yellow Green

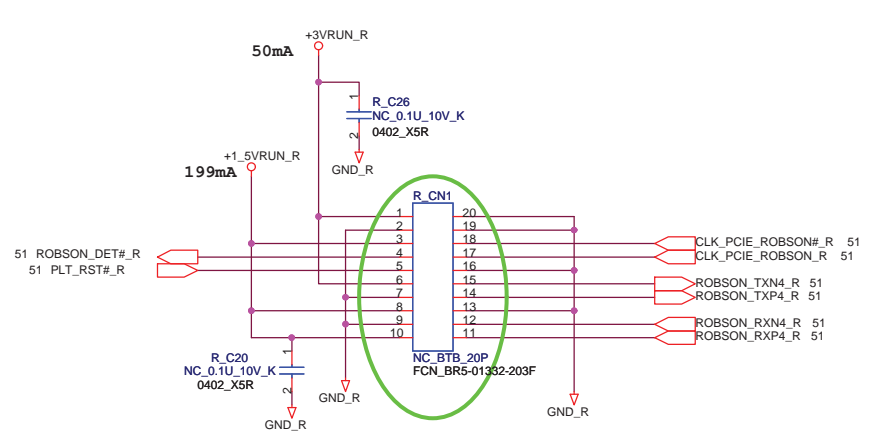




**LAYOUT NOTE:**  
Place as close as possible  
to +3VRUN pins of R\_U3

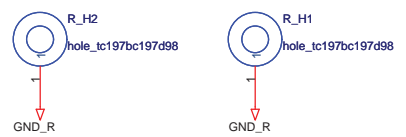


**LAYOUT NOTE:**  
Place as close as possible  
to +3VRUN pins of R\_U1



will change the connector type to bluetooth connector

**ROBSON Board CONN**



## M790 EVT

(2008/01/23)

Update 8Layer H/L versio to 6Layer L version.

(2008/01/24)

Page 6. Change Clock to B version.

Page 25. Change SPI rom to new version.

Page 36. Change L62,delete L63 same as M760.

(2008/01/28)

Page 14/15. Add C767~C778 for EMI reserve.

Page 19. Add R610 damping resistor for adjustment for MOR request.

Page 20. Change GPIO18,20 to GPIO36,37 and delete R269,R270.

Page 23. Change D13 to mount.

Page 24. Change RP39,RP41 to +3VALW.Add D17,D18 for EC leakage current issue.

Page 29. Add R602,R603 damping resistor for adjustment for MOR request.

Page 32. Add R601 for MOR request.

Page 36. Add R604,R605 damping resistor for adjustment for MOR request.

Page 37. Add R611,R612,C779,C780 for EMI reserve.

Page 48. Change PQ40 from SI2304BDS-T1-E3 to SI2316DS-T1-E3 and Change PQ19 from IRF8714PBF to FDS8880\_NL for MOR request.

(2008/01/29)

Page 50. Add H13~H16,P\_H3.

(2008/01/30)

Page 50. Update H4,U\_H1,U\_H2.

(2008/01/31)

Page 20. Not AMT support,so delete R556, R557 and C722.

Page 32. Change GP2,GP3 to R556,R557.

Page 33. Change R486 connect to D\_GND.

Page 50. Add Boss10.

(2008/02/01)

Page 49. Change PJ17 from PD13 pin1 to pin2.

(2008/02/02)

Page 17/24. Add FAN error detect function in panel switch pin4.

Page 32. Change C624 to 2.2uF for pop noise issue.

(2008/02/14)

Update some error discription for MOR request.

(2008/02/18)

Page 32. Mount Audio cable short components for EVT test.

(2008/02/20)

Page 32. Change U30 from TI(TPA6017) to GMT(G1431F2U) for pop noise issue.

(2008/02/21)

Page 17. Update Panel ID table.

Page 24. Update R447 CA to Mount,R437 Mount to CA.

Page 46. Add PJ10.

Page 14/15.Add J2/J3 for EMI request.

Page 6. Add reserverve C781,C782,C783 for EMI request.

Page 29. Add reserverve C784,C785 for EMI request.

(2008/02/22)

Page 14/15.Add J4/J5 for EMI request.

Page 6. Add reserverve C786,C787 for EMI request.

(2008/02/26)

Page 5. Change C76 from 6.3V to 10V for PUR request.

Page 11. Change C201,C225,C679,C681,C143,C168,C596,C601,C605 from 10V to 16V for PUR request.

Page 18/29. Change C32,C35,C449,C450,C725,C726,C727,C728,C729,C730 to 0.1uF,6.3V,10% for PUR request.

Page 31. Change R202 for PUR request.

Page 31. Change Q37,Q39,Q40,Q41 to PBSS2515E.115 for PUR request.

Page 32/33. Change Q6,Q25,Q34,Q38 to MMBT3906K for PUR request.

Page 33. Change Q33/Q44 to MMBT3904 for PUR request.

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(2008/02/28)

Page 33. Change Q33/Q44 to PMBT3904.215 for PUR request.

(2008/03/03)

Page 52. Change R\_U1,R\_U3 to 8Gbit size and change R\_R11,R\_R18,R\_R25 to mount.

(2008/03/05)

Page 24. Mirror CN3 for Int. keyboard issue.

(2008/03/06)

Page 38. Mirror CN6 for easy A'ssy.

Page 44. Change PR146 to 6.8K,PR147 to 5.49K for OCP current adjust.

Page 45. Change PR193 to 5.49K for OCP current adjust.

(2008/03/24)

For PUR request change C624 2.2uF(1.25mm) to (0.8mm),C510/PC42 0.33uF(X5R) to (X7R).

Page 38. SWAP L60 for CN6 mirror issue.

Page 24/40. Change CHARGE\_LED# low enable to H enable same as M750/M760.

(2008/03/28)

Page 24. Add C722(1000pF) for FAN speed stable.

(2008/04/02)

Page 28/51/52. Change Robson function to no mount.

(2008/04/07)

Page 23. Del PJ4 Change PJ3 type for JIG.

Page 43. Add for charger ocp improve.

Page 43~46,48. A\_GND and P\_GND change to GP2~6.

Page 47. Add PR134,PR115 for Power Solution- C4 Hang up issue.

Page 47. tpc40b\_50 Change to tpc40t\_75 power point part for JIG.

Page 49. Add Battery UVP protect for power issue.

(2008/04/08)

Page 29. Add C733,R269,R270/R616(no mount),Change R44 to 4.99Kohm and NC CTRL\_LD8 circuit for 88E8057.

Page 32. Change R98,R450,Q8,Q27 to NC and Add R614,R615 no mount for speaker cable short protection circuit.

Page 35/40. Change MS/SD LED to Low active.

(2008/04/11)

Page 31. Change C182,C194 to 0.1uF for MIC THD+N issue

Page 49.Change PR199 to 215Kohm for Battery UVP adjust.

(2008/04/14)

Page 31. Change C626,C662 to 4.7uF for MIC FSIV issue.

Page 29. Design for 88E8055.

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(2008/04/14)

Page 16. Change L14,L16,L17 to 120ohm/100Mhz bead for CRT EMI issue.  
Page 32. Add C797~C800(220pF)for Speaker EMI issue.  
Page 37. Change R611,R612 to L26,L28 120ohm/100Mhz bead and C779,C780 to 15pF for Camera EMI issue.  
Page 41. Add C790~C79(2200pF)for power board EMI issue.

(2008/04/15)

Page 50. Change Boss7 pin2 connect to RC for EMI reserve and Add Finger SPR1,SPR2 for EMI issue.  
Page 32. Add C802~C805(220pF)for Speaker EMI issue.

(2008/04/18)

Page 23. Update ODD connector for MOR request.  
Page 26. Add R611,R612 and Change U24,C534 to no mount for MOR request.

(2008/04/21)

Page 19. Change C388,C389 to 15pF for Y6 test fail.  
Page 24. Change C245,C246 to 18pF for Y2 test fail.  
Page 31. Change C629,C652 to 220pF same as M760.  
Page 36. Change C496,C497 to 27pF for Y3 test fail.Change R352,R353,R356,R357 to 100ohm,R590 to 33ohm for MS/SD fail items.

(2008/04/23)

Page 16. Update CN2 VGA connector type.

(2008/04/24)

Page 41. Change U\_R1~R4 to NC,U\_L1,L2 to mount.  
Page 43. Add PC187,and Change PC23,PC33 to 680P for EMI request.

(2008/04/25)

Page 16. Update D11 to SL22 for CRT ripple noise.

(2008/04/28)

Add C806~C808,PC188,PC189(0.1uF) for ESD solution.  
Page 27. Change CN14 to FOX\_1CX42201-SM for ME request.  
Page 36. Change CN11 to Gray color,C459,C488 to X5R and R568,R359,R377 to mount for MOR request.

(2008/04/29)

Page 21. Change C717,C723 to X5R.

(2008/04/30)

Page 26. Change C538 to mount for ripple noise.  
Page 37. Change R7/F3 to mount,R9/R4 to NC for 3.3V Camera.  
Page 50. Change BOSS3,6,7,10 to 1M-1F50M20-5000 and NC BOSS6.

(2008/05/02)

For MOR request,add F5,F6,F7.  
Page 6. Add R618~R621 475ohm for CR# issue.  
Page 21. Change C721 to 1uF for Intel design change.

(2008/05/06)

Page 16. Change R418,R424 to 30 ohm for Graphic test fail item.  
Page 50. Update PAD1,2 size.

(2008/05/07)

Page 36. Change R590 to 22ohm for SD card clock issue.  
Page 37. Add resver regulator IC for Camera power.  
Page 41. Add C811 for ESD issue.  
Page 50. Add resver C812,R623 for EMI issue.  
Page 43. Change PQ5 from AO4433 to SI4825DY-T1-E3 for EMI issue.  
Page 47. Add PC190 for EMI issue.

(2008/05/08)

Page 6. Add TP153,TP154 for FSB easy measure.

**BOM Change**

Change CN25 to LN27131-A403-4F.  
Change R352,R353,R356,R357 to 68ohm.  
Change R601 to mount,F5 to NC.  
Change U41,C813~C817,R626,R625,R4 to mount,R7,F3 to NC.

(2008/05/14)

Page 16. Change R418,R424 to 22ohm for CRT issue.  
Page 43. Change PL6,PL8 to no mount,Change PL7 to 1000R-100MHZ\_0.015R for EMI issue.  
Page 47. Change PR115 to no mount.

**M790 PVT**

(2008/06/03)

Page 25. Add lable1 for BIOS.  
Page 39. Change CN8,CN9 to grey color.

(2008/06/11)

Page 23. Delete PJ3 for unnecessary  
Page 43. Change PL7 to 1L-FPWC090-7H01 for EMI request.  
Page 43. Change PQ1,PQ2 from17-S134240-VT00 to 17-S13424B-DV00 for PUR request.  
Page 43. Delete PR20 for unnecessary  
Page 44. Delete PJ18,PJ19 for unnecessary  
Page 45. Delete PJ12,PJ13,PJ14,PJ20 ,PJ21for unnecessary  
Page 46. Delete PJ6,PJ7,PJ8,PJ9 ,PJ10 for unnecessary  
Page 47. Delete PJ11,PR97,PR89,PR105,PR108 for unnecessary  
Page 48. Delete PR77,PR72,PR65 for unnecessary  
Page 49. Delete PR12,PR38,PR46 for unnecessary

(2008/06/16)

Page 32. Change F5 to 1.5A and to mount for MOR request.

(2008/06/23)

Page 41. Change C790~C796,C811 to 220pF for EMI and Hotkey issue.  
Page 41. Add Fuse(F8) in power source on power board for short test.  
Page 43. Mount PC156,PC157 and Add PC191 for EMI issue.  
Page 50. Change BOSS7,10 connect to GND.

(2008/06/24)

Page 40. Change LED1,LED2,LED6 to HT-110UY,LED5 to HT-110UD.R383,R598 to 120ohm for MOR request.  
Page 41. Change P\_LED1~P\_LED3 to HT-150YG.P\_R1~P\_R3 to 100 ohm for MOR request.

(2008/07/02)

Page 31. Change C184,C192 to 4.7uf 0603 for MIC THD+N issue this change same as M761.  
Add ESD solution C810,C812,C818,PC192(0.1uF).

**M790 MP**

(2008/07/24)

Page 25. Change CN26,U11,C308,R221 to no mount,R233 to mount.  
Page 40. Change R385 to 33ohm,R383,R598,R599 to 68ohm for LED bright issue.

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