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Project Code & Schematics Subject: MS72 Main Board

PCB P/N: (FUBAI) 1P-006B100-60SA  
 (NAN YA) 1P-006B200-60SA  
 (HANSTAR) 1P-006B500-60SA

F. Leader	Check by	Design by
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<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd CCPBG - R&D Division		
File Index Page		
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11	CALIST (VCC CORE) 6/7	0.1	12/04	46	SYS Power (+3_3V/+5V)	0.1	12/04
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13	DDR2(SO-DIMM_0) 1/3	0.1	12/04	48	DDR2 Power(+1_8V/+0_9V)	0.1	12/04
14	DDR2(SO-DIMM_1) 2/3	0.1	12/04	49	CPU_Vcore ---MAX8771	0.1	12/04
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34	AUDIO( AMP & HP & SPK)	0.1	12/04				
35	AUDIO( EXTMIC)	0.1	12/04				

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Project Code & Schematics Subject: MS72 Main Board      PCB P/N: (FUBAI) 1P-006B100-60SA  
 (NAN YA) 1P-006B200-60SA  
 (HANSTAR) 1P-006B500-60SA

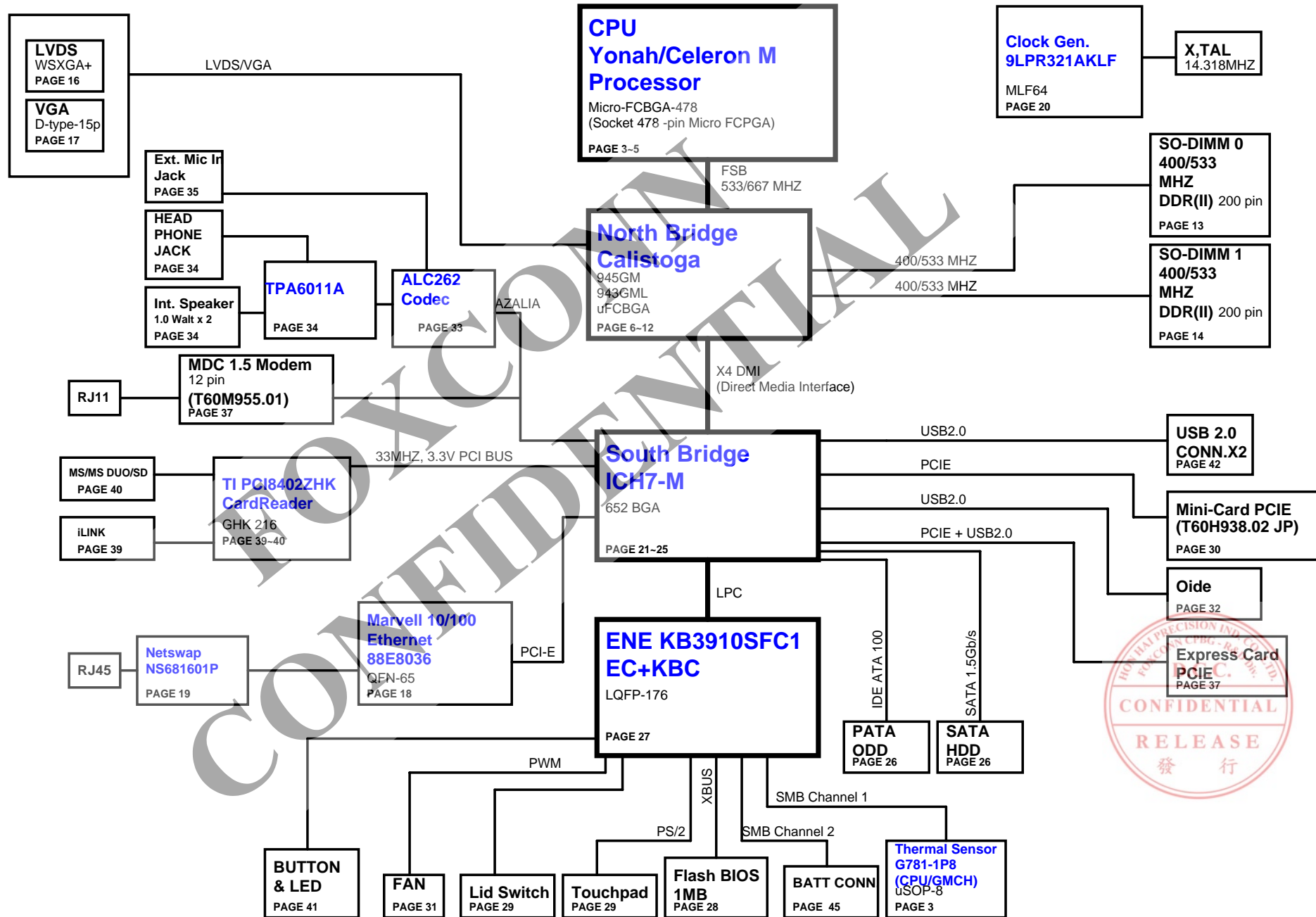
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 CCPBG - R&D Division

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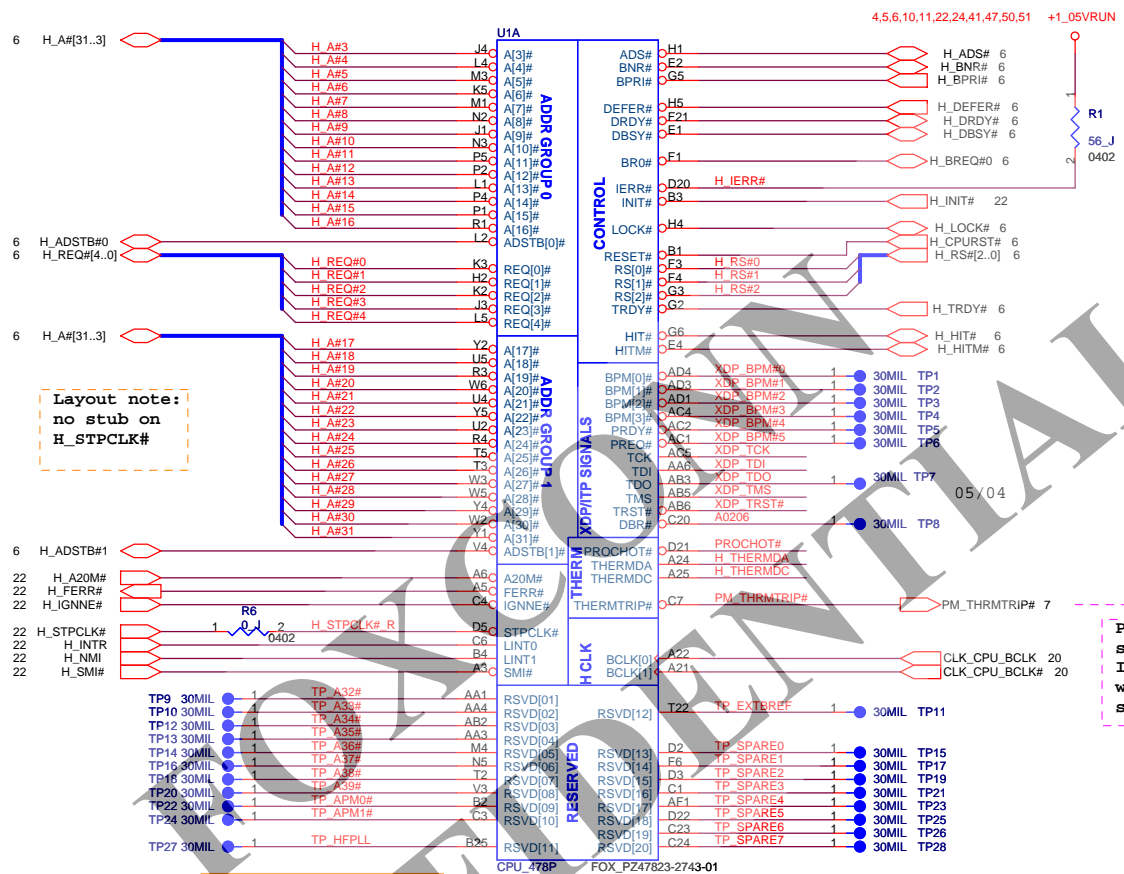
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# RAPTOR3/MS72(CALISTOGA GM/GML Block Diagram)



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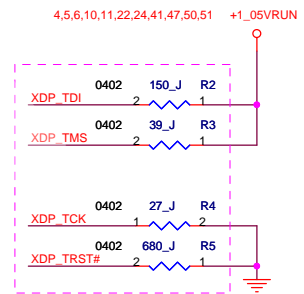




Layout note:  
no stub on  
H\_STPCLK#

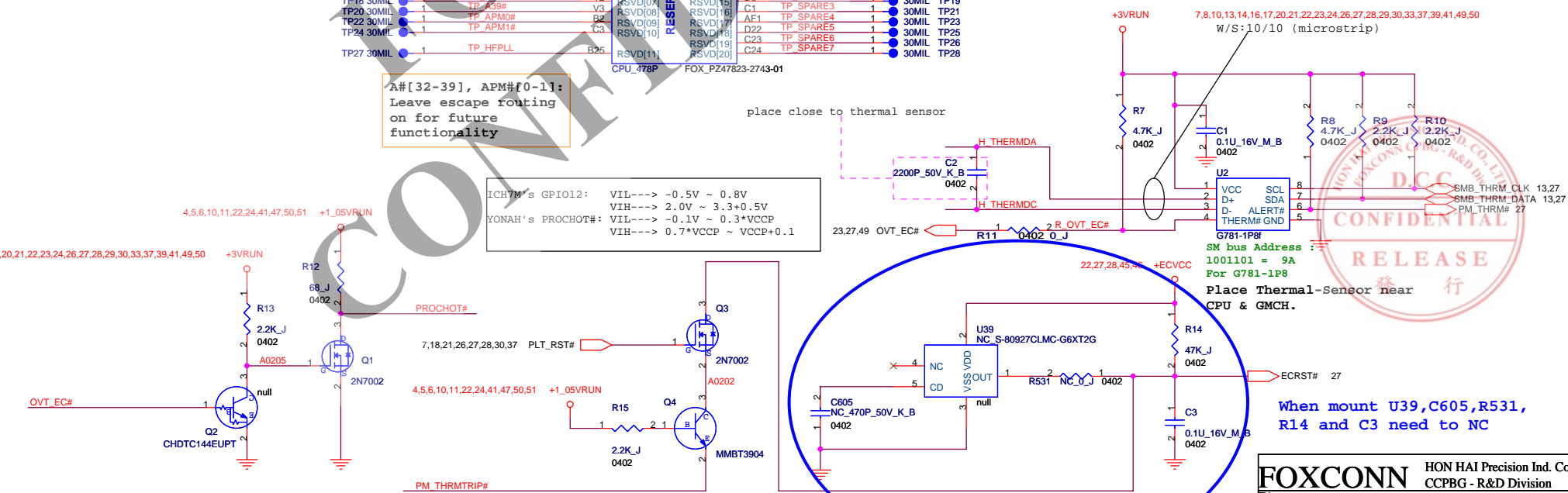
A#[32-39], APM#[0-11]:  
Leave escape routing  
on for future  
functionality

ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V  
VIH----> 2.0V ~ 3.3+0.5V  
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3\*VCCP  
VIH----> 0.7\*VCCP ~ VCCP+0.1



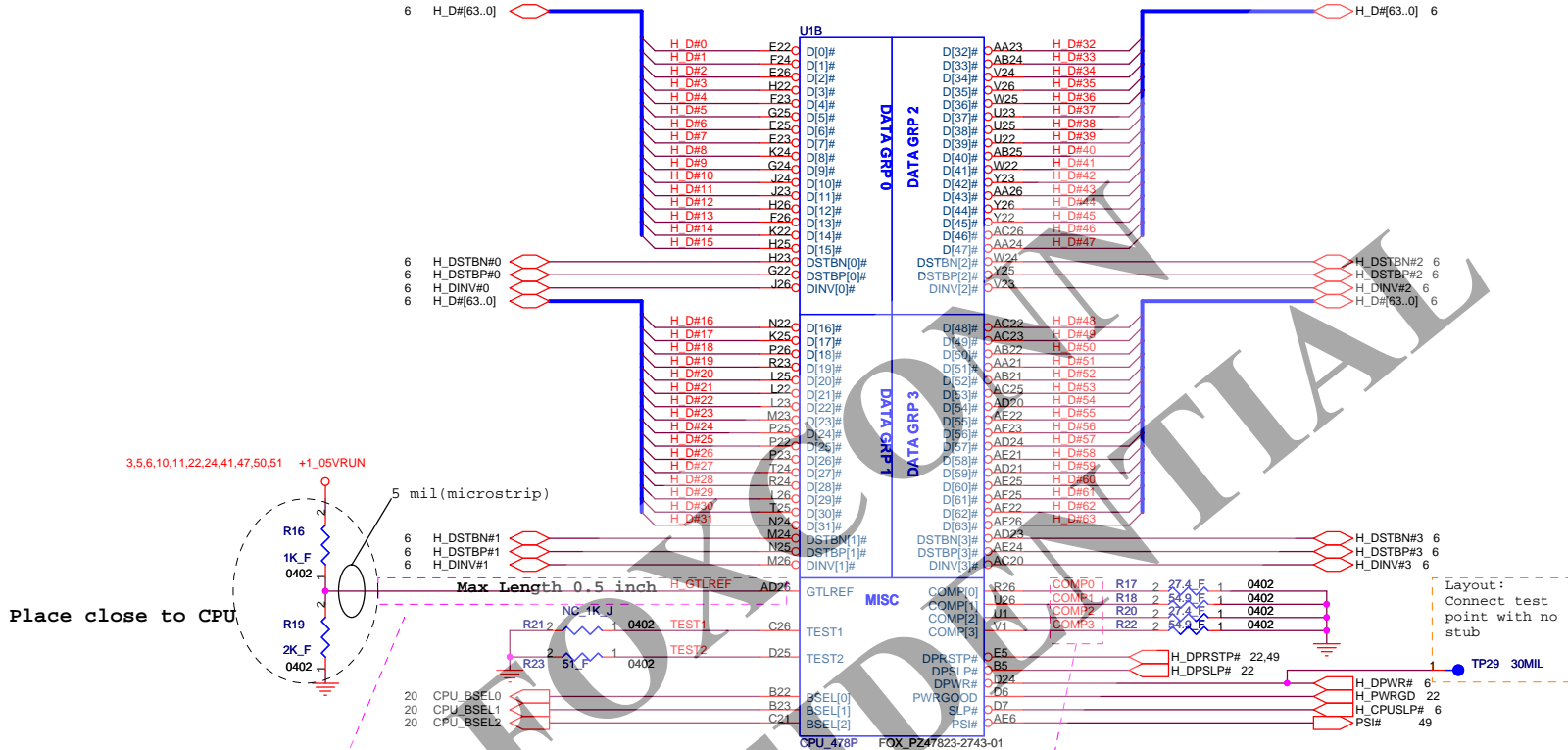
Debug port not used.  
resistors close to CPU.

PM\_THRMTRIP#  
should connect to  
ICH7-M and GMCH  
without T-ing (No  
stub)

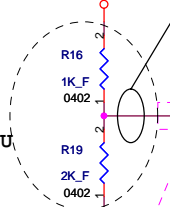


SM bus Address :  
1001101 = 9A  
For G781-1P8  
Place Thermal-Sensor near  
CPU & GMCH.

When mount U39,C605,R531,  
R14 and C3 need to NC



3,5,6,10,11,22,24,41,47,50,51 +1\_05VRUN



Place close to CPU

Max Length 0.5 inch H\_GTLREF

Layout Note:  
Zo=55 ohm, 0.5" max for GTLREF.

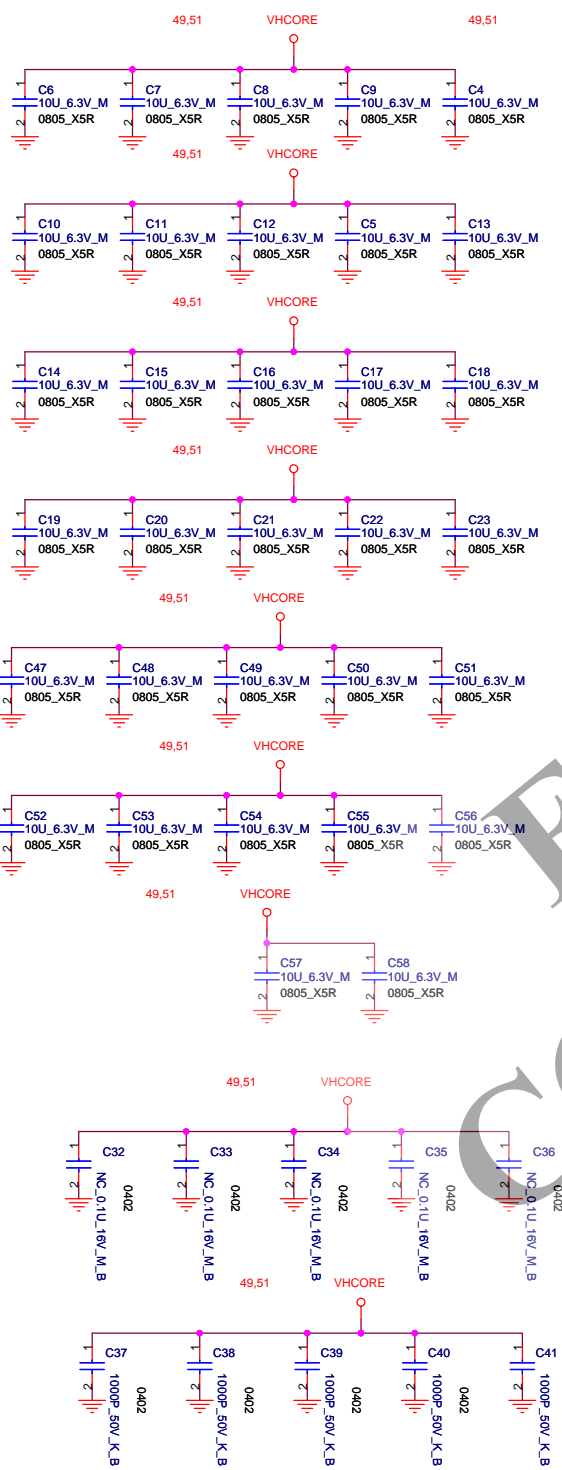
Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter then 0.5".

IMVP6 (max8736)  
cpu PSI# <-> max8736 PSI#  
max8736: VIHmin=0.67V  
VILmax=0.33V  
(ref. max8736 datasheet )

Layout:  
Connect test point with no stub

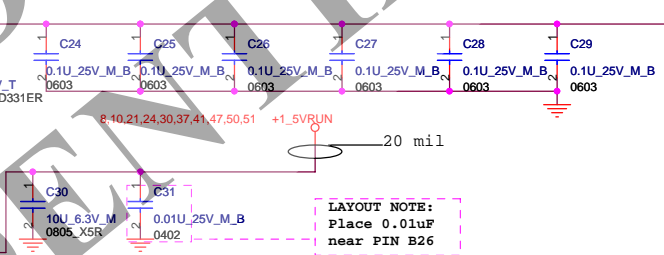
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Pin	Signal	Value
A7	VCC[001]	AB20
A9	VCC[002]	AB7
A10	VCC[003]	AC7
A12	VCC[004]	AC9
A13	VCC[005]	AC12
A15	VCC[006]	AC13
A17	VCC[007]	AC15
A18	VCC[008]	AC17
A20	VCC[009]	AC18
B7	VCC[010]	AD7
B9	VCC[011]	AD9
B10	VCC[012]	AD10
B12	VCC[013]	AD12
B14	VCC[014]	AD14
B15	VCC[015]	AD15
B17	VCC[016]	AD17
B18	VCC[017]	AD18
B20	VCC[018]	AE9
C9	VCC[019]	AE10
C10	VCC[020]	AE12
C12	VCC[021]	AE13
C13	VCC[022]	AE15
C15	VCC[023]	AE17
C17	VCC[024]	AE18
C18	VCC[025]	AE20
D9	VCC[026]	AF9
D10	VCC[027]	AF10
D12	VCC[028]	AF12
D14	VCC[029]	AF14
D15	VCC[030]	AF15
D17	VCC[031]	AF17
D18	VCC[032]	AF18
E7	VCC[033]	AF20
E9	VCC[034]	AF20
F10	VCC[035]	AG21
F12	VCC[036]	AG21
F13	VCC[037]	AG21
F15	VCC[038]	AG21
F17	VCC[039]	AG21
F18	VCC[040]	AG21
E20	VCC[041]	AG21
F9	VCC[042]	AG21
F10	VCC[043]	AG21
F12	VCC[044]	AG21
F14	VCC[045]	AG21
F15	VCC[046]	AG21
F17	VCC[047]	AG21
F18	VCC[048]	AG21
F20	VCC[049]	AG21
AA7	VCC[050]	AG21
AA9	VCC[051]	AG21
AA10	VCC[052]	AG21
AA12	VCC[053]	AG21
AA13	VCC[054]	AG21
AA15	VCC[055]	AG21
AA17	VCC[056]	AG21
AA18	VCC[057]	AG21
AA20	VCC[058]	AG21
AB9	VCC[059]	AG21
AC10	VCC[060]	AG21
AB10	VCC[061]	AG21
AB12	VCC[062]	AG21
AB14	VCC[063]	AG21
AB15	VCC[064]	AG21
AB17	VCC[065]	AG21
AB18	VCC[066]	AG21
AB18	VCC[067]	AG21

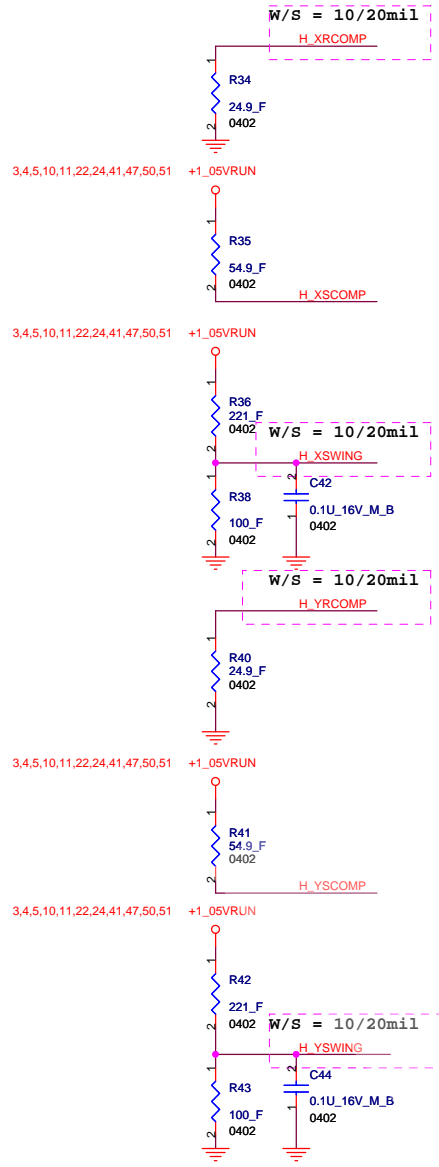
CPU\_VCCA---->120mA  
 CPU\_VCCP----->2.5A  
 CPU\_VCC----->36A



LAYOUT NOTE:  
Place 0.01uF near PIN B26

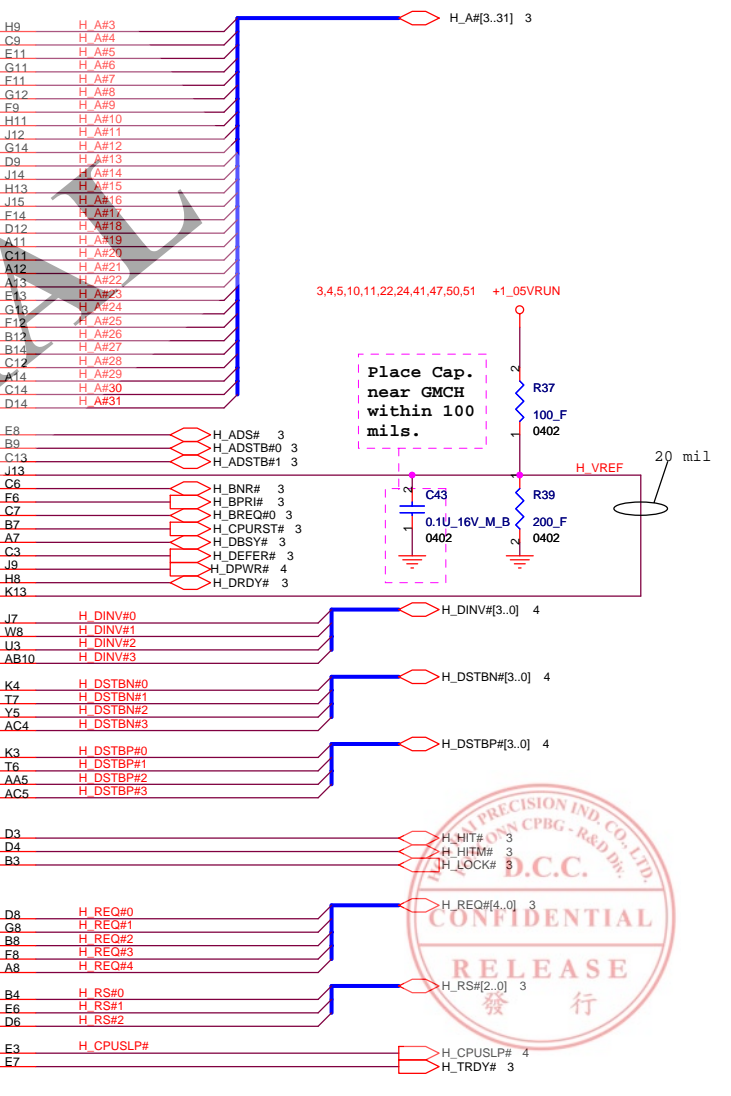
Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.  
 width=18 mil  
 spacing=7 mil

Pin	Signal	Value
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A26	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B16	VSS[012]	VSS[093]
B19	VSS[013]	VSS[094]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C11	VSS[018]	VSS[099]
C14	VSS[019]	VSS[100]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D8	VSS[027]	VSS[108]
D9	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F17	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F22	VSS[050]	VSS[131]
F25	VSS[051]	VSS[132]
G4	VSS[052]	VSS[133]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L16	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M5	VSS[074]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]



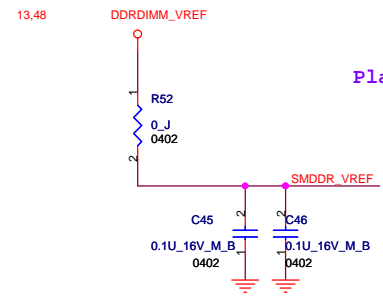
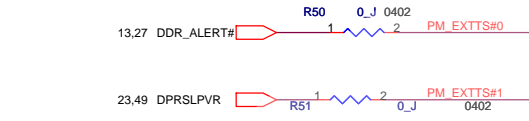
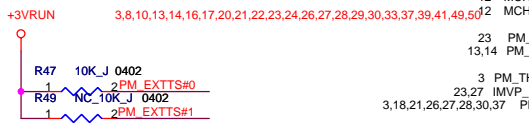
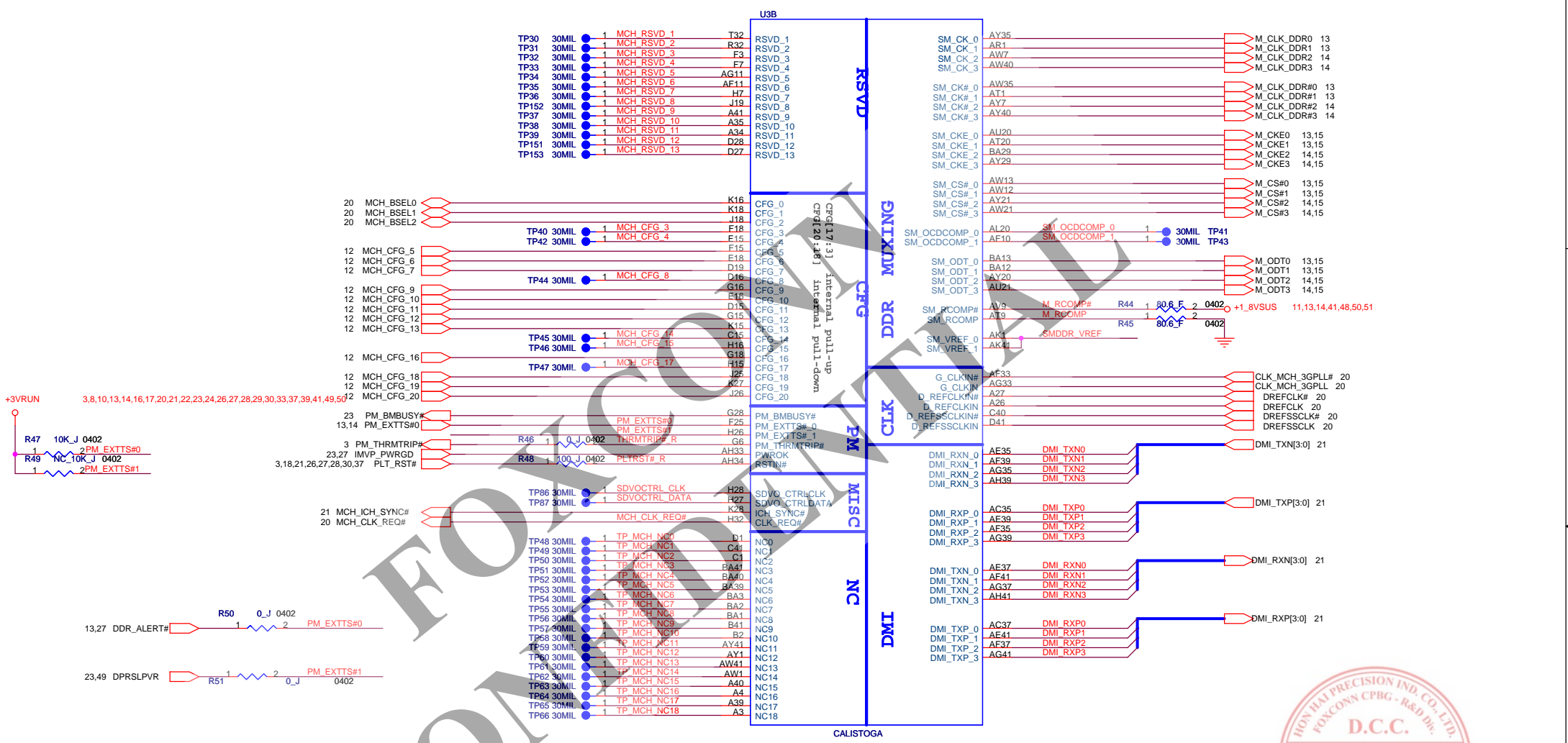
4 H\_D#[63..0] H\_D#[63..0]

USA		HOST	
H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	L10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U8	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y8	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB6	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC8	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	
H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
20 CLK_MCH_BCLK	AG2	H_CLKIN	
20 CLK_MCH_BCLK#	AG1	H_CLKIN#	



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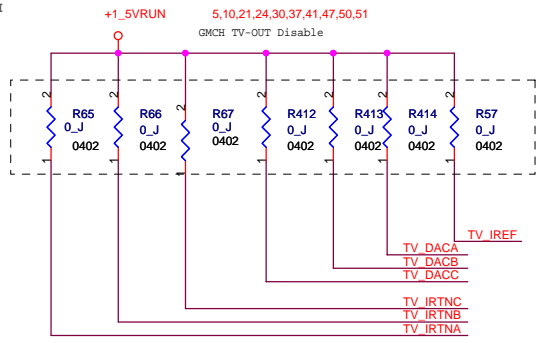
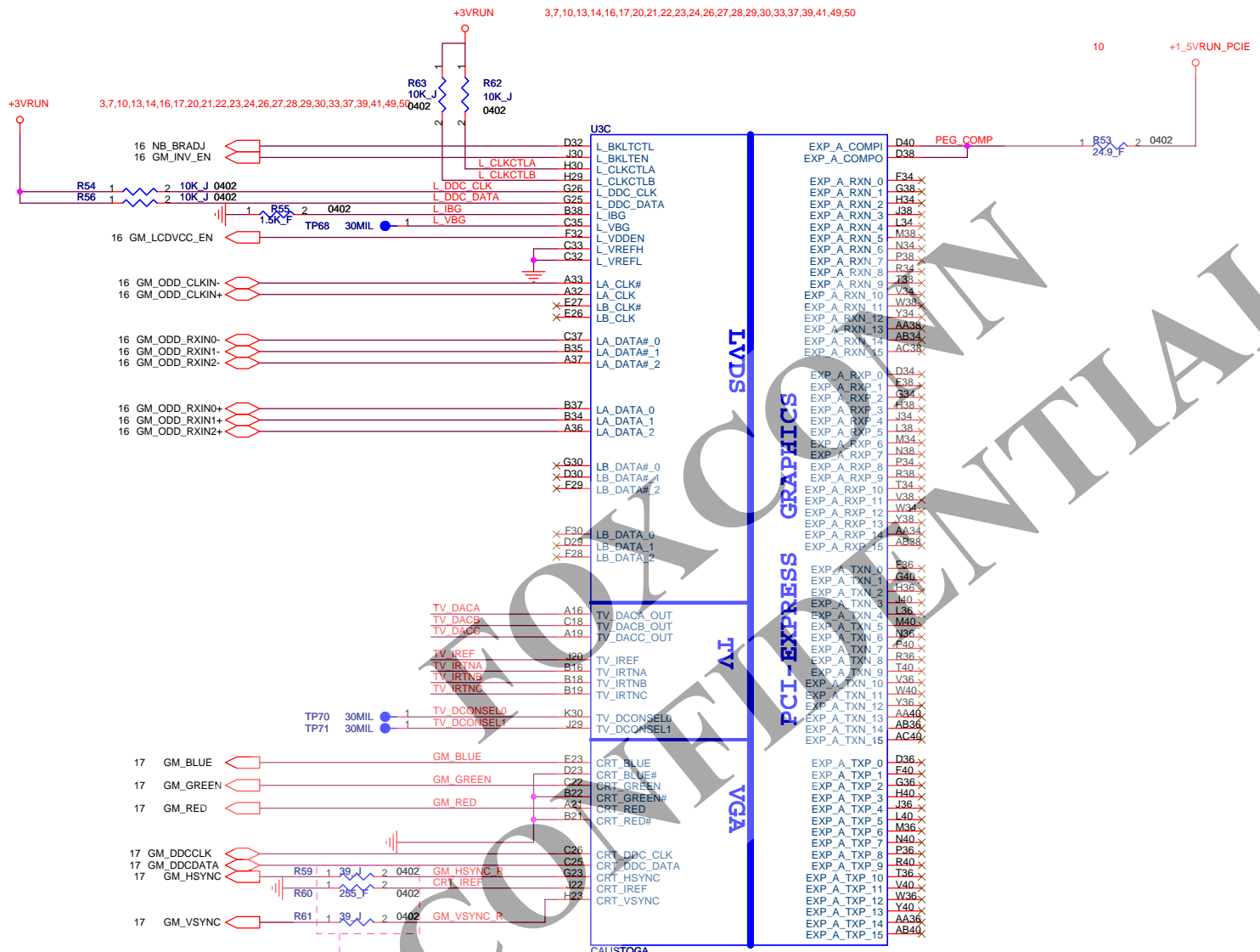




Place close to chipset







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LVDS

PCI-EXPRESS GRAPHICS

TV

VGA

EXP_A_COMP0	D40	PEG_COMP
EXP_A_COMP0	D38	
EXP_A_RXN_0	F34	
EXP_A_RXN_1	G38	
EXP_A_RXN_2	H34	
EXP_A_RXN_3	J38	
EXP_A_RXN_4	L34	
EXP_A_RXN_5	M38	
EXP_A_RXN_6	N34	
EXP_A_RXN_7	P38	
EXP_A_RXN_8	R34	
EXP_A_RXN_9	T38	
EXP_A_RXN_10	W38	
EXP_A_RXN_11	Y34	
EXP_A_RXN_12	AA38	
EXP_A_RXN_13	AB34	
EXP_A_RXN_14	AC38	
EXP_A_RXN_15	AD34	
EXP_A_RXP_0	E38	
EXP_A_RXP_1	F34	
EXP_A_RXP_2	G38	
EXP_A_RXP_3	H34	
EXP_A_RXP_4	J38	
EXP_A_RXP_5	L34	
EXP_A_RXP_6	M38	
EXP_A_RXP_7	N34	
EXP_A_RXP_8	P38	
EXP_A_RXP_9	R34	
EXP_A_RXP_10	T38	
EXP_A_RXP_11	W38	
EXP_A_RXP_12	Y34	
EXP_A_RXP_13	AA34	
EXP_A_RXP_14	AB38	
EXP_A_RXP_15	AC34	
EXP_A_TXN_0	E36	
EXP_A_TXN_1	F40	
EXP_A_TXN_2	H40	
EXP_A_TXN_3	L36	
EXP_A_TXN_4	M40	
EXP_A_TXN_5	N36	
EXP_A_TXN_6	P40	
EXP_A_TXN_7	R36	
EXP_A_TXN_8	T40	
EXP_A_TXN_9	V36	
EXP_A_TXN_10	W40	
EXP_A_TXN_11	Y36	
EXP_A_TXN_12	AA40	
EXP_A_TXN_13	AB36	
EXP_A_TXN_14	AC40	
EXP_A_TXN_15	AD36	
EXP_A_TXP_0	D36	
EXP_A_TXP_1	F40	
EXP_A_TXP_2	G36	
EXP_A_TXP_3	H40	
EXP_A_TXP_4	J36	
EXP_A_TXP_5	L40	
EXP_A_TXP_6	M36	
EXP_A_TXP_7	N40	
EXP_A_TXP_8	P36	
EXP_A_TXP_9	R40	
EXP_A_TXP_10	T36	
EXP_A_TXP_11	W40	
EXP_A_TXP_12	Y36	
EXP_A_TXP_13	AA40	
EXP_A_TXP_14	AB36	
EXP_A_TXP_15	AC40	



13 M\_A\_DQ[63.0]

U3D

M A DQ0	AJ35	SA_DQ0
M A DQ1	AJ34	SA_DQ1
M A DQ2	AM31	SA_DQ2
M A DQ3	AM33	SA_DQ3
M A DQ4	AJ36	SA_DQ4
M A DQ5	AK35	SA_DQ5
M A DQ6	AJ32	SA_DQ6
M A DQ7	AK31	SA_DQ7
M A DQ8	AN35	SA_DQ8
M A DQ9	AP33	SA_DQ9
M A DQ10	AR31	SA_DQ10
M A DQ11	AP31	SA_DQ11
M A DQ12	AN38	SA_DQ12
M A DQ13	AM36	SA_DQ13
M A DQ14	AM34	SA_DQ14
M A DQ15	AK26	SA_DQ15
M A DQ16	AL27	SA_DQ16
M A DQ17	AL28	SA_DQ17
M A DQ18	AM26	SA_DQ18
M A DQ19	AN24	SA_DQ19
M A DQ20	AK28	SA_DQ20
M A DQ21	AL28	SA_DQ21
M A DQ22	AM24	SA_DQ22
M A DQ23	AP26	SA_DQ23
M A DQ24	AP23	SA_DQ24
M A DQ25	AL22	SA_DQ25
M A DQ26	AP21	SA_DQ26
M A DQ27	AV20	SA_DQ27
M A DQ28	AL23	SA_DQ28
M A DQ29	AP24	SA_DQ29
M A DQ30	AP20	SA_DQ30
M A DQ31	AT21	SA_DQ31
M A DQ32	AR12	SA_DQ32
M A DQ33	AR14	SA_DQ33
M A DQ34	AP13	SA_DQ34
M A DQ35	AP12	SA_DQ35
M A DQ36	AT13	SA_DQ36
M A DQ37	AT12	SA_DQ37
M A DQ38	AL14	SA_DQ38
M A DQ39	AL12	SA_DQ39
M A DQ40	AK9	SA_DQ40
M A DQ41	AN7	SA_DQ41
M A DQ42	AK8	SA_DQ42
M A DQ43	AK7	SA_DQ43
M A DQ44	AP9	SA_DQ44
M A DQ45	AN9	SA_DQ45
M A DQ46	AT5	SA_DQ46
M A DQ47	AY2	SA_DQ47
M A DQ48	AW2	SA_DQ48
M A DQ49	AP1	SA_DQ49
M A DQ50	AN2	SA_DQ50
M A DQ51	AV2	SA_DQ51
M A DQ52	AT3	SA_DQ52
M A DQ53	AN1	SA_DQ53
M A DQ54	AL2	SA_DQ54
M A DQ55	AG7	SA_DQ55
M A DQ56	AF9	SA_DQ56
M A DQ57	AG4	SA_DQ57
M A DQ58	AF6	SA_DQ58
M A DQ59	AG9	SA_DQ59
M A DQ60	AH6	SA_DQ60
M A DQ61	AF4	SA_DQ61
M A DQ62	AF4	SA_DQ62
M A DQ63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12
SA_BS_1	AV14
SA_BS_2	BA20
SA_CAS#	AY13
SA_DM_0	AJ33 M A DM0
SA_DM_1	AM35 M A DM1
SA_DM_2	AL26 M A DM2
SA_DM_3	AM22 M A DM3
SA_DM_4	AM14 M A DM4
SA_DM_5	AL9 M A DM5
SA_DM_6	AR3 M A DM6
SA_DM_7	AH4 M A DM7
SA_DQS_0	AK33 M A DQS0
SA_DQS_1	AT33 M A DQS1
SA_DQS_2	AN28 M A DQS2
SA_DQS_3	AM22 M A DQS3
SA_DQS_4	AN12 M A DQS4
SA_DQS_5	AN8 M A DQS5
SA_DQS_6	AP3 M A DQS6
SA_DQS_7	AK32 M A DQS#0
SA_DQS#_0	AU33 M A DQS#1
SA_DQS#_1	AN27 M A DQS#2
SA_DQS#_2	AM21 M A DQS#3
SA_DQS#_3	AM12 M A DQS#4
SA_DQS#_4	AL8 M A DQS#5
SA_DQS#_5	AN3 M A DQS#6
SA_DQS#_6	AH5 M A DQS#7
SA_DQS#_7	
SA_MA_0	AY16 M A A0
SA_MA_1	AU14 M A A1
SA_MA_2	AW15 M A A2
SA_MA_3	BA16 M A A3
SA_MA_4	PA17 M A A4
SA_MA_5	AU16 M A A5
SA_MA_6	AV17 M A A6
SA_MA_7	AU17 M A A7
SA_MA_8	AW17 M A A8
SA_MA_9	AT16 M A A9
SA_MA_10	AU13 M A A10
SA_MA_11	AT17 M A A11
SA_MA_12	AV20 M A A12
SA_MA_13	AV12 M A A13
SA_RAS#	AW14
SA_RCVENIN#	AK23 TP MA RCVENIN#
SA_RCVENOUT#	AK24 TP MA RCVENOUT#
SA_WE#	AY14

M_A_BS0 13,15	M A BS0 13,15
M_A_BS1 13,15	M A BS1 13,15
M_A_BS2 13,15	M A BS2 13,15
M_A_CAS# 13,15	M A CAS# 13,15
M_A_DM[7.0] 13	M A DM[7.0] 13
M_A_DQS[7.0] 13	M A DQS[7.0] 13
M_A_DQS#[7.0] 13	M A DQS#[7.0] 13
M_A_A[13.0] 13,15	M A A[13.0] 13,15
M_A_RAS# 13,15	M A RAS# 13,15
M_A_WE# 13,15	M A WE# 13,15

30MIL TP72  
30MIL TP73

14 M\_B\_DQ[63.0]

U3E

M B DQ0	AK39	SB_DQ0
M B DQ1	AJ37	SB_DQ1
M B DQ2	AP32	SB_DQ2
M B DQ3	AR41	SB_DQ3
M B DQ4	AJ38	SB_DQ4
M B DQ5	AK38	SB_DQ5
M B DQ6	AN41	SB_DQ6
M B DQ7	AP41	SB_DQ7
M B DQ8	AT40	SB_DQ8
M B DQ9	AV41	SB_DQ9
M B DQ10	AU38	SB_DQ10
M B DQ11	AV38	SB_DQ11
M B DQ12	AP38	SB_DQ12
M B DQ13	AR40	SB_DQ13
M B DQ14	AW38	SB_DQ14
M B DQ15	AW38	SB_DQ15
M B DQ16	BA38	SB_DQ16
M B DQ17	AW36	SB_DQ17
M B DQ18	AR36	SB_DQ18
M B DQ19	AP36	SB_DQ19
M B DQ20	AU36	SB_DQ20
M B DQ21	AP35	SB_DQ21
M B DQ22	AP34	SB_DQ22
M B DQ23	AP34	SB_DQ23
M B DQ24	AY33	SB_DQ24
M B DQ25	BA33	SB_DQ25
M B DQ26	AT31	SB_DQ26
M B DQ27	AP29	SB_DQ27
M B DQ28	AU31	SB_DQ28
M B DQ29	AW31	SB_DQ29
M B DQ30	AV29	SB_DQ30
M B DQ31	AW29	SB_DQ31
M B DQ32	AM19	SB_DQ32
M B DQ33	AL19	SB_DQ33
M B DQ34	AP14	SB_DQ34
M B DQ35	AN14	SB_DQ35
M B DQ36	AN17	SB_DQ36
M B DQ37	AM16	SB_DQ37
M B DQ38	AP15	SB_DQ38
M B DQ39	AL15	SB_DQ39
M B DQ40	AJ11	SB_DQ40
M B DQ41	AH10	SB_DQ41
M B DQ42	AJ9	SB_DQ42
M B DQ43	AN10	SB_DQ43
M B DQ44	AK13	SB_DQ44
M B DQ45	AH11	SB_DQ45
M B DQ46	AJ8	SB_DQ46
M B DQ47	AJ8	SB_DQ47
M B DQ48	BA10	SB_DQ48
M B DQ49	AW10	SB_DQ49
M B DQ50	BA4	SB_DQ50
M B DQ51	AW4	SB_DQ51
M B DQ52	AY10	SB_DQ52
M B DQ53	AY9	SB_DQ53
M B DQ54	AW5	SB_DQ54
M B DQ55	AY5	SB_DQ55
M B DQ56	AV4	SB_DQ56
M B DQ57	AR5	SB_DQ57
M B DQ58	AK4	SB_DQ58
M B DQ59	AK3	SB_DQ59
M B DQ60	AT4	SB_DQ60
M B DQ61	AK5	SB_DQ61
M B DQ62	AJ5	SB_DQ62
M B DQ63	AJ3	SB_DQ63

DDR SYSTEM MEMORY B

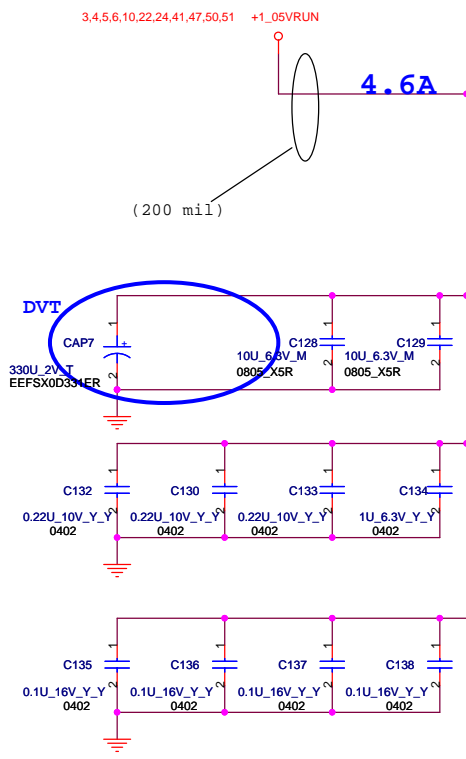
SB_BS_0	AT24
SB_BS_1	AV23
SB_BS_2	AY28
SB_CAS#	AR24
SB_DM_0	AK36 M B DM0
SB_DM_1	AR38 M B DM1
SB_DM_2	AT36 M B DM2
SB_DM_3	BA31 M B DM3
SB_DM_4	AL17 M B DM4
SB_DM_5	AH8 M B DM5
SB_DM_6	BA5 M B DM6
SB_DM_7	AN4 M B DM7
SB_DQS_0	AM39 M B DQS0
SB_DQS_1	AT39 M B DQS1
SB_DQS_2	AU35 M B DQS2
SB_DQS_3	AR29 M B DQS3
SB_DQS_4	AR16 M B DQS4
SB_DQS_5	AR10 M B DQS5
SB_DQS_6	AR7 M B DQS6
SB_DQS_7	AN5 M B DQS7
SB_DQS#_0	AM40 M B DQS#0
SB_DQS#_1	AU39 M B DQS#1
SB_DQS#_2	AT35 M B DQS#2
SB_DQS#_3	AP29 M B DQS#3
SB_DQS#_4	AP16 M B DQS#4
SB_DQS#_5	AT10 M B DQS#5
SB_DQS#_6	AT7 M B DQS#6
SB_DQS#_7	AP5 M B DQS#7
SB_MA_0	AY23 M B A0
SB_MA_1	AW24 M B A1
SB_MA_2	AY24 M B A2
SB_MA_3	AR28 M B A3
SB_MA_4	AT27 M B A4
SB_MA_5	AT28 M B A5
SB_MA_6	AU27 M B A6
SB_MA_7	AV28 M B A7
SB_MA_8	AW27 M B A8
SB_MA_9	AW27 M B A9
SB_MA_10	AV24 M B A10
SB_MA_11	BA27 M B A11
SB_MA_12	AY27 M B A12
SB_MA_13	AR23 M B A13
SB_RAS#	AU23
SB_RCVENIN#	AK16 TP MB RCVENIN#
SB_RCVENOUT#	AK18 TP MB RCVENOUT#
SB_WE#	AR27

M_B_BS0 14,15	M B BS0 14,15
M_B_BS1 14,15	M B BS1 14,15
M_B_BS2 14,15	M B BS2 14,15
M_B_CAS# 14,15	M B CAS# 14,15
M_B_DM[7.0] 14	M B DM[7.0] 14
M_B_DQS[7.0] 14	M B DQS[7.0] 14
M_B_DQS#[7.0] 14	M B DQS#[7.0] 14
M_B_A[13.0] 14,15	M B A[13.0] 14,15
M_B_RAS# 14,15	M B RAS# 14,15
M_B_WE# 14,15	M B WE# 14,15

30MIL TP74  
30MIL TP75



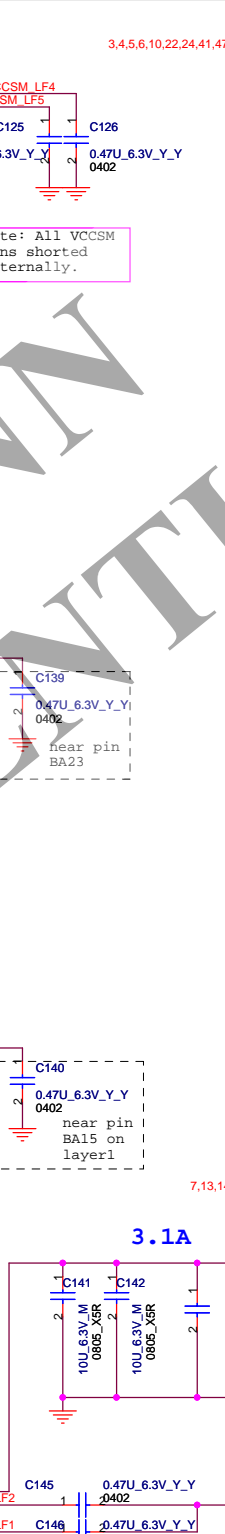




Pin	Signal
AA33	VCC_0
W33	VCC_1
P33	VCC_2
L33	VCC_3
J33	VCC_4
AA32	VCC_5
Y32	VCC_6
W32	VCC_7
V32	VCC_8
P32	VCC_9
N32	VCC_10
M32	VCC_11
L32	VCC_12
J32	VCC_13
AA31	VCC_14
W31	VCC_15
V31	VCC_16
T31	VCC_17
R31	VCC_18
P31	VCC_19
N31	VCC_20
M31	VCC_21
AA30	VCC_22
Y30	VCC_23
W30	VCC_24
V30	VCC_25
U30	VCC_26
T30	VCC_27
R30	VCC_28
P30	VCC_29
N30	VCC_30
M30	VCC_31
L30	VCC_32
AA29	VCC_33
Y29	VCC_34
W29	VCC_35
V29	VCC_36
U29	VCC_37
T29	VCC_38
R29	VCC_39
P29	VCC_40
M29	VCC_41
L29	VCC_42
AA28	VCC_43
Y28	VCC_44
W28	VCC_45
V28	VCC_46
U28	VCC_47
T28	VCC_48
R28	VCC_49
P28	VCC_50
N28	VCC_51
M28	VCC_52
L28	VCC_53
AA27	VCC_54
Y27	VCC_55
W27	VCC_56
V27	VCC_57
U27	VCC_58
T27	VCC_59
R27	VCC_60
P27	VCC_61
N27	VCC_62
M27	VCC_63
L27	VCC_64
AA26	VCC_65
Y26	VCC_66
W26	VCC_67
V26	VCC_68
U26	VCC_69
T26	VCC_70
R26	VCC_71
P26	VCC_72
N26	VCC_73
M26	VCC_74
L26	VCC_75
AA25	VCC_76
Y25	VCC_77
W25	VCC_78
V25	VCC_79
U25	VCC_80
T25	VCC_81
R25	VCC_82
P25	VCC_83
N25	VCC_84
M25	VCC_85
L25	VCC_86
AA24	VCC_87
Y24	VCC_88
W24	VCC_89
V24	VCC_90
U24	VCC_91
T24	VCC_92
R24	VCC_93
P24	VCC_94
N24	VCC_95
M24	VCC_96
L24	VCC_97
AA23	VCC_98
Y23	VCC_99
W23	VCC_100
V23	VCC_101
U23	VCC_102
T23	VCC_103
R23	VCC_104
P23	VCC_105
N23	VCC_106
M23	VCC_107
L23	VCC_108
AA22	VCC_109
Y22	VCC_110

Pin	Signal
AA41	VCC_SM_0
AT41	VCC_SM_1
AM41	VCC_SM_2
AU40	VCC_SM_3
BA34	VCC_SM_4
AV34	VCC_SM_5
AW34	VCC_SM_6
AU34	VCC_SM_7
AT34	VCC_SM_8
AR34	VCC_SM_9
BA30	VCC_SM_10
AV30	VCC_SM_11
AW30	VCC_SM_12
AV30	VCC_SM_13
AW30	VCC_SM_14
AU30	VCC_SM_15
AT30	VCC_SM_16
AR30	VCC_SM_17
AN30	VCC_SM_18
AM30	VCC_SM_19
AM29	VCC_SM_20
AL29	VCC_SM_21
AK29	VCC_SM_22
AJ29	VCC_SM_23
AH29	VCC_SM_24
AJ28	VCC_SM_25
AH28	VCC_SM_26
AJ27	VCC_SM_27
AH27	VCC_SM_28
AK26	VCC_SM_29
AK26	VCC_SM_30
AV26	VCC_SM_31
AV26	VCC_SM_32
AJ26	VCC_SM_33
AT26	VCC_SM_34
AR26	VCC_SM_35
AJ26	VCC_SM_36
AH26	VCC_SM_37
AJ25	VCC_SM_38
AH25	VCC_SM_39
AJ24	VCC_SM_40
AH24	VCC_SM_41
BA23	VCC_SM_42
AJ23	VCC_SM_43
BA22	VCC_SM_44
AY22	VCC_SM_45
AV22	VCC_SM_46
AV22	VCC_SM_47
AV22	VCC_SM_48
AT22	VCC_SM_49
AR22	VCC_SM_50
AR22	VCC_SM_51
AK22	VCC_SM_52
AJ22	VCC_SM_53
AK21	VCC_SM_54
AK20	VCC_SM_55
BA19	VCC_SM_56
AV19	VCC_SM_57
AV19	VCC_SM_58
AV19	VCC_SM_59
AU19	VCC_SM_60
AU19	VCC_SM_61
AT19	VCC_SM_62
AP19	VCC_SM_63
AK19	VCC_SM_64
AJ19	VCC_SM_65
AJ18	VCC_SM_66
AJ17	VCC_SM_67
AH17	VCC_SM_68
AH16	VCC_SM_69
VCC_SM_70	VCC_SM_70
VCC_SM_71	VCC_SM_71
VCC_SM_72	VCC_SM_72
VCC_SM_73	VCC_SM_73
VCC_SM_74	VCC_SM_74
VCC_SM_75	VCC_SM_75
VCC_SM_76	VCC_SM_76
VCC_SM_77	VCC_SM_77
VCC_SM_78	VCC_SM_78
VCC_SM_79	VCC_SM_79
VCC_SM_80	VCC_SM_80
VCC_SM_81	VCC_SM_81
VCC_SM_82	VCC_SM_82
VCC_SM_83	VCC_SM_83
VCC_SM_84	VCC_SM_84
VCC_SM_85	VCC_SM_85
VCC_SM_86	VCC_SM_86
VCC_SM_87	VCC_SM_87
VCC_SM_88	VCC_SM_88
VCC_SM_89	VCC_SM_89
VCC_SM_90	VCC_SM_90
VCC_SM_91	VCC_SM_91
VCC_SM_92	VCC_SM_92
VCC_SM_93	VCC_SM_93
VCC_SM_94	VCC_SM_94
VCC_SM_95	VCC_SM_95
VCC_SM_96	VCC_SM_96
VCC_SM_97	VCC_SM_97
VCC_SM_98	VCC_SM_98
VCC_SM_99	VCC_SM_99
VCC_SM_100	VCC_SM_100
VCC_SM_101	VCC_SM_101
VCC_SM_102	VCC_SM_102
VCC_SM_103	VCC_SM_103
VCC_SM_104	VCC_SM_104
VCC_SM_105	VCC_SM_105
VCC_SM_106	VCC_SM_106
VCC_SM_107	VCC_SM_107

Pin	Signal
AD27	VCC_NCTF0
AB27	VCC_NCTF1
AA27	VCC_NCTF2
Y27	VCC_NCTF3
W27	VCC_NCTF4
V27	VCC_NCTF5
U27	VCC_NCTF6
T27	VCC_NCTF7
R27	VCC_NCTF8
AD26	VCC_NCTF9
AC26	VCC_NCTF10
AB26	VCC_NCTF11
AA26	VCC_NCTF12
Y26	VCC_NCTF13
W26	VCC_NCTF14
V26	VCC_NCTF15
U26	VCC_NCTF16
T26	VCC_NCTF17
AD25	VCC_NCTF18
AC25	VCC_NCTF19
AA25	VCC_NCTF20
Y25	VCC_NCTF21
W25	VCC_NCTF22
V25	VCC_NCTF23
U25	VCC_NCTF24
T25	VCC_NCTF25
R25	VCC_NCTF26
AD24	VCC_NCTF27
AC24	VCC_NCTF28
AB24	VCC_NCTF29
AA24	VCC_NCTF30
Y24	VCC_NCTF31
W24	VCC_NCTF32
V24	VCC_NCTF33
U24	VCC_NCTF34
T24	VCC_NCTF35
R24	VCC_NCTF36
AD23	VCC_NCTF37
AC23	VCC_NCTF38
AA23	VCC_NCTF39
Y23	VCC_NCTF40
W23	VCC_NCTF41
V23	VCC_NCTF42
U23	VCC_NCTF43
T23	VCC_NCTF44
R23	VCC_NCTF45
AD22	VCC_NCTF46
AC22	VCC_NCTF47
AA22	VCC_NCTF48
Y22	VCC_NCTF49
W22	VCC_NCTF50
V22	VCC_NCTF51
U22	VCC_NCTF52
T22	VCC_NCTF53
R22	VCC_NCTF54
AD21	VCC_NCTF55
AC21	VCC_NCTF56
AA21	VCC_NCTF57
Y21	VCC_NCTF58
W21	VCC_NCTF59
V21	VCC_NCTF60
U21	VCC_NCTF61
T21	VCC_NCTF62
R21	VCC_NCTF63
AD20	VCC_NCTF64
V20	VCC_NCTF65
U20	VCC_NCTF66
T20	VCC_NCTF67
R20	VCC_NCTF68
AD19	VCC_NCTF69
V19	VCC_NCTF70
U19	VCC_NCTF71
T19	VCC_NCTF72
AD18	VCC_NCTF73
AC18	VCC_NCTF74
AB18	VCC_NCTF75
AA18	VCC_NCTF76
Y18	VCC_NCTF77
W18	VCC_NCTF78
V18	VCC_NCTF79
U18	VCC_NCTF80
T18	VCC_NCTF81
AD17	VCC_NCTF82
AC17	VCC_NCTF83
AB17	VCC_NCTF84
AA17	VCC_NCTF85
Y17	VCC_NCTF86
W17	VCC_NCTF87
V17	VCC_NCTF88
U17	VCC_NCTF89
T17	VCC_NCTF90
R17	VCC_NCTF91
AD16	VCC_NCTF92
AC16	VCC_NCTF93
AB16	VCC_NCTF94
AA16	VCC_NCTF95
Y16	VCC_NCTF96
W16	VCC_NCTF97
V16	VCC_NCTF98
U16	VCC_NCTF99
T16	VCC_NCTF100
R16	VCC_NCTF101
AD15	VCC_NCTF102
AC15	VCC_NCTF103
AB15	VCC_NCTF104
AA15	VCC_NCTF105
Y15	VCC_NCTF106
W15	VCC_NCTF107
V15	VCC_NCTF108
U15	VCC_NCTF109
T15	VCC_NCTF110
R15	VCC_NCTF111
AD14	VCC_NCTF112
AC14	VCC_NCTF113
AB14	VCC_NCTF114
AA14	VCC_NCTF115
Y14	VCC_NCTF116
W14	VCC_NCTF117
V14	VCC_NCTF118
U14	VCC_NCTF119
T14	VCC_NCTF120
R14	VCC_NCTF121
AD13	VCC_NCTF122
AC13	VCC_NCTF123
AB13	VCC_NCTF124
AA13	VCC_NCTF125
Y13	VCC_NCTF126
W13	VCC_NCTF127
V13	VCC_NCTF128
U13	VCC_NCTF129
T13	VCC_NCTF130
R13	VCC_NCTF131
AD12	VCC_NCTF132
AC12	VCC_NCTF133
AB12	VCC_NCTF134
AA12	VCC_NCTF135
Y12	VCC_NCTF136
W12	VCC_NCTF137
V12	VCC_NCTF138
U12	VCC_NCTF139
T12	VCC_NCTF140
R12	VCC_NCTF141
AD11	VCC_NCTF142
AC11	VCC_NCTF143
AB11	VCC_NCTF144
AA11	VCC_NCTF145
Y11	VCC_NCTF146
W11	VCC_NCTF147
V11	VCC_NCTF148
U11	VCC_NCTF149
T11	VCC_NCTF150
R11	VCC_NCTF151
AD10	VCC_NCTF152
AC10	VCC_NCTF153
AB10	VCC_NCTF154
AA10	VCC_NCTF155
Y10	VCC_NCTF156
W10	VCC_NCTF157
V10	VCC_NCTF158
U10	VCC_NCTF159
T10	VCC_NCTF160
R10	VCC_NCTF161
AD9	VCC_NCTF162
AC9	VCC_NCTF163
AB9	VCC_NCTF164
AA9	VCC_NCTF165
Y9	VCC_NCTF166
W9	VCC_NCTF167
V9	VCC_NCTF168
U9	VCC_NCTF169
T9	VCC_NCTF170
R9	VCC_NCTF171
AD8	VCC_NCTF172
AC8	VCC_NCTF173
AB8	VCC_NCTF174
AA8	VCC_NCTF175
Y8	VCC_NCTF176
W8	VCC_NCTF177
V8	VCC_NCTF178
U8	VCC_NCTF179
T8	VCC_NCTF180
R8	VCC_NCTF181
AD7	VCC_NCTF182
AC7	VCC_NCTF183
AB7	VCC_NCTF184
AA7	VCC_NCTF185
Y7	VCC_NCTF186
W7	VCC_NCTF187
V7	VCC_NCTF188
U7	VCC_NCTF189
T7	VCC_NCTF190
R7	VCC_NCTF191
AD6	VCC_NCTF192
AC6	VCC_NCTF193
AB6	VCC_NCTF194
AA6	VCC_NCTF195
Y6	VCC_NCTF196
W6	VCC_NCTF197
V6	VCC_NCTF198
U6	VCC_NCTF199
T6	VCC_NCTF200
R6	VCC_NCTF201
AD5	VCC_NCTF202
AC5	VCC_NCTF203
AB5	VCC_NCTF204
AA5	VCC_NCTF205
Y5	VCC_NCTF206
W5	VCC_NCTF207
V5	VCC_NCTF208
U5	VCC_NCTF209
T5	VCC_NCTF210
R5	VCC_NCTF211
AD4	VCC_NCTF212
AC4	VCC_NCTF213
AB4	VCC_NCTF214
AA4	VCC_NCTF215
Y4	VCC_NCTF216
W4	VCC_NCTF217
V4	VCC_NCTF218
U4	VCC_NCTF219
T4	VCC_NCTF220
R4	VCC_NCTF221
AD3	VCC_NCTF222
AC3	VCC_NCTF223
AB3	VCC_NCTF224
AA3	VCC_NCTF225
Y3	VCC_NCTF226
W3	VCC_NCTF227
V3	VCC_NCTF228
U3	VCC_NCTF229
T3	VCC_NCTF230
R3	VCC_NCTF231
AD2	VCC_NCTF232
AC2	VCC_NCTF233
AB2	VCC_NCTF234
AA2	VCC_NCTF235
Y2	VCC_NCTF236
W2	VCC_NCTF237
V2	VCC_NCTF238
U2	VCC_NCTF239
T2	VCC_NCTF240
R2	VCC_NCTF241
AD1	VCC_NCTF242
AC1	VCC_NCTF243
AB1	VCC_NCTF244
AA1	VCC_NCTF245
Y1	VCC_NCTF246
W1	VCC_NCTF247
V1	VCC_NCTF248
U1	VCC_NCTF249
T1	VCC_NCTF250
R1	VCC_NCTF251
AD0	VCC_NCTF252
AC0	VCC_NCTF253
AB0	VCC_NCTF254
AA0	VCC_NCTF255
Y0	VCC_NCTF256
W0	VCC_NCTF257
V0	VCC_NCTF258
U0	VCC_NCTF259
T0	VCC_NCTF260
R0	VCC_NCTF261
AD0	VCC_NCTF262
AC0	VCC_NCTF263
AB0	VCC_NCTF264
AA0	VCC_NCTF265
Y0	VCC_NCTF266
W0	VCC_NCTF267
V0	VCC_NCTF268
U0	VCC_NCTF269
T0	VCC_NCTF270
R0	VCC_NCTF271
AD0	VCC_NCTF272



Pin	Signal
AE27	VSS_NCTF0
AE26	VSS_NCTF1
AE25	VSS_NCTF2
AE24	VSS_NCTF3
AE23	VSS_NCTF4
AE22	VSS_NCTF5
AE21	VSS_NCTF6
AE20	VSS_NCTF7
AE19	VSS_NCTF8
AE18	VSS_NCTF9
AC17	VSS_NCTF10
Y17	VSS_NCTF11
U17	VSS_NCTF12
AG27	VCC_AUX_NCTF0
AF27	VCC_AUX_NCTF1
AG26	VCC_AUX_NCTF2
AF26	VCC_AUX_NCTF

7 MCH\_CFG\_5 ← 1 ● 30MIL TP76

MCH\_CFG\_5  
Low = DMIX2  
High = DMIX4

7 MCH\_CFG\_6 ← 1 ● 30MIL TP77

MCH\_CFG\_6  
Low = Moby Dick  
High = Calistoga  
DDR2 select (default high)

7 MCH\_CFG\_7 ← 1 ● 30MIL TP78

MCH\_CFG\_7 (CPU Strap)  
Low = RSVD  
High = Mobile Yonah processor

7 MCH\_CFG\_9 ← 1 ● 30MIL TP81

MCH\_CFG\_9 (PCIe Graphics Lane)  
Low = Reverse Lane operation  
High = Normal operation

For layout convenience

7 MCH\_CFG\_10 ← 1 ● 30MIL TP82

MCH\_CFG\_10 (HOST PLL VCC SELECT)  
Low = RESERVED  
High = MOBILITY

7 MCH\_CFG\_11 ← 1 ● 30MIL TP83

MCH\_CFG\_11 (PSB 4x CLK ENABLE)  
Low = Calistoga  
High = Reserved



7 MCH\_CFG\_12 ← 1 ● 30MIL TP84

7 MCH\_CFG\_13 ← 1 ● 30MIL TP85

MCH\_CFG\_[13:12] (XOR/ALLZ)  
00=Partial Clock Gating Disable  
01=XOR Mode Enable  
10=All-Z Mode Enable  
11=Normal Operation(Default)

7 MCH\_CFG\_16 ← 1 ● 30MIL TP160

MCH\_CFG\_16 (FSB Dynamic ODT)  
Low = Dynamic ODT Disabled  
High = Dynamic ODT Enable

MCH\_CFG\_18 (VCC\_CORE Select)  
Low = 1.05V(default)  
High = 1.5V

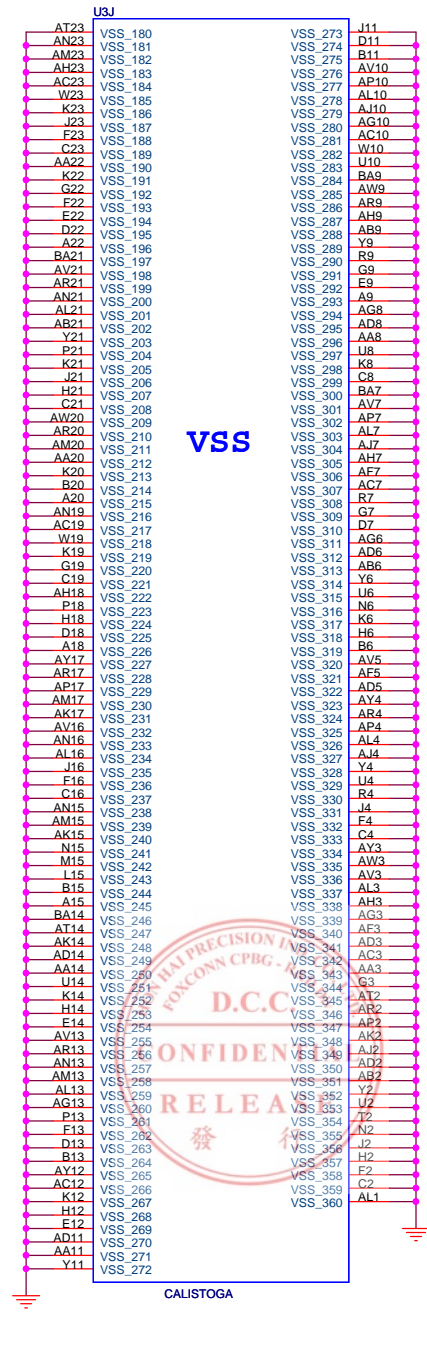
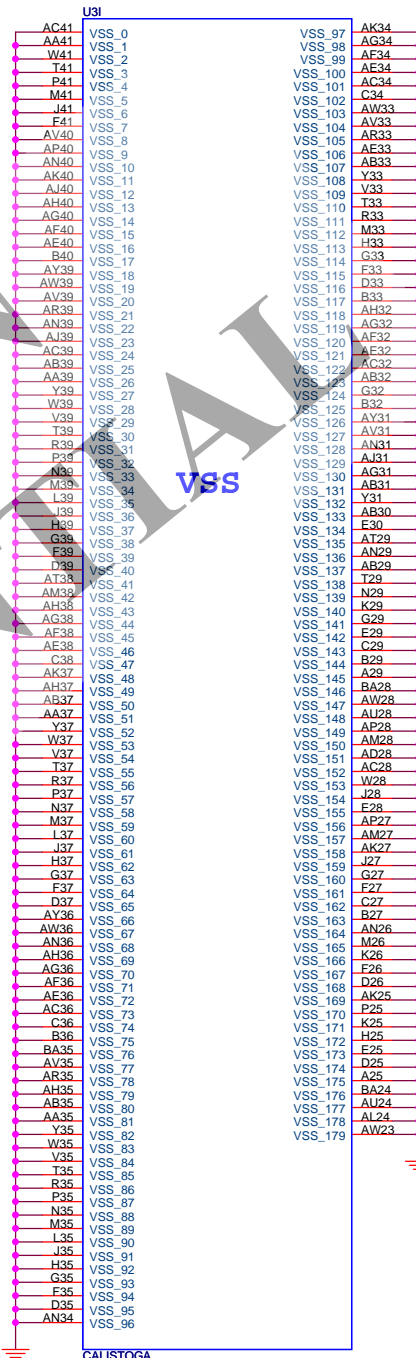
7 MCH\_CFG\_18 ← 1 ● 30MIL TP79

MCH\_CFG\_19 (DMI LANE REVERSAL)  
Low = Normal(default)  
High = LANES REVERSED

7 MCH\_CFG\_19 ← 1 ● 30MIL TP80

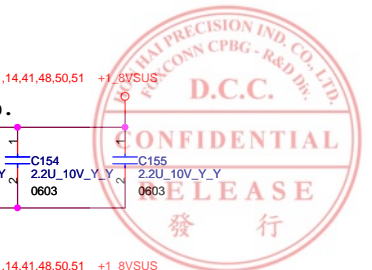
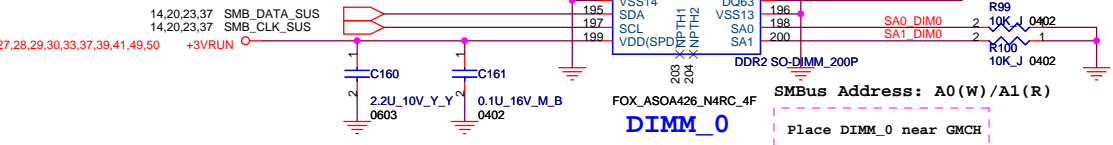
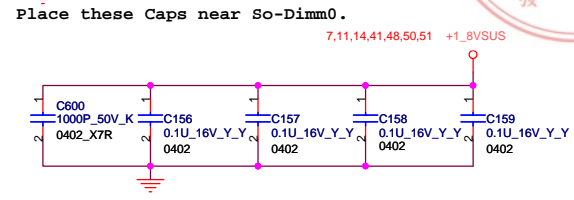
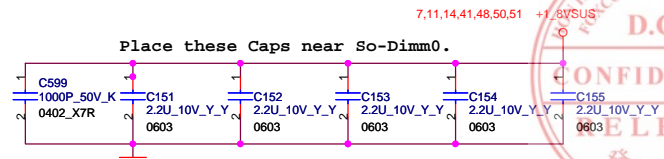
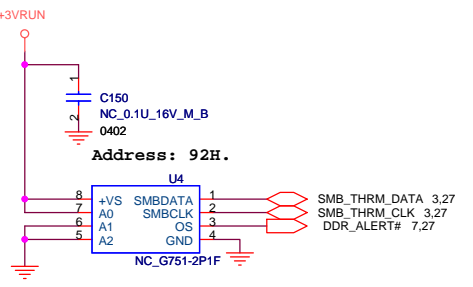
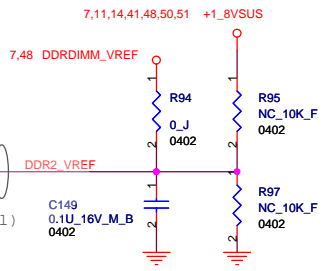
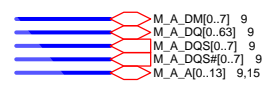
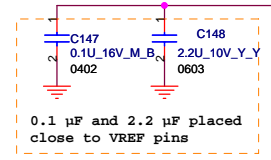
MCH\_CFG\_20  
Low = Only SDVO or PCIe x1 is operational (defaults)  
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

Layout Noe:  
Location of all MCH\_CFG strap resistors needs to be close to trace to minimize stub

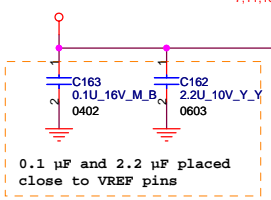


7,11,14,41,48,50,51 +1\_8VSUS

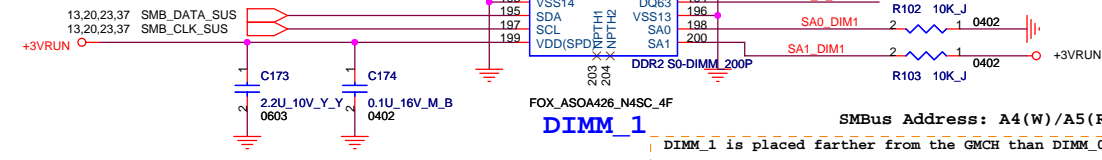
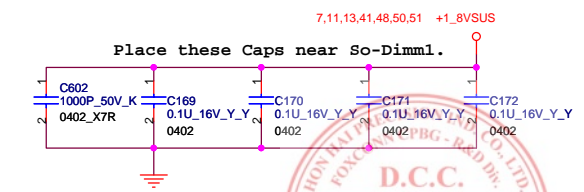
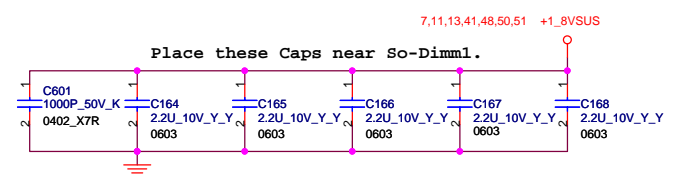
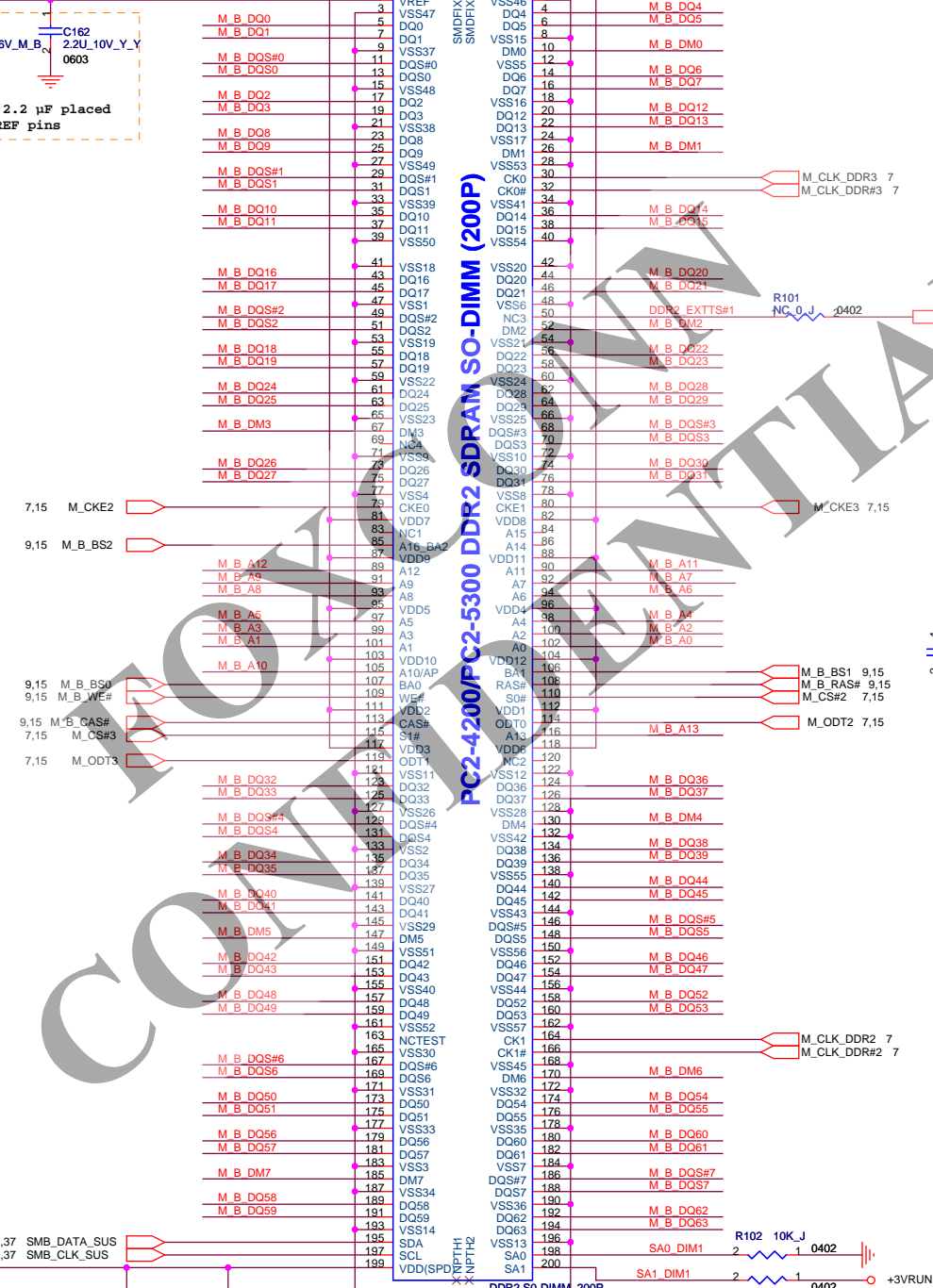
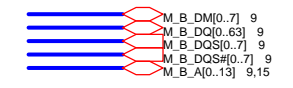
1.8V per DIMM=3.08A



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title: <b>DDR(H)SO-DIMM_0</b>		
Size: A3	Document Number: MS72-1-01	Rev: 0.1
Date: Tuesday, December 05, 2006	Sheet: 13	of: 55



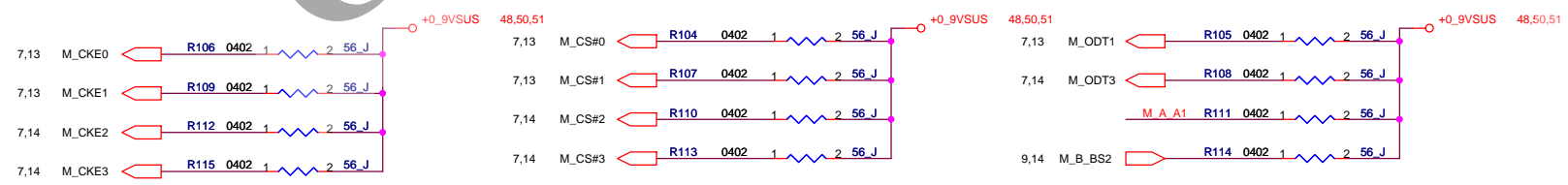
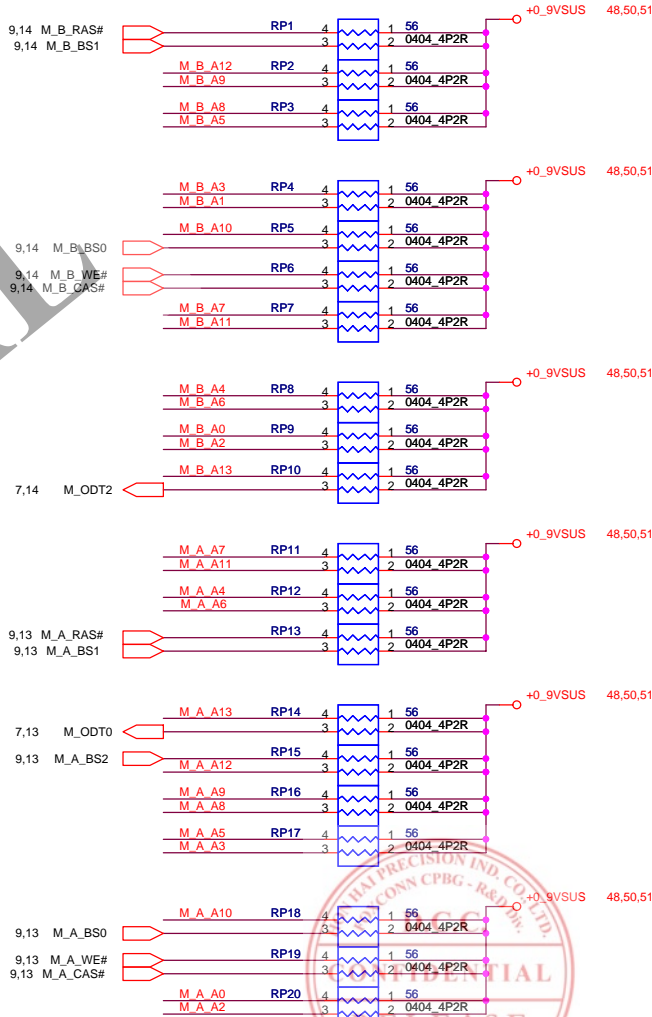
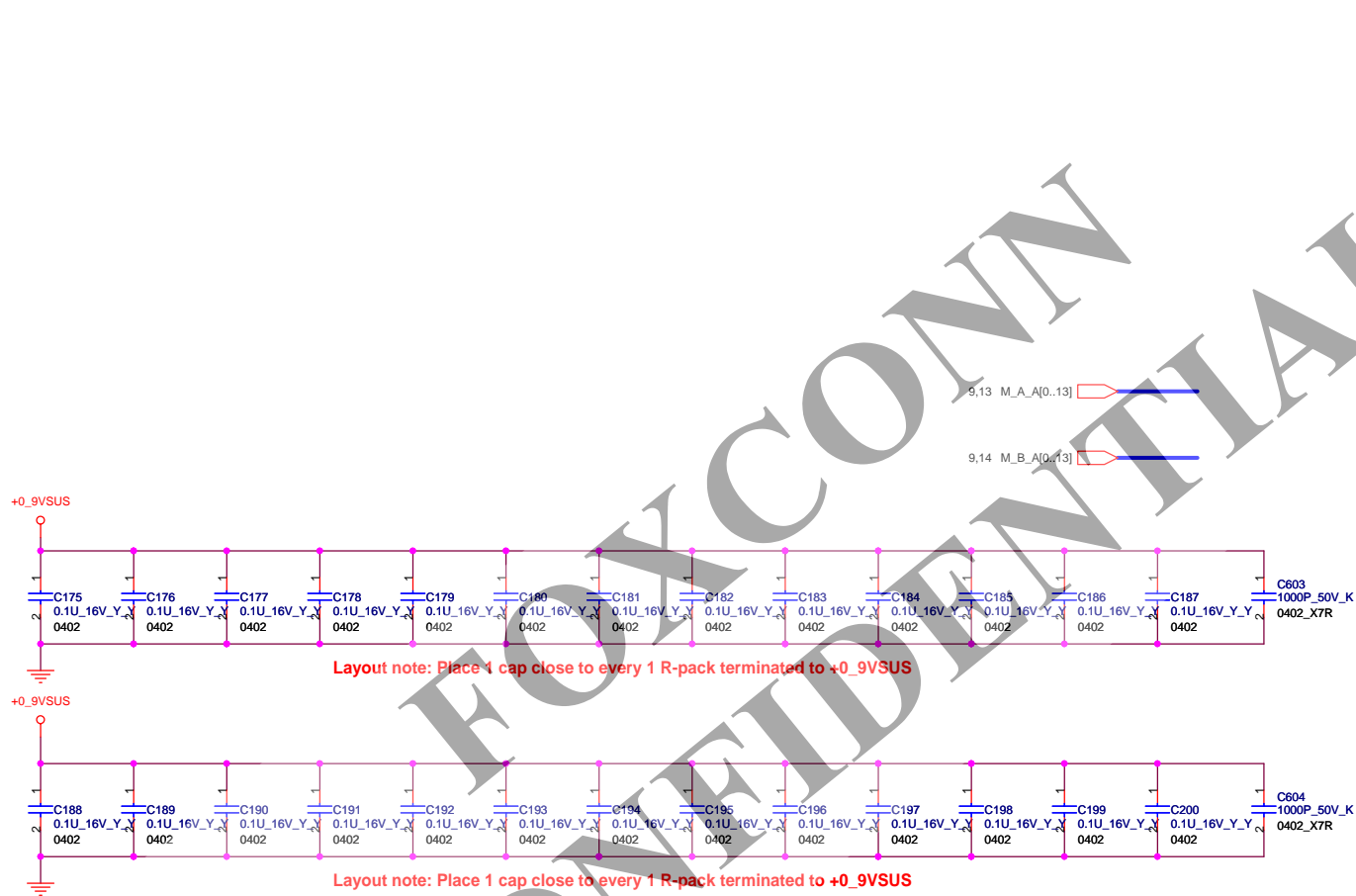
1.8V per DIMM=3.08A



FOX\_AS0A426\_N4SC\_4F  
DIMM\_1  
SMBus Address: A4(W)/A5(R)  
DIMM\_1 is placed farther from the GMCH than DIMM\_0

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
File	DDR(I)SO-DIMM_1	
Size	Document Number	Rev
A3	MST2-1-01	0.1
Date:	Tuesday, December 05, 2006	Sheet 14 of 55

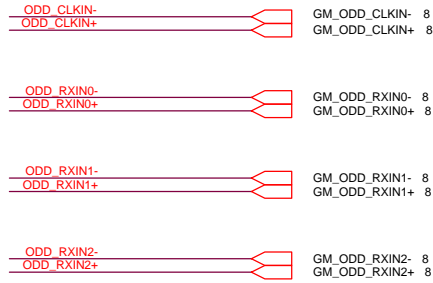
A  
B  
C  
D



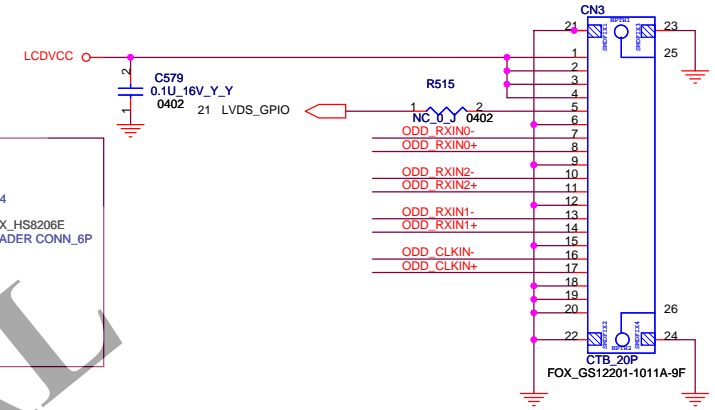
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# LVDS

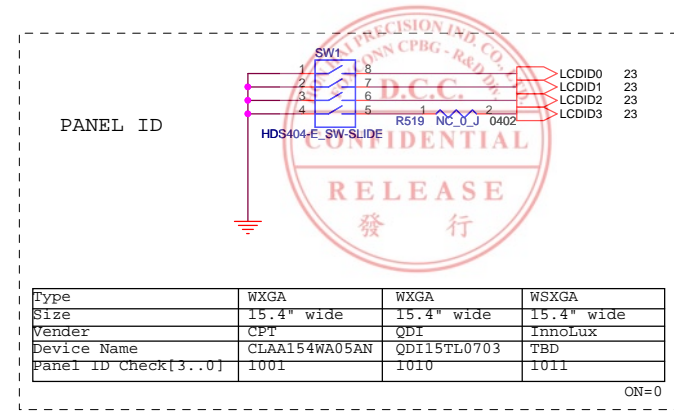
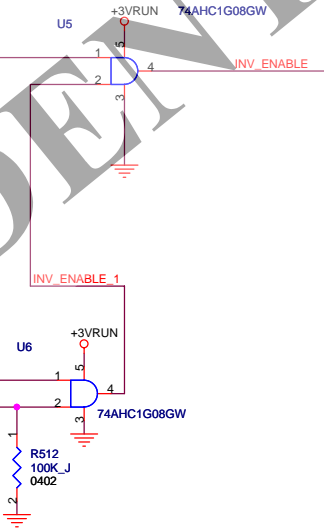


# LVDS CONNECTOR

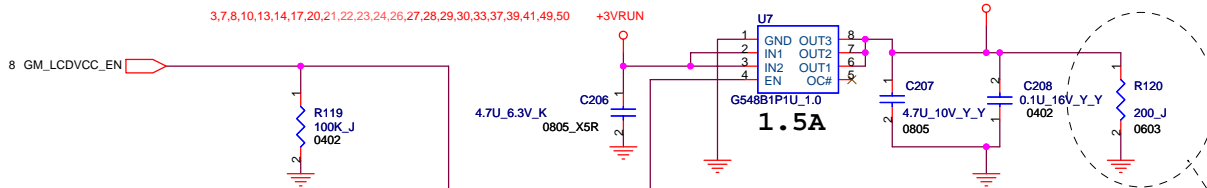


# INVERTER CONNECTOR

FOXC CONFIDENTIAL



Type	WXGA	WXGA	WSXGA
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	CPT	QDI	InnoLux
Device Name	CLAA154WA05AN	QDI15TL0703	TBD
Panel ID Check[3..0]	1001	1010	1011

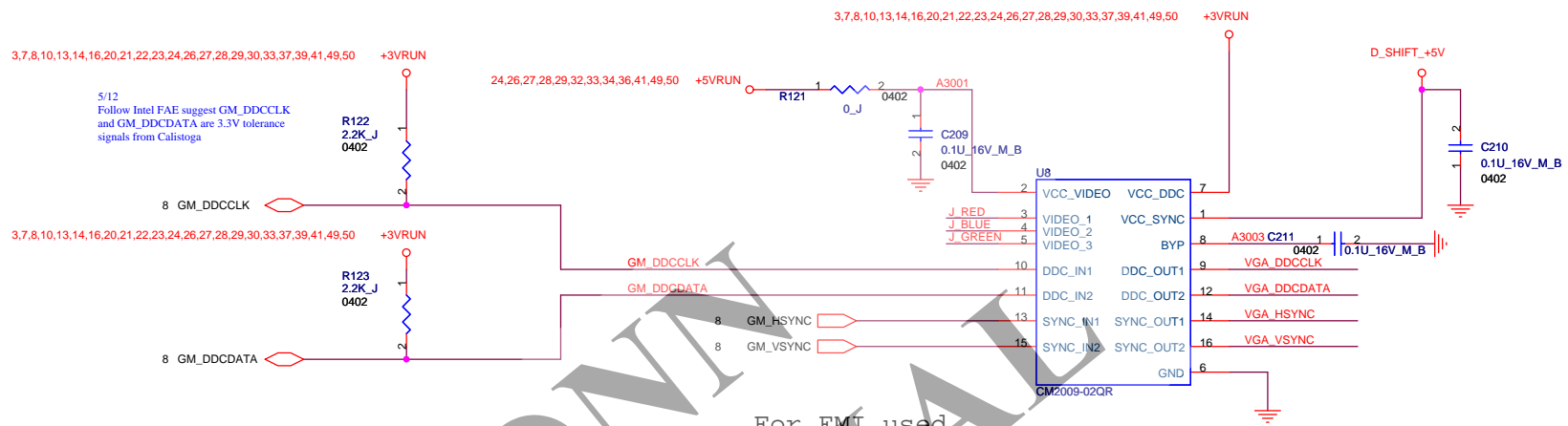


The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

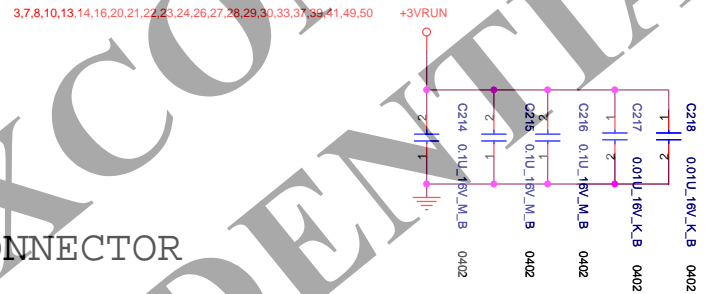
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **LVDS**

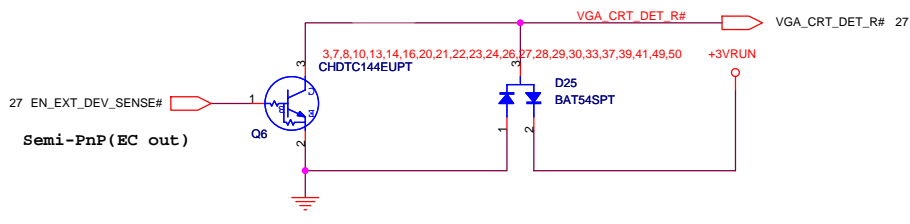
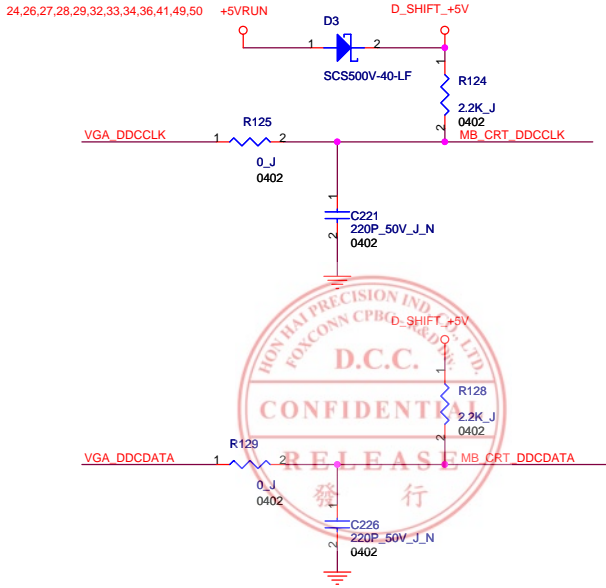
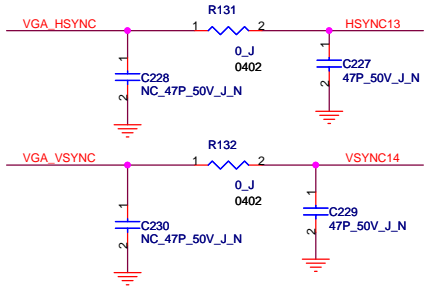
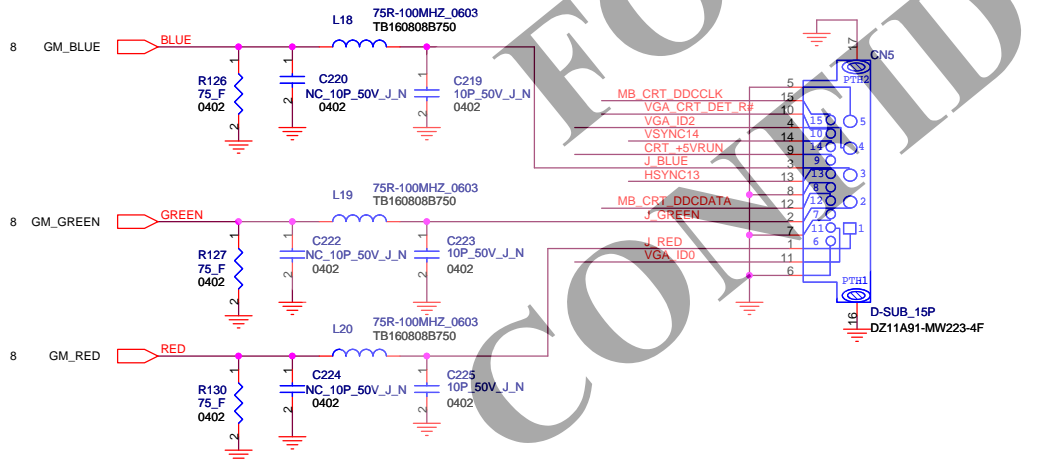
Size A3	Document Number MS72-1-01	Rev 0.1
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For EMI used

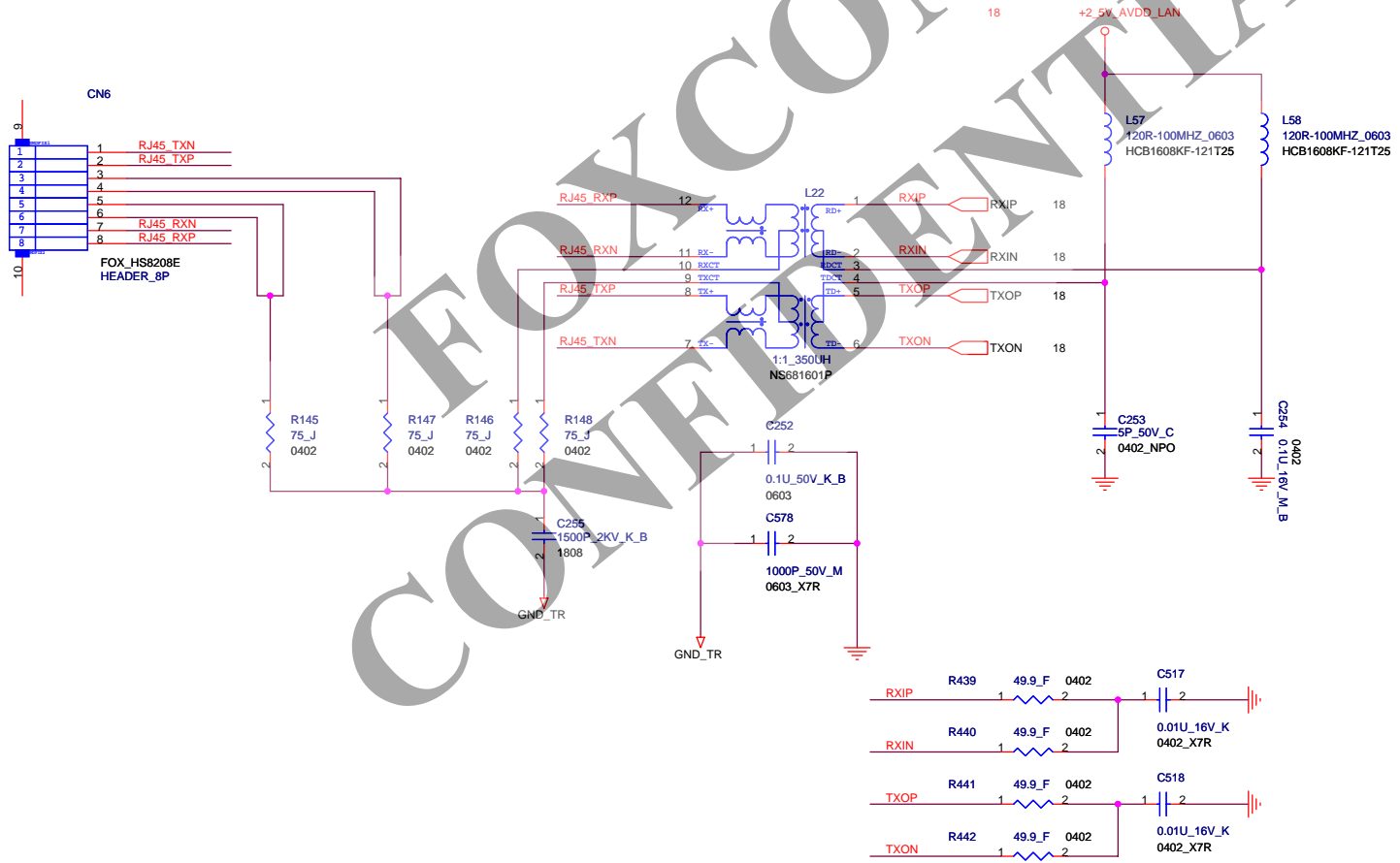


### CRT CONNECTOR



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
File	CRT	
Size	Document Number	Rev
A3	MS72-1-01	0.1
Date:	Tuesday, December 05, 2006	Sheet 17 of 55





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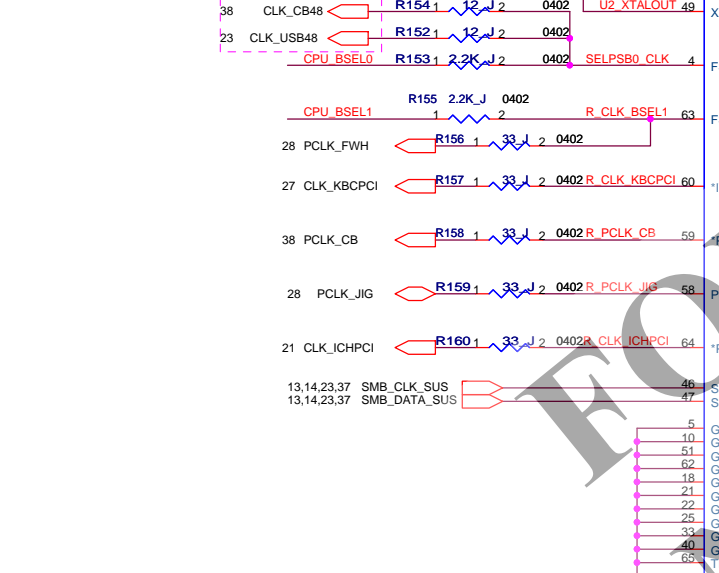


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>LAN Transformer</b>		CCPBG - R&D Division	
Size A3	Document Number MS72-1-01	Rev 0.1	
Date: Tuesday, December 05, 2006	Sheet 19	of 55	

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	C256 0402
NC_10P_50V_E_N	2	1	C257 0402
NC_10P_50V_E_N	2	1	C258 0402
NC_10P_50V_E_N	2	1	C265 0402
NC_10P_50V_E_N	2	1	C266 0402
NC_10P_50V_E_N	2	1	C267 0402
NC_10P_50V_E_N	2	1	C268 0402
NC_10P_50V_E_N	2	1	C271 0402

close to clk gen (For EMI)

Length as short as possible.



ICH7 DMI

06/17  
CLK\_PCIE\_ICH changed to SRCLK7  
CLK\_DOCK\_LAN changed to SRCLK8  
SW Note: datasheet page13 Byte8.1 => SRCLK7 should be configured as "Not Controlled"

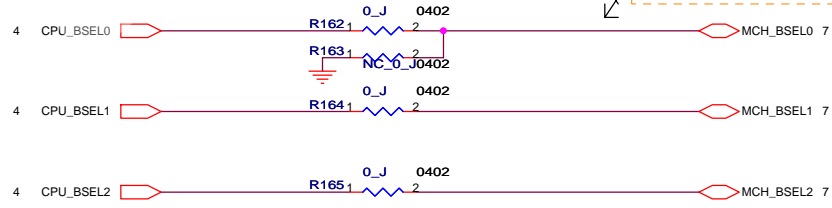
SM bus Address: 96S9LP321BKLF  
1101001 (ICH7)  
For clock generator

06/09  
DEL pull-up resistor R80~82  
pull-down resistor R85,R88  
del R84,R87,R90

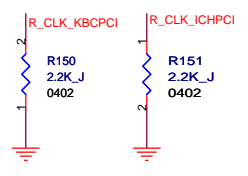
06/16  
ICS have recognized, FSLA/FSLB setting is different from CK410M spec. But MS10 will not use 100MHz, For test purpose, please move R91 from MCH\_BSEL2 to MCH\_BSEL0, and mount R89.

FSB Frequency Table:

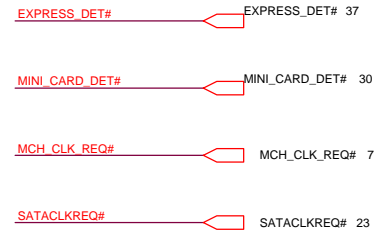
FSLB	FSLA	CPU SRC[7:0]	PCI	
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33



Pin Straps	
pin 53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin 59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin 60	pin 37/38
0	SRCLK8 (v)
1	CPU 2 ITP
pin 64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCCLK1 (NV)



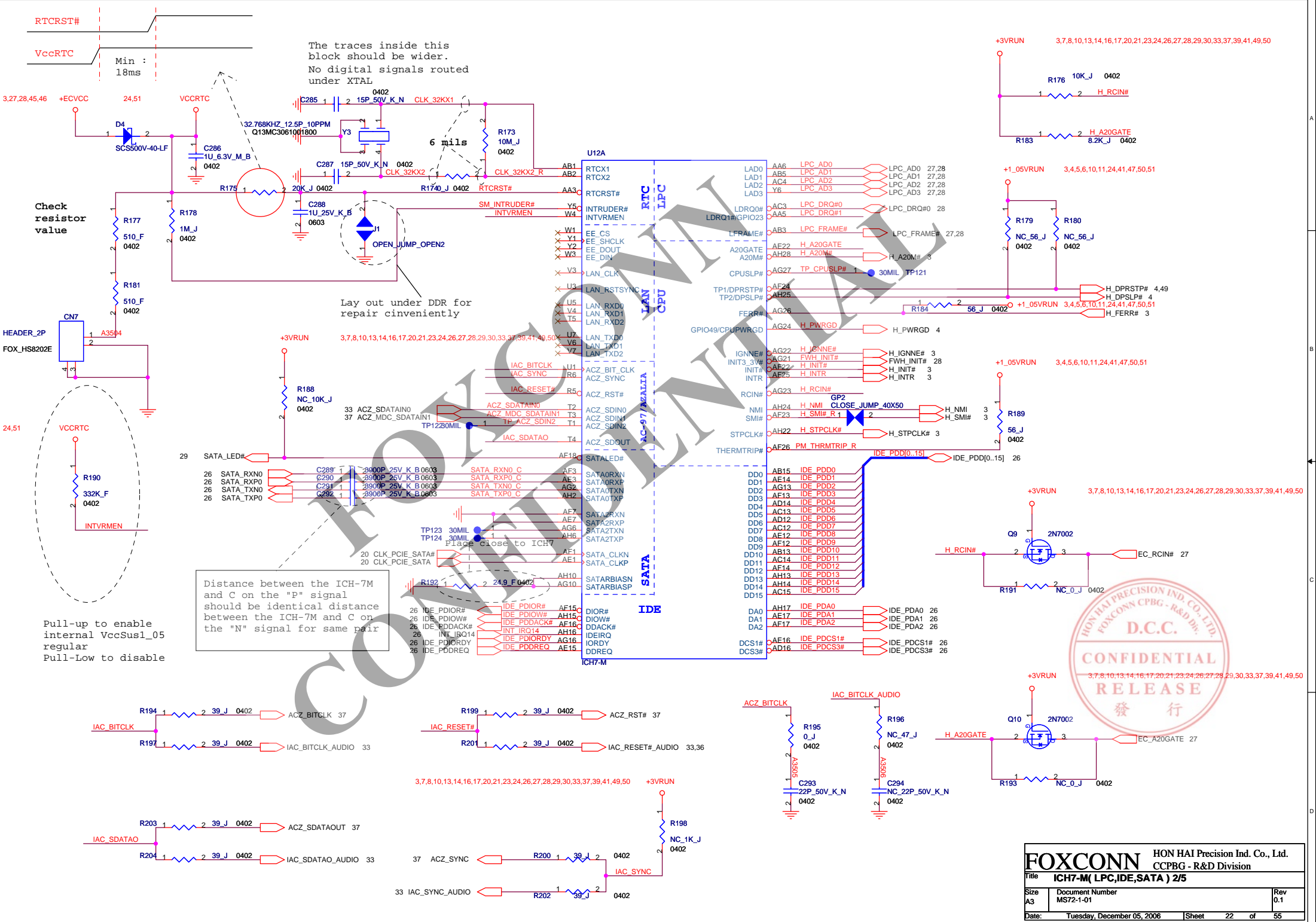
06/16  
pin53/59/60/64 with internal pull-up resistor  
No Stuff Pull-up Resistor



06/09  
CLKREQ with internal pull-up resistor  
No Stuff Pull-up Resistor







The traces inside this block should be wider.  
No digital signals routed under XTAL

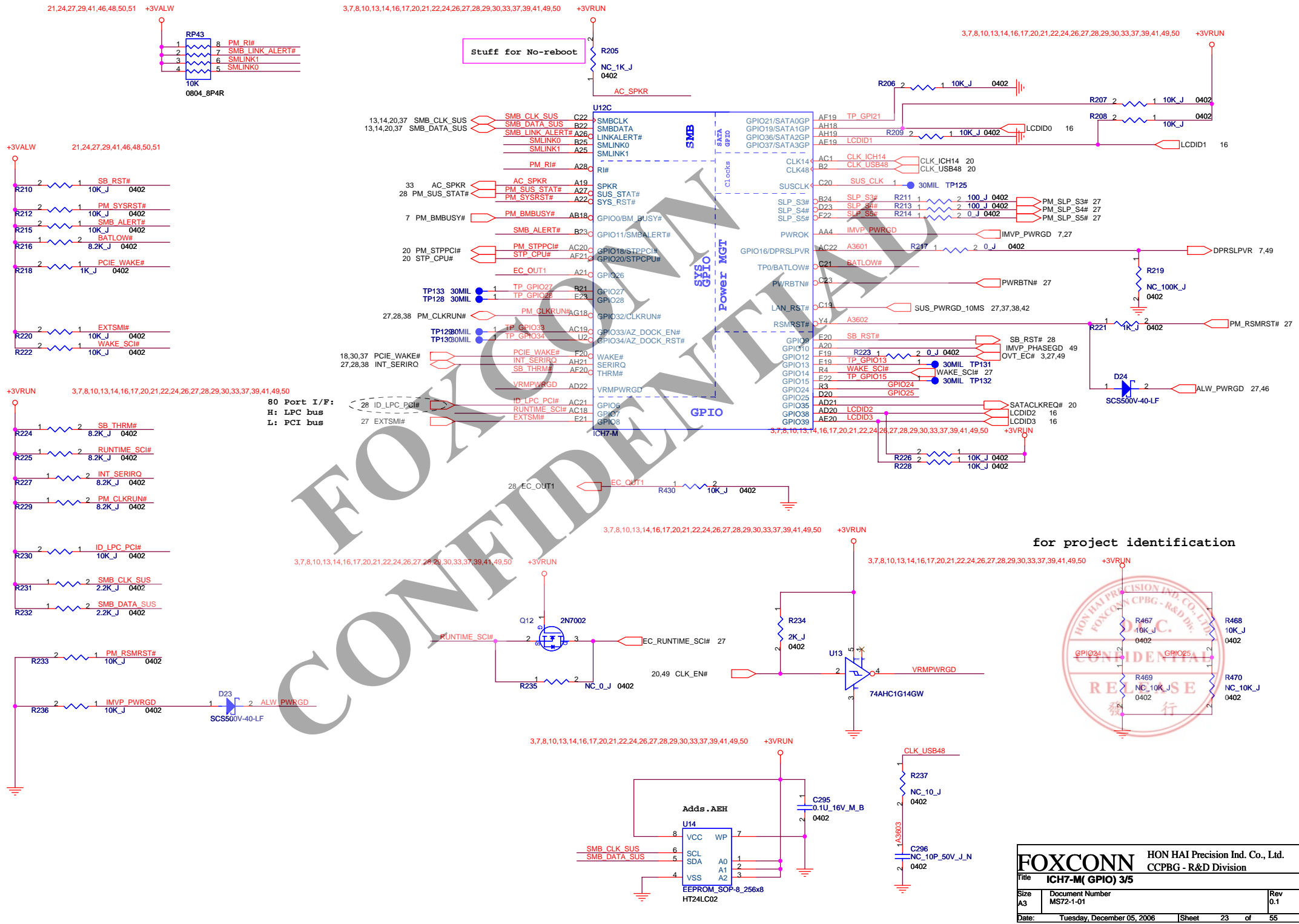
Check resistor value

Lay out under DDR for repair conveniently

Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

Pull-up to enable internal VccSus1\_05 regular  
Pull-Low to disable





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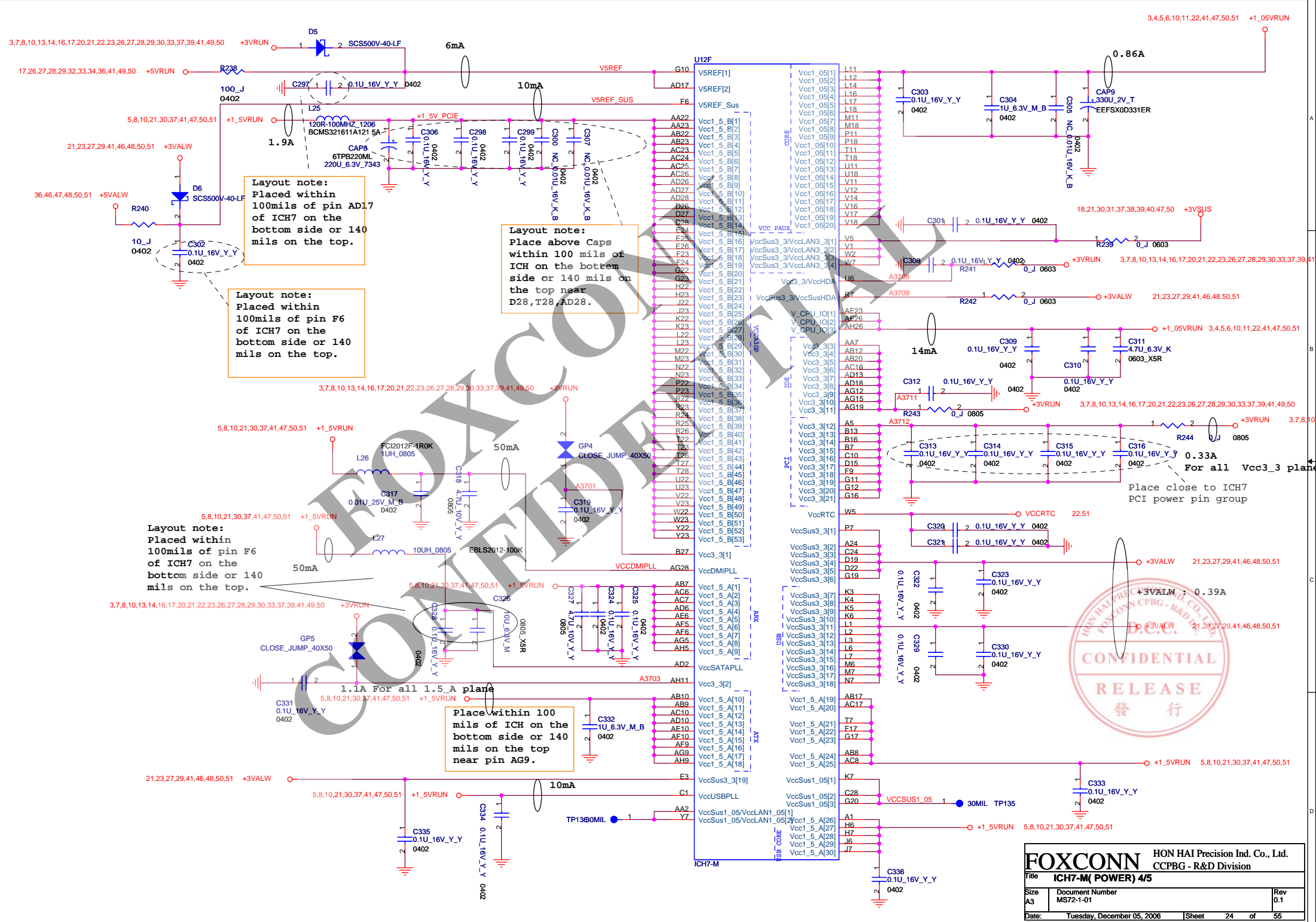
for project identification

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RELEASE

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		ICHT7-M (GPIO) 3/5	
Size	Document Number	Date	Rev
A3	MS72-1-01	Tuesday, December 05, 2006	0.1
Date:		Sheet	23 of 55





**Layout note:**  
Placed within 100mils of pin AD1.7 of ICH7 on the bottom side or 140 mils on the top.

**Layout note:**  
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

**Layout note:**  
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

**Layout note:**  
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

**Layout note:**  
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

For all Vcc3\_3 plane  
Place close to ICH7 PCI power pin group



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
Title <b>ICH7-M (POWER) 4/5</b>		
Size A3	Document Number MS72-1-01	Rev 0.1
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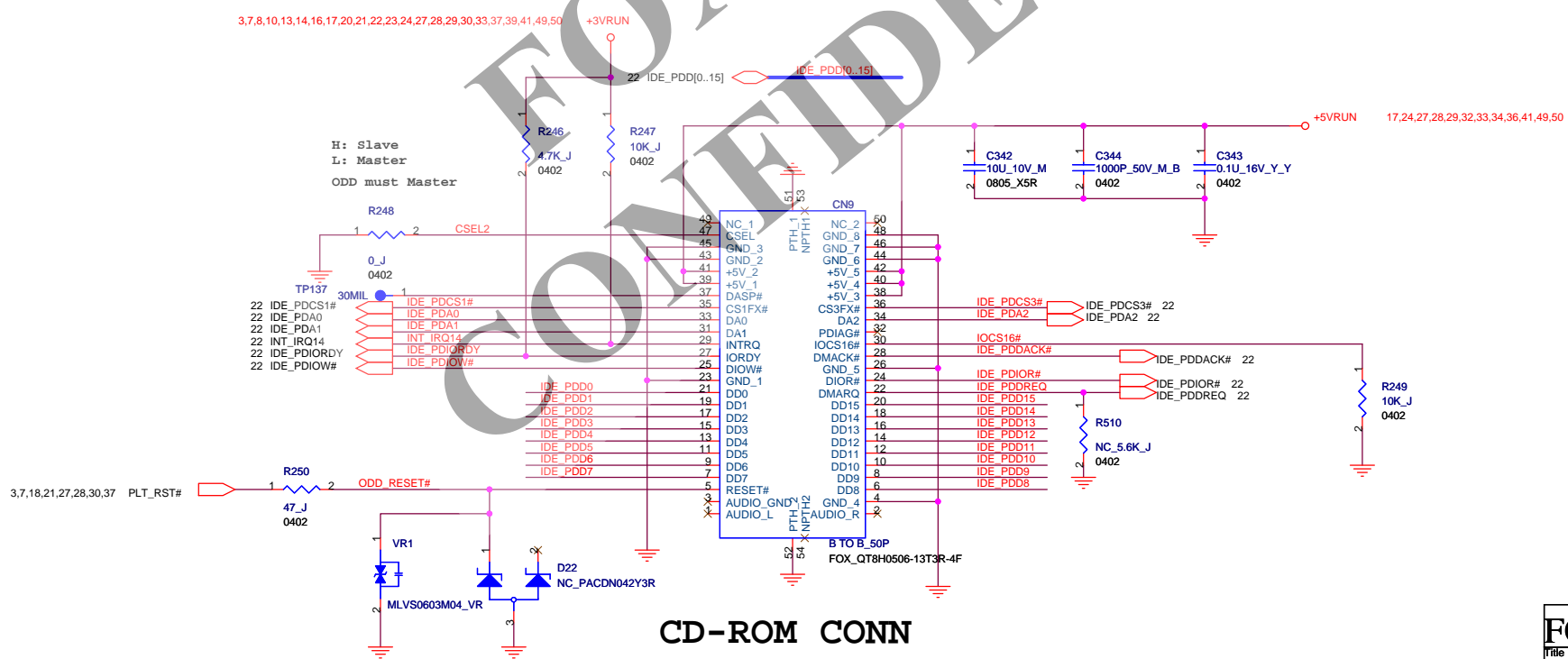
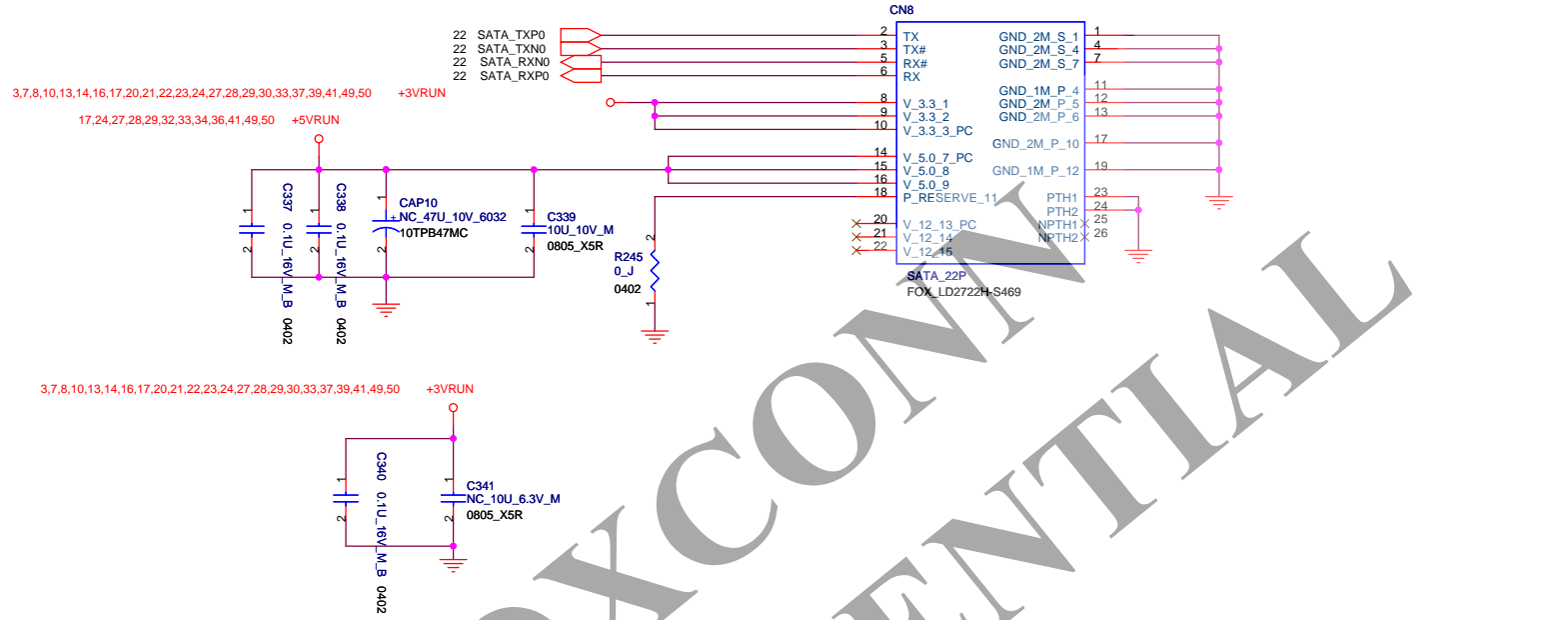
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U12E			P28		
A4	VSS11	VSS108	P28		
A23	VSS12	VSS109	R1		
B1	VSS13	VSS100	R11		
B8	VSS14	VSS101	R12		
B11	VSS15	VSS102	R13		
B14	VSS16	VSS103	R14		
B17	VSS17	VSS104	R15		
B20	VSS18	VSS105	R16		
B26	VSS19	VSS106	R17		
B28	VSS10	VSS107	R18		
C2	VSS11	VSS108	T6		
C6	VSS12	VSS109	T12		
C27	VSS13	VSS110	T13		
D10	VSS14	VSS111	T14		
D13	VSS15	VSS112	T15		
D18	VSS16	VSS113	T16		
D21	VSS17	VSS114	T17		
D24	VSS18	VSS115	U4		
E1	VSS19	VSS116	U12		
E2	VSS20	VSS117	U13		
E4	VSS21	VSS118	U14		
E8	VSS22	VSS119	U15		
E16	VSS23	VSS120	U16		
F3	VSS24	VSS121	U17		
F4	VSS25	VSS122	U22		
F5	VSS26	VSS123	U25		
F12	VSS27	VSS124	U26		
F27	VSS28	VSS125	V2		
F28	VSS29	VSS126	V13		
G1	VSS30	VSS127	V15		
G2	VSS31	VSS128	V24		
G5	VSS32	VSS129	V27		
G6	VSS33	VSS130	V28		
G9	VSS34	VSS131	W6		
G14	VSS35	VSS132	W24		
G18	VSS36	VSS133	W25		
G21	VSS37	VSS134	W26		
G24	VSS38	VSS135	Y3		
G25	VSS39	VSS136	Y24		
G26	VSS40	VSS137	Y27		
H3	VSS41	VSS138	Y28		
H4	VSS42	VSS139	AA1		
H5	VSS43	VSS140	AA24		
H24	VSS44	VSS141	AA25		
H27	VSS45	VSS142	AA26		
H28	VSS46	VSS143	AB4		
J1	VSS47	VSS144	AB6		
J2	VSS48	VSS145	AB11		
J5	VSS49	VSS146	AB14		
J24	VSS50	VSS147	AB16		
J25	VSS51	VSS148	AB19		
J26	VSS52	VSS149	AB21		
K24	VSS53	VSS150	AB24		
K27	VSS54	VSS151	AB27		
K28	VSS55	VSS152	AB28		
L13	VSS56	VSS153	AC2		
L15	VSS57	VSS154	AC5		
L24	VSS58	VSS155	AC9		
L25	VSS59	VSS156	AC11		
L26	VSS60	VSS157	AD1		
M3	VSS61	VSS158	AD3		
M4	VSS62	VSS159	AD4		
M5	VSS63	VSS160	AD7		
M12	VSS64	VSS161	AD8		
M13	VSS65	VSS162	AD11		
M14	VSS66	VSS163	AD15		
M15	VSS67	VSS164	AD19		
M16	VSS68	VSS165	AD23		
M17	VSS69	VSS166	AE2		
M24	VSS70	VSS167	AE4		
M27	VSS71	VSS168	AE8		
M28	VSS72	VSS169	AE11		
N1	VSS73	VSS170	AE13		
N2	VSS74	VSS171	AE18		
N5	VSS75	VSS172	AE21		
N6	VSS76	VSS173	AE24		
N11	VSS77	VSS174	AE25		
N12	VSS78	VSS175	AE2		
N13	VSS79	VSS176	AF4		
N14	VSS80	VSS177	AF8		
N15	VSS81	VSS178	AF11		
N16	VSS82	VSS179	AF27		
N17	VSS83	VSS180	AF28		
N18	VSS84	VSS181	AG1		
N24	VSS85	VSS182	AG3		
N25	VSS86	VSS183	AG7		
N26	VSS87	VSS184	AG11		
P3	VSS88	VSS185	AG14		
P4	VSS89	VSS186	AG17		
P12	VSS90	VSS187	AG20		
P13	VSS91	VSS188	AG25		
P14	VSS92	VSS189	AH1		
P15	VSS93	VSS190	AH3		
P16	VSS94	VSS191	AH7		
P17	VSS95	VSS192	AH12		
P24	VSS96	VSS193	AH23		
P27	VSS97	VSS194	AH27		



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CCPBG - R&D Division		
Title <b>ICH7-M( GND) 5/5</b>		
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# SATA HDD CONN

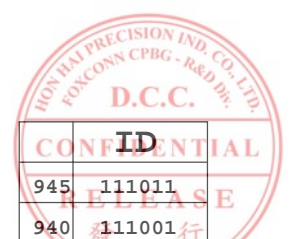
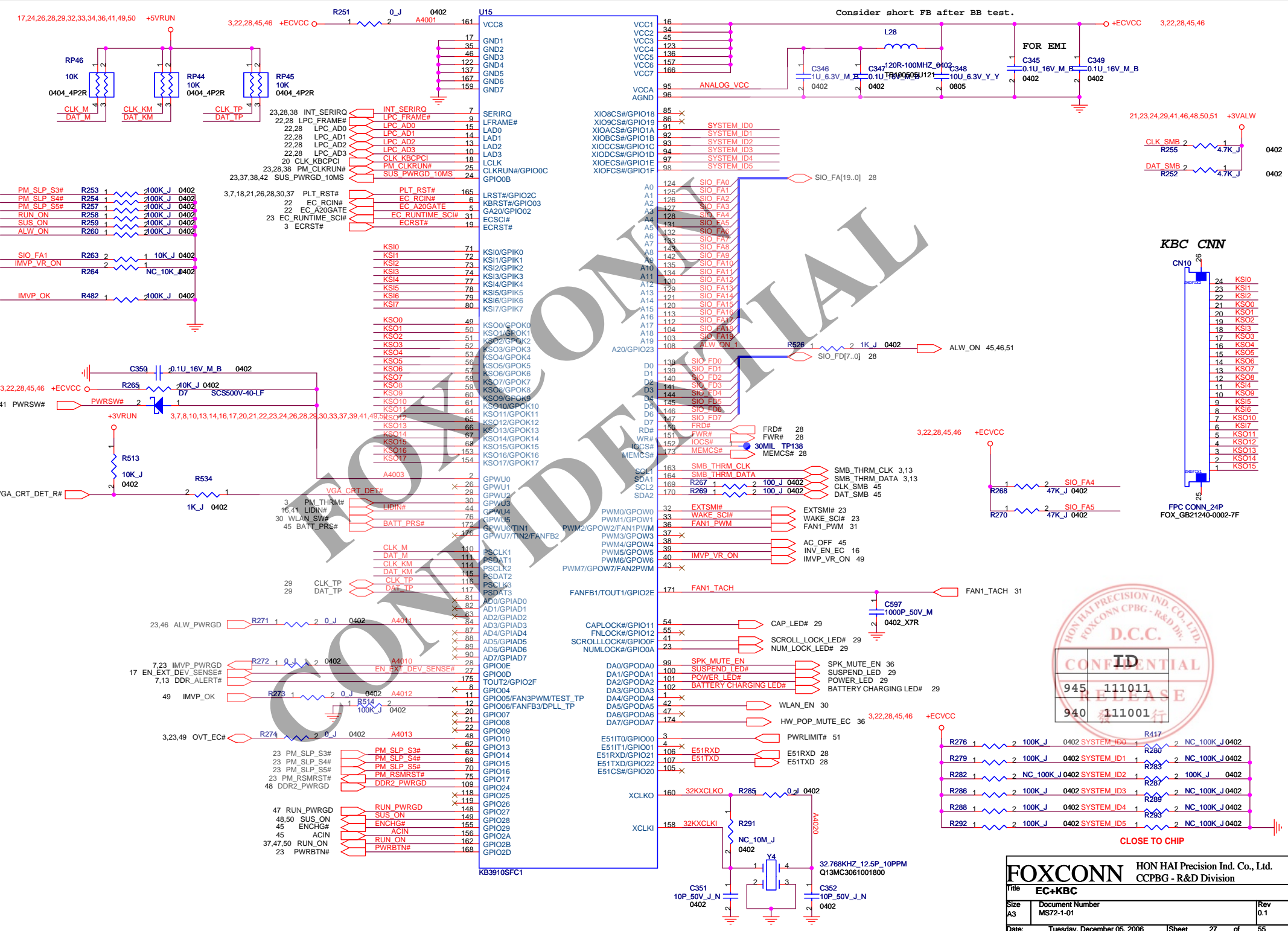


# CD-ROM CONN

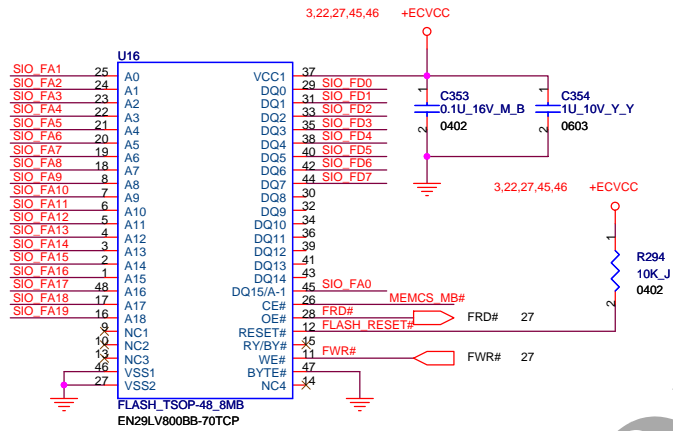
Follow Adoi san suggest ODD: Master/HDD:Slave



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>SATA HDD/CD-ROM</b>		
Size A3	Document Number MS72-1-01	Rev 0.1
Date: Tuesday, December 05, 2006	Sheet 26	of 55

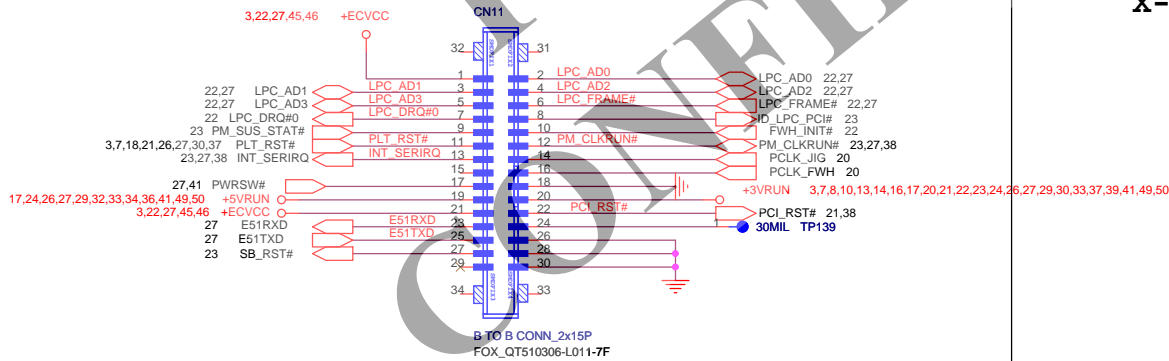


27 SIO\_FA[19..0]  
27 SIO\_FD[7..0]

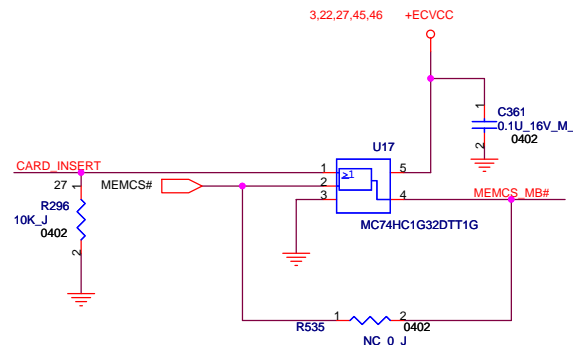
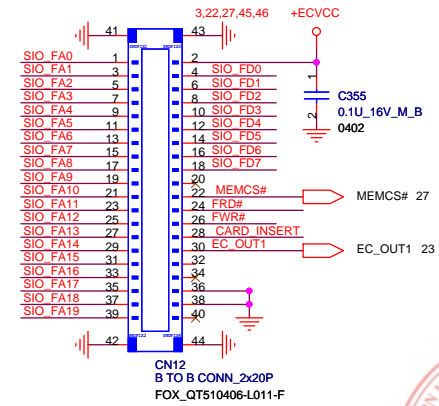


**FLASH BIOS**

**JIG-120**



**X-BUS**



# Touch Pad Board

# CAP\_LED#

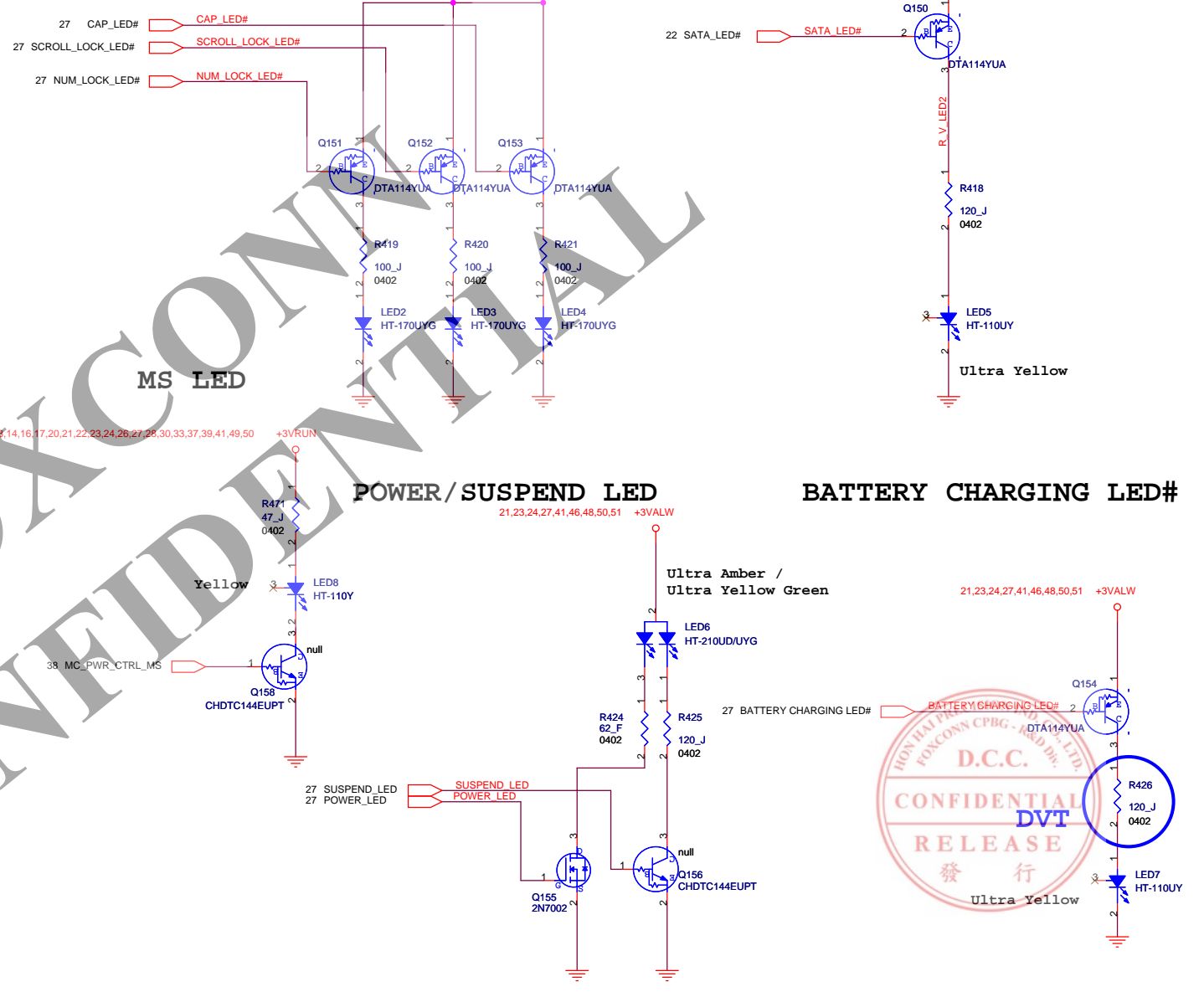
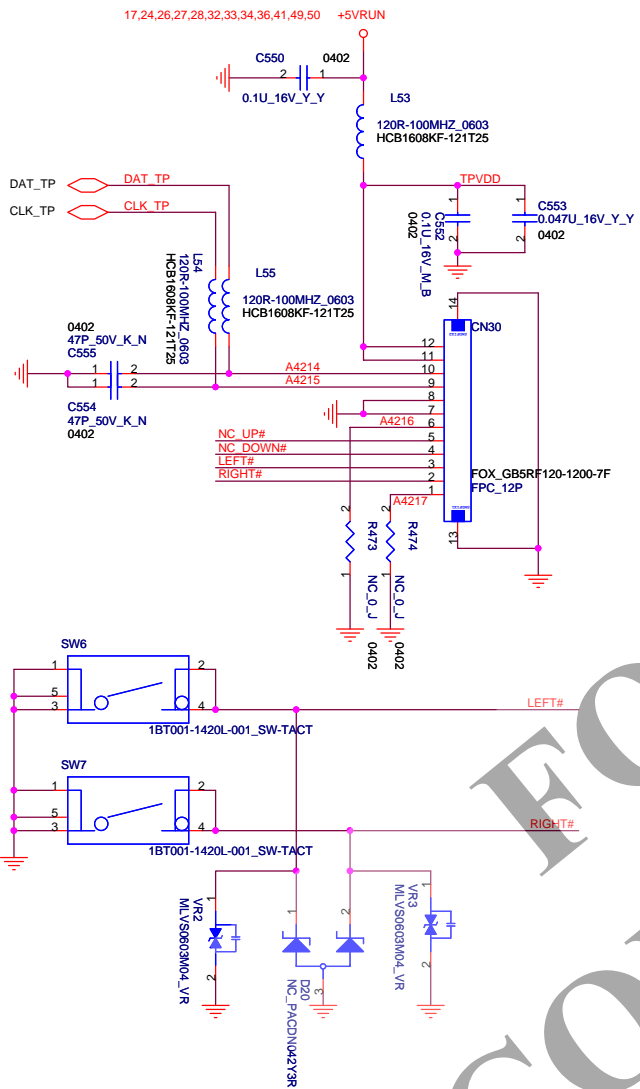
# SCROLL\_LOCK\_LED#

# NUM\_LOCK\_LED#

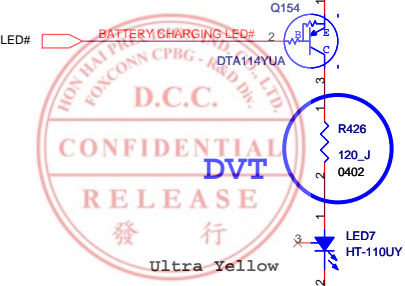
# HDD\_LED#

# POWER/SUSPEND LED

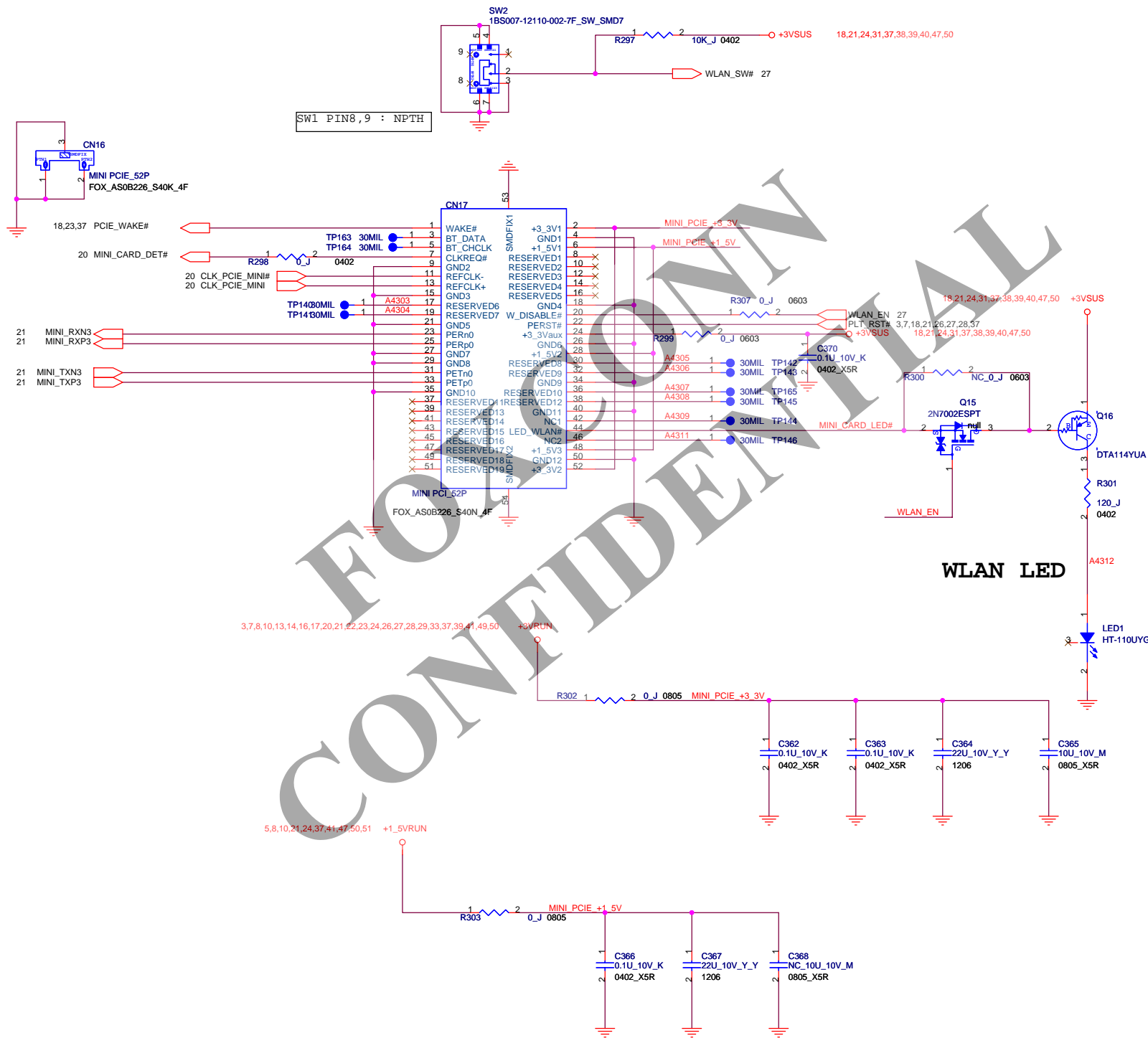
# BATTERY CHARGING LED#



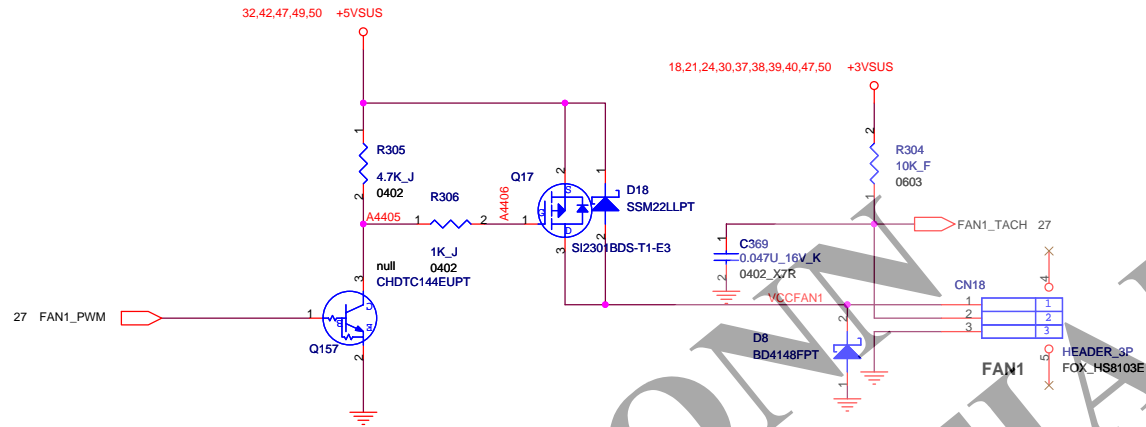
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Title <b>LED/Touch PAD</b>	
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# FAN1



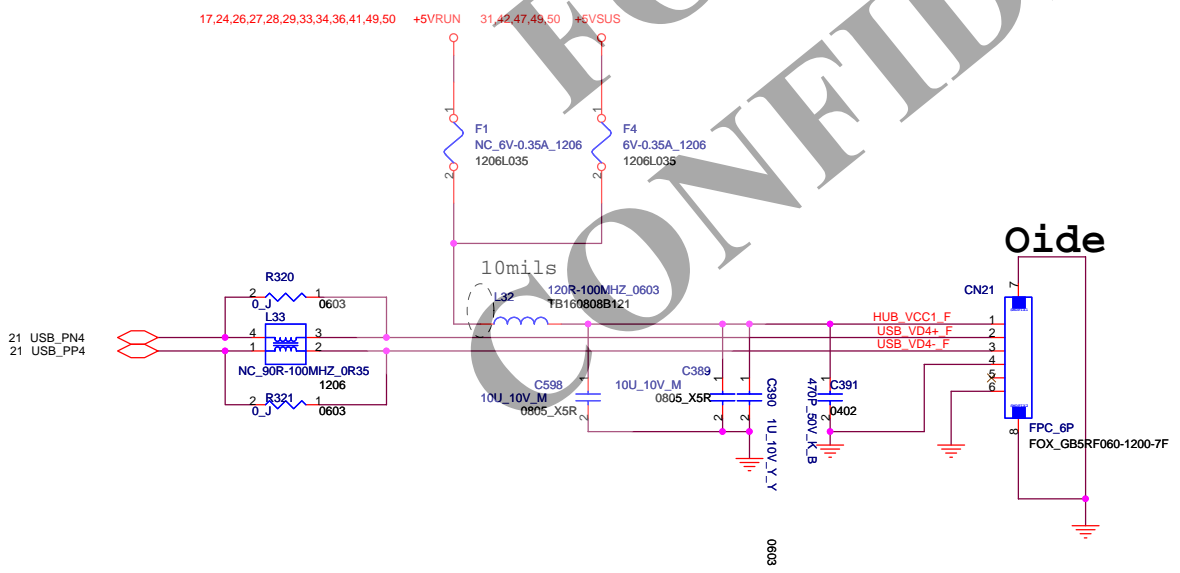
FOXCONN CONFIDENTIAL



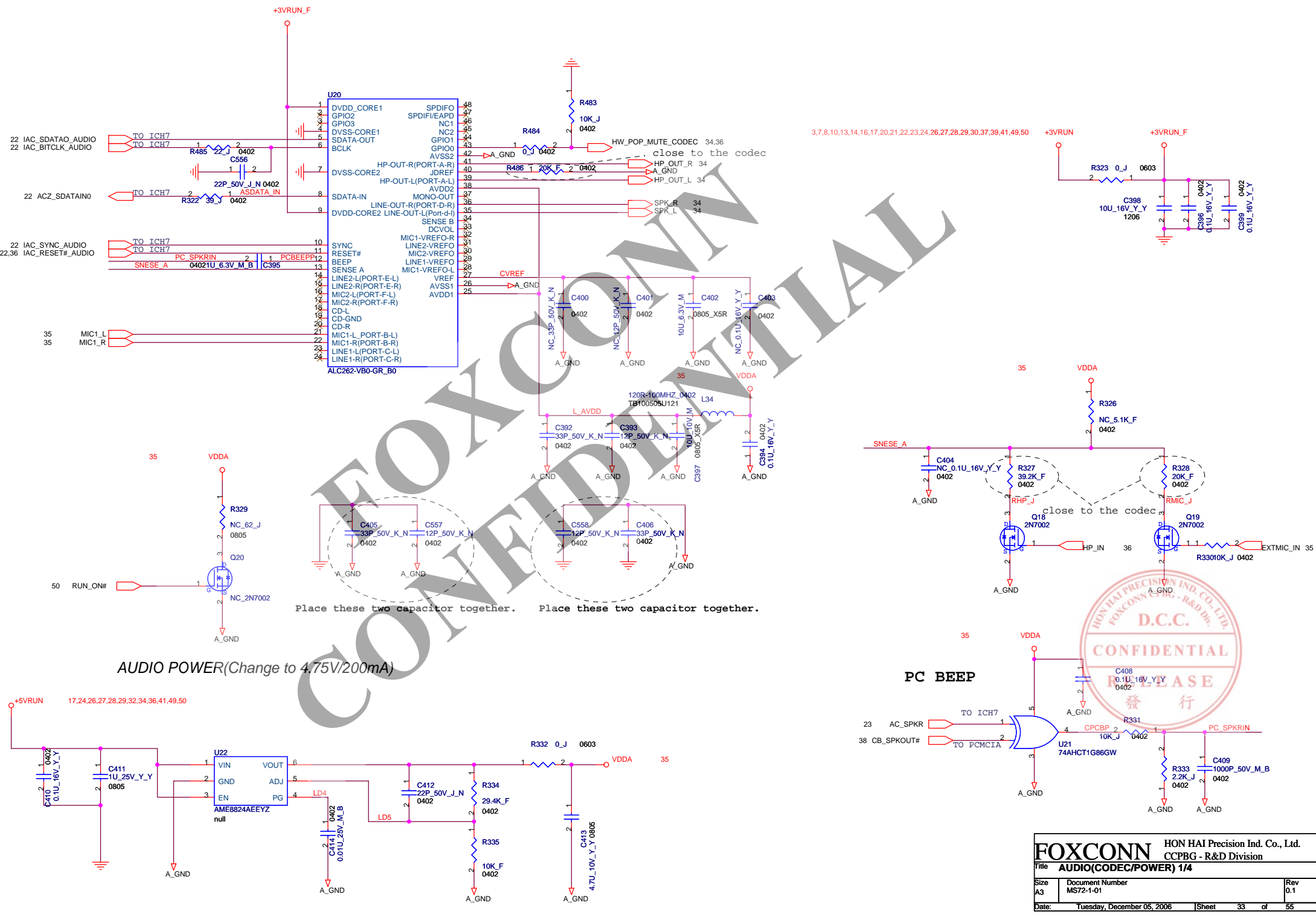
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>FAN</b>		CCPBG - R&D Division	
Size A3	Document Number MS72-1-01	Rev 0.1	
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Place these two capacitor together. Place these two capacitor together.

AUDIO POWER(Change to 4.75V/200mA)

PC BEEP

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HON HAI PRECISION IND. CO., LTD.  
FOXCONN (HONG KONG) R&D DIV.

**D.C.C.**

I N T E R N A T I O N A L  
發 行

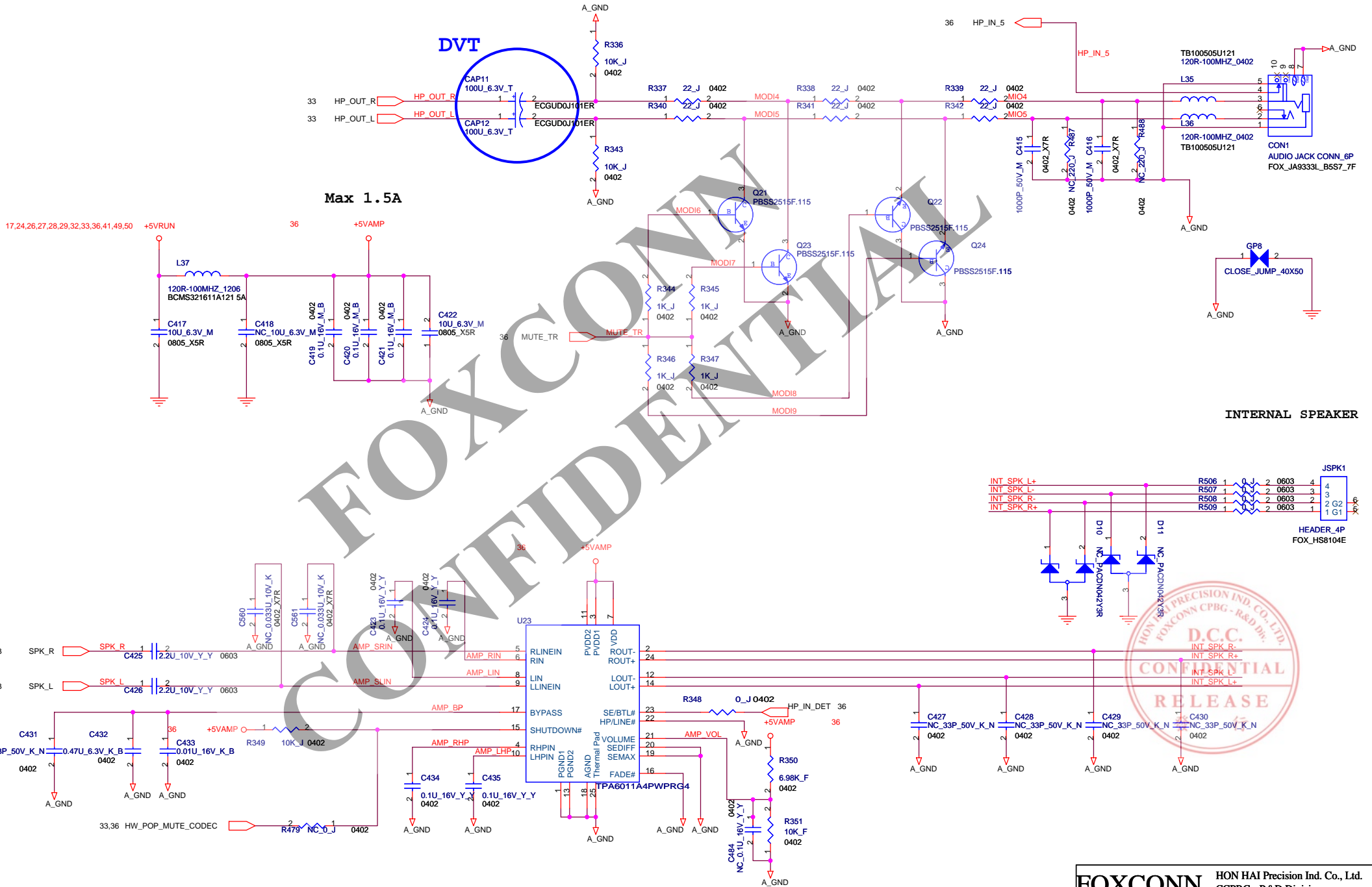
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CCPBG - R&D Division

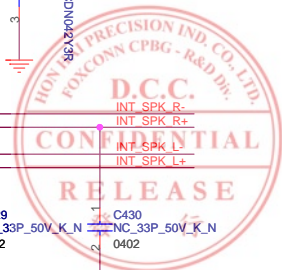
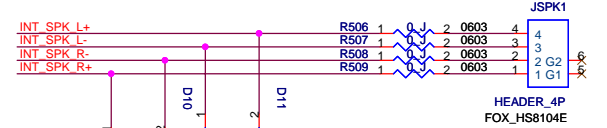
File	AUDIO(CODEC/POWER) 1/A	
Size	Document Number	Rev
A3	MS72-1-01	0.1
Date:	Tuesday, December 05, 2006	Sheet 33 of 55

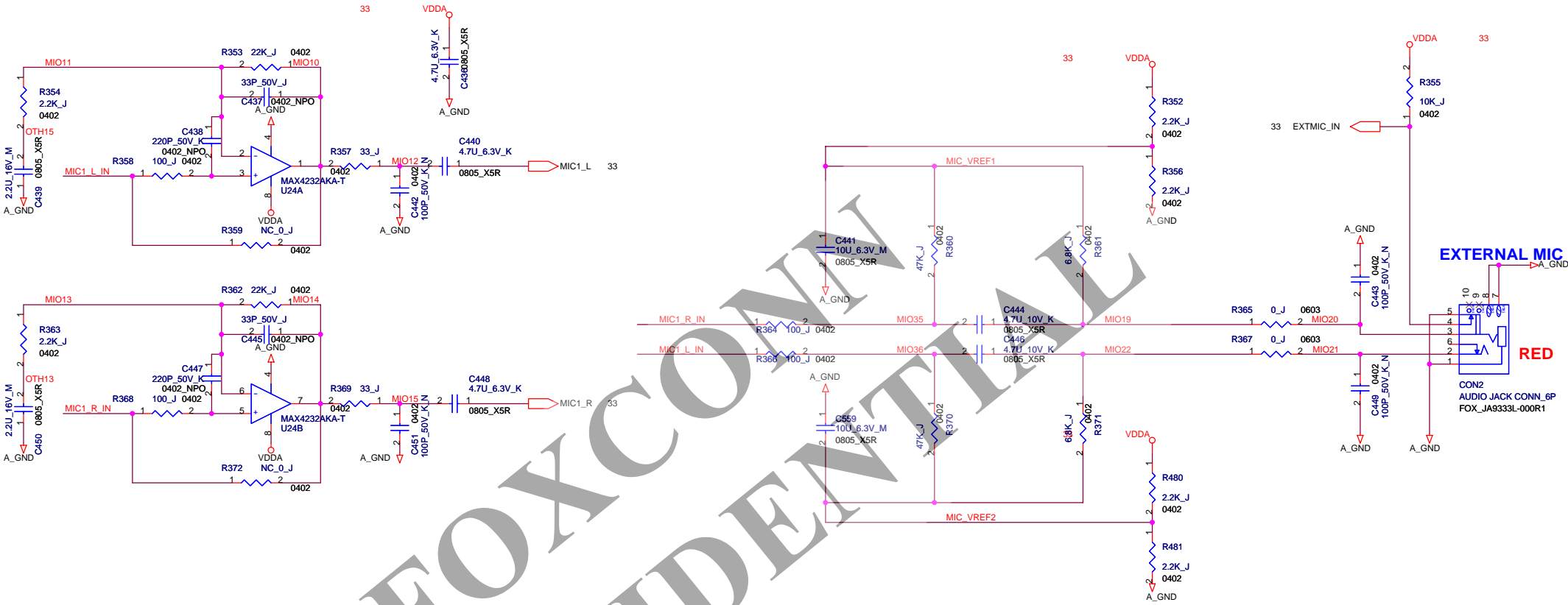
DVT

Max 1.5A



INTERNAL SPEAKER

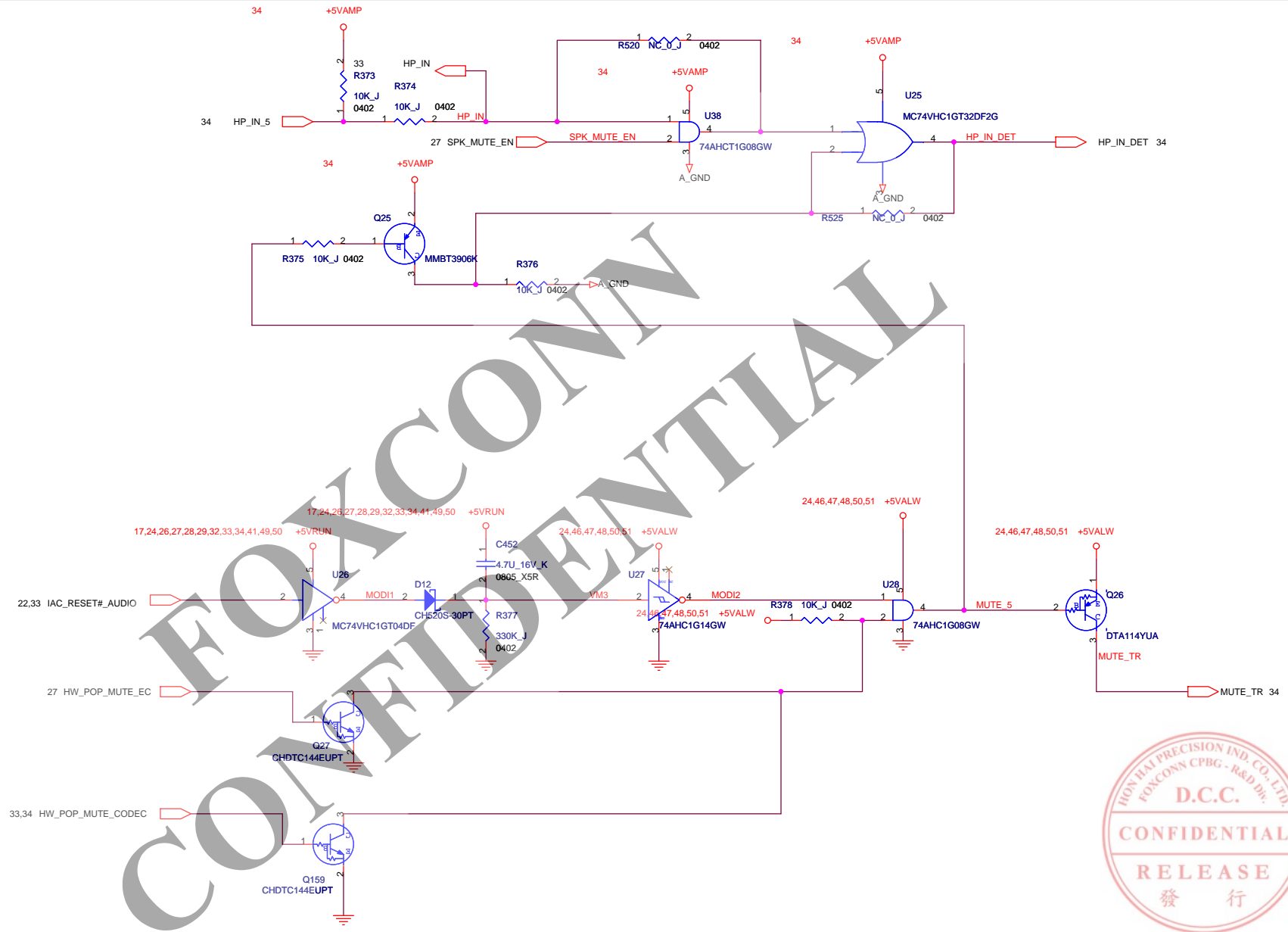




FOXC  
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<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title <b>AUDIO( EXT MIC) 3/4</b>		
Size A3	Document Number MS72-1-01	Rev 0.1
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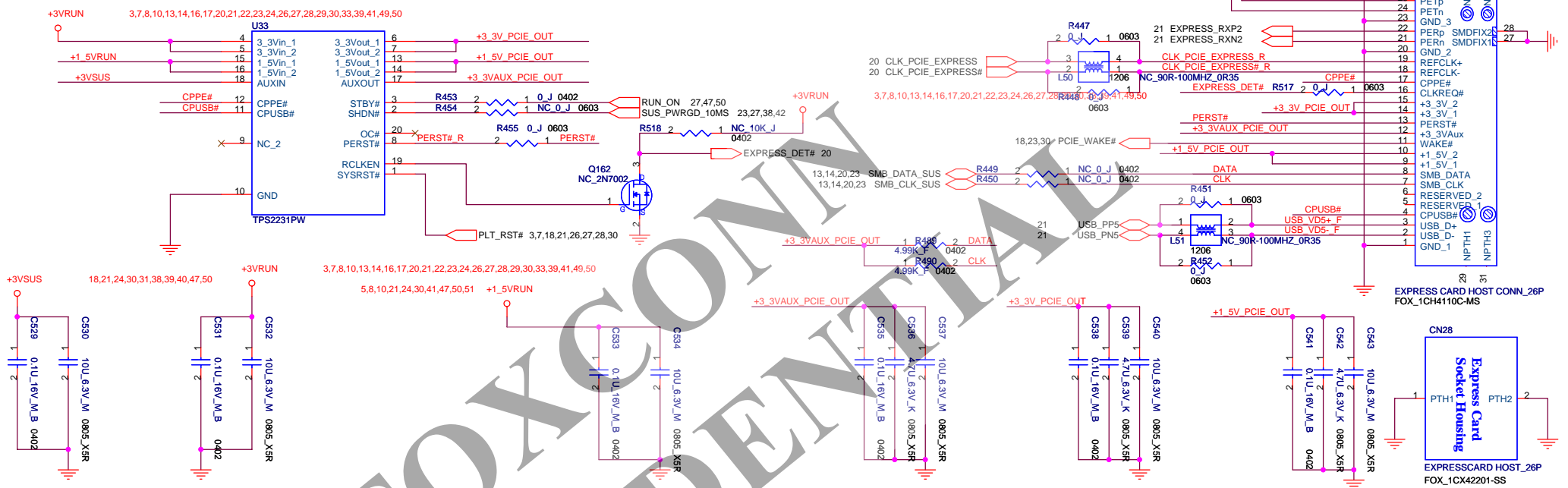


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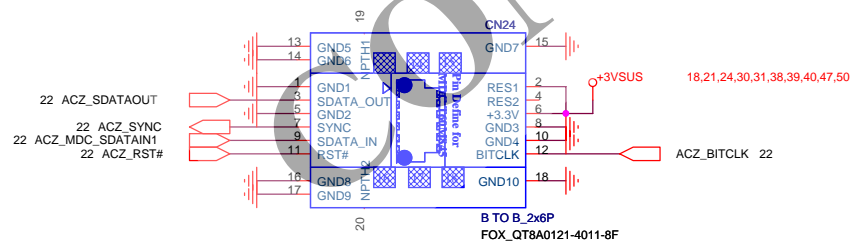


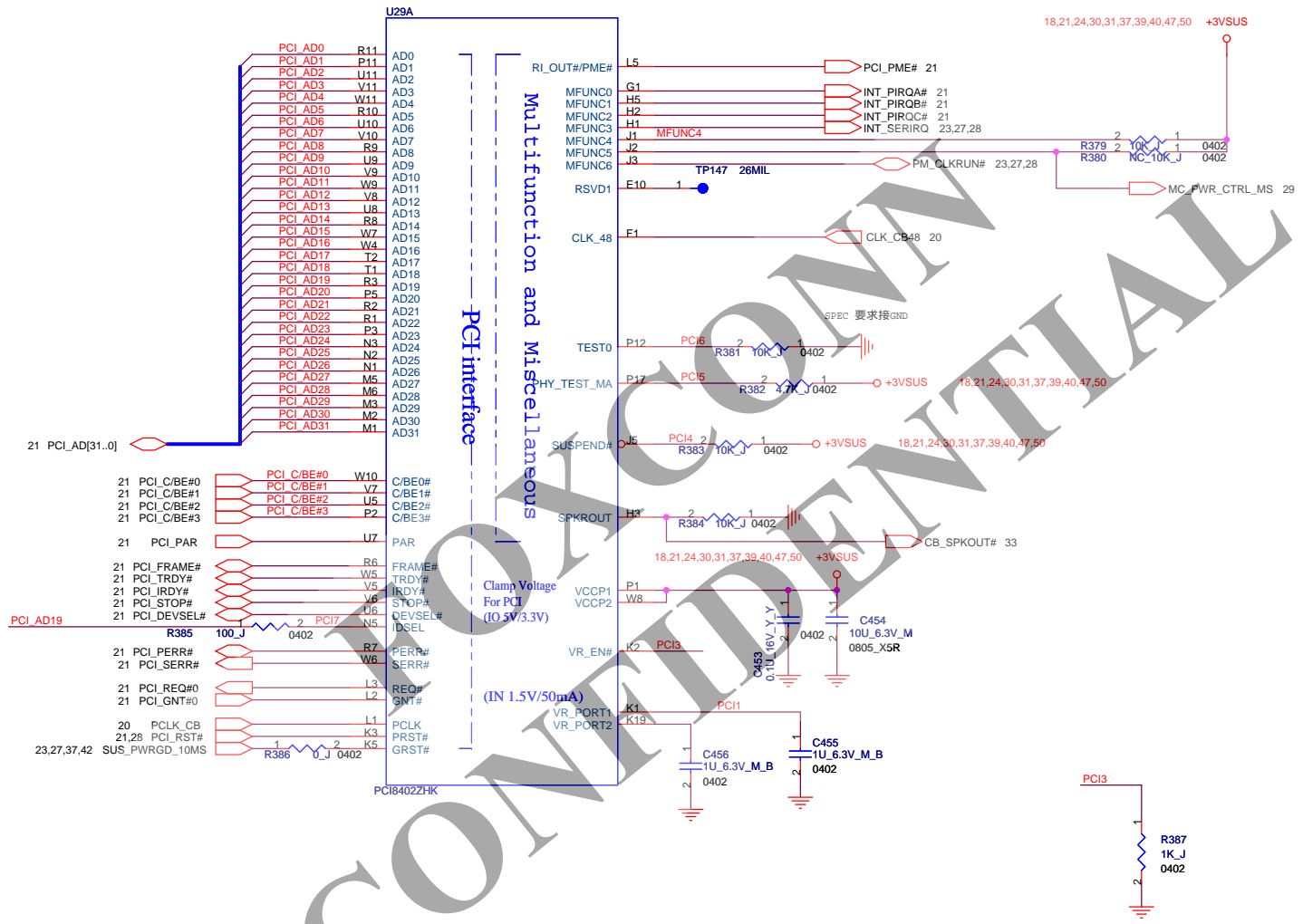
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Title <b>AUDIO (MUTE) 4/4</b>			
Size A3	Document Number MS72-1-01	Rev 0.1	
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# EXPRESS CONN

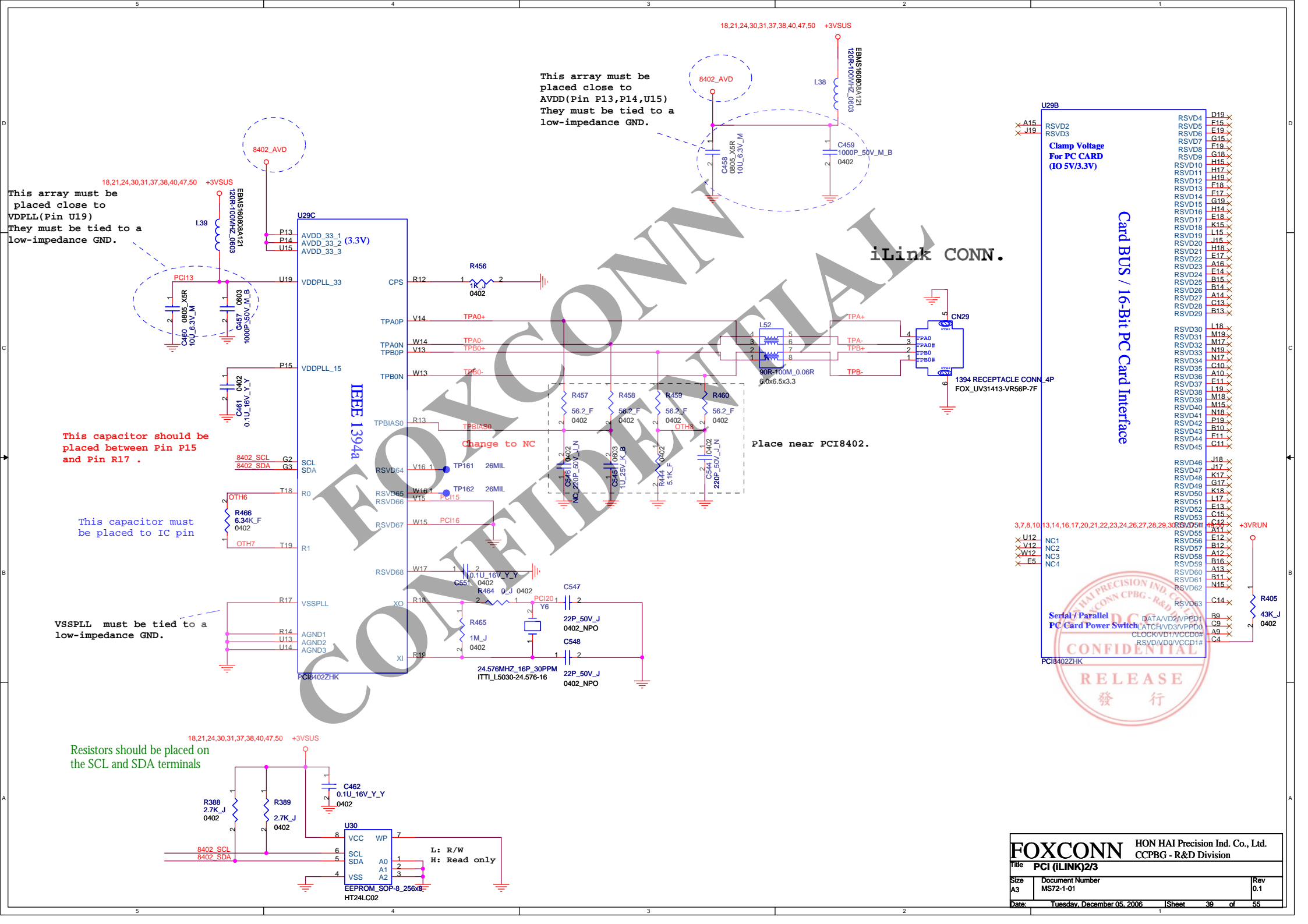


# MDC CONN.





<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
File <b>PCI (PCI BUS) 1/3</b>		CCPBG - R&D Division	
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This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.

This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

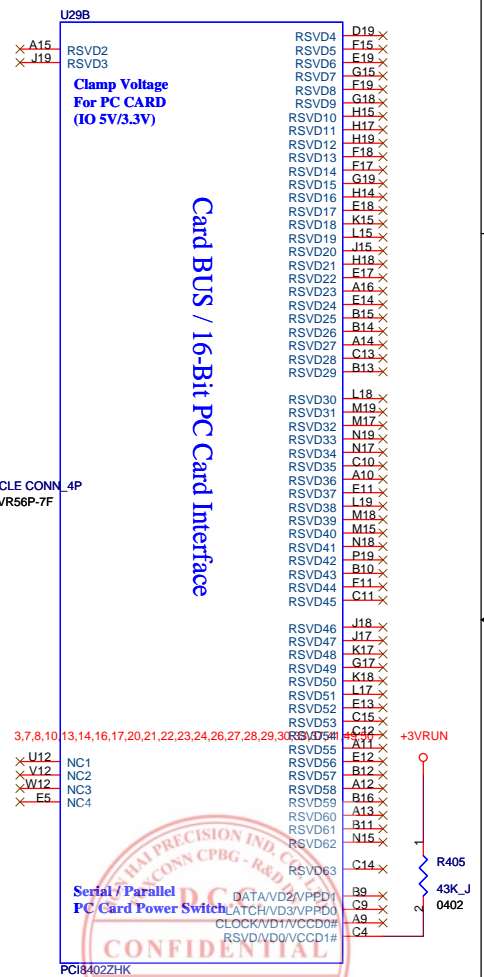
This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

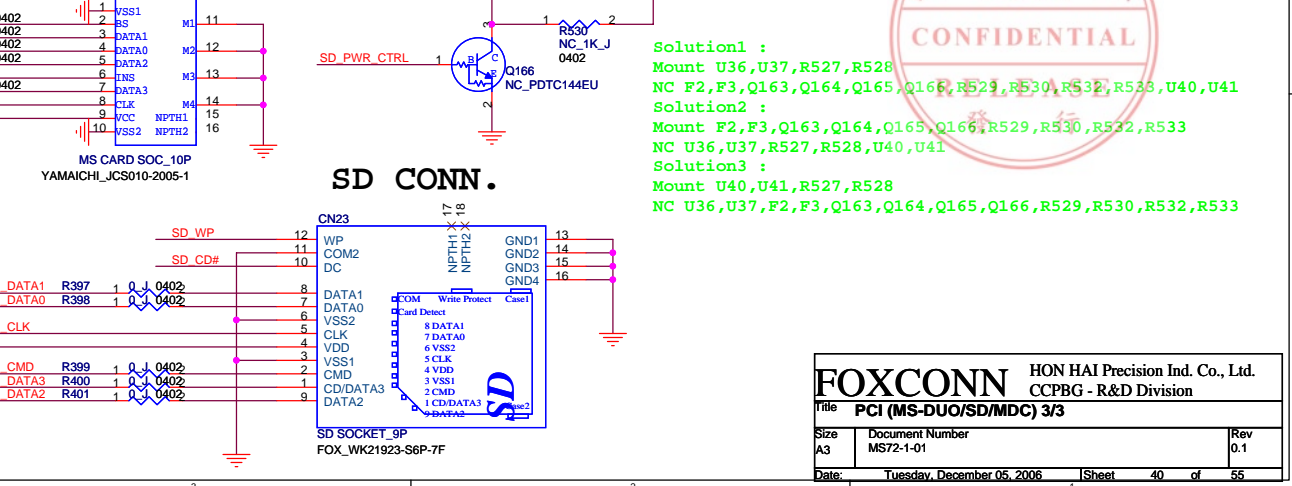
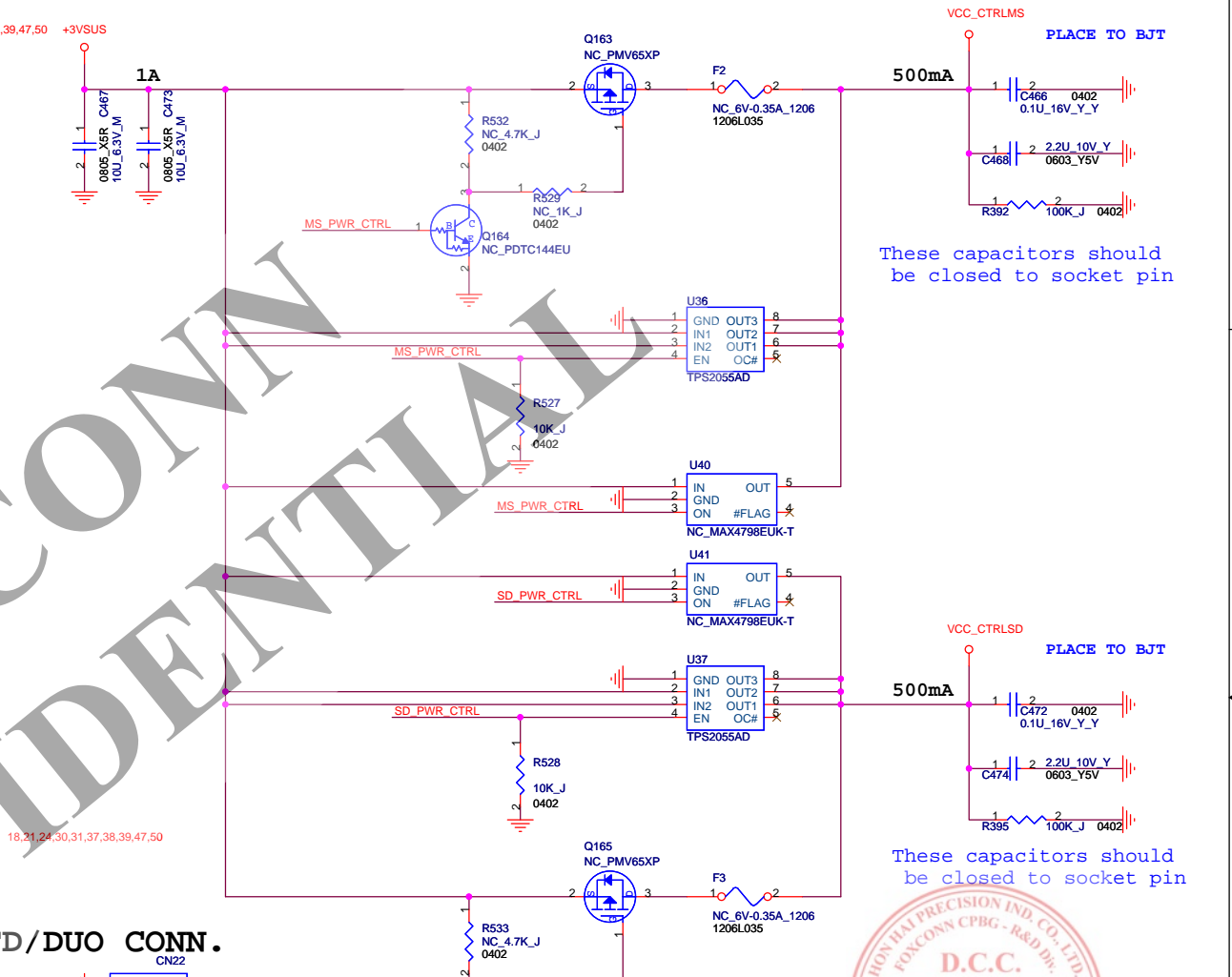
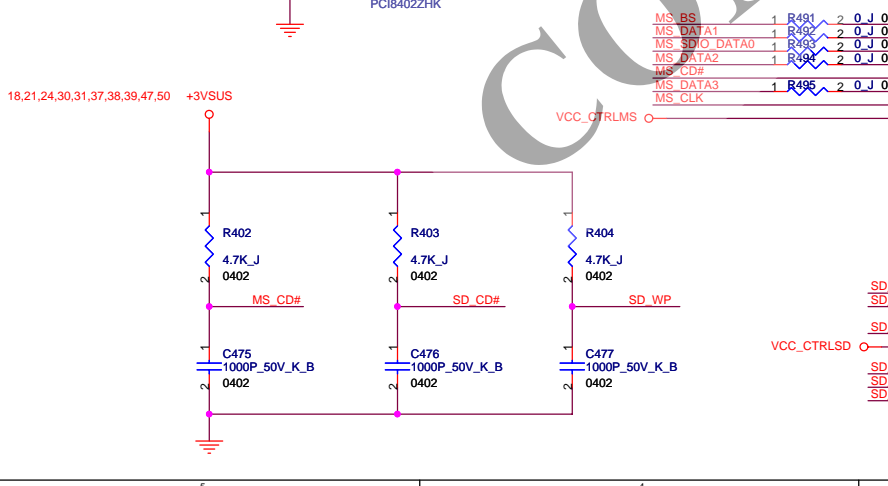
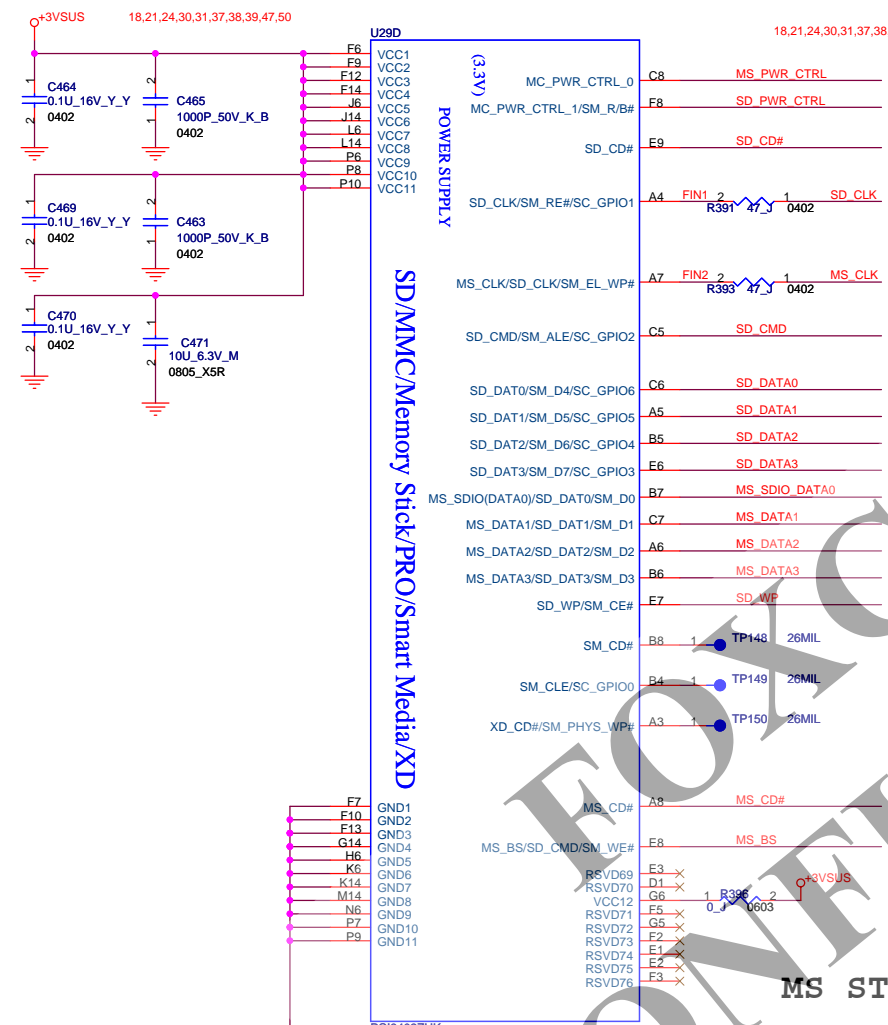
Resistors should be placed on the SCL and SDA terminals

Place near PCI8402.

iLink CONN.







PLACE TO BJT

500mA

These capacitors should be closed to socket pin

PLACE TO BJT

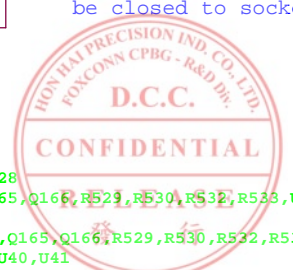
500mA

These capacitors should be closed to socket pin

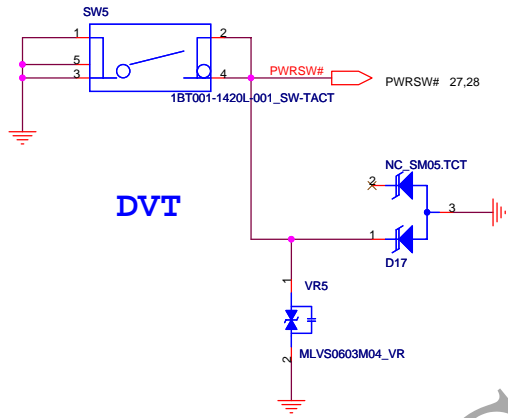
**Solution1 :**  
 Mount U36,U37,R527,R528  
 NC F2,F3,Q163,Q164,Q165,Q166,R529,R530,R532,R533,U40,U41

**Solution2 :**  
 Mount F2,F3,Q163,Q164,Q165,Q166,R529,R530,R532,R533  
 NC U36,U37,R527,R528,U40,U41

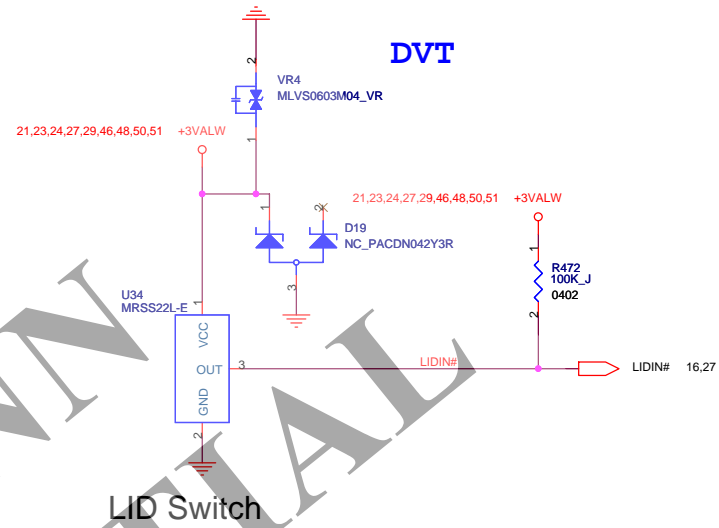
**Solution3 :**  
 Mount U40,U41,R527,R528  
 NC U36,U37,F2,F3,Q163,Q164,Q165,Q166,R529,R530,R532,R533



POWER BUTTON

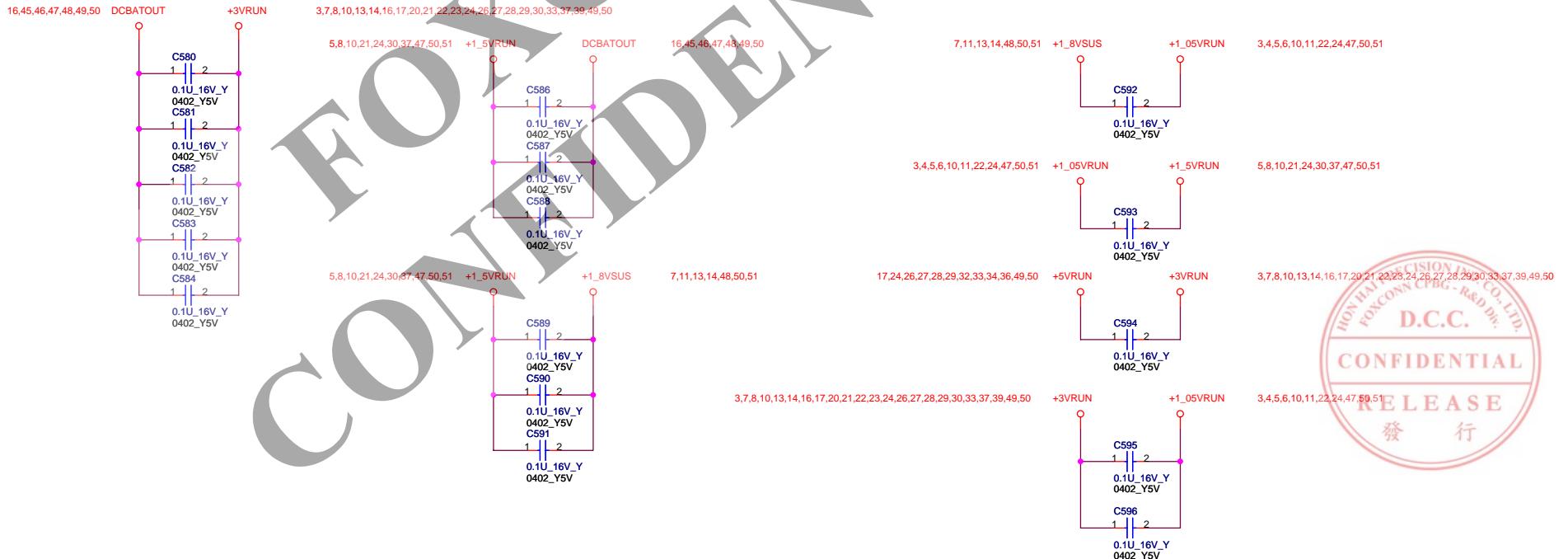


DVT



LID Switch

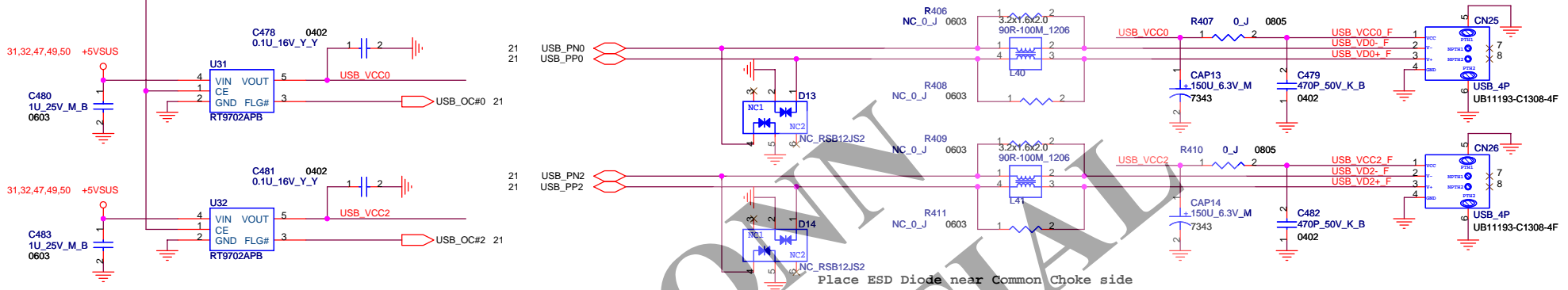
EMI CAP



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>Button/LID Switch/EMI CAP</b>		
Size A3	Document Number MS72-1-01	Rev 0.1
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# USB CONN X 2

23,27,37,38 SUS\_PWRGD\_10MS

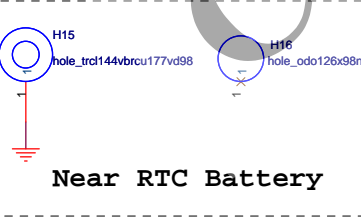
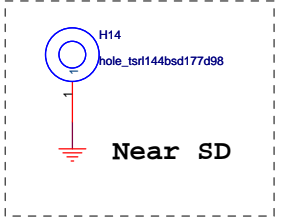
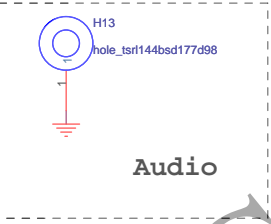
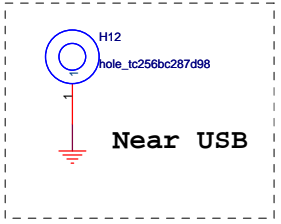
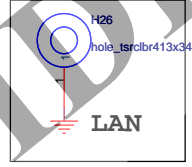
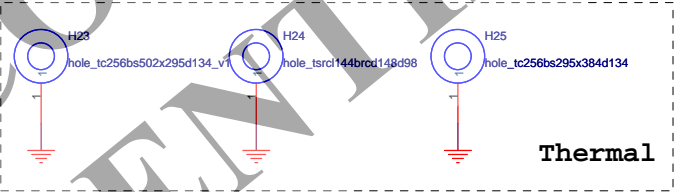
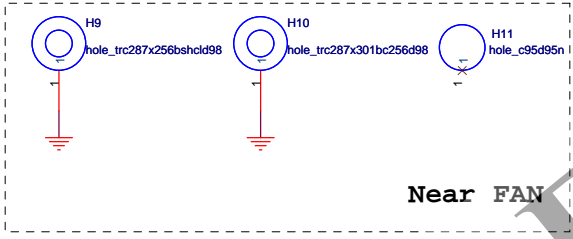
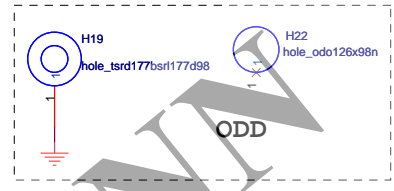
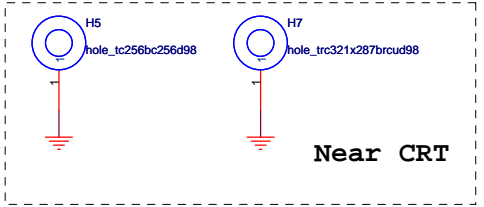
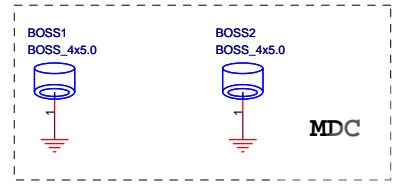
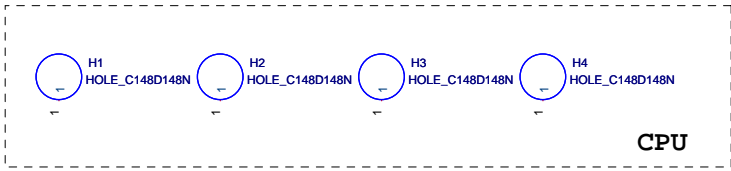


Place ESD Diode near Common Choke side

FOXC  
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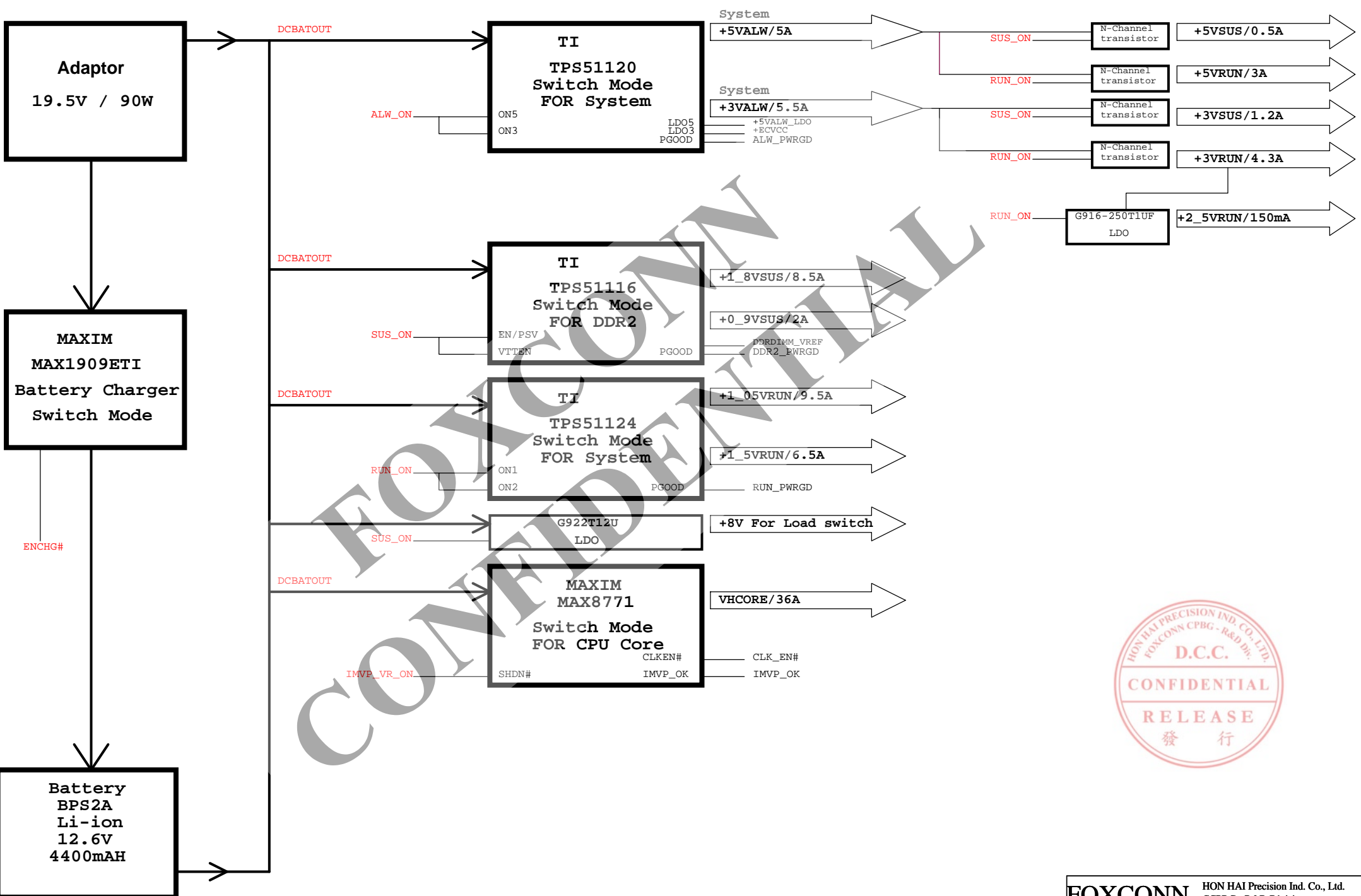
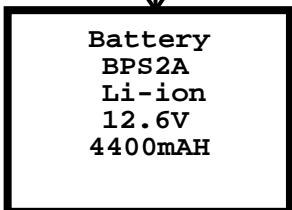
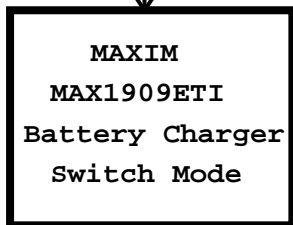
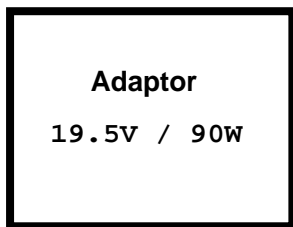
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>USB2.0</b>		CCPBG - R&D Division	
Size A3	Document Number MS72-1-01	Rev 0.1	
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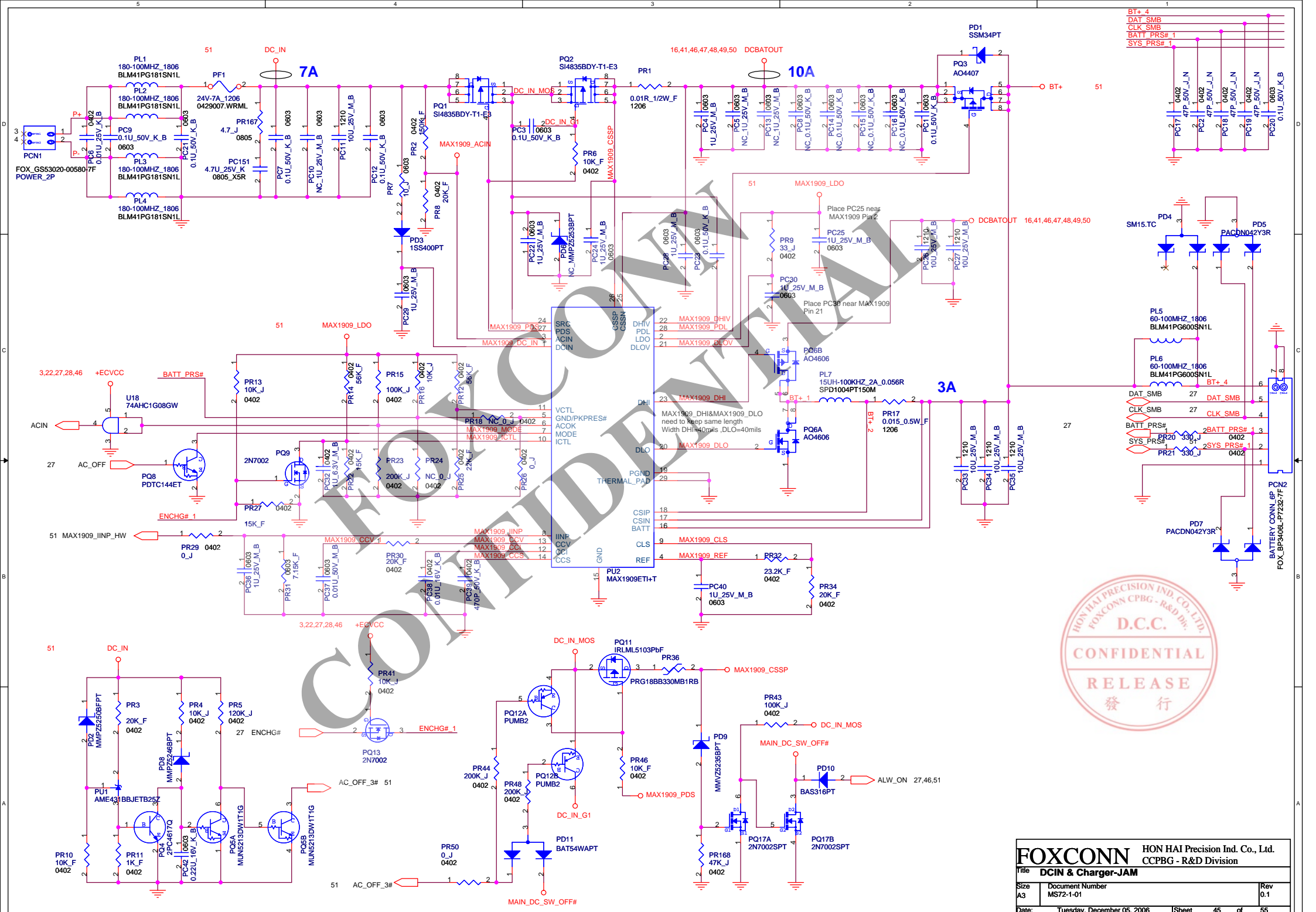
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>HOLE</b>			
Size A3	Document Number MS72-1-01	Rev 0.1	
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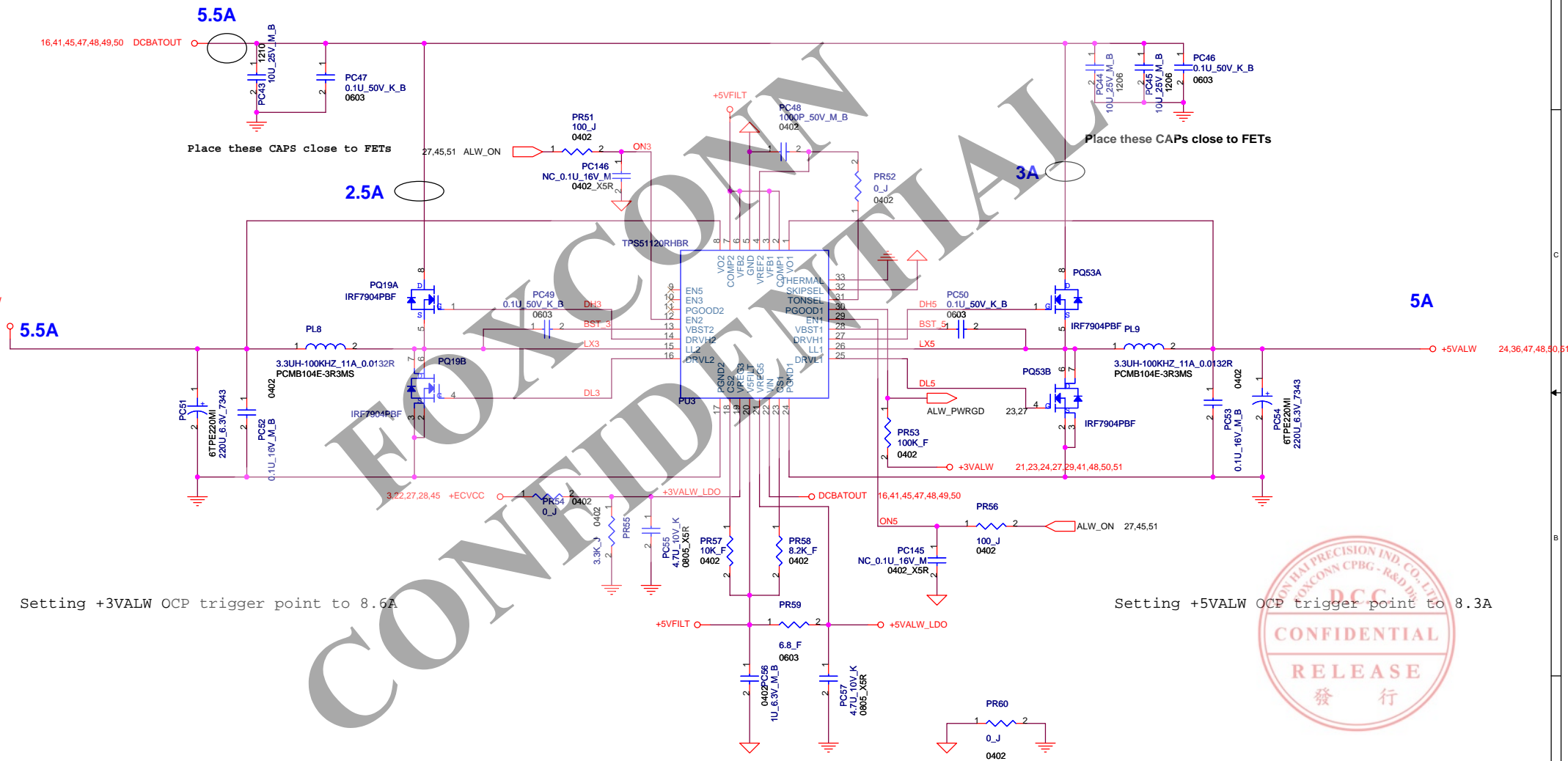


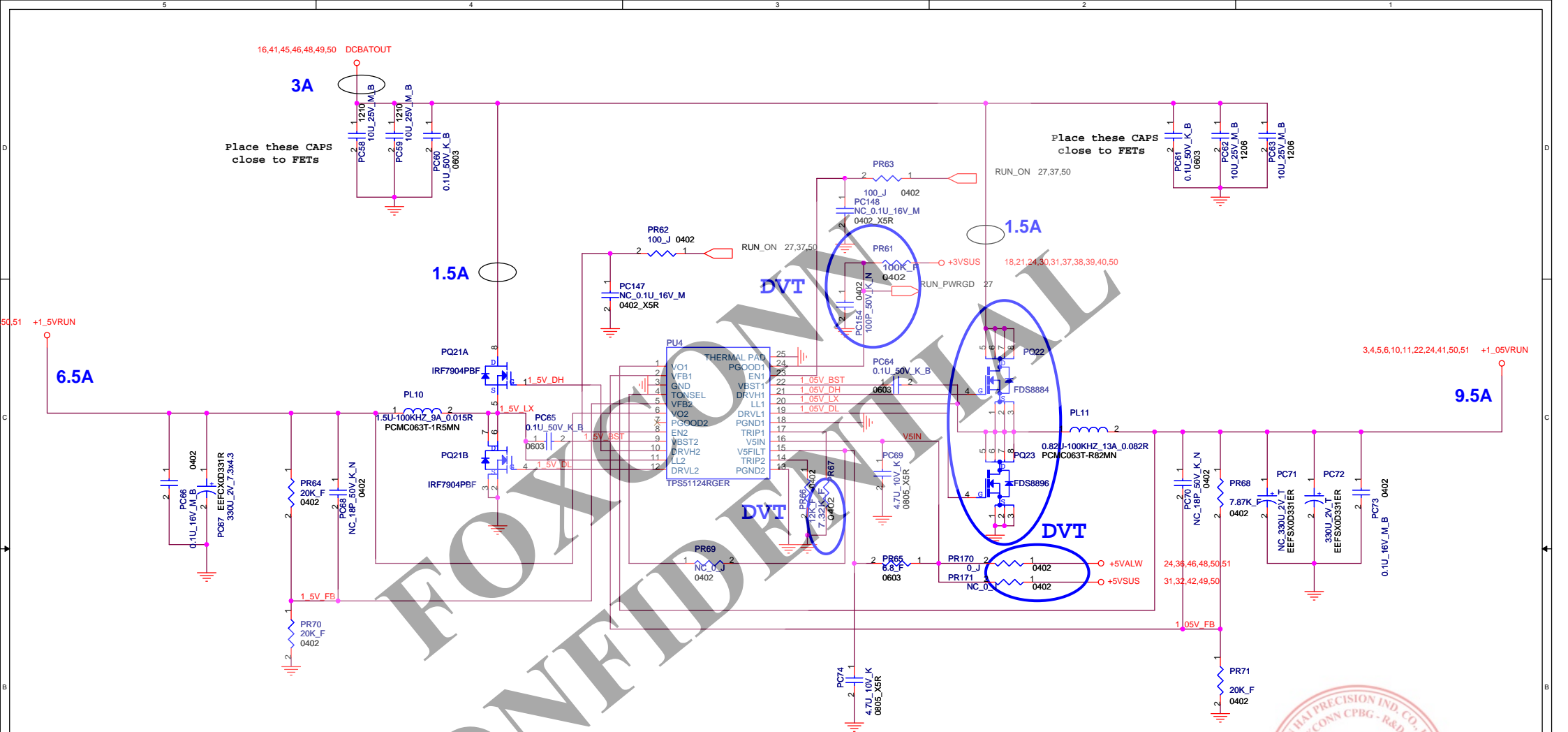
CONFIDENTIAL



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Power Design Diagram-ZG</b>			
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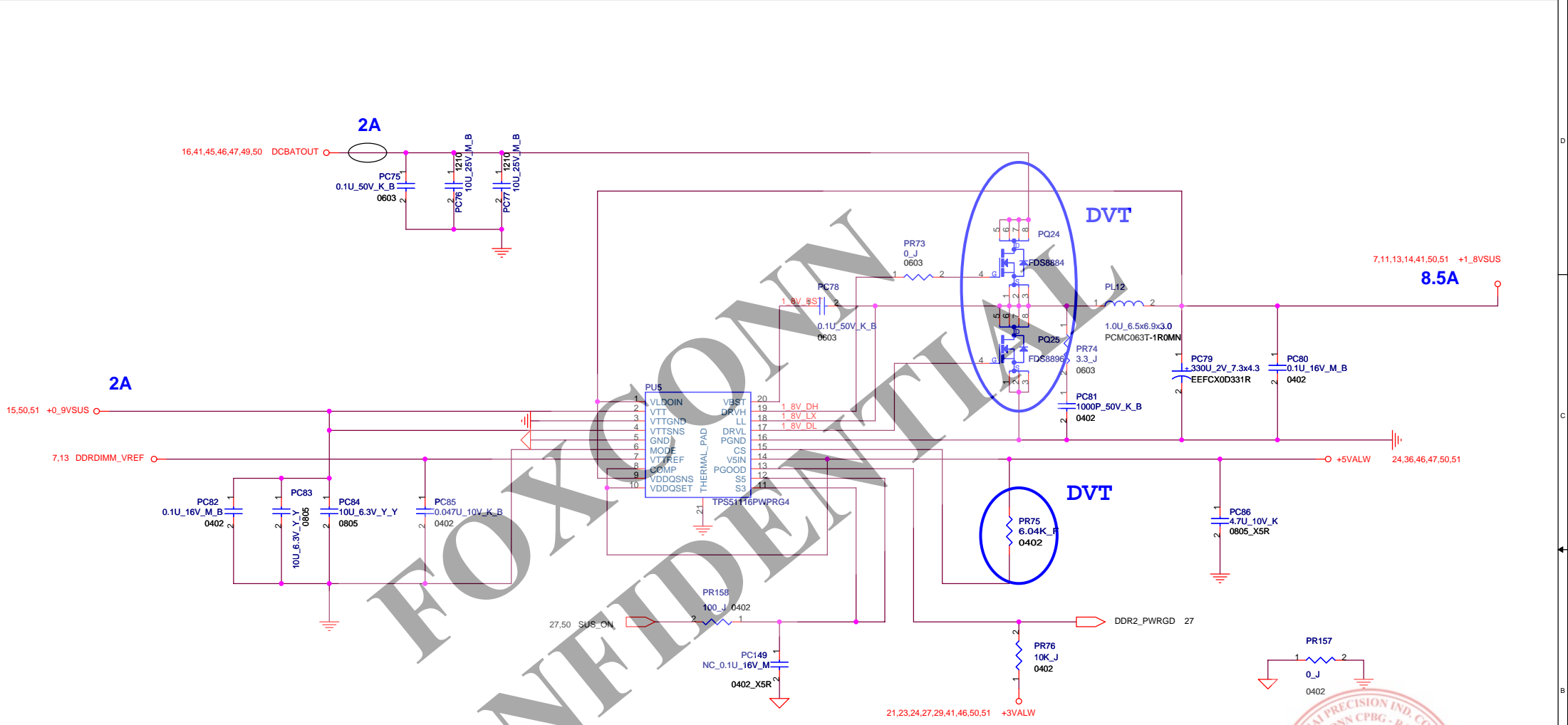
Setting +1\_5VRUN OCP trigger point to 10.5A

Setting +1\_05VRUN OCP trigger point to 12.8A



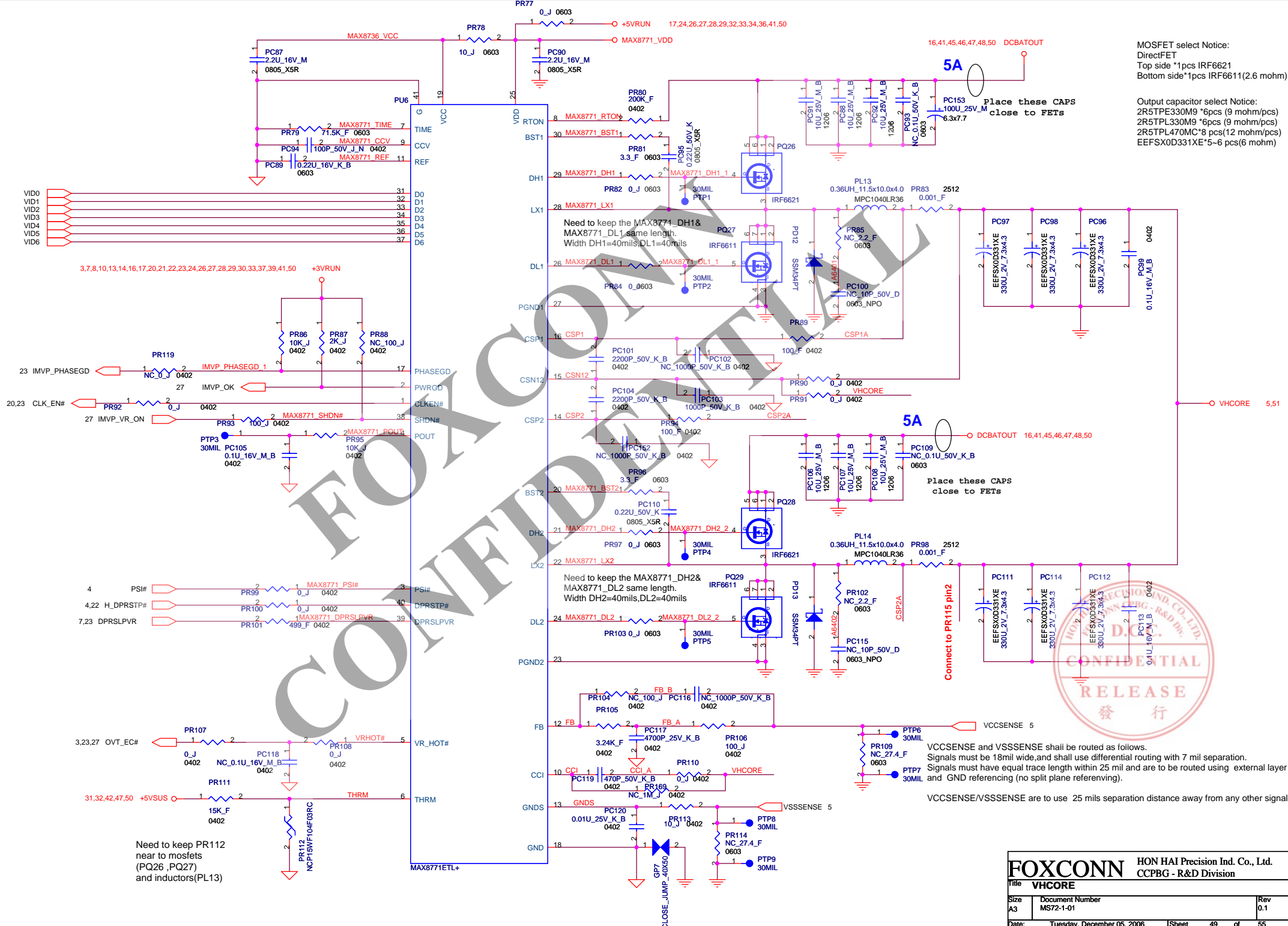
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>1.5V/1.05V-JAM</b>		
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Setting +1\_8VSUS OCP trigger point to 11.6A





MOSFET select Notice:  
 DirectFET  
 Top side \*1pcs IRF6621  
 Bottom side \*1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:  
 2R5TPE330M9 \*6pcs (9 mohm/pcs)  
 2R5TPL330M9 \*6pcs (9 mohm/pcs)  
 2R5TPL470M8 \*8 pcs(12 mohm/pcs)  
 EEFSXOD331XE\*5-6 pcs(6 mohm)

Place these CAPS close to FETs

Place these CAPS close to FETs

Need to keep the MAX8771\_DH1 & MAX8771\_DL1 same length. Width DH1=40mils, DL1=40mils

Need to keep the MAX8771\_DH2 & MAX8771\_DL2 same length. Width DH2=40mils, DL2=40mils

Connect to PR115 pin2

VCCSENSE and VSSSENSE shall be routed as follows. Signals must be 18mil wide, and shall use differential routing with 7 mil separation. Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referencing).

VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

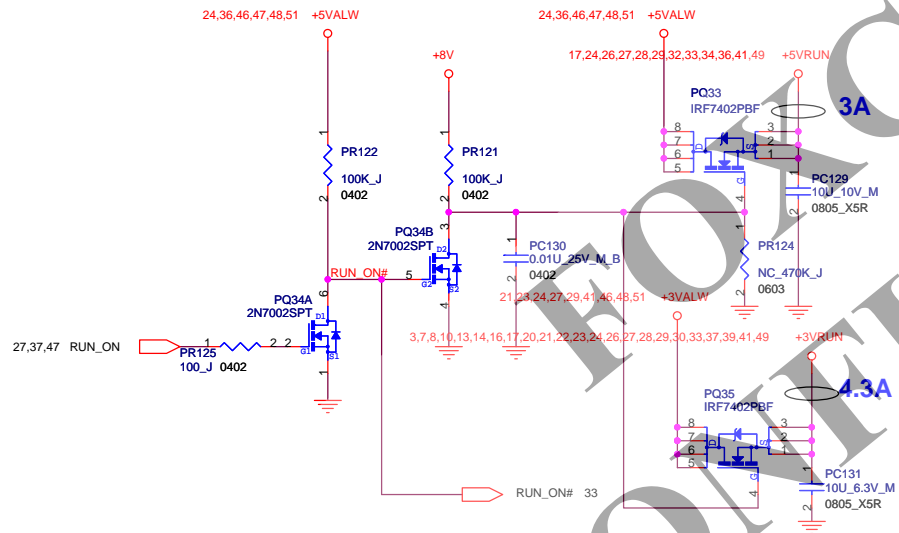
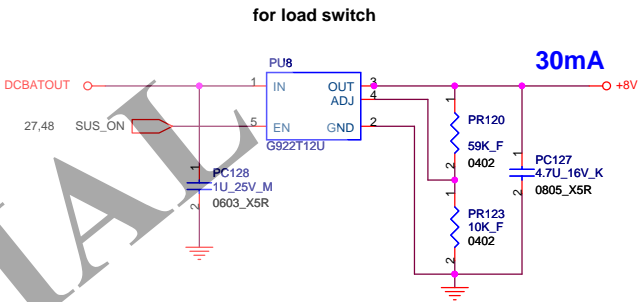
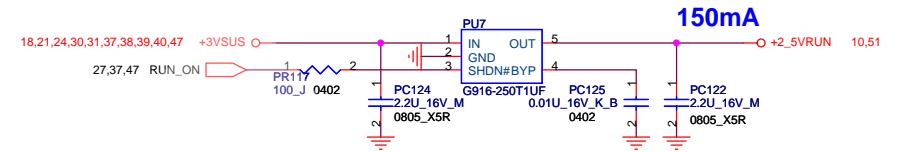
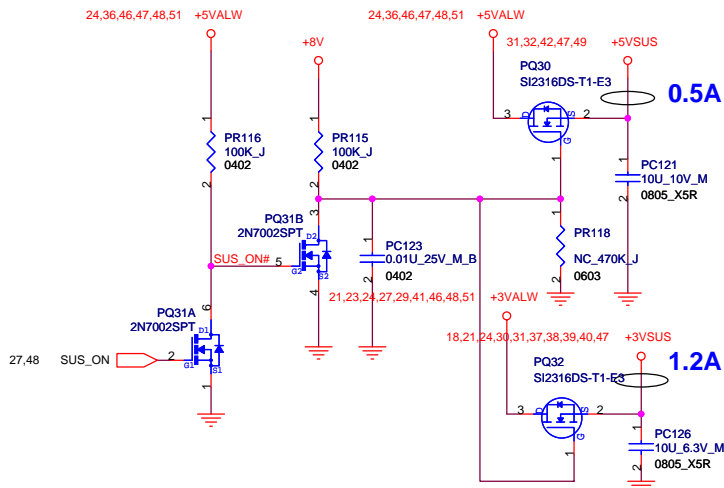
Need to keep PR112 near to mosfets (PQ26, PQ27) and inductors(PL13)

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 CCPBG - R&D Division

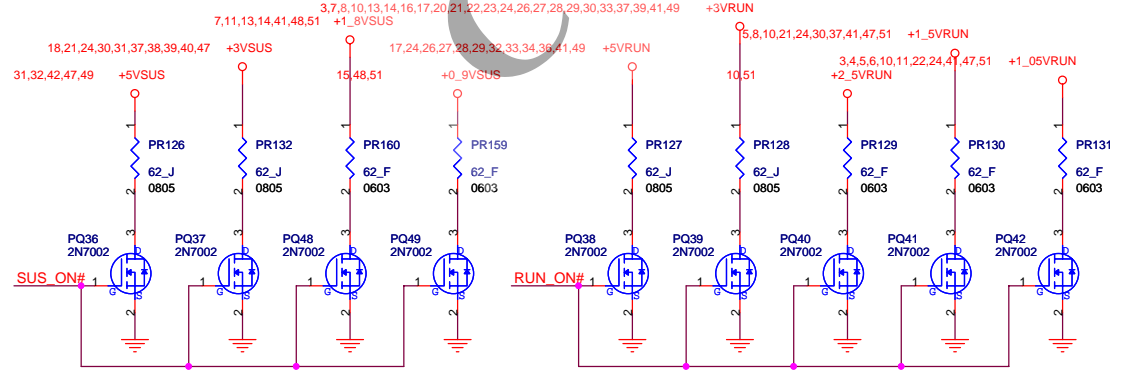
Title: **VHCORE**

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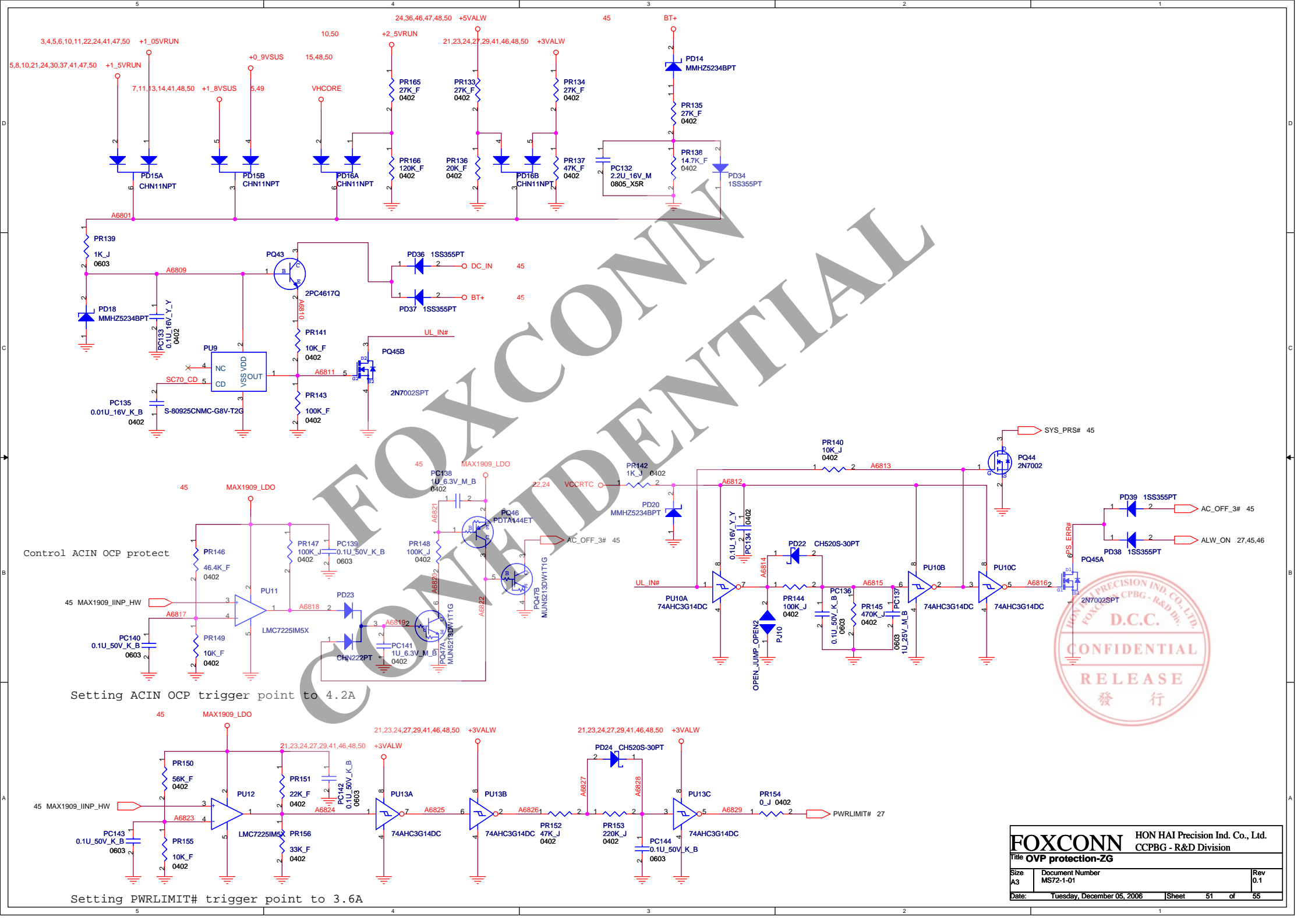




Discharge circuit for power-off



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Other power plan-ZG</b>			
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Control ACIN OCP protect

Setting ACIN OCP trigger point to 4.2A

Setting PWRLIMIT# trigger point to 3.6A



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>OVP protection-ZG</b>		
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# HISTORY (1)

## DVT

(2006/11/14)  
P.11 Add C608 and NC CAP7 for purchase convenient.  
P.17 Add R544 and NC R121for CRB requirement(refer to Capell\_Valley\_CRB\_Schematics\_Rev1\_502 page18)  
P.33 NC R483 for Page36 had pull low 10k resistor to GND  
P.34 Change CAP11,CAP12 from 1C-31T0337-M101 to 1C-42T0107-M100 for application modification  
P.36 Add Q167, Q168, R536 and NC U26, U27,U28, D12, C452, R377,R378 for application modification  
Change Q27, Q159, from 17-CHDTC14-4E01 to 17-PMBT390-4200 for application modification  
Change Q26 from 17-DTAl14Y-UA00 to 17-MMBT390-6K00 for application modification  
Add R540,R541,R542,R543,R537,R538,R539,C609 for application modification

(2006/11/15)  
P.47 Change PQ22 from 17-1RF7807-2000 to 17-FDS8884-0000 for application modification  
Change PQ23 from 17-1RF8113-0000 to 17-FDS8896-0000 for application modification  
P.48 Change PQ24 from 17-1RF7807-2000 to 17-FDS8884-0000 for application modification  
Change PQ25 from 17-1RF8113-0000 to 17-FDS8896-0000 for application modification

(2006/11/20)  
P.11 Del C608 and mount CAP7 for MOR requirement  
P.17 Del R544 and mount R121 for MOR requirement  
P.47 Change PR67 from 1R-0000472-F200 to 1R-0007321-F200 for power PWM OCP application modification  
P.48 Change PR75 from 1R-0000562-F200 to 1R-0006041-F200 for power PWM OCP application modification

(2006/11/21)  
P.33 Add R483 for MOR requirement  
P.36 Del Q167, Q168, R536 and add U26, U27,U28,D12, C452, R377,R378 for MOR requirement  
Change Q27, Q159, from 17-PMBT390-42001 to 17-CHDTC14-4E01for MOR requirement  
Change Q26 from 17-MMBT390-6K00 to 17-DTAl14Y-UA00 for MOR requirement  
Del R540,R541,R542,R543,R537,R538,R539,C609 for MOR requirement

(2006/11/22)  
P.28 Add R535 0om for X-BUS CONN del on MP  
P.47 Add PC154 and change PR61 from 10k to 100k for RUN\_PWRGD glitch issue  
Change the power supply of PU4 pin16 from +5VSUS to +5VALW for application modification

(2006/11/23)  
P.47 Add PR170,PR171 for MOR requirement

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