Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	0.20	06/5/22
02	Block Diagram	0.20	06/5/22
03	Yonah(HOST BUS) 1/2	0.20	06/5/22
04	Yonah(HOST BUS) 2/3	0.20	06/5/22
05	Yonah(Power/Gnd) 3/3	0.20	06/5/22
06	CALISTOGA (HOST) 1/7	0.20	06/5/22
07	CALISTOG (DMI) 2/7	0.20	06/5/22
08	CALIST (GRAPHIC) 3/7	0.20	06/5/22
09	CALISTOGA (DDRII) 4/7	0.20	06/5/22
10	CALIST (POWER,VCC) 5/7	0.20	06/5/22
11	CALIST (VCC CORE) 6/7	0.20	06/5/22
12	CALIST (VSS) 7/7	0.20	06/5/22
13	DDRII(SO-DIMM_0) 1/3	0.20	06/5/22
14	DDRII(SO-DIMM_1) 2/3	0.20	06/5/22
15	DDRII(Termination) 3/3	0.20	06/5/22
16	LVDS / S_VIDEO	0.20	06/5/22
17	ICH7-M(PCI/USB) 1/5	0.20	06/5/22
18	ICH7-M(LPC,IDE,SATA)2/5	0.20	06/5/22
19	ICH7-M(GPIO) 3/5	0.20	06/5/22
20	ICH7-M(POWER) 4/5	0.20	06/5/22
21	ICH7-M(GND) 5/5	0.20	06/5/22
22	SATA HDD/CD-ROM	0.20	06/5/22
23	EC+KBC	0.20	06/5/22
24	Flash ROM/XBUS	0.20	06/5/22
25	Mini_Card/BT	0.20	06/5/22
26	FAN/HW THERMAL PROTECT	0.20	06/5/22
27	EXPRESS/OIDE/TP	0.20	06/5/22
28	PCI (PCI BUS)	0.20	06/5/22
29	PCI (ILINK)	0.20	06/5/22
30	PCI (MS)	0.20	06/5/22
31	PCI (PCMCIA)	0.20	06/5/22
32	USB2.0	0.20	06/5/22
33	CRT	0.20	06/5/22
34	DB CONNS & LED	0.20	06/5/22
35	Power Design Diagram	0.20	06/5/22
36	DC_IN/Charger (MAX1909)	0.20	06/5/22
37	SYSPWR(+3VALW/+5VALW)	0.20	06/5/22
38	SYSPWR(+1_5VRUN/+1_05VRUN)	0.20	06/5/22
39	VHCORE(ISL6262)	0.20	06/5/22
40	Others power plan	0.20	06/5/22
41	OVP protection	0.20	06/5/22
42	DDR2PWR(+1_8V_SUS/+0_9VRUN)	0.20	06/5/22
43	CLOCK GEN	0.20	06/5/22
44	HOLE	0.20	06/5/22
45	POWER SEQUENCE	0.20	06/5/22
46	History	0.20	06/5/22
47	History	0.20	06/5/22

P. Leader	Check by	Design by

PCB P/N:

1P-0065102-80SA - FUBAI

1P-0065201-80SA - NANYA

1P-0065503-80SA - HANNSTAR

Project Code & Schematics Subject: MS60-L Main Board

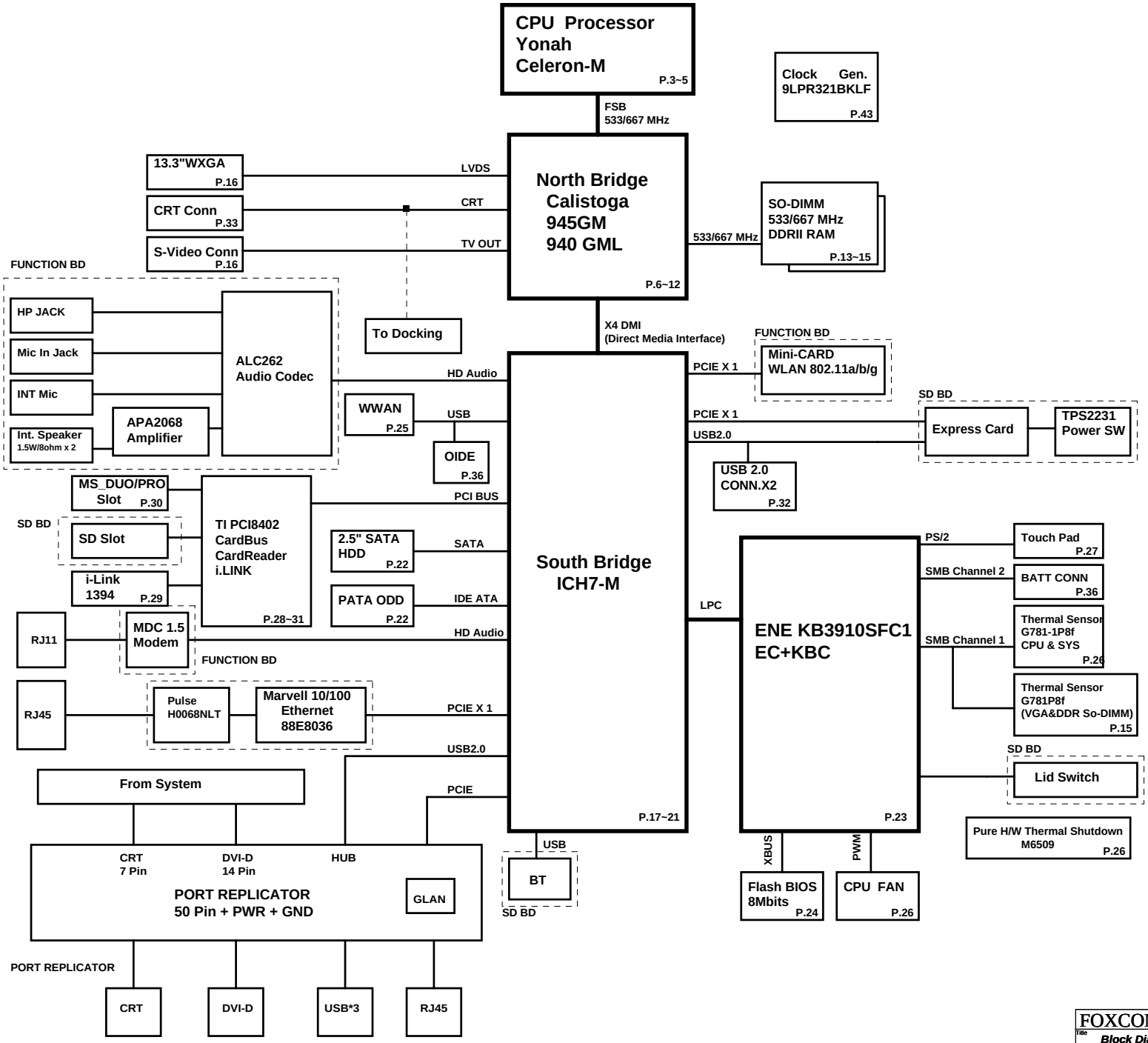
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *Index Page*

Size: Custom | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 1 of 47

MS60 (CALISTOGA GM Block Diagram)



SYSTEM DC/DC
MAX8734 P.37

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC
MAX8743 P.38

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SC486 P.42

DCBATOUT	+1_8V_S3_SUS +0_9VRUN

CPU DC/DC
ISL6262 P.39

INPUTS	OUTPUTS
DCBATOUT	VHCORE

AMP DC/DC
MAX1616 P.40

INPUTS	OUTPUTS
DCBATOUT	+8VRUN

MAXIM CHARGER
MAX1909 P.36

INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

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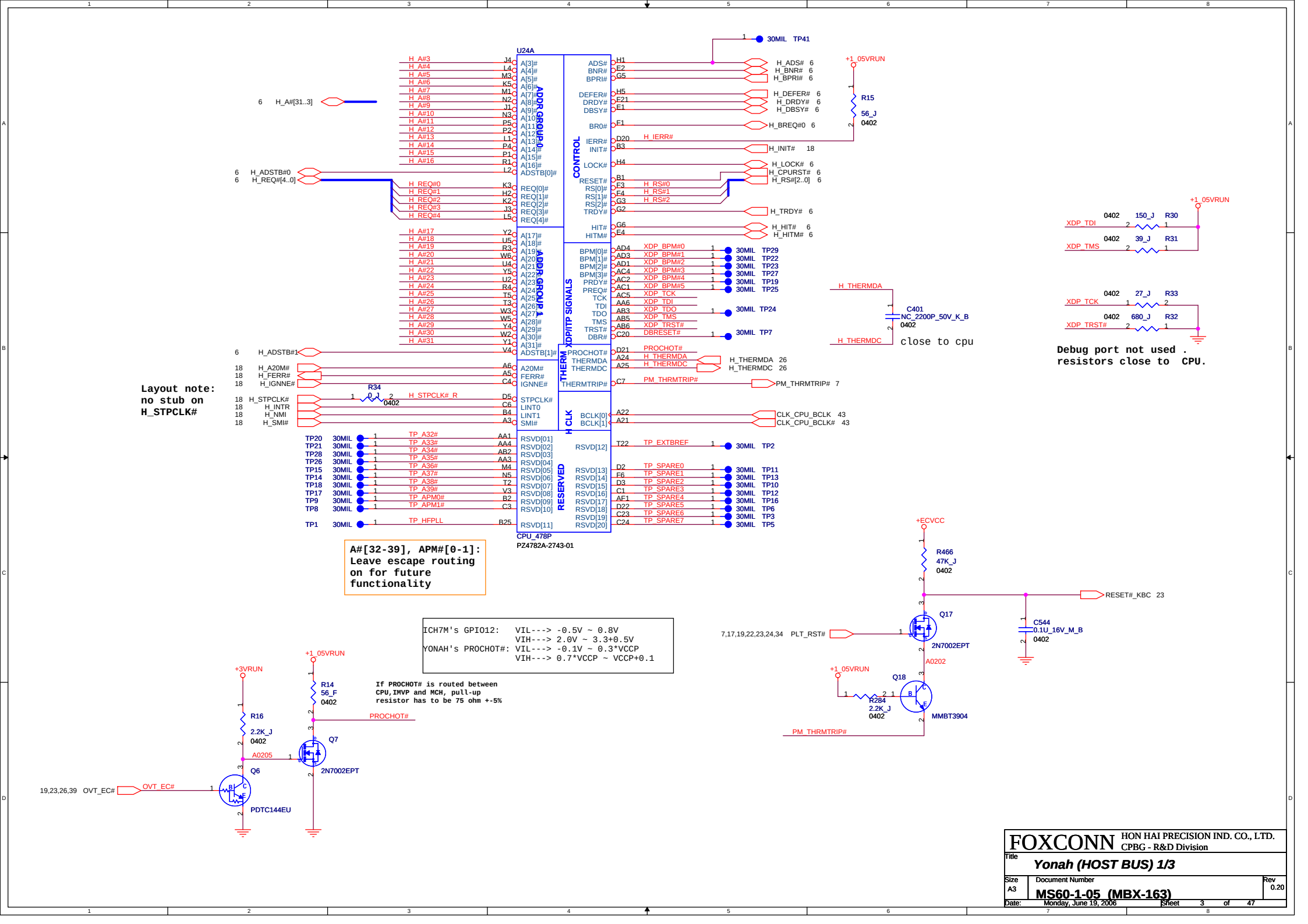
Title: *Block Diagram (All)*

Size: Custom | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 2 of 47

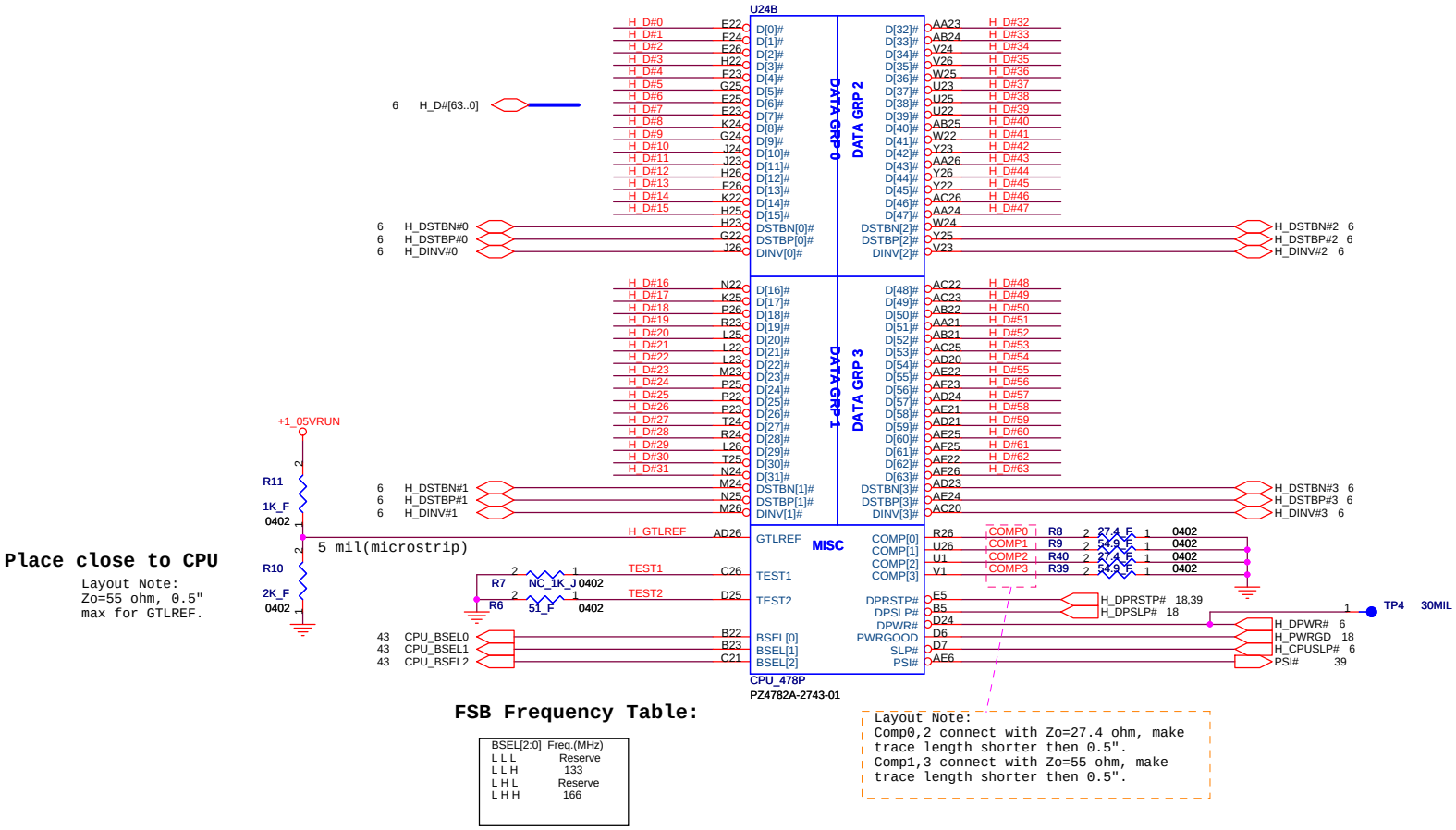


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: Yonah (HOST BUS) 1/3

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 3 of 47



Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

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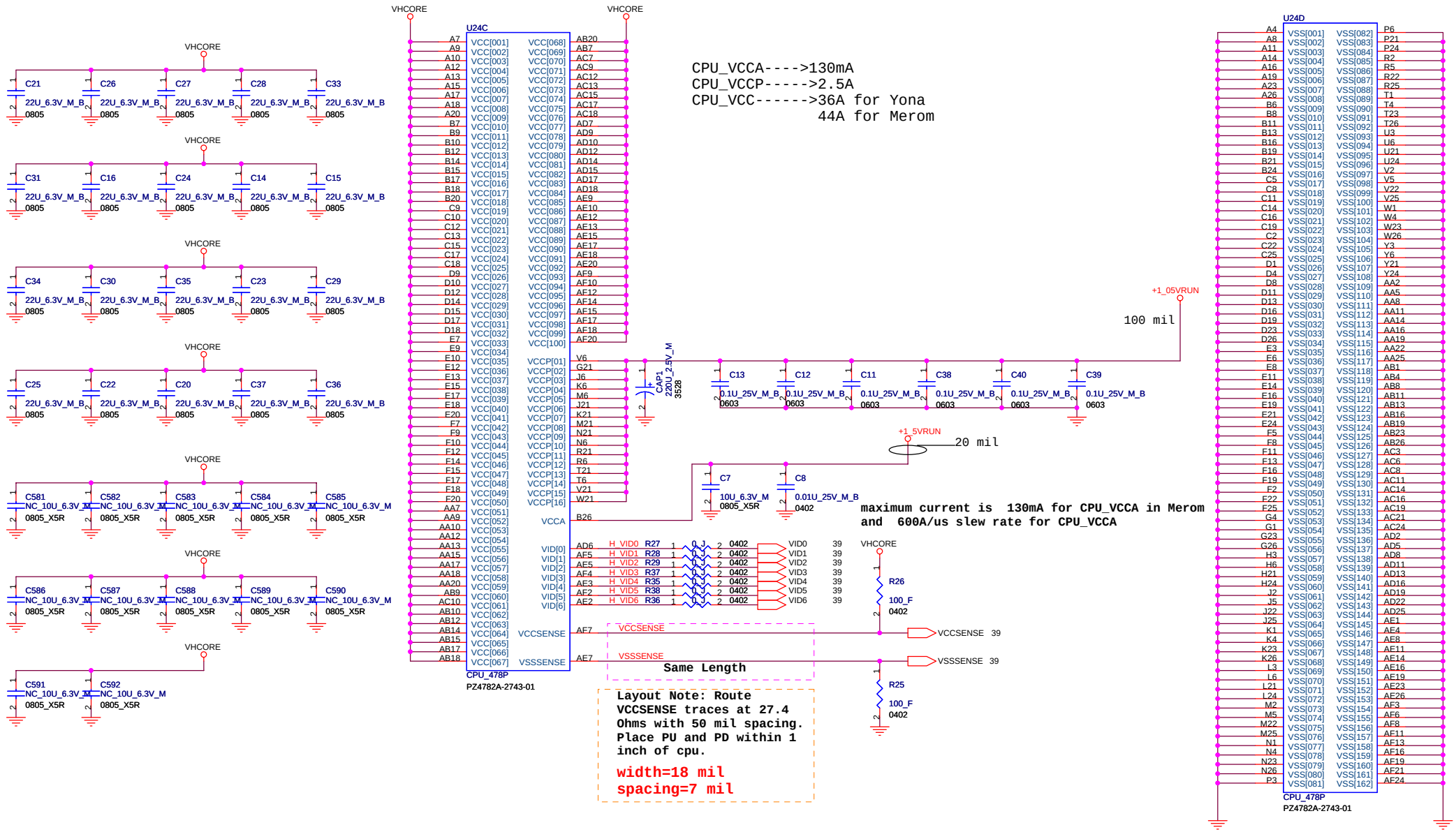
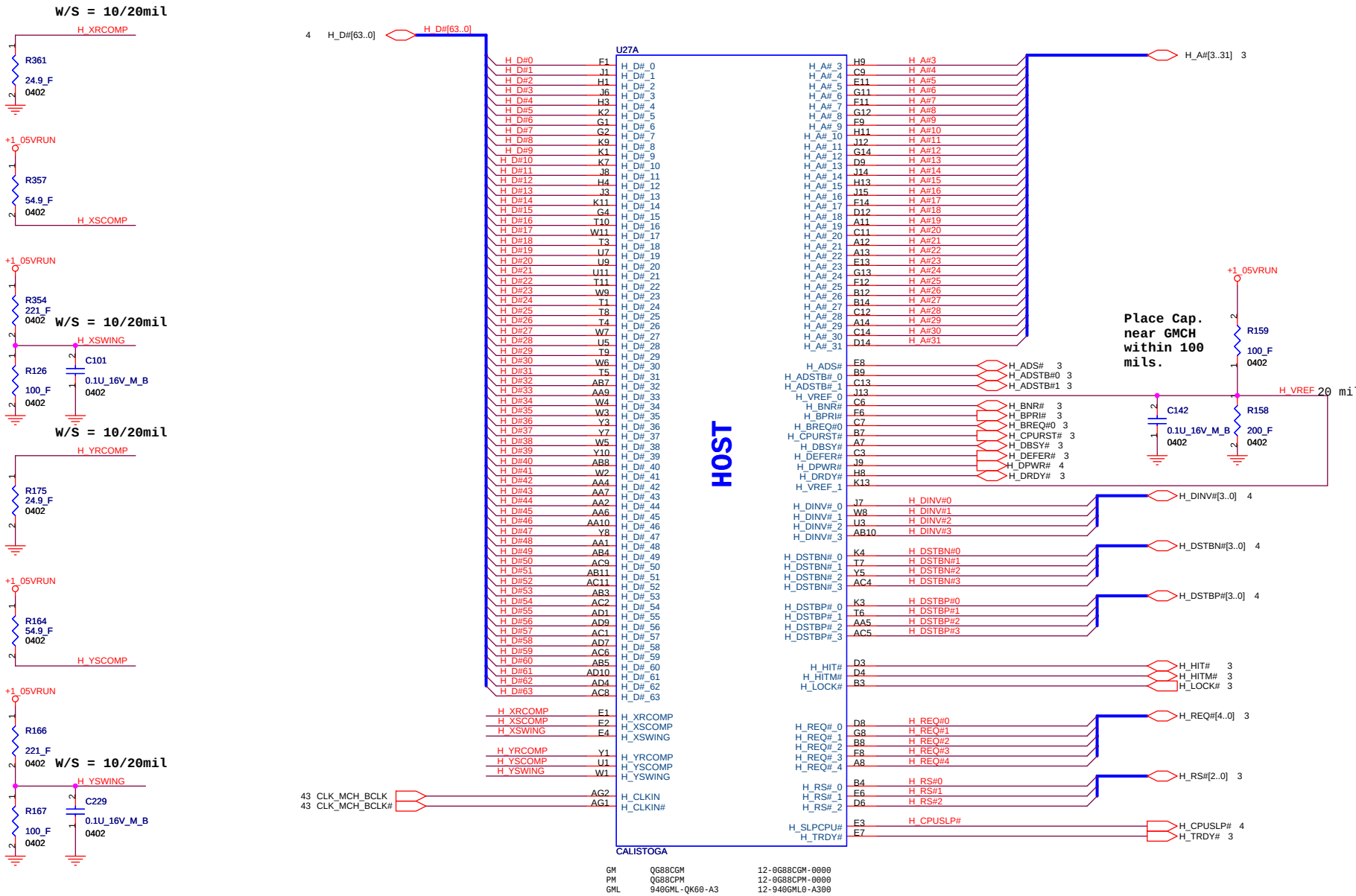
Title: *Yonah (HOST BUS) 2/3*

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

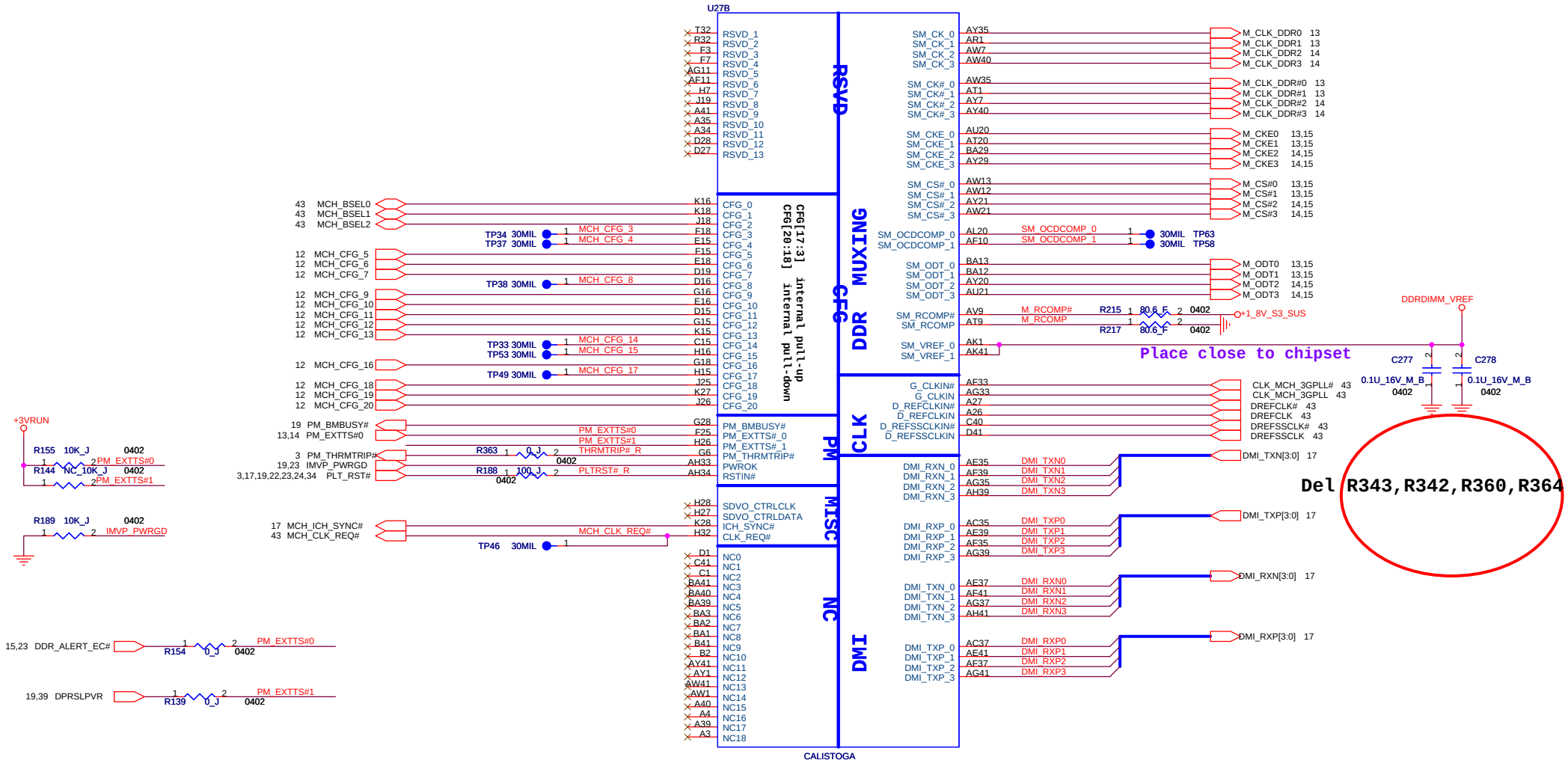
Date: Monday, June 19, 2006 | Sheet 4 of 47



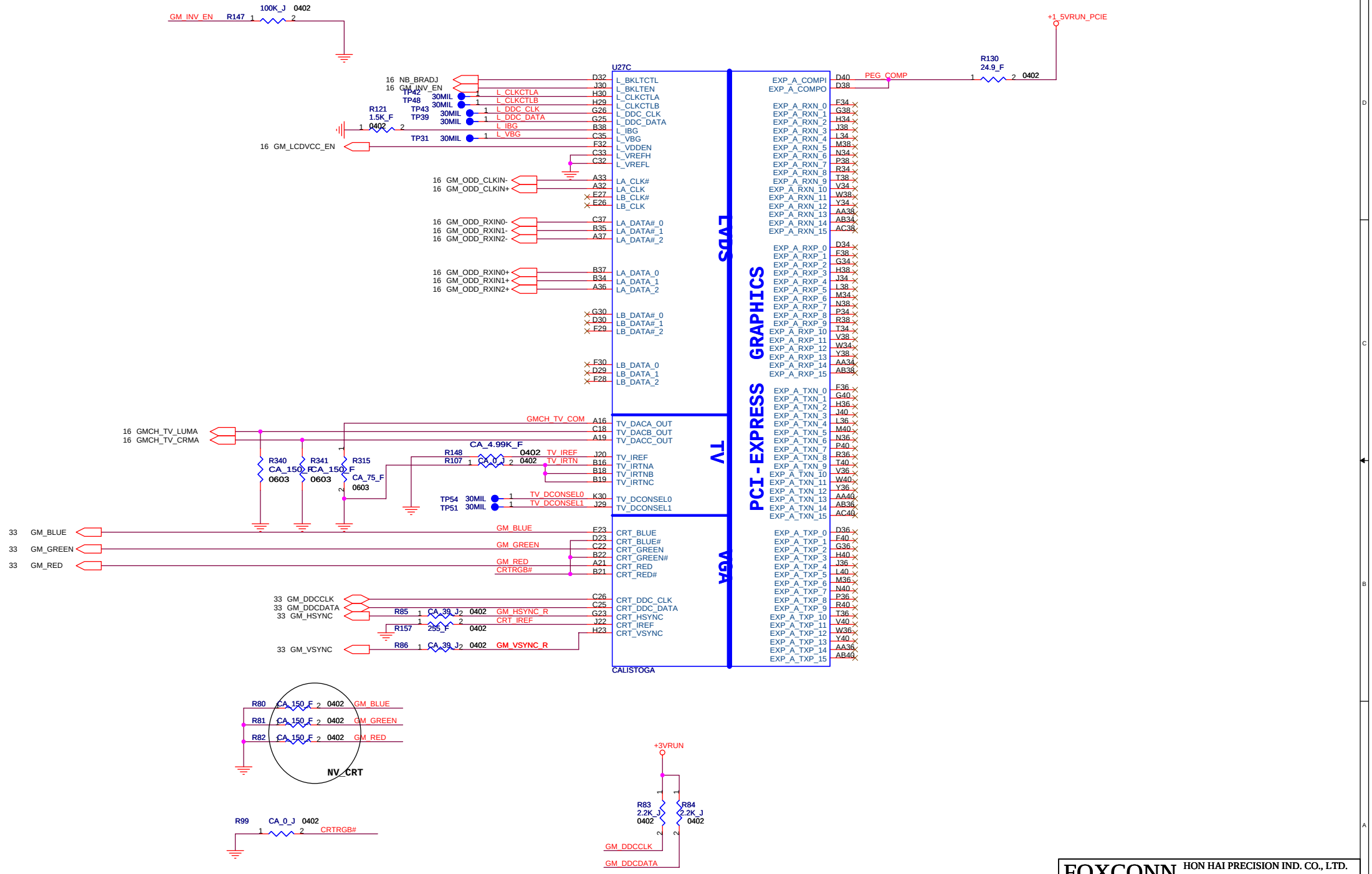
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	Yonah (POWER/GROUND) 3/3		
Size A3	Document Number MS60-1-05 (MBX-163)		Rev 0.20
Date: Monday, June 19, 2006	Sheet 5 of 47		



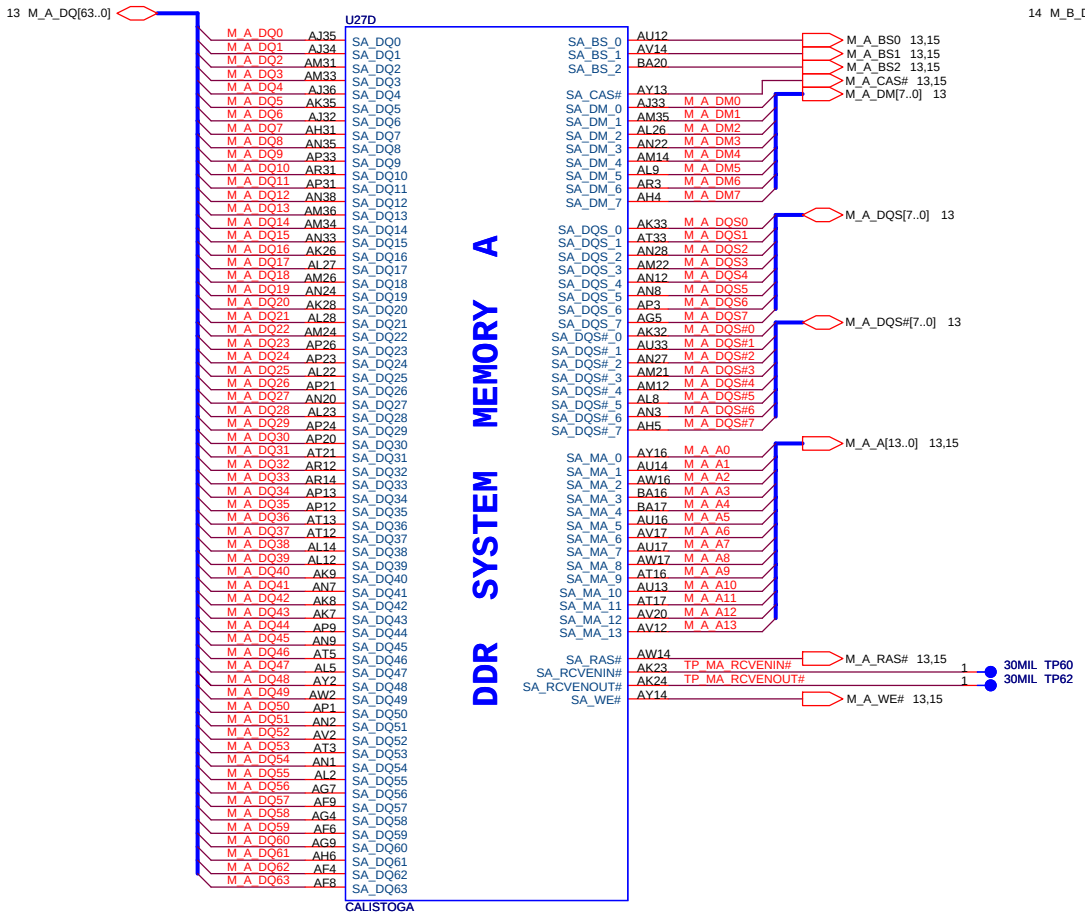
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOHA (HOST)	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 6 of 47	

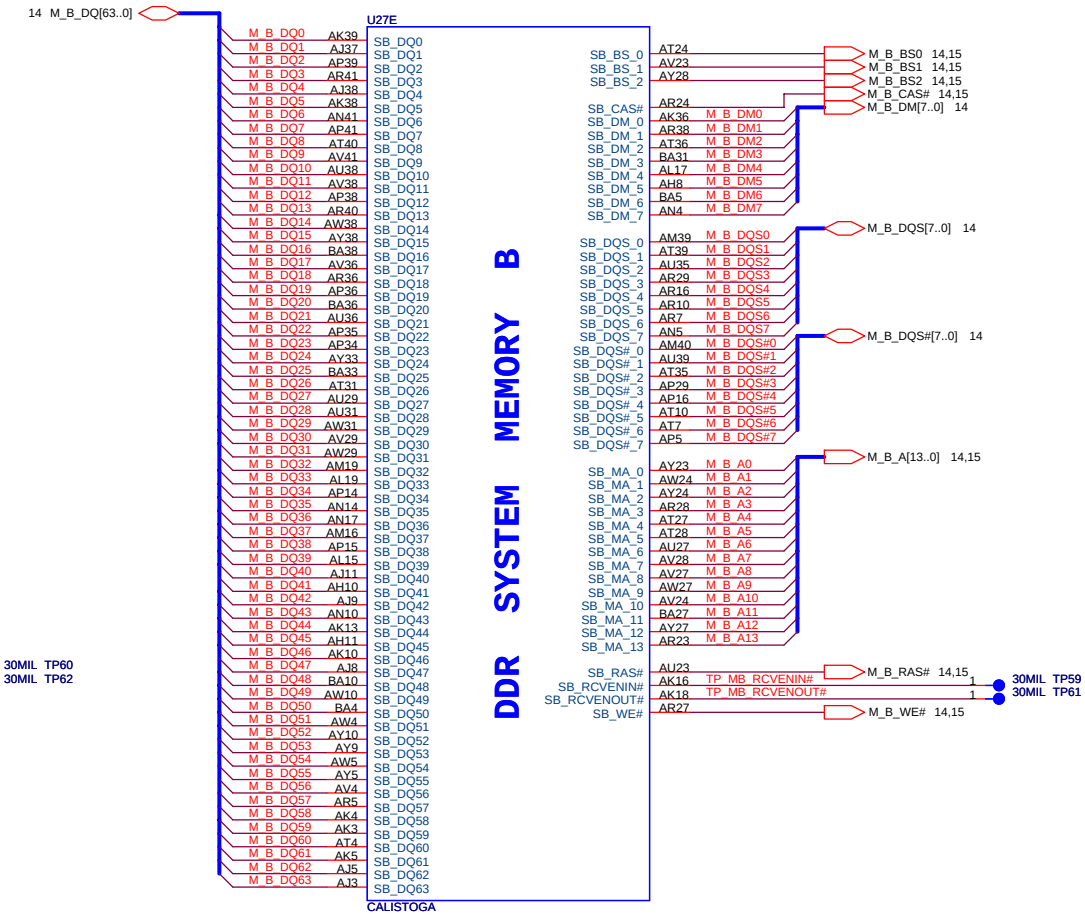


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CALISTOGA (DMI) 2 of 7
Size A3	Document Number MS60-1-05 (MBX-163)
Rev	0.20
Date: Monday, June 19, 2006	Sheet 7 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	CALISTOGA (DMI) 3 of 7		
Size A3	Document Number MS60-1-05 (MBX-163)		Rev 0.20
Date: Monday, June 19, 2006	Sheet 8 of 47		





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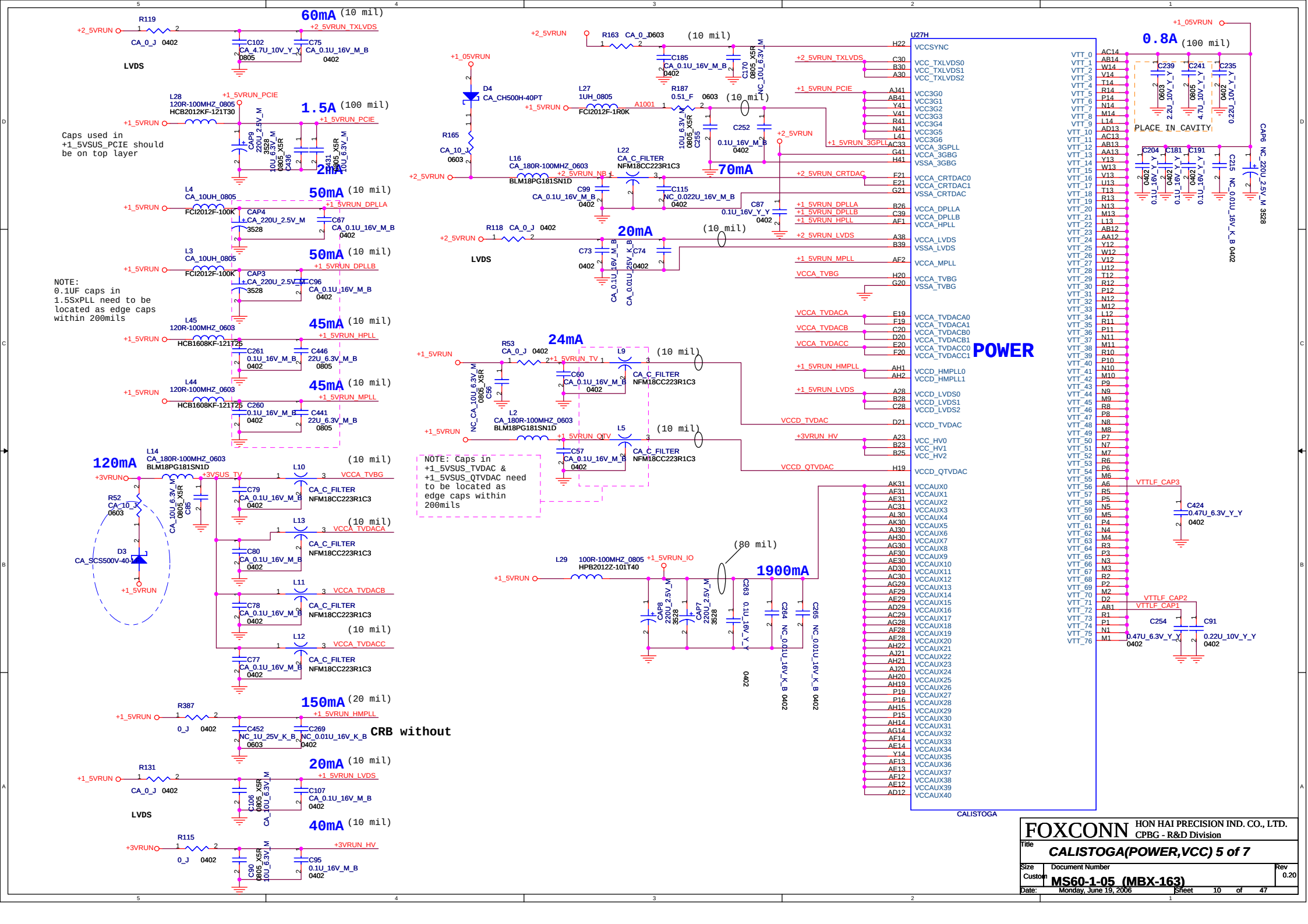
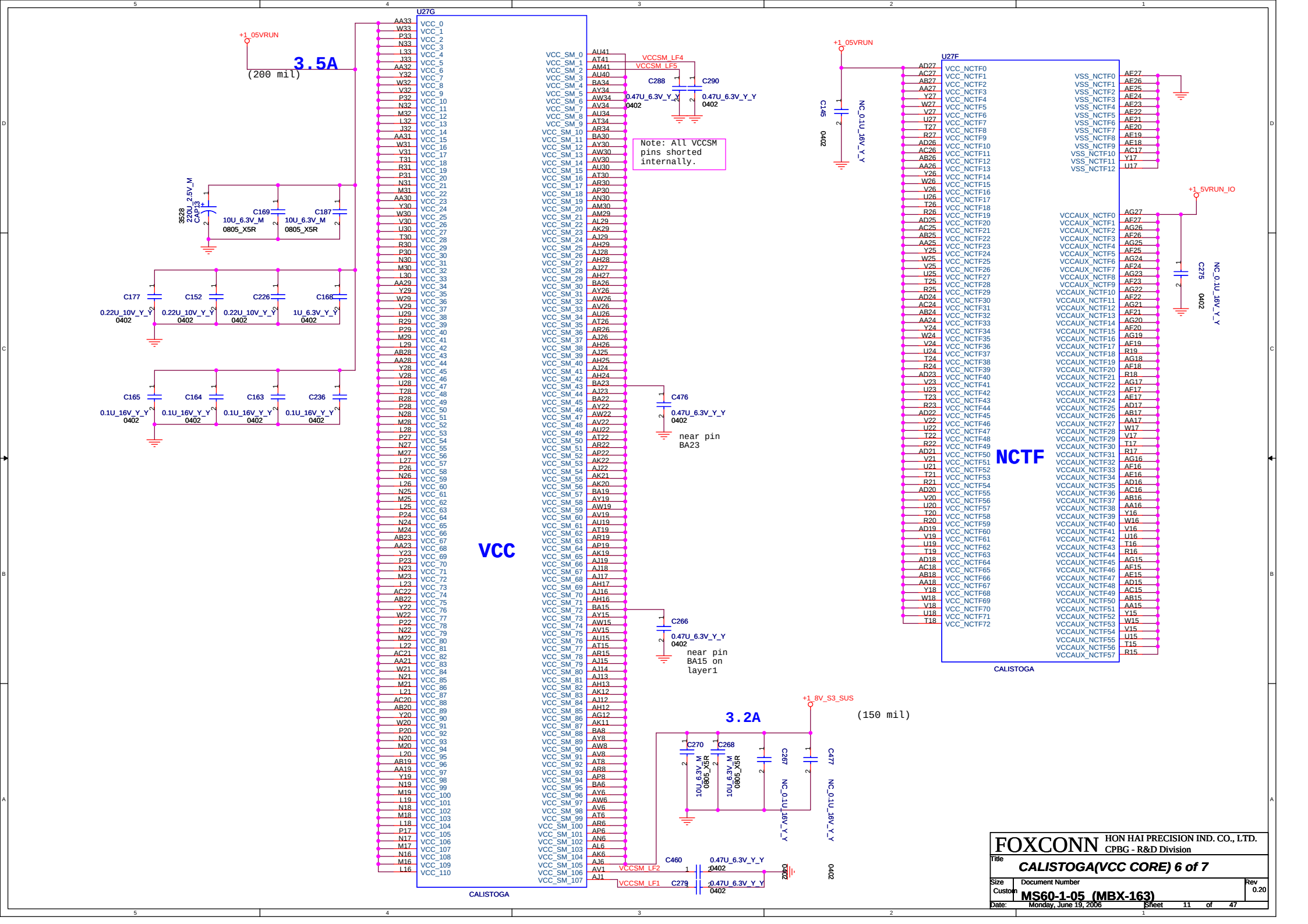
Title: CALISTOGA (DDRII) 4 of 7

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 9 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CALISTOGA(POWER,VCC) 5 of 7
Size: Custom	Document Number: MS60-1-05 (MBX-163)
Rev	0.20
Date:	Monday, June 19, 2006
Sheet	10 of 47


U27G
VCC
CALISTOGA
U27F
NCTF
CALISTOGA
3.5A
(200 mil)
3.2A
(150 mil)
+1_05VRUN
+1_8V_S3_SUS
+1_5VRUN_IO
VCCSM_LF4
VCCSM_LF5
VCCSM_LF2
VCCSM_LF1
Note: All VCCSM pins shorted internally.
near pin BA23
near pin BA15 on layer1
C288
C290
C476
C266
C460
C279
C270
C268
C267
C477
C145
C275
C177
C152
C226
C168
C165
C164
C163
C236
C169
C187
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
CALISTOGA(VCC CORE) 6 of 7
MS60-1-05 (MBX-163)
Monday, June 19, 2006
Sheet 11 of 47

7 MCH_CFG_5 → 30MIL TP45

MCH_CFG_5	Low = DMIx2 High = DMIx4

7 MCH_CFG_6 → 30MIL TP40

MCH_CFG_6	Low = Moby Dick High = Calistoga

DDR2 select (default high)

7 MCH_CFG_7 → 30MIL TP36

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor

7 MCH_CFG_9 → R153 NC_2.2K_J 0402

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

7 MCH_CFG_10 → 30MIL TP35

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY

7 MCH_CFG_11 → R128 NC_2.2K_J 0402

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga

7 MCH_CFG_12 → 30MIL TP47
7 MCH_CFG_13 → 30MIL TP55

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

7 MCH_CFG_16 → 30MIL TP44

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V

+3VRUN → R156 NC_2.2K_J 0402 → 7 MCH_CFG_18

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED

+3VRUN → R151 NC_2.2K_J 0402 → 7 MCH_CFG_19

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 → 30MIL TP52

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U27I

VSS

CALISTOGA

U27J

VSS

CALISTOGA

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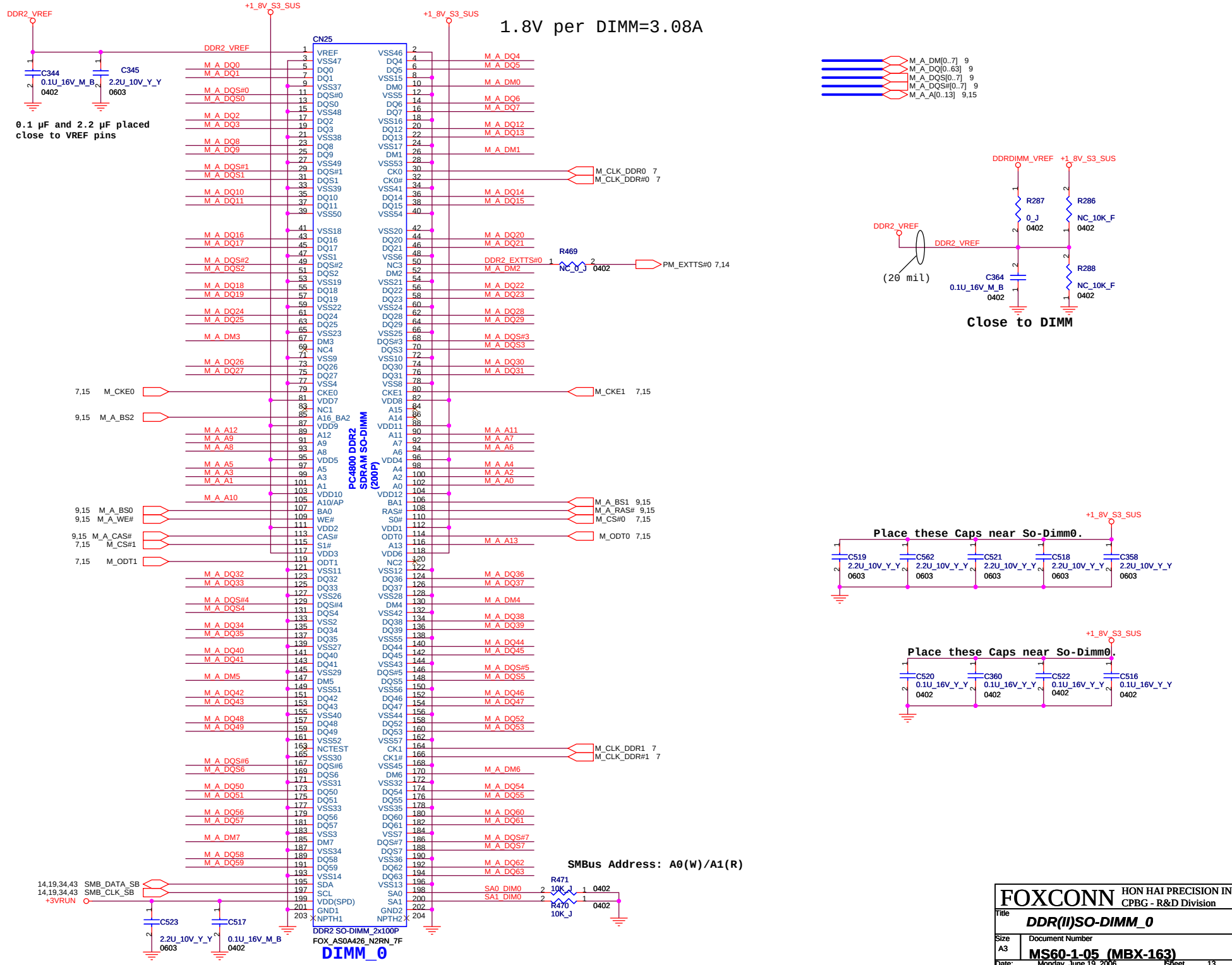
Title: CALISTOGA(VSS) 7 of 7

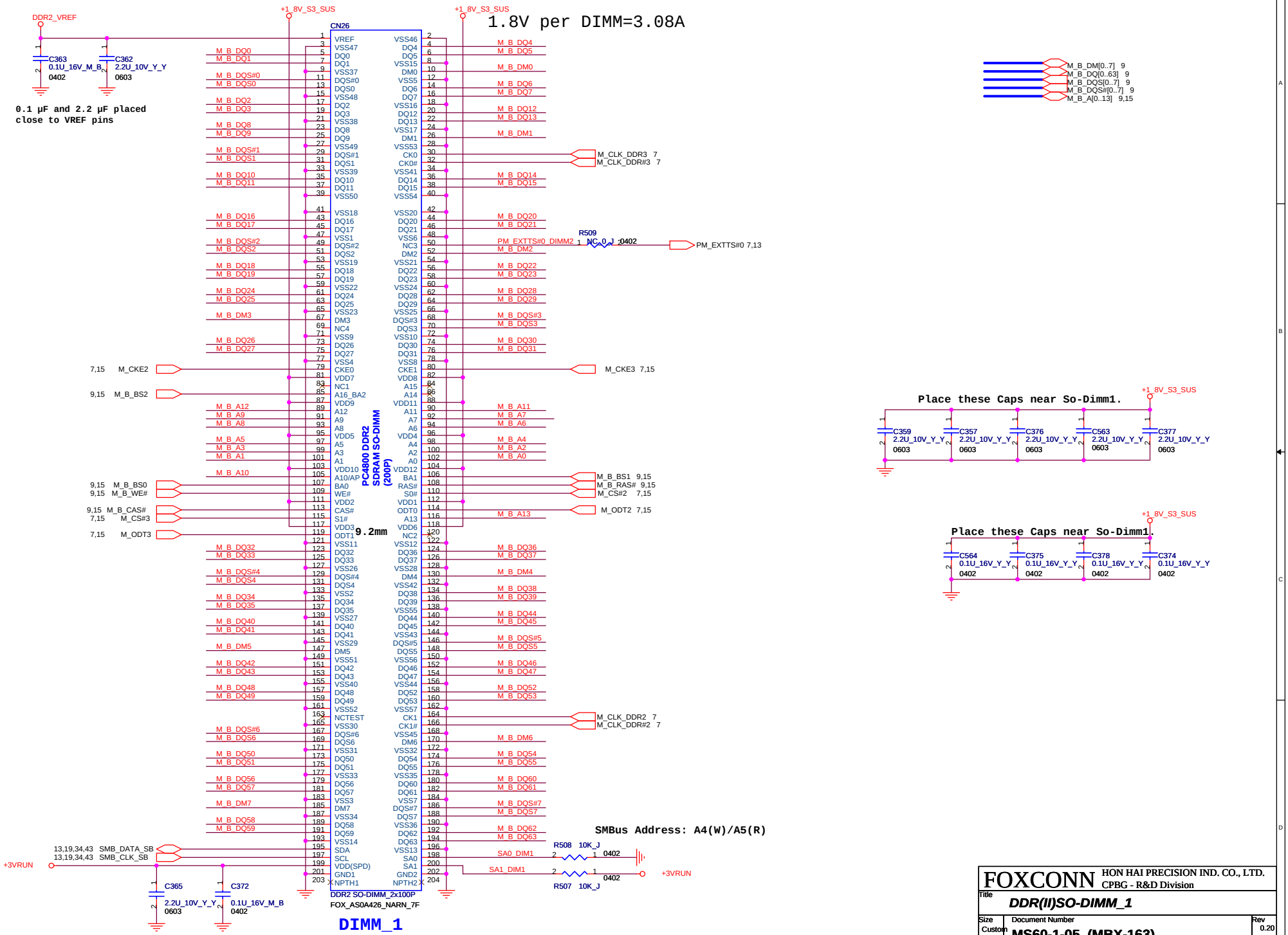
Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

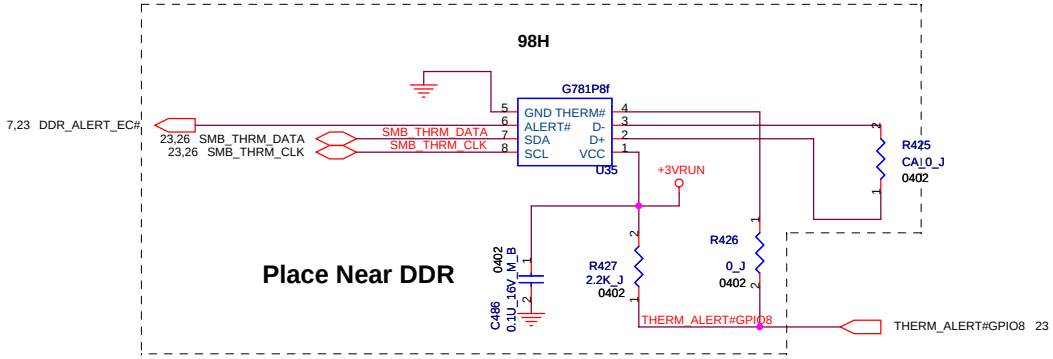
Date: Monday, June 19, 2006 | Sheet 12 of 47

1.8V per DIMM=3.08A



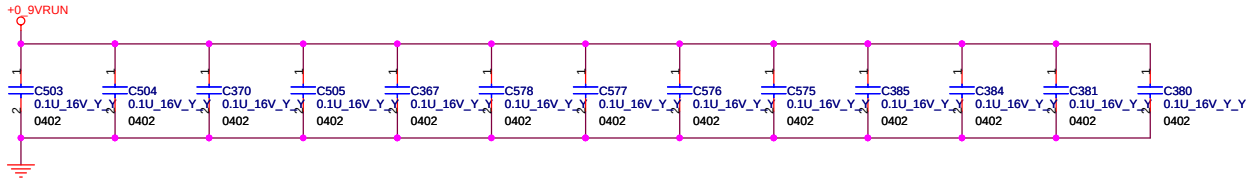
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	DDR(II)SO-DIMM_0
Size A3	Document Number MS60-1-05 (MBX-163) Rev 0.20
Date: Monday, June 19, 2006	Sheet 13 of 47


1.8V per DIMM=3.08A
DDR2_VREF
+1_8V_S3_SUS
CN26
C363 0.1U_16V_M_B 0402
C362 2.2U_10V_Y_Y 0603
0.1 µF and 2.2 µF placed close to VREF pins
PC4800 DDR2 SDRAM SO-DIMM (200P)
9.2mm
R509 NC_0_J 0402
PM_EXTTS#0_DIMM2
PM_EXTTS#0 7,13
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
M_CKE2 7,15
M_CKE3 7,15
M_B_BS1 9,15
M_B_RAS# 9,15
M_CS#2 7,15
M_ODT2 7,15
M_ODT3 7,15
M_B_BS0 9,15
M_B_WE# 9,15
M_B_CAS# 9,15
M_CS#3 7,15
M_B_BS2 9,15
M_B_DM[0..7] 9
M_B_DQ[0..63] 9
M_B_DQS[0..7] 9
M_B_DQS#[0..7] 9
M_B_A[0..13] 9,15
Place these Caps near So-Dimm1.
C359 2.2U_10V_Y_Y 0603
C357 2.2U_10V_Y_Y 0603
C376 2.2U_10V_Y_Y 0603
C563 2.2U_10V_Y_Y 0603
C377 2.2U_10V_Y_Y 0603
Place these Caps near So-Dimm1.
C564 0.1U_16V_Y_Y 0402
C375 0.1U_16V_Y_Y 0402
C378 0.1U_16V_Y_Y 0402
C374 0.1U_16V_Y_Y 0402
SMBus Address: A4(W)/A5(R)
13,19,34,43 SMB_DATA_SB
13,19,34,43 SMB_CLK_SB
+3VRUN
R508 10K_J 0402
R507 10K_J 0402
SA0_DIM1
SA1_DIM1
C365 2.2U_10V_Y_Y 0603
C372 0.1U_16V_M_B 0402
DDR2 SO-DIMM_2x100P
FOX_AS0A426_NARN_7F
DIMM_1
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
DDR(II)SO-DIMM_1
Size Custom
Document Number
MS60-1-05 (MBX-163)
Rev 0.20
Date: Monday, June 19, 2006
Sheet 14 of 47

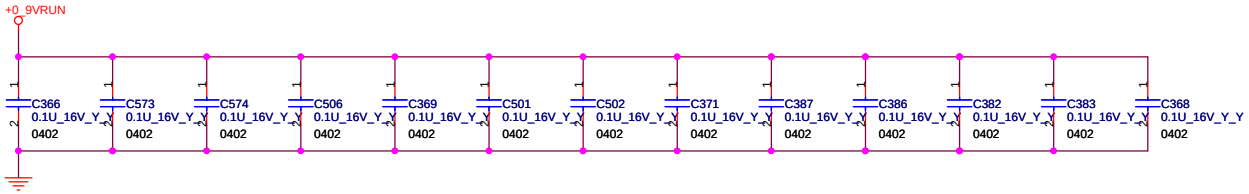


9,13 M_A_A[0..13]

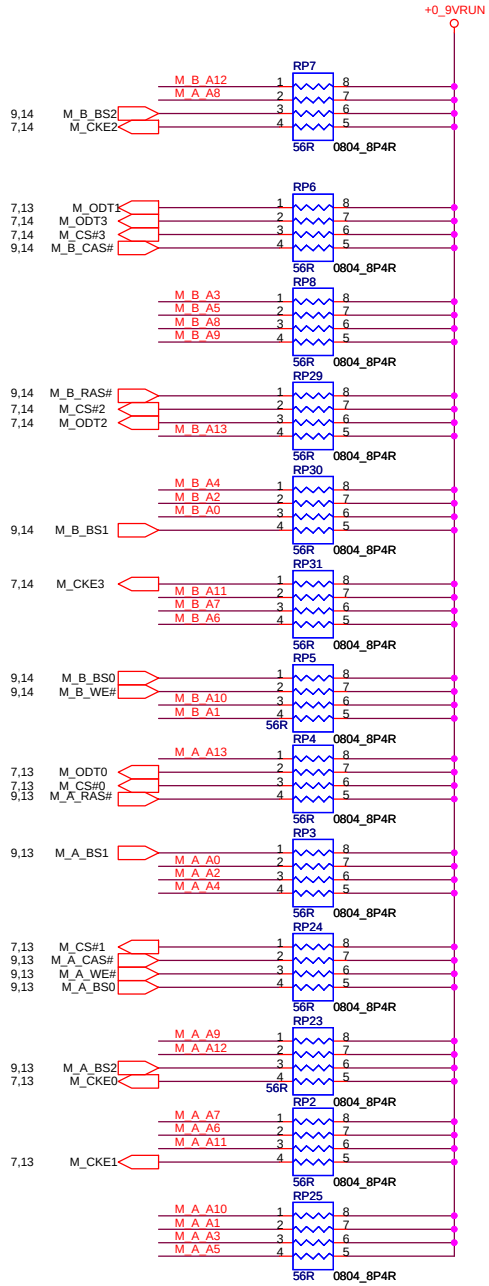
9,14 M_B_A[0..13]



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



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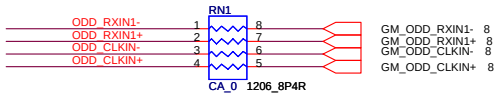
CPBG - R&D Division

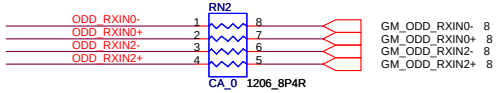
Title: ***DDR(II)Termination***

Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20

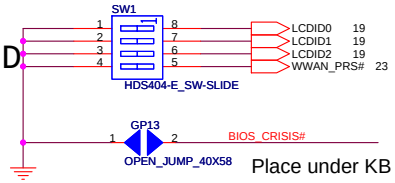
Date: Monday, June 19, 2006 Sheet 15 of 47

LVDS

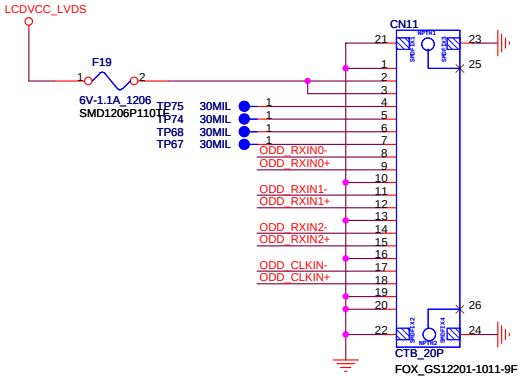




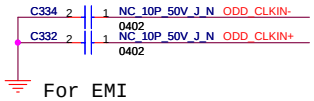
PANEL ID



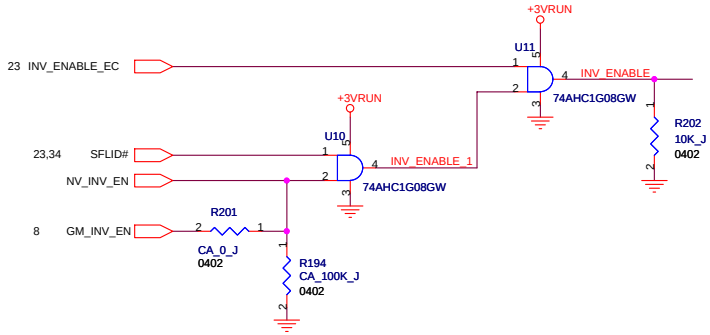
Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	



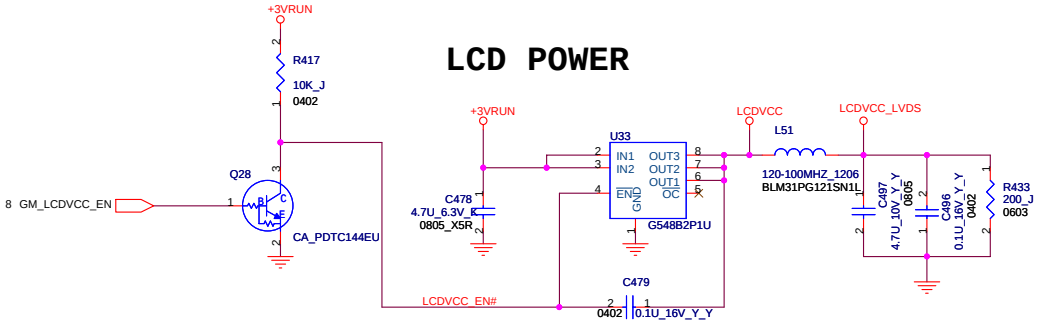
LVDS CONNECTOR

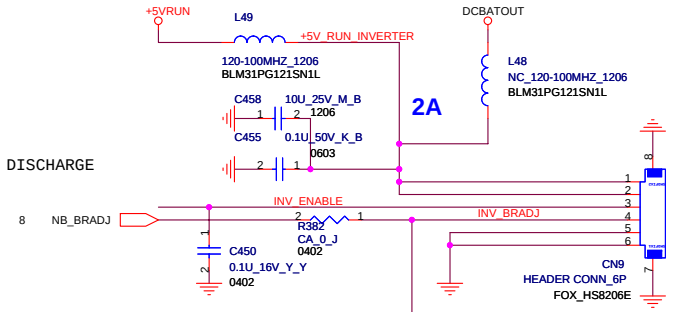


For EMI

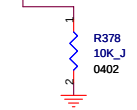


LCD POWER

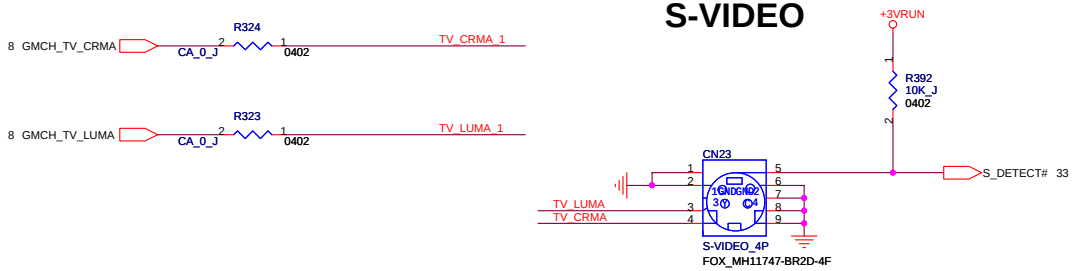


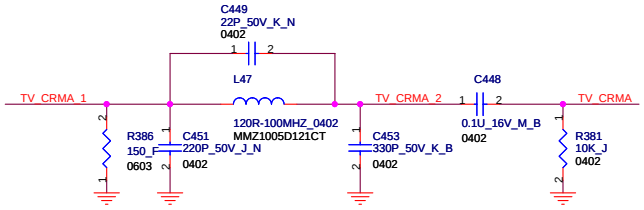


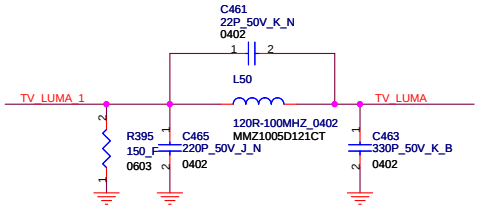
INVERTER CONNECTOR



S-VIDEO

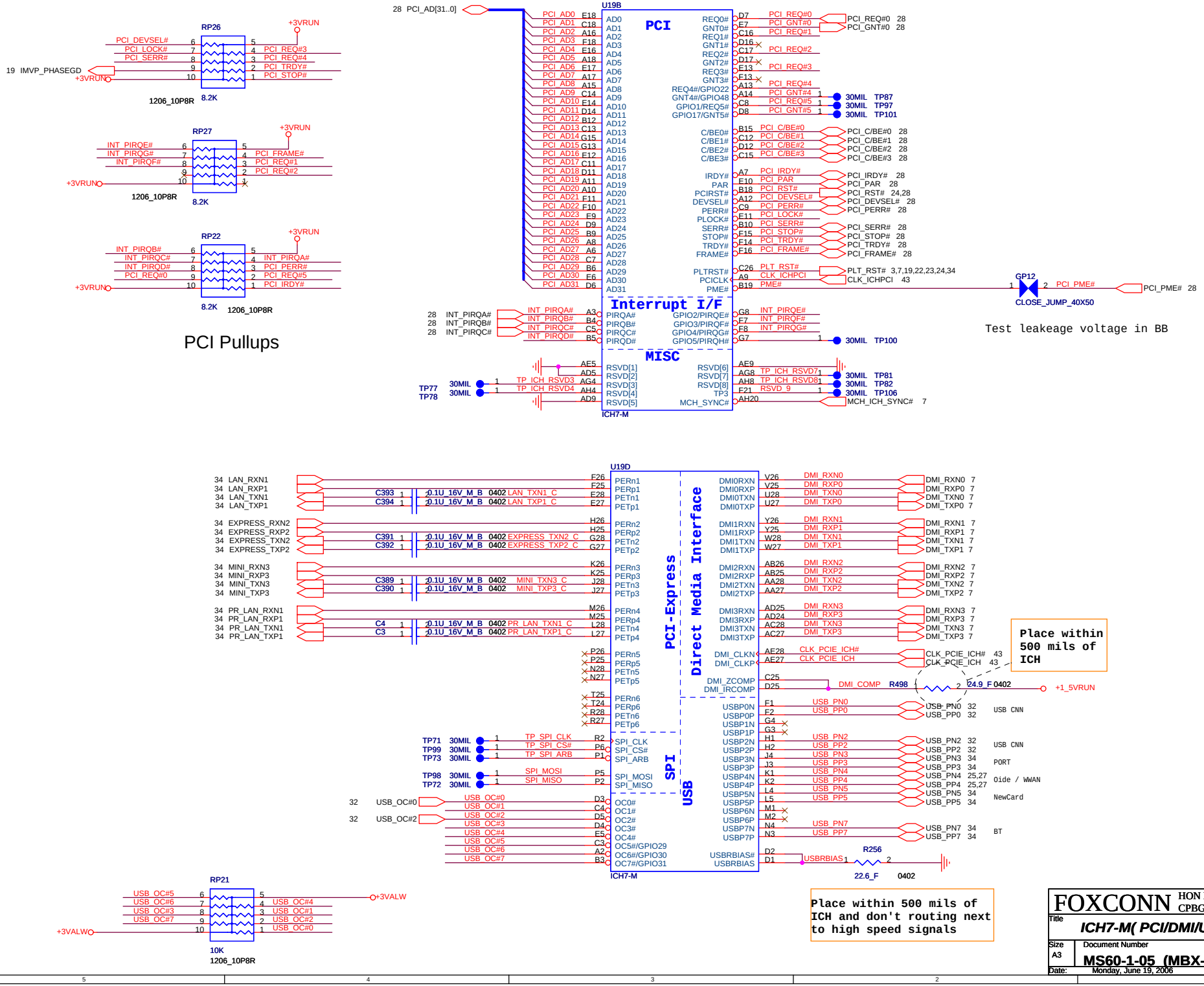


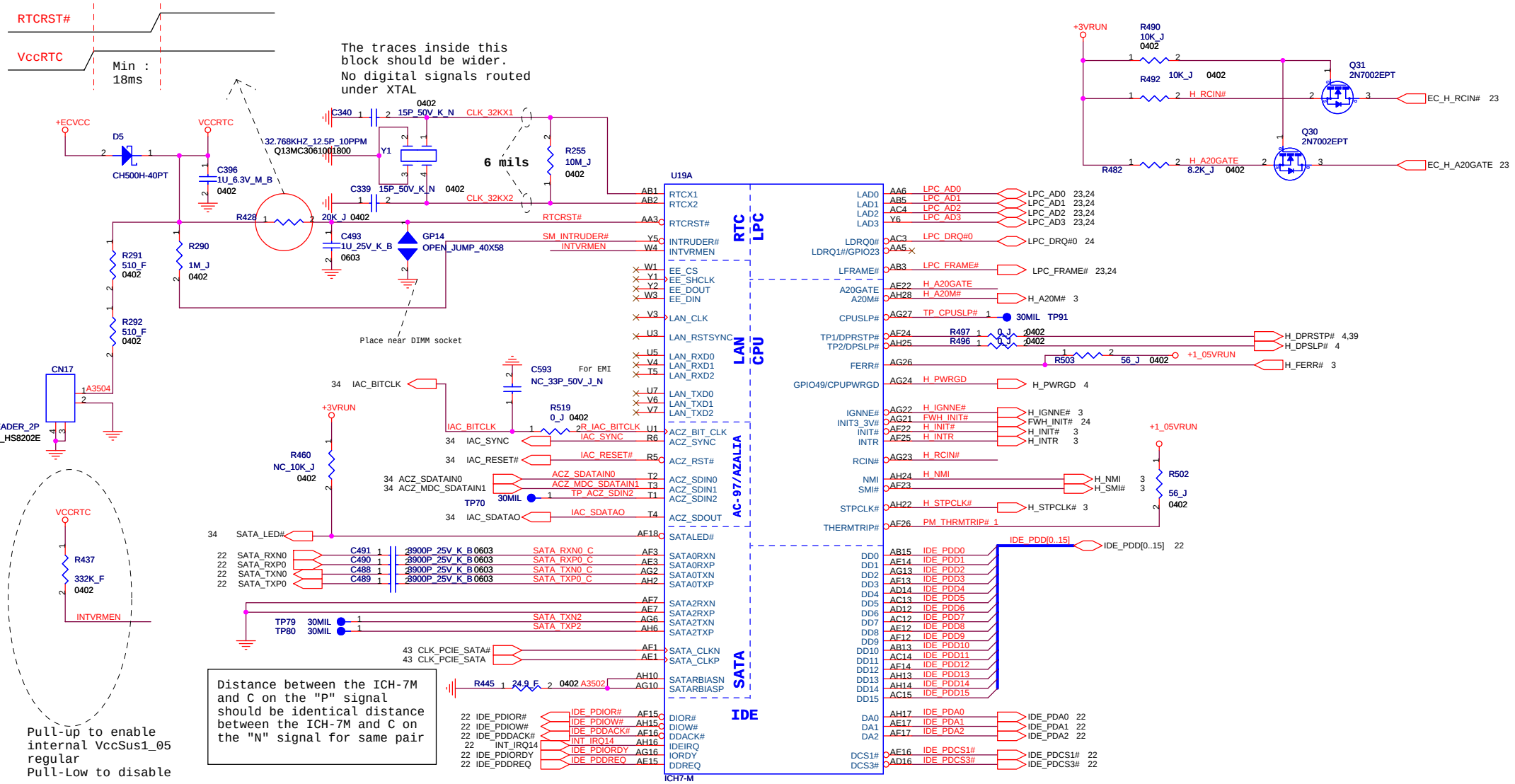




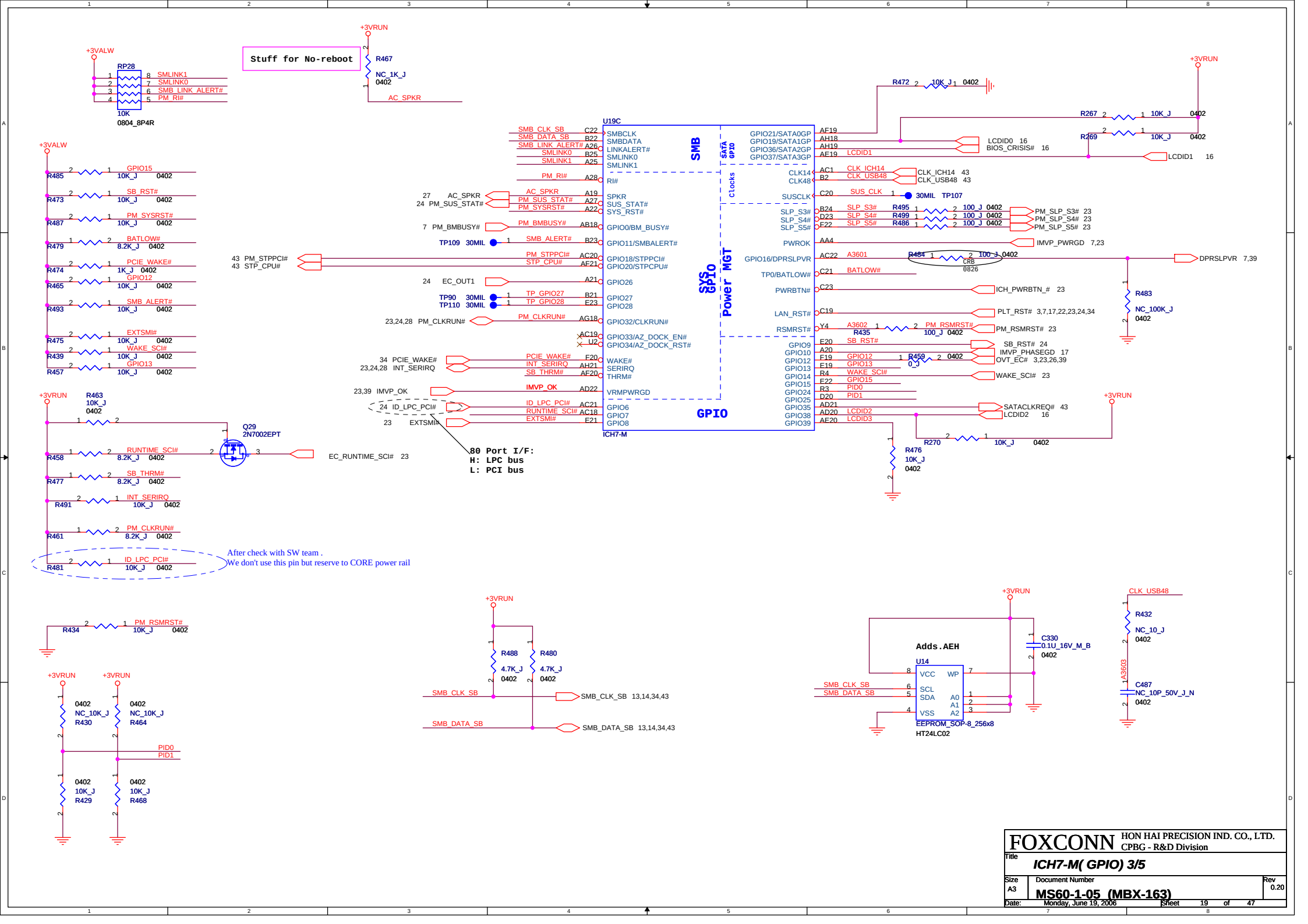
INVERTER CONNECTOR

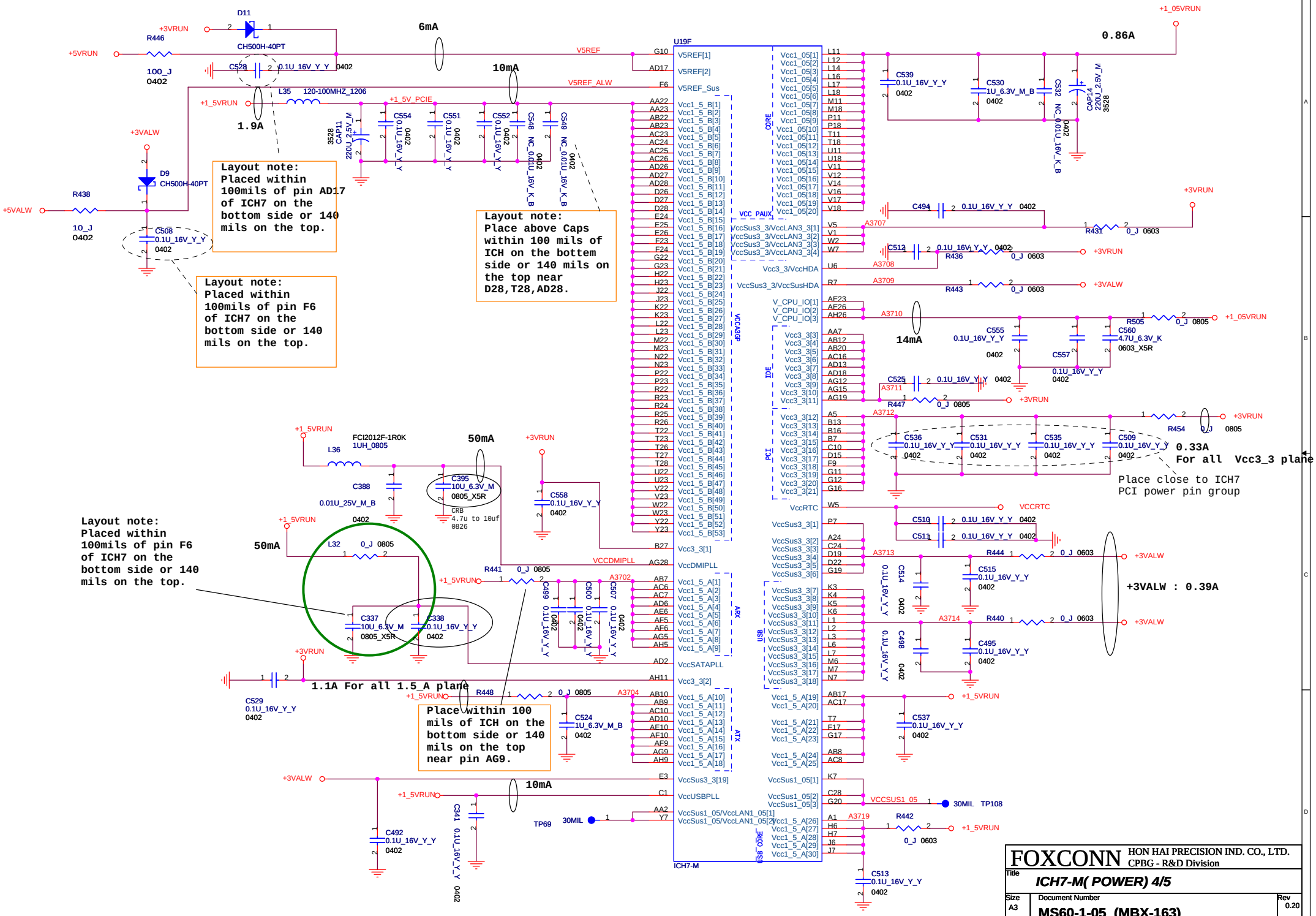
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	LVDS / S_VIDEO		
Size: Custom	Document Number: MS60-1-05 (MBX-163)		Rev: 0.20
Date: Monday, June 19, 2006	Sheet 16 of 47		

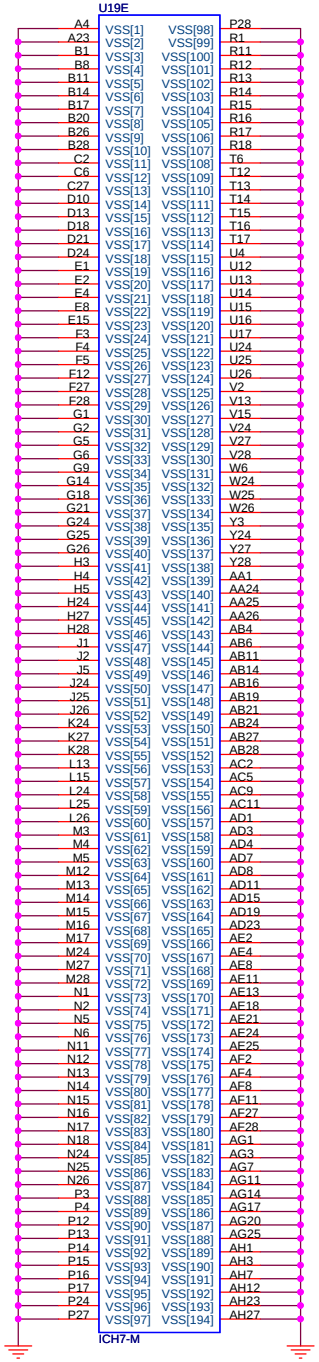

RP26
RP27
RP22
RP21
1206_10P8R
8.2K
10K
+3VRUN
+3VALW
PCI_DEVSEL#
PCI_LOCK#
PCI_SERR#
PCI_REQ#3
PCI_REQ#4
PCI_TRDY#
PCI_STOP#
19 IMVP_PHASEGD
INT_PIRQE#
INT_PIRQG#
INT_PIRQF#
PCI_FRAME#
PCI_REQ#1
PCI_REQ#2
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
PCI_REQ#0
INT_PIRQA#
PCI_PERR#
PCI_REQ#5
PCI_IRDY#
USB_OC#5
USB_OC#6
USB_OC#3
USB_OC#7
USB_OC#4
USB_OC#1
USB_OC#2
USB_OC#0
PCI Pullups
U19B
PCI
Interrupt I/F
MISC
ICH7-M
28 PCI_AD[31..0]
PCI_REQ#0 28
PCI_GNT#0 28
PCI_C/BE#0 28
PCI_C/BE#1 28
PCI_C/BE#2 28
PCI_C/BE#3 28
PCI_IRDY# 28
PCI_PAR 28
PCI_RST# 24,28
PCI_DEVSEL# 28
PCI_PERR# 28
PCI_SERR# 28
PCI_STOP# 28
PCI_TRDY# 28
PCI_FRAME# 28
PLT_RST# 3,7,19,22,23,24,34
CLK_ICHPCI 43
PME# 28
30MIL TP87
30MIL TP97
30MIL TP101
30MIL TP100
30MIL TP81
30MIL TP82
30MIL TP106
MCH_ICH_SYNC# 7
TP77
TP78
GP12
CLOSE_JUMP_40X50
Test leakeage voltage in BB
U19D
PCI-Express
Direct Media Interface
SPI
USB
ICH7-M
LAN_RXN1
LAN_RXP1
LAN_TXN1
LAN_TXP1
EXPRESS_RXN2
EXPRESS_RXP2
EXPRESS_TXN2
EXPRESS_TXP2
MINI_RXN3
MINI_RXP3
MINI_TXN3
MINI_TXP3
PR_LAN_RXN1
PR_LAN_RXP1
PR_LAN_TXN1
PR_LAN_TXP1
0.1U_16V_M_B 0402
LAN_TXN1_C
LAN_TXP1_C
EXPRESS_TXN2_C
EXPRESS_TXP2_C
MINI_TXN3_C
MINI_TXP3_C
PR_LAN_TXN1_C
PR_LAN_TXP1_C
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
CLK_PCIE_ICH#
CLK_PCIE_ICH
DMI_COMP
R498
24.9_F 0402
+1_5VRUN
Place within 500 mils of ICH
USB_PN0
USB_PP0
USB_PN2
USB_PP2
USB_PN3
USB_PP3
USB_PN4
USB_PP4
USB_PN5
USB_PP5
USB_PN7
USB_PP7
USB CNN
PORT
Oide / WWAN
NewCard
BT
TP_SPI_CLK
TP_SPI_CS#
TP_SPI_ARB
SPI_MOSI
SPI_MISO
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USBRBIAS
R256
22.6_F 0402
Place within 500 mils of ICH and don't routing next to high speed signals
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
ICH7-M(PCI/DMI/USB/PCIE) 1/5
Size A3
Document Number
MS60-1-05 (MBX-163)
Rev 0.20
Date: Monday, June 19, 2006
Sheet 17 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	ICH7-M(LPC,IDE,SATA) 2/5	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 18 of 47	


Stuff for No-reboot
R467
NC_1K_J
0402
AC_SPKR
+3VRUN
+3VALW
RP28
SMLINK1
SMLINK0
SMB_LINK_ALERT#
PM_RI#
10K
0804_8P4R
U19C
SMB
SYS GPIO
Power MGT
GPIO
Clocks
SATA GPIO
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
ICH7-M
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
80 Port I/F:
H: LPC bus
L: PCI bus
Q29
2N7002EPT
After check with SW team .
We don't use this pin but reserve to CORE power rail
Adds.AEH
U14
EEPROM_SOP-8_256x8
HT24LC02
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH7-M(GPIO) 3/5
MS60-1-05 (MBX-163)
Rev 0.20
Monday, June 19, 2006
Sheet 19 of 47

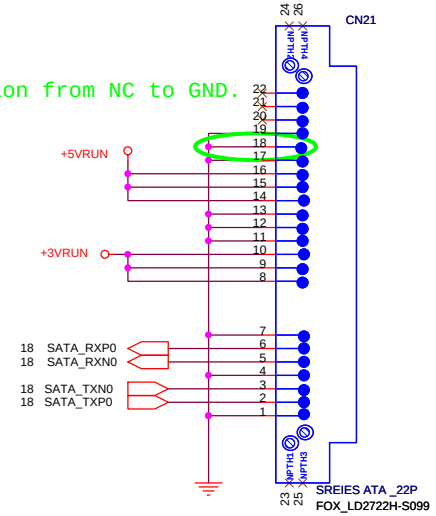

Layout note: Placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top.
Layout note: Place above Caps within 100 mils of ICH on the bottem side or 140 mils on the top near D28,T28,AD28.
Layout note: Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.
Layout note: Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.
1.1A For all 1.5_A plane
0.33A For all Vcc3_3 plane
Place close to ICH7 PCI power pin group
+3VALW : 0.39A
0.86A
14mA
50mA
10mA
6mA
1.9A
ICH7-M
U19F
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH7-M(POWER) 4/5
MS60-1-05 (MBX-163)
Rev 0.20
Monday, June 19, 2006
Sheet 20 of 47

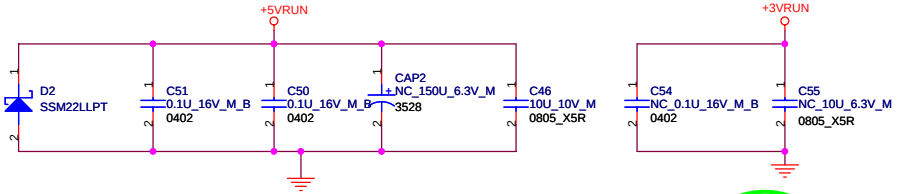


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*ICH7-M(GND) 5/5*	
Size A3	Document Number **MS60-1-05 (MBX-163)**	Rev 0.20
Date: Monday, June 19, 2006	Sheet 21 of 47	

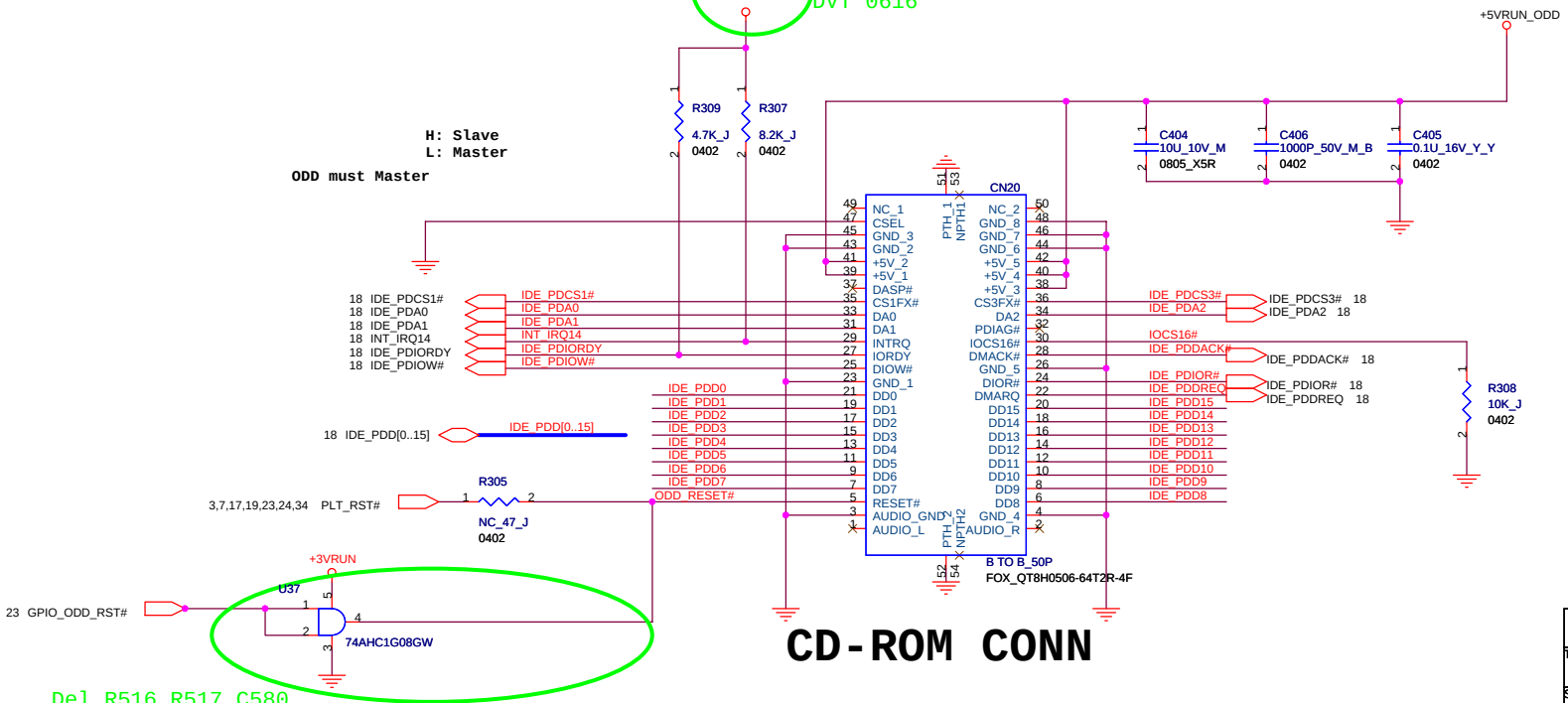
SATA HDD CONN

CN21's pin18 change connection from NC to GND.
DVT 0616





Change from +3VRUN to +3VRUN_ODD
DVT 0616



CD-ROM CONN

Del R516,R517,C580
DVT 0615

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SATA HDD/CD-ROM	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 22 of 47	

Consider short FB after BB test.

FOX_GB21240-0002-7F
FPC CONN_24P
CN4

RP1 10K 0804_8P4R

U16
KB3910SFC1

MODEL ID check with software define

M-ID	0	1	2	3	4	5	
MS60-L	1	0	1	1	1	0	940GML
MS60-H	0	1	1	1	1	0	945PM
MS60-M	1	1	1	1	1	0	945GM

M-ID 5: 0- MS60 and the following MS60 type
1- MS70 and the following MS70 type
M-ID 2~4: 1- Reserved
M-ID 1: 0- Intel 940 series
1- Intel 945 series
M-ID 0: 0- External Gfx.
1- Internal Gfx.

Add R521 DVT 0615

change R244 connection form ''ALW_ON'' to ''ALW_ON_1'' DVT 0615

PORT_DET# change from pin81 to pin176 TP85 change from pin176 to pin81 DVT 0616

Add VISTA_SUPPORT# for Vista. DVT 0616

Add GPIO_ODD_RST# for ODD reset. DVT 0615

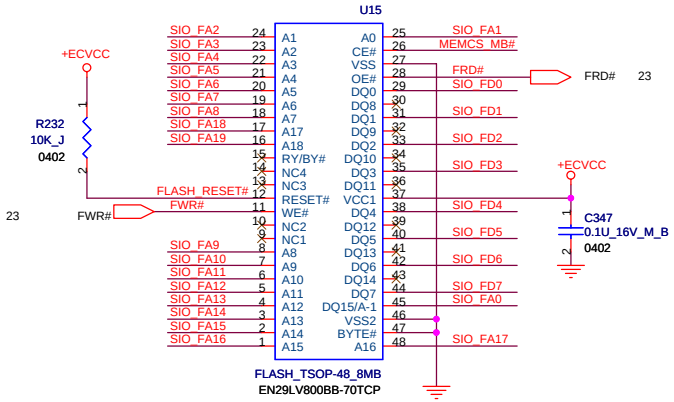
FOR EMI

CN3
FPC_12P
FOX_GB5RF120-1200-7F

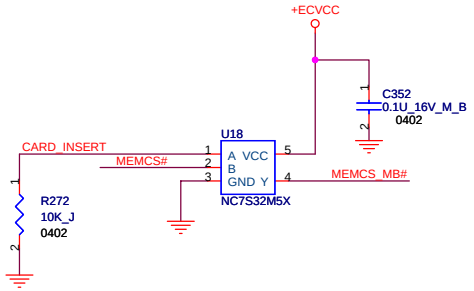
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	EC+KBC	
Size: Custom	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 23 of 47	

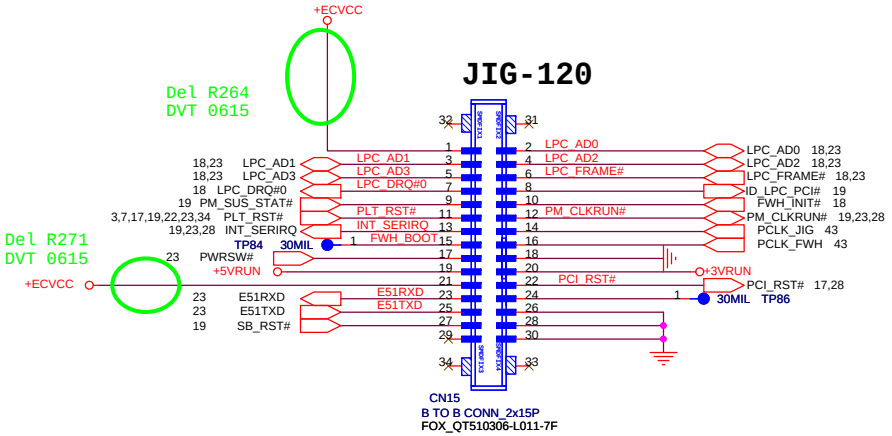
23 SIO_FA[19..0]

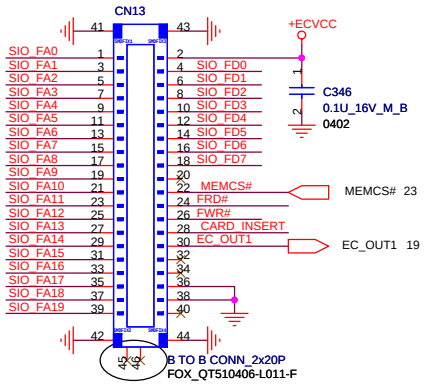
23 SIO_FD[7..0]



BIOS ROM





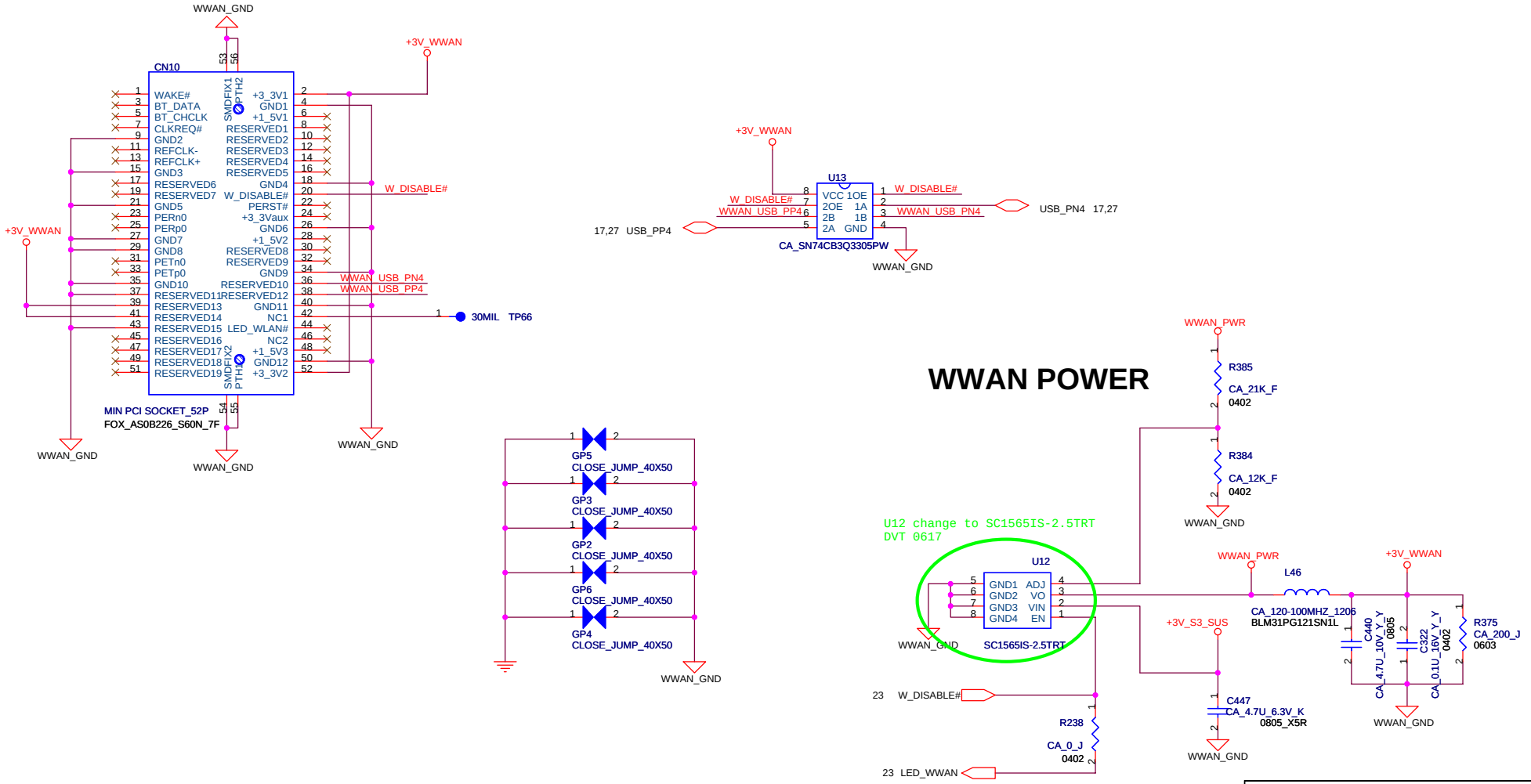


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *Flash ROM/X-Bus CONN*

Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20

Date: Monday, June 19, 2006 Sheet 24 of 47



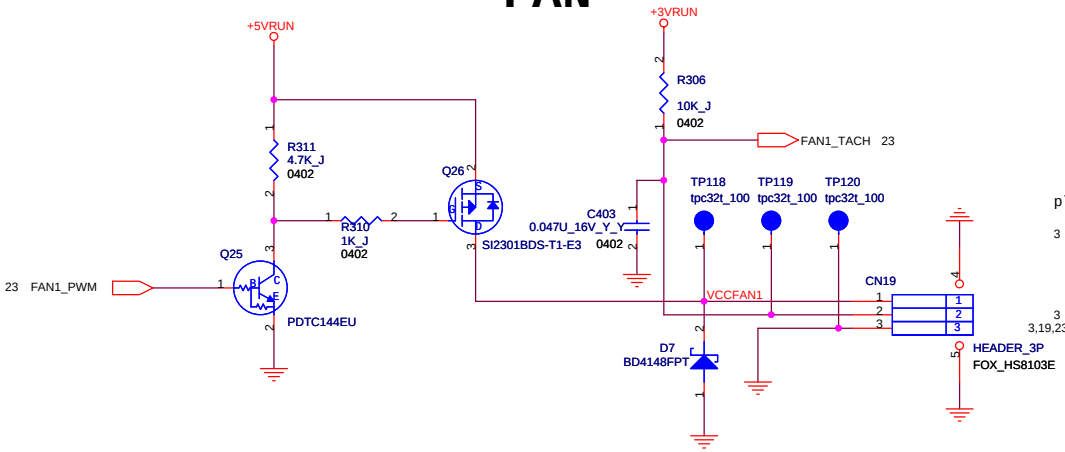
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: WWAN

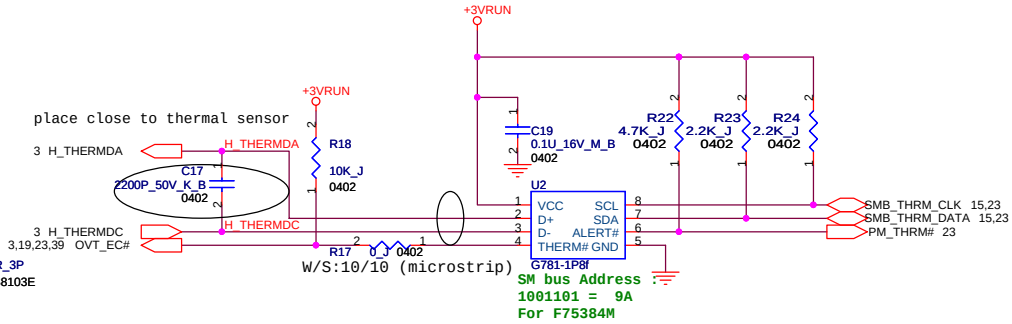
Size: Custom | Document Number: MS60-1-05_(MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 25 of 47

FAN

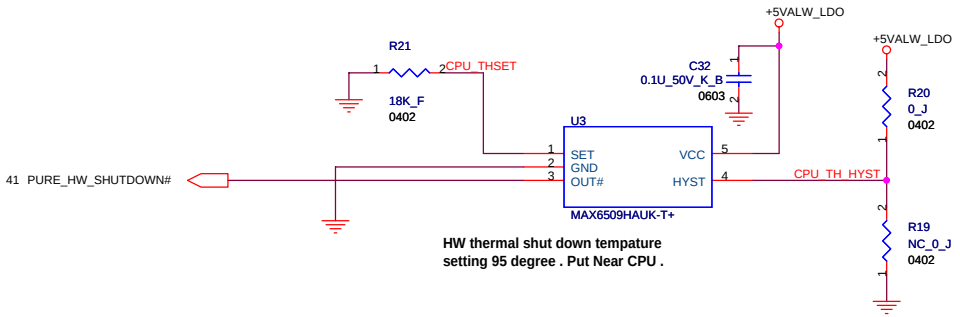


CPU SENSOR



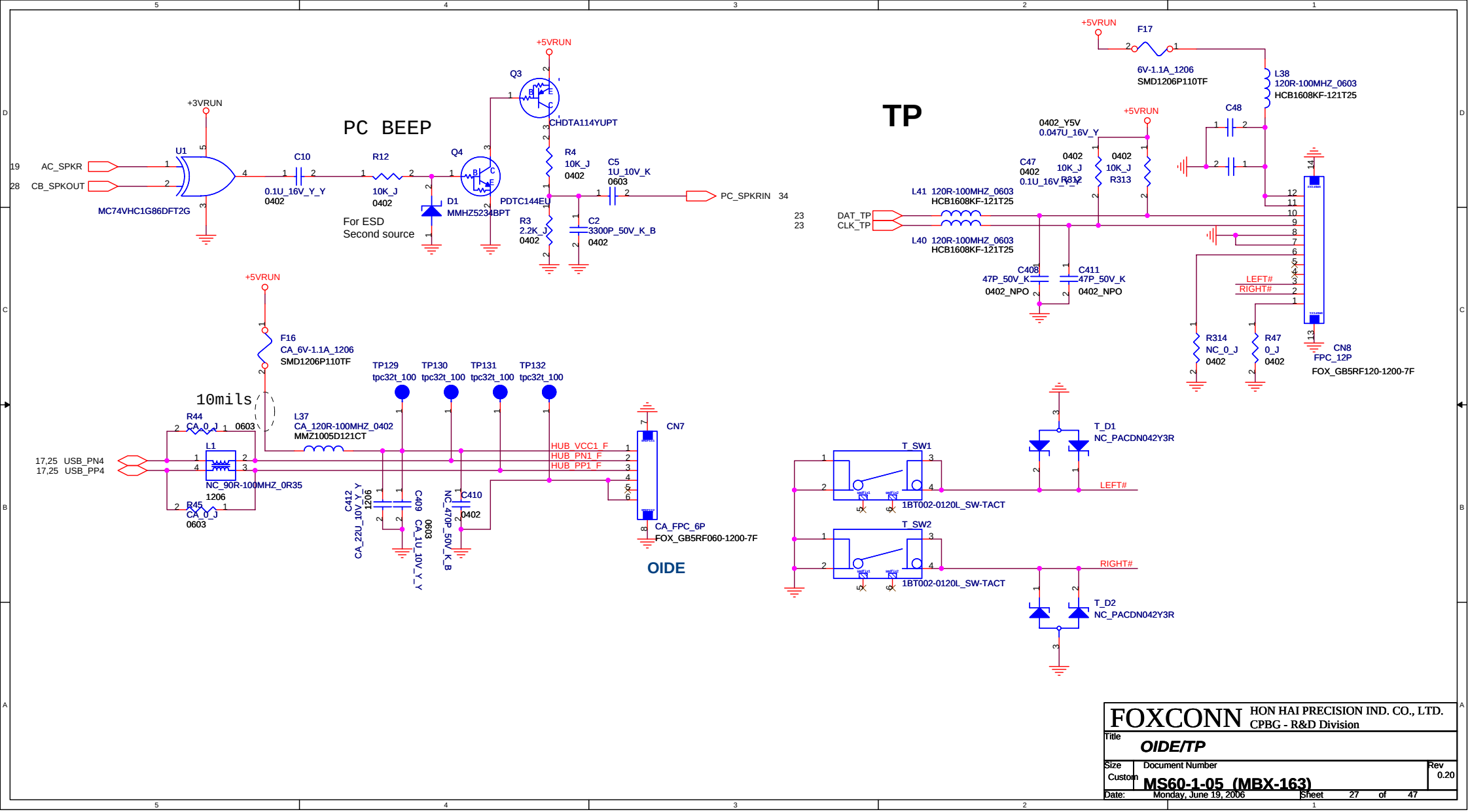
Place Thermal-Sensor near CPU & GMCH.

HW THERMAL PROTECTION

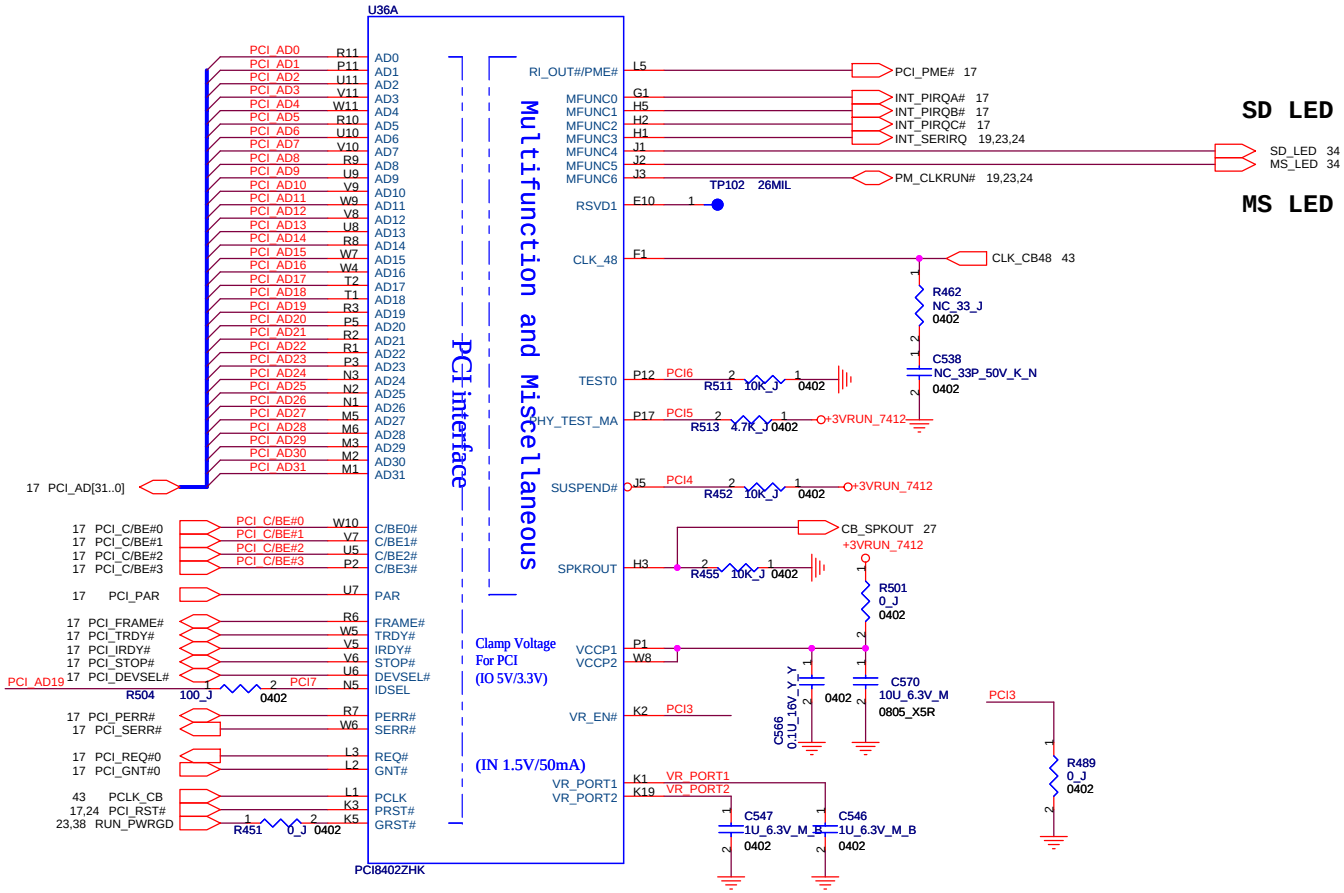


HW thermal shut down tempature setting 95 degree . Put Near CPU .

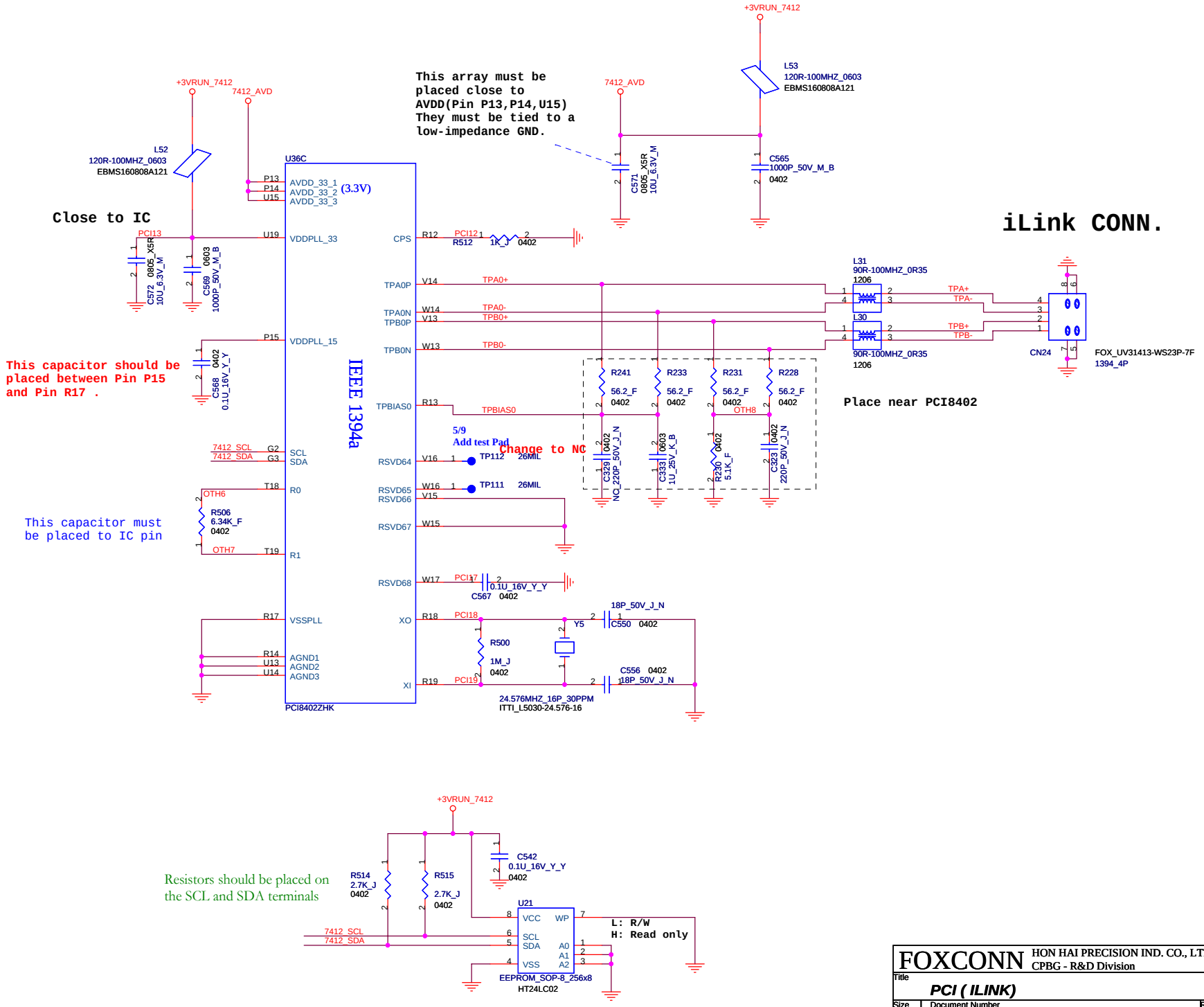
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	FAN/HW THERMAL PROTECT	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 26 of 47	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	OIDE/TP	
Size: Custom	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 27 of 47	

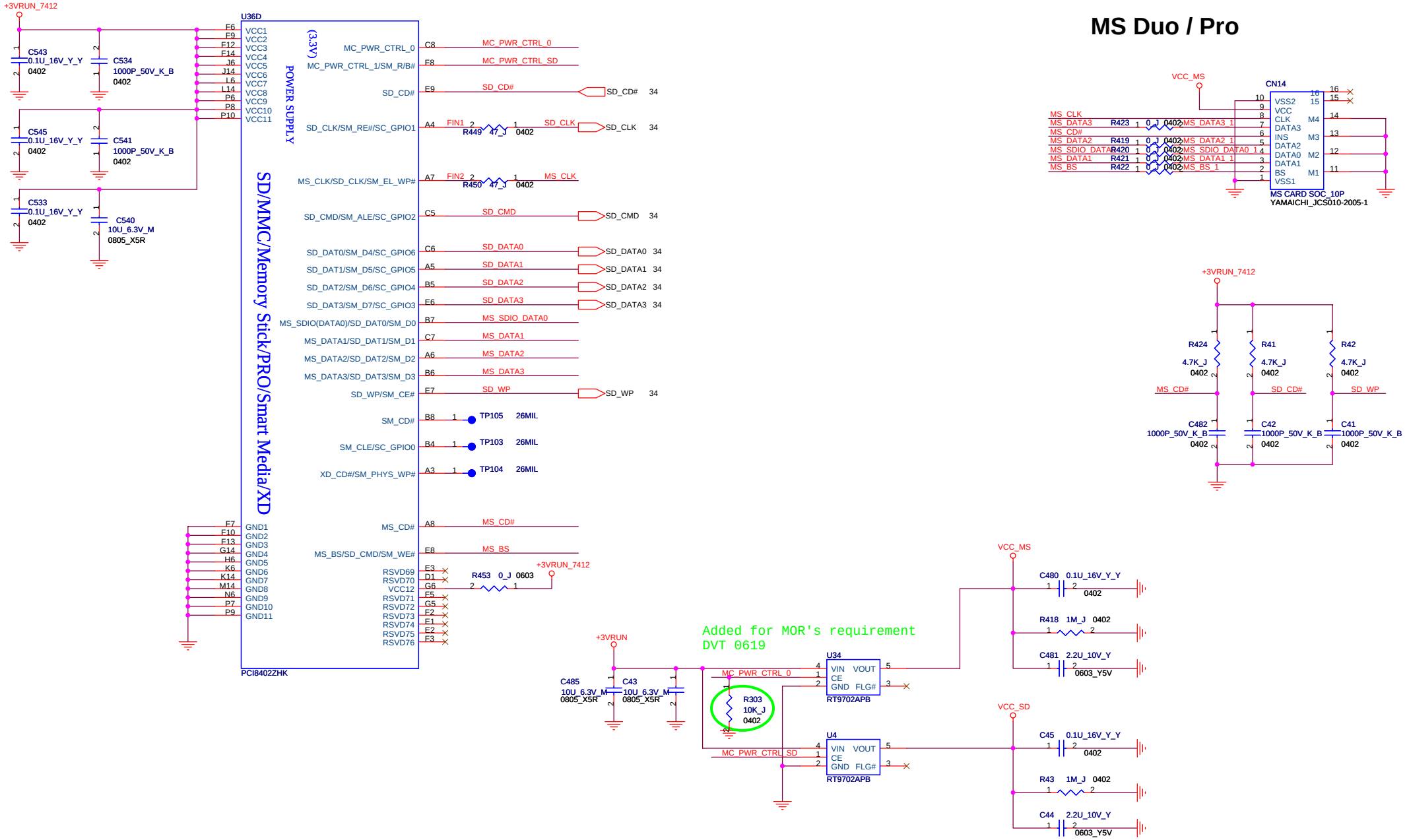


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: PCI (PCI BUS)			
Size: A3	Document Number: MS60-1-05 (MBX-163)		Rev: 0.20
Date: Monday, June 19, 2006	Sheet 28 of 47		

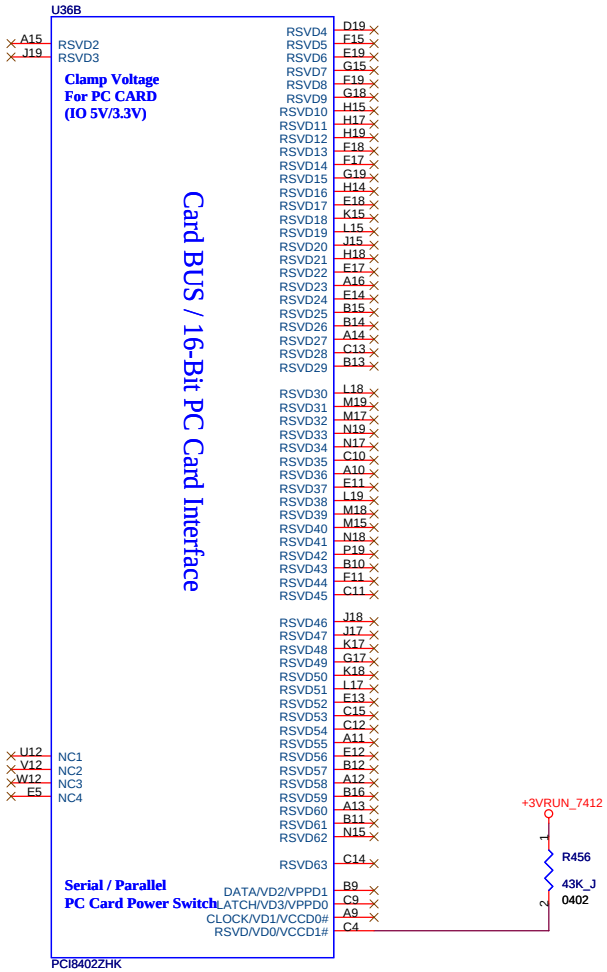


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (ILINK)
Size A3	Document Number MS60-1-05 (MBX-163) Rev 0.20
Date: Monday, June 19, 2006	Sheet 29 of 47

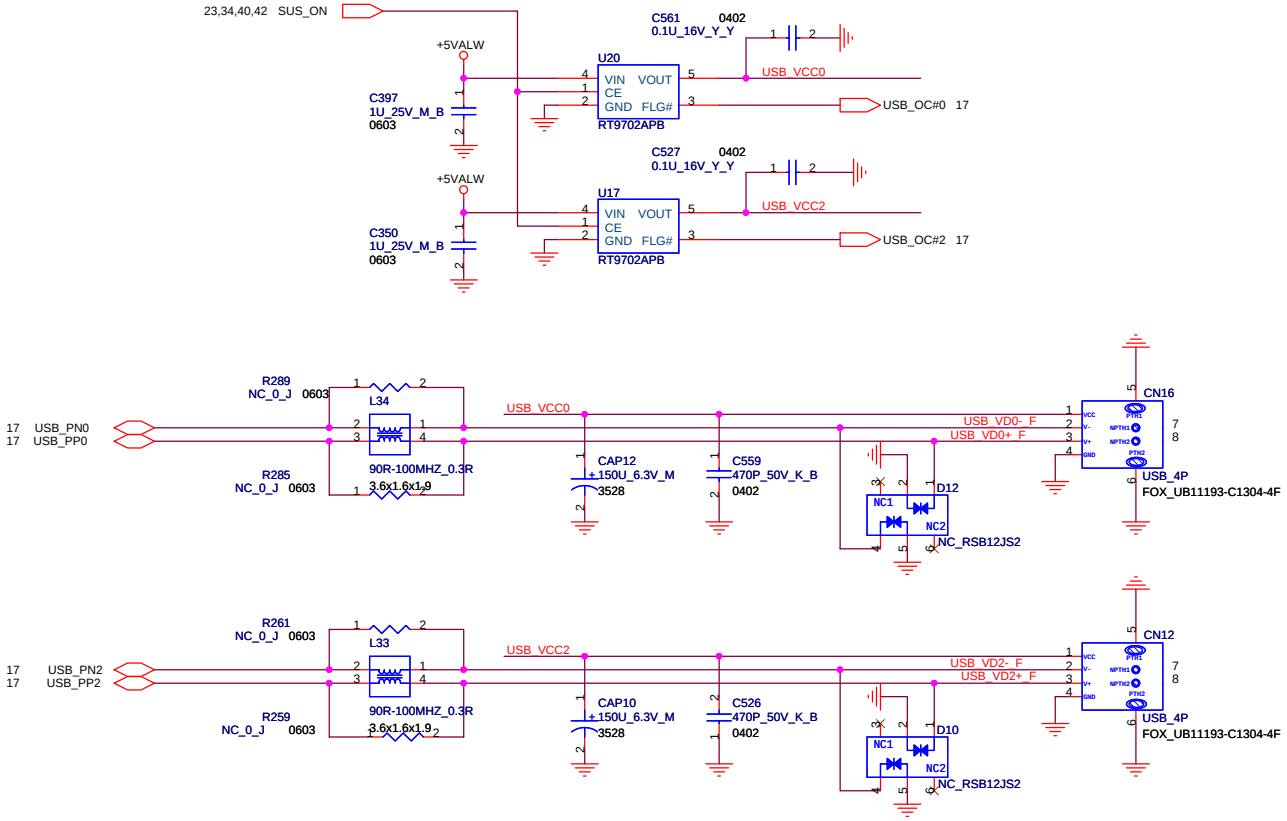
MS Duo / Pro



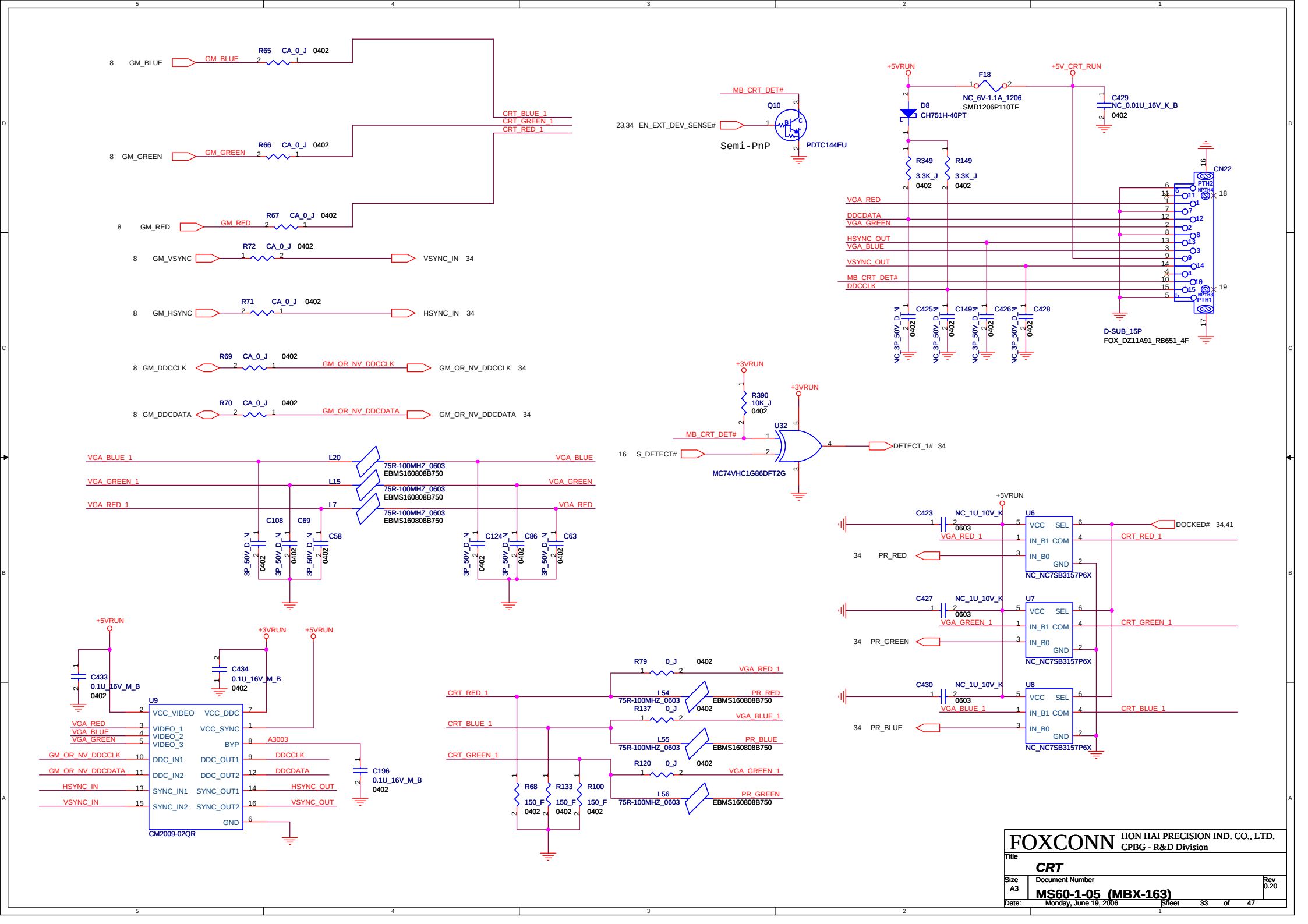
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (MS)	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 30 of 47	



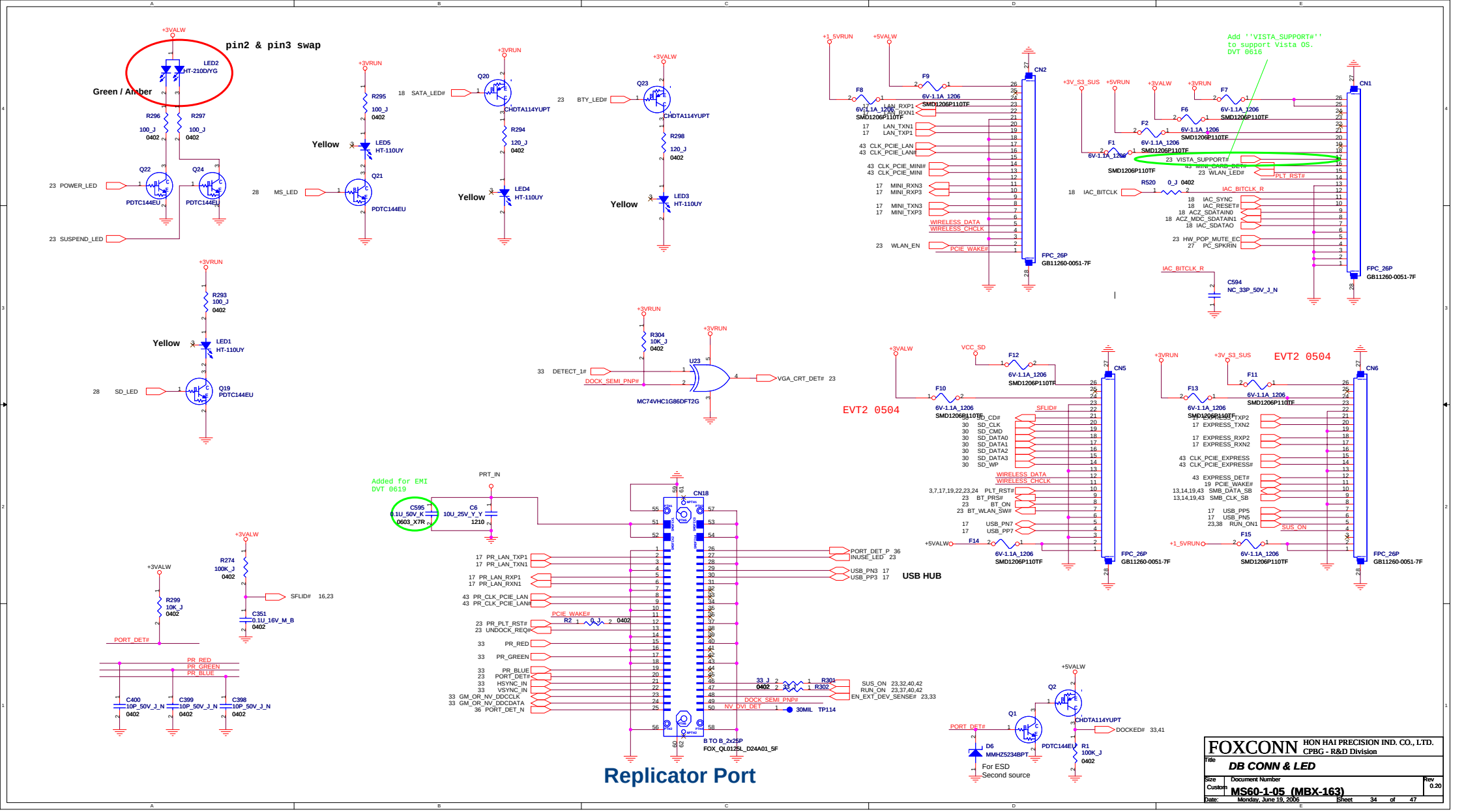
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCI (PCMCIA)		
Size: A3	Document Number: MS60	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 31 of 47	

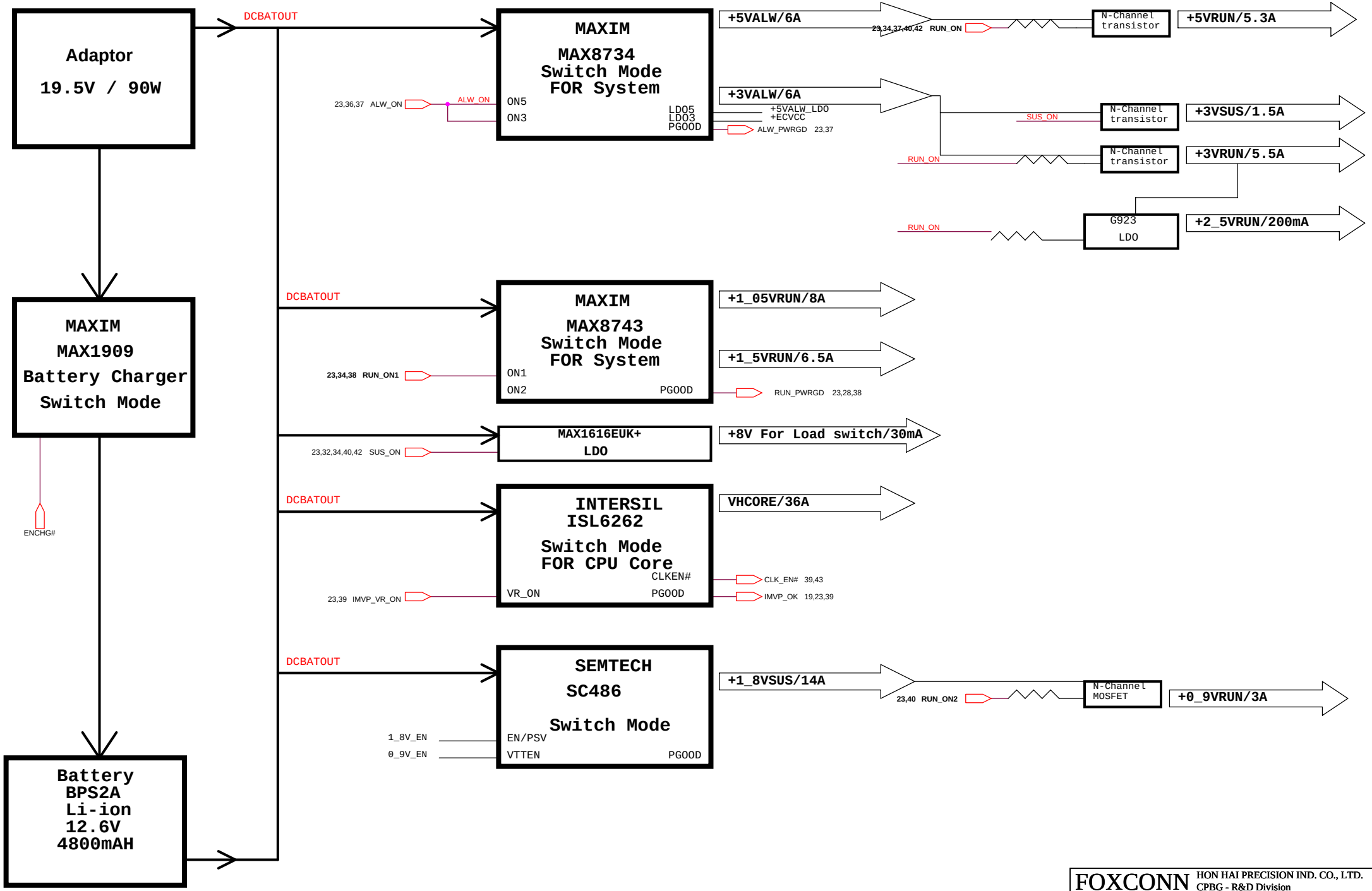


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***USB2.0/DOCKING CONN.***	
Size A3	Document Number **MS60-1-05 (MBX-163)**	Rev 0.20
Date: Monday, June 19, 2006	Sheet 32 of 47	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: CRT			
Size: A3	Document Number: MS60-1-05 (MBX-163)		Rev: 0.20
Date: Monday, June 19, 2006	Sheet 33 of 47		


pin2 & pin3 swap
Green / Amber
LED2 HT-210D/YG
R296 100_J 0402
R297 100_J 0402
Q22 PDTC144EU
Q24 PDTC144EU
23 POWER_LED
23 SUSPEND_LED
Yellow
LED5 HT-110UY
R295 100_J 0402
Q21 PDTC144EU
28 MS_LED
Yellow
LED4 HT-110UY
Q20 CHDTA114YUPT
R294 120_J 0402
18 SATA_LED#
Yellow
LED3 HT-110UY
Q23 CHDTA114YUPT
R298 120_J 0402
23 BTY_LED#
Yellow
LED1 HT-110UY
R293 100_J 0402
Q19 PDTC144EU
28 SD_LED
R304 10K_J 0402
U23 MC74VHC1G86DFT2G
33 DETECT_1#
DOCK_SEMI_PNP#
VGA_CRT_DET# 23
CN2 FPC_26P GB11260-0051-7F
F8 F9 6V-1.1A_1206 SMD1206P110TF
LAN_RXP1 LAN_RXN1 LAN_TXN1 LAN_TXP1
CLK_PCIE_LAN CLK_PCIE_LAN#
CLK_PCIE_MINI# CLK_PCIE_MINI
MINI_RXN3 MINI_RXP3 MINI_TXN3 MINI_TXP3
WIRELESS_DATA WIRELESS_CHCLK
WLAN_EN PCIE_WAKE#
Add ''VISTA_SUPPORT#'' to support Vista OS. DVT 0616
CN1 FPC_26P GB11260-0051-7F
F1 F2 F6 F7 6V-1.1A_1206 SMD1206P110TF
VISTA_SUPPORT# MINI_CARD_DET# WLAN_LED#
PLT_RST#
IAC_BITCLK R520 0_J 0402
IAC_SYNC IAC_RESET# ACZ_SDATAIN0 ACZ_MDC_SDATAIN1 IAC_SDATAO
HW_POP_MUTE_EC PC_SPKRIN
IAC_BITCLK_R C594 NC_33P_50V_J_N
EVT2 0504
CN5 FPC_26P GB11260-0051-7F
F10 F12 6V-1.1A_1206 SMD1206P110TF
SD_CD# SD_CLK SD_CMD SD_DATA0 SD_DATA1 SD_DATA2 SD_DATA3 SD_WP
SFLID#
WIRELESS_DATA WIRELESS_CHCLK
PLT_RST# BT_PRS# BT_ON BT_WLAN_SW#
USB_PN7 USB_PP7
F14
EVT2 0504
CN6 FPC_26P GB11260-0051-7F
F11 F13 F15 6V-1.1A_1206 SMD1206P110TF
EXPRESS_TXP2 EXPRESS_TXN2 EXPRESS_RXP2 EXPRESS_RXN2
CLK_PCIE_EXPRESS CLK_PCIE_EXPRESS#
EXPRESS_DET# PCIE_WAKE# SMB_DATA_SB SMB_CLK_SB
USB_PP5 USB_PN5 RUN_ON1
SUS_ON
USB HUB
Added for EMI DVT 0619
PRT_IN
C595 0.1U_50V_K 0603_X7R
C6 10U_25V_Y_Y 1210
CN18 B TO B_2x25P FOX_QL0125L_D24A01_5F
PR_LAN_TXP1 PR_LAN_TXN1 PR_LAN_RXP1 PR_LAN_RXN1
PR_CLK_PCIE_LAN PR_CLK_PCIE_LAN#
PCIE_WAKE# R2 0_J 0402
PR_PLT_RST# UNDOCK_REQ#
PR_RED PR_GREEN PR_BLUE PORT_DET# HSYNC_IN VSYNC_IN
GM_OR_NV_DDCCLK GM_OR_NV_DDCDATA PORT_DET_N
PORT_DET_P INUSE_LED
USB_PN3 USB_PP3
R301 R302 33_J 0402
SUS_ON RUN_ON EN_EXT_DEV_SENSE#
DOCK_SEMI_PNP#
NV_DVI_DET
30MIL TP114
R299 10K_J 0402
R274 100K_J 0402
SFLID# 16,23
C351 0.1U_16V_M_B 0402
PORT_DET#
PR_RED PR_GREEN PR_BLUE
C400 C399 C398 10P_50V_J_N 0402
Q2 Q1 CHDTA114YUPT
PORT_DET#
D6 MMHZ5234BPT
For ESD Second source
R1 100K_J 0402
DOCKED# 33,41
Replicator Port
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
DB CONN & LED
Size Custom
Document Number MS60-1-05 (MBX-163)
Rev 0.20
Date: Monday, June 19, 2006
Sheet 34 of 47

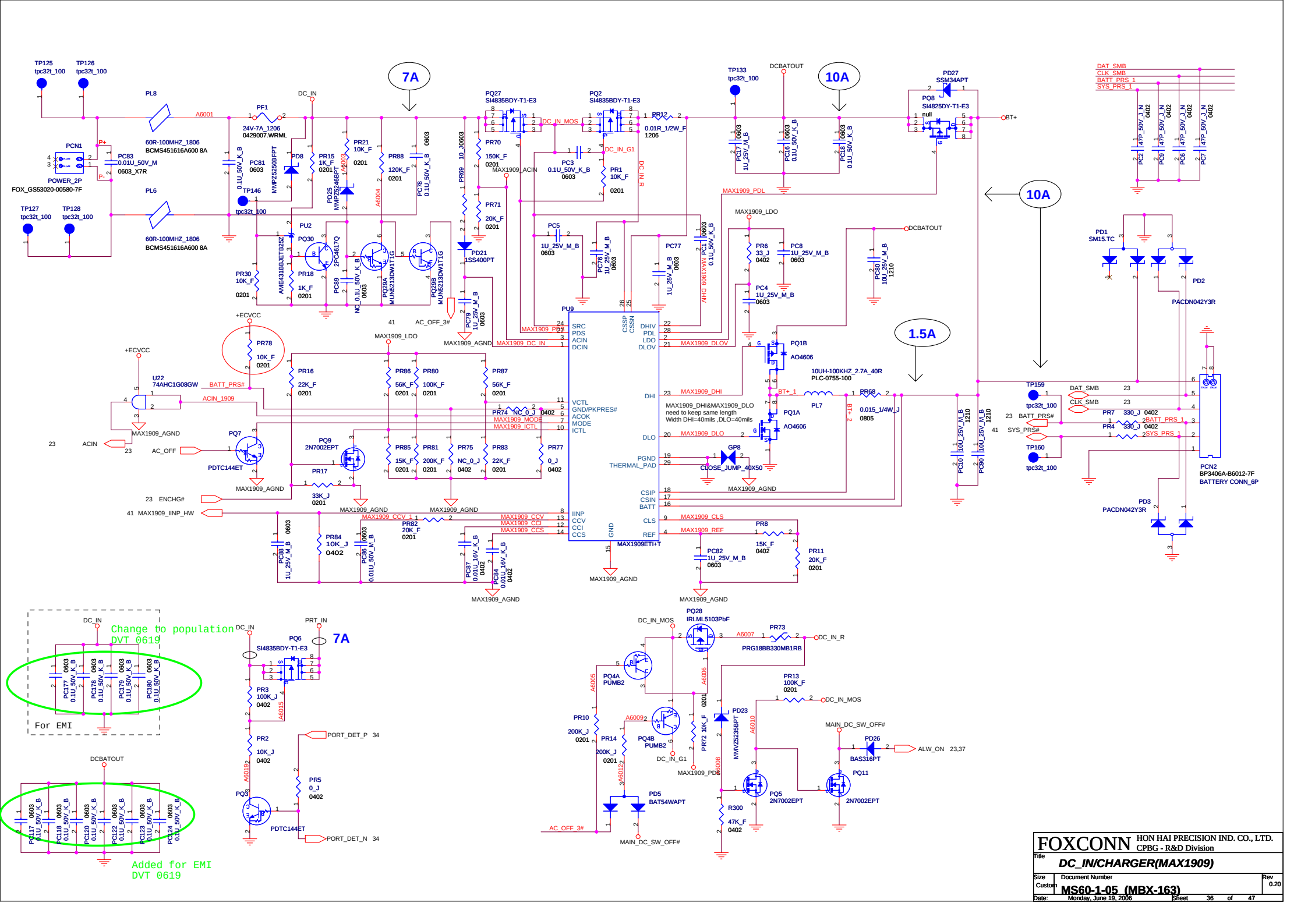


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

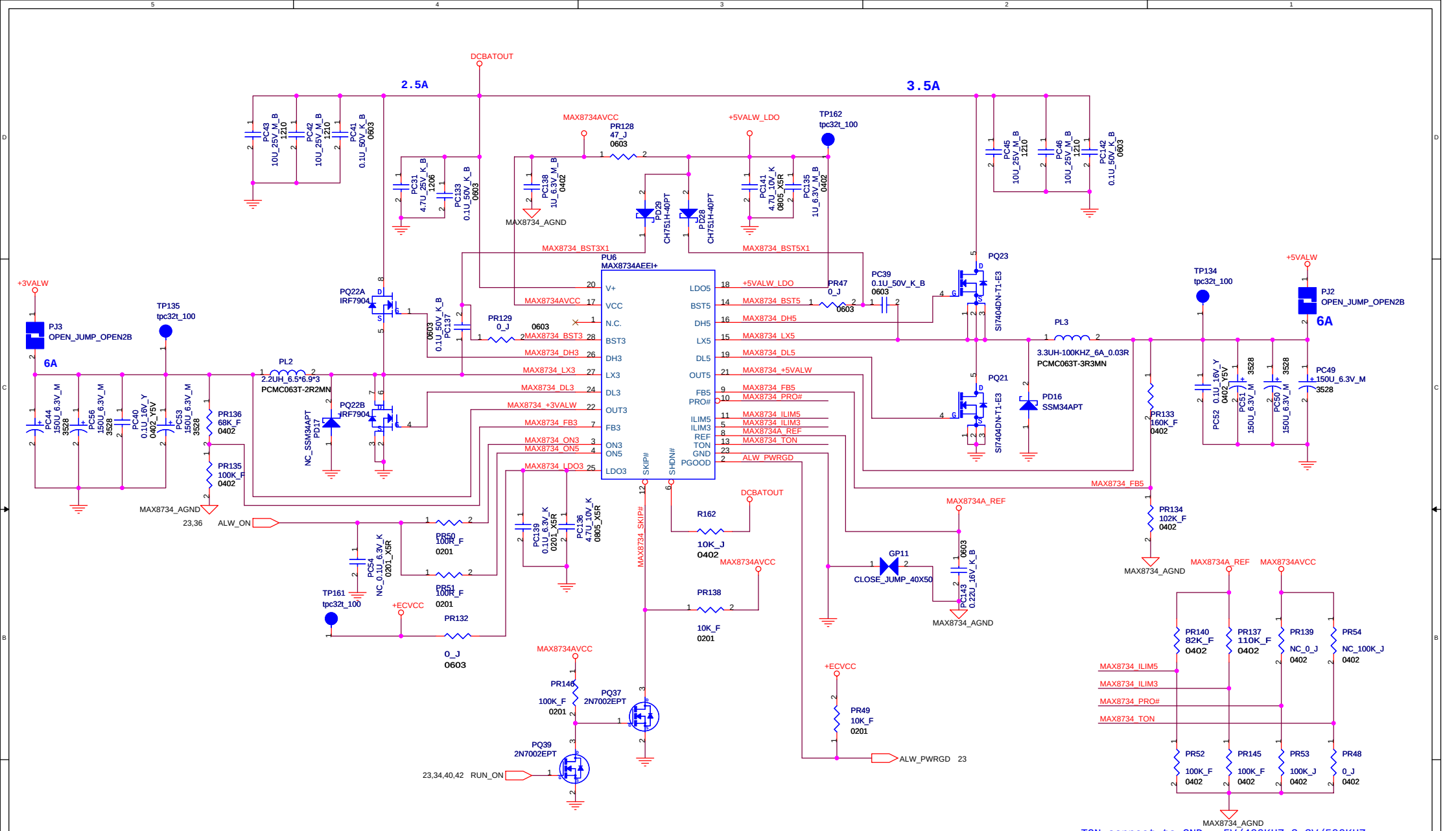
Title: *Power Design Diagram*

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 35 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	DC_IN/CHARGER(MAX1909)		
Size: Custom	Document Number: MS60-1-05 (MBX-163)		Rev: 0.20
Date: Monday, June 19, 2006	Sheet 36 of 47		

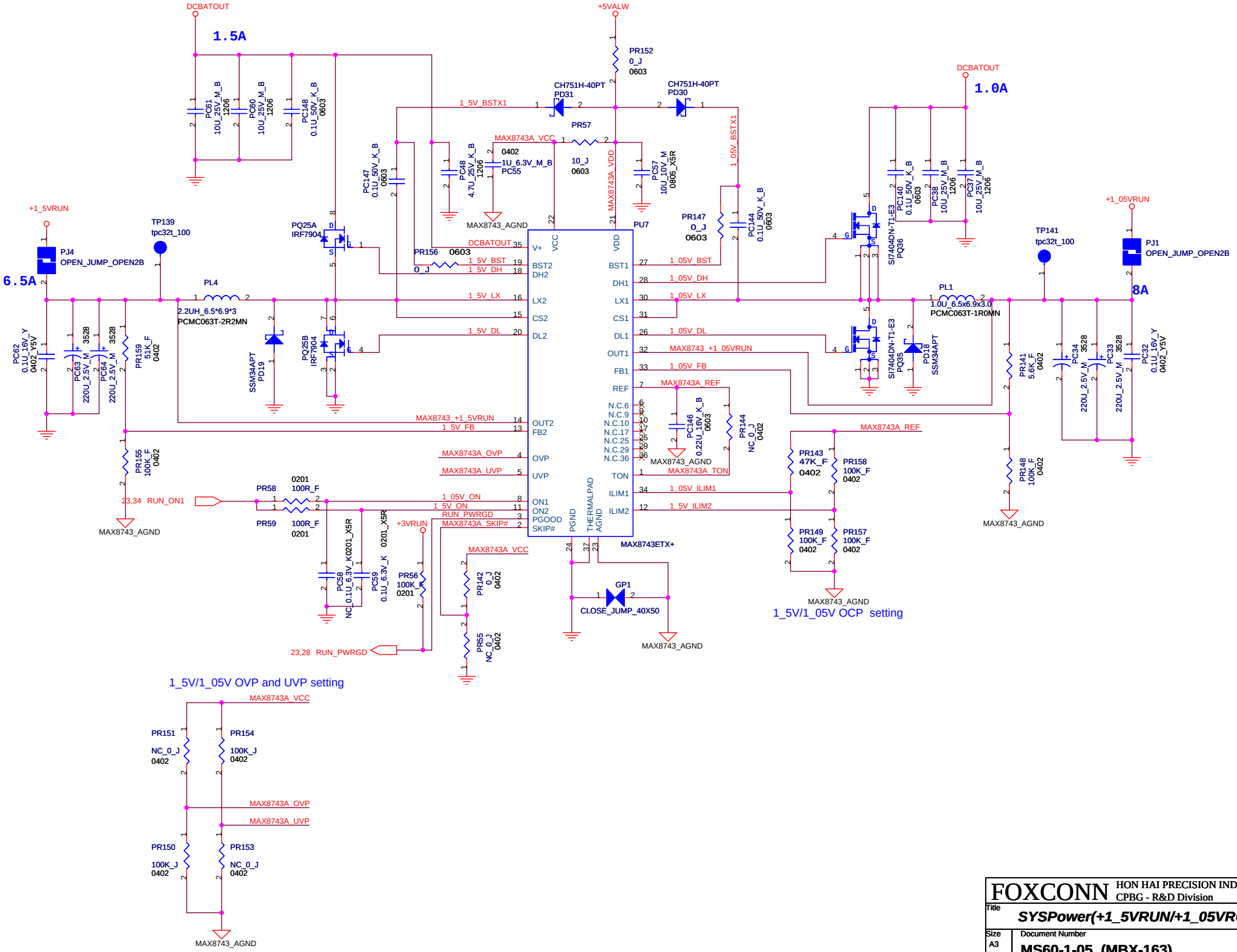


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

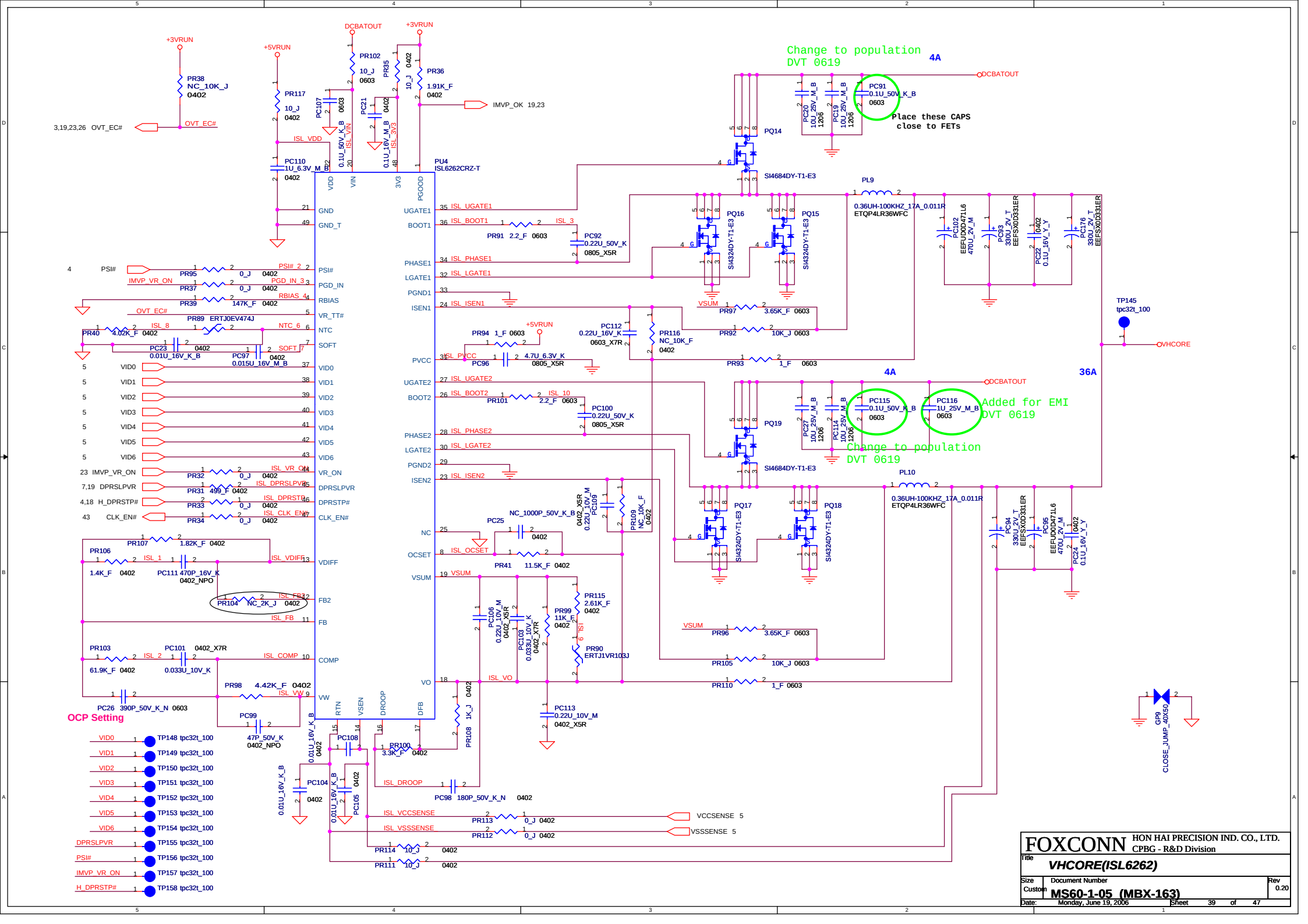
Title: SYS Power (3D3VALW/5VALW)

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 37 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYSPower(+1_5VRUN/+1_05VRUN)	
Size A3	Document Number MS60-1-05_(MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 38 of 47	


Change to population
DVT 0619
4A
Place these CAPS
close to FETs
Added for EMI
DVT 0619
Change to population
DVT 0619
36A
OCP Setting
FOXCONN
HON HAI PRECISION IND. CO., LTD.
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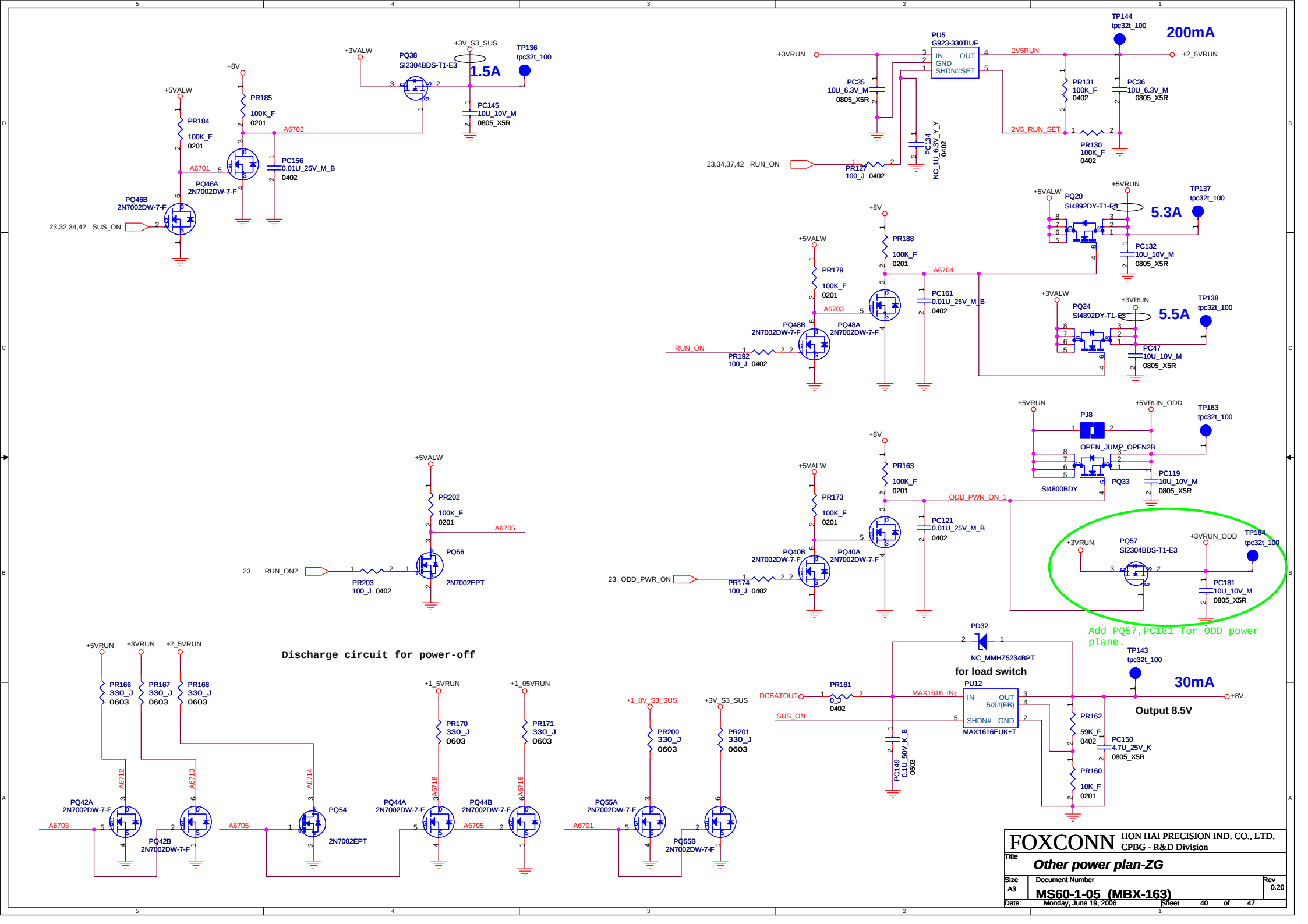
VHCORE(ISL6262)
MS60-1-05 (MBX-163)
Monday, June 19, 2006



FOXCONN HON HAI PRECISION IND. CO., LTD.
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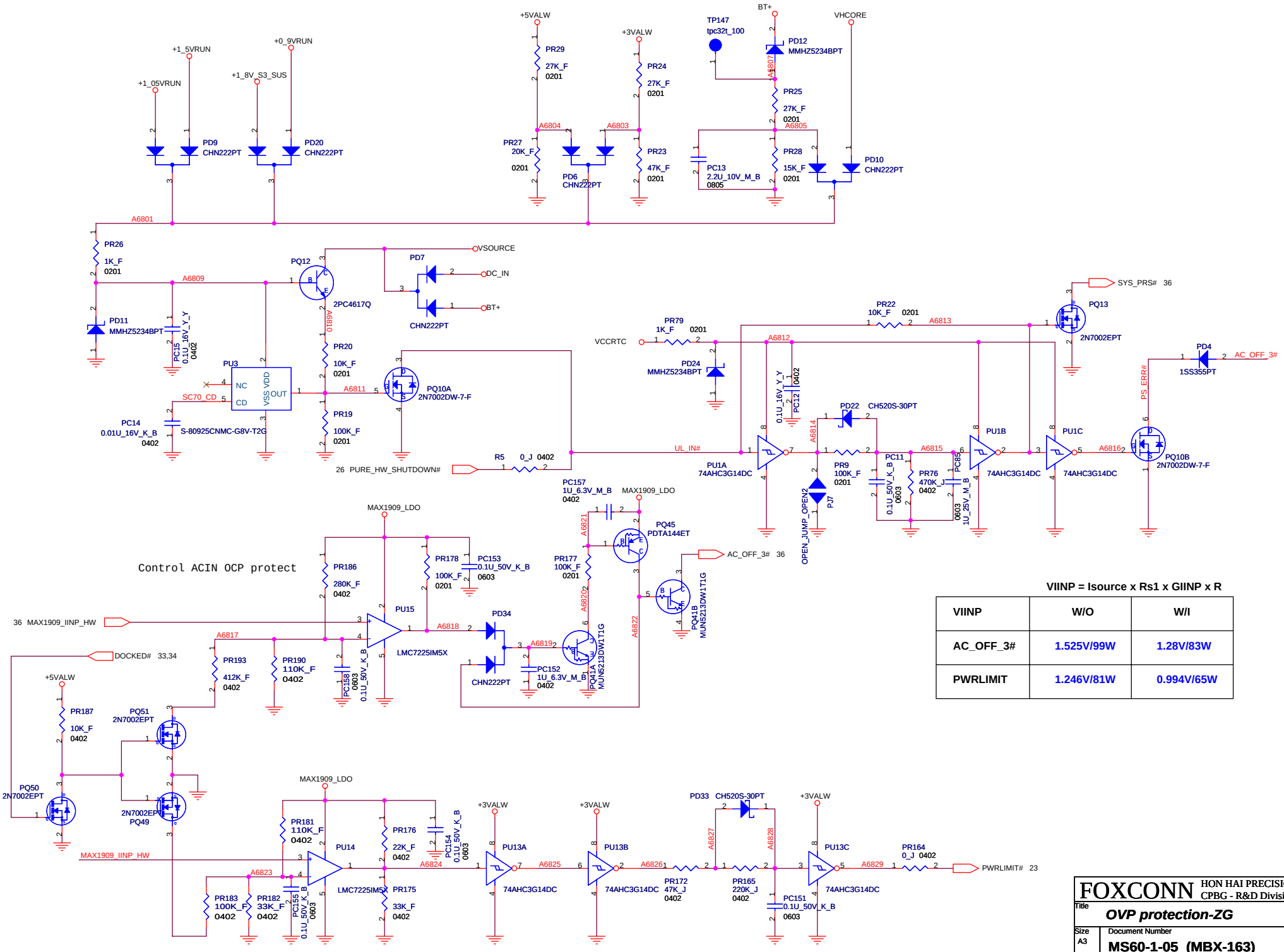
Title: *Other power plan-ZG*

Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20

Date: Monday, June 19, 2006 Sheet 40 of 47



VIINP = Isource x Rs1 x GIINP x R

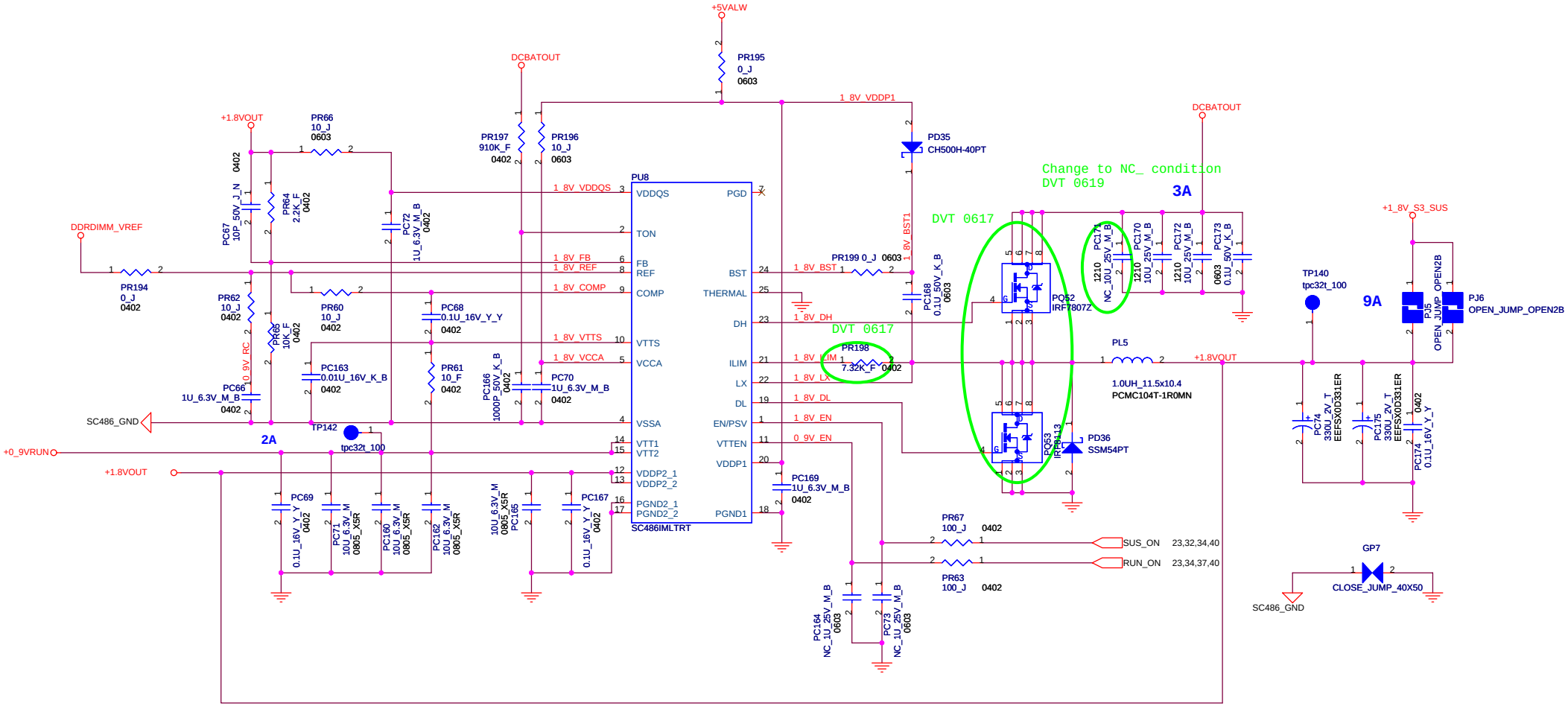
VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.246V/81W	0.994V/65W

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

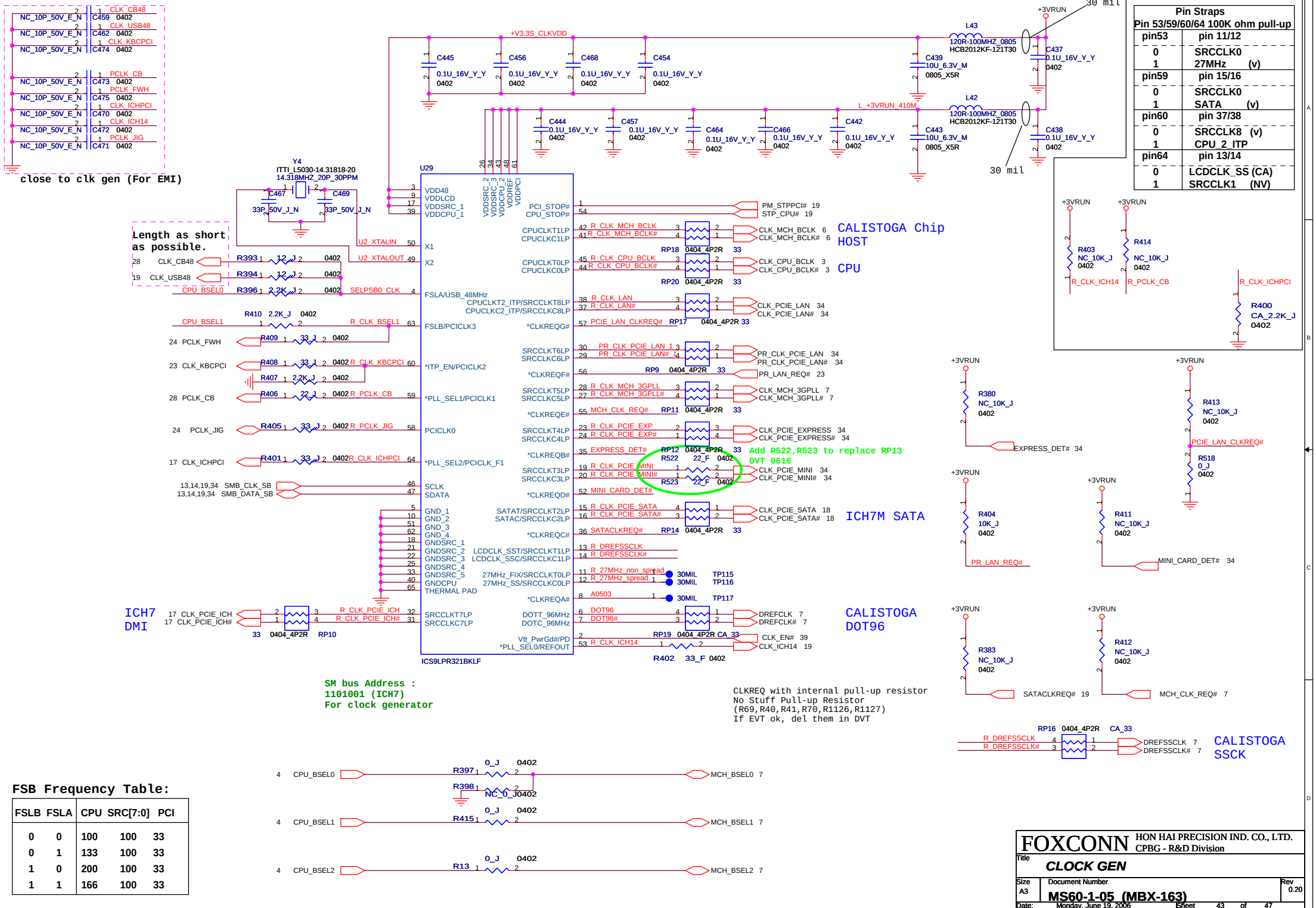
Title: ***OVP protection-ZG***

Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20

Date: Monday, June 19, 2006 Sheet 41 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 42 of 47	



Pin Straps Pin 53/59/60/64 100K ohm pull-up	
pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU_2_ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)

FSB Frequency Table:

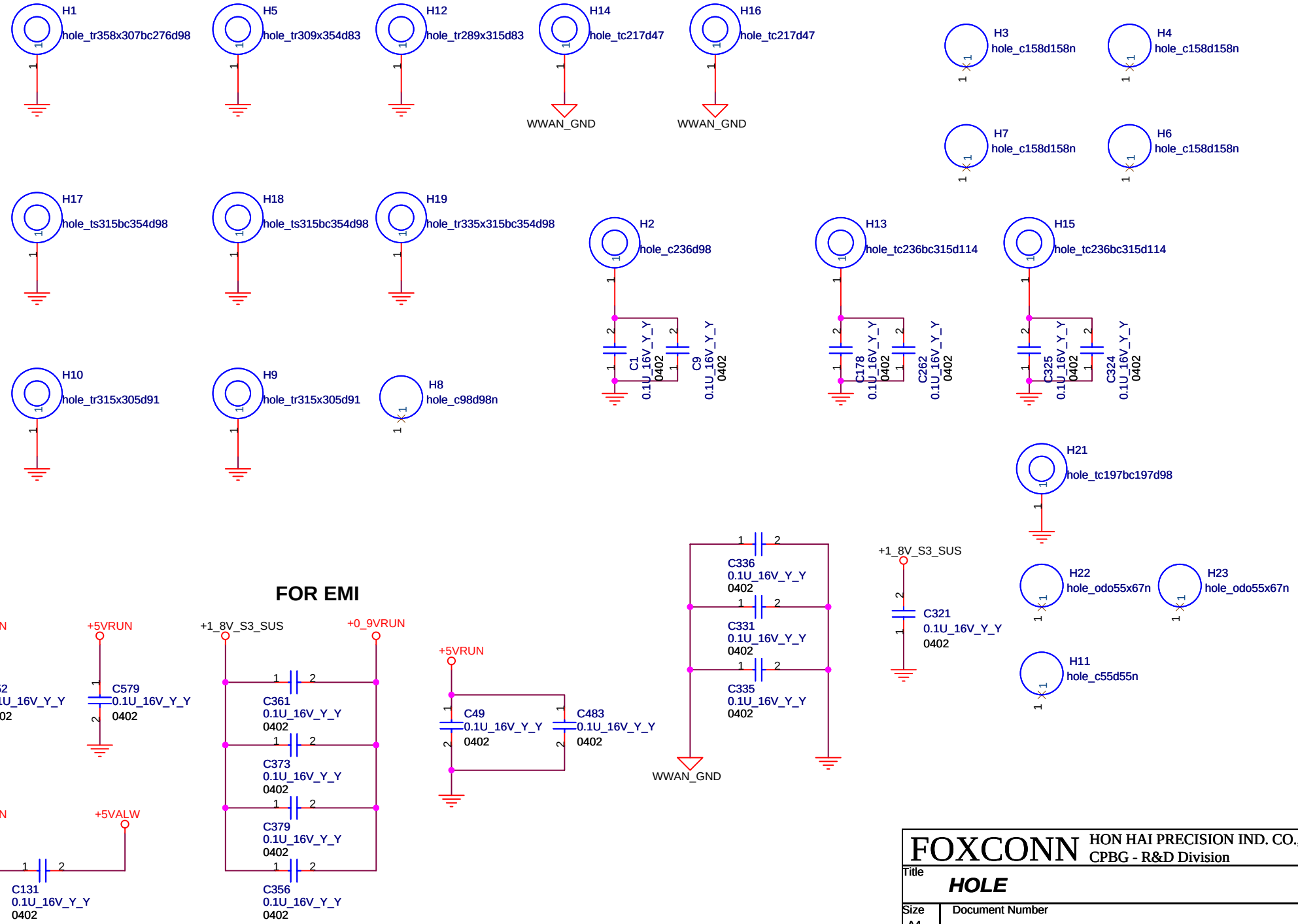
FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: CLOCK GEN

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 43 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: ***HOLE***		
Size: A4	Document Number: **MS60-1-05 (MBX-163)**	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 44 of 47	

MS60 Power On Sequerce Timing

Version : 0.0
Modified date : 2/14/2006

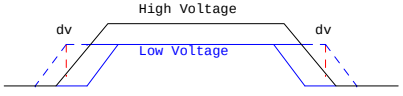
NOTE : (EC KB3910 Min. response time is 1ms)

1. T00 : R=47K , C = 0.1uF is ENE recommand value please refer to KB3910B0-AN4A-200
2. T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
   PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
3. T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
4. T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
5. T05 : RSMRST# active High to SLP_S5# avtive High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing
6. T06(Please reference Intel 16971 Page 301 of t234 timing
7. T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
8. T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
9. T09 : For MS01 current SPEC
10. T10 :Please refer to Intel 16971 Page 300 of t214 timing
11. T11 :Please refer to Intel 16971 Page 303 of t216 timing
12. T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing)
13. T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
14. T14 : For MS01 current SPEC Min. is 5 ms
15. DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
16. IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
17. In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
18. T15 : Please refer to MAX8771 datasheet
20. T16: Please refer to MAX8771 datasheet
21. T17 : Please refer to Intel CK410(14690) page 53
22. T18 : The ICH7 drives PLTRST# active a mininum of 1ms when initiated through the Reset Control register I/O Register CF9h)
23. CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
24. T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add dischage circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
2. V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
3. +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
4. +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
5. +3.3VRUN -> +2_5VRUN, dt:0.3mV
6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
7. +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV

R/C delay (47K/ 0.1uF)



T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns~2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms

T11	T12	T13	T14	T15	T16	T17	T18	T19	T20
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min :1s

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: Power Sequence

Size: C | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 45 of 47

<1>2006/3/28 remove U36.SW no need to program for present application.

<2>2006/3/28 Change PR5 from 13K to common parts 10KOhm.

<3>2006/3/29 Change USB CONN. CN16 & CN40 for ID requirement.
P/N : FOX_UB11193-C1301-4F

<4>2006/3/29 Change ODD CONN. CN21 for ID requirement.
P/N : FOXCONN_QT8H0506_64T2R_4F

<5>2006/3/29 Change PC359,PC360 to 10uF
P/N : 1C-2B70106-M100

<6>2006/3/29 update new HDD CONN CN24.
P/N : 2N-0022002-F0G0

<7>2006/3/29 update new DC-IN CONN PCN1.
P/N : FOX_GS53020-00580-7F

<8>2006/3/29 update new BTY CONN PCN2.
P/N : FOXCONN_BP34063_B6012_7F

<9>2006/3/30 U18.U19.U21.R277.R300.R315change to NC according to Customer's feedback.

<10>2006/3/30 R269,R273,R276,R286,R287,R300 change to Populate according to Customer's feedback.

<11>2006/3/30 New add INV_ENABLE_EC logic dur to BIOS Code merge issue.add new component :
U53.U54 P/N : 14-74AHC1G-0800
R762 P/N : 1R-0000103-J200
R763 P/N : 1R-0000000-J200
R764 P/N : 1R-0000104-J200
Delete R176.R177

<12>2006/3/31 Add C20,C21,C22,C31,C33,C68 for EMI slution.
P/N : 1C-2Y20104-Y000

<13>2006/3/31 Add R5 for Customer feedback.
P/N : 1R-0000000-J200

<14>2006/3/31 Dummy R482,R483 for Customer feedback.

<15>2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component :
U55.U56 P/N : 15-RT9702A-0000
C521.C522 P/N : 1C-2Y20104-Y000
R569.R573 P/N : 1R-0000105-J200
C870.C871 P/N : 1C-2Y30225-Y000
C535.C751 P/N : 1C-2B70106-M100
Deleted Component :
Q12.Q13.Q20.Q21.C535.C527.C521.C751.C753.C752.R486.R476.R568.R569

<16>2006/3/31 CN2 Pin11 change to +3V_S3_SUS for Customer feedback.

<17>2006/4/3 CN20.CN32.CN33 Pin assignment modified due to Customer's concern.

<18>2006/4/3 CN31.CN32.CN33 CN34 Connector change.
P/N : GB11261_1051_7F

<19>2006/4/3 L17 & L19 updated according to Customer feedback
P/N : 1L-DCS0603-1000

<20>2006/4/4 Add PWR_MIZER circuit.
U6J GPIO10 with new signal "NV_PWR_MIZER"
new Components added and modified as below :
10K Ohm -- R130.R766 -- P/N : 1R-0000103-J200
7.5K Ohm -- R765.R767.R768.R769.R770 -- P/N : 1R-0000752-F200
4.3K Ohm -- R128 -- P/N : 1R-0000432-F200
2N7002EPT -- Q54.Q55.Q56.Q57.Q58 -- P/N : 17-2N7002E-PT00

<21>2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.

<22>2006/4/4 D6.D7.D8 change to Q59.Q60.Q61
P/N : 17-2N7002E-PT00

<23>2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate.
P/N : 1R-0000121-J200

<24>2006/4/4 new add Q62 for WLAN LED Logic
P/N : 17-2N7002E-PT00

<25>2006/4/4 NC F1 and C859 according to customer's feedback.

<26>2006/4/4 delete R482.R483 according to customer's feedback.

<27>2006/4/6 add H3 ~ H20

<28>2006/4/6 Update BTY Connector PCN2 for ME requirement.
P/N : 2N-0006001-MKX0

<29>2006/4/6 R278.R289.R270 change to 75Ohm and circuit modified as customer's feedback.
P/N : 1R-0000750-F200

<30>2006/4/6 R543 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-F300

<31>2006/4/6 R553 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-J200

<32>2006/4/6 R99.R94.R97.R109.R67.R64.R65.R75 change to NC as customer's feedback.
and R66.R69.R98.R101 change to 120Ohm.
P/N : 1R-0000121-J200

<33>2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.

<34>2006/4/6 CN31 Pin1.2 change to +3V_S3_SUS as customer's feedback.

<35>2006/4/6 add 1A Fuse F4.F5.F9.F11.F15.F17.F18.F19
P/N : 1M-F32V1A0-F000

<36>2006/4/6 add 0.5A Fuse F2.F3.F6.F7.F8.F10.F12.F13.F14.F16.F18
P/N : 1M-F32V0A5-F000

<37>2006/4/6 add C872 according to MS20 lesson learn.
P/N : 1C-2B20102-M000

<38>2006/4/6 CN34 Pin23.24 change to +3VRUN.

<39>2006/4/6 add C71.C74.C87 for EMI.
P/N : 1C-2Y20104-Y000

<40>2006/4/6 add C89.C188.C199.C208.C213.C214
P/N : 1C-2Y20104-Y000

<40>2006/4/7 add C215.C216.C217.C218.C219 for EMI solution.
P/N : 1C-2Y20104-Y000

<41>2006/4/7 R118.R119.R351 change to populate as customer's feedback.

<42>2006/4/7 Y1.C104.C107.C492.C497.C501.R433.R434.R427.R428.R429.R430.R132.
R133.R134.R136.R117 change to NC as customer's feedback.

<43>2006/4/7 R439.R443 change to 0 Ohm as customer's feedback.
P/N : 1R-0000000-J200

<44>2006/4/7 update Net name EN_EXT_DEV_SENSE# as customer's feedback.

<45>2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component :
PQ183 P/N : 17-2N7002D-W000
PR115 P/N : 1R-0000101-J200
PR103.PR114 P/N : 1R-0000104-F100
PC87 P/N : 1C-2B20103-M000
PQ38 P/N : 17-S14800B-DY00
PC76 P/N : 1C-2B70106-M200

<46>2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component :
PR273 P/N : 1R-0000103-F200
PR773 P/N : 1R-0004992-F200
PQ20 P/N : 17-2N7002E-PT00
PR774 P/N : 1R-0000102-J200
PC873 P/N : 1C-2Y20105-Y000

<47>2006/4/10 add H21~H24.

<48>2006/4/10 Rename Schematic Part referene.
new version since 4/11

<49>2006/4/11 change R68.R133.R100
P/N : 1R-0000151-F200

<50>2006/4/11 PR111.PR114 change to NC according to PWR team's suggestion in EVT.

<51>2006/4/11 Modify ODD reset circuit as customer's feedback.
Add U37 P/N : 15-MAX809S-0000
Add R516 P/N : 1R-0000104-J200
NC R305

<52>2006/4/11 Remove C257 for EMI comment.

<53>2006/4/11 add ODD Reset RC.
Add R517 P/N : 1R-0000103-J200
Add C580 P/N : 1C-2Y20104-Y000

<54>2006/4/14 change R197.R198.R199.R200 to 60.4Ohm
P/N : 1R-000604X-F200

<55>2006/4/14 add R518 for 0Ohm
P/N : 1R-0000000-J200

<56>2006/4/14 CN7.C409.C412.L37.F16.R44.R45 change to CA from NV to fit configuration.

<57>2006/4/27 PR111.PR114 change to Populate from NC according to PWR team's suggestion in EVT.
P/N : 1R-0000100-J200

****

MS60-L change list base on MS60-H

<58>2006/5/02 Del all NV_ components for L-model only.

<59>2006/5/03 Remove +1_8VRUN discharge circuit.Delete PR169,PQ44. Add PQ54 P/N:17-2N7002E-PT00

<60>2006/5/03 LED2 pin2,pin3 swap for Power LED color opposite issue

<61>2006/5/03 Change CAP93,CAP94 to NEC,TEPSGV0E337M9-12R,330uF,2.5V
P/N:1C-31T0337-MX00
Add CAP95 P/N:1C-31T0337-MX00

<62>2006/5/04 F1,F2,F3,F4,F5,F6,F7,F8,F9,F10,F11,F12,F13,F14,F15,F16,F17,F19 change to fuse,1.1A PTC type
P/N:1M-F06V1A1-F000

<63>2006/5/05 follow M/E change to exchange PCN1 pin1 & pin2 connection.Layout change placement form top side to bottom side.

<64>2006/5/05 Add GP14,GP15 open jump for repair conveniently

<65>2006/5/05 Add C581,C582,C583,C584,C585,C586,C587,C588,C589,C590,C591,C592 for 22uF_0805_6.3V shortage.

<66>2006/5/08 As to M/E assemble issue, we will need rotat 180degree about T/P module.So that R47 change to stuff

<67>2006/05/09 Rename CAP93,CAP94,CAP95 to PC93,PC94,PC176.And change component to Panasonic,EEFSX0D331ER,330uF,2V
P/N:1C-42T0337-MX00

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *History*		
Size: Custom	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 46 of 47	

<68>2006/05/09 PC54,PC58,PC59,PC139 change to X5R,0.1uF,6.3V,10%,0201 for X7R,0.1uF,10V,0201 shortage.
P/N:1C-2B10104-K100

<69>2006/05/11 L33,L34 pin swap .D12 & D10 change to TOP side for layout conveniently

<70>2006/05/12 PR198 change to 5.6k/0402_1% to modify 1.8V OCP seting value.
P/N:1R-0000562-F200

<71>2006/05/12 CN23 change to ''FOX_MH11747-BR2D-4F'' for ME requirement.
P/N:2N-000400N-FKG0

<72>2006/05/12 CN3,CN8 change to ''FOX_GB5RF120-1200-7F'' for ME requirement.
P/N:1N-0012001-F0T0

<73>2006/05/12 CN7 change to ''FFOXCONN_GB5RF060_1200_7F'' for ME requirement.
P/N:1N-0006000-F0T0

<74>2006/05/12 CN12,CN16 change to ''FOXCONN_UB11193_C1304_4F'' for ME requirement.
P/N:1N-0004000-FEG0

<75>2006/05/12 CN9 change to ''FOXCONN_HS8206E'' for ME requirement.
P/N:1N-0006001-M1T0

<76>2006/05/16 Due to ripple noise issue.PC74,PC175 change to ''Panasonic,EEFSX0D331ER'' .Del PC75 for power requirement.
P/N:1C-42T0337-MX00

<77>2006/05/17 Add PQ55,PQ56,PR200,PR201,PR202,PR203 for power discharge.
P/N:17-2N7002D-W000
P/N:1R-0000331-J300
P/N:1R-0000104-F100
P/N:1R-0000101-J200

<78>2006/05/17 U24 change to ''FOXCONN_PZ4782A_2743_01'' for ME requirement.
P/N:1N-1478002-0000

<79>2006/05/18 PC67 change to 10pF 0402,and need to mount for power requirement.
P/N:1C-2N20100-J000

<80>2006/05/18   CN12,CN16 change footprint to ''FOXCONN_UB11193_C1304_4F_HM'' for DFM.

<81>2006/05/18   Add R519,R520,C593,C594 on ''IAC_BITCLK'' signal for EMI requirement.
P/N:1R-0000000-J200
P/N:1C-2N20330-J000

<82>2006/05/18 H13,H15 footprint change to '' hole_tc236bc315d114'' for ME requirement.
P/N:1X-HOLE000-0232

<83>2006/05/19 CN25 need change to P/N:1N-1200007-0000. CN26 need change to P/N:1N-1200008-0000. Because P/N:1N-120000C-0000 & P/N:1N-120000D-0000 part number are not available.

<84>2006/05/19 Add PC177,PC178,PC179,PC180 on DC_IN trace for EMI requirement.
P/N:1C-2B30104-K000

<85>2006/05/22 Del R89,R140,R127.Add L54,L55,L56 (0 ohm change to bead) for EMI requirement.
P/N:1L-BEBMS16-0801

<86>2006/05/30 change R517 from 10Kohm to 0ohm for solving the ODD issue.
P/N:1R-0000000-J200

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DVT change list

<87>2006/06/15 Delete R264.R271 for Debug BD LED.

<88>2006/06/15 Del reset IC form ODD portion.Del R516,R517,C580. Change U37 to 74AHC1G08GW and connect GPIO_ODD_RST# form KBC for ODD reset.

<89>2006/06/15 Add R521 1k ohm and change R244 connection form ''ALW_ON'' to ''ALW_ON_1'' for customer's requirement.
P/N : 1R-0000102-J200

<90>2006/06/16 PORT_DET# change from EC's pin81 to EC's pin176 for noise decreasing.

<91>2006/6/16 remove RP13 and replace with R519/R520 for WLAN issue improving.
P/N : 1R-0000220-F200

<92>2006/6/16 Add one GPIO signal ''VISTA_SUPPORT#'' that is connected form EC's pin99 to CN1's pin17 to support Vista OS.

<93>2006/6/16 Add PQ57,PC181 for ODD power plane.
P/N:17-S12304B-DS00
P/N:1C-2B70106-M200

<94>2006/6/16 (HDD connector)CN21's pin18 change connection from NC to GND for the starting timing improvement.

<95>2006/6/17 Change PQ52 from SI7392DP to IRF807Z and change PQ53 from SI7336ADP to IRF8113 for power requirement.
P/N:17-1RF7807-2000
P/N:17-1RF8113-0000

<96>2006/6/17 PR198 change from 5.6K ohm to 7.32K ohm to modify OCP setting value.
P/N:1R- 0007321-F200

<97>2006/6/17 U12 change from G961-18ADJEU to SC1565IS-2.5TRT for WWAN voltage drop improvement.
P/N:15-SC15651-0000

<98>2006/6/19 pc117,pc179,pc178,pc180,pc115,pc91 change to populate for EMI requirement.

<99>2006/6/19 Add C595 at PRT_IN power trace for EMI requirement.
P/N:1C-2B30104-K000

<100>2006/6/19 Add PC116,PC117,PC118,PC120,PC122,PC123,PC124 at DCBATOUT power trace for EMI requirement.
P/N:1C-2B30105-M000
P/N:1C-2B30104-K000

<101>2006/6/19 Add R303 10K pulldown at U34's pin1 to avoid start abnormally for customer's requirement.
P/N:1R-0000103-J200

<102>2006/6/19 PC171 change to NC_ condition for power requirement.

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Date: Monday, June 19, 2006	Sheet 47 of 47	