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PCB P/N: 1P-0065102-80SA - FUBAI
 1P-0065201-80SA - NANYA
 1P-0065503-80SA - HANNSTAR

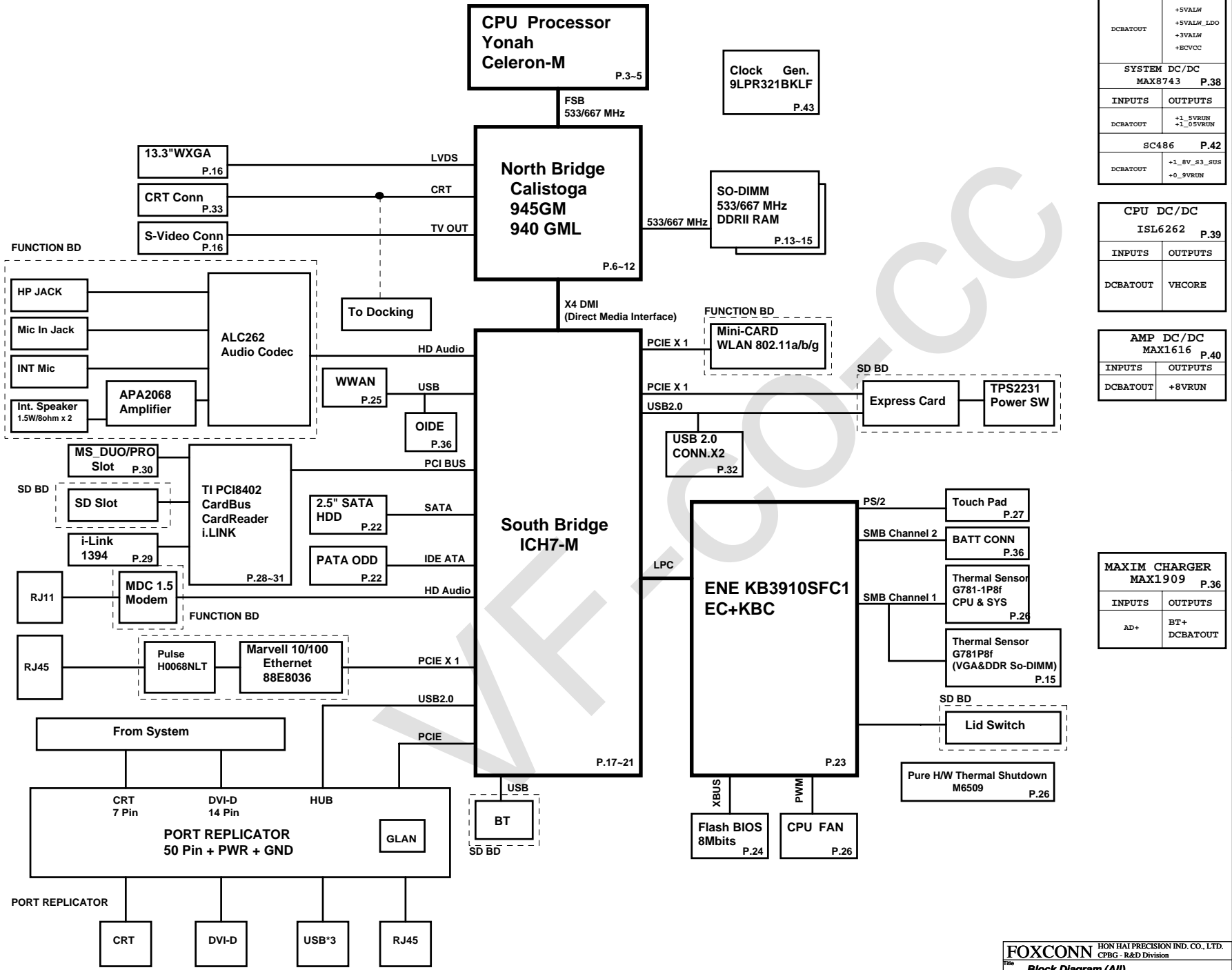
Project Code & Schematics Subject: MS60-L Main Board

P. Leader	Check by	Design by

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MS60 (CALISTOGA GM Block Diagram)

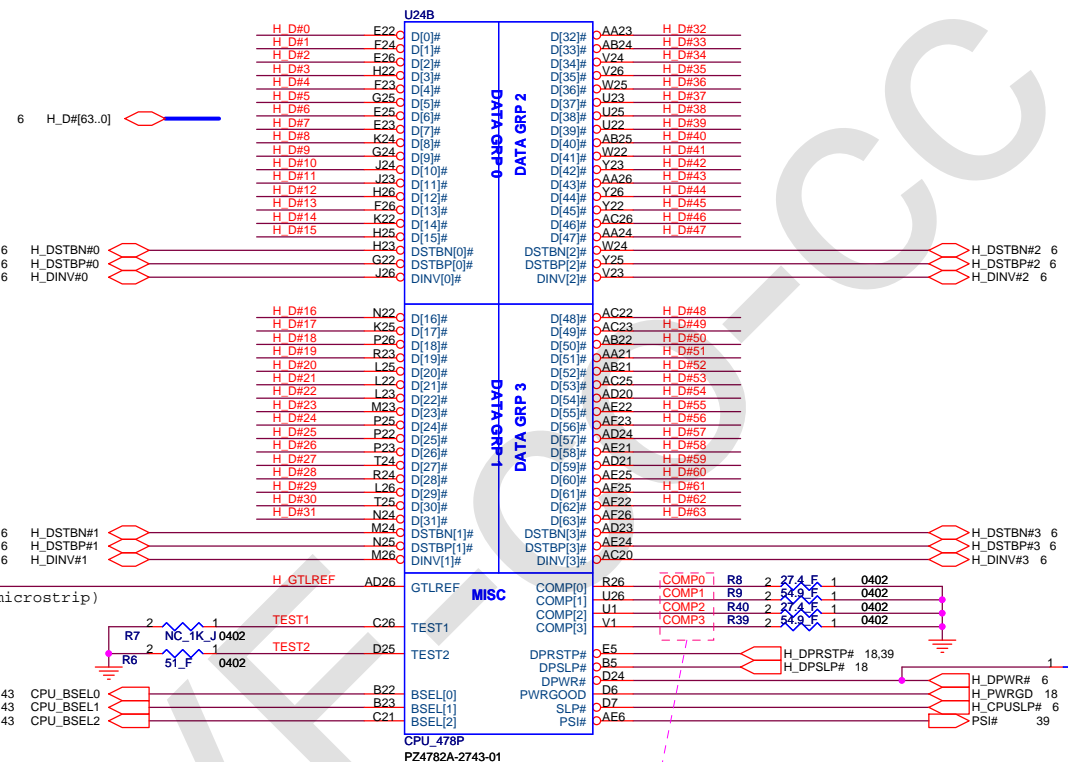


SYSTEM DC/DC MAX8734 P.37	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC
SYSTEM DC/DC MAX8743 P.38	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_0VRUN
SC486 P.42	
DCBATOUT	+1_8V_83_SUS +0_9VRUN

CPU DC/DC ISL6262 P.39	
INPUTS	OUTPUTS
DCBATOUT	VHORE

AMP DC/DC MAX1616 P.40	
INPUTS	OUTPUTS
DCBATOUT	+8VRUN

MAXIM CHARGER MAX1909 P.36	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

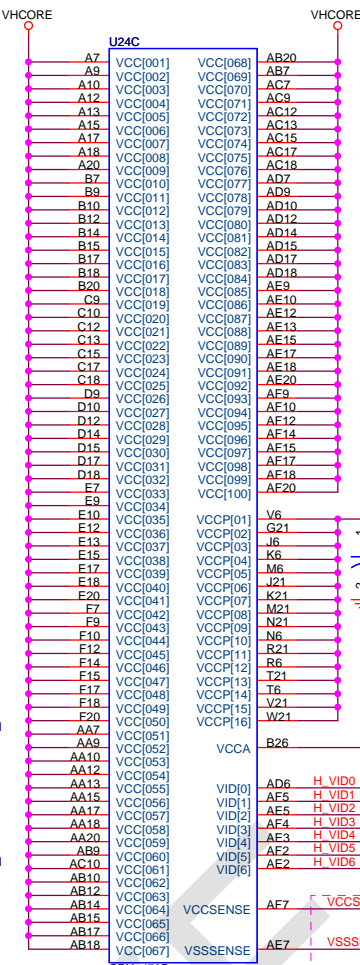
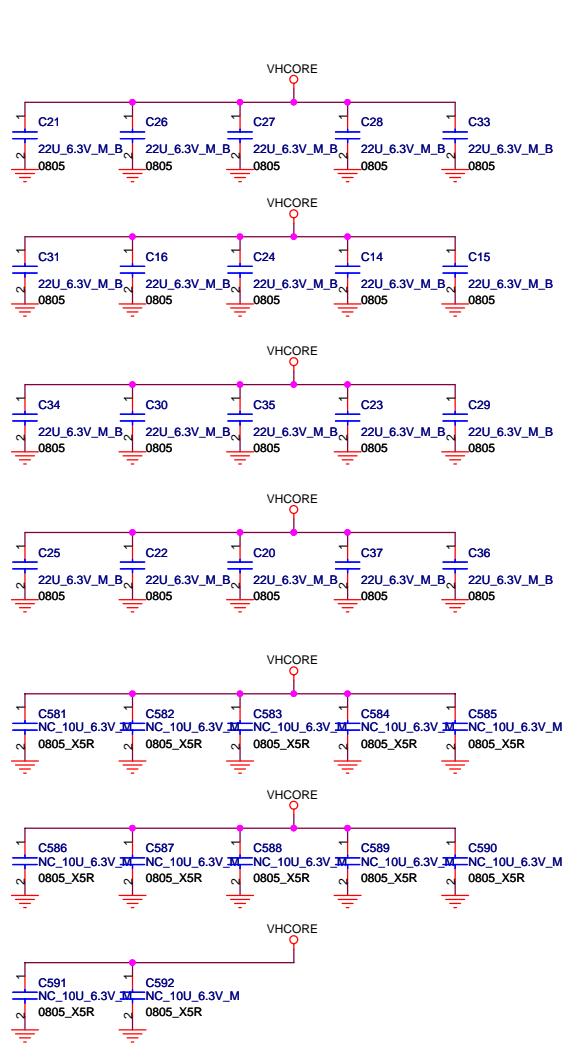


Place close to CPU
 Layout Note:
 Zo=55 ohm, 0.5"
 max for GTLREF.

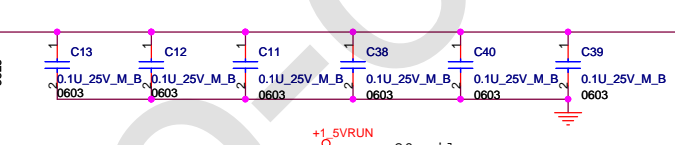
FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
LLL	Reserve
LLH	133
LHL	Reserve
LHH	166

Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
 Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".



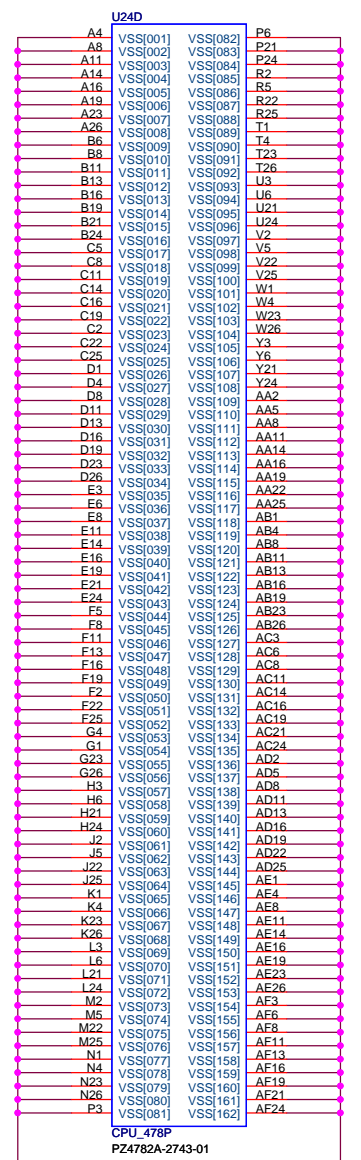
CPU_VCCA---->130mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A for Yona
 44A for Merom

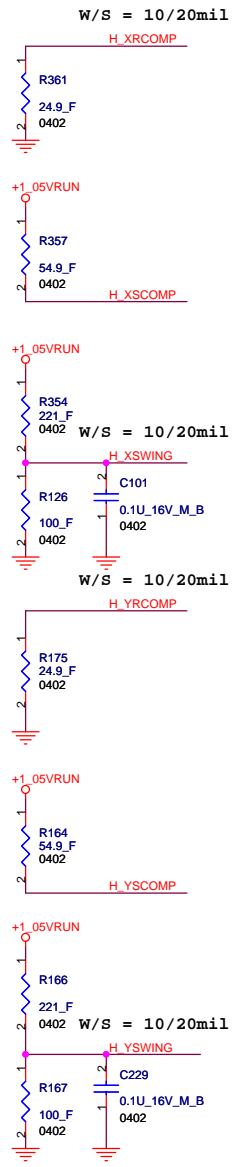


maximum current is 130mA for CPU_VCCA in Merom
 and 600A/us slew rate for CPU_VCCA

Same Length

Layout Note: Route
 VCCSENSE traces at 27.4
 Ohms with 50 mil spacing.
 Place PU and PD within 1
 inch of cpu.
 width=18 mil
 spacing=7 mil





4 H_D#[63..0] H_D#[63..0]

U27A

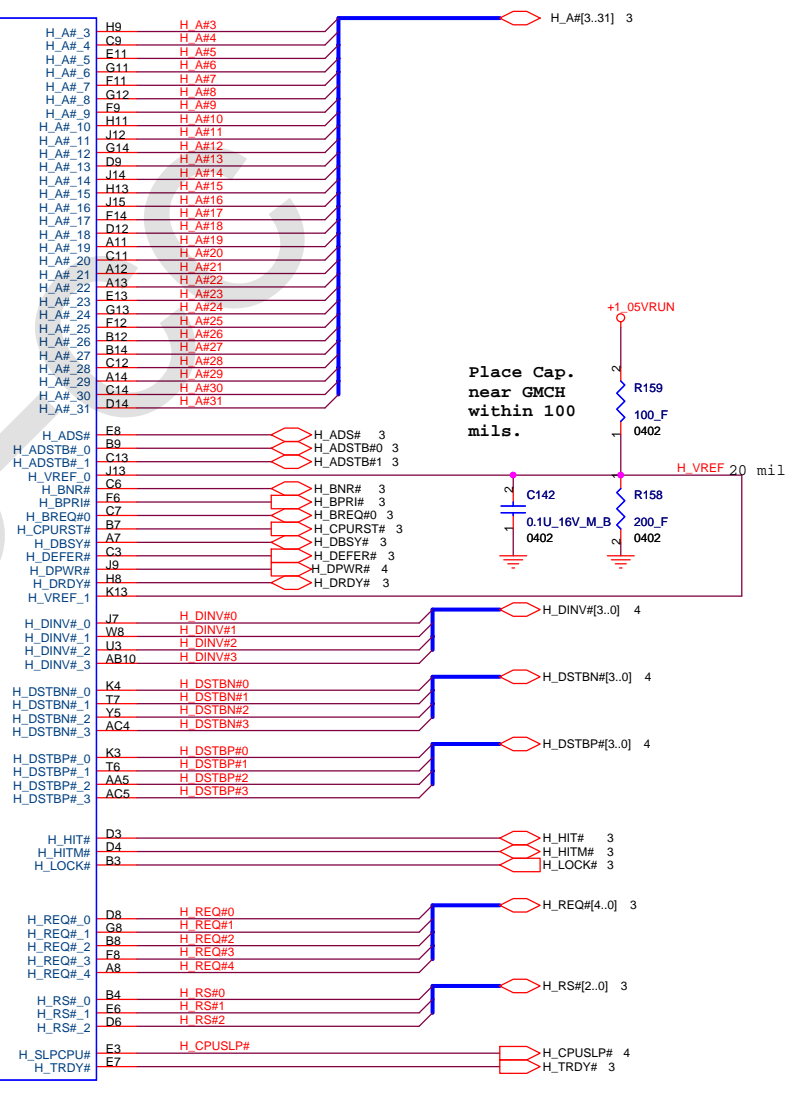
H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA2	H_D#_43
H_D#44	AA6	H_D#_44
H_D#45	AA10	H_D#_45
H_D#46	Y8	H_D#_46
H_D#47	AA1	H_D#_47
H_D#48	AA4	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4

H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1

H_CLKIN AG2
H_CLKIN# AG1

HOST



CALISTOGA

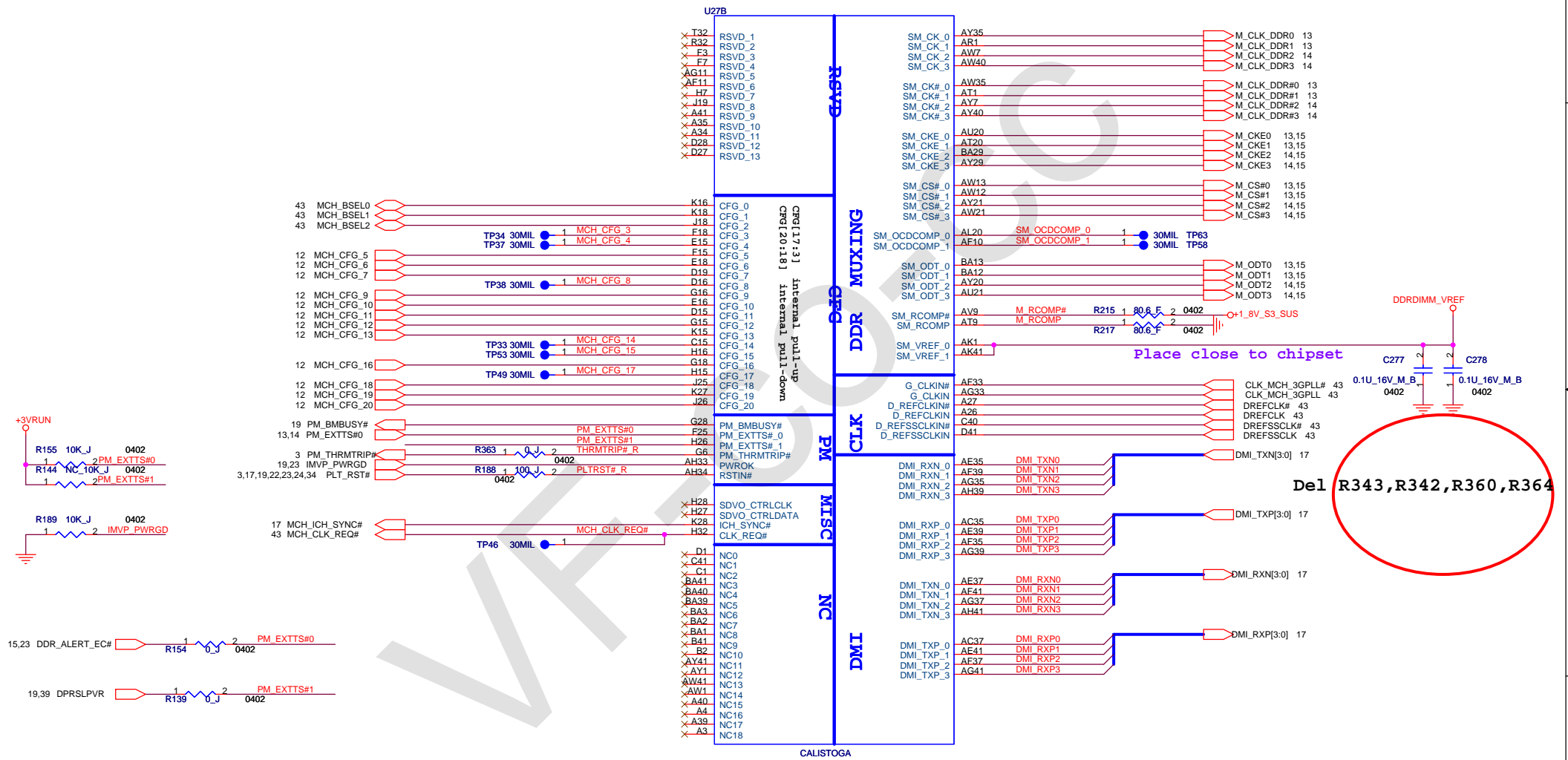
GM	Q988CGM	12-0G88CGM-0000
PM	Q988CPM	12-0G88CPM-0000
GML	940GML-QK60-A3	12-940GML0-A300

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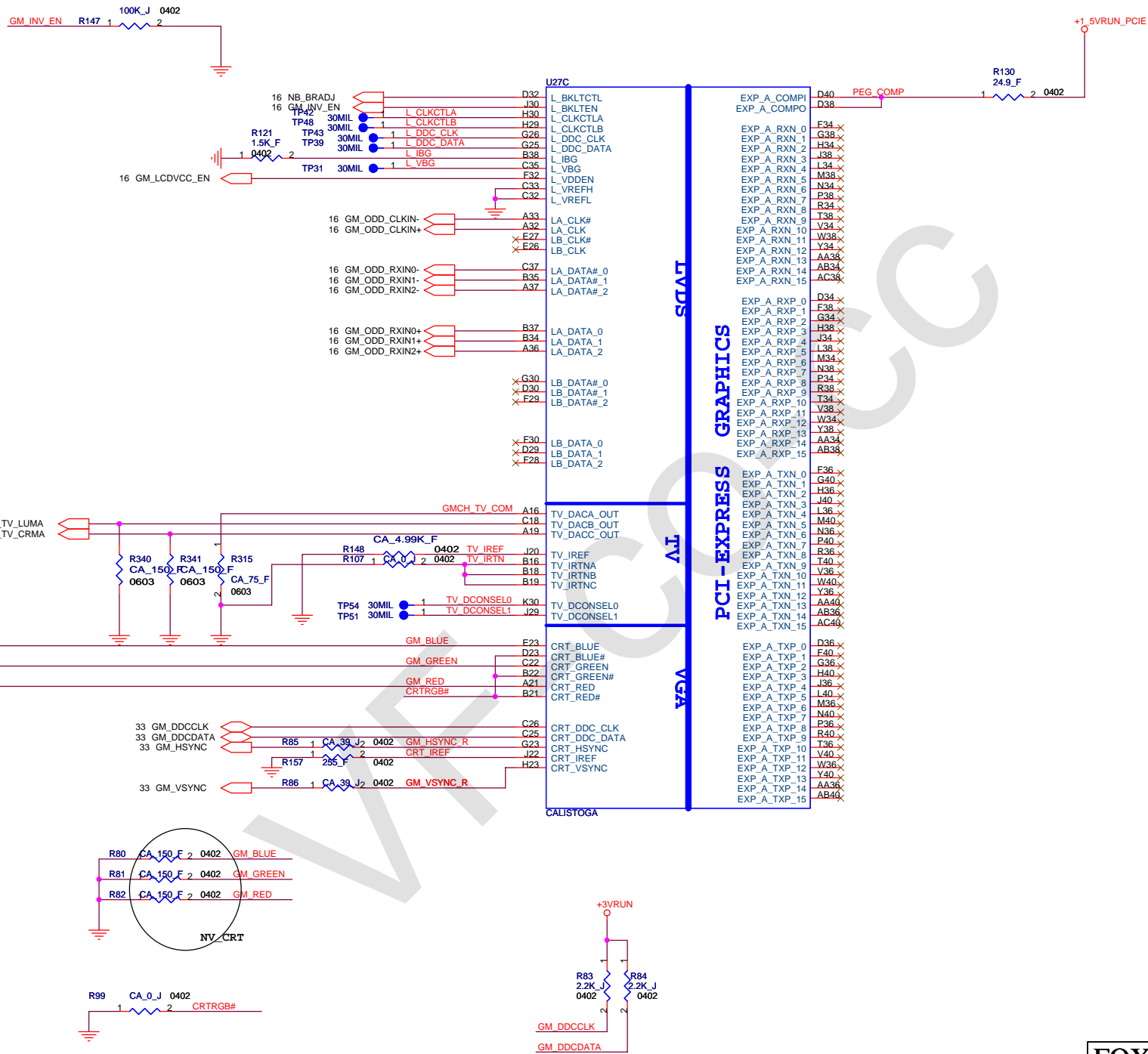
Title: **CALISTOHA (HOST)**

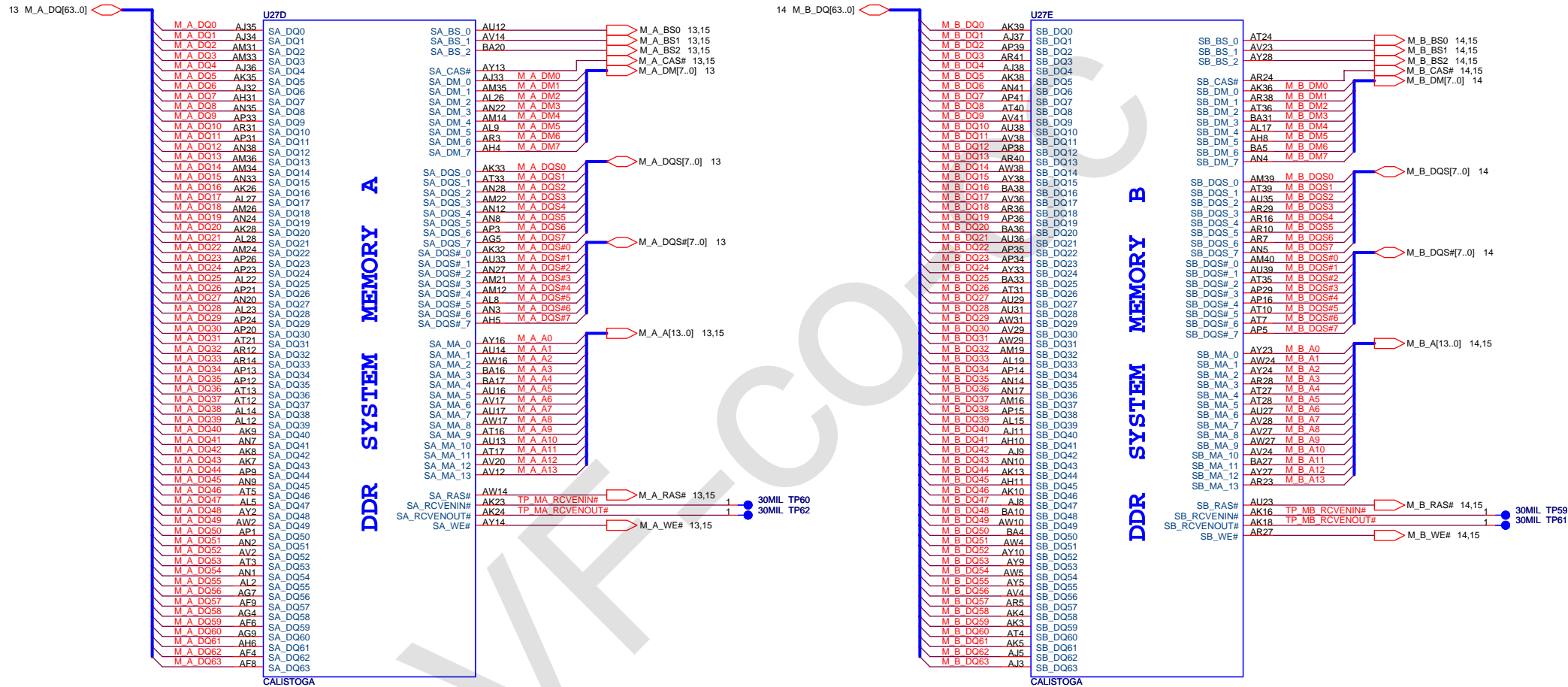
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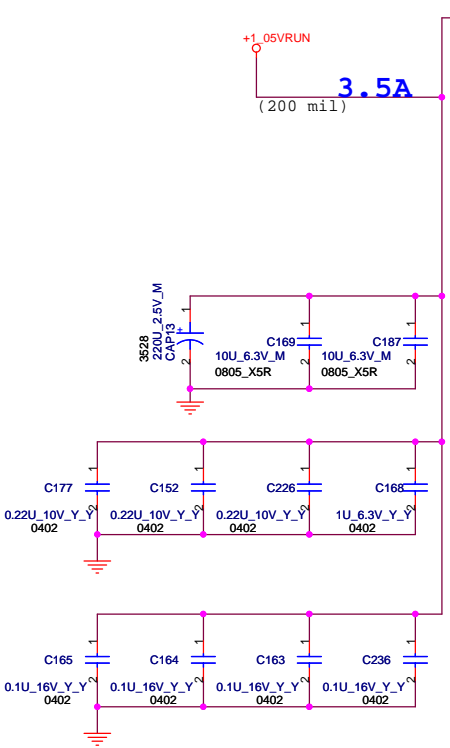
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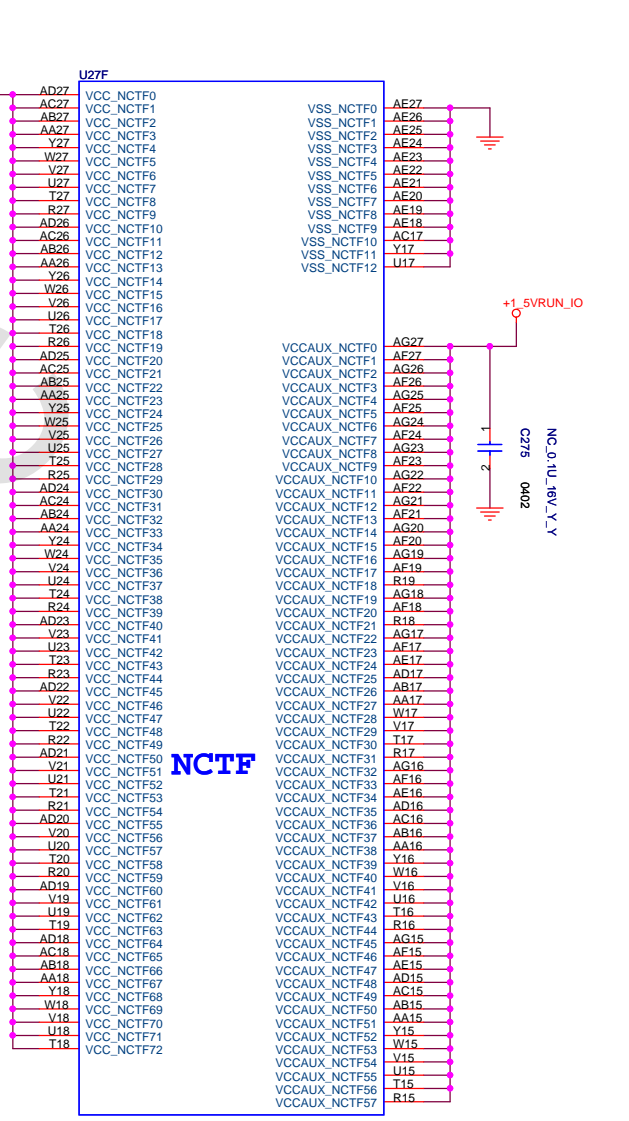
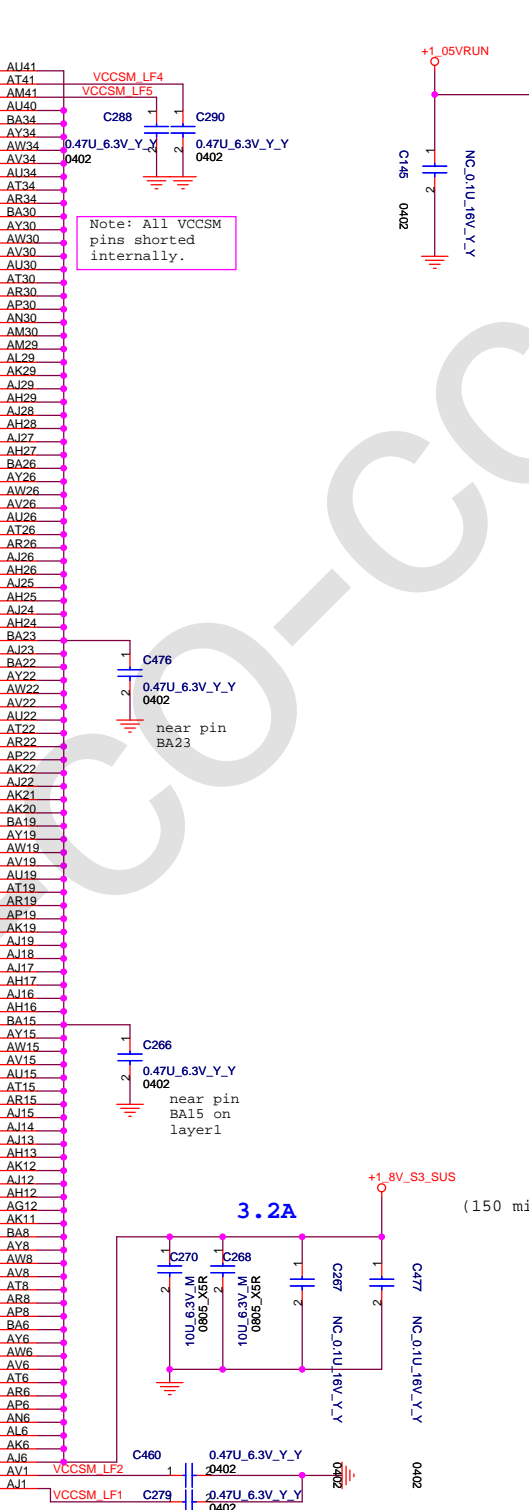
Del R343, R342, R360, R364







Pin	Signal
AA33	VCC_0
W33	VCC_1
P33	VCC_2
N33	VCC_3
L33	VCC_4
J33	VCC_5
AA32	VCC_6
Y32	VCC_7
W32	VCC_8
V32	VCC_9
P32	VCC_10
N32	VCC_11
M32	VCC_12
L32	VCC_13
J32	VCC_14
AA31	VCC_15
W31	VCC_16
V31	VCC_17
T31	VCC_18
P31	VCC_19
N31	VCC_20
M31	VCC_21
AA30	VCC_22
Y30	VCC_23
W30	VCC_24
V30	VCC_25
U30	VCC_26
T30	VCC_27
R30	VCC_28
P30	VCC_29
N30	VCC_30
M30	VCC_31
L30	VCC_32
AA29	VCC_33
W29	VCC_34
V29	VCC_35
U29	VCC_36
T29	VCC_37
R29	VCC_38
P29	VCC_39
N29	VCC_40
M29	VCC_41
L29	VCC_42
AA28	VCC_43
W28	VCC_44
V28	VCC_45
U28	VCC_46
T28	VCC_47
R28	VCC_48
P28	VCC_49
N28	VCC_50
M28	VCC_51
L28	VCC_52
AA27	VCC_53
W27	VCC_54
V27	VCC_55
U27	VCC_56
T27	VCC_57
R27	VCC_58
P27	VCC_59
N27	VCC_60
M27	VCC_61
L27	VCC_62
AA26	VCC_63
W26	VCC_64
V26	VCC_65
U26	VCC_66
T26	VCC_67
R26	VCC_68
P26	VCC_69
N26	VCC_70
M26	VCC_71
L26	VCC_72
AA25	VCC_73
W25	VCC_74
V25	VCC_75
U25	VCC_76
T25	VCC_77
R25	VCC_78
P25	VCC_79
N25	VCC_80
M25	VCC_81
L25	VCC_82
AA24	VCC_83
W24	VCC_84
V24	VCC_85
U24	VCC_86
T24	VCC_87
R24	VCC_88
P24	VCC_89
N24	VCC_90
M24	VCC_91
L24	VCC_92
AA23	VCC_93
W23	VCC_94
V23	VCC_95
U23	VCC_96
T23	VCC_97
R23	VCC_98
P23	VCC_99
N23	VCC_100
M23	VCC_101
L23	VCC_102
AA22	VCC_103
W22	VCC_104
V22	VCC_105
U22	VCC_106
T22	VCC_107
R22	VCC_108
P22	VCC_109
N22	VCC_110
M22	VCC_111
L22	VCC_112
AA21	VCC_113
W21	VCC_114
V21	VCC_115
U21	VCC_116
T21	VCC_117
R21	VCC_118
P21	VCC_119
N21	VCC_120
M21	VCC_121
L21	VCC_122
AA20	VCC_123
W20	VCC_124
V20	VCC_125
U20	VCC_126
T20	VCC_127
R20	VCC_128
P20	VCC_129
N20	VCC_130
M20	VCC_131
L20	VCC_132
AA19	VCC_133
W19	VCC_134
V19	VCC_135
U19	VCC_136
T19	VCC_137
R19	VCC_138
P19	VCC_139
N19	VCC_140
M19	VCC_141
L19	VCC_142
AA18	VCC_143
W18	VCC_144
V18	VCC_145
U18	VCC_146
T18	VCC_147
R18	VCC_148
P18	VCC_149
N18	VCC_150
M18	VCC_151
L18	VCC_152
AA17	VCC_153
W17	VCC_154
V17	VCC_155
U17	VCC_156
T17	VCC_157
R17	VCC_158
P17	VCC_159
N17	VCC_160
M17	VCC_161
L17	VCC_162
AA16	VCC_163
W16	VCC_164
V16	VCC_165
U16	VCC_166
T16	VCC_167
R16	VCC_168
P16	VCC_169
N16	VCC_170
M16	VCC_171
L16	VCC_172
AA15	VCC_173
W15	VCC_174
V15	VCC_175
U15	VCC_176
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R15	VCC_178
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R14	VCC_188
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N14	VCC_190
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W13	VCC_194
V13	VCC_195
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T13	VCC_197
R13	VCC_198
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M13	VCC_201
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AA12	VCC_203
W12	VCC_204
V12	VCC_205
U12	VCC_206
T12	VCC_207
R12	VCC_208
P12	VCC_209
N12	VCC_210
M12	VCC_211
L12	VCC_212
AA11	VCC_213
W11	VCC_214
V11	VCC_215
U11	VCC_216
T11	VCC_217
R11	VCC_218
P11	VCC_219
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L11	VCC_222
AA10	VCC_223
W10	VCC_224
V10	VCC_225
U10	VCC_226
T10	VCC_227
R10	VCC_228
P10	VCC_229
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M10	VCC_231
L10	VCC_232
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V9	VCC_235
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AA8	VCC_243
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V8	VCC_245
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T8	VCC_247
R8	VCC_248
P8	VCC_249
N8	VCC_250
M8	VCC_251
L8	VCC_252
AA7	VCC_253
W7	VCC_254
V7	VCC_255
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AA6	VCC_263
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M6	VCC_271
L6	VCC_272
AA5	VCC_273
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P4	VCC_289
N4	VCC_290
M4	VCC_291
L4	VCC_292
AA3	VCC_293
W3	VCC_294
V3	VCC_295
U3	VCC_296
T3	VCC_297
R3	VCC_298
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N3	VCC_300
M3	VCC_301
L3	VCC_302
AA2	VCC_303
W2	VCC_304
V2	VCC_305
U2	VCC_306
T2	VCC_307
R2	VCC_308
P2	VCC_309
N2	VCC_310
M2	VCC_311
L2	VCC_312
AA1	VCC_313
W1	VCC_314
V1	VCC_315
U1	VCC_316
T1	VCC_317
R1	VCC_318
P1	VCC_319
N1	VCC_320
M1	VCC_321
L1	VCC_322



CALISTOGA

NCTF

CALISTOGA

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
CALISTOGA(VCC CORE) 6 of 7			
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7 MCH_CFG_5 ← 1 ● 30MIL TP45

MCH_CFG_5
Low = DMIX2
High = DMIX4

7 MCH_CFG_6 ← 1 ● 30MIL TP40

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

7 MCH_CFG_7 ← 1 ● 30MIL TP36

MCH_CFG_7 (CPU Strap)
Low = RSVD
High = Mobile Yonah processor

7 MCH_CFG_9 ← 1 ● 30MIL TP35

MCH_CFG_9 (PCIe Graphics Lane)
Low = Reverse Lane operation
High = Normal operation

For layout convenience

7 MCH_CFG_10 ← 1 ● 30MIL TP35

MCH_CFG_10 (HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

7 MCH_CFG_11 ← 1 ● 30MIL TP35

MCH_CFG_11 (PSB 4x CLK ENABLE)
Low = Reserved
High = Calistoga

7 MCH_CFG_12 ← 1 ● 30MIL TP47

7 MCH_CFG_13 ← 1 ● 30MIL TP55

MCH_CFG_[13:12] (XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 ← 1 ● 30MIL TP44

MCH_CFG_16 (FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

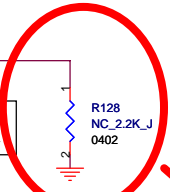
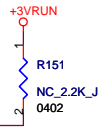
MCH_CFG_18 (VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

MCH_CFG_19 (DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

MCH_CFG_20 (PCIe Backward Interoperability mode)
Low = Only SDVO or PCIe x1 is operational (defaults)
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

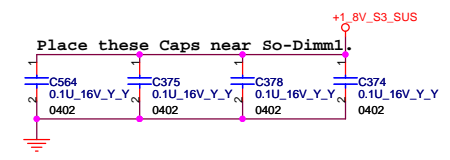
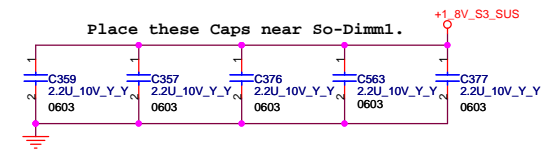
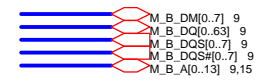
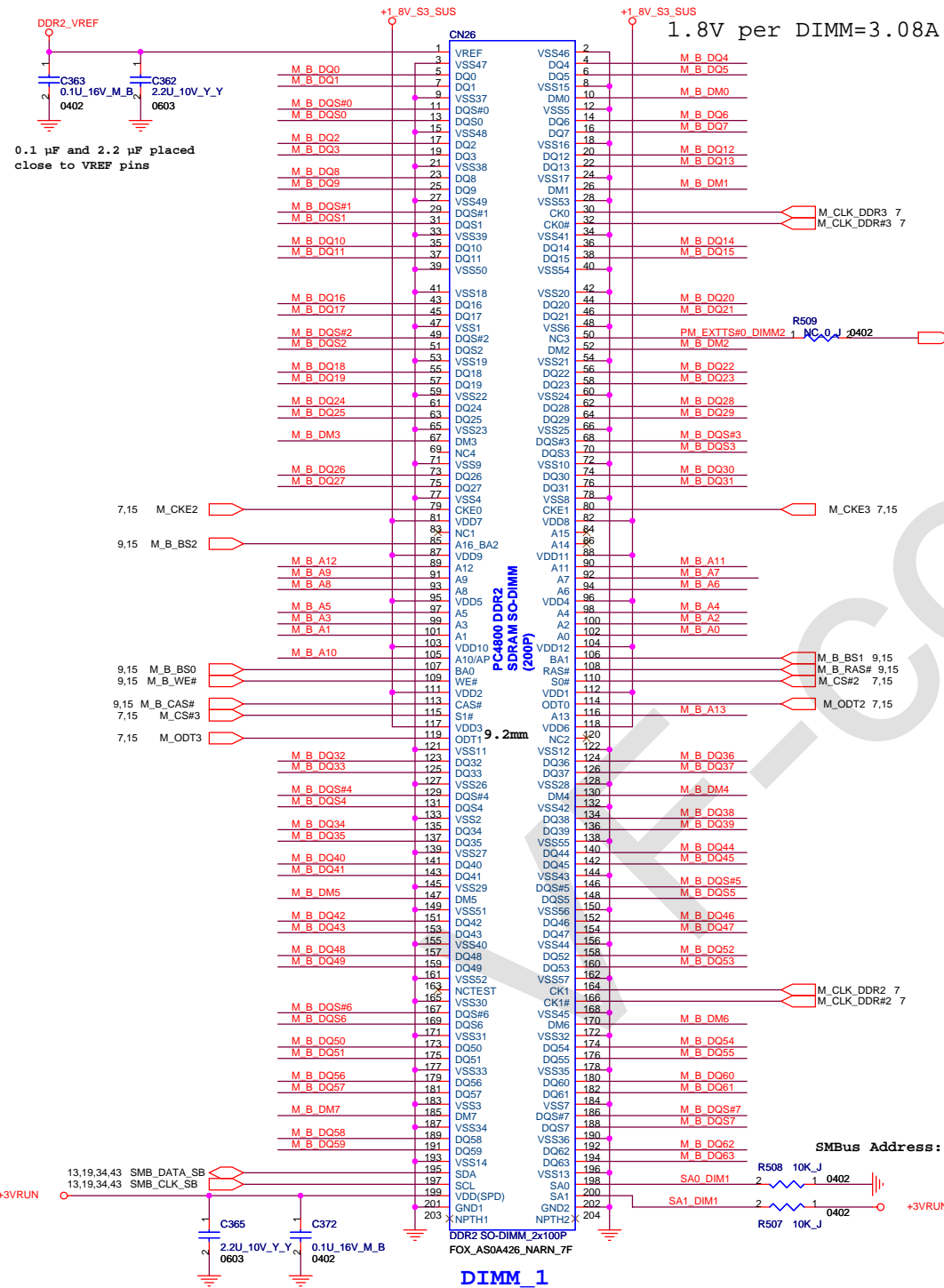
Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

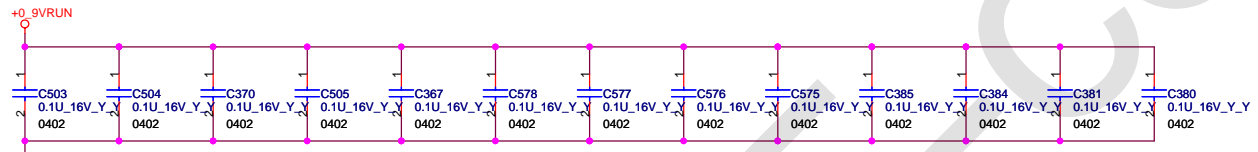
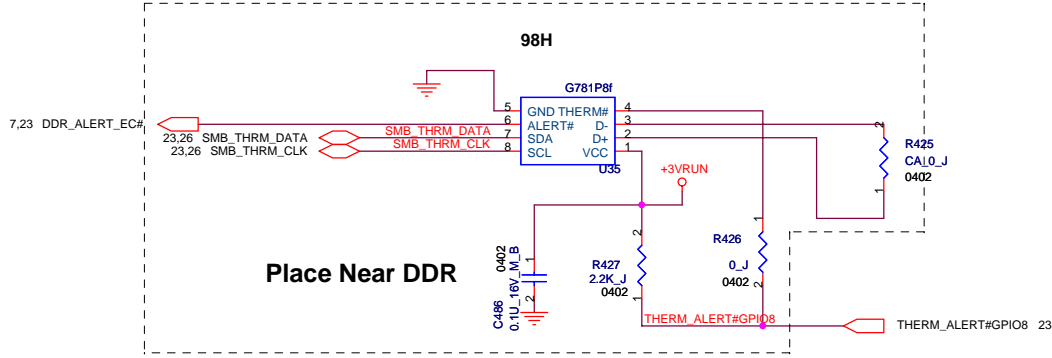


AC41	VSS_0	AK34	VSS_97
AA41	VSS_1	AG34	VSS_98
W41	VSS_2	AF34	VSS_99
T41	VSS_3	AE34	VSS_100
P41	VSS_4	AC34	VSS_101
M41	VSS_5	C34	VSS_102
J41	VSS_6	AW33	VSS_103
F41	VSS_7	AV33	VSS_104
AV40	VSS_8	AR33	VSS_105
AP40	VSS_9	AE33	VSS_106
AN40	VSS_10	AB33	VSS_107
AK40	VSS_11	Y33	VSS_108
AH40	VSS_12	V33	VSS_109
AG40	VSS_13	T33	VSS_110
AF40	VSS_14	R33	VSS_111
AE40	VSS_15	M33	VSS_112
AE40	VSS_16	H33	VSS_113
B40	VSS_17	G33	VSS_114
AY39	VSS_18	F33	VSS_115
AW39	VSS_19	D33	VSS_116
AV39	VSS_20	B33	VSS_117
AR39	VSS_21	AH32	VSS_118
AN39	VSS_22	AG32	VSS_119
AJ39	VSS_23	AF32	VSS_120
AC39	VSS_24	AE32	VSS_121
AB39	VSS_25	E32	VSS_122
AA39	VSS_26	D32	VSS_123
Y39	VSS_27	C32	VSS_124
W39	VSS_28	B32	VSS_125
V39	VSS_29	AY31	VSS_126
T39	VSS_30	AV31	VSS_127
R39	VSS_31	AW30	VSS_128
P39	VSS_32	AN31	VSS_129
N39	VSS_33	AA20	VSS_130
M39	VSS_34	AA20	VSS_131
L39	VSS_35	Y31	VSS_132
J39	VSS_36	AB30	VSS_133
H39	VSS_37	E30	VSS_134
G39	VSS_38	AT29	VSS_135
F39	VSS_39	AN29	VSS_136
D39	VSS_40	AG29	VSS_137
C39	VSS_41	AE29	VSS_138
AT38	VSS_42	T29	VSS_139
AM38	VSS_43	N29	VSS_140
AH38	VSS_44	P18	VSS_141
AG38	VSS_45	H18	VSS_142
AF38	VSS_46	E29	VSS_143
AE38	VSS_47	D18	VSS_144
C38	VSS_48	A18	VSS_145
AK37	VSS_49	B29	VSS_146
AH37	VSS_50	A29	VSS_147
AB37	VSS_51	BA28	VSS_148
AA37	VSS_52	AM17	VSS_149
Y37	VSS_53	AM17	VSS_150
W37	VSS_54	AL28	VSS_151
V37	VSS_55	AP28	VSS_152
T37	VSS_56	AM28	VSS_153
R37	VSS_57	AD28	VSS_154
P37	VSS_58	AC28	VSS_155
N37	VSS_59	W28	VSS_156
M37	VSS_60	J28	VSS_157
L37	VSS_61	C18	VSS_158
J37	VSS_62	E28	VSS_159
H37	VSS_63	AP27	VSS_160
G37	VSS_64	AM27	VSS_161
F37	VSS_65	AK27	VSS_162
D37	VSS_66	J27	VSS_163
C37	VSS_67	L15	VSS_164
AK14	VSS_68	F15	VSS_165
AH14	VSS_69	C27	VSS_166
AG14	VSS_70	B27	VSS_167
AF14	VSS_71	AM26	VSS_168
AE14	VSS_72	M26	VSS_169
AE14	VSS_73	AD26	VSS_170
B14	VSS_74	AA14	VSS_171
AY14	VSS_75	F26	VSS_172
AW14	VSS_76	D26	VSS_173
AV14	VSS_77	U14	VSS_174
AR14	VSS_78	K14	VSS_175
AN14	VSS_79	P25	VSS_176
AJ14	VSS_80	H14	VSS_177
AK14	VSS_81	E14	VSS_178
AH14	VSS_82	AV13	VSS_179
AG14	VSS_83	E25	
AF14	VSS_84	D25	
AE14	VSS_85	A25	
AE14	VSS_86	BA24	
B14	VSS_87	AU24	
AY14	VSS_88	AL24	
AW14	VSS_89	P13	
AV14	VSS_90	D13	
AR14	VSS_91	B13	
AN14	VSS_92	AY12	
AJ14	VSS_93	AC12	
AK14	VSS_94	VSS_267	
AH14	VSS_95	H12	
AG14	VSS_96	E12	
AF14		AD11	
AE14		AA11	
AE14		VSS_270	
B14		Y11	

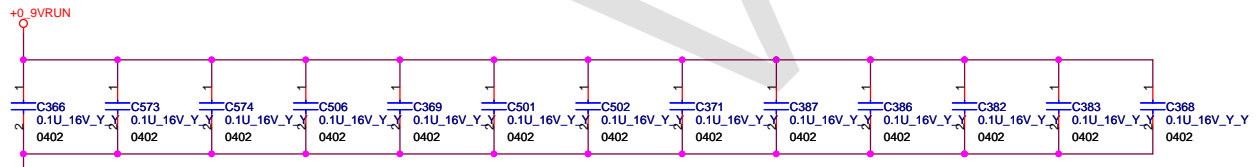
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AN23	VSS_181	D11	VSS_274
AM23	VSS_182	B11	VSS_275
AH23	VSS_183	AV10	VSS_276
AG23	VSS_184	AP10	VSS_277
AF23	VSS_185	AL10	VSS_278
AE23	VSS_186	AJ10	VSS_279
AE23	VSS_187	AG10	VSS_280
B23	VSS_188	AC10	VSS_281
C23	VSS_189	W10	VSS_282
AA22	VSS_190	U10	VSS_283
Y22	VSS_191	BA9	VSS_284
G22	VSS_192	AW9	VSS_285
E22	VSS_193	AR9	VSS_286
D22	VSS_194	AH9	VSS_287
A22	VSS_195	AB9	VSS_288
G33	VSS_196	Y9	VSS_289
F33	VSS_197	E9	VSS_290
AR21	VSS_198	G9	VSS_291
AN21	VSS_199	E9	VSS_292
AL21	VSS_200	A9	VSS_293
AB21	VSS_201	AG8	VSS_294
P21	VSS_202	AD8	VSS_295
VSS_203	VSS_203	AA8	VSS_296
VSS_204	VSS_204	VSS_297	VSS_297
VSS_205	VSS_205	VSS_298	VSS_298
VSS_206	VSS_206	VSS_299	VSS_299
VSS_207	VSS_207	VSS_300	VSS_300
VSS_208	VSS_208	VSS_301	VSS_301
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VSS_212	VSS_212	VSS_305	VSS_305
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VSS_214	VSS_214	VSS_307	VSS_307
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VSS_230	VSS_230	VSS_323	VSS_323
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VSS_232	VSS_232	VSS_325	VSS_325
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VSS_256	VSS_256	VSS_349	VSS_349
VSS_257	VSS_257	VSS_350	VSS_350
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VSS_262	VSS_262	VSS_355	VSS_355
VSS_263	VSS_263	VSS_356	VSS_356
VSS_264	VSS_264	VSS_357	VSS_357
VSS_265	VSS_265	VSS_358	VSS_358
VSS_266	VSS_266	VSS_359	VSS_359
VSS_267	VSS_267	VSS_360	VSS_360



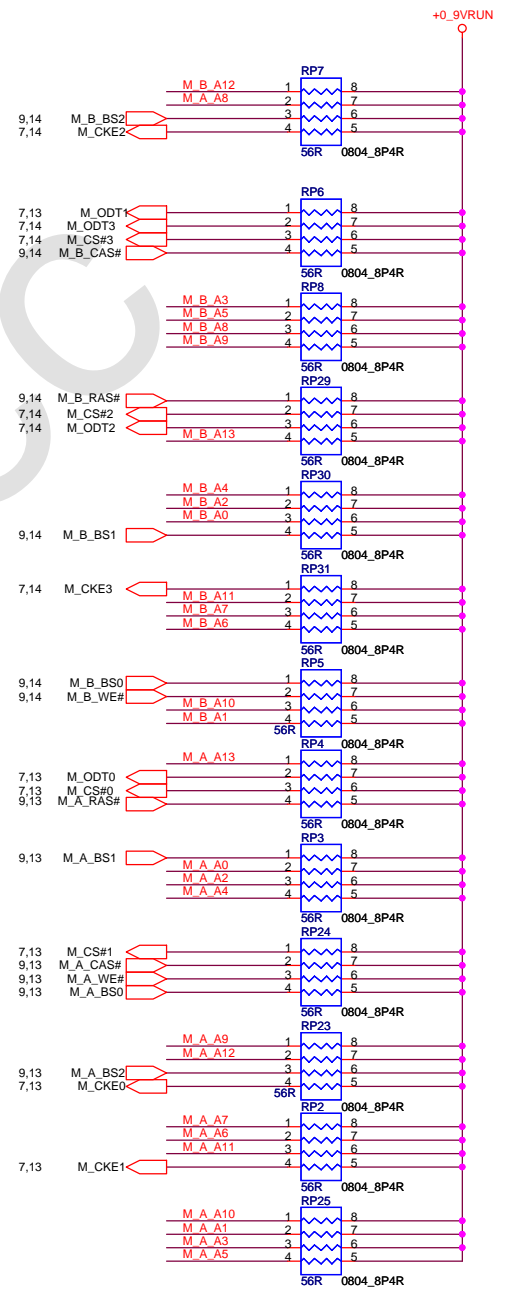
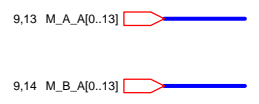
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CPBG - R&D Division		
Title DDR(I)SO-DIMM_1		
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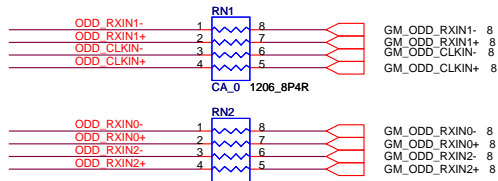
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



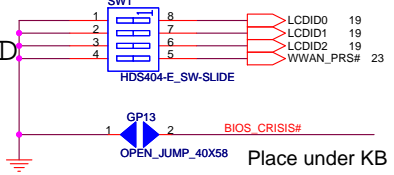
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



LVDS

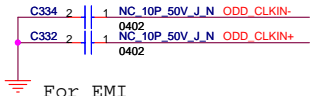


PANEL ID

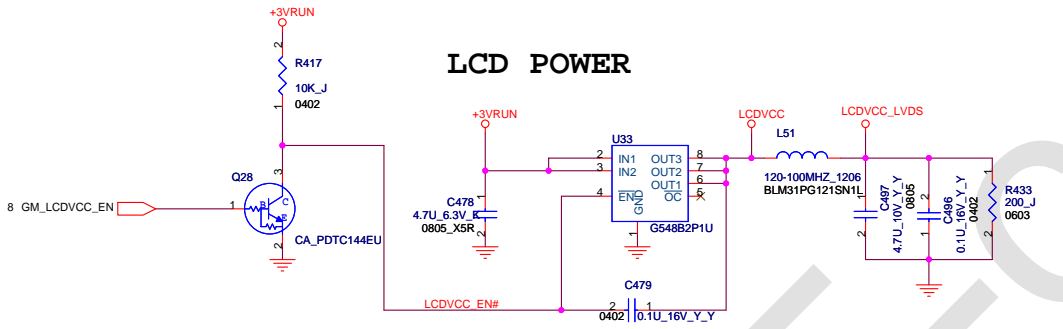


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

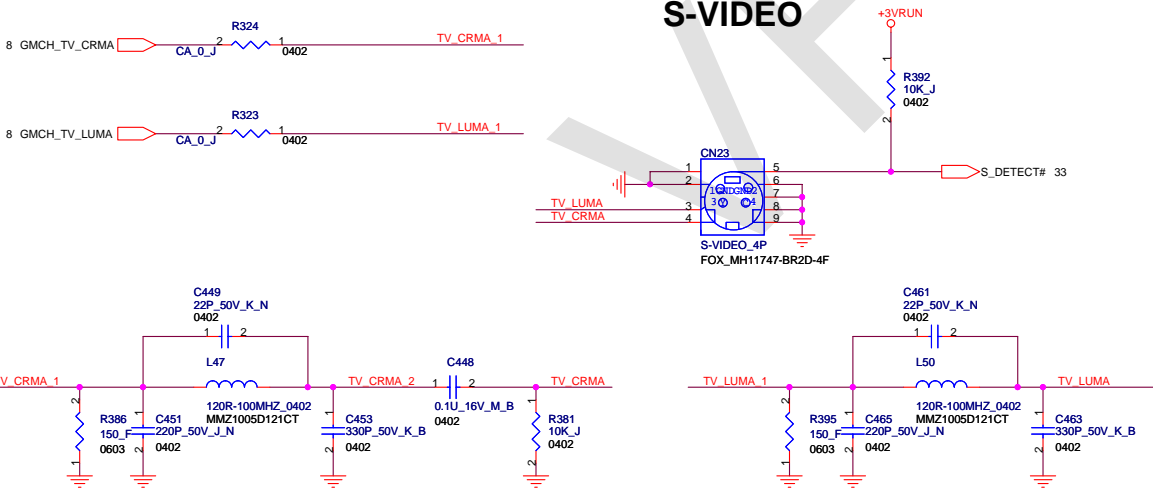
LVDS CONNECTOR



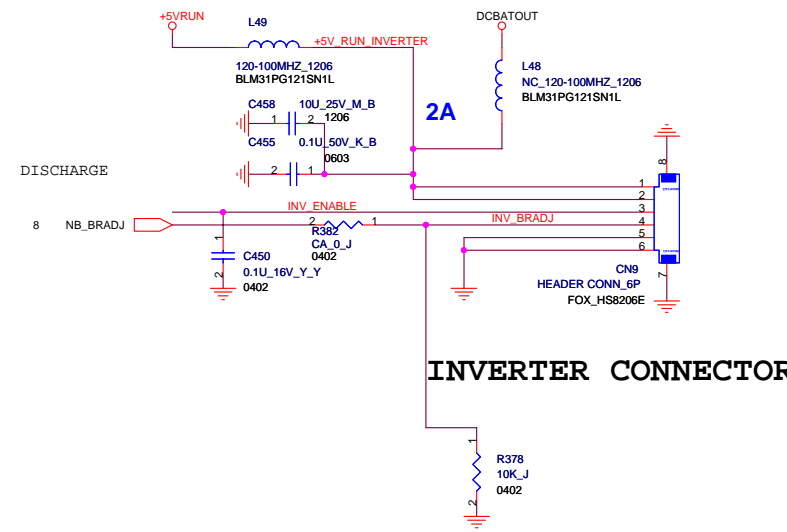
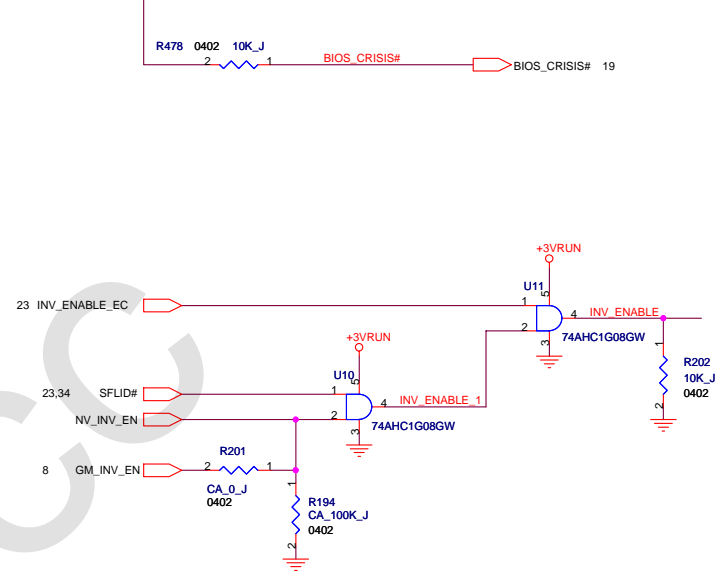
LCD POWER



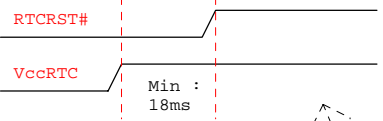
S-VIDEO



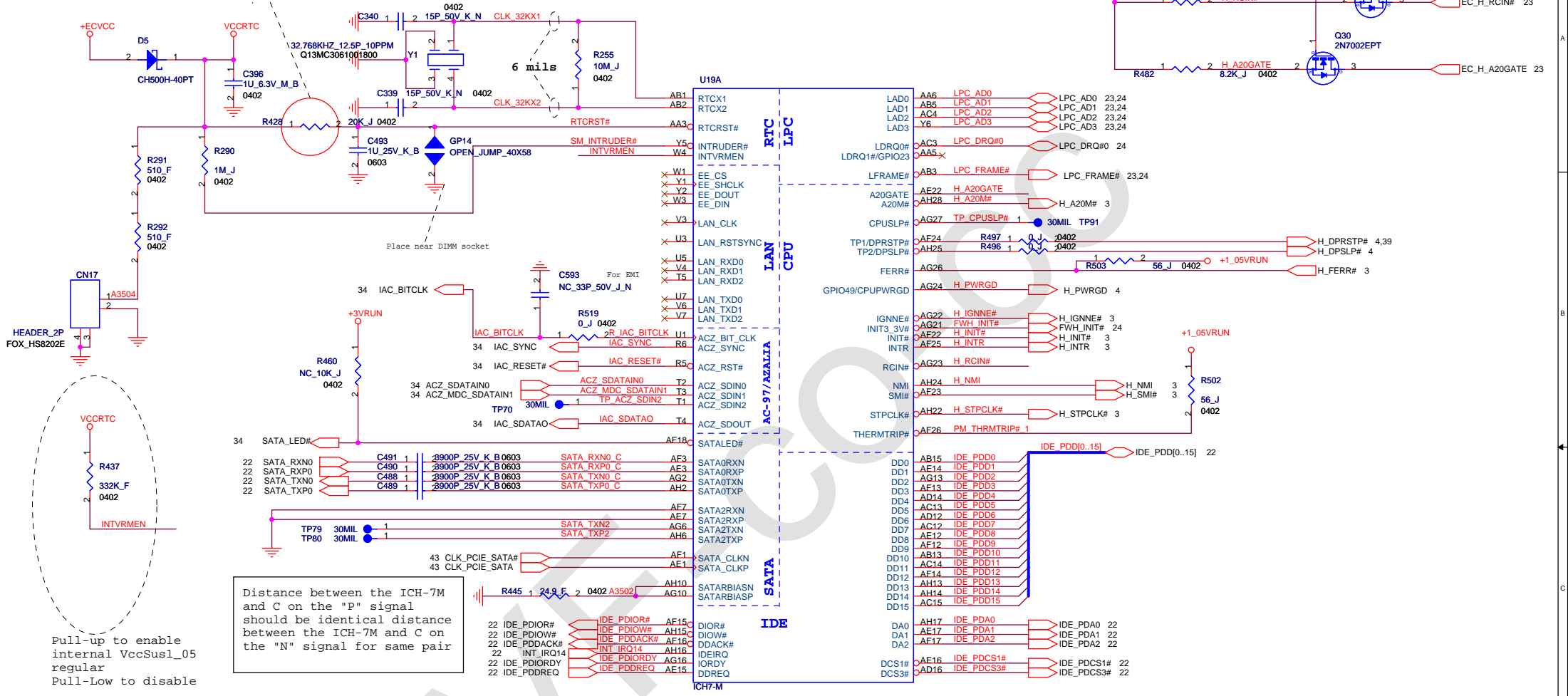
BIOS_CRISIS#



INVERTER CONNECTOR

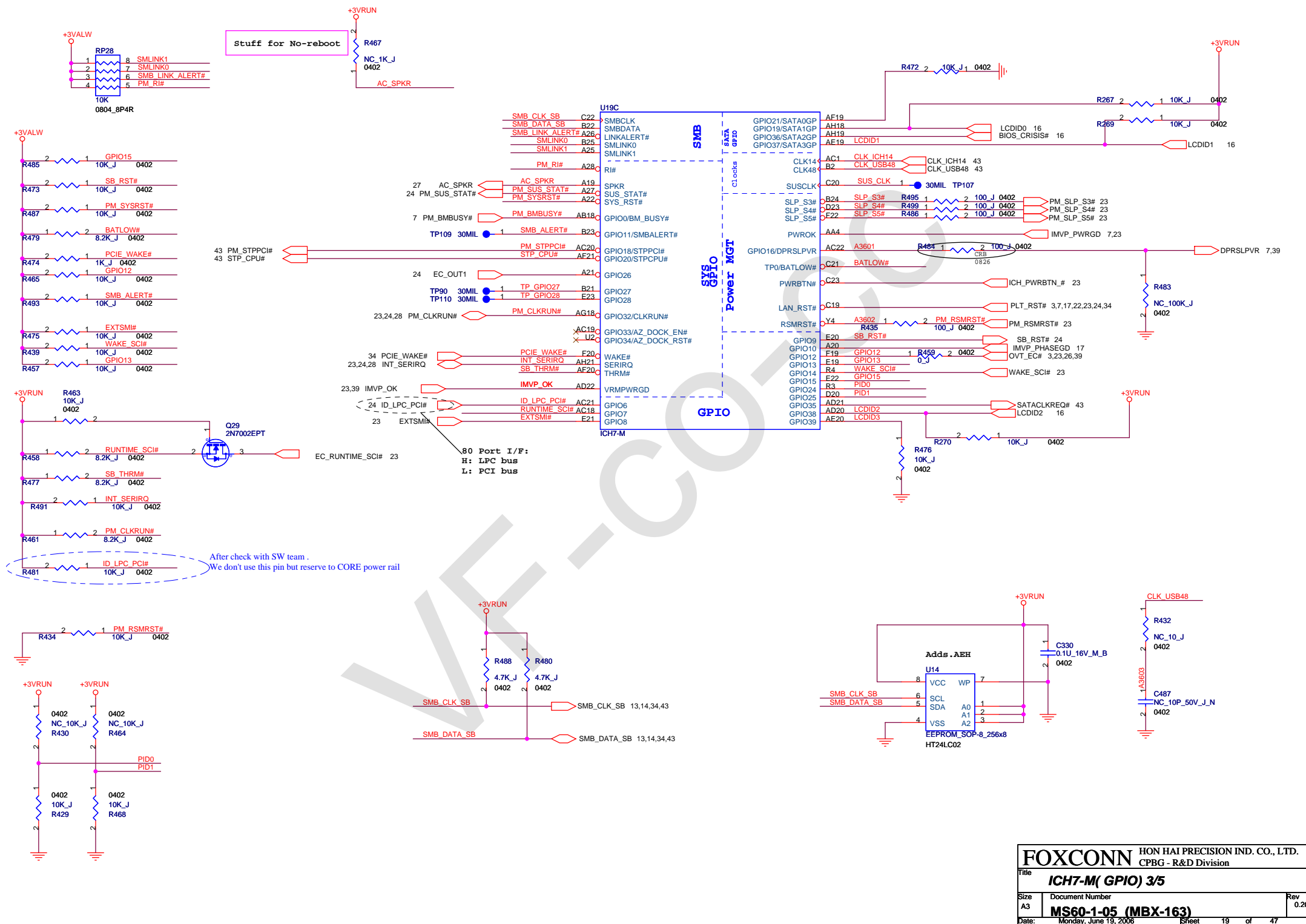


The traces inside this block should be wider.
No digital signals routed under XTAL



Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

Pull-up to enable internal VccSus1_05 regular
Pull-Low to disable



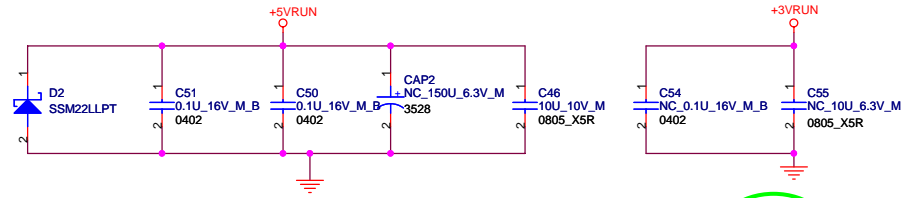
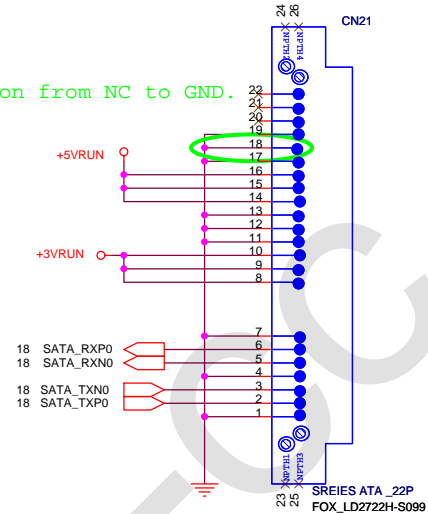
U19E			P28
A4	VSS[1]	VSS[98]	R1
A23	VSS[2]	VSS[99]	R11
B1	VSS[3]	VSS[100]	R12
B8	VSS[4]	VSS[101]	R13
B11	VSS[5]	VSS[102]	R14
B14	VSS[6]	VSS[103]	R15
B17	VSS[7]	VSS[104]	R16
B20	VSS[8]	VSS[105]	R17
B26	VSS[9]	VSS[106]	R18
B28	VSS[10]	VSS[107]	T6
C2	VSS[11]	VSS[108]	T12
C6	VSS[12]	VSS[109]	T13
C27	VSS[13]	VSS[110]	T14
D10	VSS[14]	VSS[111]	T15
D13	VSS[15]	VSS[112]	T16
D18	VSS[16]	VSS[113]	T17
D21	VSS[17]	VSS[114]	U4
D24	VSS[18]	VSS[115]	U12
E1	VSS[19]	VSS[116]	U13
E2	VSS[20]	VSS[117]	U14
F4	VSS[21]	VSS[118]	U15
F8	VSS[22]	VSS[119]	U16
F15	VSS[23]	VSS[120]	U17
F3	VSS[24]	VSS[121]	U24
F4	VSS[25]	VSS[122]	U25
F5	VSS[26]	VSS[123]	U26
F12	VSS[27]	VSS[124]	V2
F27	VSS[28]	VSS[125]	V13
F28	VSS[29]	VSS[126]	V15
G1	VSS[30]	VSS[127]	V24
G2	VSS[31]	VSS[128]	V27
G5	VSS[32]	VSS[129]	V28
G6	VSS[33]	VSS[130]	W6
G9	VSS[34]	VSS[131]	W24
G14	VSS[35]	VSS[132]	W25
G18	VSS[36]	VSS[133]	W26
G21	VSS[37]	VSS[134]	Y3
G24	VSS[38]	VSS[135]	Y24
G25	VSS[39]	VSS[136]	Y27
G26	VSS[40]	VSS[137]	Y28
H3	VSS[41]	VSS[138]	AA1
H4	VSS[42]	VSS[139]	AA24
H5	VSS[43]	VSS[140]	AA25
H24	VSS[44]	VSS[141]	AA26
H27	VSS[45]	VSS[142]	AB4
H28	VSS[46]	VSS[143]	AB6
J1	VSS[47]	VSS[144]	AB11
J2	VSS[48]	VSS[145]	AB14
J5	VSS[49]	VSS[146]	AB16
J24	VSS[50]	VSS[147]	AB19
J25	VSS[51]	VSS[148]	AB21
J26	VSS[52]	VSS[149]	AB24
K24	VSS[53]	VSS[150]	AB27
K27	VSS[54]	VSS[151]	AB28
K28	VSS[55]	VSS[152]	AC2
L13	VSS[56]	VSS[153]	AC5
L15	VSS[57]	VSS[154]	AC9
L24	VSS[58]	VSS[155]	AC11
L25	VSS[59]	VSS[156]	AD1
L26	VSS[60]	VSS[157]	AD3
M3	VSS[61]	VSS[158]	AD4
M4	VSS[62]	VSS[159]	AD7
M5	VSS[63]	VSS[160]	AD8
M12	VSS[64]	VSS[161]	AD11
M13	VSS[65]	VSS[162]	AD15
M14	VSS[66]	VSS[163]	AD19
M15	VSS[67]	VSS[164]	AD23
M16	VSS[68]	VSS[165]	AE2
M17	VSS[69]	VSS[166]	AE4
M24	VSS[70]	VSS[167]	AE8
M27	VSS[71]	VSS[168]	AE11
M28	VSS[72]	VSS[169]	AE13
N1	VSS[73]	VSS[170]	AE18
N2	VSS[74]	VSS[171]	AE21
N5	VSS[75]	VSS[172]	AE24
N6	VSS[76]	VSS[173]	AE25
N11	VSS[77]	VSS[174]	AF2
N12	VSS[78]	VSS[175]	AF4
N13	VSS[79]	VSS[176]	AF8
N14	VSS[80]	VSS[177]	AF11
N15	VSS[81]	VSS[178]	AF27
N16	VSS[82]	VSS[179]	AF28
N17	VSS[83]	VSS[180]	AG1
N24	VSS[84]	VSS[181]	AG3
N25	VSS[85]	VSS[182]	AG7
N26	VSS[86]	VSS[183]	AG11
N26	VSS[87]	VSS[184]	AG14
P3	VSS[88]	VSS[185]	AG17
P4	VSS[89]	VSS[186]	AG20
P12	VSS[90]	VSS[187]	AG25
P13	VSS[91]	VSS[188]	AH1
P14	VSS[92]	VSS[189]	AH3
P15	VSS[93]	VSS[190]	AH7
P16	VSS[94]	VSS[191]	AH12
P17	VSS[95]	VSS[192]	AH23
P24	VSS[96]	VSS[193]	AH27
P27	VSS[97]	VSS[194]	

ICH7-M

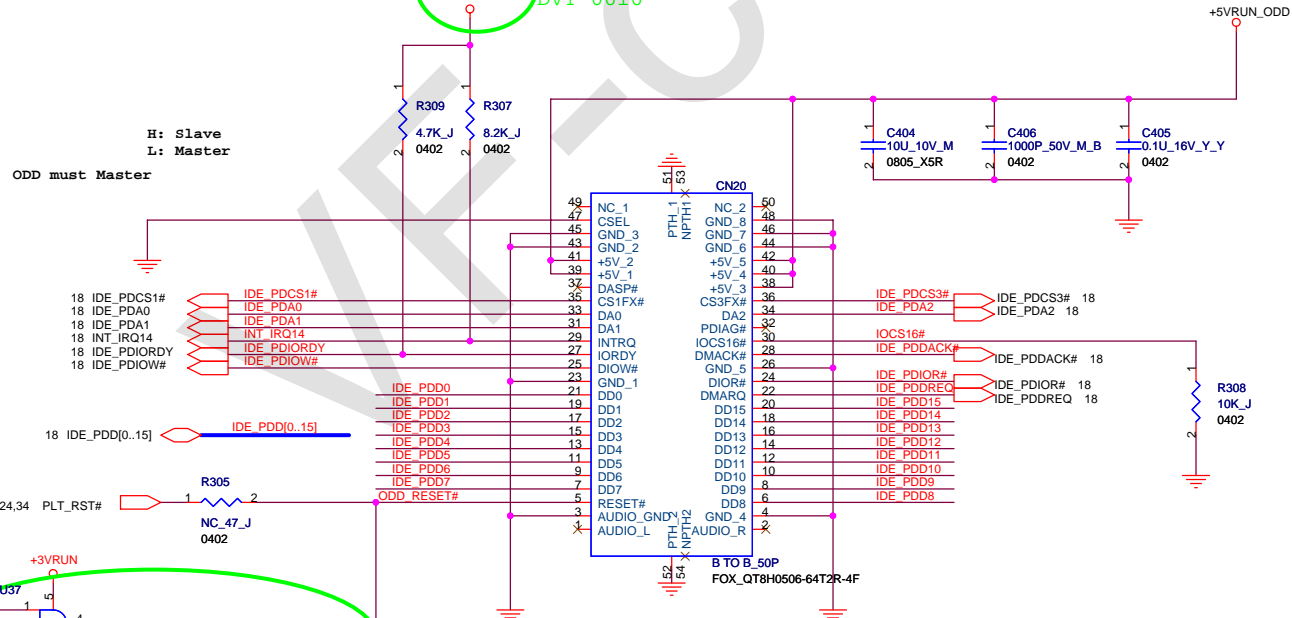
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		CPBG - R&D Division	
Title			
ICH7-M(GND) 5/5			
Size	Document Number		Rev
A3	MS60-1-05 (MBX-163)		0.20
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SATA HDD CONN

CN21's pin18 change connection from NC to GND.
DVT 0616



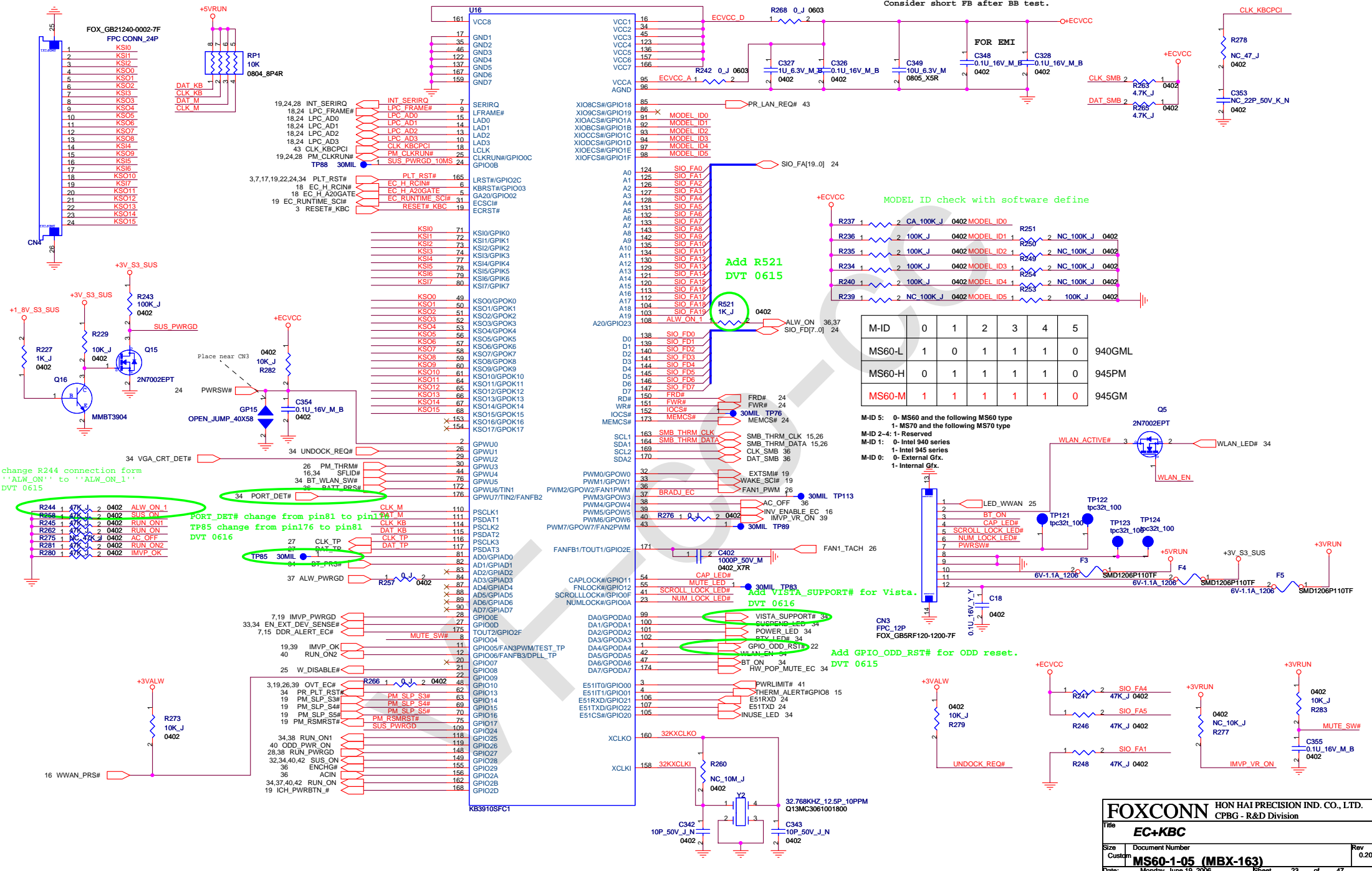
+3VRUN_ODD
Change from +3VRUN to +3VRUN_ODD
DVT 0616



CD-ROM CONN

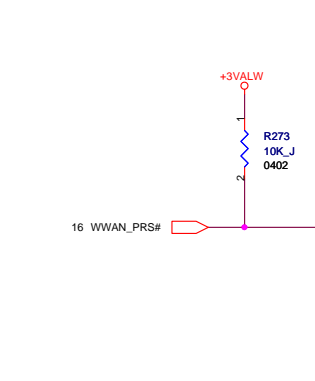
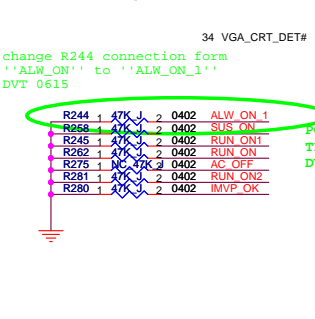
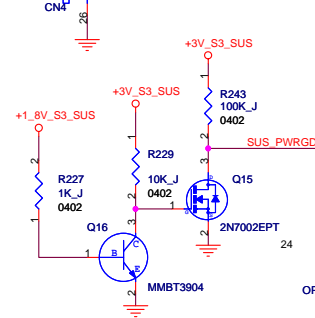
Del R516, R517, C580
DVT 0615

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
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Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20
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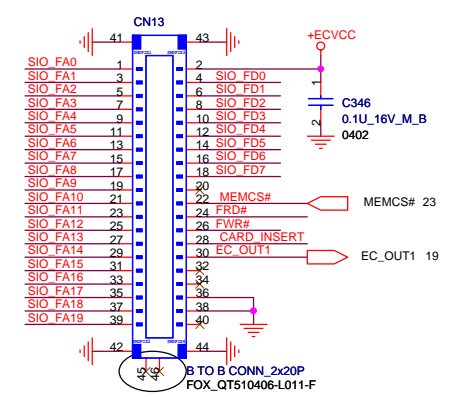
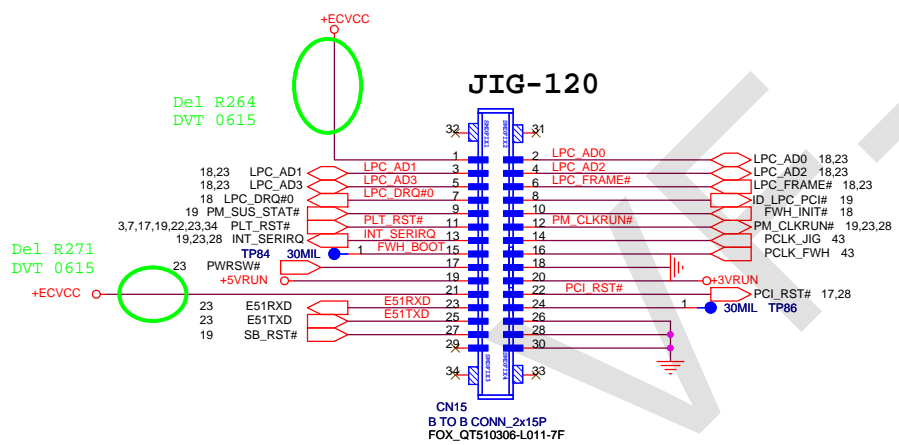
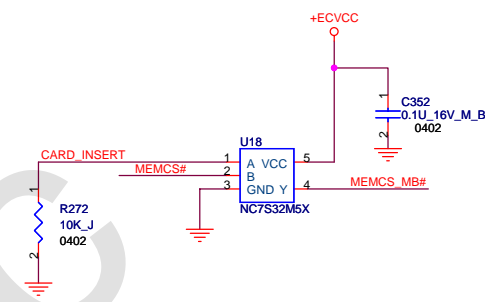
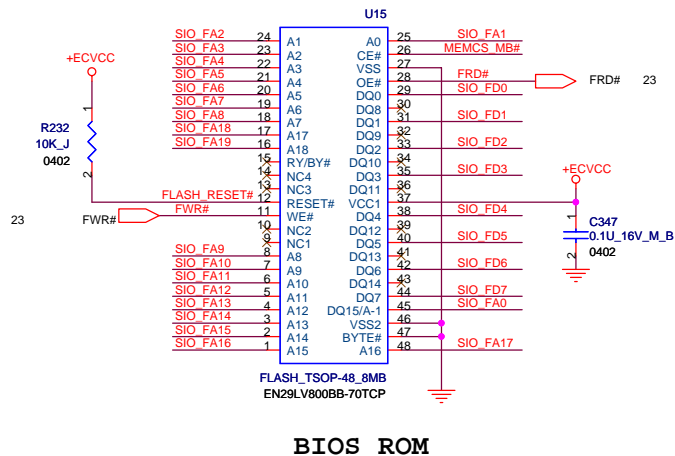
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FPC CONN_24P

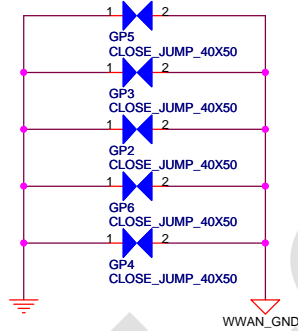
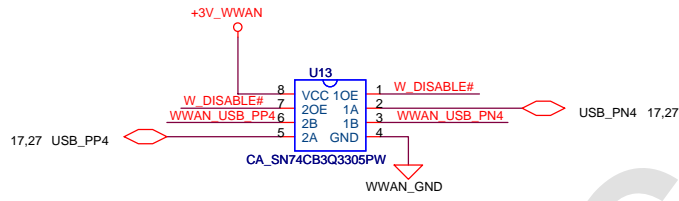
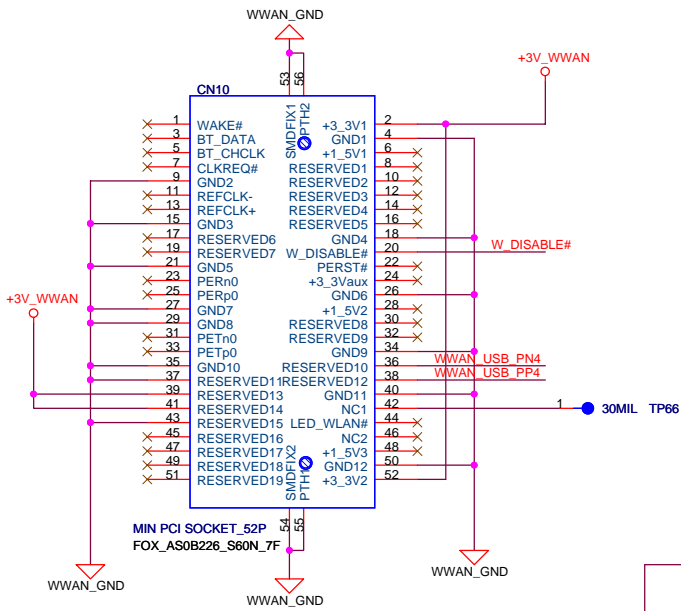
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12	KS07
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15	KS09
16	KS15
17	KS16
18	KS010
19	KS17
20	KS011
21	KS012
22	KS013
23	KS014
24	KS015



161	VCC8
17	GND1
18	GND2
19	GND3
20	GND4
21	GND5
22	GND6
23	GND7
24	GND7
7	INT_SERIRQ
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14	LPC_AD0
15	LPC_AD1
16	LPC_AD2
17	LPC_AD3
18	CLK_KBCPCI
25	PM_CLKRUN#
24	SUS_PWRGD
165	PLT_RST#
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5	EC_H_A20GATE
31	EC_RUNTIME_SCI#
3	RESET#_KBC
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35	SDA5
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37	SDA6
38	GPWU6/TIN1
39	SDA7
40	GPWU7/TIN2/FANFB2
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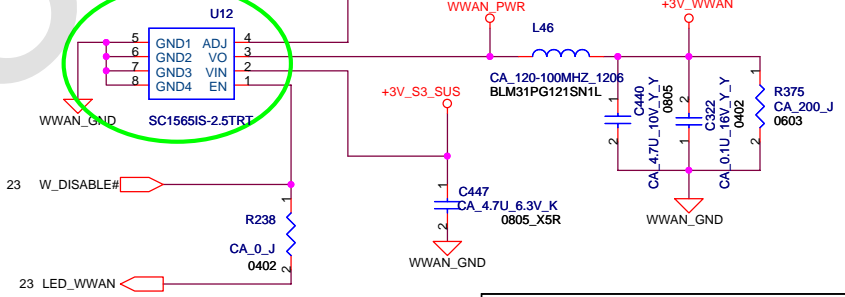
23 SIO_FA[19..0]
 23 SIO_FD[7..0]





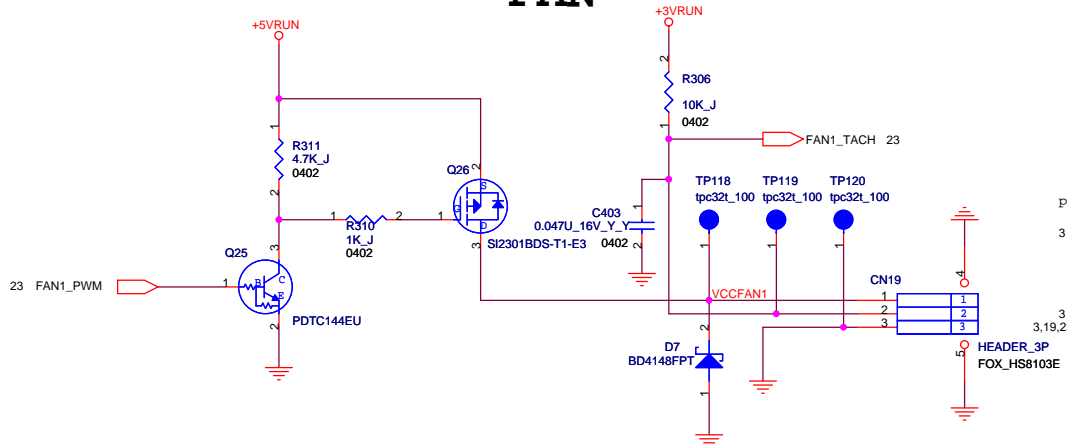
WWAN POWER

U12 change to SC1565IS-2.5TRT
DVT 0617

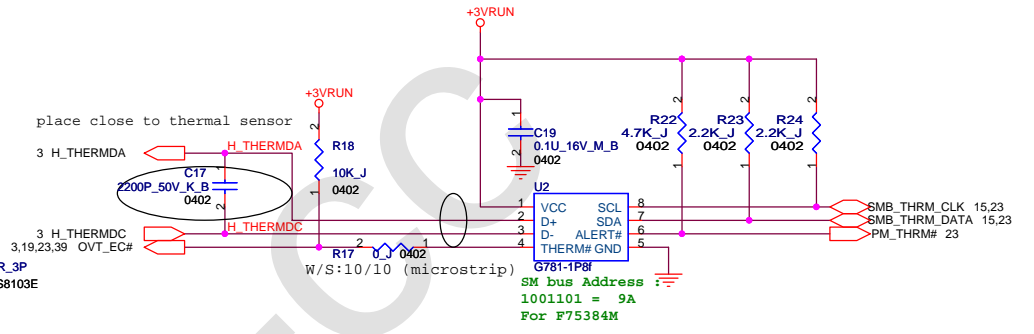


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title WWAN			
Size	Document Number		Rev
Custom	MS60-1-05 (MBX-163)		0.20
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FAN

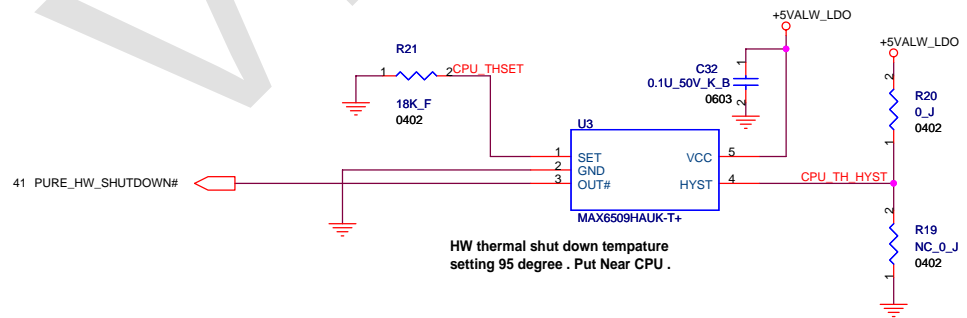


CPU SENSOR



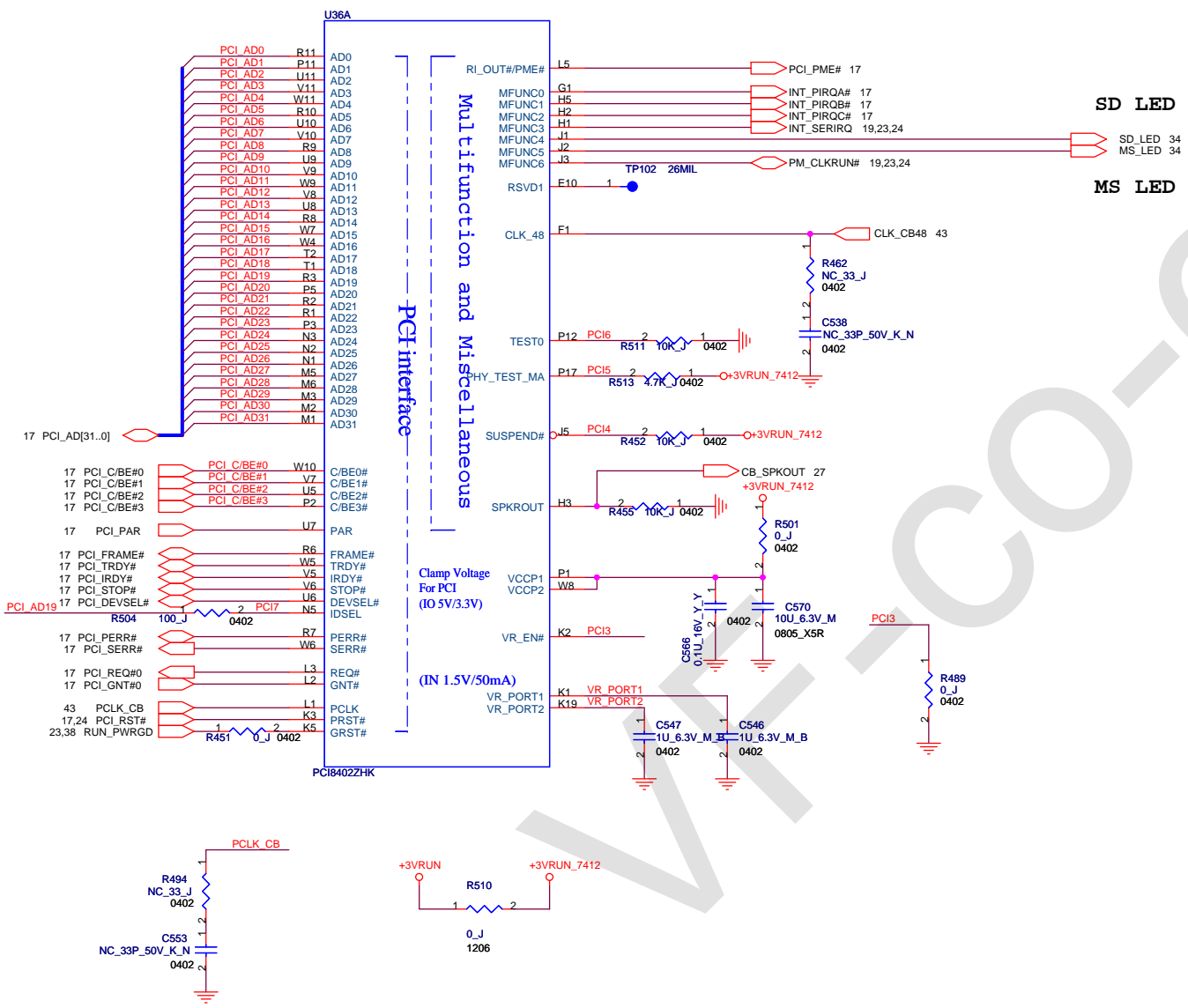
Place Thermal-Sensor near CPU & GMCH.

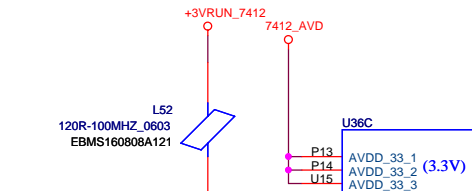
HW THERMAL PROTECTION



HW thermal shut down temperature setting 95 degree . Put Near CPU .

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
FAN/HW THERMAL PROTECT			
Size	Document Number	Rev	
A3	MS60-1-05 (MBX-163)	0.20	
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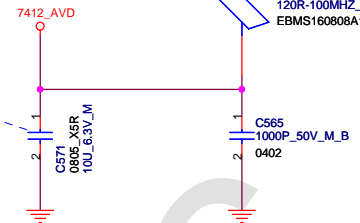


Close to IC

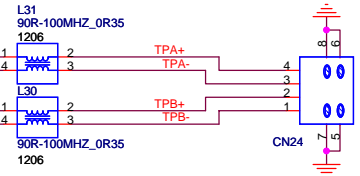
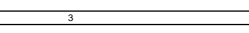
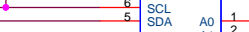
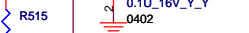
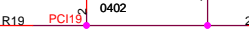
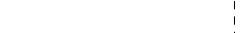
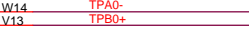
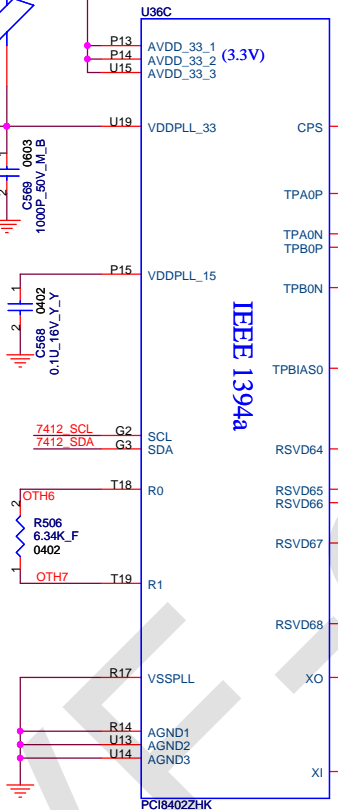
This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

This array must be placed close to AVDD (Pin P13,P14,U15) They must be tied to a low-impedance GND.



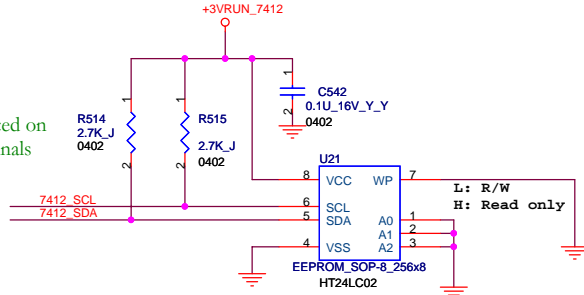
IBBE 1394a



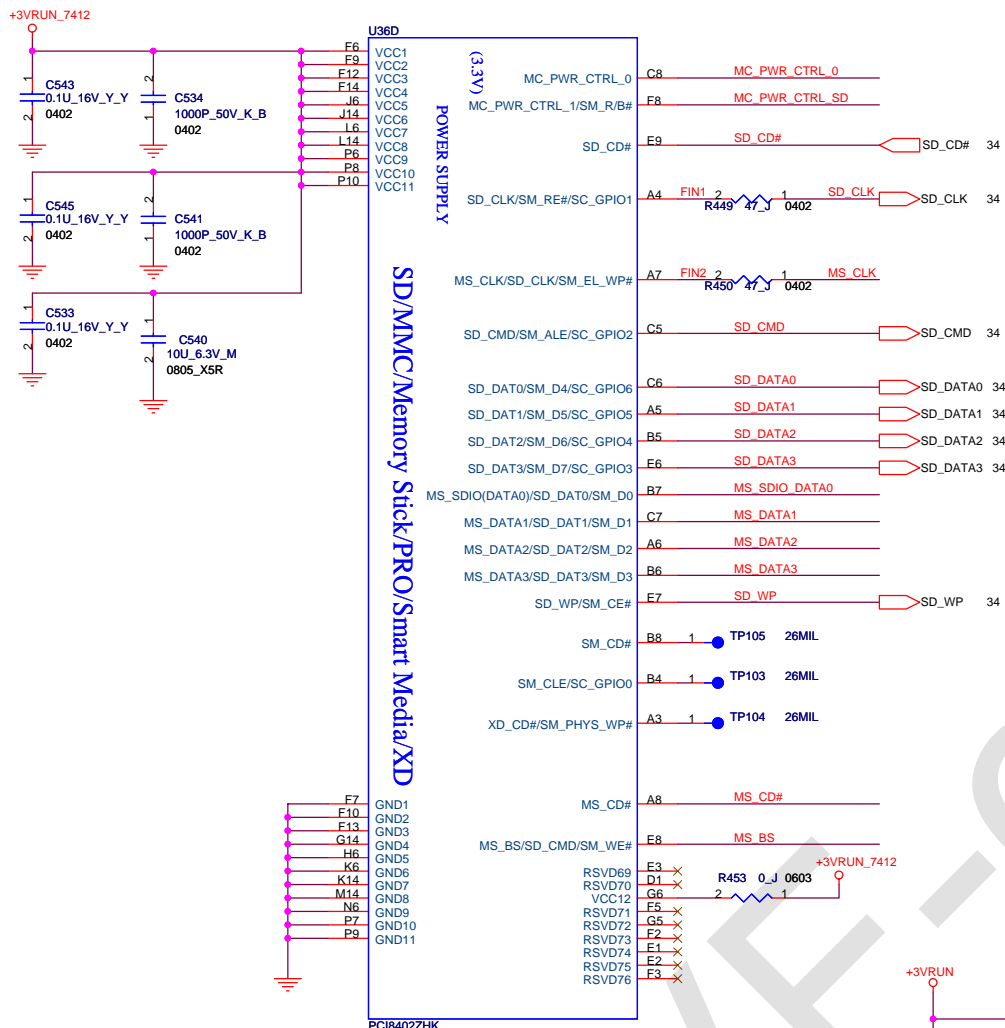
iLink CONN.

Place near PCI8402

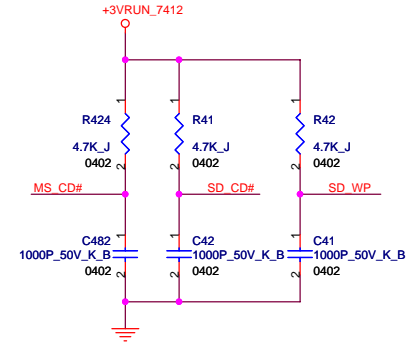
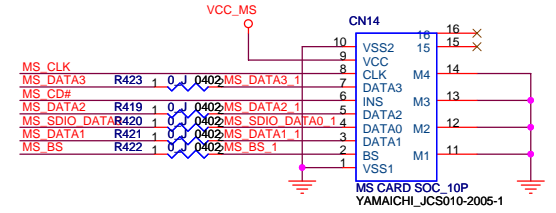
Resistors should be placed on the SCL and SDA terminals



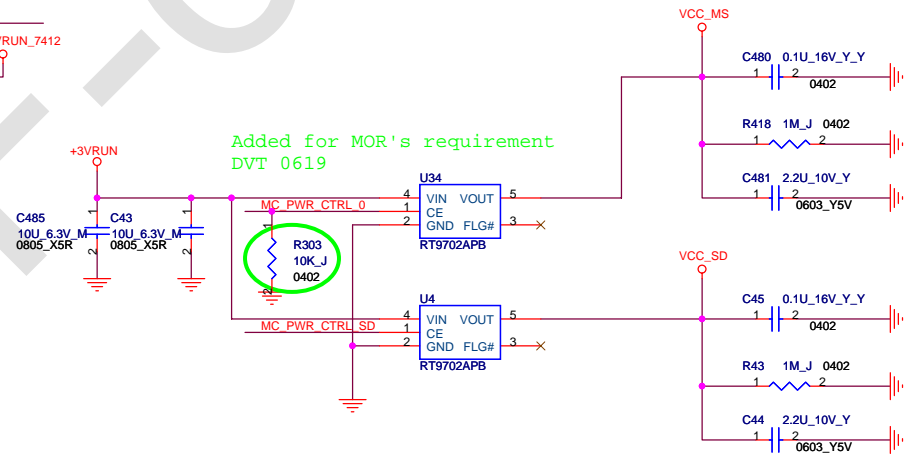
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CPBG - R&D Division		
Title	PCI (I LINK)	
Size	Document Number	Rev
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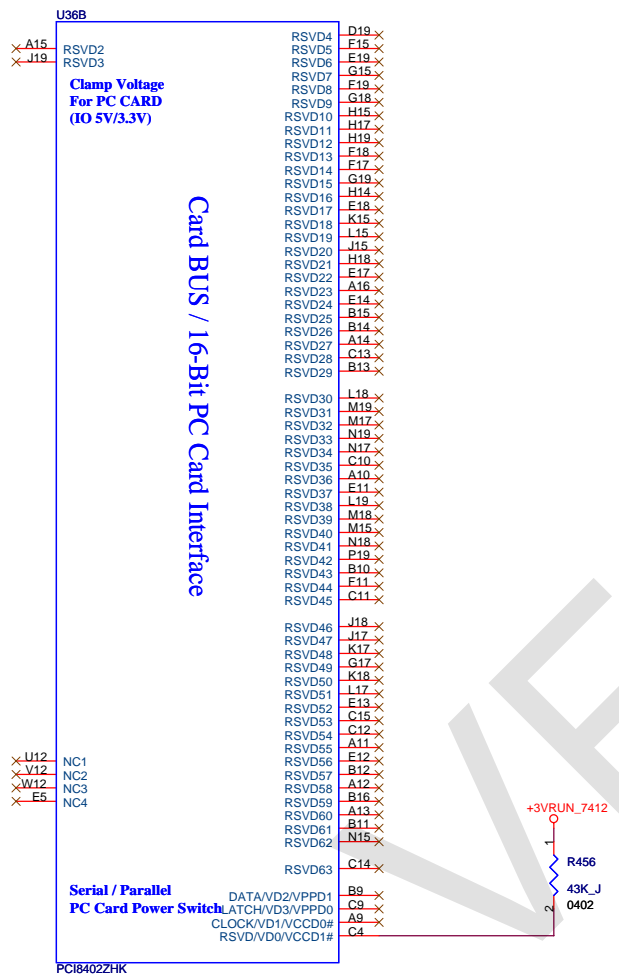


MS Duo / Pro



Added for MOR's requirement
DVT 0619



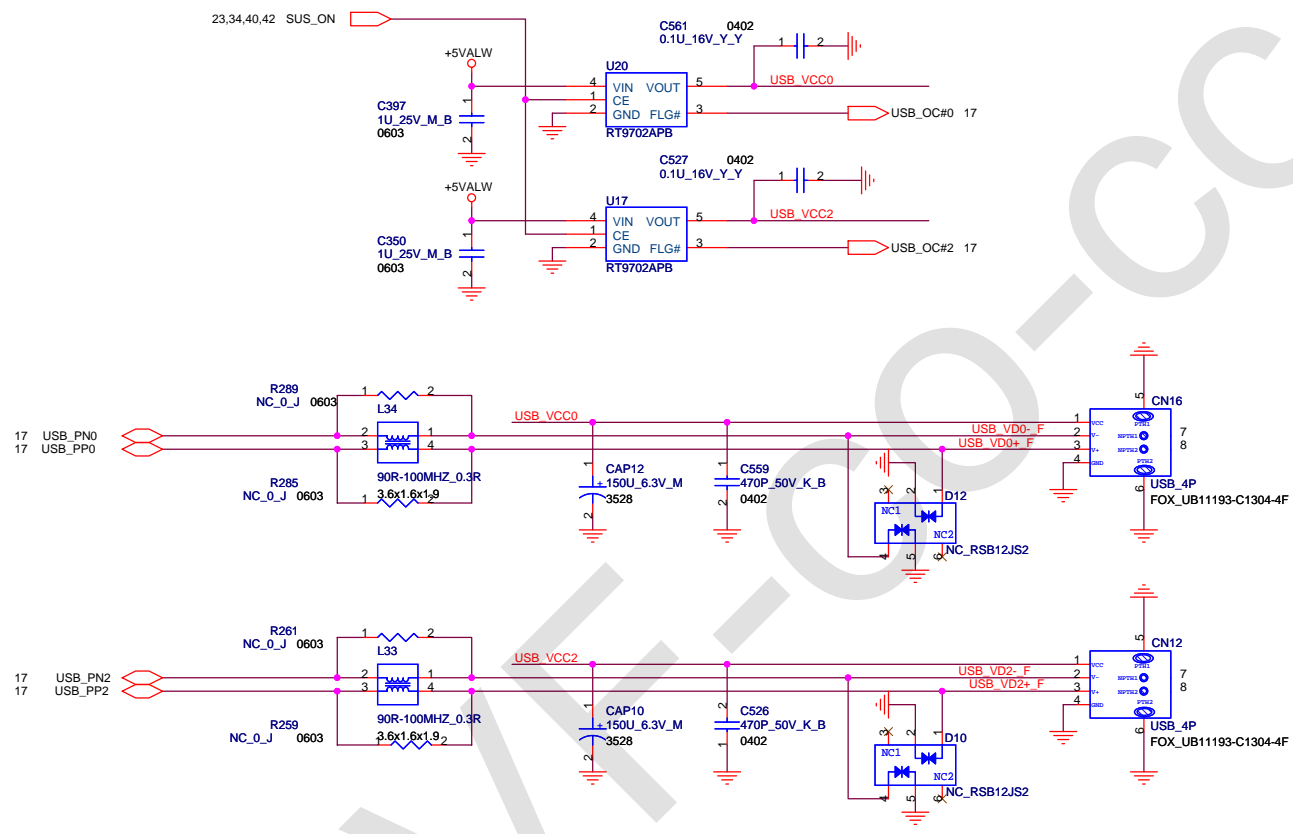


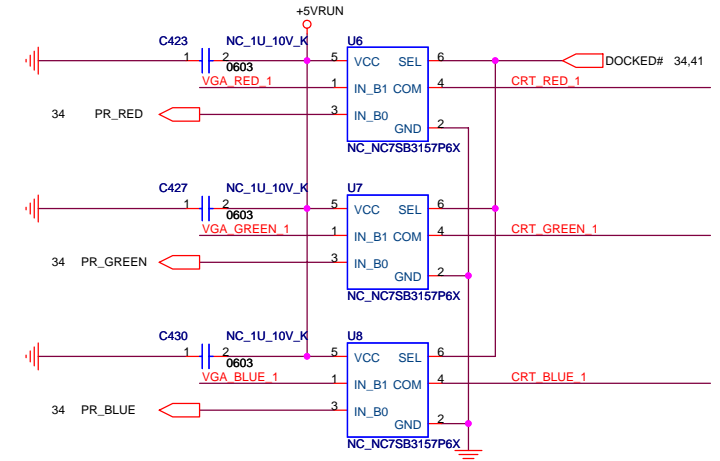
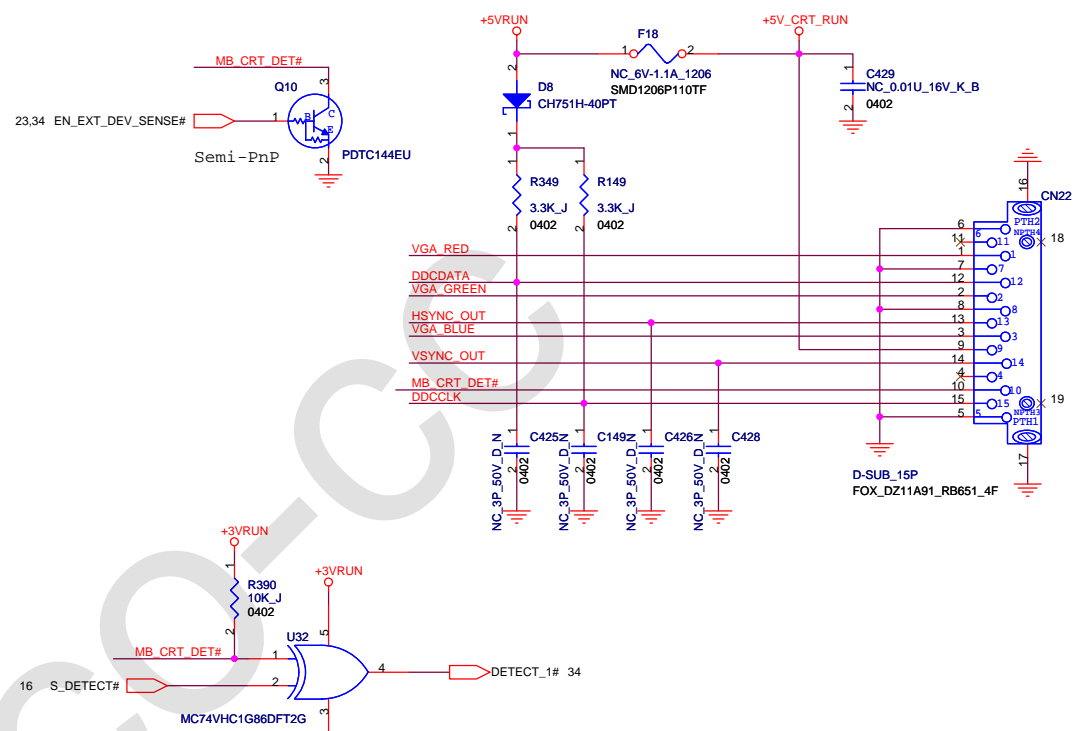
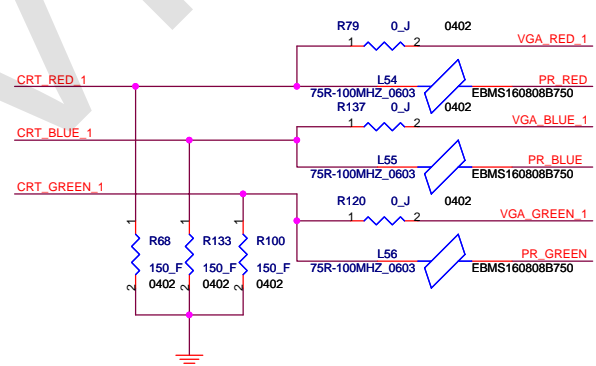
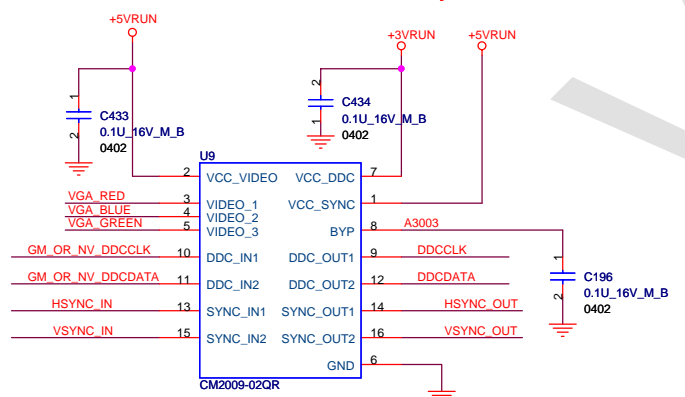
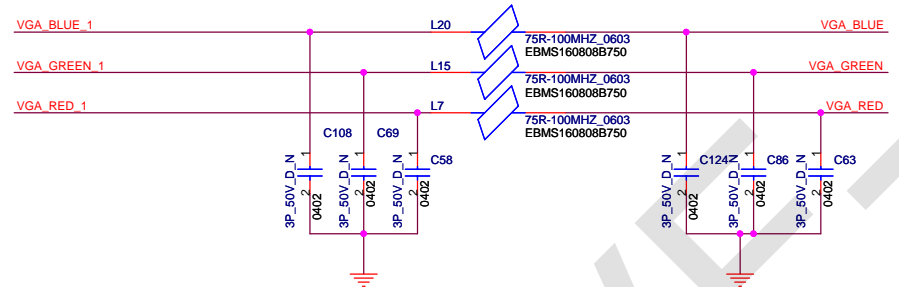
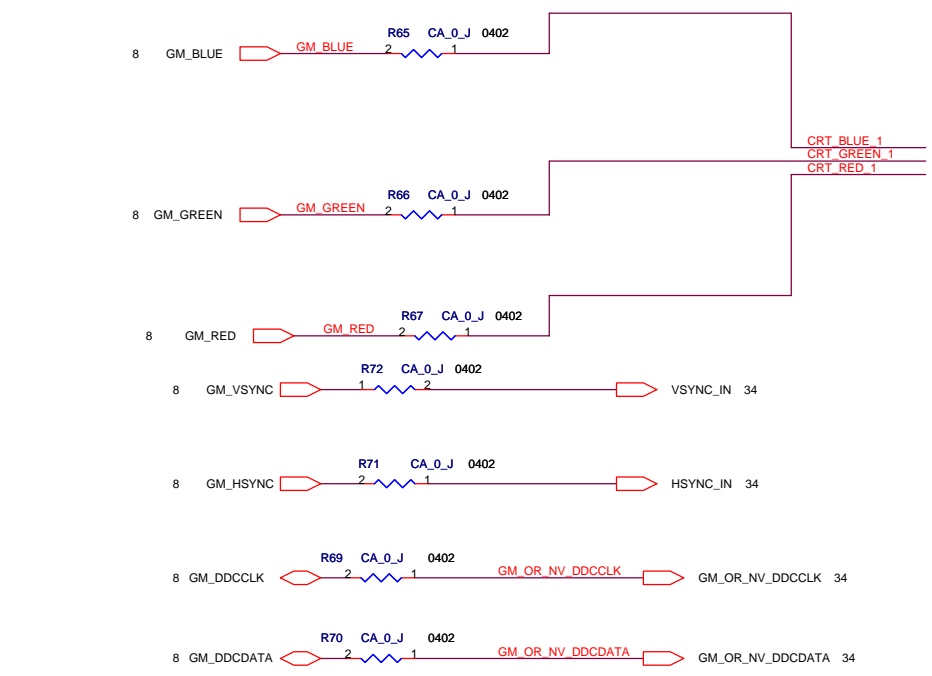
X A15
X J19

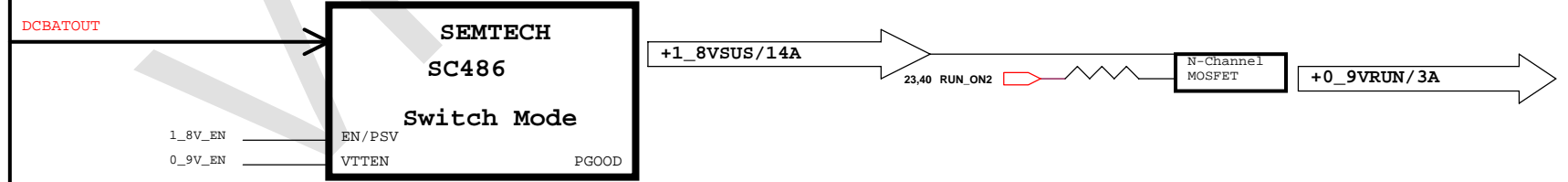
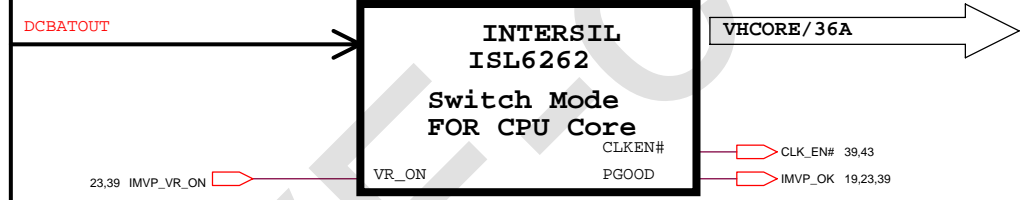
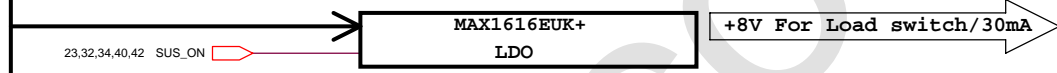
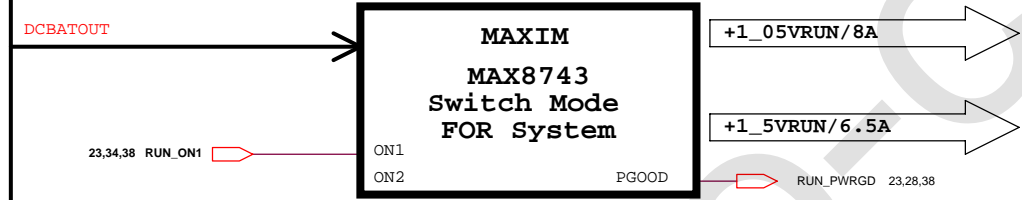
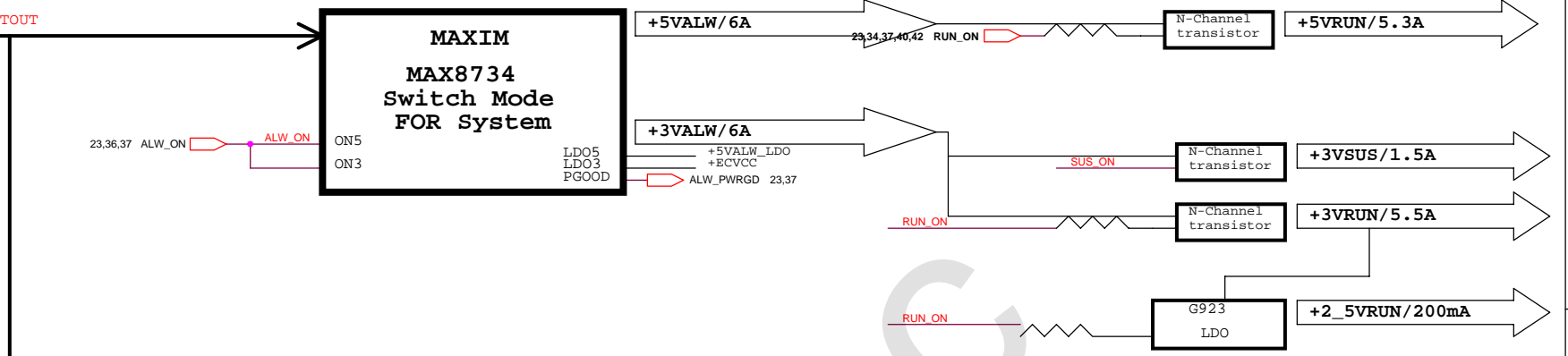
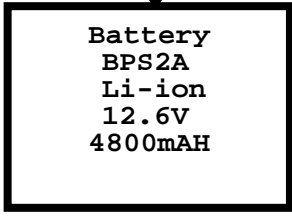
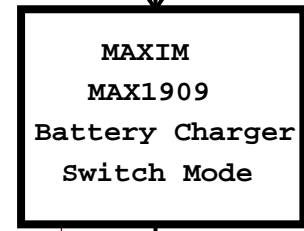
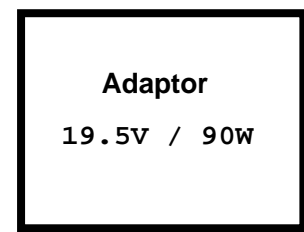
X U12
X V12
X W12
X E5

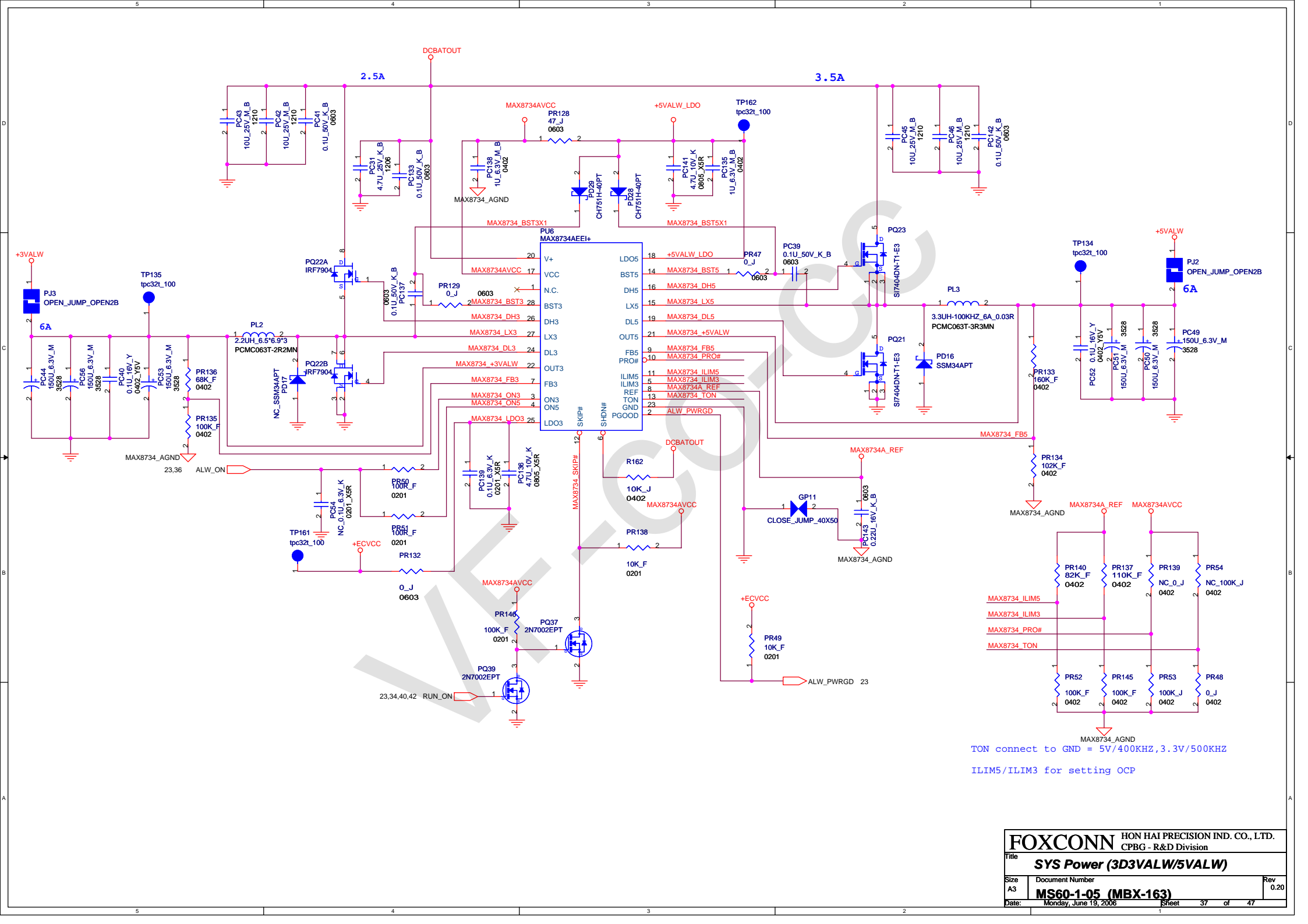
- RSVD2
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- RSVD198
- RSVD199
- RSVD200

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- E19
- G15
- F19
- G18
- H15
- H17
- H19
- F18
- F17
- G19
- H14
- E18
- K15
- L15
- J15
- H18
- E17
- A16
- E14
- B15
- B14
- A14
- C13
- B13
- L18
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- N17
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- M18
- M15
- N18
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- A13
- B11
- N15
- C14
- B9
- C3
- A9
- C4



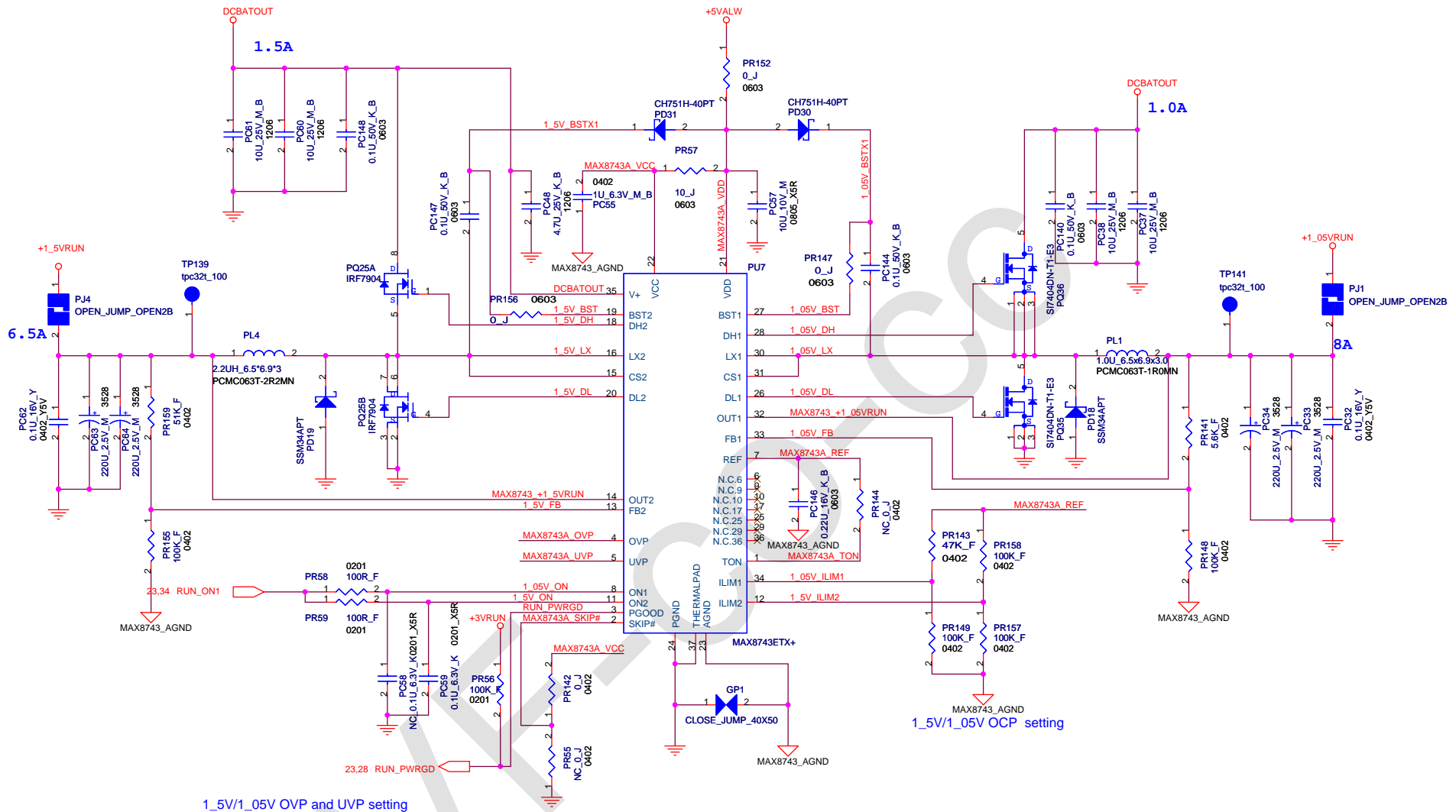




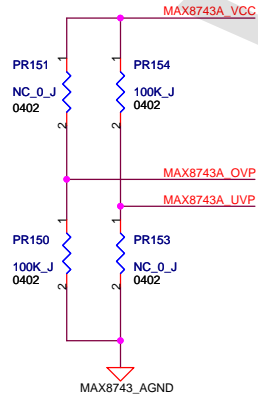


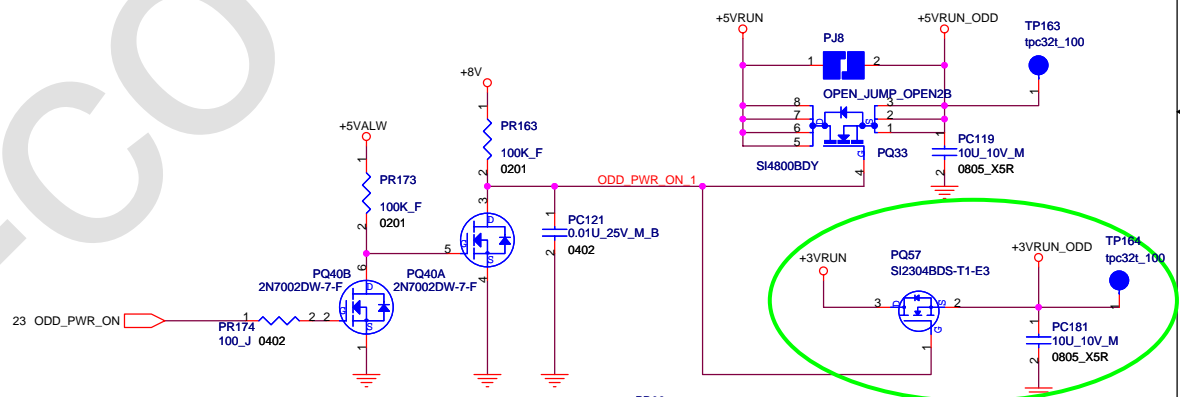
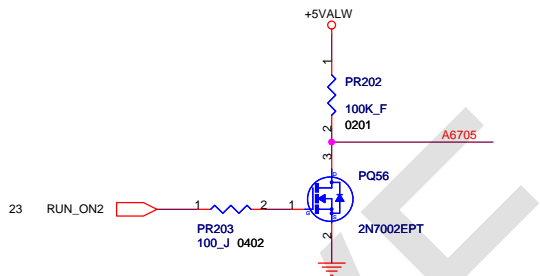
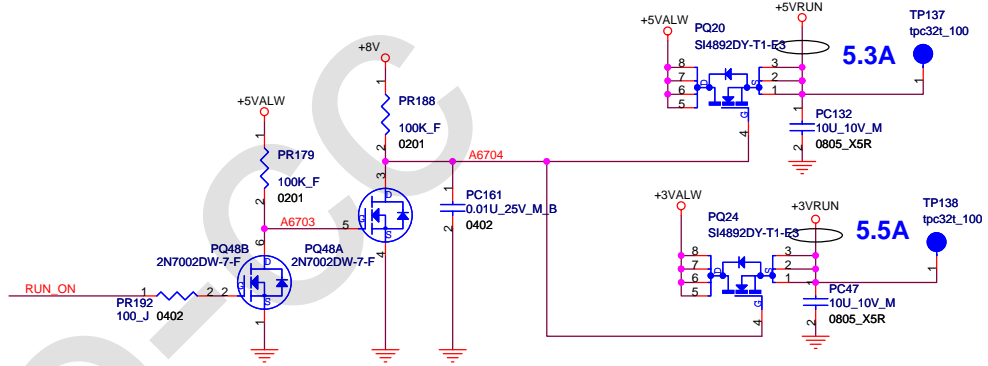
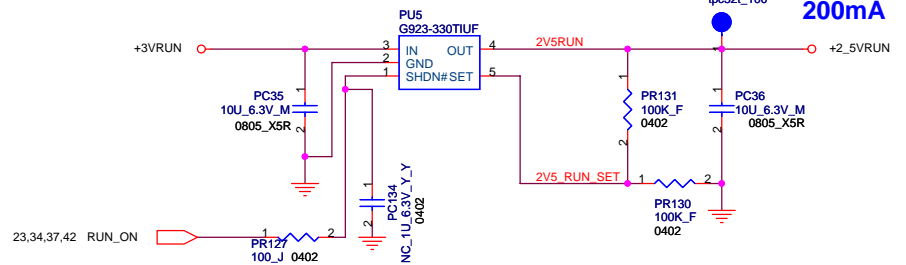
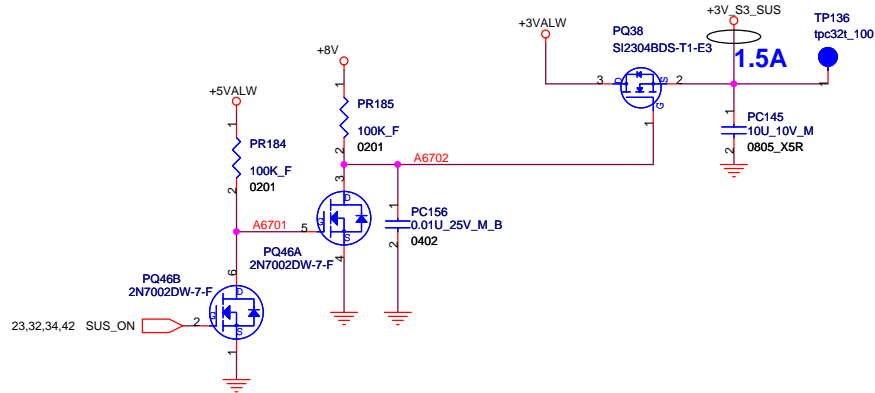
TON connect to GND = 5V/400KHZ, 3.3V/500KHZ
 ILIM5/ILIM3 for setting OCP

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title SYS Power (3D3VALW/5VALW)		
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 37	of 47

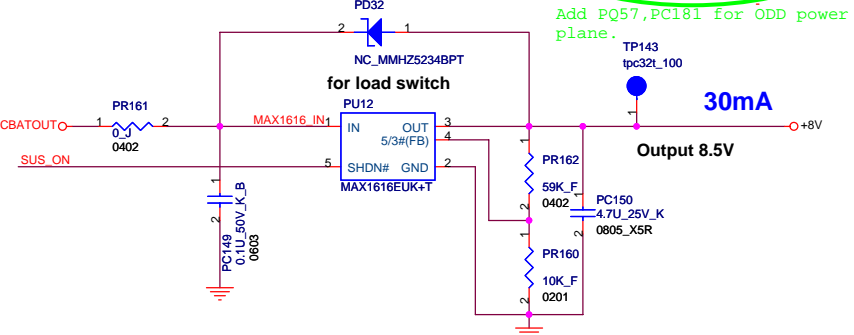
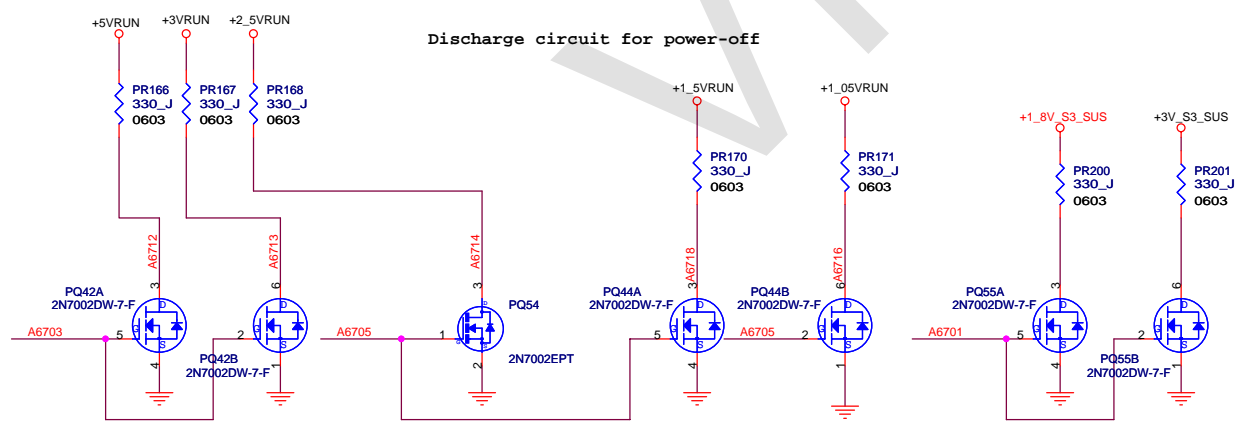


1.5V/1.05V OVP and UVP setting

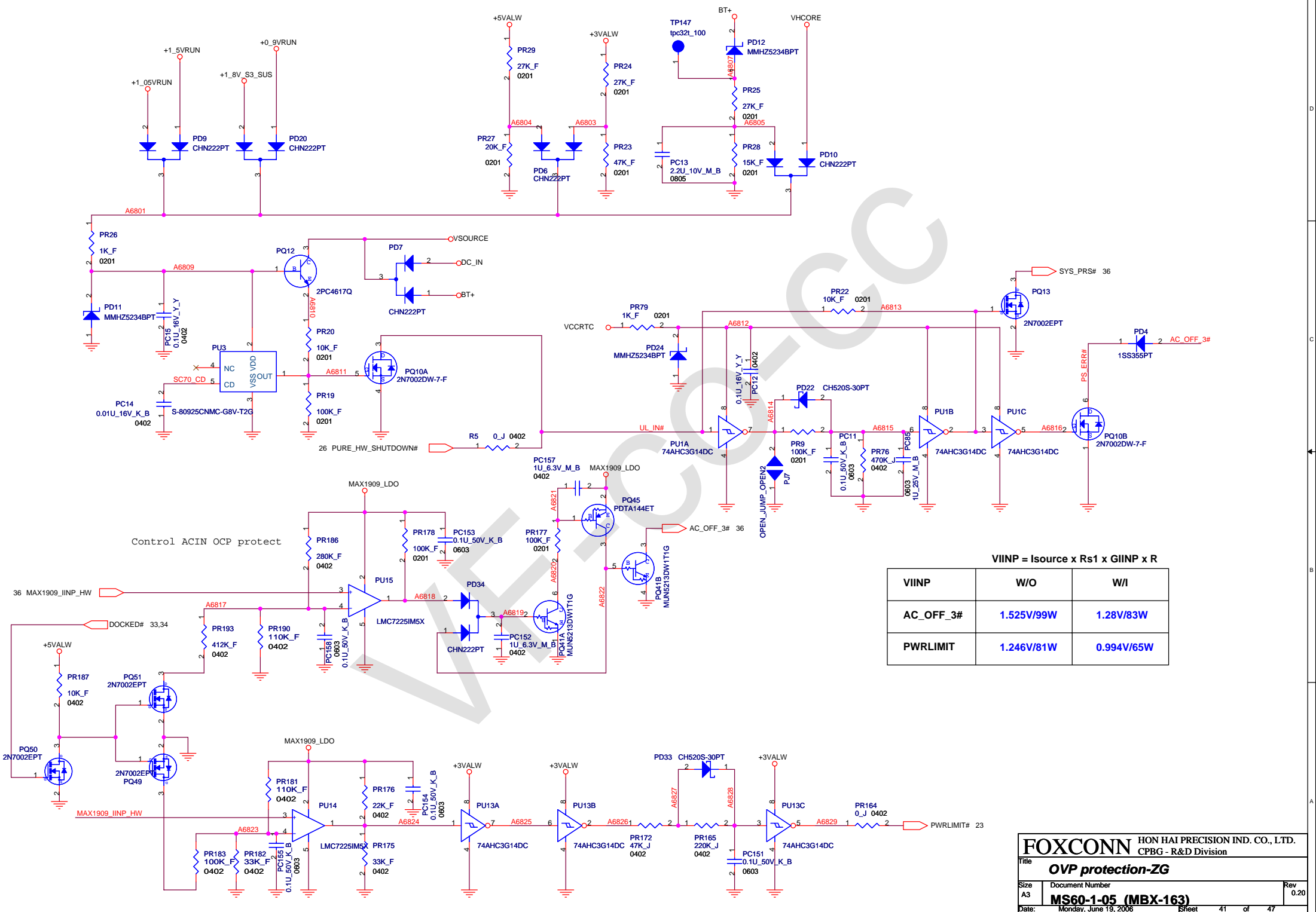




Discharge circuit for power-off



Add PQ57, PC181 for ODD power plane.



Control ACIN OCP protect

$$VIINP = I_{source} \times R_{s1} \times GIINP \times R$$

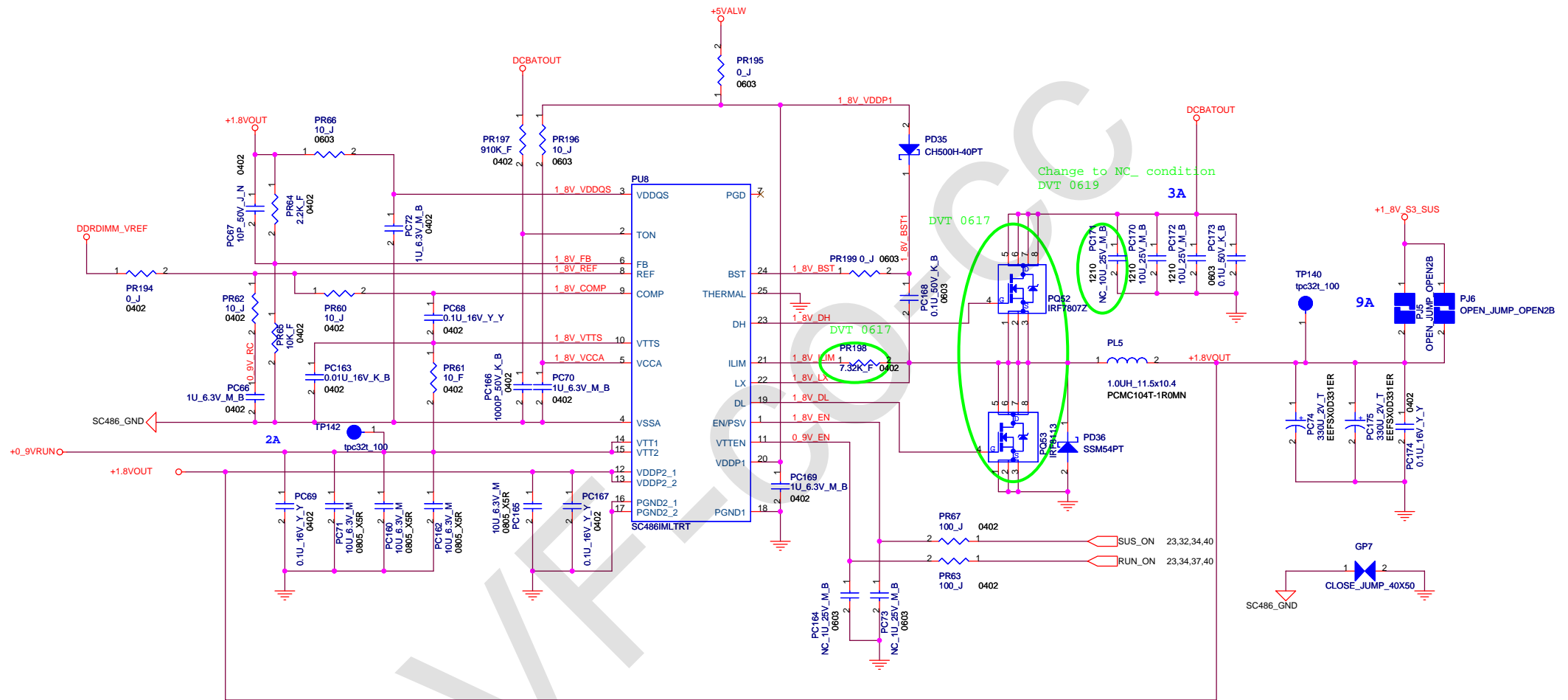
VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.246V/81W	0.994V/65W

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **OVP protection-ZG**

Size A3 Document Number: **MS60-1-05 (MBX-163)** Rev 0.20

Date: Monday, June 19, 2006 Sheet 41 of 47



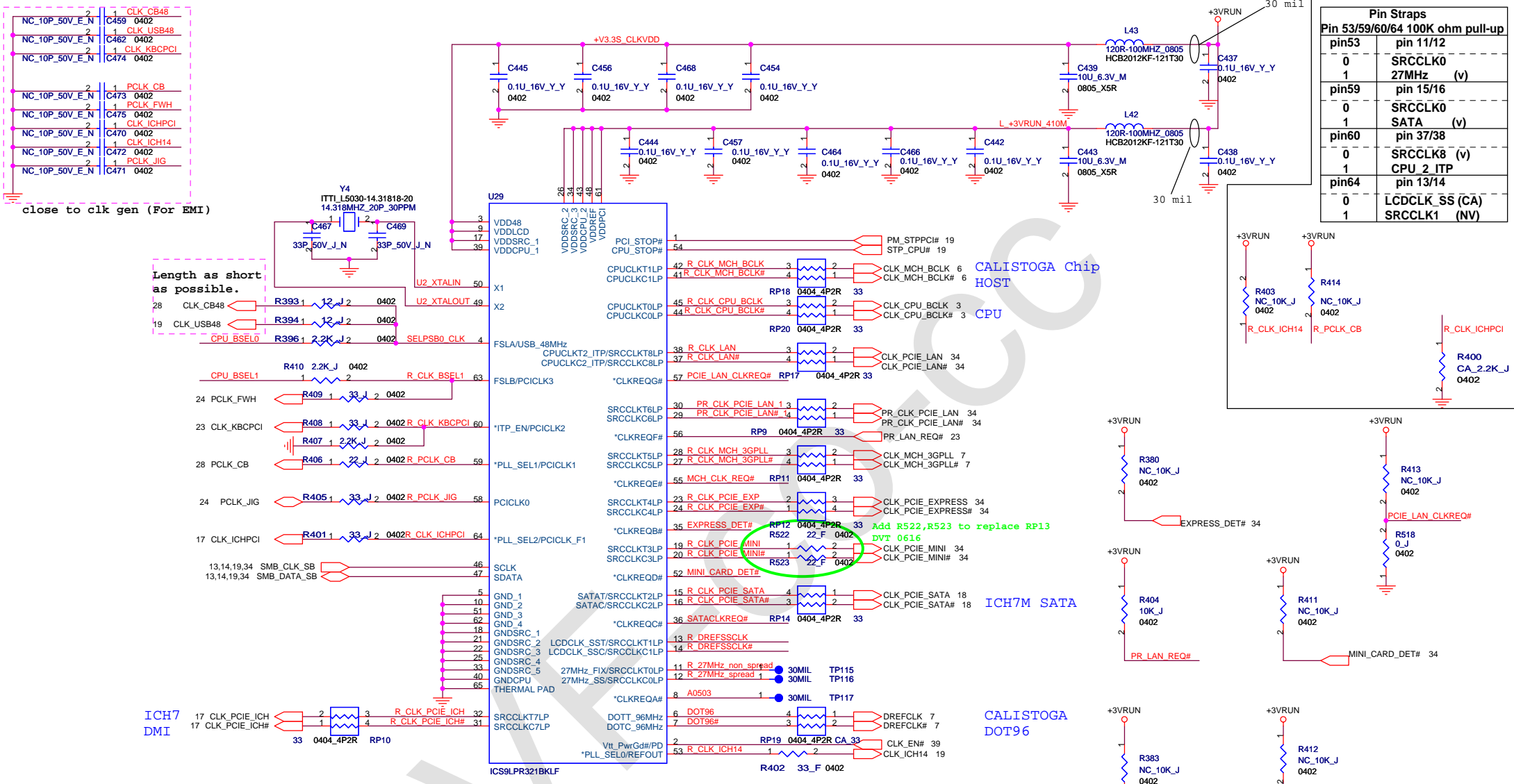
Change to NC_condition
DVT 0619

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title DDR2Power(+1.8V_S3_SUS/+0.9VRUN)		
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 42	of 47

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	PCLK_ICHPCI
NC_10P_50V_E_N	2	1	PCLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG

close to clk gen (For EMI)

Length as short as possible.



Pin Straps			
pin53	pin 11/12	pin59	pin 15/16
0	SRCLK0	0	SRCLK0
1	27MHz (v)	1	SATA (v)
pin60	pin 37/38	0	SRCLK8 (v)
0	SRCLK8 (v)	1	CPU 2 ITP
1	CPU 2 ITP	pin64	pin 13/14
0	LDCCLK_SS (CA)	0	SRCLK1 (NV)
1	SRCLK1 (NV)		

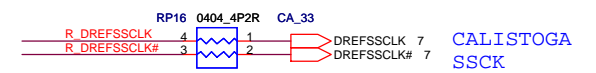
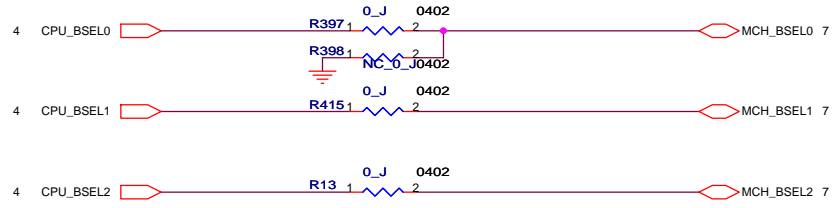
ICH7 DMI

SM bus Address : 1101001 (ICH7)
For clock generator

CLKREQ with internal pull-up resistor
No. Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
if EVT ok, del them in DVT

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

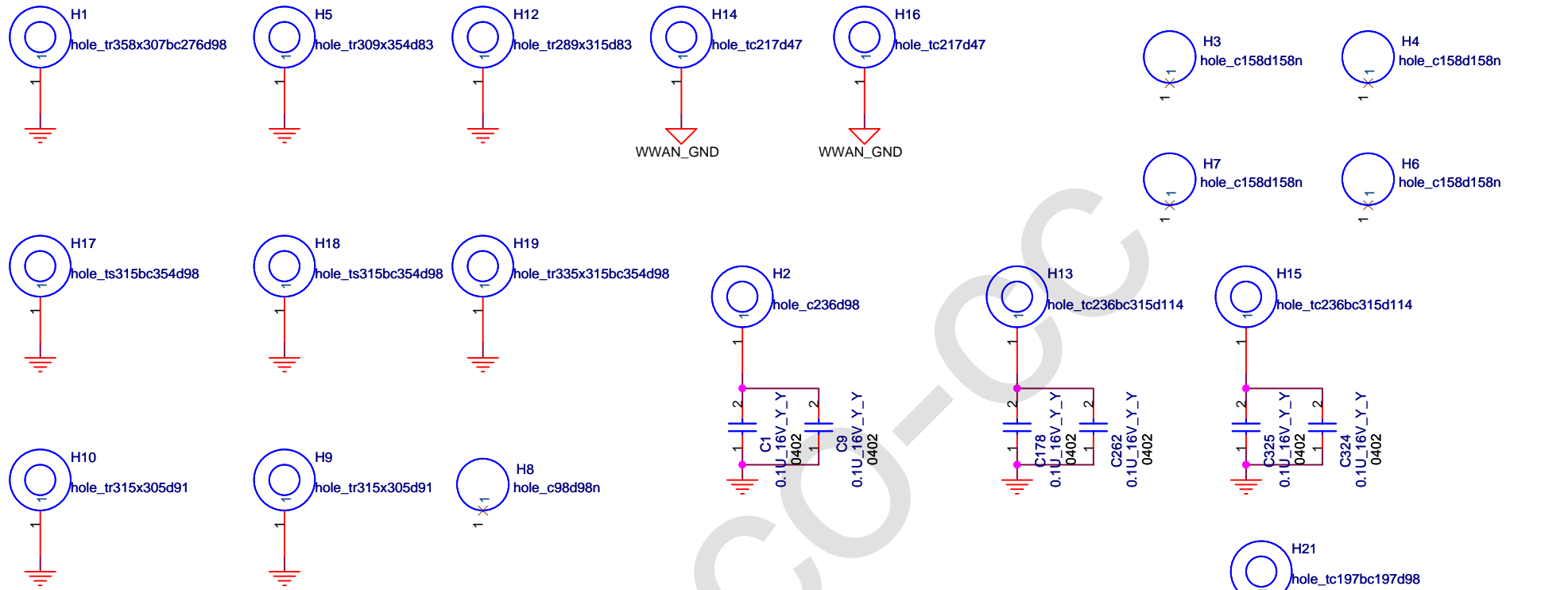


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

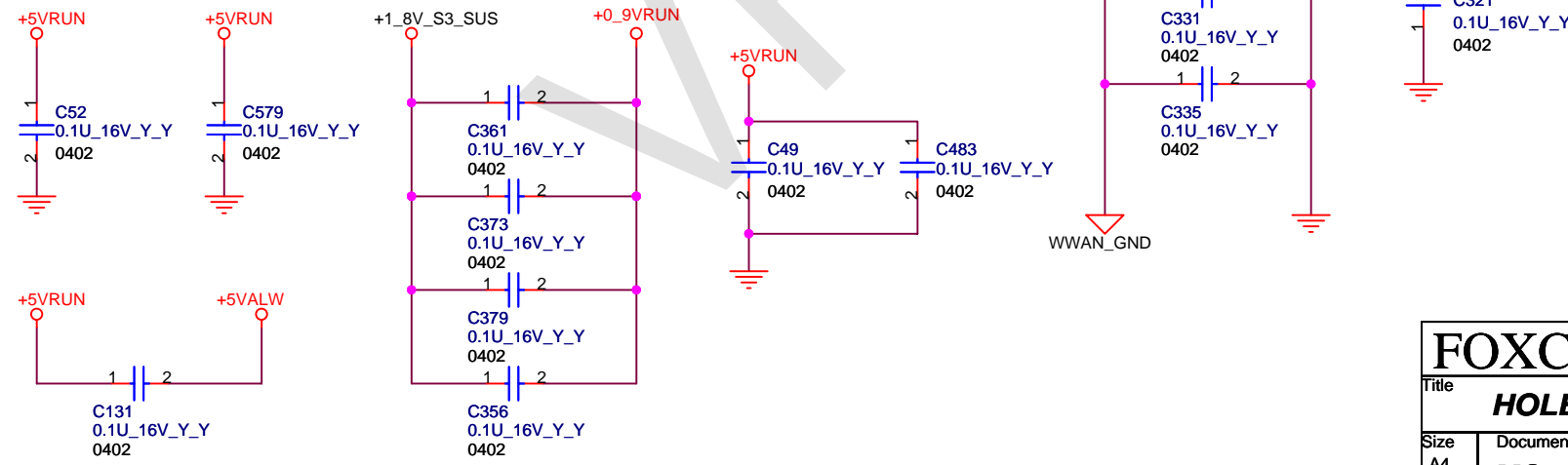
Title: **CLOCK GEN**

Size A3 Document Number: **MS60-1-05 (MBX-163)** Rev 0.20

Date: Monday, June 19, 2006 Sheet 43 of 47



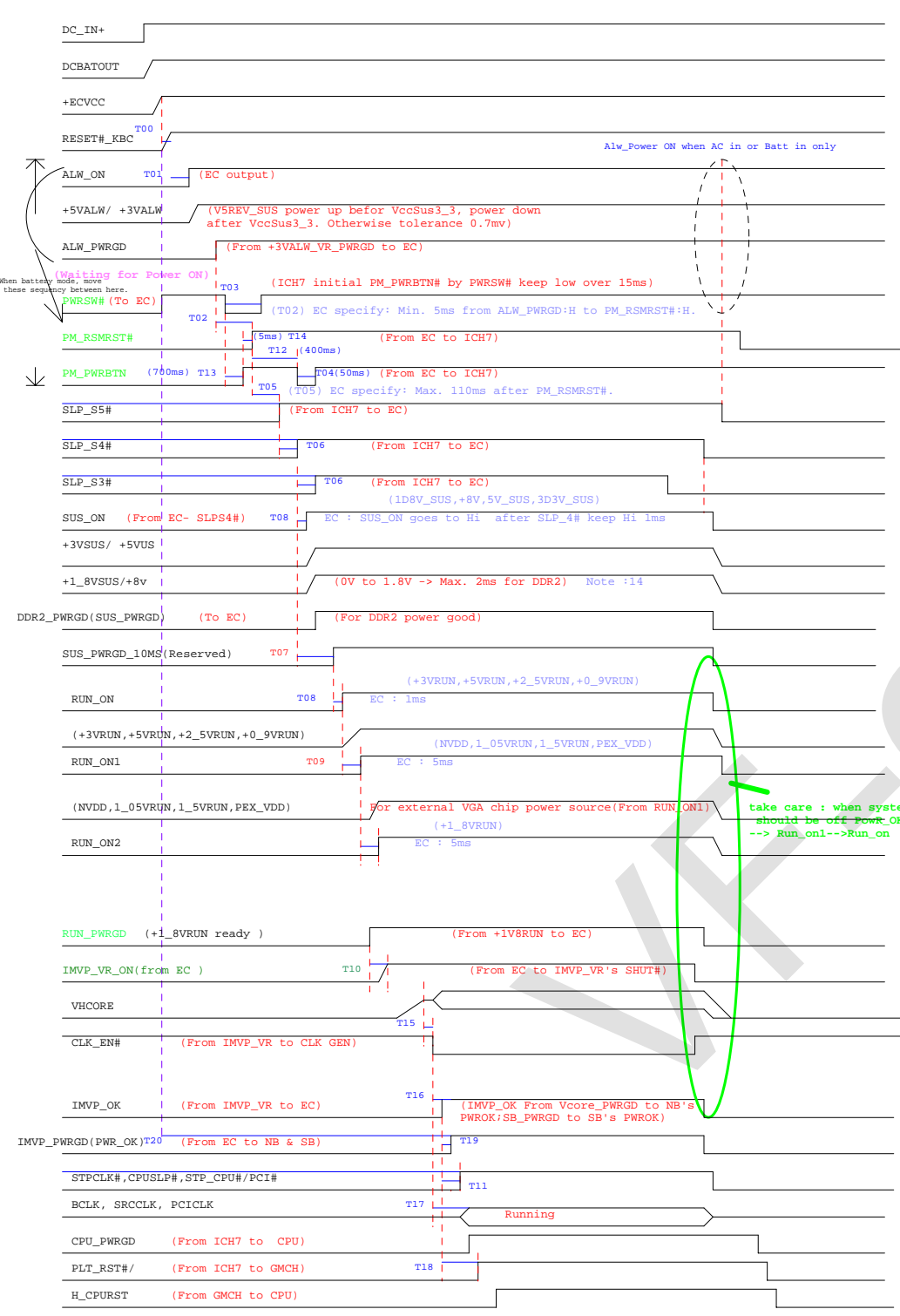
FOR EMI



FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title HOLE		
Size A4	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 44	of 47

MS60 Power On Sequence Timing

Version : 0.0
Modified date : 2/14/2006



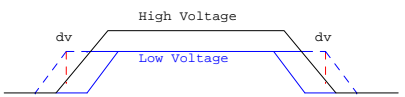
NOTE : (EC KB3910 Min. response time is 1ms)

- T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
- T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, We measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
- T02 : ALM_PWRGD#;H to PM_RSMRST#;H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
- T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing)
- T06(Please reference Intel 16971 Page 301 of t234 timing)
- T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
- T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
- T09 : For MS01 current SPEC
- T10 :Please refer to Intel 16971 Page 300 of t214 timing
- T11 :Please refer to Intel 16971 Page 303 of t216 timing
- T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms+Please reference Intel 16971 Page 301of t232 timing)
- T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
- In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
- T15 : Please refer to MAX8771 datasheet
- T16: Please refer to MAX8771 datasheet
- T17 : Please refer to Intel CK410(14690) page 53
- T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

take care : when system off , the sequence should be off Power OK ,then Run_on2 --> Run_on1-->Run_on

Remark : (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV) SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
- +3.3VRUN -> +2_5VRUN, dt:0.3mV
- +3_3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV



R/C delay (47K/0.1uF)

T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns-2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Min. 110ms	1 - 2 RTCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	

<1>2006/3/28 remove U36.SW no need to program for present application.

<2>2006/3/28 Change PR5 from 13K to common parts 10KOhm.

<3>2006/3/29 Change USB CONN. CN16 & CN40 for ID requirement.
P/N : FOX_UB11193-C1301-4F

<4>2006/3/29 Change ODD CONN. CN21 for ID requirement.
P/N : FOXCONN_QT8H0506_64T2R_4F

<5>2006/3/29 Change PC359,PC360 to 10uF
P/N : 1C-2B70106-M100

<6>2006/3/29 update new HDD CONN CN24.
P/N : 2N-0022002-F0G0

<7>2006/3/29 update new DC-IN CONN PCN1.
P/N : FOX_GS53020-00580-7F

<8>2006/3/29 update new BTY CONN PCN2.
P/N : FOXCONN_BP34063_B6012_7F

<9>2006/3/30 U18.U19.U21.R277.R300.R315change to NC according to Customer's feedback.

<10>2006/3/30 R269,R273,R276,R286,R287,R300 change to Populate according to Customer's feedback.

<11>2006/3/30 New add INV_ENABLE_EC logic dur to BIOS Code merge issue.add new component :
U53.U54 P/N : 14-74AHC1G-0800
R762 P/N : 1R-0000103-J200
R763 P/N : 1R-0000000-J200
R764 P/N : 1R-0000104-J200
Delete R176.R177

<12>2006/3/31 Add C20,C21,C22,C31,C33,C68 for EMI slution.
P/N : 1C-2Y20104-Y000

<13>2006/3/31 Add R5 for Customer feedback.
P/N : 1R-0000000-J200

<14>2006/3/31 Dummy R482,R483 for Customer feedback.

<15>2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component :
U55.U56 P/N : 15-RT9702A-0000
C521.C522 P/N : 1C-2Y20104-Y000
R569.R573 P/N : 1R-0000105-J200
C870.C871 P/N : 1C-2Y30225-Y000
C535.C751 P/N : 1C-2B70106-M100
Deleted Component :
Q12.Q13.Q20.Q21.C535.C527.C521.C751.C753.C752.R486.R476.R568.R569

<16>2006/3/31 CN2 Pin11 change to +3V_S3_SUS for Customer feedback.

<17>2006/4/3 CN20.CN32.CN33 Pin assignment modified due to Customer's concern.

<18>2006/4/3 CN31.CN32.CN33 CN34 Connector change.
P/N : GB11261_1051_7F

<19>2006/4/3 L17 & L19 updated according to Customer feedback
P/N : 1L-DCS0603-1000

<20>2006/4/4 Add PWR_MIZER circuit.
U6J GPIO10 with new signal "NV_PWR_MIZER"
new Components added and modified as below :
10K Ohm -- R130.R766 -- P/N : 1R-0000103-J200
7.5K Ohm -- R765.R767.R768.R769.R770 -- P/N : 1R-0000752-F200
4.3K Ohm -- R128 -- P/N : 1R-0000432-F200
2N7002EPT -- Q54.Q55.Q56.Q57.Q58 -- P/N : 17-2N7002E-PT00

<21>2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.

<22>2006/4/4 D6.D7.D8 change to Q59.Q60.Q61
P/N : 17-2N7002E-PT00

<23>2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate.
P/N : 1R-0000121-J200

<24>2006/4/4 new add Q62 for WLAN LED Logic
P/N : 17-2N7002E-PT00

<25>2006/4/4 NC F1 and C859 according to customer's feedback.

<26>2006/4/4 delete R482.R483 according to customer's feedback.

<27>2006/4/6 add H3 ~ H20

<28>2006/4/6 Update BTY Connector PCN2 for ME requirement.
P/N : 2N-0006001-MKX0

<29>2006/4/6 R278.R289.R270 change to 75Ohm and circuit modified as customer's feedback.
P/N : 1R-0000750-F200

<30>2006/4/6 R543 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-F300

<31>2006/4/6 R553 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-J200

<32>2006/4/6 R99.R94.R97.R109.R67.R64.R65.R75 change to NC as customer's feedback.
and R66.R69.R98.R101 change to 120Ohm.
P/N : 1R-0000121-J200

<33>2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.

<34>2006/4/6 CN31 Pin1.2 change to +3V_S3_SUS as customer's feedback.

<35>2006/4/6 add 1A Fuse F4.F5.F9.F11.F15.F17.F18.F19
P/N : 1M-F32V1A0-F000

<36>2006/4/6 add 0.5A Fuse F2.F3.F6.F7.F8.F10.F12.F13.F14.F16.F18
P/N : 1M-F32V0A5-F000

<37>2006/4/6 add C872 according to MS20 lesson learn.
P/N : 1C-2B20102-M000

<38>2006/4/6 CN34 Pin23.24 change to +3VRUN.

<39>2006/4/6 add C71.C74.C87 for EMI.
P/N : 1C-2Y20104-Y000

<40>2006/4/6 add C89.C188.C199.C208.C213.C214
P/N : 1C-2Y20104-Y000

<40>2006/4/7 add C215.C216.C217.C218.C219 for EMI solution.
P/N : 1C-2Y20104-Y000

<41>2006/4/7 R118.R119.R351 change to populate as customer's feedback.

<42>2006/4/7 Y1.C104.C107.C492.C497.C501.R433.R434.R427.R428.R429.R430.R132.
R133.R134.R136.R117 change to NC as customer's feedback.

<43>2006/4/7 R439.R443 change to 0 Ohm as customer's feedback.
P/N : 1R-0000000-J200

<44>2006/4/7 update Net name EN_EXT_DEV_SENSE# as customer's feedback.

<45>2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component :
PQ183 P/N : 17-2N7002D-W000
PR115 P/N : 1R-0000101-J200
PR103,PR114 P/N : 1R-0000104-F100
PC87 P/N : 1C-2B20103-M000
PQ38 P/N : 17-S14800B-DY00
PC76 P/N : 1C-2B70106-M200

<46>2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component :
PR273 P/N : 1R-0000103-F200
PR773 P/N : 1R-0004992-F200
PQ20 P/N : 17-2N7002E-PT00
PR774 P/N : 1R-0000102-J200
PC873 P/N : 1C-2Y20105-Y000

<47>2006/4/10 add H21-H24.

<48>2006/4/10 Rename Schematic Part referene.
new version since 4/11

<49>2006/4/11 change R68.R133.R100
P/N : 1R-0000151-F200

<50>2006/4/11 PR111.PR114 change to NC according to PWR team's suggestion in EVT.

<51>2006/4/11 Modify ODD reset circuit as customer's feedback.
Add U37 P/N : 15-MAX809S-0000
Add R516 P/N : 1R-0000104-J200
NC R305

<52>2006/4/11 Remove C257 for EMI comment.

<53>2006/4/11 add ODD Reset RC.
Add R517 P/N : 1R-0000103-J200
Add C580 P/N : 1C-2Y20104-Y000

<54>2006/4/14 change R197.R198.R199.R200 to 60.4Ohm
P/N : 1R-000604X-F200

<55>2006/4/14 add R518 for 0Ohm
P/N : 1R-0000000-J200

<56>2006/4/14 CN7.C409.C412.L37.F16.R44.R45 change to CA from NV to fit configuration.

<57>2006/4/27 PR111.PR114 change to Populate from NC according to PWR team's suggestion in EVT.
P/N : 1R-0000100-J200

MS60-L change list base on MS60-H

<58>2006/5/02 Del all NV_ components for L-model only.

<59>2006/5/03 Remove +1_8VRUN discharge circuit.Delete PR169,PQ44. Add PQ54 P/N:17-2N7002E-PT00

<60>2006/5/03 LED2 pin2,pin3 swap for Power LED color opposite issue

<61>2006/5/03 Change CAP93,CAP94 to NEC,TEPSGV0E337M9-12R,330uF,2.5V
P/N:1C-31T0337-MX00
Add CAP95 P/N:1C-31T0337-MX00

<62>2006/5/04 F1,F2,F3,F4,F5,F6,F7,F8,F9,F10,F11,F12,F13,F14,F15,F16,F17,F19 change to fuse,1.1A PTC type
P/N:1M-F06V1A1-F000

<63>2006/5/05 follow M/E change to exchange PCN1 pin1 & pin2 connection.Layout change placement form top side to bottom side.

<64>2006/5/05 Add GP14,GP15 open jump for repair conveniently

<65>2006/5/05 Add C581,C582,C583,C584,C585,C586,C587,C588,C589,C590,C591,C592 for 22uF_0805_6.3V shortage.

<66>2006/5/08 As to M/E assemble issue, we will need rotat 180degree about T/P module.So that R47 change to stuff

<67>2006/05/09 Rename CAP93,CAP94,CAP95 to PC93,PC94,PC176.And change component to Panasonic,EEFSX0D331ER,330uF,2V
P/N:1C-42T0337-MX00

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<68>2006/05/09 PC54,PC58,PC59,PC139 change to X5R,0.1uF,6.3V,10%,0201 for X7R,0.1uF,10V,0201 shortage
P/N:1C-2B10104-K100

<69>2006/05/11 L33,L34 pin swap .D12 & D10 change to TOP side for layout conveniently

<70>2006/05/12 PR198 change to 5.6k/0402_1% to modify 1.8V OCP seting value.
P/N:1R-0000562-F200

<71>2006/05/12 CN23 change to 'FOX_MH11747-BR2D-4F' for ME requirement.
P/N:2N-000400N-FK00

<72>2006/05/12 CN3,CN8 change to 'FOX_GB5RF120-1200-7F' for ME requirement.
P/N:1N-0012001-F0T0

<73>2006/05/12 CN7 change to 'FFOXCONN_GB5RF060_1200_7F' for ME requirement.
P/N:1N-0006000-F0T0

<74>2006/05/12 CN12,CN16 change to 'FOXCONN_UB11193_C1304_4F' for ME requirement.
P/N:1N-0004000-FEG0

<75>2006/05/12 CN9 change to 'FOXCONN_HS8206E' for ME requirement.
P/N:1N-0006001-M1T0

<76>2006/05/16 Due to ripple noise issue.PC74,PC175 change to 'Panasonic,EEFSX0D331ER'
.Del PC75 for power requirement.
P/N:1C-42T0337-MX00

<77>2006/05/17 Add PQ55,PQ56,PR200,PR201,PR202,PR203 for power discharge.
P/N:17-2N7002D-W000
P/N:1R-0000331-J300
P/N:1R-0000104-F100
P/N:1R-0000101-J200

<78>2006/05/17 U24 change to 'FOXCONN_P24782A_2743_01' for ME requirement.
P/N:1N-1478002-0000

<79>2006/05/18 PC67 change to 10pF 0402,and need to mount for power requirement.
P/N:1C-2N20100-J000

<80>2006/05/18 CN12,CN16 change footprint to 'FOXCONN_UB11193_C1304_4F_HM' for DFM.

<81>2006/05/18 Add R519,R520,C593,C594 on 'IAC_BITCLK' signal for EMI requirement.
P/N:1R-0000000-J200
P/N:1C-2N20330-J000

<82>2006/05/18 H13,H15 footprint change to ' hole_tc236bc315d114' for ME requirement.
P/N:1X-HOLE000-0232

<83>2006/05/19 CN25 need change to P/N:1N-1200007-0000. CN26 need change to P/N:1N-1200008-0000. Because P/N:1N-120000C-0000 & P/N:1N-120000D-0000 part number are not available.

<84>2006/05/19 Add PC177,PC178,PC179,PC180 on DC_IN trace for EMI requirement.
P/N:1C-2B30104-K000

<85>2006/05/22 Del R89,R140,R127.Add L54,L55,L56 (0 ohm change to bead) for EMI requirement.
P/N:1L-BEBMS16-0801

<86>2006/05/30 change R517 from 10Kohm to 0ohm for solving the ODD issue.
P/N:1R-0000000-J200

DVT change list

<87>2006/06/15 Delete R264.R271 for Debug BD LED.

<88>2006/06/15 Del reset IC form ODD portion.Del R516,R517,C580. Change U37 to 74AHC1G08GW and connect GPIO_ODD_RST# form KBC for ODD reset.

<89>2006/06/15 Add R521 1k ohm and change R244 connection form 'ALW_ON' to 'ALW_ON_1' for customer's requirement.
P/N : 1R-0000102-J200

<90>2006/06/16 PORT_DET# change from EC's pin81 to EC's pin176 for noise decreasing.

<91>2006/6/16 remove RP13 and replace with R519/R520 for WLAN issue improving.
P/N : 1R-0000220-F200

<92>2006/6/16 Add one GPIO signal 'VISTA_SUPPORT#' that is connected form EC's pin99 to CN1's pin17 to support Vista OS.

<93>2006/6/16 Add PQ57,PC181 for ODD power plane.
P/N:17-S12304B-DS00
P/N:1C-2B70106-M200

<94>2006/6/16 (HDD connector)CN21's pin18 change connection from NC to GND for the starting timing improvement.

<95>2006/6/17 Change PQ52 from SI7392DP to IRF807Z and change PQ53 from SI7336ADP to IRF8113 for power requirement.
P/N:17-1RF7807-2000
P/N:17-1RF8113-0000

<96>2006/6/17 PR198 change from 5.6K ohm to 7.32K ohm to modify OCP setting value.
P/N:1R- 0007321-F200

<97>2006/6/17 U12 change from G961-18ADJEU to SC1565IS-2.5TRT for WWAN voltage drop improvement.
P/N:15-SC15651-0000

<98>2006/6/19 pc117,pc179,pc178,pc180,pc115,pc91 change to populate for EMI requirement.

<99>2006/6/19 Add C595 at PRT_IN power trace for EMI requirement.
P/N:1C-2B30104-K000

<100>2006/6/19 Add PC116,PC117,PC118,PC120,PC122,PC123,PC124 at DCBATOUT power trace for EMI requirement.
P/N:1C-2B30105-M000
P/N:1C-2B30104-K000

<101>2006/6/19 Add R303 10K pulldown at U34's pin1 to avoid start abnormally for customer's requirement.
P/N:1R-0000103-J200

<102>2006/6/19 PC171 change to NC_ condition for power requirement.

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