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46	SYSPWR(+3VALW/+5VALW)	1.0	06/10/2
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48	VHCORE(ISL6262)	1.0	06/10/2
49	Others power plan	1.0	06/10/2
50	OVP protection	1.0	06/10/2
51	VGAPWR(VGACORE(10)	1.0	06/10/2
52	DDR2PWR(+1 8V SUS/+0 9VTT	1.0	06/10/2
53	CHARGER(ISL6251)	1.0	06/10/2
54	HOLE	1.0	06/10/2
55	POWERBYPASS	1.0	06/10/2
56	FIDUCIAL	1.0	06/10/2

P. Leader	Check by	Design by
10/3		10/06

PCB P/N: 1P-0069700-8011 - Unimicro
1P-0069201-8011 - NANYA

Project Code & Schematics Subject: MS60 Main Board

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division

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51	VGAPWR(VGACORE&IO)	1.0	06/10/2
52	DDR2PWR(+1_8V_SUS/+0_9VRUN)	1.0	06/10/2
53	CLOCK GEN	1.0	06/10/2
54	HOLE	1.0	06/10/2
55	POWER SEQUENCE	1.0	06/10/2
56	History	1.0	06/10/2

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Project Code & Schematics Subject: MS60 Main Board

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

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MS60 (CALISTOGA PM/GM+Gfx Block Diagram)

CPU Processor
Yonah
Celeron-M
P.3~5

FSB
533/667 MHz

Clock Gen.
9LPR321BKLF
P.53

GDDR3 Video RAM
8Mx32bx2pcs
/16MX32bx2pcs
P.23~24

n-VIDIA
G72M
23x23 mm
P.16~22

PCIE X16

13.3"WXGA
P.25

LVDS

CRT Conn
P.42

CRT

S-Video Conn
P.25

TV OUT

North Bridge
Calistoga
945GM / PM
940 GML
P.6~12

533/667 MHz

SO-DIMM
533/667 MHz
DDRII RAM
P.13~15

TMDS

FUNCTION BD

HP JACK

Mic In Jack

Int. Speaker
1.5W/8ohm x 2

APA2068
Amplifier

ALC262
Audio Codec

INT Mic

MIC BD

To Docking

X4 DMI
(Direct Media Interface)

HD Audio

WWAN
P.34

USB

MS60_L ONLY

OIDE
P.36

PCI BUS

FUNCTION BD

Mini-CARD
WLAN 802.11a/b/g

PCIE X 1

EXPRESS CARD BD

Express Card

TPS2231
Power SW

PCIE X 1

USB2.0

USB 2.0
CONN.X2
P.41

MS_DUO/PRO
Slot
P.39

i-Link
1394
P.38

TI PCI8402
CardBus
CardReader
i.LINK
P.37~40

2.5" SATA
HDD
P.31

SATA

PATA ODD
P.31

IDE ATA

HD Audio

South Bridge
ICH7-M
P.26~30

LPC

ENE KB3910SFC1
EC+KBC
P.32

PS/2

Touch Pad
P.36

SMB Channel 2

BATT CONN
P.45

SMB Channel 1

Thermal Sensor
G781-1P8f
CPU & SYS
P.35

Thermal Sensor
G781P8f
(VGA&DDR So-DIMM)
P.21

EXPRESS CARD BD

Lid Switch

Pure H/W Thermal Shutdown
M6509
P.35

RJ11

MDC 1.5
Modem

FUNCTION BD

RJ45

NS681601P

Marvell 10/100
Ethernet
88E8036

PCIE X 1

USB2.0

From System

PCIE

CRT
7 Pin

DVI-D
14 Pin

HUB

PORT REPLICATOR
50 Pin + PWR + GLAN

USB

BT

EXPRESS CARD BD

XBUS

Flash BIOS
8Mbits
P.33

PWM

CPU FAN
P.35

PORT REPLICATOR

CRT

DVI-D

USB*3

RJ45

SYSTEM DC/DC
MAX8734 P.46

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC
MAX8743 P.47

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SC486 P.52

DCBATOUT	+1_8V_S3_SUS +0_9VRUN

CPU DC/DC
ISL6262 P.48

INPUTS	OUTPUTS
DCBATOUT	VHCORE

AMP DC/DC
MAX1616 P.49

INPUTS	OUTPUTS
DCBATOUT	+8VRUN

SC411 P.51

INPUTS	OUTPUTS
DCBATOUT	NV_VDD

GMT966 P.51

+1_5VRUN	PEX_VDD

MAXIM CHARGER
MAX1909 P.45

INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

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Title: *Block Diagram (All)*

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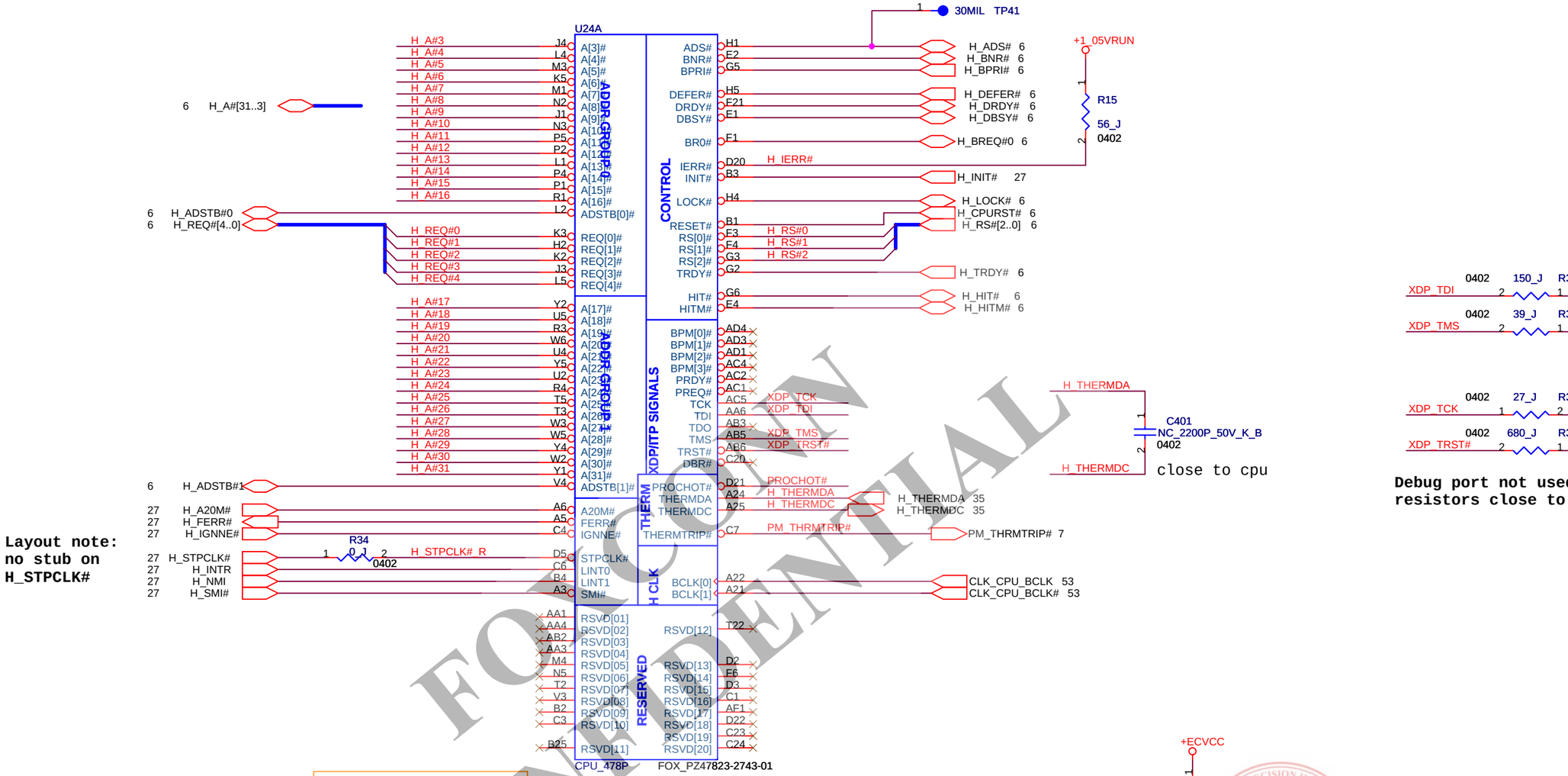

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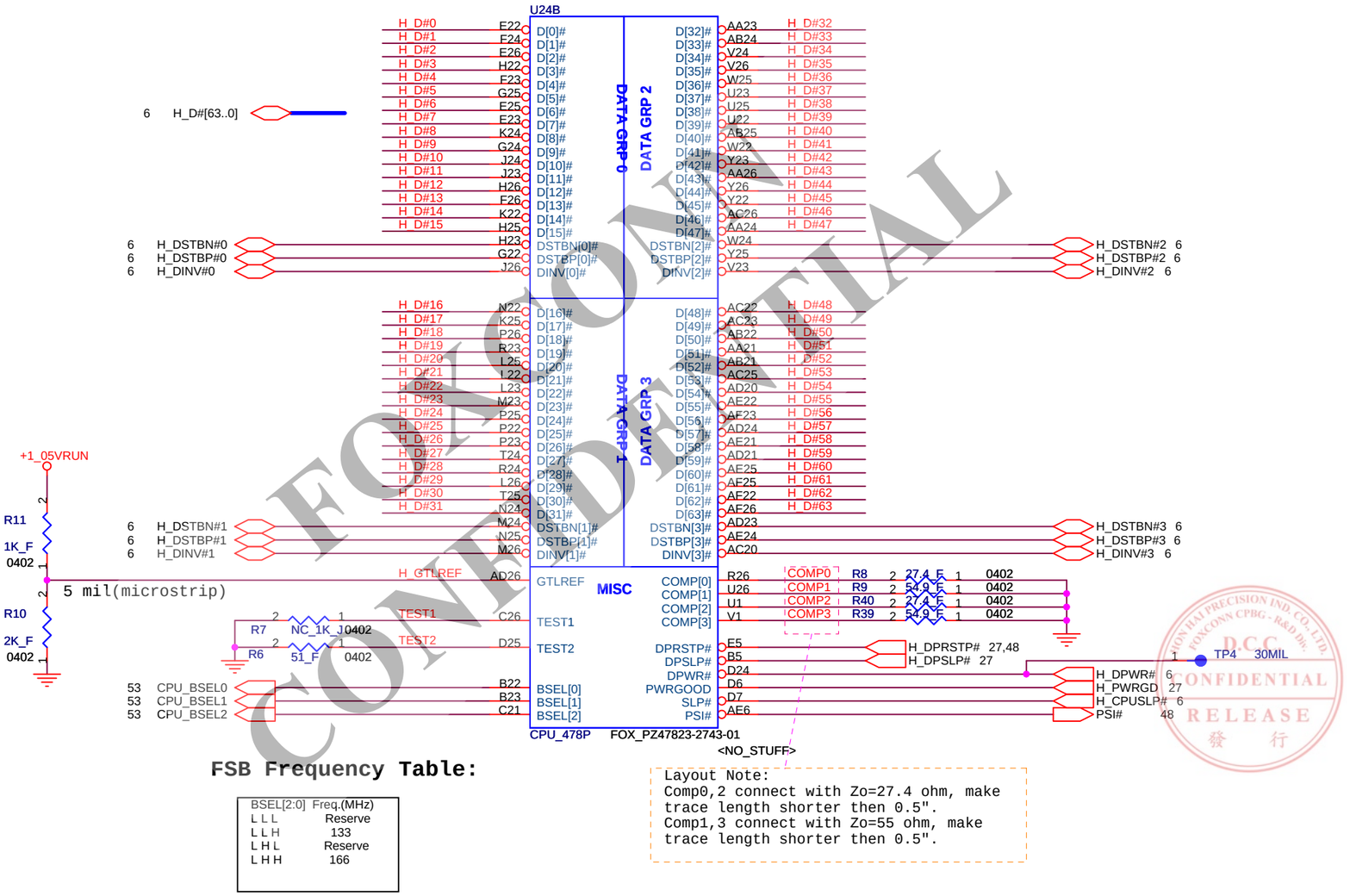

Place close to CPU

Layout Note:
Zo=55 ohm, 0.5" max for GTLREF.

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

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Title: *Yonah (HOST BUS) 2/3*

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CPU_VCCA---->130mA
CPU_VCCP----->2.5A
CPU_VCC------>36A

maximum current is 130mA for CPU_VCCA in Merom and 600A/us slew rate for CPU_VCCA

Same Length

Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.

width=18 mil
spacing=7 mil

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Title	*Yonah (POWER/GROUND) 3/3*		
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W/S = 10/20mil

H_XRCOMP
R361
24.9_F
0402

+1_05VRUN
R357
54.9_F
0402
H_XSCOMP

+1_05VRUN
R354
221_F
0402
W/S = 10/20mil
H_XSWING
R126
100_F
0402
C101
0.1U_16V_M_B
0402

W/S = 10/20mil
H_YRCOMP
R175
24.9_F
0402

+1_05VRUN
R164
54.9_F
0402
H_YSCOMP

+1_05VRUN
R166
221_F
0402
W/S = 10/20mil
H_YSWING
R167
100_F
0402
C229
0.1U_16V_M_B
0402

4 H_D#[63..0]

U27A

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	

H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
53 CLK_MCH_BCLK	AG2	H_CLKIN	
53 CLK_MCH_BCLK#	AG1	H_CLKIN#	

HOST

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	J12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	J14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	J15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	

H_A#[3..31] 3

H_ADS#	E8	H_ADS#	3
H_ADSTB#_0	B9	H_ADSTB#0	3
H_ADSTB#_1	C13	H_ADSTB#1	3
H_VREF_0	J13		
H_BNR#	C6	H_BNR#	3
H_BPRI#	F6	H_BPRI#	3
H_BREQ#0	C7	H_BREQ#0	3
H_CPURST#	B7	H_CPURST#	3
H_DBSY#	A7	H_DBSY#	3
H_DEFER#	C3	H_DEFER#	3
H_DPWR#	J9	H_DPWR#	4
H_DRDY#	H8	H_DRDY#	3
H_VREF_1	K13		

Place Cap. near GMCH within 100 mils.

+1_05VRUN
R159
100_F
0402
H_VREF 20 mil
C142
0.1U_16V_M_B
0402
R158
200_F
0402

H_DINV#_0	J7	H_DINV#0	
H_DINV#_1	W8	H_DINV#1	
H_DINV#_2	U3	H_DINV#2	
H_DINV#_3	AB10	H_DINV#3	

H_DINV#[3..0] 4

H_DSTBN#_0	K4	H_DSTBN#0	
H_DSTBN#_1	T7	H_DSTBN#1	
H_DSTBN#_2	Y5	H_DSTBN#2	
H_DSTBN#_3	AC4	H_DSTBN#3	

H_DSTBN#[3..0] 4

H_DSTBP#_0	K3	H_DSTBP#0	
H_DSTBP#_1	T6	H_DSTBP#1	
H_DSTBP#_2	AA5	H_DSTBP#2	
H_DSTBP#_3	AC5	H_DSTBP#3	

H_DSTBP#[3..0] 4

H_HIT#	D3	H_HIT#	3
H_HITM#	D4	H_HITM#	3
H_LOCK#	B3	H_LOCK#	3

H_REQ#_0	D8	H_REQ#0	
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	

H_REQ#[4..0] 3

H_RS#_0	B4	H_RS#0	
H_RS#_1	E6	H_RS#1	
H_RS#_2	D6	H_RS#2	

H_RS#[2..0] 3

H_SLPCPU#	E3	H_CPUSLP#	
H_TRDY#	E7		

H_CPUSLP#	4		
H_TRDY#	3		

CALISTOGA

GM	QG88CGM	12-0G88CGM-0000
PM	QG88CPM	12-0G88CPM-0000
GML	940GML-QK60-A3	12-940GML0-A300

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: CALISTOHA (HOST)

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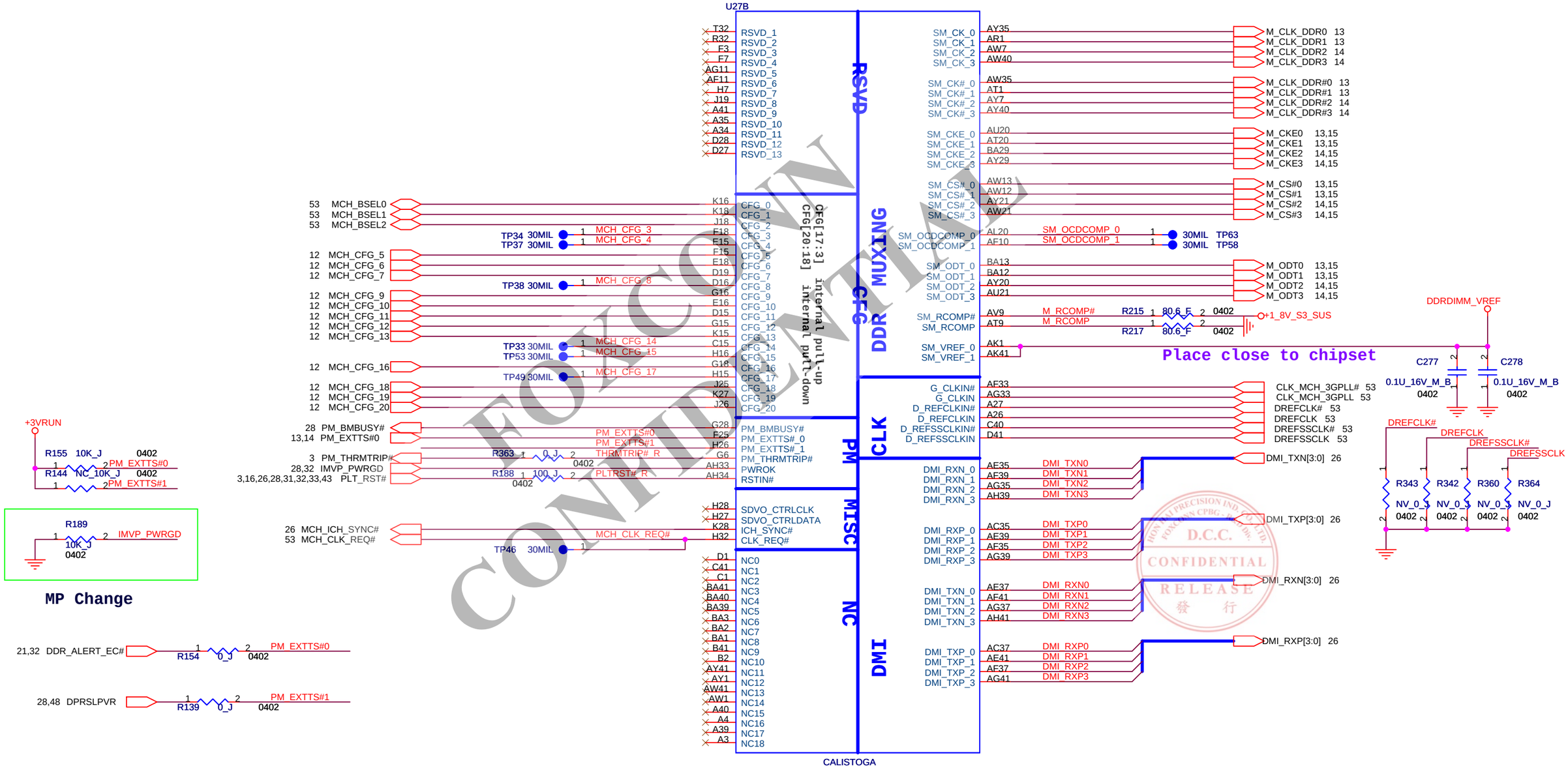
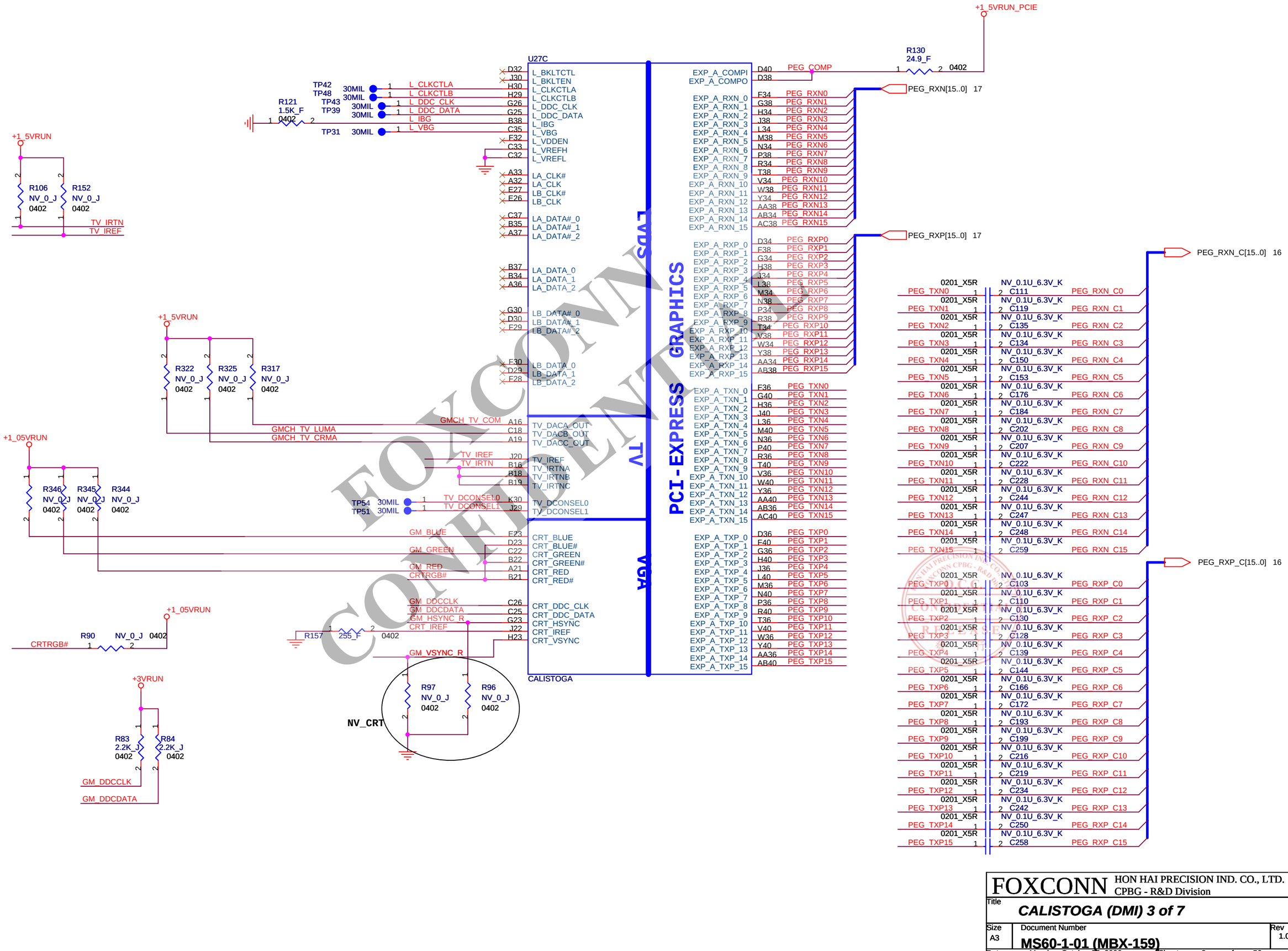
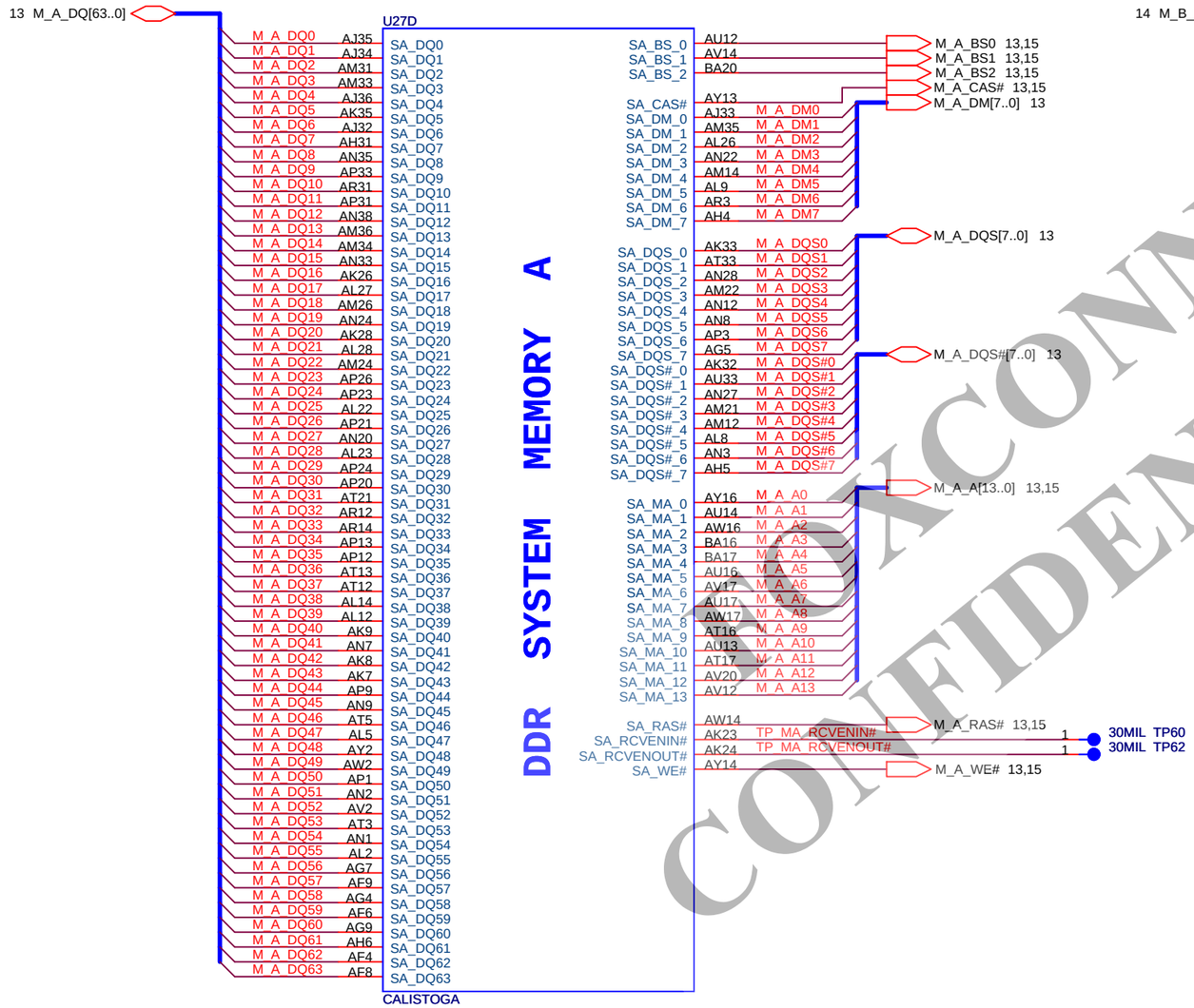
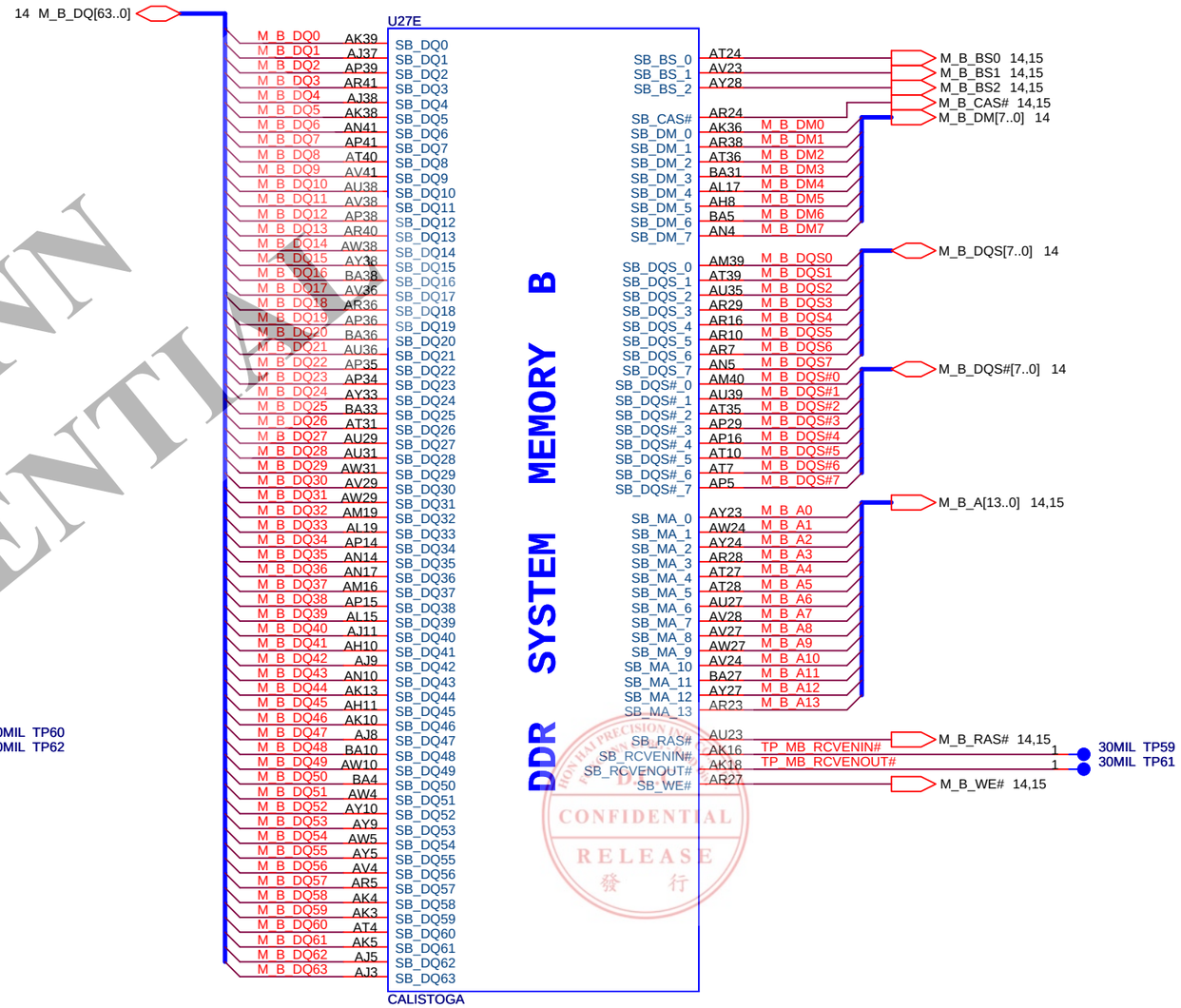


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOGA (DMI) 2 of 7	
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 1.0
Date: Monday, October 02, 2006	Sheet 7 of 56	

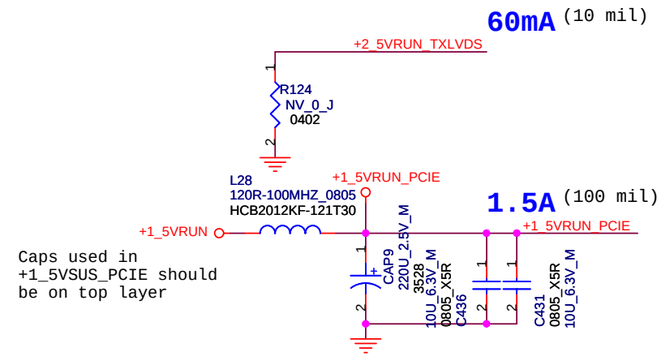


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOGA (DMI) 3 of 7	
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 1.0
Date: Monday, October 02, 2006	Sheet 8 of 56	

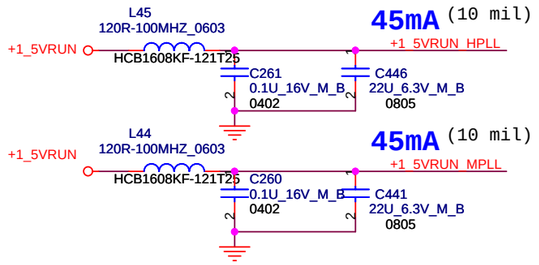


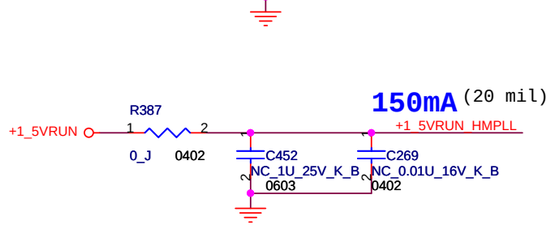


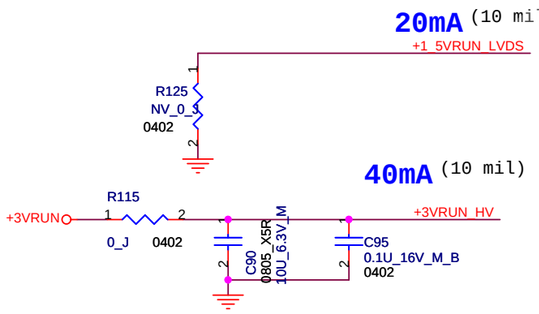
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOGA (DDRII) 4 of 7	
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 1.0
Date: Monday, October 02, 2006	Sheet 9 of 56	

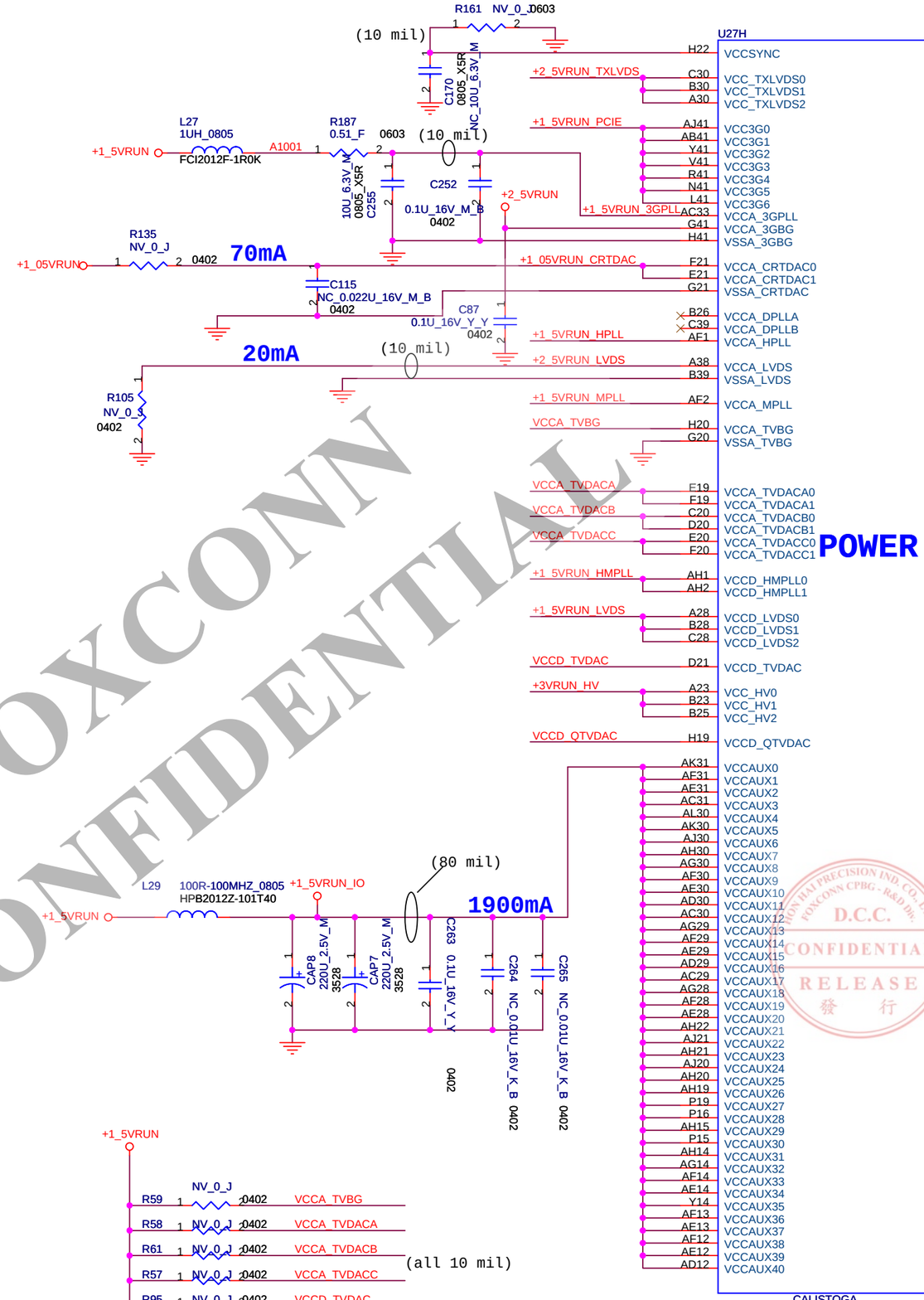


NOTE:
0.1UF caps in
1.5SxPLL need to be
located as edge caps
within 200mils









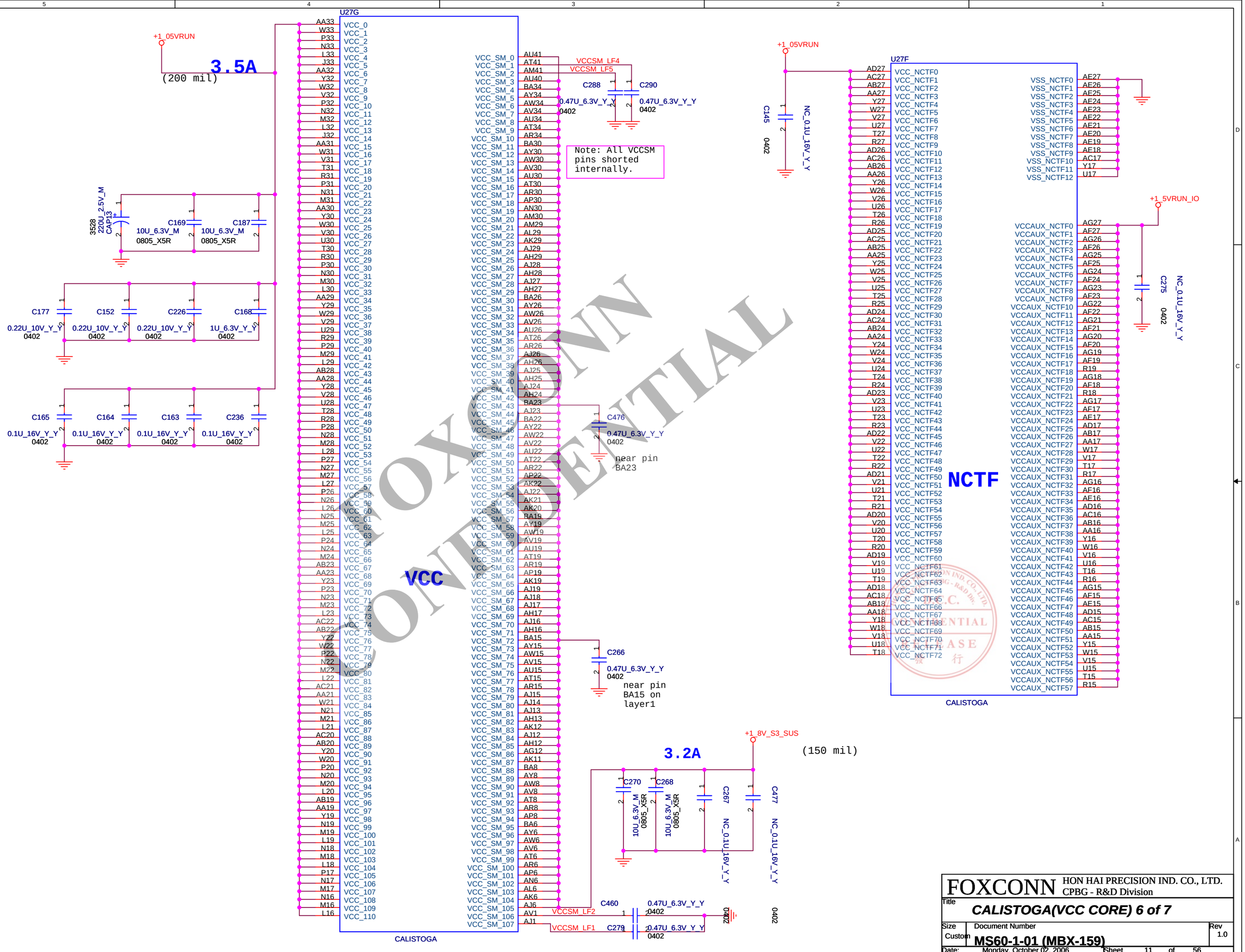
GMCH TV-OUT Disable

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: CALISTOGA(POWER,VCC) 5 of 7

Size: Custom | Document Number: MS60-1-01 (MBX-159) | Rev: 1.0

Date: Monday, October 02, 2006 | Sheet 10 of 56



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*CALISTOGA(VCC CORE) 6 of 7*	
Size: Custom	Document Number: MS60-1-01 (MBX-159)	Rev: 1.0
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7 MCH_CFG_5 — 1 — 30MIL TP45

MCH_CFG_5	Low = DMIx2 High = DMIx4

7 MCH_CFG_6 — 1 — 30MIL TP40

MCH_CFG_6	Low = Moby Dick High = Calistoga

DDR2 select (default high)

7 MCH_CFG_7 — 1 — 30MIL TP36

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor

7 MCH_CFG_9

R153 NC_2.2K_J 0402

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

7 MCH_CFG_10 — 1 — 30MIL TP35

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY

7 MCH_CFG_11

R128 NC_2.2K_J 0402

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga

7 MCH_CFG_12 — 1 — 30MIL TP47
7 MCH_CFG_13 — 1 — 30MIL TP55

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

7 MCH_CFG_16 — 1 — 30MIL TP44

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable

+3VRUN

R156 NC_2.2K_J 0402

7 MCH_CFG_18

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V

+3VRUN

R151 NC_2.2K_J 0402

7 MCH_CFG_19

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED

7 MCH_CFG_20 — 1 — 30MIL TP52

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U27I

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AE32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	E27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

VSS

CALISTOGA

U27J

AT23	VSS_180	VSS_273 J11
AN23	VSS_181	VSS_274 D11
AM23	VSS_182	VSS_275 B11
AH23	VSS_183	VSS_276 AV10
AC23	VSS_184	VSS_277 AP10
W23	VSS_185	VSS_278 AL10
K23	VSS_186	VSS_279 AJ10
J23	VSS_187	VSS_280 AG10
F23	VSS_188	VSS_281 AC10
C23	VSS_189	VSS_282 W10
AA22	VSS_190	VSS_283 U10
K22	VSS_191	VSS_284 BA9
G22	VSS_192	VSS_285 AW9
F22	VSS_193	VSS_286 AR9
E22	VSS_194	VSS_287 AH9
D22	VSS_195	VSS_288 AB9
A22	VSS_196	VSS_289 Y9
BA21	VSS_197	VSS_290 R9
AV21	VSS_198	VSS_291 G9
AR21	VSS_199	VSS_292 E9
AN21	VSS_200	VSS_293 A9
AL21	VSS_201	VSS_294 AG8
AB21	VSS_202	VSS_295 AD8
Y21	VSS_203	VSS_296 AA8
P21	VSS_204	VSS_297 U8
K21	VSS_205	VSS_298 K8
J21	VSS_206	VSS_299 C8
H21	VSS_207	VSS_300 BA7
C21	VSS_208	VSS_301 AV7
AW20	VSS_209	VSS_302 AP7
AR20	VSS_210	VSS_303 AL7
AM20	VSS_211	VSS_304 AJ7
AA20	VSS_212	VSS_305 AH7
K20	VSS_213	VSS_306 AE7
B20	VSS_214	VSS_307 AC7
A20	VSS_215	VSS_308 R7
AN19	VSS_216	VSS_309 G7
AC19	VSS_217	VSS_310 D7
W19	VSS_218	VSS_311 AG6
K19	VSS_219	VSS_312 AD6
G19	VSS_220	VSS_313 AB6
C19	VSS_221	VSS_314 Y6
AH18	VSS_222	VSS_315 U6
P18	VSS_223	VSS_316 N6
H18	VSS_224	VSS_317 K6
D18	VSS_225	VSS_318 H6
A18	VSS_226	VSS_319 B6
AY17	VSS_227	VSS_320 AV5
AR17	VSS_228	VSS_321 AF5
AP17	VSS_229	VSS_322 AD5
AM17	VSS_230	VSS_323 AY4
AK17	VSS_231	VSS_324 AR4
AV16	VSS_232	VSS_325 AP4
AN16	VSS_233	VSS_326 AL4
AL16	VSS_234	VSS_327 AJ4
J16	VSS_235	VSS_328 Y4
F16	VSS_236	VSS_329 U4
C16	VSS_237	VSS_330 R4
AN15	VSS_238	VSS_331 J4
AM15	VSS_239	VSS_332 F4
AK15	VSS_240	VSS_333 C4
N15	VSS_241	VSS_334 AY3
M15	VSS_242	VSS_335 AW3
L15	VSS_243	VSS_336 AV3
B15	VSS_244	VSS_337 AL3
A15	VSS_245	VSS_338 AH3
BA14	VSS_246	VSS_339 AG3
AT14	VSS_247	VSS_340 AF3
AK14	VSS_248	VSS_341 AD3
AD14	VSS_249	VSS_342 AC3
AA14	VSS_250	VSS_343 AA3
U14	VSS_251	VSS_344 G3
K14	VSS_252	VSS_345 AT2
H14	VSS_253	VSS_346 AR2
E14	VSS_254	VSS_347 AP2
AV13	VSS_255	VSS_348 AK2
AR13	VSS_256	VSS_349 AJ2
AN13	VSS_257	VSS_350 AD2
AM13	VSS_258	VSS_351 AB2
AL13	VSS_259	VSS_352 Y2
AG13	VSS_260	VSS_353 U2
P13	VSS_261	VSS_354 T2
F13	VSS_262	VSS_355 N2
D13	VSS_263	VSS_356 J2
B13	VSS_264	VSS_357 H2
AY12	VSS_265	VSS_358 F2
AC12	VSS_266	VSS_359 C2
K12	VSS_267	VSS_360 AL1
H12	VSS_268	
E12	VSS_269	
AD11	VSS_270	
AA11	VSS_271	
Y11	VSS_272	

VSS

CALISTOGA

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1.8V per DIMM=3.08A

DDR2_VREF
C344 0.1U_16V_M_B 0402
C345 2.2U_10V_Y_Y 0603
0.1 µF and 2.2 µF placed close to VREF pins

+1_8V_S3_SUS
+1_8V_S3_SUS

CN25

		1	VREF	VSS46	2	
DDR2_VREF		3	VSS47	DQ4	4	M_A_DQ4
M_A_DQ0		5	DQ0	DQ5	6	M_A_DQ5
M_A_DQ1		7	DQ1	VSS15	8	
		9	VSS37	DM0	10	M_A_DM0
M_A_DQS#0		11	DQS#0	VSS5	12	
M_A_DQS0		13	DQS0	DQ6	14	M_A_DQ6
		15	VSS48	DQ7	16	M_A_DQ7
M_A_DQ2		17	DQ2	VSS16	18	
M_A_DQ3		19	DQ3	DQ12	20	M_A_DQ12
		21	VSS38	DQ13	22	M_A_DQ13
M_A_DQ8		23	DQ8	VSS17	24	
M_A_DQ9		25	DQ9	DM1	26	M_A_DM1
		27	VSS49	VSS53	28	
M_A_DQS#1		29	DQS#1	CK0	30	M_CLK_DDR0 7
M_A_DQS1		31	DQS1	CK0#	32	M_CLK_DDR#0 7
		33	VSS39	VSS41	34	
M_A_DQ10		35	DQ10	DQ14	36	M_A_DQ14
M_A_DQ11		37	DQ11	DQ15	38	M_A_DQ15
		39	VSS50	VSS54	40	
		41	VSS18	VSS20	42	
M_A_DQ16		43	DQ16	DQ20	44	M_A_DQ20
M_A_DQ17		45	DQ17	DQ21	46	M_A_DQ21
		47	VSS1	VSS6	48	
M_A_DQS#2		49	DQS#2	NC3	50	DDR2_EXTTS#0 1 — R469 NC_0_J 0402 — 2 PM_EXTTS#0 7,14
M_A_DQS2		51	DQS2	DM2	52	M_A_DM2
		53	VSS19	VSS21	54	
M_A_DQ18		55	DQ18	DQ22	56	M_A_DQ22
M_A_DQ19		57	DQ19	DQ23	58	M_A_DQ23
		59	VSS22	VSS24	60	
M_A_DQ24		61	DQ24	DQ28	62	M_A_DQ28
M_A_DQ25		63	DQ25	DQ29	64	M_A_DQ29
		65	VSS23	VSS25	66	
M_A_DM3		67	DM3	DQS#3	68	M_A_DQS#3
		69	NC4	DQS3	70	M_A_DQS3
		71	VSS9	VSS10	72	
M_A_DQ26		73	DQ26	DQ30	74	M_A_DQ30
M_A_DQ27		75	DQ27	DQ31	76	M_A_DQ31
		77	VSS4	VSS8	78	
7,15 M_CKE0		79	CKE0	CKE1	80	M_CKE1 7,15
		81	VDD7	VDD8	82	
		83	NC1	A15	84	
9,15 M_A_BS2		85	A16_BA2	A14	86	
		87	VDD9	VDD11	88	
M_A_A12		89	A12	A11	90	M_A_A11
M_A_A9		91	A9	A7	92	M_A_A7
M_A_A8		93	A8	A6	94	M_A_A6
		95	VDD5	VDD4	96	
M_A_A5		97	A5	A4	98	M_A_A4
M_A_A3		99	A3	A2	100	M_A_A2
M_A_A1		101	A1	A0	102	M_A_A0
		103	VDD10	VDD12	104	
M_A_A10		105	A10/AP	BA1	106	M_A_BS1 9,15
9,15 M_A_BS0		107	BA0	RAS#	108	M_A_RAS# 9,15
9,15 M_A_WE#		109	WE#	S0#	110	M_CS#0 7,15
		111	VDD2	VDD1	112	
9,15 M_A_CAS#		113	CAS#	ODT0	114	M_ODT0 7,15
7,15 M_CS#1		115	S1#	A13	116	M_A_A13
		117	VDD3	VDD6	118	
7,15 M_ODT1		119	ODT1	NC2	120	
		121	VSS11	VSS12	122	
M_A_DQ32		123	DQ32	DQ36	124	M_A_DQ36
M_A_DQ33		125	DQ33	DQ37	126	M_A_DQ37
		127	VSS26	VSS28	128	
M_A_DQS#4		129	DQS#4	DM4	130	M_A_DM4
M_A_DQS4		131	DQS4	VSS42	132	
		133	VSS2	DQ38	134	M_A_DQ38
M_A_DQ34		135	DQ34	DQ39	136	M_A_DQ39
M_A_DQ35		137	DQ35	VSS55	138	
		139	VSS27	DQ44	140	M_A_DQ44
M_A_DQ40		141	DQ40	DQ45	142	M_A_DQ45
M_A_DQ41		143	DQ41	VSS43	144	
		145	VSS29	DQS#5	146	M_A_DQS#5
M_A_DM5		147	DM5	DQS5	148	M_A_DQS5
		149	VSS51	VSS56	150	
M_A_DQ42		151	DQ42	DQ46	152	M_A_DQ46
M_A_DQ43		153	DQ43	DQ47	154	M_A_DQ47
		155	VSS40	VSS44	156	
M_A_DQ48		157	DQ48	DQ52	158	M_A_DQ52
M_A_DQ49		159	DQ49	DQ53	160	M_A_DQ53
		161	VSS52	VSS57	162	
		163	NCTEST	CK1	164	M_CLK_DDR1 7
		165	VSS30	CK1#	166	M_CLK_DDR#1 7
M_A_DQS#6		167	DQS#6	VSS45	168	
M_A_DQS6		169	DQS6	DM6	170	M_A_DM6
		171	VSS31	VSS32	172	
M_A_DQ50		173	DQ50	DQ54	174	M_A_DQ54
M_A_DQ51		175	DQ51	DQ55	176	M_A_DQ55
		177	VSS33	VSS35	178	
M_A_DQ56		179	DQ56	DQ60	180	M_A_DQ60
M_A_DQ57		181	DQ57	DQ61	182	M_A_DQ61
		183	VSS3	VSS7	184	
M_A_DM7		185	DM7	DQS#7	186	M_A_DQS#7
		187	VSS34	DQS7	188	M_A_DQS7
M_A_DQ58		189	DQ58	VSS36	190	
M_A_DQ59		191	DQ59	DQ62	192	M_A_DQ62
		193	VSS14	DQ63	194	M_A_DQ63
14,28,43,53 SMB_DATA_SB		195	SDA	VSS13	196	
14,28,43,53 SMB_CLK_SB		197	SCL	SA0	198	SA0_DIM0 — R471 10K_J 0402
+3VRUN		199	VDD(SPD)	SA1	200	SA1_DIM0 — R470 10K_J 0402
		201	GND1	GND2	202	
		203	NPTH1	NPTH2	204	

PC4800 DDR2 SDRAM SO-DIMM (200P)

DDR2 SO-DIMM_2x100P
FOX_AS0A426_N2RN_7F

SMBus Address: A0(W)/A1(R)

C523 2.2U_10V_Y_Y 0603
C517 0.1U_16V_M_B 0402

DIMM_0

M_A_DM[0..7] 9
M_A_DQ[0..63] 9
M_A_DQS[0..7] 9
M_A_DQS#[0..7] 9
M_A_A[0..13] 9,15

DDRDIMM_VREF +1_8V_S3_SUS
R287 0_J 0402
R286 NC_10K_F 0402
DDR2_VREF
DDR2_VREF
(20 mil)
C364 0.1U_16V_M_B 0402
R288 NC_10K_F 0402
R287 NC_10K_F 0402
Close to DIMM

+1_8V_S3_SUS
Place these Caps near So-Dimm0.
C519 2.2U_10V_Y_Y 0603
C562 2.2U_10V_Y_Y 0603
C521 2.2U_10V_Y_Y 0603
C518 2.2U_10V_Y_Y 0603
C358 2.2U_10V_Y_Y 0603

+1_8V_S3_SUS
Place these Caps near So-Dimm0.
C520 0.1U_16V_Y_Y 0402
C360 0.1U_16V_Y_Y 0402
C522 0.1U_16V_Y_Y 0402
C516 0.1U_16V_Y_Y 0402

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***DDR(II)SO-DIMM_0***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
Date: Monday, October 02, 2006	Sheet 13 of 56	

1.8V per DIMM=3.08A

DDR2_VREF

C363 0.1U_16V_M_B 0402

C362 2.2U_10V_Y_Y 0603

0.1 µF and 2.2 µF placed close to VREF pins

+1_8V_S3_SUS

+1_8V_S3_SUS

CN26

	1	VREF	VSS46	2	
	3	VSS47	DQ4	4	M_B_DQ4
M_B_DQ0	5	DQ0	DQ5	6	M_B_DQ5
M_B_DQ1	7	DQ1	VSS15	8	
	9	VSS37	DM0	10	M_B_DM0
M_B_DQS#0	11	DQS#0	VSS5	12	
M_B_DQS0	13	DQS0	DQ6	14	M_B_DQ6
	15	VSS48	DQ7	16	M_B_DQ7
M_B_DQ2	17	DQ2	VSS16	18	
M_B_DQ3	19	DQ3	DQ12	20	M_B_DQ12
	21	VSS38	DQ13	22	M_B_DQ13
M_B_DQ8	23	DQ8	VSS17	24	
M_B_DQ9	25	DQ9	DM1	26	M_B_DM1
	27	VSS49	VSS53	28	
M_B_DQS#1	29	DQS#1	CK0	30	M_CLK_DDR3 7
M_B_DQS1	31	DQS1	CK0#	32	M_CLK_DDR#3 7
	33	VSS39	VSS41	34	
M_B_DQ10	35	DQ10	DQ14	36	M_B_DQ14
M_B_DQ11	37	DQ11	DQ15	38	M_B_DQ15
	39	VSS50	VSS54	40	
	41	VSS18	VSS20	42	
M_B_DQ16	43	DQ16	DQ20	44	M_B_DQ20
M_B_DQ17	45	DQ17	DQ21	46	M_B_DQ21
	47	VSS1	VSS6	48	
M_B_DQS#2	49	DQS#2	NC3	50	PM_EXTTS#0_DIMM2
M_B_DQS2	51	DQS2	DM2	52	M_B_DM2
	53	VSS19	VSS21	54	
M_B_DQ18	55	DQ18	DQ22	56	M_B_DQ22
M_B_DQ19	57	DQ19	DQ23	58	M_B_DQ23
	59	VSS22	VSS24	60	
M_B_DQ24	61	DQ24	DQ28	62	M_B_DQ28
M_B_DQ25	63	DQ25	DQ29	64	M_B_DQ29
	65	VSS23	VSS25	66	
M_B_DM3	67	DM3	DQS#3	68	M_B_DQS#3
	69	NC4	DQS3	70	M_B_DQS3
	71	VSS9	VSS10	72	
M_B_DQ26	73	DQ26	DQ30	74	M_B_DQ30
M_B_DQ27	75	DQ27	DQ31	76	M_B_DQ31
	77	VSS4	VSS8	78	
7,15 M_CKE2	79	CKE0	CKE1	80	M_CKE3 7,15
	81	VDD7	VDD8	82	
9,15 M_B_BS2	83	NC1	A15	84	
	85	A16_BA2	A14	86	
	87	VDD9	VDD11	88	
M_B_A12	89	A12	A11	90	M_B_A11
M_B_A9	91	A9	A7	92	M_B_A7
M_B_A8	93	A8	A6	94	M_B_A6
	95	VDD5	VDD4	96	
M_B_A5	97	A5	A4	98	M_B_A4
M_B_A3	99	A3	A2	100	M_B_A2
M_B_A1	101	A1	A0	102	M_B_A0
	103	VDD10	VDD12	104	
M_B_A10	105	A10/AP	BA1	106	M_B_BS1 9,15
9,15 M_B_BS0	107	BA0	RAS#	108	M_B_RAS# 9,15
9,15 M_B_WE#	109	WE#	S0#	110	M_CS#2 7,15
	111	VDD2	VDD1	112	
9,15 M_B_CAS#	113	CAS#	ODT0	114	M_ODT2 7,15
7,15 M_CS#3	115	S1#	A13	116	M_B_A13
	117	VDD3	VDD6	118	
7,15 M_ODT3	119	ODT1	NC2	120	
	121	VSS11	VSS12	122	
M_B_DQ32	123	DQ32	DQ36	124	M_B_DQ36
M_B_DQ33	125	DQ33	DQ37	126	M_B_DQ37
	127	VSS26	VSS28	128	
M_B_DQS#4	129	DQS#4	DM4	130	M_B_DM4
M_B_DQS4	131	DQS4	VSS42	132	
	133	VSS2	DQ38	134	M_B_DQ38
M_B_DQ34	135	DQ34	DQ39	136	M_B_DQ39
M_B_DQ35	137	DQ35	VSS55	138	
	139	VSS27	DQ44	140	M_B_DQ44
M_B_DQ40	141	DQ40	DQ45	142	M_B_DQ45
M_B_DQ41	143	DQ41	VSS43	144	
	145	VSS29	DQS#5	146	M_B_DQS#5
M_B_DM5	147	DM5	DQS5	148	M_B_DQS5
	149	VSS51	VSS56	150	
M_B_DQ42	151	DQ42	DQ46	152	M_B_DQ46
M_B_DQ43	153	DQ43	DQ47	154	M_B_DQ47
	155	VSS40	VSS44	156	
M_B_DQ48	157	DQ48	DQ52	158	M_B_DQ52
M_B_DQ49	159	DQ49	DQ53	160	M_B_DQ53
	161	VSS52	VSS57	162	
	163	NCTEST	CK1	164	M_CLK_DDR2 7
	165	VSS30	CK1#	166	M_CLK_DDR#2 7
M_B_DQS#6	167	DQS#6	VSS45	168	
M_B_DQS6	169	DQS6	DM6	170	M_B_DM6
	171	VSS31	VSS32	172	
M_B_DQ50	173	DQ50	DQ54	174	M_B_DQ54
M_B_DQ51	175	DQ51	DQ55	176	M_B_DQ55
	177	VSS33	VSS35	178	
M_B_DQ56	179	DQ56	DQ60	180	M_B_DQ60
M_B_DQ57	181	DQ57	DQ61	182	M_B_DQ61
	183	VSS3	VSS7	184	
M_B_DM7	185	DM7	DQS#7	186	M_B_DQS#7
	187	VSS34	DQS7	188	M_B_DQS7
M_B_DQ58	189	DQ58	VSS36	190	
M_B_DQ59	191	DQ59	DQ62	192	M_B_DQ62
	193	VSS14	DQ63	194	M_B_DQ63
13,28,43,53 SMB_DATA_SB	195	SDA	VSS13	196	
13,28,43,53 SMB_CLK_SB	197	SCL	SA0	198	SA0_DIM1
	199	VDD(SPD)	SA1	200	SA1_DIM1
	201	GND1	GND2	202	
	203	NPTH1	NPTH2	204	

PC4800 DDR2 SDRAM SO-DIMM (200P)

9.2mm

DDR2 SO-DIMM_2x100P

FOX_AS0A426_NARN_7F

DIMM_1

R509 1 NC_0_J 0402 2

PM_EXTTS#0 7,13

M_B_DM[0..7] 9
M_B_DQ[0..63] 9
M_B_DQS[0..7] 9
M_B_DQS#[0..7] 9
M_B_A[0..13] 9,15

Place these Caps near So-Dimm1.

+1_8V_S3_SUS

C359 2.2U_10V_Y_Y 0603

C357 2.2U_10V_Y_Y 0603

C376 2.2U_10V_Y_Y 0603

C563 2.2U_10V_Y_Y 0603

C377 2.2U_10V_Y_Y 0603

Place these Caps near So-Dimm1.

+1_8V_S3_SUS

C564 0.1U_16V_Y_Y 0402

C375 0.1U_16V_Y_Y 0402

C378 0.1U_16V_Y_Y 0402

C374 0.1U_16V_Y_Y 0402

SMBus Address: A4(W)/A5(R)

+3VRUN

R508 10K_J 0402

R507 10K_J 0402

+3VRUN

C365 2.2U_10V_Y_Y 0603

C372 0.1U_16V_M_B 0402

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ***DDR(II)SO-DIMM_1***

Size: Custom | Document Number: **MS60-1-01 (MBX-159)** | Rev: 1.0

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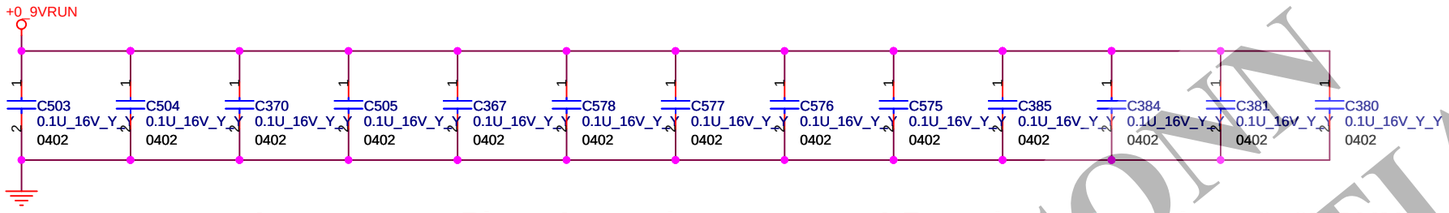
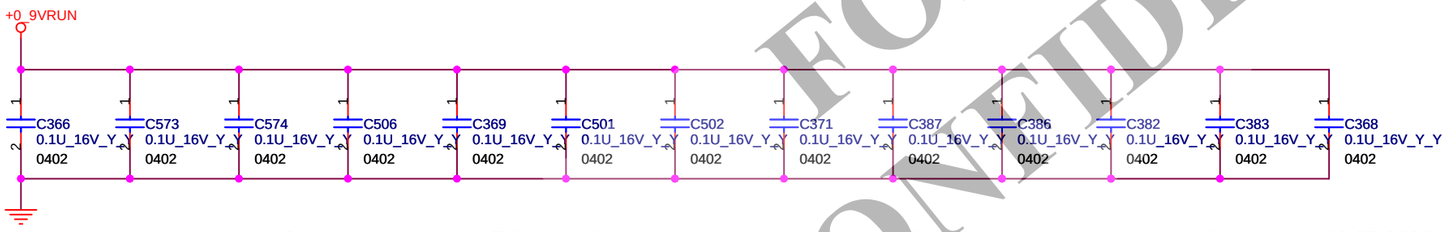


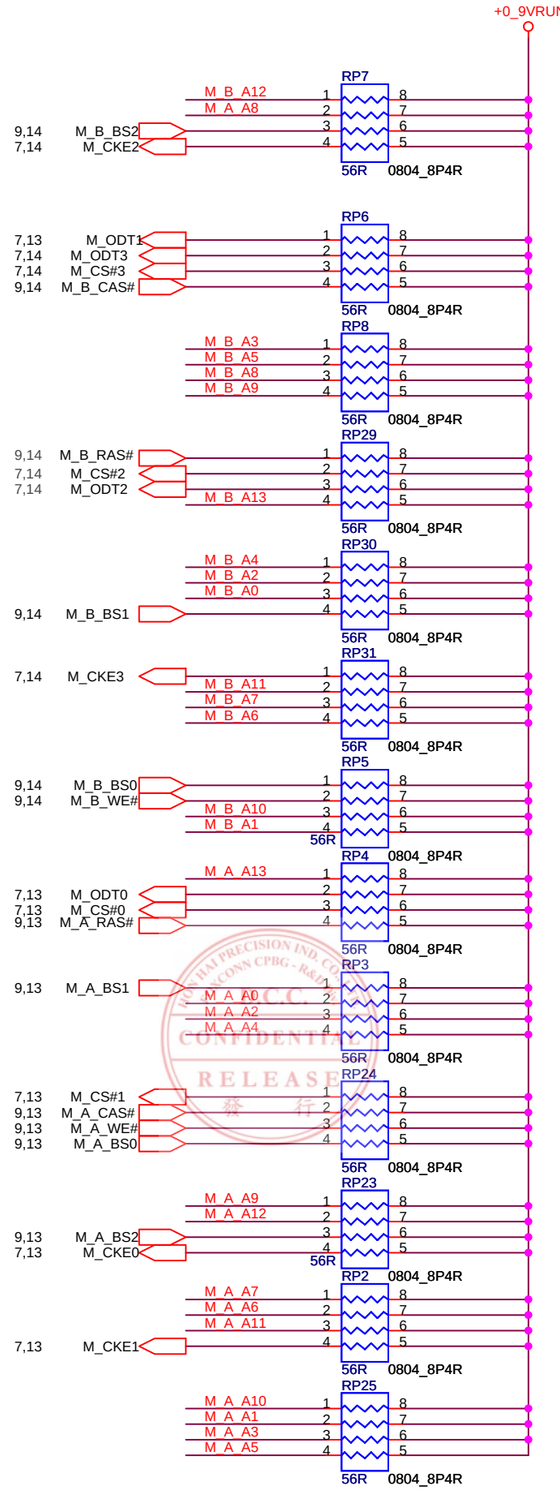
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN

9,13 M_A_A[0..13]

9,14 M_B_A[0..13]



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ***DDR(II)Termination***

Size	Document Number	Rev
A3	**MS60-1-01 (MBX-159)**	1.0

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17 TXP[0..15]
TXP0 TXP1 TXP2 TXP3 TXP4 TXP5 TXP6 TXP7 TXP8 TXP9 TXP10 TXP11 TXP12 TXP13 TXP14 TXP15

17 TXN[0..15]
TXN0 TXN1 TXN2 TXN3 TXN4 TXN5 TXN6 TXN7 TXN8 TXN9 TXN10 TXN11 TXN12 TXN13 TXN14 TXN15

8 PEG_RXP_C[0..15]
PEG_RXP_C0 PEG_RXP_C1 PEG_RXP_C2 PEG_RXP_C3 PEG_RXP_C4 PEG_RXP_C5 PEG_RXP_C6 PEG_RXP_C7 PEG_RXP_C8 PEG_RXP_C9 PEG_RXP_C10 PEG_RXP_C11 PEG_RXP_C12 PEG_RXP_C13 PEG_RXP_C14 PEG_RXP_C15

8 PEG_RXN_C[0..15]
PEG_RXN_C0 PEG_RXN_C1 PEG_RXN_C2 PEG_RXN_C3 PEG_RXN_C4 PEG_RXN_C5 PEG_RXN_C6 PEG_RXN_C7 PEG_RXN_C8 PEG_RXN_C9 PEG_RXN_C10 PEG_RXN_C11 PEG_RXN_C12 PEG_RXN_C13 PEG_RXN_C14 PEG_RXN_C15

PLT_RST# NV
26MIL TP94 1
26MIL TP95 1
53 CLK_PCIE_PEG
53 CLK_PCIE_PEG#

U25A
NV_GF-GO7400-N-A3-A3

1.2V 1420mA(Internal Core Power)
C141 NV_1U_25V_K_B 0201_X5R
C138 NV_4.7U_10V_Y_Y 0603
C218 NV_4.7U_10V_Y_Y 0805
C604 NV_1000P_50V_M_B 0402
C201 NV_4.7U_10V_Y_Y 0805
Close to ball
Close to BGA

1.2V 1420mA (I/O Power)
C209 NV_0.1U_6.3V_K 0201_X5R
C243 NV_1U_25V_K_B 0201_X5R
C233 NV_0.1U_6.3V_K 0603
C182 NV_10U_6.3V_M 0805_X5R
C175 NV_1000P_50V_M_B 0402
C231 NV_1000P_50V_M_B 0402
Close to BGA

16.25A(Internal logic core power)
NV_VDD 1.025V
C157 NV_0.1U_6.3V_K 0201_X5R
C151 NV_0.1U_6.3V_K 0201_X5R
C211 NV_0.1U_6.3V_K 0201_X5R
C203 NV_0.1U_6.3V_K 0201_X5R
NVVDD_SENSE
C183 NV_0.1U_6.3V_K 0201_X5R
C171 NV_0.1U_6.3V_K 0201_X5R
C210 NV_0.1U_6.3V_K 0201_X5R
C194 NV_0.1U_6.3V_K 0201_X5R
C192 NV_0.1U_6.3V_K 0201_X5R
C200 NV_0.1U_6.3V_K 0201_X5R
C174 NV_1000P_50V_M_B 0402
C160 NV_1000P_50V_M_B 0402
C189 NV_10U_6.3V_M 0805_X5R
C190 NV_10U_6.3V_M 0805_X5R
CAP5 NV_220U_2.5V_M 3528

CRB circuit
C137 NV_0.01U_16V_K_B 0402
NVVDD_SENSE GND_SENSE

110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)
C154 NV_0.1U_6.3V_K 0201_X5R
C173 NV_0.022U_16V_M_B 0402
C161 NV_1000P_50V_M_B 0402
C143 NV_1U_10V_Y_Y 0603
+3VRUN

PEX_PLL_AVDD
PEX_PLL_DVDD 20mA(Power rail) 1.2V
C68 NV_1000P_50V_M_B 0402
C83 NV_0.1U_16V_M_B 0402
C100 NV_4.7U_10V_Y_Y 0805
L23 NV_10NH_0603 WL1608C10NJ
C158 NV_4.7U_10V_Y_Y 0805

U25D
GND_SENSE

+1_8VRUN
FBCAL_PD_VDDQ R160 NV_60.4_F 0402
Vendor recommand
FBCAL_PU_GND R150 NV_40.2_F 0603
FBCAL_TERM_GND R171 NV_40.2_F 0603

+3VRUN
C53 NV_1U_6.3V_M 0402_X5R
PVT Change
U5 NV_74AHCT1G08GW
3,7,26,28,31,32,33,43 PLT_RST#
R50 NV_100_J 0402
R49 NV_10K_J 0402
R48 NC_0_J 0402
PLT_RST# NV

U25K
R316 NV_0_J 0603
C419 NV_4.7U_10V_Y_Y 0805
10mA
MIOB_VDD
C112 NV_0.1U_6.3V_K 0201_X5R
C120 NV_0.1U_6.3V_K 0201_X5R
R113 NC_1K_F 0402
26MIL TP32
26MIL TP30
MIOB_PD_VDDQ
MIOB_PU_GND
MIOB_VREF
C93 NC_0.1U_6.3V_K 0201_X5R
R114 NC_1K_F 0402
MIOB_CLKIN
R98 NV_10K_J 0402
NC for present design.
only for NV43 strapping.
change to TP in next version

R129 NV_2K_F 0402
R323 NV_0_J 0603
C185 1U_6.3V_Y_Y 0402
U25C
FBVDDQ 3600mA(Frame Buffer core power for I/O)
C213 C212 C208 C217 NV_0.1U_6.3V_K 0201_X5R
C217 NV_47U_10V_Y_Y 0805

4/26
Follow FAE suggest
BCAL_TERM_GND is not used for DDR.

VDD_LP (Secondary internal core power) 1.025V
C122 NV_1000P_50V_M_B 0402
C155 NV_0.1U_6.3V_K 0201_X5R
C146 NV_0.1U_6.3V_K 0201_X5R
C127 0805_X5R NV_10U_6.3V_M
L24 NV_120R-100MHZ_0603 EBMS160808A121
NV_VDD
PC177 NV_220U_2.5V_M 3528

PEX_PLL_AVDD 100mA(Analog Power) 1.2V
C84 NV_1000P_50V_M_B 0402
C89 NV_0.1U_6.3V_K 0201_X5R
C65 NV_4.7U_10V_Y_Y 0805
L21 NV_10NH_0603 WL1608C10NJ
PEX_VDD
NIVIDIA FBA suggest to use 1000p capacitor

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VGA(PCI-E/STRAP) 1/7		
Size A2	Document Number MS60-1-01 (MBX-159)		Rev 1.0
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8 PEG_RXP[0..15]

PEG_RXP0	C88	NV_0.1U_6.3V_K	0201_X5R	TXP0	
PEG_RXP1	C104	NV_0.1U_6.3V_K	0201_X5R	TXP1	
PEG_RXP2	C116	NV_0.1U_6.3V_K	0201_X5R	TXP2	
PEG_RXP3	C126	NV_0.1U_6.3V_K	0201_X5R	TXP3	
PEG_RXP4	C133	NV_0.1U_6.3V_K	0201_X5R	TXP4	
PEG_RXP5	C140	NV_0.1U_6.3V_K	0201_X5R	TXP5	
PEG_RXP6	C148	NV_0.1U_6.3V_K	0201_X5R	TXP6	
PEG_RXP7	C167	NV_0.1U_6.3V_K	0201_X5R	TXP7	
PEG_RXP8	C179	NV_0.1U_6.3V_K	0201_X5R	TXP8	
PEG_RXP9	C195	NV_0.1U_6.3V_K	0201_X5R	TXP9	
PEG_RXP10	C205	NV_0.1U_6.3V_K	0201_X5R	TXP10	
PEG_RXP11	C225	NV_0.1U_6.3V_K	0201_X5R	TXP11	
PEG_RXP12	C230	NV_0.1U_6.3V_K	0201_X5R	TXP12	
PEG_RXP13	C240	NV_0.1U_6.3V_K	0201_X5R	TXP13	
PEG_RXP14	C249	NV_0.1U_6.3V_K	0201_X5R	TXP14	
PEG_RXP15	C253	NV_0.1U_6.3V_K	0201_X5R	TXP15	

TXP[0..15] 16

8 PEG_RXN[0..15]

PEG_RXN0	C98	NV_0.1U_6.3V_K	0201_X5R	TXN0	
PEG_RXN1	C113	NV_0.1U_6.3V_K	0201_X5R	TXN1	
PEG_RXN2	C123	NV_0.1U_6.3V_K	0201_X5R	TXN2	
PEG_RXN3	C132	NV_0.1U_6.3V_K	0201_X5R	TXN3	
PEG_RXN4	C136	NV_0.1U_6.3V_K	0201_X5R	TXN4	
PEG_RXN5	C147	NV_0.1U_6.3V_K	0201_X5R	TXN5	
PEG_RXN6	C156	NV_0.1U_6.3V_K	0201_X5R	TXN6	
PEG_RXN7	C180	NV_0.1U_6.3V_K	0201_X5R	TXN7	
PEG_RXN8	C188	NV_0.1U_6.3V_K	0201_X5R	TXN8	
PEG_RXN9	C206	NV_0.1U_6.3V_K	0201_X5R	TXN9	
PEG_RXN10	C214	NV_0.1U_6.3V_K	0201_X5R	TXN10	
PEG_RXN11	C232	NV_0.1U_6.3V_K	0201_X5R	TXN11	
PEG_RXN12	C238	NV_0.1U_6.3V_K	0201_X5R	TXN12	
PEG_RXN13	C245	NV_0.1U_6.3V_K	0201_X5R	TXN13	
PEG_RXN14	C251	NV_0.1U_6.3V_K	0201_X5R	TXN14	
PEG_RXN15	C256	NV_0.1U_6.3V_K	0201_X5R	TXN15	

TXN[0..15] 16

TVMODE
NTSC (01)

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball
0001 16Mx32 Infineon
0010 16Mx32 Hynix
0011 16Mx32 Samsung
0101 8Mx32 Infineon
0110 8Mx32 Hynix
0111 8Mx32 Samsung

SUBVENDOR
0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

PANEL ID CONFIG
NC

MIOAD0 is used to set the PCI Express PLL termination enable.
DEFAULT "0"

3GIO_PADCFG[2:0]
001 for G7X

G72M/G73M
PCI_DEVID[3:0]="1000"->8

CRYSTAL
10 (27M Hz)

MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

ROM_TYPE NC

00 PARALLEL
01 SERIAL_AT25F
10 SERIAL_SST45VF
11 LPC

MIOAD0 MIOAD1 MIOAD6 MIOAD7 MIOAD8 MIOAD9 MIOAD10 — 16

MIOBD0 MIOBD1 MIOBD2 MIOBD3 MIOBD4 MIOBD5 MIOBD6 MIOBD8 MIOBD9 MIOBD11 — 16

+3VRUN

MIOAD7	R74	NC_2K_J	0402	R55	NV_2K_J	0402	
MIOAD10	R75	NV_2K_J	0402	R56	NC_2K_J	0402	
RAM_CFG0	MIOBD0	R104	NV_2K_J	0402	R103	NC_2K_J	0402
RAM_CFG1	MIOBD1	R117	NC_2K_J	0402	R116	NV_2K_J	0402
RAM_CFG2	MIOBD8	R337	NC_2K_J	0402	R319	NV_2K_J	0402
RAM_CFG3	MIOBD9	R338	NV_2K_J	0402	R320	NC_2K_J	0402
SUBVENDOR	MIOAD1	R352	NV_2K_J	0402	R353	NC_2K_J	0402
PEX_PLL_EN_TERM	MIOAD0	R350	NV_2K_J	0402	R351	NC_2K_J	0402
3GIO_PADCFG0	MIOAD6	R358	NC_NV_2K_J	0402	R359	NV_2K_J	0402
3GIO_PADCFG1	MIOAD8	R355	NV_2K_J	0402	R356	NC_NV_2K_J	0402
3GIO_PADCFG2	MIOAD9	R123	NV_2K_J	0402	R122	NC_2K_J	0402
PCI_DEVID 0	MIOBD4	R94	NV_2K_J	0402	R93	NC_2K_J	0402
PCI_DEVID 1	MIOBD5	R339	NV_2K_J	0402	R321	NC_2K_J	0402
PCI_DEVID 2	MIOBD3	R347	NV_2K_J	0402	R348	NC_2K_J	0402
PCI_DEVID 3	MIOBD11	R336	NC_2K_J	0402	R318	NV_2K_J	0402
CRYSTAL 0	MIOBD2	R88	NV_2K_J	0402	R87	NC_2K_J	0402
CRYSTAL 1	MIOBD6	R73	NC_2K_J	0402	R54	NV_2K_J	0402

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA(PCI-E/STRAP) 2/7

Size: A3 | Document Number: MS60-1-01 (MBX-159) | Rev: 1.0

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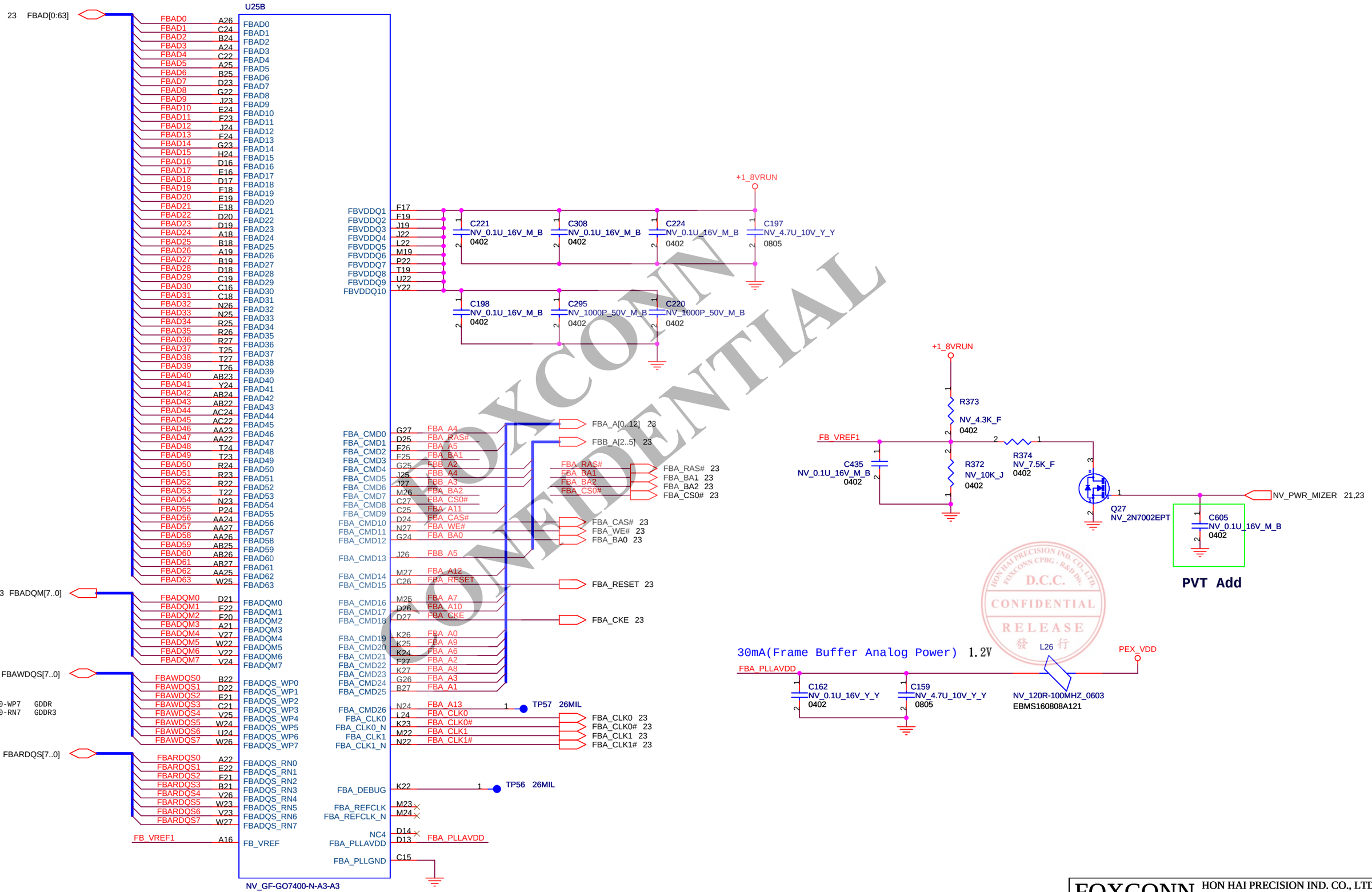

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(GDDR3) 3/7	
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 1.0
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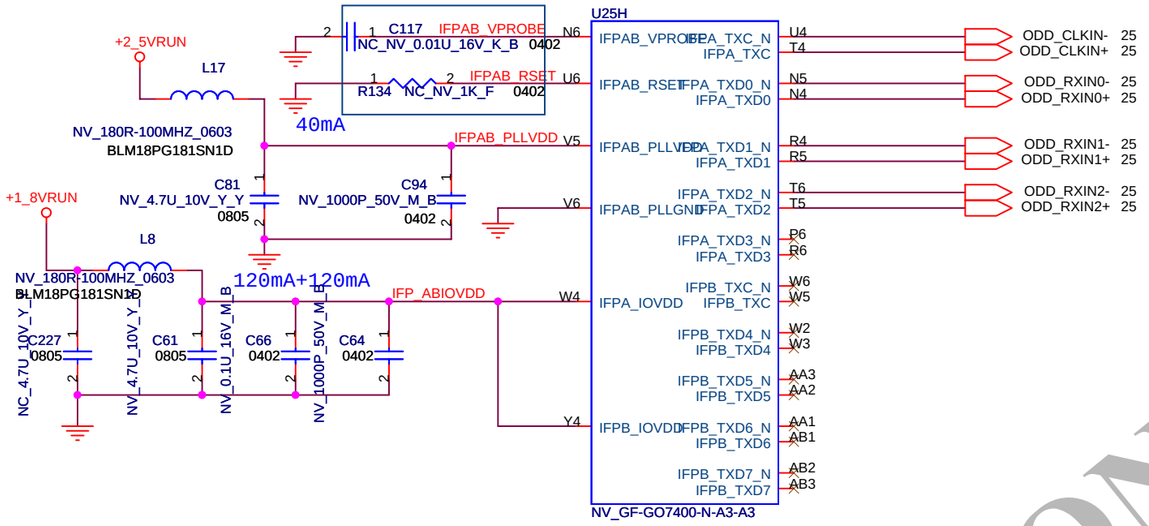
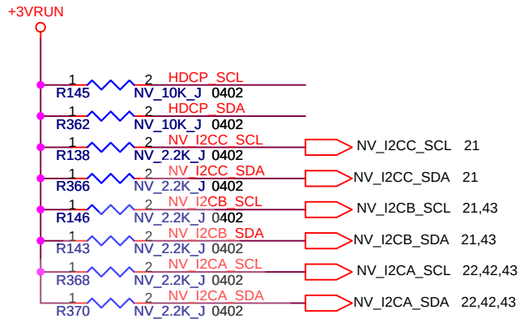
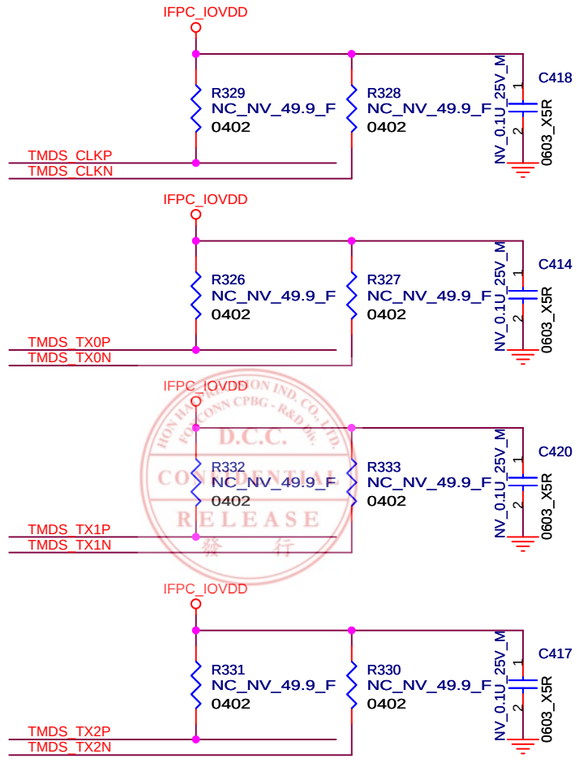
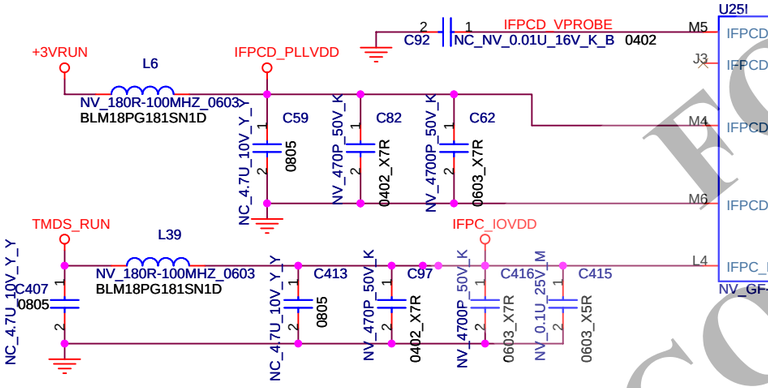
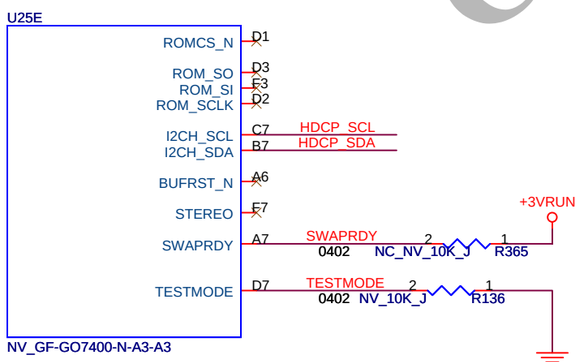
UN STUFF FOR G7X

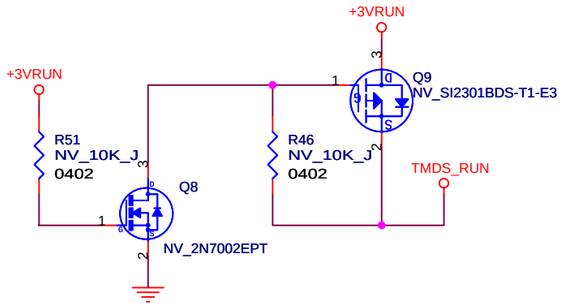












FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*VGA(TMDS/LVDS) 4/7*	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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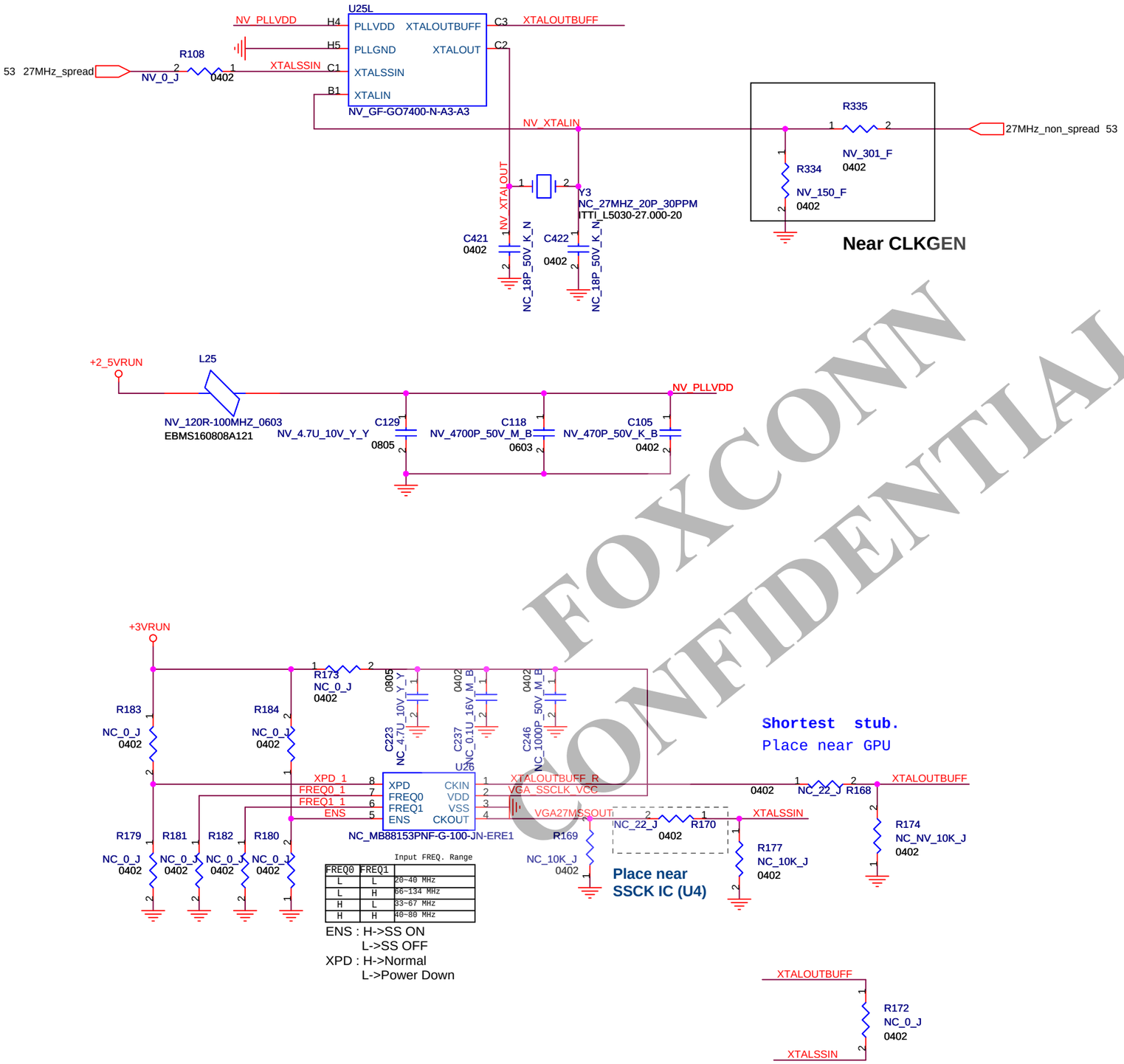

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VGA(SS) 5/7		
Size A3	Document Number MS60-1-01 (MBX-159)		Rev 1.0
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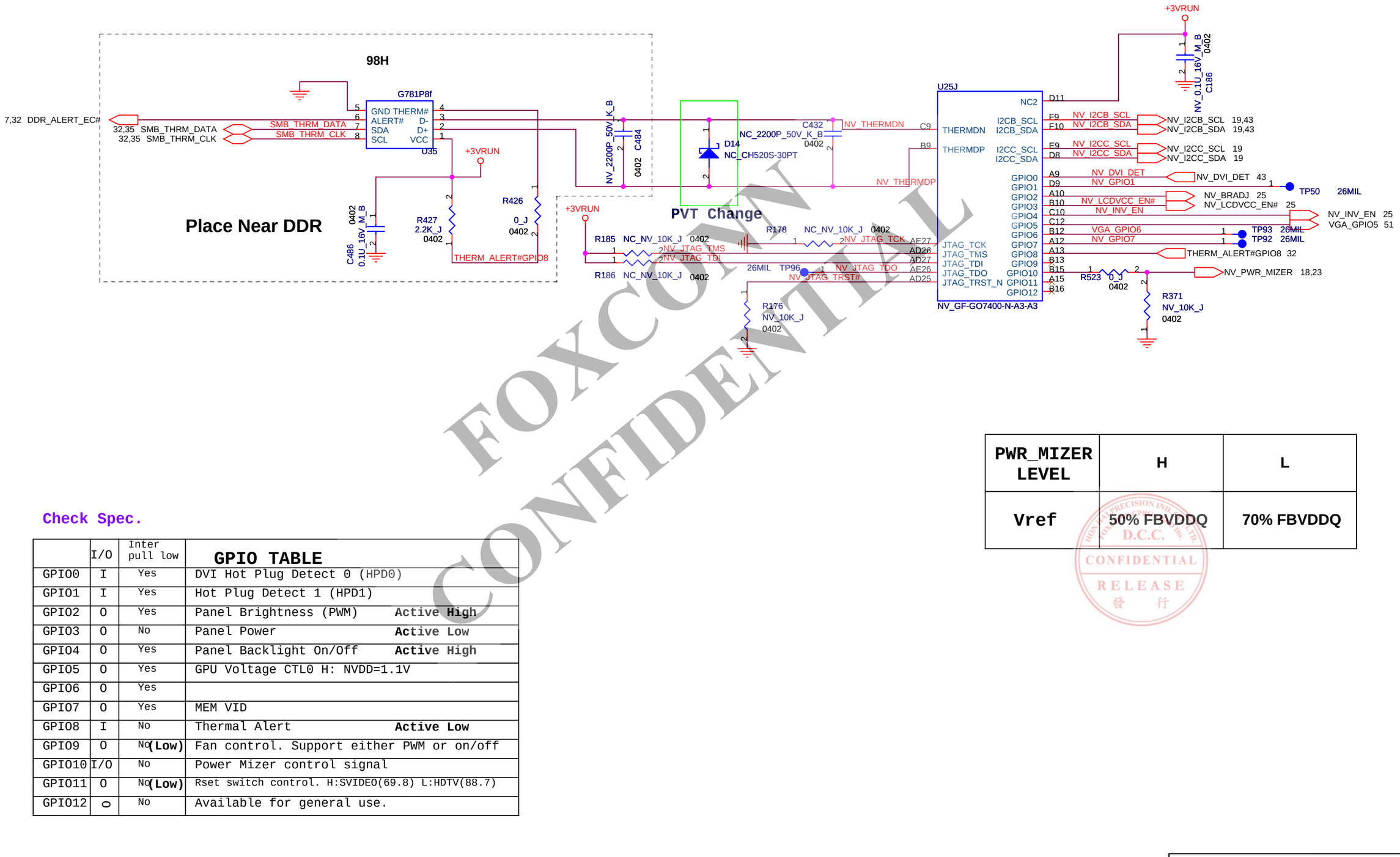

Check Spec.

	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) **Active High**
GPIO3	O	No	Panel Power **Active Low**
GPIO4	O	Yes	Panel Backlight On/Off **Active High**
GPIO5	O	Yes	GPU Voltage CTL0 H: NVDD=1.1V
GPIO6	O	Yes	
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert **Active Low**
GPIO9	O	No **(Low)**	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Power Mizer control signal
GPIO11	O	No **(Low)**	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

PWR_MIZER LEVEL	H	L
Vref	50% FBVDDQ	70% FBVDDQ

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *VGA(MULTIUSE) 6/7*

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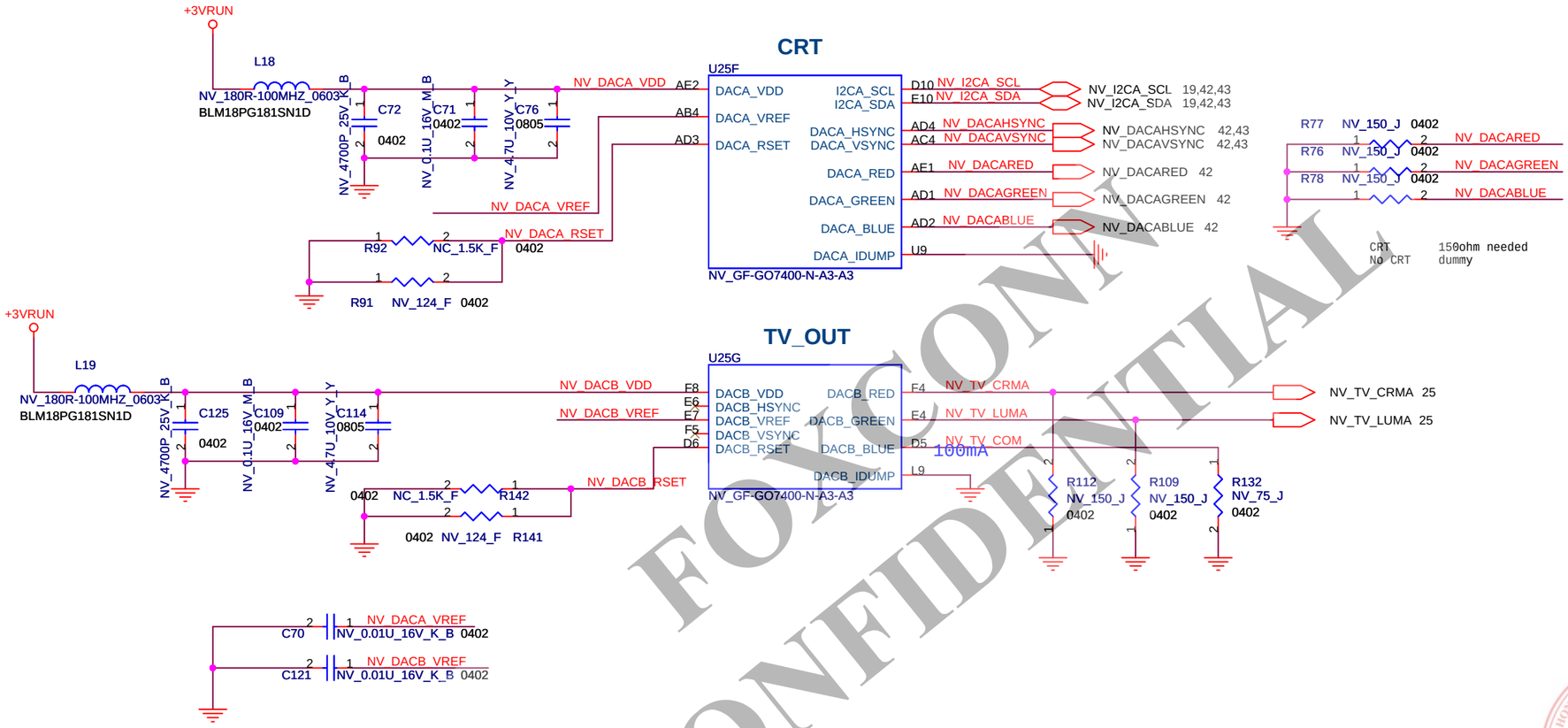

DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCCLK			SCL
	VGA-DDCDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE	PB	
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCCLK			SCL
	DVI-DDCDATA			SDA

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA(TV/CRT) 7/7

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Address / Command on Die termination is set to 120 ohm.

U30 — NV_HY5RS573225AFP-2

U31 — NV_HY5RS573225AFP-2

DLL POWER --- Add decoupling C and L ?

Minimum 200us delay required prior to applying any executable command after stable power and clock.

For 16Mx32 Bit stuff
8Mx32 Bit no stuff

For 8Mx32 Bit Stuff
16Mx32 Bit no stuff

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

VRAM_VREF is 70%FBVDDQ for GDDR3

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*VRAM(GDDR3)*
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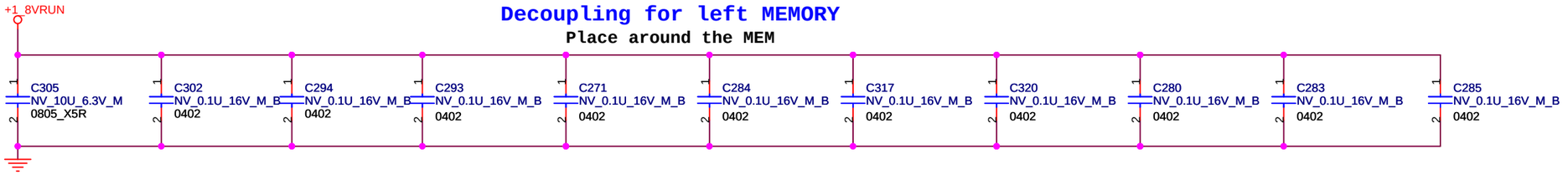
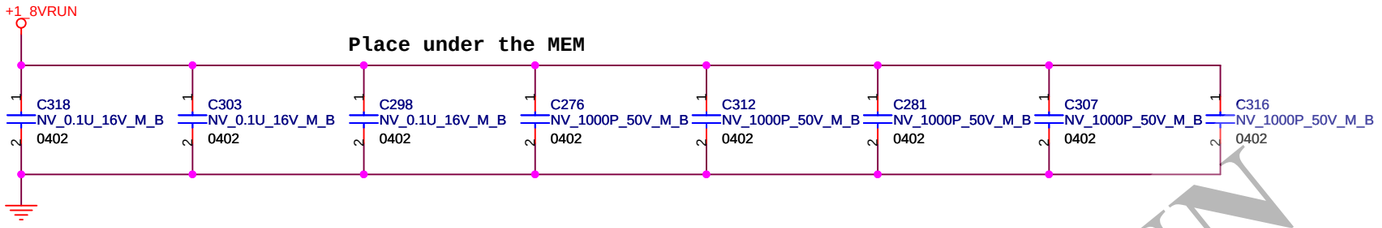
Decoupling for left MEMORY

Place around the MEM

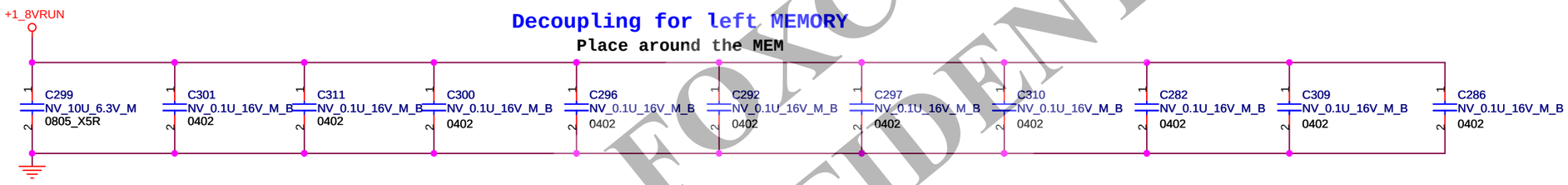


Place under the MEM

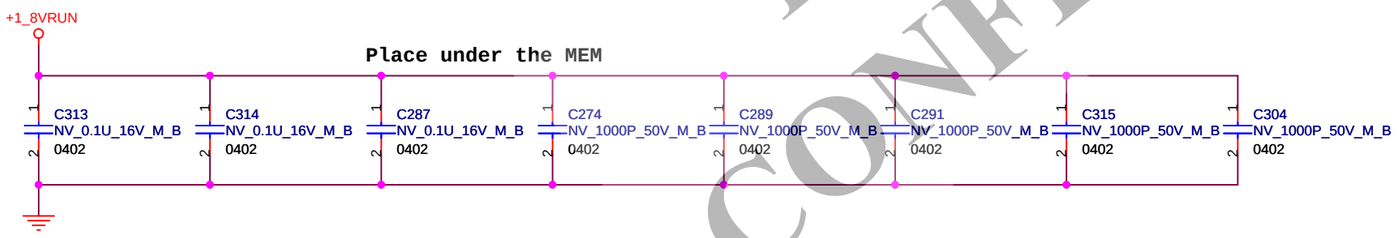


Decoupling for left MEMORY

Place around the MEM



Place under the MEM



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***VRAM(POWERBYPASS)***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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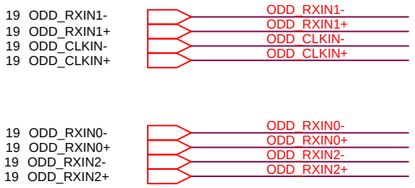
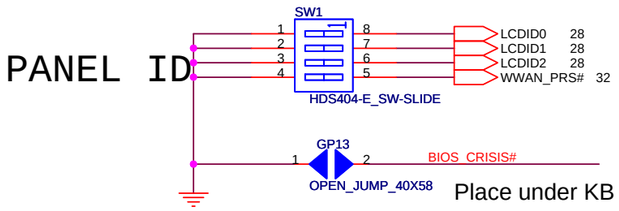
LVDS

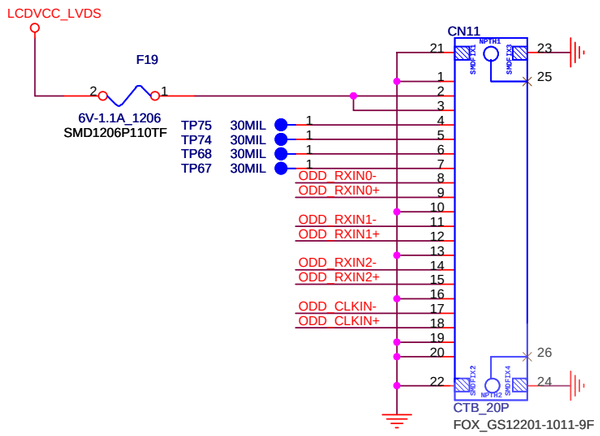


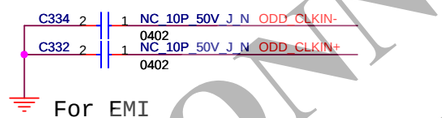
PANEL ID

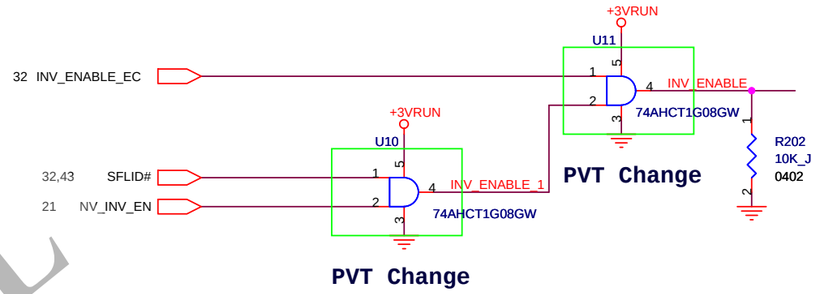


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

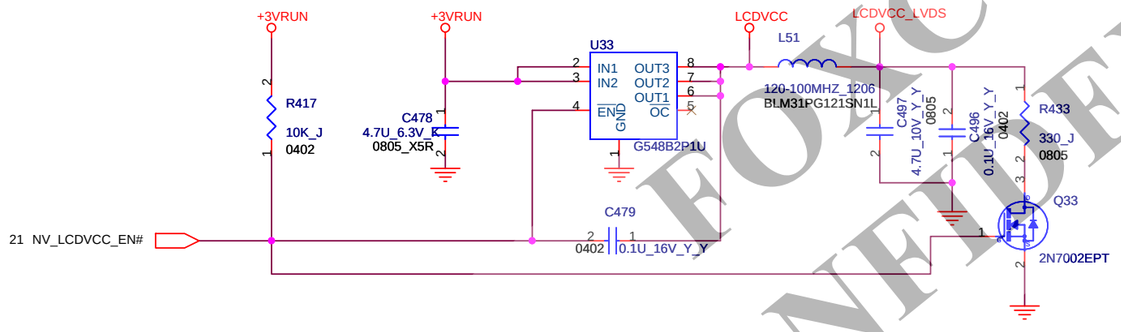
LVDS CONNECTOR

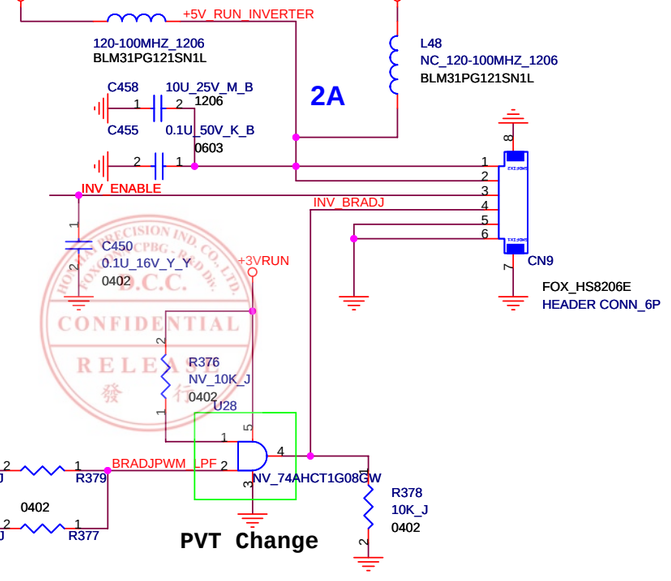




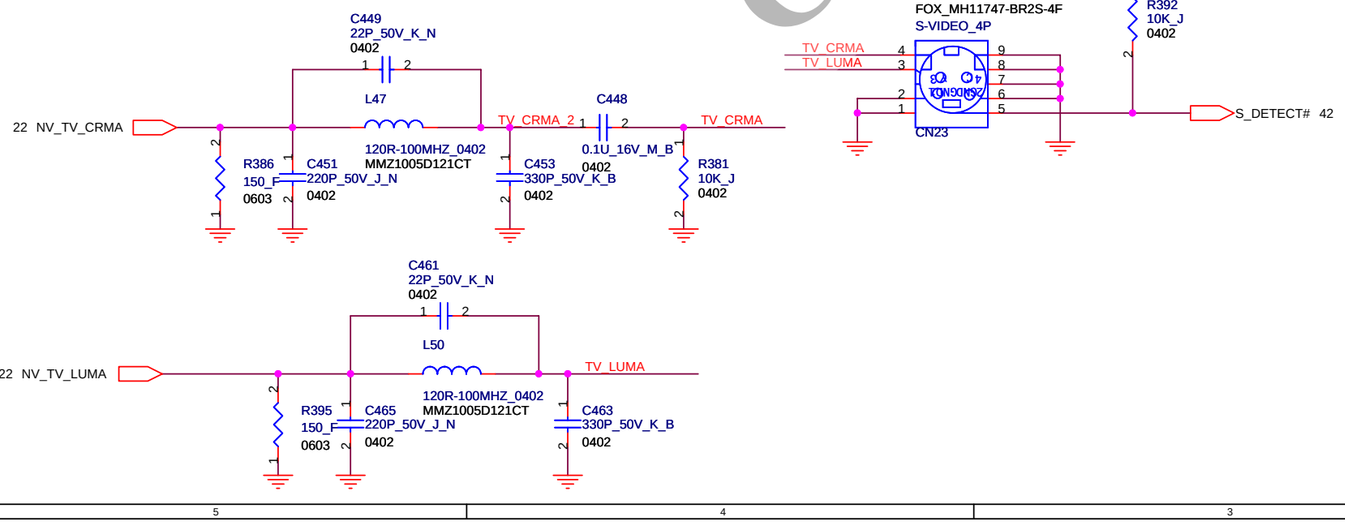


LCD POWER





S-VIDEO



INVERTER CONNECTOR

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*LVDS / S_VIDEO*	
Size: Custom	Document Number: MS60-1-01 (MBX-159)	Rev: 1.0
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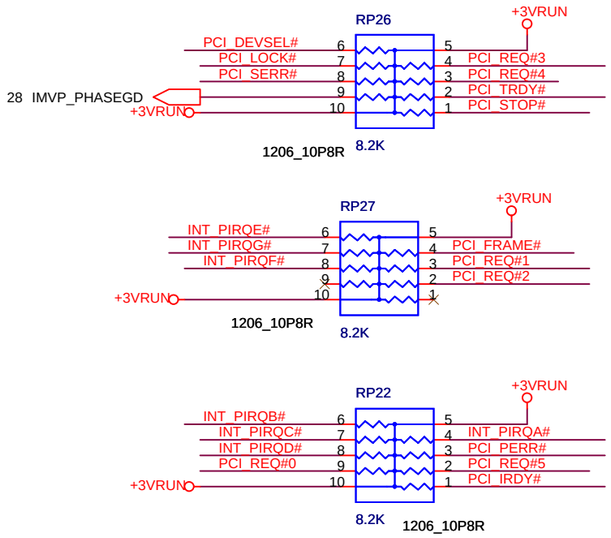
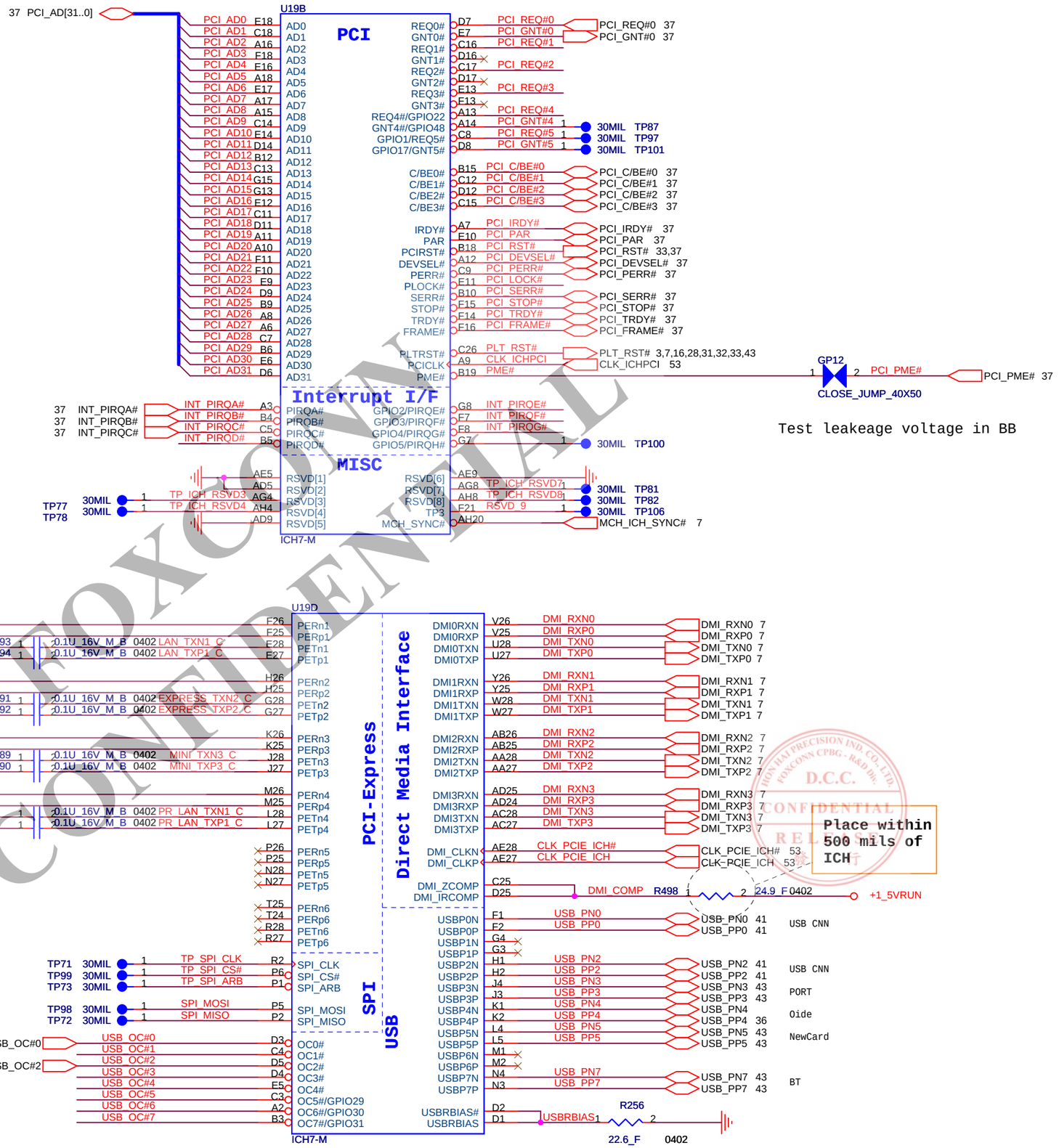


PCI Pullups



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	ICH7-M(PCI/DMI/USB/PCIE) 1/5	
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RTCRST#

VccRTC

Min : 5ms

The traces inside this block should be wider.
No digital signals routed under XTAL

+ECVCC
D5
CH500H-40PT
VCCRTC
C396 1U_6.3V_M_B 0402
32.768KHZ_12.5P_10PPM Q13MC3061001800
Y1
C340 15P_50V_K_N 0402 CLK_32KX1
C339 15P_50V_K_N 0402 CLK_32KX2
6 mils
R255 10M_J 0402
R428 20K_J 0402
C493 1U_25V_K_B 0603
R290 1M_J 0402
R291 510_F 0402
R292 510_F 0402
CN17
A3504
HEADER_2P FOX_HS8202E

U19A

RTCX1 AB1
RTCX2 AB2
RTCRST# AA3
INTRUDER# Y5
INTVRMEN W4
EE_CS W1
EE_SHCLK Y1
EE_DOUT Y2
EE_DIN W3
LAN_CLK V3
LAN_RSTSYNC U3
LAN_RXD0 U5
LAN_RXD1 V4
LAN_RXD2 T5
LAN_TXD0 U7
LAN_TXD1 V6
LAN_TXD2 V7
ACZ_BIT_CLK U1
ACZ_SYNC R6
ACZ_RST# R5
ACZ_SDIN0 T2
ACZ_SDIN1 T3
ACZ_SDIN2 T1
ACZ_SDOUT T4
SATALED# AE18
SATA0RXN AE3
SATA0RXP AE3
SATA0TXN AG2
SATA0TXP AH2
SATA2RXN AF7
SATA2RXP AE7
SATA2TXN AG6
SATA2TXP AH6
SATA_CLKN AF1
SATA_CLKP AE1
SATARBIASN AH10
SATARBIASP AG10
DIOR# AE15
DIOW# AH15
DDACK# AE16
IDEIRQ AH16
IORDY AG16
DDREQ AE15

RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE

ICH7-M

LAD0 AA6 LPC_AD0 → LPC_AD0 32,33
LAD1 AB5 LPC_AD1 → LPC_AD1 32,33
LAD2 AC4 LPC_AD2 → LPC_AD2 32,33
LAD3 Y6 LPC_AD3 → LPC_AD3 32,33
LDRQ0# AC3 LPC_DRQ#0 → LPC_DRQ#0 33
LDRQ1#/GPIO23 AA5
LFRAME# AB3 LPC_FRAME# → LPC_FRAME# 32,33
A20GATE AE22 H_A20GATE
A20M# AH28 H_A20M# → H_A20M# 3
CPUSLP# AG27 TP_CPUSLP# 1 — 30MIL TP91
TP1/DPRSTP# AE24 — R497 1 0_J 2 0402 → H_DPRSTP# 4,48
TP2/DPSLP# AH25 — R496 1 0_J 2 0402 → H_DPSLP# 4
FERR# AG26 — R503 1 2 56_J 0402 +1_05VRUN → H_FERR# 3
GPIO49/CPUPWRGD AG24 H_PWRGD → H_PWRGD 4
IGNNE# AG22 H_IGNNE# → H_IGNNE# 3
INIT3_3V# AG21 FWH_INIT# → FWH_INIT# 33
INIT# AF22 H_INIT# → H_INIT# 3
INTR AF25 H_INTR → H_INTR 3
RCIN# AG23 H_RCIN#
NMI AH24 H_NMI → H_NMI 3
SMI# AF23 H_SMI# → H_SMI# 3
STPCLK# AH22 H_STPCLK# → H_STPCLK# 3
THERMTRIP# AF26 PM_THRMTRIP# 1

DD0 AB15 IDE_PDD0
DD1 AE14 IDE_PDD1
DD2 AG13 IDE_PDD2
DD3 AE13 IDE_PDD3
DD4 AD14 IDE_PDD4
DD5 AC13 IDE_PDD5
DD6 AD12 IDE_PDD6
DD7 AC12 IDE_PDD7
DD8 AE12 IDE_PDD8
DD9 AE12 IDE_PDD9
DD10 AB13 IDE_PDD10
DD11 AC14 IDE_PDD11
DD12 AE14 IDE_PDD12
DD13 AH13 IDE_PDD13
DD14 AH14 IDE_PDD14
DD15 AC15 IDE_PDD15
IDE_PDD[0..15] → IDE_PDD[0..15] 31
DA0 AH17 IDE_PDA0 → IDE_PDA0 31
DA1 AE17 IDE_PDA1 → IDE_PDA1 31
DA2 AE17 IDE_PDA2 → IDE_PDA2 31
DCS1# AE16 IDE_PDCS1# → IDE_PDCS1# 31
DCS3# AD16 IDE_PDCS3# → IDE_PDCS3# 31

+3VRUN
R516 0_J 0402
43 IAC_BITCLK → IAC_BITCLK_ICH
43 IAC_SYNC → IAC_SYNC
43 IAC_RESET# → IAC_RESET#
43 ACZ_SDATAIN0 → ACZ_SDATAIN0
43 ACZ_MDC_SDATAIN1 → ACZ_MDC_SDATAIN1
TP_ACZ_SDIN2 30MIL
TP70
43 IAC_SDATAO → IAC_SDATAO
R460 NC_10K_J 0402
43 SATA_LED#

+3VRUN
R490 10K_J 0402
R492 10K_J 0402
H_RCIN# → EC_H_RCIN# 32
Q31 2N7002EPT
Q30 2N7002EPT
R482 H_A20GATE 8.2K_J 0402 → EC_H_A20GATE 32

+1_05VRUN
R502 56_J 0402

31 SATA_RXN0 → C491 3900P_25V_K_B0603 → SATA_RXN0_C
31 SATA_RXP0 → C490 3900P_25V_K_B0603 → SATA_RXP0_C
31 SATA_TXN0 → C488 3900P_25V_K_B0603 → SATA_TXN0_C
31 SATA_TXP0 → C489 3900P_25V_K_B0603 → SATA_TXP0_C
TP79 30MIL
TP80 30MIL
SATA_TXN2
SATA_TXP2
53 CLK_PCIE_SATA#
53 CLK_PCIE_SATA
R445 24.9_F 0402 A3502

31 IDE_PDIOR# → IDE_PDIOR#
31 IDE_PDIOW# → IDE_PDIOW#
31 IDE_PDDACK# → IDE_PDDACK#
31 INT_IRQ14 → INT_IRQ14
31 IDE_PDIORDY → IDE_PDIORDY
31 IDE_PDDREQ → IDE_PDDREQ

VCCRTC
R437 332K_F 0402
INTVRMEN

Pull-up to enable internal VccSus1_05 regular
Pull-Low to disable

Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division

Title: ICH7-M(LPC,IDE,SATA) 2/5

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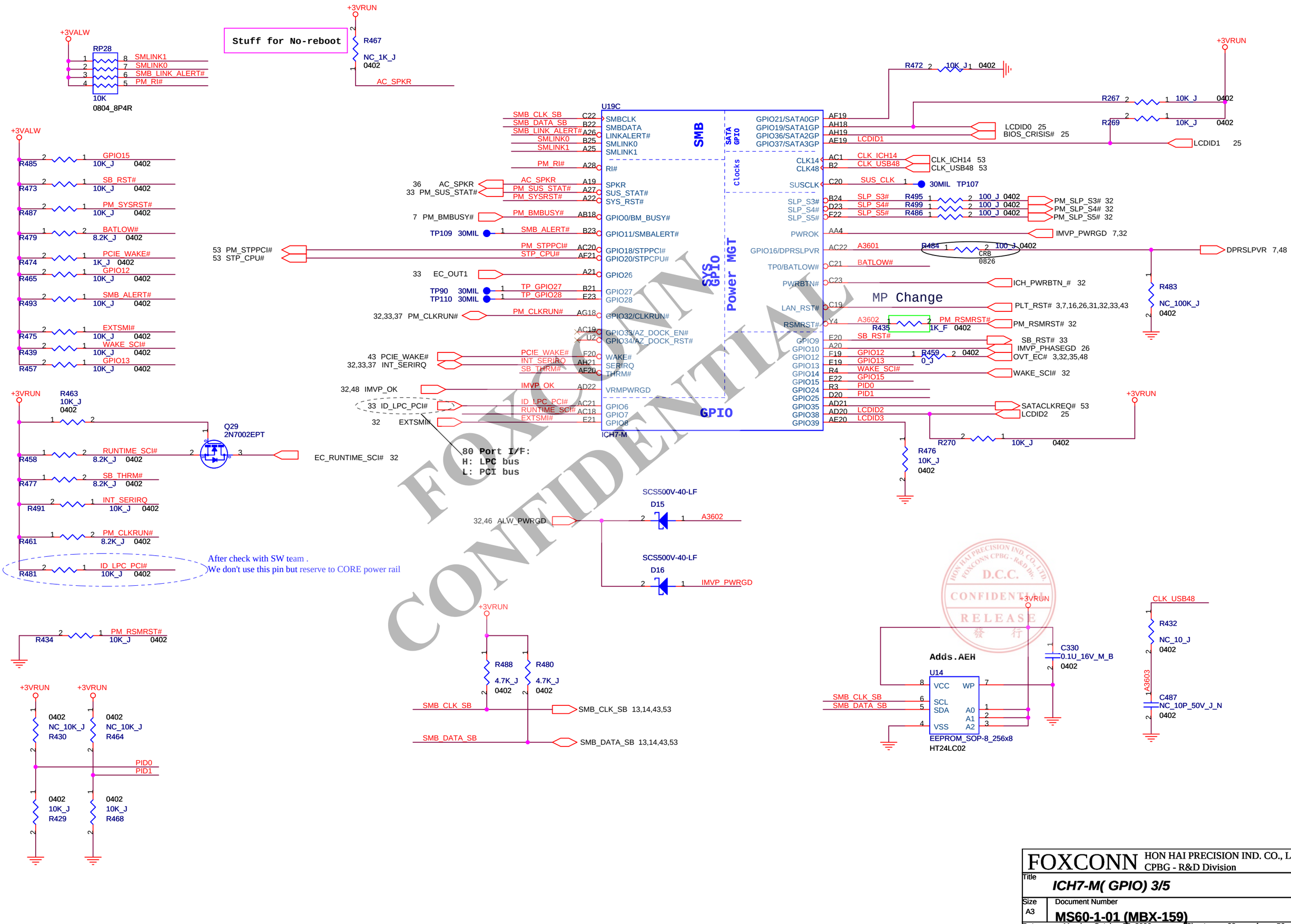
+3VALW
RP28
SMLINK1
SMLINK0
SMB_LINK_ALERT#
PM_RI#
10K
0804_8P4R
Stuff for No-reboot
+3VRUN
R467
NC_1K_J
0402
AC_SPKR
U19C
SMB
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
ICH7-M
SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
Clocks
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
Power MGT
SYS GPIO
GPIO
SMB_CLK_SB
SMB_DATA_SB
LINK_ALERT#
SMLINK0
SMLINK1
PM_RI#
AC_SPKR
PM_SUS_STAT#
PM_SYSRST#
PM_BMBUSY#
SMB_ALERT#
PM_STPPCI#
STP_CPU#
EC_OUT1
TP_GPIO27
TP_GPIO28
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
SB_THRM#
IMVP_OK
ID_LPC_PCI#
RUNTIME_SCI#
EXTSMI#
R472 10K_J 0402
R267 10K_J 0402
R269 10K_J 0402
LCDID0 25
BIOS_CRISIS# 25
LCDID1 25
CLK_ICH14
CLK_USB48
SUS_CLK
30MIL TP107
SLP_S3# R495 100_J 0402
SLP_S4# R499 100_J 0402
SLP_S5# R486 100_J 0402
PM_SLP_S3# 32
PM_SLP_S4# 32
PM_SLP_S5# 32
IMVP_PWRGD 7,32
A3601
R484 100_J 0402 CRB 0826
DPRSLPVR 7,48
BATLOW#
ICH_PWRBTN_# 32
R483
NC_100K_J
0402
MP Change
PLT_RST# 3,7,16,26,31,32,33,43
A3602
R435 1K_F 0402
PM_RSMRST# 32
SB_RST# 33
IMVP_PHASEGD 26
R459 0_J 0402
OVT_EC# 3,32,35,48
WAKE_SCI# 32
PID0
PID1
SATACLKREQ# 53
LCDID2 25
LCDID3
R270 10K_J 0402
R476 10K_J 0402
SCS500V-40-LF
D15
A3602
D16
IMVP_PWRGD
R488 4.7K_J 0402
R480 4.7K_J 0402
SMB_CLK_SB 13,14,43,53
SMB_DATA_SB 13,14,43,53
Adds.AEH
U14
VCC
WP
SCL
SDA
A0
A1
A2
VSS
EEPROM_SOP-8_256x8
HT24LC02
C330 0.1U_16V_M_B 0402
CLK_USB48
R432
NC_10_J
0402
A3603
C487 NC_10P_50V_J_N 0402
R463 10K_J 0402
Q29
2N7002EPT
RUNTIME_SCI# 8.2K_J 0402
SB_THRM# 8.2K_J 0402
INT_SERIRQ 10K_J 0402
PM_CLKRUN# 8.2K_J 0402
ID_LPC_PCI# 10K_J 0402
EC_RUNTIME_SCI# 32
80 Port I/F:
H: LPC bus
L: PCI bus
After check with SW team .
We don't use this pin but reserve to CORE power rail
R485 GPIO15 10K_J 0402
R473 SB_RST# 10K_J 0402
R487 PM_SYSRST# 10K_J 0402
R479 BATLOW# 8.2K_J 0402
R474 PCIE_WAKE# 1K_J 0402
R465 GPIO12 10K_J 0402
R493 SMB_ALERT# 10K_J 0402
R475 EXTSMI# 10K_J 0402
R439 WAKE_SCI# 10K_J 0402
R457 GPIO13 10K_J 0402
R434 PM_RSMRST# 10K_J 0402
R430 0402 NC_10K_J
R464 0402 NC_10K_J
R429 0402 10K_J
R468 0402 10K_J
FOXCONN CONFIDENTIAL
HON HAI PRECISION IND. CO., LTD. FOXCONN CPBG - R&D DIV. D.C.C. CONFIDENTIAL RELEASE 發行
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title ICH7-M(GPIO) 3/5
Size A3
Document Number MS60-1-01 (MBX-159)
Rev 1.0
Date: Monday, October 02, 2006
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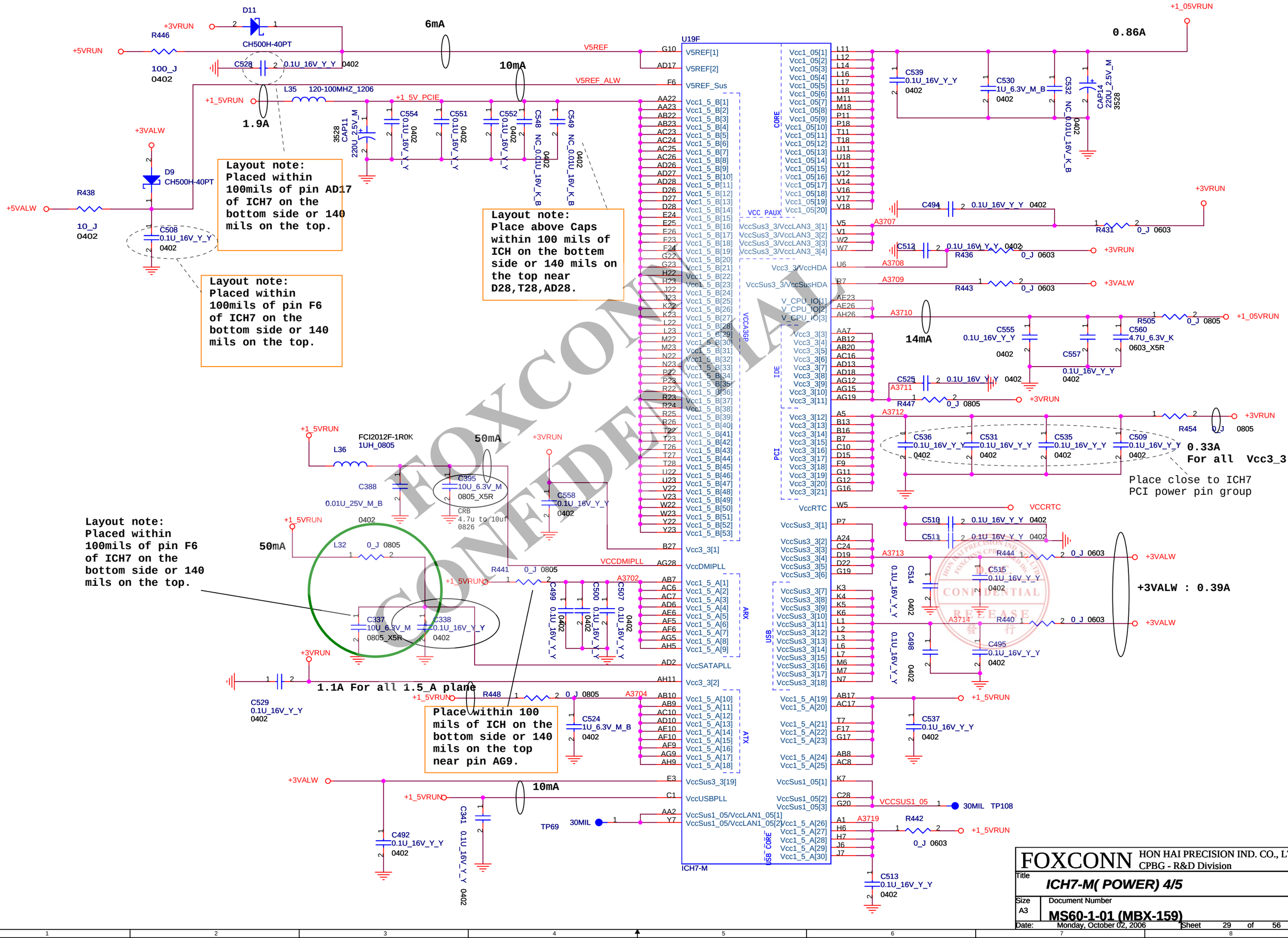
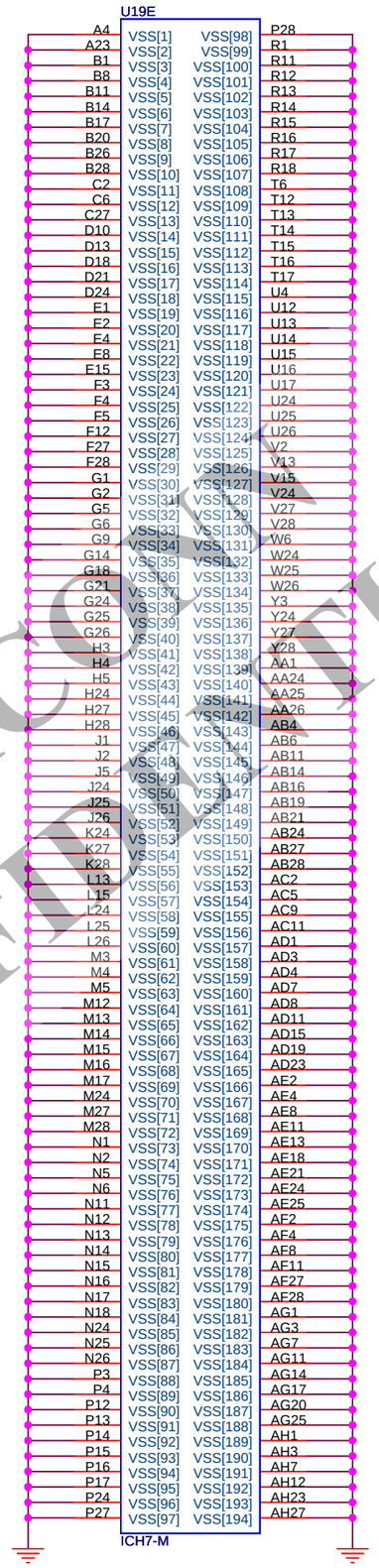


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ICH7-M(POWER) 4/5

Size	Document Number	Rev
A3	MS60-1-01 (MBX-159)	1.0

Date: Monday, October 02, 2006 Sheet 29 of 56



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***ICH7-M(GND) 5/5***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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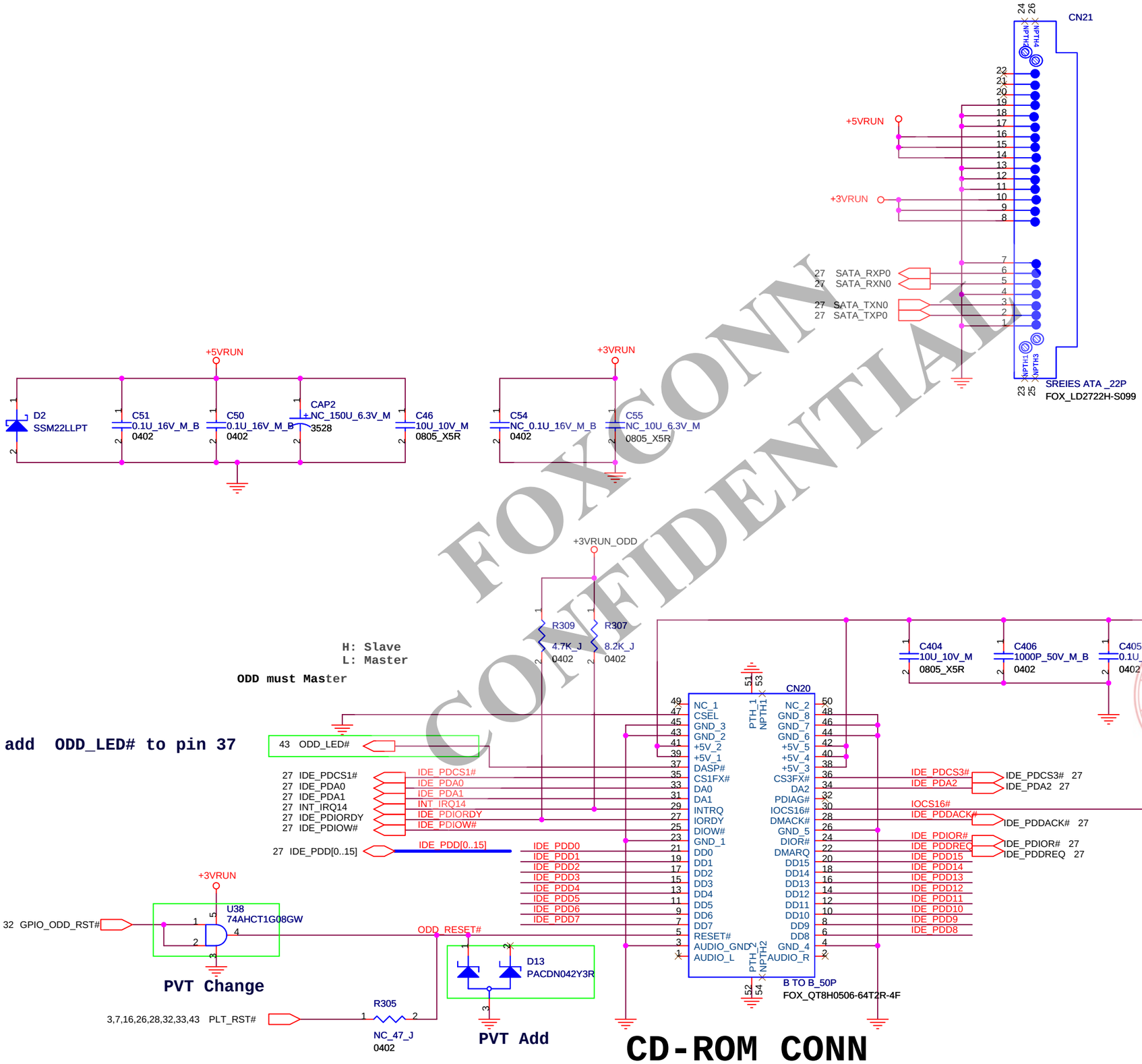
SATA HDD CONN



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*SATA HDD/CD-ROM*	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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Consider short FB after BB test.

FOX_GB21240-0002-7F
FPC CONN_24P
CN4

RP1 10K 0804_8P4R

U16

FOR EMI

PVT Change

PVT Add

MODEL ID check with software define

M-ID	0	1	2	3	4	5	
MS60-L	1	0	1	1	1	0	940GML
MS60-H	0	1	1	1	1	0	945PM
MS60-M	1	1	1	1	1	0	945GM
MS61-L	1	0	0	1	1	0	940GML
MS61-H	0	1	0	1	1	0	945PM
MS61-M	1	1	0	1	1	0	945GM

M-ID 5: 0- MS60 and the following MS60 type
1- MS70 and the following MS70 type
M-ID 2~4: 1- Reserved
M-ID 1: 0- Intel 940 series
1- Intel 945 series
M-ID 0: 0- External Gfx.
1- Internal Gfx.

M-ID3: 0- MS61 type

MP Add

PDTC144EU Q5

WLAN_LED# 43

WLAN_EN

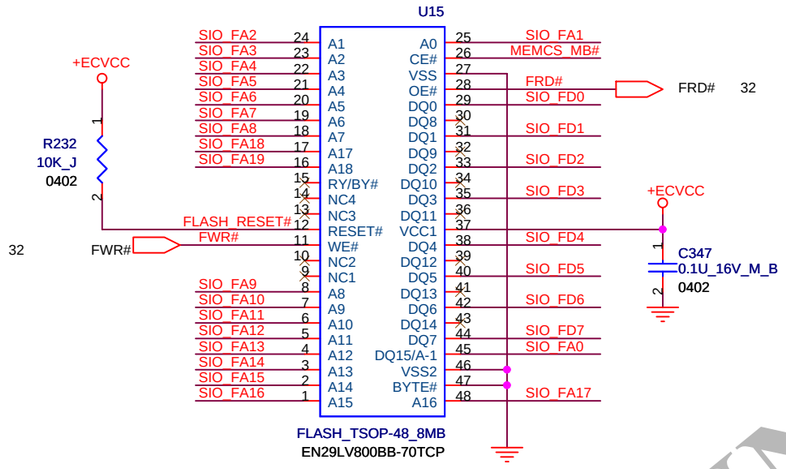
MP Add

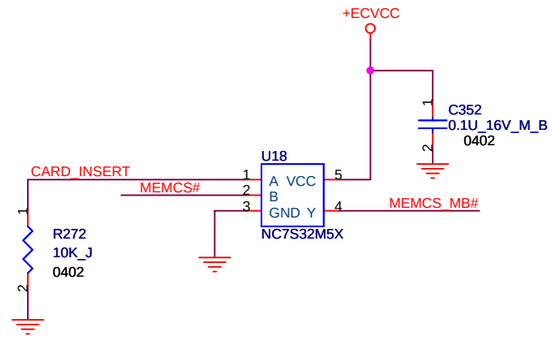
FPC_12P
FOX_GB5RF120-1200-7F

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	EC+KBC
Size	A2
Document Number	MS60-1-01 (MBX-159)
Rev	1.0
Date:	Monday, October 02, 2006
Sheet	32 of 56

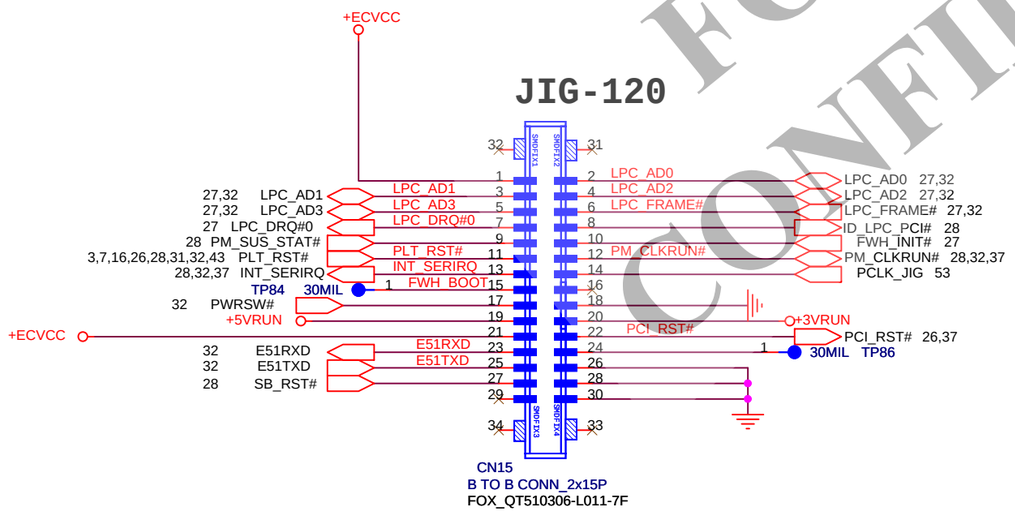
32 SIO_FA[19..0]

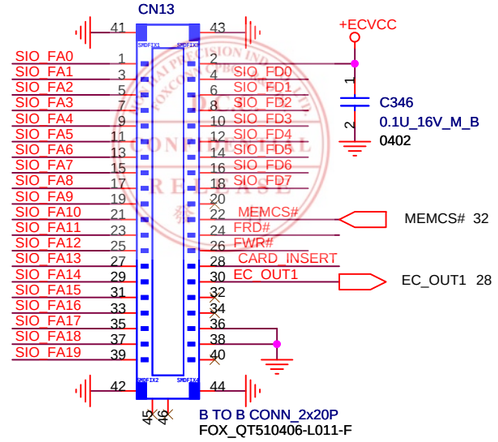
32 SIO_FD[7..0]





BIOS ROM





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***Flash ROM/X-Bus CONN***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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WWAN FOR MS60-L ONLY !!

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***WWAN***	
Size: Custom	Document Number: **MS60-1-01 (MBX-159)**	Rev: 1.0
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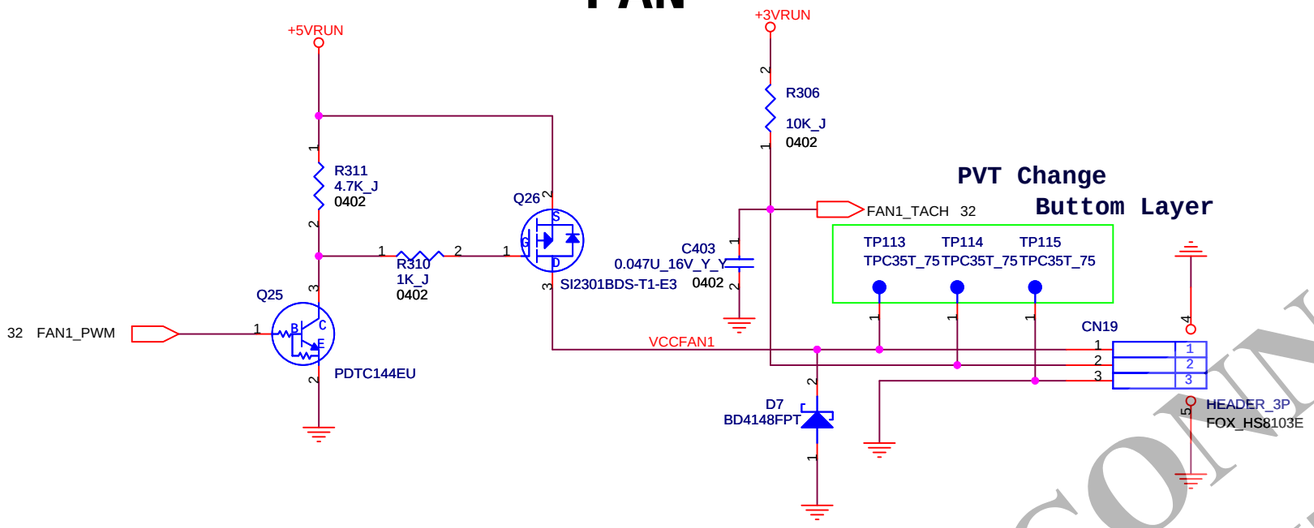
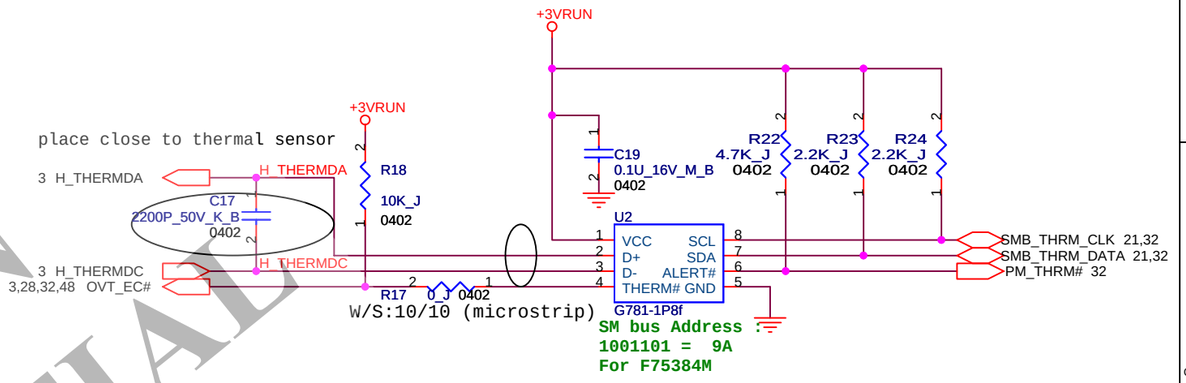
FAN

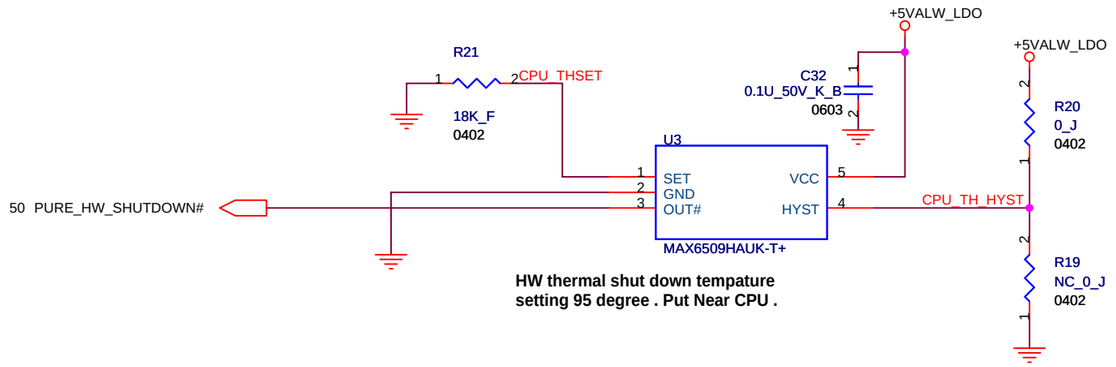


CPU SENSOR



Place Thermal-Sensor near CPU & GMCH.

HW THERMAL PROTECTION



HW thermal shut down tempature setting 95 degree . Put Near CPU .

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***FAN/HW THERMAL PROTECT***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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PC BEEP

+3VRUN

U1
MC74VHC1G86DFT2G

28 AC_SPKR
37 CB_SPKOUT

C10
0.1U_16V_Y_Y
0402

R12
10K_J
0402

Q4

D1
MMHZ5234BPT

For ESD
Second source

+5VRUN

Q3
CHDTA114YUPT

R4
10K_J
0402

C5
1U_10V_K
0603

PDTC144EU

R3
2.2K_J
0402

C2
3300P_50V_K_B
0402

PC_SPKRIN 43

32
32

TP

+5VRUN

F17
6V-1.1A_1206
SMD1206P110TF

0.047U_16V_Y
C48
0402_Y5V

0402
10K_J
R312

0402
10K_J
R313

0402C47
0.1U_16V_Y_Y

FPC_12P
FOX_GB5RF120-1200-7F
CN8

L41 120R-100MHZ_0603
HCB1608KF-121T25

L40 120R-100MHZ_0603
HCB1608KF-121T25

DAT_TP
CLK_TP

C408
47P_50V_K
0402_NPO

C411
47P_50V_K
0402_NPO

LEFT#
RIGHT#

R314
NC_0_J
0402

R47
0_J
0402

PVT Change reverse 180

+5VRUN

F16
NC_6V-1.1A_1206
SMD1206P110TF

OIDE stuff

10mils

PVT Change
Buttom Layer

TP120 TPC35T_75
TP121 TPC35T_75
TP122 TPC35T_75
TP123 TPC35T_75

OIDE

CN7

R44
NC_0_J
0603

L1
NC_90R-100MHZ_0R35
1206

L37
NC_120R-100MHZ_0402
MMZ1005D121CT

R45
NC_0_J
0603

C412
NC_22U_10V_Y_Y
1206

C409
NC_1U_10V_Y_Y
0603

C410
NC_470P_50V_K_B
0402

26 USB_PN4
26 USB_PP4

HUB_VCC1_F
HUB_PN1_F
HUB_PP1_F

NC_FPC_6P
FOX_GB5RF060-1200-7F

T_SW1
1BT002-0120L_SW-TACT

T_SW2
1BT002-0120L_SW-TACT

T_D1
NC_PACDN042Y3R

T_D2
NC_PACDN042Y3R

LEFT#
RIGHT#

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: OIDE/TP

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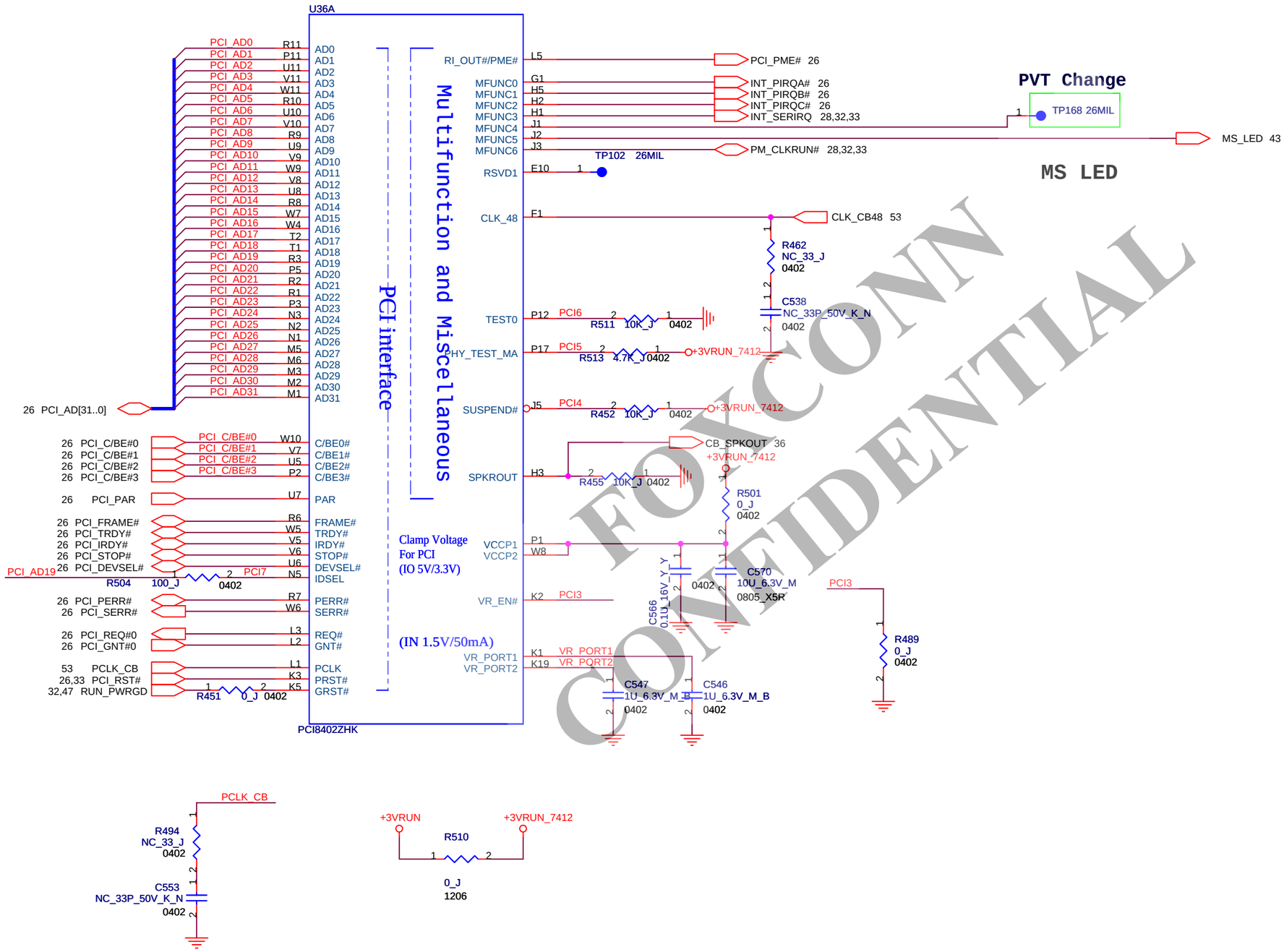

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *PCI (PCI BUS)*

Size	Document Number	Rev
A3	MS60-1-01 (MBX-159)	1.0

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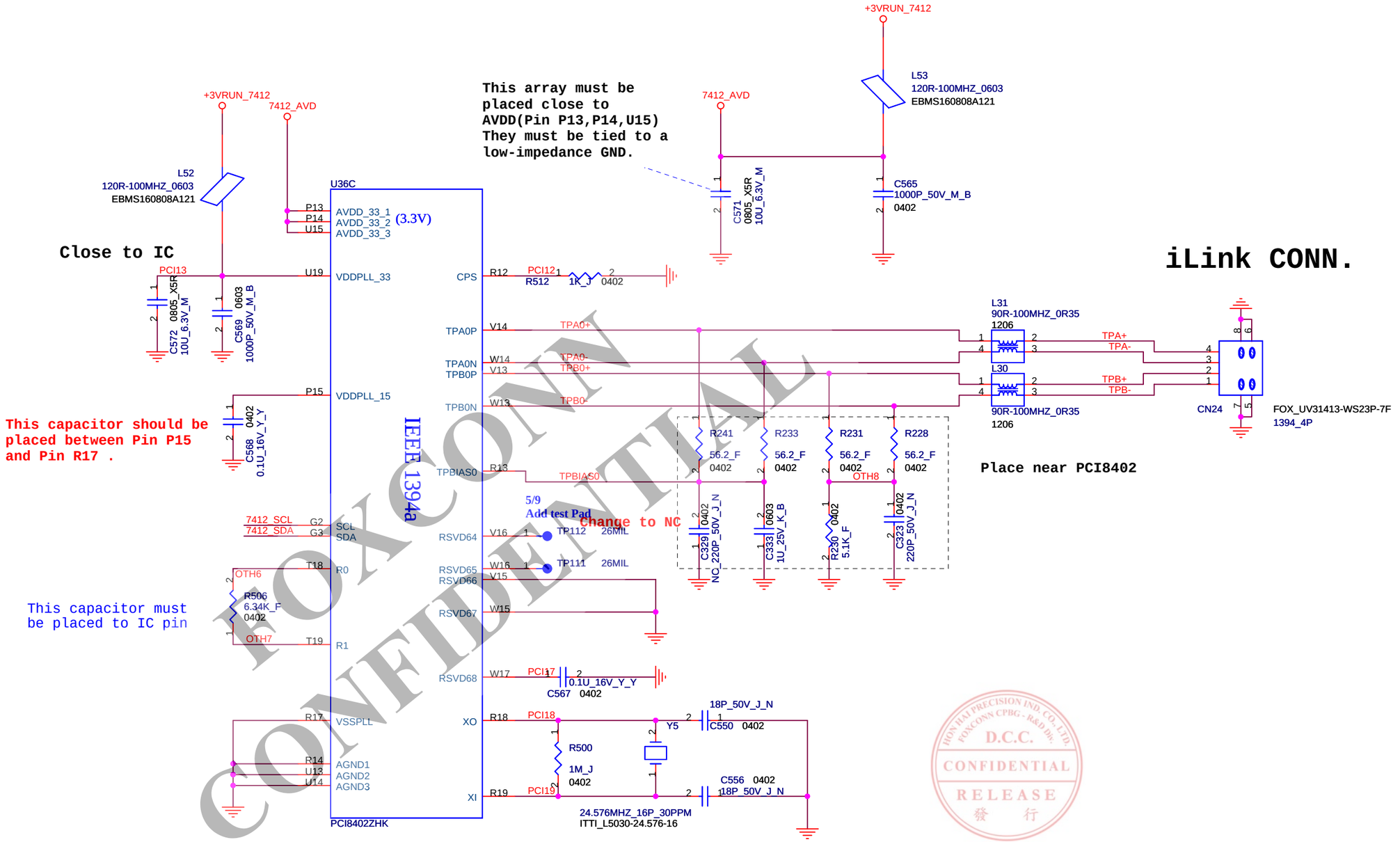

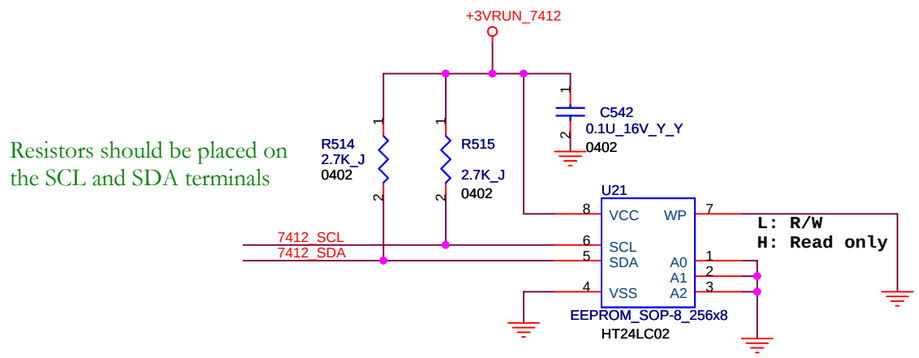

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (ILINK)	
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 1.0
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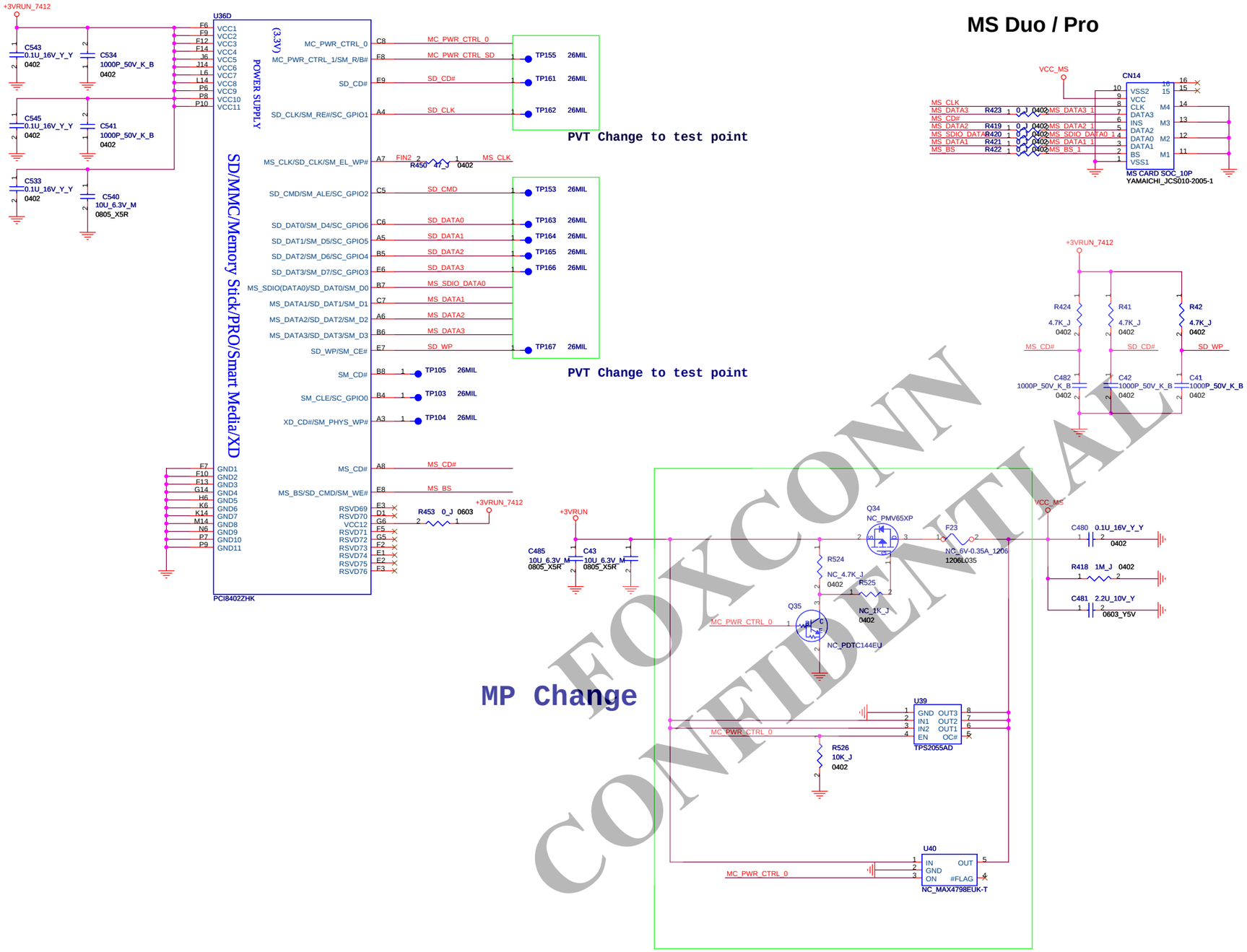
MS Duo / Pro



MP Change

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (MS)	
Size A2	Document Number MS60-1-01 (MBX-159)	Rev 1.0
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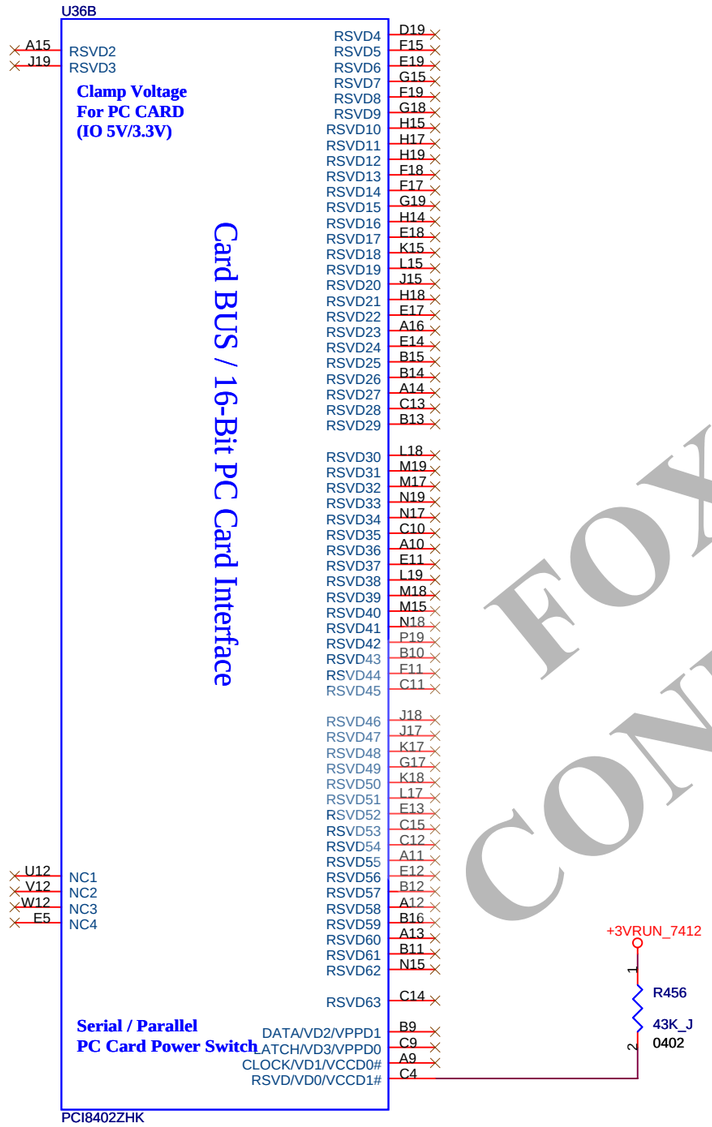

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***PCI (PCMCIA)***	
Size A3	Document Number **MS60**	Rev 1.0
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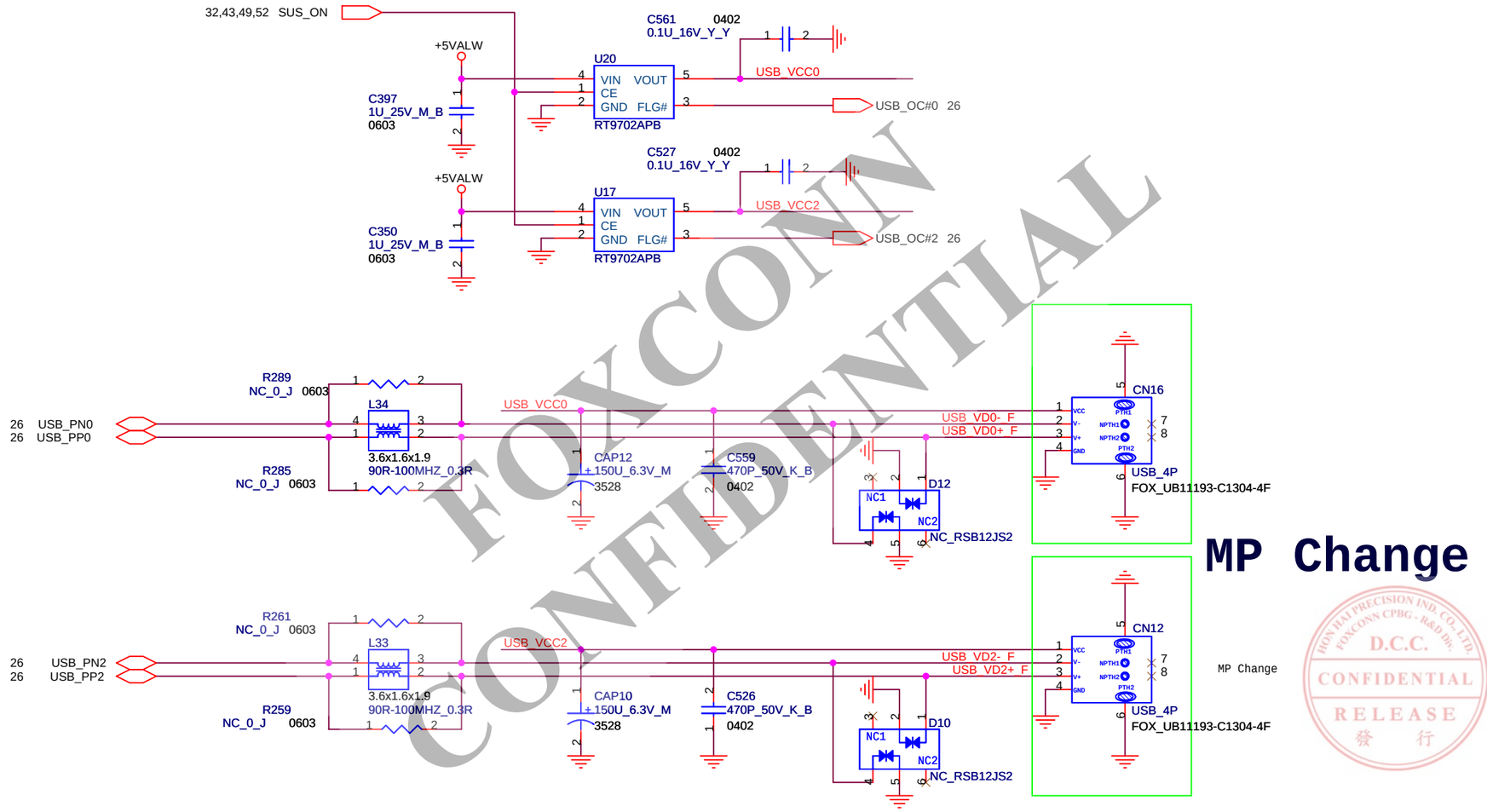

MP Change

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***USB2.0/DOCKING CONN.***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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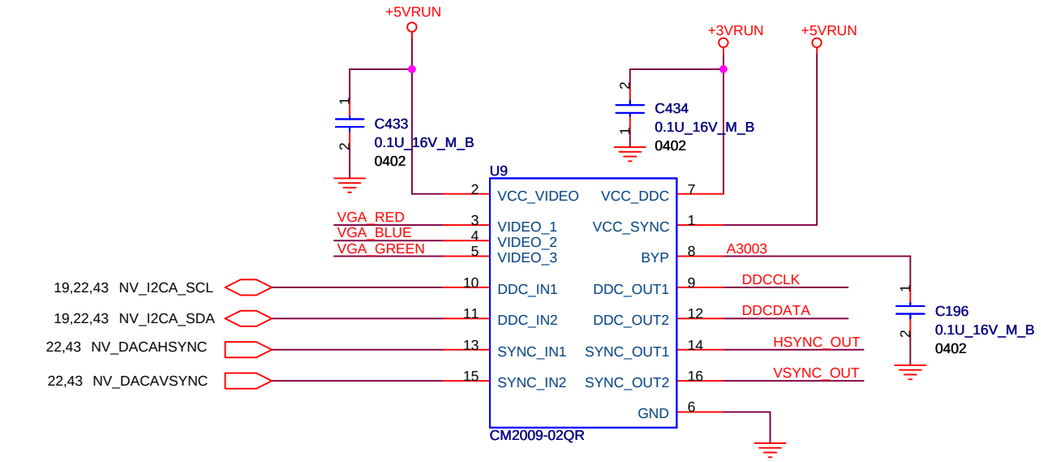

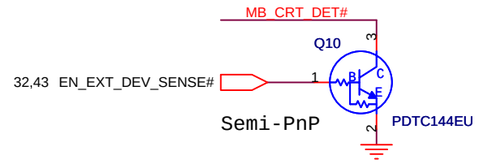

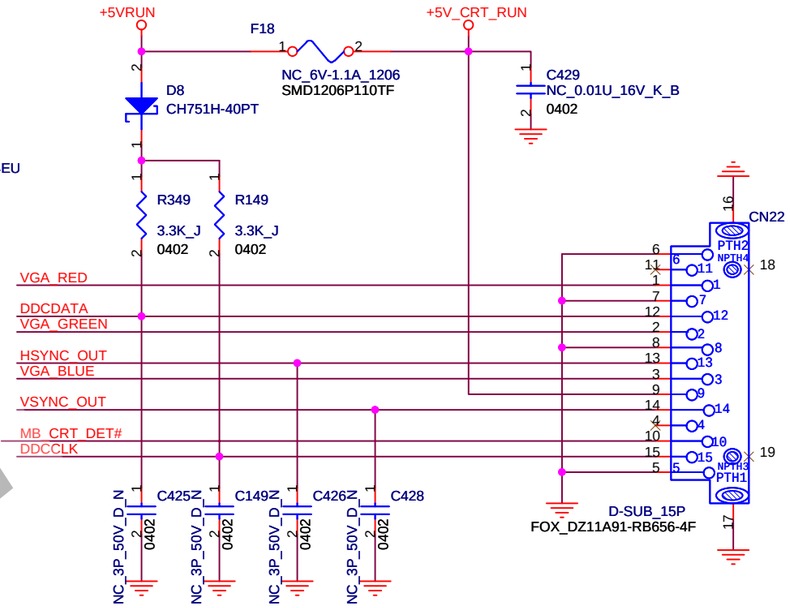

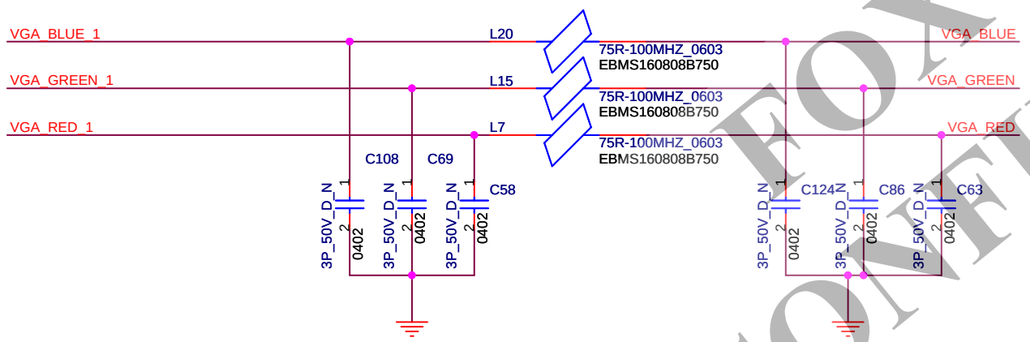

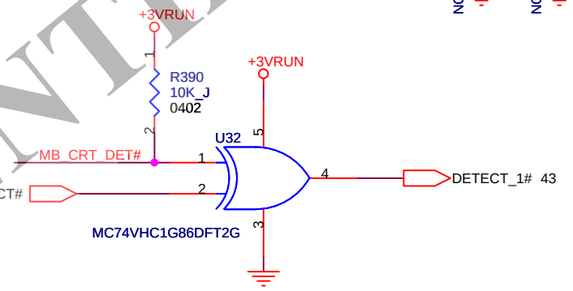

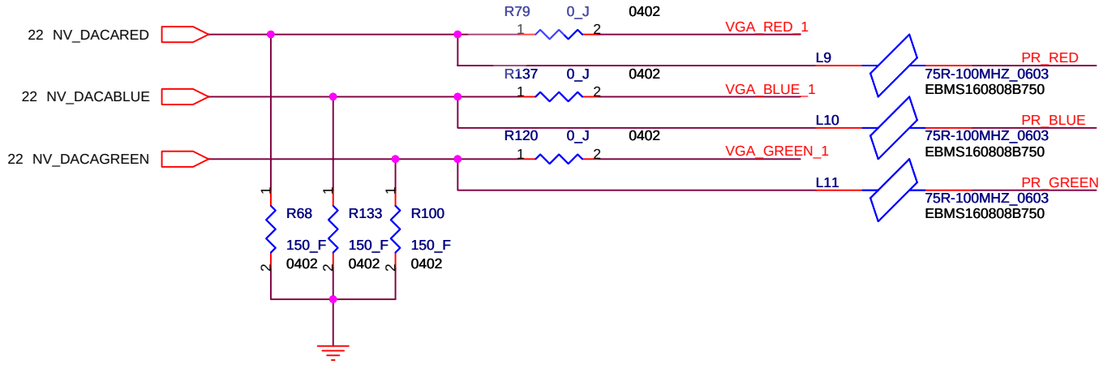

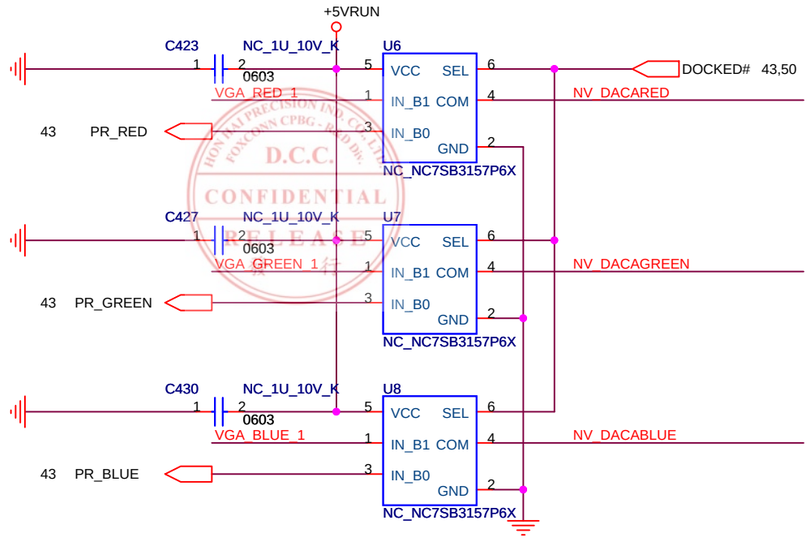

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CRT	
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 1.0
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MP Change

Amber / Green

LED2 HT-210D/YG

R296 60.4_F 0402

R297 60.4_F 0402

Q22 PDTC144EU

Q24 PDTC144EU

32 SUSPEND_LED

32 POWER_LED

Yellow

LED5 HT-110UY

Q21 PDTC144EU

37 MS_LED

R295 150_F 0402

Q20 CHDTA114YUPT

27 SATA_LED#

R294 150_F 0402

Yellow

LED4 HT-110UY

Q23 CHDTA114YUPT

32 BTY_LED#

R298 150_F 0402

Yellow

LED3 HT-110UY

+1_5VRUN +5VALW

F8 6V-1.1A_1206 SMD1206P110TF

F9 6V-1.1A_1206 SMD1206P110TF

CN2 FFC_26P FOX_GB11261_1051_7F

26 LAN_RXP1
26 LAN_RXN1
26 LAN_TXN1
26 LAN_TXP1
53 CLK_PCIE_LAN
53 CLK_PCIE_LAN#
53 CLK_PCIE_MINI#
53 CLK_PCIE_MINI
26 MINI_RXN3
26 MINI_RXP3
26 MINI_TXN3
26 MINI_TXP3
WIRELESS_DATA
WIRELESS_CHCLK
32 WLAN_EN
PCIE_WAKE#

PVT Change to GB11261_1051_7F

+3V_S3_SUS +5VRUN +3VALW +3VRUN

F1 6V-1.1A_1206 SMD1206P110TF

F2 6V-1.1A_1206 SMD1206P110TF

F6 6V-1.1A_1206 SMD1206P110TF

F7 6V-1.1A_1206 SMD1206P110TF

CN1 FFC_26P FOX_GB11261_1051_7F

32 VISTA_SUPPORT#
53 MINI_CARD_DET#
32 WLAN_LED#
PLT_RST#
27 IAC_BITCLK
27 IAC_SYNC
27 IAC_RESET#
27 ACZ_SDATAIN0
27 ACZ_MDC_SDATAIN1
27 IAC_SDATAO
32 HW_POP_MUTE_EC
36 PC_SPKRIN

PVT Change to GB11261_1051_7F

+3VRUN_ODD

R522 10K_J 0402

Q19 CHDTA114YUPT

31 ODD_LED#

2N7002EPT Q32

PVT Change

R315 150_F 0402

Yellow

LED1 HT-110UY

+3VRUN

R304 10K_J 0402

U23 MC74VHC1G86DFT2G

42 DETECT_1#

DOCK_SEMI_PNP#

VGA_CRT_DET# 32

PVT Change to NC

+1_5VRUN +3VRUN +3VALW

F10 6V-1.1A_1206 SMD1206P110TF

F21 6V-1.1A_1206 SMD1206P110TF

F22 6V-1.1A_1206 SMD1206P110TF

PVT Add

CN5 FFC_26P FOX_GB11261_1051_7F

+3V_S3_SUS_1

SFLID#

WIRELESS_DATA
WIRELESS_CHCLK
3,7,16,26,28,31,32,33 PLT_RST#
32 BT_PRS#
32 BT_ON
32 BT_WLAN_SW#
26 USB_PN7
26 USB_PP7
+5VALW

F14 6V-1.1A_1206 SMD1206P110TF

PVT Change to GB11261_1051_7F

+3VRUN +3V_S3_SUS

SMD1206P110TF 6V-1.1A_1206

F11 6V-1.1A_1206 SMD1206P110TF

F13 6V-1.1A_1206 SMD1206P110TF

CN6 FFC_26P FOX_GB11261_1051_7F

+3V_S3_SUS_1

26 EXPRESS_TXP2
26 EXPRESS_TXN2
26 EXPRESS_RXP2
26 EXPRESS_RXN2
53 CLK_PCIE_EXPRESS
53 CLK_PCIE_EXPRESS#
53 EXPRESS_DET#
28 PCIE_WAKE#
13,14,28,53 SMB_DATA_SB
13,14,28,53 SMB_CLK_SB
26 USB_PP5
26 USB_PN5
32,47,51 RUN_ON1
SUS_ON
+1_5VRUN

F15 6V-1.1A_1206 SMD1206P110TF

PVT Change to GB11261_1051_7F

+3VALW

R274 100K_J 0402

SFLID# 25,32

R299 10K_J 0402

C351 0.1U_16V_M_B 0402

PORT_DET#

PR_RED
PR_GREEN
PR_BLUE

C400 10P_50V_J_N 0402

C399 10P_50V_J_N 0402

C398 10P_50V_J_N 0402

PRT_IN

C440 0.1U_16V_M_B 0402

C6 10U_25V_Y_Y 1210

CN18 B TO B_2x25P FOX_QL0125L_D24A01_5F

26 PR_LAN_TXP1
26 PR_LAN_TXN1
26 PR_LAN_RXP1
26 PR_LAN_RXN1
53 PR_CLK_PCIE_LAN
53 PR_CLK_PCIE_LAN#
PCIE_WAKE#
R2 0_J 0402
32 PR_PLT_RST#
32 UNDOCK_REQ#
42 PR_RED
42 PR_GREEN
42 PR_BLUE
32 PORT_DET#
22,42 NV_DACAHSYNC
22,42 NV_DACAVSYNC
19,22,42 NV_I2CA_SCL
19,22,42 NV_I2CA_SDA
45 PORT_DET_N

PORT_DET_P 45
INUSE_LED 32

USB HUB

USB_PN3 26
USB_PP3 26

TMDS_TX0N 19
TMDS_TX0P 19
TMDS_TX1N 19
TMDS_TX1P 19
TMDS_TX2P 19
TMDS_TX2N 19
TMDS_CLKP 19
TMDS_CLKN 19

TMDS

NV_I2CB_SCL 19,21
NV_I2CB_SDA 19,21
SUS_ON 32,41,49,52
RUN_ON 32,46,49,52
EN_EXT_DEV_SENSE# 32,42
NV_DVI_DET 21

33_J 0402 R301
33 0402 R302
DOCK_SEMI_PNP#
NC_0_J 0402 R303

Replicator Port

+5VALW

Q2 CHDTA114YUPT

Q1 PDTC144EU

PORT_DET#

D6 MMHZ5234BPT

For ESD
Second source

R1 100K_J 0402

DOCKED# 42,50

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: DB CONN & LED

Size: A2 | Document Number: MS60-1-01 (MBX-159) | Rev: 1.0

Date: Monday, October 02, 2006 | Sheet 43 of 56

Adaptor

19.5V / 90W

DCBATOUT

MAXIM

MAX8734

Switch Mode

FOR System

ON5

ON3

LDO5

LDO3

PGOOD

32,45,46 ALW_ON

ALW_ON

+5VALW/6A

32,43,46,49,52 RUN_ON

N-Channel transistor

+5VRUN/5.3A

+3VALW/6A

+5VALW_LDO

+ECVCC

ALW_PWRGD 28,32,46

SUS_ON

N-Channel transistor

+3VSUS/1.5A

RUN_ON

N-Channel transistor

+3VRUN/5.5A

RUN_ON

G923

LDO

+2_5VRUN/200mA

MAXIM

MAX1909

Battery Charger

Switch Mode

ENCHG#

DCBATOUT

MAXIM

MAX8743

Switch Mode

FOR System

32,43,47,51 RUN_ON1

ON1

ON2

PGOOD

+1_05VRUN/8A

+1_5VRUN/6.5A

RUN_PWRGD 32,37,47

RUN_ON1

GMT966

LDO

PEX_VDD(1.2V)/0.9A

MAX1616EUK+

LDO

32,41,43,49,52 SUS_ON

+8V For Load switch/30mA

DCBATOUT

INTERSIL

ISL6262

Switch Mode

FOR CPU Core

32,48 IMVP_VR_ON

VR_ON

CLKEN#

PGOOD

VHCORE/36A

CLK_EN# 48,53

IMVP_OK 28,32,48

DCBATOUT

SEMTECH

SC486

Switch Mode

1_8V_EN

0_9V_EN

EN/PSV

VTTEN

PGOOD

+1_8VSUS/14A

32,49 RUN_ON2

N-Channel MOSFET

+1_8VRUN/2A

+0_9VRUN/3A

Battery

BPS2A

Li-ion

12.6V

4800mAH

SEMTECH

SC411

Switch Mode

RUN_ON1

EN/PSV

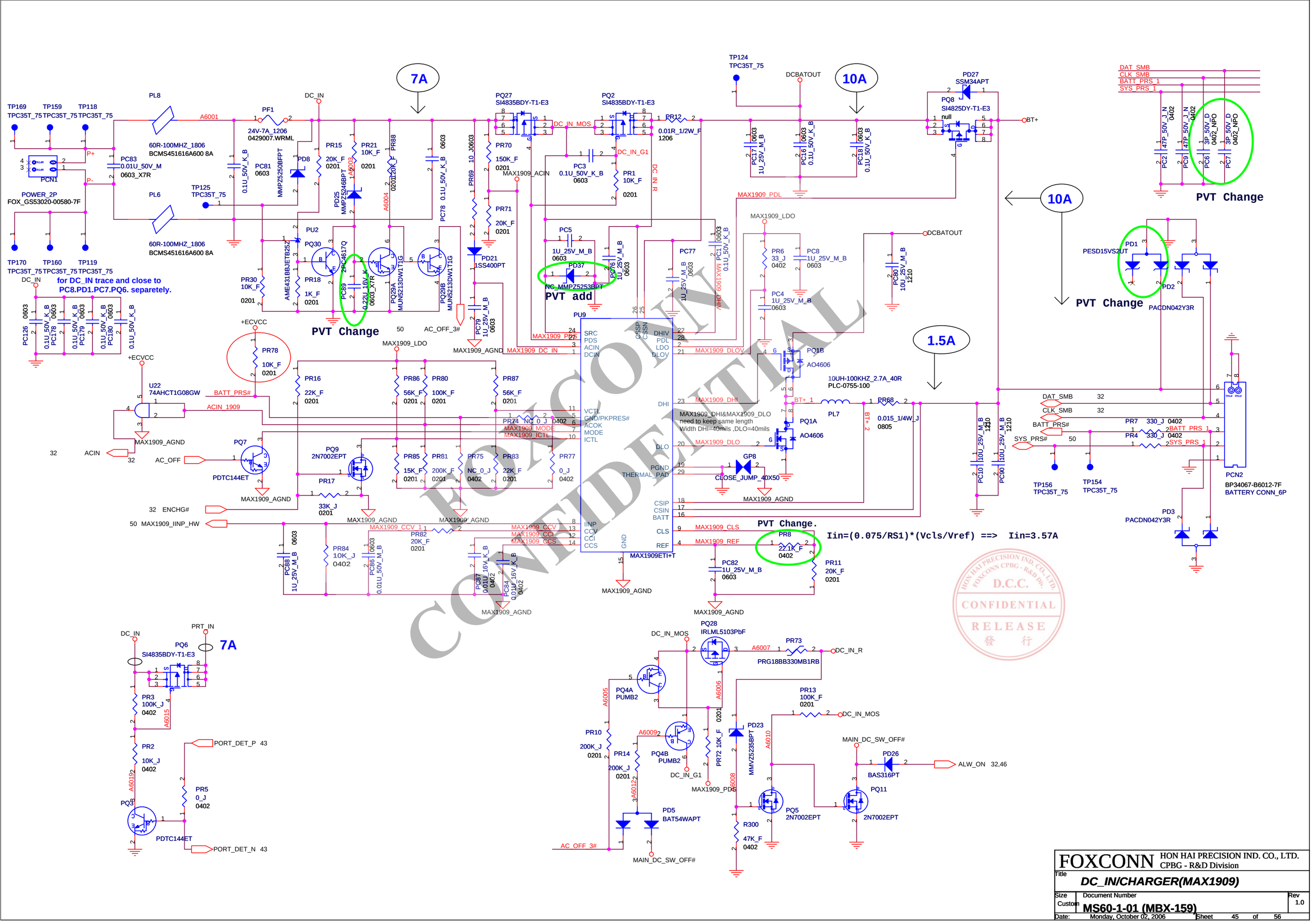
NV_VDD(1.1V)/10A

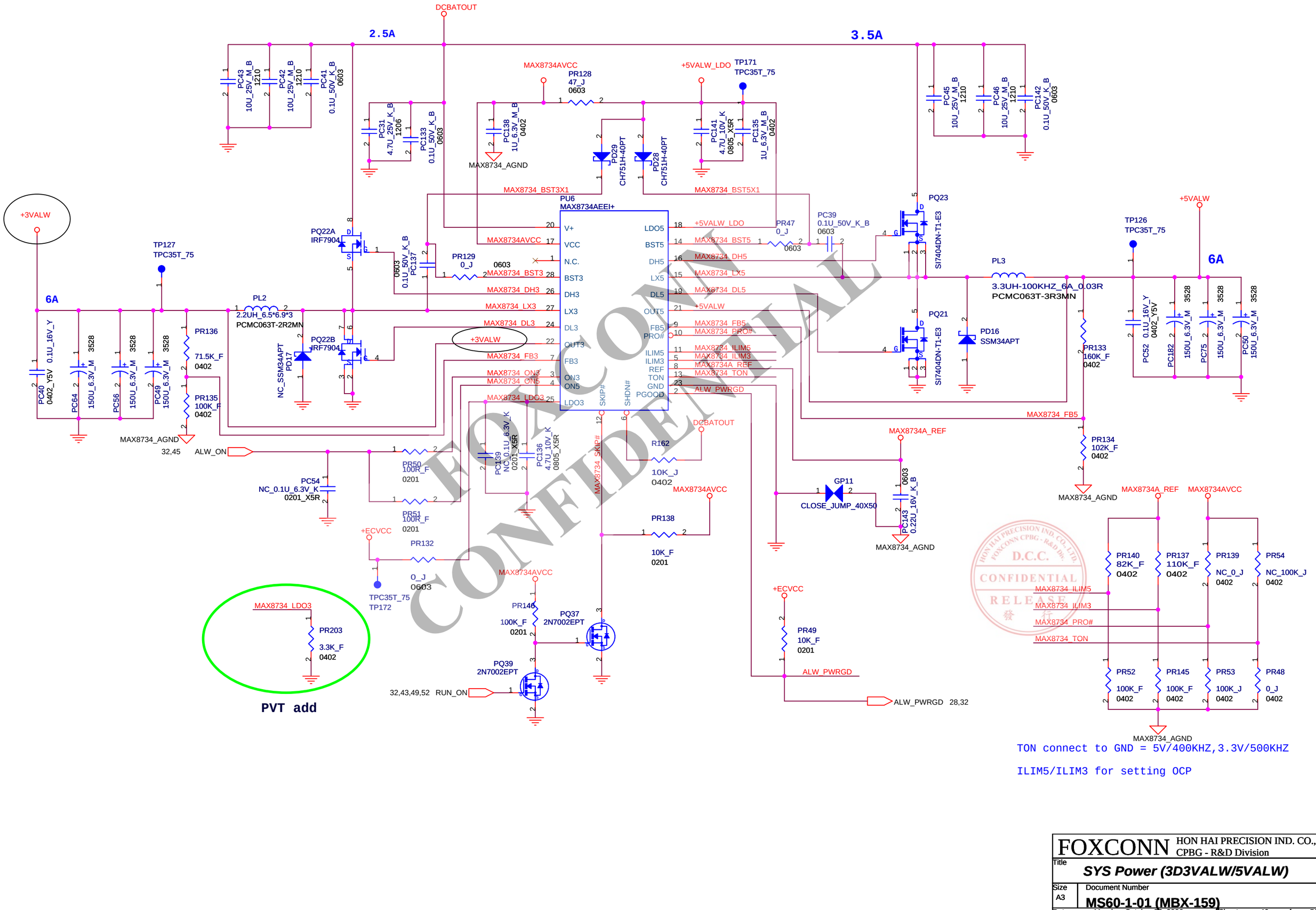
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division

Title: Power Design Diagram

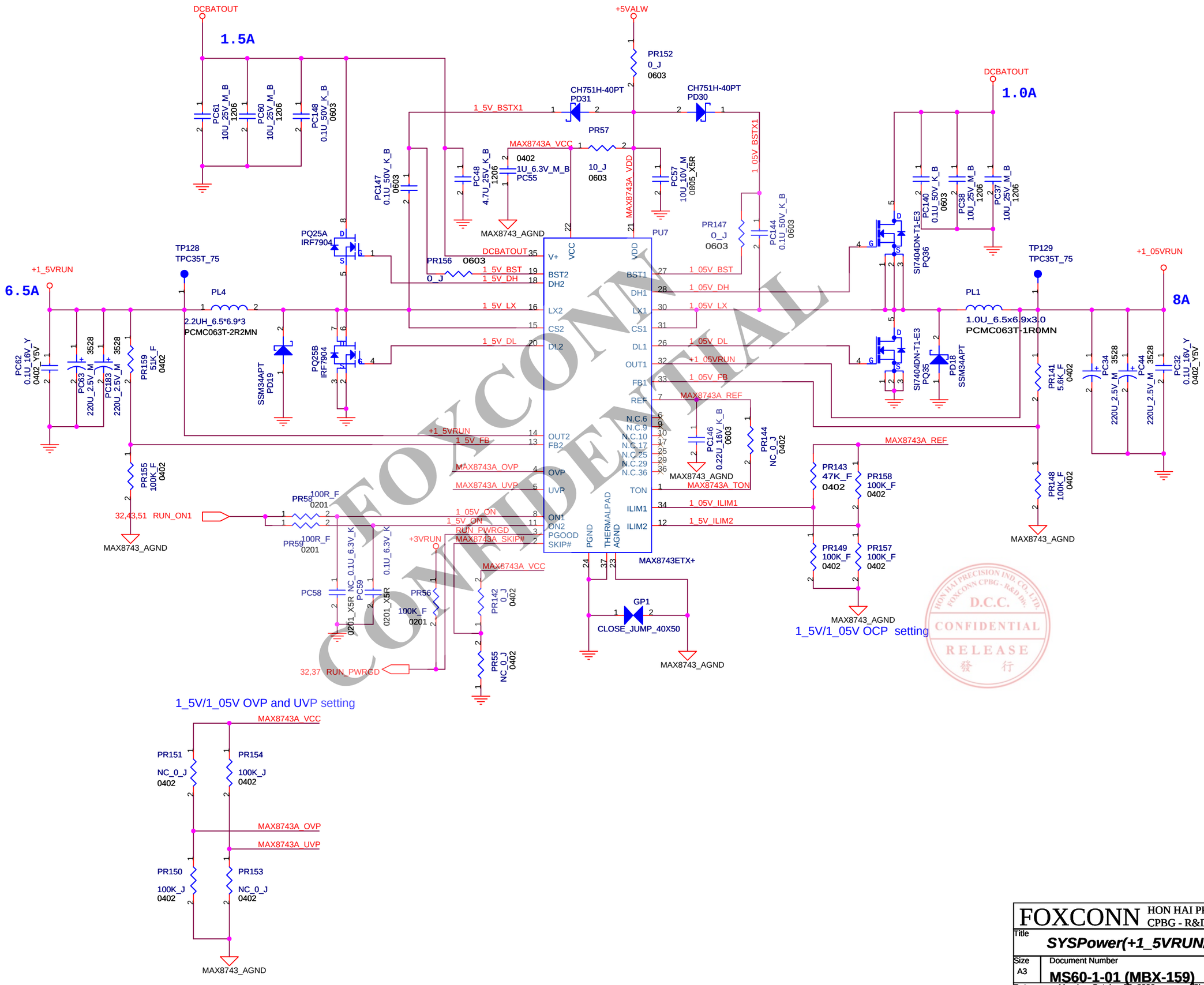
Size: A3 | Document Number: MS60-1-01 (MBX-159) | Rev: 1.0

Date: Monday, October 02, 2006 | Sheet 44 of 56

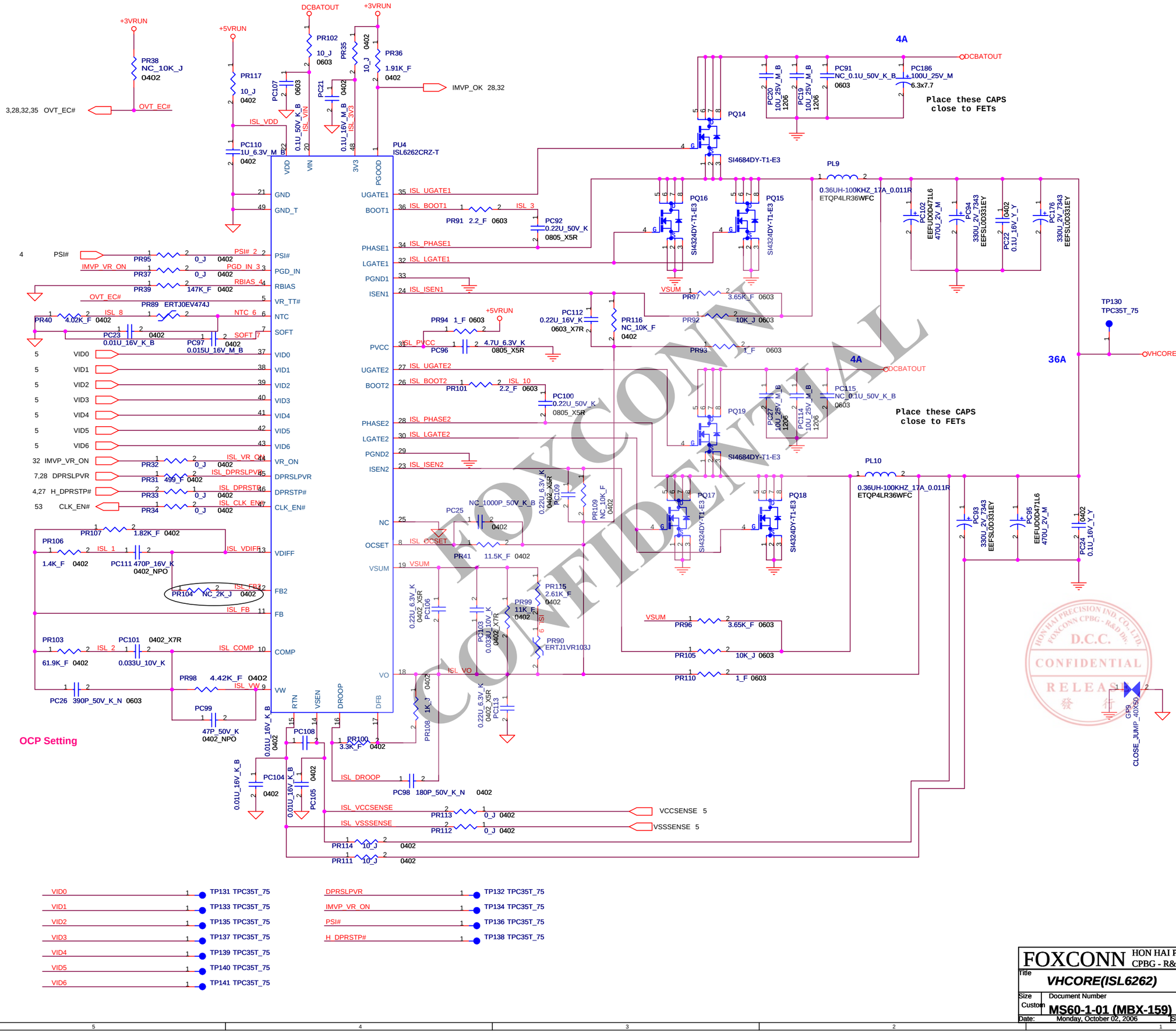




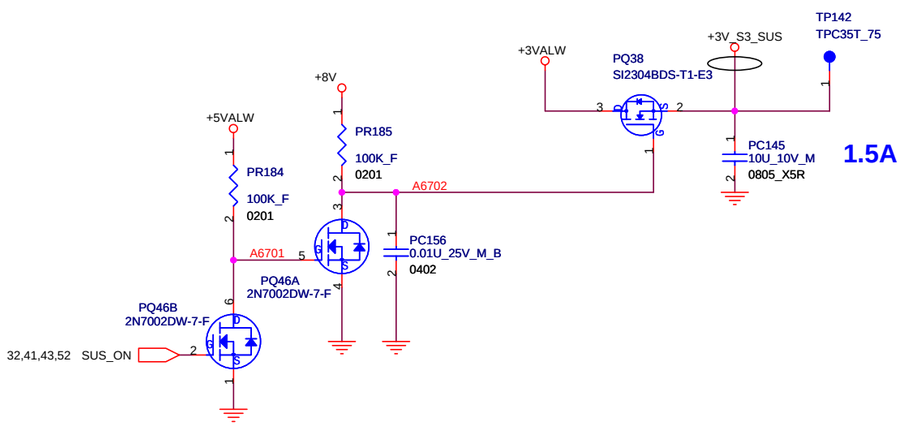
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	SYS Power (3D3VALW/5VALW)		
Size A3	Document Number MS60-1-01 (MBX-159)		Rev 1.0
Date: Monday, October 02, 2006	Sheet 46 of 56		

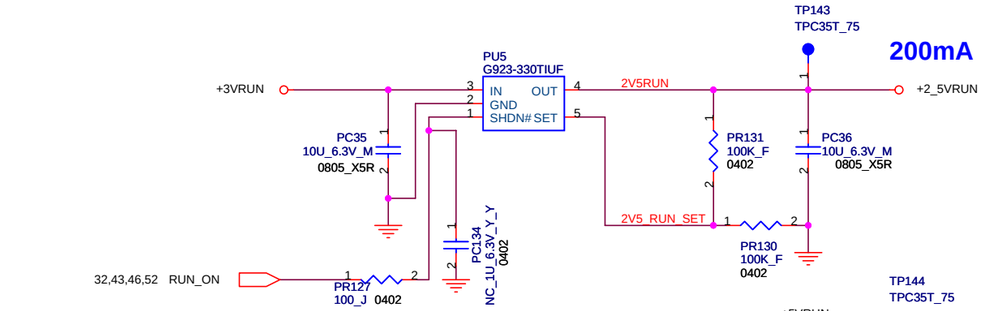


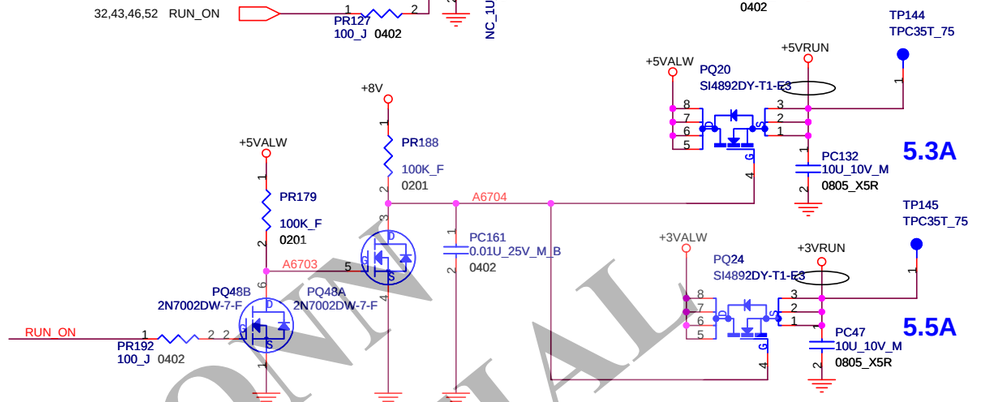
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	SYSPower(+1_5VRUN/+1_05VRUN)
Size A3	Document Number MS60-1-01 (MBX-159)
Rev	1.0
Date: Monday, October 02, 2006	Sheet 47 of 56

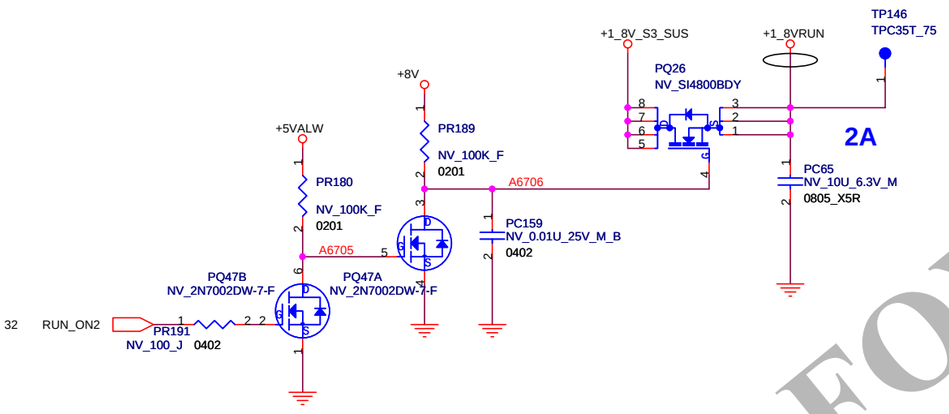


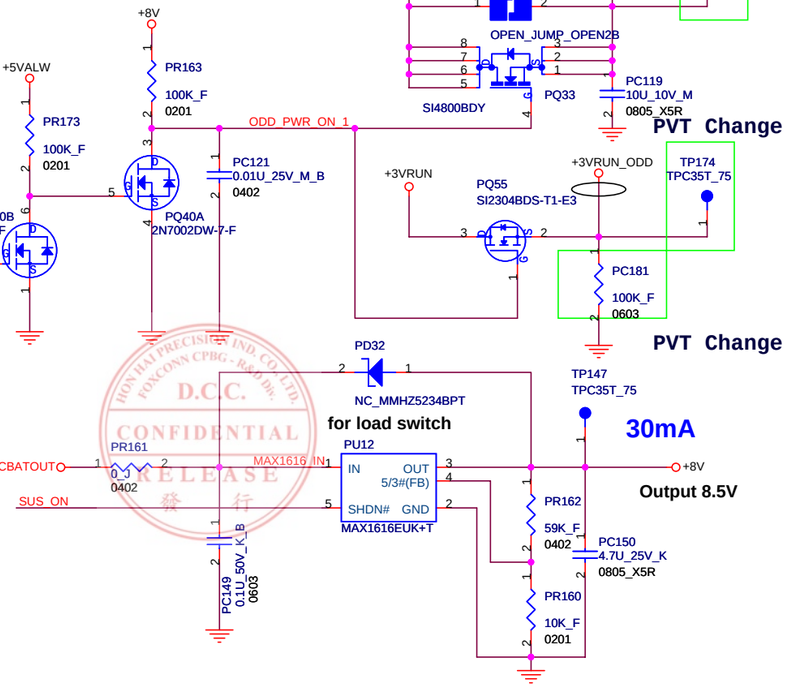
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VHCORE(ISL6262)		
Size: Custom	Document Number: MS60-1-01 (MBX-159)		Rev: 1.0
Date: Monday, October 02, 2006	Sheet 48 of 56		



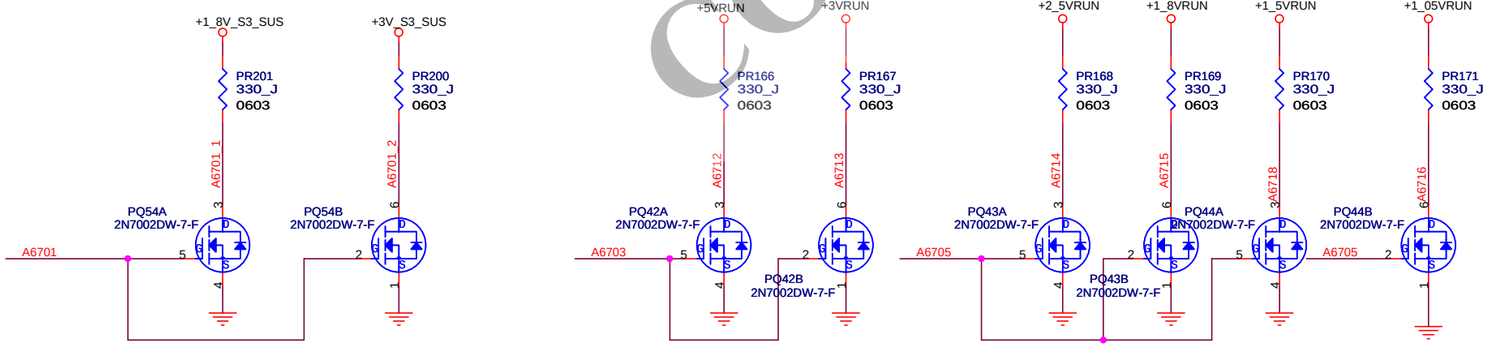




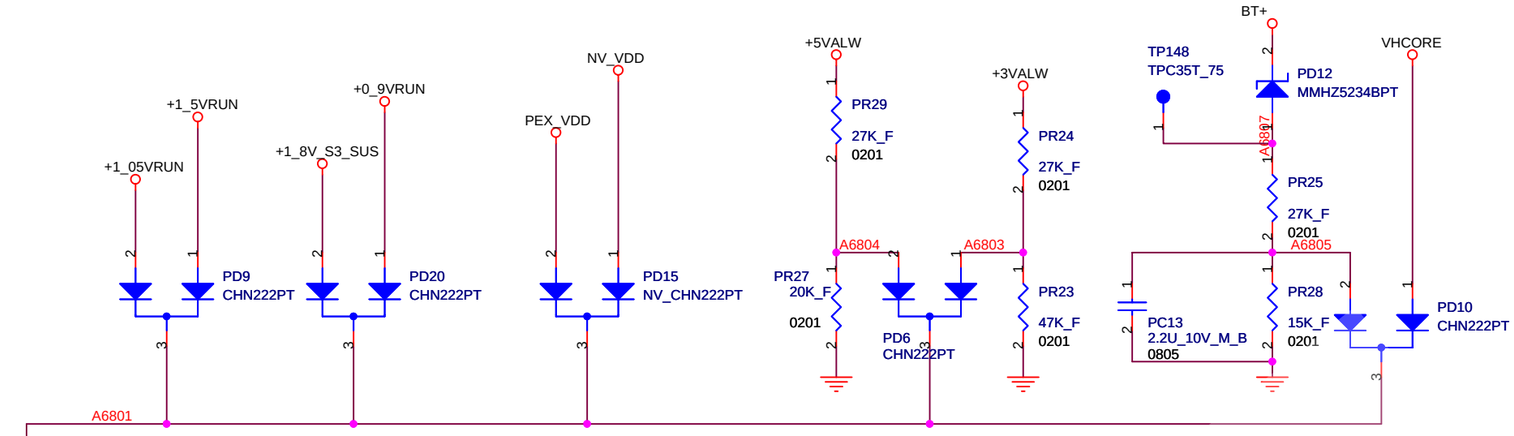


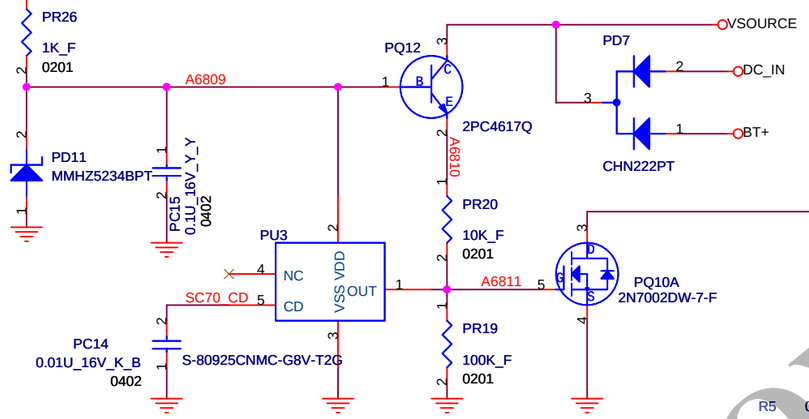


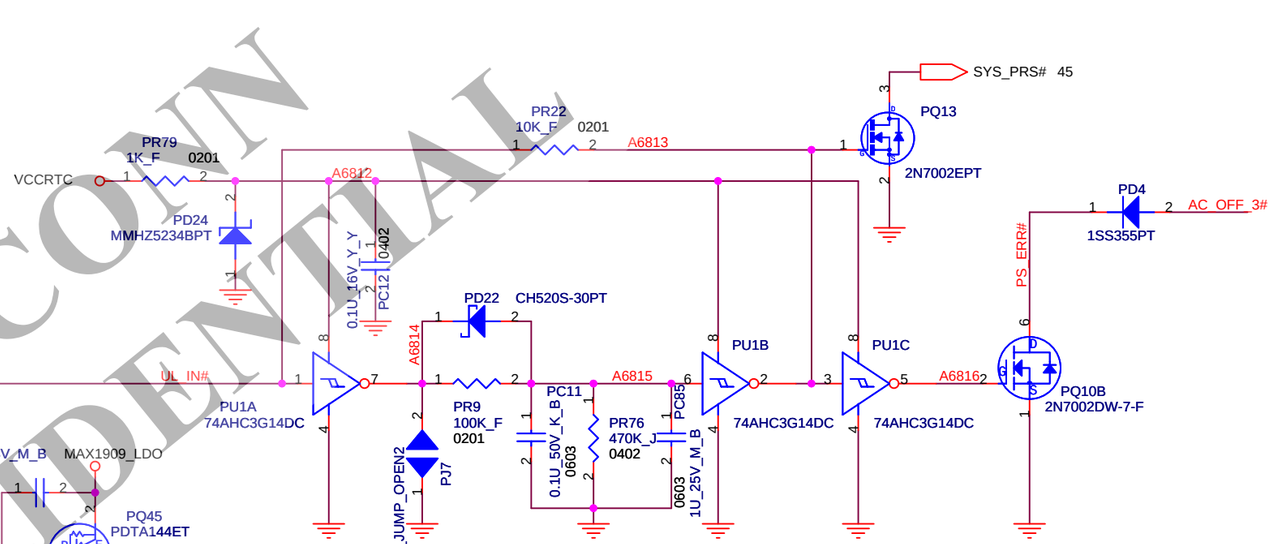
Discharge circuit for power-off

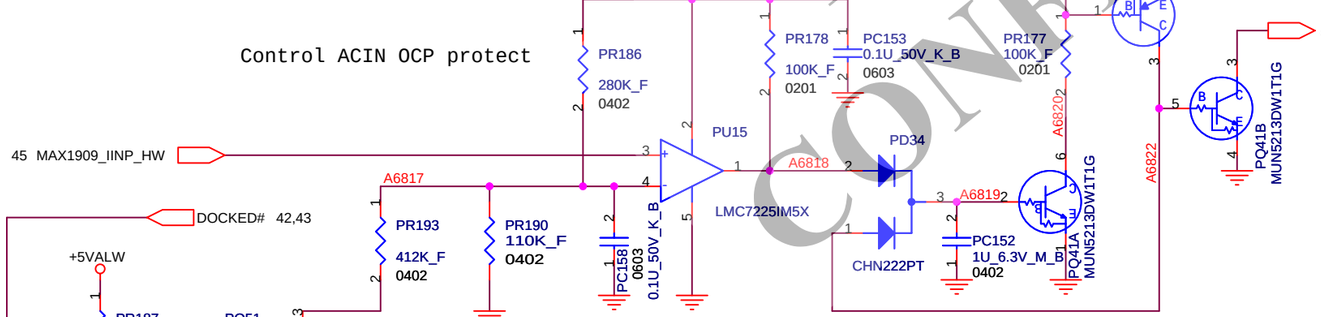


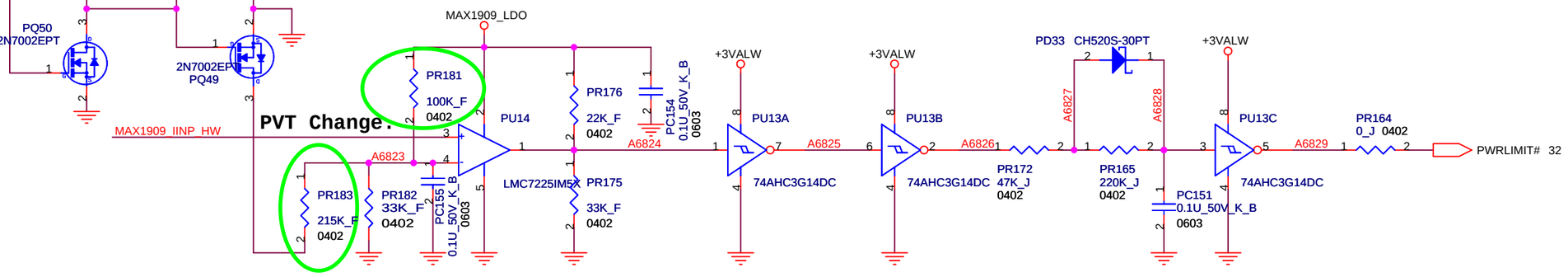
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Other power plan-ZG*		
Size: Custom	Document Number: MS60-1-01 (MBX-159)	Rev: 1.0
Date: Monday, October 02, 2006	Sheet 49 of 56	











VIINP = Isource x Rs1 x GIINP x R

VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.340V/87W	1.2V/78W

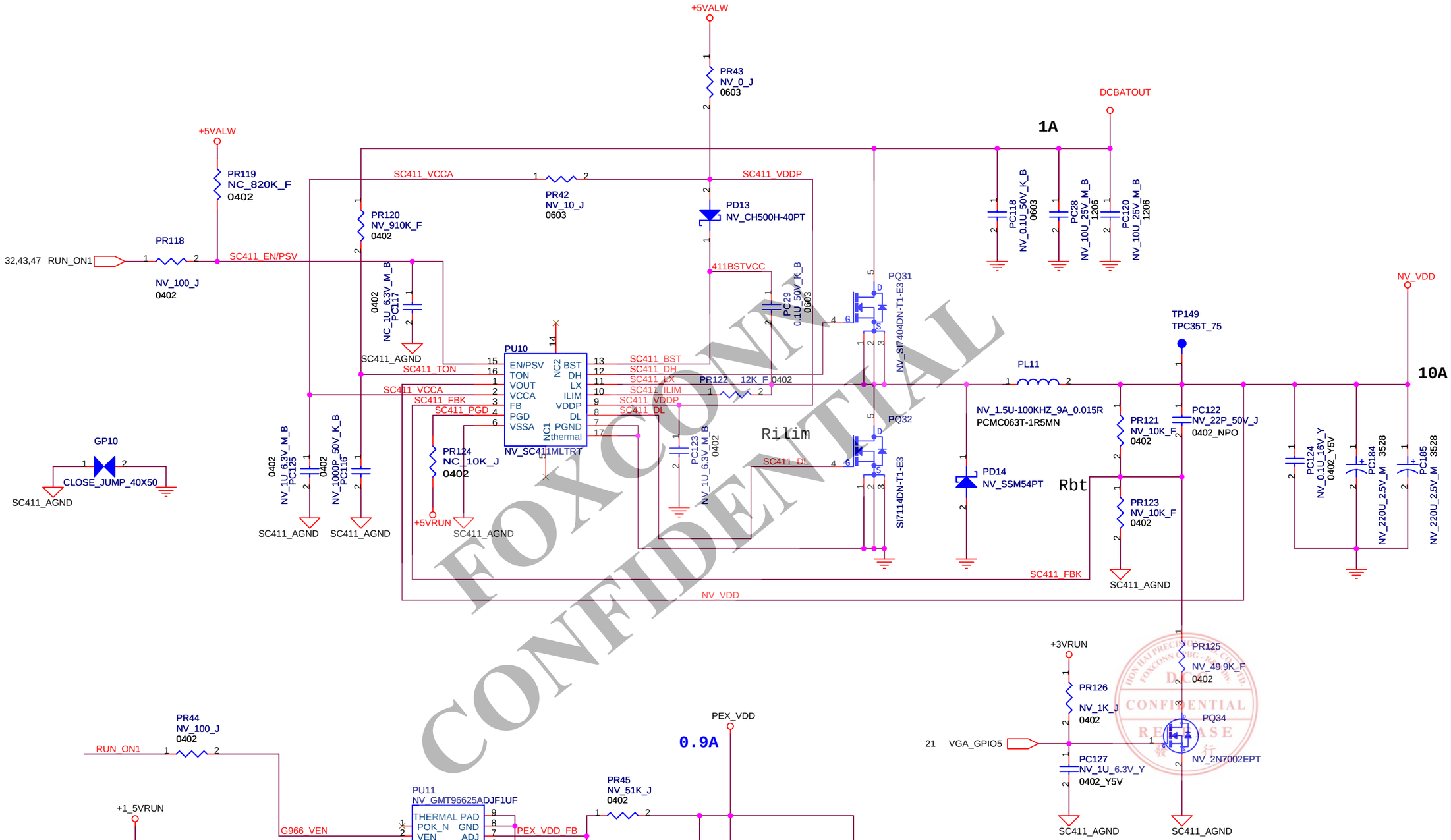
PVT Change

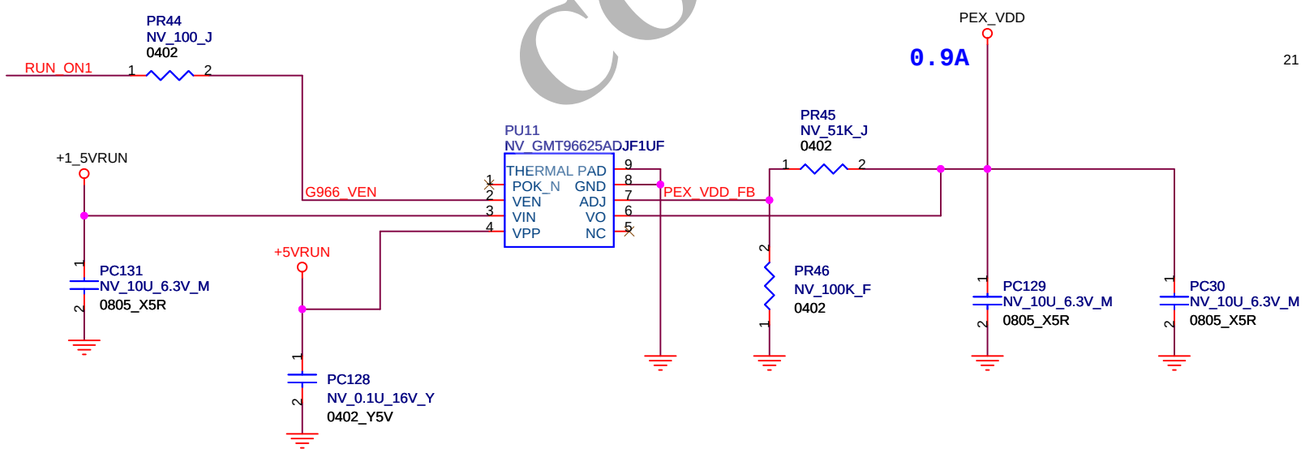
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *OVP protection-ZG*

Size: A3 | Document Number: MS60-1-01 (MBX-159) | Rev: 1.0

Date: Monday, October 02, 2006 | Sheet 50 of 56





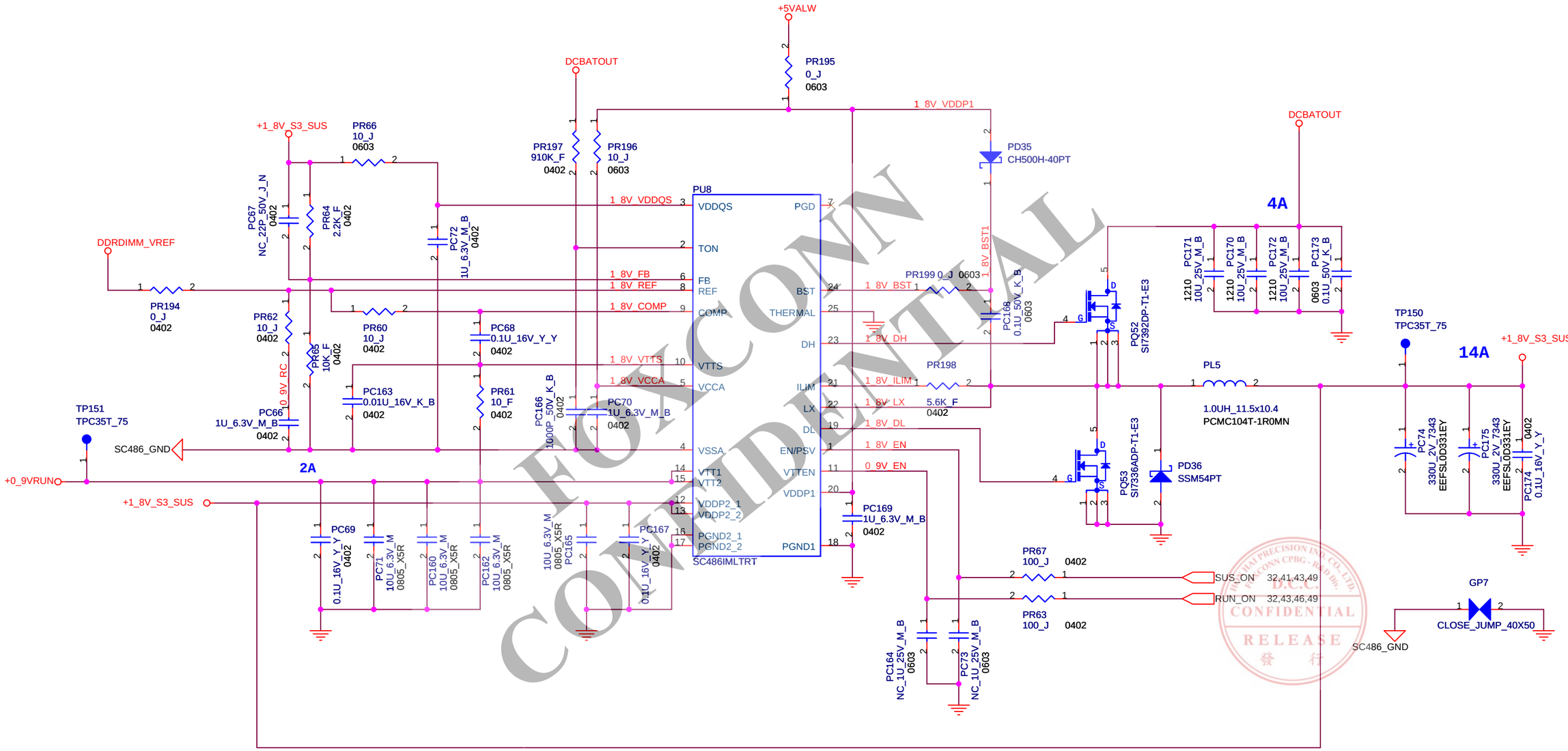
	I/O	Inter pull low	GPIO TABLE
GPIO5	O	Yes	GPU Voltage H: NVDD=1.1V
			GPU Voltage L: NVDD=1.0V

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA POWER(VGACORE&IO)

Size: A3 | Document Number: MS60-1-01 (MBX-159) | Rev: 1.0

Date: Monday, October 02, 2006 | Sheet 51 of 56



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***DDR2Power(+1_8V_S3_SUS/+0_9VRUN)***	
Size A3	Document Number **MS60-1-01 (MBX-159)**	Rev 1.0
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close to clk gen (For EMI)

NC_10P_50V_E_N C459 0402 — CLK_CB48
NC_10P_50V_E_N C462 0402 — CLK_USB48
NC_10P_50V_E_N C474 0402 — CLK_KBCPCI
NC_10P_50V_E_N C473 0402 — PCLK_CB
NC_10P_50V_E_N C470 0402 — CLK_ICHPCI
NC_10P_50V_E_N C472 0402 — CLK_ICH14
NC_10P_50V_E_N C471 0402 — PCLK_JIG

Y4
ITTI_L5030-14.31818-20
14.318MHZ_20P_30PPM
C467 33P_50V_J_N
C469 33P_50V_J_N

Length as short as possible.

U29
ICS9LPR321BKLF

3	VDD48		
9	VDDLCD		
17	VDDSRC_1	PCI_STOP#	1
39	VDDCPU_1	CPU_STOP#	54
26	VDDSRC_2	CPUCLKT1LP	42
34	VDDSRC_3	CPUCLKC1LP	41
43	VDDCPU_2	CPUCLKT0LP	45
48	VDDREF	CPUCLKC0LP	44
61	VDDPCI		
50	U2_XTALIN / X1		
49	U2_XTALOUT / X2		
4	SELPSB0_CLK	FSLA/USB_48MHz	
		CPUCLKT2_ITP/SRCCLKT8LP	38
		CPUCLKC2_ITP/SRCCLKC8LP	37
63	R_CLK_BSEL1	FSLB/PCICLK3	
		*CLKREQG#	57
		SRCCLKT6LP	30
		SRCCLKC6LP	29
60	R_CLK_KBCPCI	*ITP_EN/PCICLK2	
		*CLKREQF#	56
		SRCCLKT5LP	28
		SRCCLKC5LP	27
59	R_PCLK_CB	*PLL_SEL1/PCICLK1	
		*CLKREQE#	55
		SRCCLKT4LP	23
		SRCCLKC4LP	24
58	R_PCLK_JIG	PCICLK0	
		*CLKREQB#	35
64	R_CLK_ICHPCI	*PLL_SEL2/PCICLK_F1	
		SRCCLKT3LP	19
		SRCCLKC3LP	20
46	SCLK		
47	SDATA		
		*CLKREQD#	52
5	GND_1	SATAT/SRCCLKT2LP	15
10	GND_2	SATAC/SRCCLKC2LP	16
51	GND_3		
62	GND_4	*CLKREQC#	36
18	GNDSRC_1		
21	GNDSRC_2	LCDCLK_SST/SRCCLKT1LP	
22	GNDSRC_3	LCDCLK_SSC/SRCCLKC1LP	
25	GNDSRC_4		
33	GNDSRC_5	27MHz_FIX/SRCCLKT0LP	
40	GNDCPU	27MHz_SS/SRCCLKC0LP	
65	THERMAL PAD		
		*CLKREQA#	8
		SRCCLKT7LP	6
		SRCCLKC7LP	7
		DOTT_96MHz	13
		DOTC_96MHz	14
		Vtt_PwrGd#/PD	2
		*PLL_SEL0/REFOUT	53

+V3.3S_CLKVDD
C445 0.1U_16V_Y_Y 0402
C456 0.1U_16V_Y_Y 0402
C468 0.1U_16V_Y_Y 0402
C454 0.1U_16V_Y_Y 0402
C444 0.1U_16V_Y_Y 0402
C457 0.1U_16V_Y_Y 0402
C464 0.1U_16V_Y_Y 0402
C466 0.1U_16V_Y_Y 0402
C442 0.1U_16V_Y_Y 0402

L_+3VRUN_410M
L43 120R-100MHZ_0805 HCB2012KF-121T30
L42 120R-100MHZ_0805 HCB2012KF-121T30
C439 10U_6.3V_M 0805_X5R
C443 10U_6.3V_M 0805_X5R
C437 0.1U_16V_Y_Y 0402
C438 0.1U_16V_Y_Y 0402
+3VRUN
30 mil
30 mil

Pin Straps Pin 53/59/60/64 100K ohm pull-up	
pin53	pin 11/12
0 1	SRCCLK0 27MHz (v)
pin59	pin 15/16
0 1	SRCCLK0 SATA (v)
pin60	pin 37/38
0 1	SRCCLK8 (v) CPU_2_ITP
pin64	pin 13/14
0 1	LCDCLK_SS (CA) SRCCLK1 (NV)

CALISTOGA Chip
HOST CPU

RP18 0404_4P2R 33
RP20 0404_4P2R 33
RP17 0404_4P2R 33
RP9 0404_4P2R 33
RP11 0404_4P2R 33
RP12 0404_4P2R 33
RP14 0404_4P2R 33
RP19 0404_4P2R CA_33
R519 22_F 0402
R520 22_F 0402
R402 33_F 0402
R389 NV_0_J 0402
R388 NV_0_J 0402
R391 NV_0_J 0402

ICH7M SATA
Nvidia Graphic
CALISTOGA DOT96

ICH7 DMI
RP10 0404_4P2R 33

R403 NC_10K_J 0402 — R_CLK_ICH14
R414 NC_10K_J 0402 — R_PCLK_CB
R399 NV_10K_J 0402
R_CLK_ICHPCI
R400 CA_2.2K_J 0402

R380 NC_10K_J 0402 — EXPRESS_DET# 43
R413 NC_10K_J 0402 — PCIE_LAN_CLKREQ#
R518 0_J 0402
R404 10K_J 0402 — PR_LAN_REQ#
R411 NC_10K_J 0402 — MINI_CARD_DET# 43
R383 NC_10K_J 0402 — SATACLKREQ# 28
R412 NC_10K_J 0402 — MCH_CLK_REQ# 7

SM bus Address :
1101001 (ICH7)
For clock generator

CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor
(R69,R40,R41,R70,R1126,R1127)
If EVT ok, del them in DVT

RP16 0404_4P2R CA_33
RP15 0404_4P2R NV_33
CALISTOGA SSCK
Nvidia Graphic

R397 0_J 0402 — CPU_BSEL0 4 — MCH_BSEL0 7
R398 NC_0_J 0402
R415 0_J 0402 — CPU_BSEL1 4 — MCH_BSEL1 7
R13 0_J 0402 — CPU_BSEL2 4 — MCH_BSEL2 7

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title: CLOCK GEN
Size: A3
Document Number: MS60-1-01 (MBX-159)
Rev: 1.0
Date: Monday, October 02, 2006
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H1
hole_tr358x307bc276d98

H5
hole_tr309x354d83

H12
hole_tr289x315d83

H3
hole_c158d158n

H4
hole_c158d158n

H7
hole_c158d158n

H6
hole_c158d158n

H17
hole_ts315bc354d98

H18
hole_ts315bc354d98

H19
hole_tr335x315bc354d98

H2
HOLE_TC236BC276D98

C1
0.1U_16V_Y_Y
0402

C9
0.1U_16V_Y_Y
0402

H13
hole_tc236bc315d114

C178
0.1U_16V_Y_Y
0402

C262
0.1U_16V_Y_Y
0402

H15
hole_tc236bc315d114

C325
0.1U_16V_Y_Y
0402

C324
0.1U_16V_Y_Y
0402

H10
hole_tr315x305d91

H9
hole_tr315x305d91

H8
hole_c98d98n

H24
hole_c67d67n

H21
hole_tc197bc197d98

H22
hole_odo55x67n

H23
hole_odo55x67n

H11
hole_c55d55n

FOR EMI

+5VRUN

C52
0.1U_16V_Y_Y
0402

+5VRUN

C579
0.1U_16V_Y_Y
0402

+1_8V_S3_SUS

+0_9VRUN

C361
0.1U_16V_Y_Y
0402

C373
0.1U_16V_Y_Y
0402

C379
0.1U_16V_Y_Y
0402

C356
0.1U_16V_Y_Y
0402

+5VRUN

C49
0.1U_16V_Y_Y
0402

C483
0.1U_16V_Y_Y
0402

+5VRUN

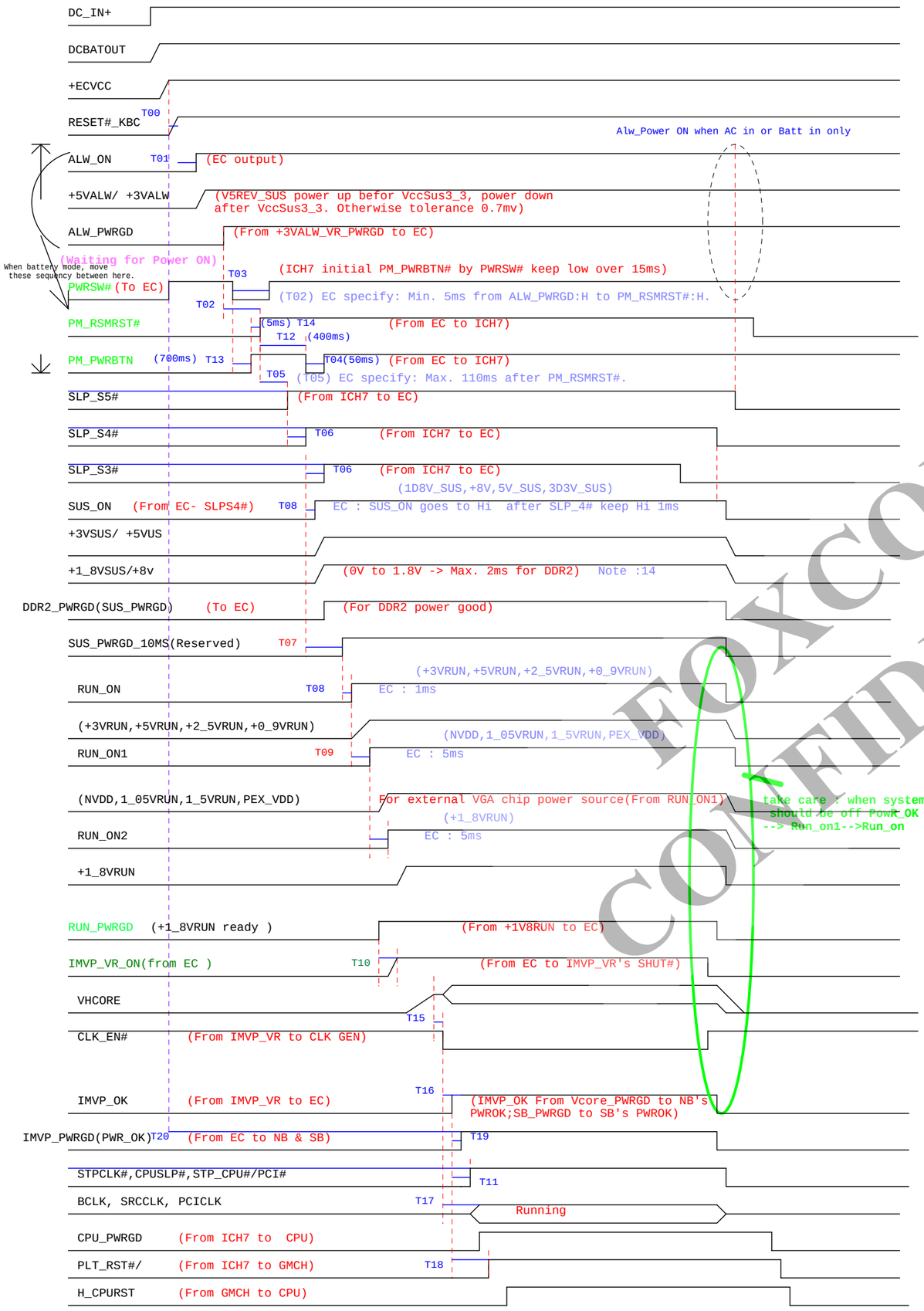
+5VALW

C131
0.1U_16V_Y_Y
0402

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: **HOLE**		
Size: A4	Document Number: **MS60-1-01 (MBX-159)**	Rev: 1.0
Date: Monday, October 02, 2006	Sheet 54 of 56	

MS60 Power On Sequerce Timing

Version : 0.0
Modified date : 2/14/2006



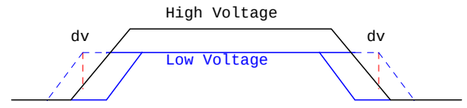
NOTE : (EC KB3910 Min. response time is 1ms)

1. T00 : R=47K , C = 0.1uF is ENE recommand value please refer to KB3910B0-AN4A-200
2. T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
   PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
3. T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
4. T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
5. T05 : RSMRST# active High to SLP_S5# avtive High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing
6. T06(Please reference Intel 16971 Page 301 of t234 timing
7. T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
8. T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
9. T09 : For MS01 current SPEC
10. T10 :Please refer to Intel 16971 Page 300 of t214 timing
11. T11 :Please refer to Intel 16971 Page 303 of t216 timing
12. T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing)
13. T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
14. T14 : For MS01 current SPEC Min. is 5 ms
15. DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
16. IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
17. In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
18. T15 : Please refer to MAX8771 datasheet
20. T16: Please refer to MAX8771 datasheet
21. T17 : Please refer to Intel CK410(14690) page 53
22. T18 : The ICH7 drives PLTRST# active a mininum of 1ms when initiated through the Reset Control register I/O Register CF9h)
23. CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
24. T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Don'san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add dischage circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
2. V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
3. +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
4. +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
5. +3.3VRUN -> +2_5VRUN, dt:0.3mV
6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
7. +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV

R/C delay (47K/ 0.1uF)



T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns~2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms

T11	T12	T13	T14	T15	T16	T17	T18	T19	T20
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min :1s

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Title: **Power Sequence**

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<1>2006/3/28 remove U36.5W no need to program for present application.

<2>2006/3/28 Change PR5 from 13K to common parts 10KOhm.

<3>2006/3/29 Change USB CONN. CN16 & CN40 for ID requirement.
P/N : FOX_UB111193-C1301-4F

<4>2006/3/29 Change ODD CONN. CN21 for ID requirement.
P/N : FOXCONN_QT8H0506_64T2R_4F

<5>2006/3/29 Change PC359,PC360 to 10uF
P/N : 1C-2B70106-M100

<6>2006/3/29 update new HDD CONN CN24.
P/N : 2N-0022002-F0G0

<7>2006/3/29 update new DC-IN CONN PCN1.
P/N : FOX_GS53020-00580-7F

<8>2006/3/29 update new BTY CONN PCN2.
P/N : FOXCONN_BP34063_B6012_7F

<9>2006/3/30 U18.U19.U21.R277.R300.R315change to NC according to Customer's feedback.

<10>2006/3/30 R269,R273,R276,R286,R287,R300 change to Populate according to Customer's feedback.

<11>2006/3/30 New add INV_ENABLE_EC logic dur to BIOS Code merge issue.add new component :
U53.U54 P/N : 14-74AHC1G-0800
R762 P/N : 1R-0000103-J200
R763 P/N : 1R-0000000-J200
R764 P/N : 1R-0000104-J200
Delete R176.R177

<12>2006/3/31 Add C20,C21,C22,C31,C33,C68 for EMI slution.
P/N : 1C-2Y20104-Y000

<13>2006/3/31 Add R5 for Customer feedback.
P/N : 1R-0000000-J200

<14>2006/3/31 Dummy R482,R483 for Customer feedback.

<15>2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component :
U55.U56 P/N : 15-RT9702A-0000
C521.C522 P/N : 1C-2Y20104-Y000
R569.R573 P/N : 1R-0000105-J200
C870.C871 P/N : 1C-2Y30225-Y000
C535.C751 P/N : 1C-2B70106-M100
Deleted Component :
Q12.Q13.Q20.Q21.C535.C527.C521.C751.C753.C752.R486.R476.R568.R569

<16>2006/3/31 CN2 Pin11 change to +3V_S3_SUS for Customer feedback.

<17>2006/4/3 CN20.CN32,CN33 Pin assignment modified due to Customer's concern.

<18>2006/4/3 CN31,CN32,CN33 CN34 Connector change.
P/N : GB11261_1051_7F

<19>2006/4/3 L17 & L19 updated according to Customer feedback
P/N : 1L-DCS0603-1000

<20>2006/4/4 Add PWR_MIZER circuit.
U6J GPIO10 with new signal "NV_PWR_MIZER"
new Components added and modified as below :
10K Ohm -- R130.R766 -- P/N : 1R-0000103-J200
7.5K Ohm -- R765.R767.R768.R769.R770 -- P/N : 1R-0000752-F200
4.3K Ohm -- R128 -- P/N : 1R-0000432-F200
2N7002EPT -- Q54.Q55.Q56.Q57.Q58 -- P/N : 17-2N7002E-PT00

<21>2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.

<22>2006/4/4 D6.D7.D8 change to Q59.Q60.Q61
P/N : 17-2N7002E-PT00

<23>2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate.
P/N : 1R-0000121-J200

<24>2006/4/4 new add Q62 for WLAN LED Logic
P/N : 17-2N7002E-PT00

<25>2006/4/4 NC F1 and C859 according to customer's feedback.

<26>2006/4/4 delete R482.R483 according to customer's feedback.

<27>2006/4/6 add H3 ~ H20

<28>2006/4/6 Update BTY Connector PCN2 for ME requirement.
P/N : 2N-0006001-MKX0

<29>2006/4/6 R278.R289.R270 change to 75Ohm and circuit modified as customer's feedback.
P/N : 1R-0000750-F200

<30>2006/4/6 R543 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-F300

<31>2006/4/6 R553 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-J200

<32>2006/4/6 R99.R94.R97.R109.R67.R64.R65.R75 change to NC as customer's feedback.
and R66.R69.R98.R101 change to 120Ohm.
P/N : 1R-0000121-J200

<33>2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.

<34>2006/4/6 CN31 Pin1.2 change to +3V_S3_SUS as customer's feedback.

<35>2006/4/6 add 1A Fuse F4.F5.F9.F11.F15.F17.F18.F19
P/N : 1M-F32V1A0-F000

<36>2006/4/6 add 0.5A Fuse F2.F3.F6.F7.F8.F10.F12.F13.F14.F16.F18
P/N : 1M-F32V0A5-F000

<37>2006/4/6 add C872 according to MS20 lesson learn.
P/N : 1C-2B2012-M000

<38>2006/4/6 CN34 Pin23.24 change to +3VRUN.

<39>2006/4/6 add C71.C74.C87 for EMI.
P/N : 1C-2Y20104-Y000

<40>2006/4/6 add C89.C188.C199.C208.C213.C214
P/N : 1C-2Y20104-Y000

<40>2006/4/7 add C215.C216.C217.C218.C219 for EMI solution.
P/N : 1C-2Y20104-Y000

<41>2006/4/7 R118,R119,R351 change to populate as customer's feedback.

<42>2006/4/7 Y1.C104.C107.C492.C497.C501.R433.R434.R427.R428.R429.R430.R132.
R133.R134.R136.R117 change to NC as customer's feedback.

<43>2006/4/7 R439.R443 change to 0 Ohm as customer's feedback.
P/N : 1R-0000000-J200

<44>2006/4/7 update Net name EN_EXT_DEV_SENSE# as customer's feedback.

<45>2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component :
PQ183 P/N : 1T-2N7002D-W000
PR115 P/N : 1R-0000101-J200
PR103.PR114 P/N : 1R-0000104-F100
PC87 P/N : 1C-2B20103-M000
PQ38 P/N : 1T-S148008-DY00
PC76 P/N : 1C-2B70106-M200

<46>2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component :
PR273 P/N : 1R-0000103-F200
PR773 P/N : 1R-0004992-F200
PQ20 P/N : 17-2N7002E-PT00
PR774 P/N : 1R-0000102-J200
PC873 P/N : 1C-2Y20105-Y000

<47>2006/4/10 add H21~H24.

<48>2006/4/10 Rename Schematic Part referene.
new version since 4/11

<49>2006/4/11 change R68.R133.R100
P/N : 1R-0000151-F200

<50>2006/4/11 PR111.PR114 change to NC according to PWR team's suggestion in EVT.

<51>2006/4/11 Modify ODD reset circuit as customer's feedback.
Add U37 P/N : 15-MAX809S-0000
Add R516 P/N : 1R-0000104-J200
NC R305

<52>2006/4/11 Remove C257 for EMI comment.

<53>2006/4/11 add ODD Reset RC.
Add RS17 P/N : 1R-0000103-J200
Add C580 P/N : 1C-2Y20104-Y000

<54>2006/4/14 change R197.R198.R199.R200 to 60.4Ohm
P/N : 1R-000604X-F200

<55>2006/4/14 add R518 for 0Ohm
P/N : 1R-0000000-J200

<56>2006/4/14 CN7.C409.C412.L37.F16.R44.R45 change to CA from NV to fit configuration.

<57>2006/4/27 PR111.PR114 change to Populate from NC according to PWR team's suggestion in EVT.
P/N : 1R-0000100-J200

<58>2006/5/24 PWR/SUS LED control signal swap to fit the correct definition.

<59>2006/5/24 DC_IN connector connection swap to fit the correct definition.

<60>2006/5/24 WWAN Connector remark with "CA".

<61>2006/5/24 add more 12pcs 10uF capacitor for CPU usage reseving.
P/N : 1C-2B70226-M100

<62>2006/5/24 R47 change to populate for T/P rotation.

<63>2006/5/24 L21.L23 change to 1L-DWL10-C100 from 1L-DCS0603.

<64>2006/5/24 add new GPIO07 VISTA SUPPORT for Audio mute concern as customer's comment.

<65>2006/6/1 change both USB connector according to ME requirement.
P/N : 1N-0004000-FEG0

<66>2006/6/1 change both INV connector according to ME requirement.
P/N : 1N-0006001-M1T0

<67>2006/6/1 change TP connector according to ME requirement.
P/N : 1N-0012001-F0T0

<68>2006/6/1 change OIDE connector according to ME requirement.
P/N : 1N-0006000-F0T0

<69>2006/6/1 change OIDE connector according to ME requirement.
P/N : 1N-0006000-F0T0

<70>2006/6/2 Delete GPIO8 and GNDing CN3 Pin1 for WWAN removing.

<71>2006/6/2 Delete H14 & H16 for WWAN removing.

<72>2006/6/2 Delete R264.R271 for Debug BD LED.

<73>2006/6/5 Delete RST_IC circuit and replace with PLT_RST#.

<74>2006/6/5 Delete all GM VGA related circuit in Page8/10/25/42.

<75>2006/6/8 change PORT_DET# from EC Pin81 to Pin176 for Noise decreasing.

<76>2006/6/9 PC127 change to Populate to improve VGA power feedback.

<77>2006/6/9 add +3VRUN_ODD for ODD connector.also new power plane control for this.

<78>2006/6/9 add R323 & C185 for VGA improvement.

<79>2006/6/9 add R238 1K ohm for customer's comment.
P/N : 1R-0000102-J200

<80>2006/6/13 remove RP13 and replace with R519/R520 for WLAN issue improving.
P/N : 1R-0000220-F200

<81>2006/6/15 reserve R264/R271 for VRAM.
P/N : 1R-0000000-J200

<82>2006/6/15 Change PQ32 for VGA Power modification.
P/N : 17-S17114D-NT00

<83>2006/6/15 Change USB connector footprint to FOX_UB11193_C1301_4F.
but actually will populate with BOM Connector that is FOX_UB11193_C1304_4F

<84>2006/7/18 Change TP connector to reverse 180.

<85>2006/7/18 add ODD_LED# to pin 37

<86>2006/7/18 Remove SD signal for Jugar comment.

<87>2006/7/18 add R521

<88>2006/7/19 change PD1 from SM15.TC to PESD15VS2UT.215(16-PESD15V-S200).

<89>2006/7/19 dd one test point in P+ and P- (place on bottom side).

<90>2006/7/19 add test points in net +ECVCC and +5VALW_LDO.

<91>2006/7/19 remove PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ9 .

<92>2006/7/20 add test points TP173,TP174 in net +5VRUN_ODD and +3VRUN_ODD.

<93>2006/7/25 add PD37 and PR203 for Power improvement.

<94>2006/7/27 change PC89 to (1C-2B30224-M000).

<95>2006/7/27 add C605 for NV_PWR_MIZER.

<96>2006/8/01 add C606 and C607 to 1C-2N20030-D000.

<97>2006/8/01 change R263 and R265 to (1R-0000222-J200).

<98>2006/8/01 add PC6 and PC7 to 1C-2N20030-D000.

<99>2006/8/01 add D13 to 16-PACDN04-2Y00 for ESD protector.

<100>2006/8/01 add PC186 to 1C-10X0107-M403 for PWR.

<101>2006/8/01 Change PC186 P/N:1C-10X0107-M403 to 1C-1XX0107-M400 for PWR.

<102>2006/8/02 Change R189 to 1R-0000102-J200.

<103>2006/8/03 remove R425.

<104>2006/8/03 add D14 to 16-CH520S3-0P00.

<105>2006/8/03 add GP14 to OPEN_JUMP_40X58.

<106>2006/8/03 Change U5,U10,U11,U22,U28,U38 to 14-74AHCT1-G000.

<107>2006/8/03 Change H2 to 1X-HOLE000-0282.

<108>2006/8/03 add H24.

<109>2006/8/04 add R522 to 1R-0000103-J200 .

<110>2006/8/04 add Q32 to 17-2N7002E-PT00 .

<111>2006/8/04 Change CN1,CN2,CN5,CN6 to GB11261_1051_7F.

<112>2006/8/07 add CN1 PIN3 to 3VRUN .

<113>2006/8/07 add Q33 .

<114>2006/8/07 Change Battery Conn Vender P/N to BP34067-B6012-7F.

<115>2006/8/08 Change R433 to 330.

<116>2006/8/08 add CN5 PIN26 to +3V_S3_SUS .

<117>2006/8/08 add CN5 PIN19,20 to 3VRUN .

<118>2006/8/08 add CN5 PIN16,17 to 1.5VRUN .

<119>2006/8/08 Change RR8 to 19.1K.

<120>2006/8/08 Change PR181 to 100K.

<121>2006/8/08 Change PR183 to 127K.

<122>2006/8/08 add F20,F21,F22 to 1M-F06V1A1-F000.

<123>2006/8/08 del F20

<124>2006/8/08 add R523 .

<125>2006/8/08 Would R303 NC "DVI Hot Plug Detect" is implemented by not Gfx but EC as usual.

<126>2006/8/08 Change RR8 to 22.1K.

<127>2006/8/11 Change RR15 to 1R-0000203-F100.

<128>2006/8/11 Change RR183 to 1R-0000153-F200.

<129>2006/9/04 add D15,D16 to 16-3CS500V-4000.

<130>2006/9/04 add Q34 to 17-PMV65XP-0000

<131>2006/9/04 add Q35 to 17-PDTC144-EU00

<132>2006/9/04 add R524 to 1R-0000472-J200

<133>2006/9/04 add R525 to 1R-0000102-J200.

<134>2006/9/04 add F23 to 1M-F006A35-F000

<135>2006/9/04 add U39 to 15-TPS2055-0000.

<136>2006/9/04 add U40 to 15-MAX4798-0000.

<137>2006/9/04 add R526,R527 to 1R-0000103-J200.

<138>2006/9/04 del R521,U34.

<139>2006/9/04 Change CN12,CN16 to 1N-0004000-FEG0.

<140>2006/9/04 Change R189 to 1R-0000103-J200.

<141>2006/9/05 del TP1,TP2,TP3,TP5,TP6,TP7,TP8,TP9

<142>2006/9/05 del TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19

<143>2006/9/05 del TP20,TP21,TP22,TP23,TP25,TP26,TP27,TP28,TP29

<144>2006/9/05 del R527

<145>2006/9/06 Change PR136 to 1R-0007152-F200.

<146>2006/9/09 add R527 to 100k

<147>2006/9/09 add R528 to 10k

<148>2006/9/11 Change R296,R297 to 1R-000604X-F200

<149>2006/9/11 Change PC106,PC109,PC113 TO 1C-2B20224-K101

<150>2006/9/11 Change PC89 to 1C-2B30224-K000.

<151>2006/9/12 add R529 to 1R-0000000-J200

<152>2006/9/12 add R530 to 1R-0000102-F200

<153>2006/9/12 Change CN23 to MH11747-BR2S-4F.

<154>2006/9/20 ChangeQ5 to PDTC144EU.

<155>2006/9/27 Change R294,R295,R298,R315 to 1R-0000151-F200