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P. Leader	Check by	Design by

PCB P/N: 1P-0066700-8010 - Unimicro
 1P-0066201-8010 - NANYA

Project Code & Schematics Subject: MS60 Main Board

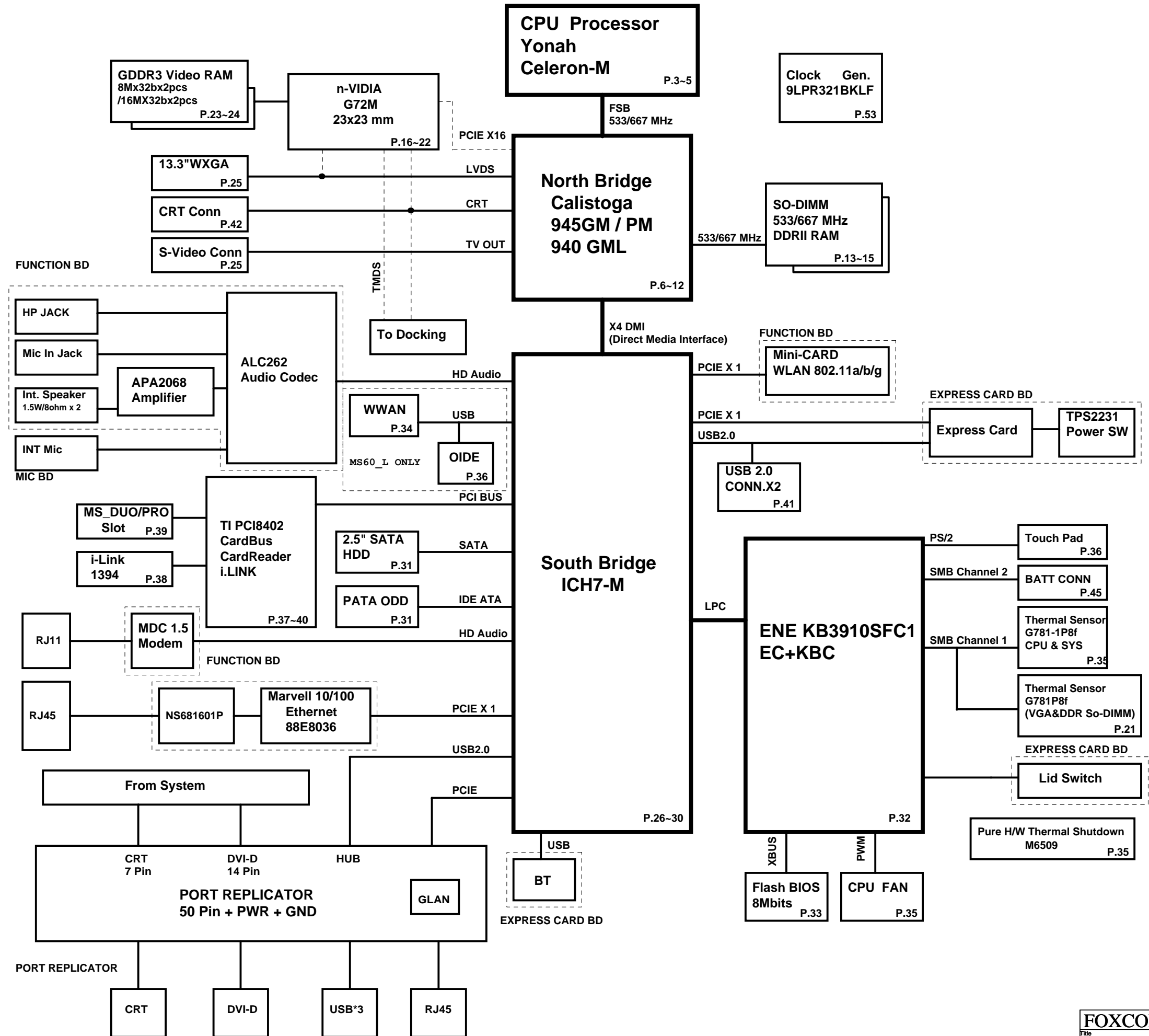
FOXCONN HON HAI PRECISION IND. CO., LTD.
 CPBG - R&D Division

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MS60 (CALISTOGA PM/GM+Gfx Block Diagram)



SYSTEM DC/DC MAX8734 P.46	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC MAX8743 P.47	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SC486 P.52	
DCBATOUT	+1_8V_S3_SUS +0_9VRUN

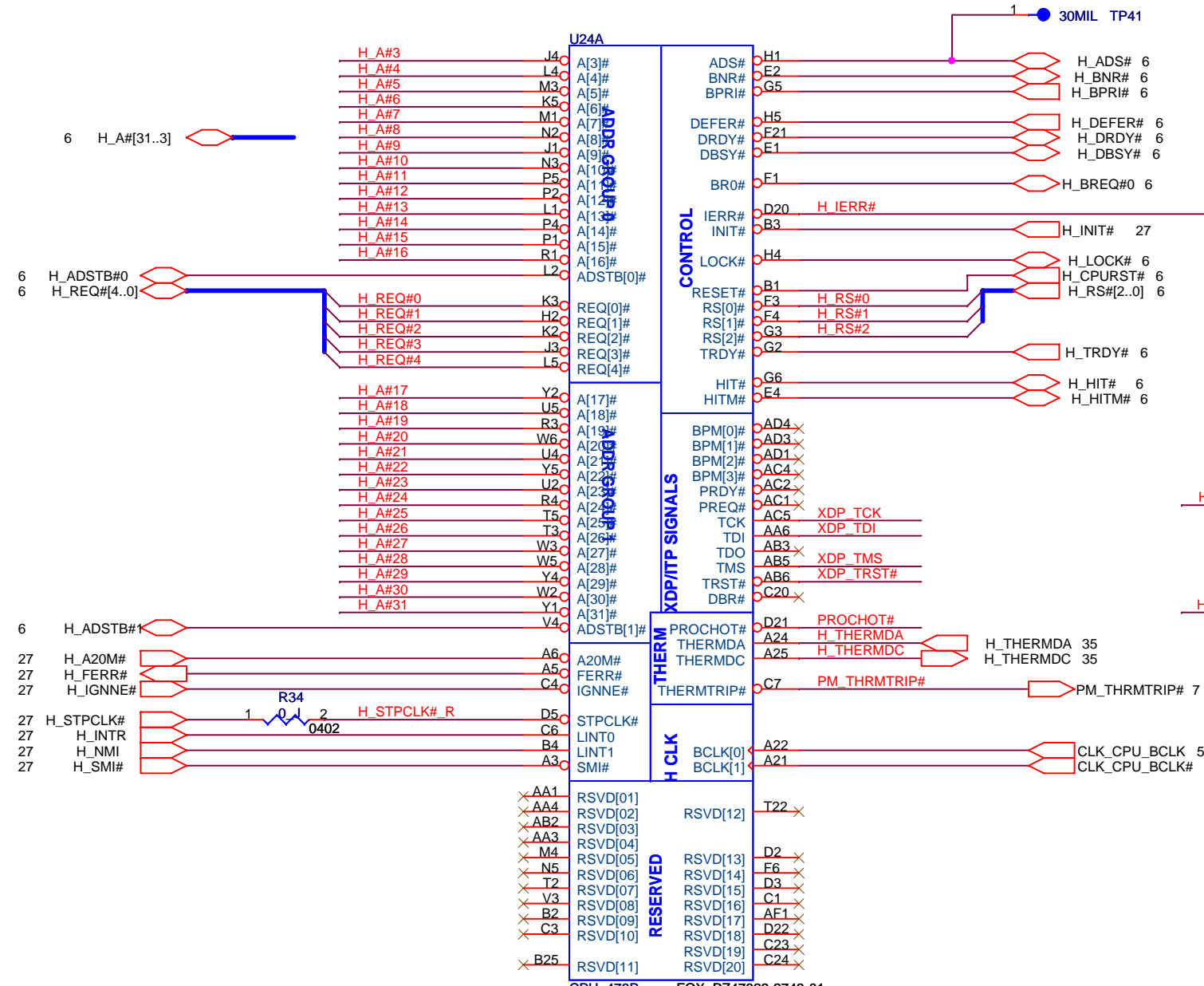
CPU DC/DC ISL6262 P.48	
INPUTS	OUTPUTS
DCBATOUT	VHORE

AMP DC/DC MAX1616 P.49	
INPUTS	OUTPUTS
DCBATOUT	+8VRUN

SC411 P.51	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

GMT966 P.51	
+1_5VRUN	PEX_VDD

MAXIM CHARGER MAX1909 P.45	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

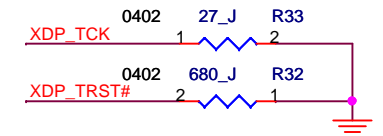
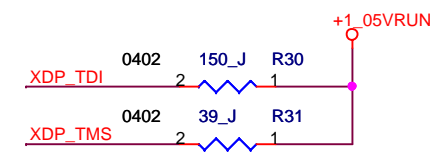


Layout note:
no stub on
H_STPCLK#

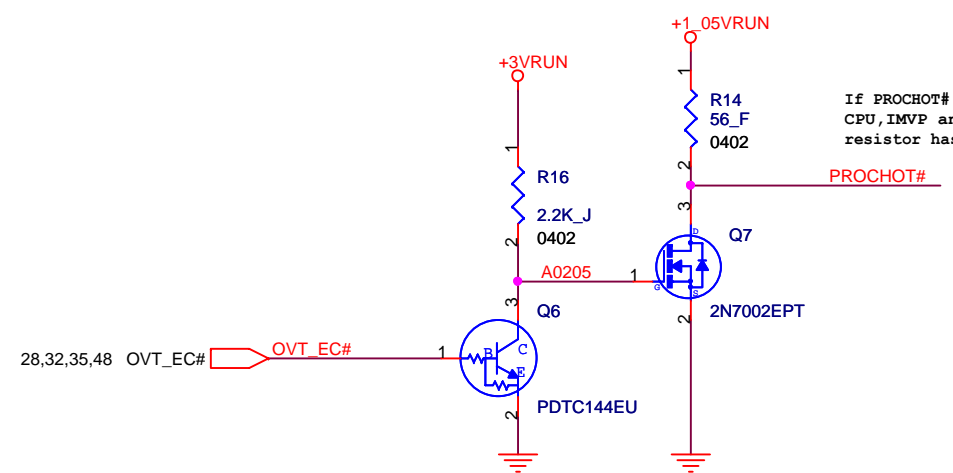
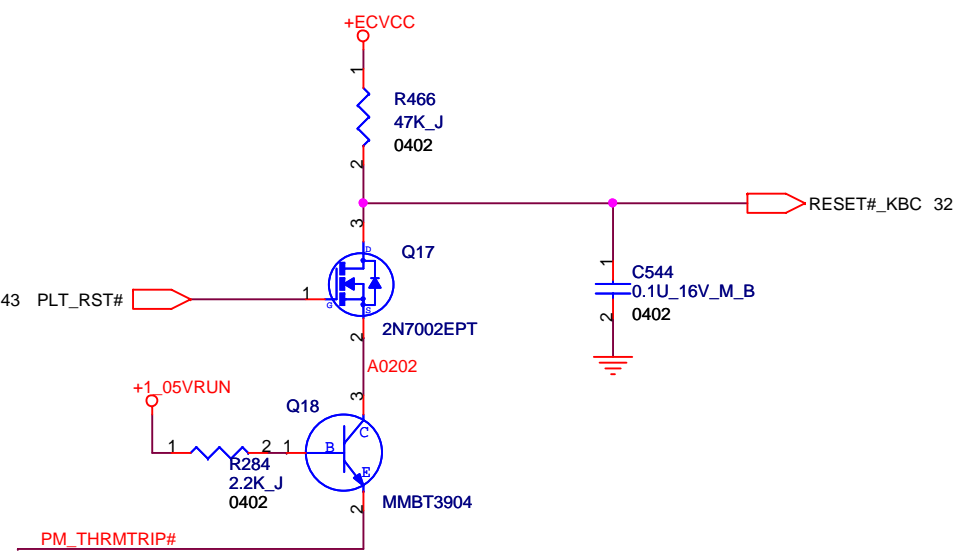
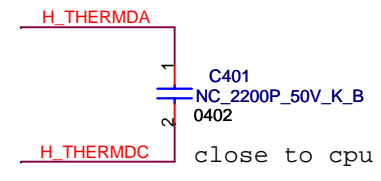
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

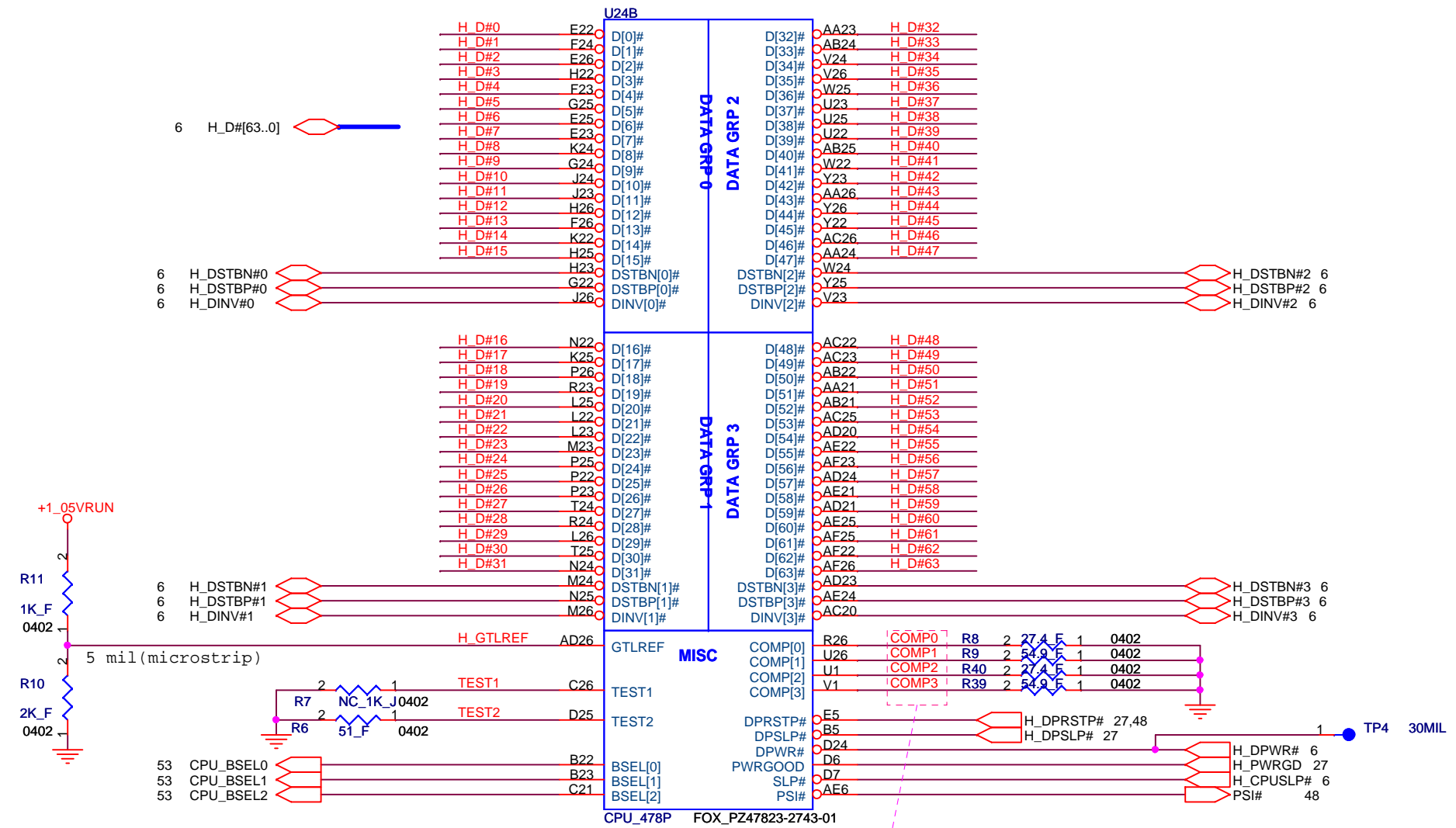
ICH7M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1

If PROCHOT# is routed between
CPU, IMVP and MCH, pull-up
resistor has to be 75 ohm +-5%



Debug port not used .
resistors close to CPU.



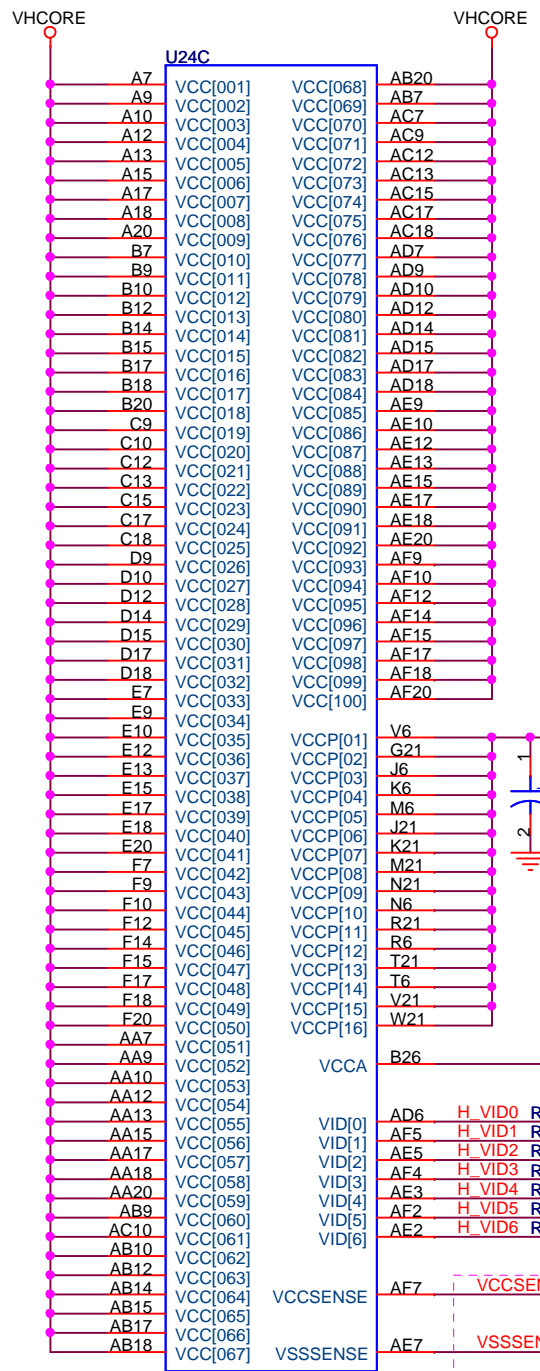
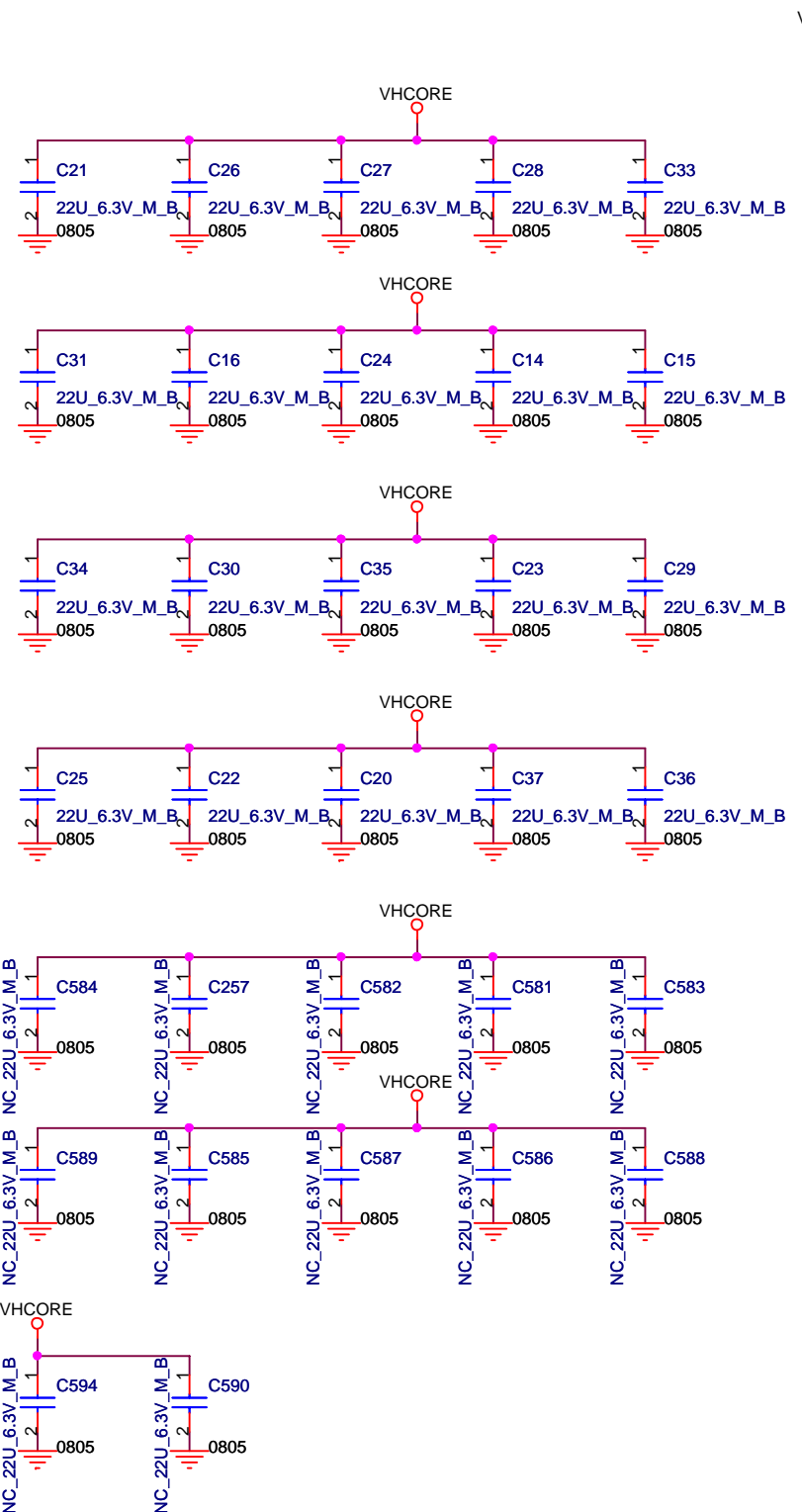


Place close to CPU
 Layout Note:
 Zo=55 ohm, 0.5"
 max for GTLREF.

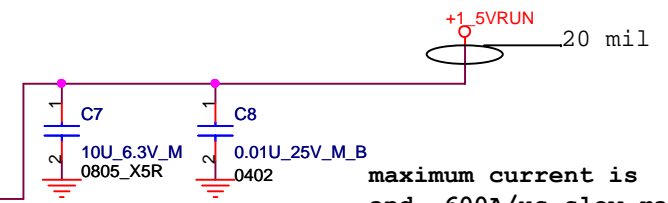
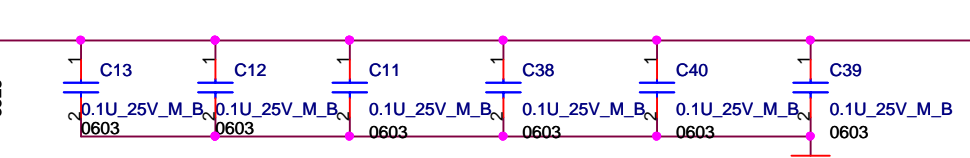
FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
LLL	Reserve
LLH	133
LHL	Reserve
LHH	166

Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".

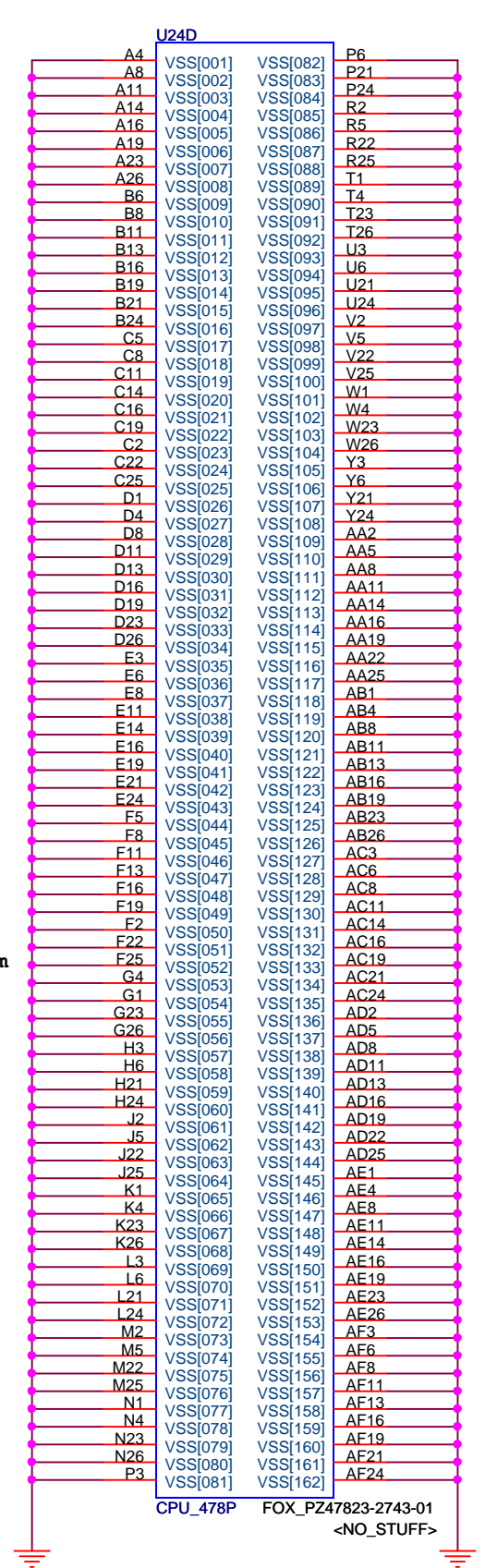


CPU_VCCA----->130mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A

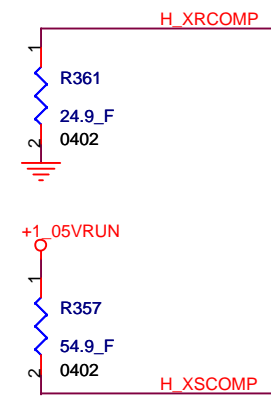


maximum current is 130mA for CPU_VCCA in Merom
 and 600A/us slew rate for CPU_VCCA

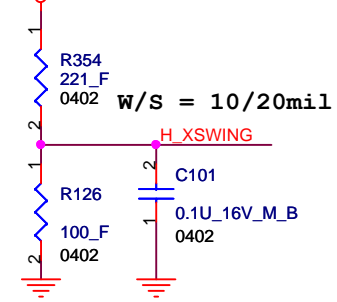
Same Length
 Layout Note: Route
 VCCSENSE traces at 27.4
 Ohms with 50 mil spacing.
 Place PU and PD within 1
 inch of cpu.
 width=18 mil
 spacing=7 mil



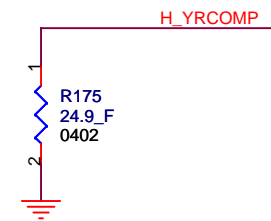
w/s = 10/20mil



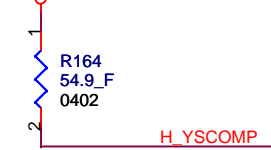
+1.05VRUN



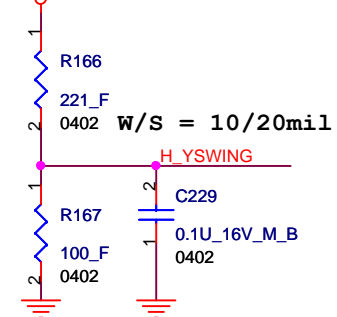
w/s = 10/20mil



+1.05VRUN

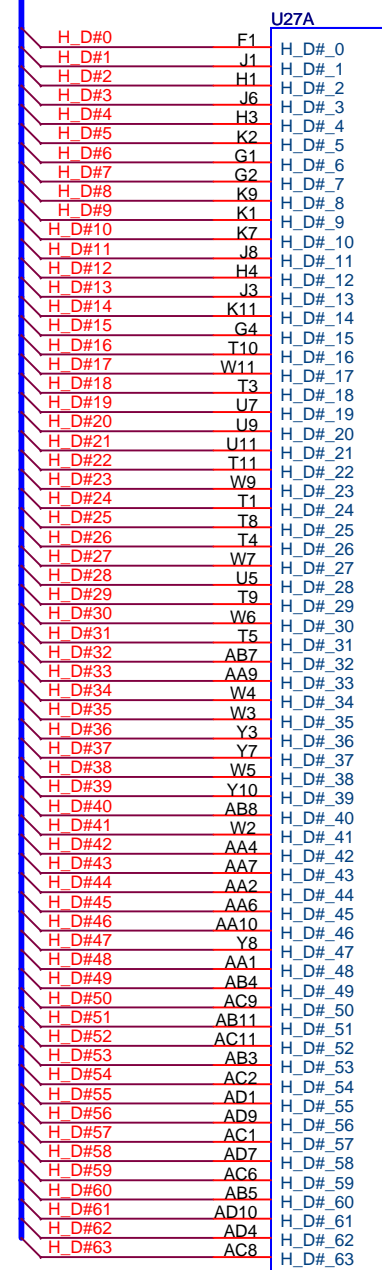


+1.05VRUN



w/s = 10/20mil

4 H_D#[63..0] H_D#[63..0]



GM QG88CGM 12-0G88CGM-0000
 PM QG88CPM 12-0G88CPM-0000
 GML 940GML-QR60-A3 12-940GML0-A300

HOST

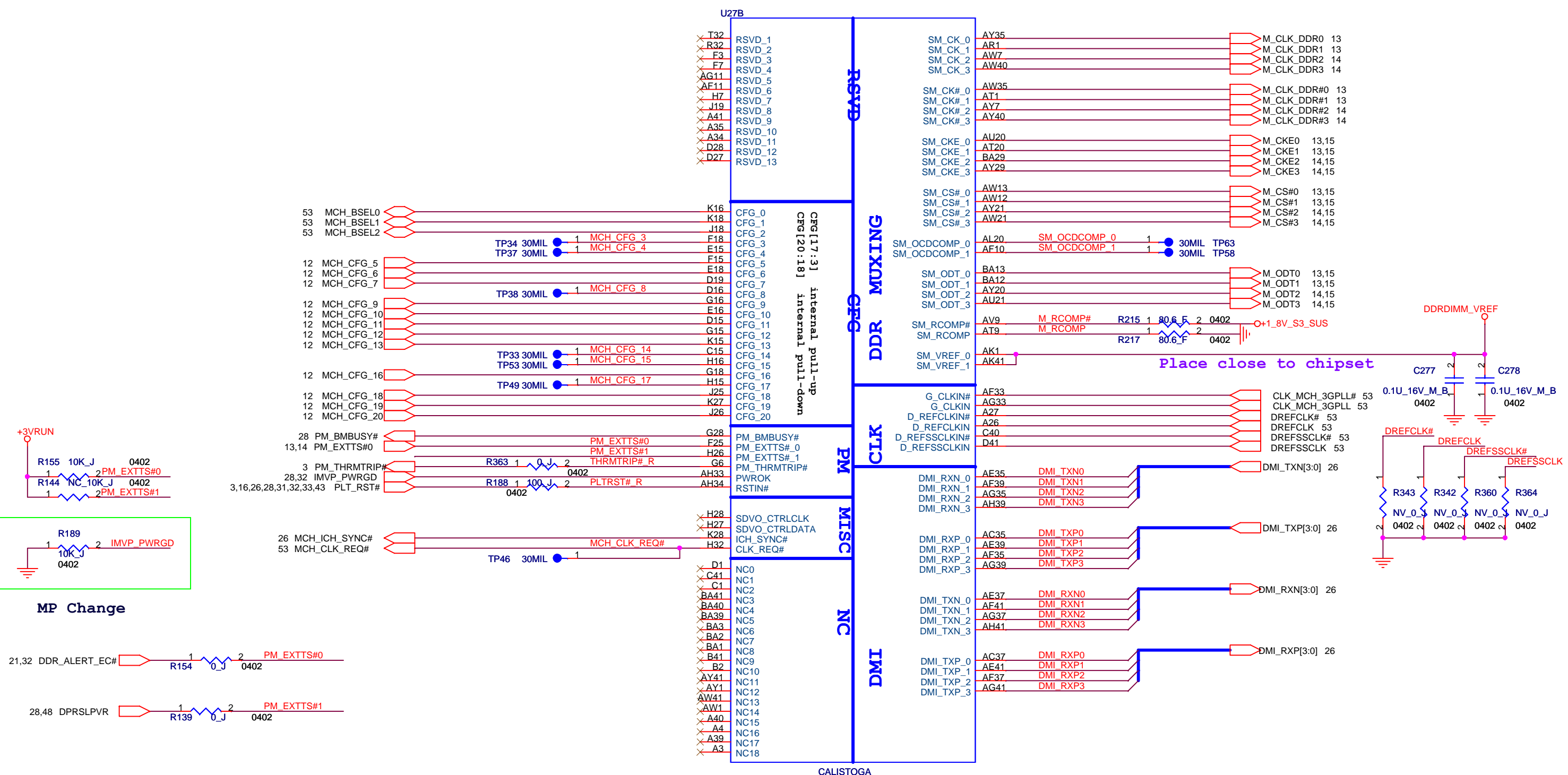
Place Cap. near GMCH within 100 mils.

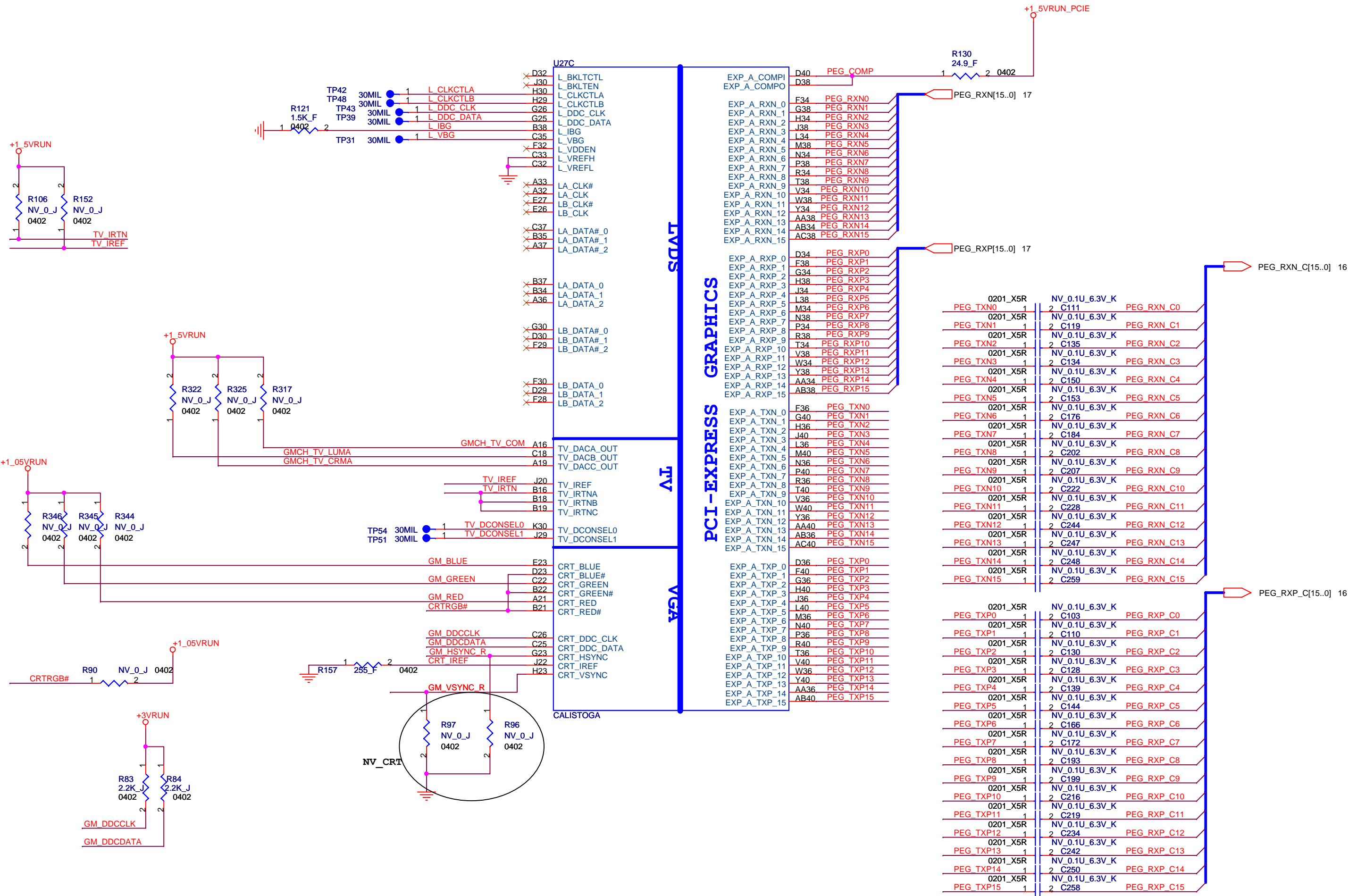
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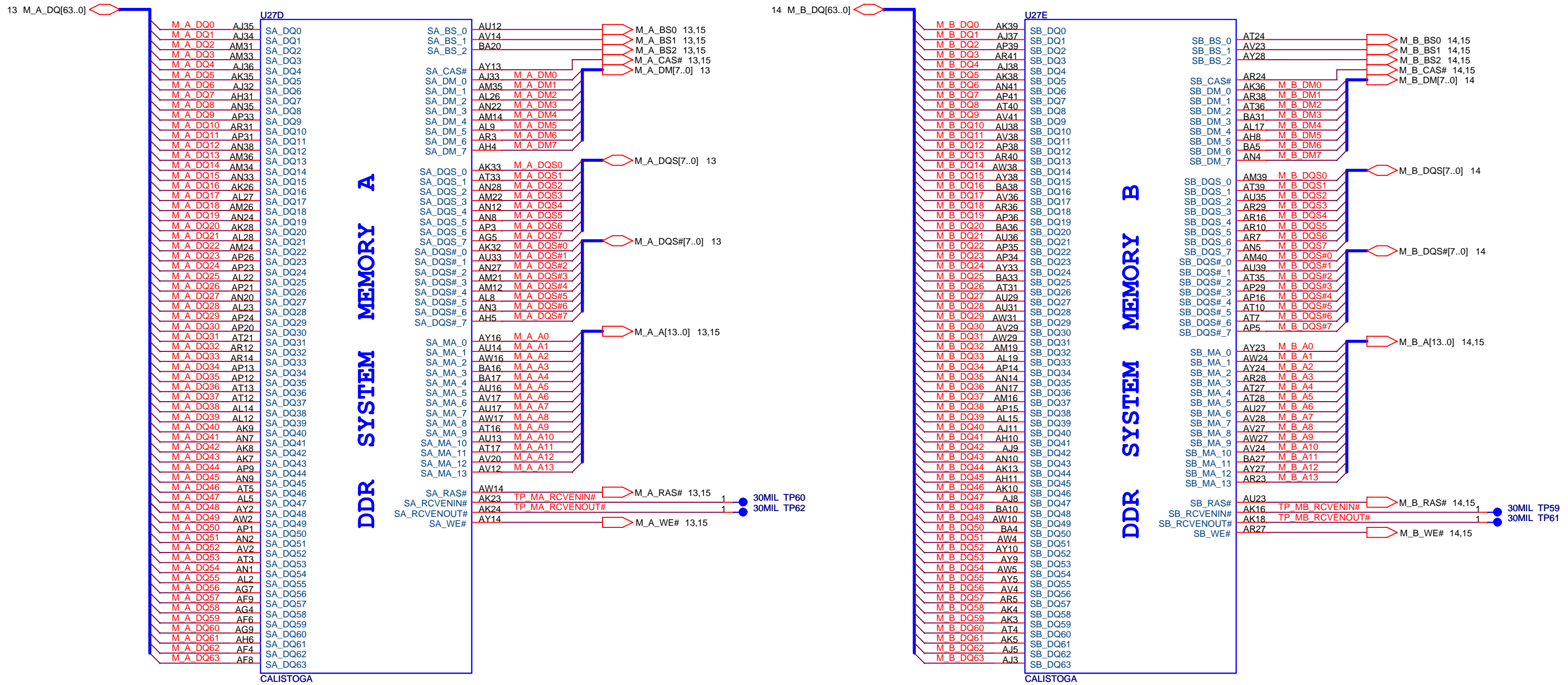
Title: **CALISTOHA (HOST)**

Size: A3 Document Number: **MS60-1-01 (MBX-159)** Rev: 0.30

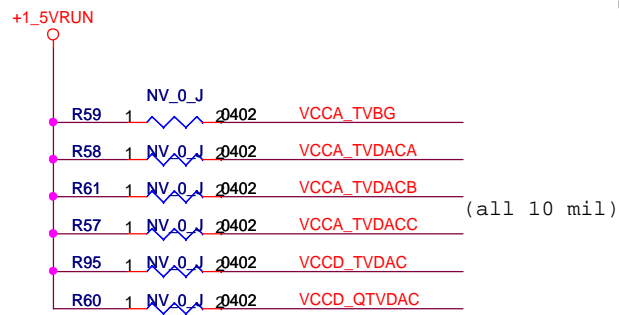
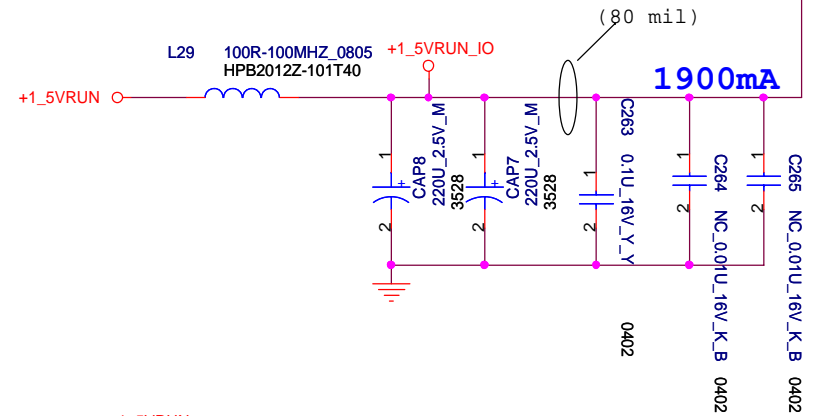
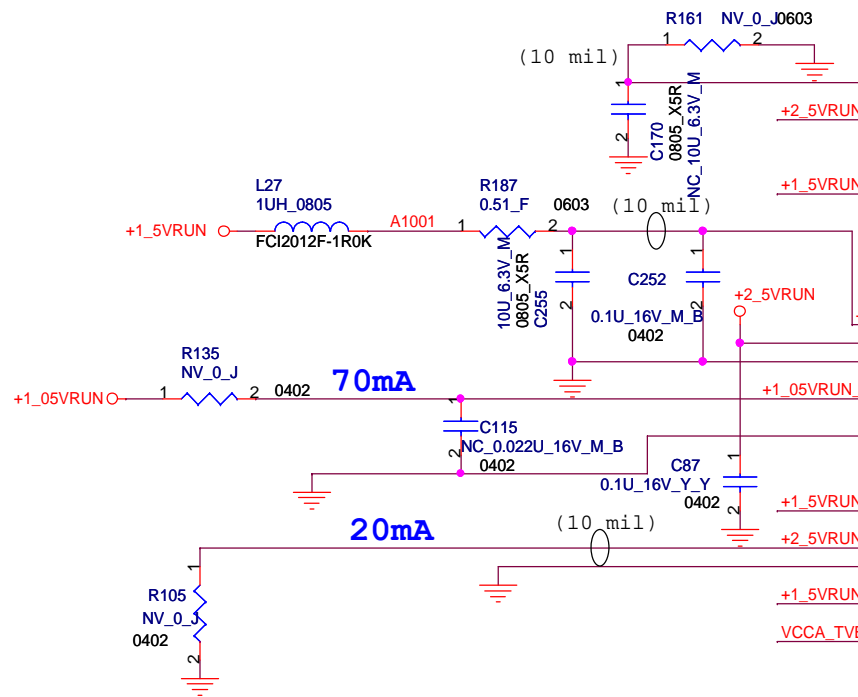
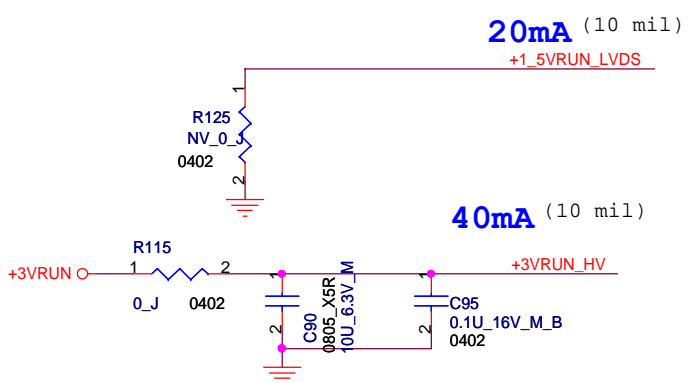
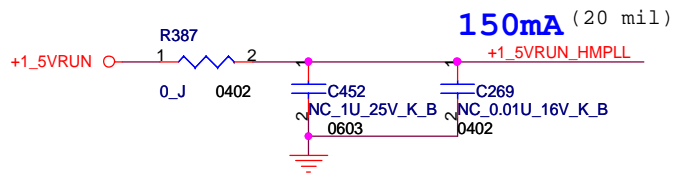
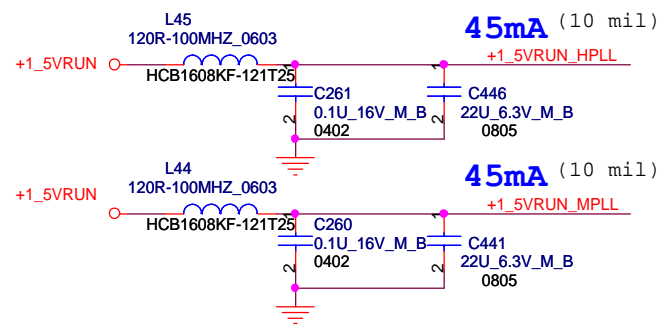
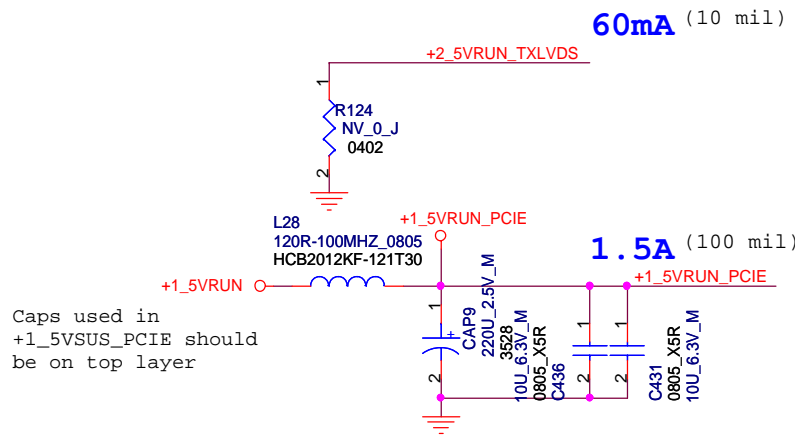
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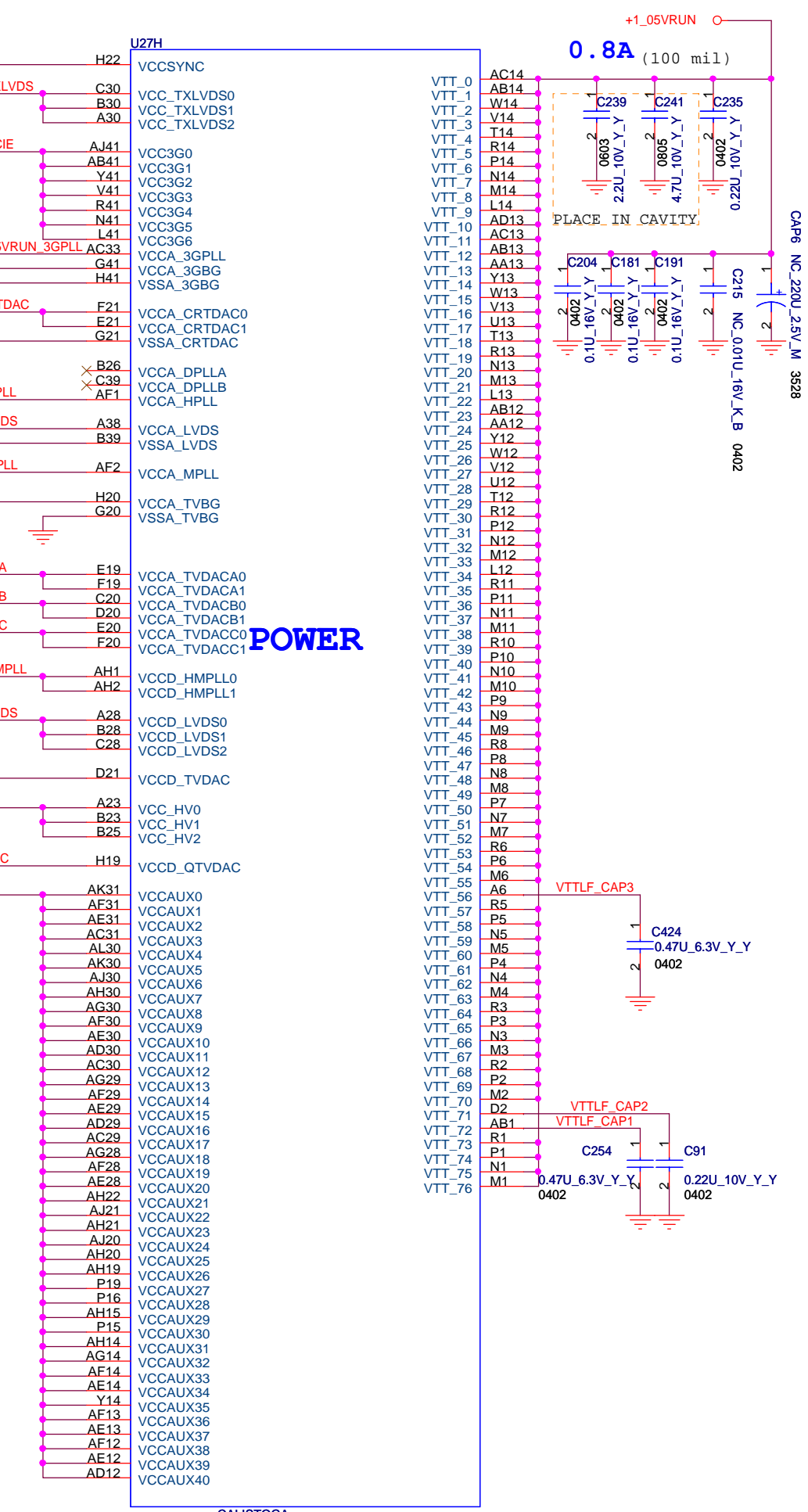




NOTE:
0.1uF caps in
1.5xPLL need to be
located as edge caps
within 200mils



GMCH TV-OUT Disable

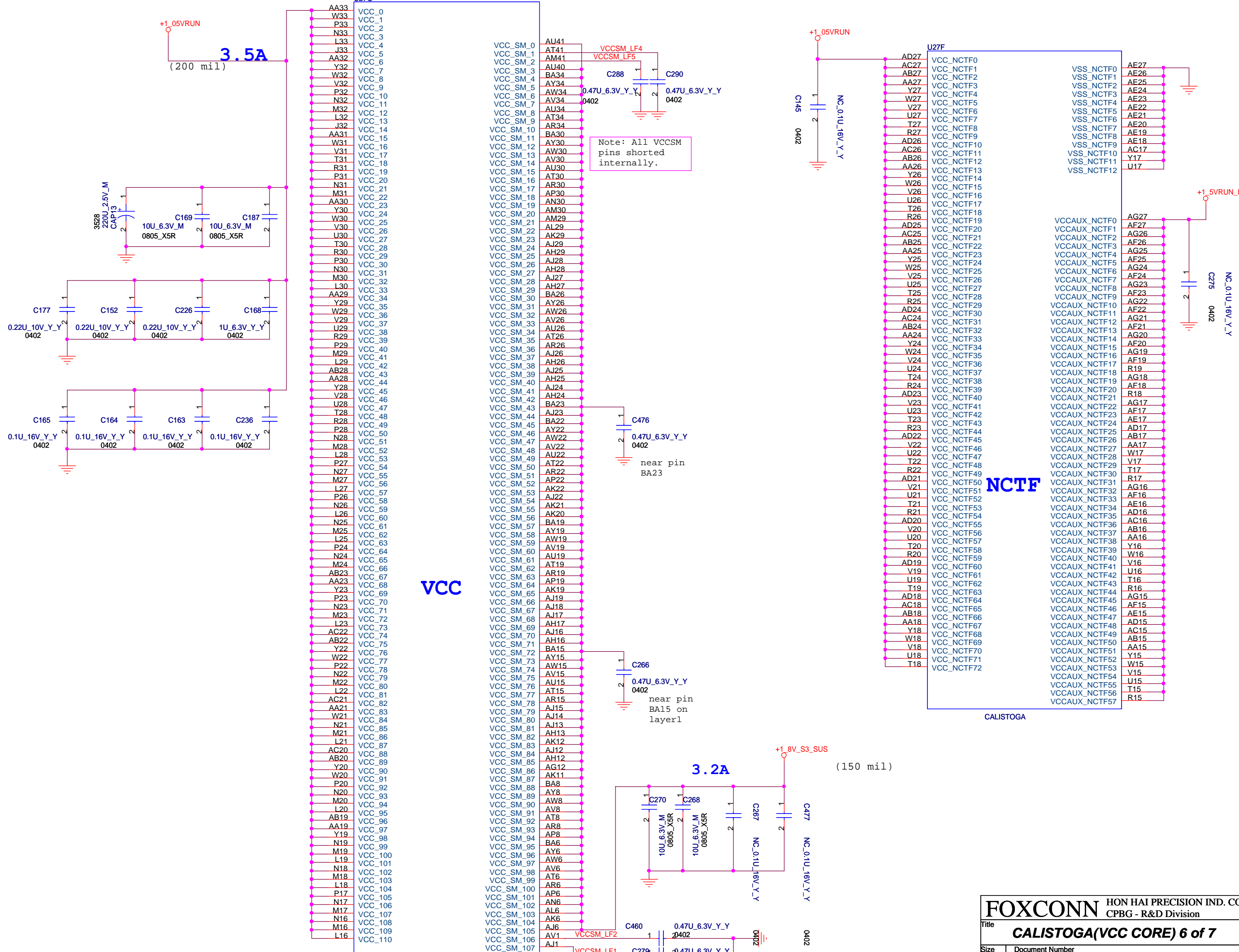


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CPBG - R&D Division

Title: **CALISTOGA(POWER,VCC) 5 of 7**

Size: Document Number
Custor: **MS60-1-01 (MBX-159)** Rev: 0.30

Date: Wednesday, October 04, 2006 Sheet: 10 of 56



Note: All VCCSM pins shorted internally.

NCTF

VCC

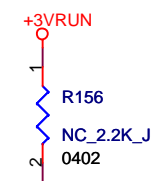
CALISTOGA

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	CALISTOGA(VCC CORE) 6 of 7	
Size	Document Number	Rev
Custom	MS60-1-01 (MBX-159)	0.30
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7 MCH_CFG_5 ← 1 ● 30MIL TP45

MCH_CFG_5	Low = DMIx2 High = DMIx4
-----------	-----------------------------

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------



7 MCH_CFG_6 ← 1 ● 30MIL TP40

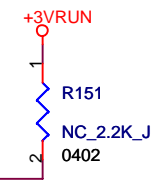
MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	-------------------------------------------------------------------

7 MCH_CFG_18 ←

7 MCH_CFG_7 ← 1 ● 30MIL TP36

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
--------------------------	---------------------------------------------

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
-----------------------------------	------------------------------------------------



7 MCH_CFG_19 ←

7 MCH_CFG_9 ←

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation
-----------------------------------	-----------------------------------------------



MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults) High = SDVO and PCIE x1 are operating simultaneously via the PEG port
-----------------------------------------------------	-------------------------------------------------------------------------------------------------------------------------------

For layout convenience

7 MCH_CFG_10 ← 1 ● 30MIL TP35

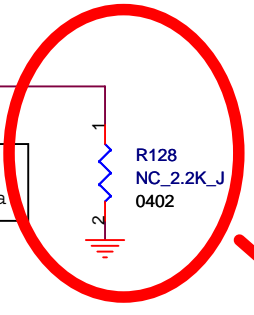
MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
-------------------------------------	-----------------------------------

7 MCH_CFG_20 ← 1 ● 30MIL TP52

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

7 MCH_CFG_11 ←

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High = Calistoga
-----------------------------------	------------------------------------



7 MCH_CFG_12 ← 1 ● 30MIL TP47

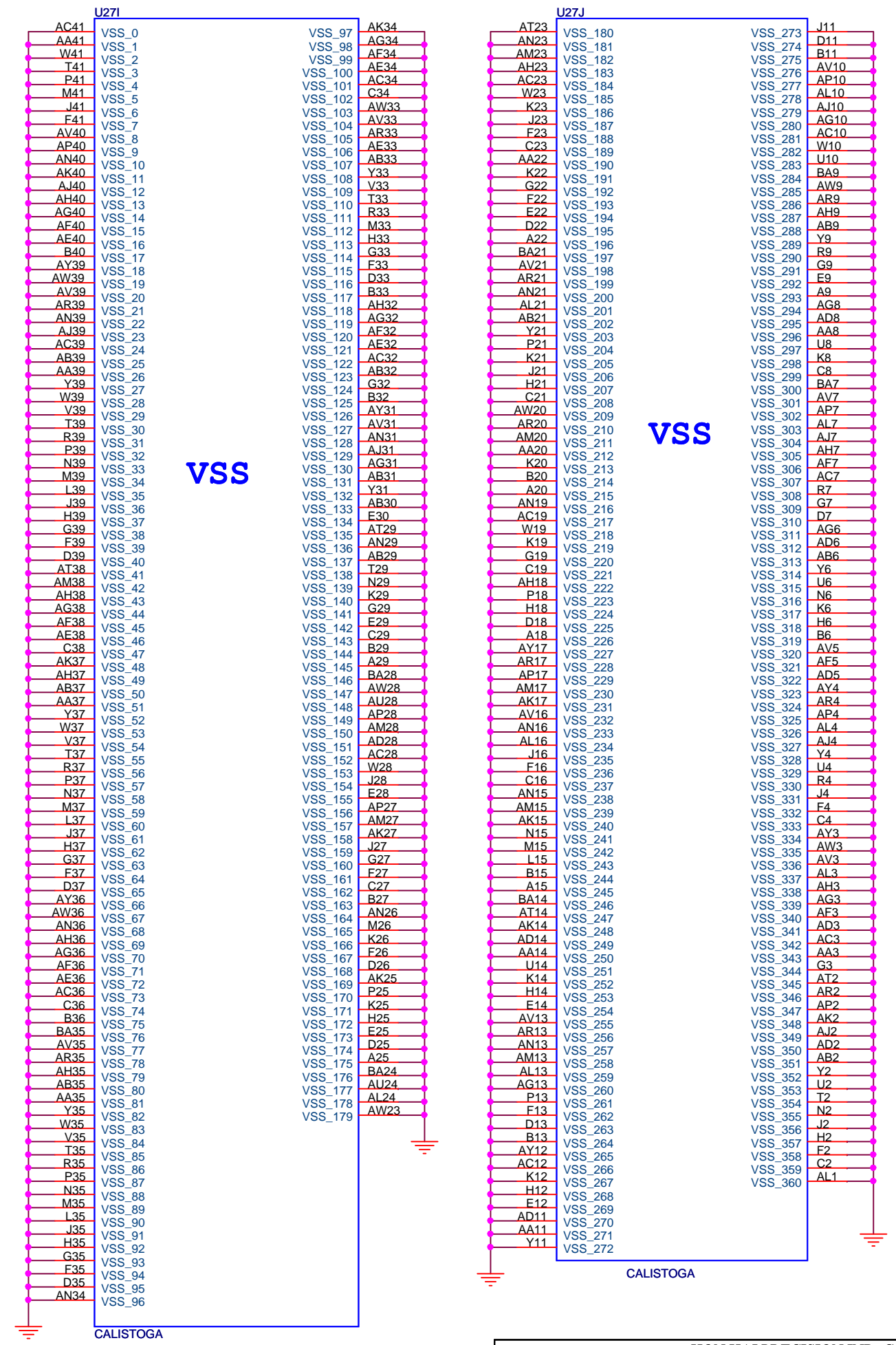
7 MCH_CFG_13 ← 1 ● 30MIL TP55

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
-------------------------------	---------------------------------------------------------------------------------------------------------------

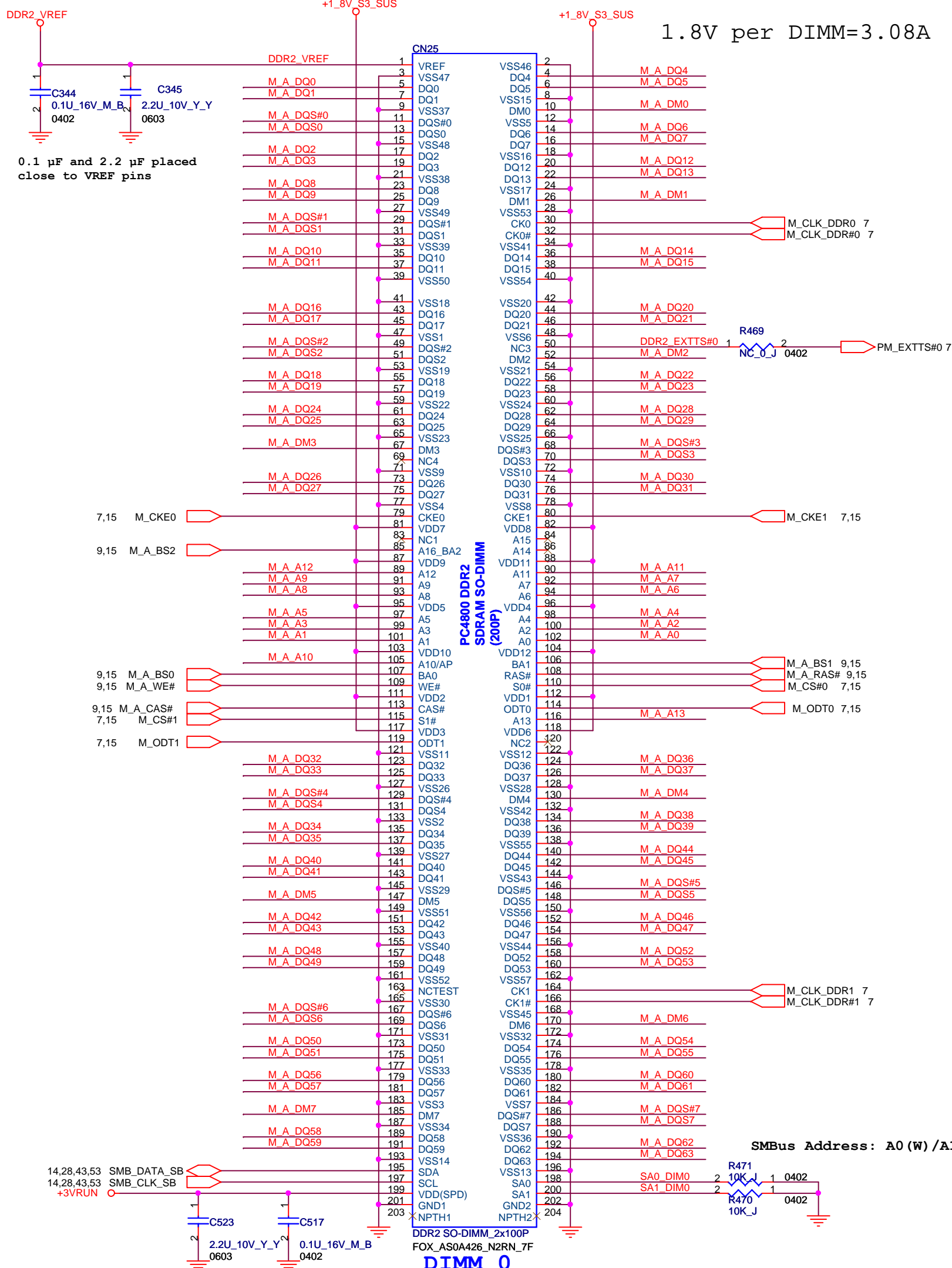
Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

7 MCH_CFG_16 ← 1 ● 30MIL TP44

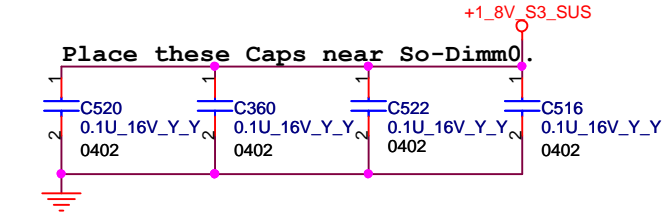
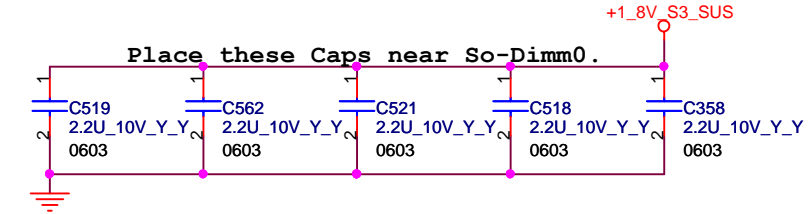
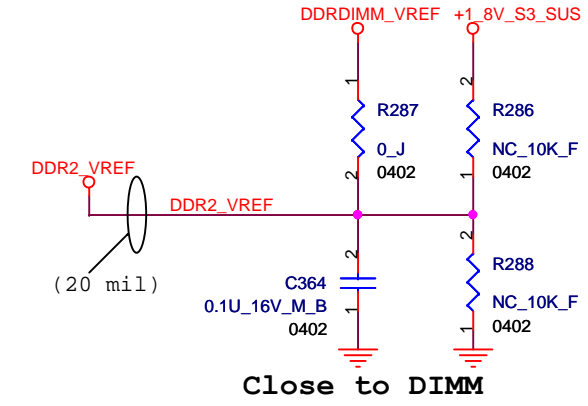
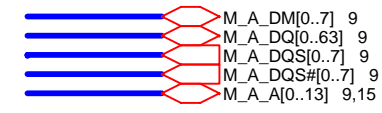
MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
---------------------------------	---------------------------------------------------------



1.8V per DIMM=3.08A

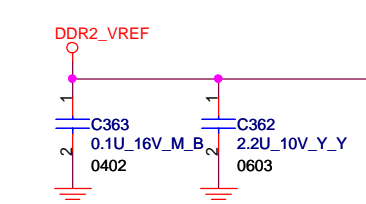


0.1 μF and 2.2 μF placed close to VREF pins



SMBus Address: A0 (W) / A1 (R)

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title DDR(II)SO-DIMM_0		
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 0.30
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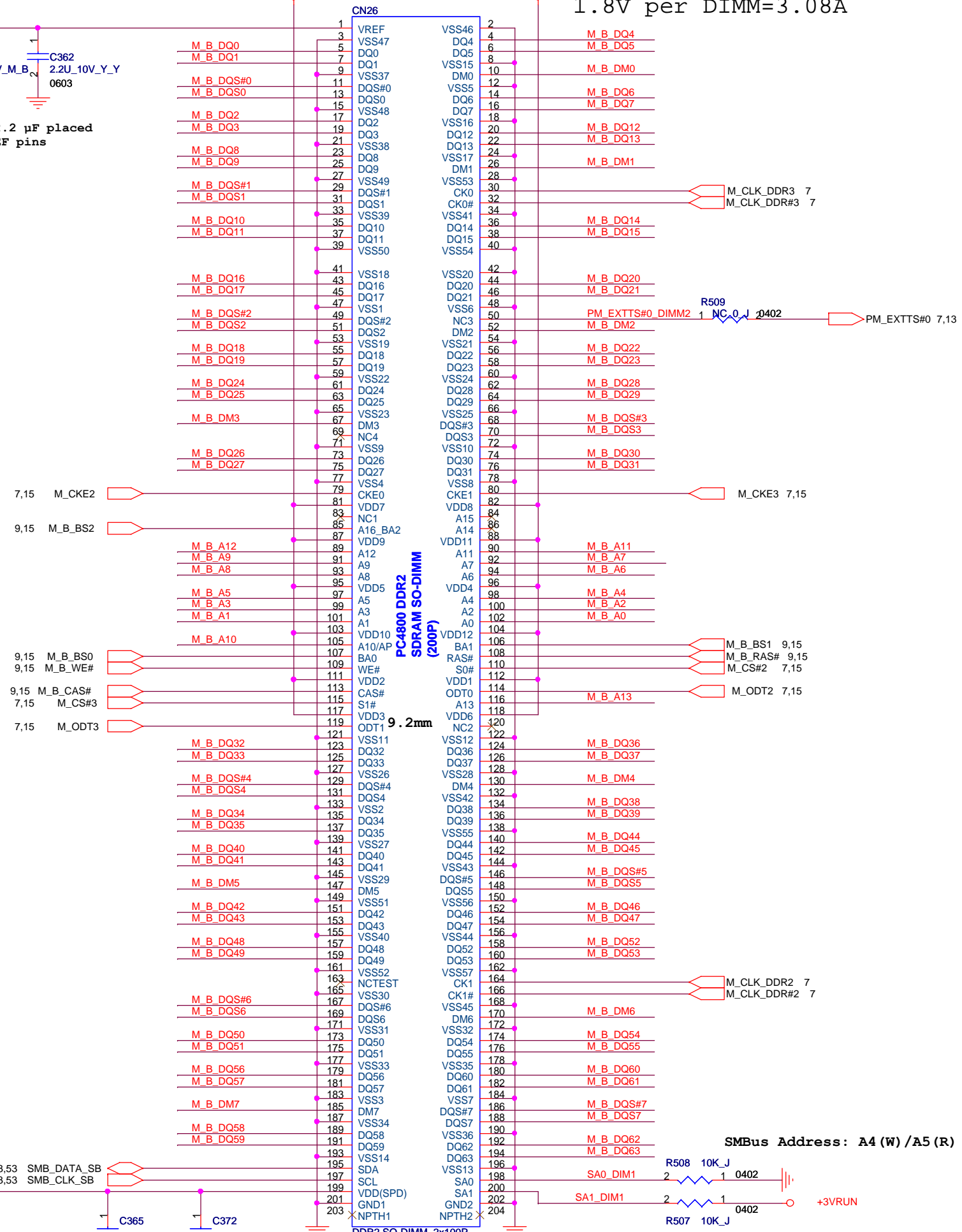
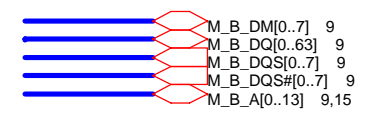


0.1 μ F and 2.2 μ F placed close to VREF pins

+1.8V_S3_SUS

+1.8V_S3_SUS

1.8V per DIMM=3.08A

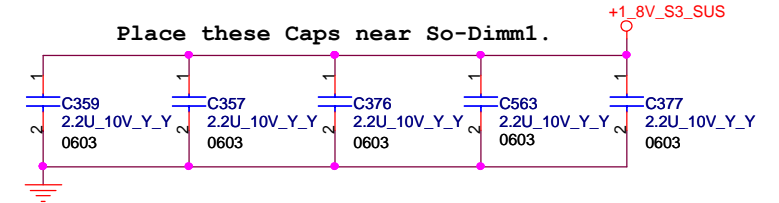


PC4800 DDR2
SDRAM SO-DIMM
(200P)
9.2mm

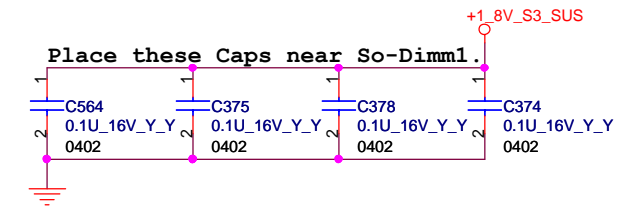
DIMM_1

SMBus Address: A4 (W) / A5 (R)

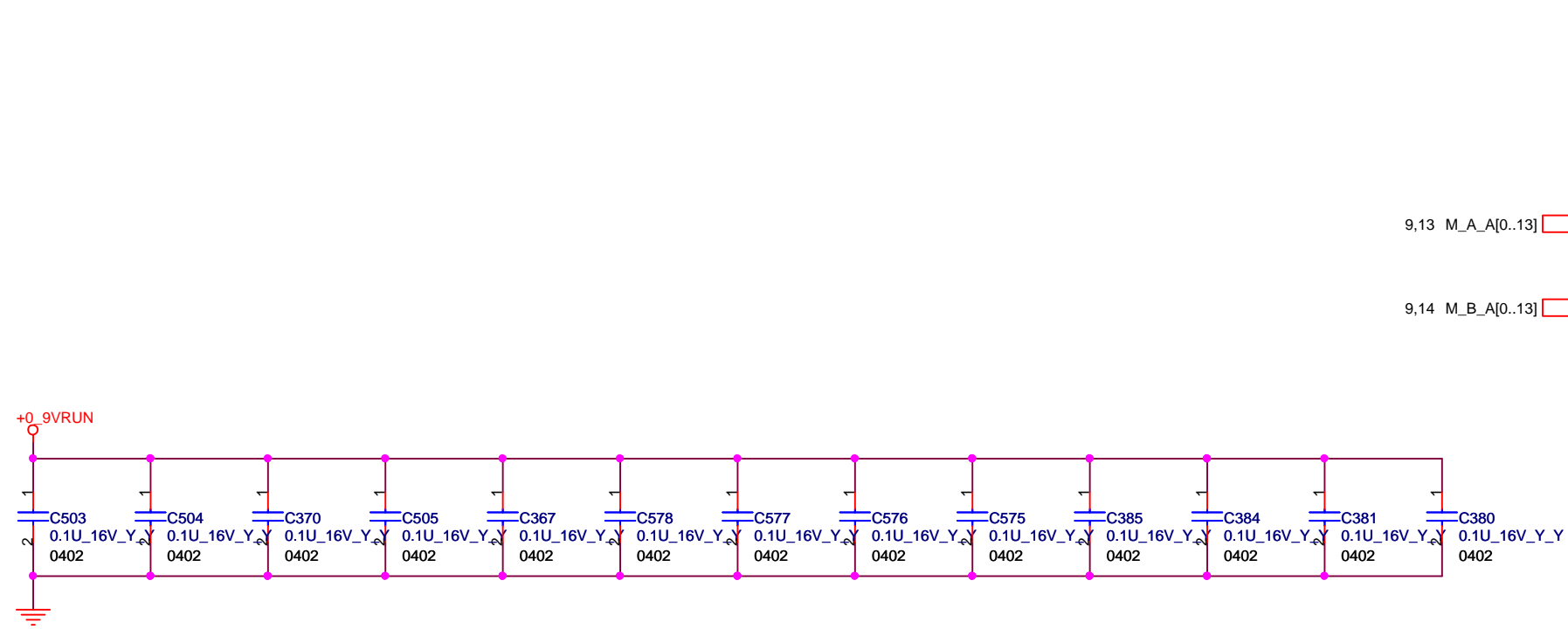
Place these Caps near So-Dimm1.



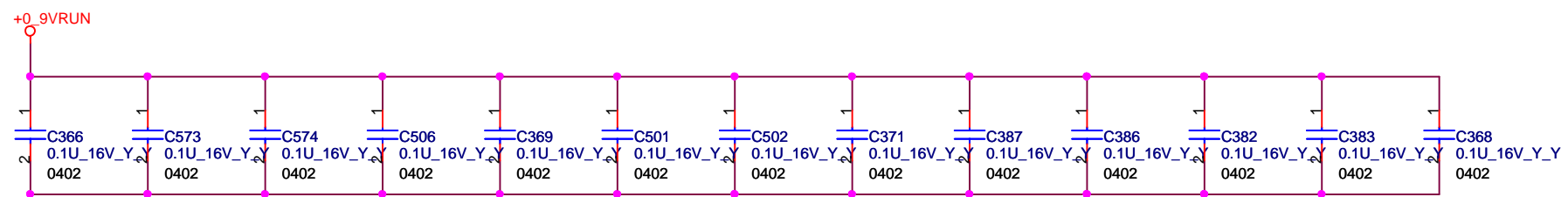
Place these Caps near So-Dimm1.



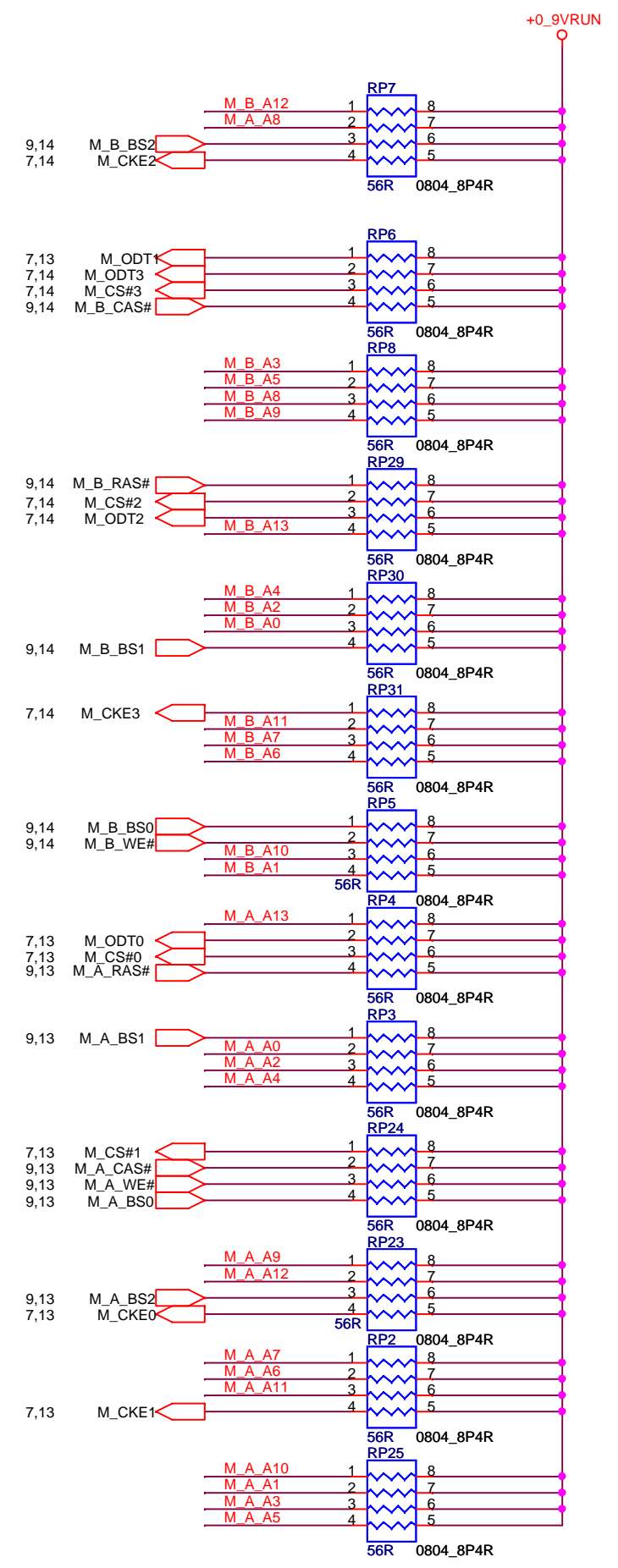
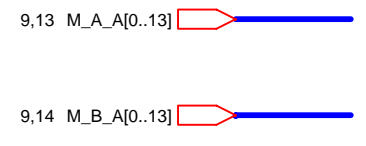
FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title DDR(II)SO-DIMM_1	
Size	Document Number
Custom	MS60-1-01 (MBX-159)
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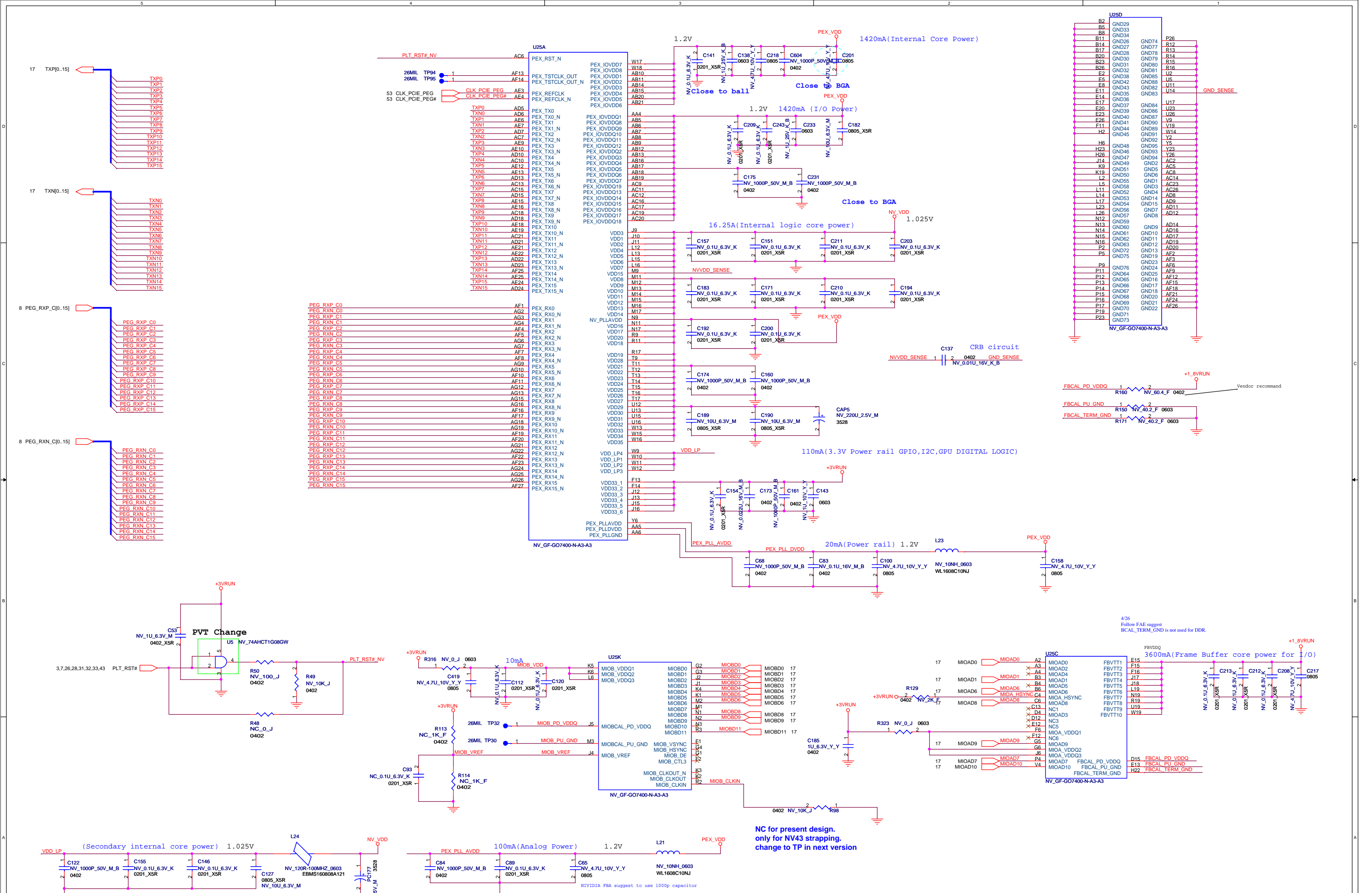


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



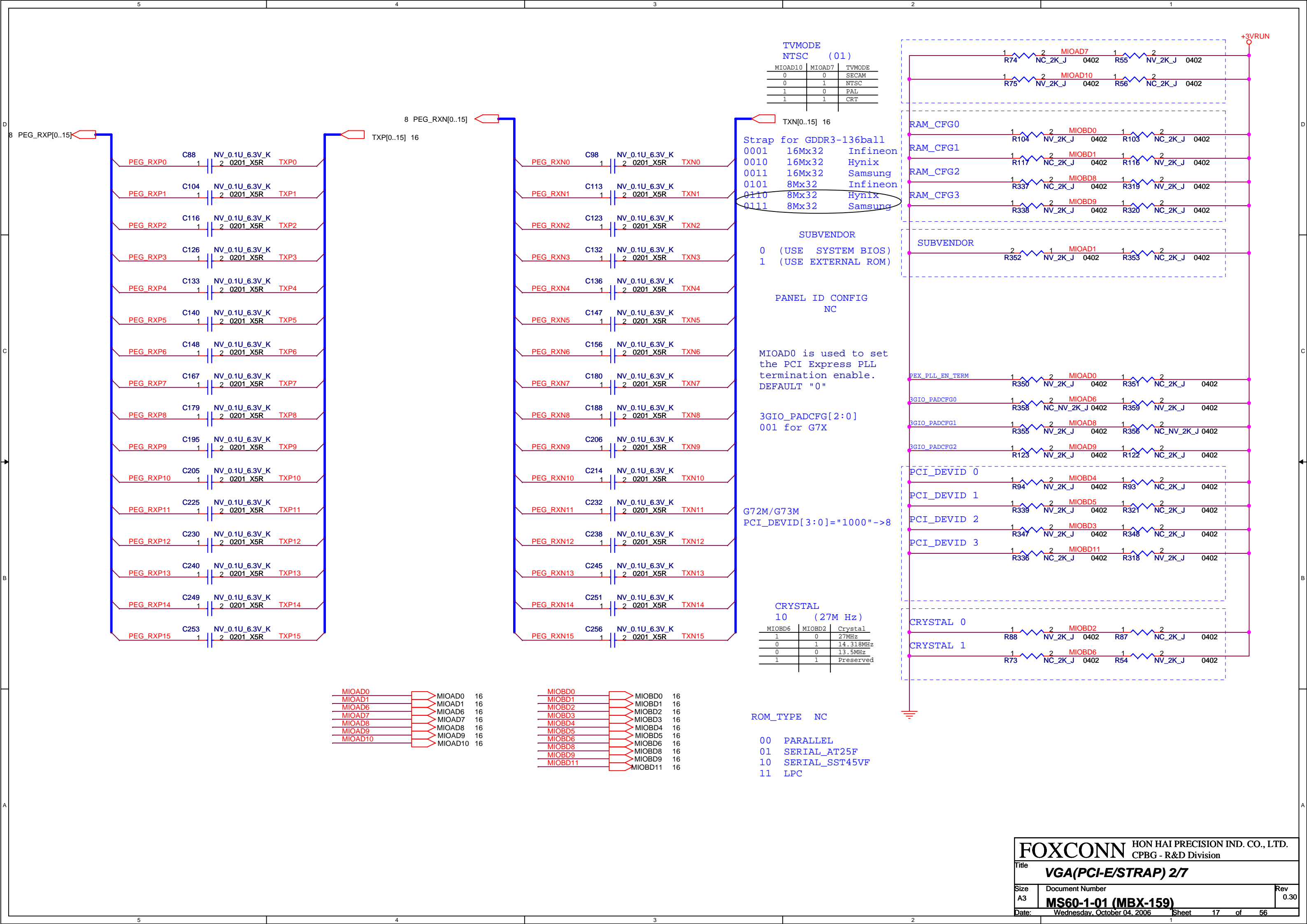
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN





NC for present design. only for NV43 strapping. change to TP in next version

4/26 Follow FAE suggest BICAL_TERM_GND is not used for DDR.



TVMODE
NTSC (01)

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball

0001	16Mx32	Infineon
0010	16Mx32	Hynix
0011	16Mx32	Samsung
0101	8Mx32	Infineon
0110	8Mx32	Hynix
0111	8Mx32	Samsung

SUBVENDOR

0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

PANEL ID CONFIG
NC

MIOAD0 is used to set the PCI Express PLL termination enable. DEFAULT "0"

3GIO_PADCFG[2:0]
001 for G7X

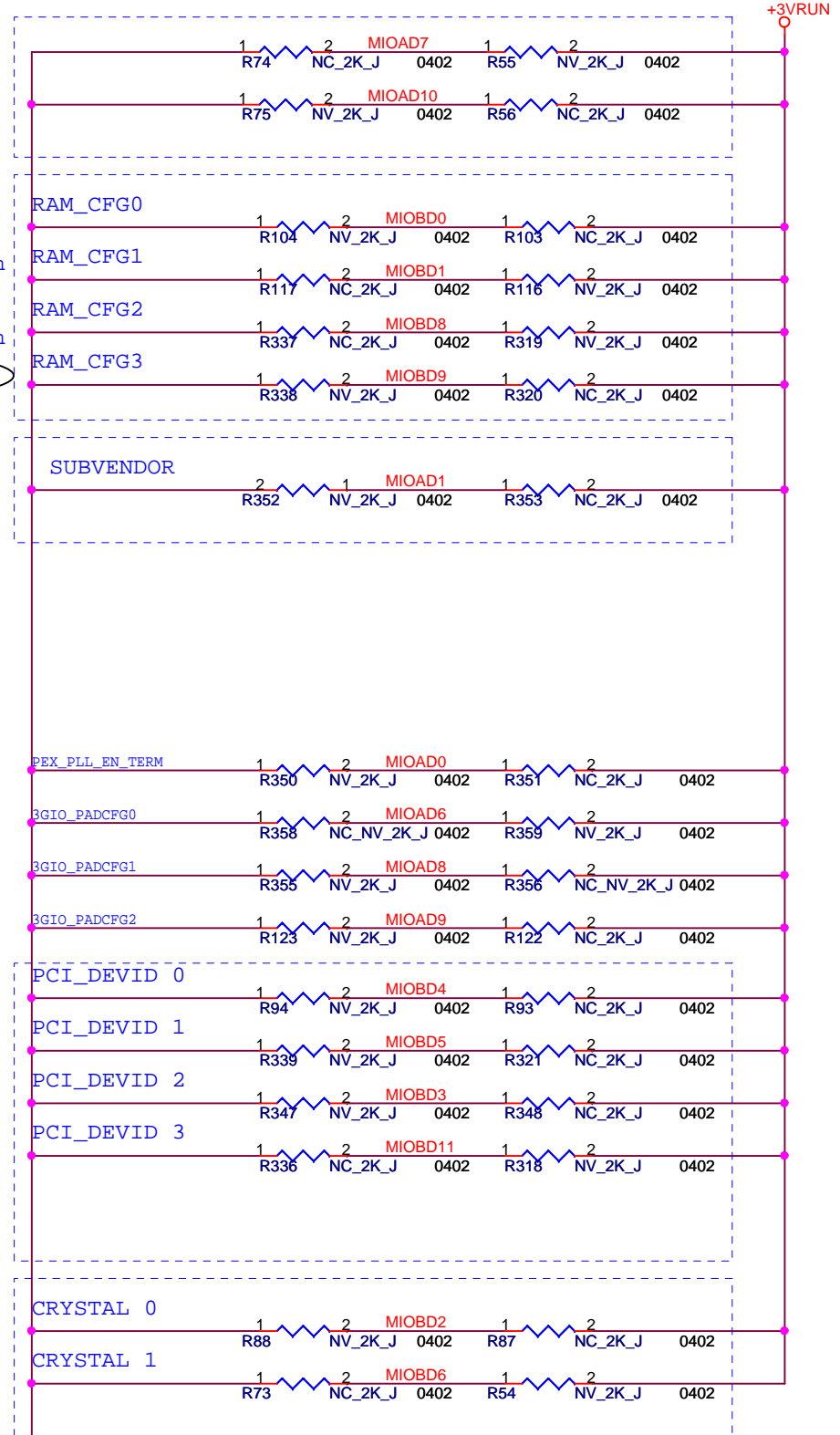
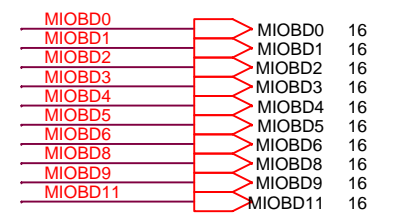
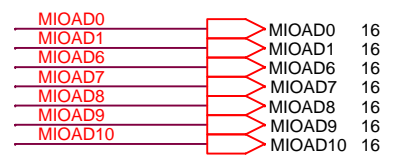
G72M/G73M
PCI_DEVID[3:0]="1000"->8

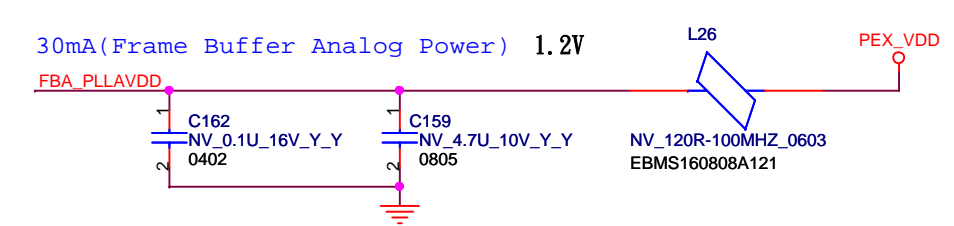
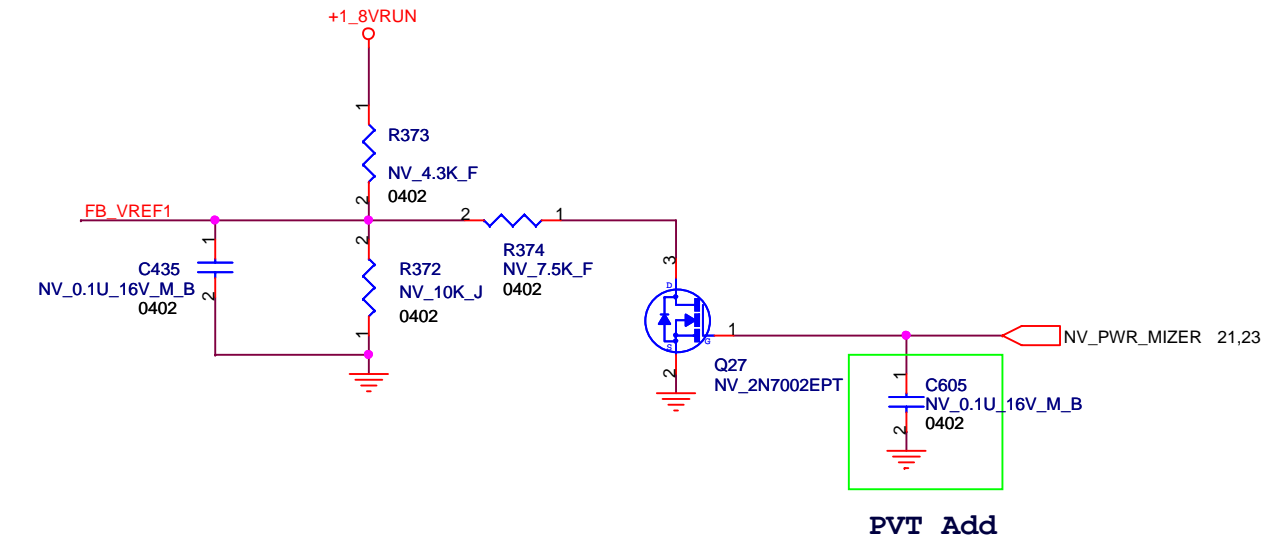
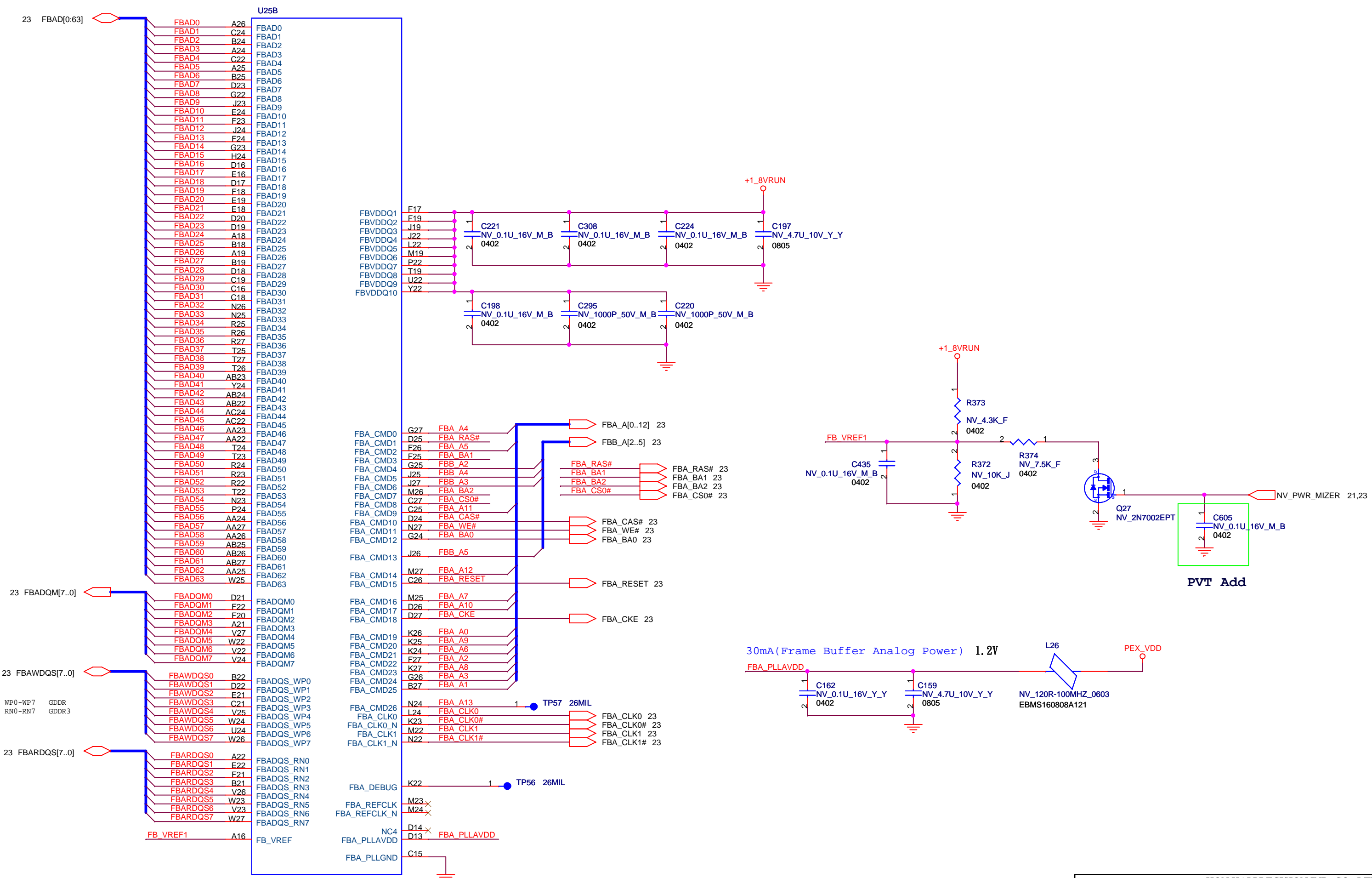
CRYSTAL
10 (27M Hz)

MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

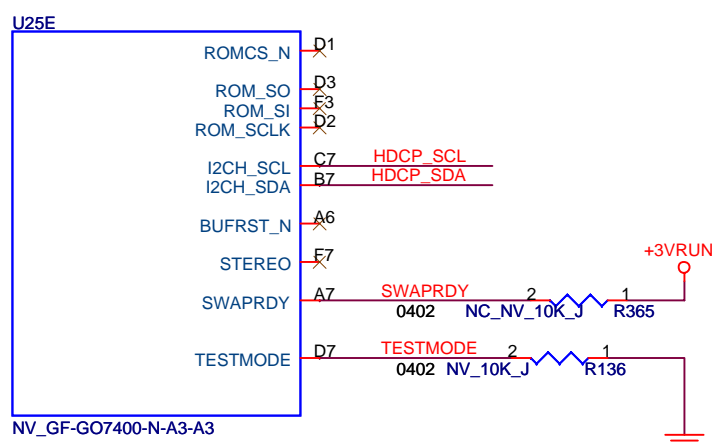
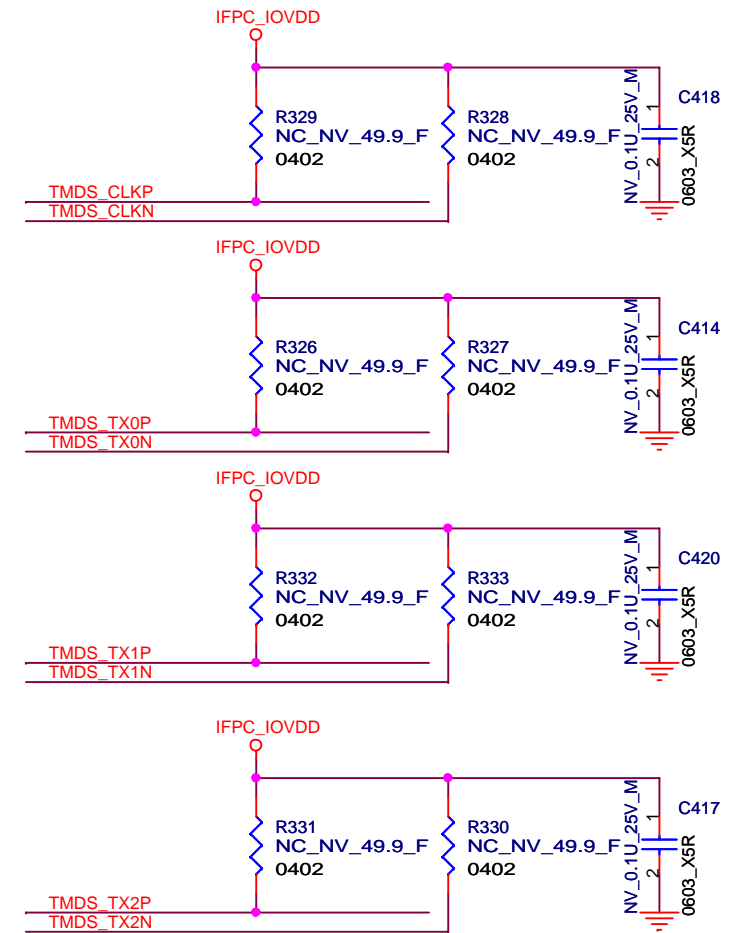
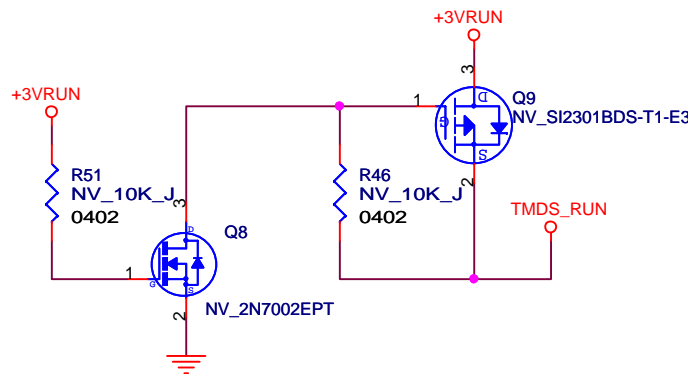
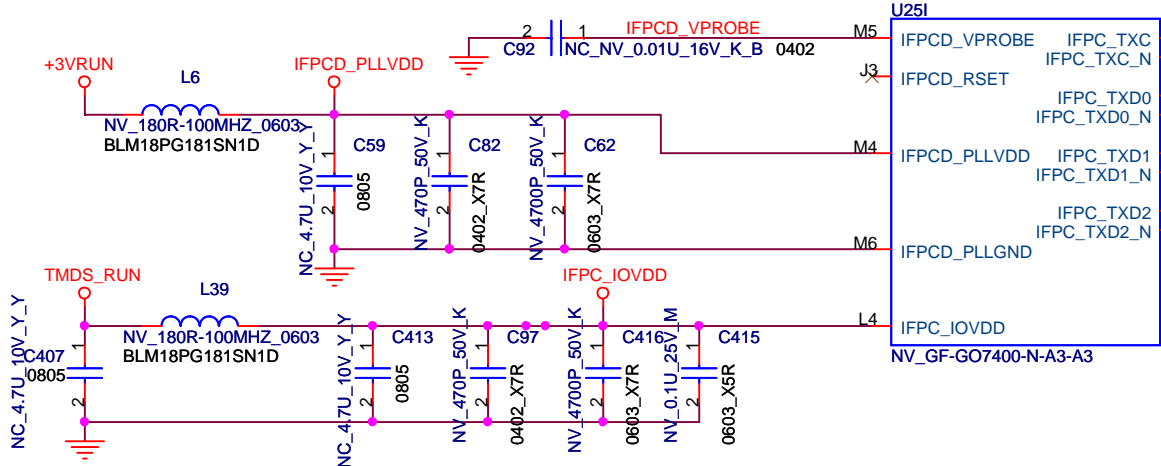
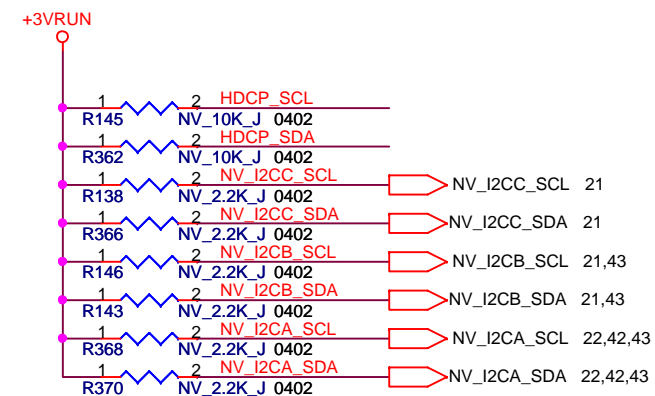
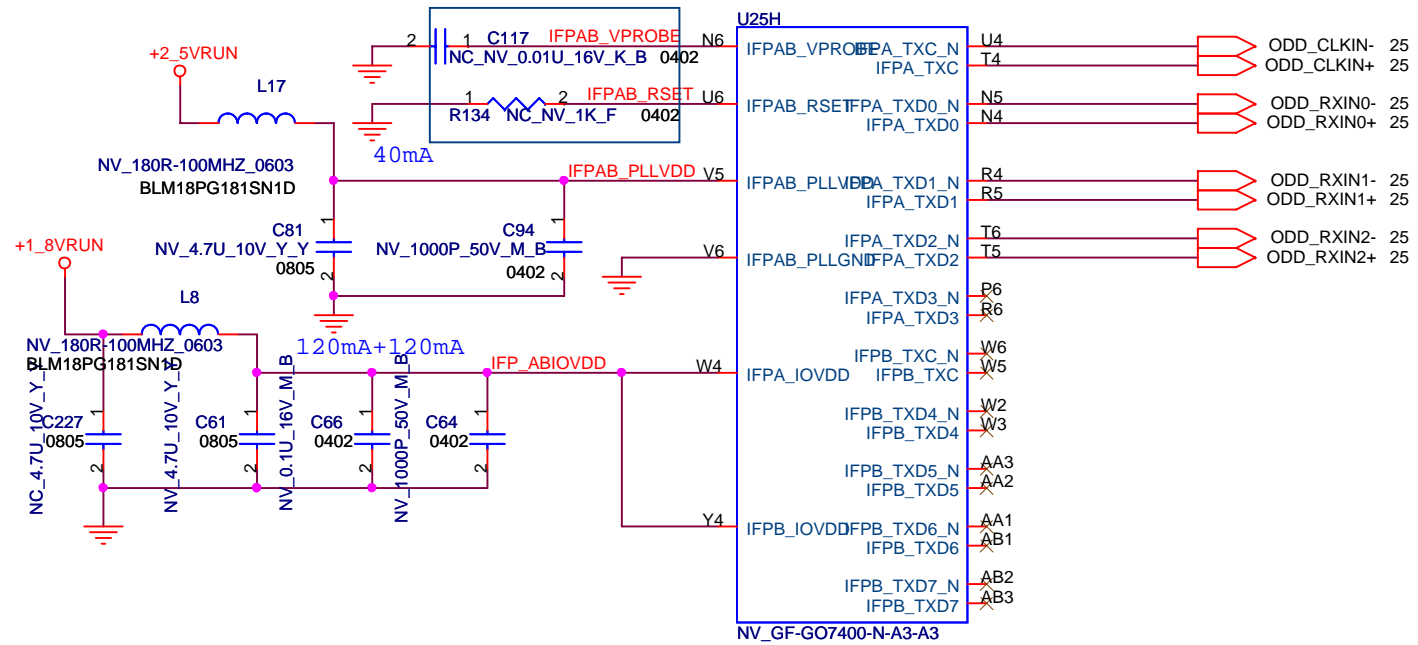
ROM_TYPE NC

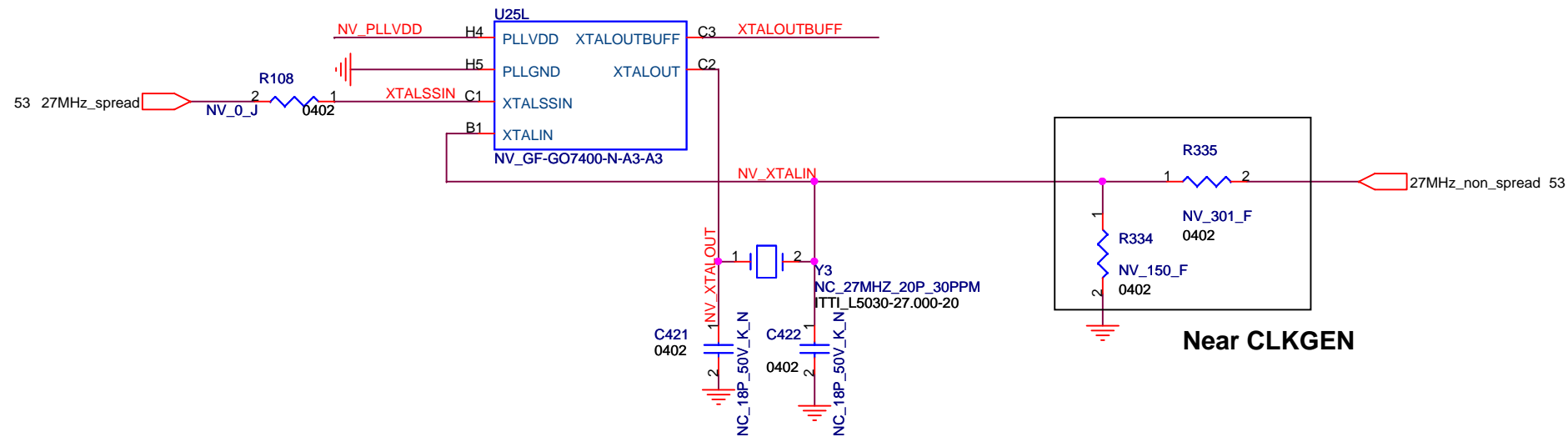
00 PARALLEL
01 SERIAL_AT25F
10 SERIAL_SST45VF
11 LPC



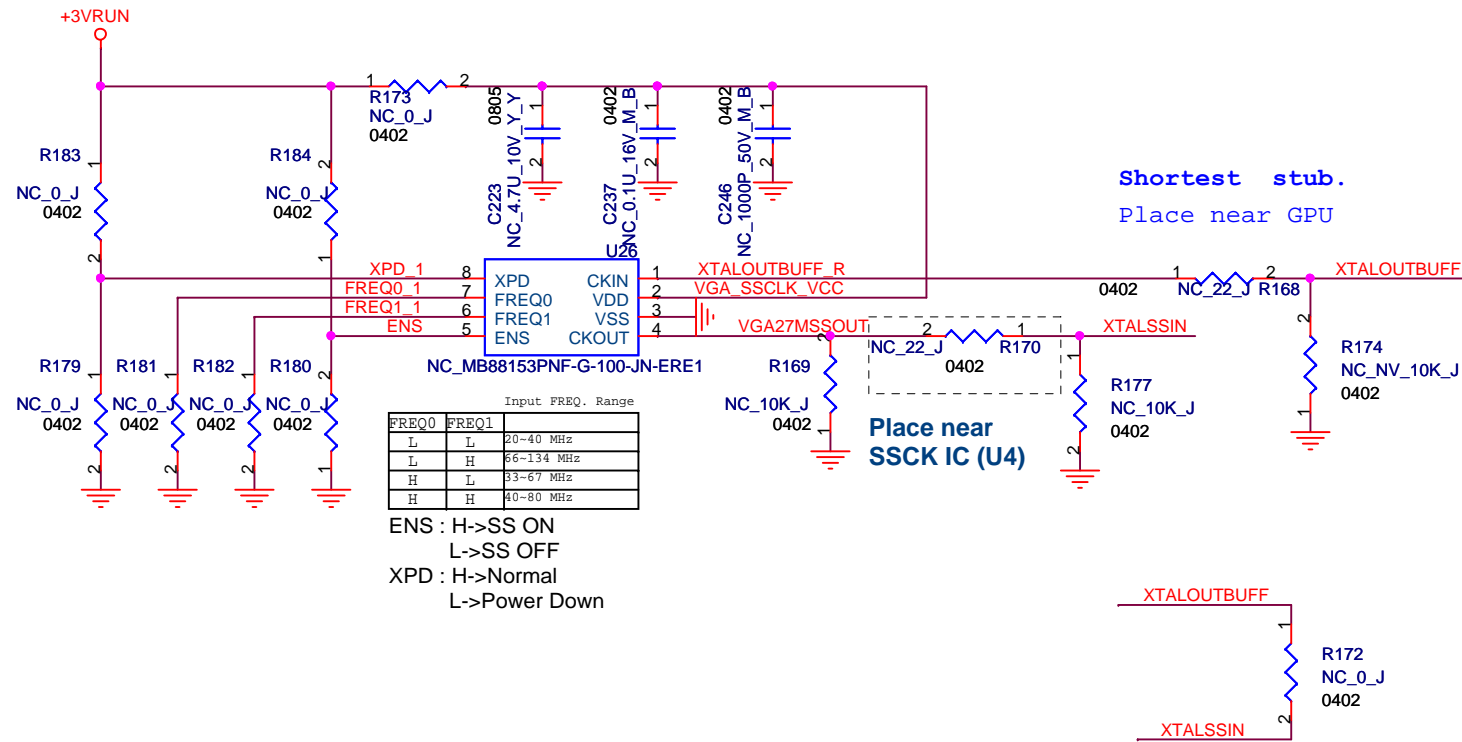
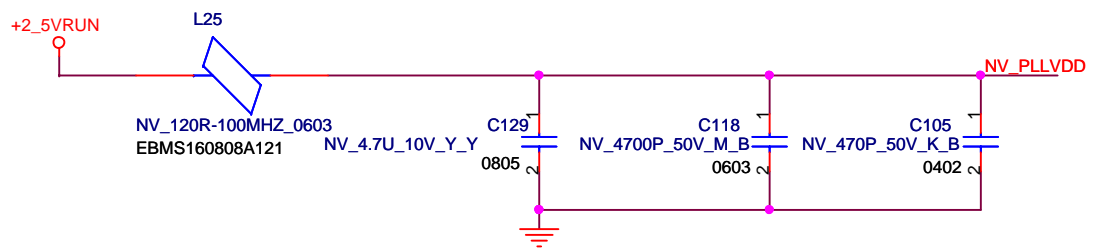


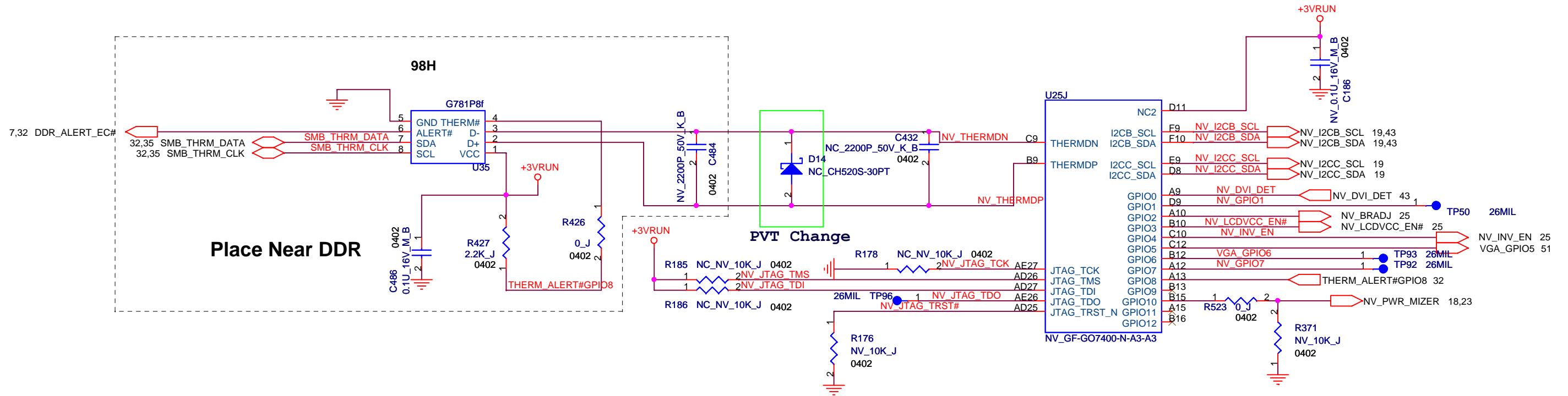
UN STUFF FOR G7X





Near CLKGEN





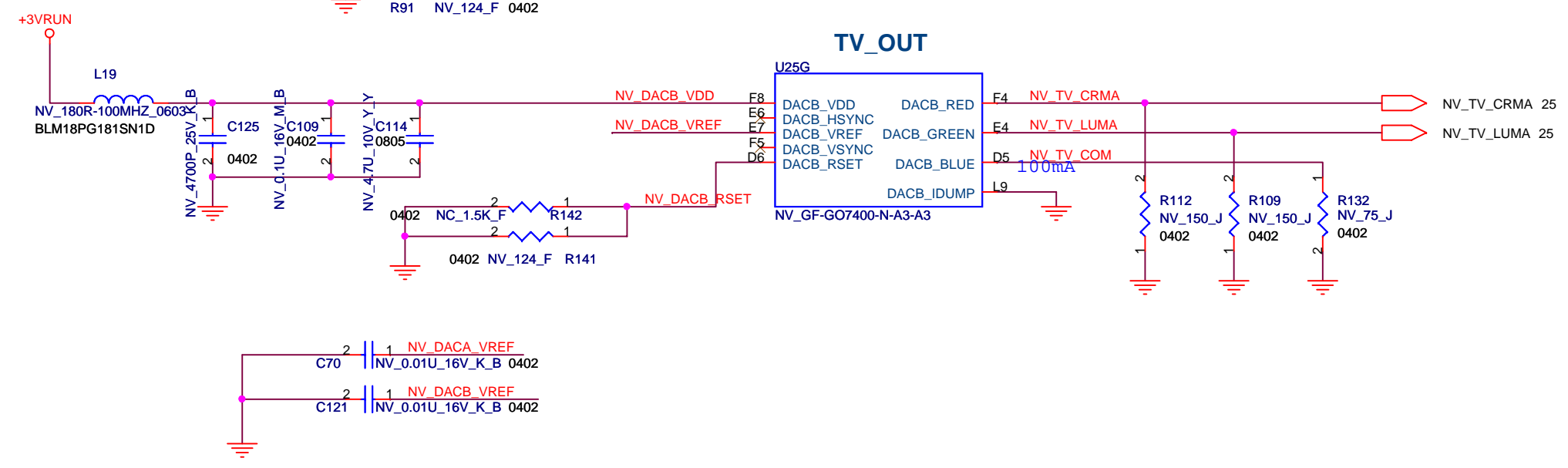
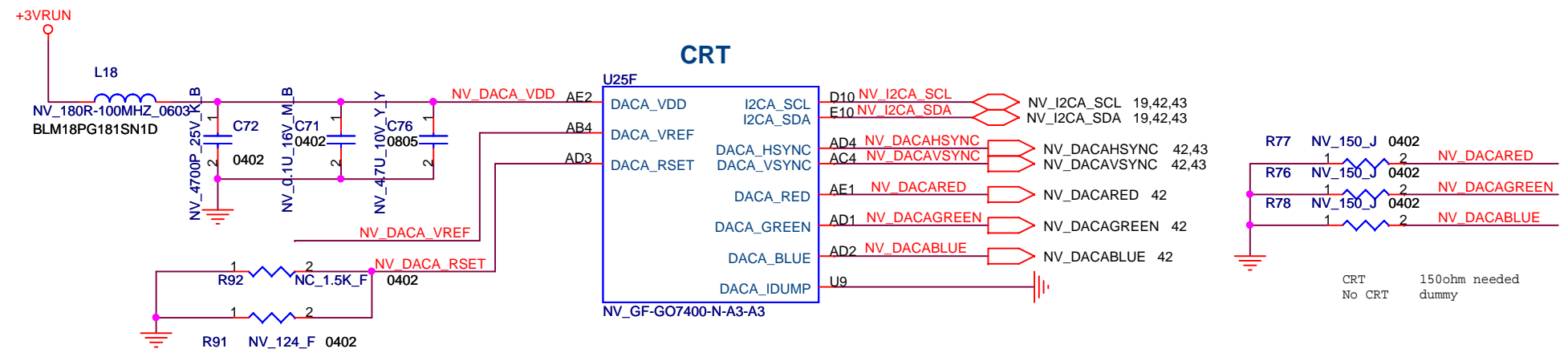
Place Near DDR

PVT Change

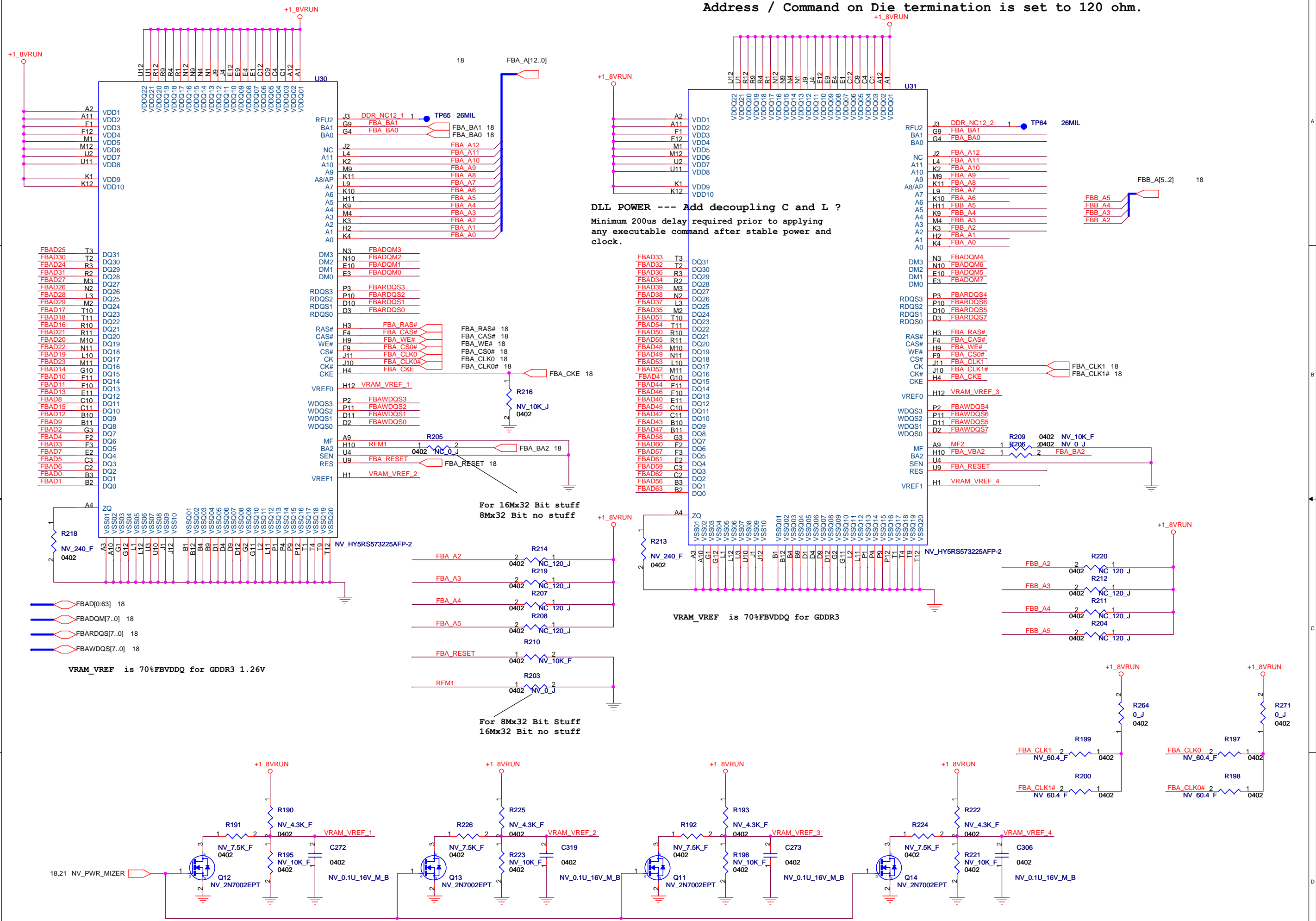
PWR_MIZER LEVEL	H	L
Vref	50% FBVDDQ	70% FBVDDQ

Check Spec.

I/O	Inter pull low	GPIO TABLE
GPIO0	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	Yes	Panel Brightness (PWM) Active High
GPIO3	No	Panel Power Active Low
GPIO4	Yes	Panel Backlight On/Off Active High
GPIO5	Yes	GPU Voltage CTL0 H: NVDD=1.1V
GPIO6	Yes	
GPIO7	Yes	MEM VID
GPIO8	No	Thermal Alert Active Low
GPIO9	No(Low)	Fan control. Support either PWM or on/off
GPIO10	No	Power Mizer control signal
GPIO11	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	No	Available for general use.



DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCLK			SCL
	VGA-DDCDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCLK			SCL
	DVI-DDCDATA			SDA



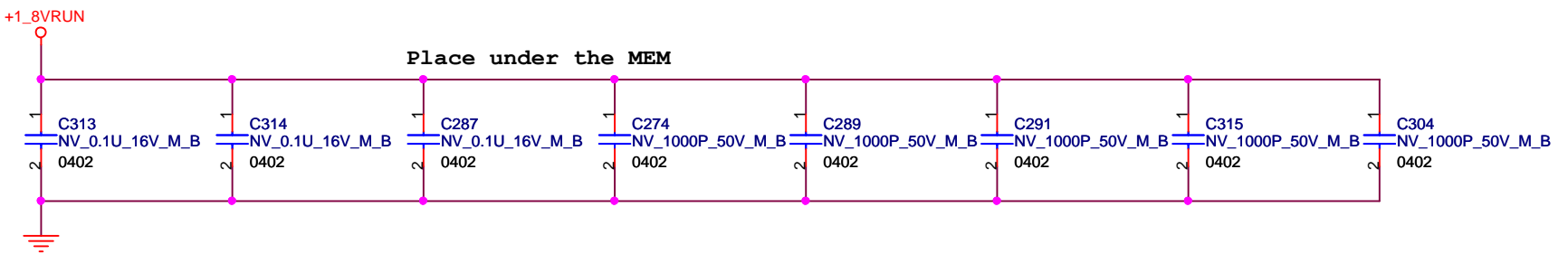
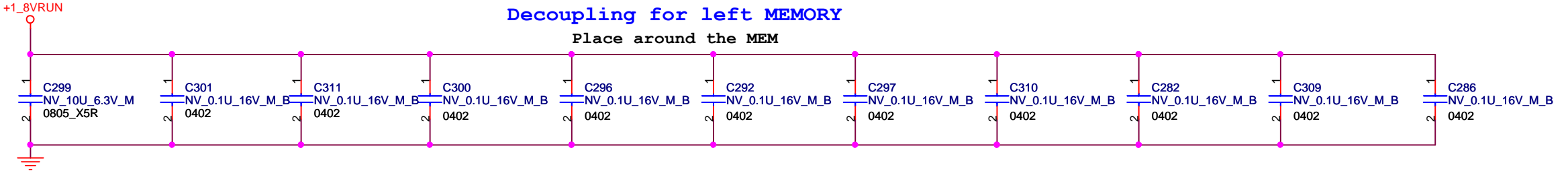
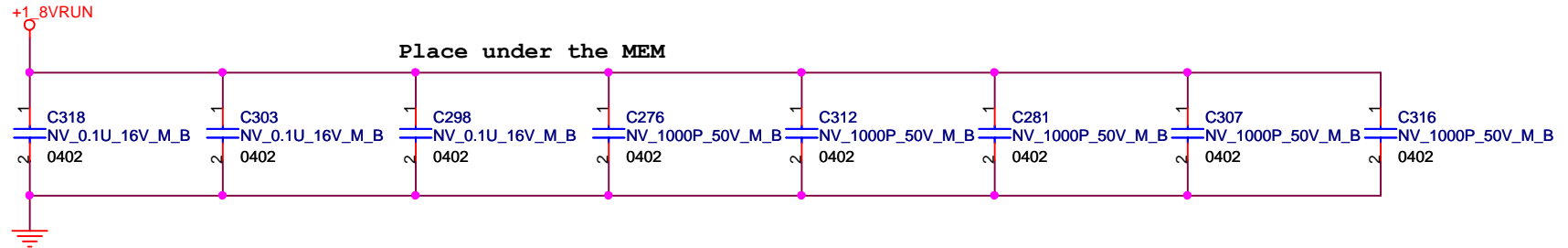
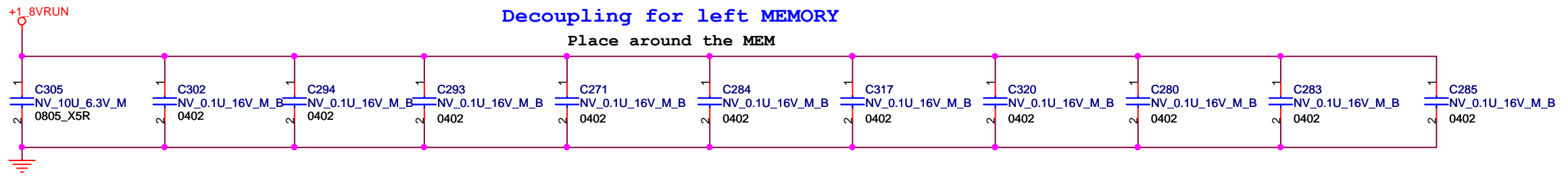
DLL POWER --- Add decoupling C and L ?
 Minimum 200us delay required prior to applying any executable command after stable power and clock.

For 16Mx32 Bit stuff
 8Mx32 Bit no stuff

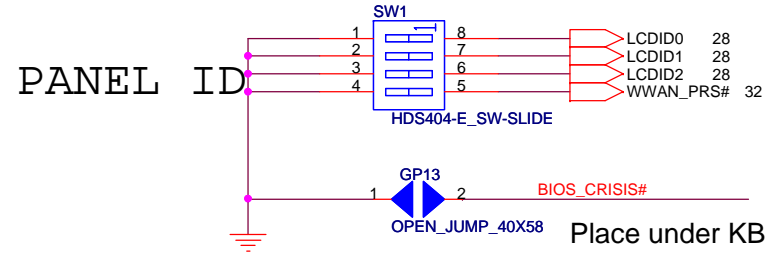
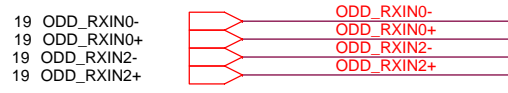
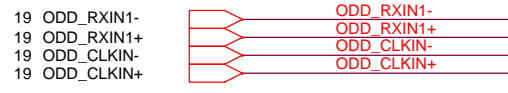
For 8Mx32 Bit Stuff
 16Mx32 Bit no stuff

VRAM_VREF is 70%FBVDDQ for GDDR3

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

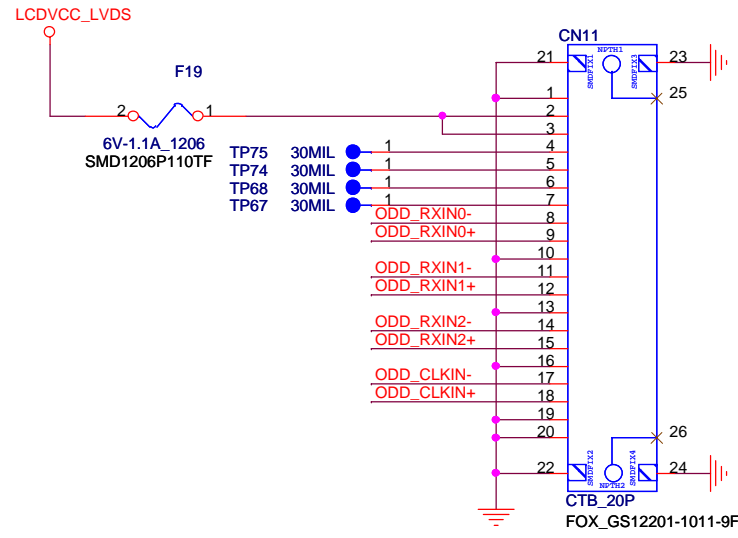
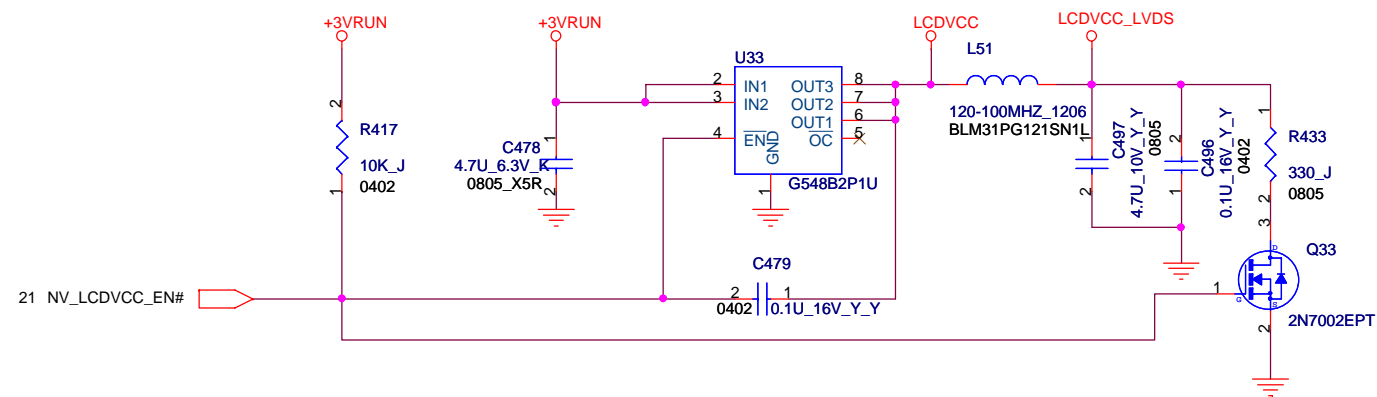


LVDS

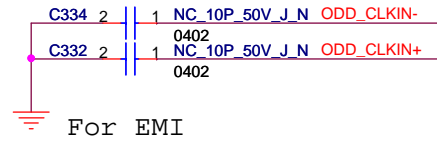


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

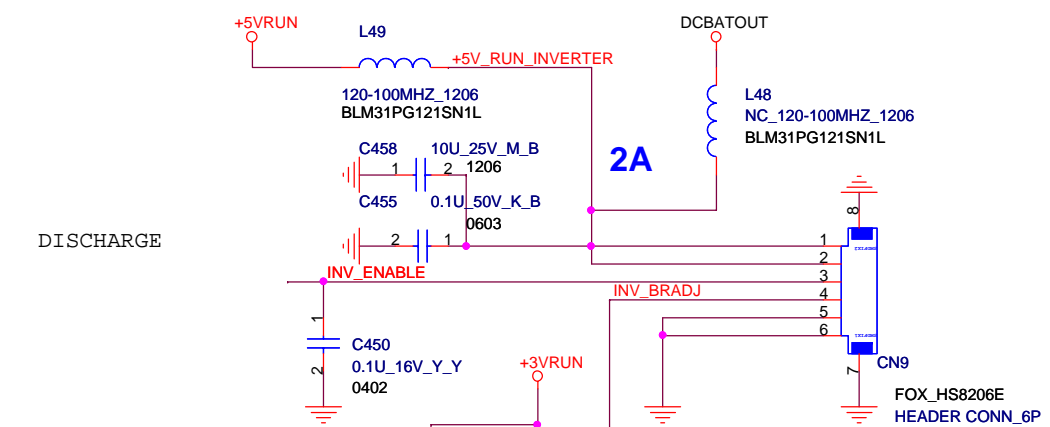
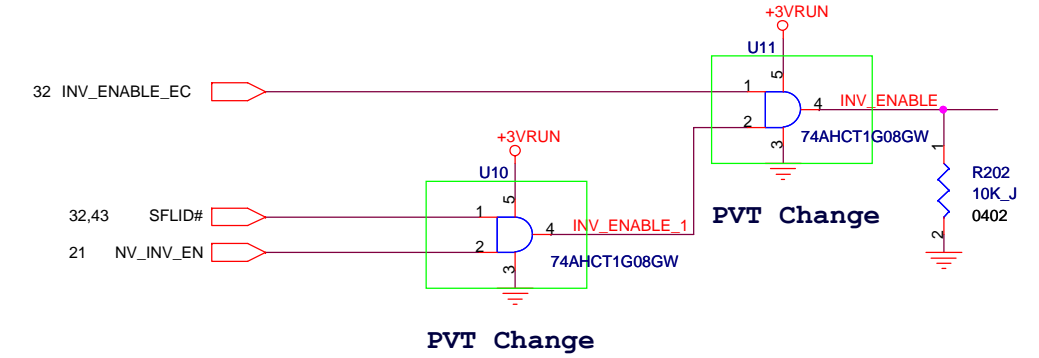
LCD POWER



LVDS CONNECTOR

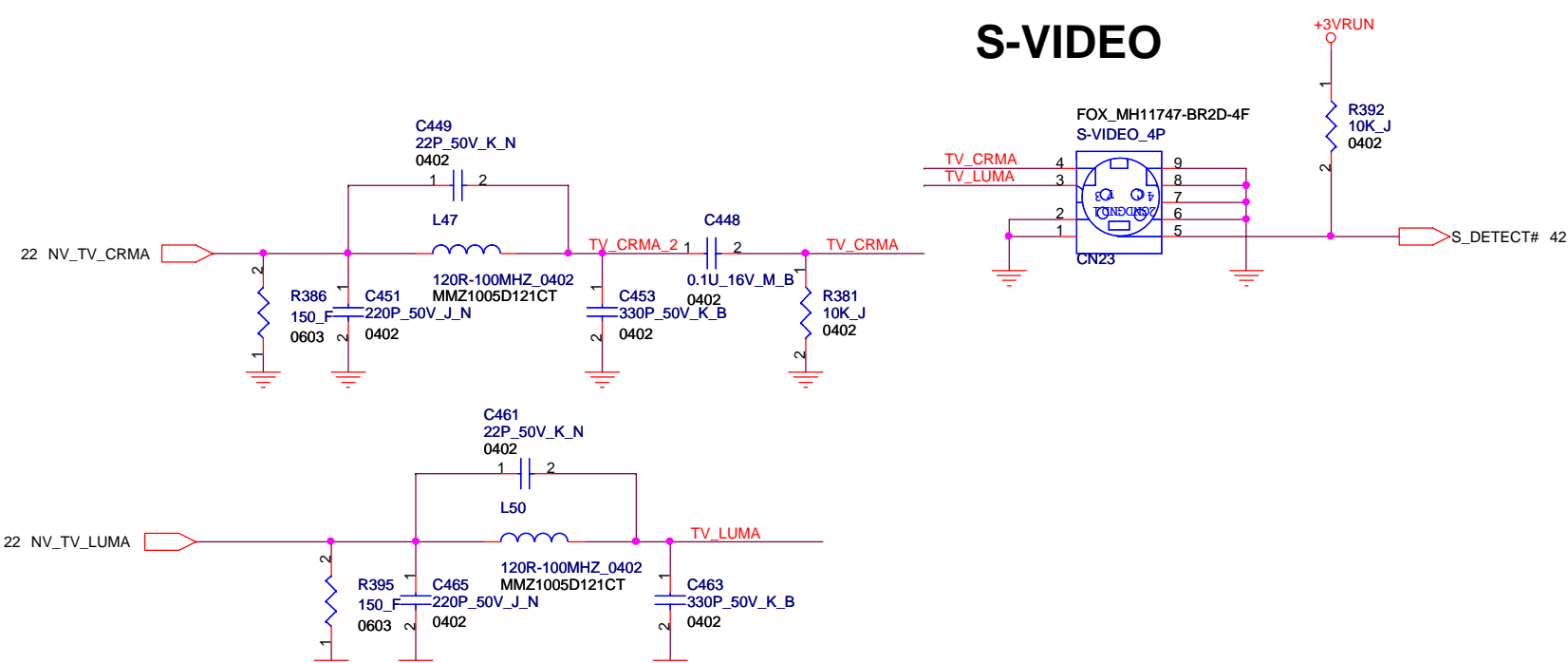


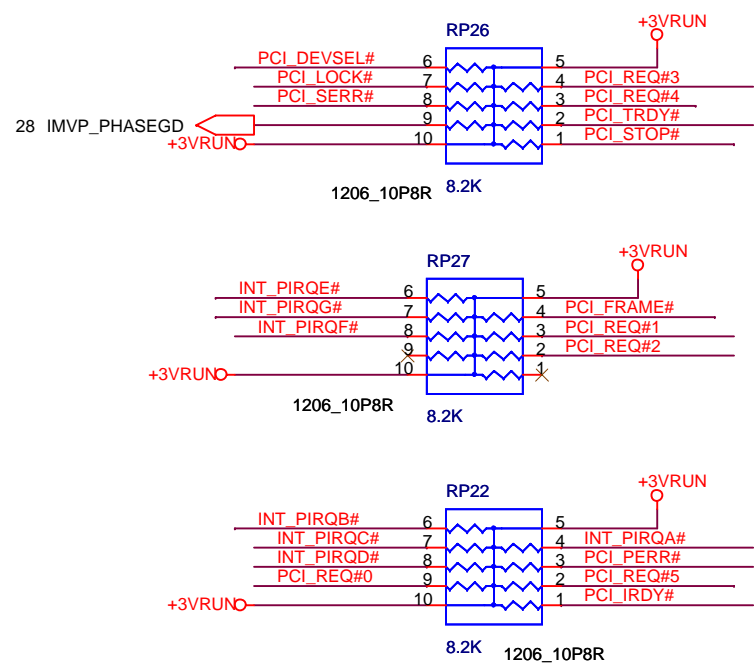
For EMI



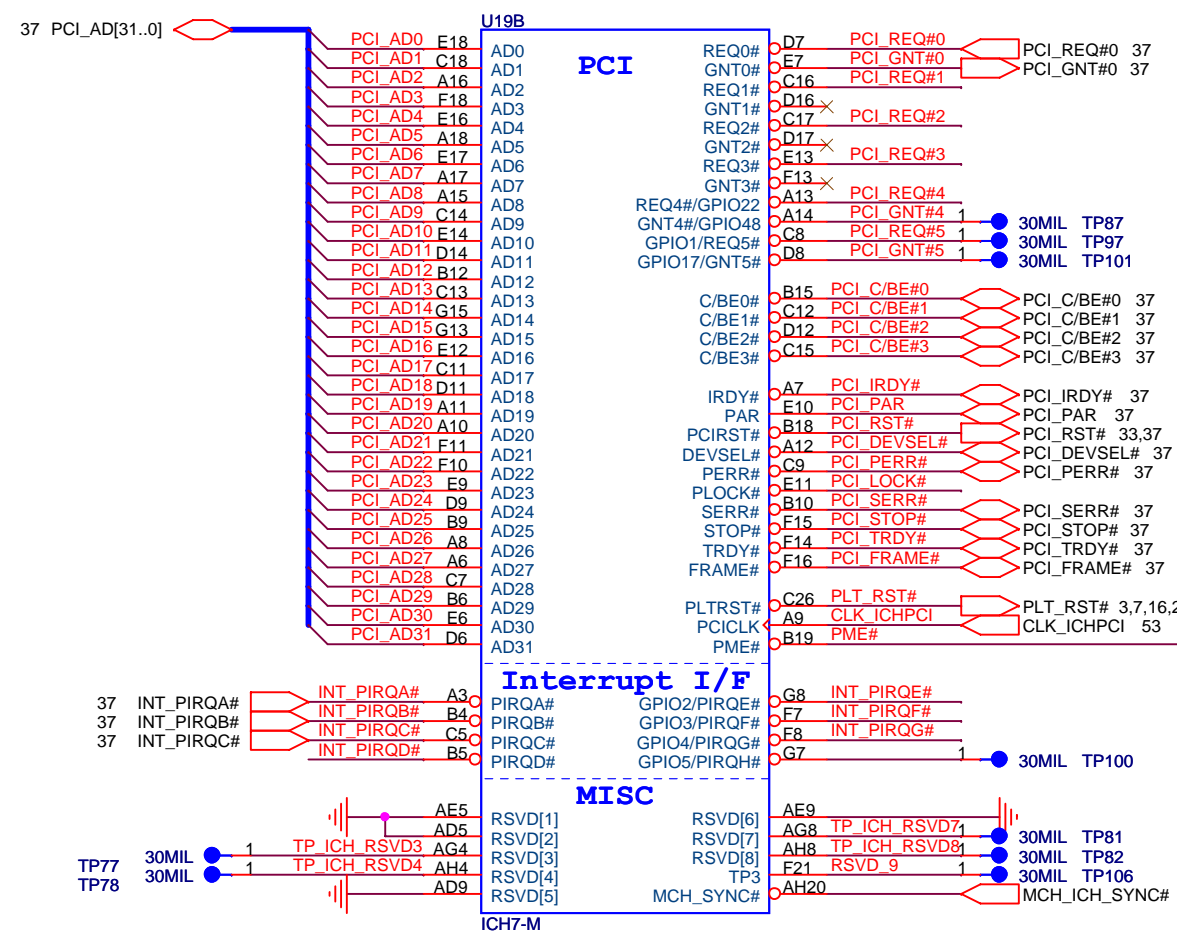
INVERTER CONNECTOR

S-VIDEO





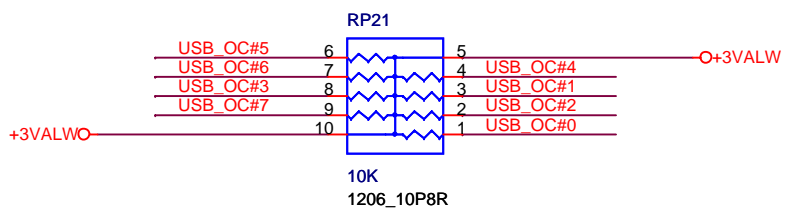
PCI Pullups



Test leakage voltage in BB

Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals

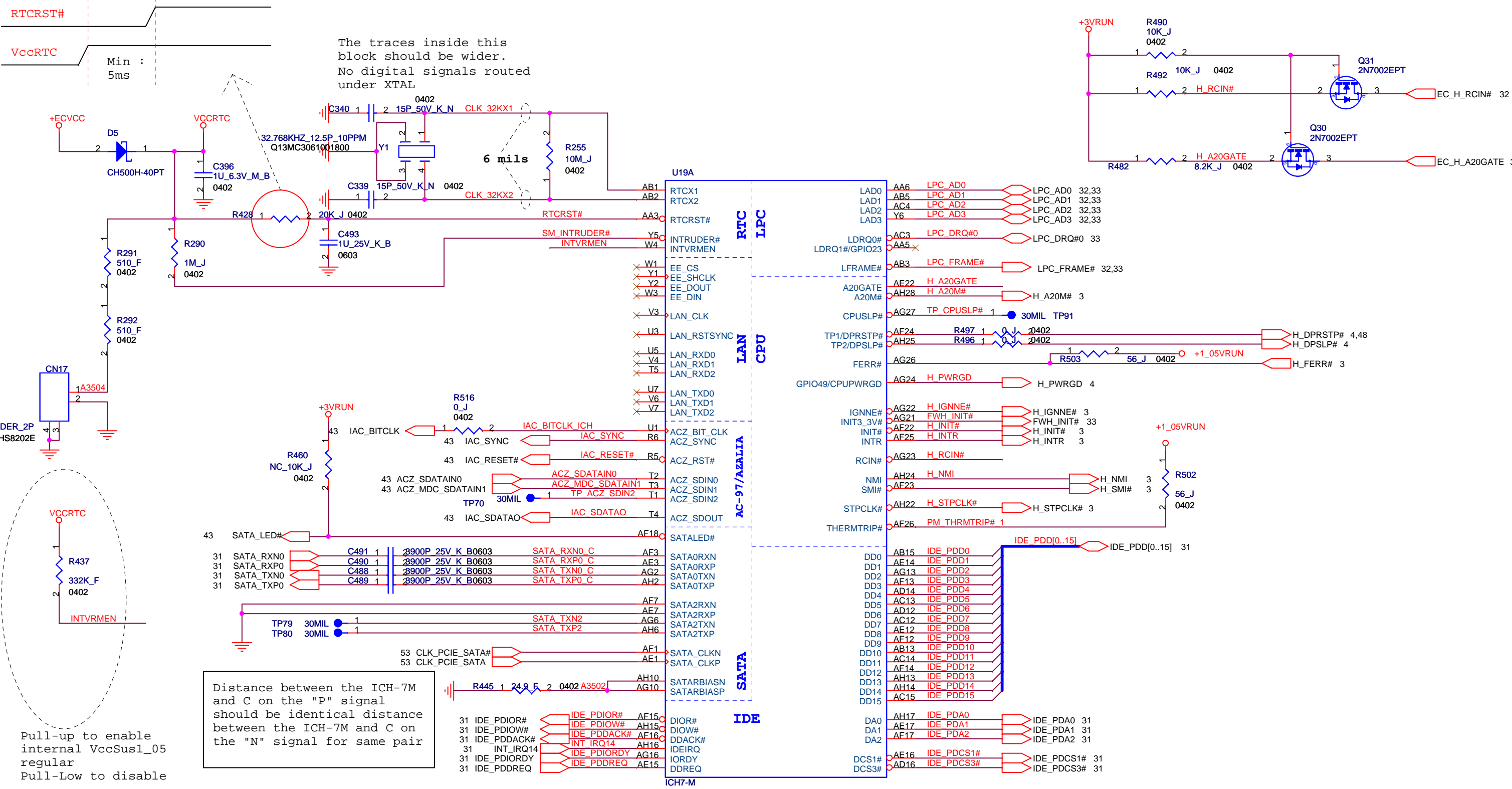


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **ICH7-M(PCI/DMI/USB/PCIE) 1/5**

Size: A3 Document Number: **MS60-1-01 (MBX-159)** Rev: 0.30

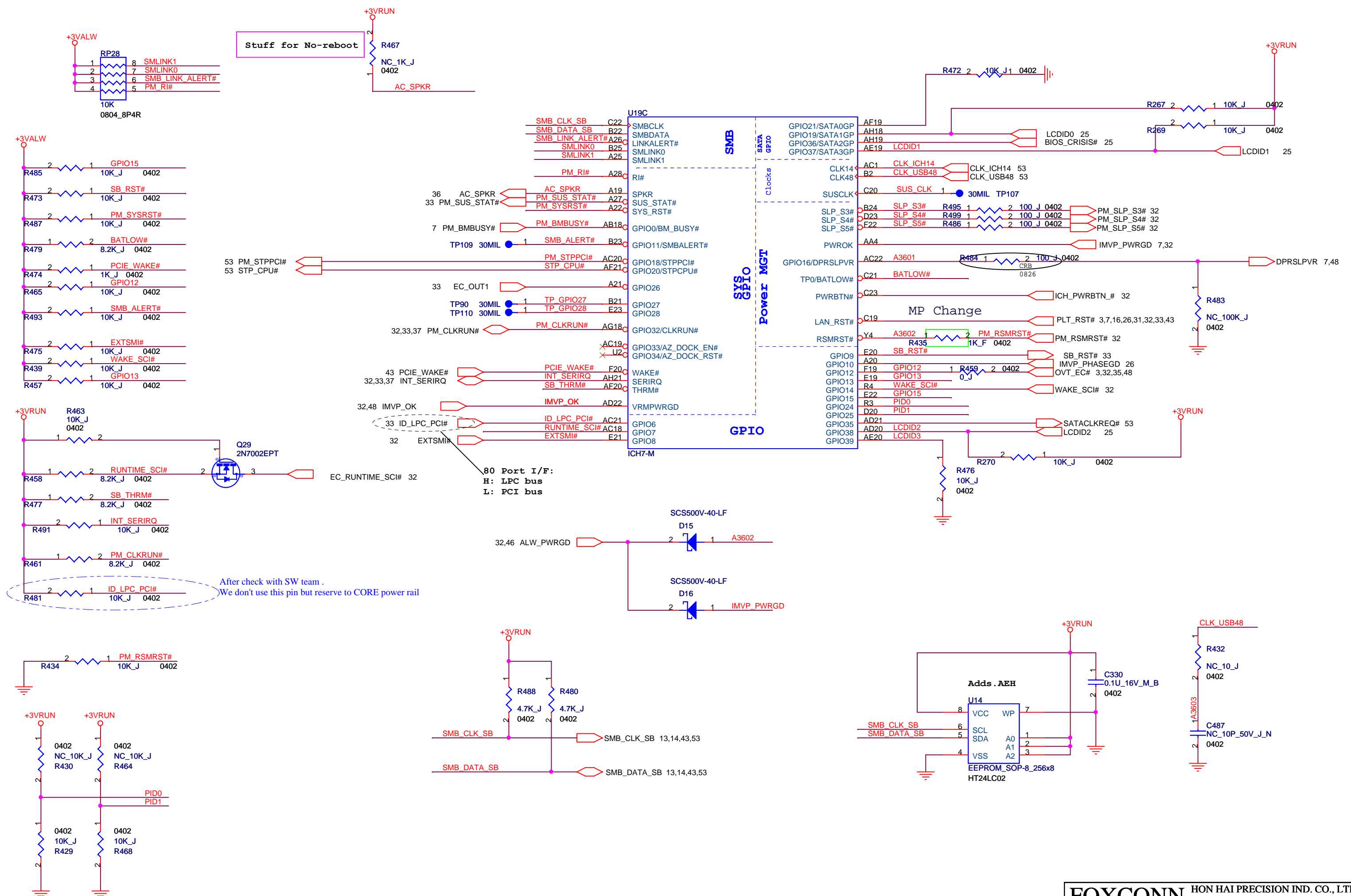
Date: Wednesday, October 04, 2006 Sheet 26 of 56



The traces inside this block should be wider.
No digital signals routed under XTAL

Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

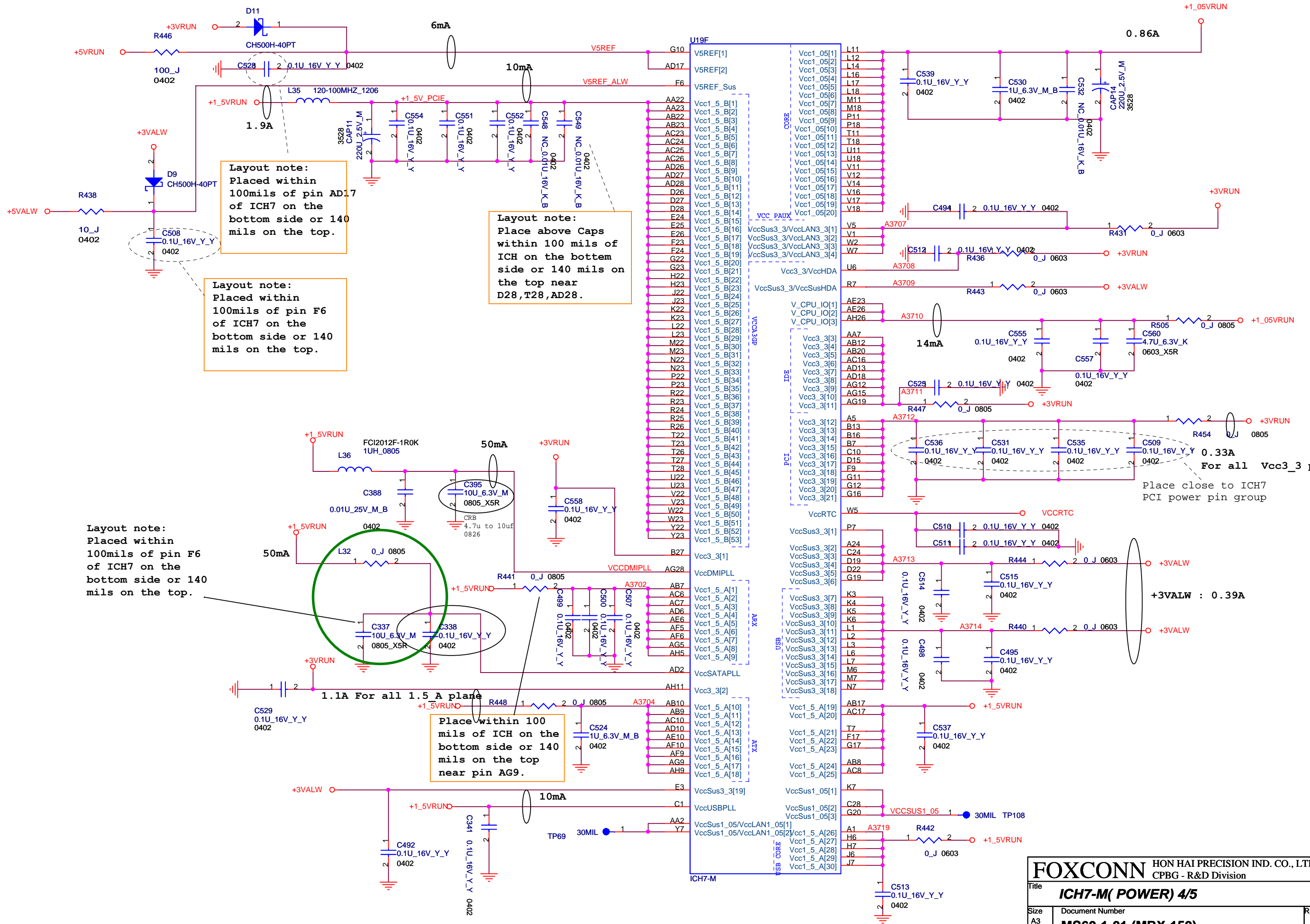
Pull-up to enable internal VccSus1_05 regular
Pull-Low to disable



Stuff for No-reboot

After check with SW team .
We don't use this pin but reserve to CORE power rail

80 Port I/F:
H: LPC bus
L: PCI bus



Layout note:
Placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

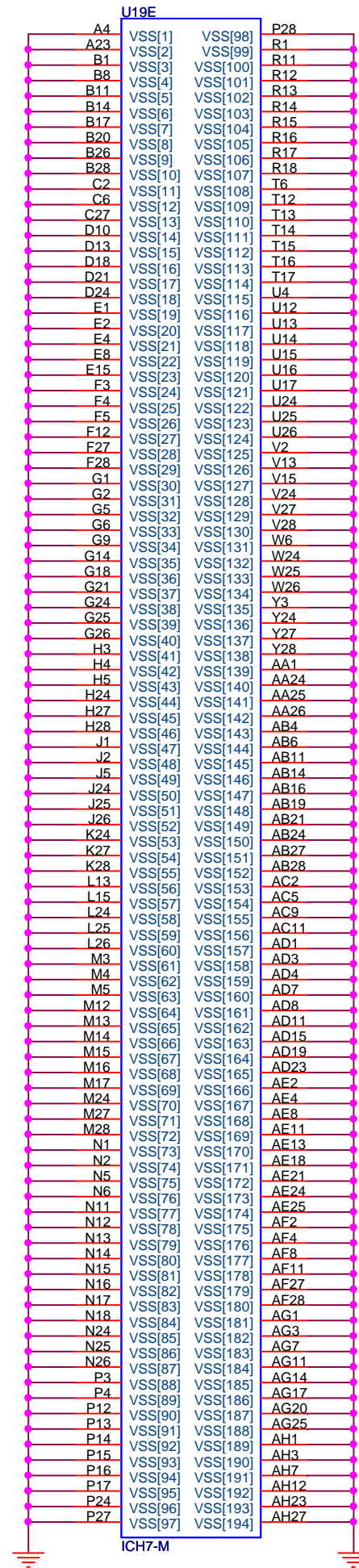
Layout note:
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

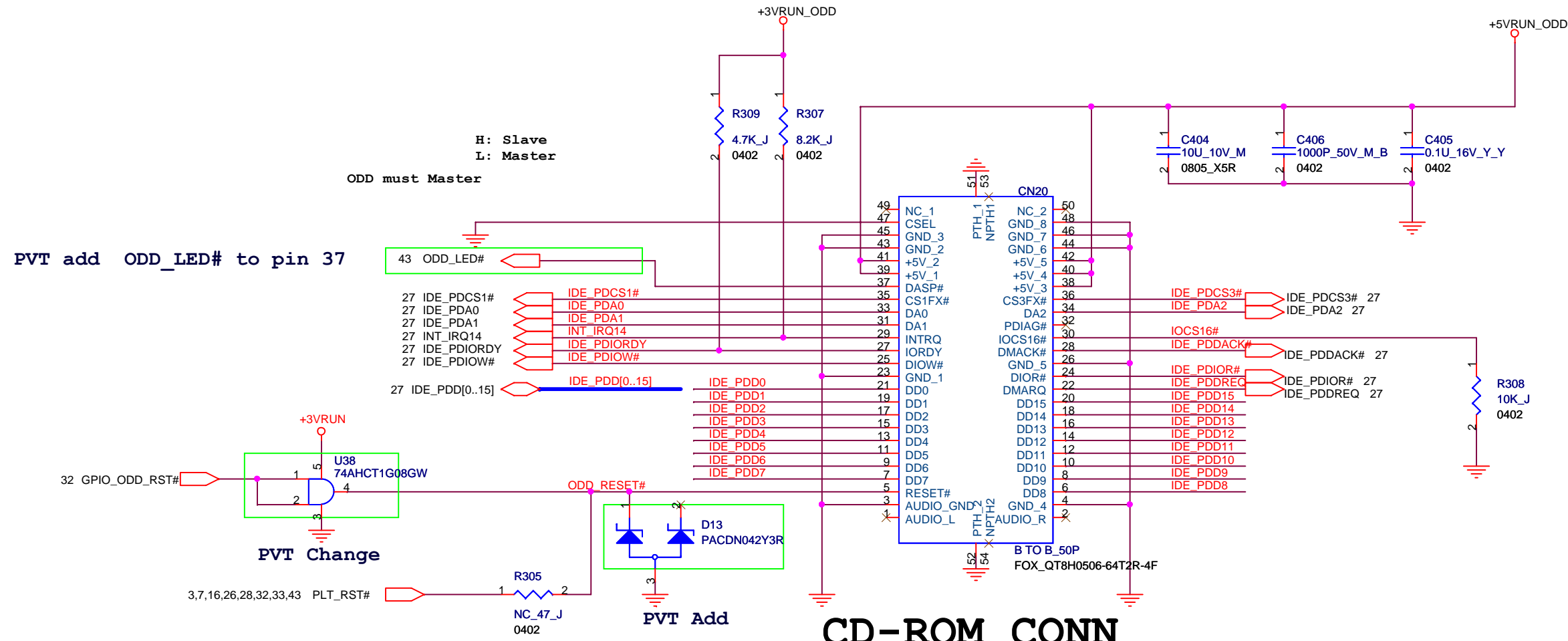
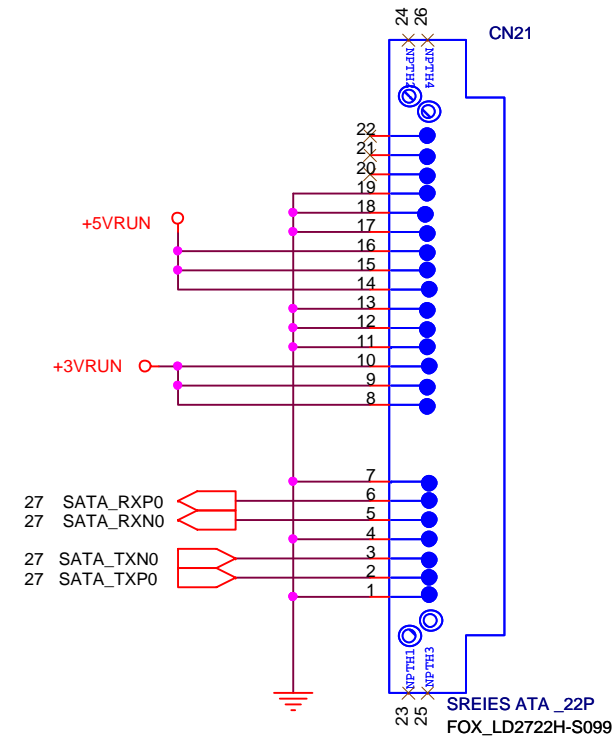
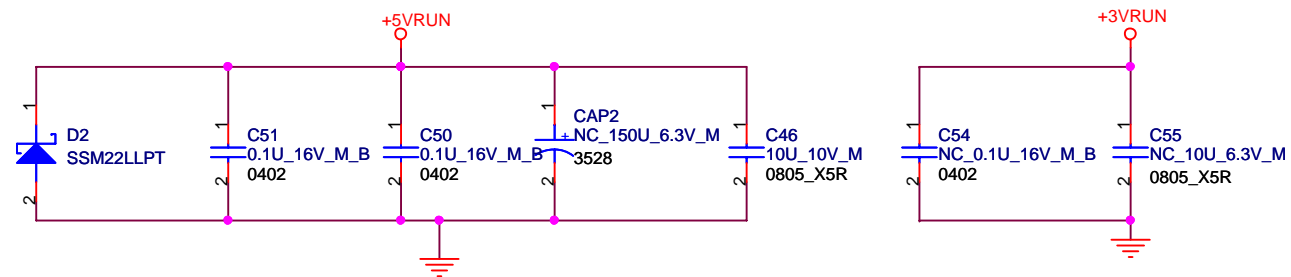
0.33A
For all Vcc3_3 plane
Place close to ICH7 PCI power pin group

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title ICH7-M (POWER) 4/5		
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 0.30
Date: Wednesday, October 04, 2006	Sheet 29	of 56

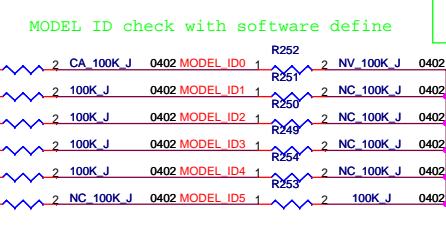
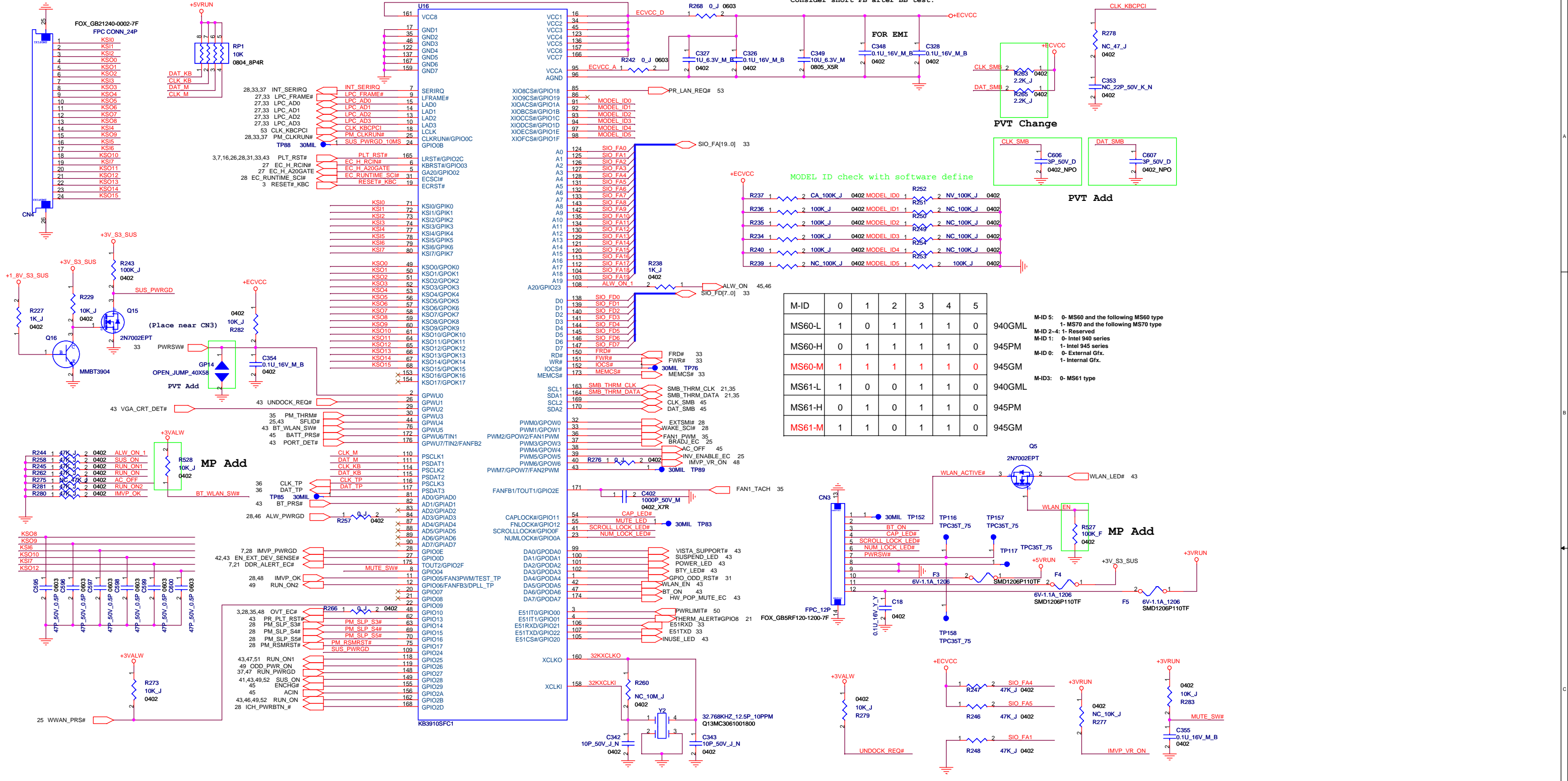


FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: ICH7-M(GND) 5/5		
Size: A3	Document Number: MS60-1-01 (MBX-159)	Rev: 0.30
Date: Wednesday, October 04, 2006	Sheet 30 of 56	

SATA HDD CONN



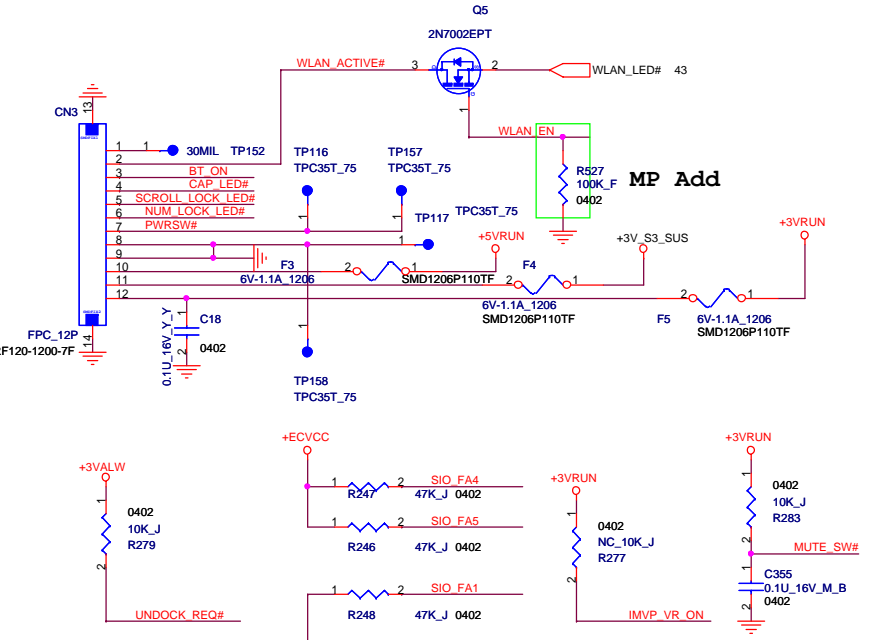
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title SATA HDD/CD-ROM		
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 0.30
Date: Wednesday, October 04, 2006	Sheet 31	of 56



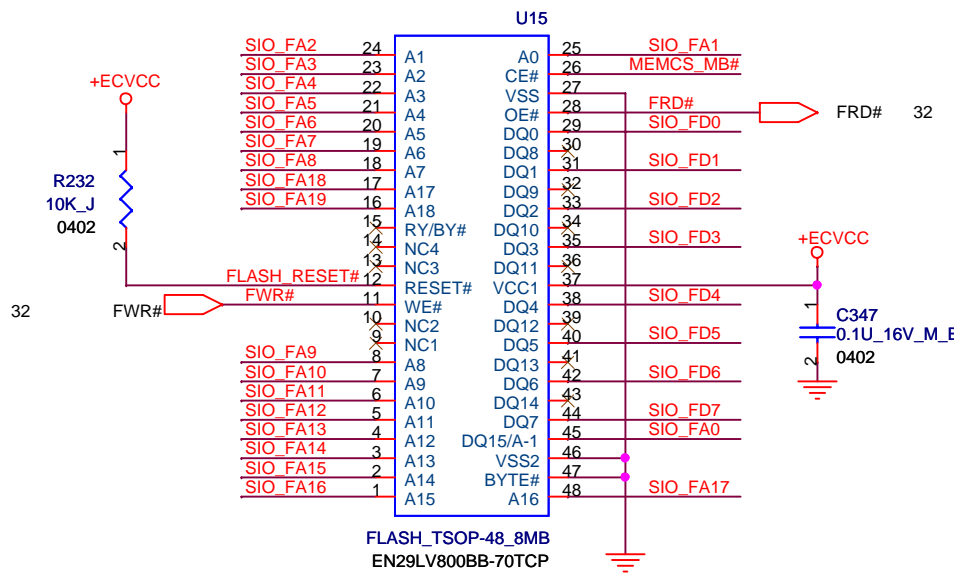
MODEL ID check with software define

M-ID	0	1	2	3	4	5	
MS60-L	1	0	1	1	1	0	940GML
MS60-H	0	1	1	1	1	0	945PM
MS60-M	1	1	1	1	1	0	945GM
MS61-L	1	0	0	1	1	0	940GML
MS61-H	0	1	0	1	1	0	945PM
MS61-M	1	1	0	1	1	0	945GM

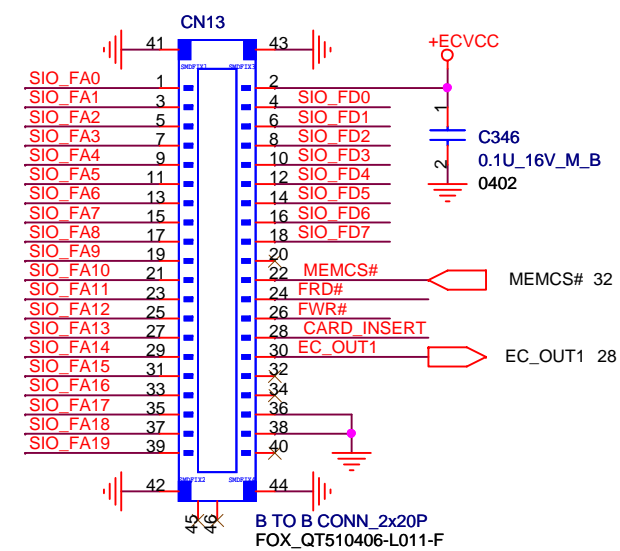
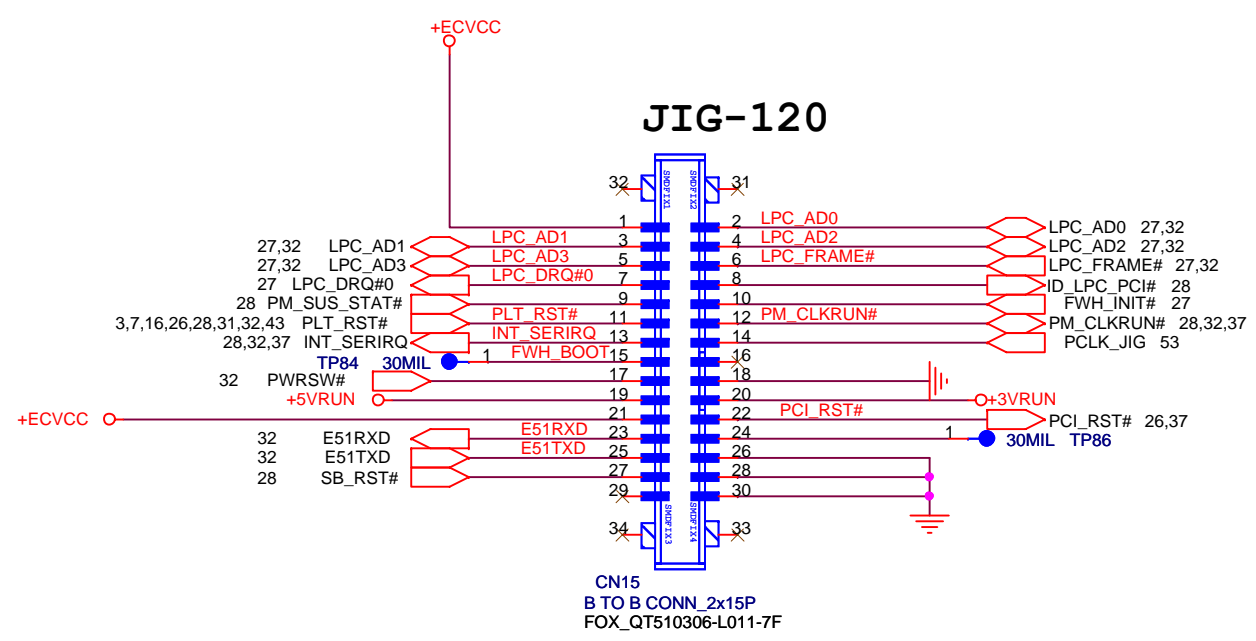
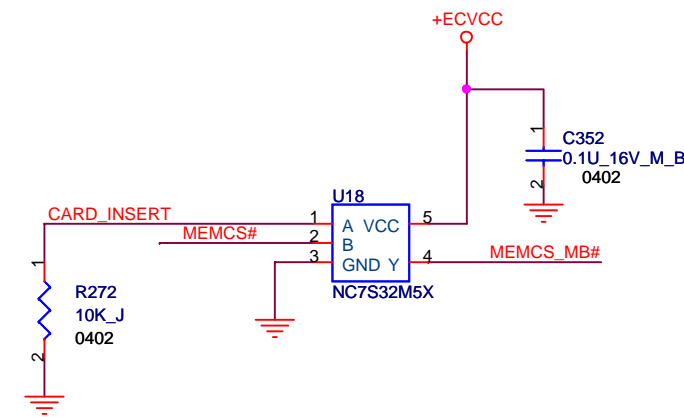
M-ID 5: 0- MS60 and the following MS60 type
 1- MS70 and the following MS70 type
 M-ID 2-4: 1- Reserved
 M-ID 1: 0- Intel 940 series
 1- Intel 945 series
 M-ID 0: 0- External Gfx.
 1- Internal Gfx.
 M-ID3: 0- MS61 type



32 SIO_FA[19..0]
 32 SIO_FD[7..0]



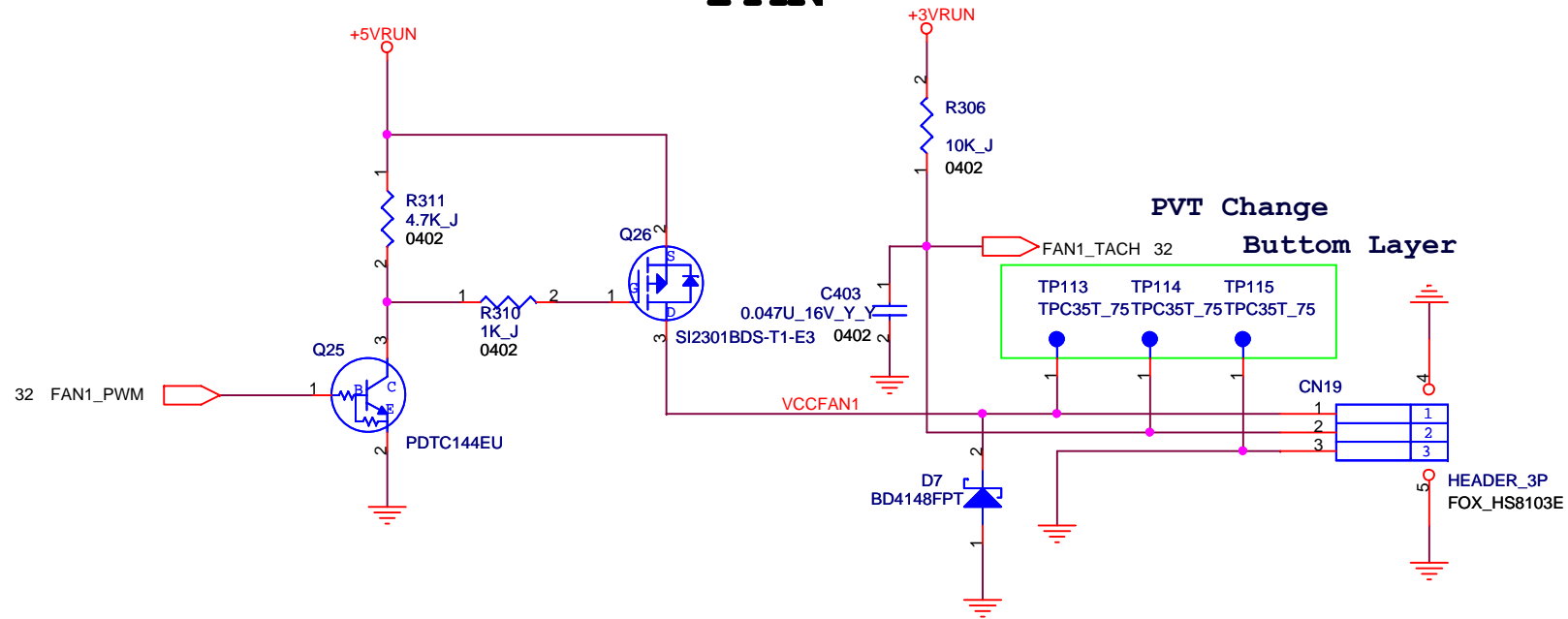
BIOS ROM



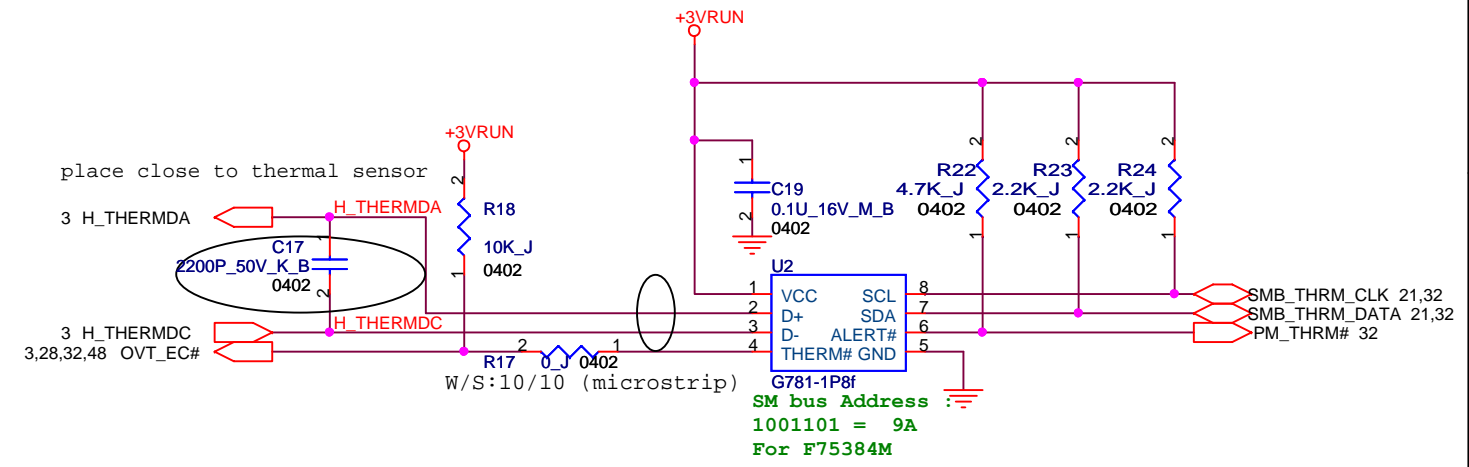
WWAN FOR MS60-L ONLY !!

FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title		WWAN	
Size	Document Number	Rev	
Custom	MS60-1-01 (MBX-159)	0.30	
Date:	Wednesday, October 04, 2006	Sheet	34 of 56

FAN

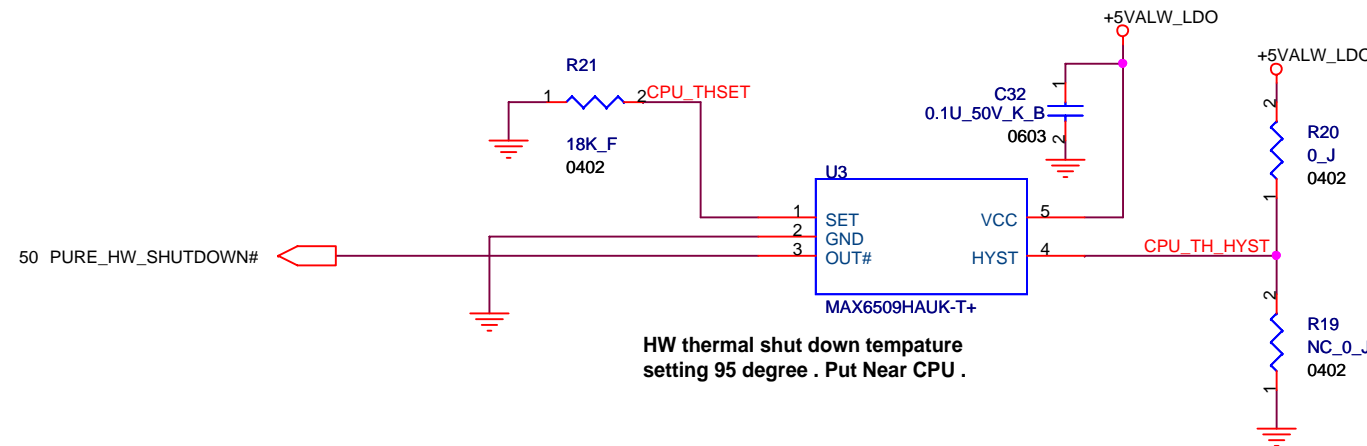


CPU SENSOR



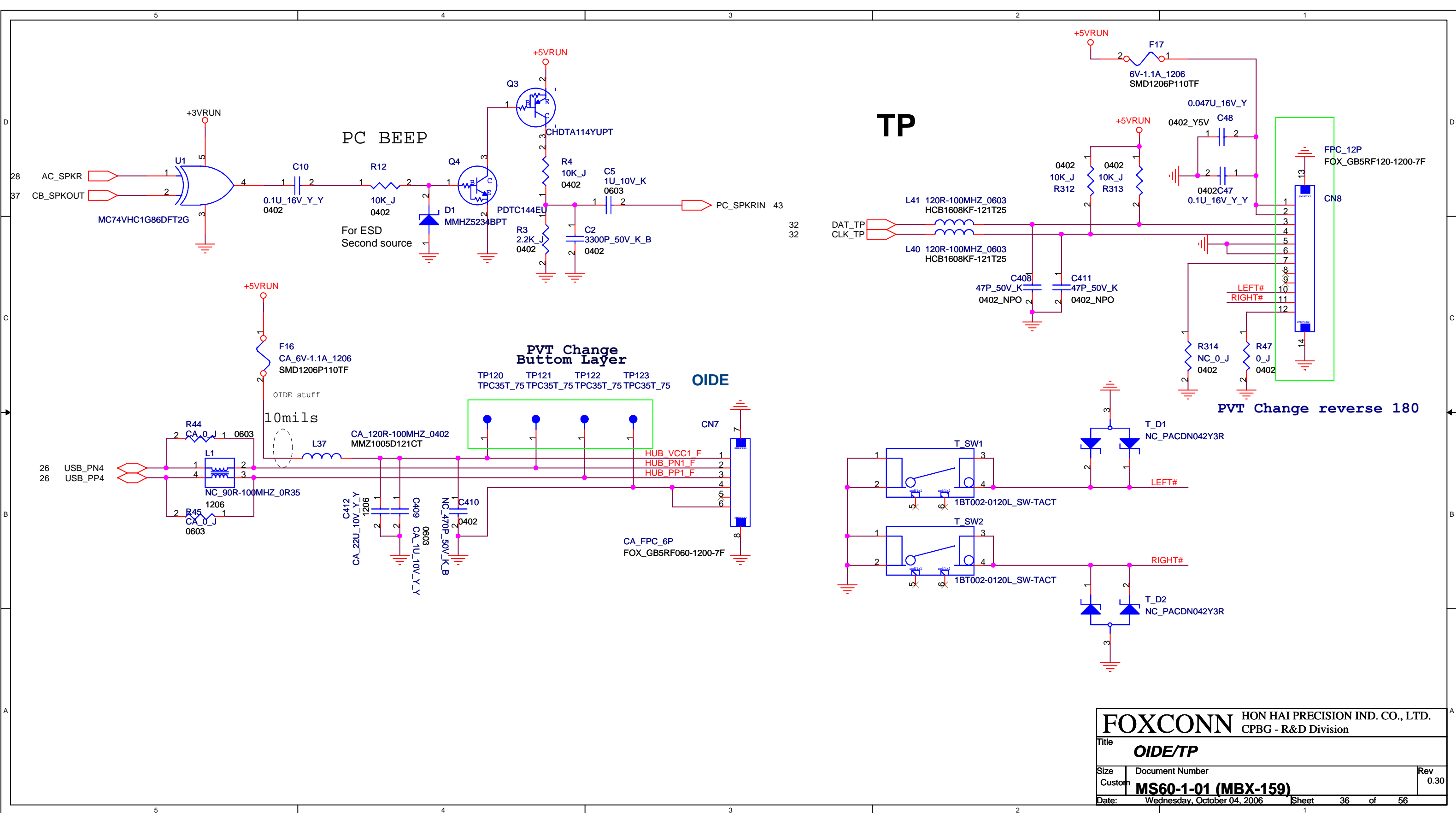
Place Thermal-Sensor near CPU & GMCH.

HW THERMAL PROTECTION

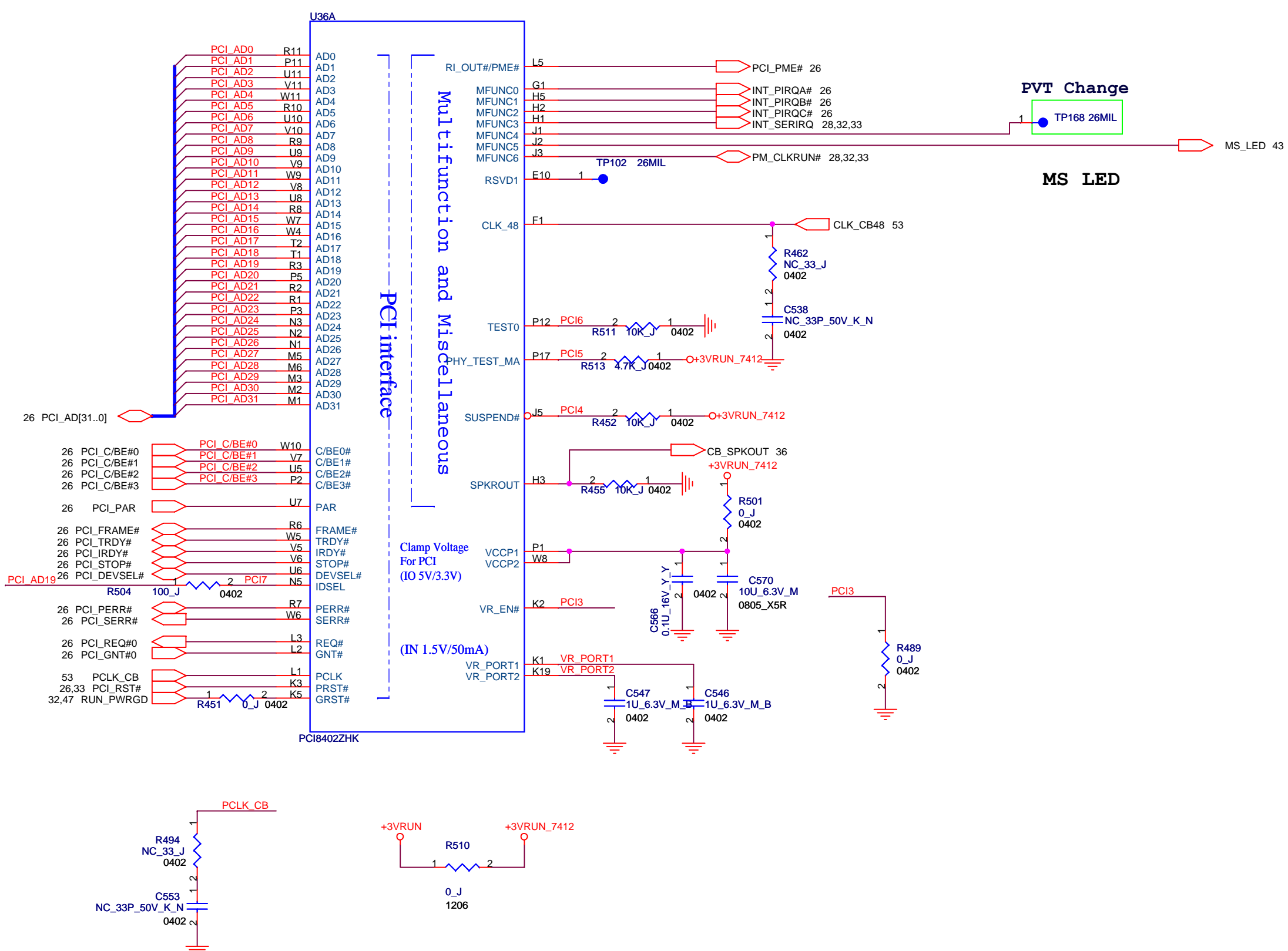


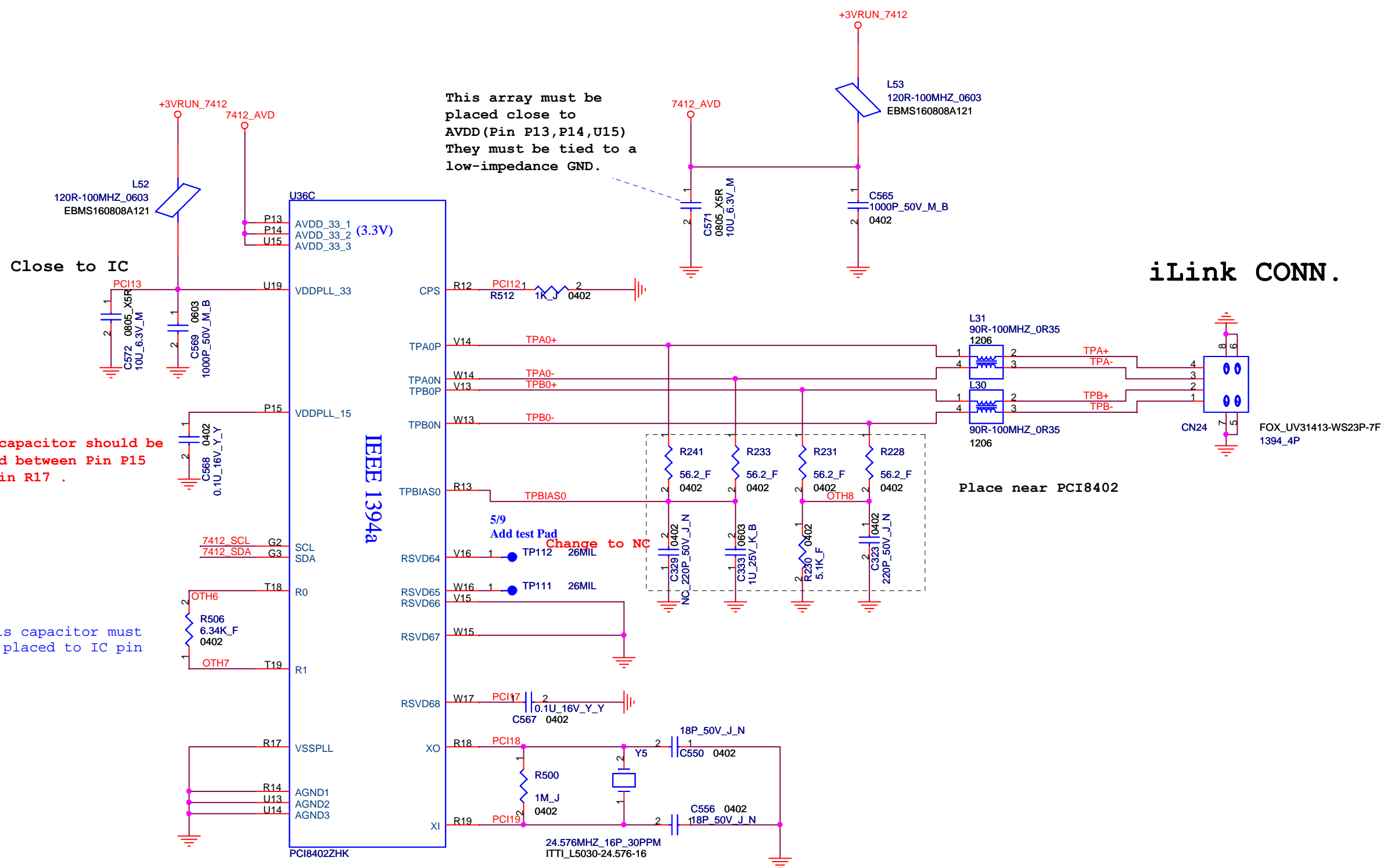
HW thermal shut down temperature setting 95 degree . Put Near CPU .

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title FAN/HW THERMAL PROTECT		
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 0.30
Date: Wednesday, October 04, 2006	Sheet 35	of 56



FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title OIDE/TP			
Size	Document Number	Rev	
Custom	MS60-1-01 (MBX-159)	0.30	
Date:	Wednesday, October 04, 2006	Sheet	36 of 56





This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.

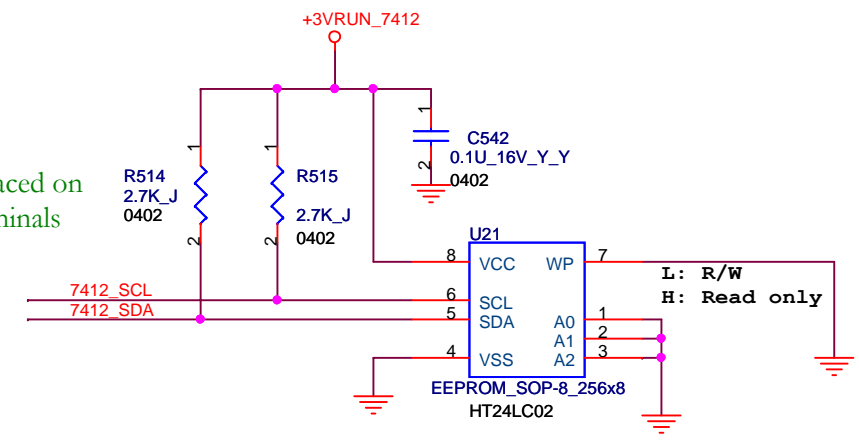
Close to IC

This capacitor should be placed between Pin P15 and Pin R17 .

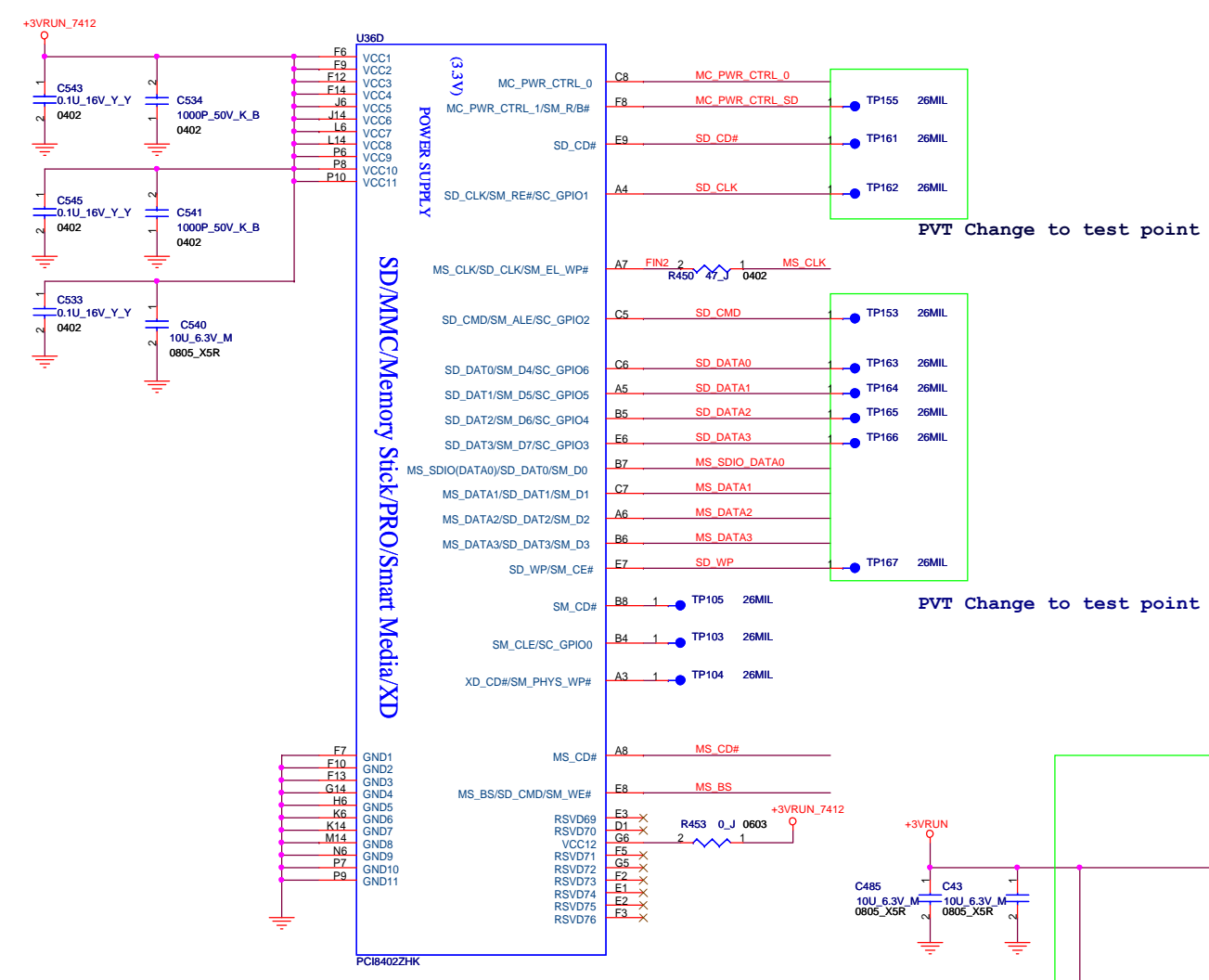
This capacitor must be placed to IC pin

Place near PCI8402

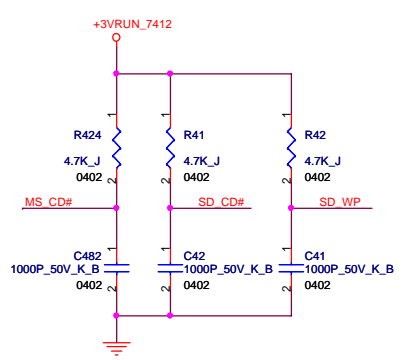
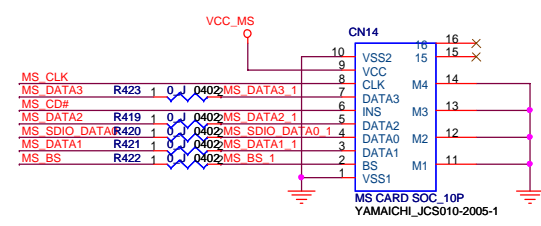
Resistors should be placed on the SCL and SDA terminals



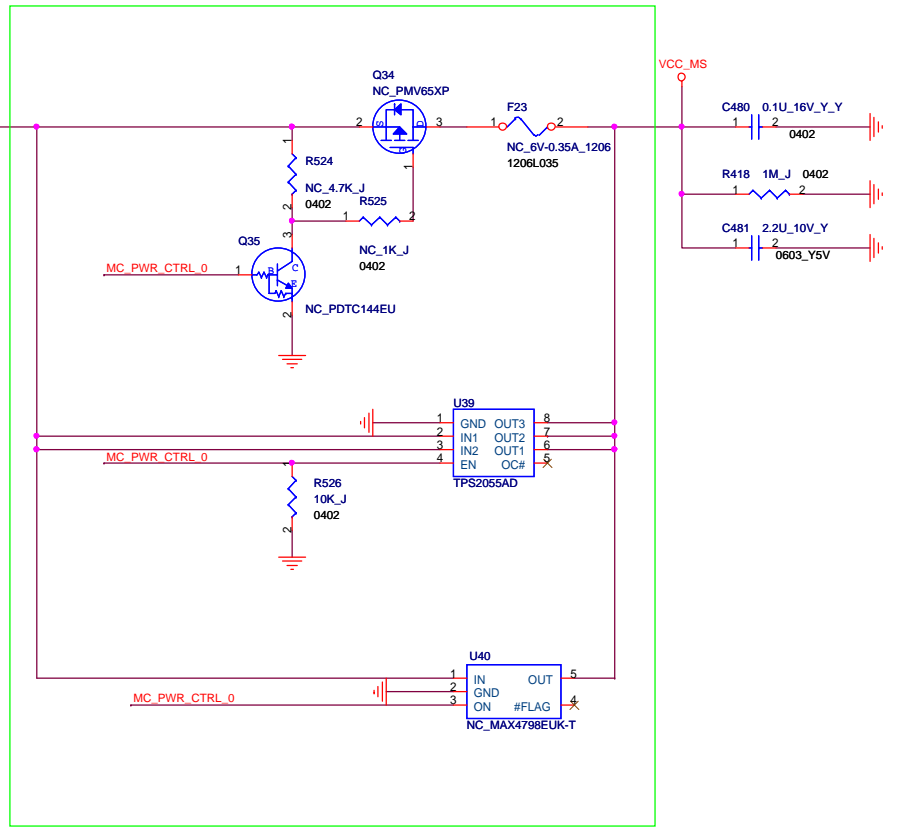
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title PCI (ILINK)		
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 0.30
Date: Wednesday, October 04, 2006 Sheet 38 of 56		

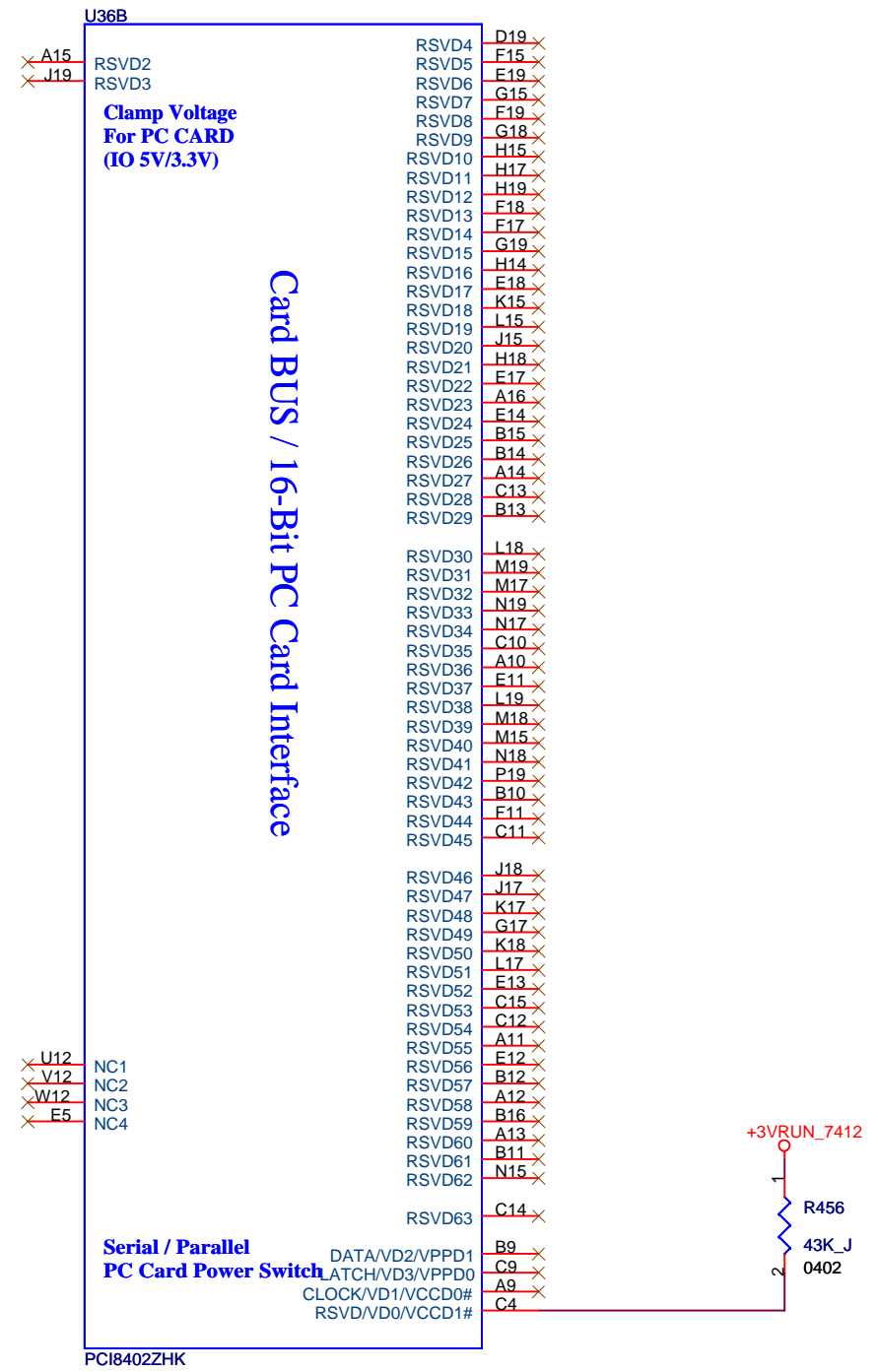


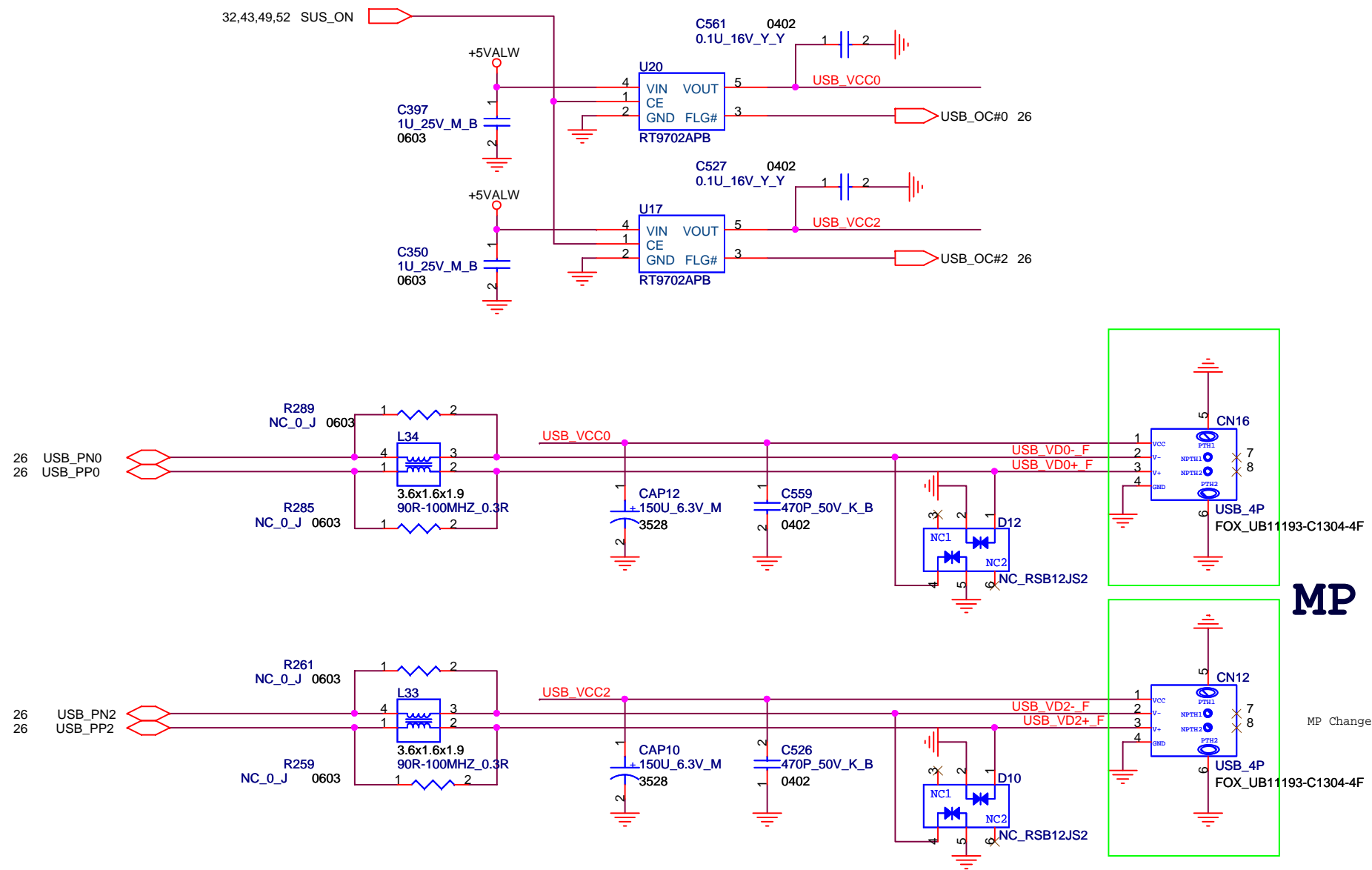
MS Duo / Pro



MP Change

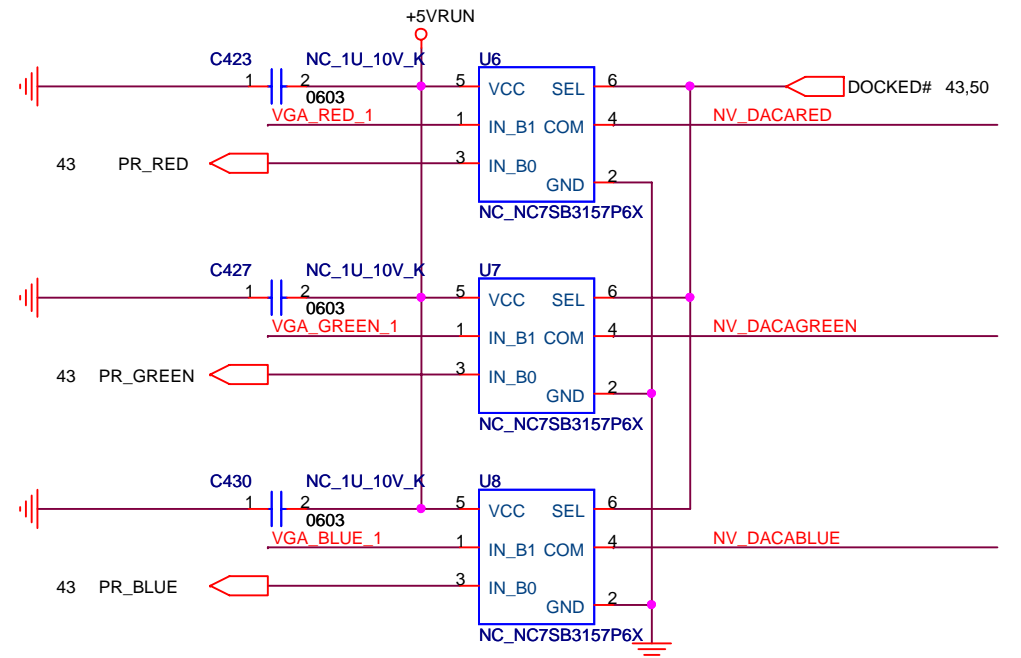
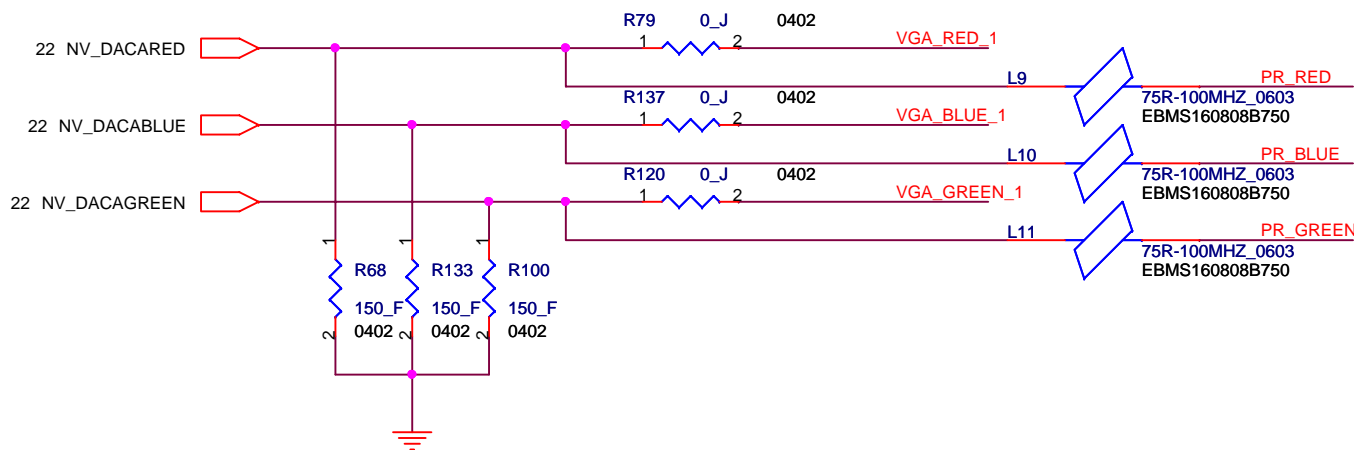
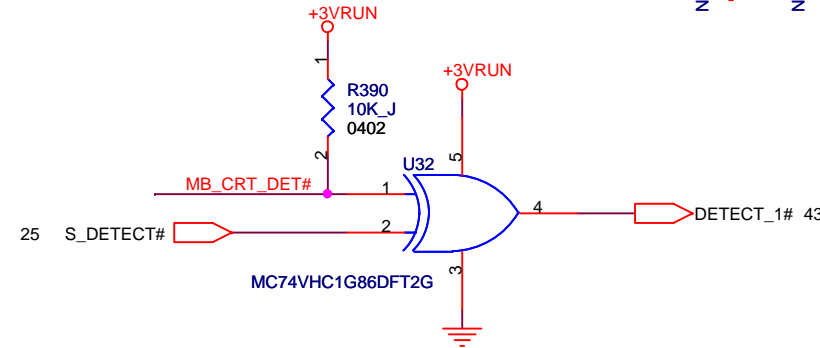
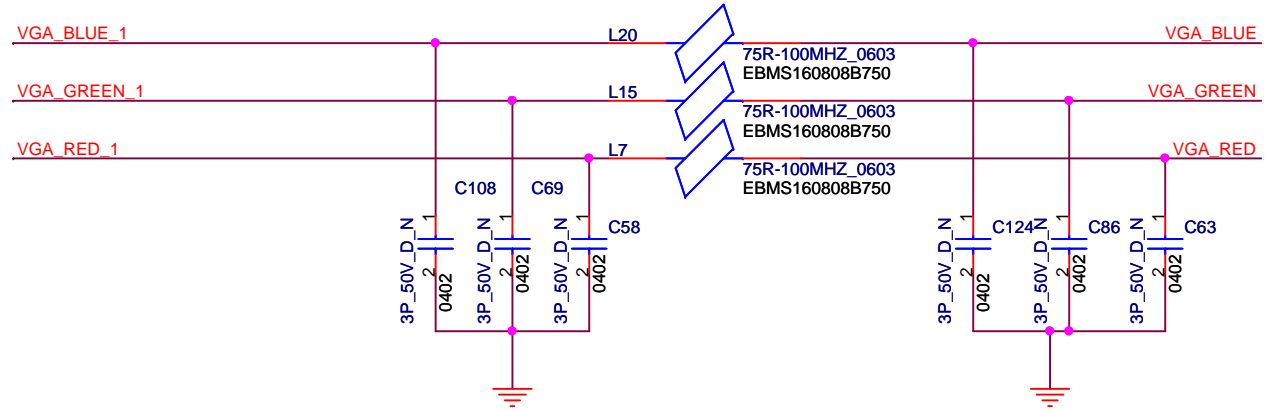
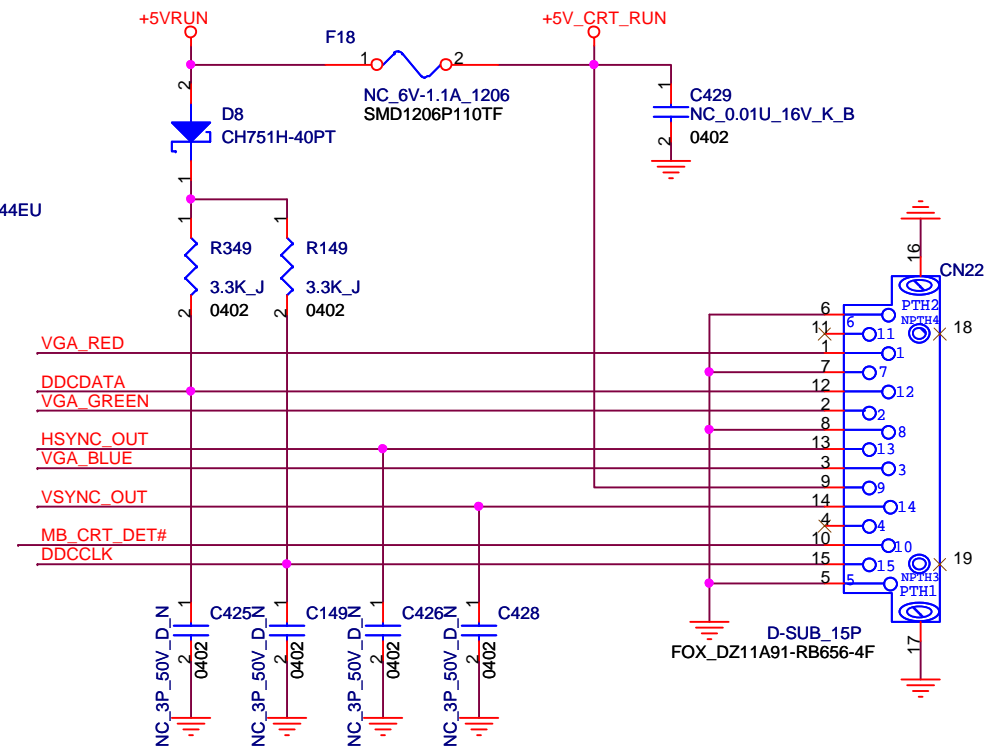
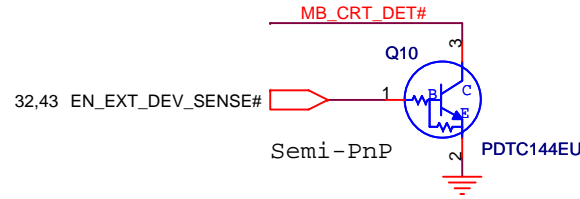
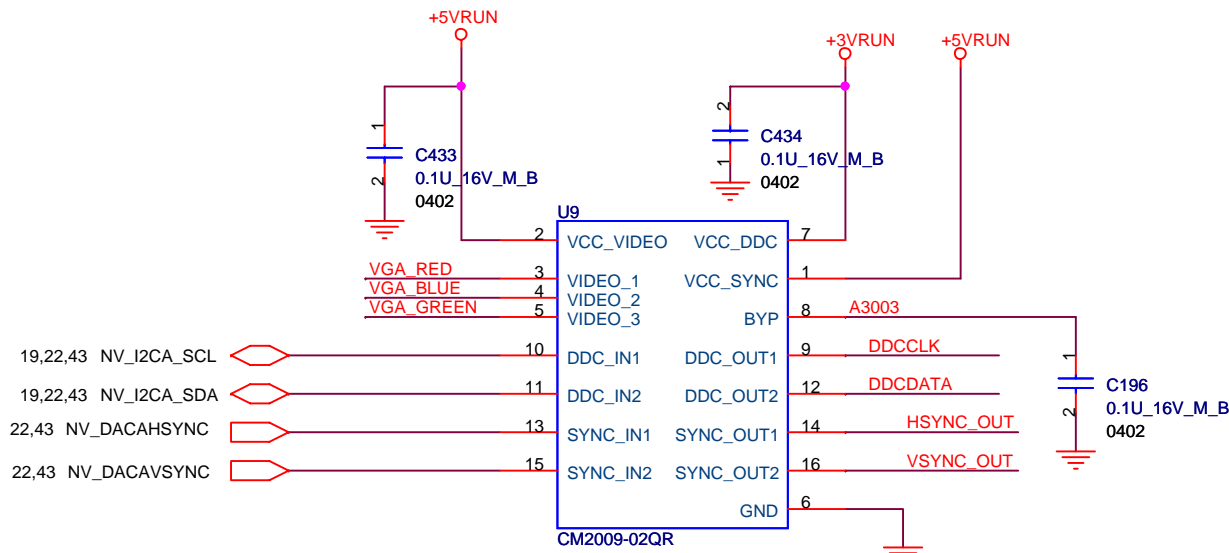


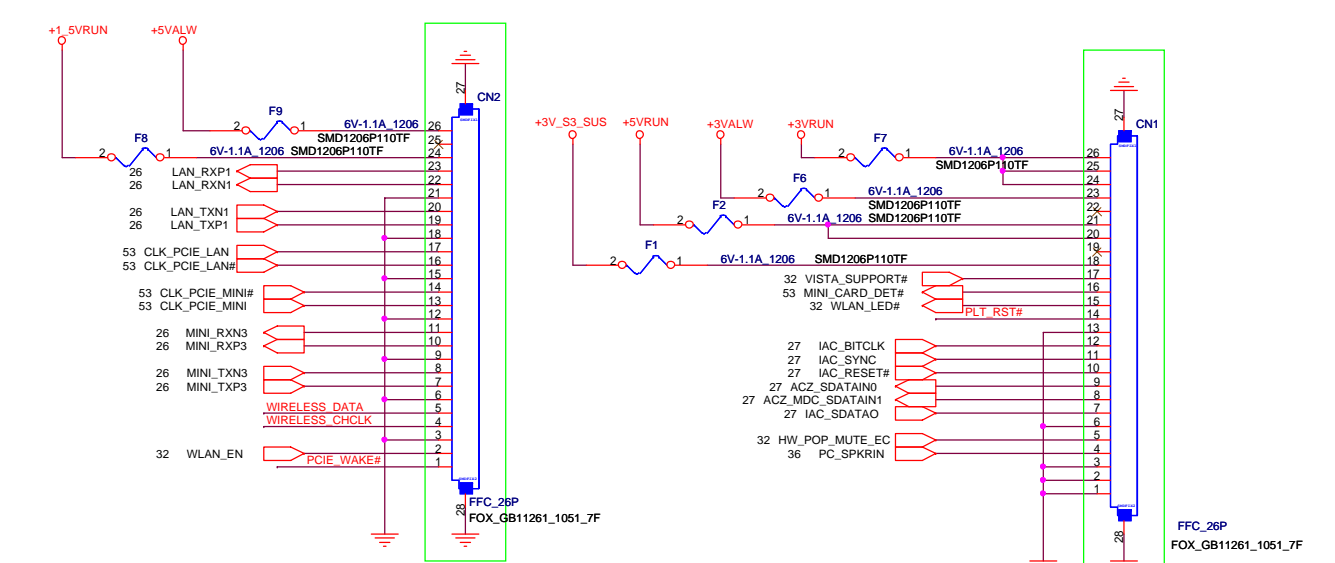
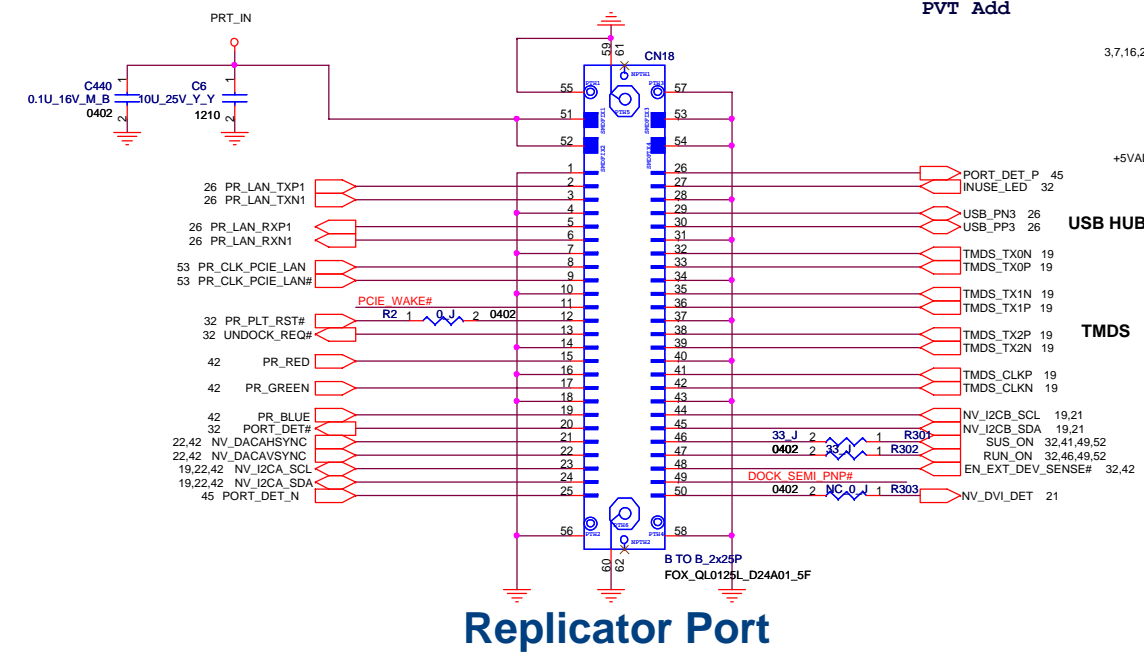
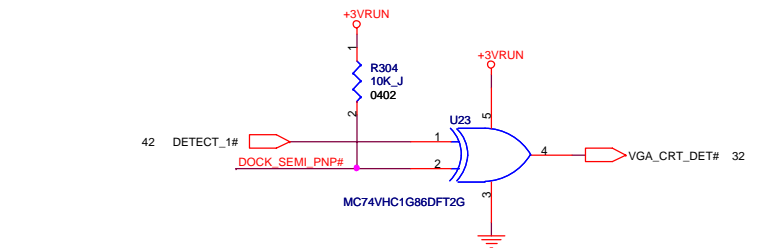
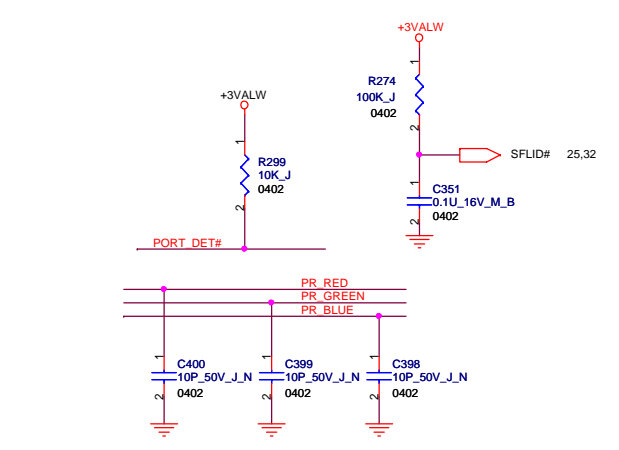
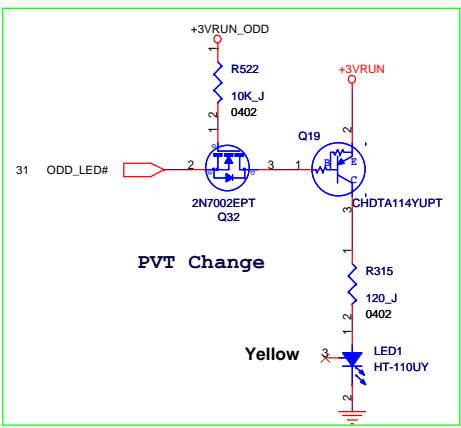
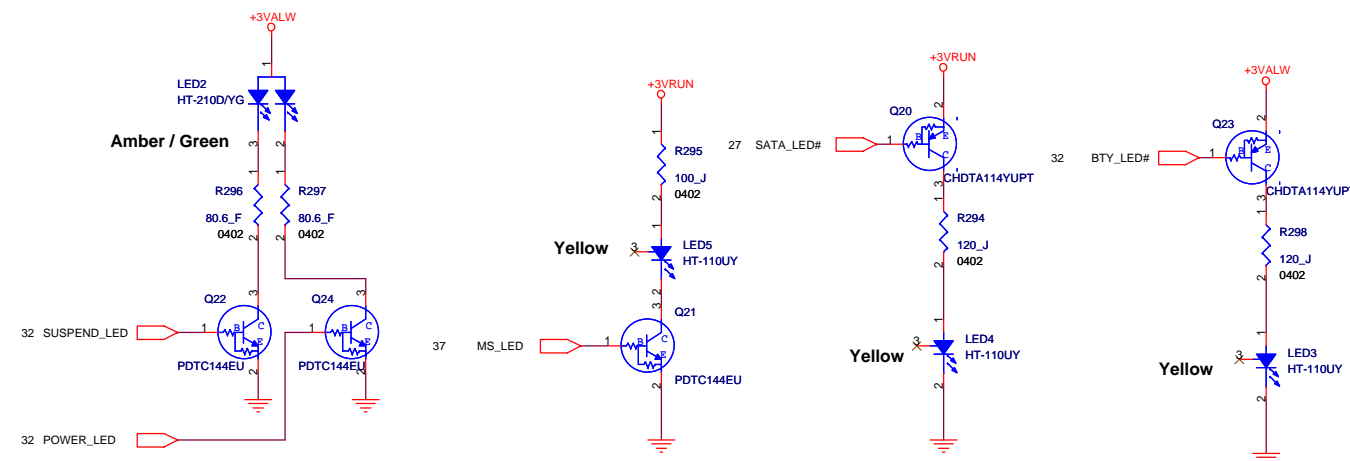




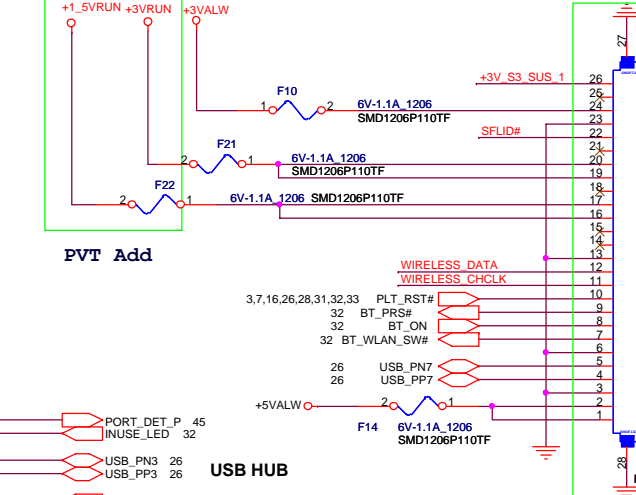
MP Change

MP Change

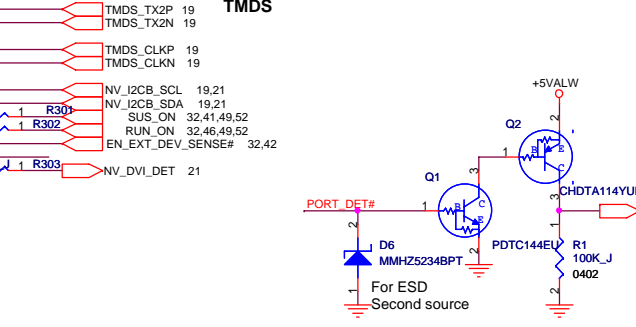




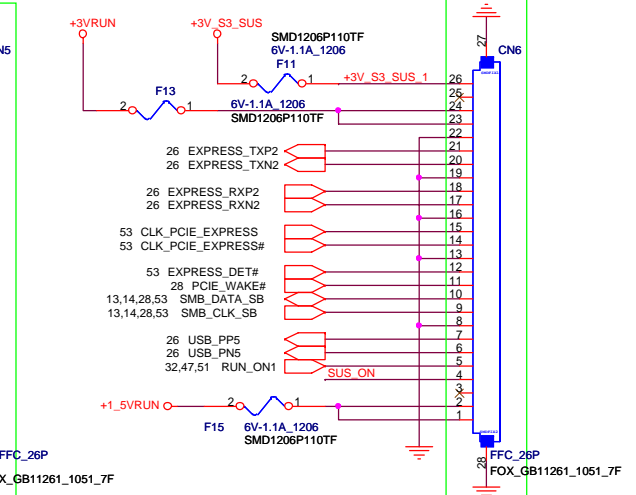
PVT Change to GB11261_1051_7F
PVT Change to NC



USB HUB
TMDS

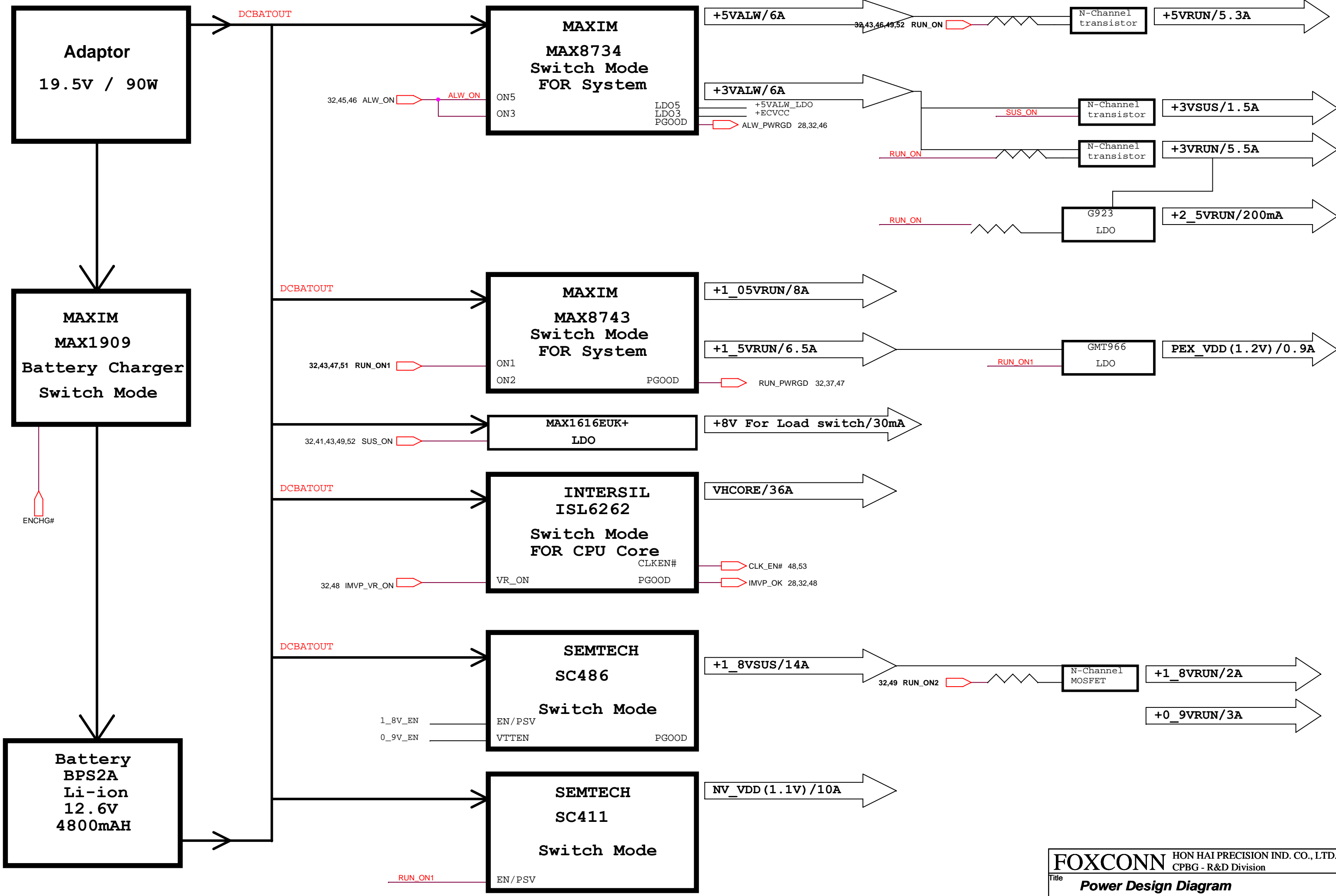


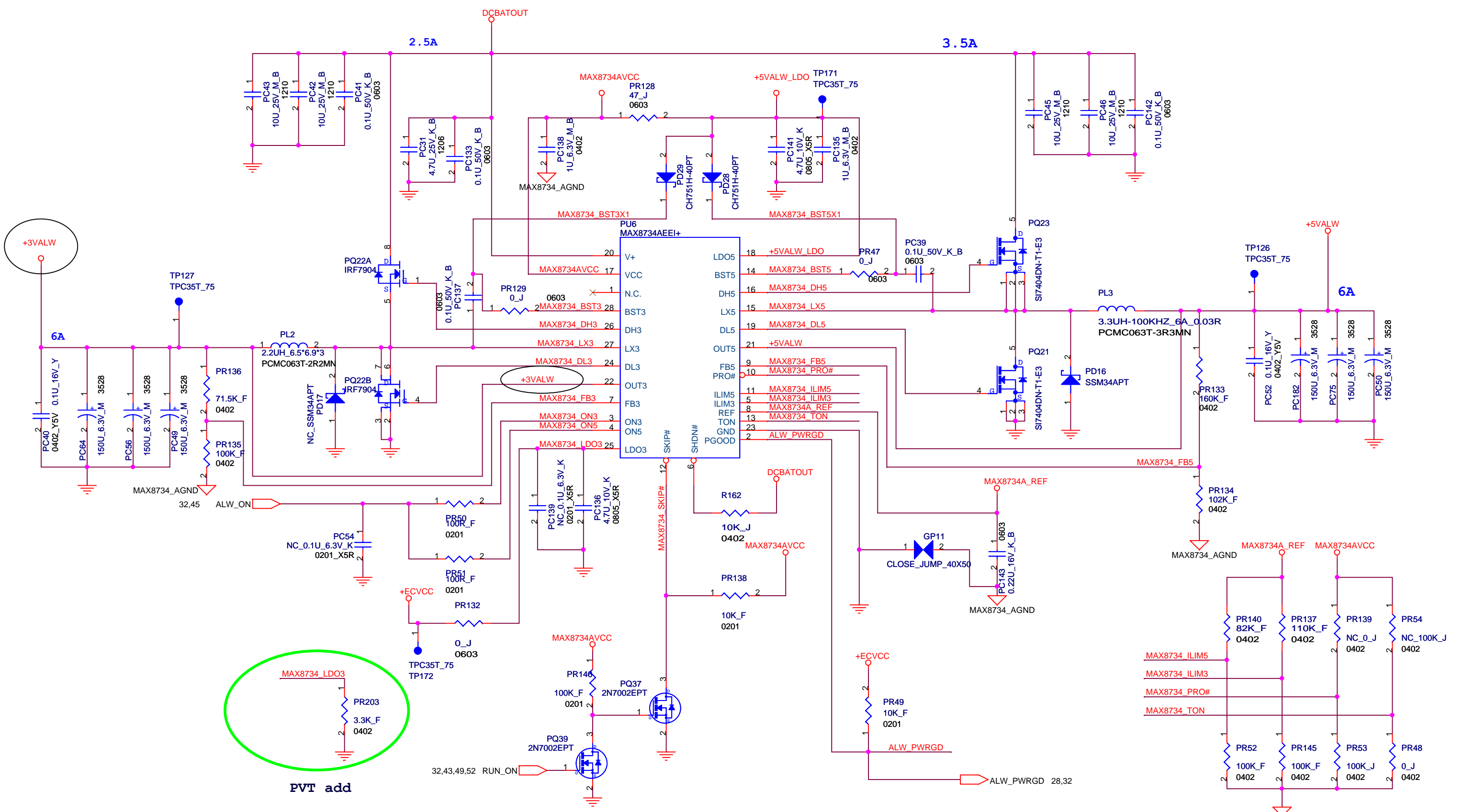
PVT Change to GB11261_1051_7F



PVT Change to GB11261_1051_7F







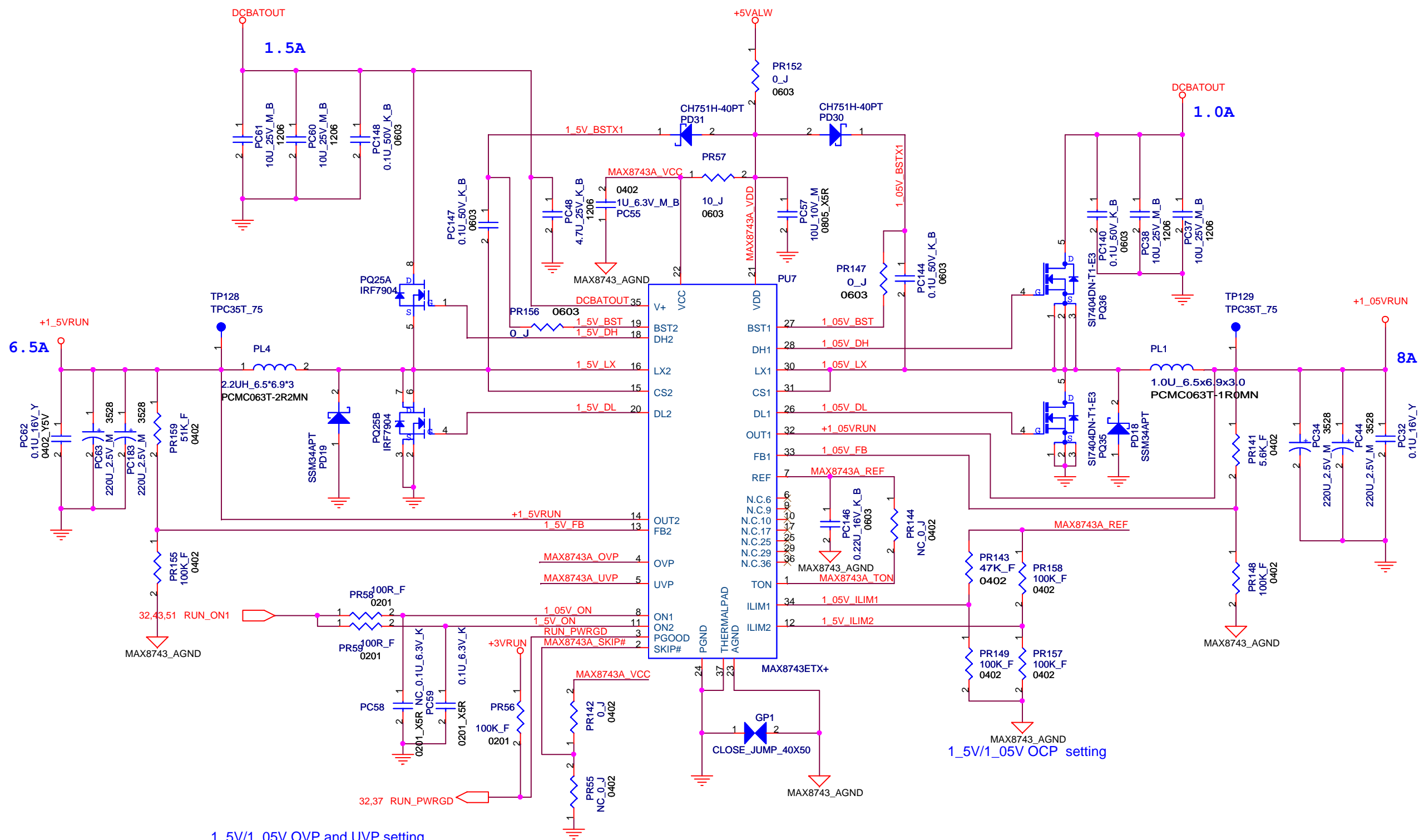
+3VALW

MAX8734_LDO3
PR203
3.3K_F
0402

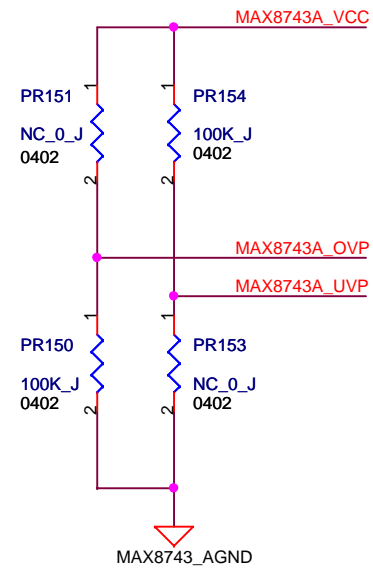
PVT add

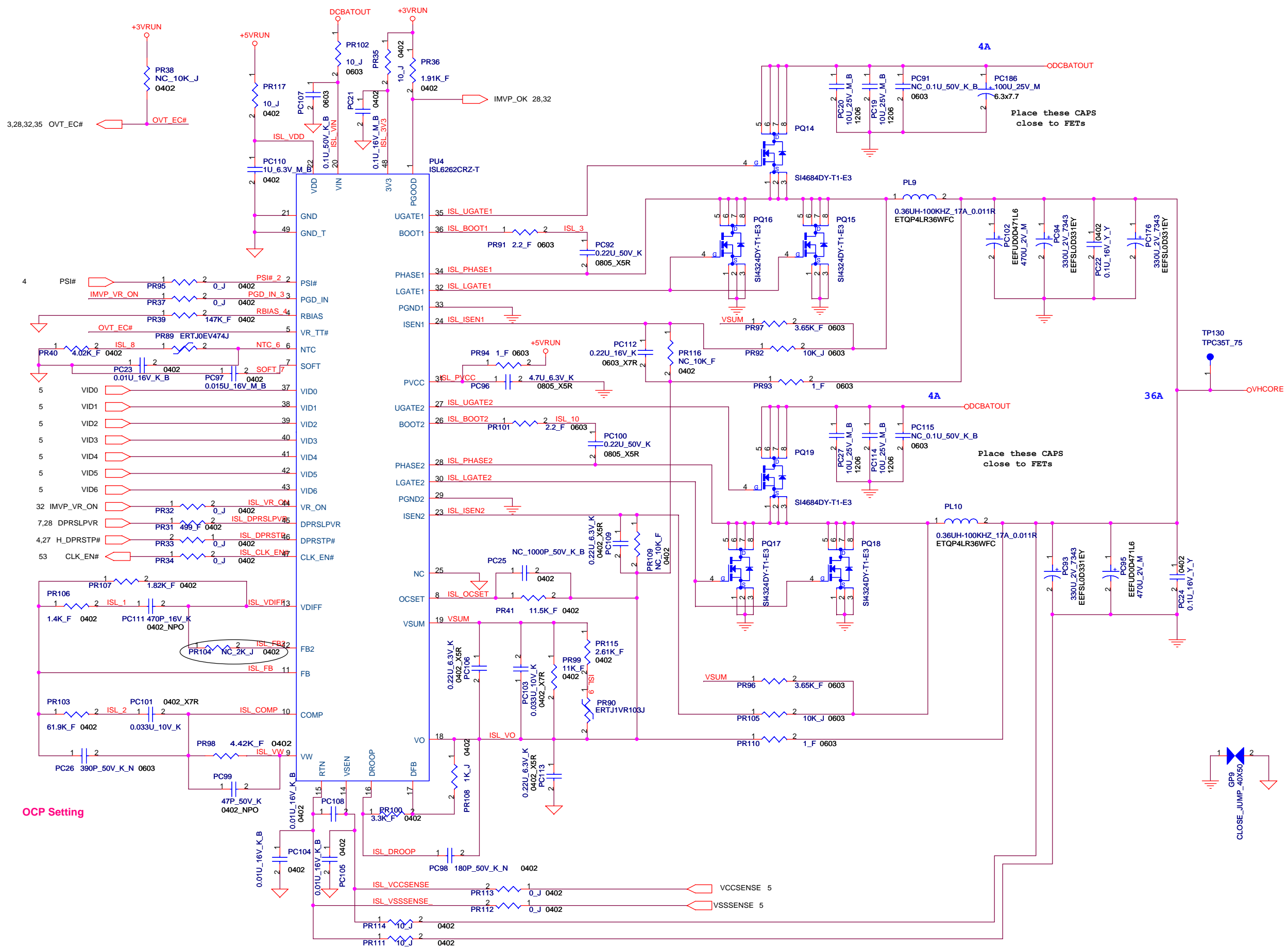
TON connect to GND = 5V/400KHZ, 3.3V/500KHZ
ILIM5/ILIM3 for setting OCP

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Title SYS Power (3D3VALW/5VALW)		
Size A3	Document Number MS60-1-01 (MBX-159)	Rev 0.30
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1_5V/1_05V OVP and UVP setting

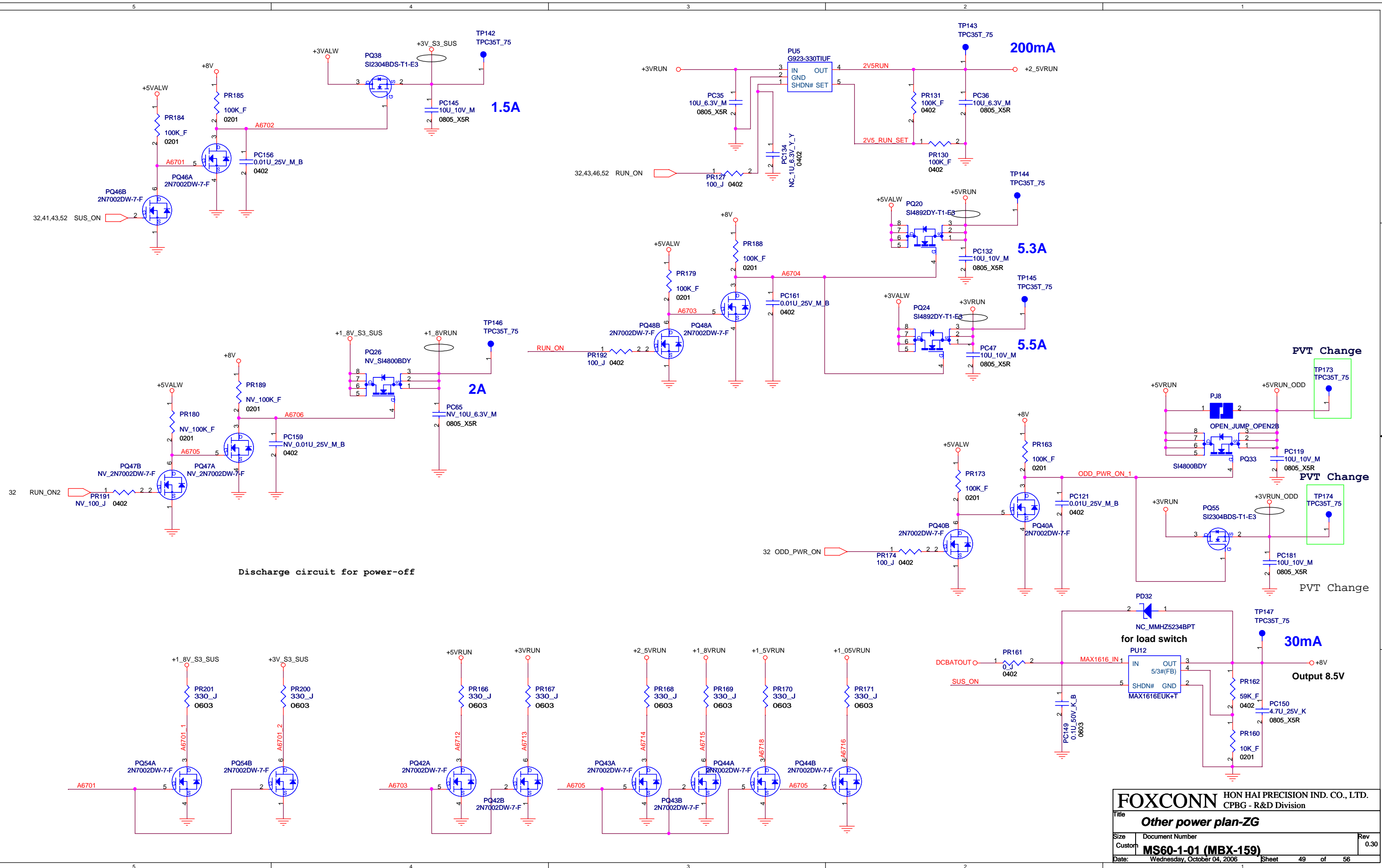




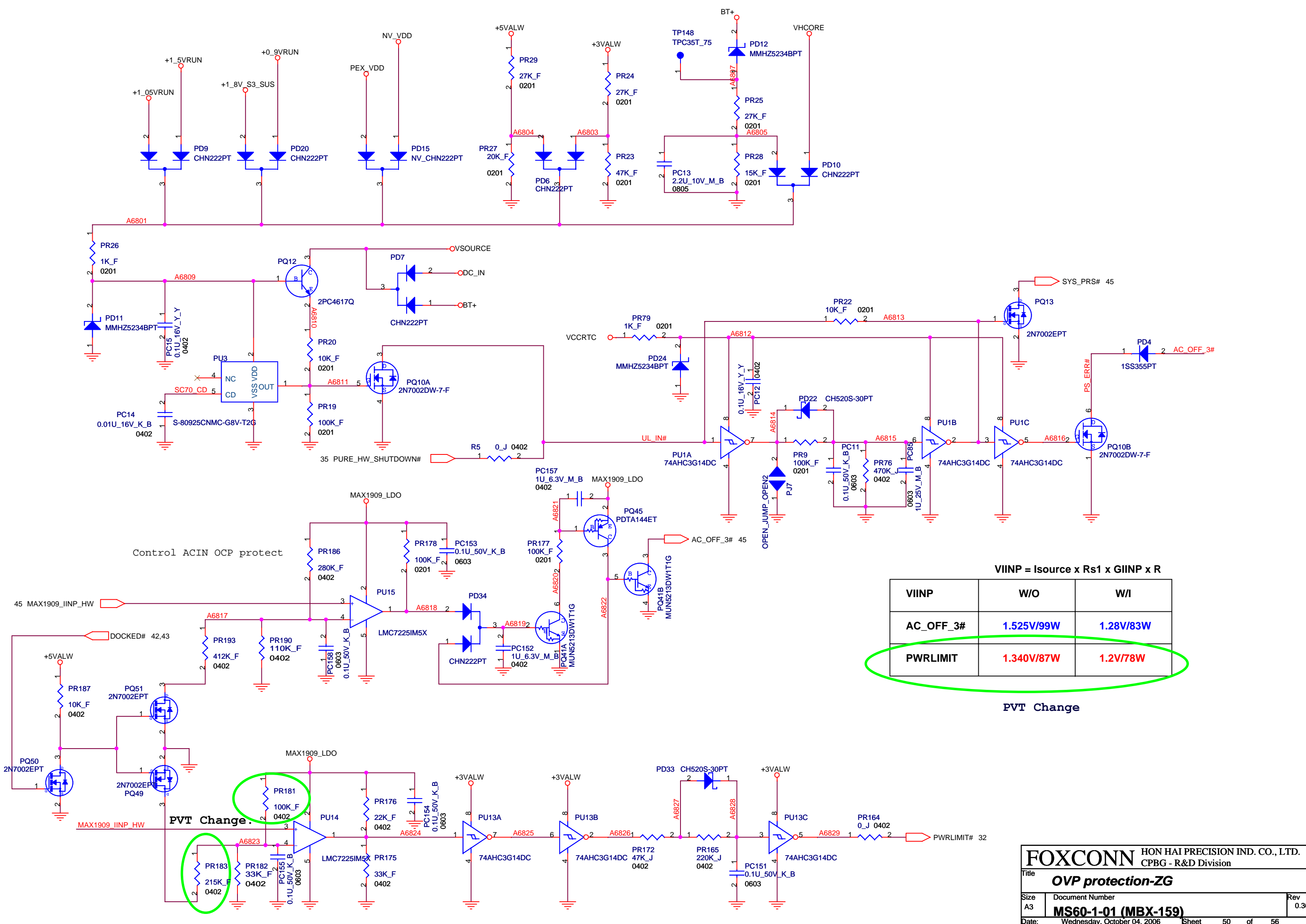
OCP Setting

- VID0 1 TP131 TPC35T_75
- VID1 1 TP133 TPC35T_75
- VID2 1 TP135 TPC35T_75
- VID3 1 TP137 TPC35T_75
- VID4 1 TP139 TPC35T_75
- VID5 1 TP140 TPC35T_75
- VID6 1 TP141 TPC35T_75
- DPRSLPVR 1 TP132 TPC35T_75
- IMVP_VR_ON 1 TP134 TPC35T_75
- PSi# 1 TP136 TPC35T_75
- H_DPRSTP# 1 TP138 TPC35T_75

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CPBG - R&D Division	
Title VHCORE(ISL6262)	
Size Custom	Document Number MS60-1-01 (MBX-159)
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Discharge circuit for power-off

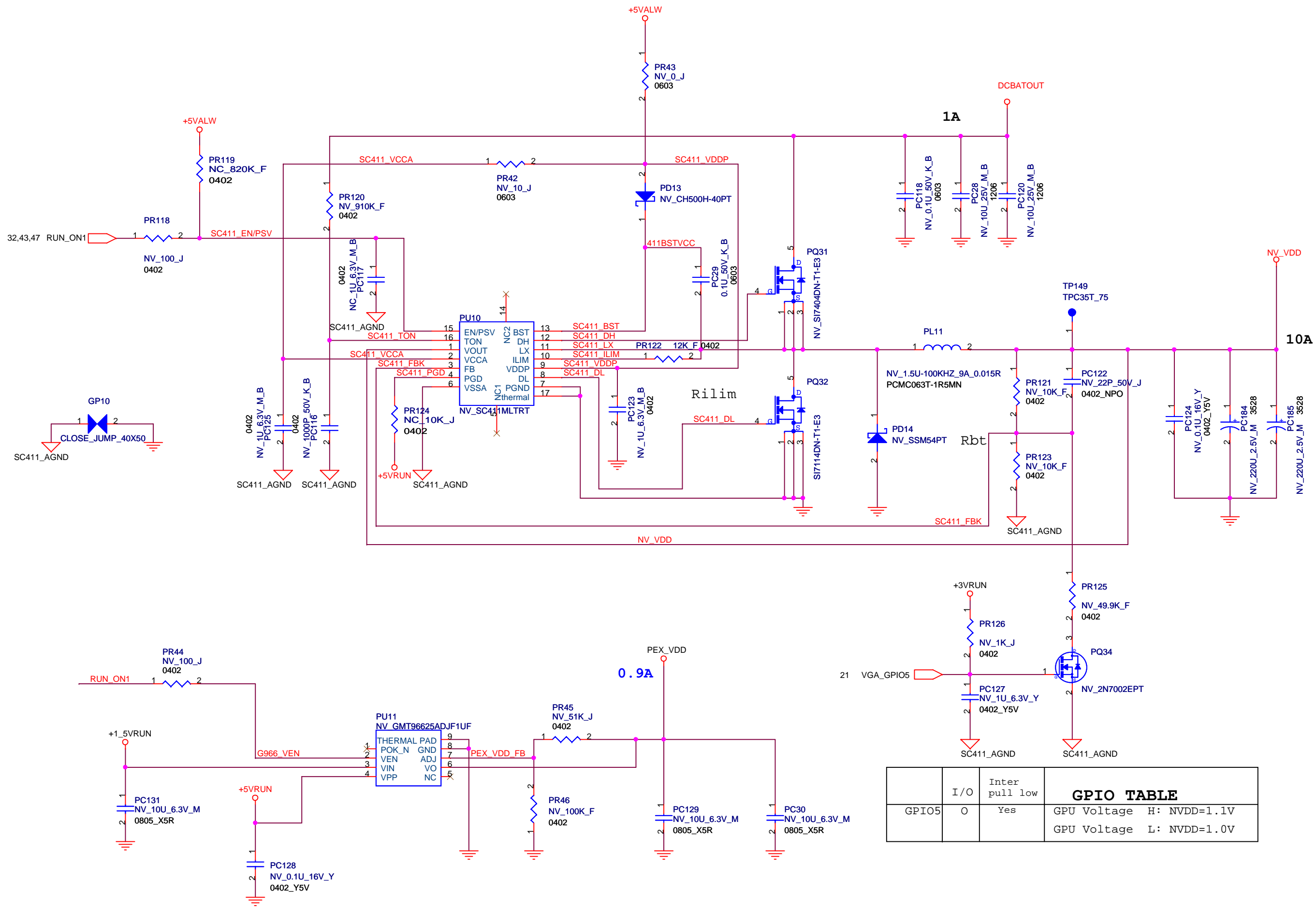


Control ACIN OCP protect

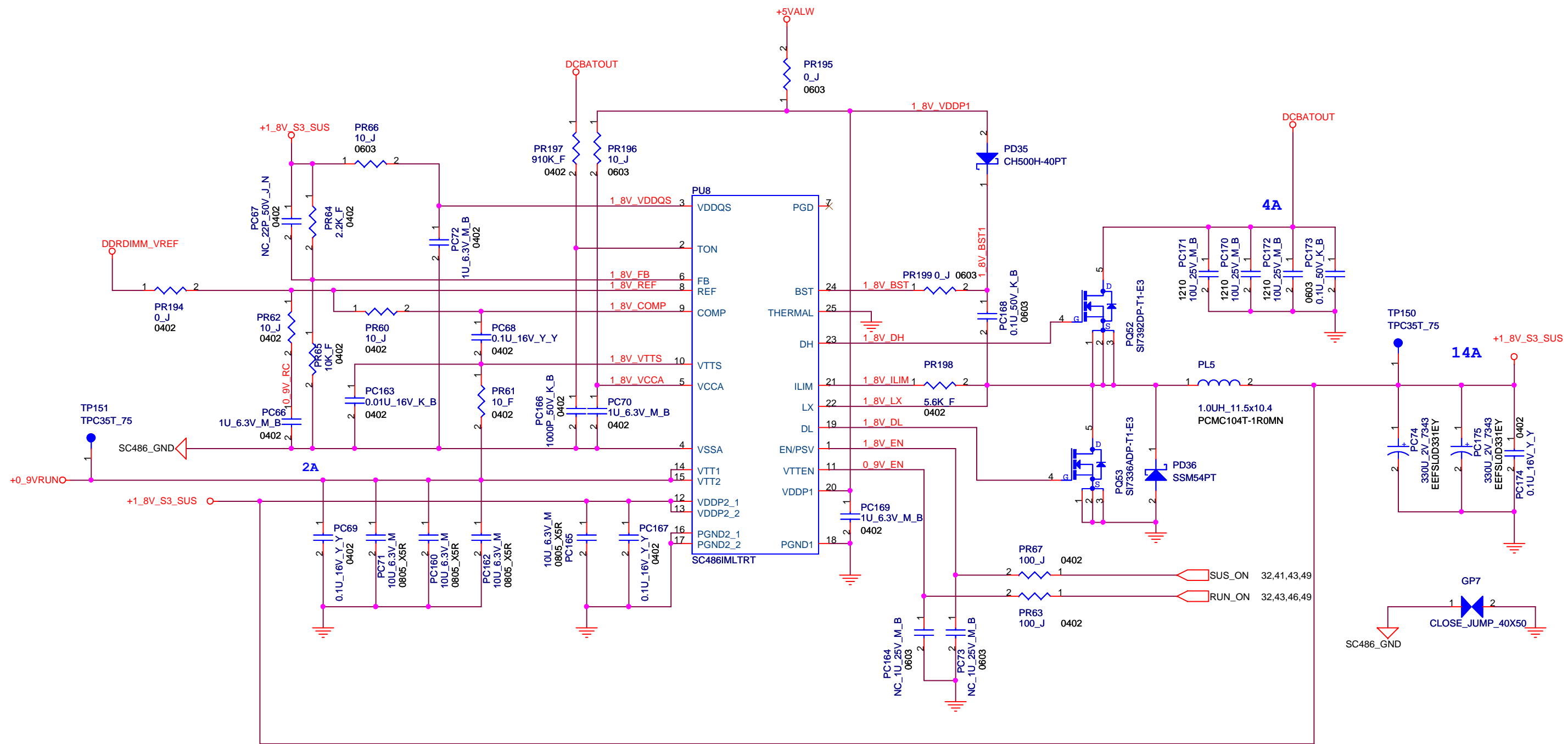
$$VIINP = I_{source} \times R_{s1} \times GIINP \times R$$

VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.340V/87W	1.2V/78W

PVT Change



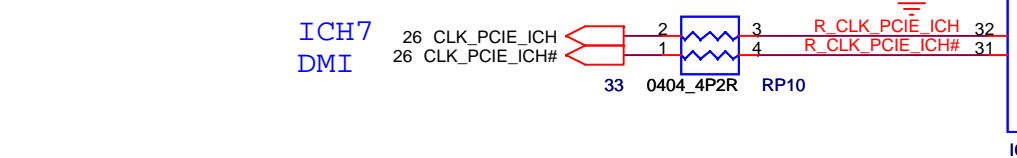
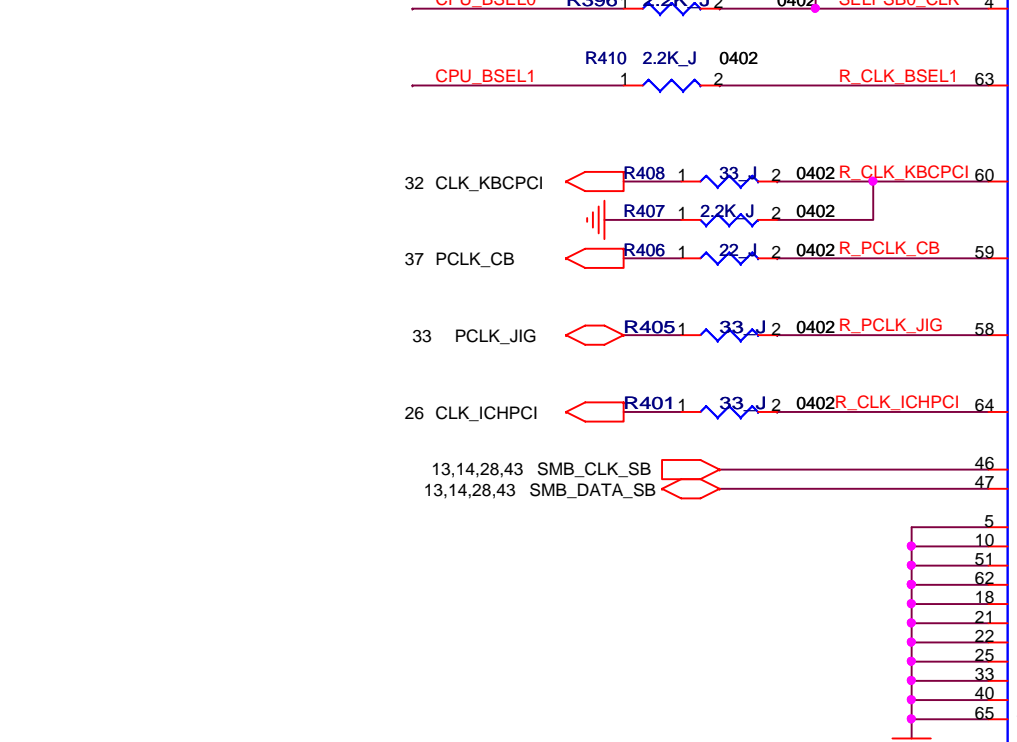
GPIO TABLE		
I/O	Inter pull low	
GPIO5	0	Yes
		GPU Voltage H: NVDD=1.1V
		GPU Voltage L: NVDD=1.0V



NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	CLK_ICHPCI

close to clk gen (For EMI)

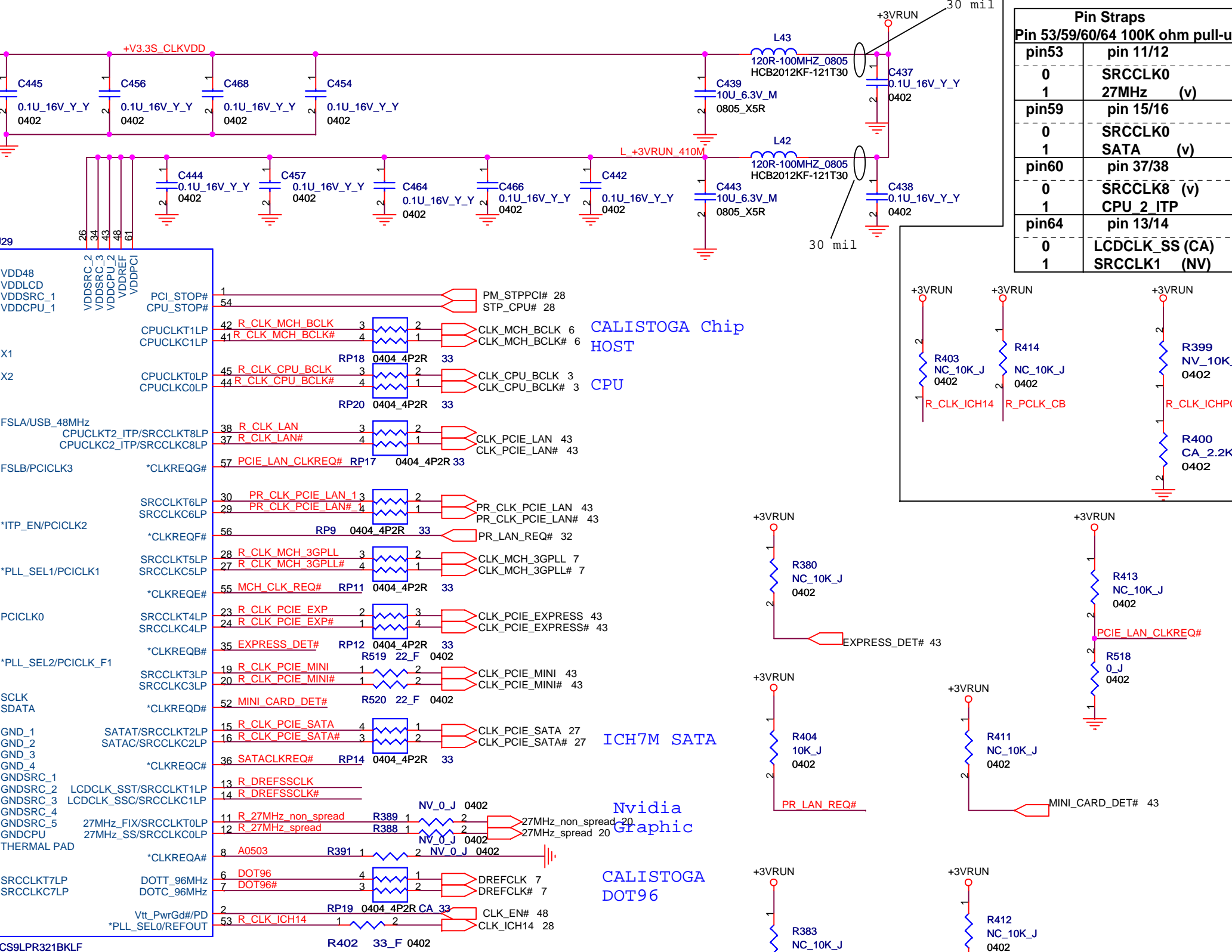
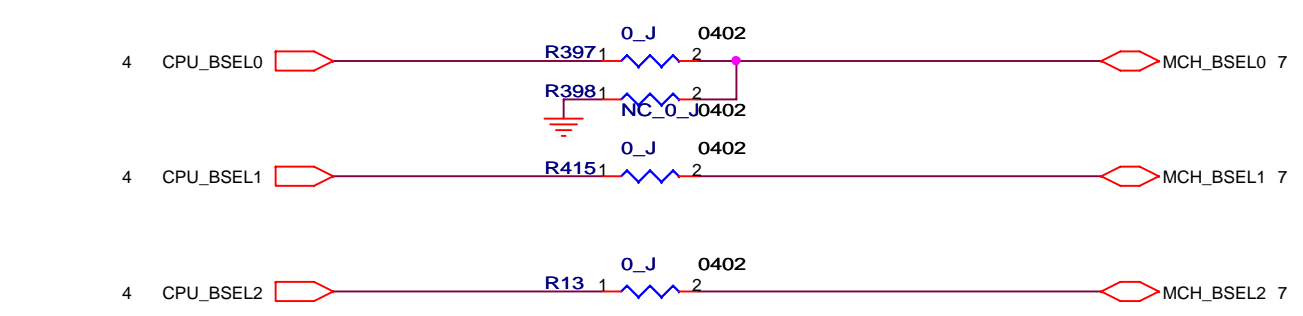
Length as short as possible.



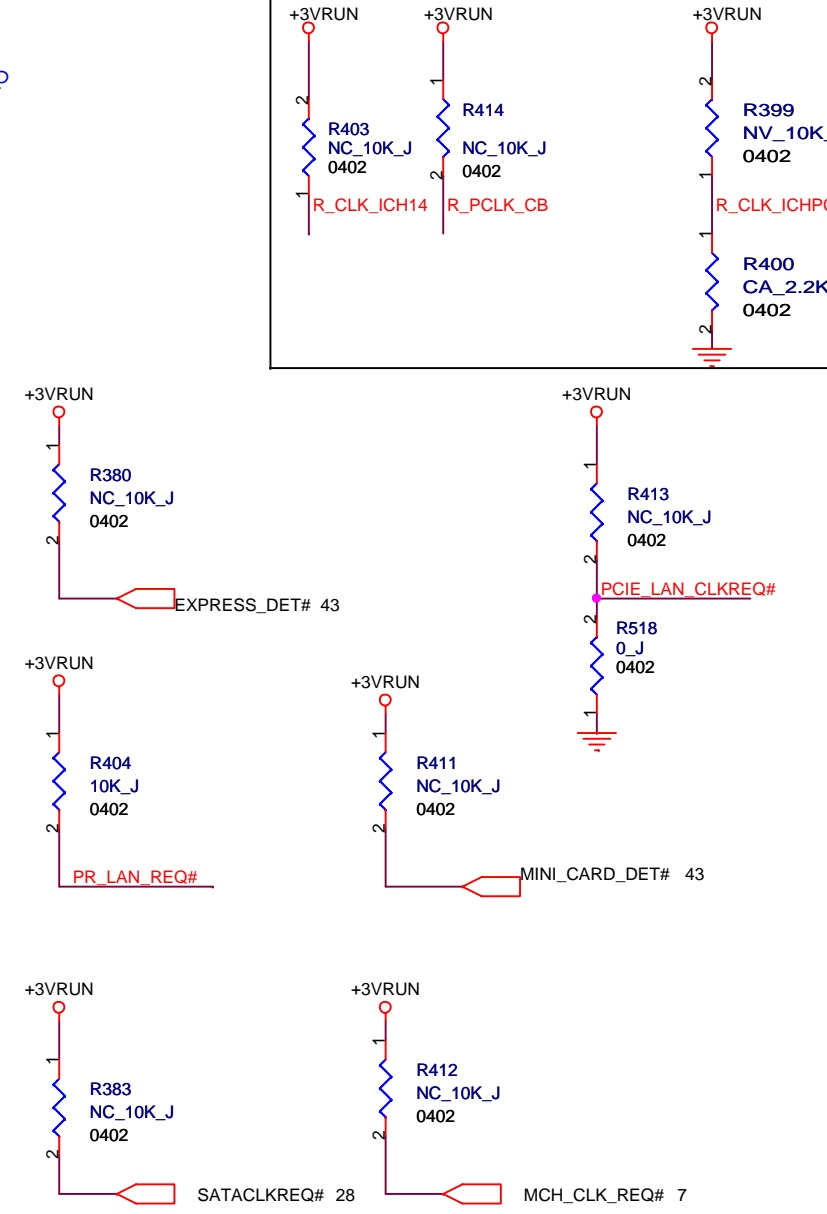
SM bus Address : 1101001 (ICH7)
For clock generator

FSB Frequency Table:

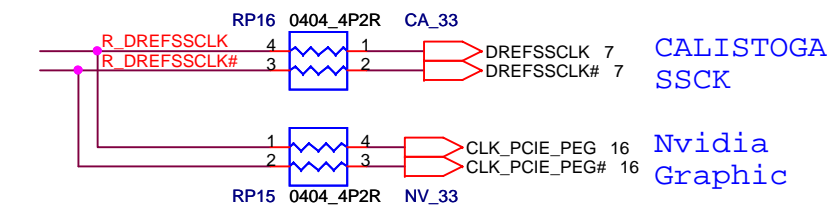
FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33

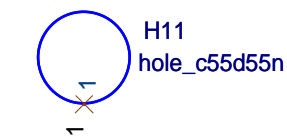
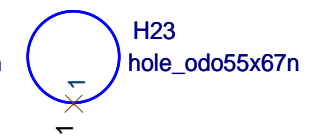
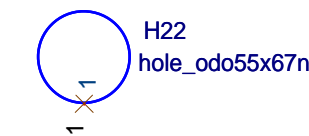
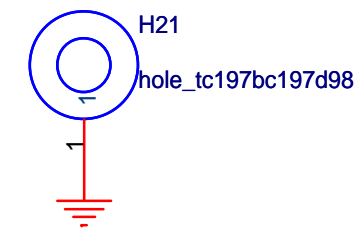
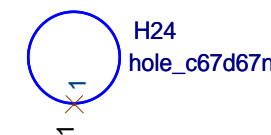
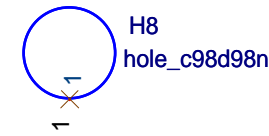
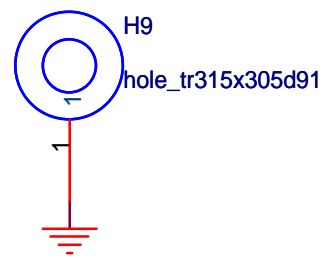
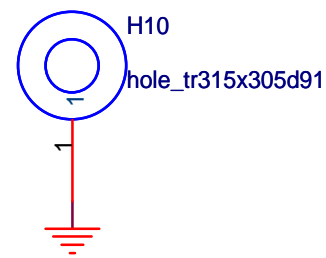
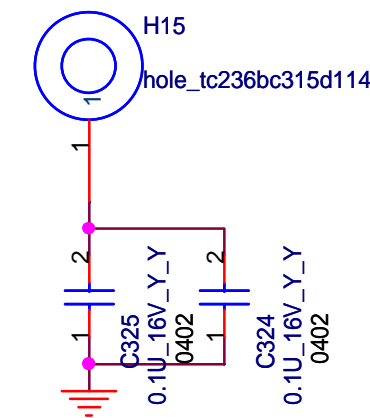
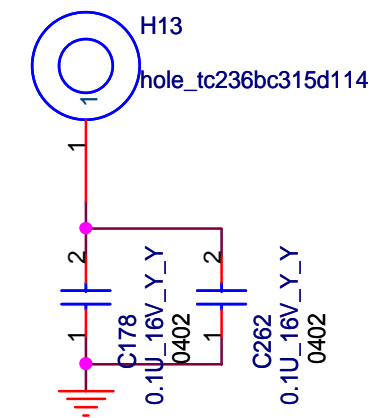
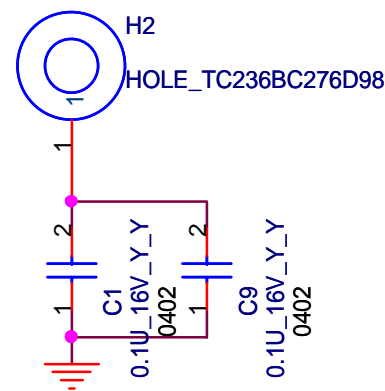
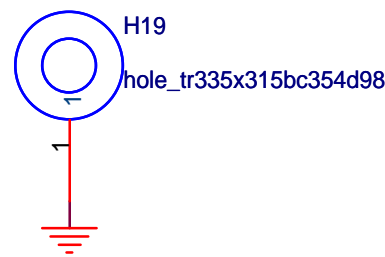
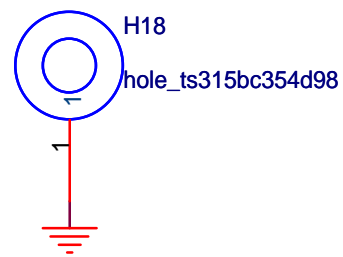
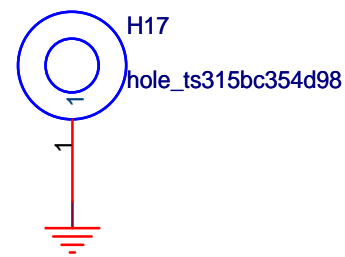
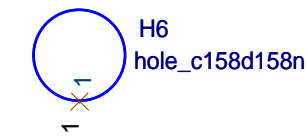
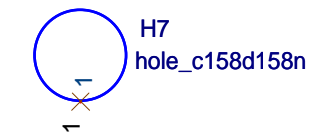
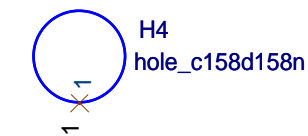
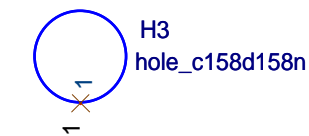
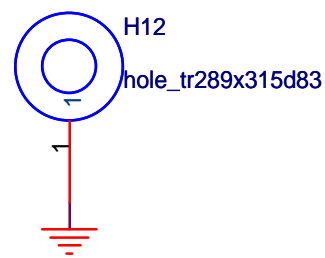
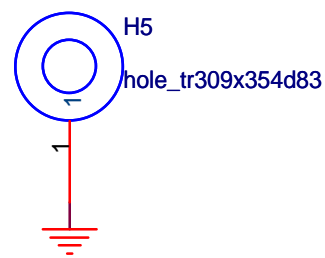
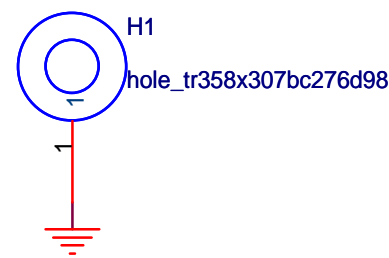


Pin Straps			
Pin 53/59/60/64 100K ohm pull-up			
pin53	pin 11/12	0	SRCCLK0
		1	27MHz (v)
pin59	pin 15/16	0	SRCCLK0
		1	SATA (v)
pin60	pin 37/38	0	SRCCLK8 (v)
		1	CPU 2 ITP
pin64	pin 13/14	0	LCDCLK_SS (CA)
		1	SRCCLK1 (NV)

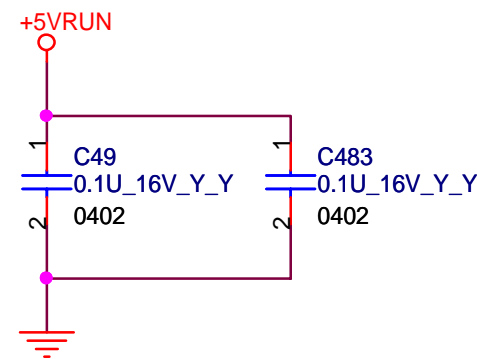
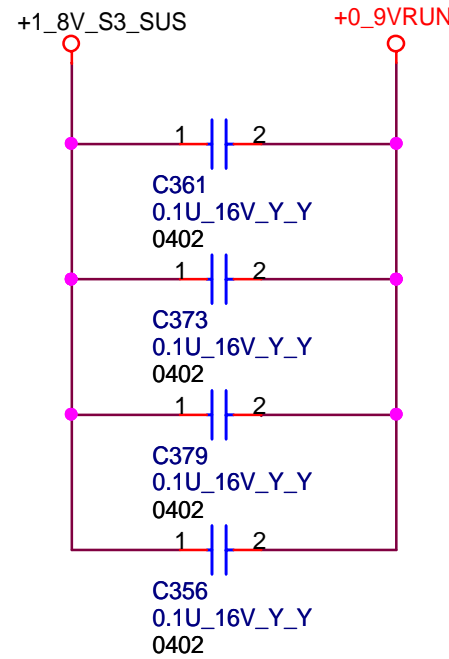
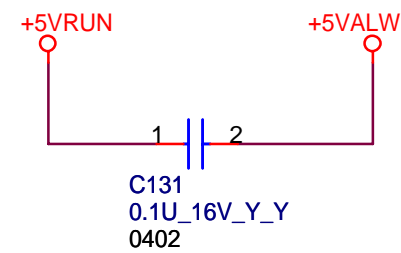
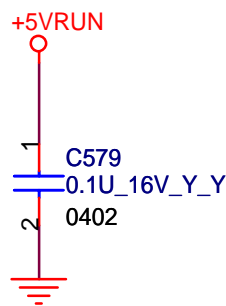
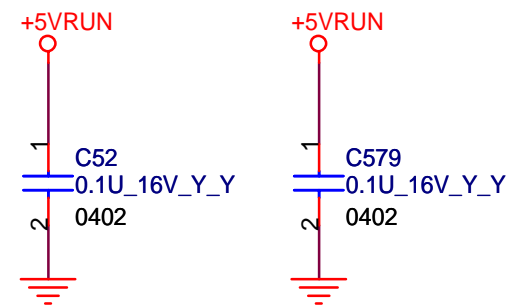


CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
If EVT ok, del them in DVT





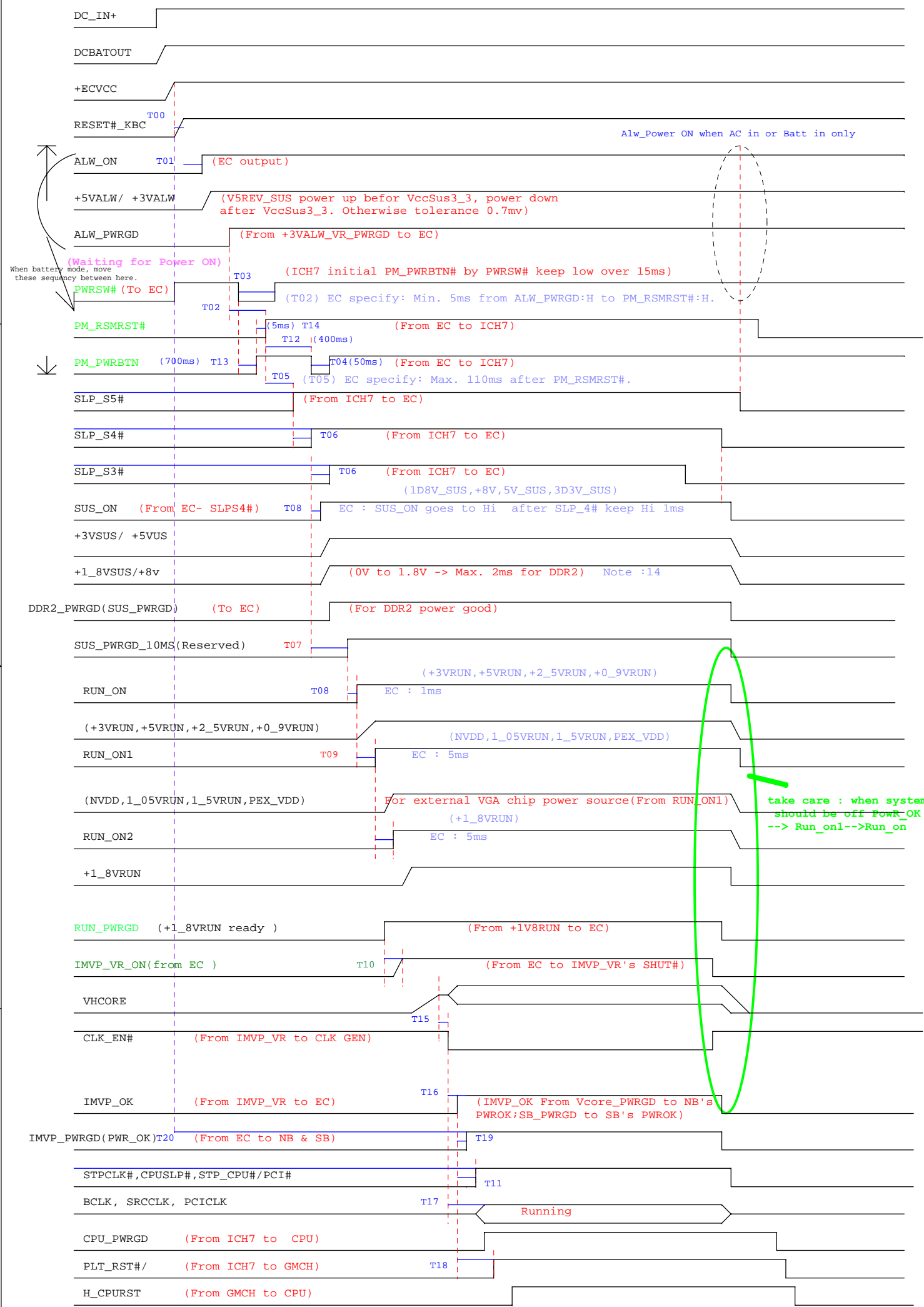
FOR EMI



FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title HOLE		
Size A4	Document Number MS60-1-01 (MBX-159)	Rev 0.30
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MS60 Power On Sequence Timing

Version : 0.0
Modified date : 2/14/2006

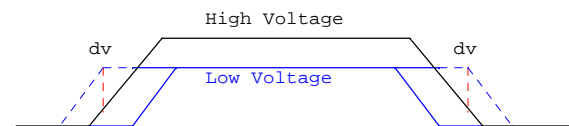


NOTE : (EC KB3910 Min. response time is 1ms)

- T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
- T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
- T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
- T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing)
- T06(Please reference Intel 16971 Page 301 of t234 timing)
- T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
- T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
- T09 : For MS01 current SPEC
- T10 :Please refer to Intel 16971 Page 300 of t214 timing
- T11 :Please refer to Intel 16971 Page 303 of t216 timing
- T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing)
- T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
- In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
- T15 : Please refer to MAX8771 datasheet
- T16: Please refer to MAX8771 datasheet
- T17 : Please refer to Intel CK410(14690) page 53
- T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark : (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- +1.5VRUN -> +GMCH(1.05V), dt:0.7mV
- +3.3VRUN -> +2.5VRUN, dt:0.3mV
- +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3.3VRUN -> +1.5VRUN(TV), dt:0.7mV



R/C delay
(47K/
0.1uF)

T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns~2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	

