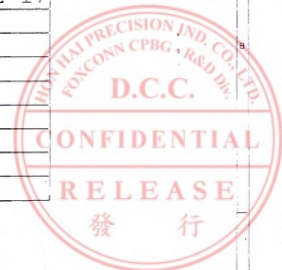


Schematics Page Index (Title / Revision / Change Date)

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02	Block Diagram	0.30	05'12'17	37	EC+KBC	0.30	05'12'17
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04	Yonah(HOST BUS) 2/3	0.30	05'12'17	39	LED/LID SW#/Touch PAD	0.30	05'12'17
05	Yonah(Power/Gnd) 3/3	0.40	06'02'08	40	Mini-PCIE Card	0.30	05'12'17
06	CALISTOGA (HOST) 1/7	0.30	05'12'17	41	FAN/Bluetooth	0.40	06'02'08
07	CALISTOG (DMI) 2/7	0.30	05'12'17	42	EXPRESS/CAM/OIDE	0.40	06'02'08
08	CALIST (GRAPHIC) 3/7	0.30	05'12'17	43	AUDIO(CODEC & POWER)	0.30	05'12'17
09	CALISTOGA (DDRII) 4/7	0.30	05'12'17	44	AUDIO( AMP & HP & SPK)	0.40	06'02'08
10	CALIST (POWER,VCC) 5/7	0.30	05'12'17	45	AUDIO( EXTMIC&PHONE OUT)	0.30	05'12'17
11	CALIST (VCC CORE) 6/7	0.30	05'12'17	46	AUDIO (MUTE & INTMIC)	0.40	06'02'08
12	CALIST (VSS) 7/7	0.30	05'12'17	47	AUDIO (PHONE OUT)	0.30	05'12'17
13	DDRII(SO-DIMM 0) 1/3	0.30	05'12'17	48	PCI (PCI BUS)	0.30	05'12'17
14	DDRII(SO-DIMM 1) 2/3	0.30	05'12'17	49	PCI ( ILINK)	0.30	05'12'17
15	DDRII(Termination) 3/3	0.30	05'12'17	50	PCI (MS-DUO/MDC)	0.30	05'12'17
16	VGA(PCI-E/STRAP) 1/8	0.30	05'12'17	51	PCI ( PGMCIA)	0.30	05'12'17
17	VGA(PCI-E/STRAP) 2/8	0.30	05'12'17	52	USB2.0/DOCKING CONN.	0.30	05'12'17
18	VGA(GDDR) 3/8	0.30	05'12'17	53	USB HUB	0.30	05'12'17
19	VGA(POWER) 4/8	0.30	05'12'17	54	LAN (82562GT)	0.30	05'12'17
20	VGA(POWER) 5/8	0.30	05'12'17	55	Power Design Diagram	0.30	05'12'17
21	VGA(POWER) 6/8	0.40	06'02'08	56	DCLN&Charger	0.30	05'12'17
22	VGA(MULTIUSE) 7/8	0.30	05'12'17	57	SYS Power (+3 3V/+5V)	0.30	05'12'17
23	VGA(LVDS/VDAC ) 8/8	0.30	05'12'17	58	SYS Power(+1 5V/+1 05V)	0.30	05'12'17
24	VRAM(GDDR) 1/5	0.30	05'12'17	59	DDR2 Power(+1 8V/+0 9V)	0.30	05'12'17
25	VRAM(GDDR) 2/5	0.30	05'12'17	60	CPU Vcore ---MAX8771	0.30	05'12'17
26	VRAM(POWERBYPASS) 3/4	0.30	05'12'17	61	Others power plan	0.30	05'12'17
27	VRAM(POWERBYPASS) 4/4	0.30	05'12'17	62	OVP protection	0.30	05'12'17
28	LVDS	0.30	05'12'17	63	VGA POWER(+1 1V/ +1 2V)	0.30	05'12'17
29	CRT	0.30	05'12'17	64	CLOCK GEN	0.30	05'12'17
30	S-VIDEO/Semi-PnP	0.30	05'12'17	65	HOLE	0.30	05'12'17
31	ICH7-M( PCI/USB ) 1/5	0.30	05'12'17	66	History ( 1 )	0.30	05'12'17
32	ICH7-M( LPC, IDE, SATA ) 2/5	0.40	06'02'08				
33	ICH7-M( GPIO) 3/5	0.30	05'12'17				
34	ICH7-M( POWER) 4/5	0.30	05'12'17				
35	ICH7-M( GND) 5/5	0.30	05'12'17				

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P. Leader	Check by	Design by
陳秋福	陳光偉	黃恩凱

Project Code & Schematics Subject: MS11 Main Board      PCB P/N: 1P-0062100-8010 (FUBAI)  
 1P-0062200-8010 (NAN YA)  
 1P-0062500-8010HANSTAR

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

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10	CALIST (POWER,VCC) 5/7	0.30	05'12'17
11	CALIST (VCC CORE) 6/7	0.30	05'12'17
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13	DDR2(SO-DIMM_0) 1/3	0.30	05'12'17
14	DDR2(SO-DIMM_1) 2/3	0.30	05'12'17
15	DDR2(Termination) 3/3	0.30	05'12'17
16	VGA(PCI-E/STRAP) 1/8	0.30	05'12'17
17	VGA(PCI-E/STRAP) 2/8	0.30	05'12'17
18	VGA(GDDR) 3/8	0.30	05'12'17
19	VGA(POWER) 4/8	0.30	05'12'17
20	VGA(POWER) 5/8	0.30	05'12'17
21	VGA(POWER) 6/8	0.40	06'02'08
22	VGA(MULTIUSE) 7/8	0.30	05'12'17
23	VGA(LVDS/VDAC) 8/8	0.30	05'12'17
24	VRAM(GDDR) 1/5	0.30	05'12'17
25	VRAM(GDDR) 2/5	0.30	05'12'17
26	VRAM(POWERBYPASS) 3/4	0.30	05'12'17
27	VRAM(POWERBYPASS) 4/4	0.30	05'12'17
28	LVDS	0.30	05'12'17
29	CRT	0.30	05'12'17
30	S-VIDEO/Semi-PnP	0.30	05'12'17
31	ICH7-M(PCI/USB) 1/5	0.30	05'12'17
32	ICH7-M(LPC,IDE,SATA) 2/5	0.40	06'02'08
33	ICH7-M(GPIO) 3/5	0.30	05'12'17
34	ICH7-M(POWER) 4/5	0.30	05'12'17
35	ICH7-M(GND) 5/5	0.30	05'12'17

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40	Mini-PCIE Card	0.30	05'12'17
41	FAN/Bluetooth	0.40	06'02'08
42	EXPRESS/CAM/OIDE	0.40	06'02'08
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44	AUDIO(AMP & HP & SPK)	0.40	06'02'08
45	AUDIO(EXTMIC&PHONE OUT)	0.30	05'12'17
46	AUDIO(MUTE & INTMIC)	0.40	06'02'08
47	AUDIO(PHONE OUT)	0.30	05'12'17
48	PCI(PCI BUS)	0.30	05'12'17
49	PCI(ILINK)	0.30	05'12'17
50	PCI(MS-DUO/MDC)	0.40	06'02'08
51	PCI(PCMCIA)	0.30	05'12'17
52	USB2.0/DOCKING CONN.	0.30	05'12'17
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54	LAN(82562GT)	0.30	05'12'17
55	Power Design Diagram	0.30	05'12'17
56	DCIN&Charger	0.30	05'12'17
57	SYS Power(+3_3V/+5V)	0.30	05'12'17
58	SYS Power(+1_5V/+1_05V)	0.30	05'12'17
59	DDR2 Power(+1_8V/+0_9V)	0.30	05'12'17
60	CPU_Vcore ---MAX8771	0.30	05'12'17
61	Others power plan	0.30	05'12'17
62	OVP protection	0.30	05'12'17
63	VGA POWER(+1_1V/ +1_2V)	0.30	05'12'17
64	CLOCK GEN	0.30	05'12'17
65	HOLE	0.30	05'12'17
66	History ( 1 )	0.30	05'12'17

CONFIDENTIAL



P. Leader	Check by	Design by

**Project Code & Schematics Subject:** MS11 Main Board

**PCB P/N:** 1P-0062100-8010 (FUBAI)  
 1P-0062200-8010 (NAN YA)  
 1P-0062500-8010(HANSTAR)

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

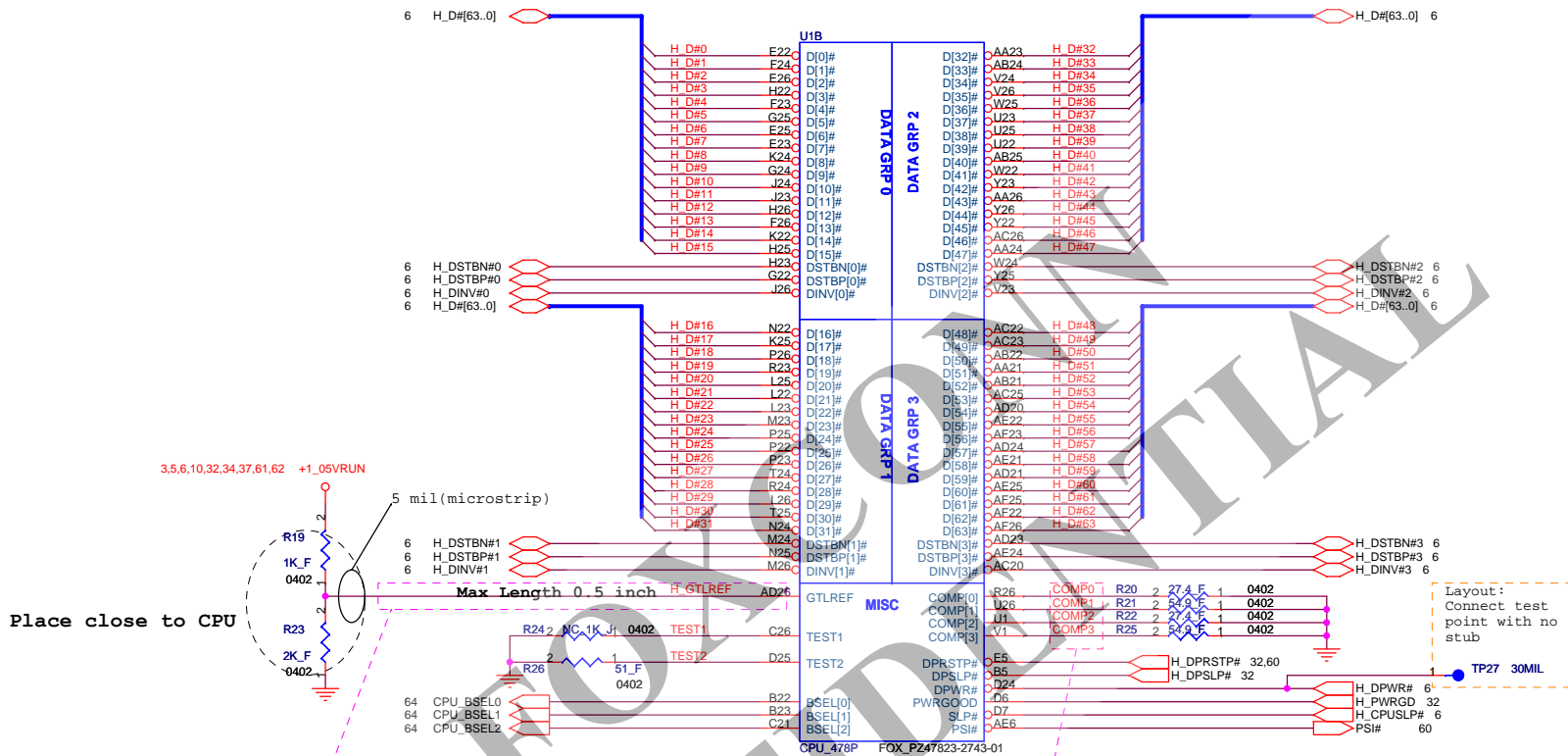
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3.5,6,10,32,34,37,61,62 +1\_05VRUN

5 mil(microstrip)

Place close to CPU

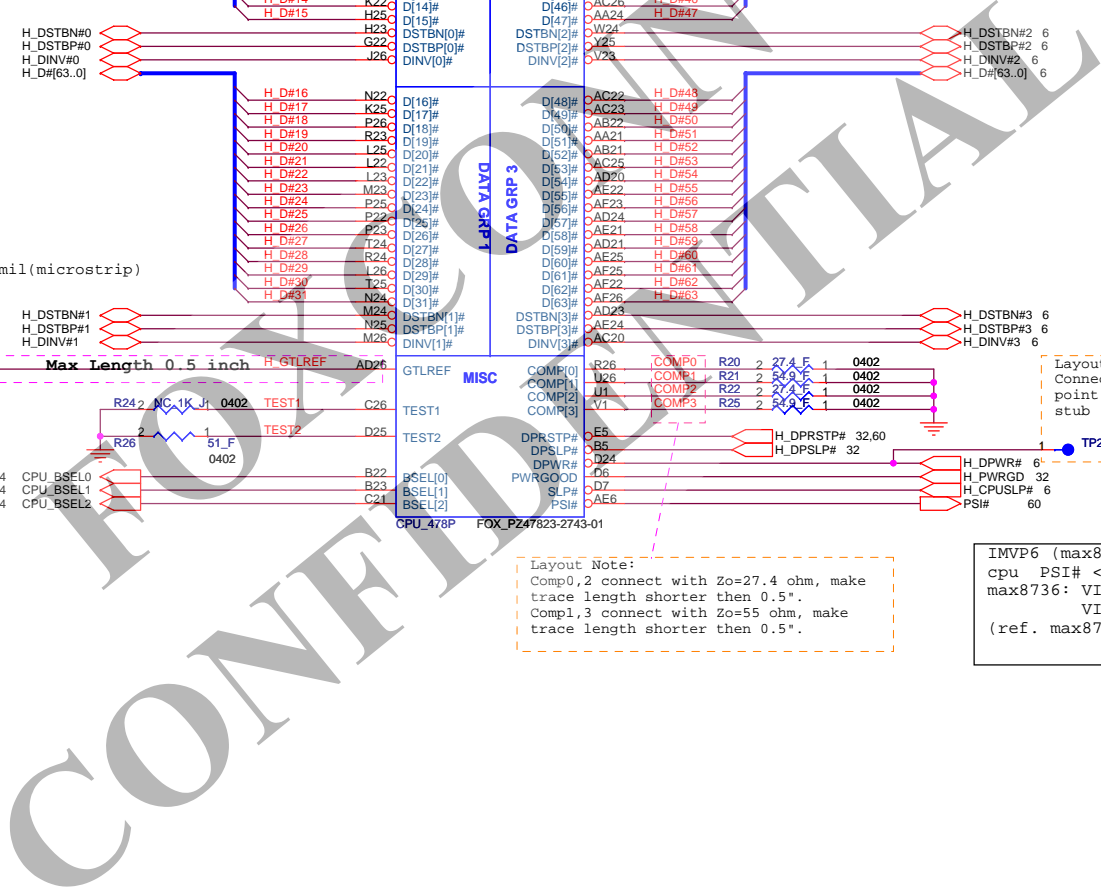
Max Length 0.5 inch H\_GTLREF

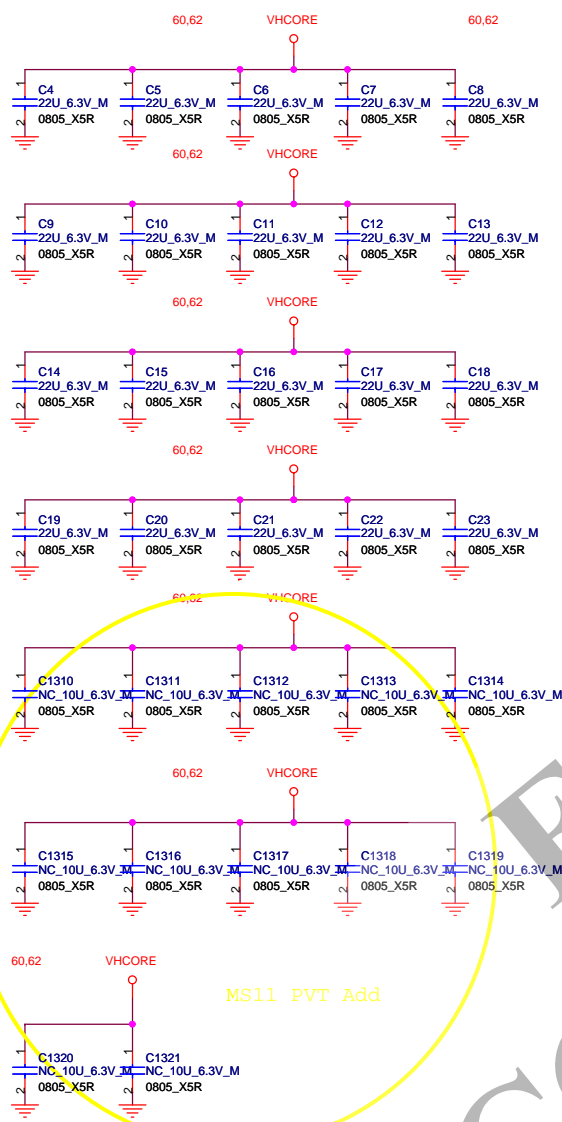
Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.

Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make  
trace length shorter then 0.5".  
Comp1, 3 connect with Zo=55 ohm, make  
trace length shorter then 0.5".

Layout:  
Connect test  
point with no  
stub

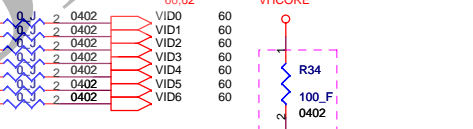
IMVP6 (max8736)  
cpu PSI# <-> max8736 PSI#  
max8736: VIHmin=0.67V  
VILmax=0.33V  
(ref. max8736 datasheet )





Pin	Signal	Value
A7	VCC[001]	AB20
A9	VCC[002]	AB7
A10	VCC[003]	AC7
A12	VCC[004]	AC9
A13	VCC[005]	AC12
A15	VCC[006]	AC13
A17	VCC[007]	AC15
A18	VCC[008]	AC17
A20	VCC[009]	AC18
B7	VCC[010]	AD7
B9	VCC[011]	AD9
B10	VCC[012]	AD10
B12	VCC[013]	AD12
B14	VCC[014]	AD14
B15	VCC[015]	AD15
B17	VCC[016]	AD17
B18	VCC[017]	AD18
B20	VCC[018]	AD19
C9	VCC[019]	AD20
C10	VCC[020]	AE10
C12	VCC[021]	AE13
C13	VCC[022]	AE15
C15	VCC[023]	AE17
C17	VCC[024]	AE18
C18	VCC[025]	AE20
D9	VCC[026]	AF9
D10	VCC[027]	AF10
D12	VCC[028]	AF12
D14	VCC[029]	AF14
D15	VCC[030]	AF15
D17	VCC[031]	AF17
D18	VCC[032]	AF18
E7	VCC[033]	AF20
E9	VCC[034]	AF20
E10	VCC[035]	AG21
E12	VCC[036]	AG21
E13	VCC[037]	AG21
E15	VCC[038]	AG21
E17	VCC[039]	AG21
E18	VCC[040]	AG21
E20	VCC[041]	AG21
F7	VCC[042]	AG21
F9	VCC[043]	AG21
F10	VCC[044]	AG21
F12	VCC[045]	AG21
F14	VCC[046]	AG21
F15	VCC[047]	AG21
F17	VCC[048]	AG21
F18	VCC[049]	AG21
F20	VCC[050]	AG21
AA7	VCC[051]	AG21
AA9	VCC[052]	AG21
AA10	VCC[053]	AG21
AA12	VCC[054]	AG21
AA13	VCC[055]	AG21
AA15	VCC[056]	AG21
AA17	VCC[057]	AG21
AA18	VCC[058]	AG21
AA20	VCC[059]	AG21
AB9	VCC[060]	AG21
AC10	VCC[061]	AG21
AB10	VCC[062]	AG21
AB12	VCC[063]	AG21
AB14	VCC[064]	AG21
AB15	VCC[065]	AG21
AB17	VCC[066]	AG21
AB18	VCC[067]	AG21

CPU\_VCCA---->120mA  
 CPU\_VCCP----->2.5A  
 CPU\_VCC----->36A

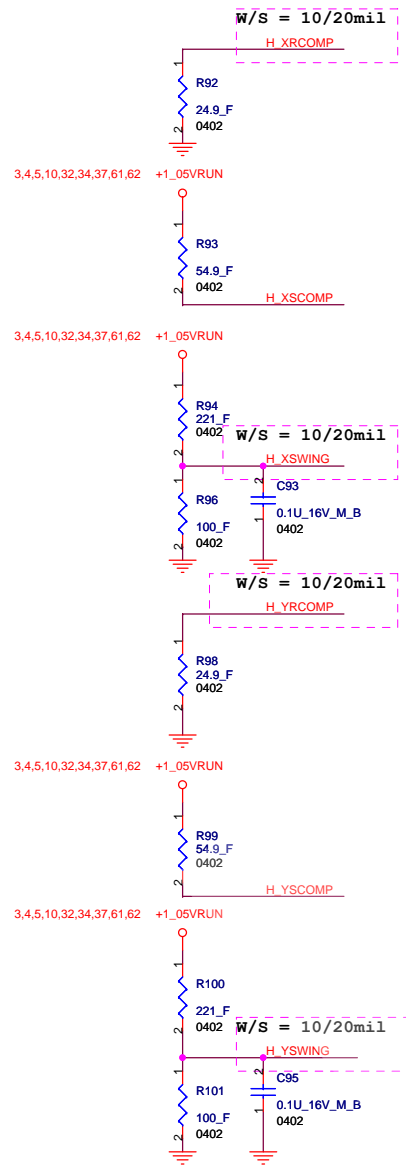


Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.  
 width=18 mil  
 spacing=7 mil

LAYOUT NOTE:  
 Place 0.01uF near PIN B26

PU & PD avoid to route with stub

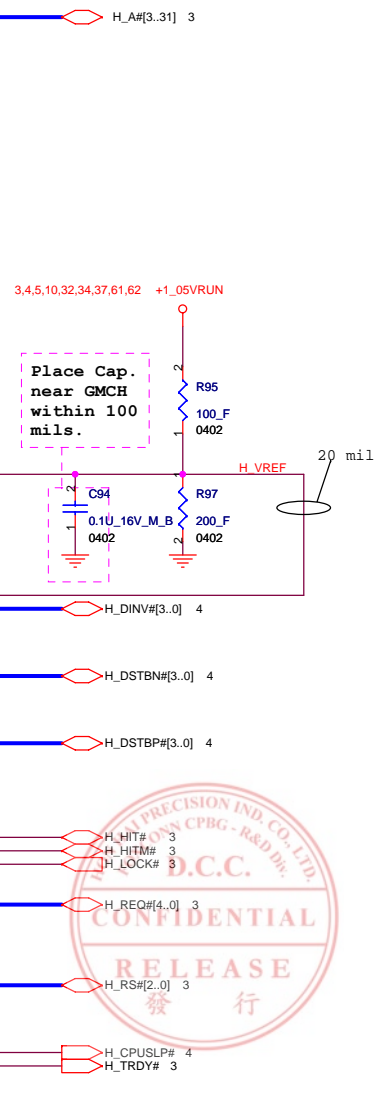
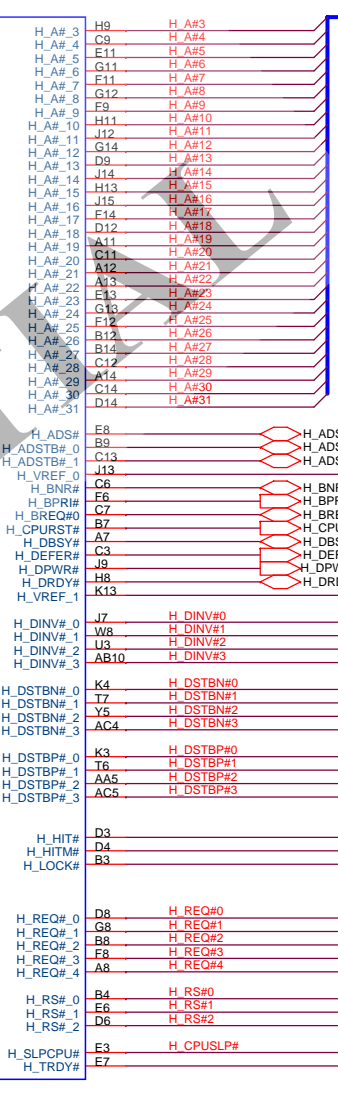
Pin	Signal	Value
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A26	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B9	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D3	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F22	VSS[049]	VSS[130]
F25	VSS[050]	VSS[131]
G4	VSS[051]	VSS[132]
G1	VSS[052]	VSS[133]
G23	VSS[053]	VSS[134]
G26	VSS[054]	VSS[135]
G26	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H21	VSS[058]	VSS[139]
H24	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J22	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K23	VSS[066]	VSS[147]
K26	VSS[067]	VSS[148]
L3	VSS[068]	VSS[149]
L6	VSS[069]	VSS[150]
L21	VSS[070]	VSS[151]
L24	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M5	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]



4 H\_D#[63..0] H\_D#[63..0]

U4A	
H_D#0	F1
H_D#1	J1
H_D#2	H1
H_D#3	J6
H_D#4	H3
H_D#5	K2
H_D#6	G2
H_D#7	G2
H_D#8	K9
H_D#9	K1
H_D#10	K7
H_D#11	J8
H_D#12	H4
H_D#13	J3
H_D#14	K11
H_D#15	G4
H_D#16	T40
H_D#17	W11
H_D#18	T3
H_D#19	U7
H_D#20	U8
H_D#21	U11
H_D#22	T11
H_D#23	W9
H_D#24	T1
H_D#25	T8
H_D#26	T4
H_D#27	W7
H_D#28	U5
H_D#29	T9
H_D#30	W6
H_D#31	T5
H_D#32	AB7
H_D#33	AA9
H_D#34	W4
H_D#35	W3
H_D#36	Y8
H_D#37	Y7
H_D#38	W5
H_D#39	Y10
H_D#40	AB6
H_D#41	W2
H_D#42	AA4
H_D#43	AA7
H_D#44	AA2
H_D#45	AA6
H_D#46	AA10
H_D#47	Y8
H_D#48	AA1
H_D#49	AB4
H_D#50	AC9
H_D#51	AB11
H_D#52	AC11
H_D#53	AB3
H_D#54	AC2
H_D#55	AD1
H_D#56	AD9
H_D#57	AC1
H_D#58	AD7
H_D#59	AC6
H_D#60	AB5
H_D#61	AD10
H_D#62	AD4
H_D#63	AC8
H_XRCOMP	E1
H_XSCOMP	E2
H_XSWING	E4
H_YRCOMP	Y1
H_YSCOMP	U1
H_YSWING	W1
H_CLKIN	AG2
H_CLKIN#	AG1

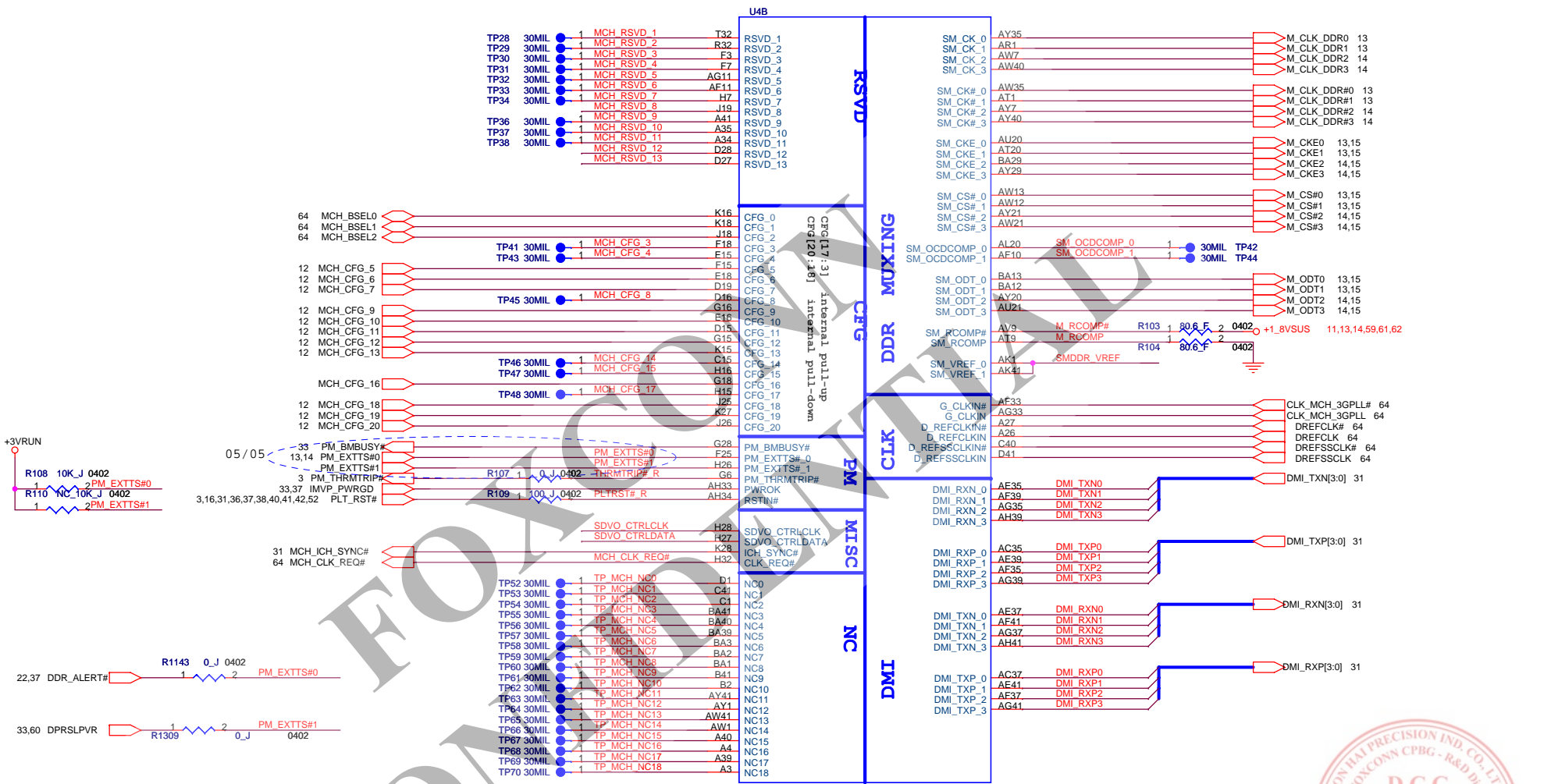
HOST



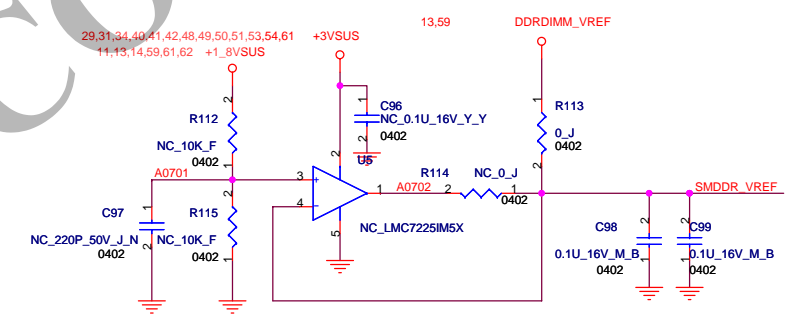
64 CLK\_MCH\_BCLK  
64 CLK\_MCH\_BCLK#

CALISTOGA

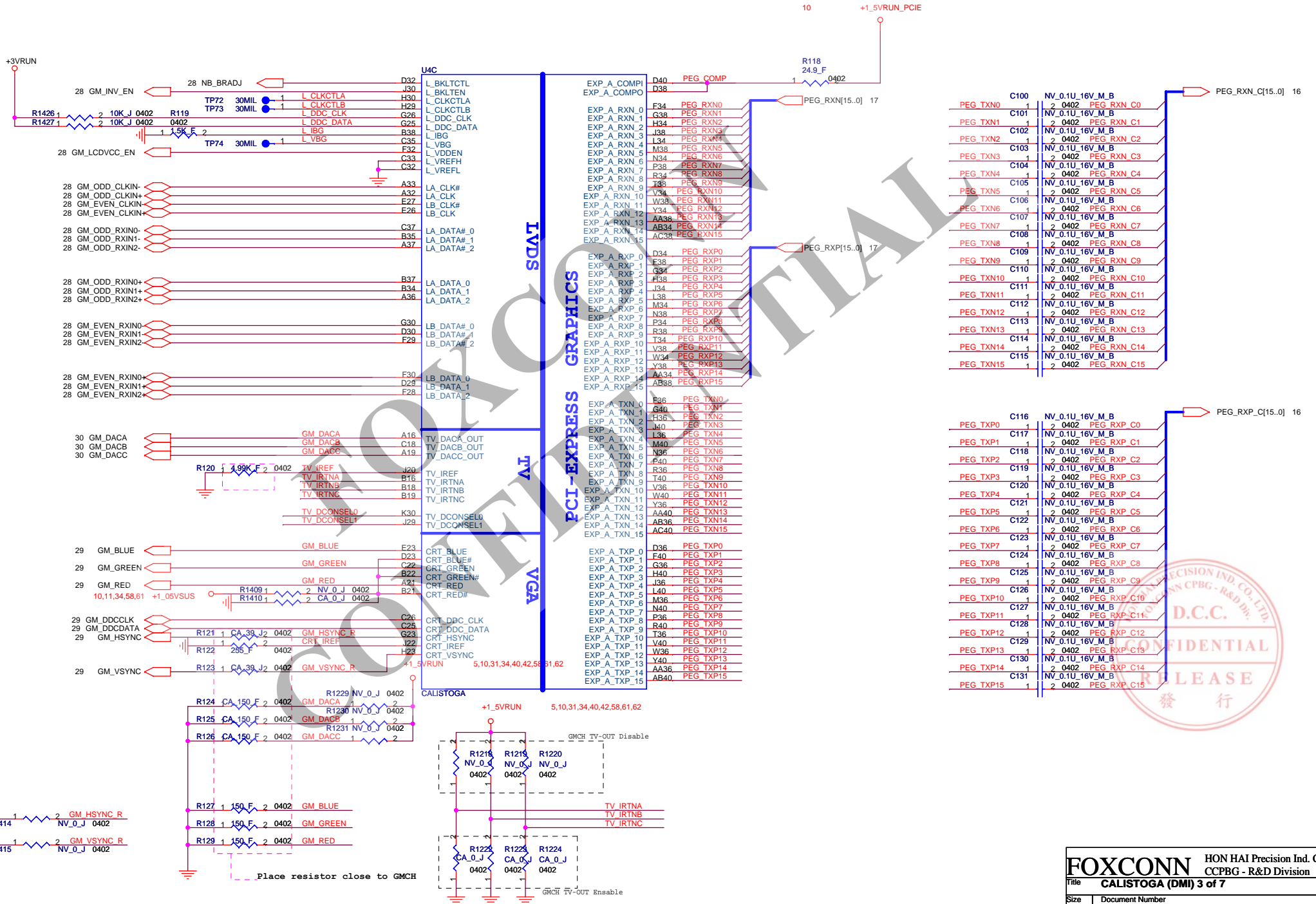




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13 M\_A\_DQ[63.0]

U4D

M A DQ0	AJ35	SA_DQ0
M A DQ1	AJ34	SA_DQ1
M A DQ2	AM31	SA_DQ2
M A DQ3	AM33	SA_DQ3
M A DQ4	AJ36	SA_DQ4
M A DQ5	AK35	SA_DQ5
M A DQ6	AJ32	SA_DQ6
M A DQ7	AK31	SA_DQ7
M A DQ8	AN35	SA_DQ8
M A DQ9	AP33	SA_DQ9
M A DQ10	AR31	SA_DQ10
M A DQ11	AP31	SA_DQ11
M A DQ12	AN38	SA_DQ12
M A DQ13	AM36	SA_DQ13
M A DQ14	AN34	SA_DQ14
M A DQ15	AN33	SA_DQ15
M A DQ16	AK26	SA_DQ16
M A DQ17	AL27	SA_DQ17
M A DQ18	AM26	SA_DQ18
M A DQ19	AN24	SA_DQ19
M A DQ20	AK28	SA_DQ20
M A DQ21	AL28	SA_DQ21
M A DQ22	AM24	SA_DQ22
M A DQ23	AP26	SA_DQ23
M A DQ24	AP23	SA_DQ24
M A DQ25	AL22	SA_DQ25
M A DQ26	AP21	SA_DQ26
M A DQ27	AV20	SA_DQ27
M A DQ28	AL23	SA_DQ28
M A DQ29	AP24	SA_DQ29
M A DQ30	AP20	SA_DQ30
M A DQ31	AT21	SA_DQ31
M A DQ32	AR12	SA_DQ32
M A DQ33	AR14	SA_DQ33
M A DQ34	AP13	SA_DQ34
M A DQ35	AP12	SA_DQ35
M A DQ36	AT13	SA_DQ36
M A DQ37	AT12	SA_DQ37
M A DQ38	AL14	SA_DQ38
M A DQ39	AL12	SA_DQ39
M A DQ40	AK9	SA_DQ40
M A DQ41	AN7	SA_DQ41
M A DQ42	AK8	SA_DQ42
M A DQ43	AK7	SA_DQ43
M A DQ44	AP9	SA_DQ44
M A DQ45	AN9	SA_DQ45
M A DQ46	AT5	SA_DQ46
M A DQ47	AL5	SA_DQ47
M A DQ48	AW2	SA_DQ48
M A DQ49	AW2	SA_DQ49
M A DQ50	AP1	SA_DQ50
M A DQ51	AN2	SA_DQ51
M A DQ52	AV2	SA_DQ52
M A DQ53	AT3	SA_DQ53
M A DQ54	AN1	SA_DQ54
M A DQ55	AL2	SA_DQ55
M A DQ56	AG7	SA_DQ56
M A DQ57	AF9	SA_DQ57
M A DQ58	AG4	SA_DQ58
M A DQ59	AF6	SA_DQ59
M A DQ60	AG9	SA_DQ60
M A DQ61	AH6	SA_DQ61
M A DQ62	AF4	SA_DQ62
M A DQ63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M A BS0 13,15
SA_BS_1	AV14	M A BS1 13,15
SA_BS_2	BA20	M A BS2 13,15
		M A CAS# 13,15
		M A DM[7.0] 13
SA_CAS#	AY13	
SA_DM_0	AJ33	M A DM0
SA_DM_1	AM35	M A DM1
SA_DM_2	AL26	M A DM2
SA_DM_3	AM22	M A DM3
SA_DM_4	AM14	M A DM4
SA_DM_5	AL9	M A DM5
SA_DM_6	AR3	M A DM6
SA_DM_7	AH4	M A DM7
SA_DQS_0	AK33	M A DQS0
SA_DQS_1	AT33	M A DQS1
SA_DQS_2	AN28	M A DQS2
SA_DQS_3	AM22	M A DQS3
SA_DQS_4	AN12	M A DQS4
SA_DQS_5	AN8	M A DQS5
SA_DQS_6	AP3	M A DQS6
SA_DQS_7	AK32	M A DQS#0
SA_DQS#_0	AU33	M A DQS#1
SA_DQS#_1	AN27	M A DQS#2
SA_DQS#_2	AM21	M A DQS#3
SA_DQS#_3	AM12	M A DQS#4
SA_DQS#_4	AL8	M A DQS#5
SA_DQS#_5	AN3	M A DQS#6
SA_DQS#_6	AH5	M A DQS#7
SA_DQS#_7		
SA_MA_0	AY16	M A A0
SA_MA_1	AU14	M A A1
SA_MA_2	AW15	M A A2
SA_MA_3	BA16	M A A3
SA_MA_4	BA17	M A A4
SA_MA_5	AU16	M A A5
SA_MA_6	AV17	M A A6
SA_MA_7	AU17	M A A7
SA_MA_8	AW17	M A A8
SA_MA_9	AT16	M A A9
SA_MA_10	AU13	M A A10
SA_MA_11	AT17	M A A11
SA_MA_12	AV20	M A A12
SA_MA_13	AV12	M A A13
SA_RAS#	AW14	M A RAS# 13,15
SA_RCVENIN#	AK23	TP MA RCVENIN# 1
SA_RCVENOUT#	AK24	TP MA RCVENOUT# 1
SA_WE#	AY14	M A WE# 13,15

CALISTOGA

14 M\_B\_DQ[63.0]

U4E

M B DQ0	AK39	SB_DQ0
M B DQ1	AJ37	SB_DQ1
M B DQ2	AP33	SB_DQ2
M B DQ3	AR41	SB_DQ3
M B DQ4	AJ38	SB_DQ4
M B DQ5	AK38	SB_DQ5
M B DQ6	AN41	SB_DQ6
M B DQ7	AP41	SB_DQ7
M B DQ8	AT40	SB_DQ8
M B DQ9	AV41	SB_DQ9
M B DQ10	AU38	SB_DQ10
M B DQ11	AV38	SB_DQ11
M B DQ12	AP38	SB_DQ12
M B DQ13	AR40	SB_DQ13
M B DQ14	AV38	SB_DQ14
M B DQ15	AV38	SB_DQ15
M B DQ16	BA38	SB_DQ16
M B DQ17	AV36	SB_DQ17
M B DQ18	AR36	SB_DQ18
M B DQ19	AP36	SB_DQ19
M B DQ20	AU38	SB_DQ20
M B DQ21	AP35	SB_DQ21
M B DQ22	AP35	SB_DQ22
M B DQ23	AP34	SB_DQ23
M B DQ24	AY33	SB_DQ24
M B DQ25	BA33	SB_DQ25
M B DQ26	AT31	SB_DQ26
M B DQ27	AU29	SB_DQ27
M B DQ28	AU31	SB_DQ28
M B DQ29	AW31	SB_DQ29
M B DQ30	AV29	SB_DQ30
M B DQ31	AW29	SB_DQ31
M B DQ32	AM19	SB_DQ32
M B DQ33	AL19	SB_DQ33
M B DQ34	AP14	SB_DQ34
M B DQ35	AN14	SB_DQ35
M B DQ36	AN17	SB_DQ36
M B DQ37	AM16	SB_DQ37
M B DQ38	AP15	SB_DQ38
M B DQ39	AL15	SB_DQ39
M B DQ40	AJ11	SB_DQ40
M B DQ41	AH10	SB_DQ41
M B DQ42	AJ9	SB_DQ42
M B DQ43	AN10	SB_DQ43
M B DQ44	AK13	SB_DQ44
M B DQ45	AH11	SB_DQ45
M B DQ46	AK10	SB_DQ46
M B DQ47	AJ8	SB_DQ47
M B DQ48	BA10	SB_DQ48
M B DQ49	AW10	SB_DQ49
M B DQ50	BA4	SB_DQ50
M B DQ51	AW4	SB_DQ51
M B DQ52	AY10	SB_DQ52
M B DQ53	AY9	SB_DQ53
M B DQ54	AW5	SB_DQ54
M B DQ55	AY5	SB_DQ55
M B DQ56	AV4	SB_DQ56
M B DQ57	AR5	SB_DQ57
M B DQ58	AK4	SB_DQ58
M B DQ59	AK3	SB_DQ59
M B DQ60	AT4	SB_DQ60
M B DQ61	AK5	SB_DQ61
M B DQ62	AJ5	SB_DQ62
M B DQ63	AJ3	SB_DQ63

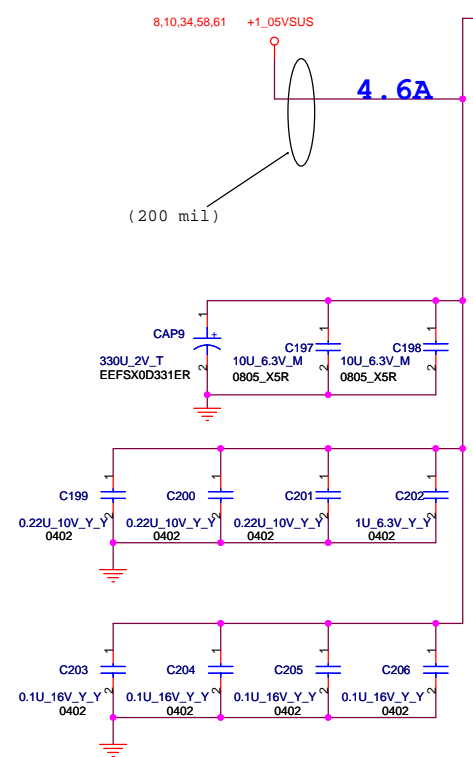
DDR SYSTEM MEMORY B

SB_DQ0	AT24	M B BS0 14,15
SB_DQ1	AV23	M B BS1 14,15
SB_DQ2	AY28	M B BS2 14,15
SB_DQ3		M B CAS# 14,15
SB_DQ4		M B DM[7.0] 14
SB_CAS#	AR24	M B DM0
SB_DM_0	AK36	M B DM1
SB_DM_1	AR38	M B DM2
SB_DM_2	AT36	M B DM3
SB_DM_3	BA31	M B DM4
SB_DM_4	AL17	M B DM5
SB_DM_5	AH8	M B DM6
SB_DM_6	BA5	M B DM7
SB_DM_7	AN4	M B DM7
SB_DQS_0	AM39	M B DQS0
SB_DQS_1	AT39	M B DQS1
SB_DQS_2	AU35	M B DQS2
SB_DQS_3	AR29	M B DQS3
SB_DQS_4	AR16	M B DQS4
SB_DQS_5	AR10	M B DQS5
SB_DQS_6	AR7	M B DQS6
SB_DQS_7	AN5	M B DQS7
SB_DQS#_0	AM40	M B DQS#0
SB_DQS#_1	AU39	M B DQS#1
SB_DQS#_2	AT35	M B DQS#2
SB_DQS#_3	AP29	M B DQS#3
SB_DQS#_4	AP16	M B DQS#4
SB_DQS#_5	AT10	M B DQS#5
SB_DQS#_6	AT7	M B DQS#6
SB_DQS#_7	AP5	M B DQS#7
SB_MA_0	AY23	M B A0
SB_MA_1	AW24	M B A1
SB_MA_2	AY24	M B A2
SB_MA_3	AR28	M B A3
SB_MA_4	AT27	M B A4
SB_MA_5	AU28	M B A5
SB_MA_6	AU27	M B A6
SB_MA_7	AV28	M B A7
SB_MA_8	AV27	M B A8
SB_MA_9	AW27	M B A9
SB_MA_10	AV24	M B A10
SB_MA_11	BA27	M B A11
SB_MA_12	AY27	M B A12
SB_MA_13	AR23	M B A13
SB_RAS#	AU23	M B RAS# 14,15
SB_RCVENIN#	AK16	TP MB RCVENIN# 1
SB_RCVENOUT#	AK18	TP MB RCVENOUT# 1
SB_WE#	AR27	M B WE# 14,15

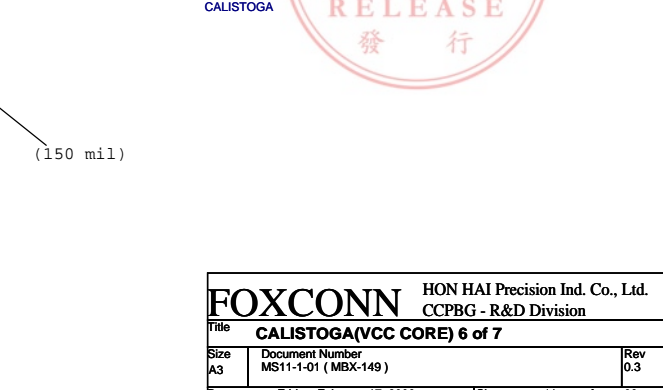
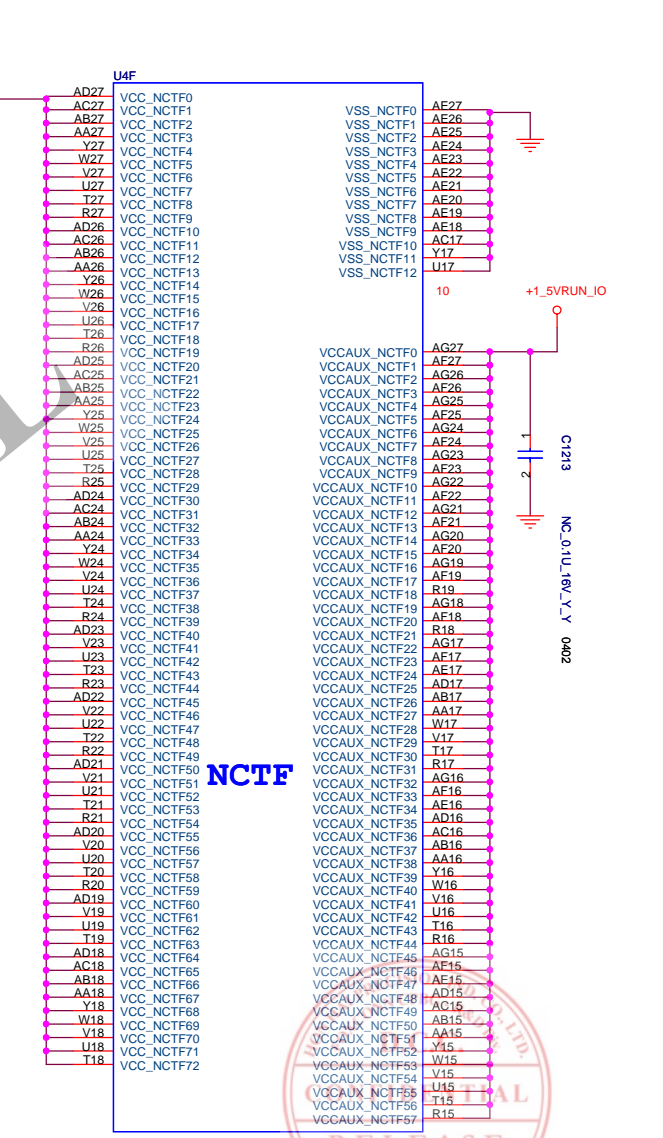
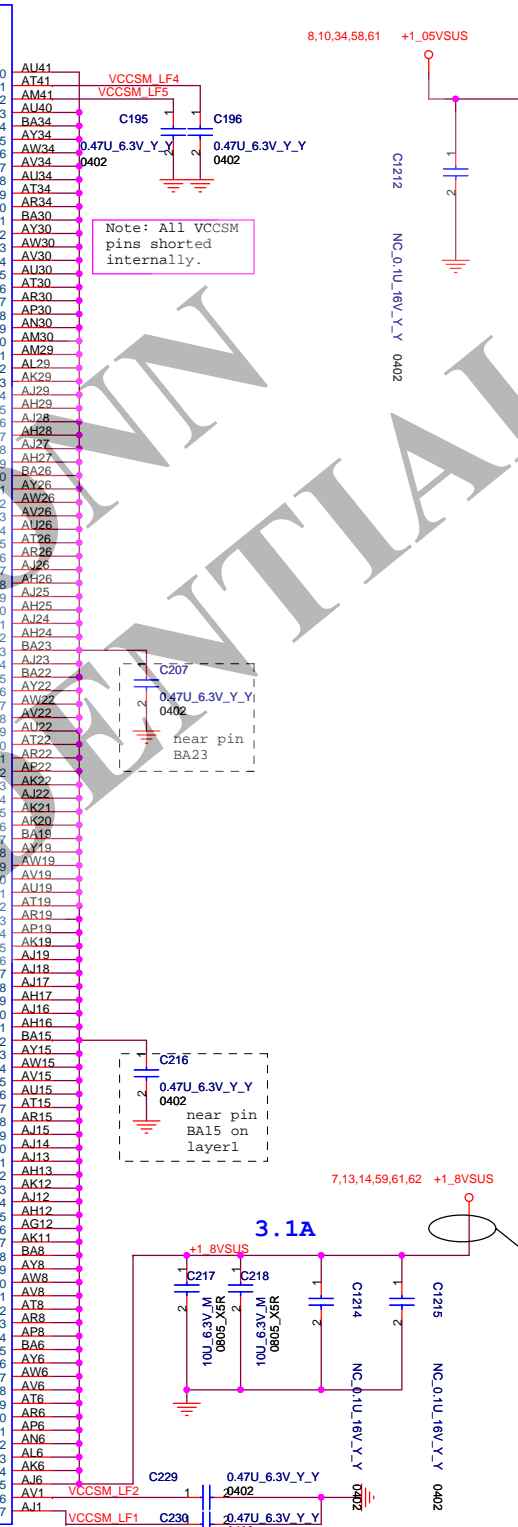
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Pin	Label
VCC_0	AA33
VCC_1	W33
VCC_2	P33
VCC_3	L33
VCC_4	J33
VCC_5	AA32
VCC_6	Y32
VCC_7	W32
VCC_8	V32
VCC_9	P32
VCC_10	N32
VCC_11	M32
VCC_12	L32
VCC_13	J32
VCC_14	AA31
VCC_15	W31
VCC_16	V31
VCC_17	T31
VCC_18	R31
VCC_19	P31
VCC_20	N31
VCC_21	M31
VCC_22	W30
VCC_23	Y30
VCC_24	T30
VCC_25	R30
VCC_26	P30
VCC_27	N30
VCC_28	M30
VCC_29	L30
VCC_30	J30
VCC_31	AA29
VCC_32	W29
VCC_33	Y29
VCC_34	T29
VCC_35	R29
VCC_36	P29
VCC_37	N29
VCC_38	M29
VCC_39	L29
VCC_40	J29
VCC_41	AA28
VCC_42	W28
VCC_43	Y28
VCC_44	T28
VCC_45	R28
VCC_46	P28
VCC_47	N28
VCC_48	M28
VCC_49	L28
VCC_50	J28
VCC_51	AA27
VCC_52	W27
VCC_53	Y27
VCC_54	T27
VCC_55	R27
VCC_56	P27
VCC_57	N27
VCC_58	M27
VCC_59	L27
VCC_60	J27
VCC_61	AA26
VCC_62	W26
VCC_63	Y26
VCC_64	T26
VCC_65	R26
VCC_66	P26
VCC_67	N26
VCC_68	M26
VCC_69	L26
VCC_70	J26
VCC_71	AA25
VCC_72	W25
VCC_73	Y25
VCC_74	T25
VCC_75	R25
VCC_76	P25
VCC_77	N25
VCC_78	M25
VCC_79	L25
VCC_80	J25
VCC_81	AA24
VCC_82	W24
VCC_83	Y24
VCC_84	T24
VCC_85	R24
VCC_86	P24
VCC_87	N24
VCC_88	M24
VCC_89	L24
VCC_90	J24
VCC_91	AA23
VCC_92	W23
VCC_93	Y23
VCC_94	T23
VCC_95	R23
VCC_96	P23
VCC_97	N23
VCC_98	M23
VCC_99	L23
VCC_100	J23
VCC_101	AA22
VCC_102	W22
VCC_103	Y22
VCC_104	T22
VCC_105	R22
VCC_106	P22
VCC_107	N22
VCC_108	M22
VCC_109	L22
VCC_110	J22



7 MCH\_CFG\_5 ← 1 ● 30MIL TP554

MCH\_CFG\_5  
Low = DMIX2  
High = DMIX4

7 MCH\_CFG\_6 ← 1 ● 30MIL TP556

MCH\_CFG\_6  
Low = Moby Dick  
High = Calistoga  
DDR2 select (default high)

7 MCH\_CFG\_7 ← 1 ● 30MIL TP557

MCH\_CFG\_7 (CPU Strap)  
Low = RSVD  
High = Mobile Yonah processor

7 MCH\_CFG\_9 ← 1 ● 30MIL TP559

MCH\_CFG\_9 (PCIe Graphics Lane)  
Low = Reverse Lane operation  
High = Normal operation

For layout convenience

7 MCH\_CFG\_10 ← 1 ● 30MIL TP560

MCH\_CFG\_10 (HOST PLL VCC SELECT)  
Low = RESERVED  
High = MOBILITY

7 MCH\_CFG\_11 ← 1 ● 30MIL TP561

MCH\_CFG\_11 (PSB 4x CLK ENABLE)  
Low = Calistoga  
High = Reserved



7 MCH\_CFG\_12 ← 1 ● 30MIL TP562

7 MCH\_CFG\_13 ← 1 ● 30MIL TP563

MCH\_CFG [13:12] (XOR/ALLZ)  
00=Partial Clock Gating Disable  
01=XOR Mode Enable  
10=All-Z Mode Enable  
11=Normal Operation(Default)

7 MCH\_CFG\_16 ← 1 ● 30MIL TP566

MCH\_CFG\_16 (FSB Dynamic ODT)  
Low = Dynamic ODT Disabled  
High = Dynamic ODT Enable

MCH\_CFG\_18  
Low = 1.05V(default)  
High = 1.5V

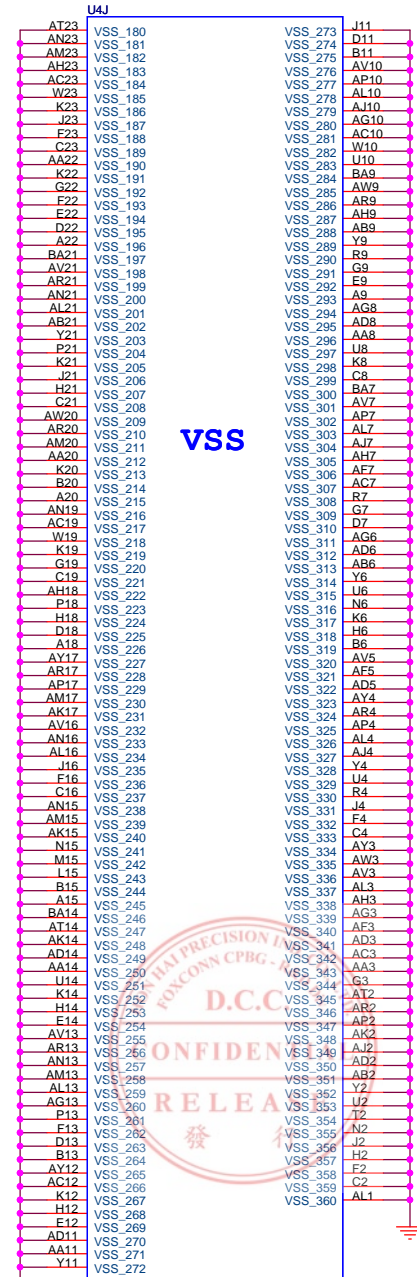
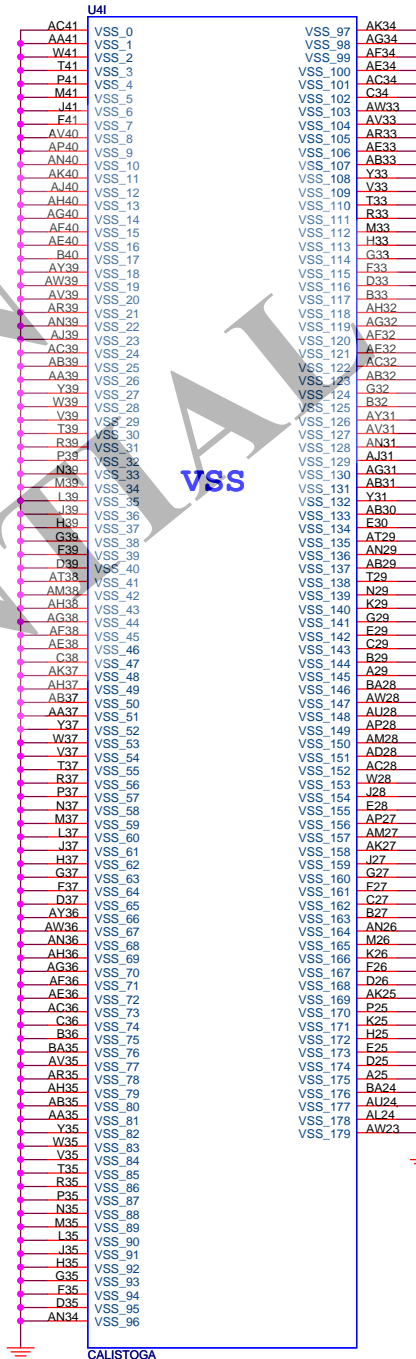
7 MCH\_CFG\_18 ← 1 ● 30MIL TP555

MCH\_CFG\_19 (DMI LANE REVERSAL)  
Low = Normal(default)  
High = LANES REVERSED

7 MCH\_CFG\_19 ← 1 ● 30MIL TP558

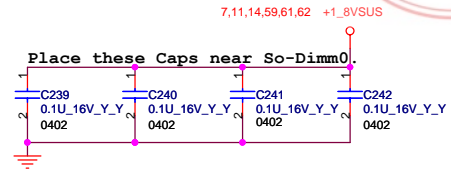
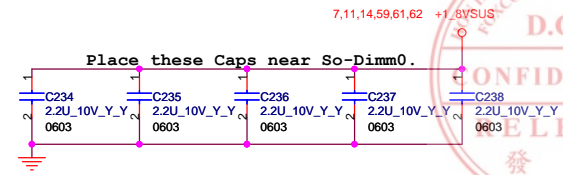
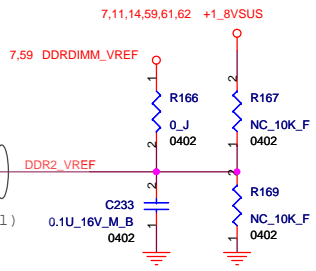
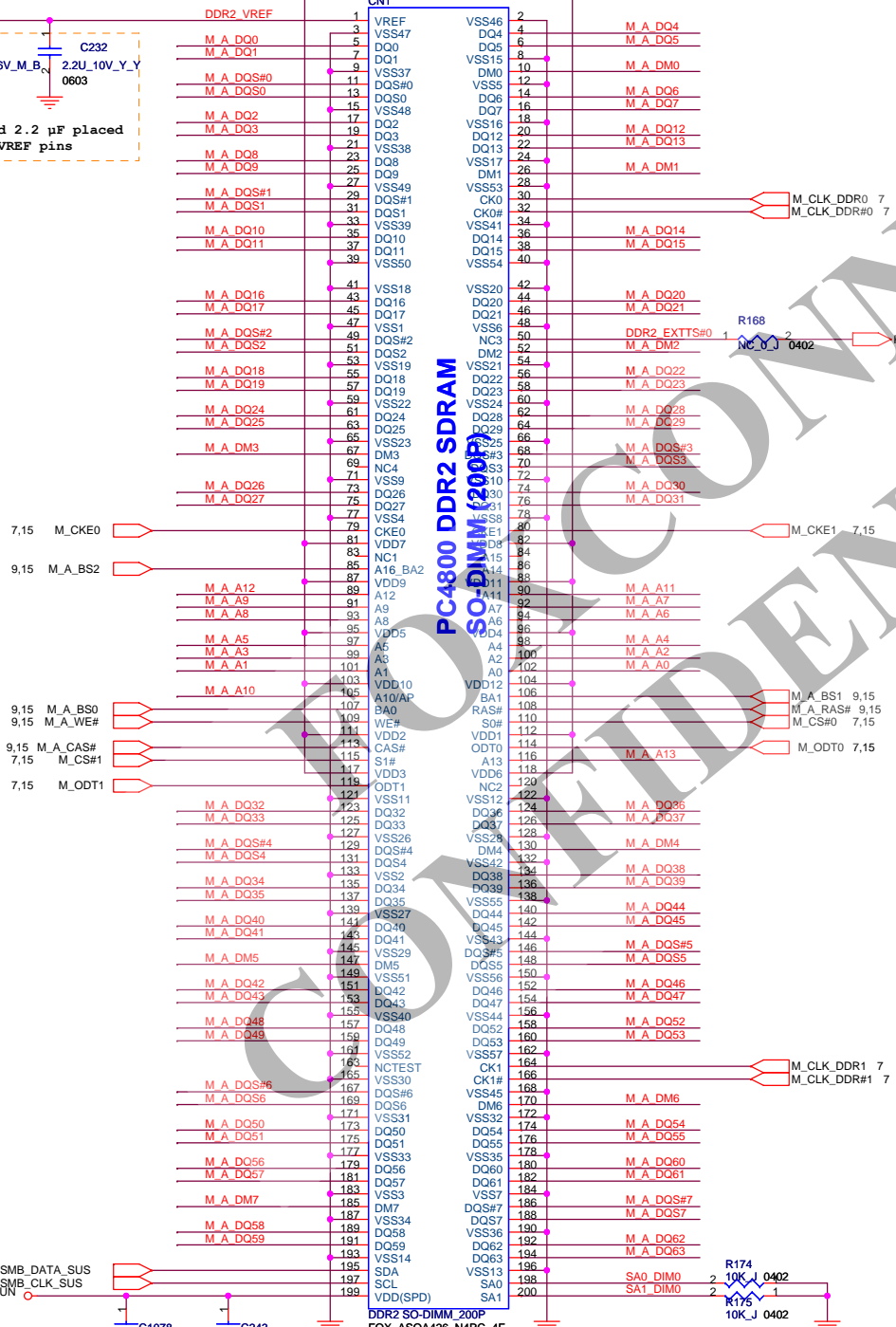
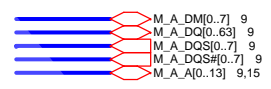
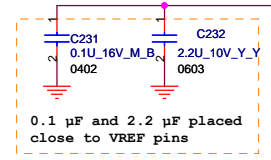
MCH\_CFG\_20  
Low = Only SDVO or PCIe x1 is operational (defaults)  
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

Layout Noe:  
Location of all MCH\_CFG strap resistors needs to be close to trace to minimize stub



7,11,14,59,61,62 +1\_8VSUS +1\_8VSUS 7,11,14,59,61,62

1.8V per DIMM=3.08A



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CCPBG - R&D Division

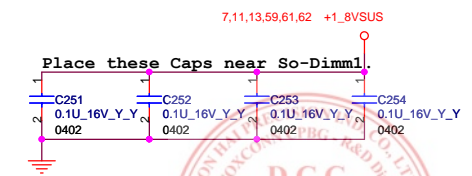
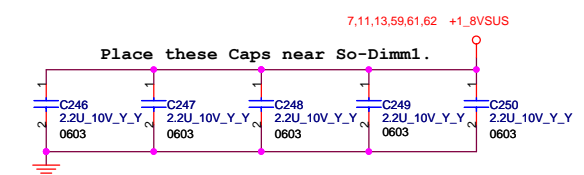
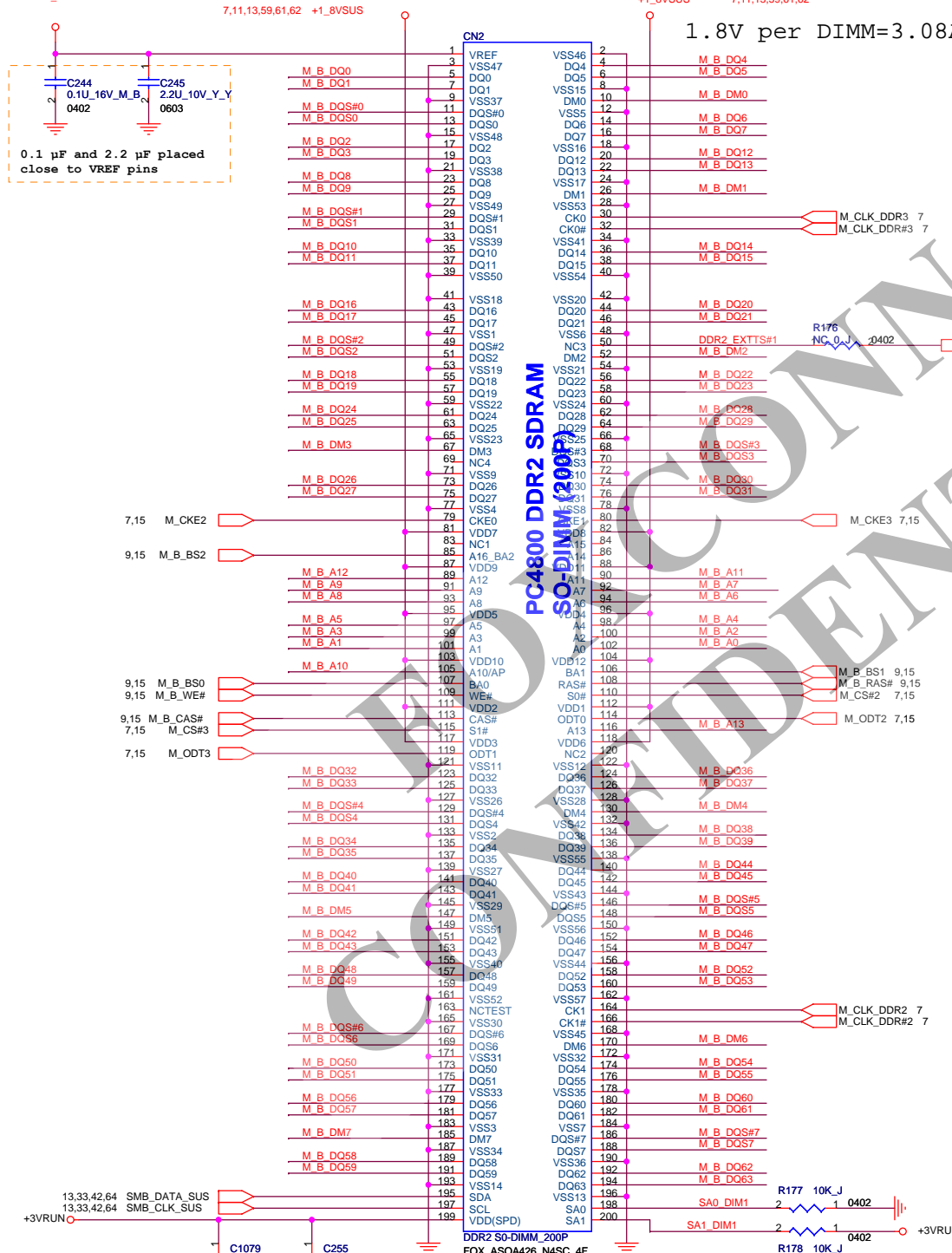
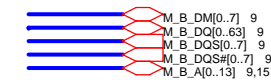
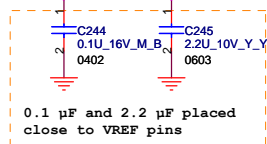
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Size: A3	Document Number: MS11-1-01 (MBX-149)	Rev: 0.3
Date: Friday, February 17, 2006	Sheet: 13	of: 66

PC4800 DDR2 SDRAM SO-DIMM(200P)

SMBus Address: A0 (W) / A1 (R)

Place DIMM\_0 near GMCH

1.8V per DIMM=3.08A



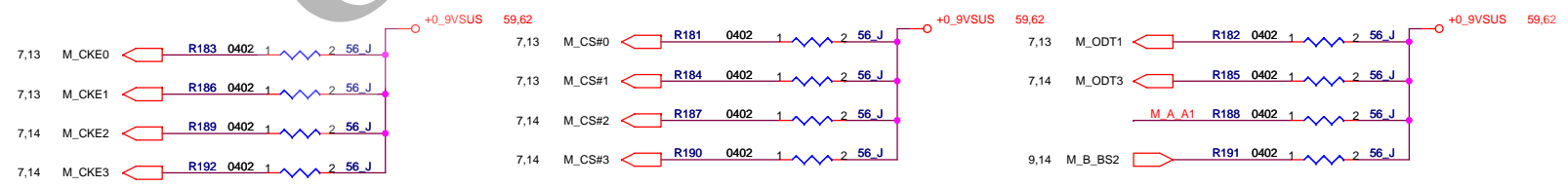
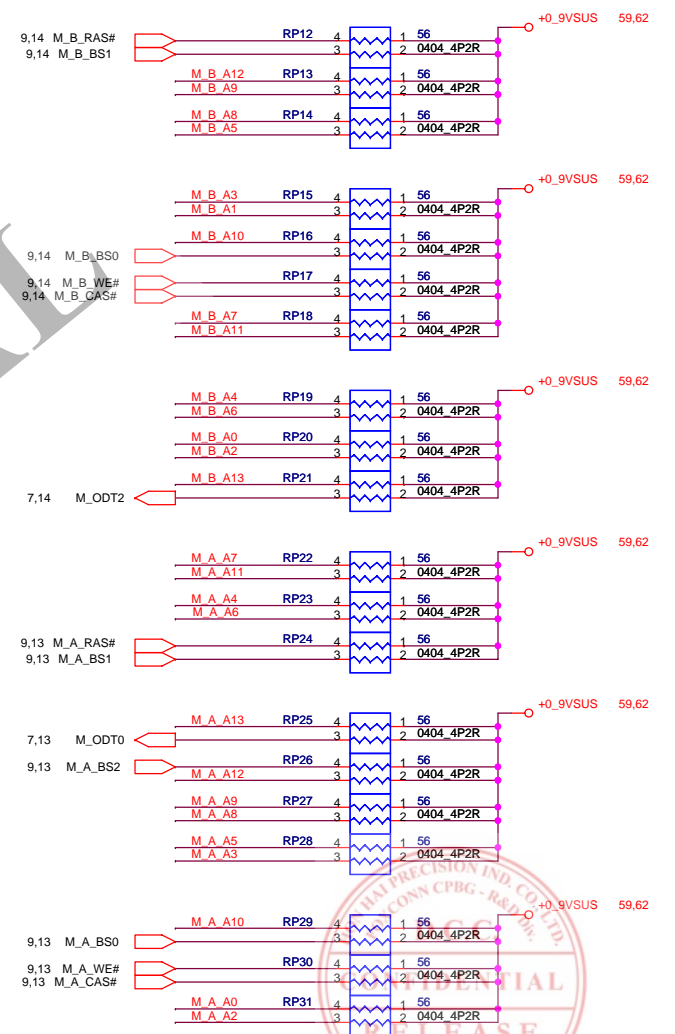
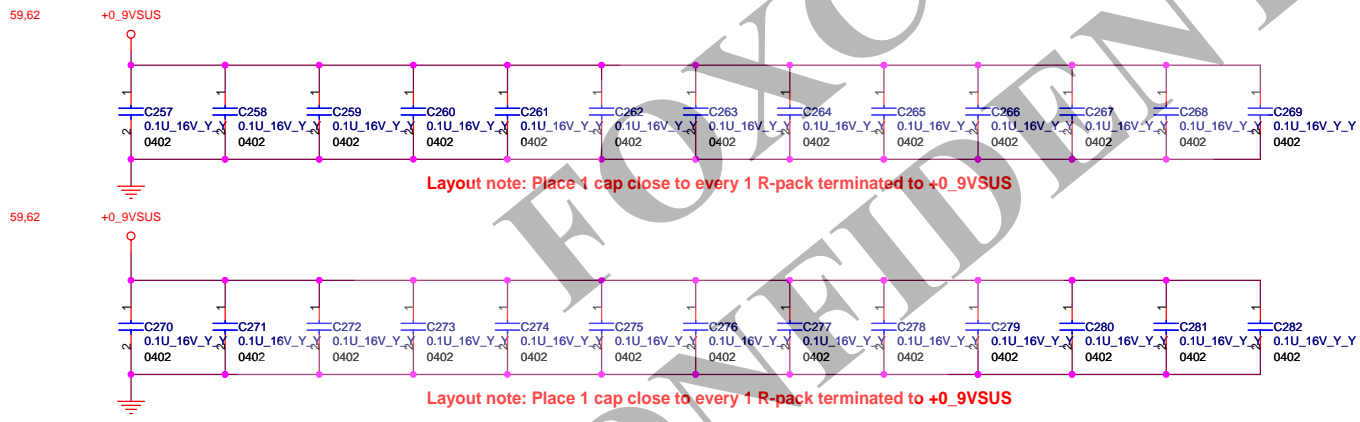
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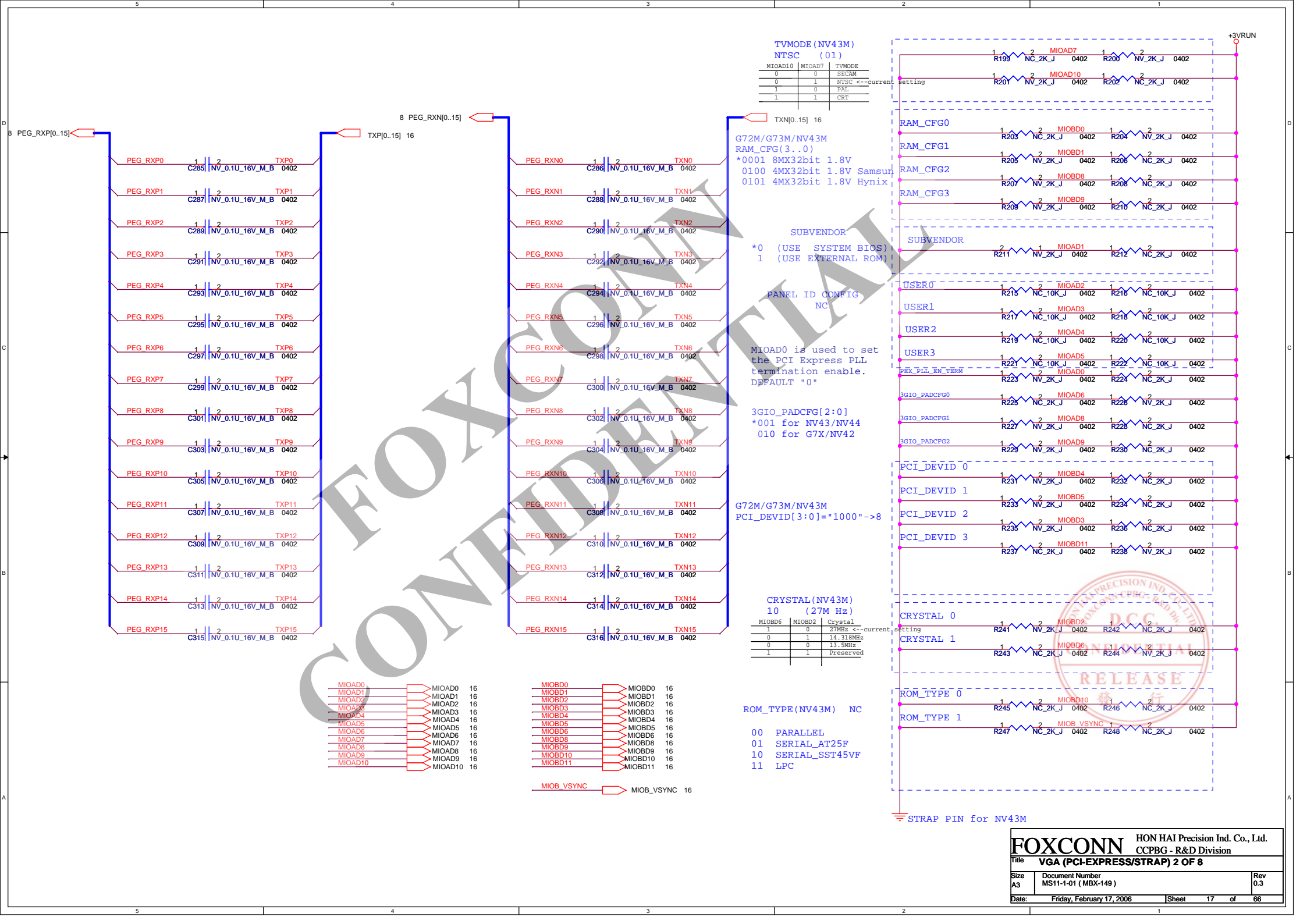
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<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
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Size: A3	MS11-1-01 (MBX-149)	Rev: 0.3	
Date: Friday, February 17, 2006	Sheet: 14	of: 66	









TVMODE(NV43M)  
NTSC (01)

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC ---current setting
1	0	PAL
1	1	CRT

G72M/G73M/NV43M  
RAM\_CFG(3..0)  
\*0001 8MX32bit 1.8V  
0100 4MX32bit 1.8V Samsung  
0101 4MX32bit 1.8V Hynix

SUBVENDOR  
\*0 (USE SYSTEM BIOS)  
1 (USE EXTERNAL ROM)

PANEL ID CONFIG  
NC

MIOAD0 is used to set  
the PCI Express PLL  
termination enable.  
DEFAULT "0"

3GIO\_PADCFG[2:0]  
\*001 for NV43/NV44  
010 for G7X/NV42

G72M/G73M/NV43M  
PCI\_DEVID[3:0]="1000"-->8

CRYSTAL(NV43M)  
10 (27M Hz)

MIOBD6	MIOBD2	Crystal
1	0	27MHz ---current setting
0	1	14.318MHz
0	0	13.5MHz
1	1	Reserved

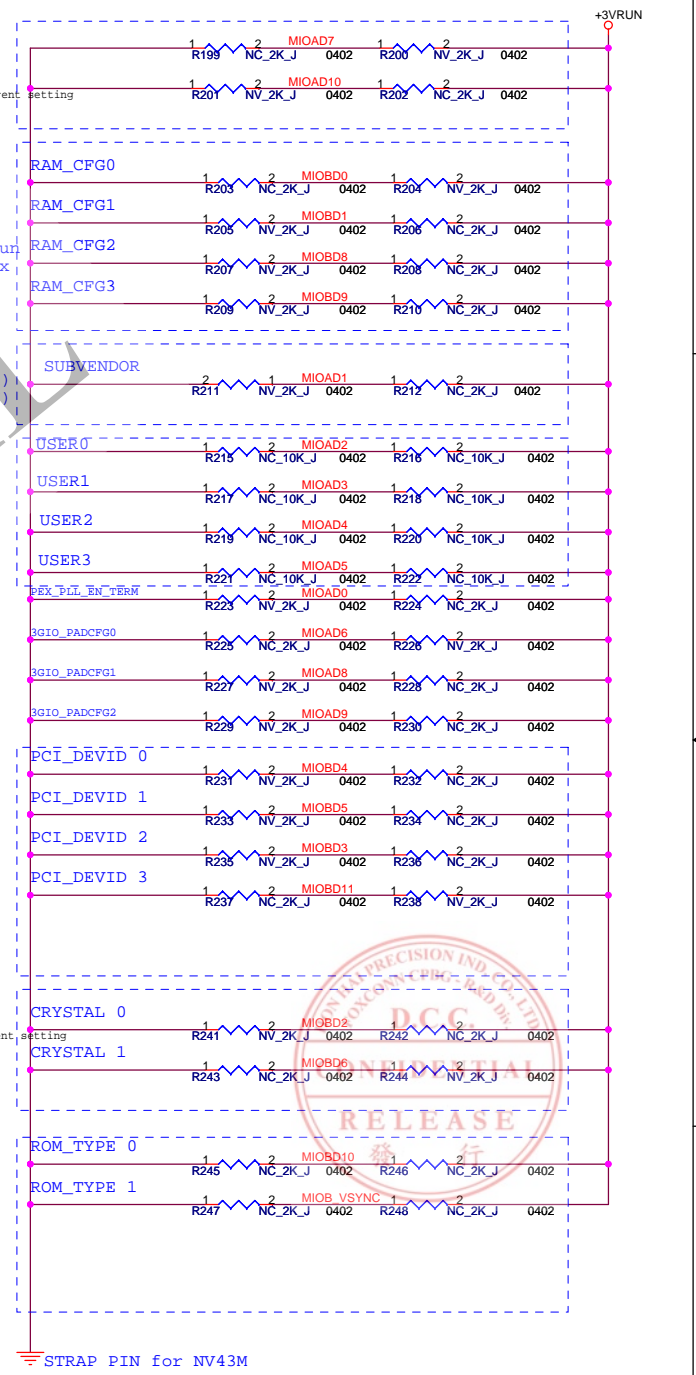
ROM\_TYPE(NV43M) NC

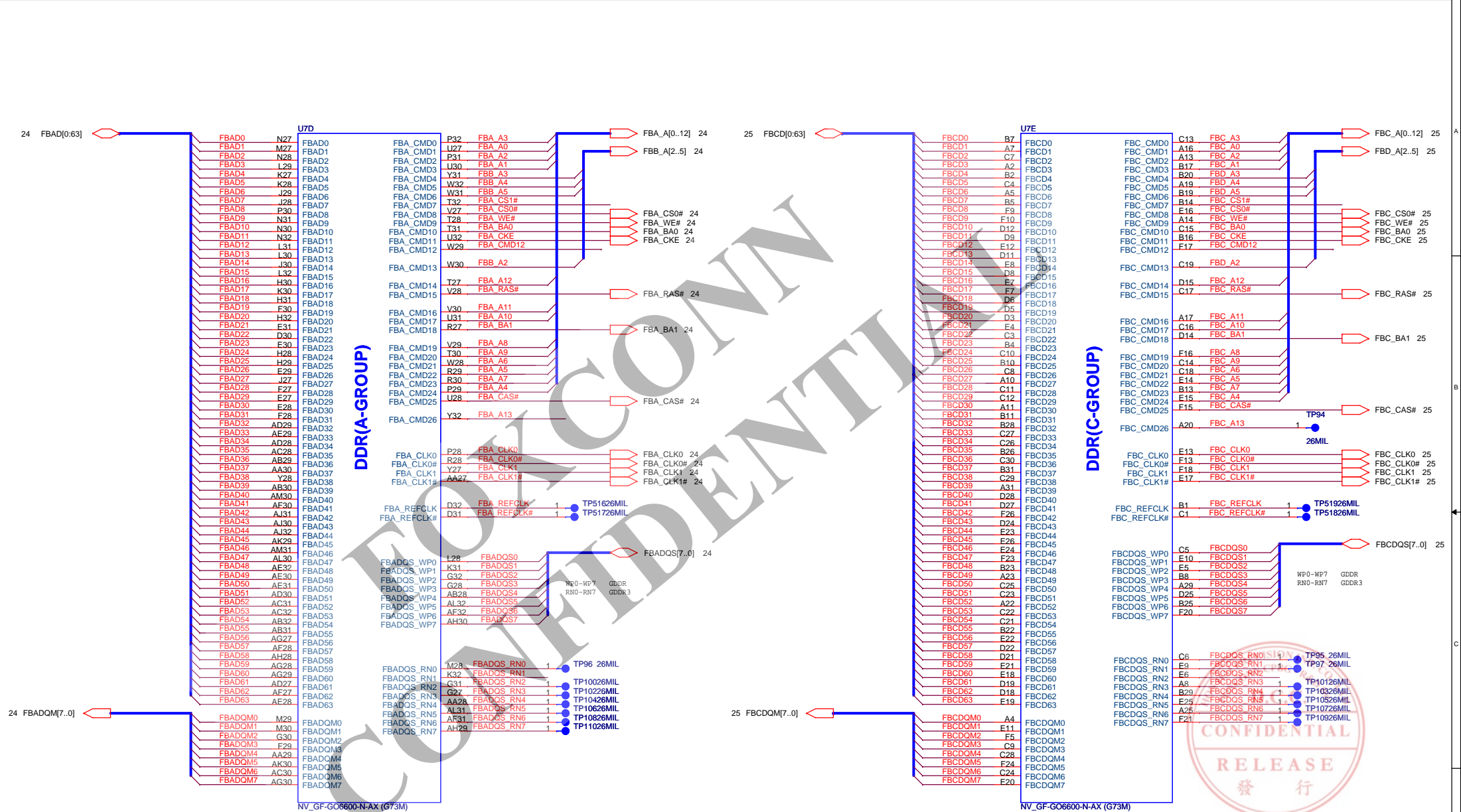
00 PARALLEL  
01 SERIAL\_AT25F  
10 SERIAL\_SST45VF  
11 LPC

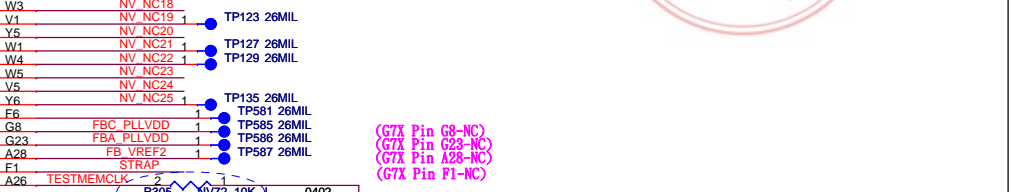
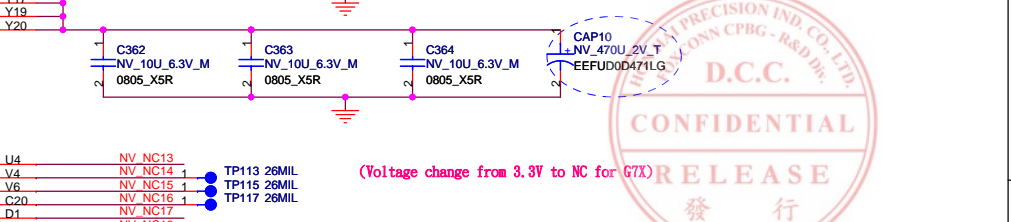
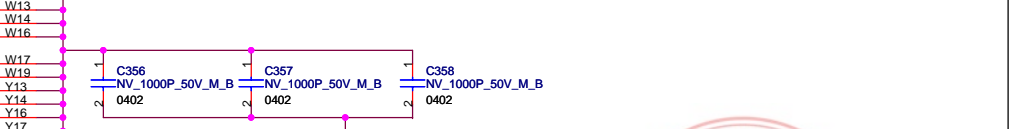
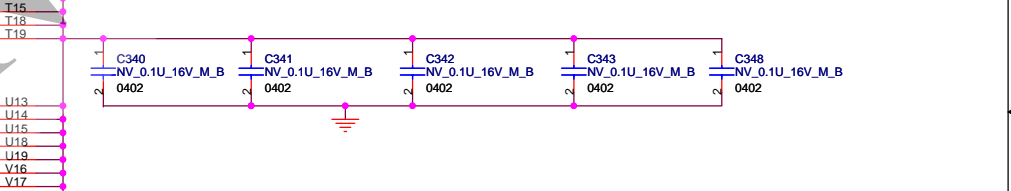
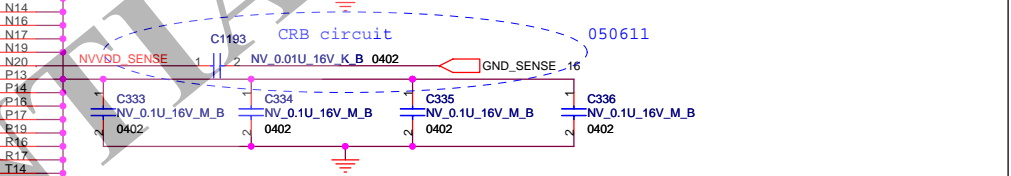
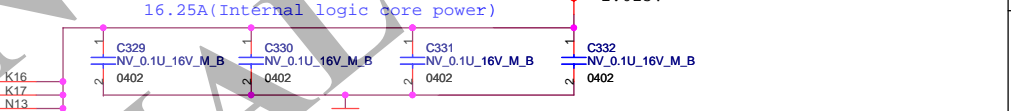
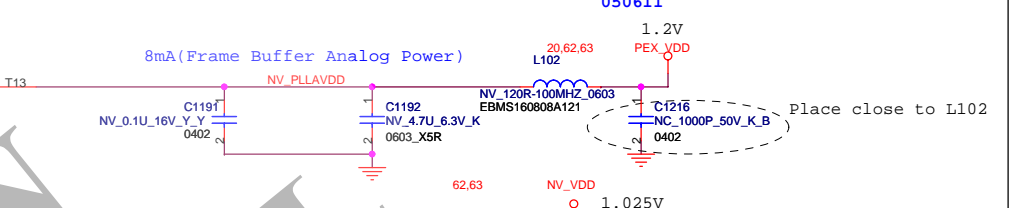
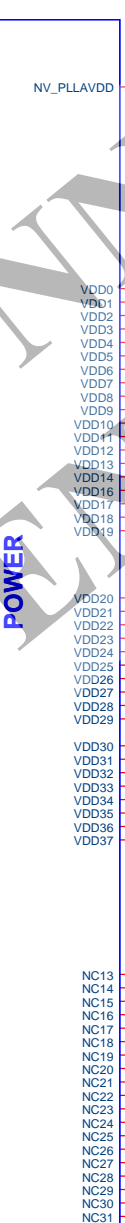
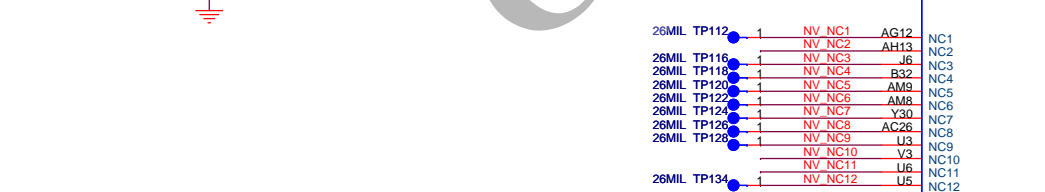
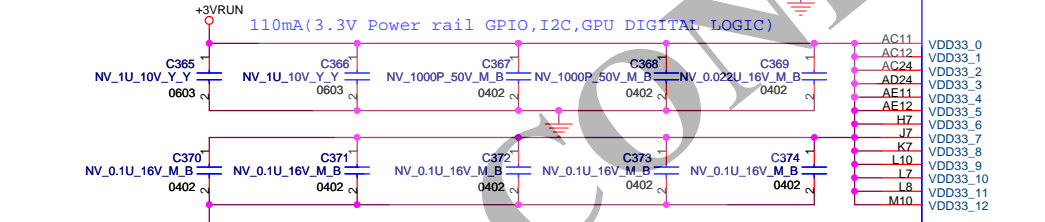
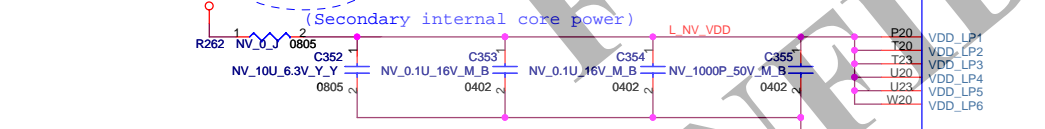
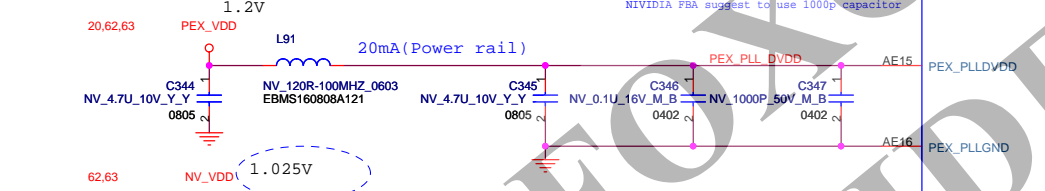
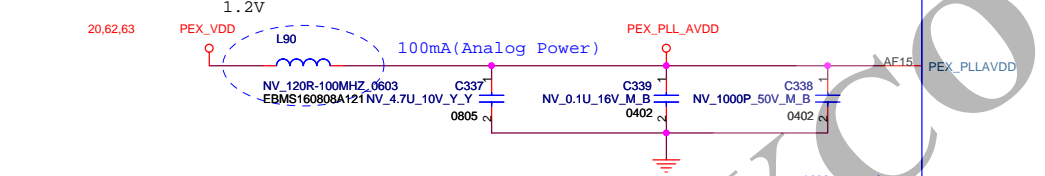
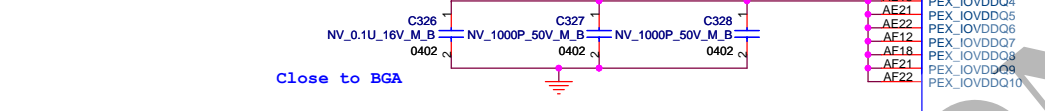
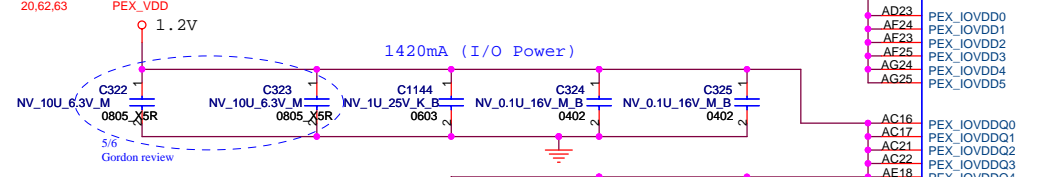
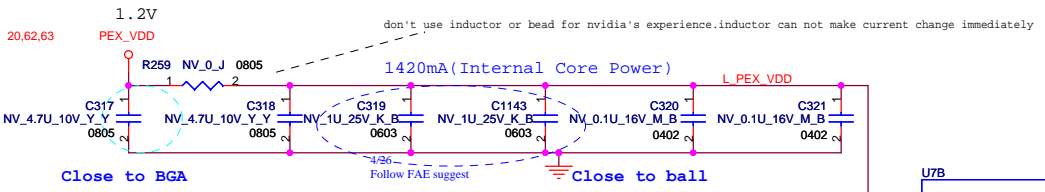
- MIOAD0
- MIOAD1
- MIOAD2
- MIOAD3
- MIOAD4
- MIOAD5
- MIOAD6
- MIOAD7
- MIOAD8
- MIOAD9
- MIOAD10

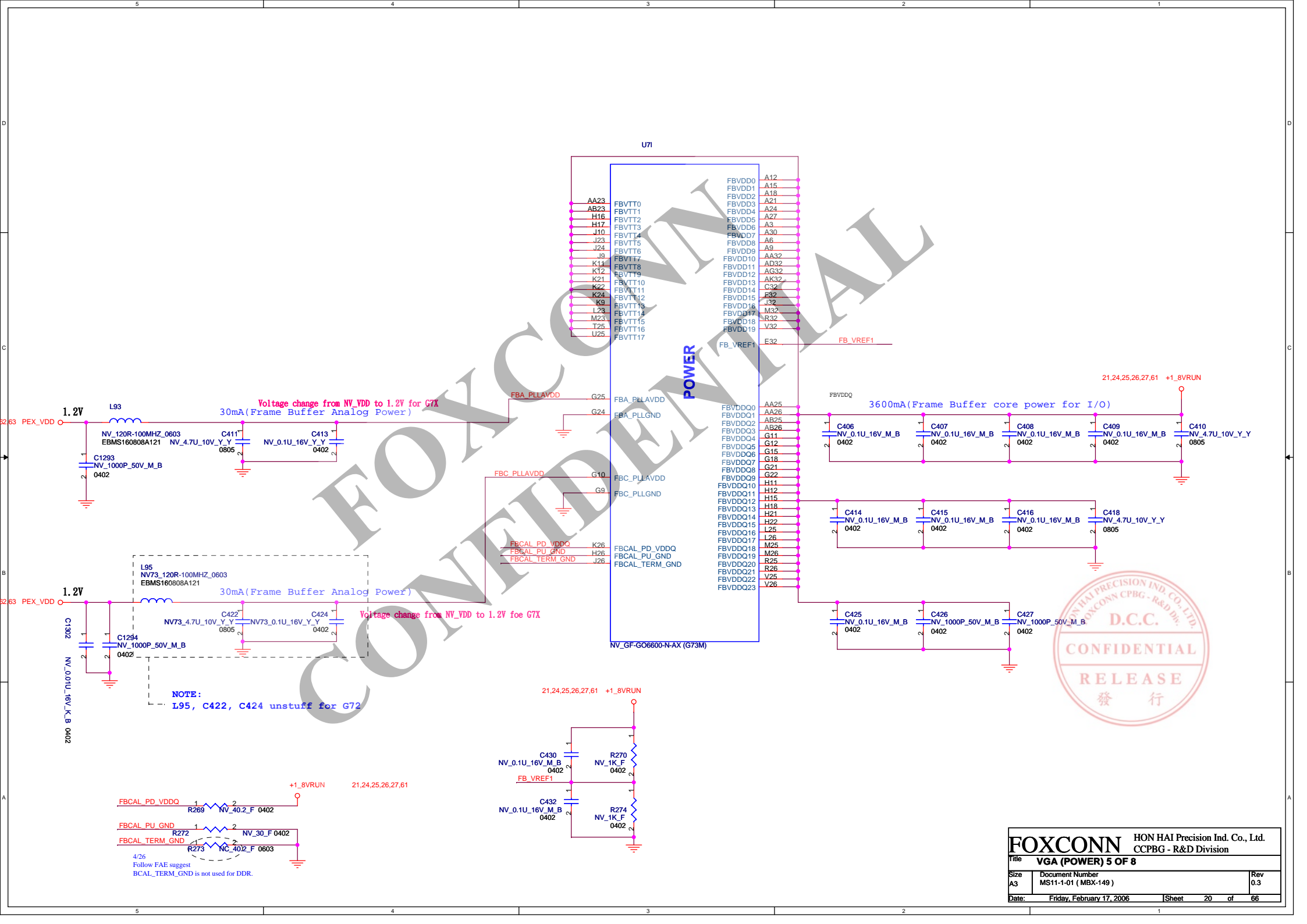
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- MIOBD1
- MIOBD2
- MIOBD3
- MIOBD4
- MIOBD5
- MIOBD6
- MIOBD8
- MIOBD9
- MIOBD10
- MIOBD11

MIOB\_VSYNC MIOB\_VSYNC 16









Voltage change from NV\_VDD to 1.2V for G7X  
30mA(Frame Buffer Analog Power)

Voltage change from NV\_VDD to 1.2V for G7X  
30mA(Frame Buffer Analog Power)

NOTE:  
L95, C422, C424 unstuff for G72

+1.8V\_RUN 21,24,25,26,27,61

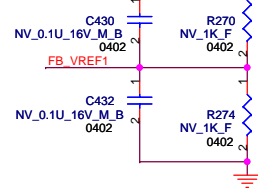
FBCAL\_PD\_VDDQ R269 NV\_40.2\_F 0402

FBCAL\_PU\_GND R272 NV\_30\_F 0402

FBCAL\_TERM\_GND R273 NC\_40.2\_F 0603

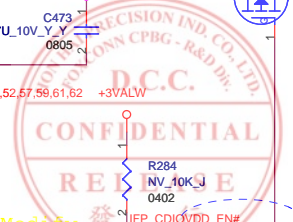
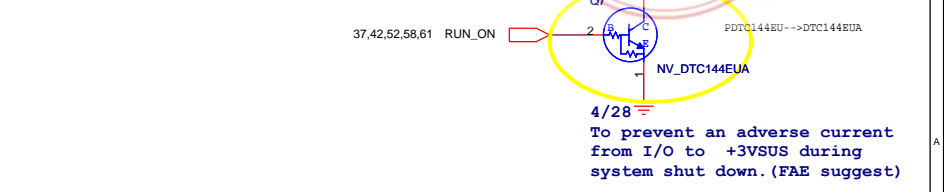
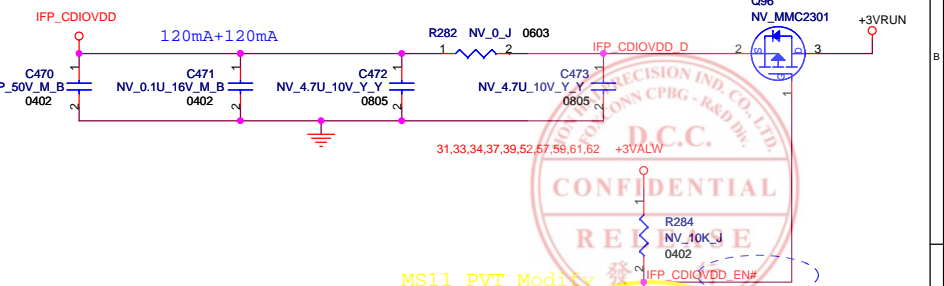
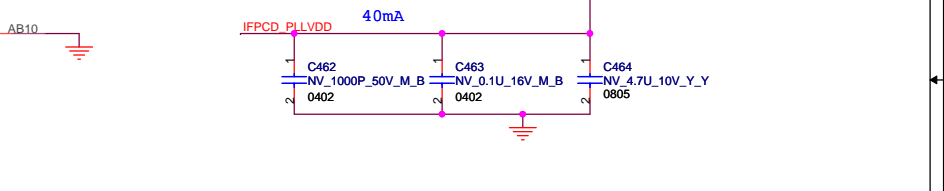
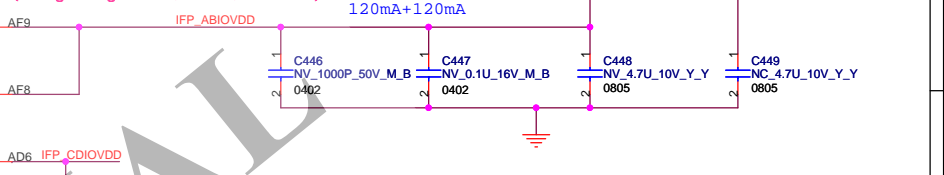
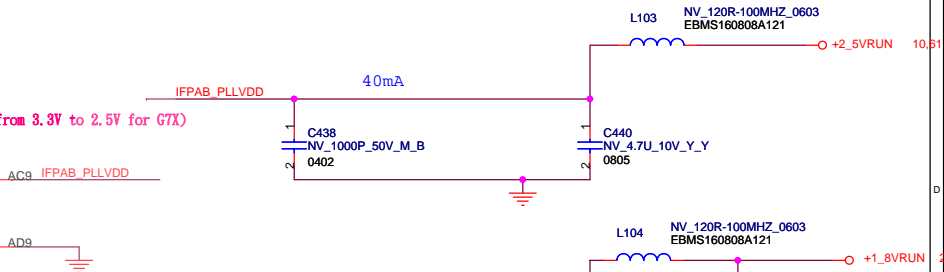
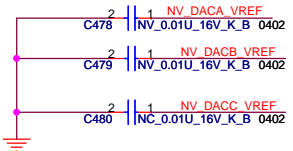
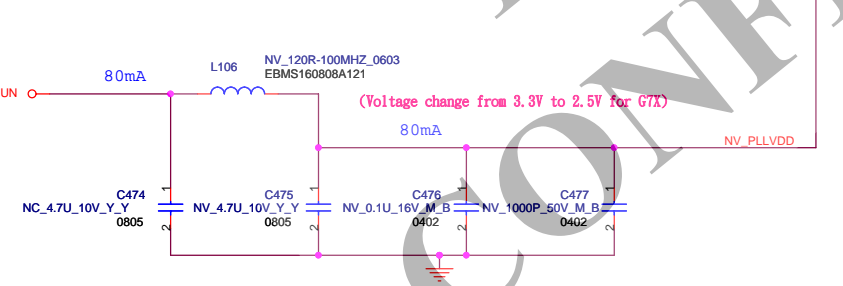
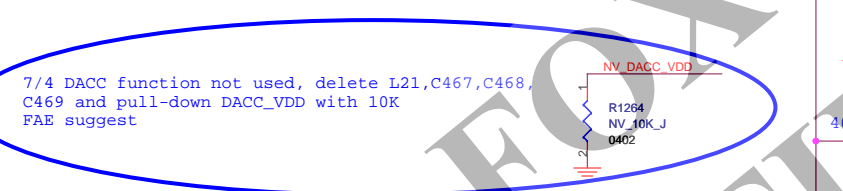
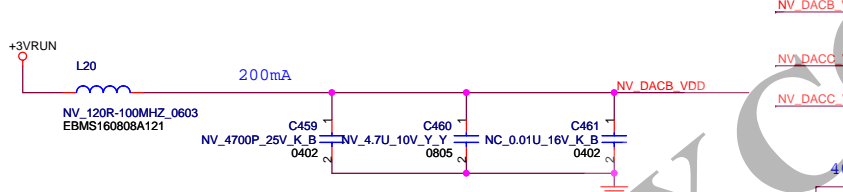
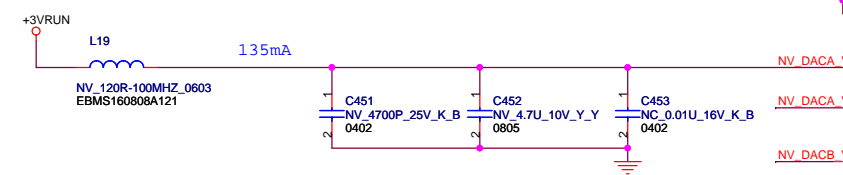
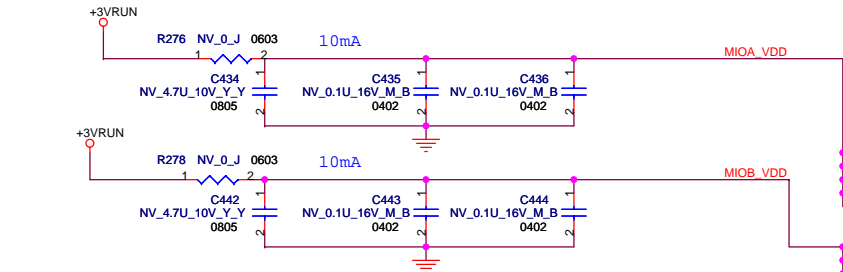
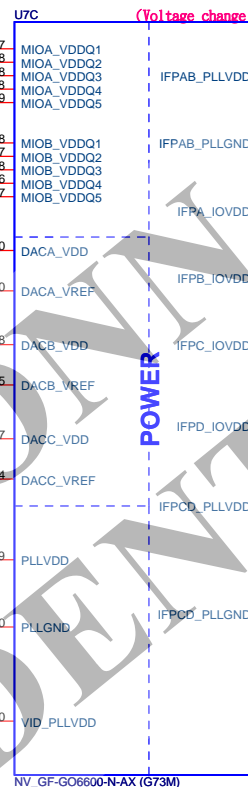
4/26  
Follow FAE suggest  
BCAL\_TERM\_GND is not used for DDR.

21,24,25,26,27,61 +1.8V\_RUN



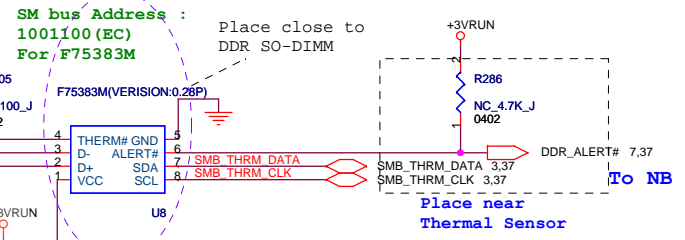
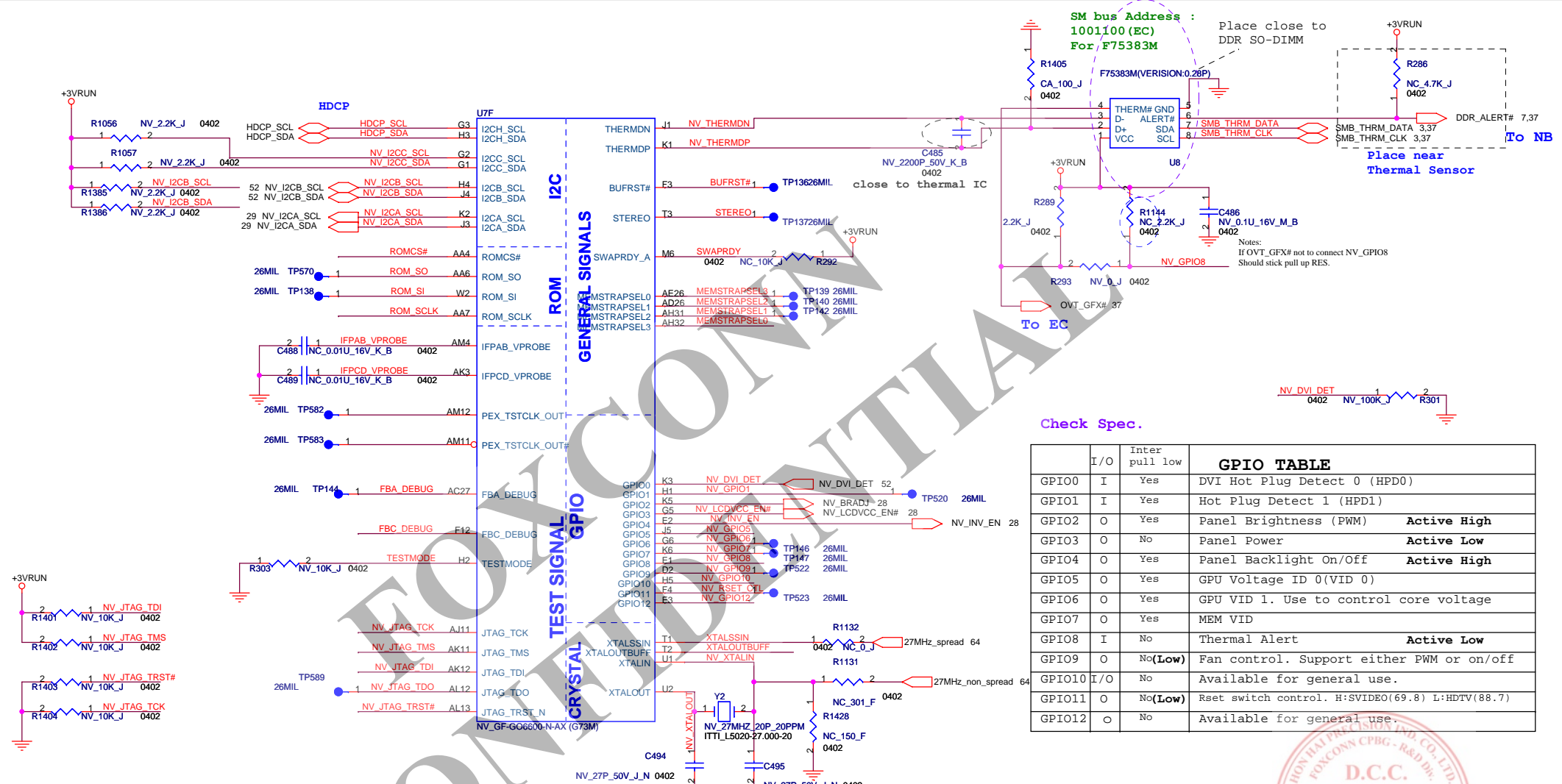
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>VGA (POWER) 5 OF 8</b>		
Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.3
Date: Friday, February 17, 2006	Sheet 20	of 66

7/4 DAC function not used, delete L21, C467, C468, C469 and pull-down DACC\_VDD with 10K FAE suggest



To prevent an adverse current from I/O to +3VSUS during system shut down. (FAE suggest)

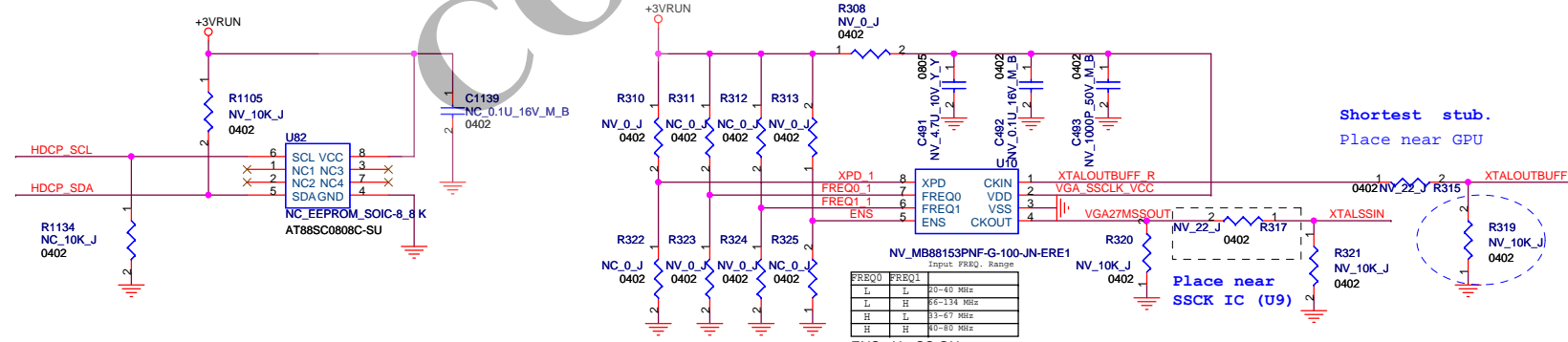
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>VGA (POWER) 6 OF 8</b>		
Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.4
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Check Spec.

I/O	Inter pull low	GPIO TABLE	
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) <b>Active High</b>
GPIO3	O	No	Panel Power <b>Active Low</b>
GPIO4	O	Yes	Panel Backlight On/Off <b>Active High</b>
GPIO5	O	Yes	GPU Voltage ID 0(VID 0)
GPIO6	O	Yes	GPU VID 1. Use to control core voltage
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert <b>Active Low</b>
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Rset switch control. H:SVIDE0(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

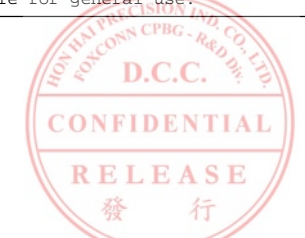
HDCP ROM



NV\_MB88153PNF-G-100-JN-ERE1

FREQ0	FREQ1	Input FREQ. Range
L	L	30-40 MHz
L	H	60-134 MHz
H	L	63-67 MHz
H	H	80-80 MHz

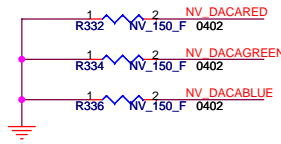
ENS : H->SS ON  
L->SS OFF  
XPD : H->Normal  
L->Power Down



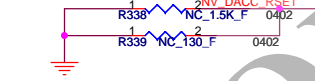
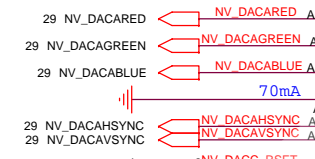
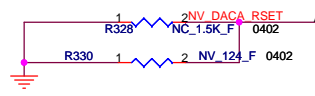
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **VGA (POWER) 7 OF 8**

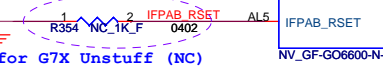
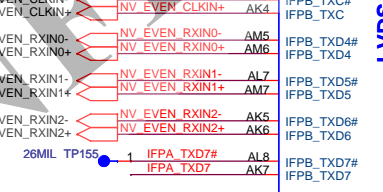
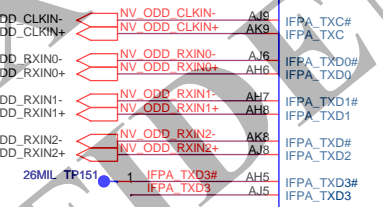
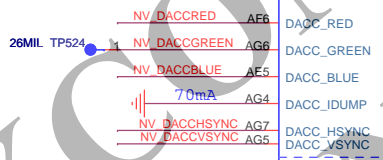
Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.3
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CLOSE TO GPU



CLOSE TO GPU



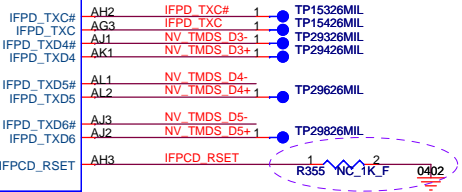
for G7X Unstuff (NC)

Place close to chipset

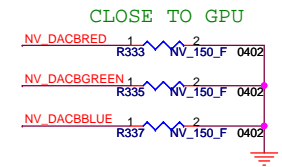
VIDEO DAC

LVDS

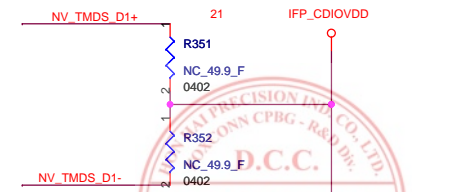
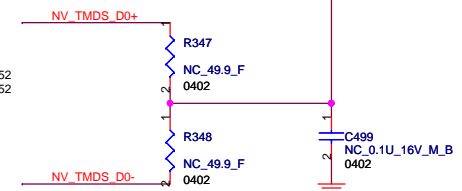
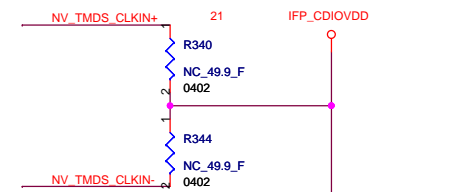
TMDS



for G7X Unstuff (NC)



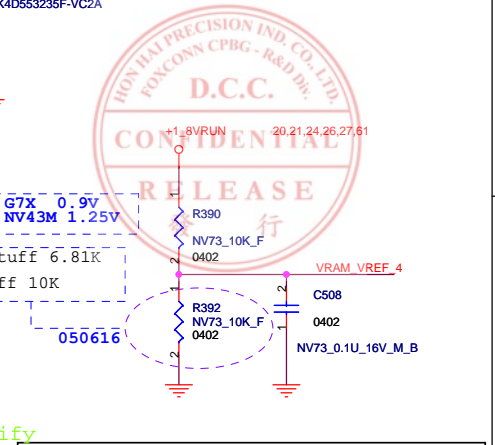
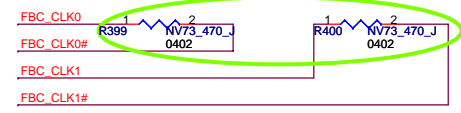
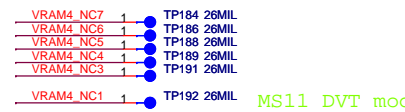
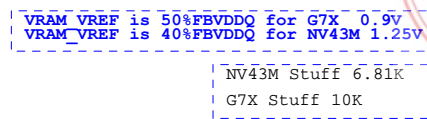
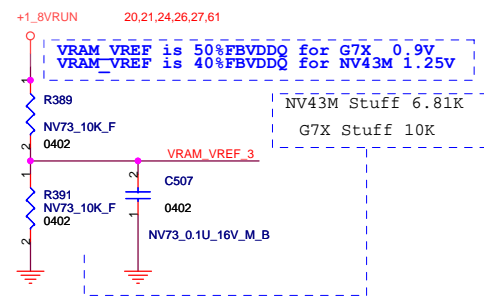
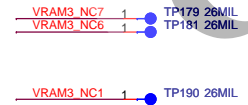
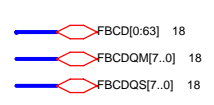
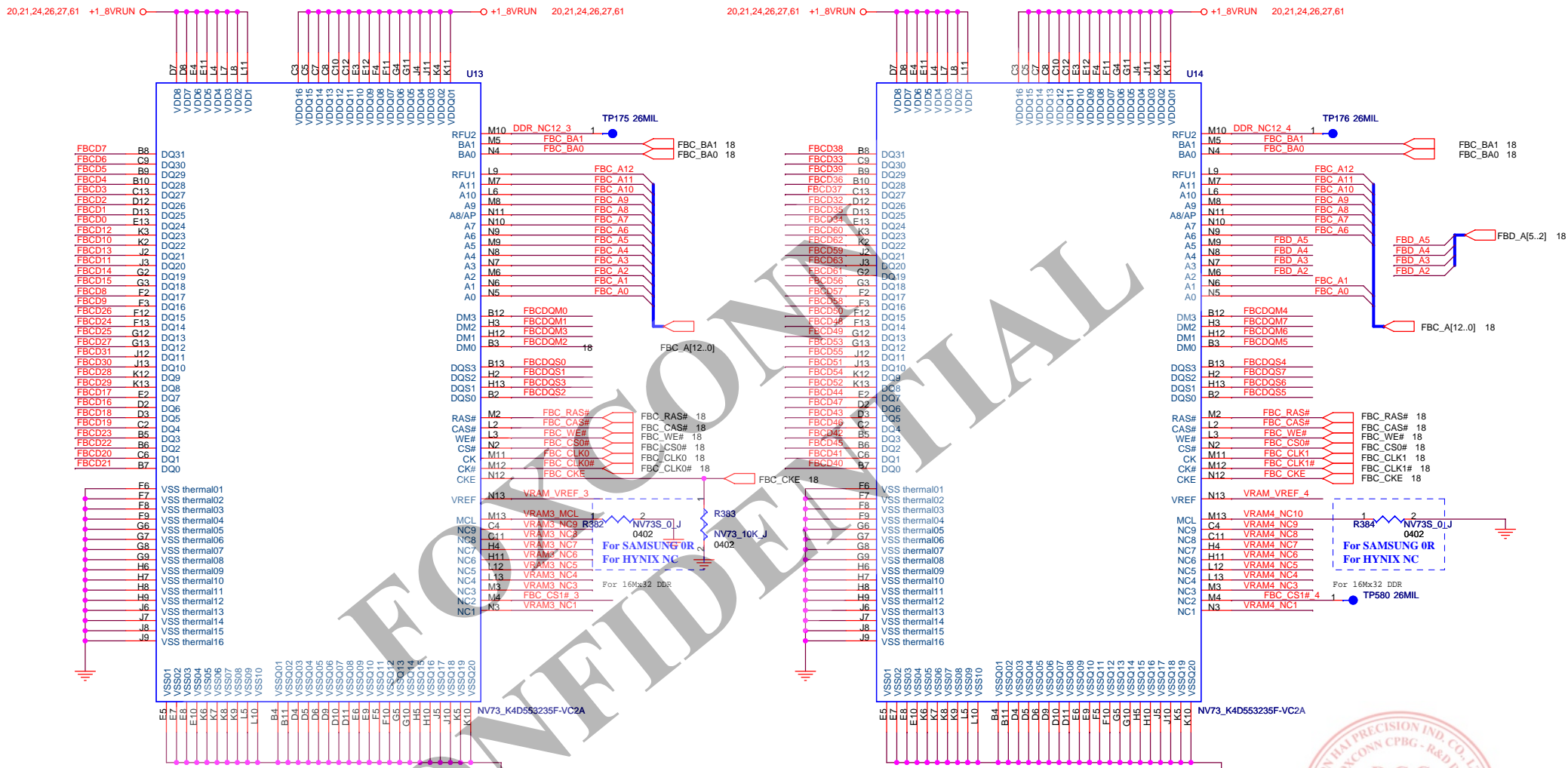
CLOSE TO GPU



DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDOCCLK			SCL
	VGA-DDOCDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDOCCLK			SCL
	DVI-DDOCDATA			SDA





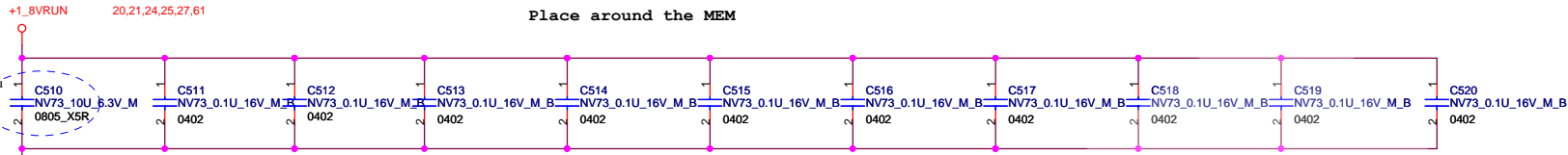


If use G72M, please unstuff U13, U14 and their related circuit

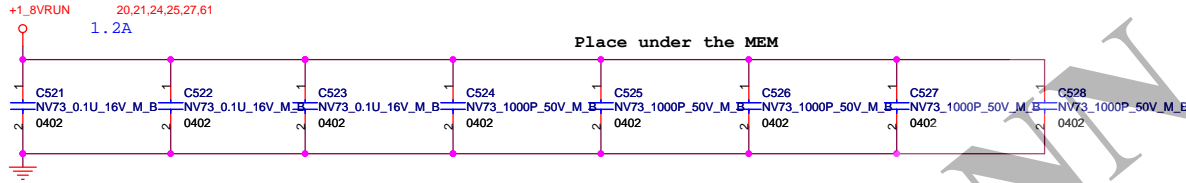
MS11 DVT modify

Decoupling for right MEMORY

Place around the MEM

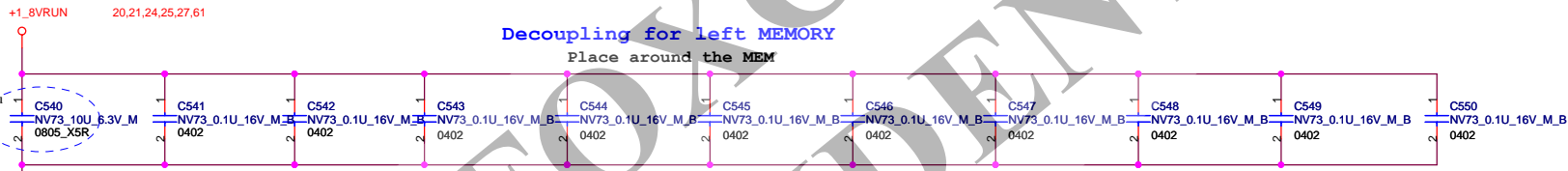


Place under the MEM

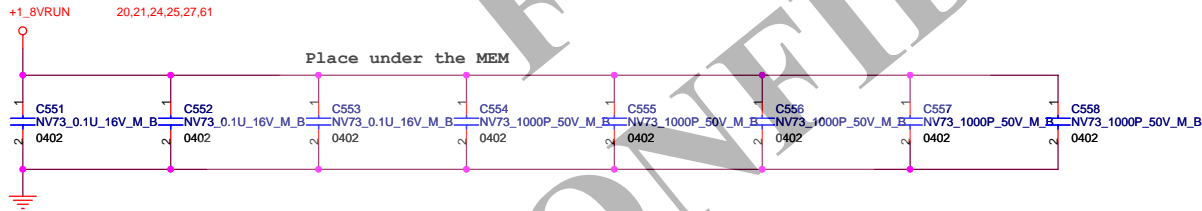


Decoupling for left MEMORY

Place around the MEM



Place under the MEM

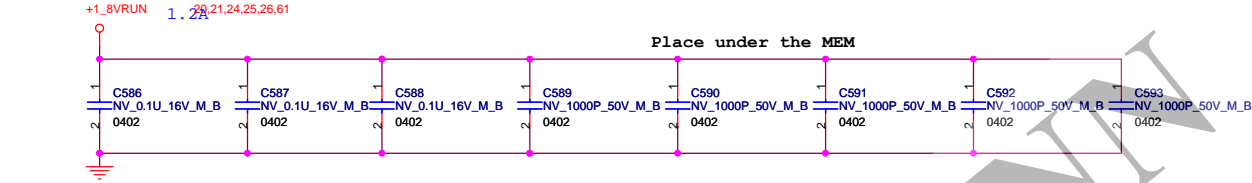
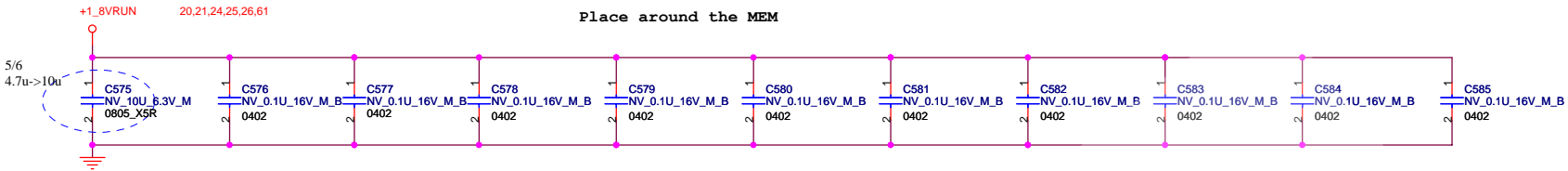


CONFIDENTIAL



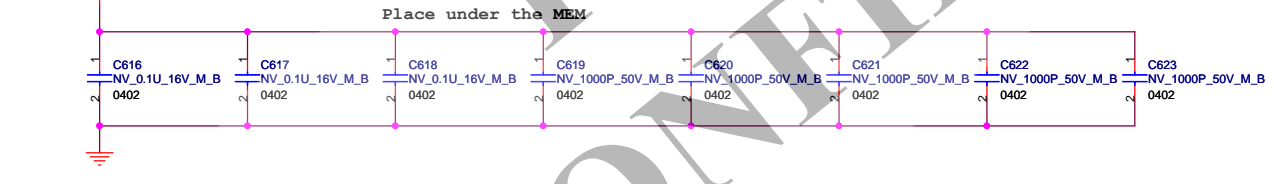
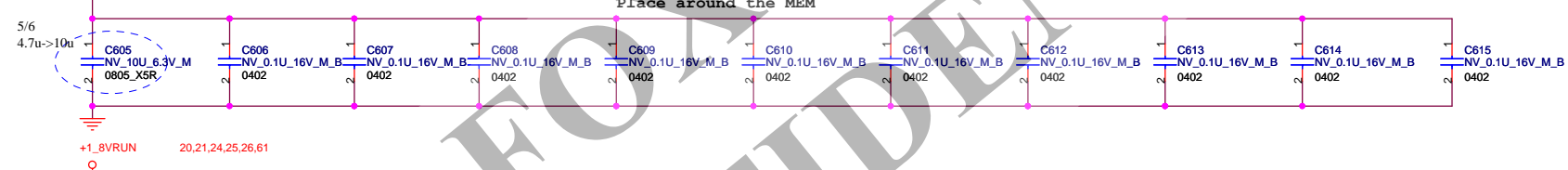
FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>VRAM (GDDR) 3 OF 4</b>		
Size A3	Document Number MS11-1-01 ( MBX-149 )	Rev 0.3
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Decoupling for right MEMORY



NO USE

Decoupling for left MEMORY



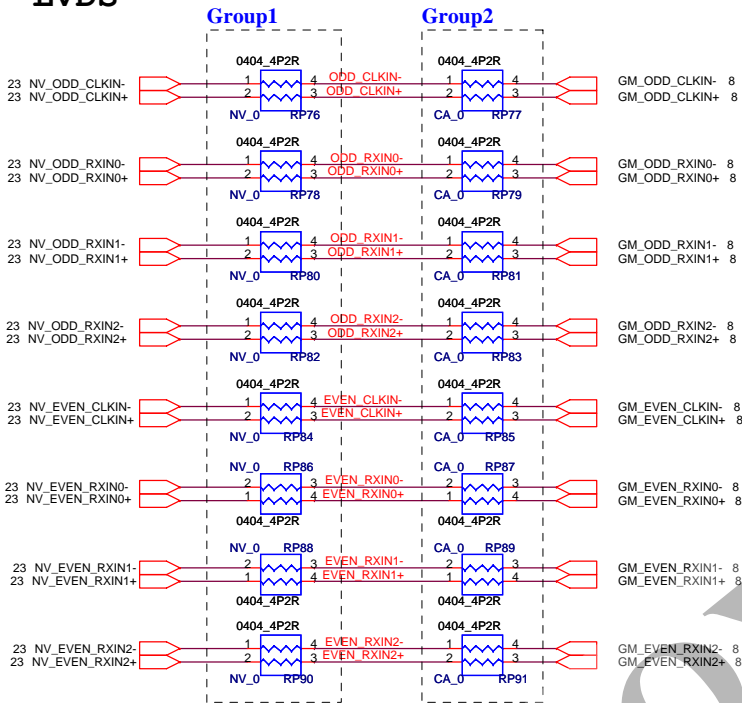
CONFIDENTIAL



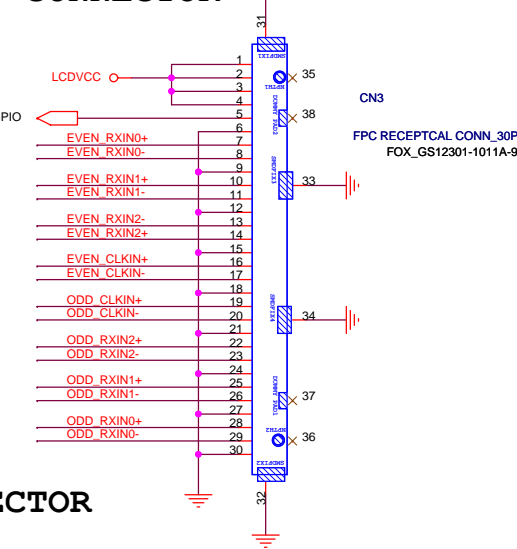
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	<b>VRAM (POWERBYPASS) 4 OF 4</b>	
Size	Document Number	Rev
A3	MS11-1-01 (MBX-149)	0.3
Date:	Friday, February 17, 2006	Sheet 27 of 66

# LVDS

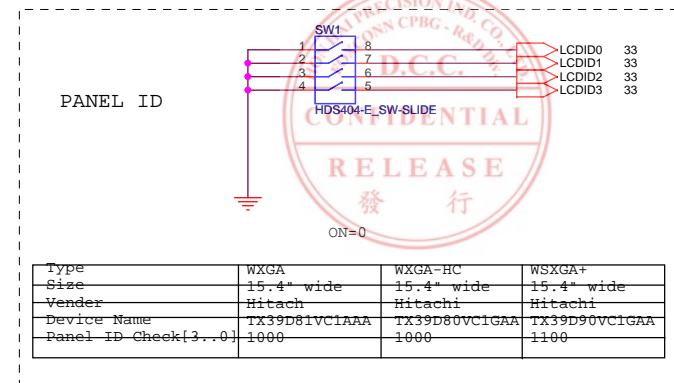
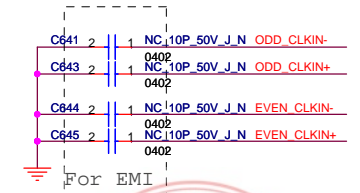
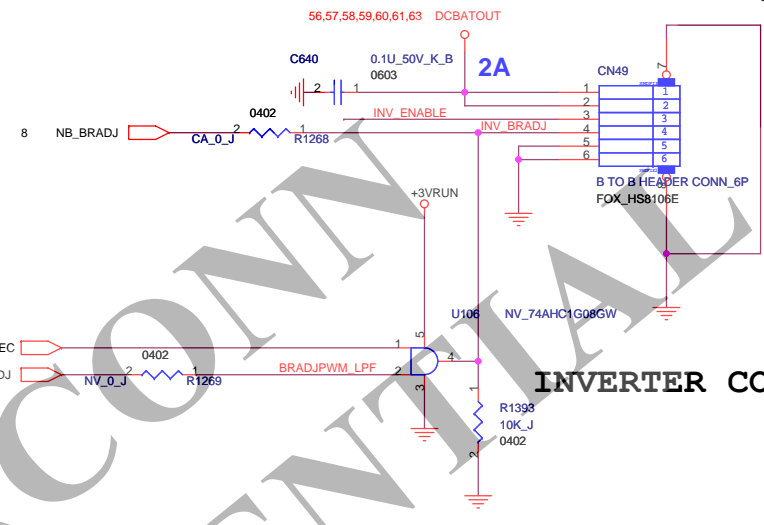
Group1, Group1 should be close



# LVDS CONNECTOR



# INVERTER CONNECTOR



Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	Hitachi	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID check[3..0]	1000	1000	1100

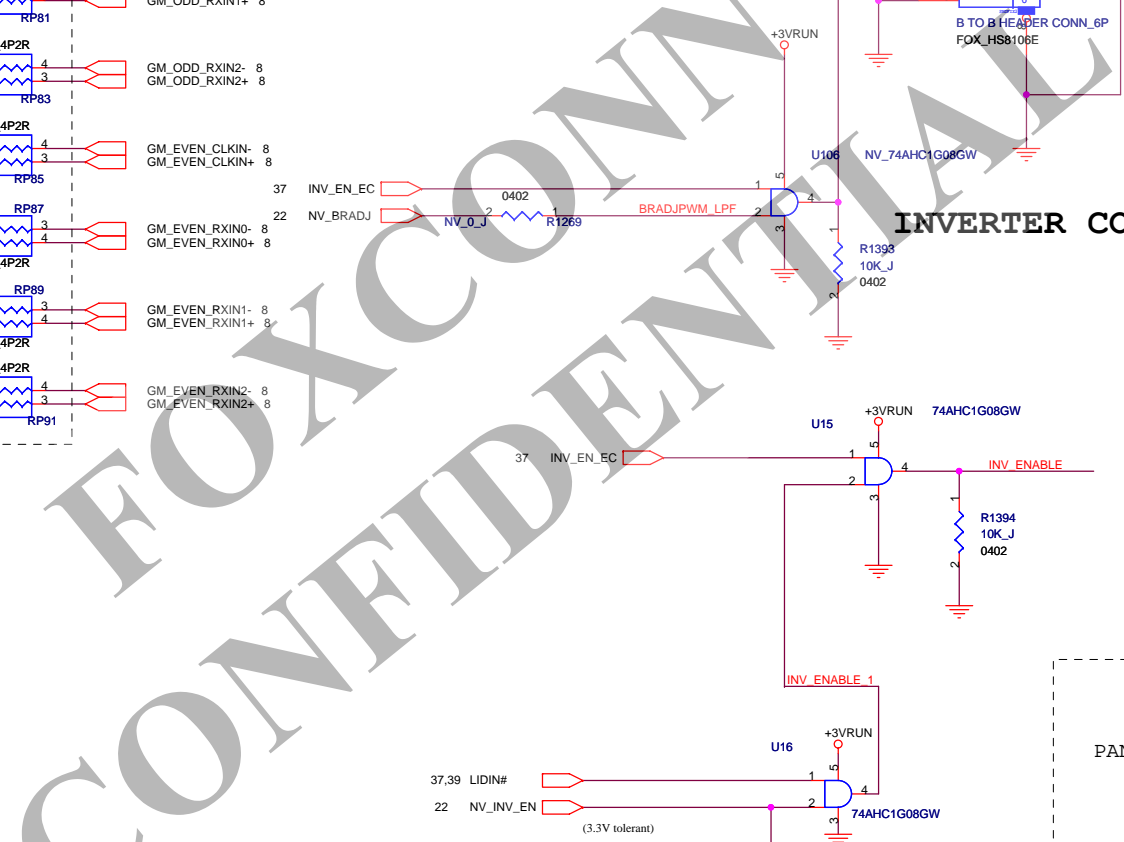
DISCHARGE  
The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

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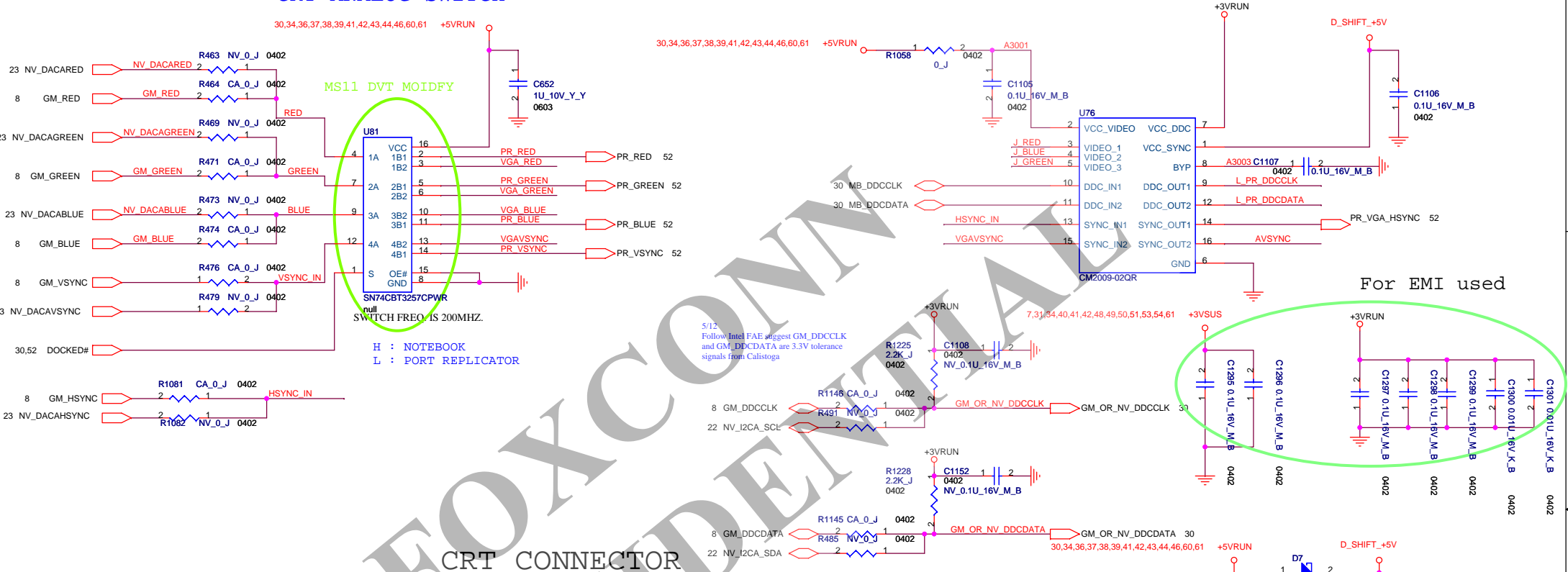
Title: **LVDS**

Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.3
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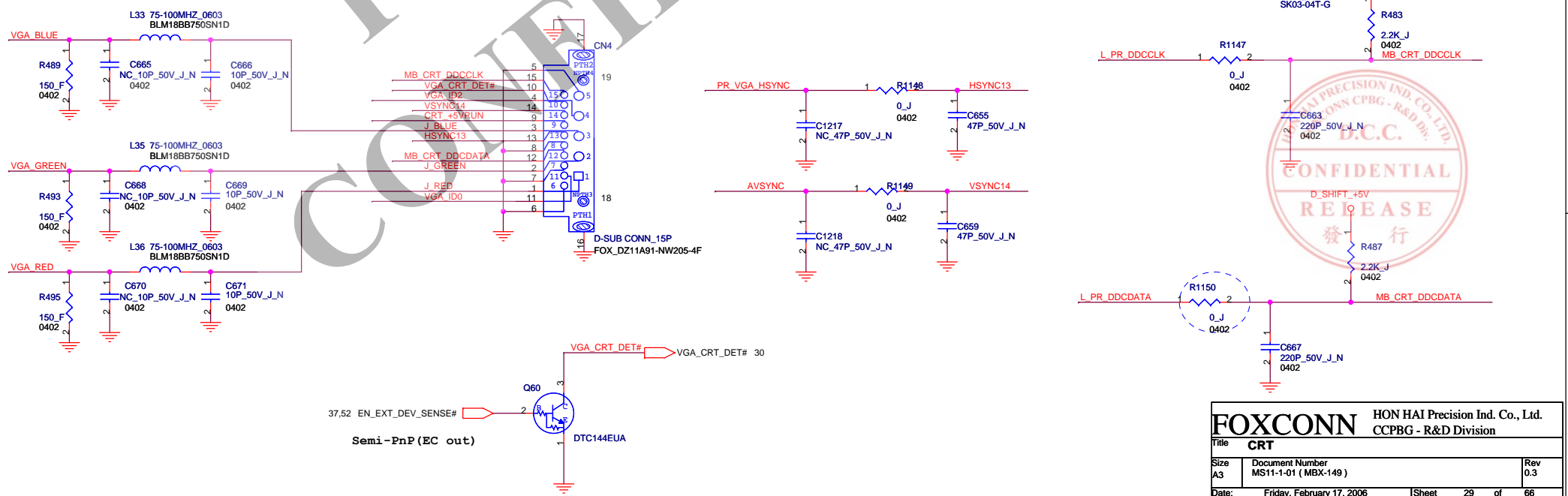
Date: Friday, February 17, 2006 | Sheet 28 of 66



# CRT ANALOG SWITCH



# CRT CONNECTOR

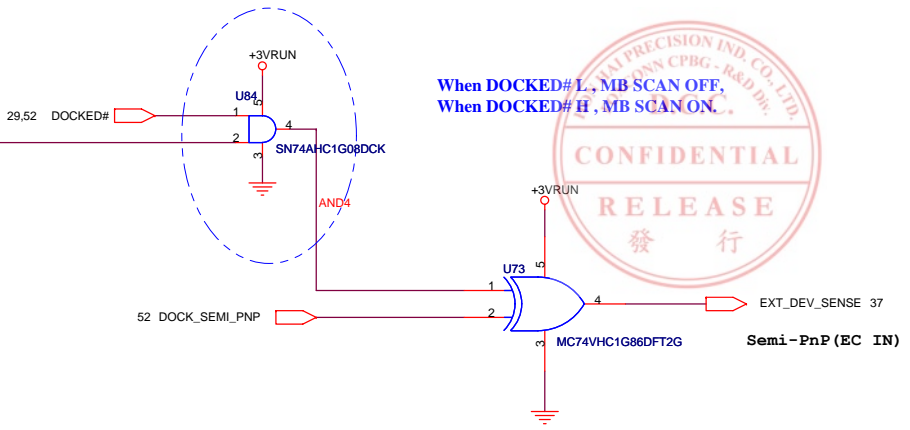
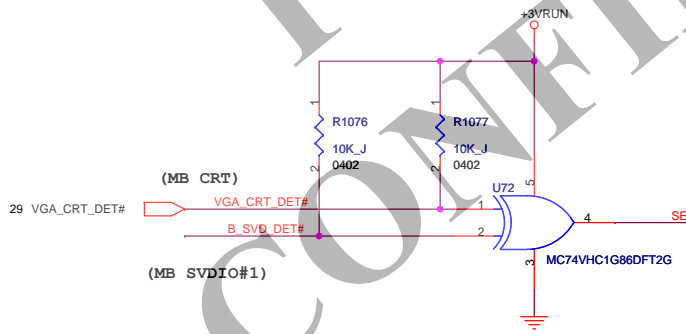
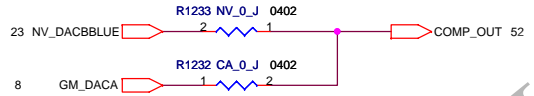
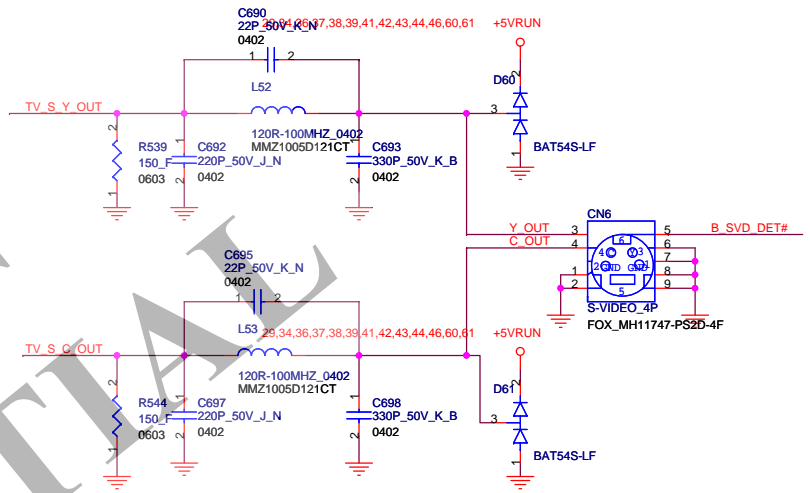
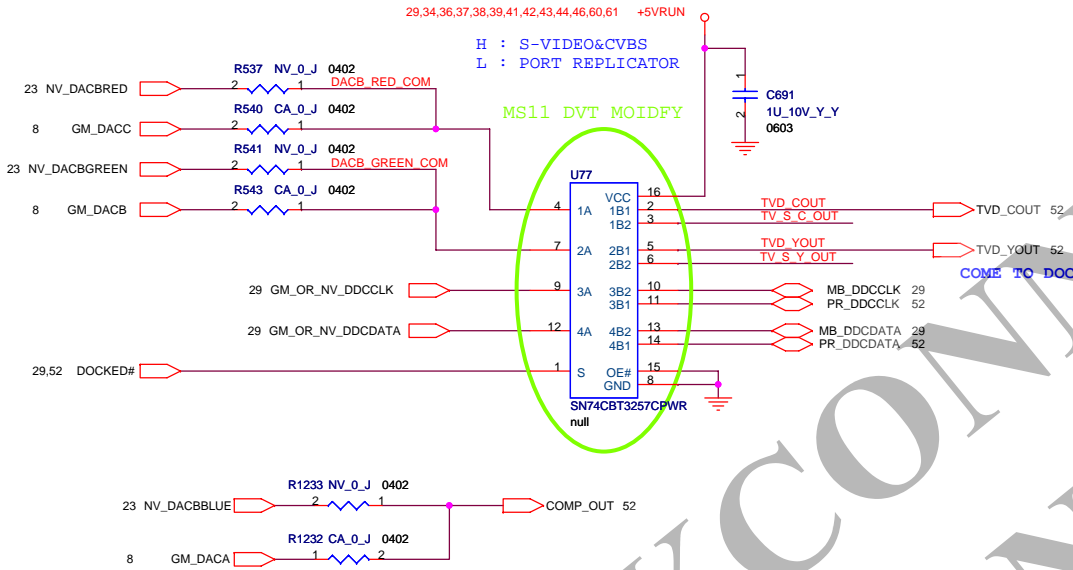


<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CRT	
Size	Document Number	Rev
A3	MS11-1-01 (MBX-149)	0.3
Date:	Friday, February 17, 2006	Sheet 29 of 66

# S-VIDEO

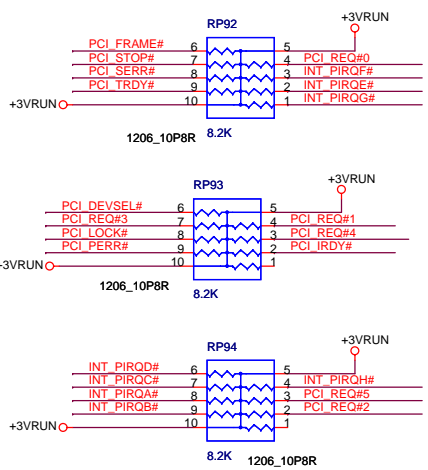
These component close to S-Video connector within 700 mil

## S-VIDEO ANALOG SWITCH

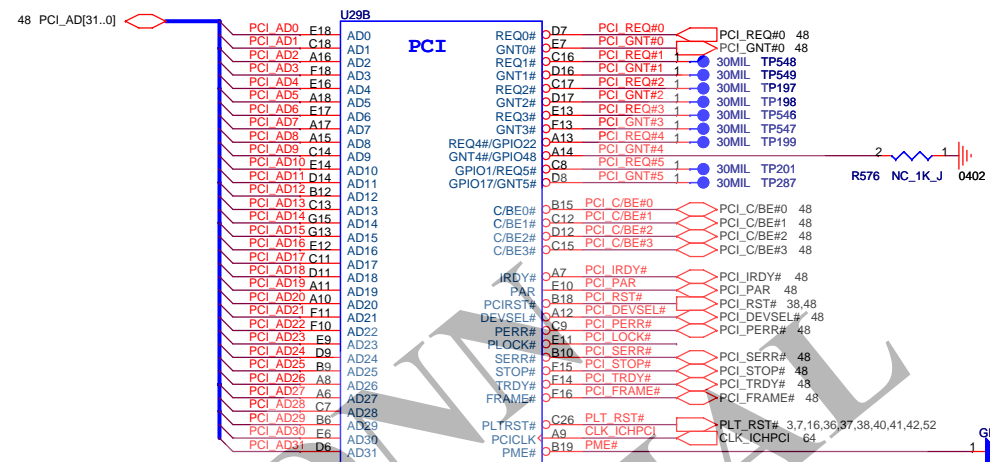


When DOCKED# L, MB SCAN OFF,  
When DOCKED# H, MB SCAN ON.

Semi-PnP

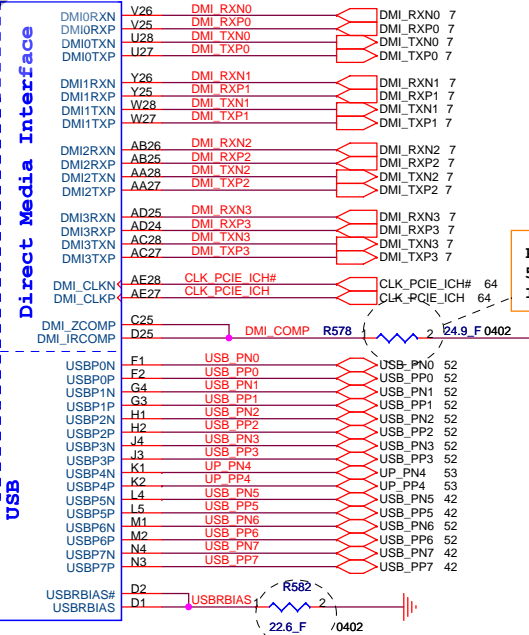
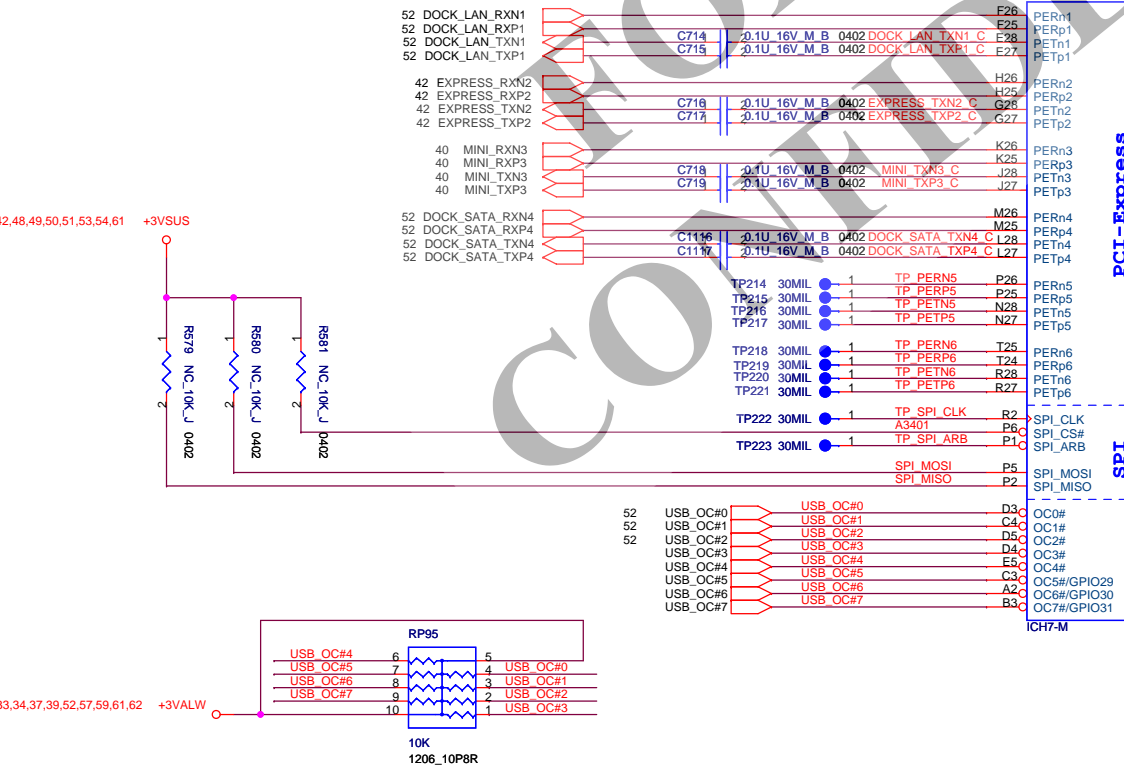
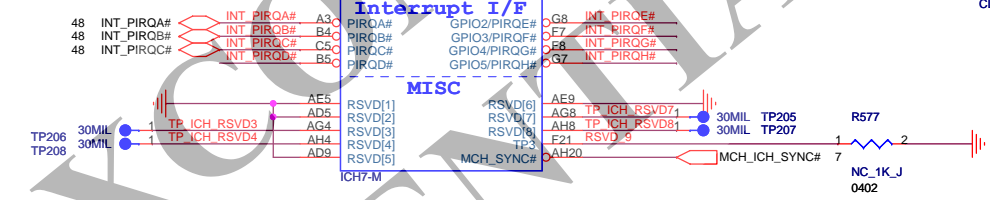


PCI Pullups



Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	H1	H1
PCI	H1	LOW

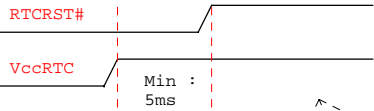


Place within 500 mils of ICH

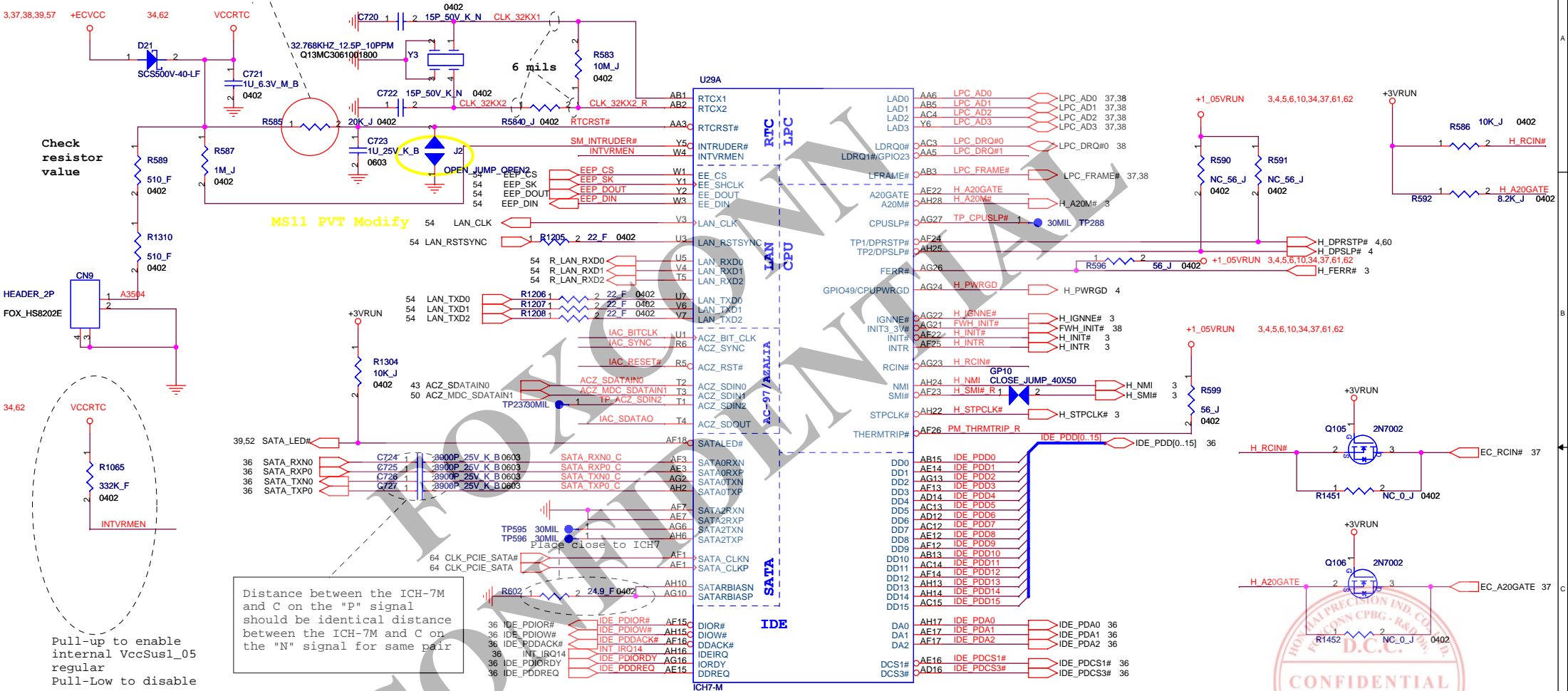
Place within 500 mils of ICH and don't routing next to high speed signals





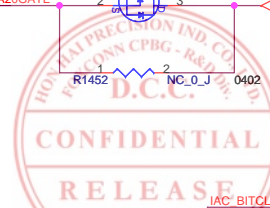
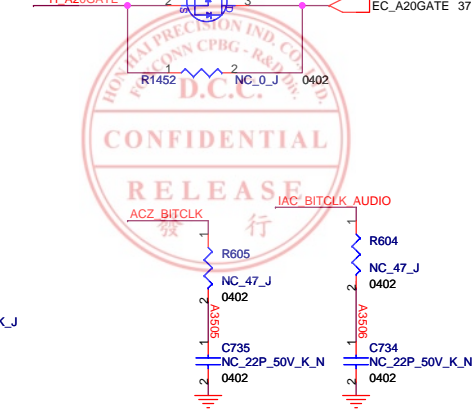
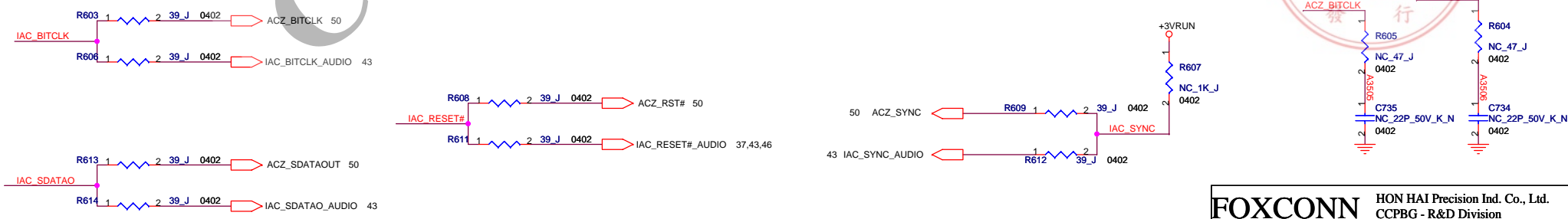


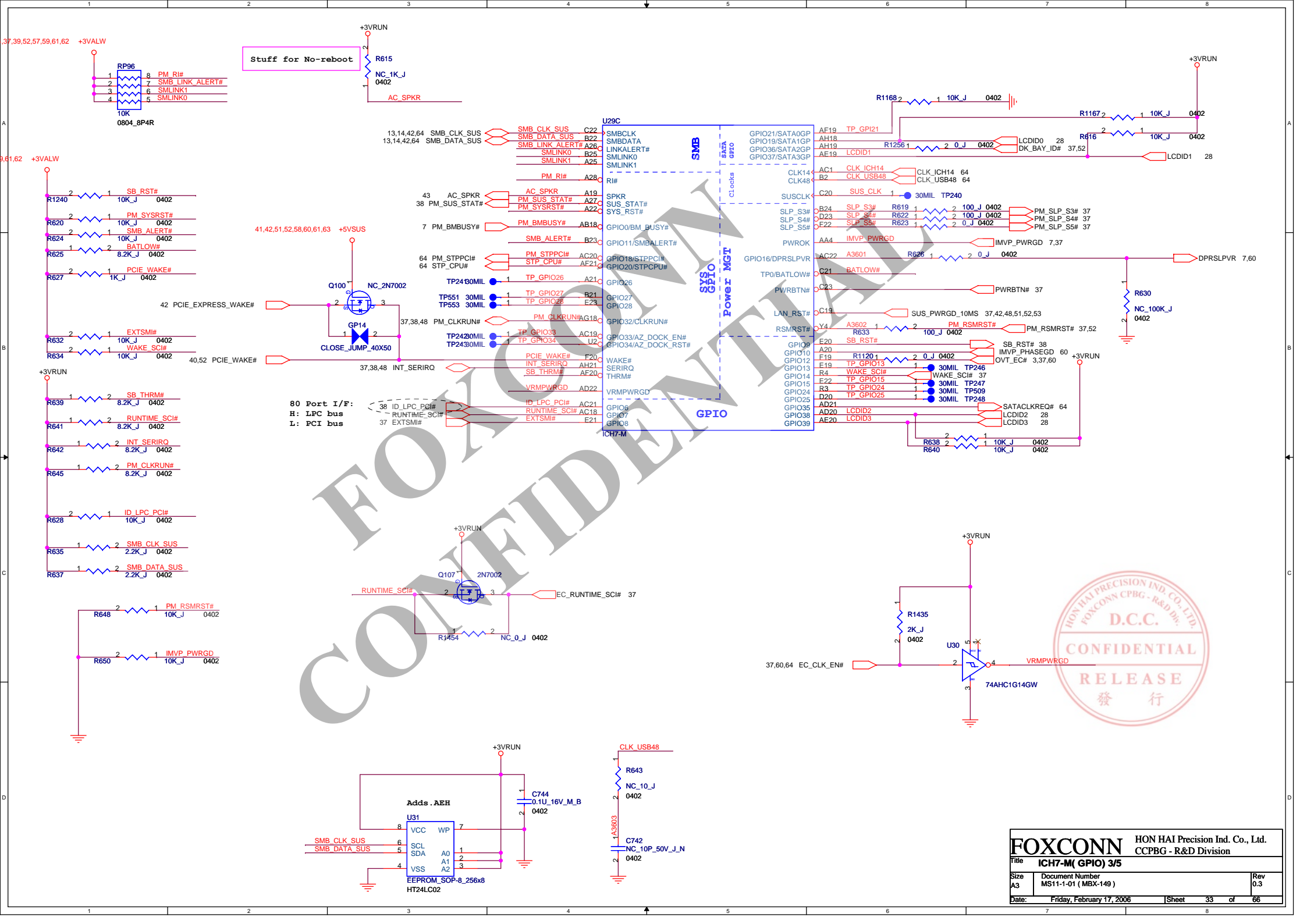
The traces inside this block should be wider.  
No digital signals routed under XTAL



Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

Pull-up to enable internal VccSus1\_05 regular  
Pull-Low to disable



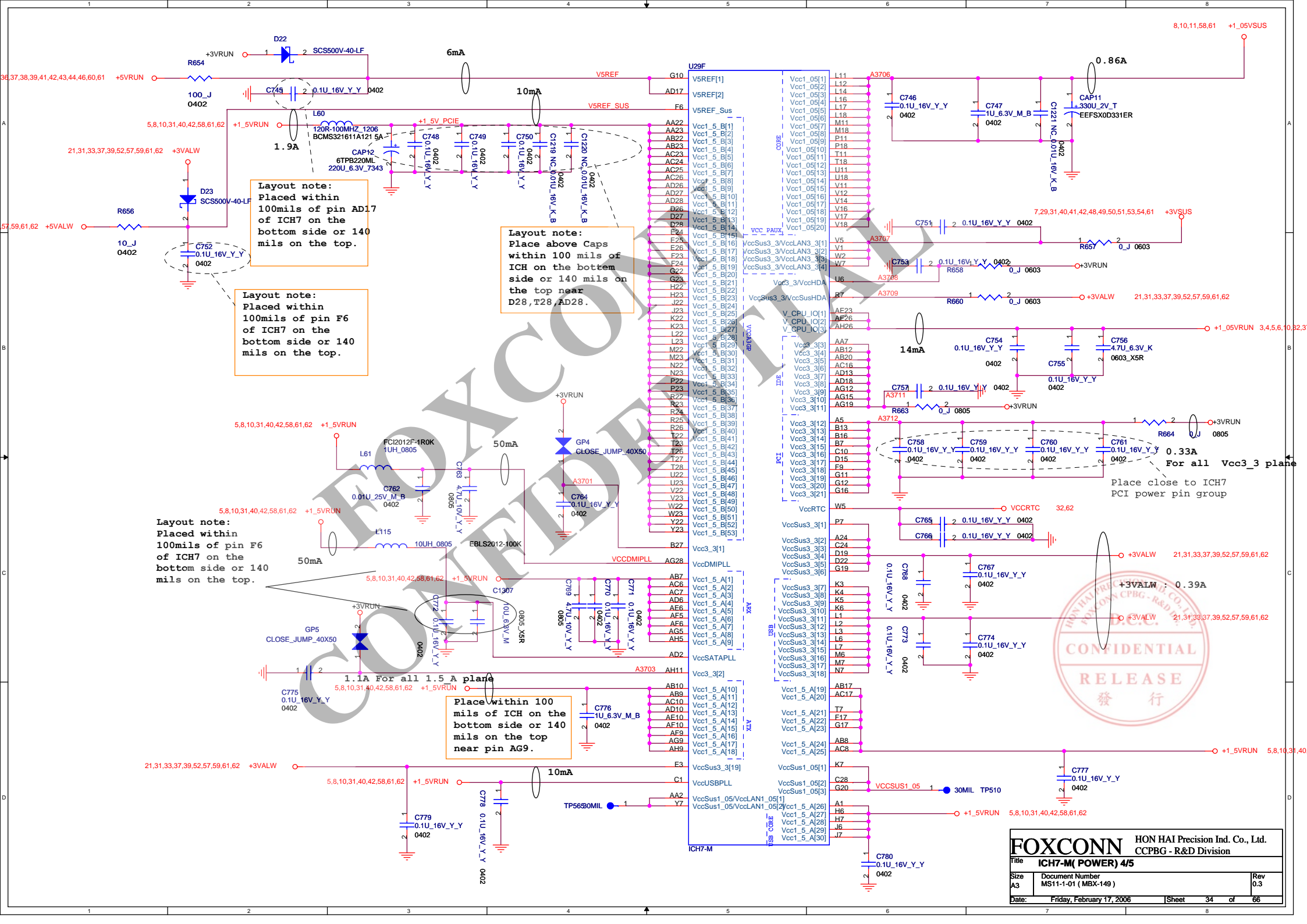


Stuff for No-reboot

80 Port I/F:  
H: LPC bus  
L: PCI bus



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
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**Layout note:**  
Placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top.

**Layout note:**  
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

**Layout note:**  
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

**Layout note:**  
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

**Layout note:**  
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

Place close to ICH7 PCI power pin group



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.	
Title <b>ICH7-M (POWER) 4/5</b>	
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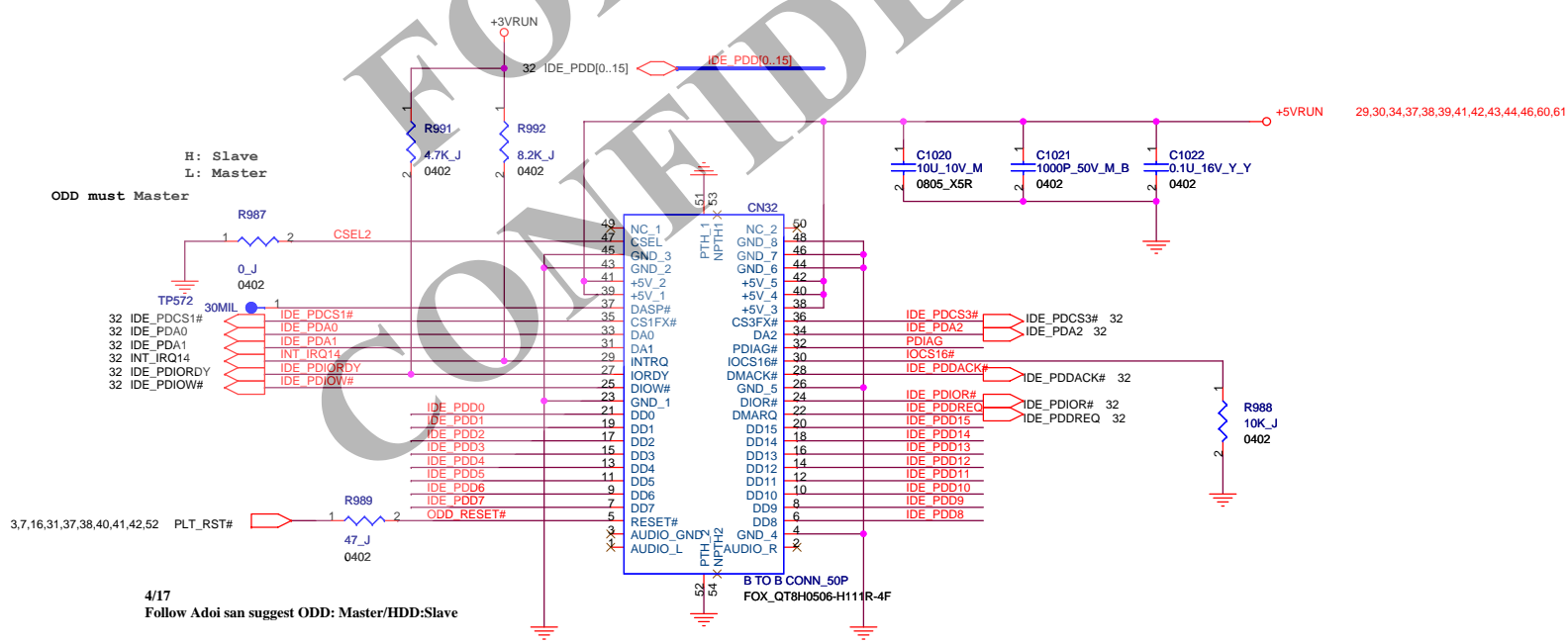
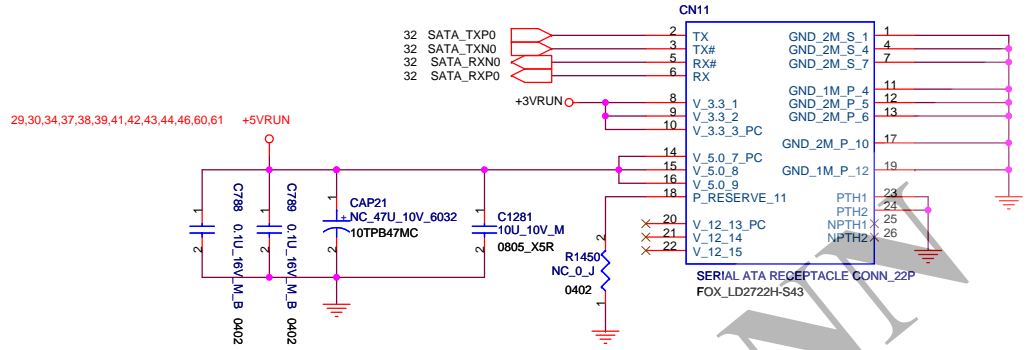
CONFIDENTIAL

U29E			
A4	VSS11	VSS108	P28
A23	VSS12	VSS109	R1
B1	VSS13	VSS110	R11
B3	VSS14	VSS111	R12
B11	VSS15	VSS112	R13
B14	VSS16	VSS113	R14
B17	VSS17	VSS114	R15
B20	VSS18	VSS115	R16
B26	VSS19	VSS116	R17
B28	VSS10	VSS107	R18
C2	VSS11	VSS108	T6
C6	VSS12	VSS109	T12
C27	VSS13	VSS110	T13
D10	VSS14	VSS111	T14
D13	VSS15	VSS112	T15
D18	VSS16	VSS113	T16
D21	VSS17	VSS114	T17
D24	VSS18	VSS115	U4
E1	VSS19	VSS116	U12
E2	VSS20	VSS117	U13
E4	VSS21	VSS118	U14
E8	VSS22	VSS119	U15
E16	VSS23	VSS120	U16
F3	VSS24	VSS121	U17
F4	VSS25	VSS122	U24
F6	VSS26	VSS123	U25
F12	VSS27	VSS124	U26
F27	VSS28	VSS125	V2
F28	VSS29	VSS126	V13
G1	VSS30	VSS127	V15
G2	VSS31	VSS128	V24
G5	VSS32	VSS129	V27
G6	VSS33	VSS130	V28
G9	VSS34	VSS131	W6
G14	VSS35	VSS132	W24
G18	VSS36	VSS133	W25
G21	VSS37	VSS134	W26
G24	VSS38	VSS135	Y3
G25	VSS39	VSS136	Y24
G26	VSS40	VSS137	Y27
H3	VSS41	VSS138	Y28
H4	VSS42	VSS139	AA1
H5	VSS43	VSS140	AA24
H24	VSS44	VSS141	AA25
H27	VSS45	VSS142	AA26
H28	VSS46	VSS143	AB4
J1	VSS47	VSS144	AB6
J2	VSS48	VSS145	AB11
J5	VSS49	VSS146	AB14
J24	VSS50	VSS147	AB16
J25	VSS51	VSS148	AB19
J26	VSS52	VSS149	AB21
K24	VSS53	VSS150	AB24
K27	VSS54	VSS151	AB27
K28	VSS55	VSS152	AB28
L13	VSS56	VSS153	AC2
L15	VSS57	VSS154	AC5
L24	VSS58	VSS155	AC9
L25	VSS59	VSS156	AC11
L26	VSS60	VSS157	AD1
M3	VSS61	VSS158	AD3
M4	VSS62	VSS159	AD4
M5	VSS63	VSS160	AD7
M12	VSS64	VSS161	AD8
M13	VSS65	VSS162	AD11
M14	VSS66	VSS163	AD15
M15	VSS67	VSS164	AD19
M16	VSS68	VSS165	AD23
M17	VSS69	VSS166	AE2
M24	VSS70	VSS167	AE4
M27	VSS71	VSS168	AE8
M28	VSS72	VSS169	AE11
N1	VSS73	VSS170	AE13
N2	VSS74	VSS171	AE18
N5	VSS75	VSS172	AE21
N6	VSS76	VSS173	AE24
N11	VSS77	VSS174	AE25
N12	VSS78	VSS175	AF2
N13	VSS79	VSS176	AF4
N14	VSS80	VSS177	AF8
N15	VSS81	VSS178	AF11
N16	VSS82	VSS179	AF27
N17	VSS83	VSS180	AF28
N18	VSS84	VSS181	AG1
N24	VSS85	VSS182	AG3
N25	VSS86	VSS183	AG7
N26	VSS87	VSS184	AG11
P3	VSS88	VSS185	AG14
P4	VSS89	VSS186	AG17
P12	VSS90	VSS187	AG20
P13	VSS91	VSS188	AG25
P14	VSS92	VSS189	AH1
P15	VSS93	VSS190	AH3
P16	VSS94	VSS191	AH7
P17	VSS95	VSS192	AH12
P24	VSS96	VSS193	AH23
P27	VSS97	VSS194	AH27

ICH7-M



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
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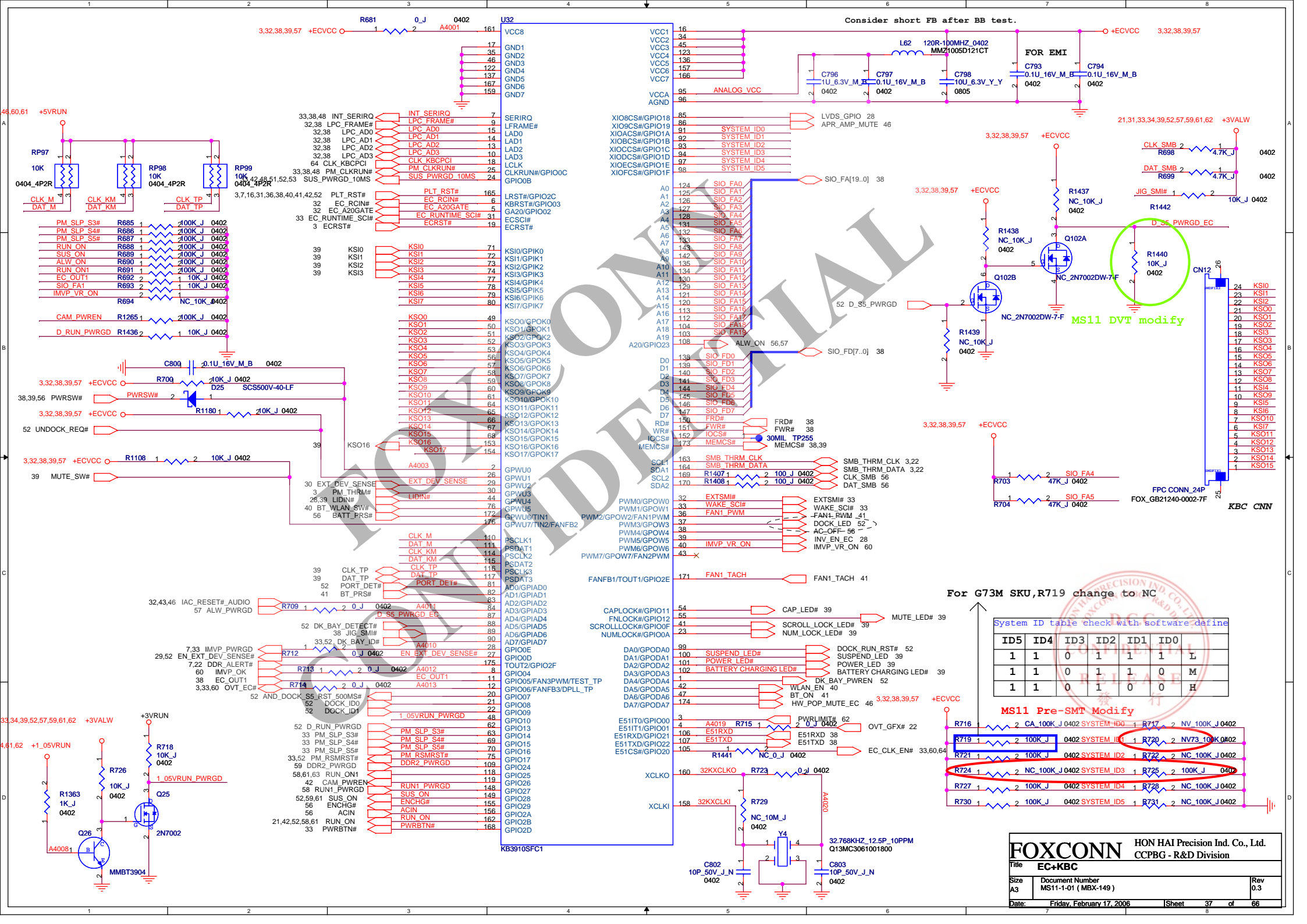


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## CD-ROM CONN

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>SATA HDD/CD-ROM</b>		
Size A3	Document Number MS11-1-01 ( MBX-149 )	Rev 0.3
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Consider short FB after BB test.

FOR EMI

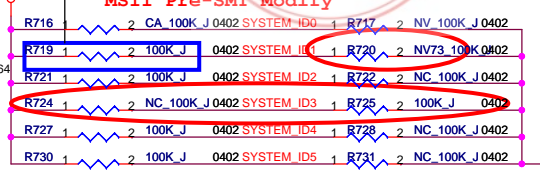
MS11 DVT modify

For G73M SKU, R719 change to NC

System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0	
1	1	0	1	1	1	L
1	1	0	1	1	0	M
1	1	0	1	0	0	H

MS11 Pre-SMT Modify



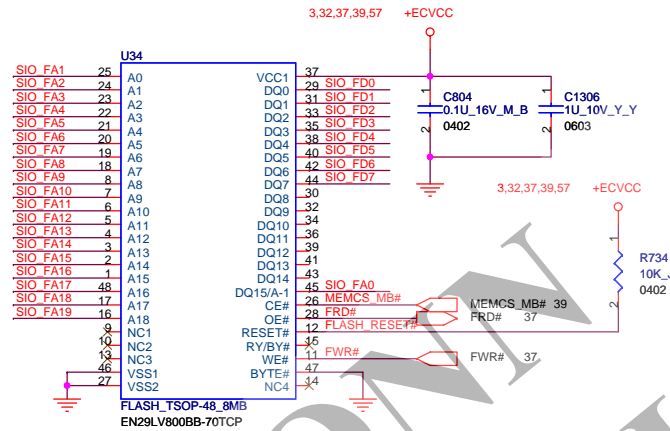
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **EC+KBC**

Size A3	Document Number MS11-1-01 ( MBX-149 )	Rev 0.3
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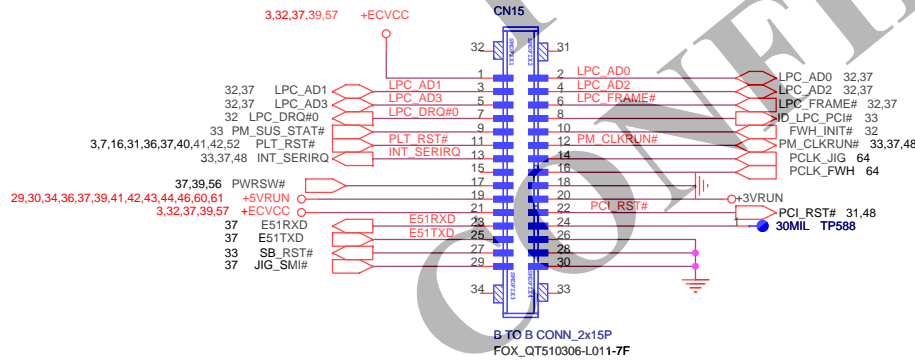
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37 SIO\_FA[19..0]  
 37 SIO\_FD[7..0]

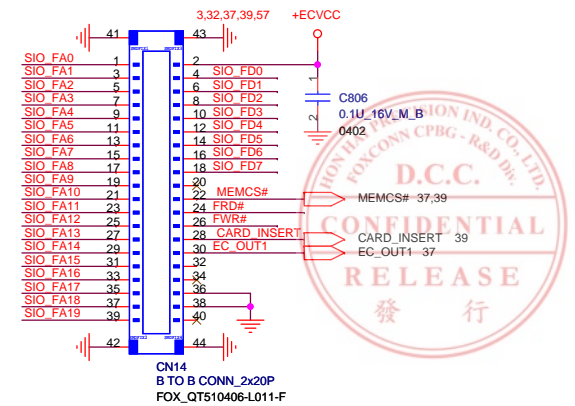


**FLASH BIOS**

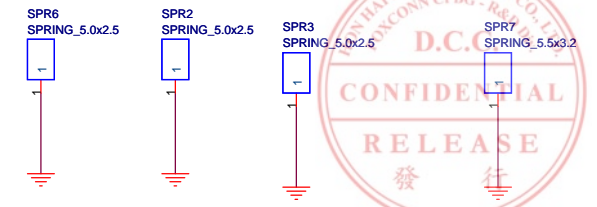
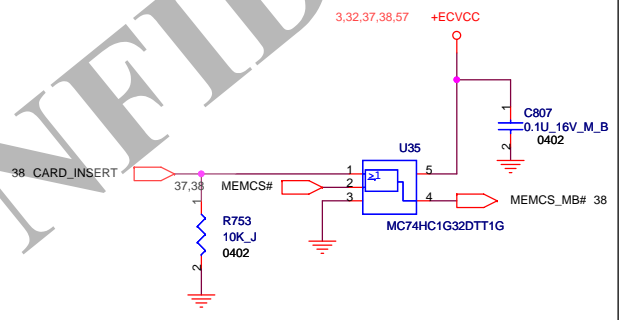
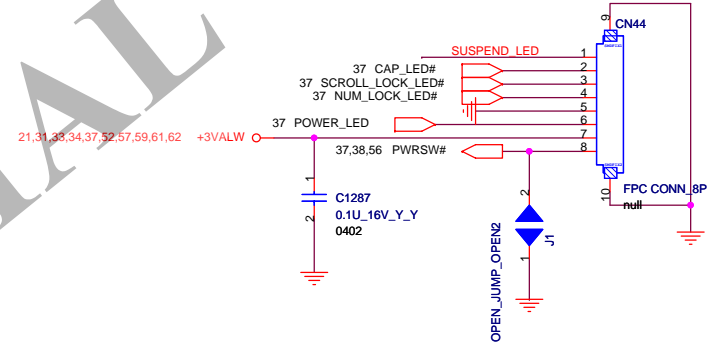
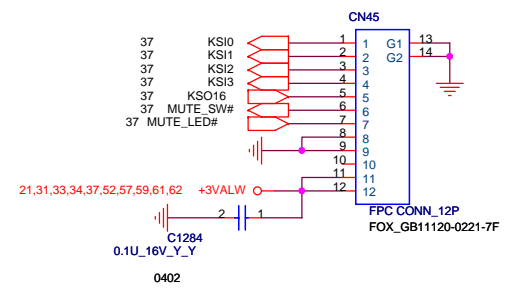
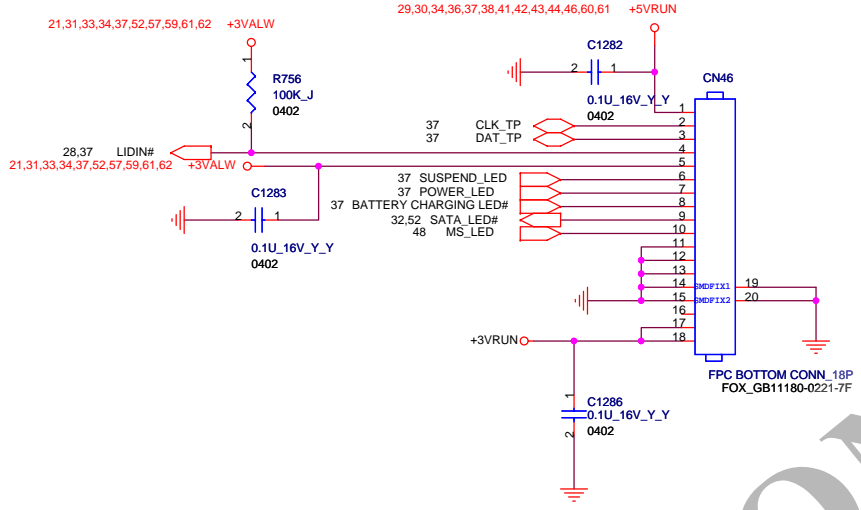
**JIG-120**



B TO B CONN\_2x15P  
 FOX\_QT510306-L011-7F



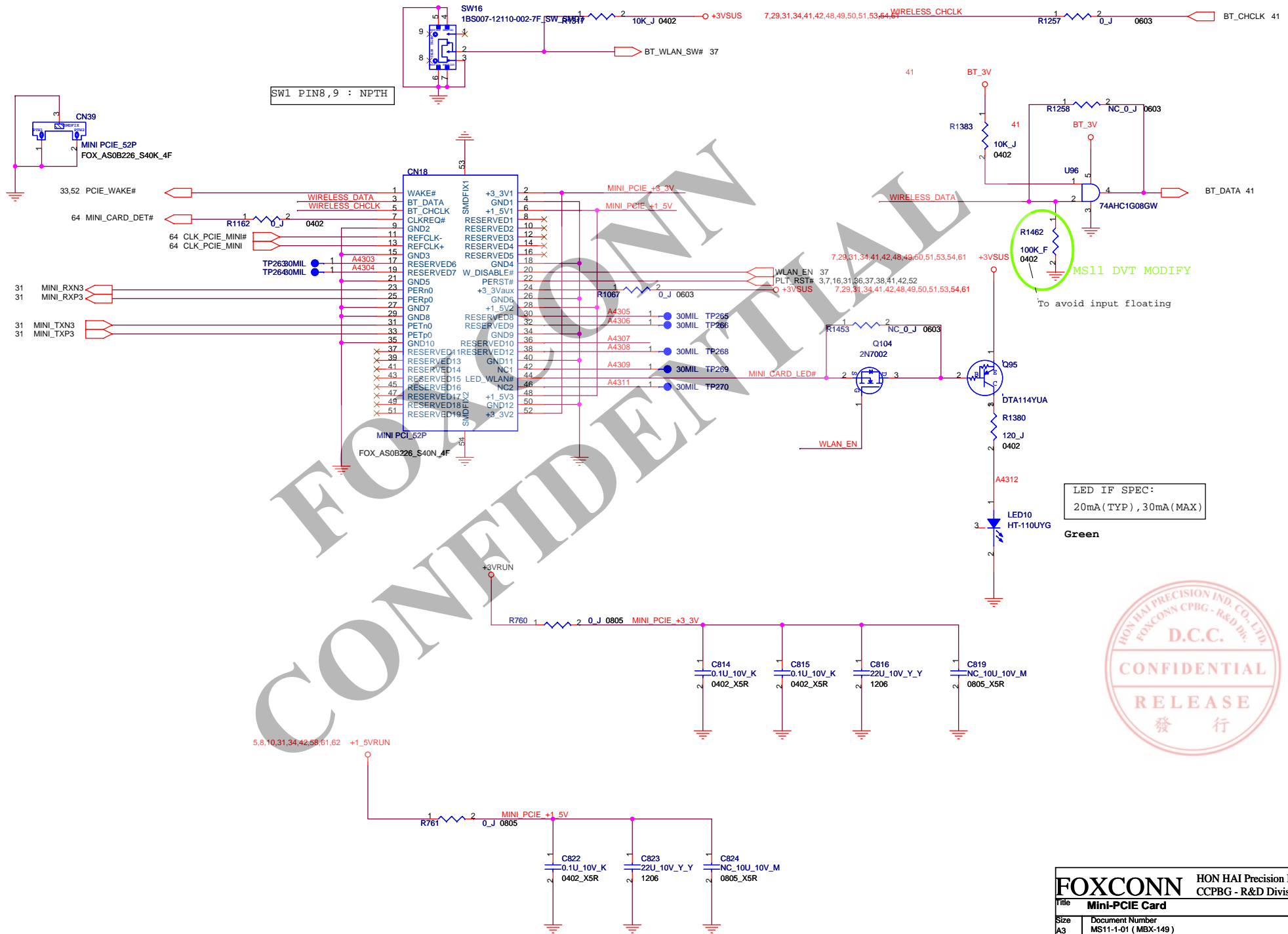
CN14  
 B TO B CONN\_2x20P  
 FOX\_QT510406-L011-F



FOXC CONN  
CONFIDENTIAL

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title <b>LED/LID SW#Touch PAD</b>	
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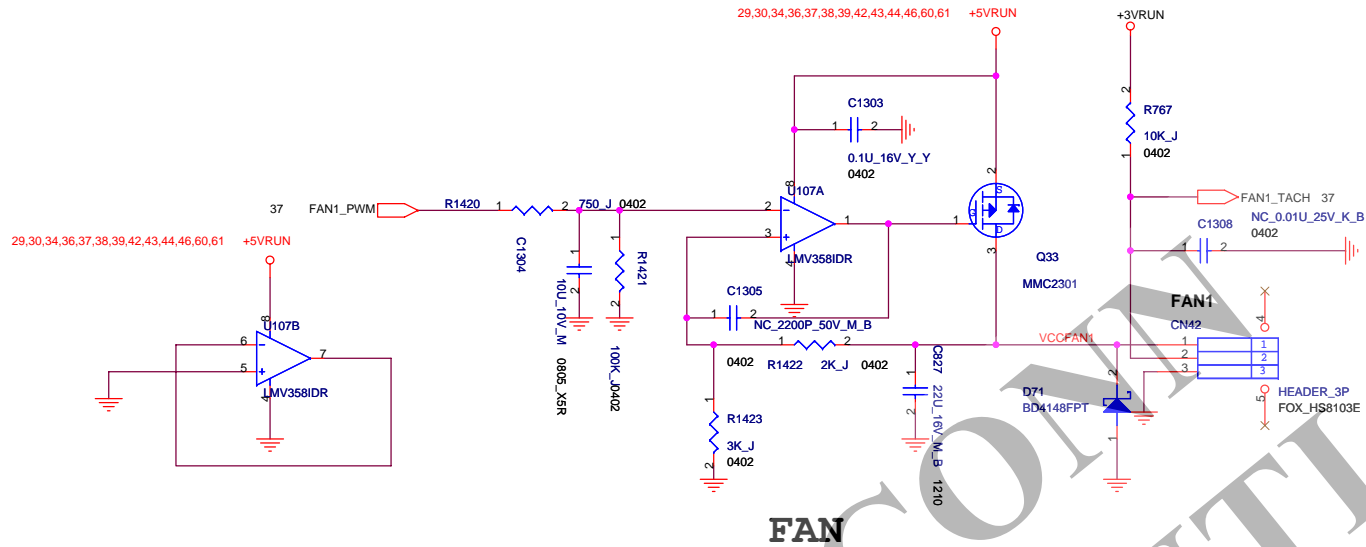
SW1 PIN8,9 : NPTH

MS11 DVT MODIFY  
To avoid input floating

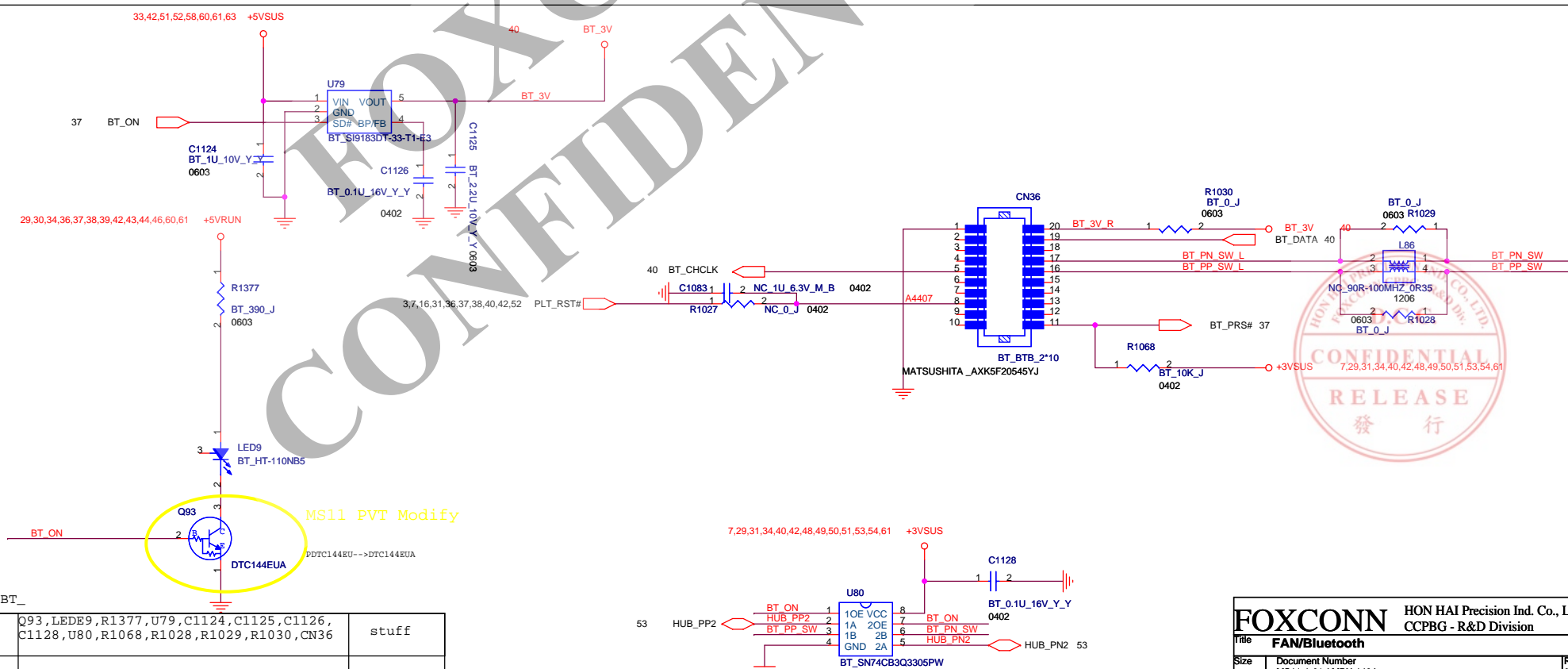
LED IF SPEC:  
20mA (TYP) , 30mA (MAX)  
Green



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>Mini-PCIE Card</b>		
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FAN



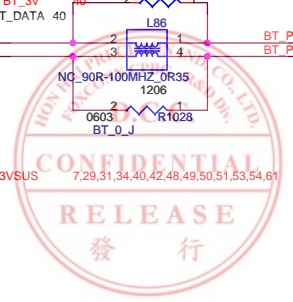
BOM Notice: BT\_

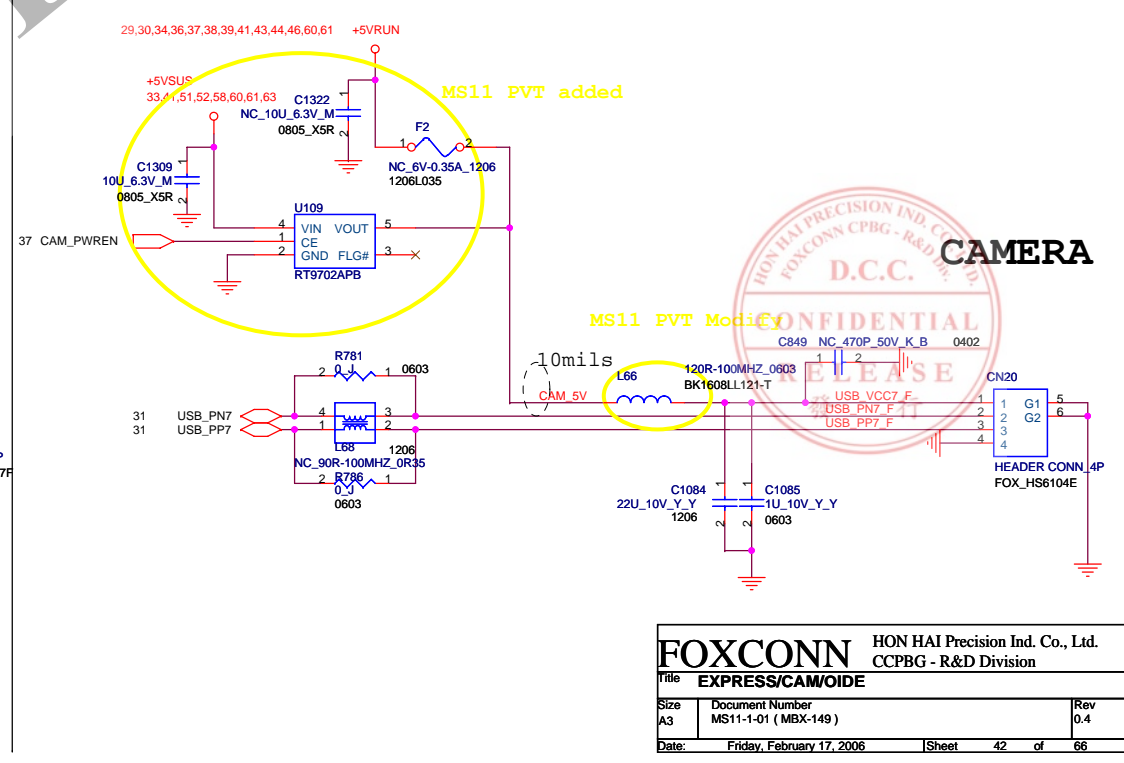
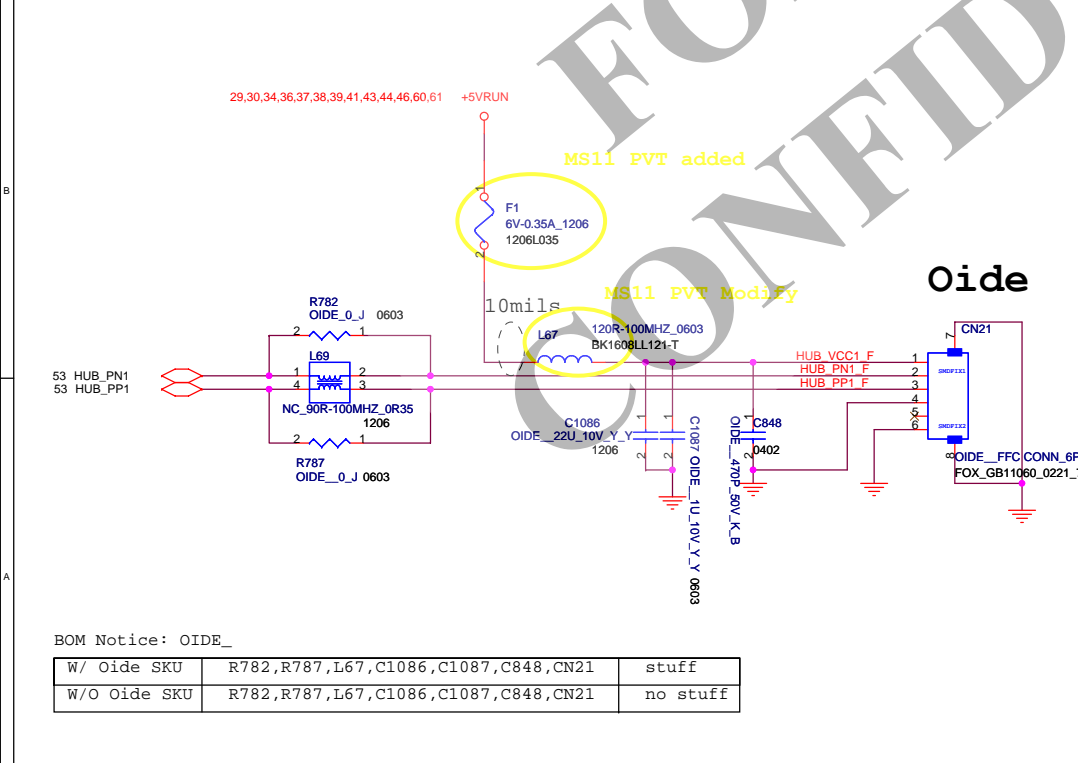
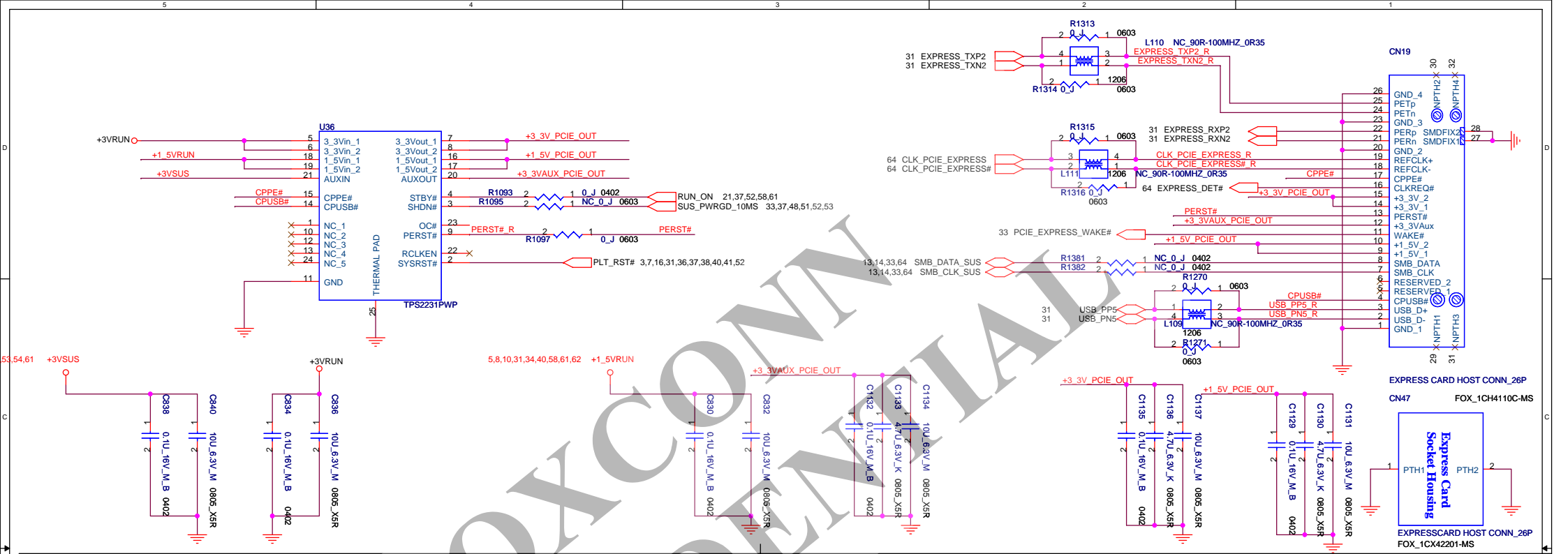
W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

File: **FAN/Bluetooth**

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BOM Notice: OIDE\_

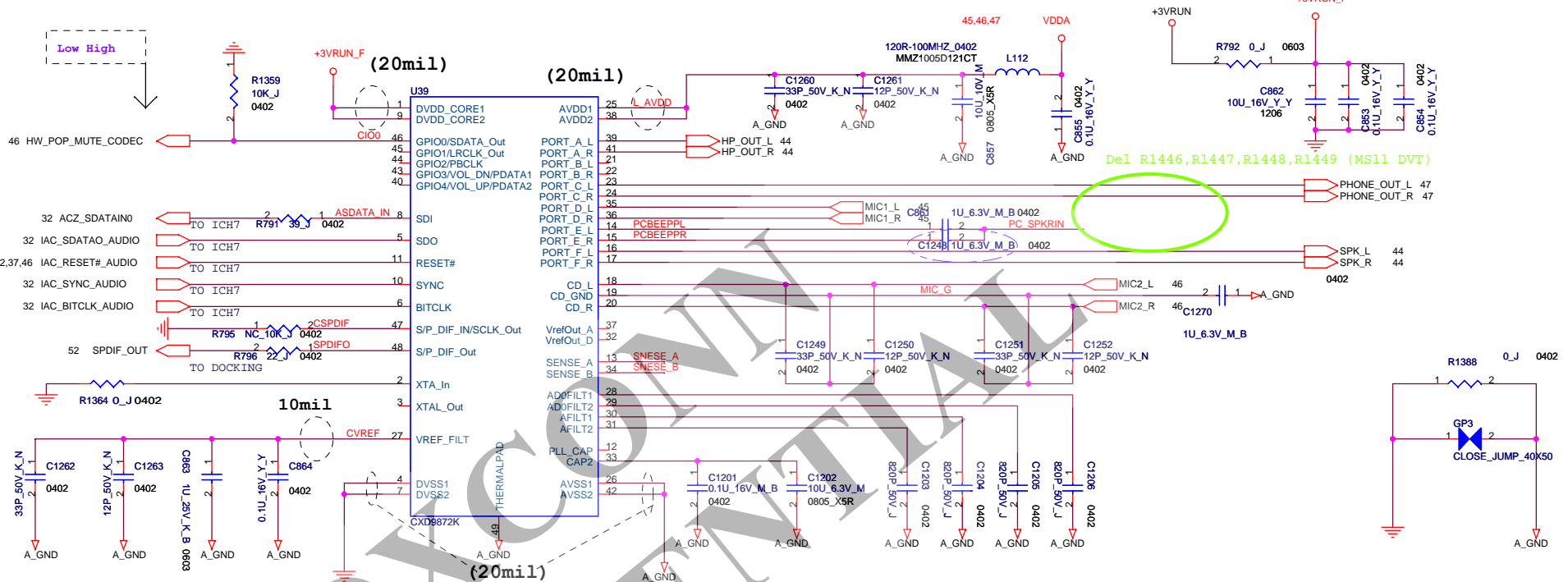
W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff

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HON HAI PRECISION IND. CO., LTD.  
D.C.C. CAMERA  
FOXCONN CPBG - R&D DIV.

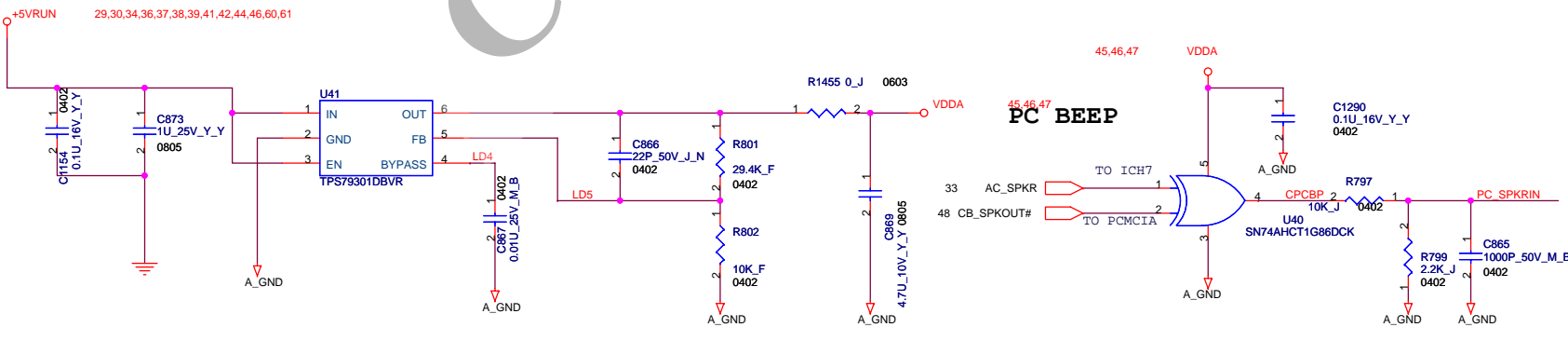
**RELEASE**

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>EXPRESS/CAM/OIDE</b>	
Size A3	Document Number MS11-1-01 (MBX-149)
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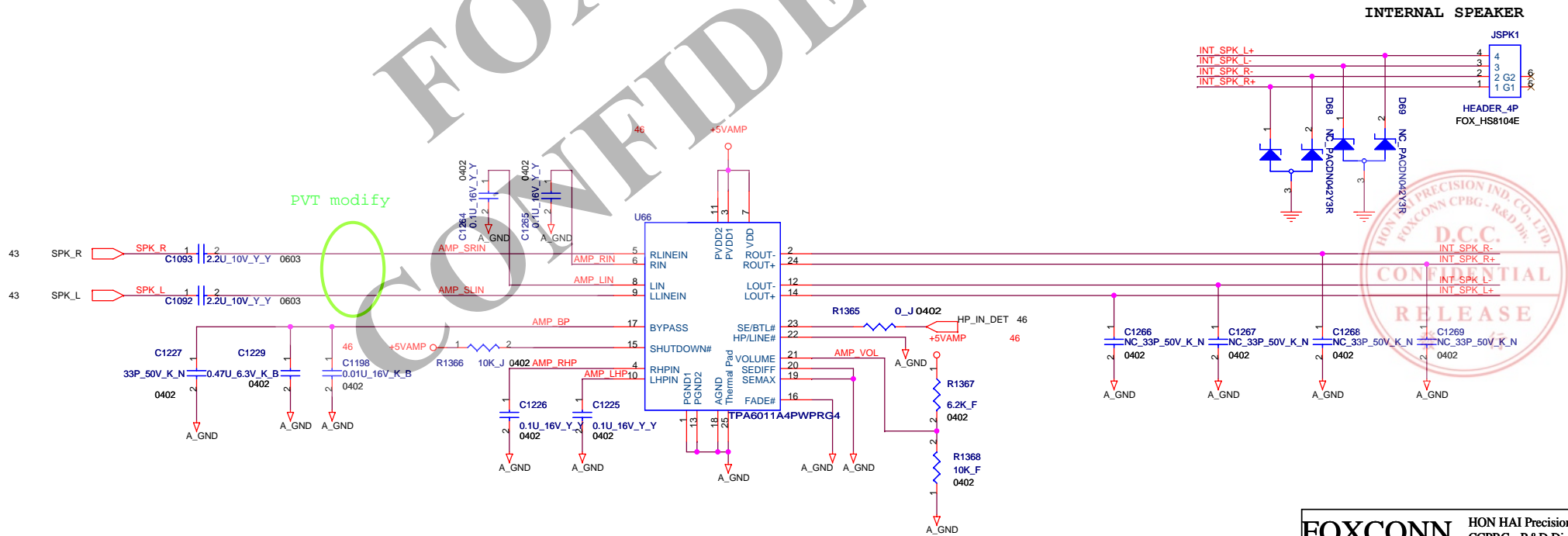
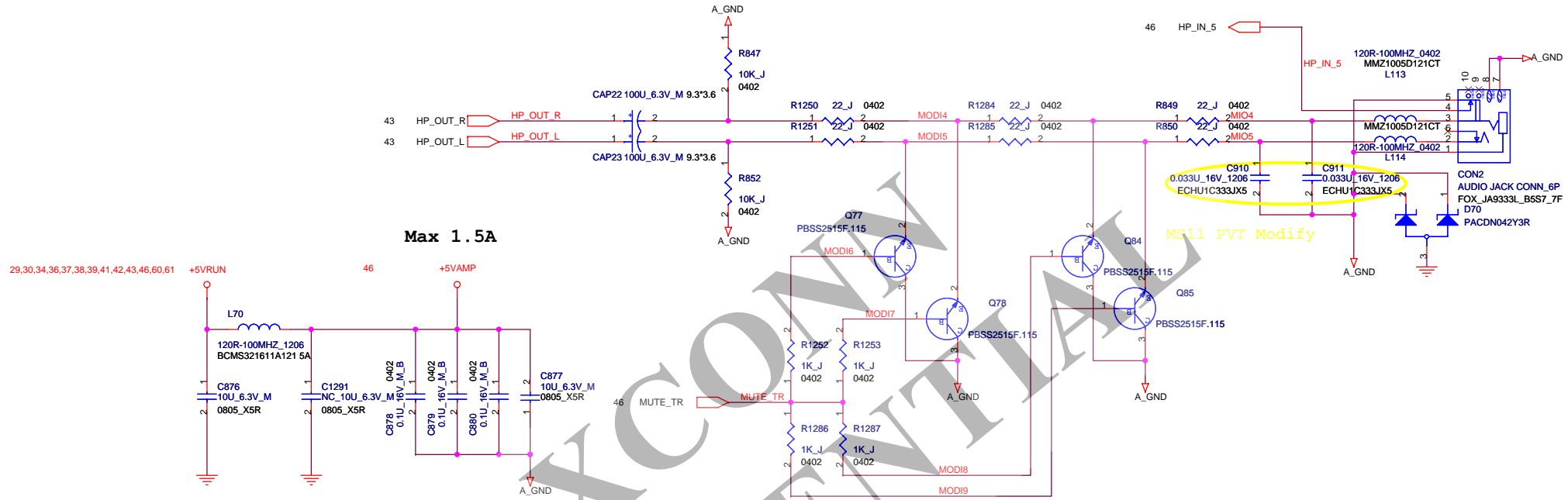


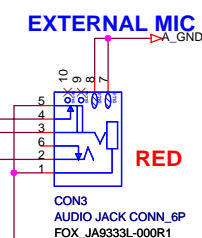
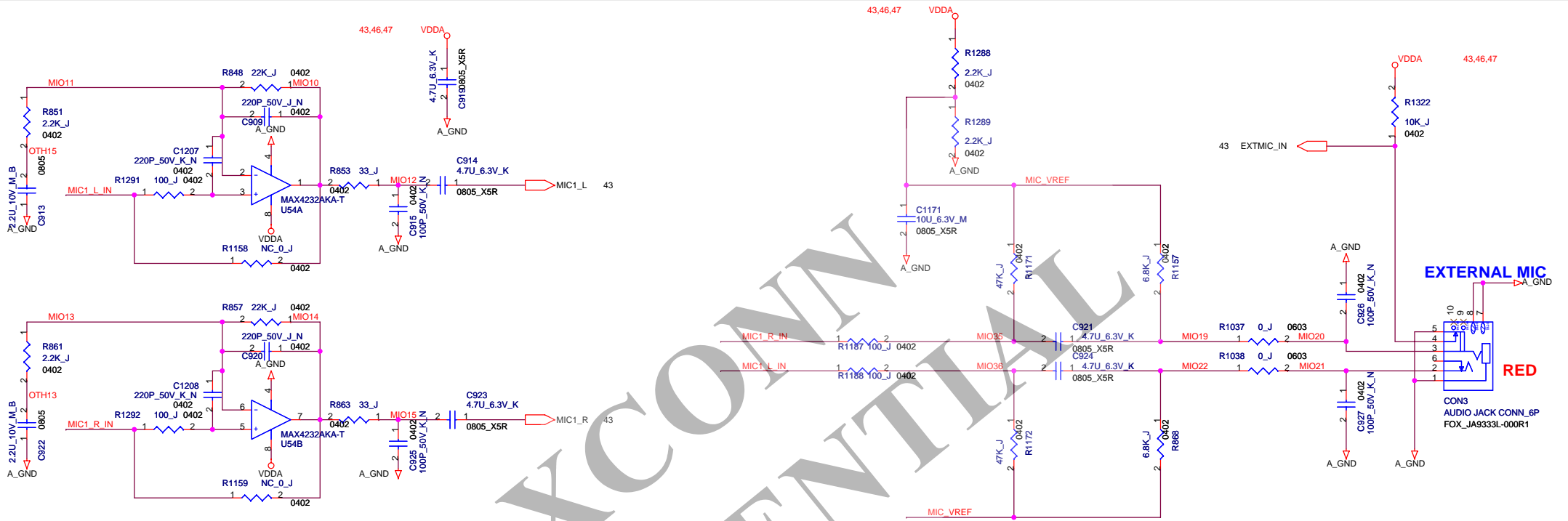
De1 R1446,R1447,R1448,R1449 (MS11 DVT)

AUDIO POWER(Change to 4.75V/200mA)



<b>FOXCONN</b>		
HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title	<b>AUDIO(CODEC &amp; POWER)</b>	
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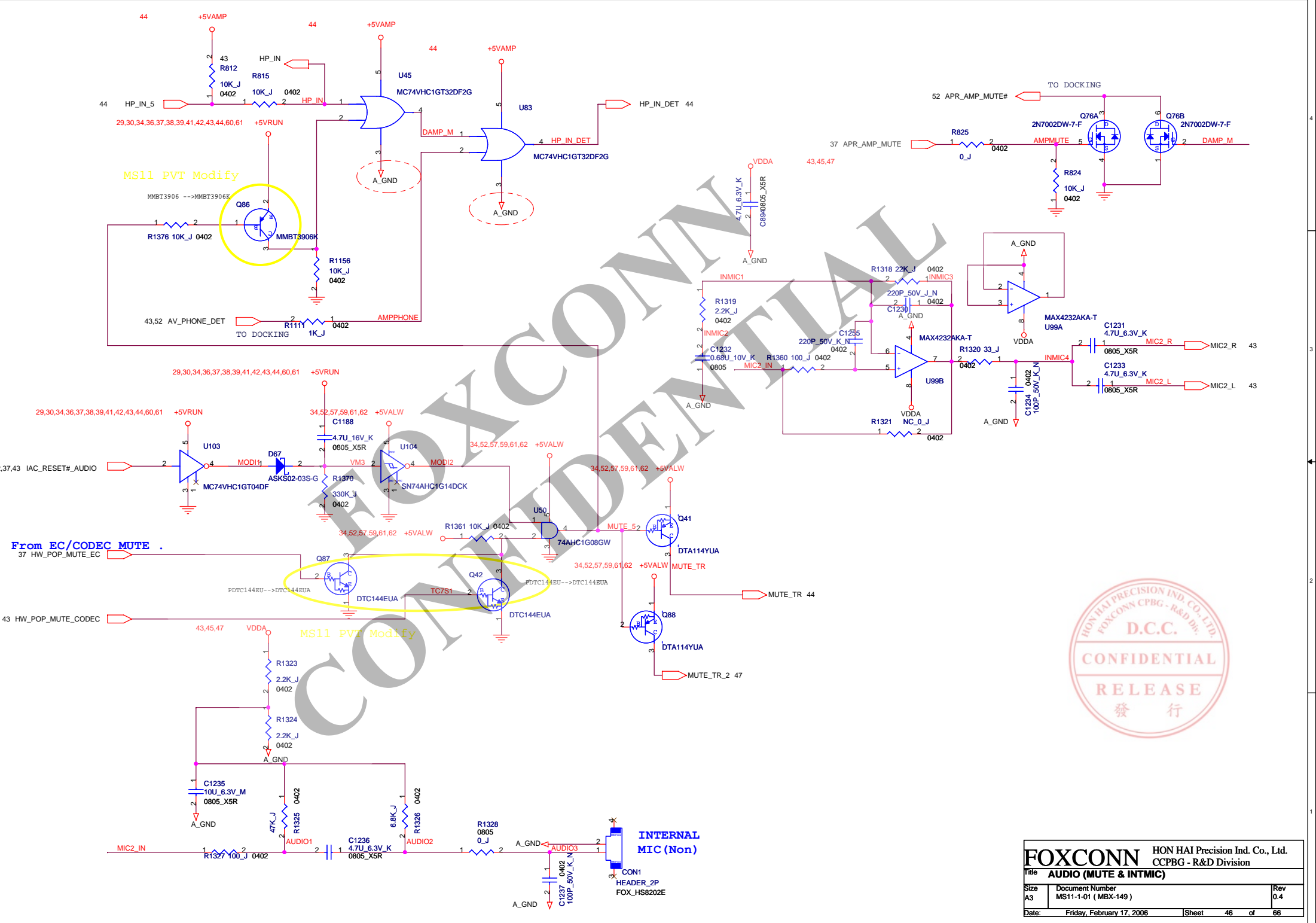




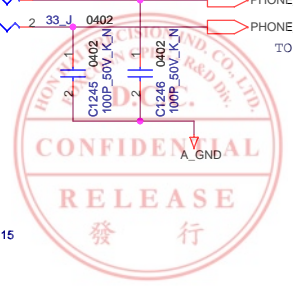
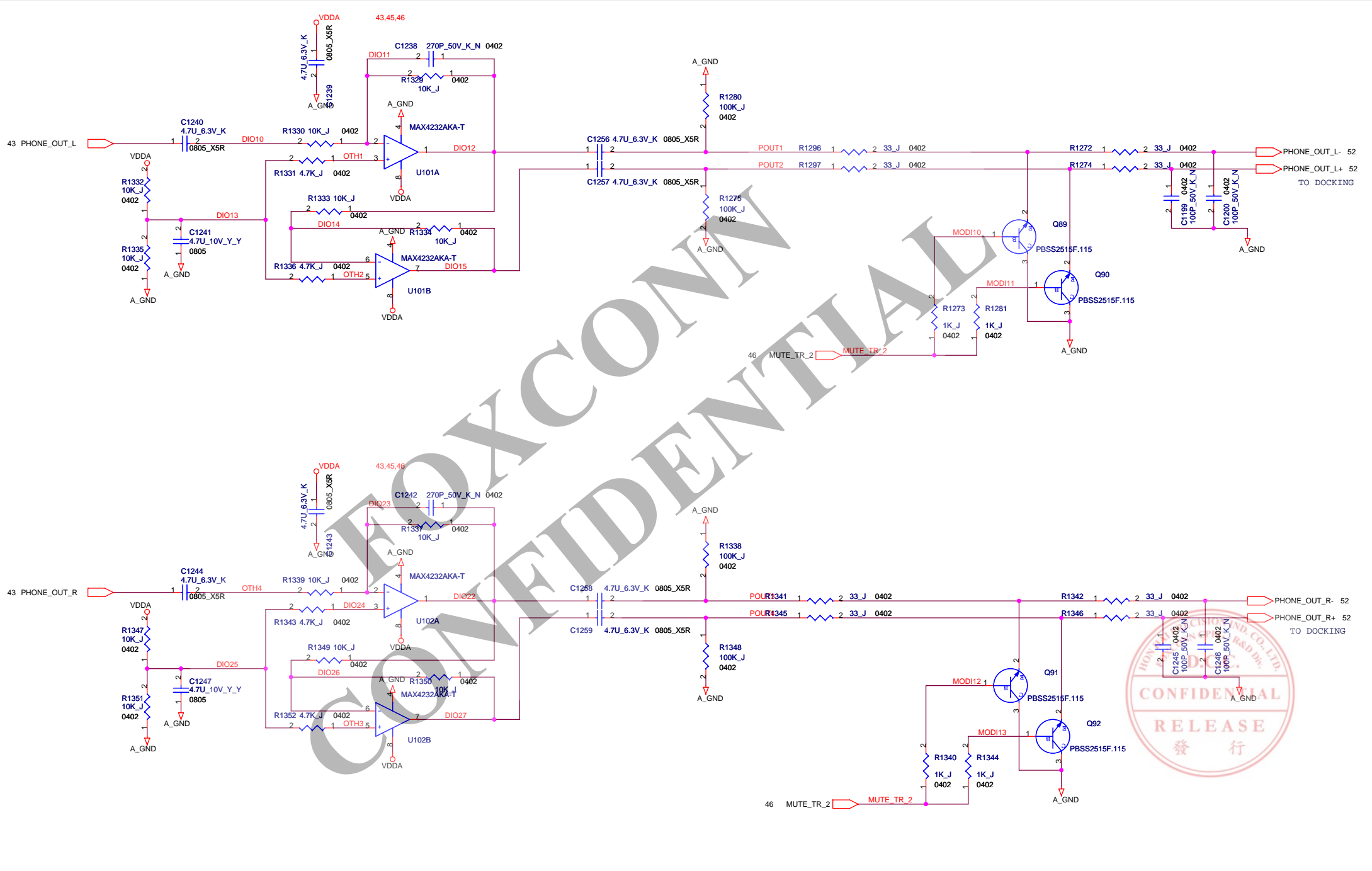
FOXC  
 CONFIDENTIAL



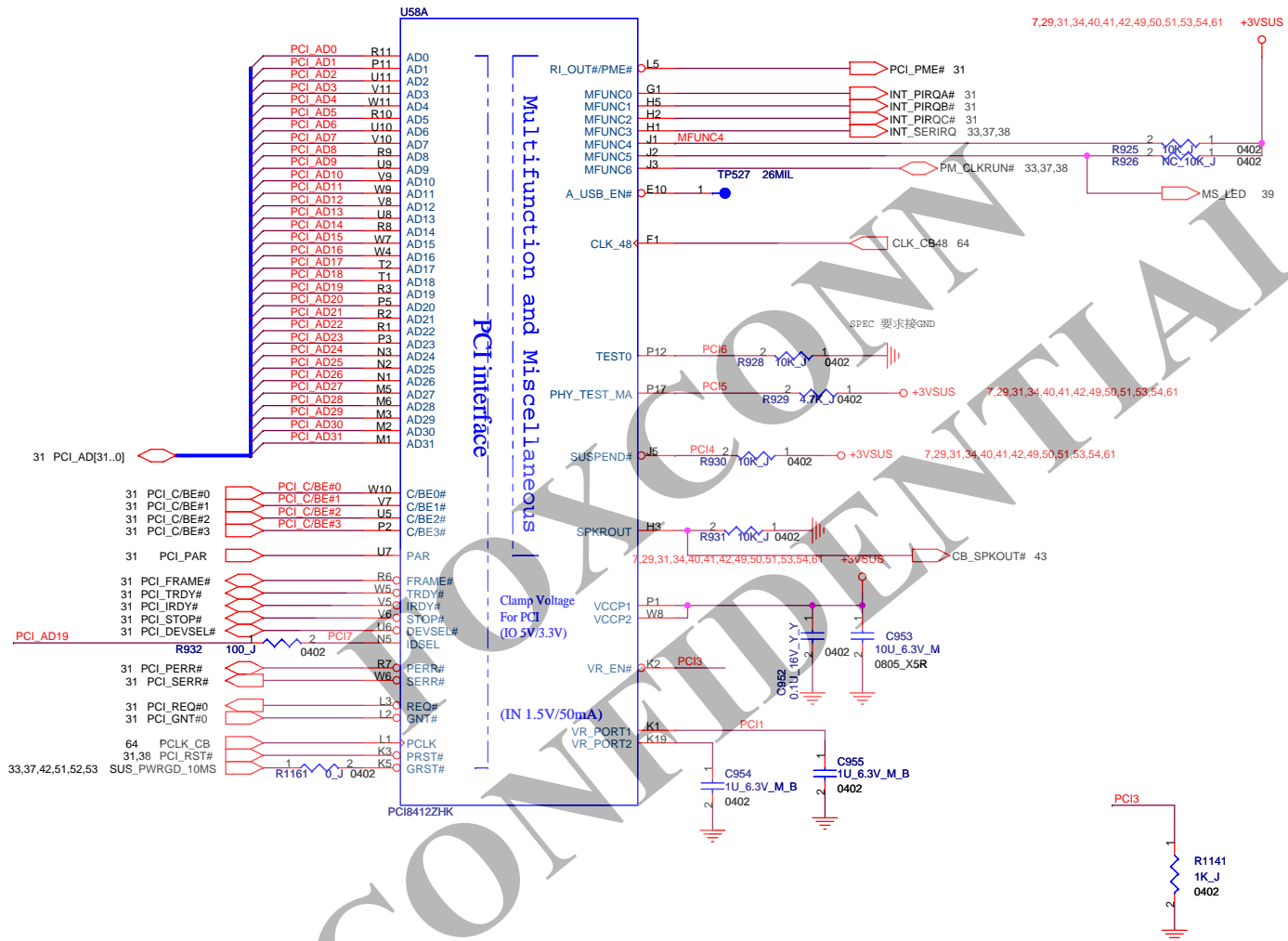
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>AUDIO( EXT MIC &amp; PHONE OUT)</b>			
Size	Document Number	Rev	
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<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>AUDIO (MUTE &amp; INTMIC)</b>		
Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.4
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7.29,31,34,40,41,42,48,50,51,53,54,61 +3VSUS  
 This array must be placed close to VDPLL (Pin U19)  
 They must be tied to a low-impedance GND.

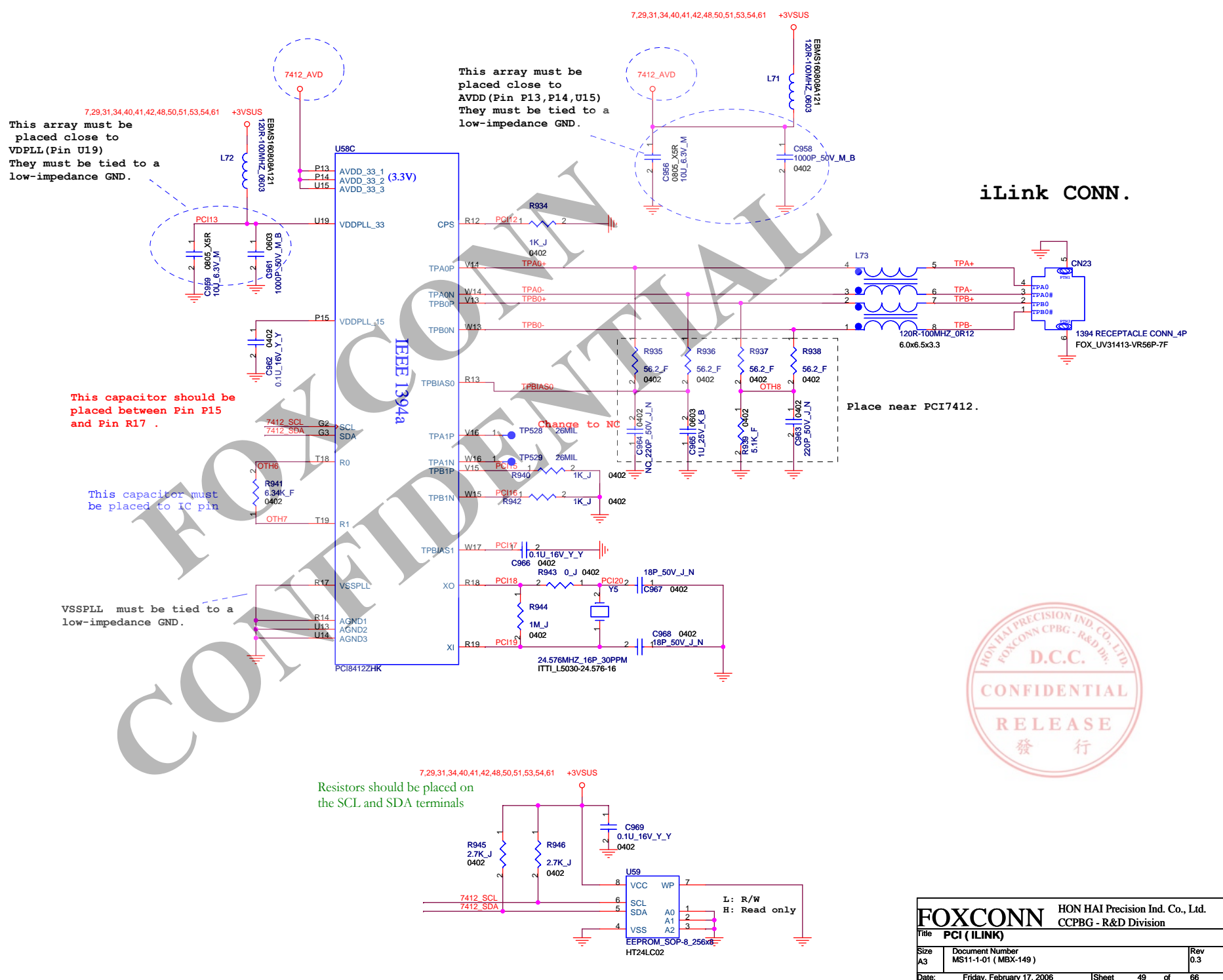
This array must be placed close to AVDD (Pin P13,P14,U15)  
 They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

Resistors should be placed on the SCL and SDA terminals

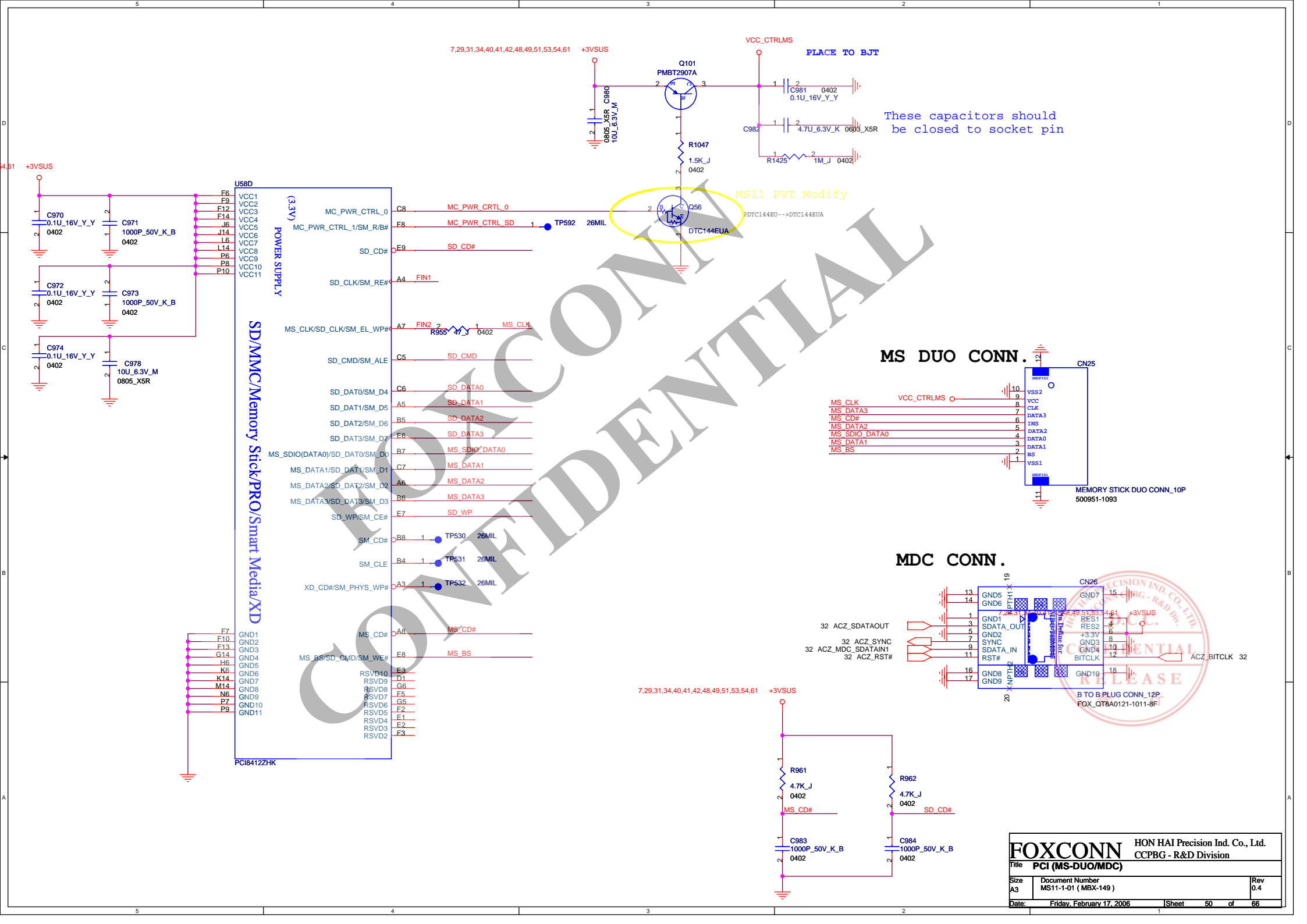


iLink CONN.

Place near PCI7412.



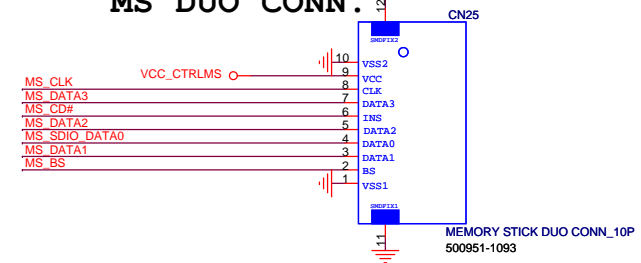
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>PCI (iLink)</b>	
Size A3	Document Number MS11-1-01 ( MBX-149)
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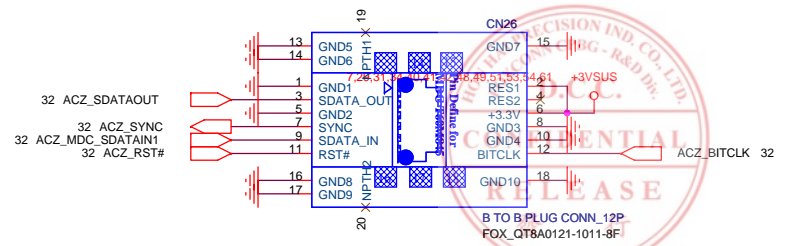
These capacitors should be closed to socket pin

MS11 PVT Modify

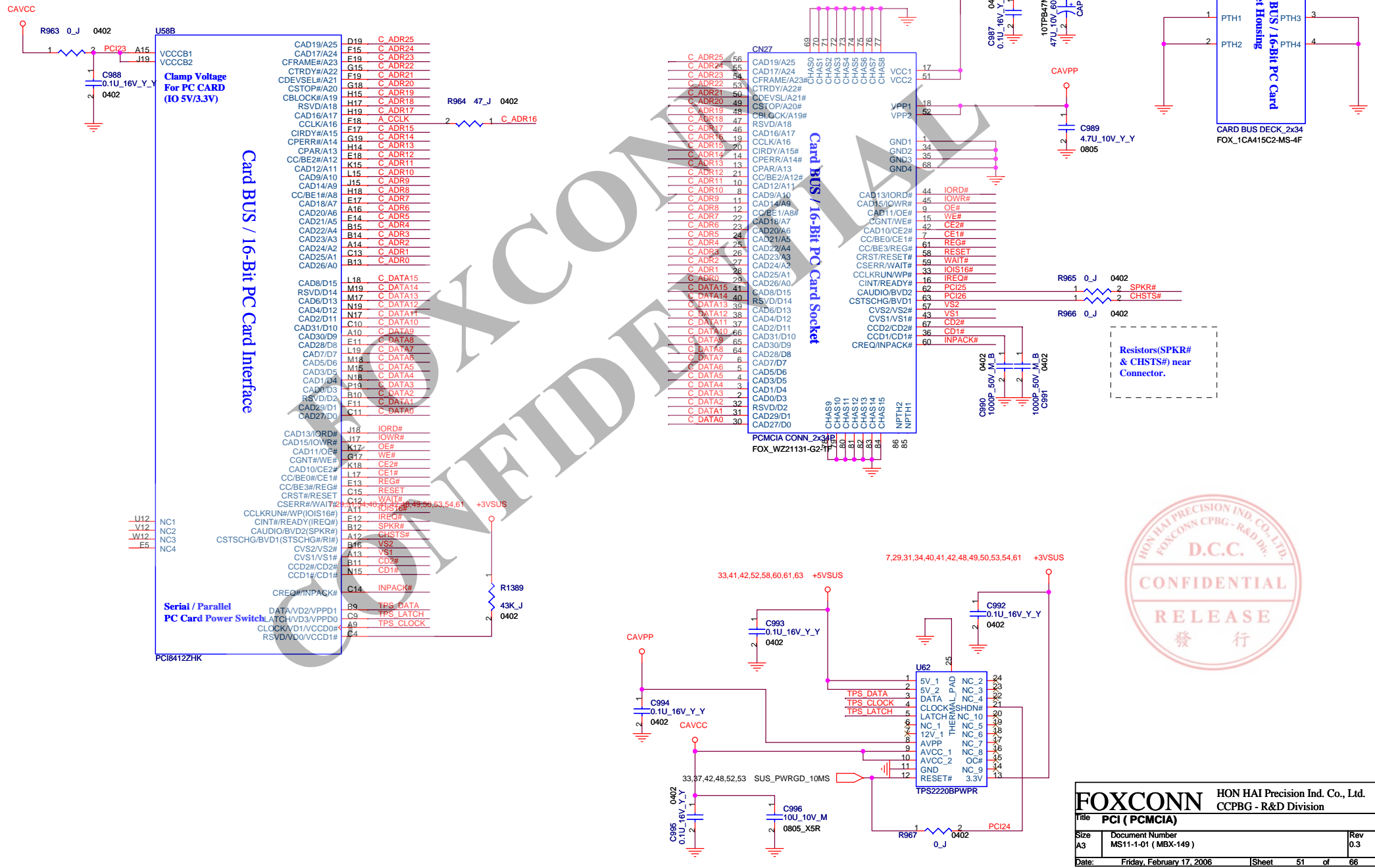
**MS DUO CONN.**



**MDC CONN.**



# PCMCIA CONN.



Card BUS / 16-Bit PC Card Interface

Clamp Voltage For PC CARD (IO 5V/3.3V)

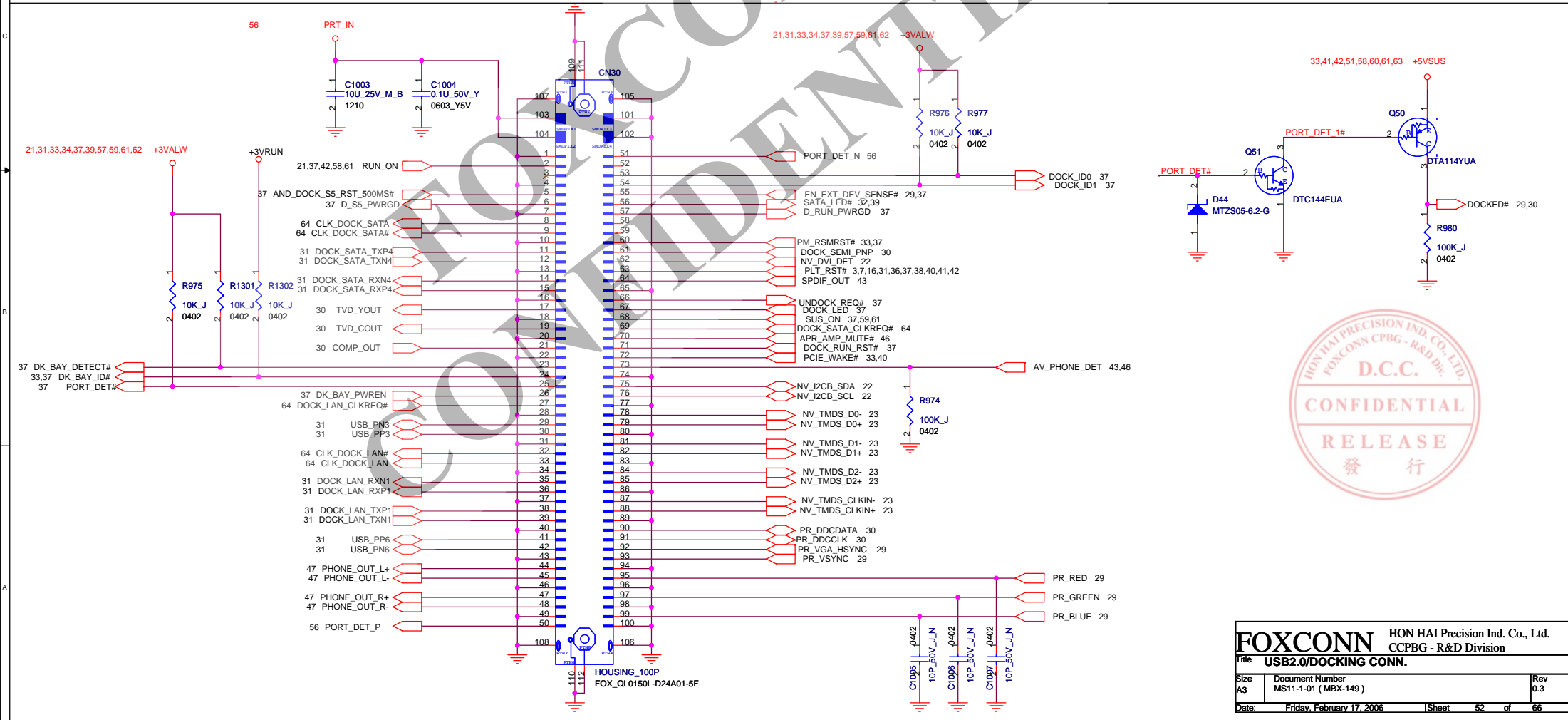
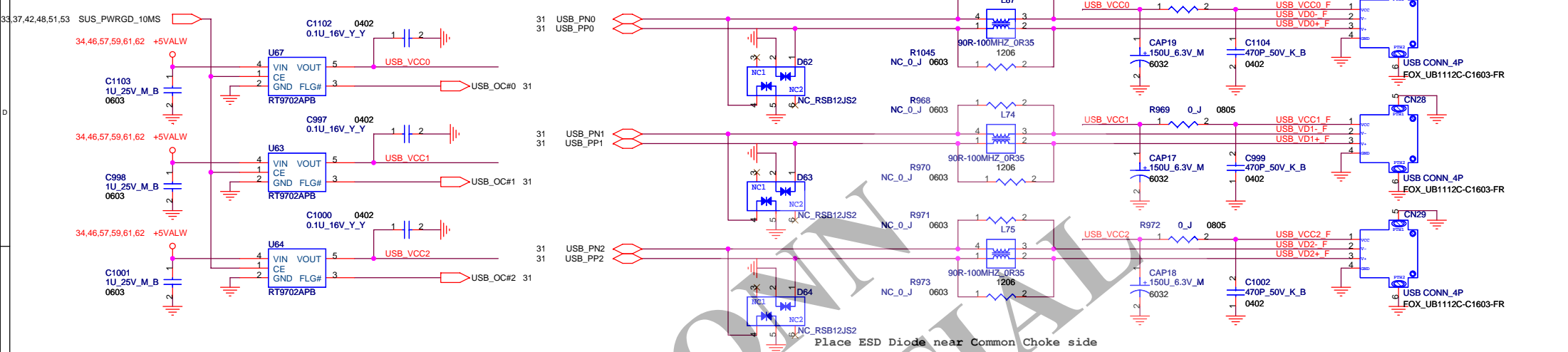
Serial / Parallel PC Card Power Switch

Resistors (SPKR# & CHSTS#) near Connector.



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>PCI (PCMCIA)</b>	
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# USB CONN X 3



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>USB2.0/DOCKING CONN.</b>		
Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.3
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BOM notice:

	R1243	R1244	R1247	R1248	R1459	R1460
BT + OIDE SKU	NC	NC	NC	NC	NC	NC
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm	NC	NC
OIDE SKU	0 ohm	0 ohm	NC	NC	0 ohm	0 ohm

BOM notice:

	R1194	R1195
BT + OIDE SKU	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm

Layout note:

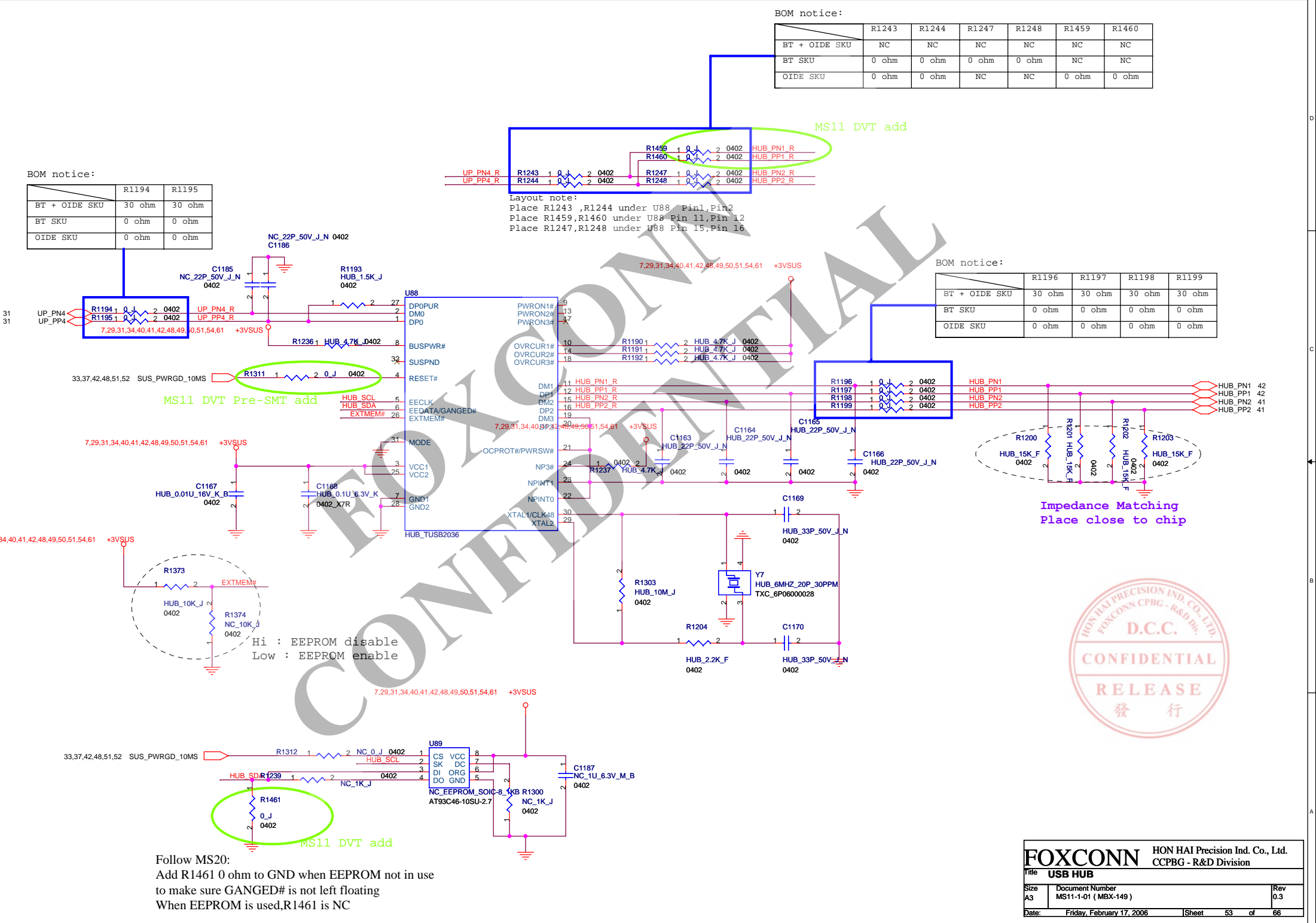
Place R1243 ,R1244 under U88 Pin1,Pin2  
 Place R1459,R1460 under U88 Pin 11,Pin 12  
 Place R1247,R1248 under U88 Pin 15,Pin 16

MS11 DVT add

BOM notice:

	R1196	R1197	R1198	R1199
BT + OIDE SKU	30 ohm	30 ohm	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm	0 ohm	0 ohm

Impedance Matching  
Place close to chip

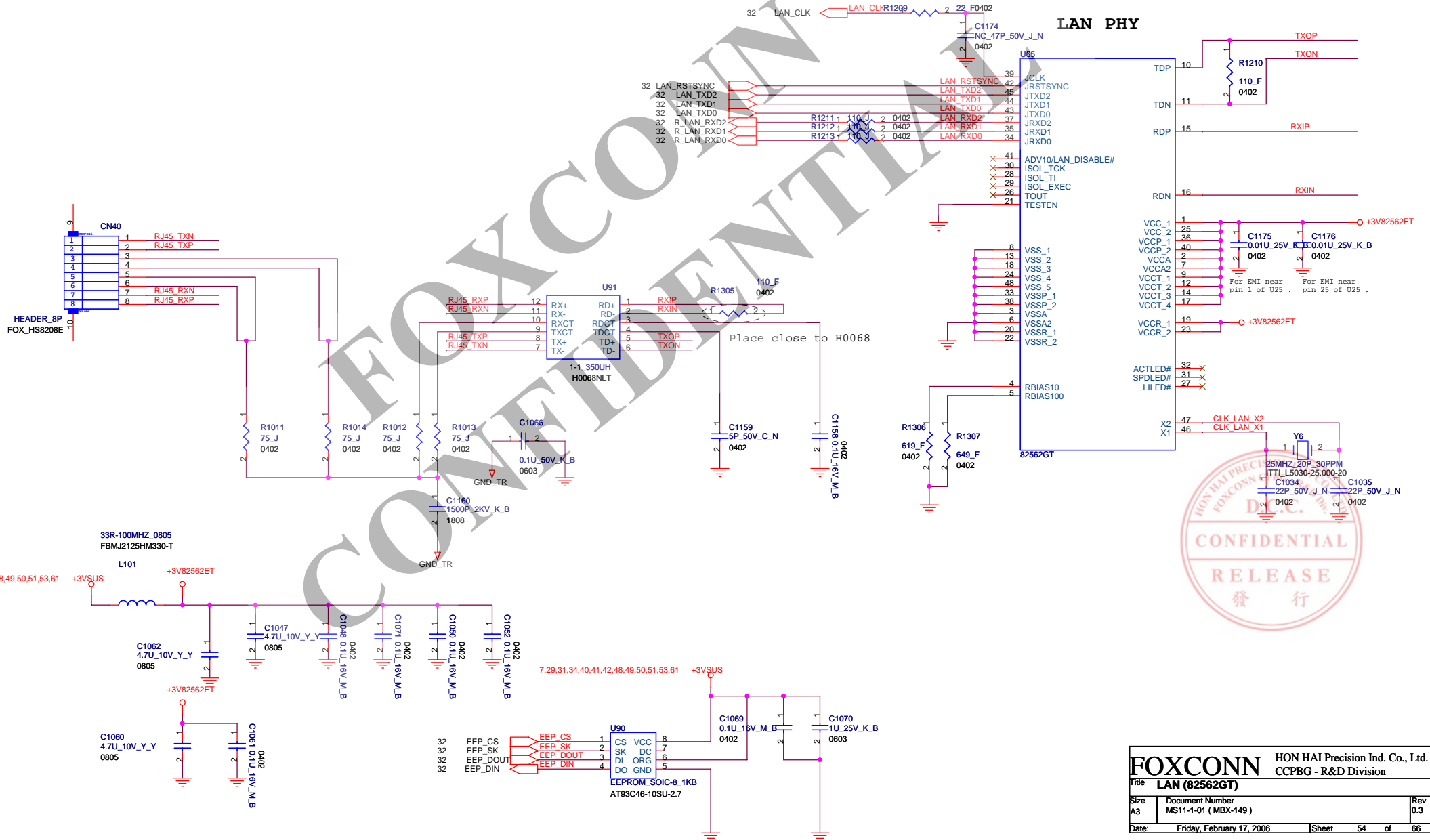


Follow MS20:  
 Add R1461 0 ohm to GND when EEPROM not in use  
 to make sure GANGED# is not left floating  
 When EEPROM is used,R1461 is NC

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Title **USB HUB**

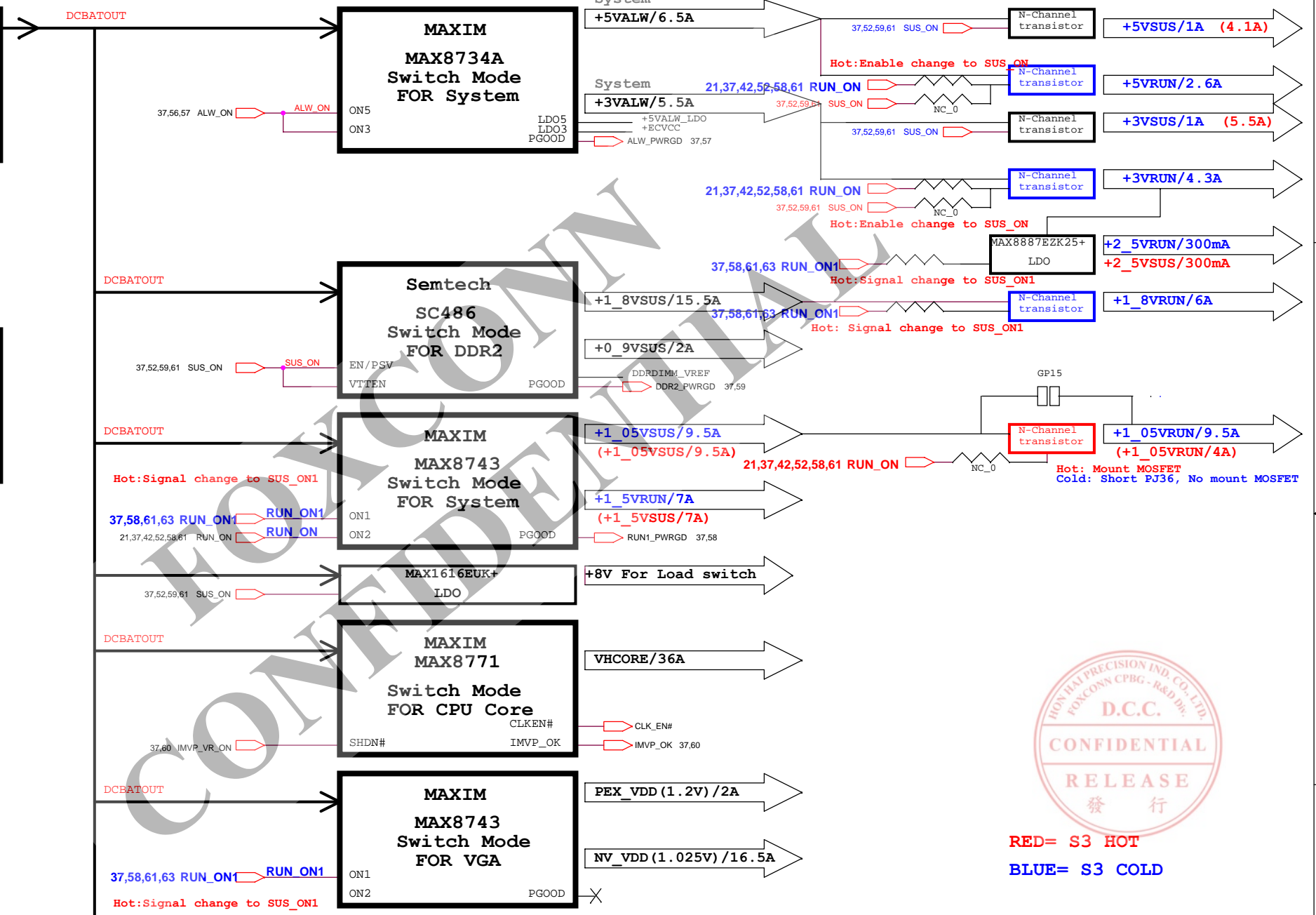
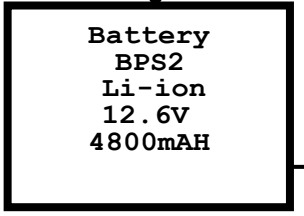
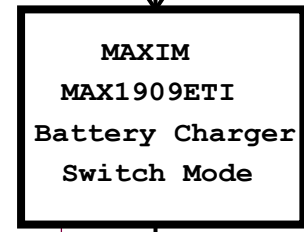
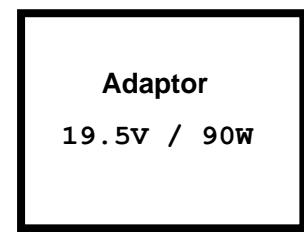
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**LAN PHY**

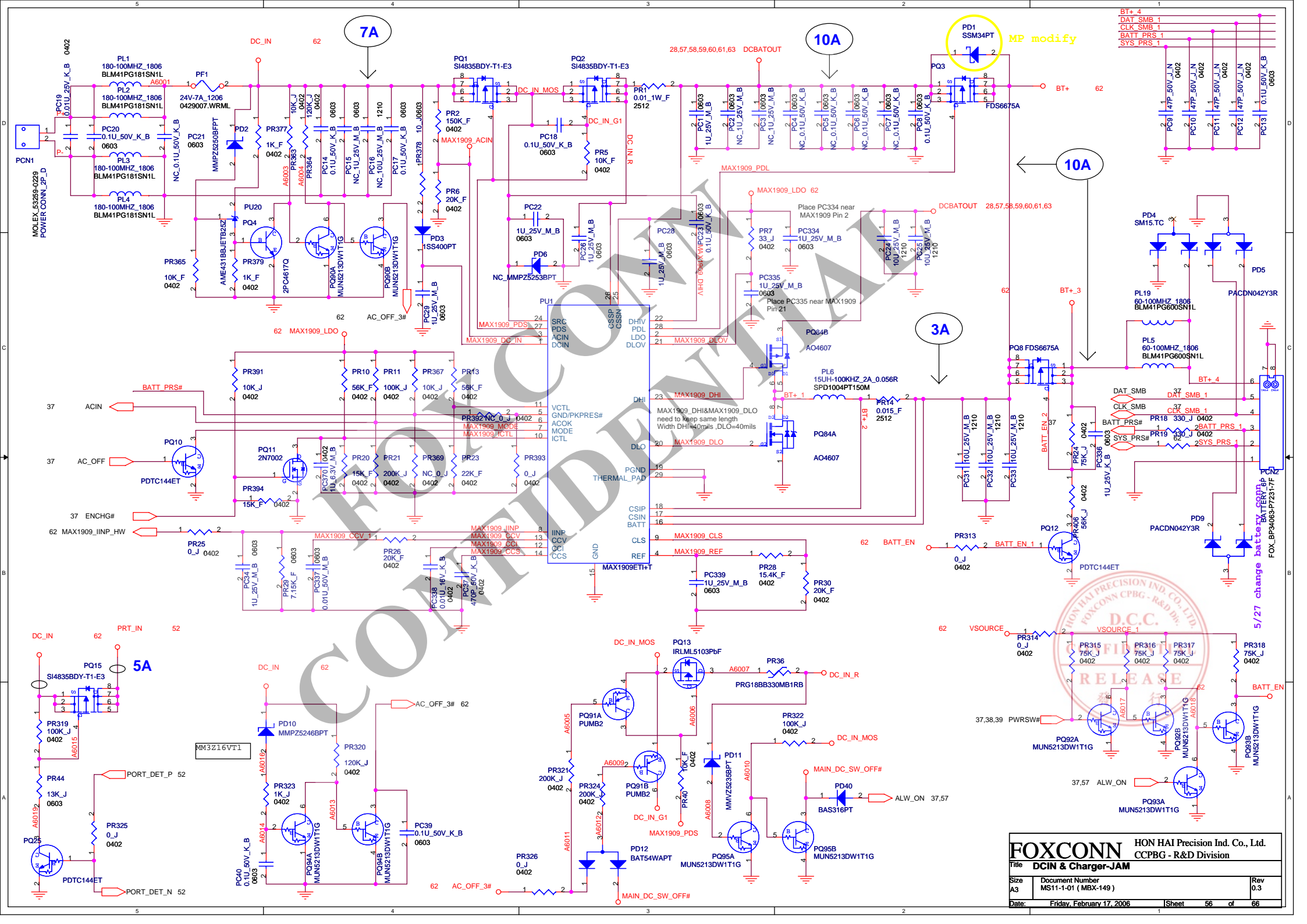


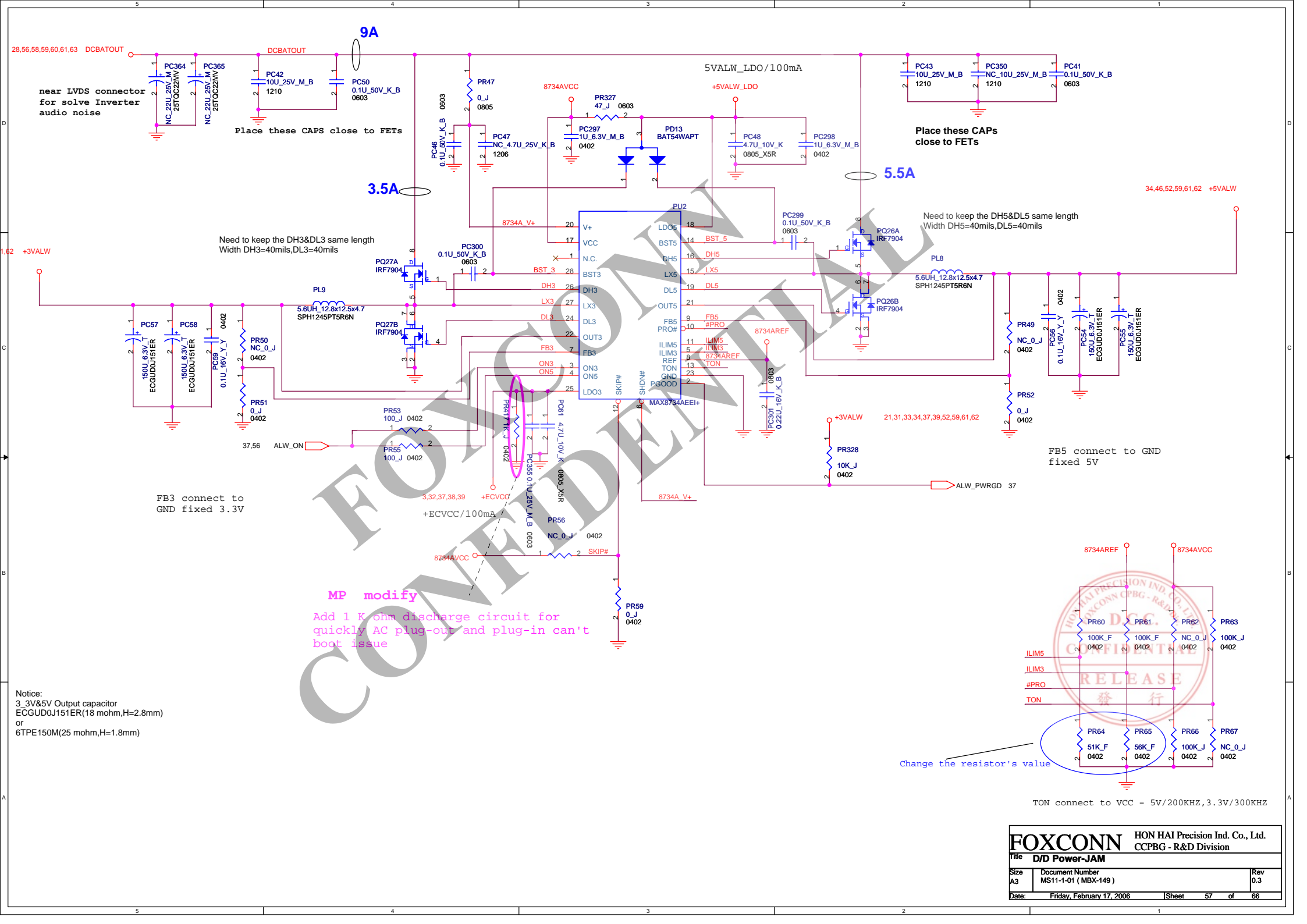
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>LAN (82562GT)</b>		
Size A3	Document Number MS11-1-01 (MBX-149)	Rev 0.3
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RED= S3 HOT  
BLUE= S3 COLD







28,56,58,59,60,61,63 DCBATOUT

near LVDS connector  
for solve Inverter  
audio noise

Place these CAPS close to FETs

Place these CAPS  
close to FETs

Need to keep the DH3&DL3 same length  
Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length  
Width DH5=40mils,DL5=40mils

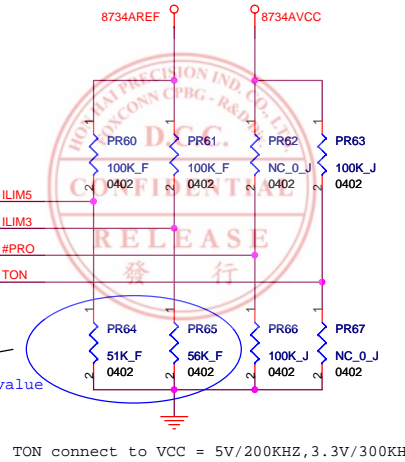
FB3 connect to  
GND fixed 3.3V

FB5 connect to GND  
fixed 5V

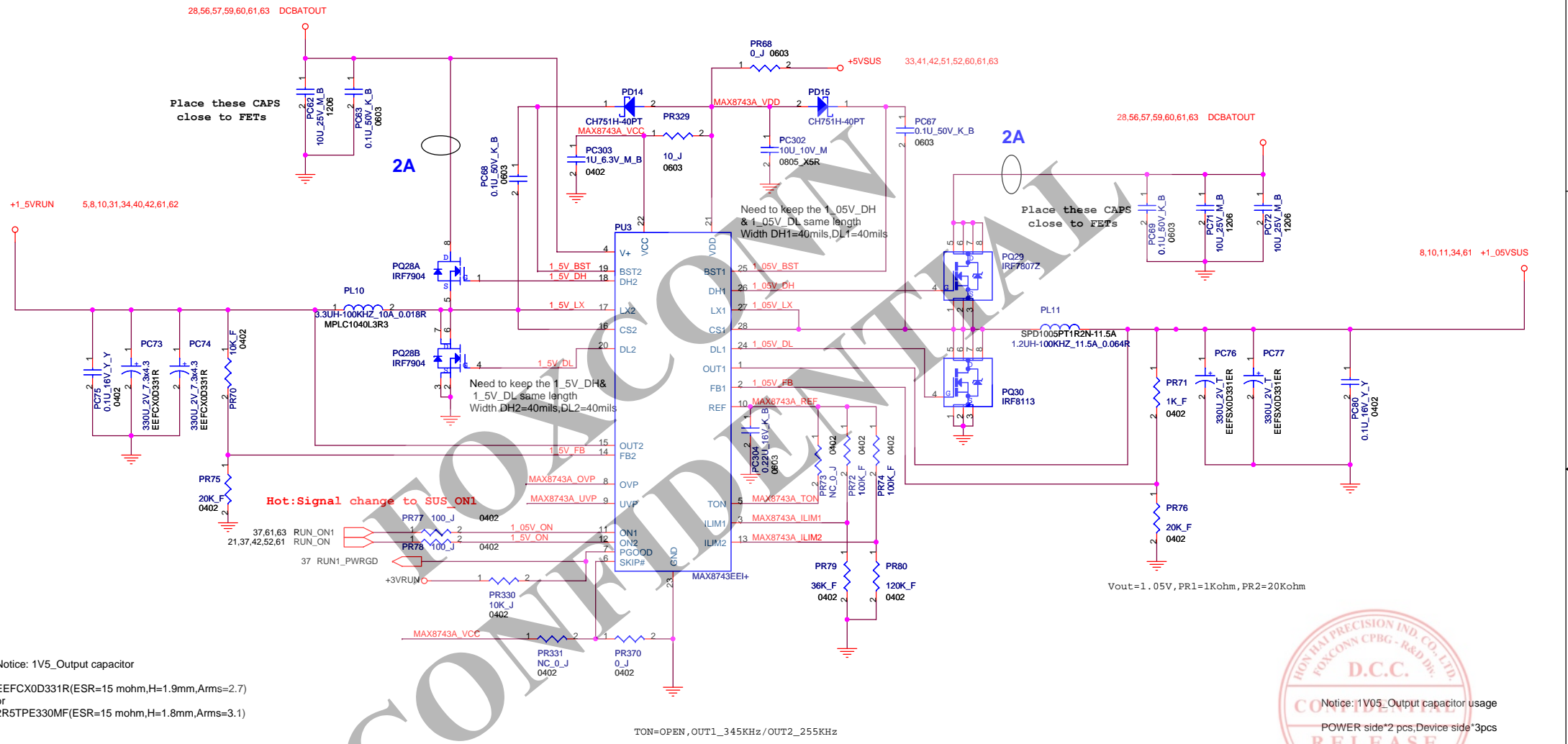
MP modify  
Add 1 K ohm discharge circuit for  
quickly AC plug-out and plug-in can't  
boot issue

Change the resistor's value

Notice:  
3\_3V&5V Output capacitor  
ECGUD0J151ER(18 mohm,H=2.8mm)  
or  
6TPE150M(25 mohm,H=1.8mm)



TON connect to VCC = 5V/200KHZ, 3.3V/300KHZ

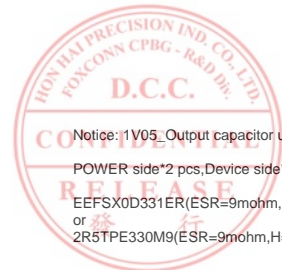
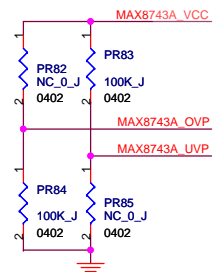


Notice: 1V5\_ Output capacitor

EEFCX0D331R (ESR=15 mohm, H=1.9mm, Arms=2.7)  
 or  
 2R5TPE330MF (ESR=15 mohm, H=1.8mm, Arms=3.1)

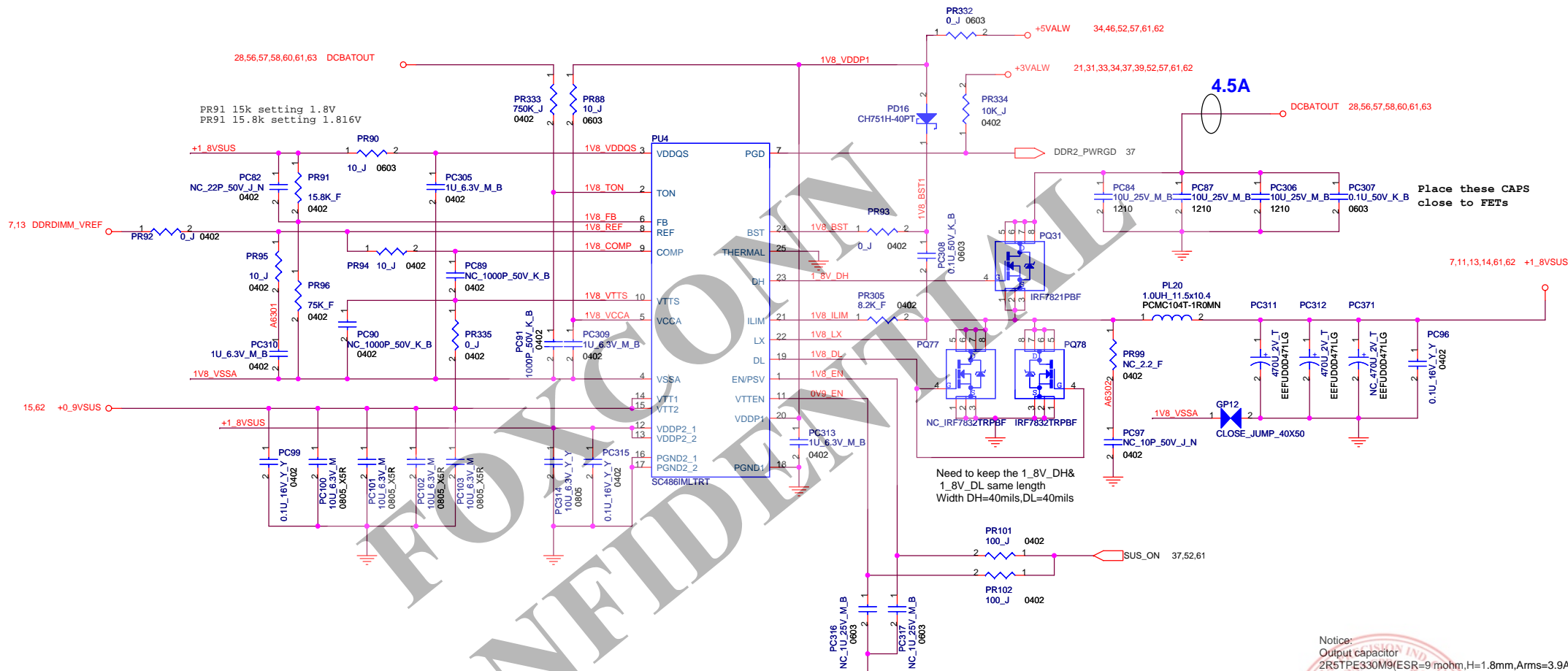
TON=OPEN, OUT1\_345KHz / OUT2\_255KHz

Vout=1.05V, PR1=1Kohm, PR2=20Kohm



Notice: 1V05\_ Output capacitor usage  
 POWER side\*2 pcs, Device side\*3pcs  
 EEFCX0D331ER (ESR=9mohm, H=1.9mm, Arms=3.0A)  
 or  
 2R5TPE330M9 (ESR=9mohm, H=1.8mm, Arms=3.9A)

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>1.5V/1.05V-JAM</b>		
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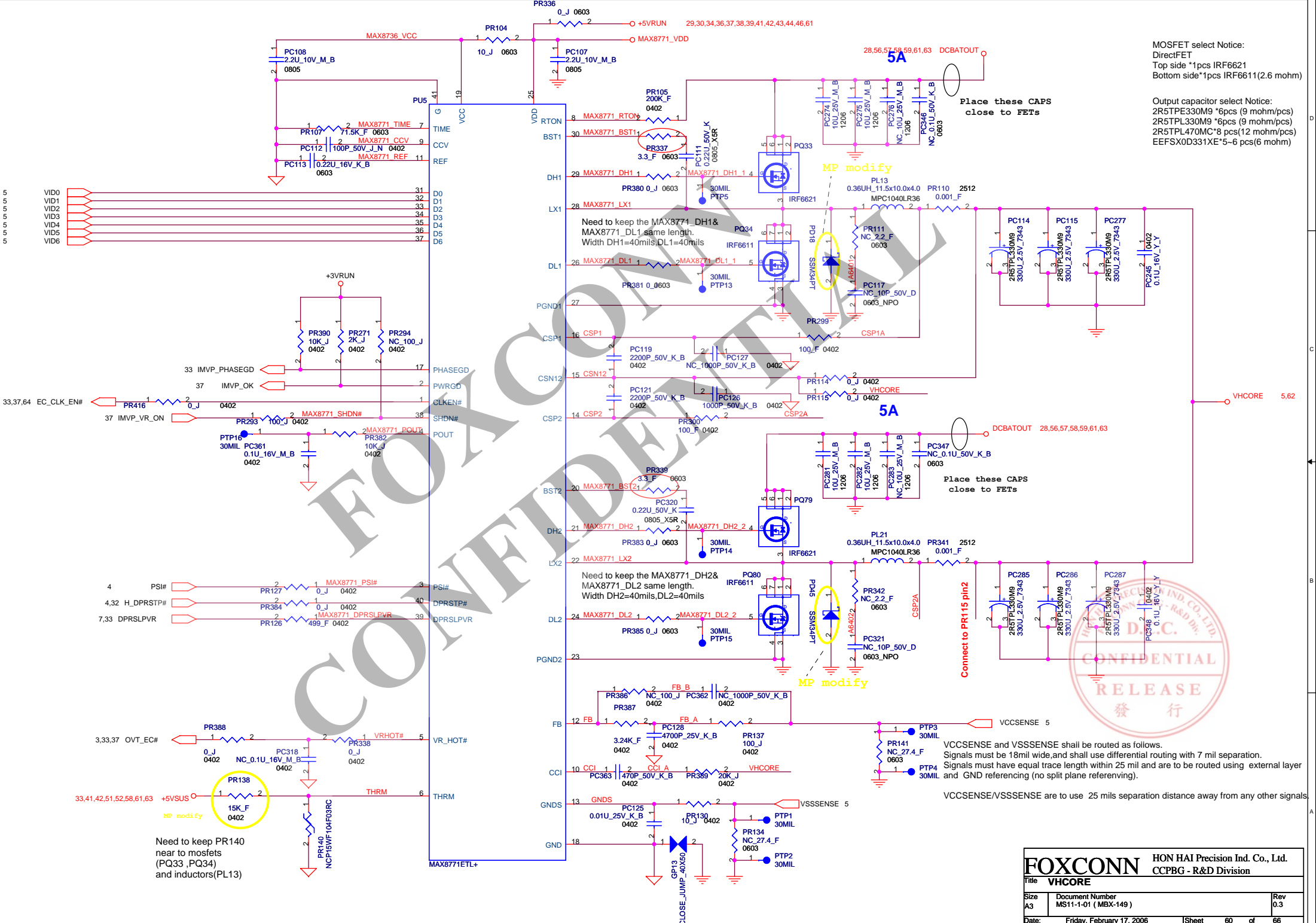
Place these CAPS close to FETs

Need to keep the 1.8V\_DH& 1.8V\_DL same length Width DH=40mils,DL=40mils

Notice:  
 Output capacitor  
 2R5TPE330M9(ESR=9 mohm,H=1.8mm,Arms=3.9A)  
 or  
 EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)

Bottom side MOSFET  
 IRF7832\*1 pcs(4 mohm/pcs)  
 or  
 IRF7811\*2 pcs(14 mohm/pcs)

發 行



MOSFET select Notice:  
 DirectFET  
 Top side \*1pcs IRF6621  
 Bottom side \*1pcs IRF6611(2.6 mohm)  
 Output capacitor select Notice:  
 2R5TP330M9 \*6pcs (9 mohm/pcs)  
 2R5TPL330M9 \*6pcs (9 mohm/pcs)  
 2R5TPL470MC \*8 pcs(12 mohm/pcs)  
 EEFSXD331XE\*5-6 pcs(6 mohm)

Place these CAPS  
 close to FETs

MP modify

Need to keep the MAX8771\_DH1 &  
 MAX8771\_DL1 same length.  
 Width DH1=40mils, DL1=40mils

Need to keep the MAX8771\_DH2 &  
 MAX8771\_DL2 same length.  
 Width DH2=40mils, DL2=40mils

MP modify

Connect to PR115 pin2

VCCSENSE and VSSSENSE shall be routed as follows.  
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.  
 Signals must have equal trace length within 25 mil and are to be routed using external layer  
 and GND referencing (no split plane referencing).

VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

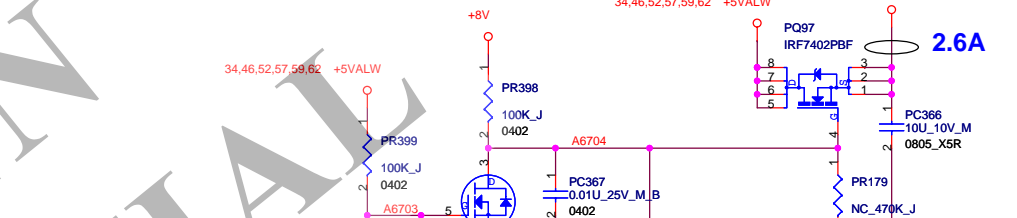
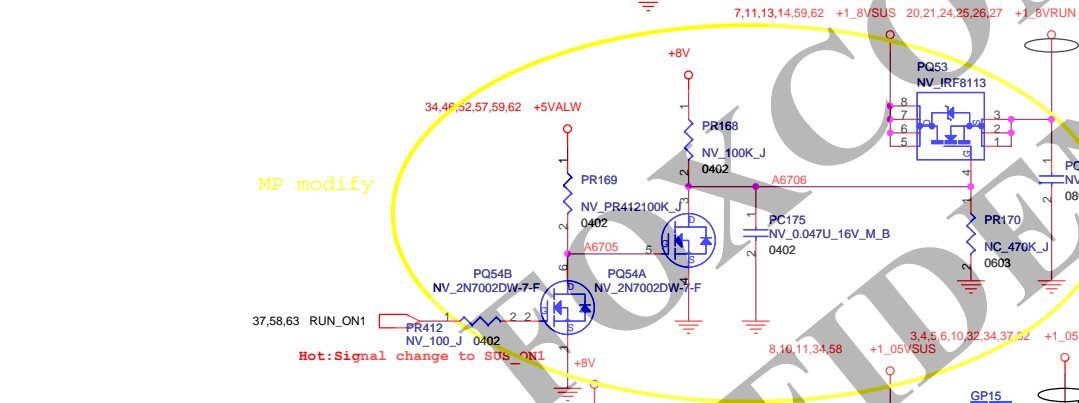
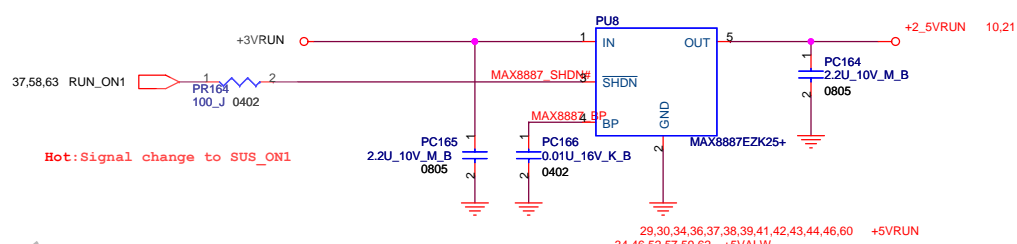
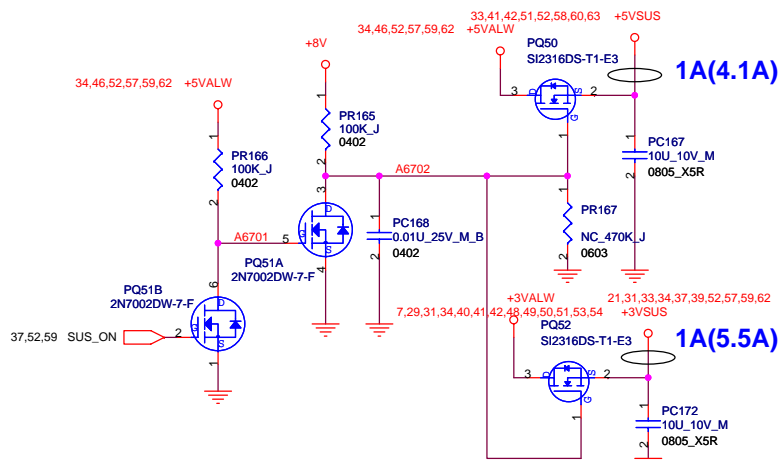
Need to keep PR140  
 near to mosfets  
 (PQ33, PQ34)  
 and inductors(PL13)

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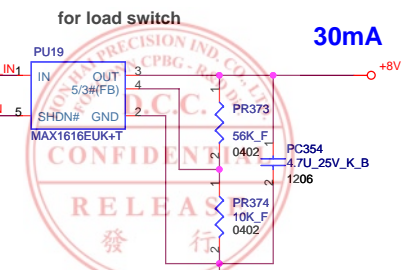
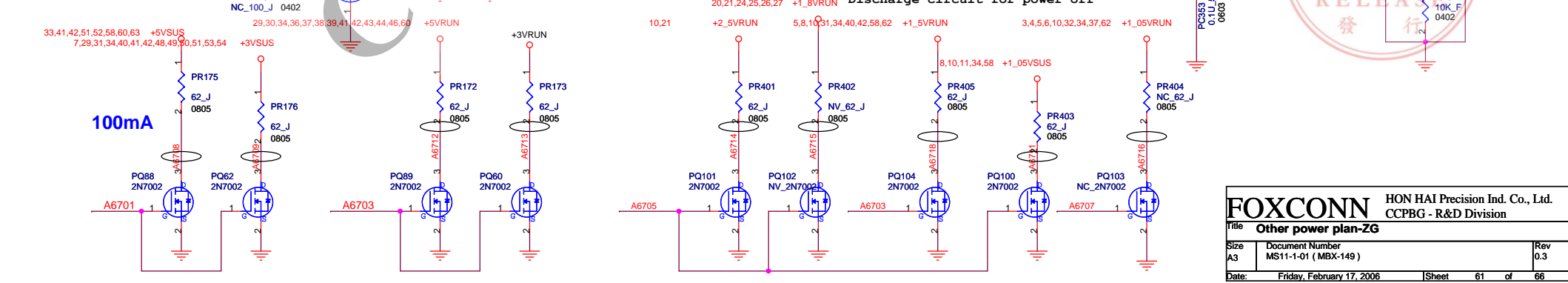
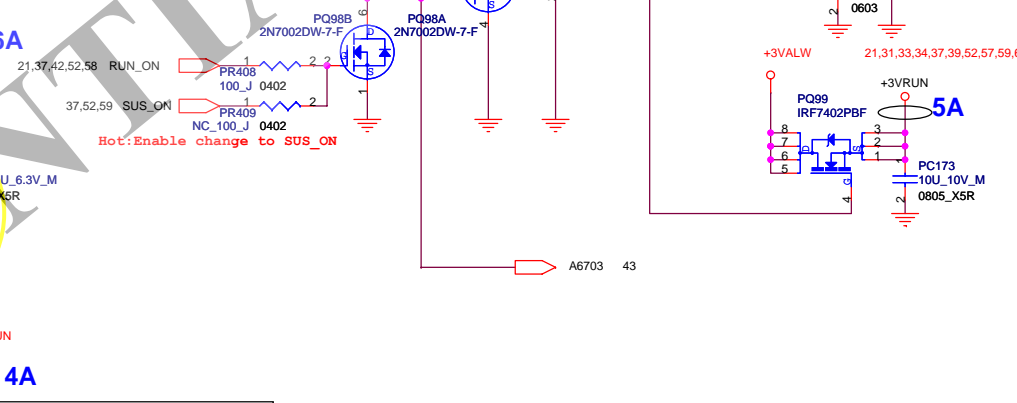
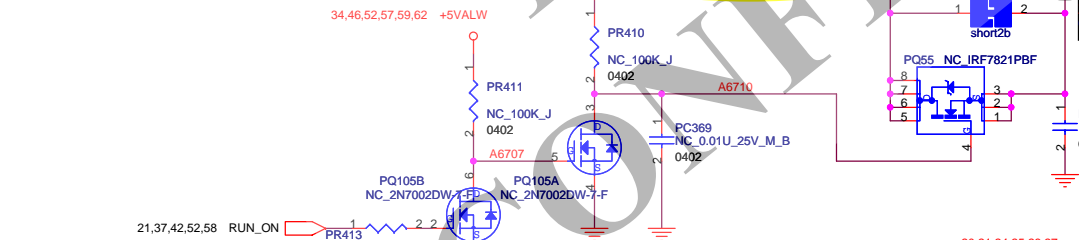
Title	VHCORE	
Size	Document Number	Rev
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300mA

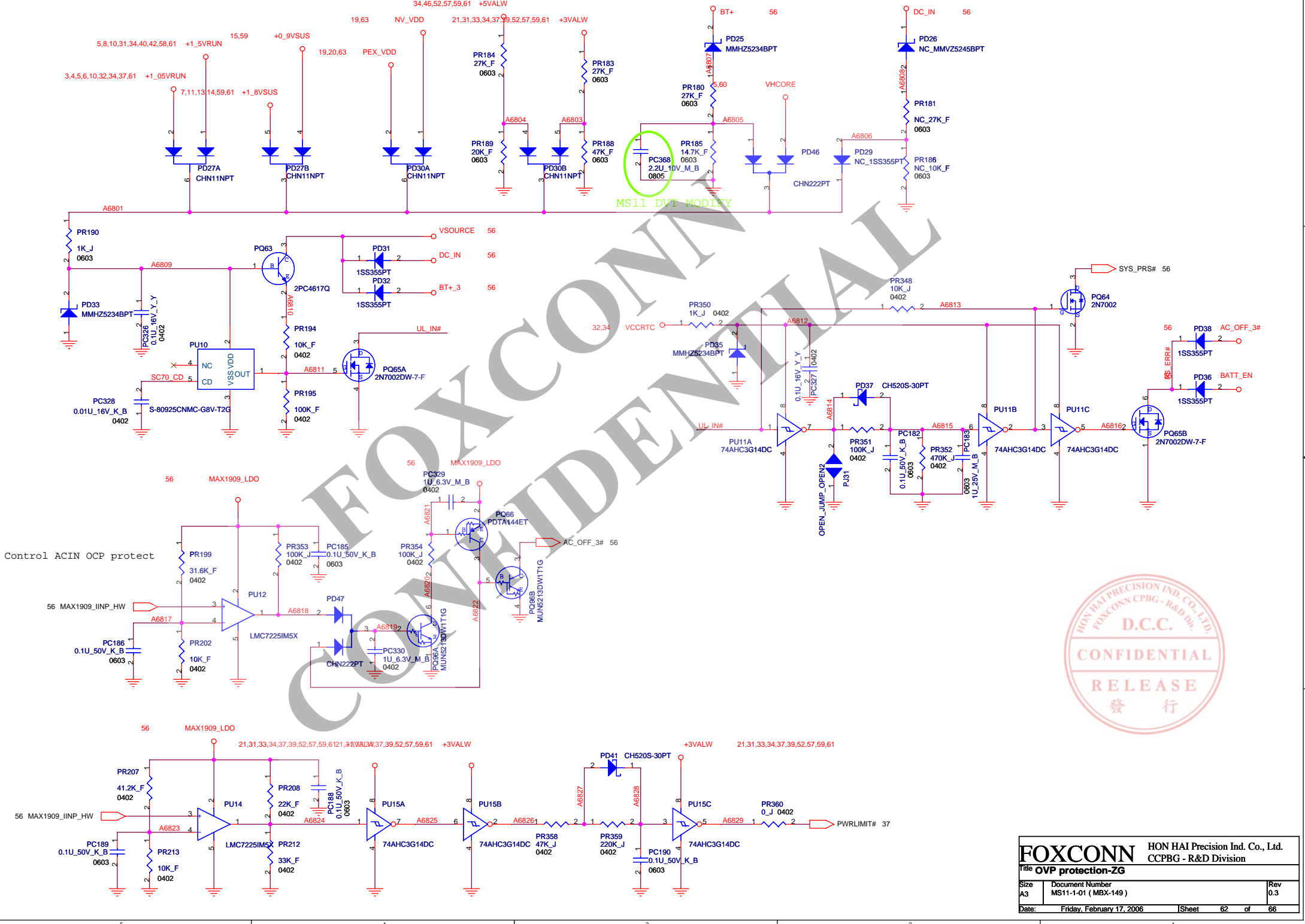
300mA



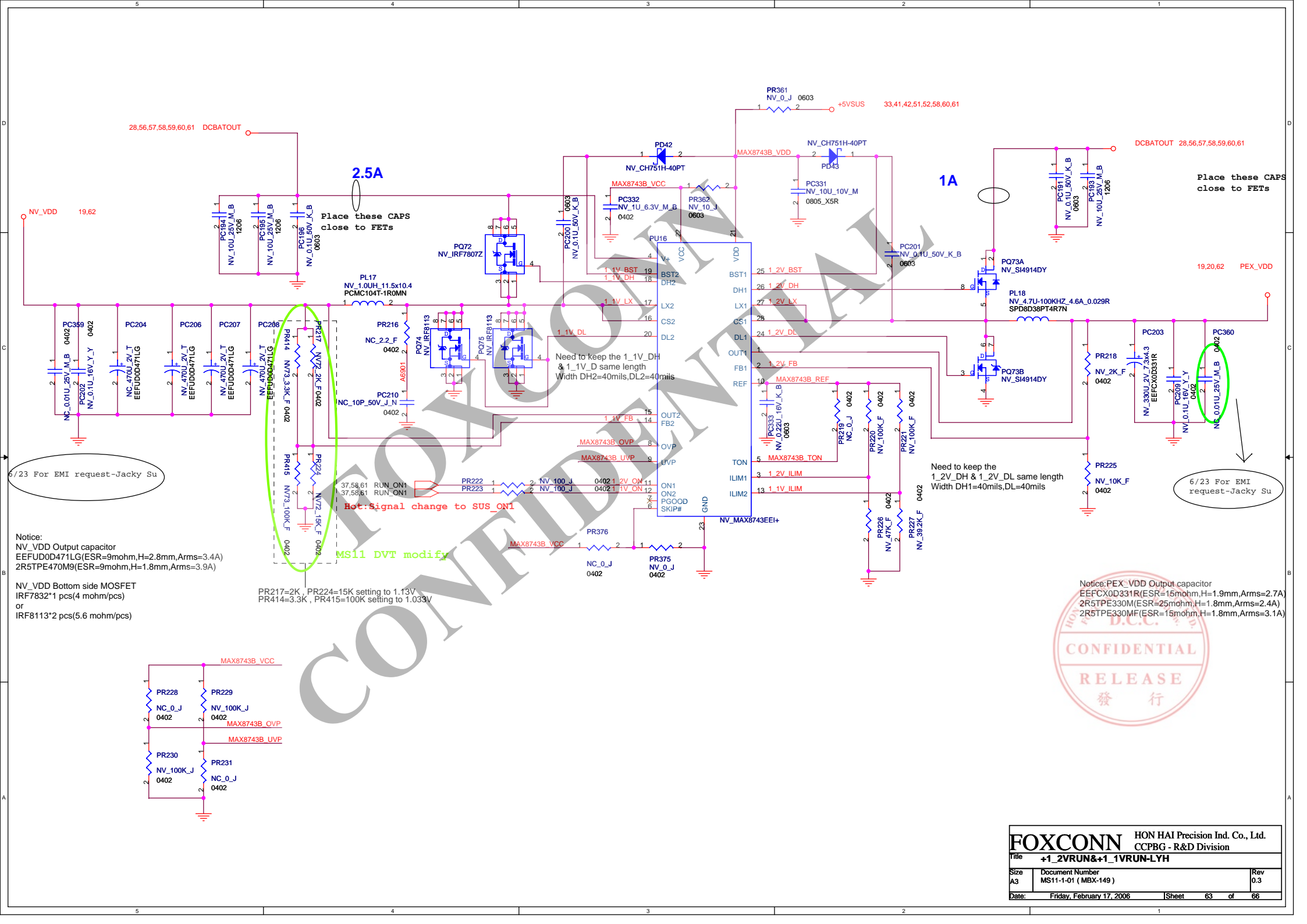
MP modify



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>Other power plan-ZG</b>		
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<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>OVP protection-ZG</b>		
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28,56,57,58,59,60,61 DCBATOUT

NV\_VDD 19,62

2.5A

Place these CAPS close to FETs

1A

DCBATOUT 28,56,57,58,59,60,61

Place these CAPS close to FETs

19,20,62 PEX\_VDD

Need to keep the 1\_1V\_DH & 1\_1V\_D same length Width DH2=40mils, DL2=40mils

Need to keep the 1\_2V\_DH & 1\_2V\_DL same length Width DH1=40mils, DL=40mils

6/23 For EMI request-Jacky Su

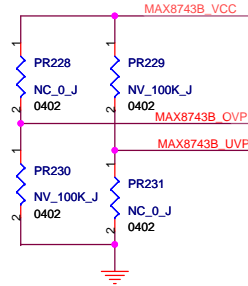
6/23 For EMI request-Jacky Su

Notice:  
NV\_VDD Output capacitor  
EEFUD0D471LG (ESR=9mohm, H=2.8mm, Arms=3.4A)  
2R5TPE470M9 (ESR=9mohm, H=1.8mm, Arms=3.9A)

NV\_VDD Bottom side MOSFET  
IRF7832\*1 pcs (4 mohm/pcs)  
or  
IRF8113\*2 pcs (5.6 mohm/pcs)

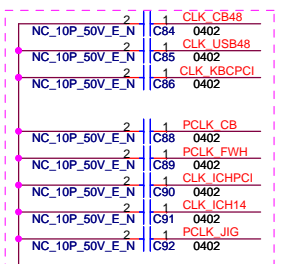
PR217=2K, PR224=15K setting to 1.13V  
PR414=3.3K, PR415=100K setting to 1.033V

Notice: PEX\_VDD Output capacitor  
EEFCX0D331R (ESR=15mohm, H=1.9mm, Arms=2.7A)  
2R5TPE330M (ESR=25mohm, H=1.8mm, Arms=2.4A)  
2R5TPE330MF (ESR=15mohm, H=1.8mm, Arms=3.1A)

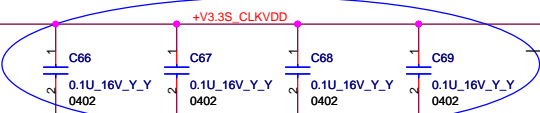


<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>+1_2VRUN&amp;+1_1VRUN-LYH</b>		
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06/17  
DEL 0 ohm resistor R38,R47,R50,  
0.1u Cap C71 C64  
10u Cap C72  
Cap C78 changed to 0.1u

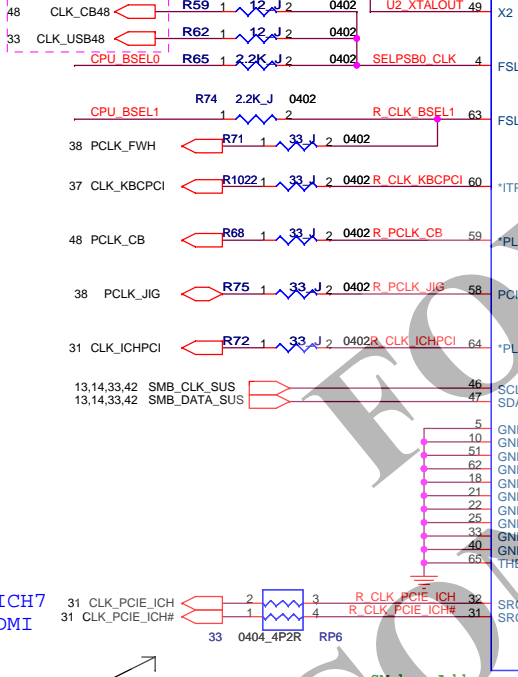


6/17  
Layout note:  
Place 1 cap close  
to each pin

Pin Straps	
Pin 53/59/60/64 100K ohm pull-up	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin 59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin 60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin 64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCCLK1 (NV)

close to clk gen (For EMI)

Length as short  
as possible.

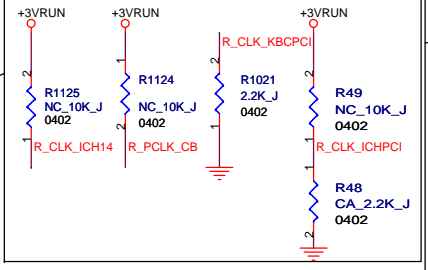


CALISTOGA Chip  
HOST

CPU

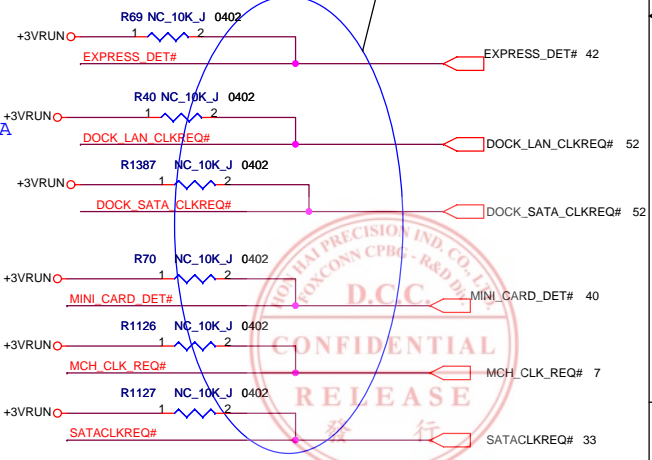
Nvidia  
Graphic

CALISTOGA  
DOT96



06/16  
pin53/59/60/64 with internal  
pull-up resistor  
No Stuff Pull-up Resistor  
(R1125,R1124,R49)  
If EVT ok, del them in DVT  
R1021/R48 changed to 2.2Kohm

06/09  
CLKREQ with internal pull-up resistor  
No Stuff Pull-up Resistor  
(R69,R40,R41,R70,R1126,R1127)  
If EVT ok, del them in DVT

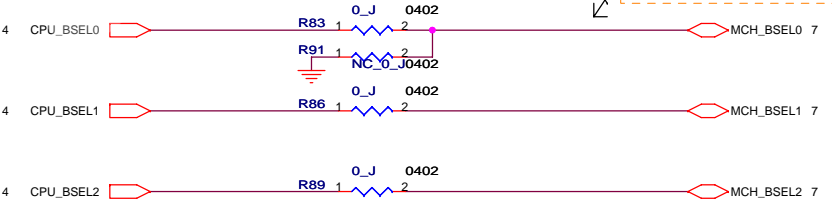


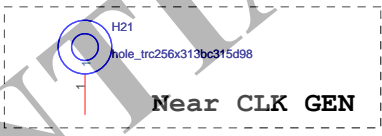
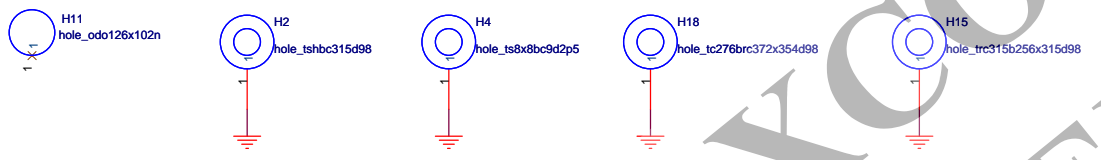
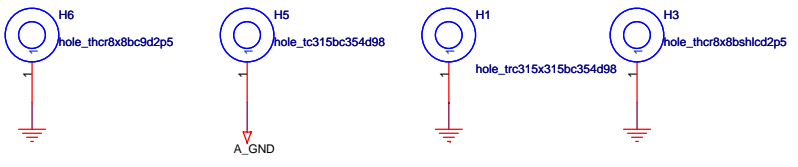
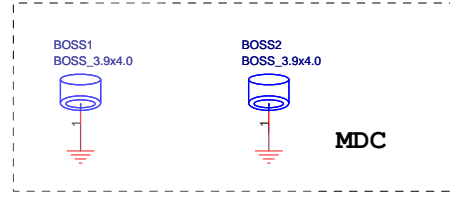
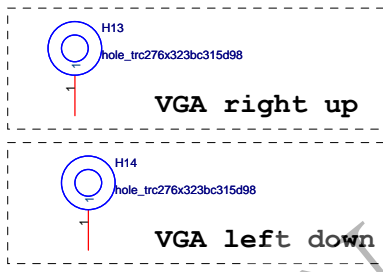
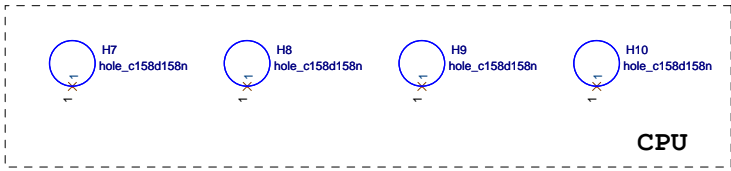
CALISTOGA  
SSCK

Nvidia  
Graphic

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33





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<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>HOLE</b>		CCPBG - R&D Division	
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# HISTORY

(2005/12/15 Initail REV 0.3 )

- P.43 Del R1446,R1447,R1448,R1449 for audio driver issue
- P.53 Add R1459,R1460 to bypass USB hub for OIDE only
- P.53 Add R1461,when U89 is not used,to make sure GANGED# is not left floating.

(2005/12/15) Power modify

- P.63 change PR217 from 2k to 11k,PR224 from 15k to 100k for G72M core voltage setting
- P.63 change PR414 from 560 to 3.3k,PR415 from 22k to 100k for G73M core voltage setting

(2005/12/21)

- P.25 Nvidia's FAE recommend to change R399 & R400 value from 120 ohm to 470 ohm for G73M's terminator setting

(2005/12/28)

- P.29 change U81 from SN74CBT3257PW to SN74CBT3257CPW.Because SN74CBT3257PW is unavailable.
- P.30 change U77 from SN74CBT3257PW to SN74CBT3257CPW.Because SN74CBT3257PW is unavailable.
- P.30 change R1440 from NC to mount.To avoid EC's input floating.

(2005/12/28) Power modify

- P.63 change PR217 from 11k to 2k,PR224 from 100k to 15k for G72M core voltage setting

(2005/12/29)

- P.40 Add R1462 pull down to avoid input floating.

(2005/12/29) Power modify

- P.62 change PC368 from NC to mount.To reduce UL\_LOCK occured rate.

(2006/01/06)

- P.37 R720 change to NV73\_ condition,R724 change to NC condition,R725 change to mount for system ID setting.

(2006/01/14)

- P.53 R1311 change to mount for USB Hub no function issue.

MS11 PVT

(2006/02/06)

- P.42 Del Q79,C1222,R1266,R1267,Q80. Add U109,C1309 for USB camera over current protect

(2006/02/08)

- P.5 Change C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21,C22,C23 from 22uF to 10uF for industry wide shortage of 0805 X5R 22uF capacitors
- P.5 Added C1310,C1311,C1312,C1313,C1314,C1315,C1316,C1317,C1318,C1319,C1320,C1321 for industry wide shortage of 0805 X5R 22uF capacitors
- P.5 Del C1271,C1272,C1273,C1274,C1275,C1276,C1277,C1278,C1279,C1280 to release the layout space in order to place 12 pcs 10uF capacitors

- P.32 Add J2 to discharge RTC for repair conveniently

(2006/02/09)

- P.42 Add F1 for Oide over current protect

(2006/02/10)

- P.42 Change L66,L67 package from 0402 to 0603.Beacuse 0402 package rating is too risky
- P.44 Change C910,C911 from 0.047uF to 0.033uF for passband ripple.

(2006/02/13)

- P.03 Change Q71 from PDTCL44EU to DTCL44EUA for make BOM conveniently.
- P.21 Change Q7 from PDTCL44EU to DTCL44EUA for make BOM conveniently.
- P.41 Change Q93 from PDTCL44EU to DTCL44EUA for make BOM conveniently.
- P.46 Change Q42,Q87 from PDTCL44EU to DTCL44EUA for make BOM conveniently.
- P.46 Change Q86 from MMBT3906 to MMBT3906K for make BOM conveniently.
- P.50 Change Q56 from PDTCL44EU to DTCL44EUA for make BOM conveniently.

(2006/02/15)

- P.42 Add F2 and C1322 to bypass U109, directly connect CAM\_5V to +5VRUN

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		CCPBG - R&D Division	
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