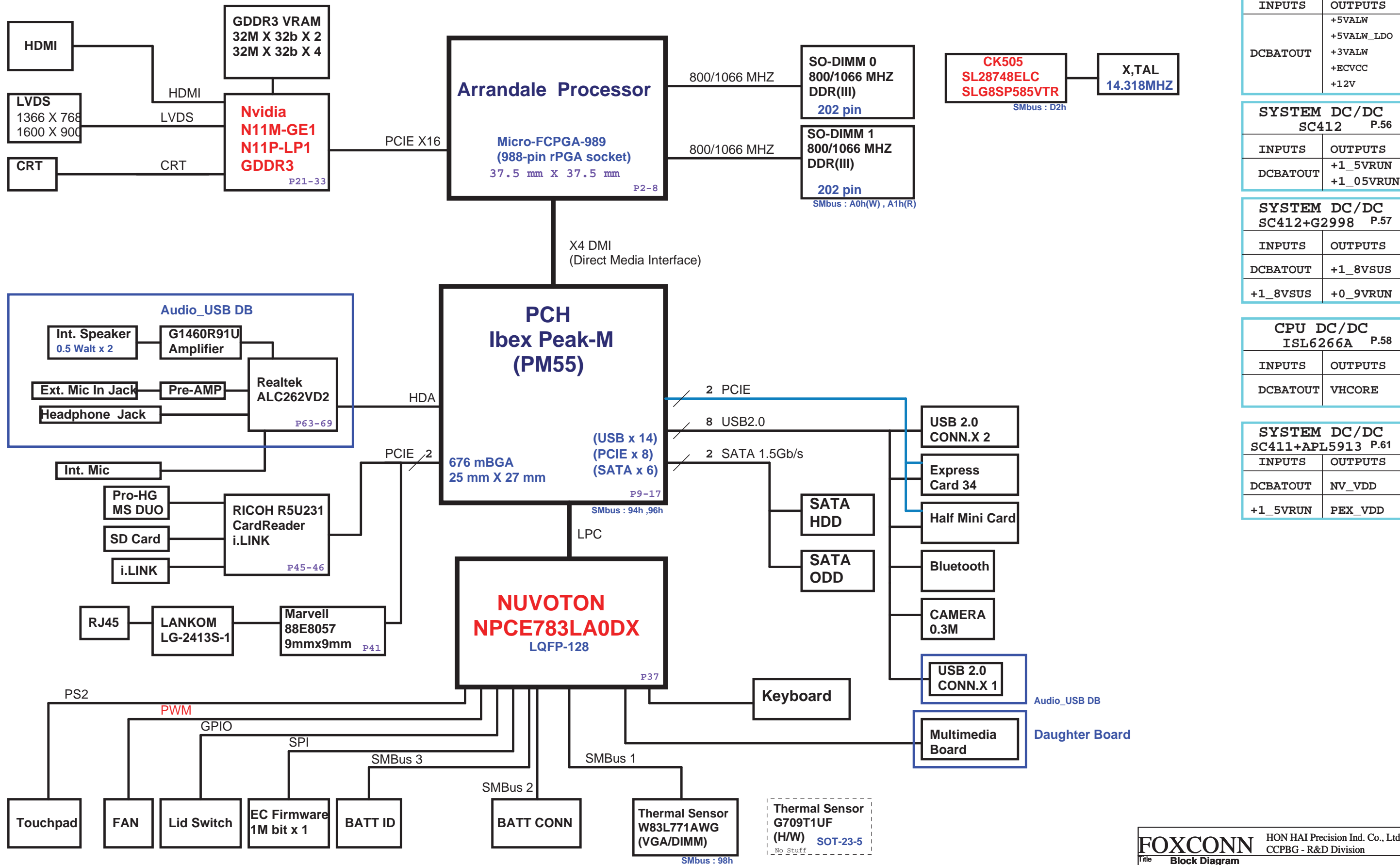


M-9A0 (Calpella + N11P/M Discrete Graphic)



TI CHARGER BQ24753 P.54	
OUTPUTS	
DC_IN	BT+ DCBATOUT

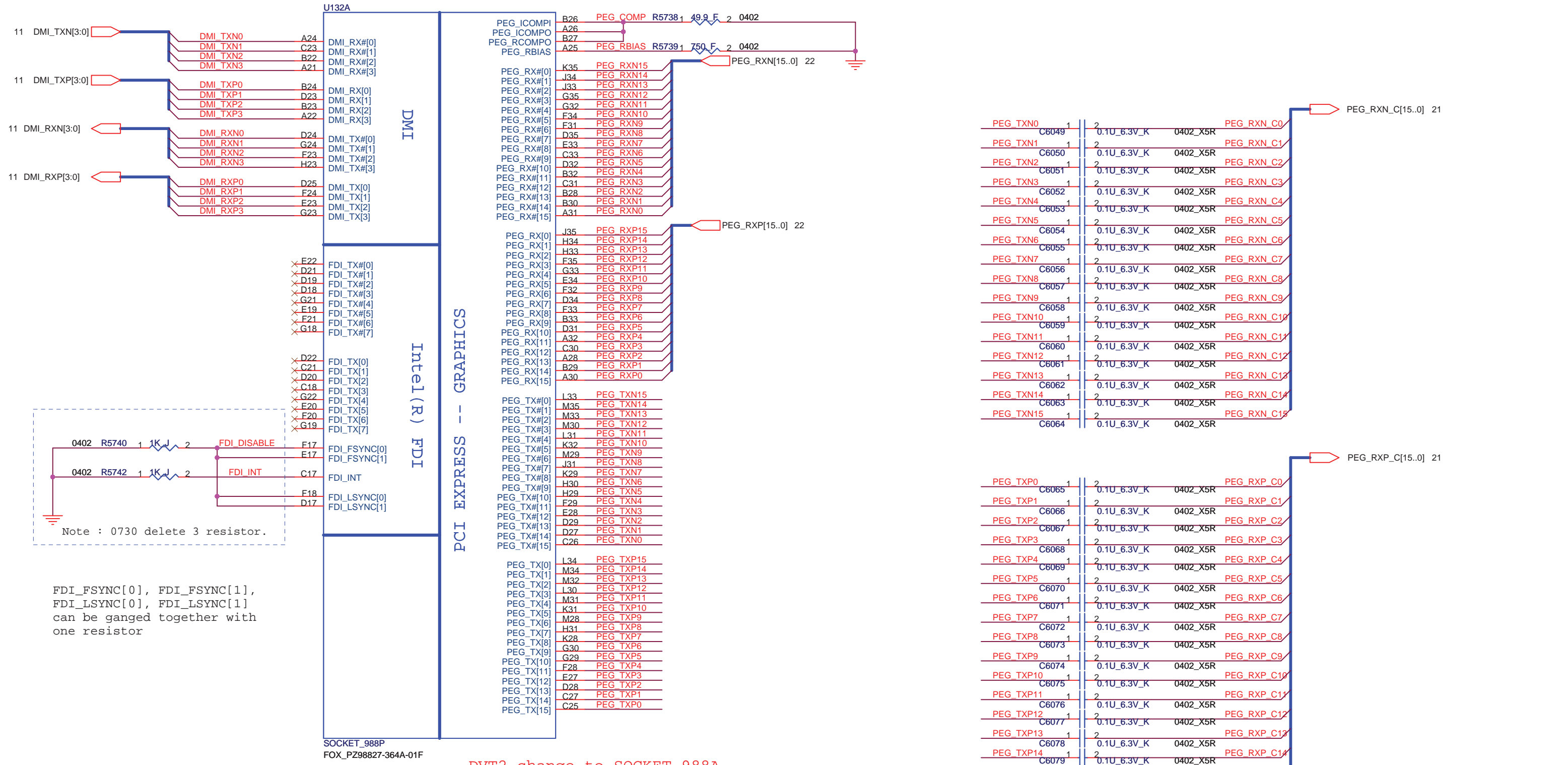
SYSTEM DC/DC MAX17020ETJ+ P.55	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +12V

SYSTEM DC/DC SC412 P.56	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SYSTEM DC/DC SC412+G2998 P.57	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS +1_8VSUS +0_9VRUN

CPU DC/DC ISL6266A P.58	
INPUTS	OUTPUTS
DCBATOUT	VHORE

SYSTEM DC/DC SC411+APL5913 P.61	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD +1_5VRUN PEX_VDD



Note : 0730 delete 3 resistor.

FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor

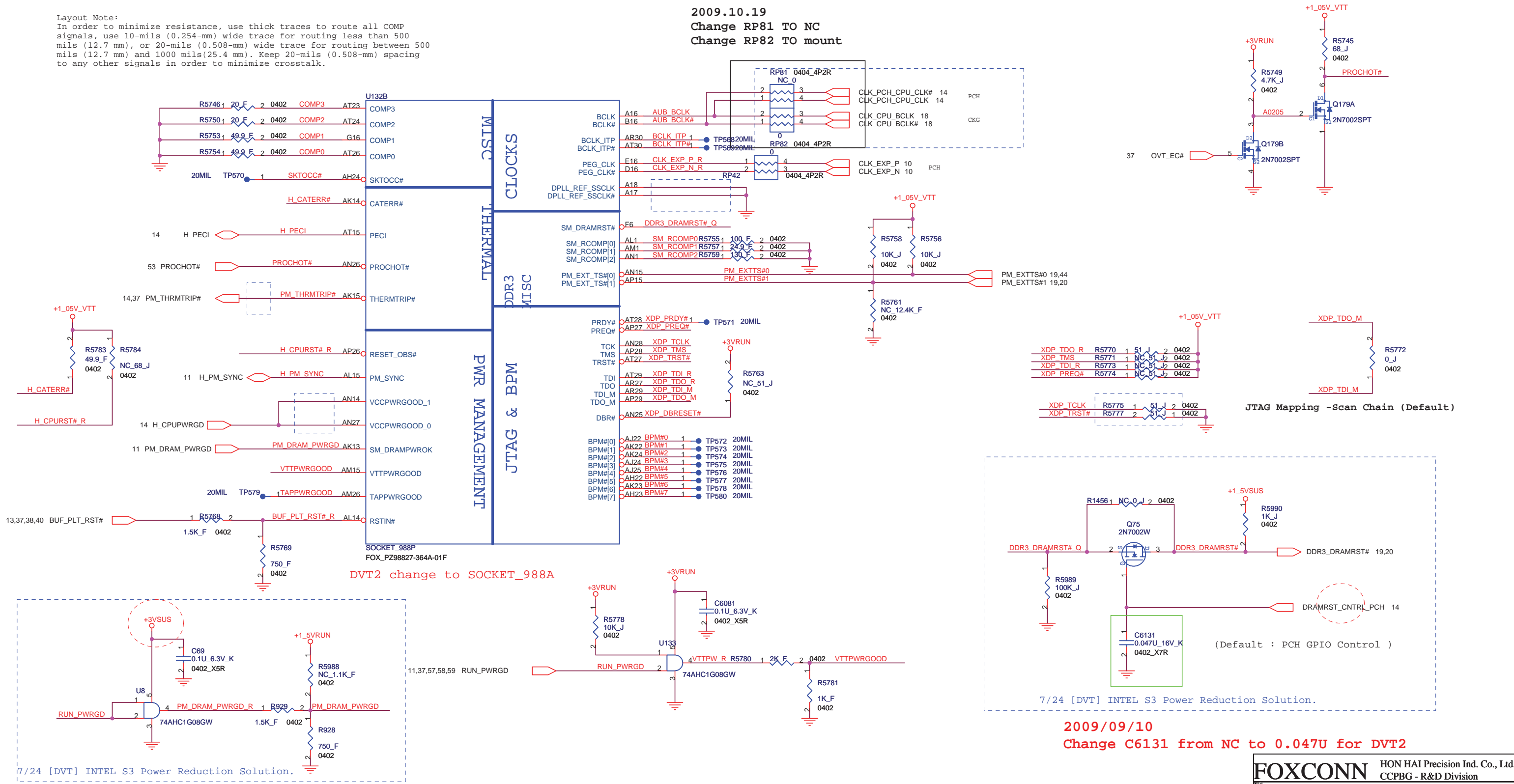
DVT2 change to SOCKET_988A

For Disable Arrandale Graphic
 In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
 FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

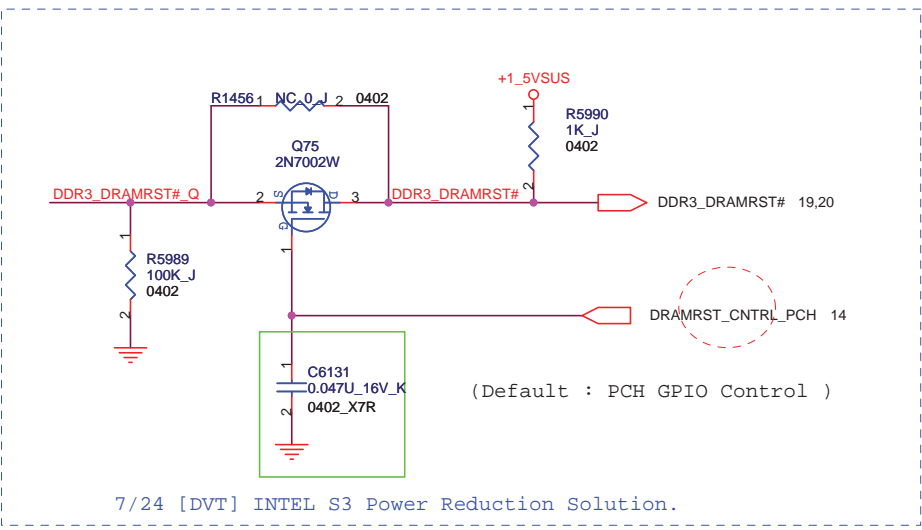
For Disable Arrandale Graphics:
 DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on
 Arrandale directly if motherboard only supports discrete graphics.

2009.10.19
 Change RP81 TO NC
 Change RP82 TO mount

Layout Note:
 In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils (0.254-mm) wide trace for routing less than 500 mils (12.7 mm), or 20-mils (0.508-mm) wide trace for routing between 500 mils (12.7 mm) and 1000 mils(25.4 mm). Keep 20-mils (0.508-mm) spacing to any other signals in order to minimize crosstalk.

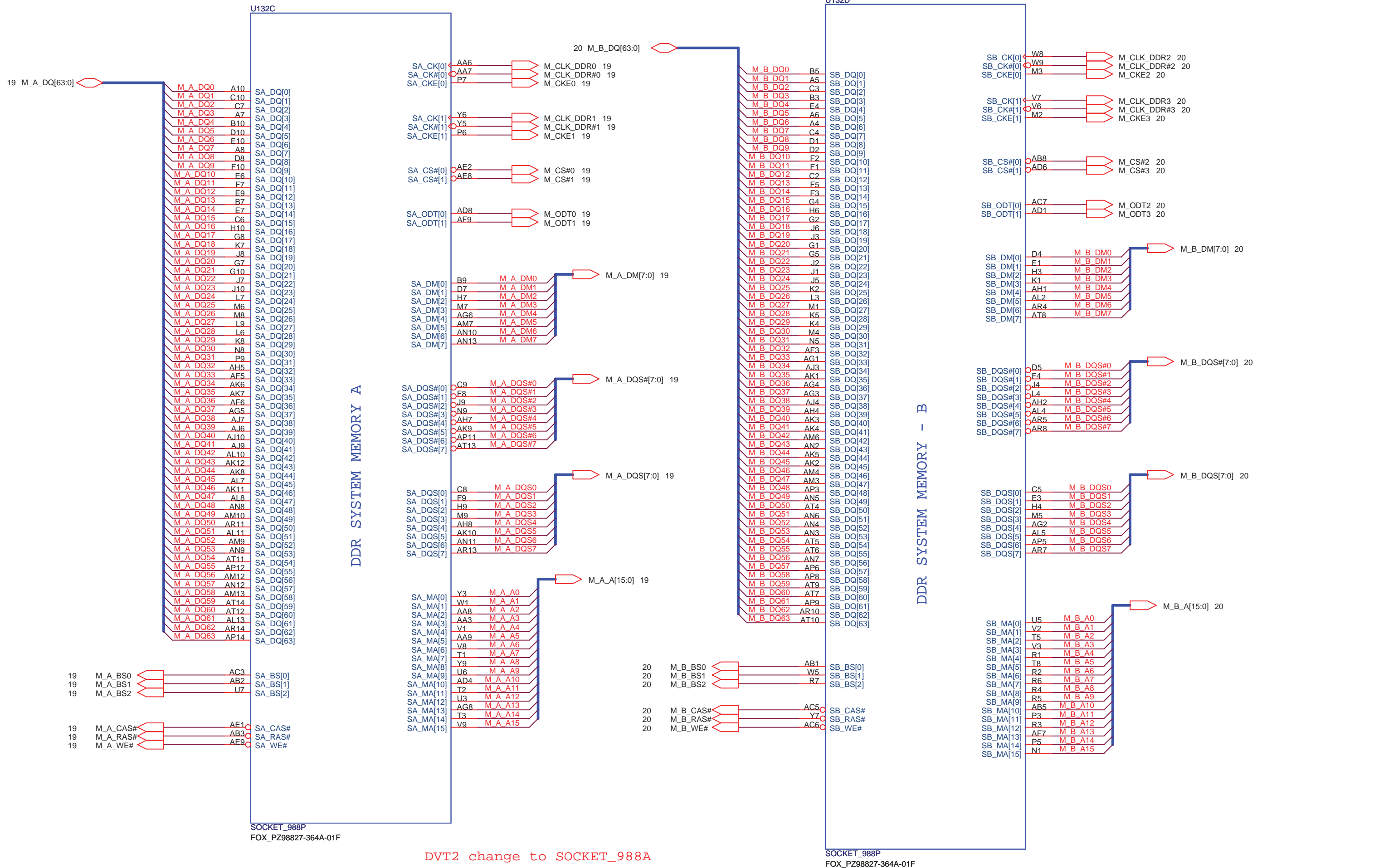


DVT2 change to SOCKET_988A



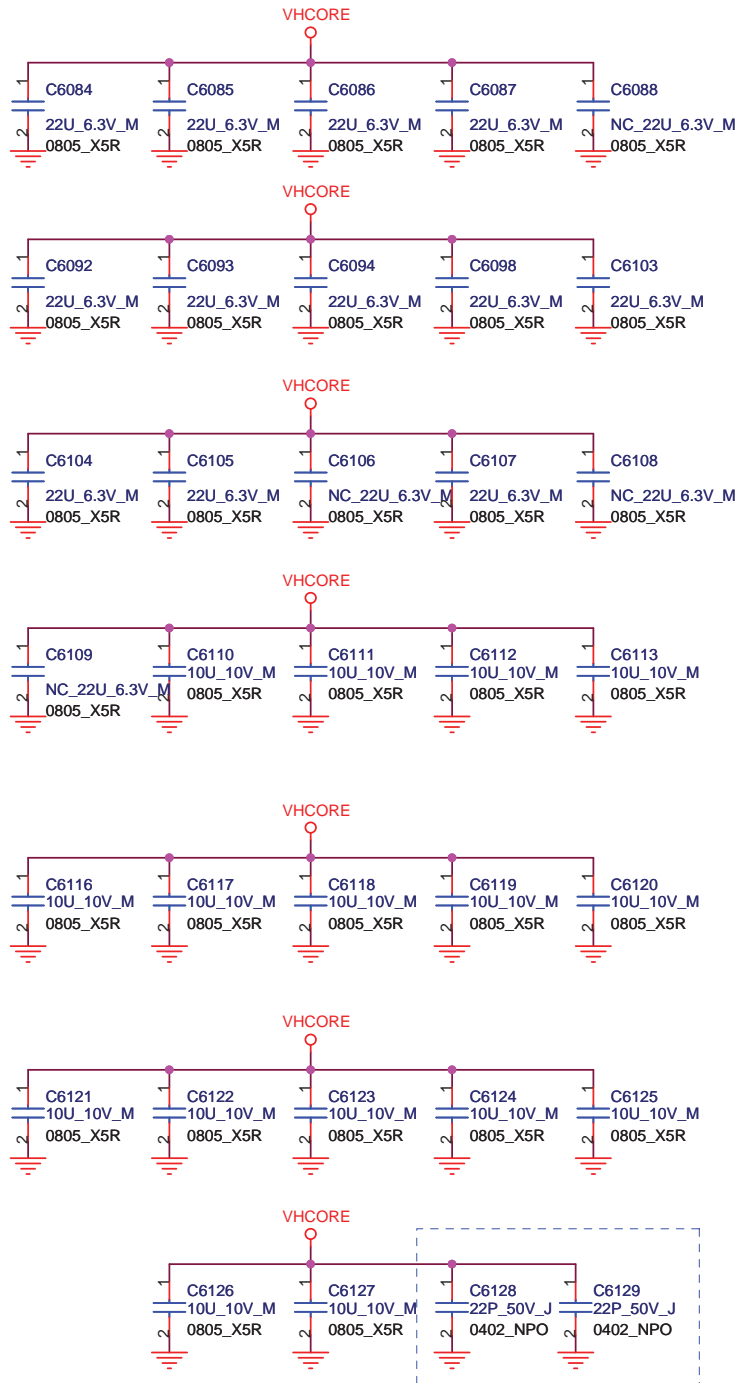
2009/09/10
 Change C6131 from NC to 0.047U for DVT2

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title ARD (CLK,MISC,JTAG)			
Size	Document Number	Rev	
Custom	M9A0 MP	1.1	
Date:	Thursday, November 19, 2009	Sheet	3 of 73



DVT2 change to SOCKET_988A

48A (ARD SV)

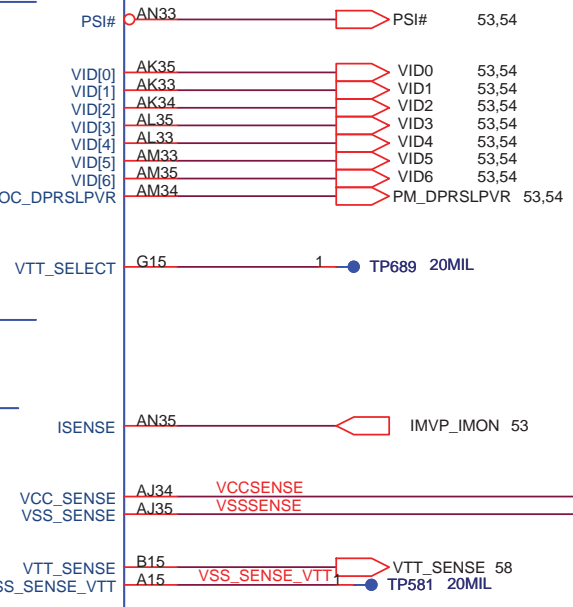


For RF Noise

- VHCORE
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

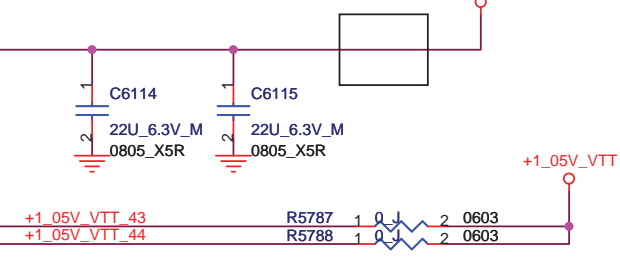
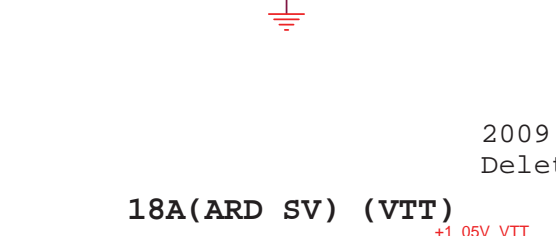
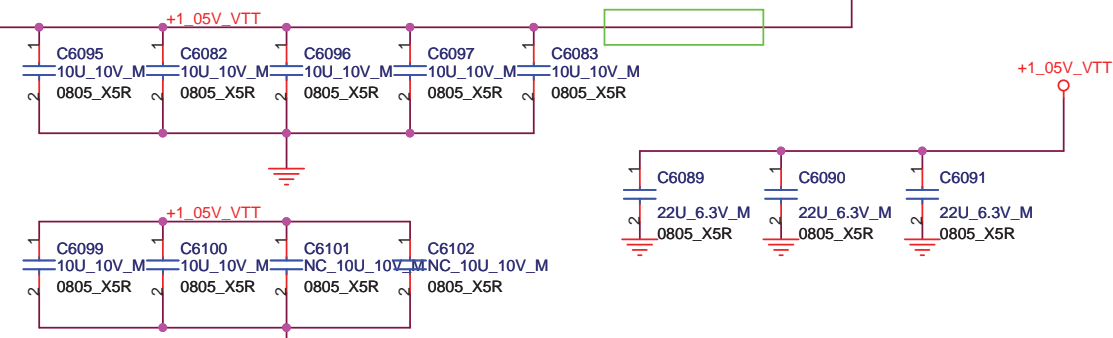
SOCKET_988P
FOX_PZ98827-364A-01F

1.1V RAIL POWER
CPU CORE SUPPLY



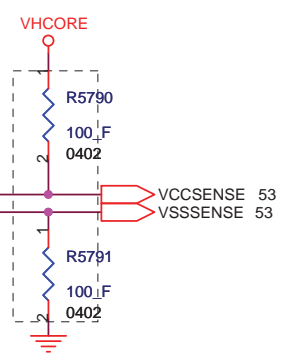
DVT2 change to SOCKET_988A

18A(ARD SV) (VTT)



2009.10.23
Delete R5786 for PVT

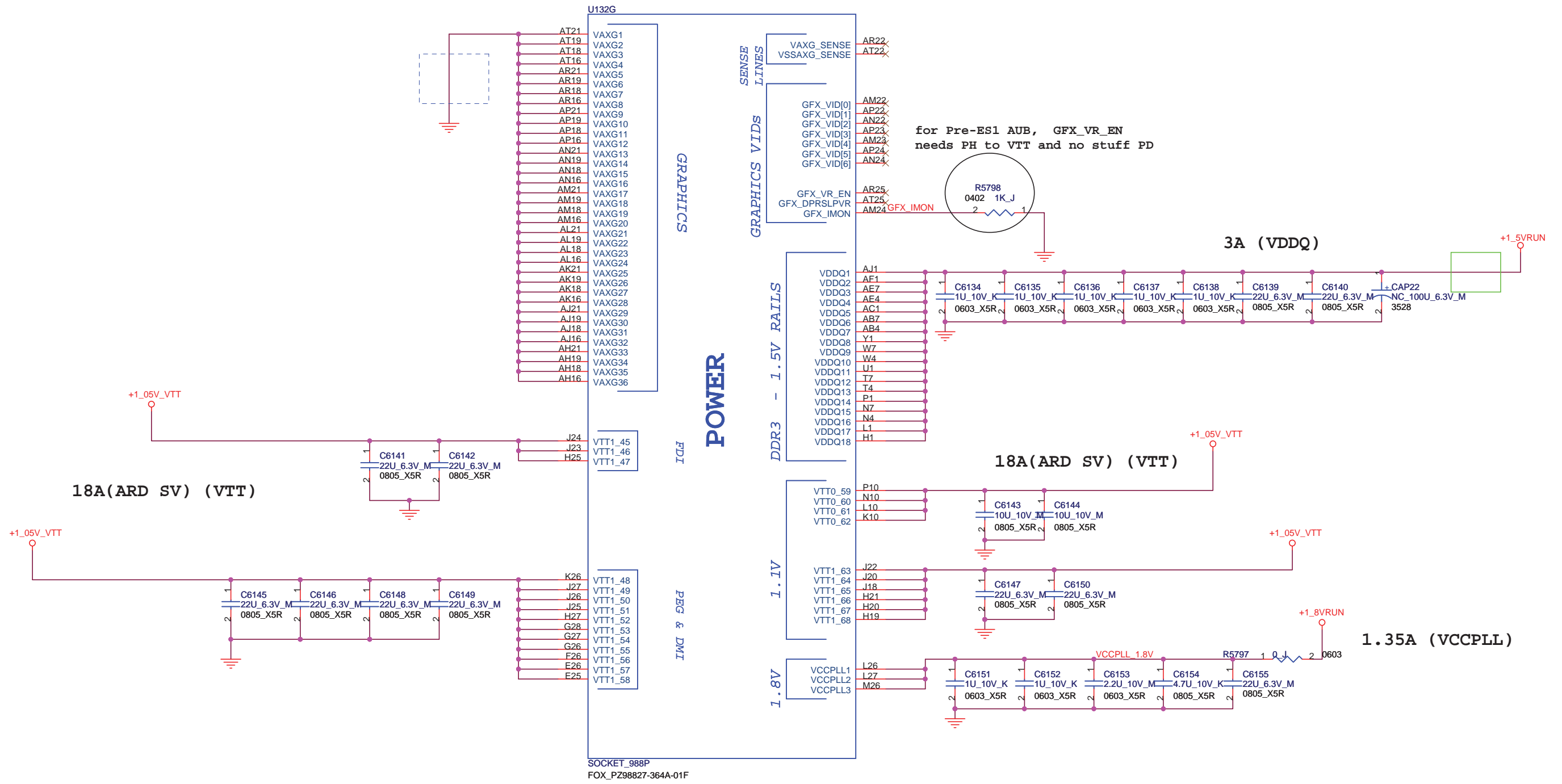
- VTT0_1 AH14
- VTT0_2 AH12
- VTT0_3 AH11
- VTT0_4 AH10
- VTT0_5 J14
- VTT0_6 J13
- VTT0_7 H14
- VTT0_8 H12
- VTT0_9 G14
- VTT0_10 G13
- VTT0_11 G12
- VTT0_12 G11
- VTT0_13 F14
- VTT0_14 F13
- VTT0_15 F12
- VTT0_16 F11
- VTT0_17 E14
- VTT0_18 E12
- VTT0_19 D14
- VTT0_20 D13
- VTT0_21 D12
- VTT0_22 C14
- VTT0_23 C13
- VTT0_24 C12
- VTT0_25 C11
- VTT0_26 B14
- VTT0_27 B12
- VTT0_28 A14
- VTT0_29 A13
- VTT0_30 A12
- VTT0_31 A11
- VTT0_32
- VTT0_33 AF10
- VTT0_34 AE10
- VTT0_35 AC10
- VTT0_36 AB10
- VTT0_37 Y10
- VTT0_38 W10
- VTT0_39 U10
- VTT0_40 T10
- VTT0_41 J12
- VTT0_42 J11
- VTT0_43 J16
- VTT0_44 J15



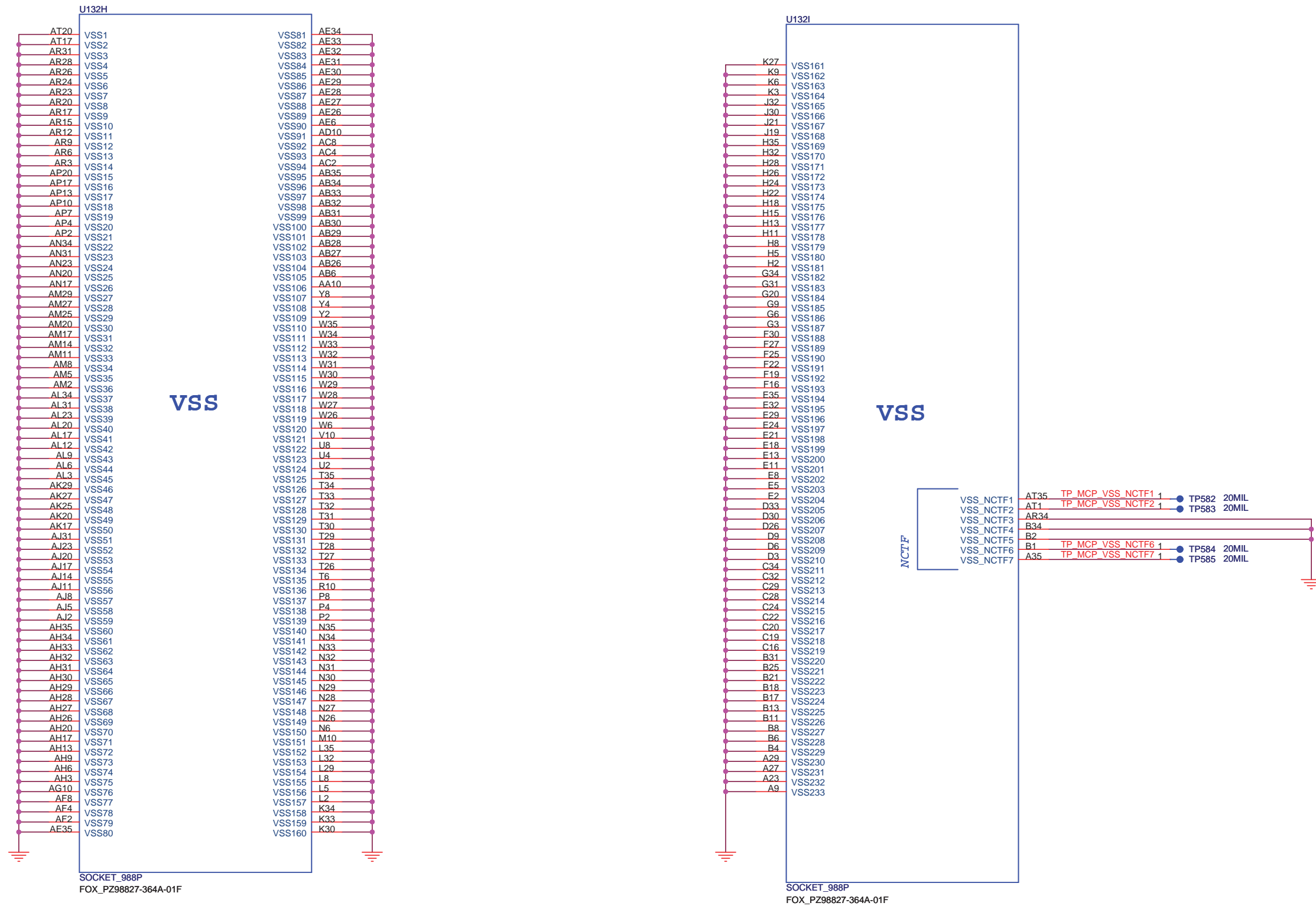
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title ARD(POWER)			
Size	Document Number	Rev	
Custom	M9A0 MP	1.1	
Date:	Wednesday, October 28, 2009	Sheet	5 of 73

For Disable Arrandale Graphic
VAXG should be connected to GND when disable iGPU.

For Disable Arrandale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as no connect.



DVT2 change to SOCKET_988A

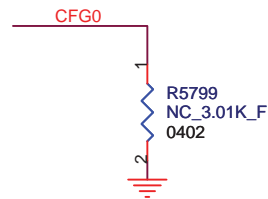


DVT2 change to SOCKET_988A

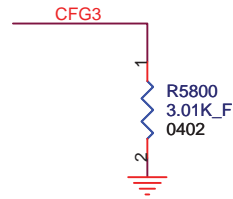
PCI Express Configuration Select
 CFG0 1 : Single PEG * default
 0 : Bifurcation enable

3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
 The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.

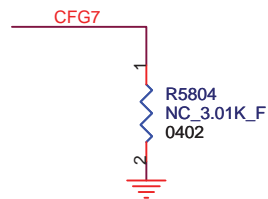
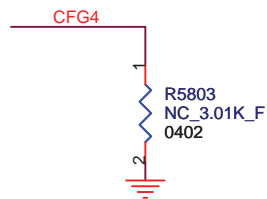
CFG pin is latch on the rising edge of CPU powergood.



CFG3 PCI Express Static Lane Reversal
 CFG3 1 : Normal
 0 : Lane Numbers Reversed *
 15 -> 0 , 14 -> 1 , ...

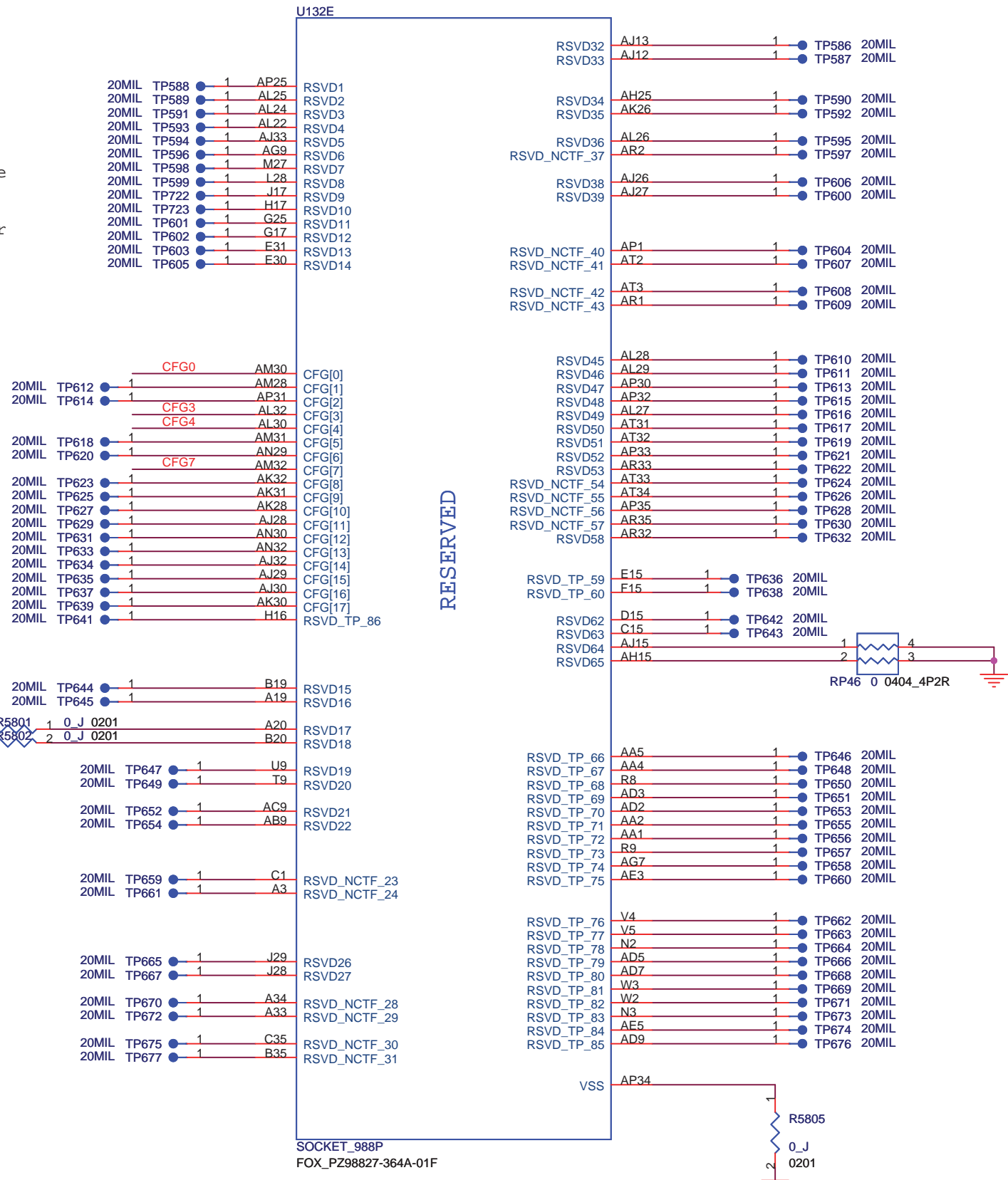


CFG4 Display Port Presence
 CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
 0 : Enable ; An external Display Port device is connected to the Embedded Display Port



2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

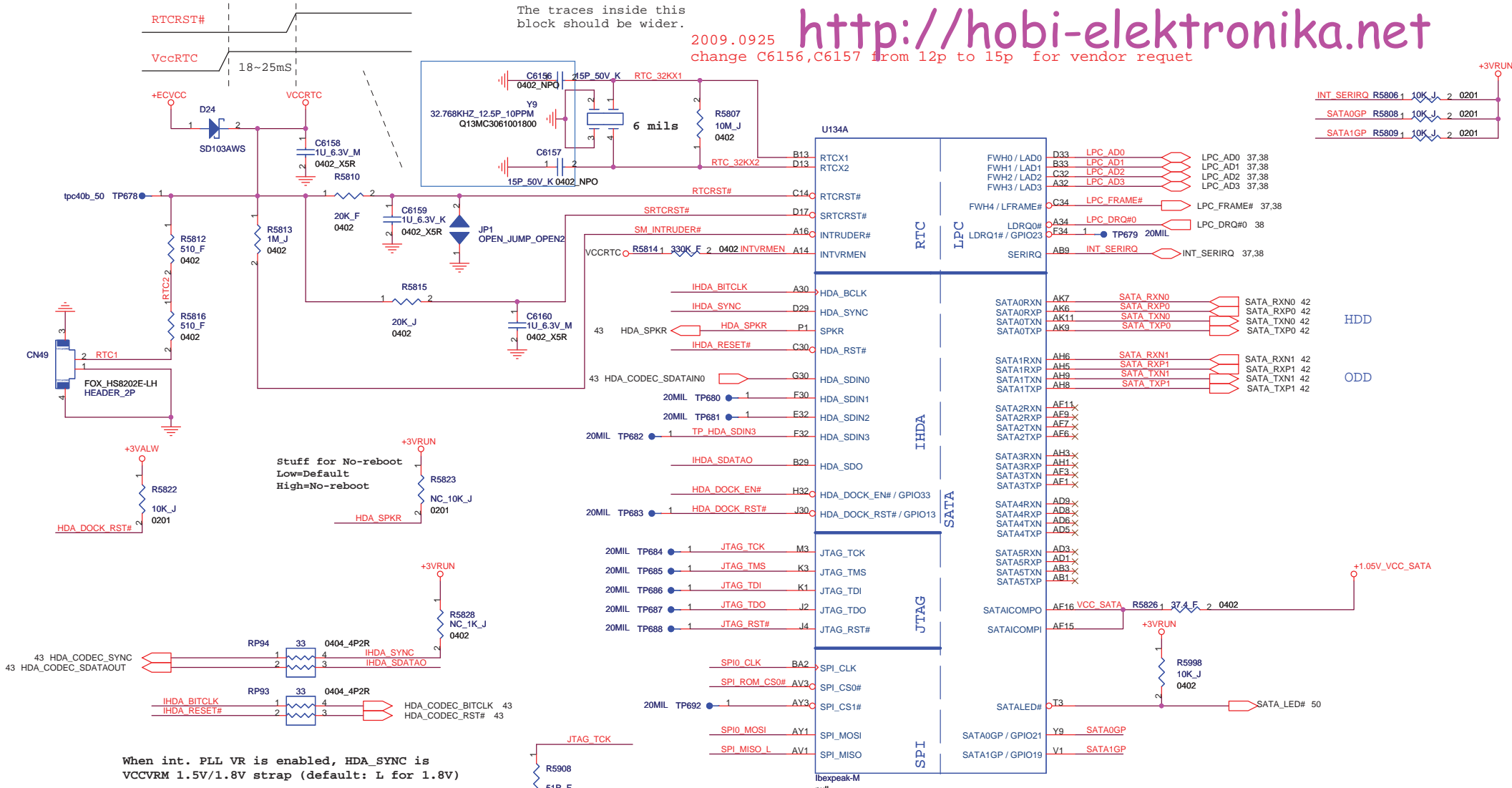
Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



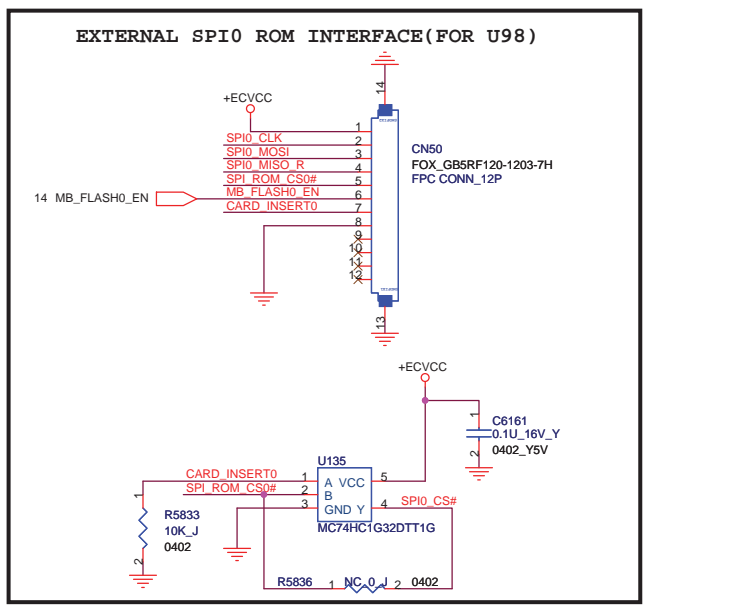
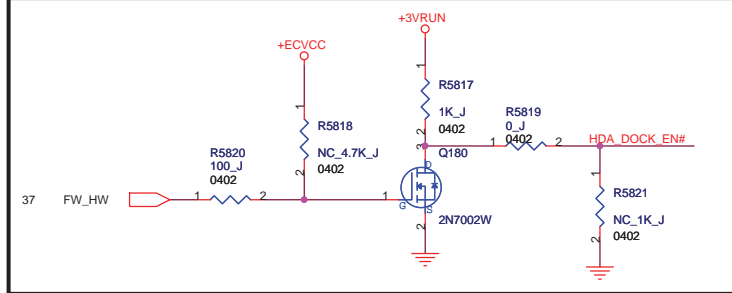
DVT2 change to SOCKET_988A

2009.0925
change C6156, C6157 from 12p to 15p for vendor request

The traces inside this block should be wider.



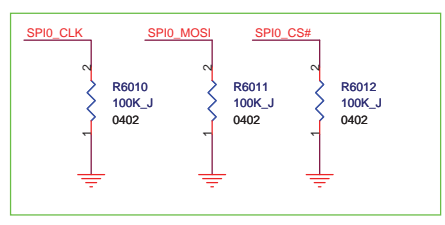
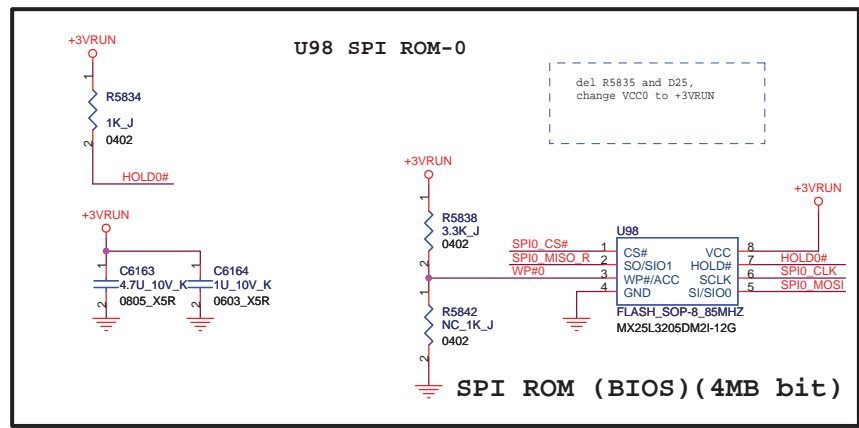
[HDA_DOCK_EN#/GPIO33]
Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) - Security measure defined in the Flash Descriptor will be enabled



Stuff for No-reboot
Low=Default
High=No-reboot

When int. PLL VR is enabled, HDA_SYNC is VCCVRM 1.5V/1.8V strap (default: L for 1.8V)

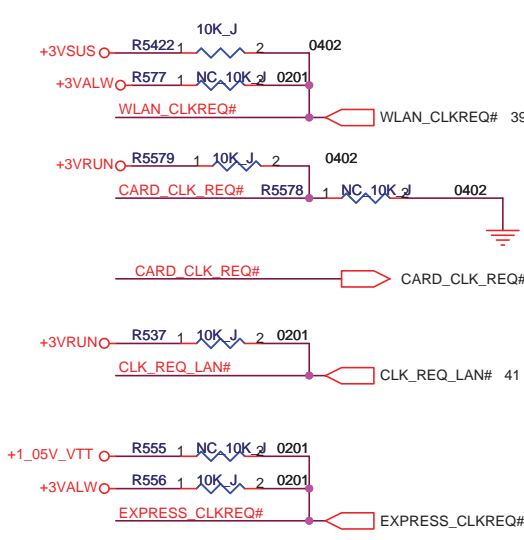
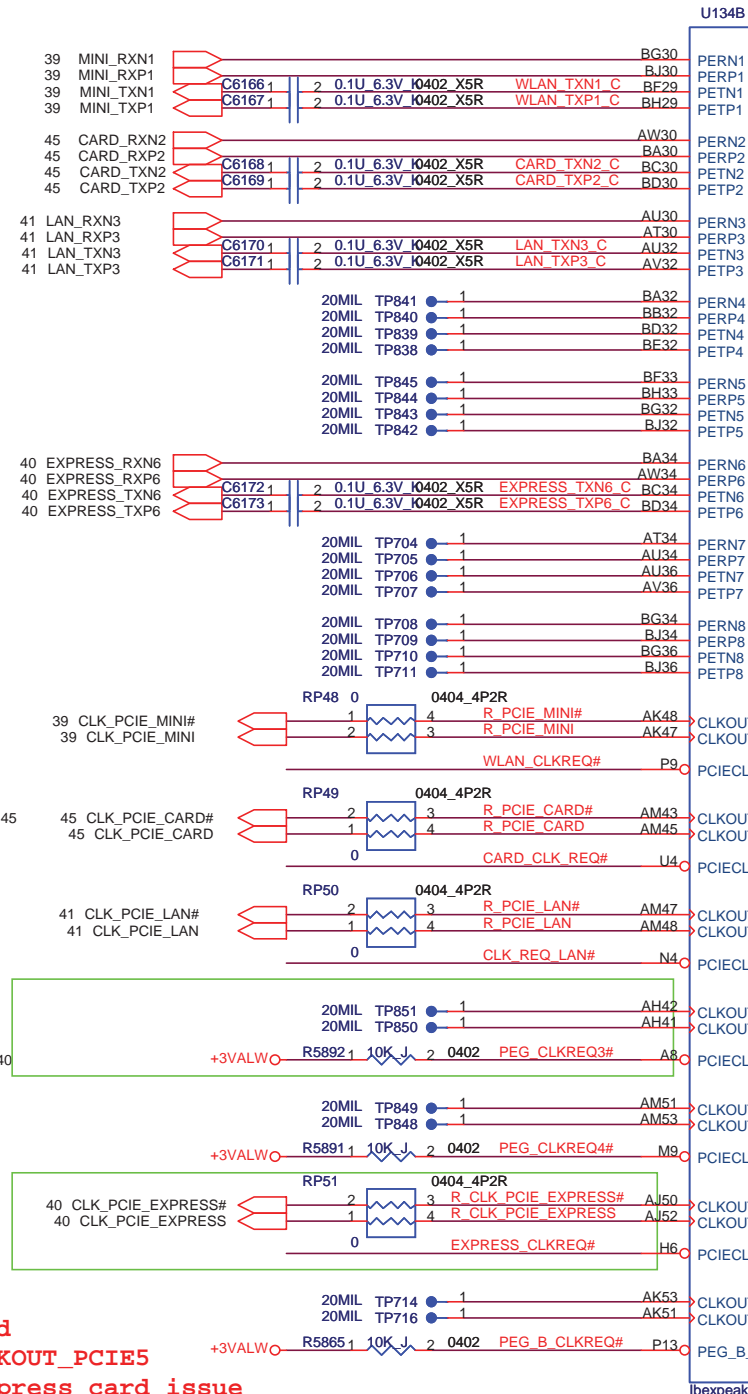
For DVT2,
ARD(QS)+PM55(MP)+4M SPI ROM



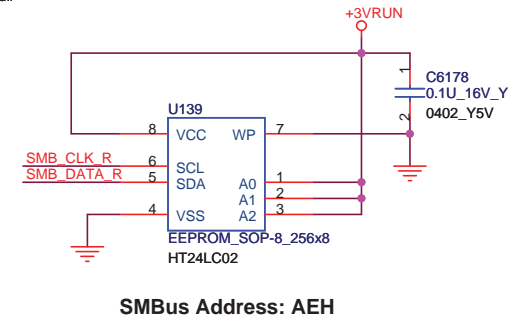
add follow EDS

PCI-E Port Table

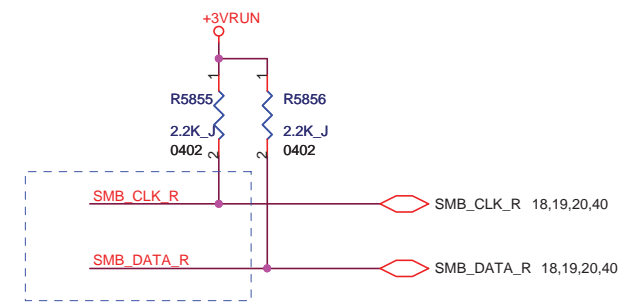
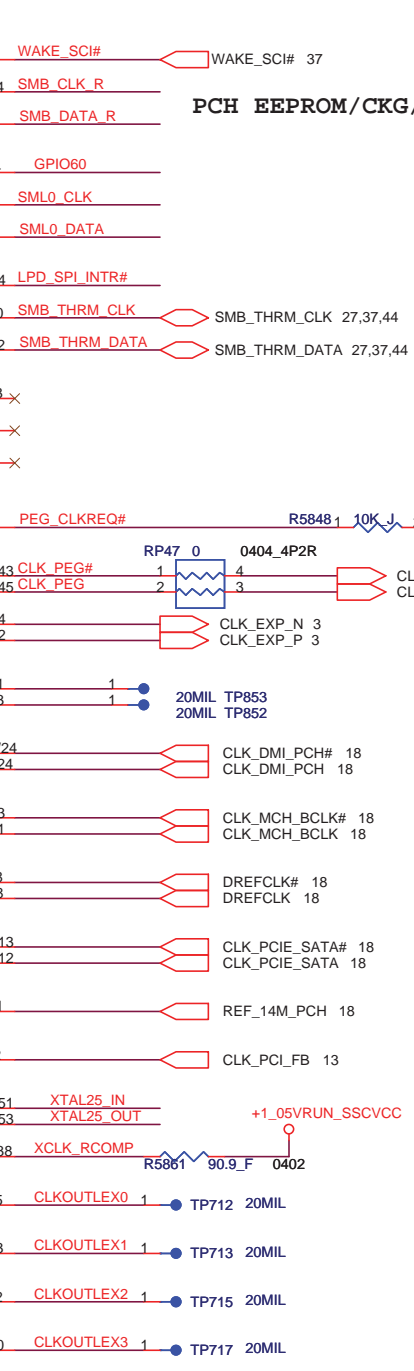
Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCI-E)
Port7	NC
Port8	NC



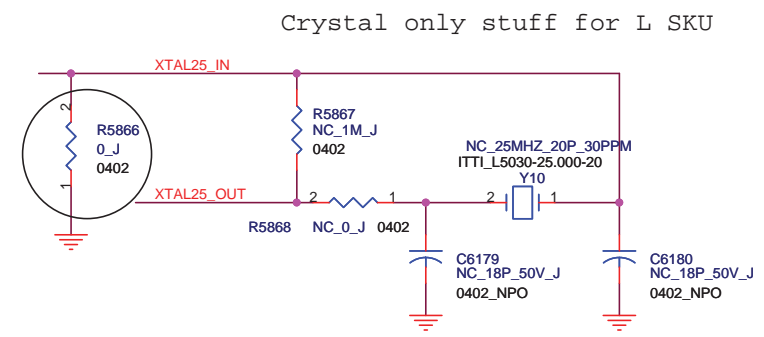
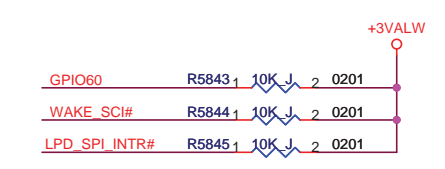
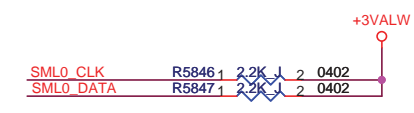
2009/09/10
 Remove PCI-E Express card
 differential clock to CLKOUT_PCIE5
 for DVT1 can't detect express card issue



SMBus Address: AEH



EC/THM/dGPU
 (SMBus Address: 94h,96h)

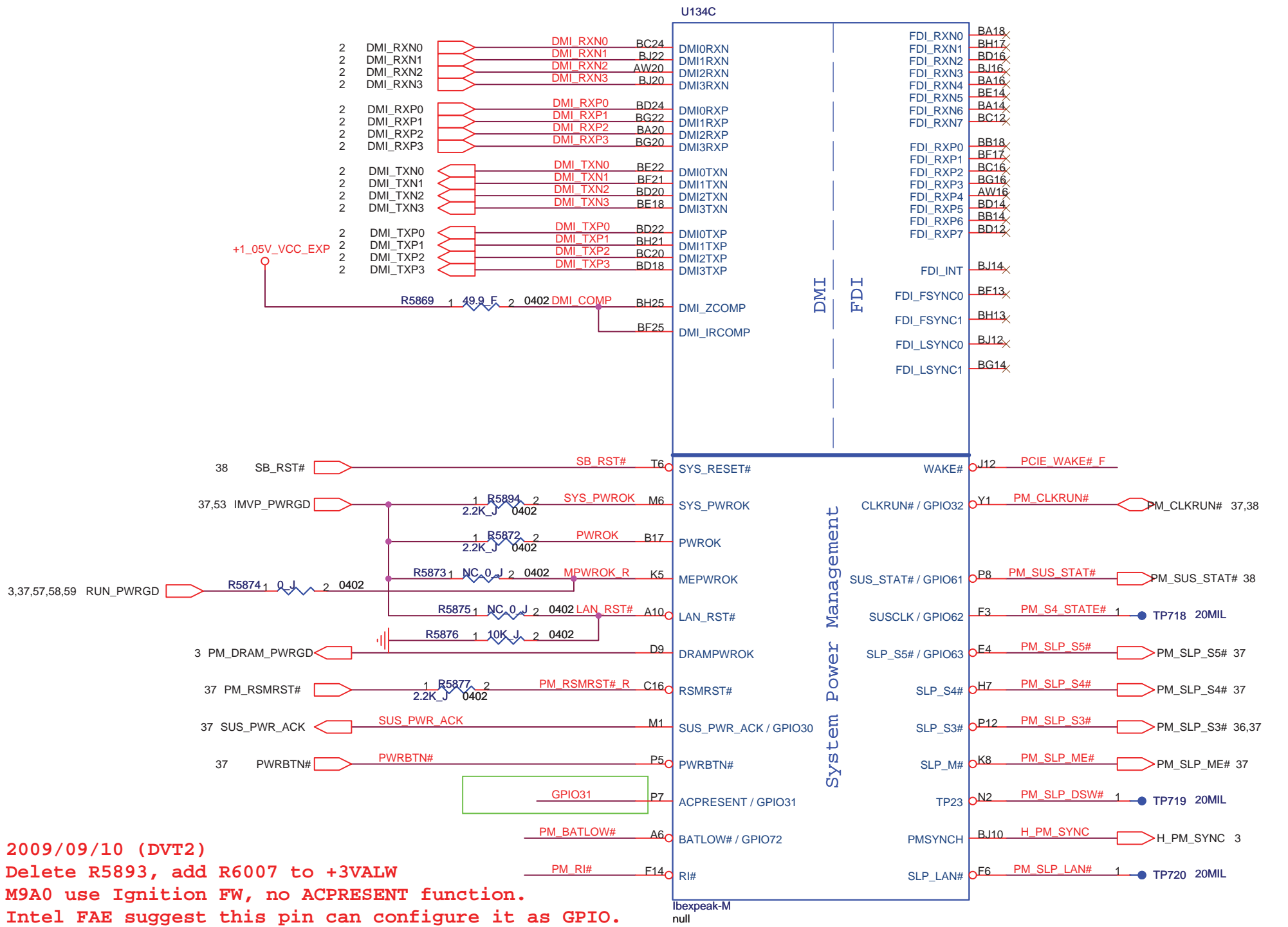


Crystal only stuff for L SKU

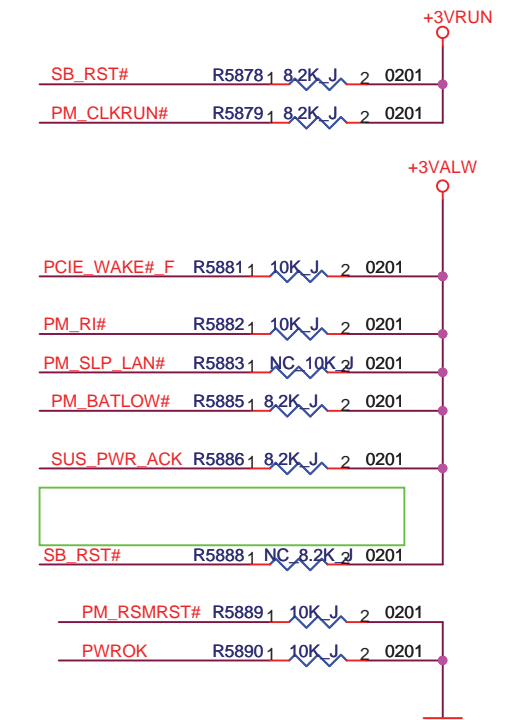
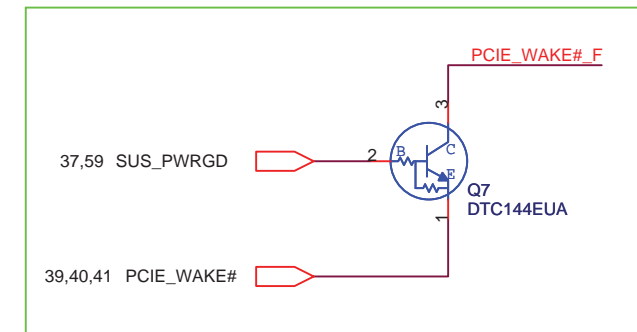
Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044).
 XTAL_IN should be pulled to GND via a 0ohm by default.
 This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	PCH (PCI-E, SMBUS, CLK)		
Size	Document Number		Rev
Custom	M9A0 MP		1.1
Date:	Friday, October 23, 2009	Sheet	10 of 73

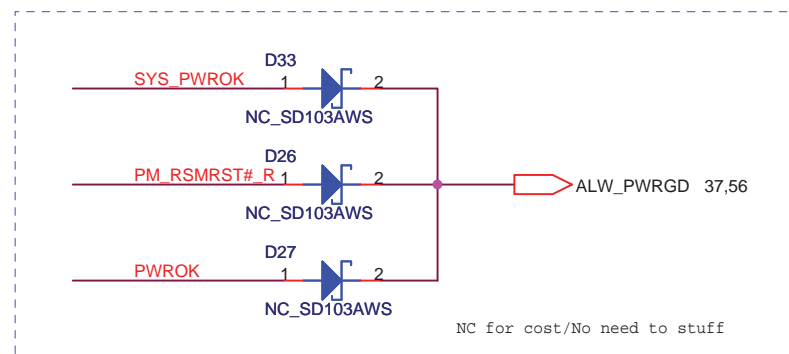
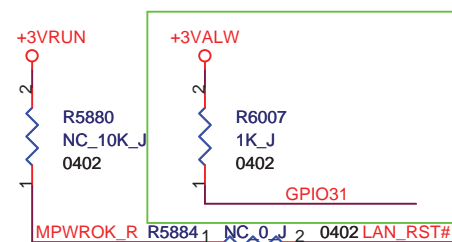
For Disable Auburndale Graphic
 In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
 FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
 GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
 signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



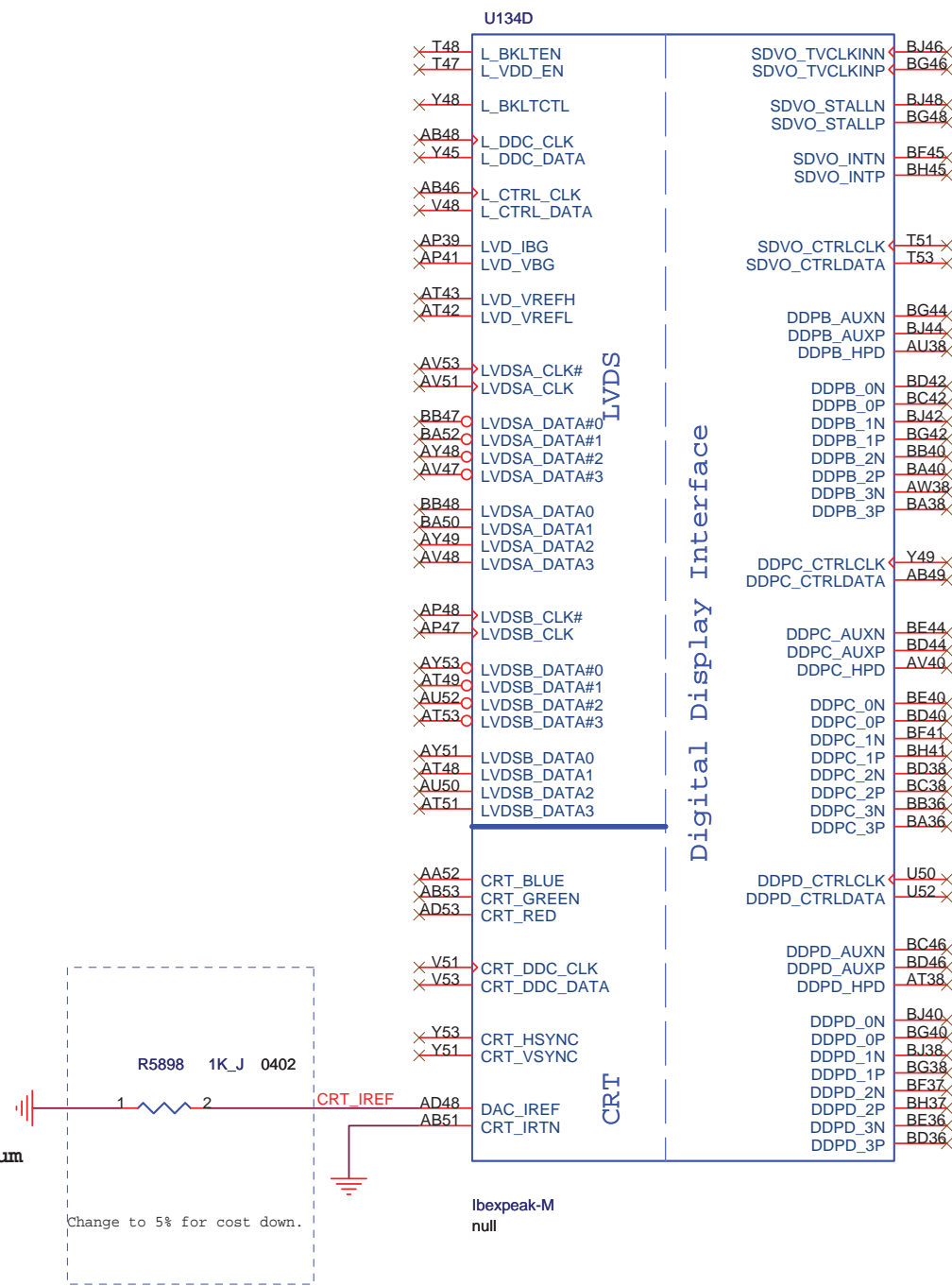
2009.0928
 Add the Q7 as MOR request.



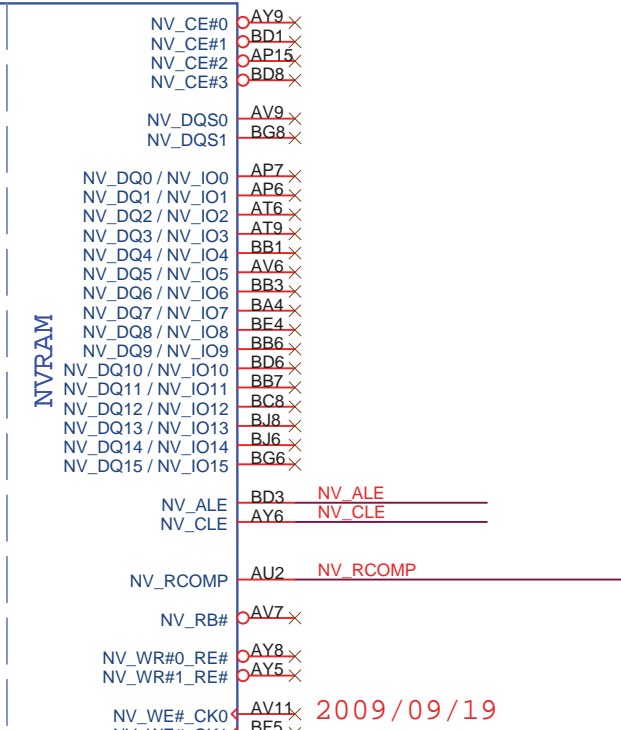
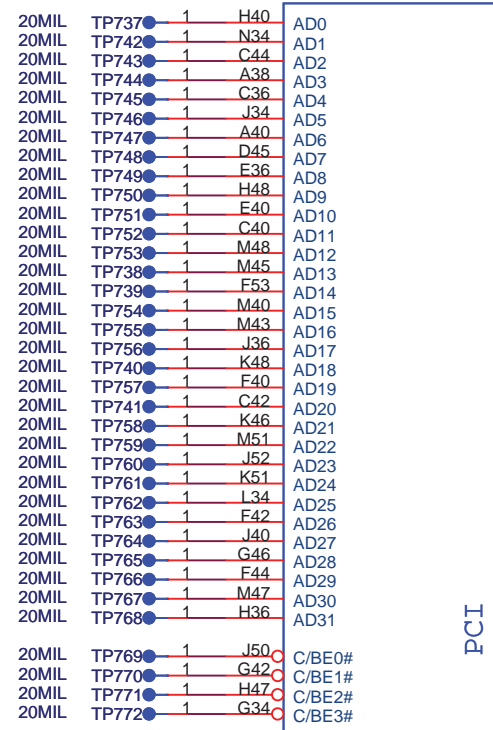
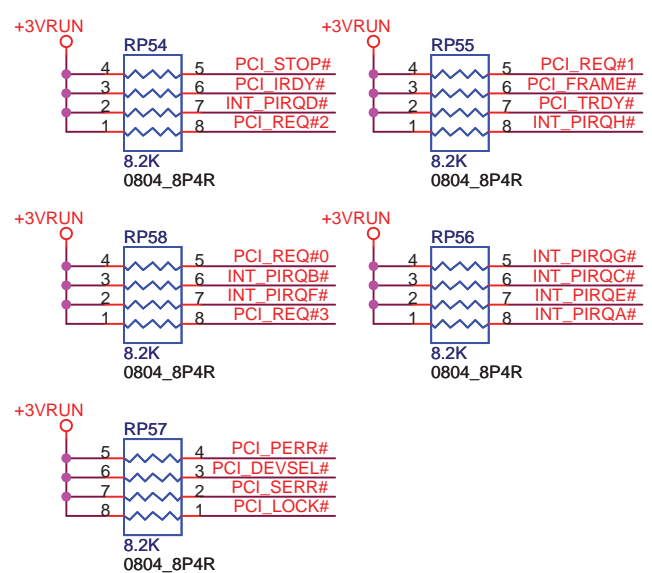
2009/09/10 (DVT2)
 Delete R5893, add R6007 to +3VALW
 M9A0 use Ignition FW, no ACPRESENT function.
 Intel FAE suggest this pin can configure it as GPIO.



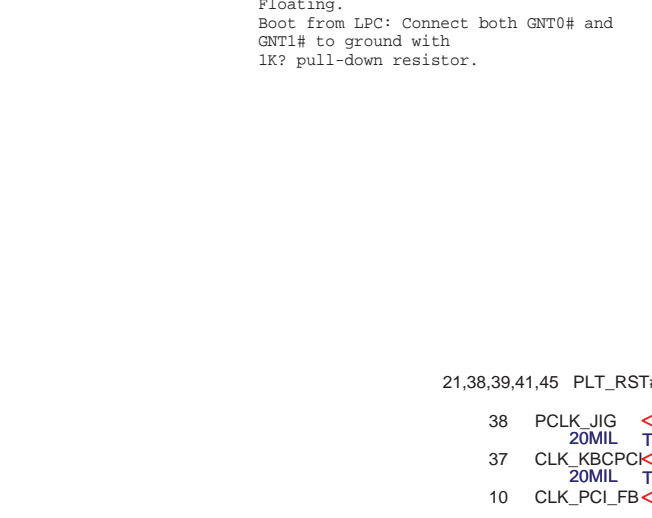
2009/09/10 (DVT2)
 Delete R5887 and Net name AC_Present
 M9A0 use Ignition FW, no ACPRESENT function.
 Intel FAE suggest this pin can configure it as GPIO.



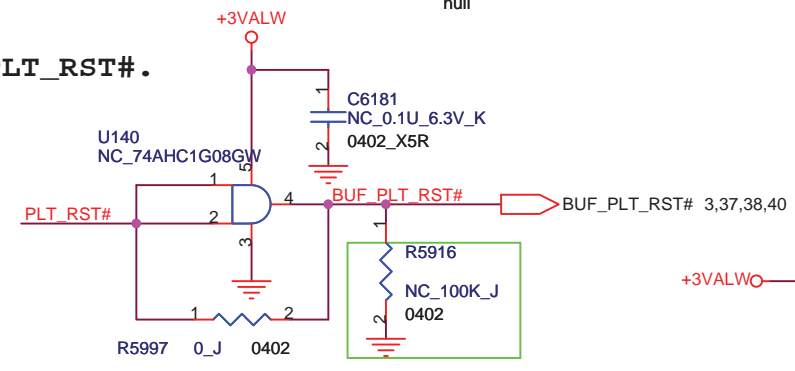
Calpella Platform - Design Guide - Addendum
/ Update - Rev. 1.52 (Doc #414044).).



Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required.
 Boot from PCI: Connect GNT1# to ground with 1-k? pull-down resistor. Leave GNT0# Floating.
 Boot from LPC: Connect both GNT0# and GNT1# to ground with 1K? pull-down resistor.



Buffer to reduce loading on PLT_RST#.

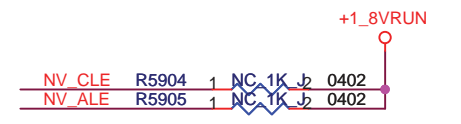


2009/09/19 Change USB_PN10/USB_PP10 to test point



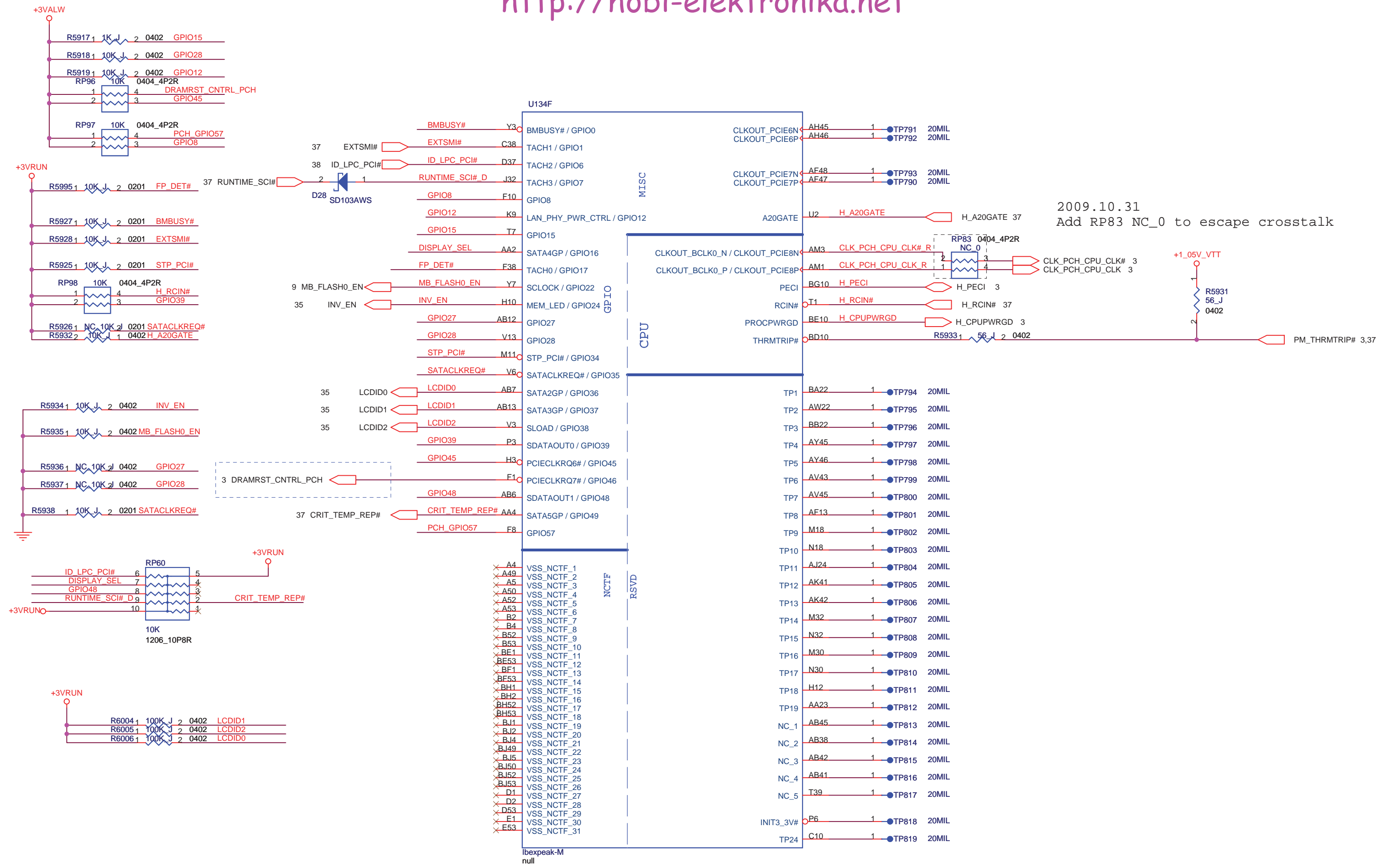
2009/09/19 Add USB_OC#1

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW
NV_CLE	Set to Vcc when HIGH



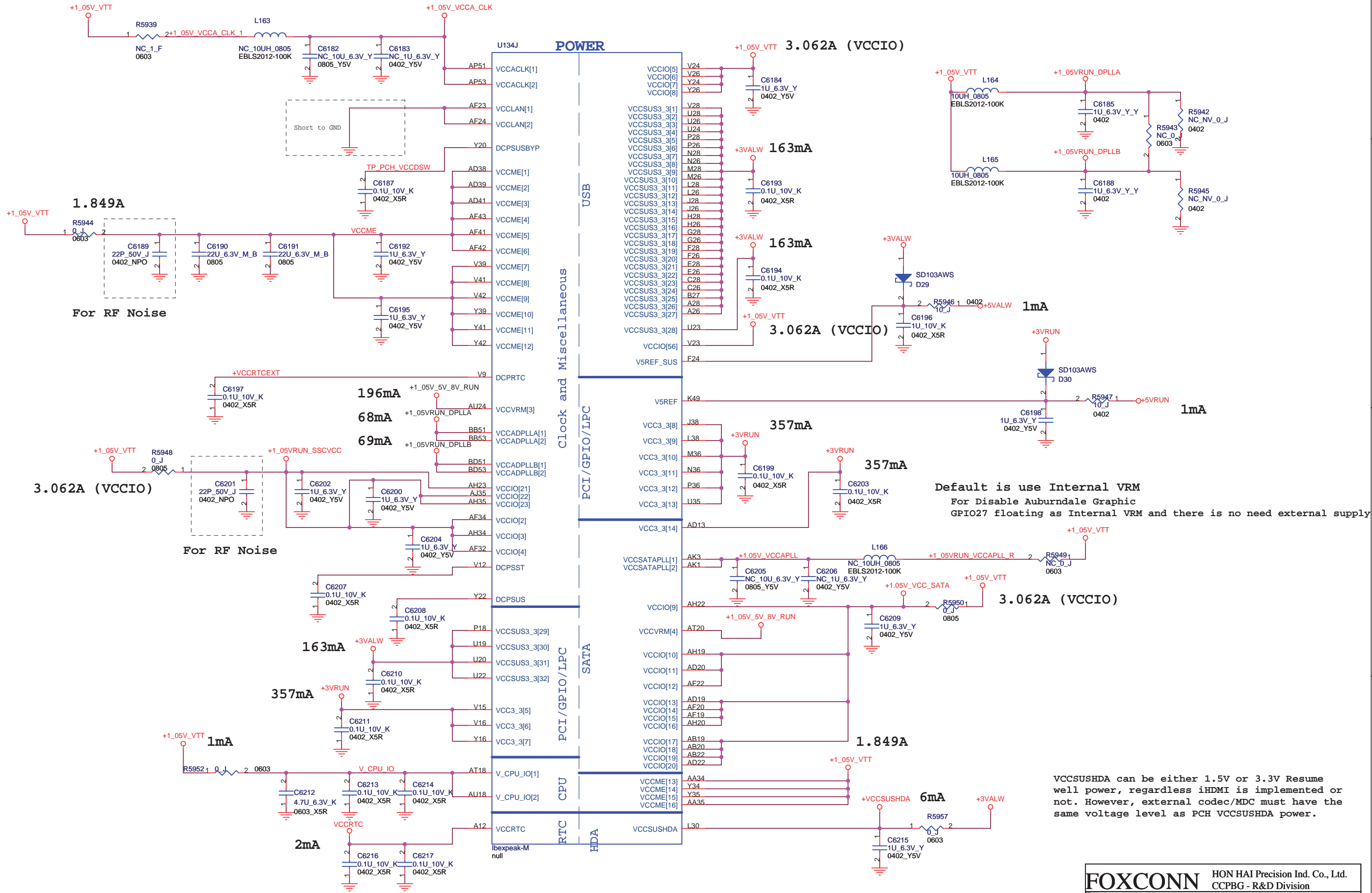
Intel Anti-Theft Technology Disabled when Low , NC R1616 Enabled when High , Stuff R1616

USB PORT	Function
PORT-0	External Port-0
PORT-1	External Port-1
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-2
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	No finger print
PORT-11	
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth

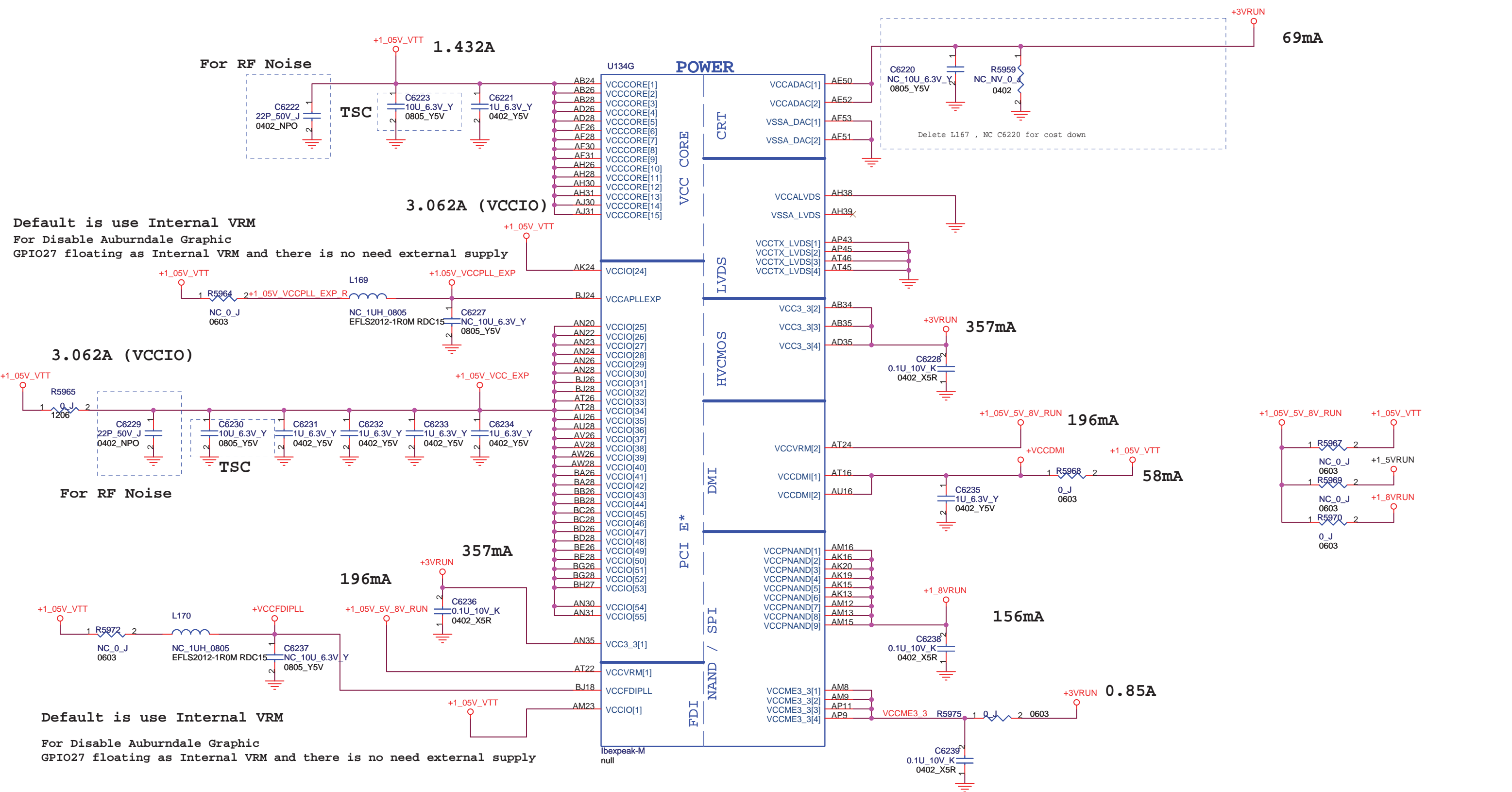


2009.10.31
Add RP83 NC_0 to escape crosstalk

Default is use Internal VRM
 For Disable Auburndale Graphic
 GPIO27 floating as Internal VRM and there is no need external supply

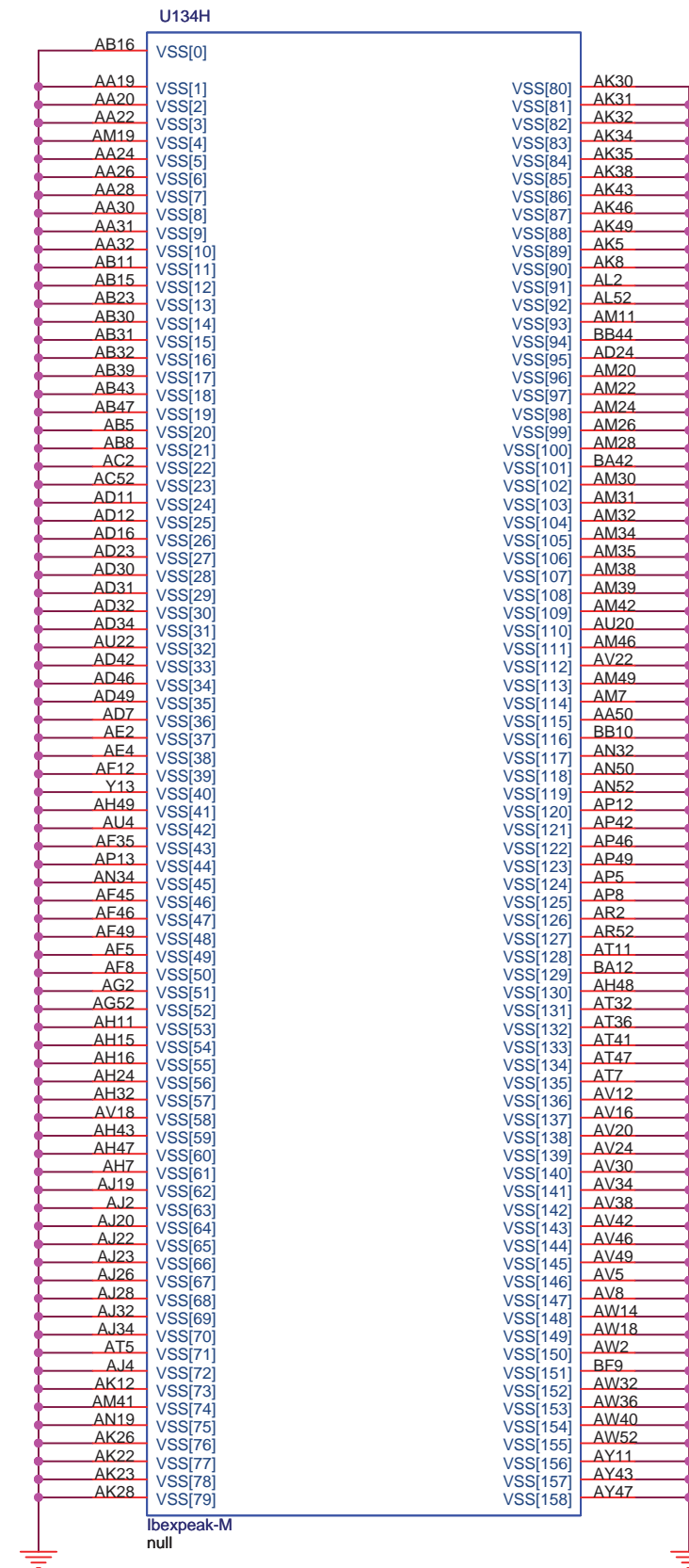
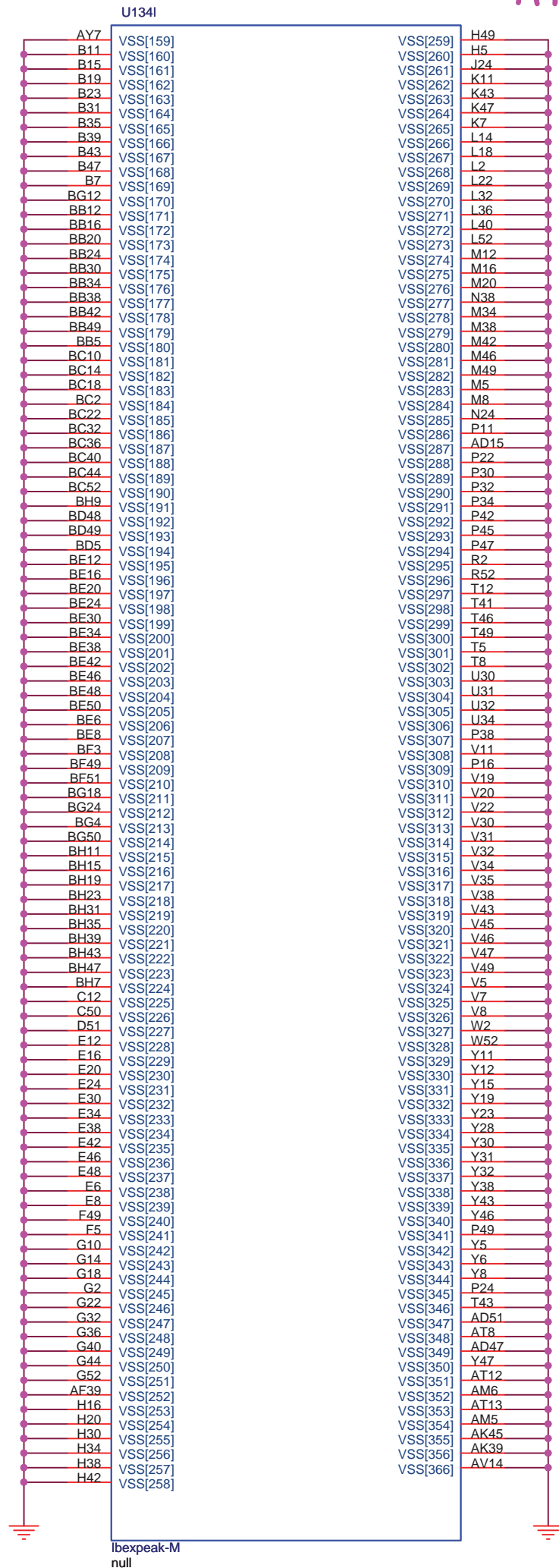


VCCSUSHDA can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.

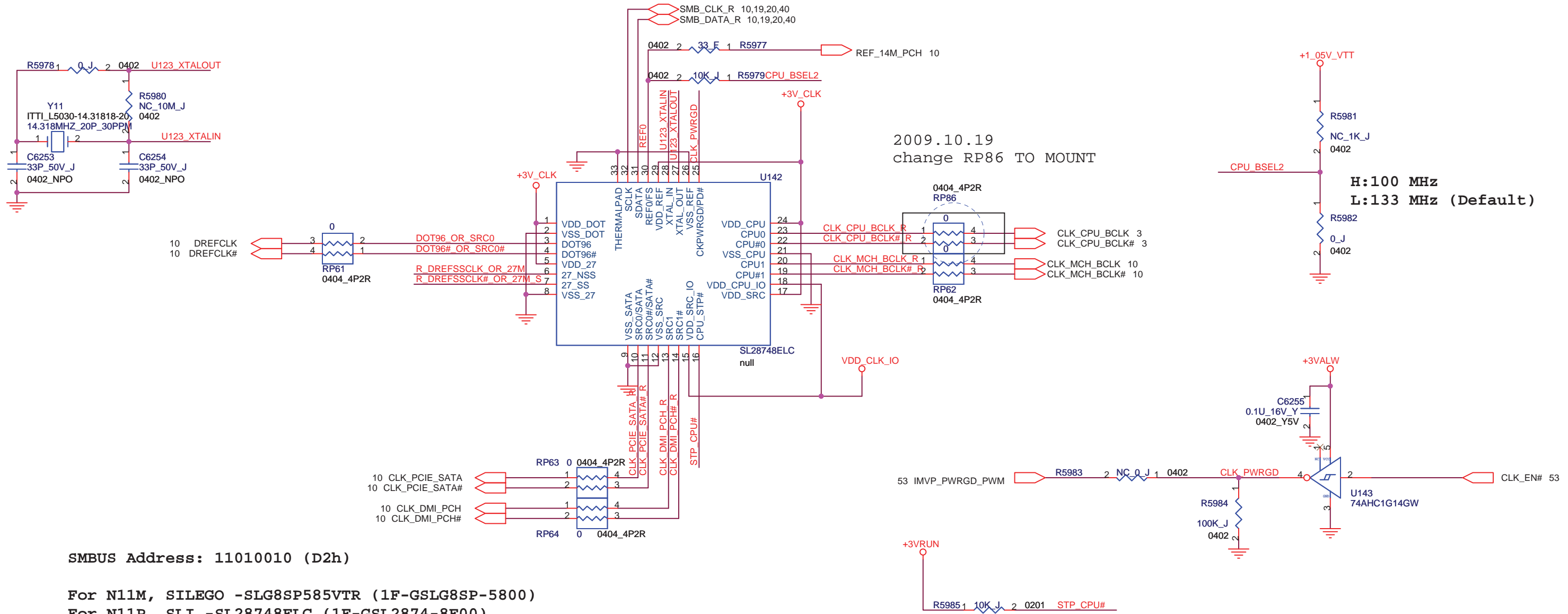
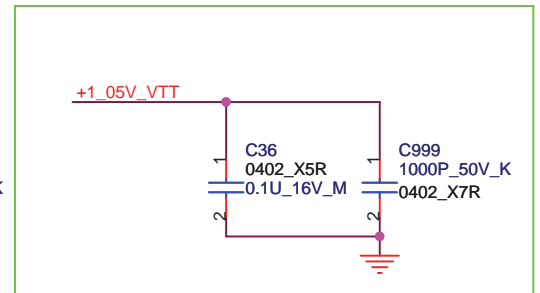
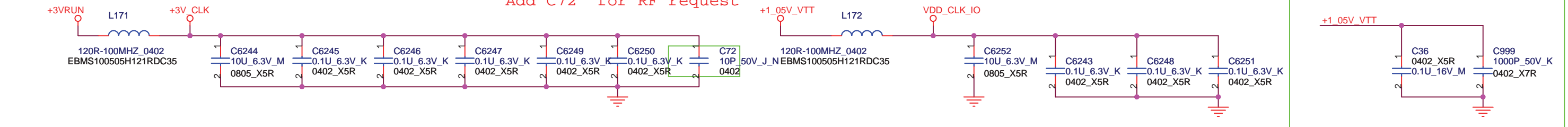


Default is use Internal VRM
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply

Default is use Internal VRM
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



2009.0925
Add C72 for RF request



2009.10.19
change RP86 TO MOUNT

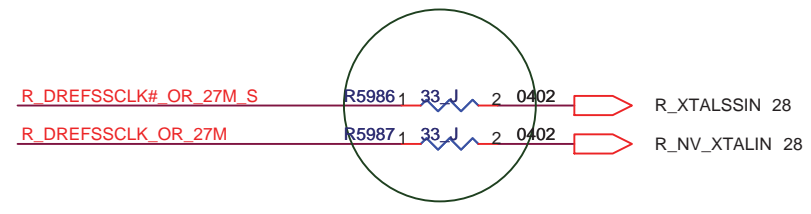
H:100 MHz
L:133 MHz (Default)

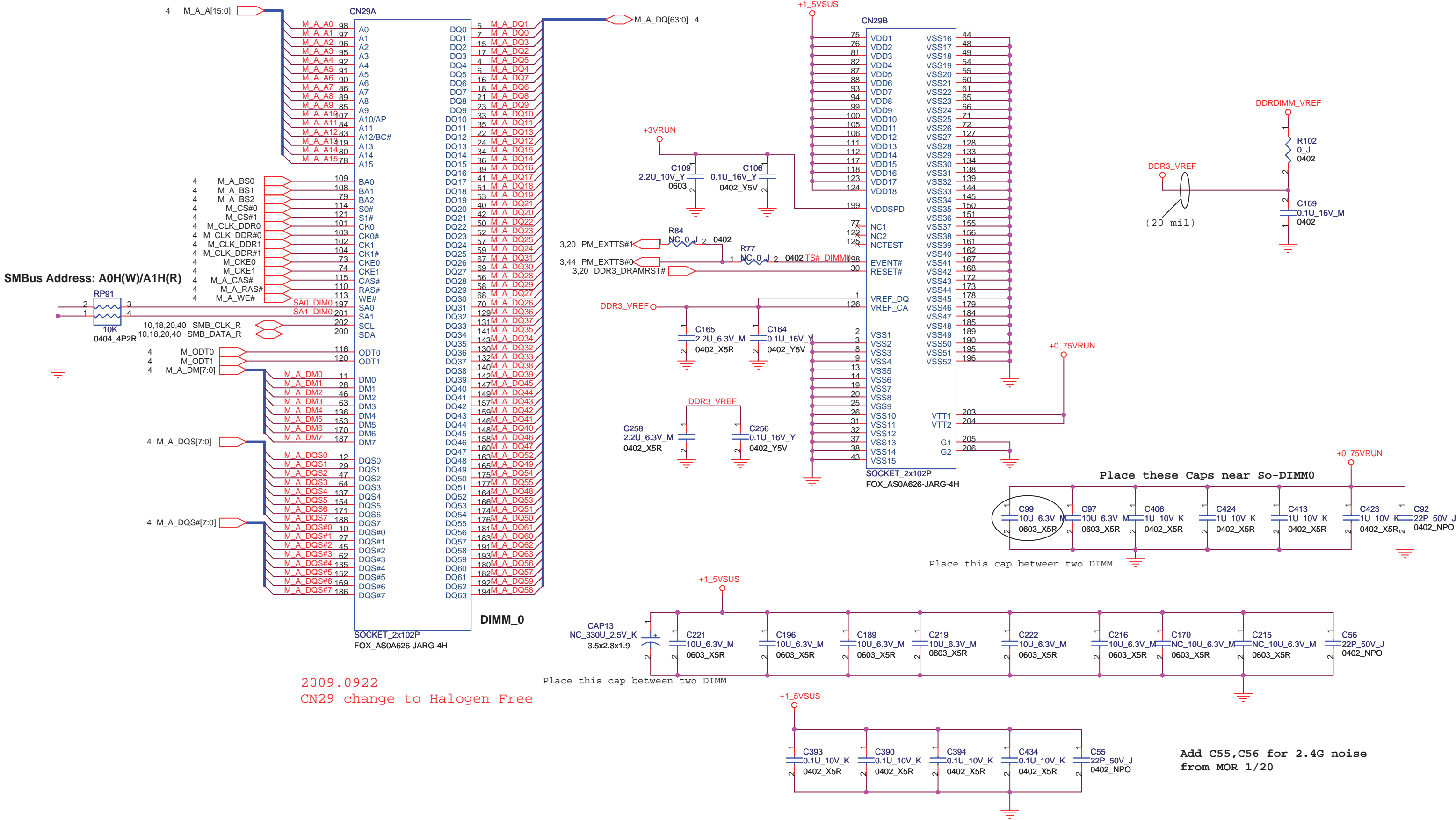
SMBUS Address: 11010010 (D2h)

For N11M, SILEGO -SLG8SP585VTR (1F-GSLG8SP-5800)
For N11P, SLI -SL28748ELC (1F-GSL2874-8E00)
Check it by Model bit0

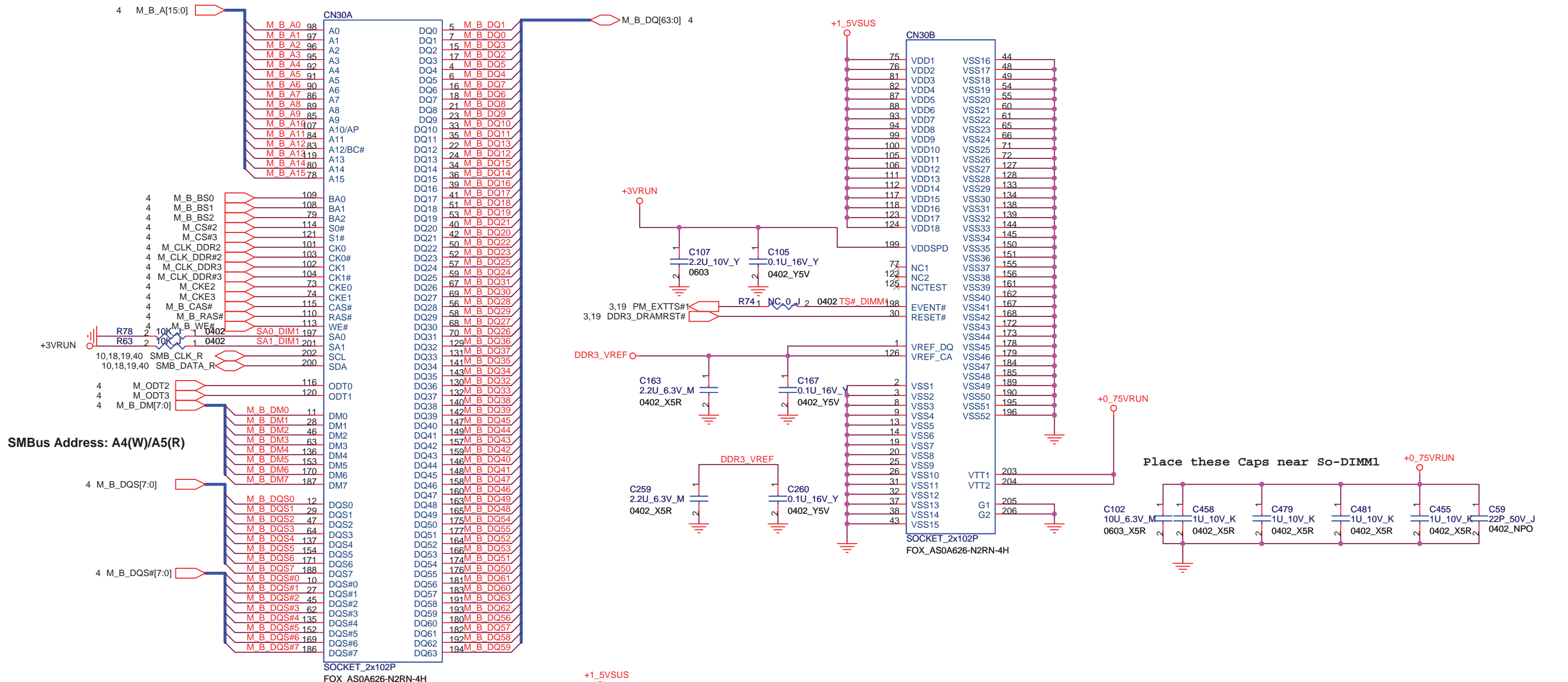
Frequency Select Pin (FS)

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						





2009.0922
CN29 change to Halogen Free

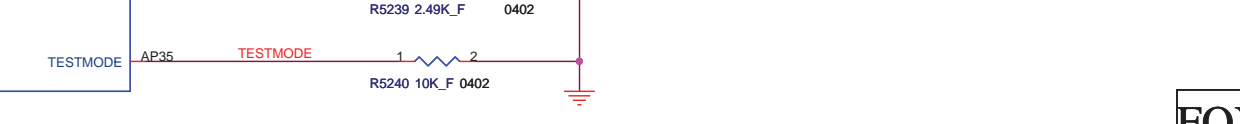
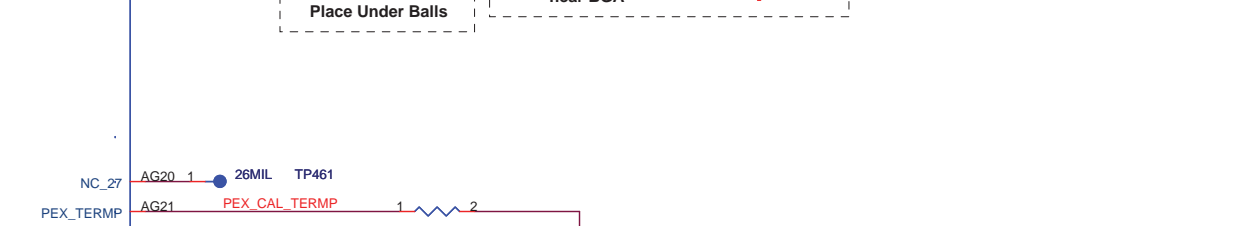
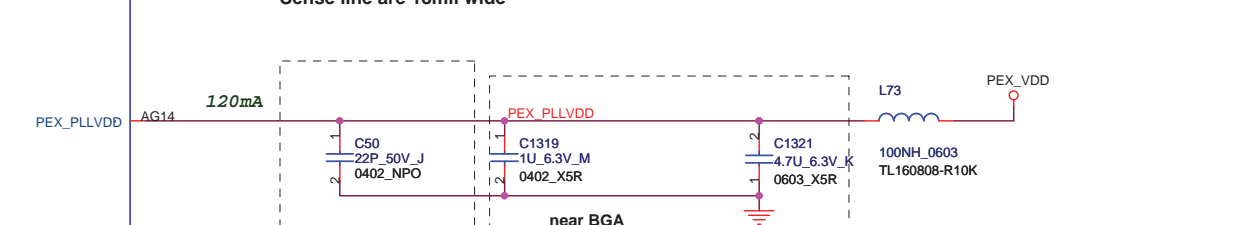
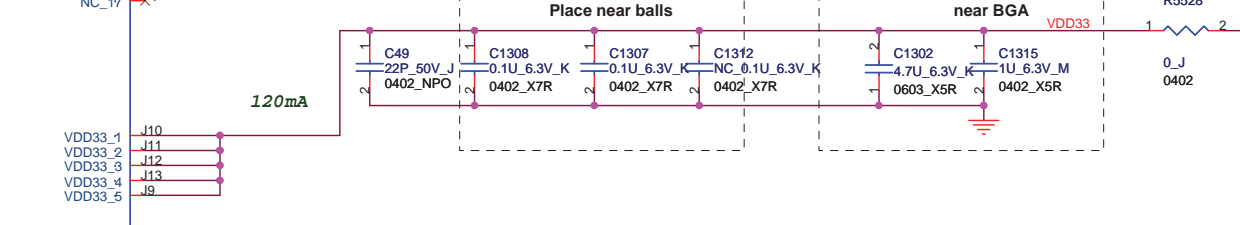
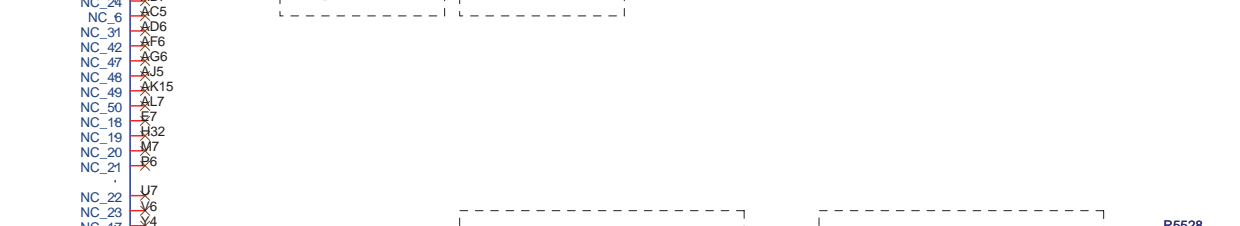
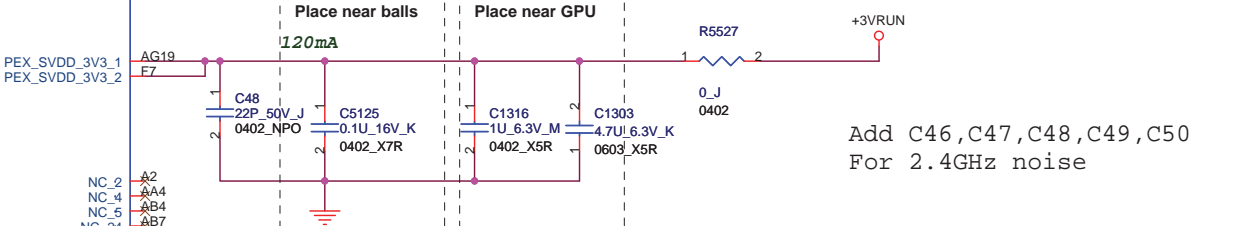
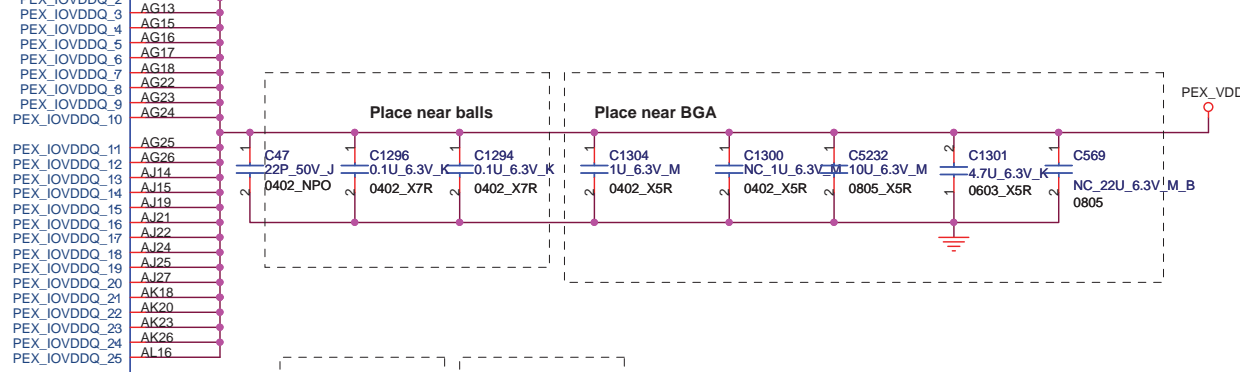
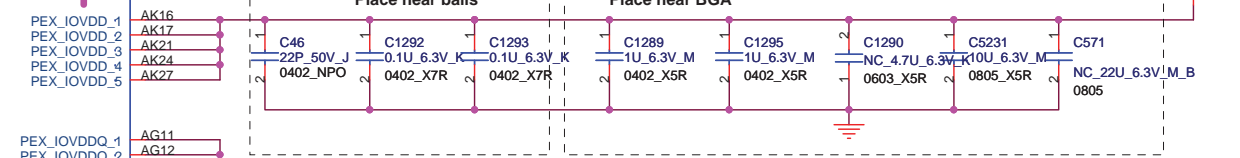
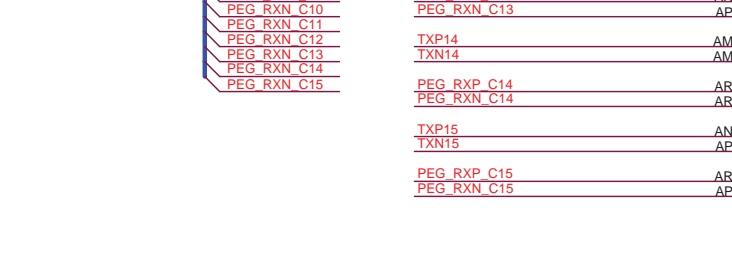
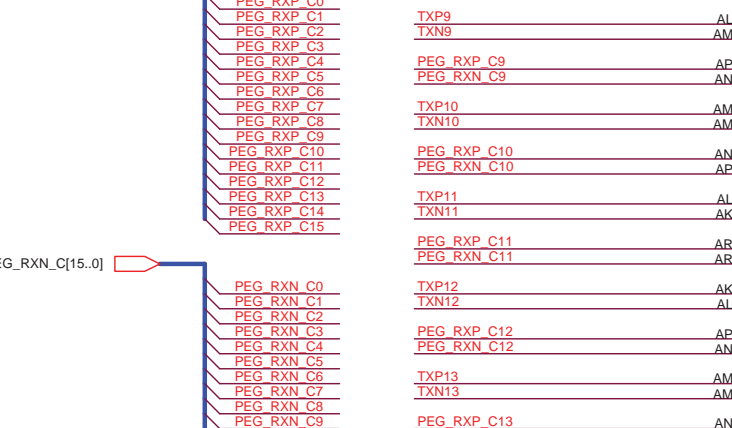
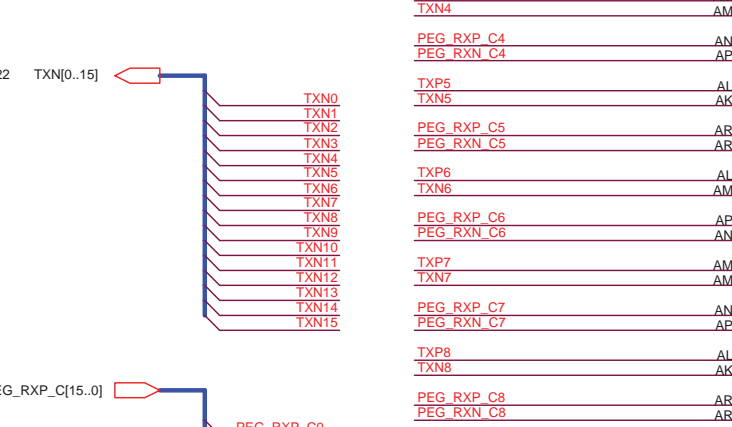
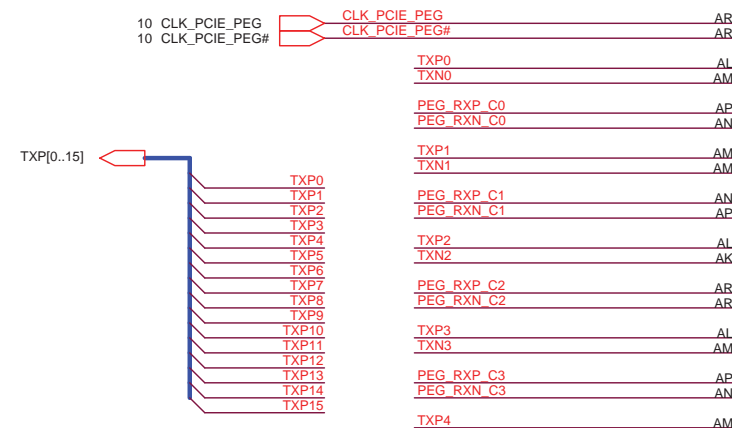
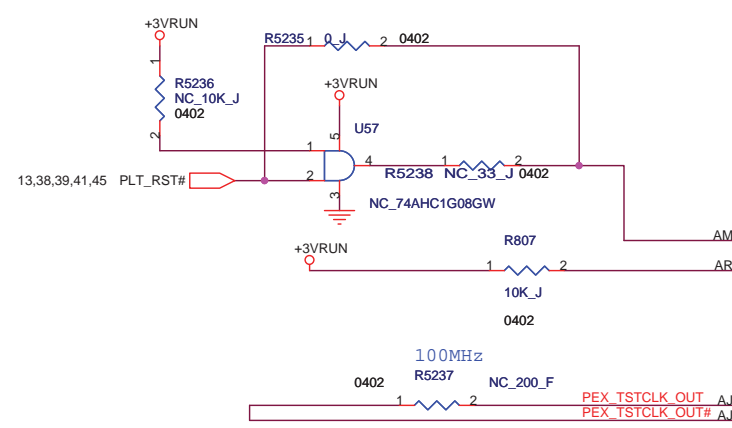
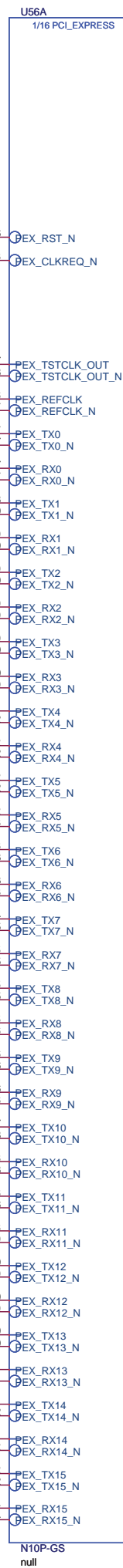


SMBus Address: A4(W)/A5(R)

2009.0922
CN30 change to Halogen Free

Place these Caps near So-DIMM1

Add C57,C58 for 2.4G noise from MOR 1/20



Add C46, C47, C48, C49, C50
For 2.4GHz noise

Sense line are 18mil wide

GPU: N11P_LP1_A3 version 12-N11PLP1-0001
N11M_GE1_A3 version 12-N11MGE1-0001

FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title VGA (PCI EXPRESS) 1 OF 9		
Size	Document Number	Rev
Custom	M9A0_MP	1.1
Date:	Thursday, November 19, 2009	Sheet 21 of 73

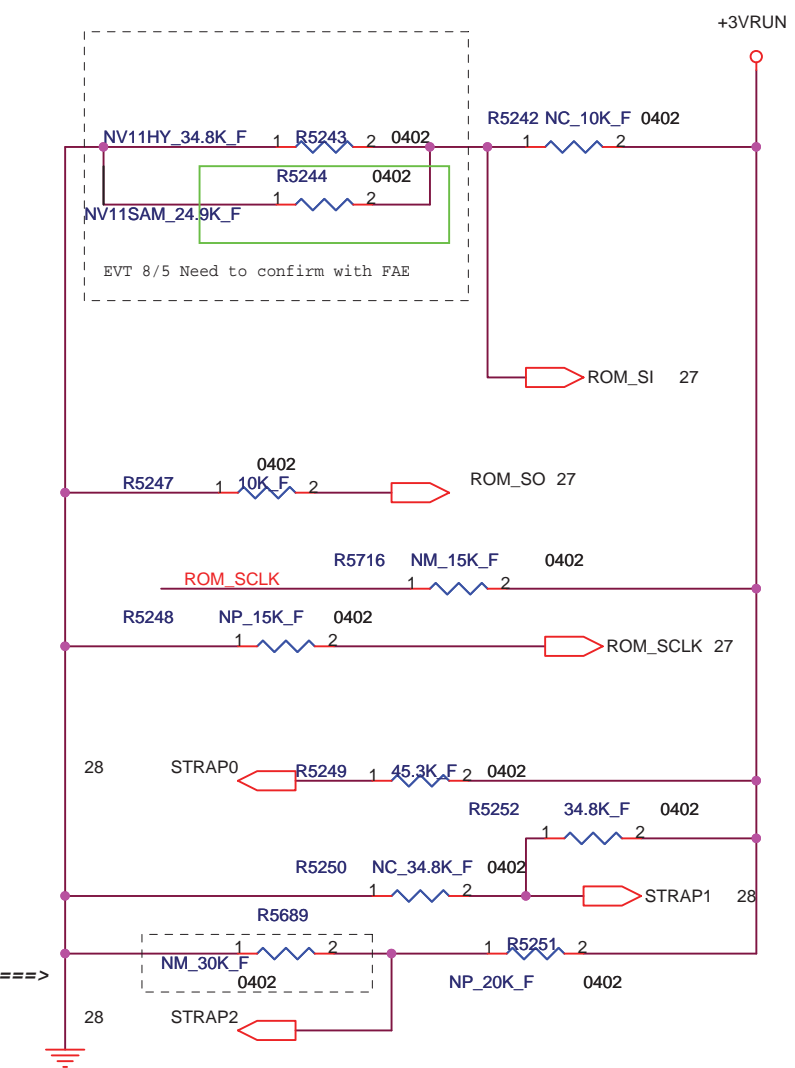


XCLK_417 0 (27M Hz) 1 (Reserved) FB_0_BAR_SIZE 0 256MB 1 (Reserved) SMB_ALT_ADDR 0 0x9E 1 0x9C(multi-GPU usage) VGA_DEVICE 0 3D device(class code 302h) 1 VGA device(class code 300h)	ROM_SO 0001
SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present)	ROM_SCLK N11P-LP1 0010 N11M-GE1 1010
SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk)	
PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	
USER[3:0] 1111	STRAP0 (1111)
N10x/N11x 3GIO_PADCFG[3:0] 1110	STRAP1 (1110)
N11X PCI_DEVID[3:0] N11P-LP1 1011b N11M-GE1 0101b PCI DEVICE IDs N11P-LP1 (0x0A2B) N11M-GE1 (0x0A75)	Strap2 N11P-LP1 1011 N11M-GE1 0101

0000 64-bit Reserved
 1110 32Mx32 GDDR3 - 136 ball 64-bit Hynix - 35K pul Low.
 0100 32Mx32 GDDR3 - 136 ball 64-bit Samsung- 25K pull Low
 ROM_SI

8/3 [DVT] Revise the Strap Pin value as FAE provided for DVT Sample.
 - N11M-GE1 x0A75
 - N11P-LP1 0x0A2B

2009/9/10
 N11P-LP1+SANSUNG(H2) SKU and N11M-GE1 +SANSUNG(M2 SKU) need change BOM
 R5244 change from 1R-0004532-F200(45.3K) to 1R-0002492-F200(24.9K) for nVIDIA FAE suggest



Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

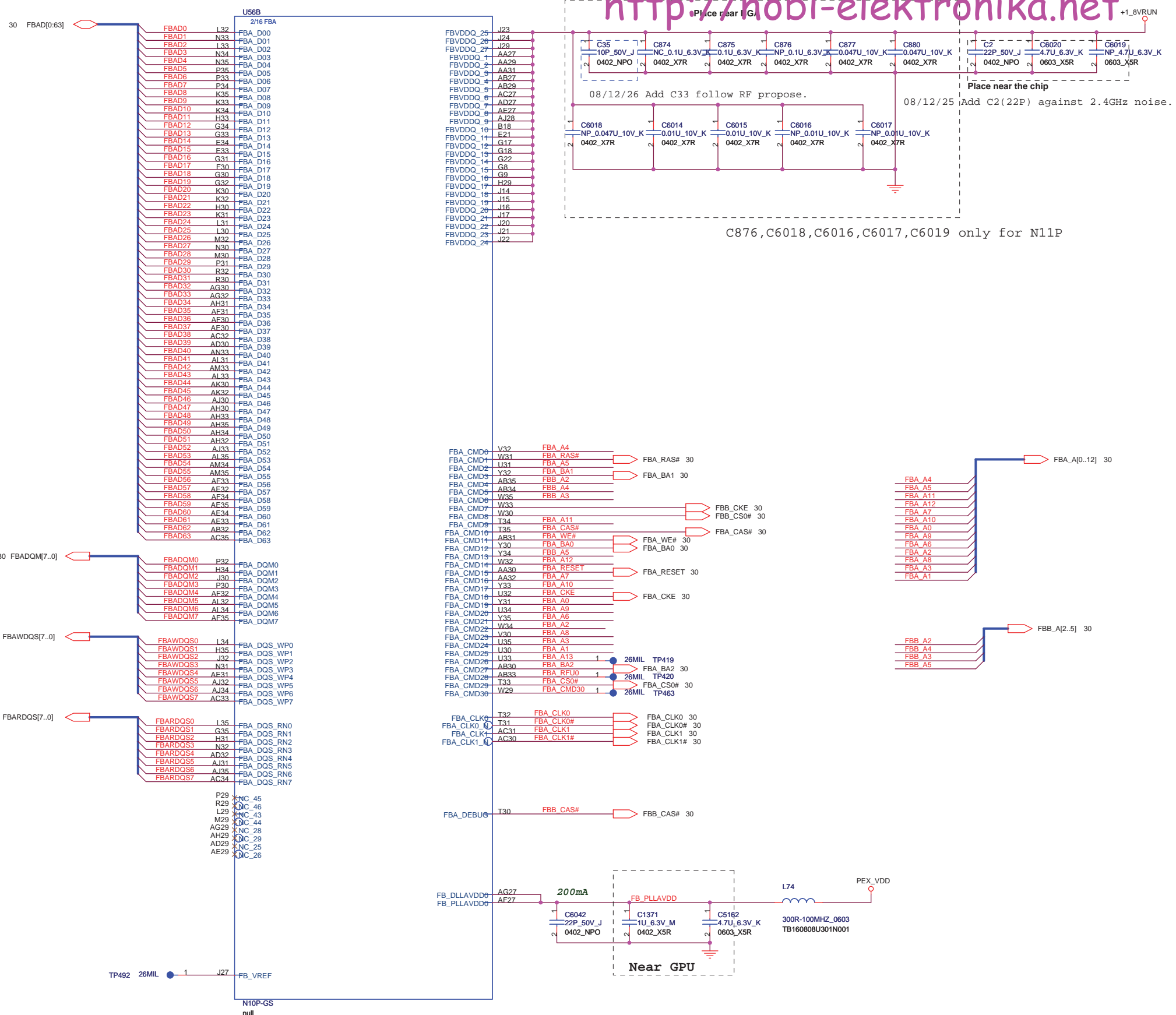
Strap Options

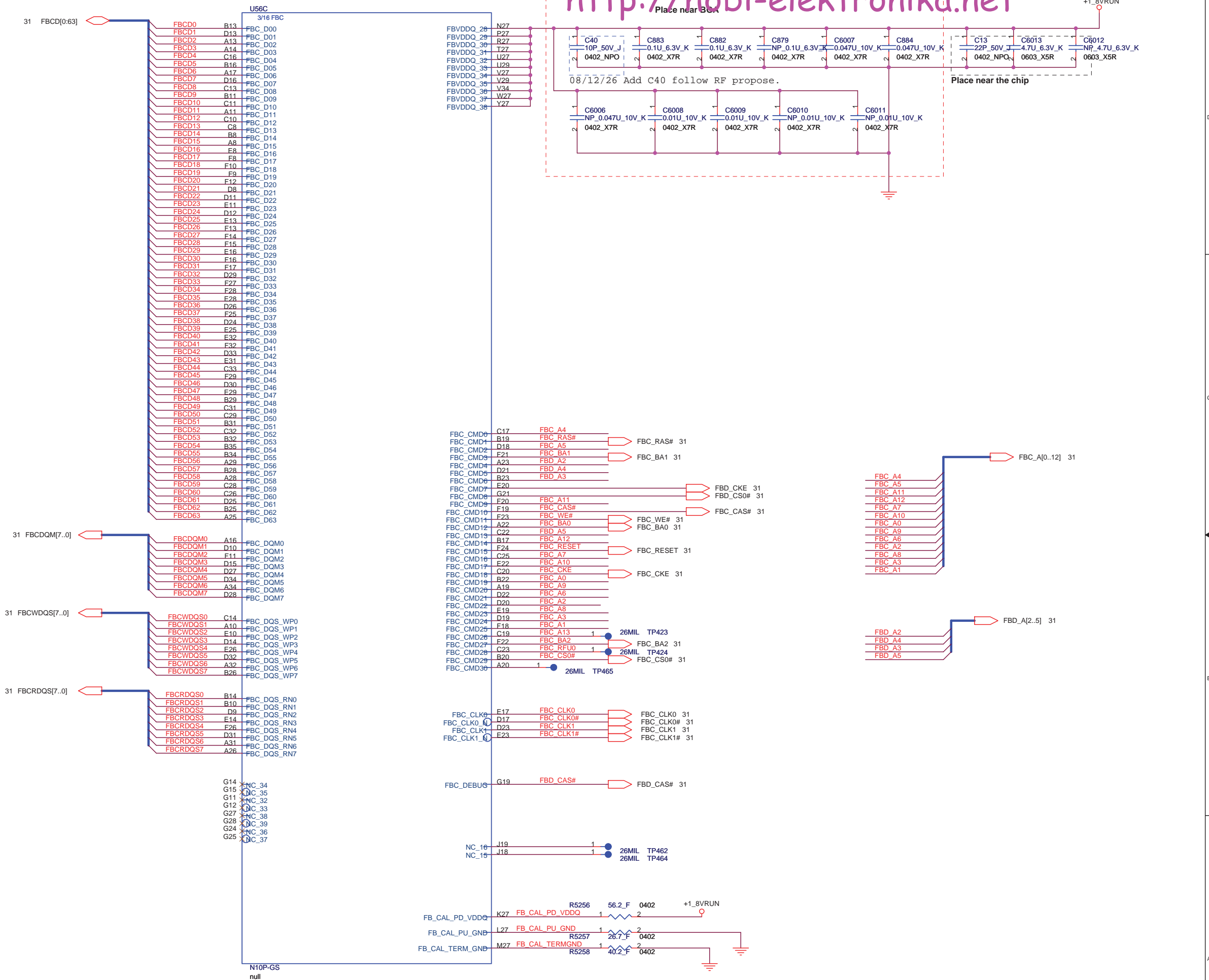
Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

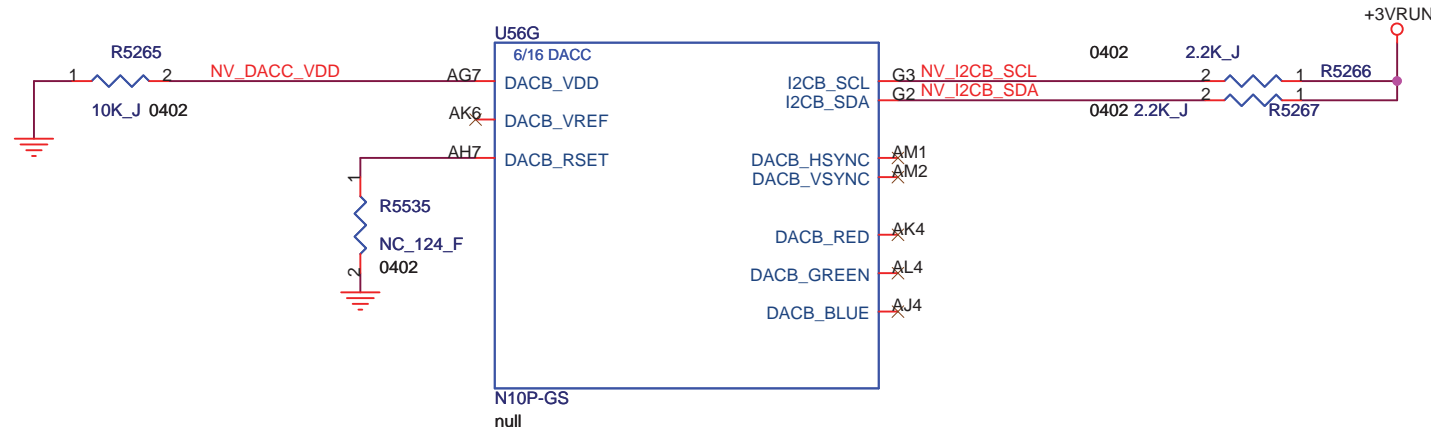
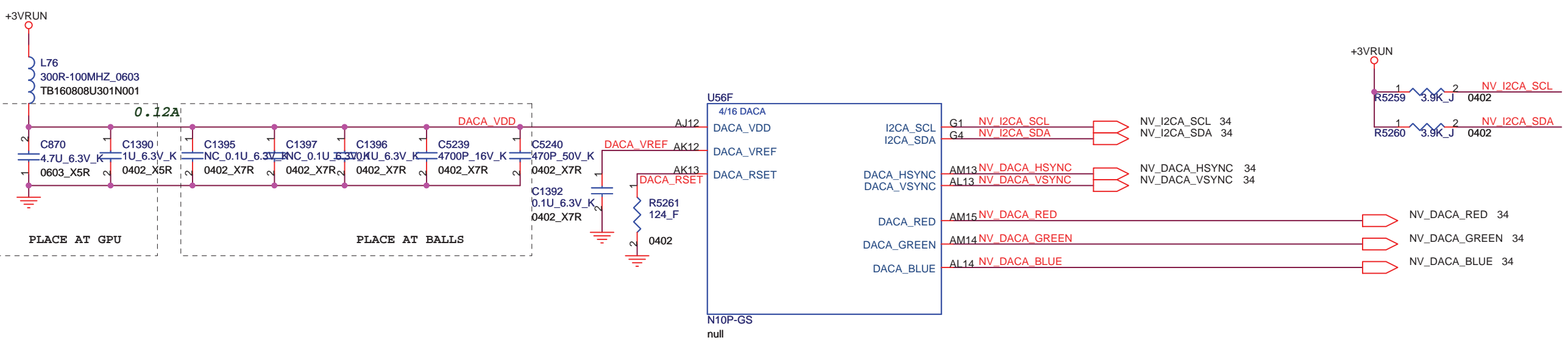
Refer to <GB1 Family Design Guide DG-04642-001_v01_secured>

<http://www.hobi-elektronika.net>

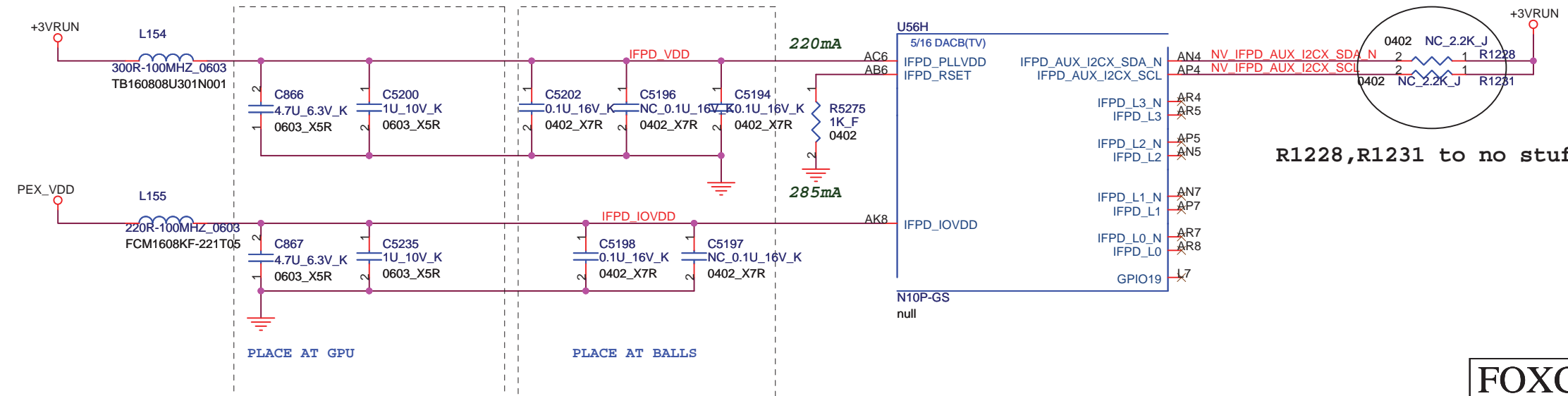
M970 FBVDDQ current N11M_VP1 is 6.5A N11M_GE1 is 3.3A







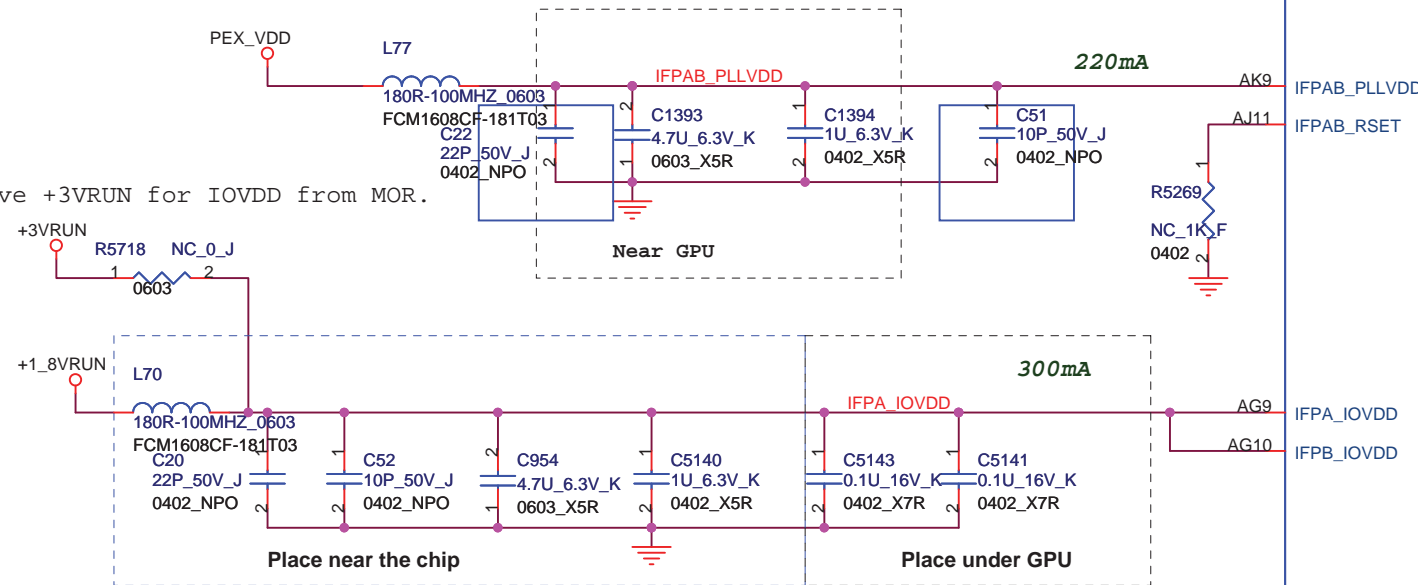
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCLK	SCL
	VGA-DDCDA	SDA



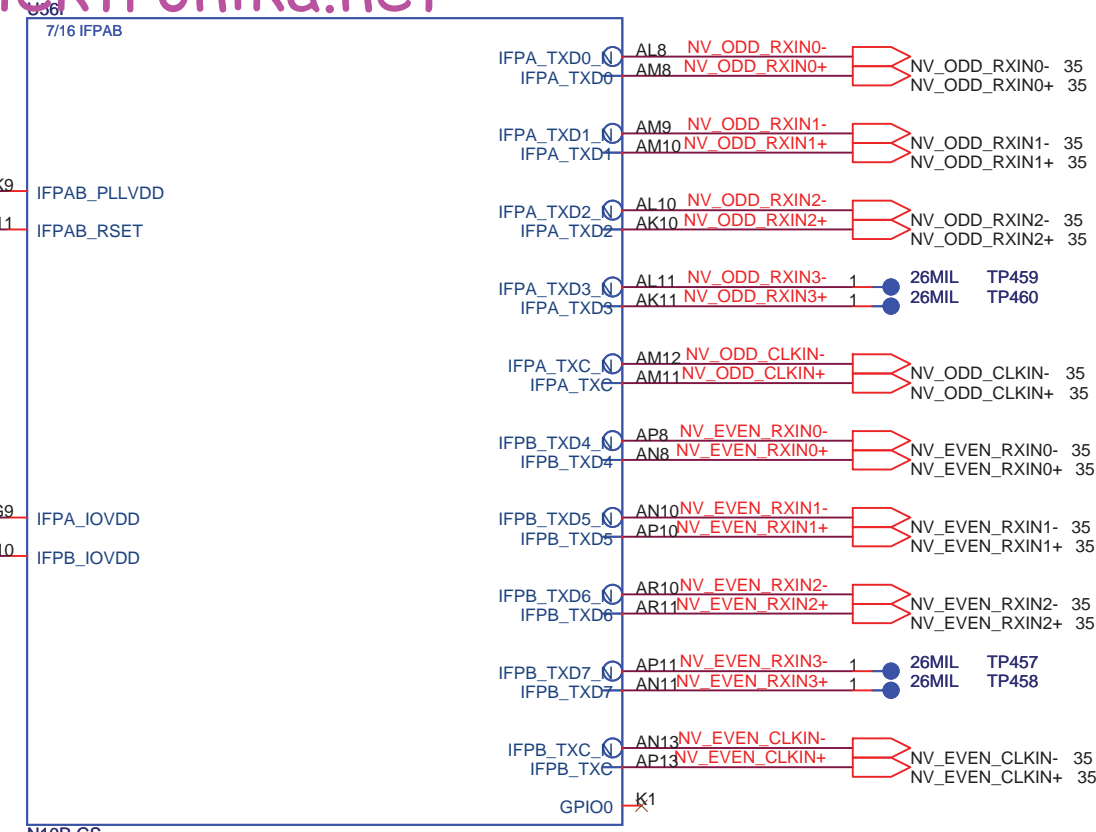
R1228,R1231 to no stuff ---MOR 5/25

08/12/26 Add C51,C52 10p follow RF propose.

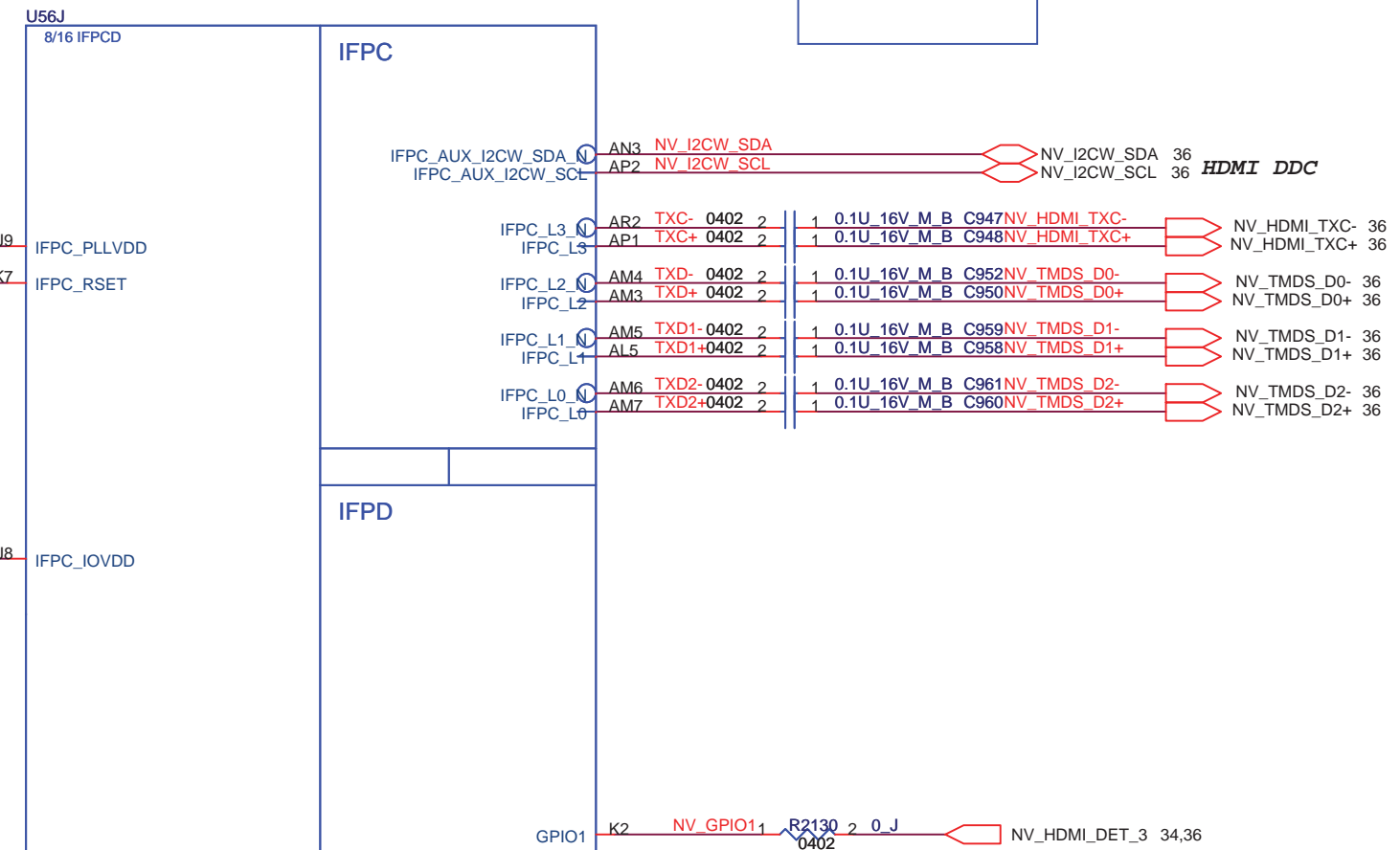
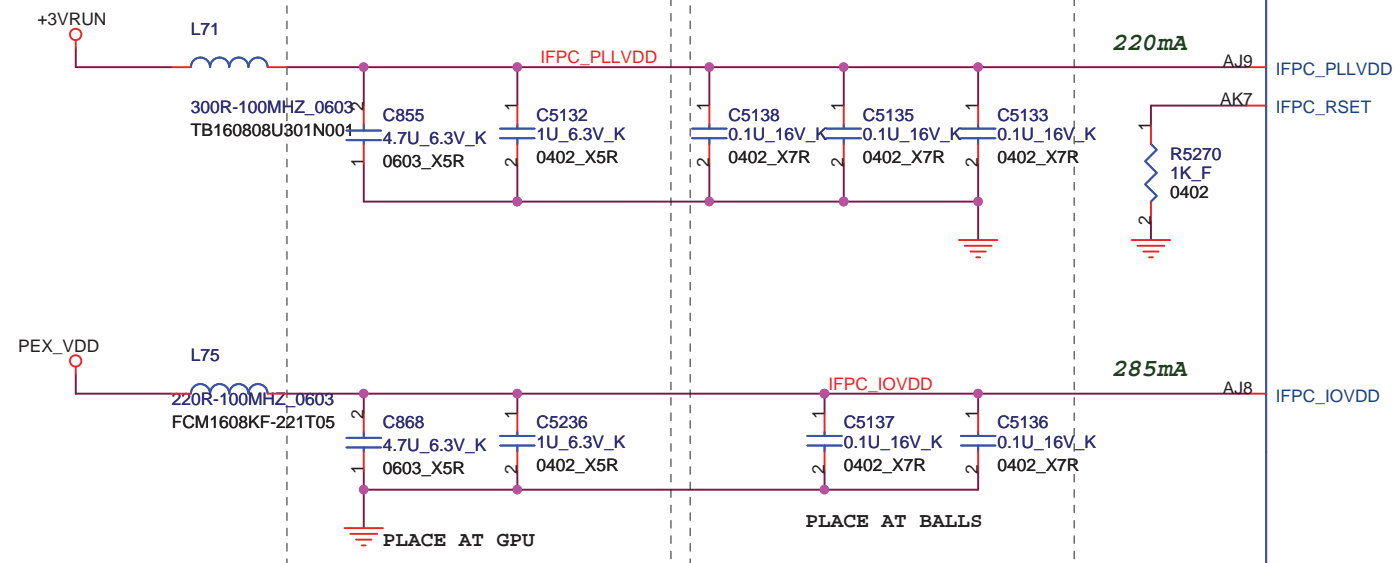
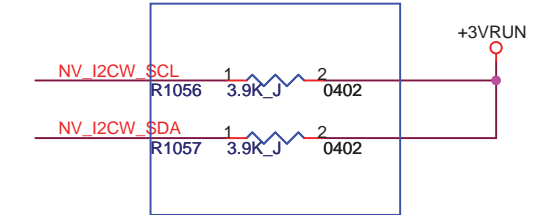
09/02/05 Reserve +3VRUN for IOVDD from MOR.

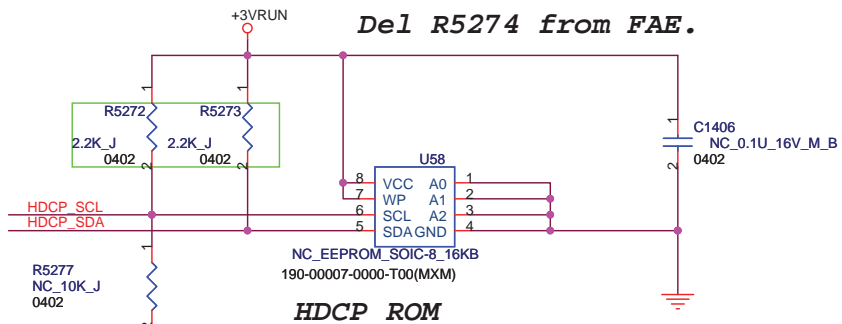


08/12/25 Add C20,C22 against 2.4GHz noise.



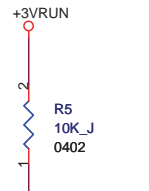
08/12/22 Change R1056,R1057 from 2.2K to 3.9K follow Mor-side propose.



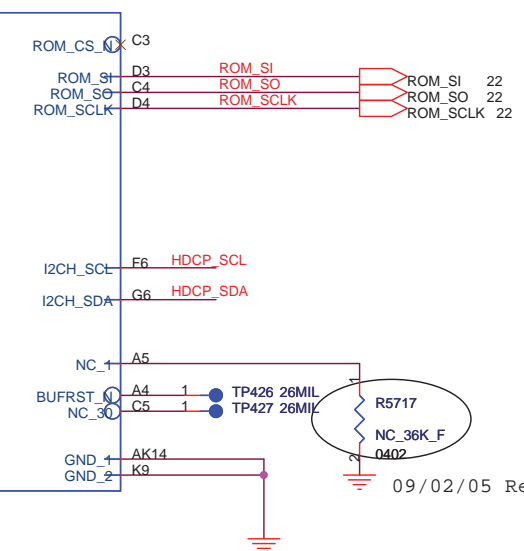


2009.0921
change R5272,R5273 from NC to mount

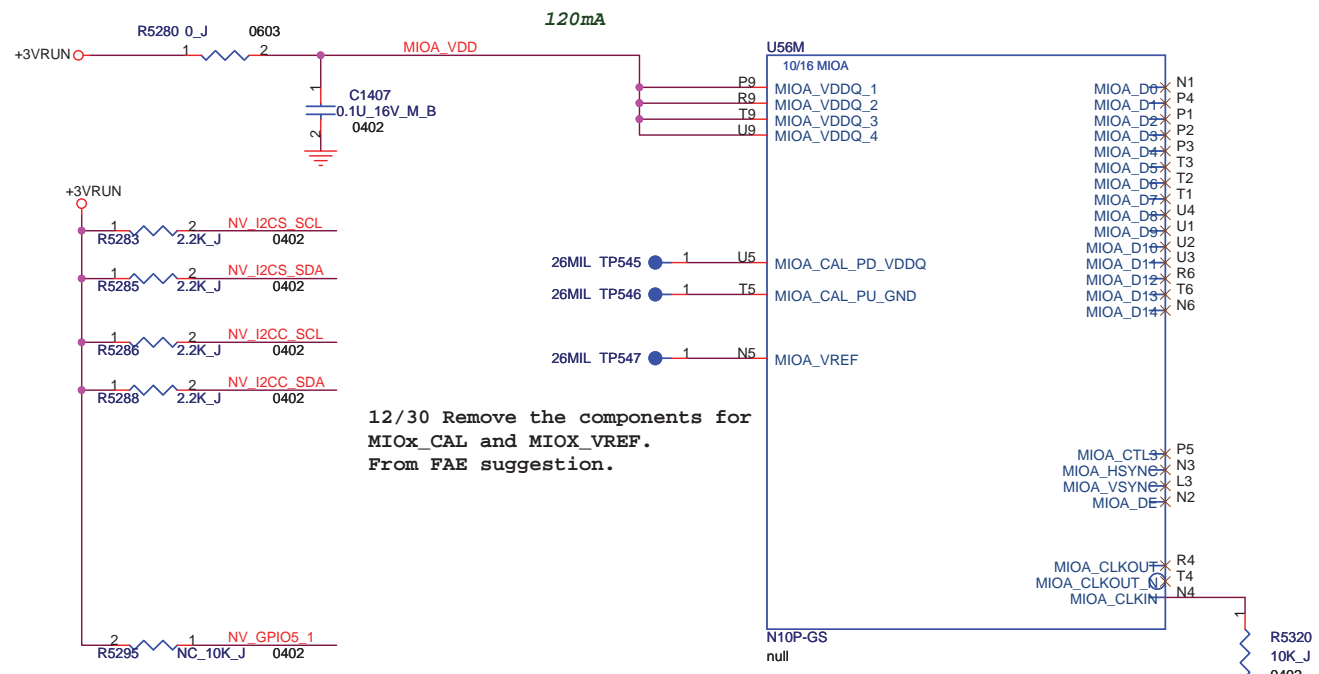
08/12/26 Add R5 follow Mor-side propose.



- 26MIL TP472 1 J26 NC_41
- 26MIL TP473 1 J25 NC_40
- 26MIL TP474 1 D7 NC_11
- 26MIL TP475 1 D6 NC_10
- 26MIL TP476 1 C7 NC_8
- 26MIL TP477 1 B7 NC_7
- 26MIL TP478 1 A7 NC_3

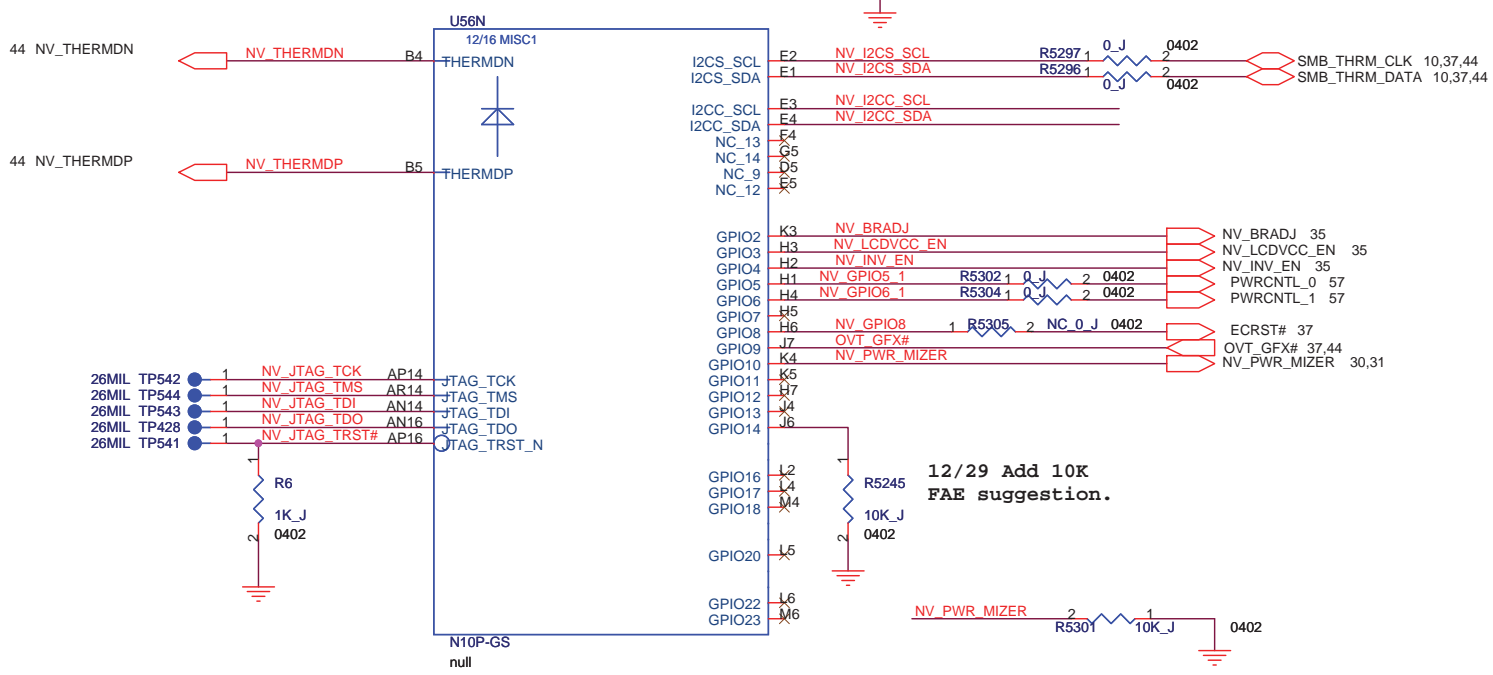
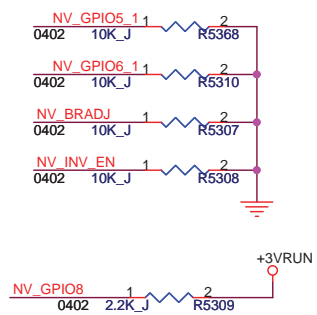


09/02/05 Reserve R5717 follow Mor-side propose.



12/30 Remove the components for MIOx_CAL and MIOx_VREF. From FAE suggestion.

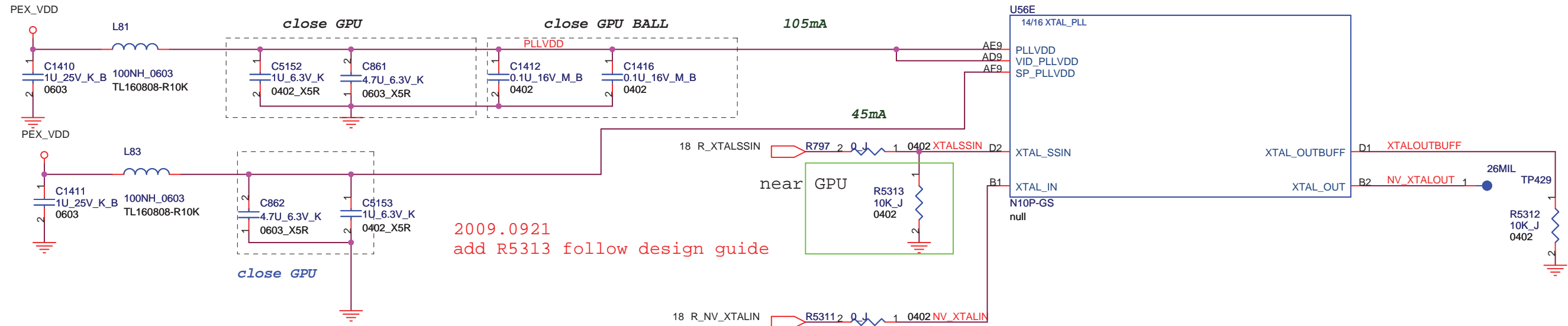
12/29 Add R5310 10K FAE suggestion.



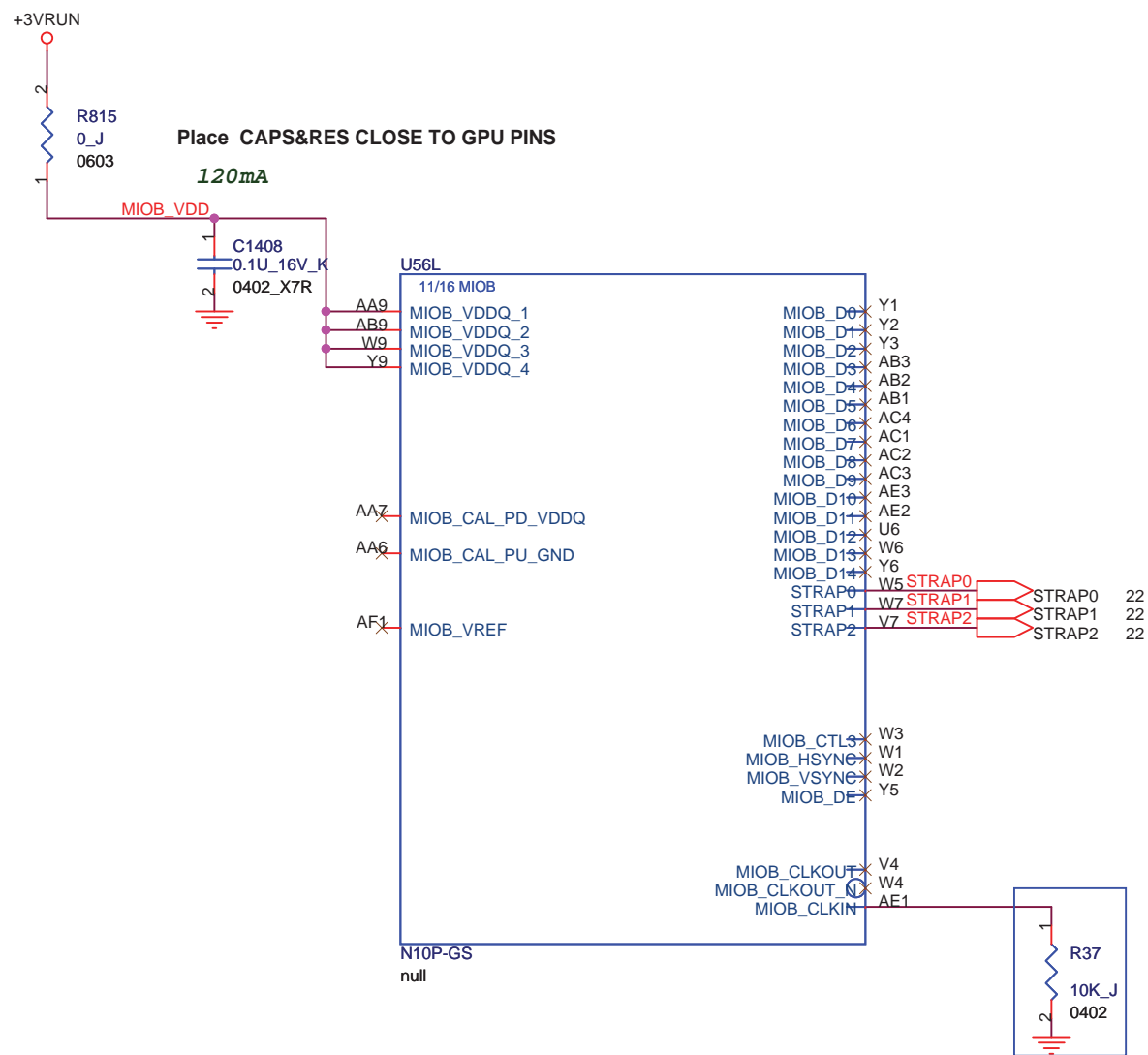
12/29 Add 10K FAE suggestion.

GPIO	I/O	Internal pull low	GPIO TABLE
GPIO0	I	YES	
GPIO1	I	Yes	HDMI Hot Plug Detect 0(HPD0) Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM) Active High
GPIO3	O	No	Panel Power(LCD0_VDD) Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN) Active High
GPIO5	O	Yes	FOR Power Control NVDD
GPIO6	O	No	FOR Power Control NVDD
GPIO8	O	No	reserve for reset EC
GPIO9	I	No	System Power Limit Alert Input Active Low

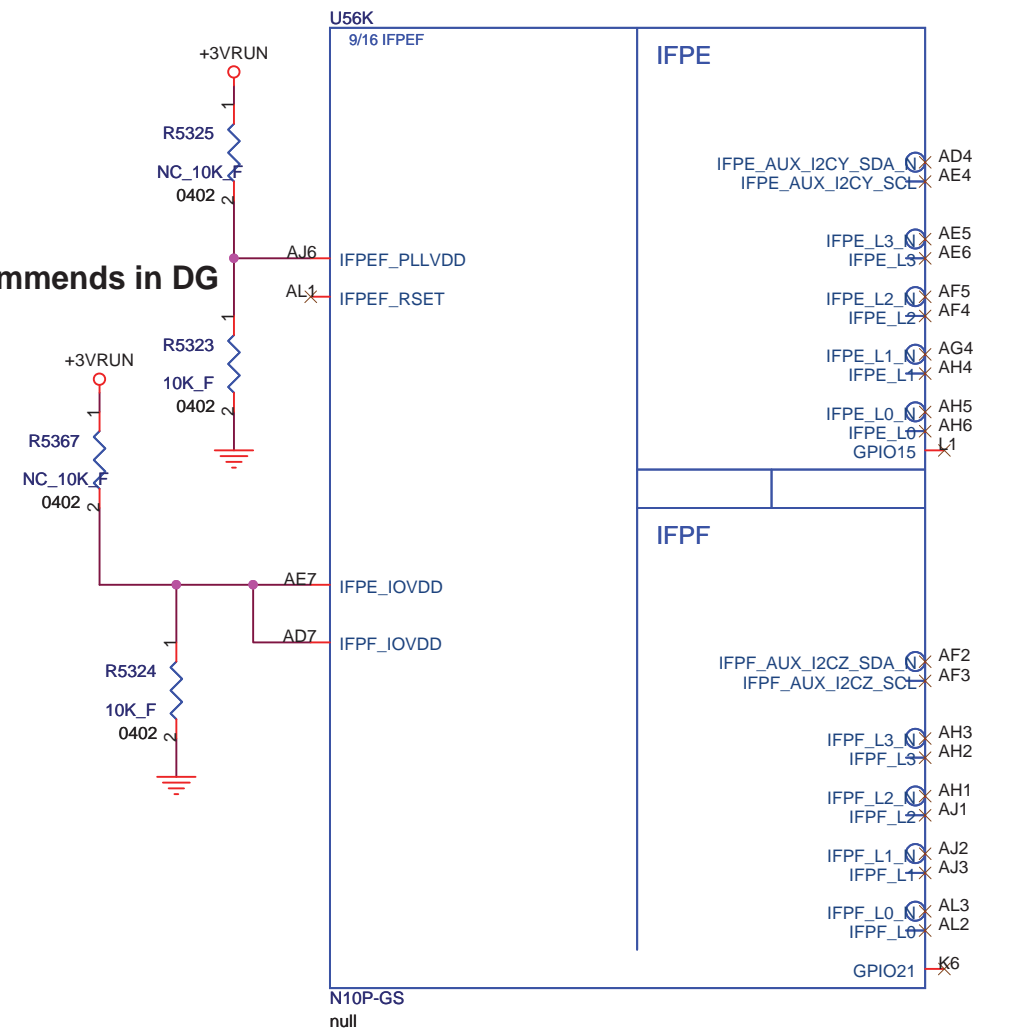
SIGNAL	I/O	Description
I2CA_SCL	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL	I/O	For VGA thermal I2C_Compatibal Bus Signals.
I2CS_SDA	I/O	Support a direct interface to the internal temperature sensor



2009.0921
add R5313 follow design guide

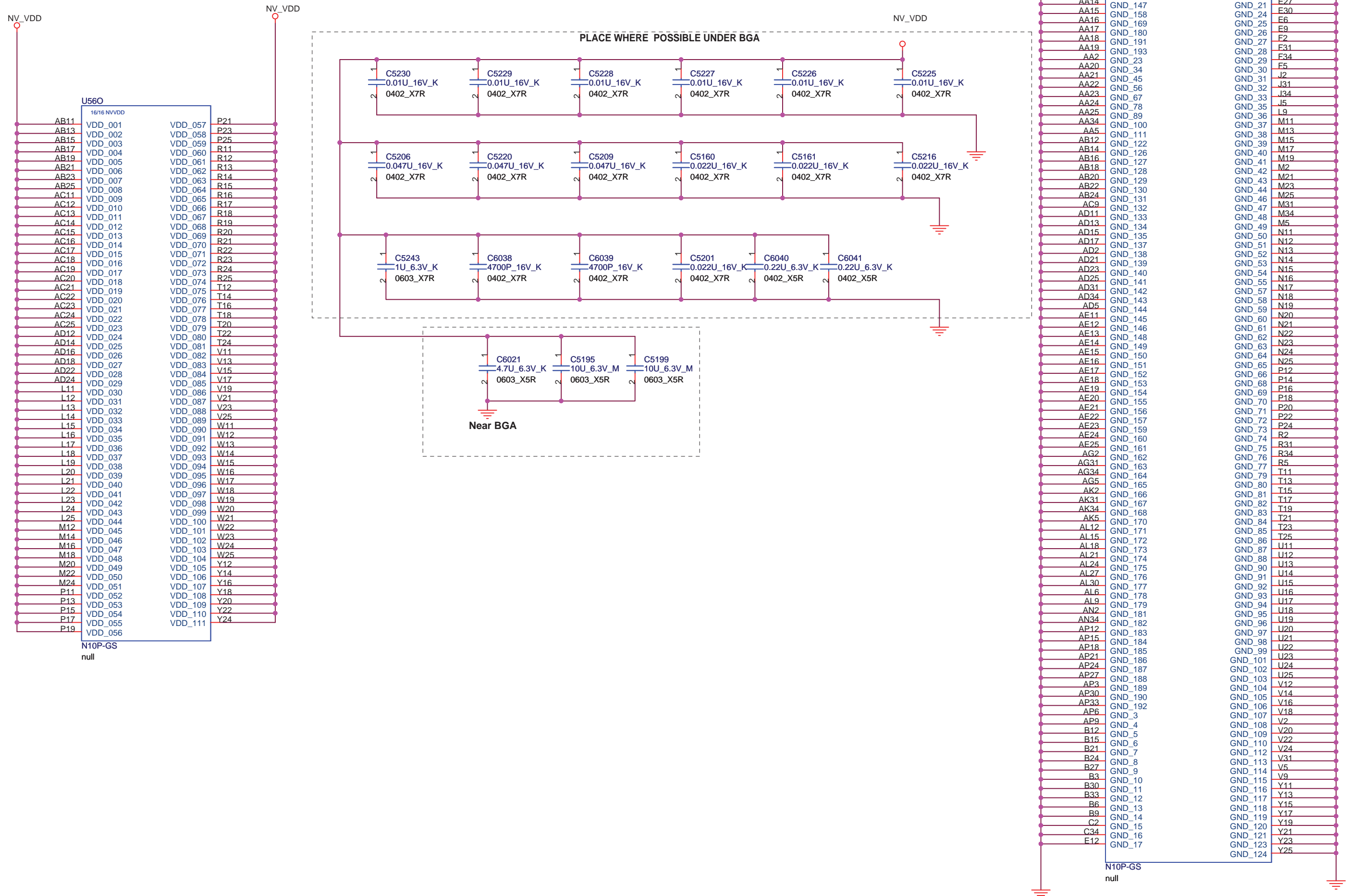


NVIDIA recommends in DG



M9A0 NVVDD current N11P_LP1 is 21.94A

N11M_GE1 is 16.29A

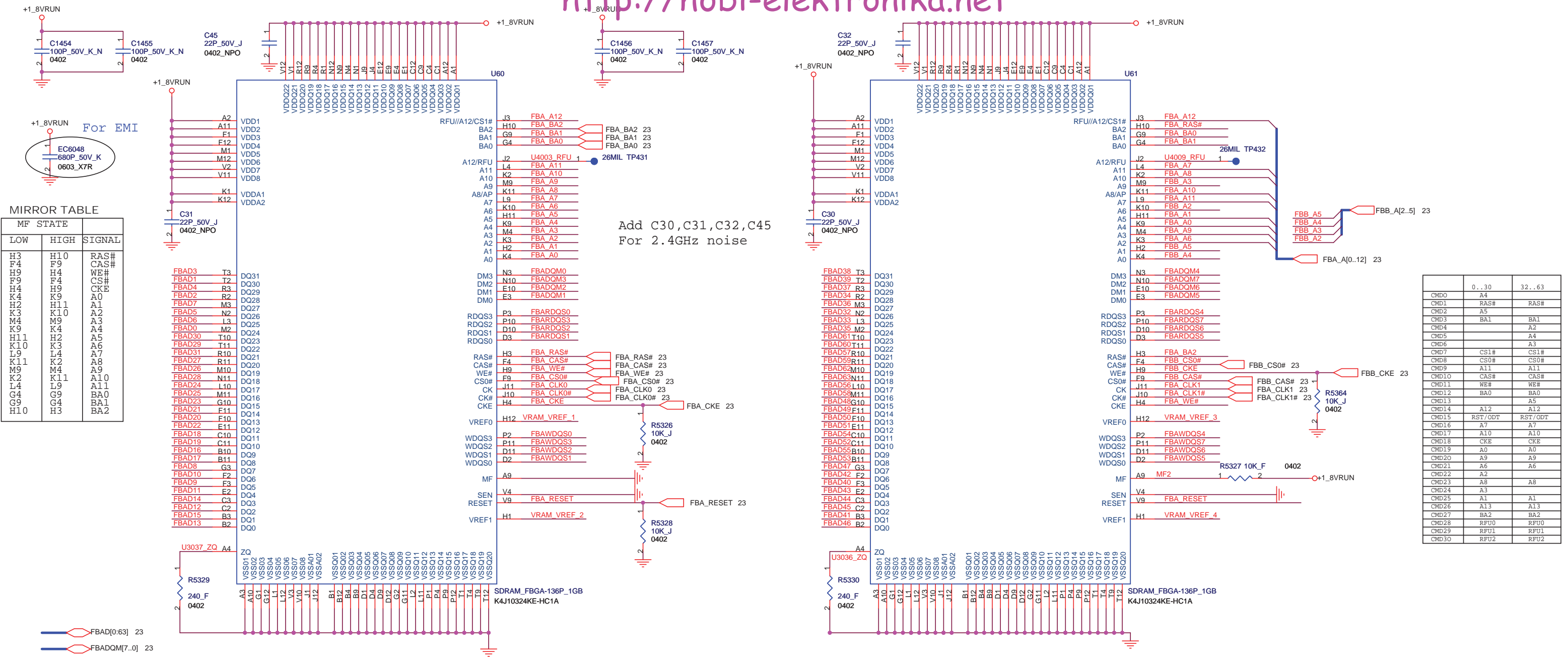


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **VGA(POWER/GROUND) 9/9**

Size: A3	Document Number: M9A0_MP	Rev: 1.1
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Date: Tuesday, November 03, 2009 Sheet 29 of 73



MIRROR TABLE

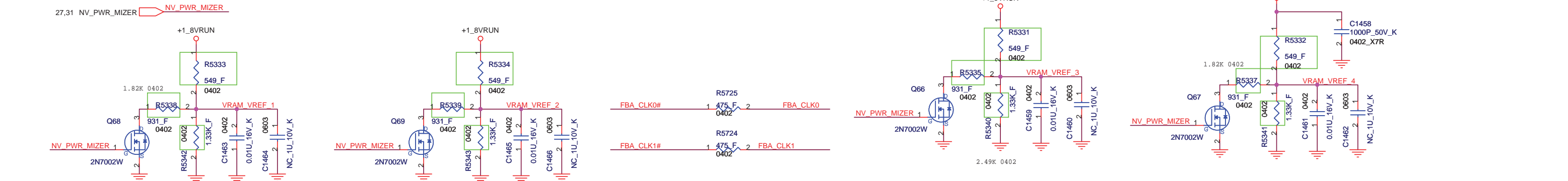
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
L4	L9	A10
G4	G9	A11
G9	G4	BA0
H10	H3	BA1
		BA2

	0..30	32..63
CMDO	A4	RAS#
CMO1	RAS#	RAS#
CMO2	A5	
CMO3	BA1	BA1
CMO4		A2
CMO5		A4
CMO6	CS1#	CS1#
CMO8	CS0#	CS0#
CMO9	A11	A11
CMO10	CAS#	CAS#
CMO11	WE#	WE#
CMO12	BA0	BA0
CMO13		A5
CMO14	A12	A12
CMO15	RST/ODT	RST/ODT
CMO16	A7	A7
CMO17	A10	A10
CMO18	CKE	CKE
CMO19	A0	A0
CMO20	A9	A9
CMO21	A6	A6
CMO22	A2	A2
CMO23	A8	A8
CMO24	A3	A3
CMO25	A1	A1
CMO26	A13	A13
CMO27	BA2	BA2
CMO28	RFU0	RFU0
CMO29	RFU1	RFU1
CMO30	RFU2	RFU2

Add C30,C31,C32,C45
For 2.4GHz noise

SAMSUNG Vendor PN : K4J10324KE-HC1A HHPN : 13-K4J1032-3006
 HYNIX Vendor PN : H5RS1H23MFR-N0C HHPN : 13-H5RS1H2-3001

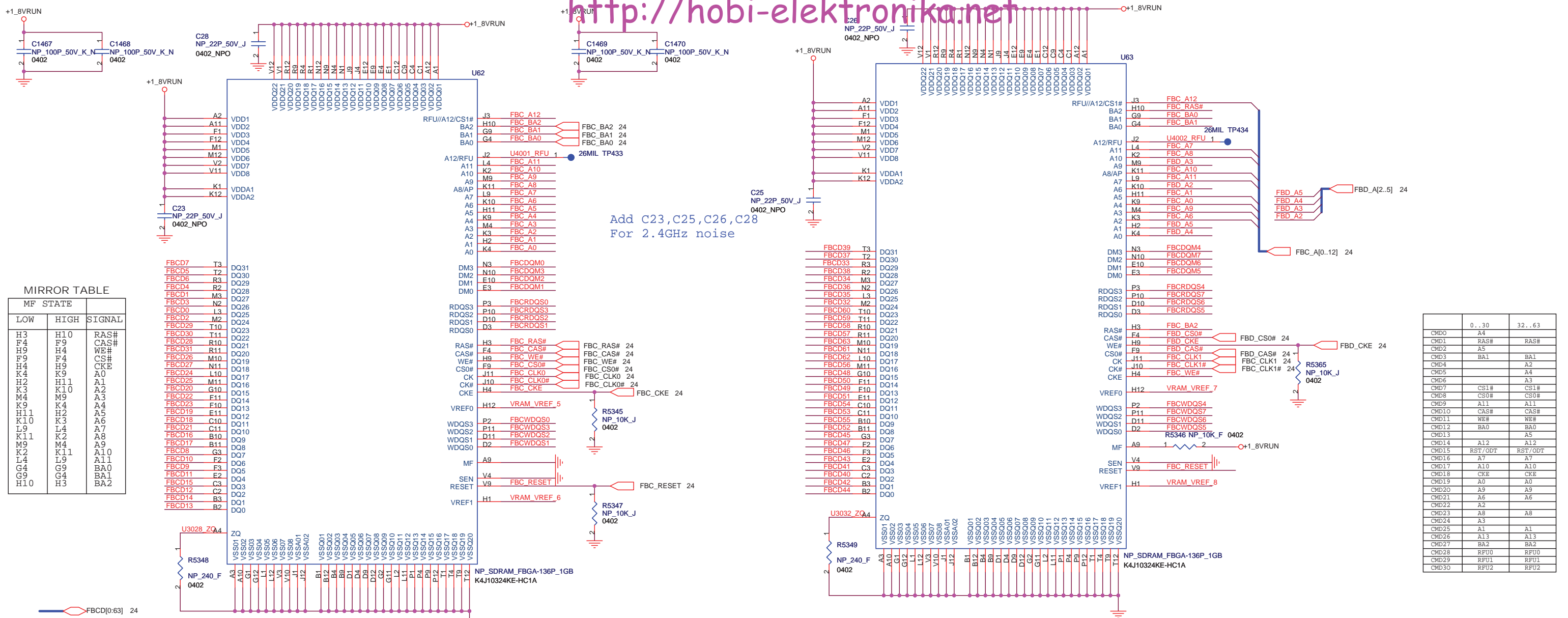
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



2009/9/10
 N11P-LP1+SAMSUNG(H2 SKU)
 Change R5340,R5341,R5342,R5343 from
 1R-0001331-F200(1.33K) to 1R-0000222-J200(2.2K)
 for nVIDIA FAE suggest.

2009/9/10
 N11P-LP1+SAMSUNG(H2 SKU)
 Change R5331,R5332,R5333,R5334 from
 1R-0005490-F200(549ohm) to 1R-0009310-F200(931ohm)
 for nVIDIA FAE suggest.

2009/9/10
 N11P-LP1+SANSUNG(H2 SKU)
 Change R5335,R5337,R5338,R5339 from
 1R-0009310-F200(931ohm) to 1R-0000122-F200(1.2K)
 for nVIDIA FAE suggest.



MIRROR TABLE

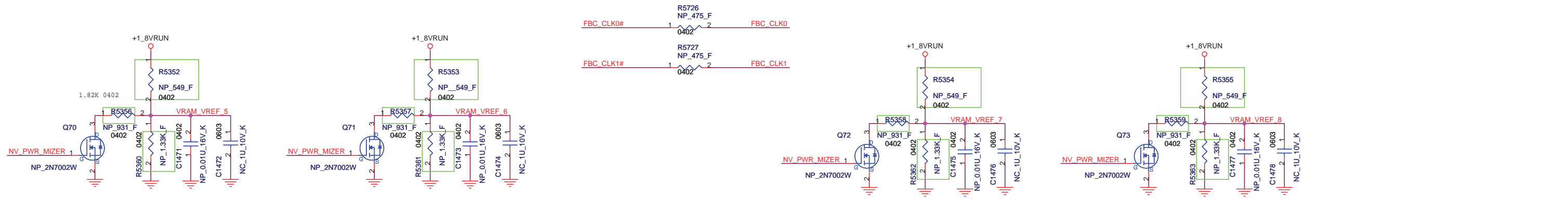
MF STATE	LOW	HIGH	SIGNAL
H3	H10	RAS#	
F4	F9	CAS#	
H9	H4	WE#	
F9	F4	CS#	
H4	H9	CK#	
K4	K9	A0	
H2	H11	A1	
K3	K10	A2	
M4	M9	A3	
K9	K4	A4	
H11	H2	A5	
K10	K3	A6	
L9	L4	A7	
K11	K2	A8	
M9	M4	A9	
K2	K11	A10	
L4	L9	A11	
G4	G9	BA0	
G9	G4	BA1	
H10	H3	BA2	

	0..30	32..63
CMD0	B4	
CMD1	RAS#	RAS#
CMD2	A5	BA1
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

SAMSUNG Vendor PN : K4J10324KE-HC1A HHPN : 13-K4J1032-3006
 HYNIX Vendor PN : H5RS1H23MFR-N0C HHPN : 13-H5RS1H2-3001

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

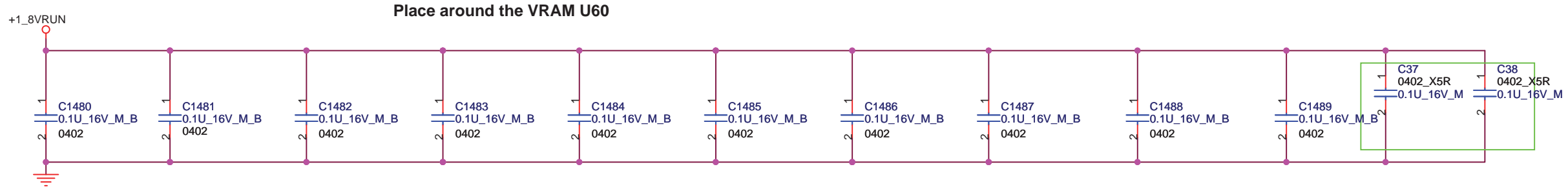
27.30 NV_PWR_MIZER NV_PWR_MIZER



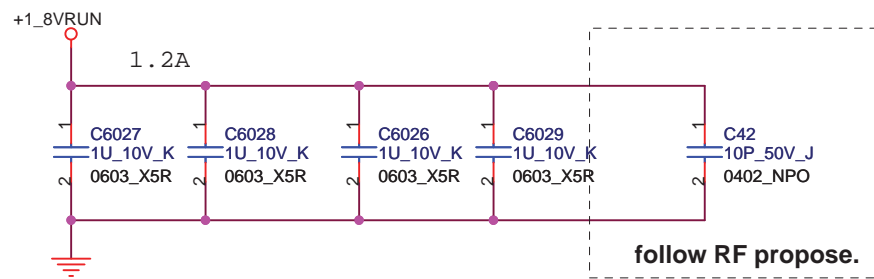
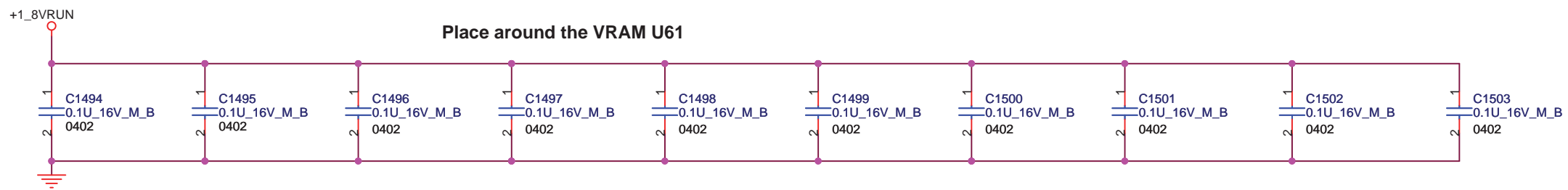
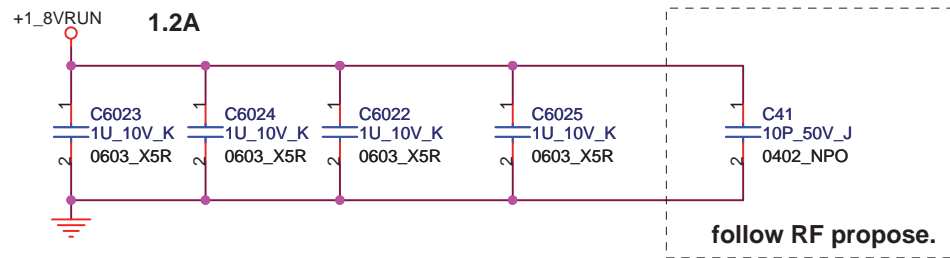
2009/9/10
 N11P-LP1+SAMSUNG(H2 SKU)
 Change R5356,R5357,R5358,R5359 from 1R-0009310-F200(931ohm) to 1R-000122-F200(1.2K) for nVIDIA FAE suggest.

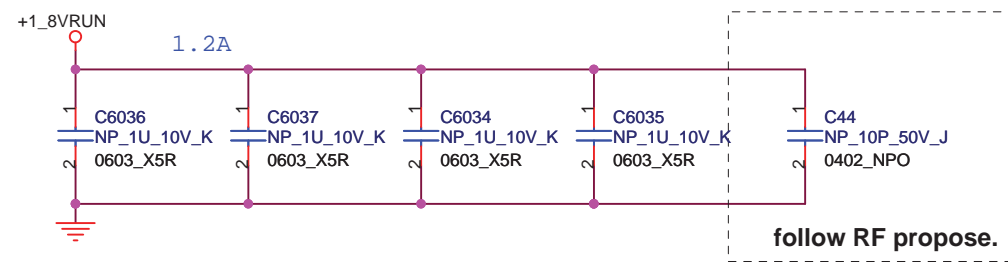
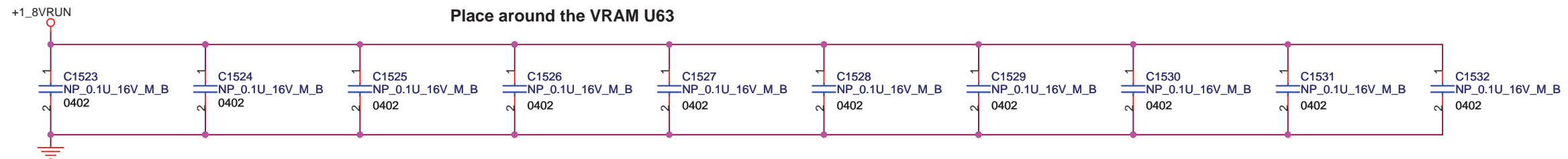
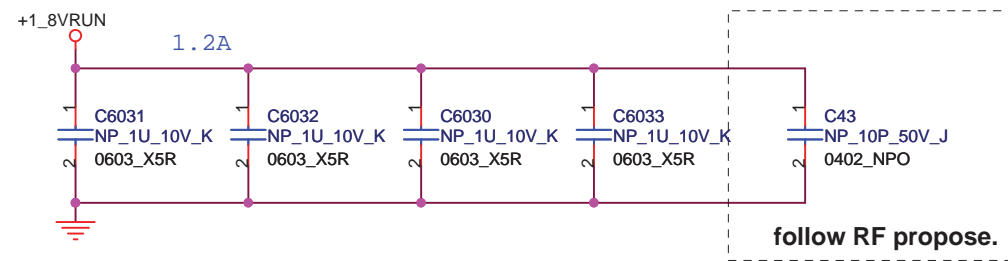
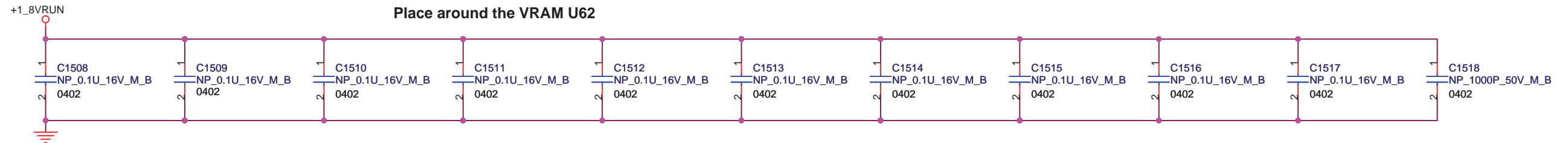
2009/9/10
 N11P-LP1+SAMSUNG(H2 SKU)
 Change R5352,R5353,R5354,R5355 from 1R-0005490-F200(549ohm) to 1R-0009310-F200(931ohm) for nVIDIA FAE suggest.

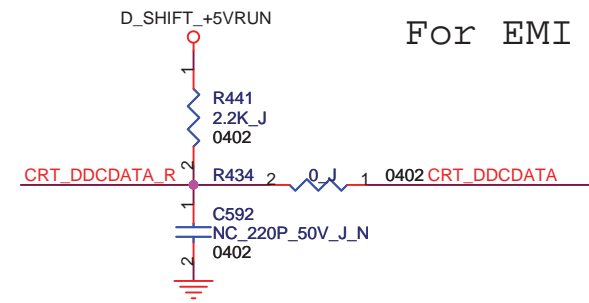
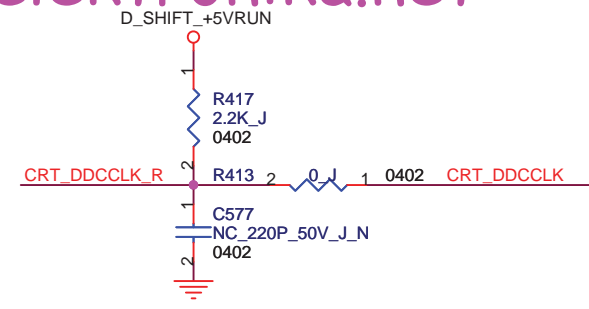
2009/9/10
 N11P-LP1+SAMSUNG(H2 SKU)
 Change R5360,R5361,R5362,R5363 from 1R-0001331-F200(1.33K) to 1R-0000222-J200(2.2K) for nVIDIA FAE suggest.



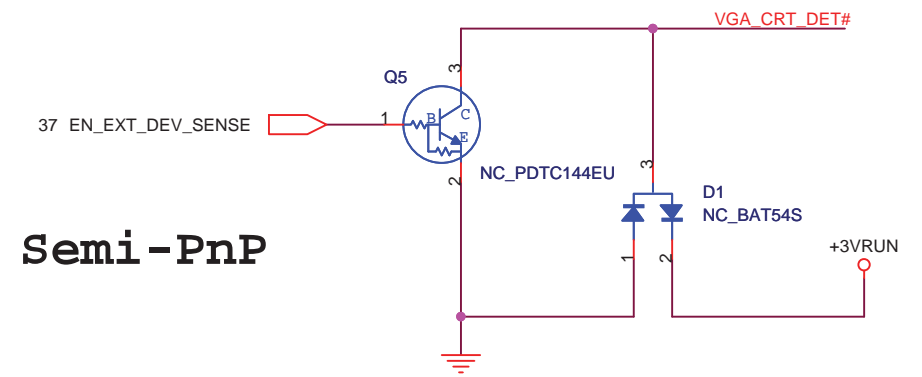
2009.0925
ADD C37,C38 for EMI request





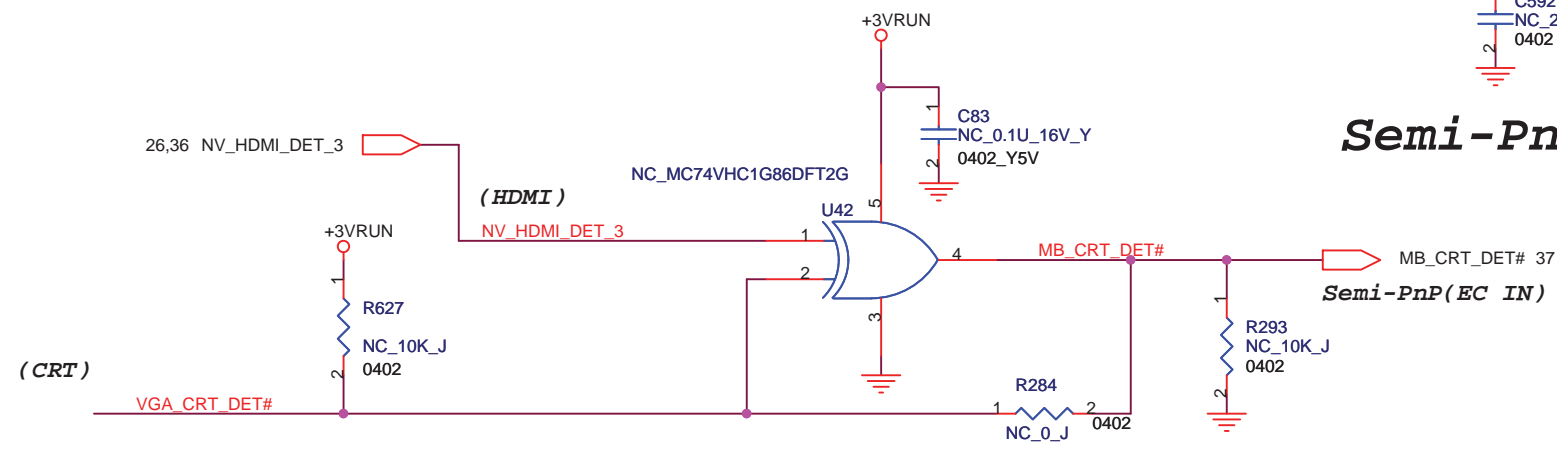


Semi-PnP

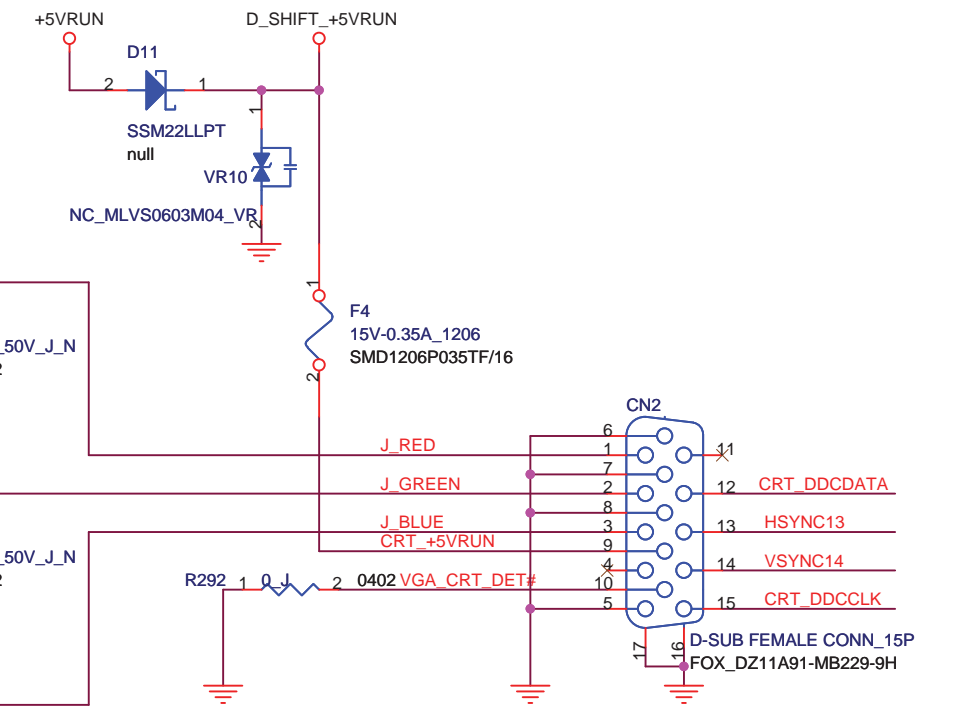


For EMI

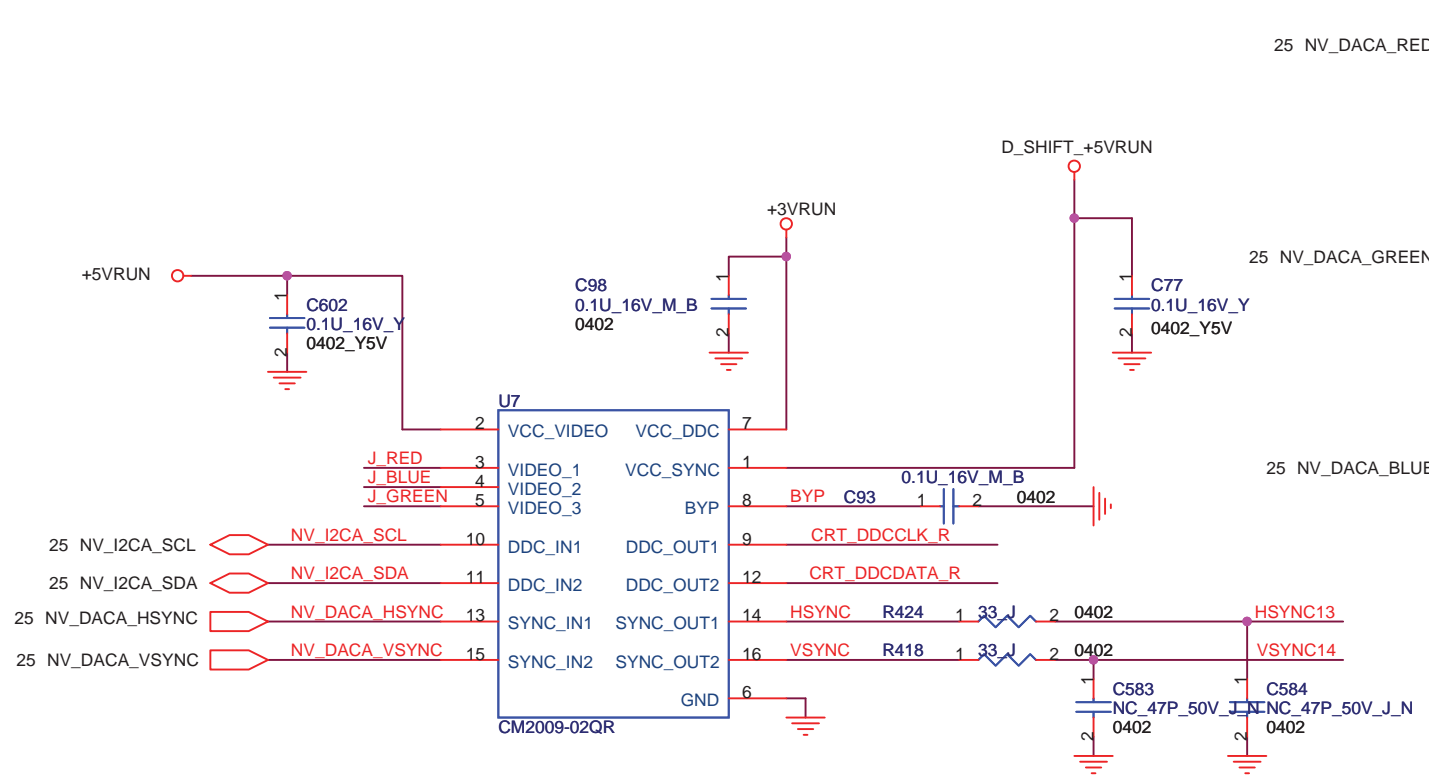
Semi-PnP Circuit

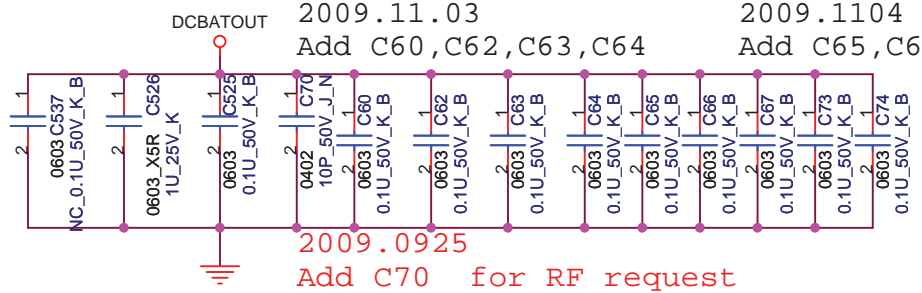


Change R83,R72,R64 to 75ohm --MOR 2/27

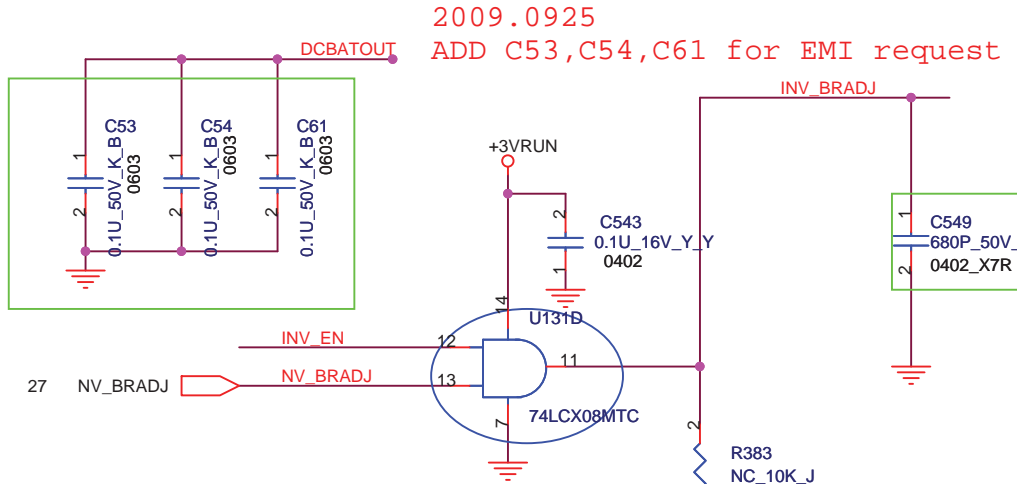
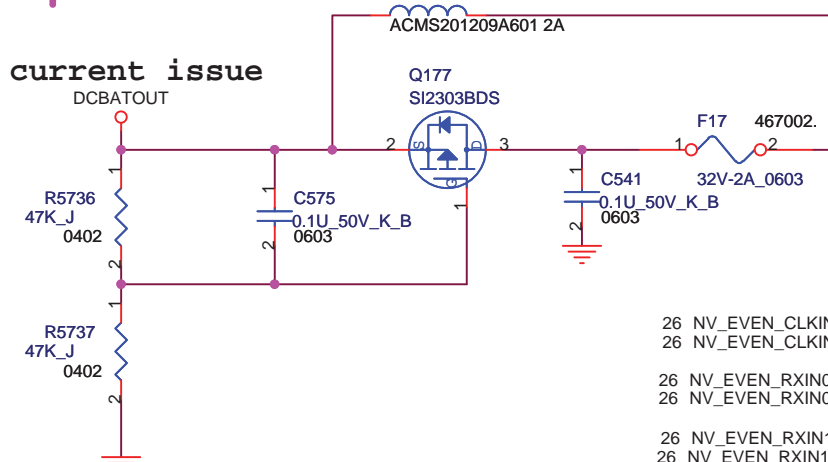


CRT CONNECTOR

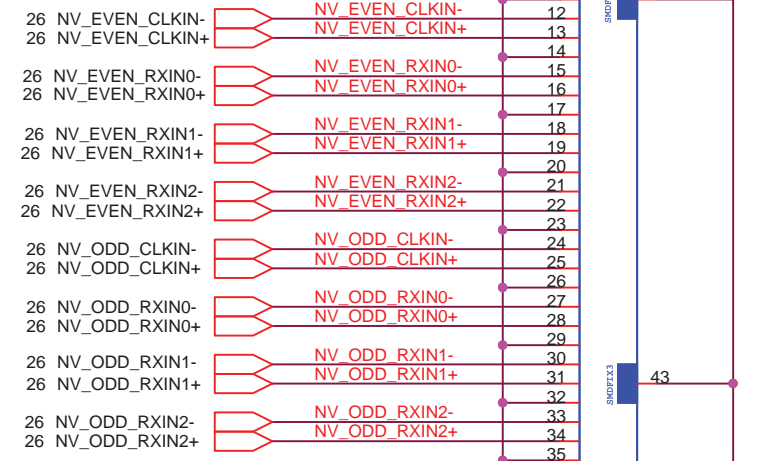




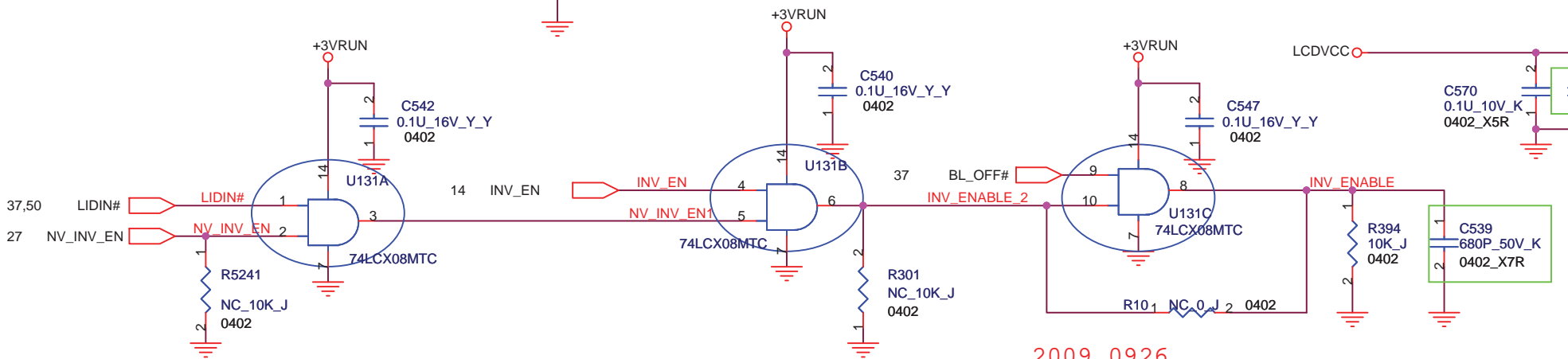
For rush current issue



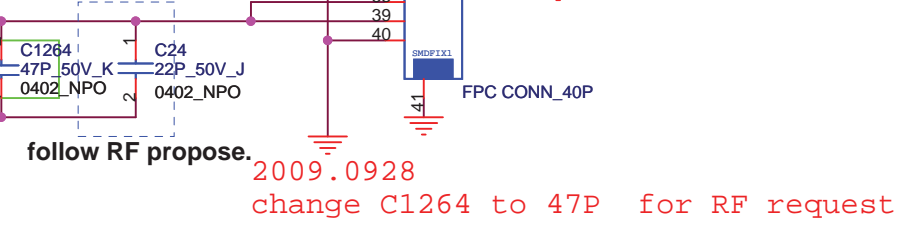
2009.0926 ADD C549 680P for EMI request place it near LVDS connector



2009.0918 DVT2 CN18 change to Halogen Free



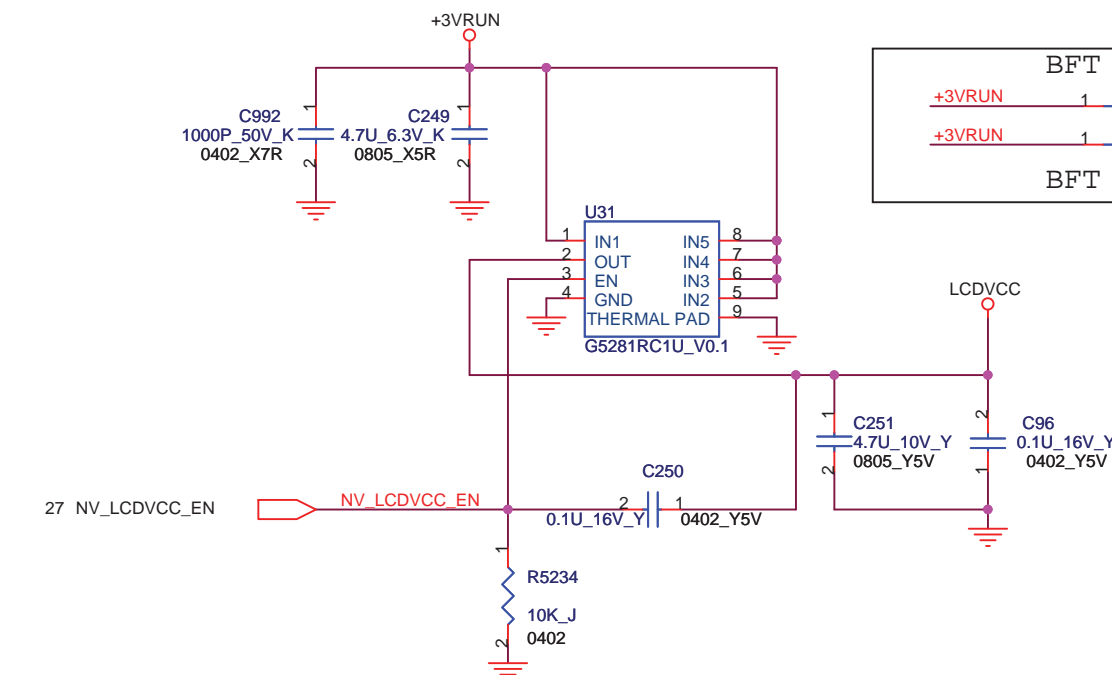
2009.0926 Change C539 TO 680P for EMI request



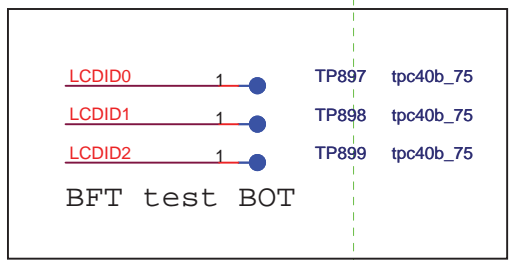
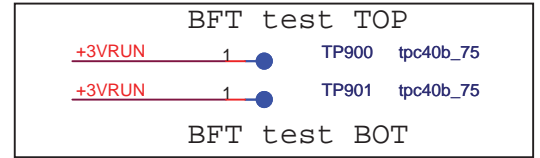
2009.0928 change C1264 to 47P for RF request

2009.10.23 Delete J2,J3

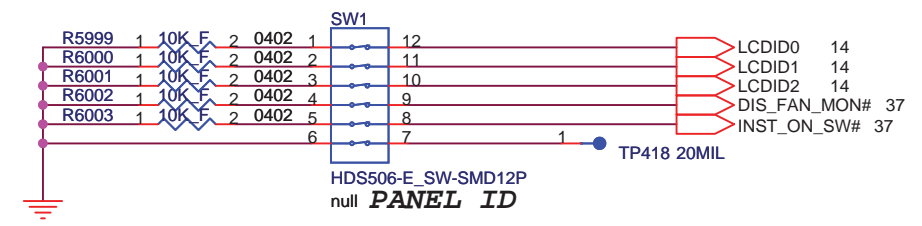
Current limit is from 1.1A to 2.1A.



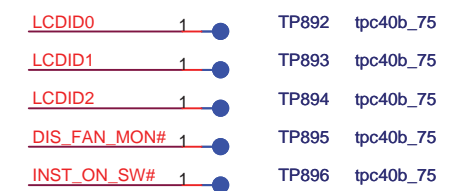
12/29 change to 10K FAE suggestion.



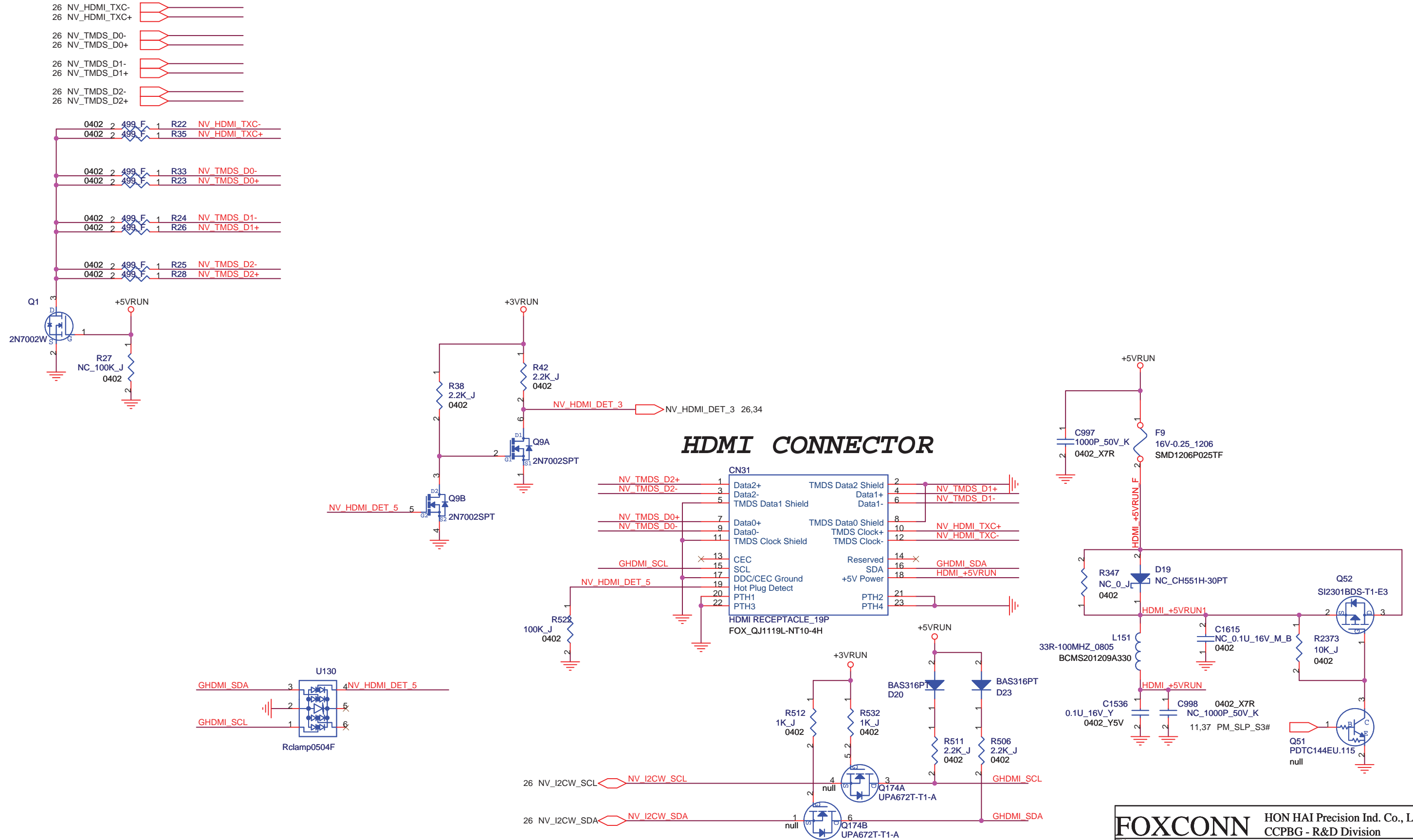
2009.10.23 Add test point TP897,TP898,TP899, TP900,TP901 for PVT

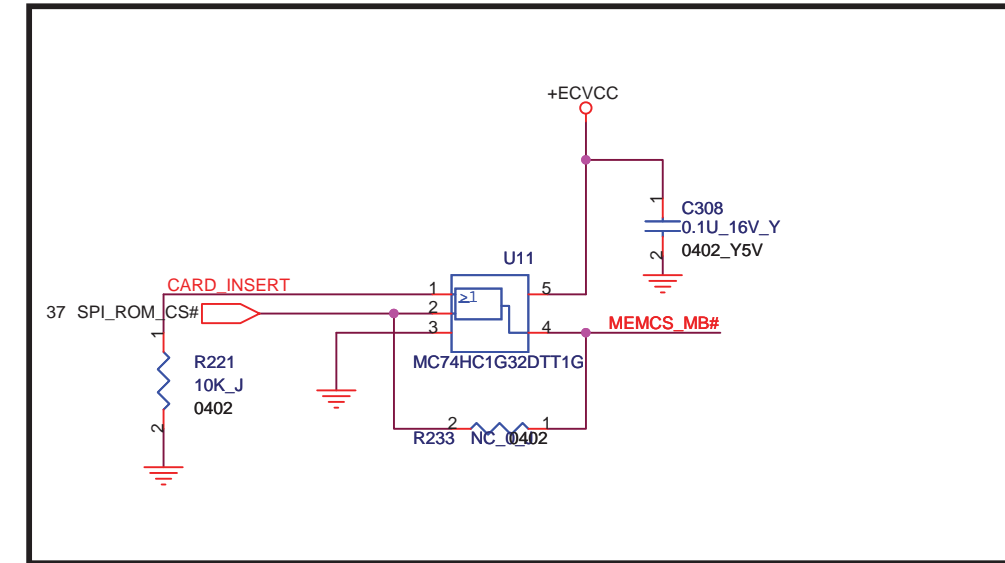
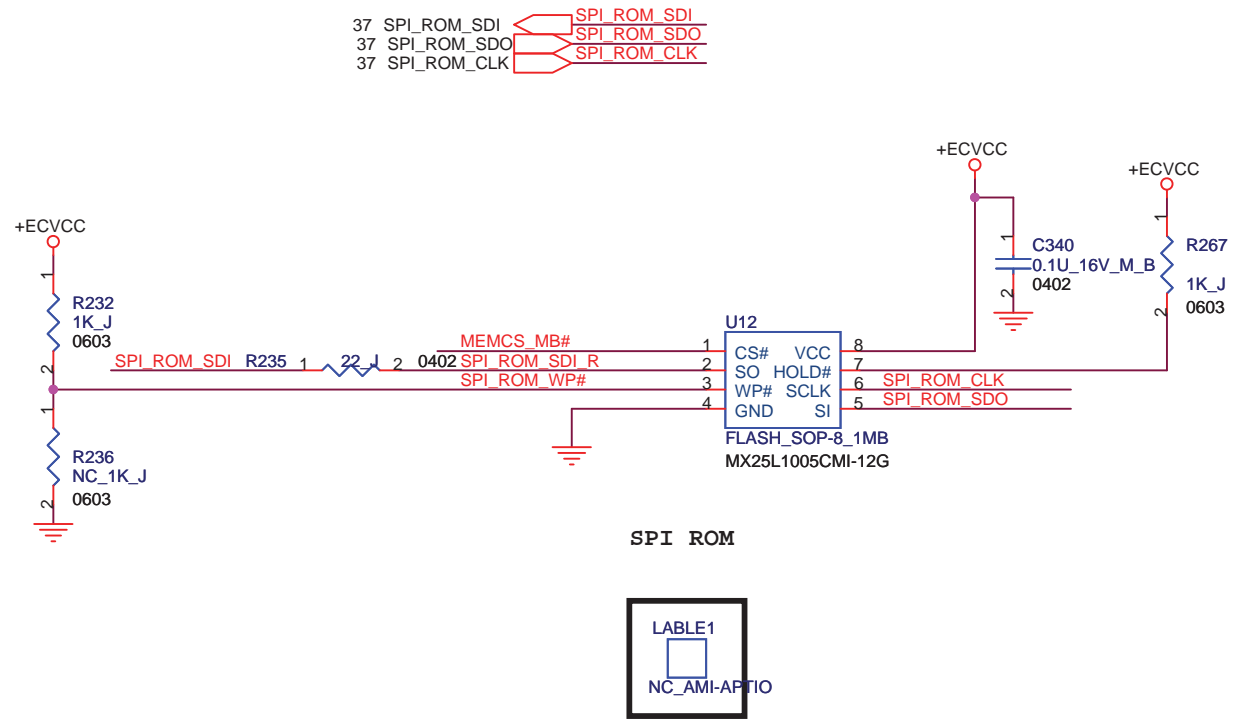


	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
AUG B140XW02 V1	0	0	0	0
LGD LP140WH2-TLN1	0	0	1	0
SAMSUNG LTN140AT08	0	0	1	1
AUG B140RW02 V0	0	1	0	0
DISABLE FAN	0	X	X	X
LOCK FUNCTION	0	X	X	X

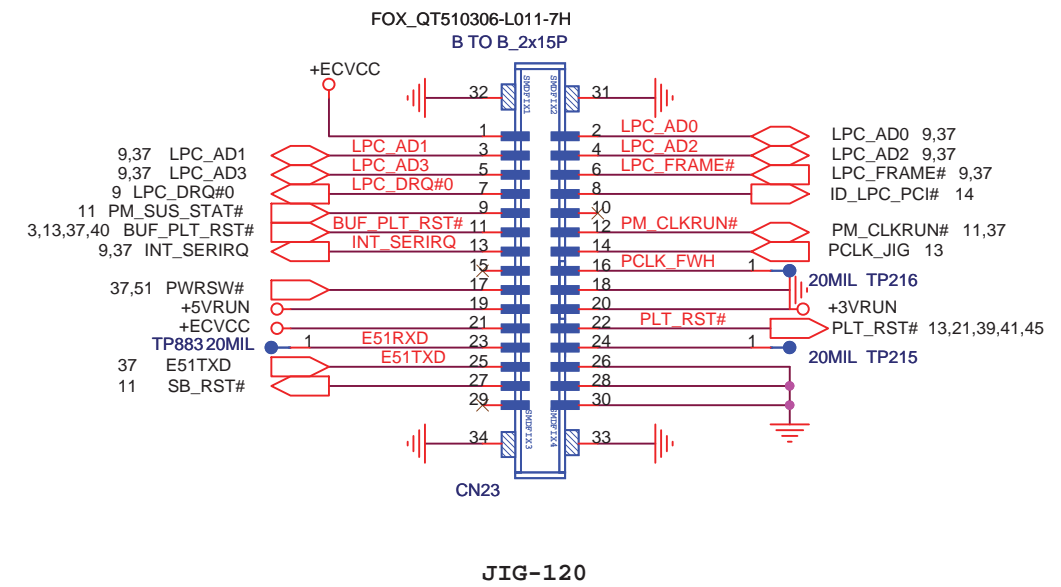
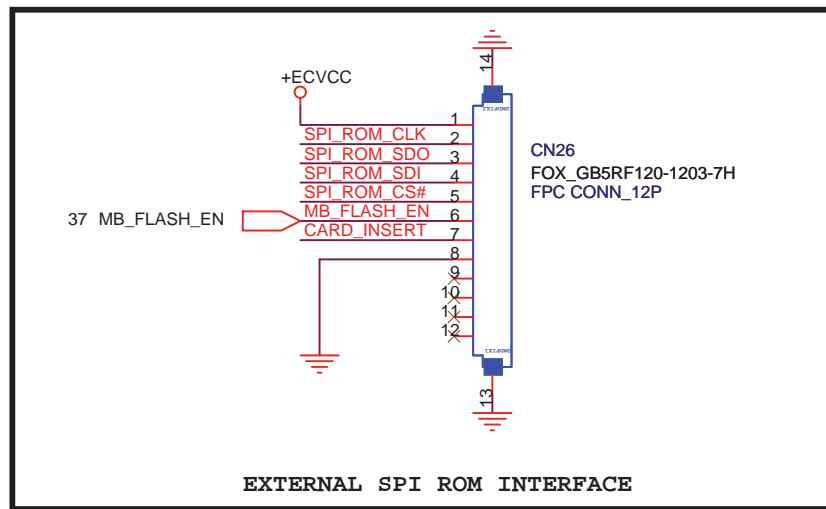


ON:0, OFF:1

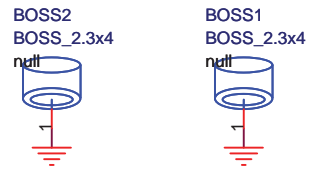




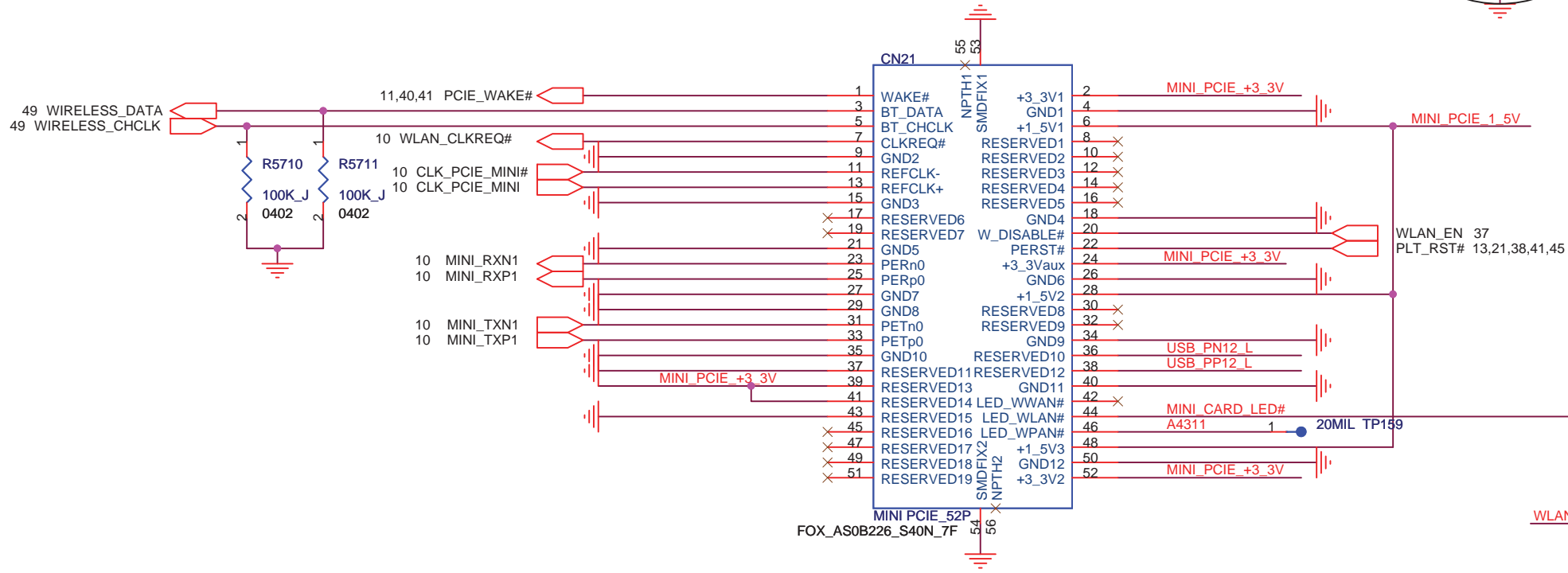
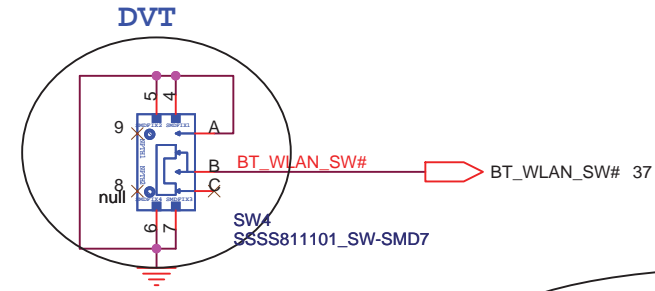
2009.10.23
Delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518



SW4.C pin delete and SW4.A connect to GND.



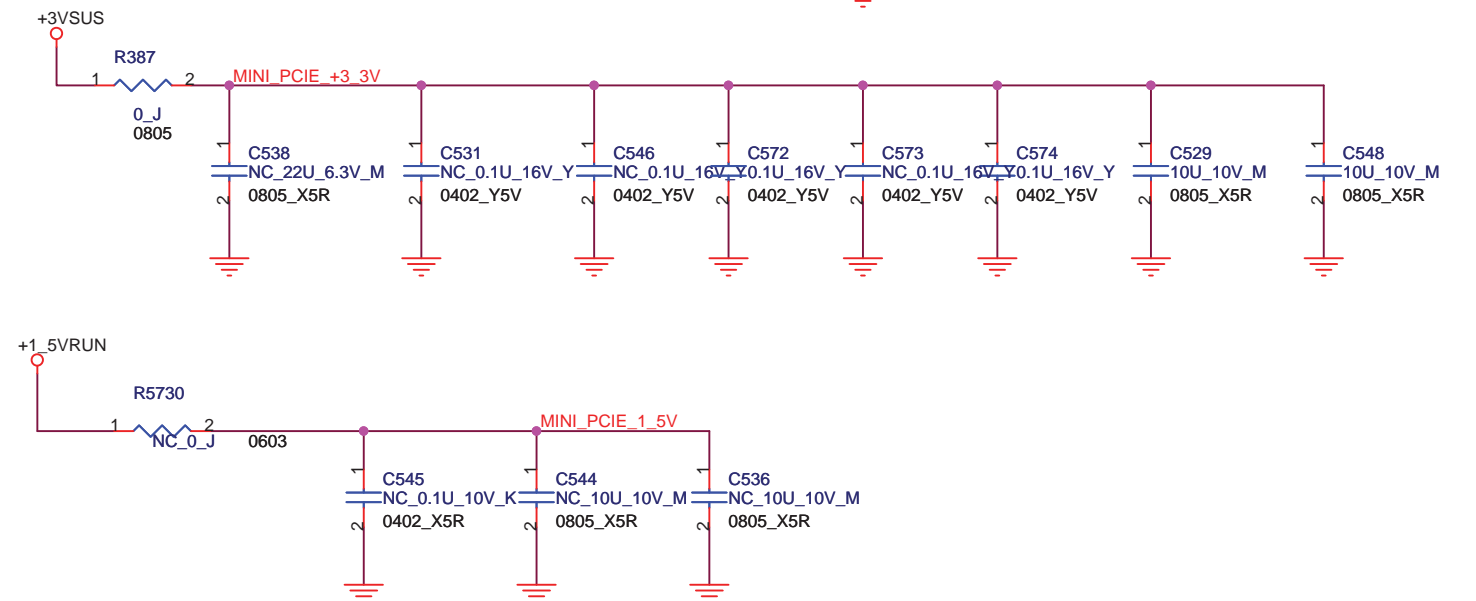
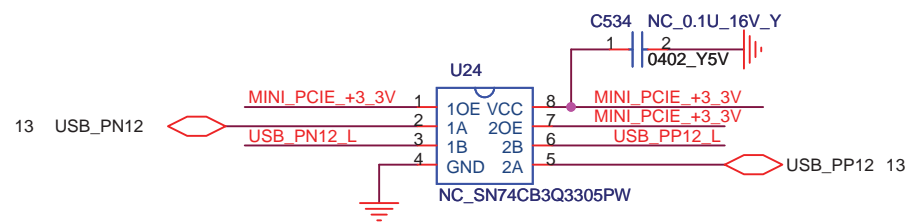
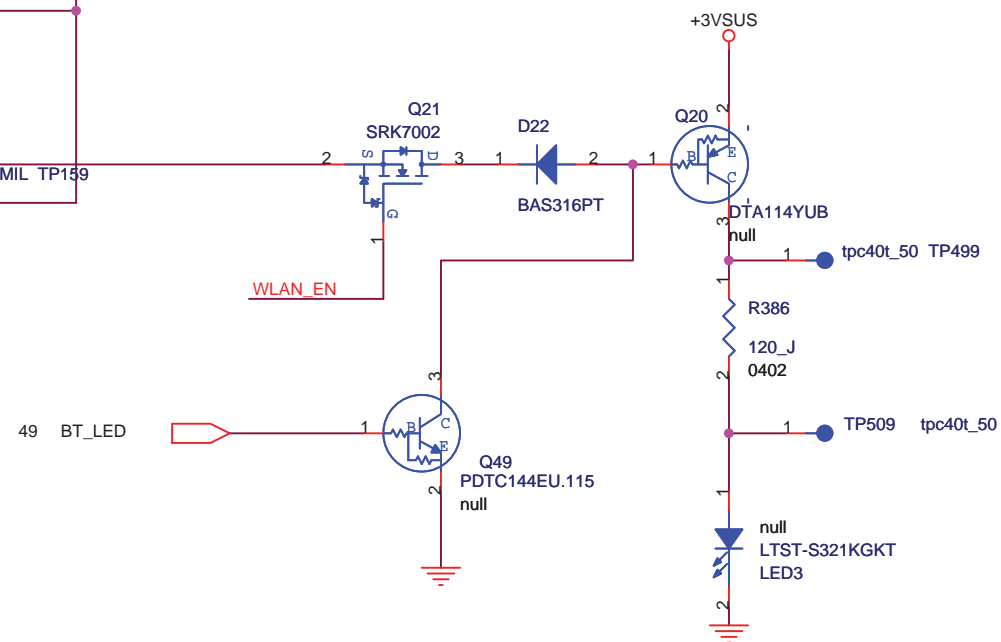
2009.0922
change BOSS1,BOSS2 to 1M-1F40M20-1500 for ME request



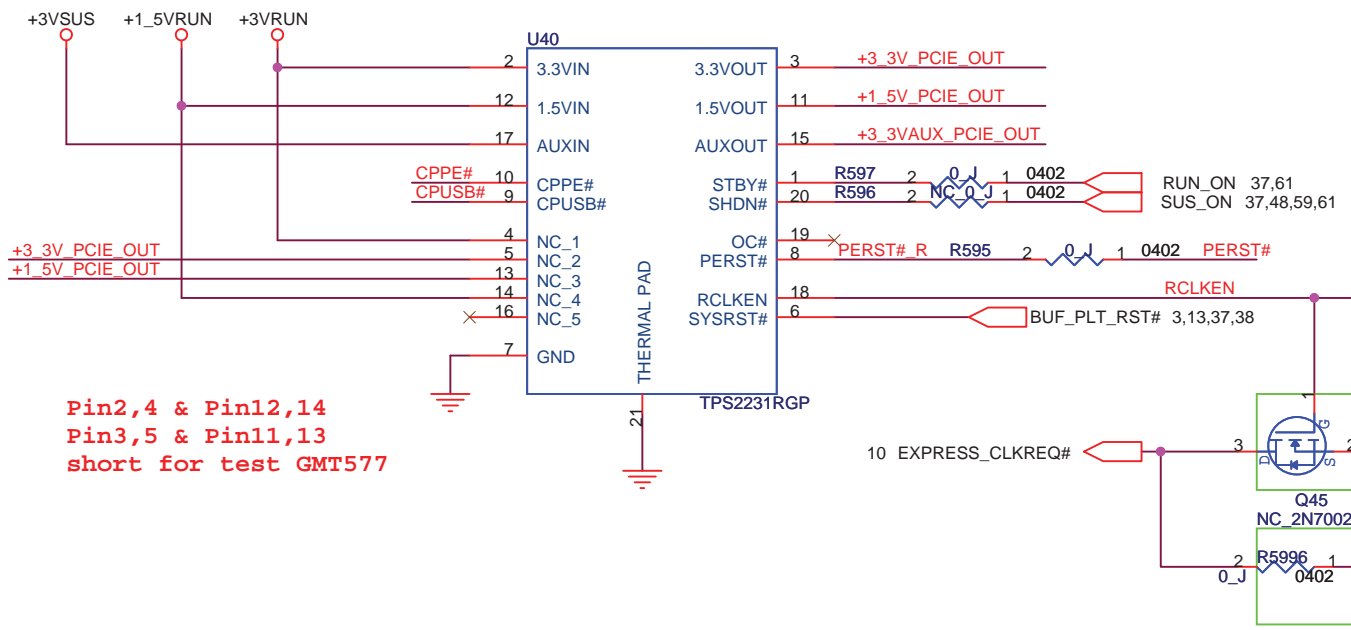
2009.0922
change CN21 TO 1N-1052000-0000 for ME request



For DVT SI validation,
Top-side and closer Pin11.13

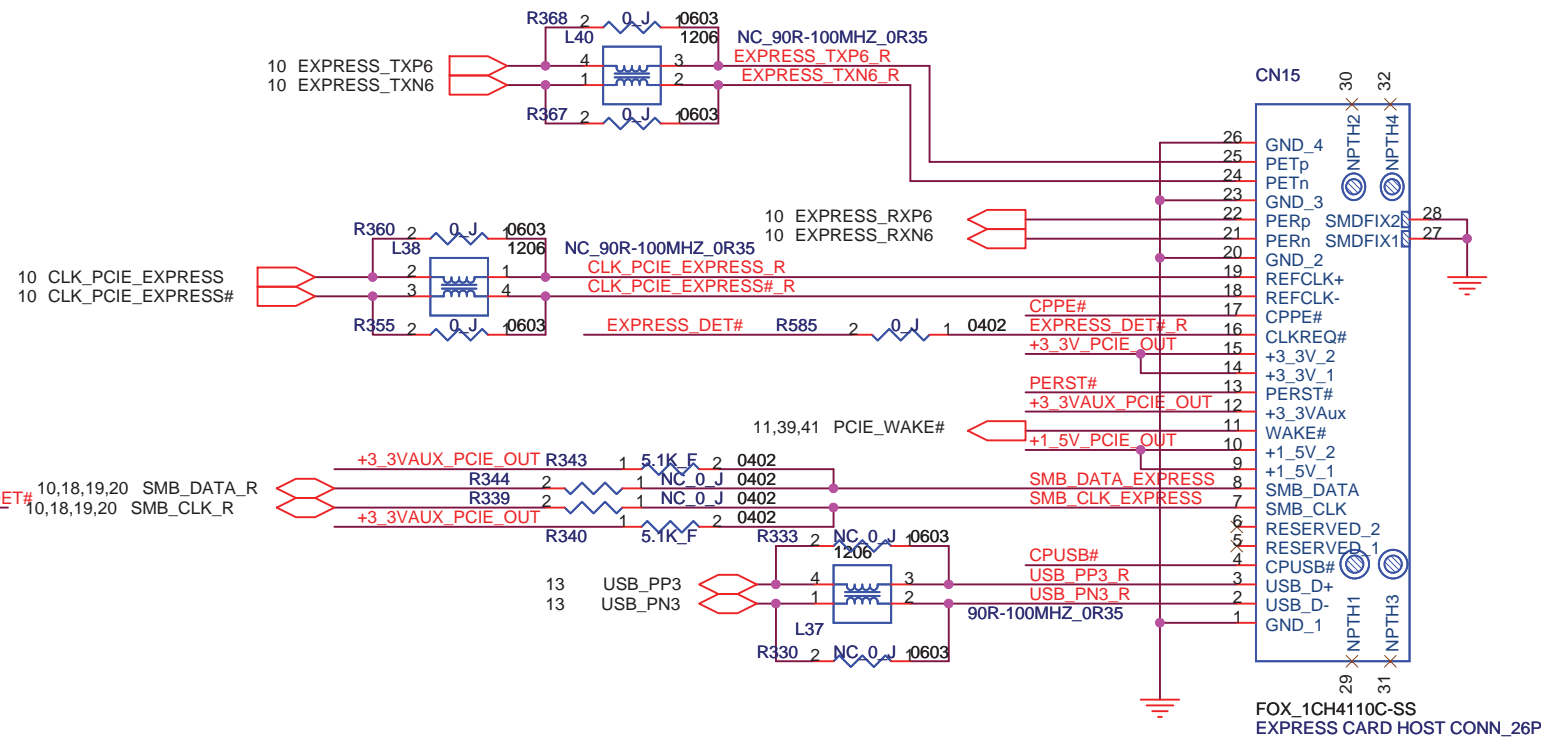


Express Card Power Switch

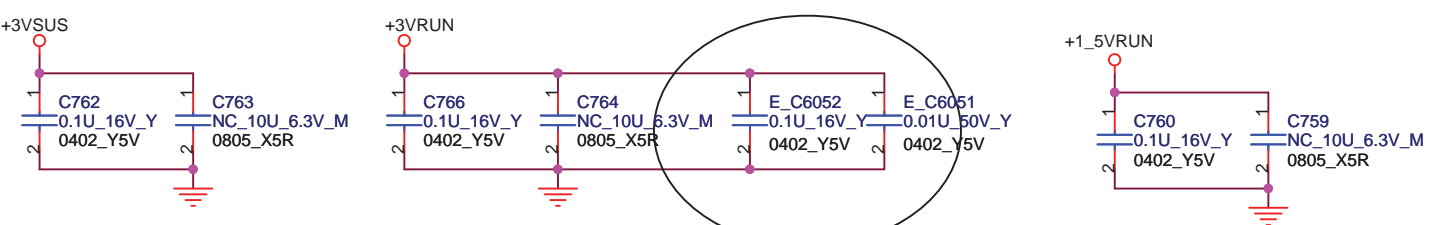


Pin2,4 & Pin12,14
Pin3,5 & Pin11,13
short for test GMT577

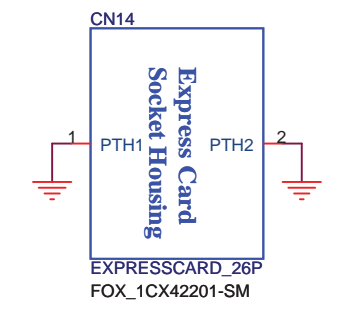
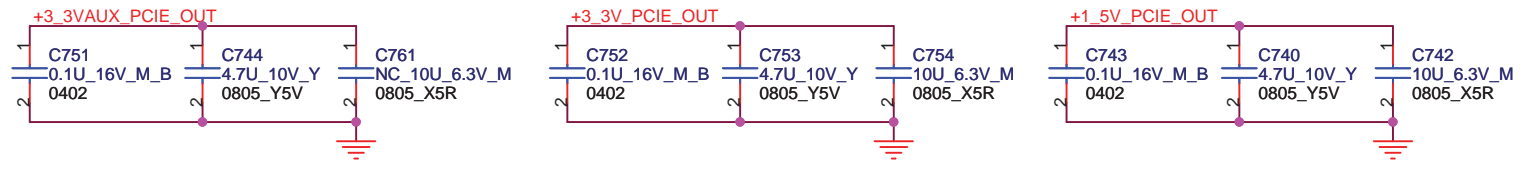
2009.0922
CHANGE Q45 TO NC ,R5996 TO MOUNT

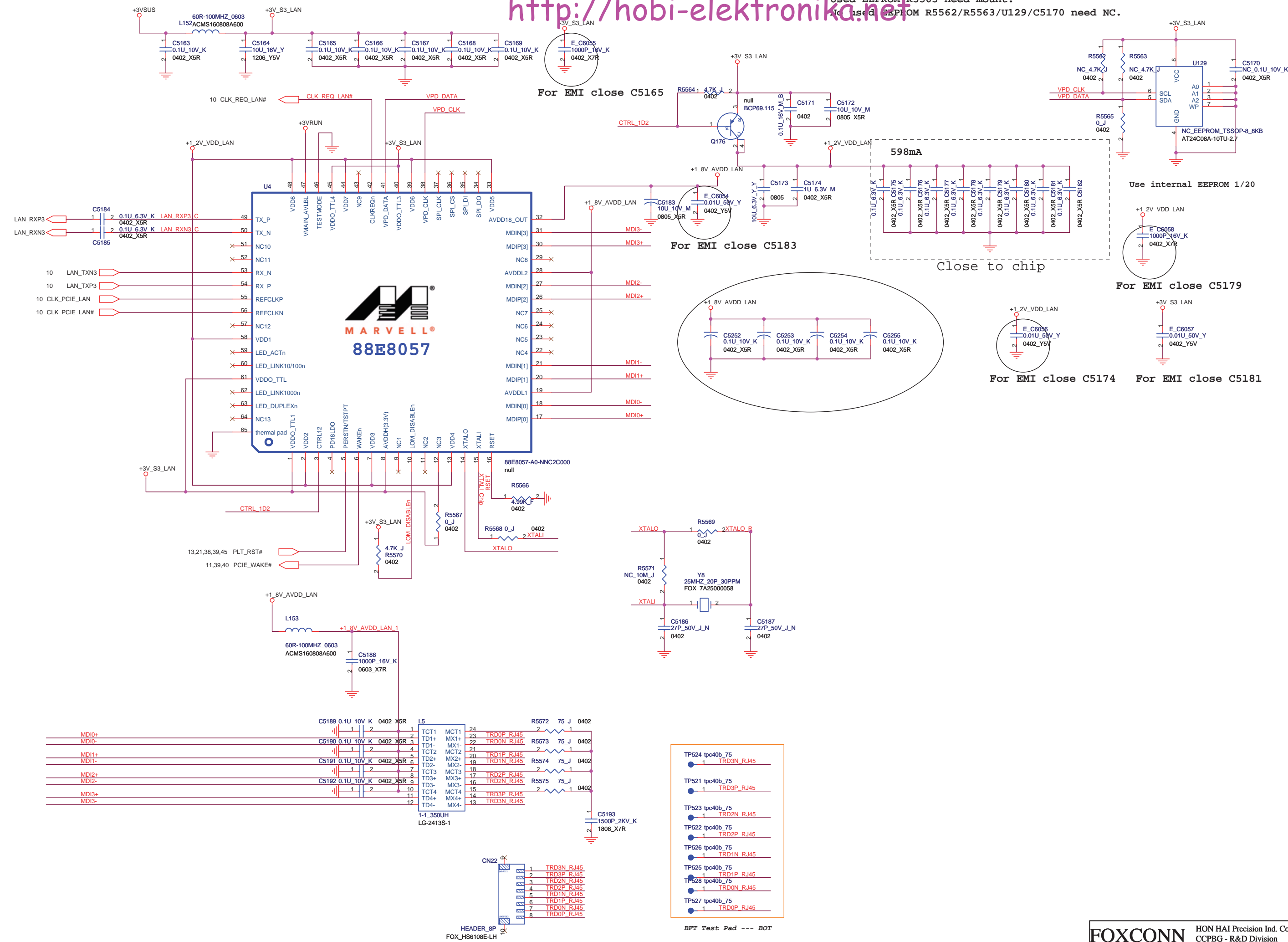


Express Card Slot.



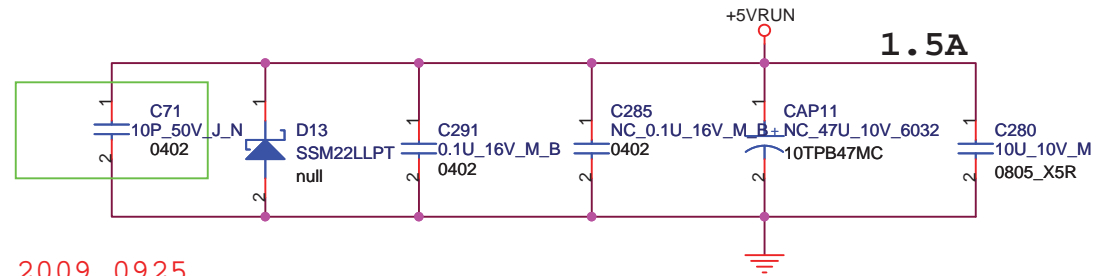
For EMI close C764



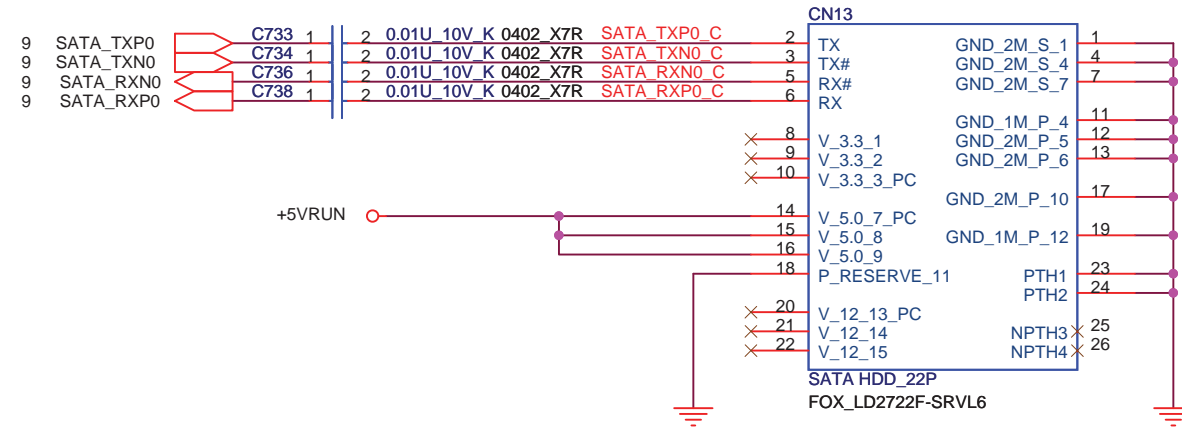


01/03 Change RJ45 From ME.

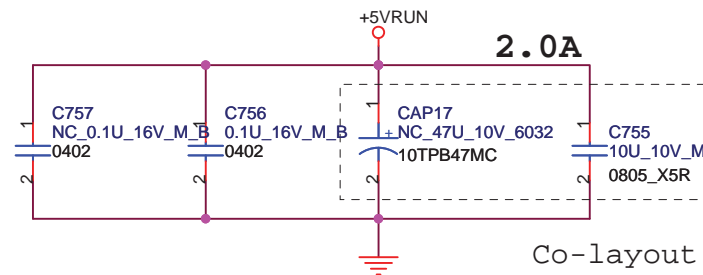
SATA HDD CONN



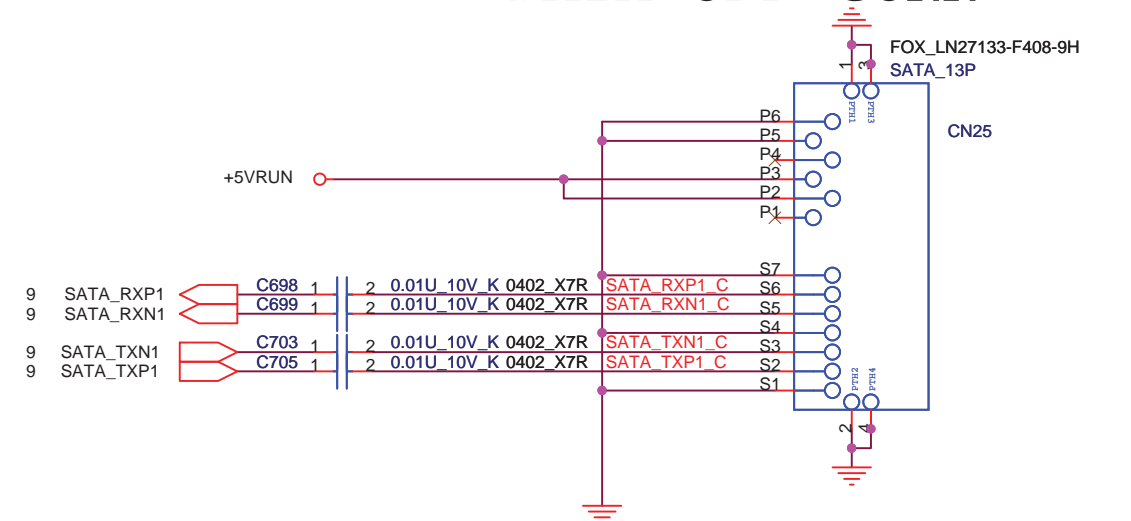
2009.0925
Add C71 for RF request



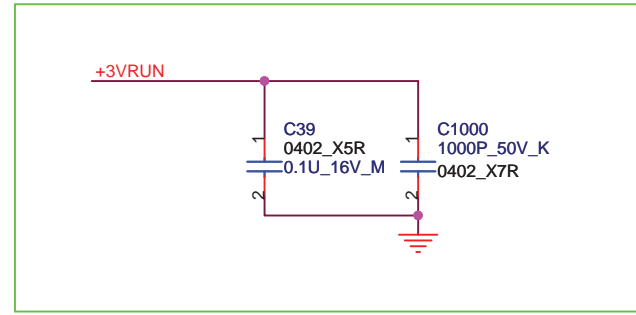
SATA ODD CONN



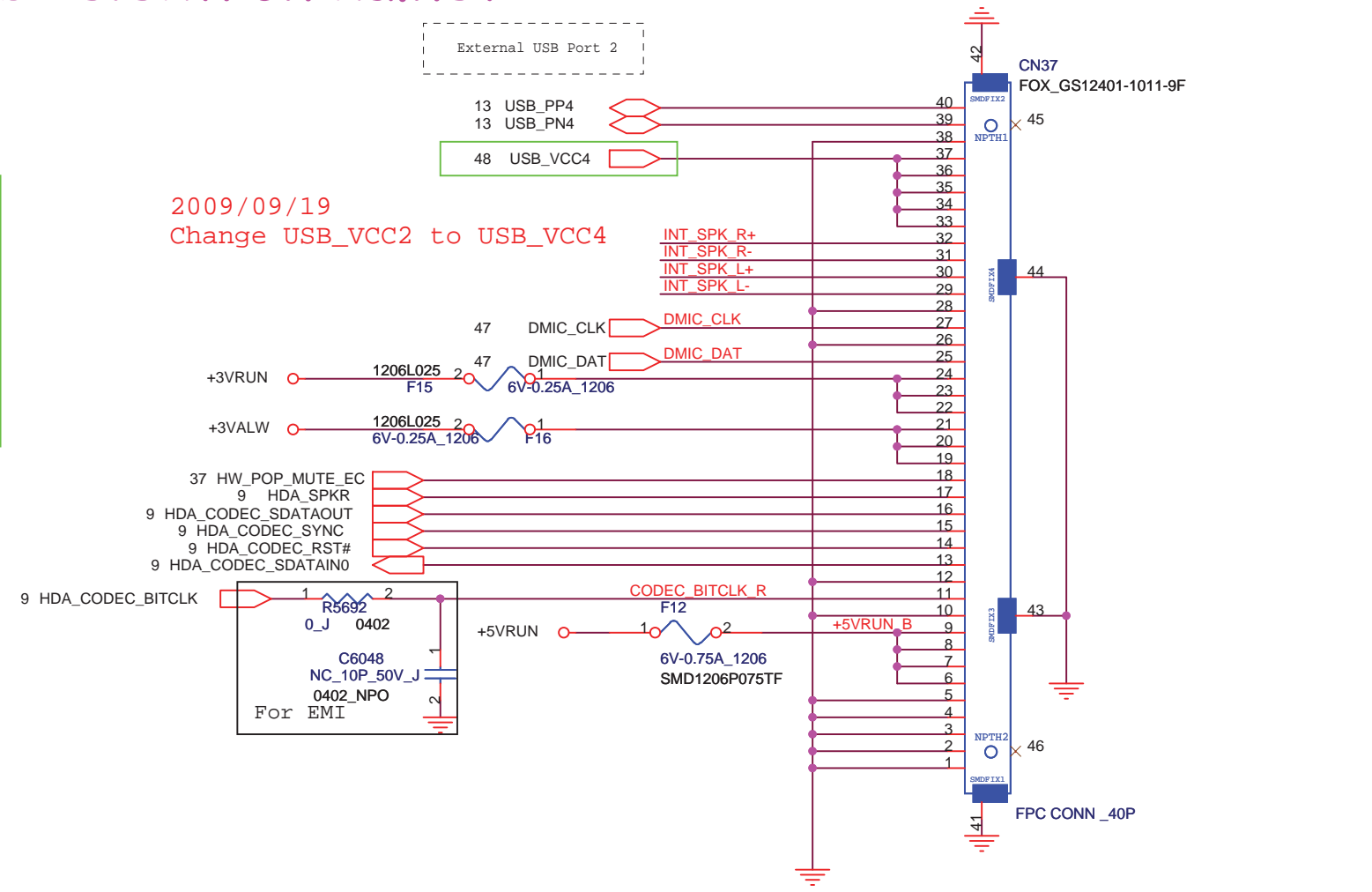
Co-layout



2009.0922
CN25 change to Halogen Free

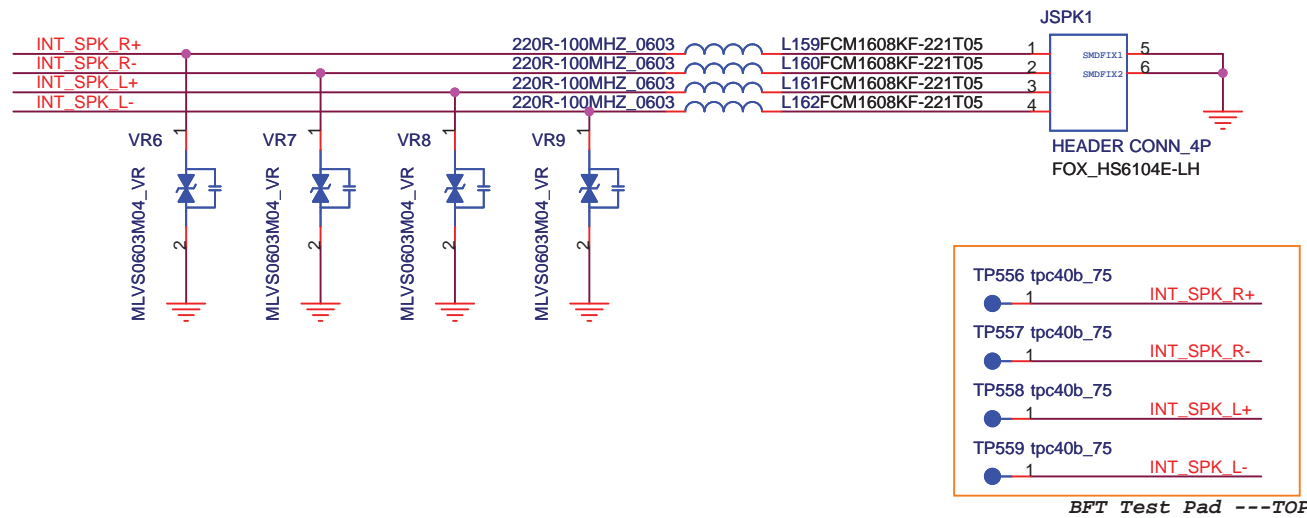


2009.0925
ADD for EMI request

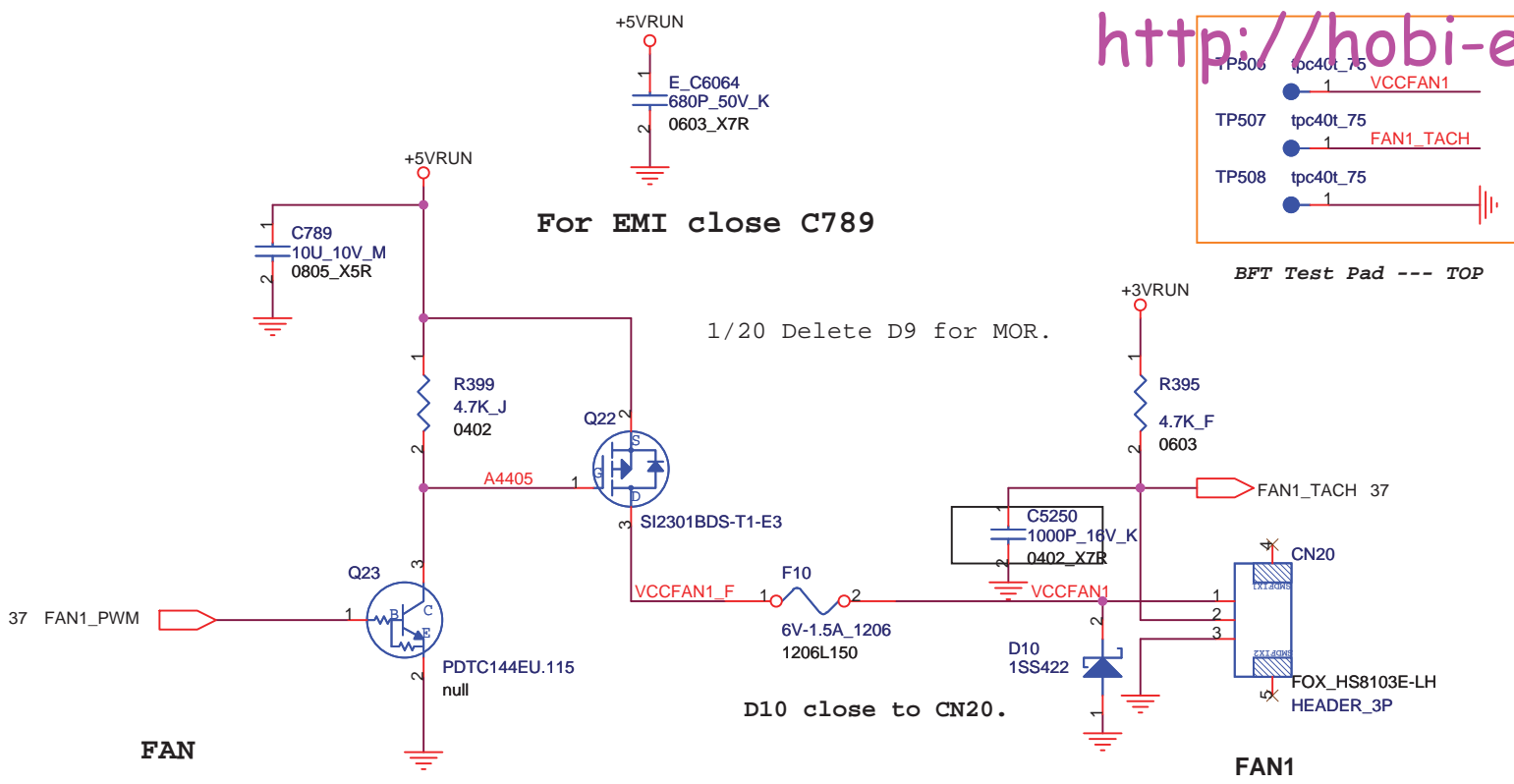


Audio & USB WTb CONN.

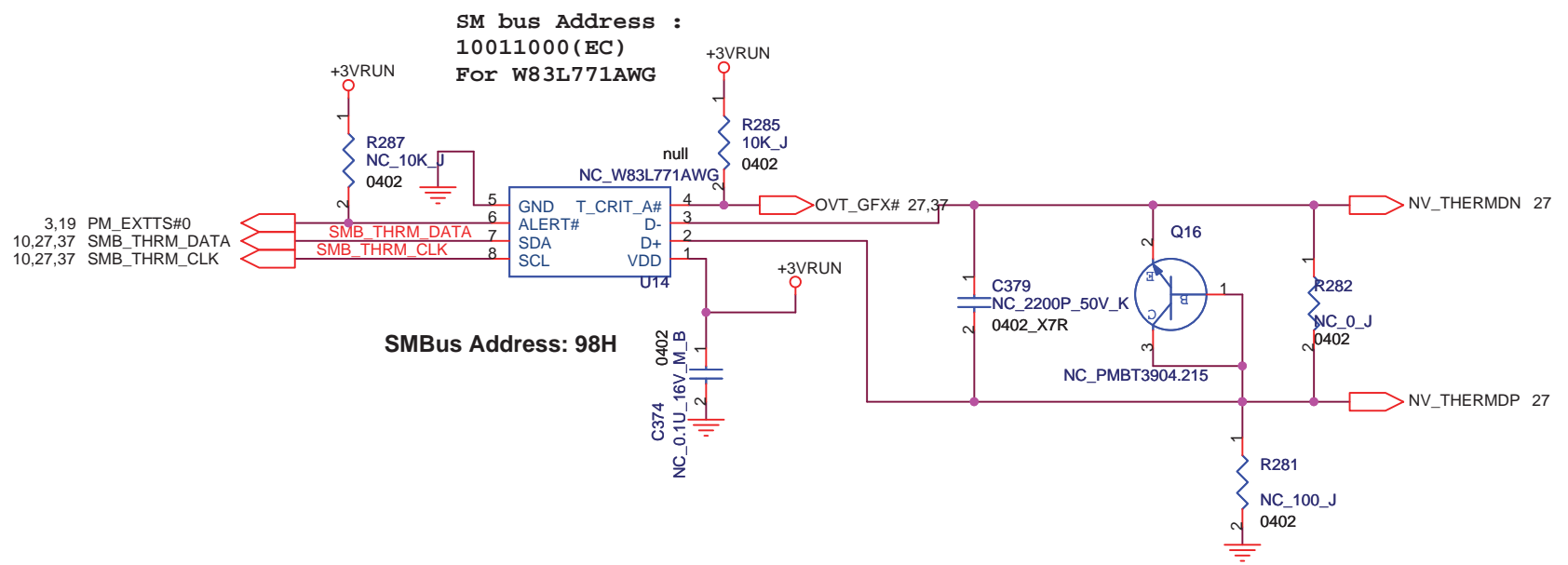
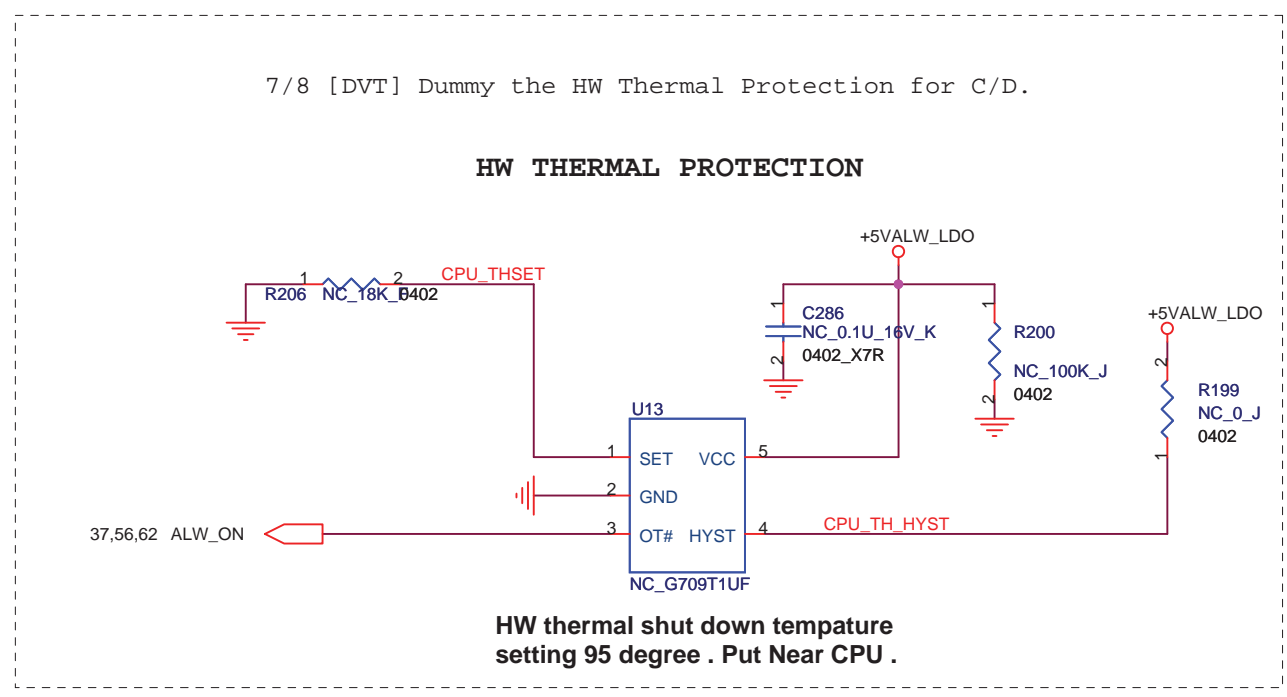
INTERNAL SPEAKER



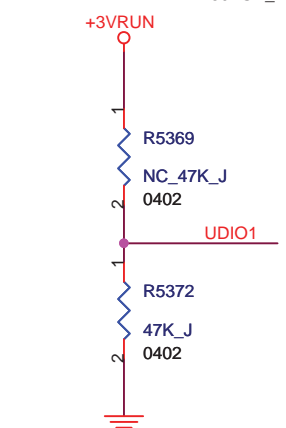
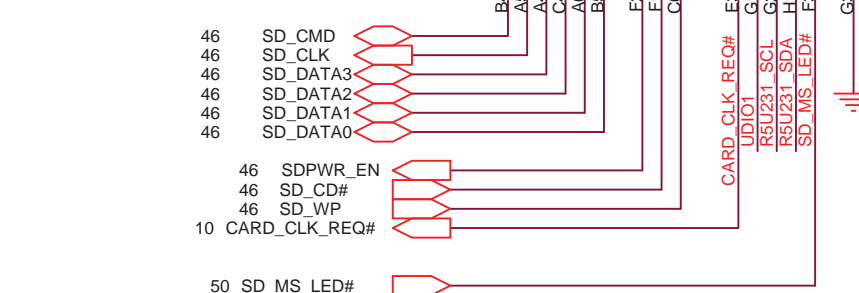
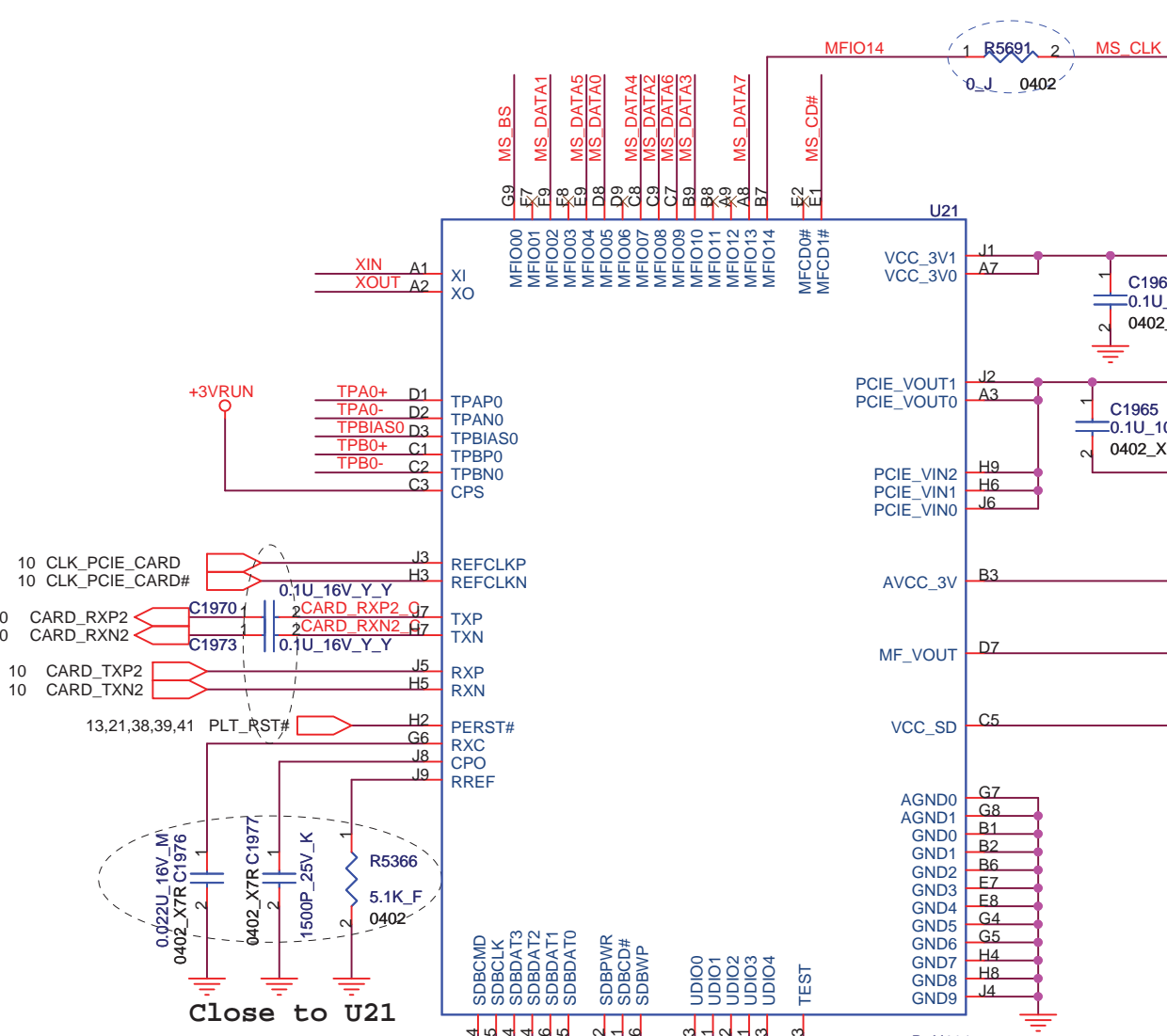
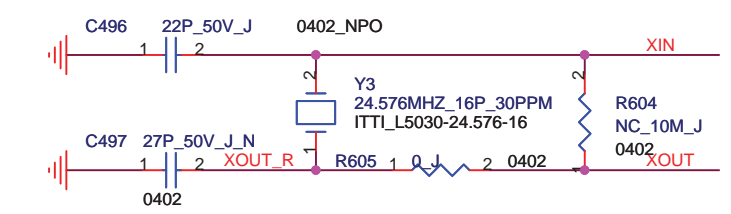
BFT Test Pad ---TOP



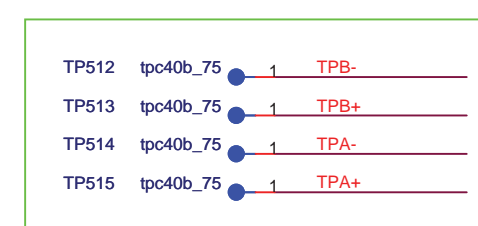
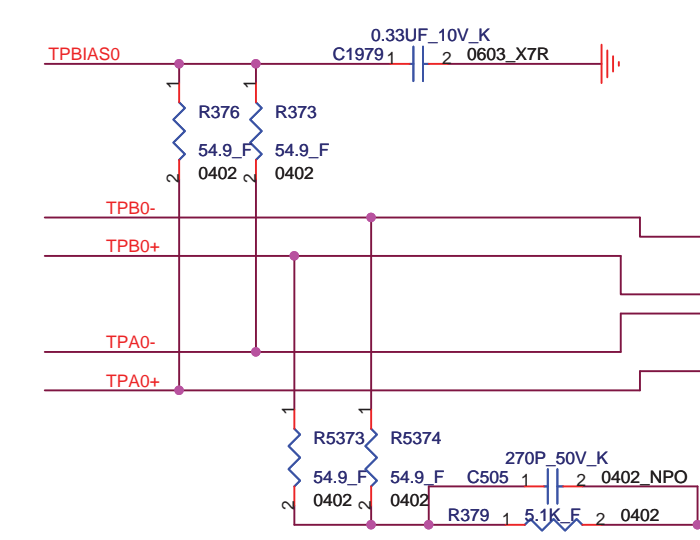
2009.10.19
 change C5250 from 1C-2B20473-K300 to
 1C-2B20102-K001 for PVT



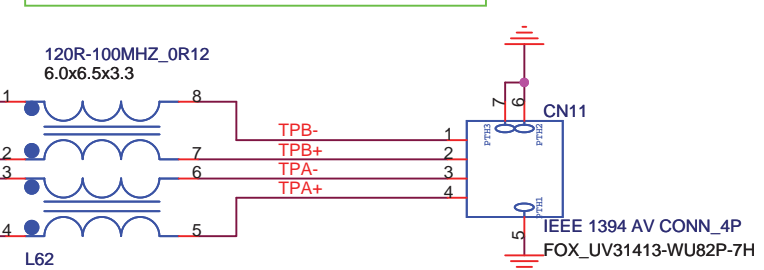
1/2 Add pull headers and resistors for PCIe protocol measurement for R5U231.
Delete parts for R5U231 protocol measurement.



SR0M: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)



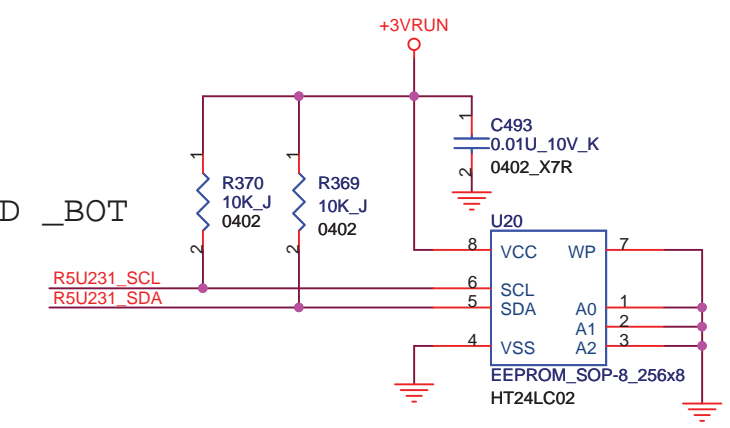
BFT TEST PAD _BOT

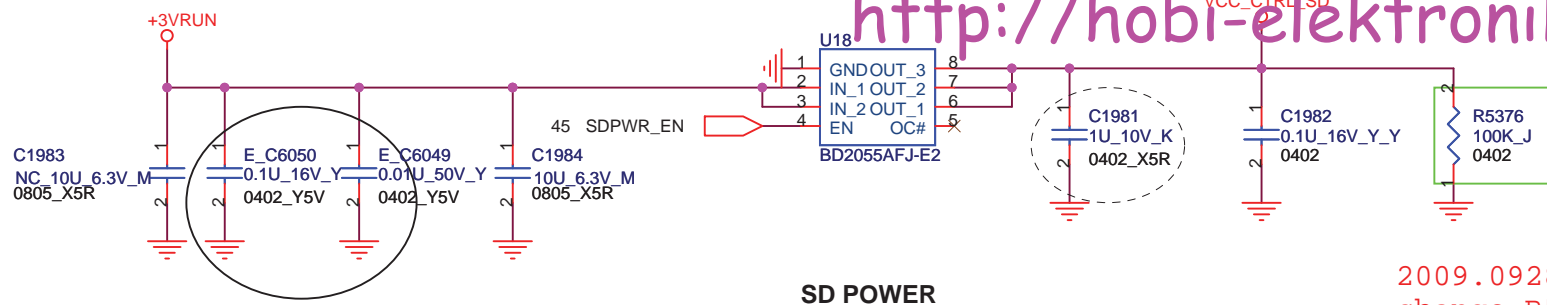


2009.0918
DVT2 CN11 change to Halogen Free

2009.0921
ADD R5991 follow design guide
change C476 TO NC_12P

2009.10.19
change R5703 from 68ohm to 75ohm for PVT





For EMI close C1983

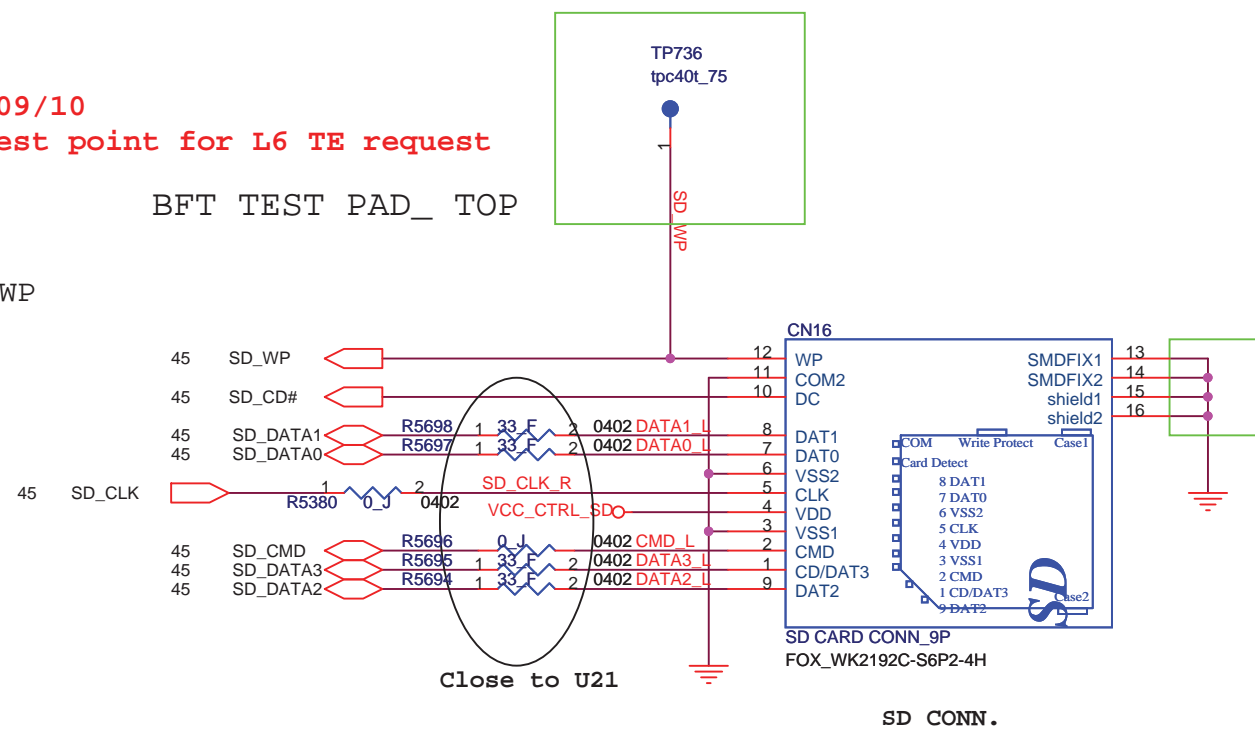
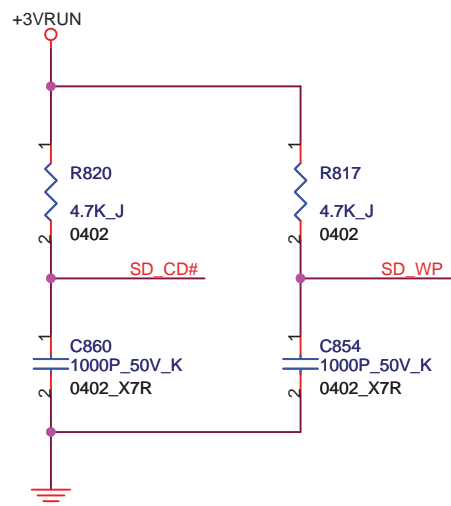
SD POWER

2009.0928
change R5376 to 100K follow design guide

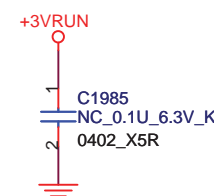
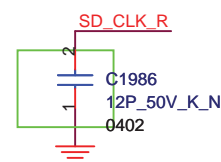
2009/09/10
Add test point for L6 TE request

BFT TEST PAD_TOP

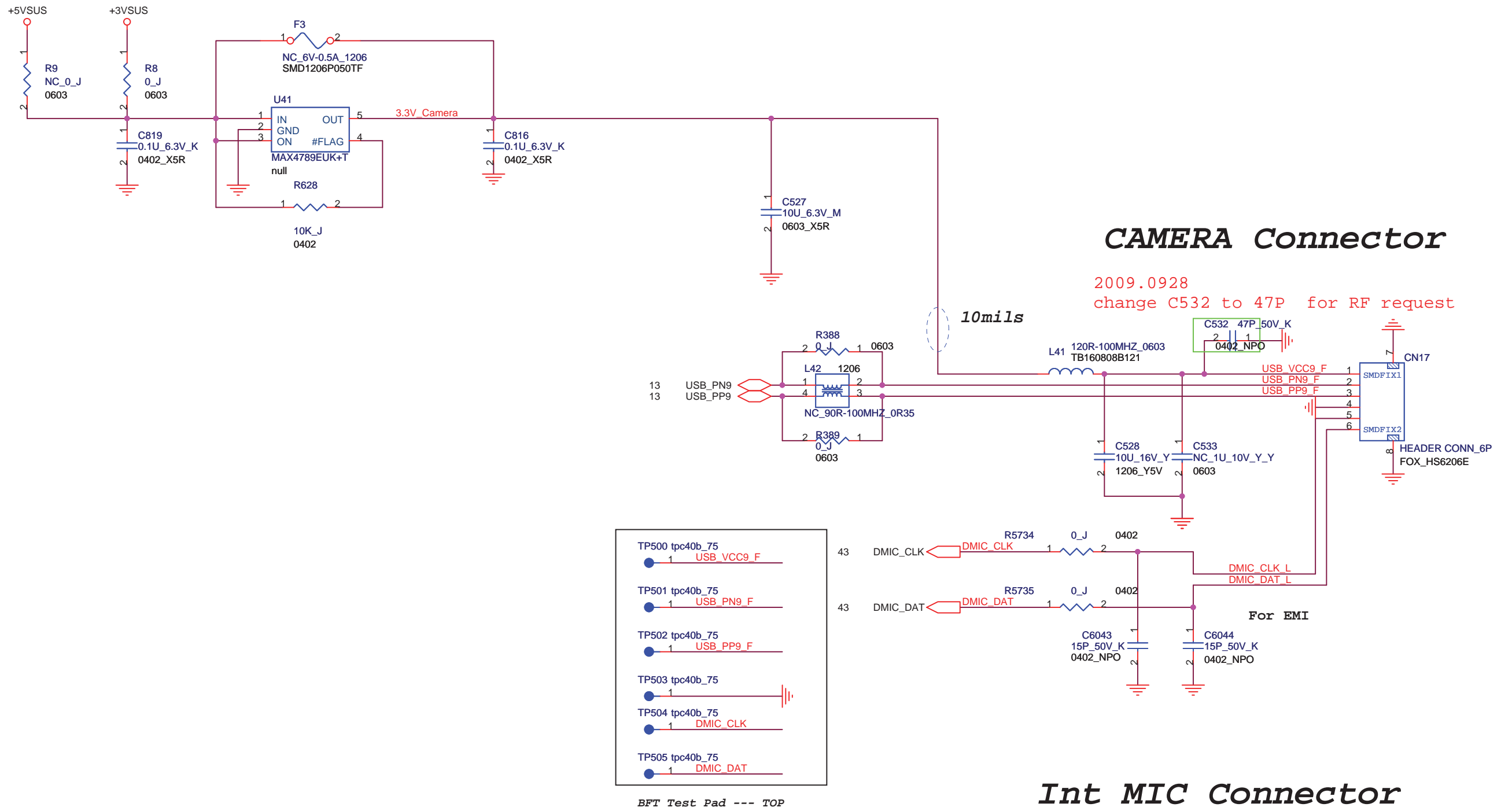
2009.10.23
change net SD_WP# to SD_WP



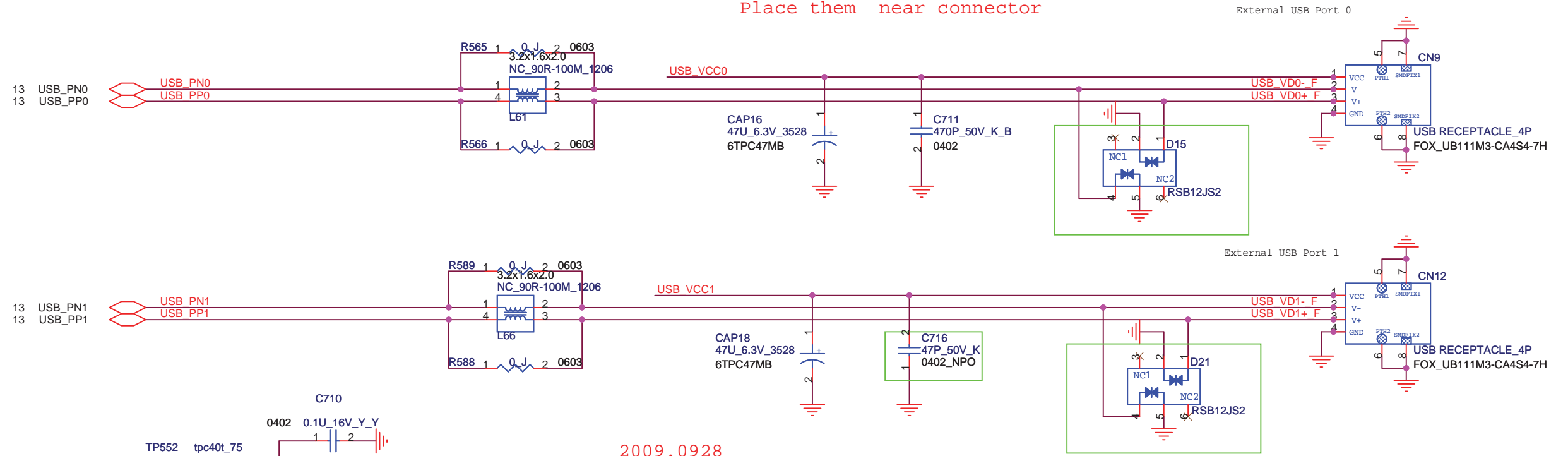
For EMI



2009.0921
change C1986 to 12p

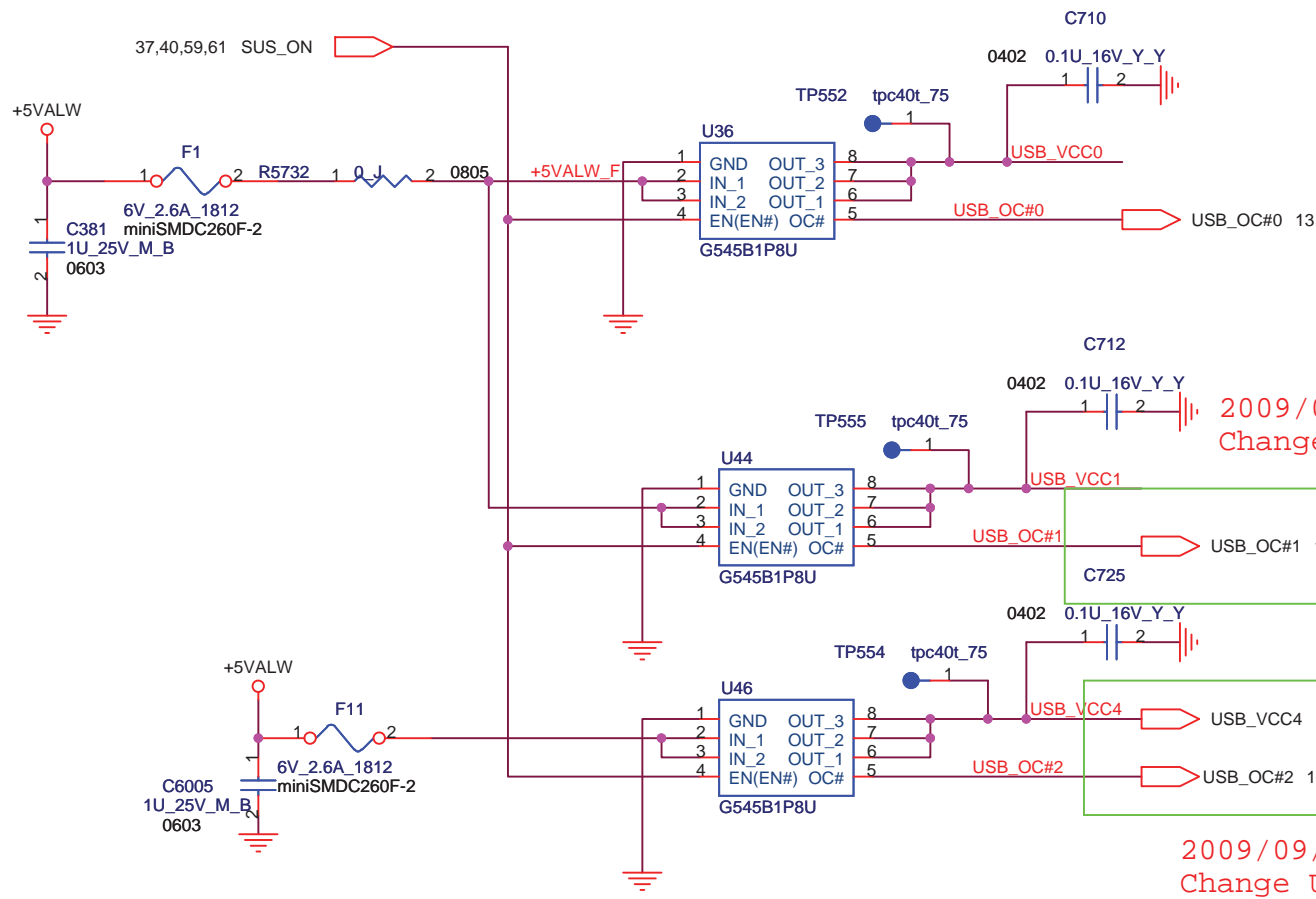


2009.0921
change D15,D21 from NC to mount
Place them near connector



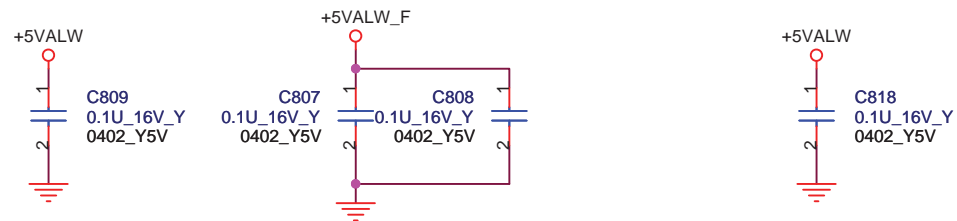
2009.0928
change C716 to 47P for RF request

2009.0918
DVT2 CN9, CN12 change to Halogen Free



2009/09/19
Change USB_OC#0 to USB_OC#1

2009/09/19
Change USB_VCC2 to USB_VCC4

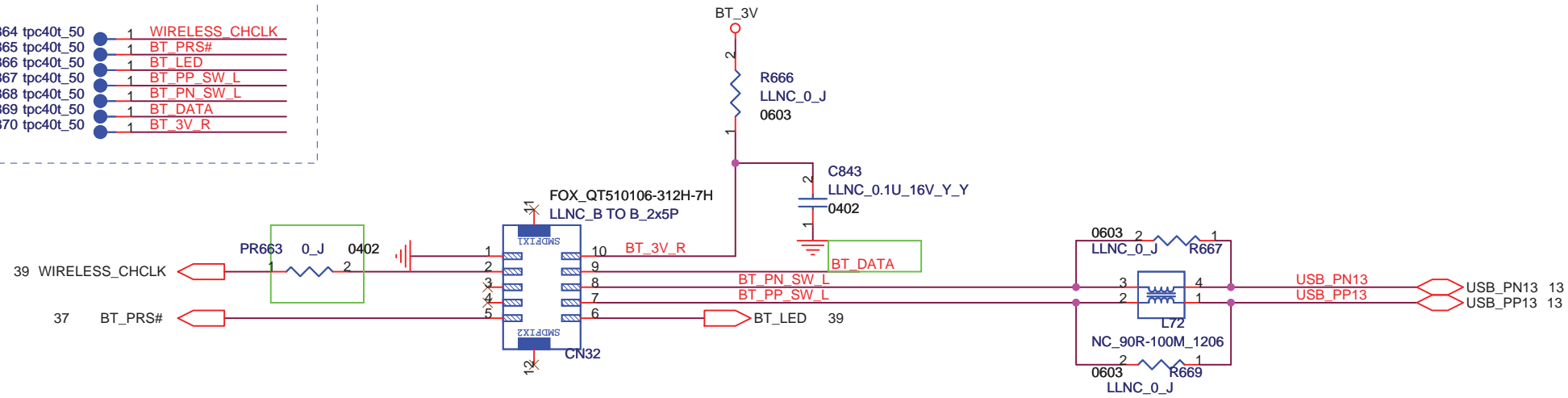


Bluetooth connector

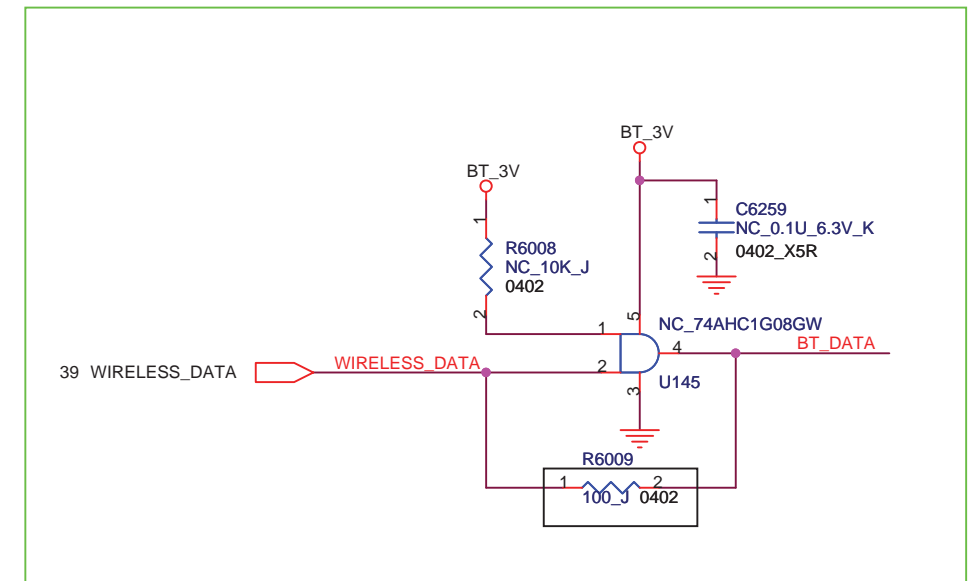
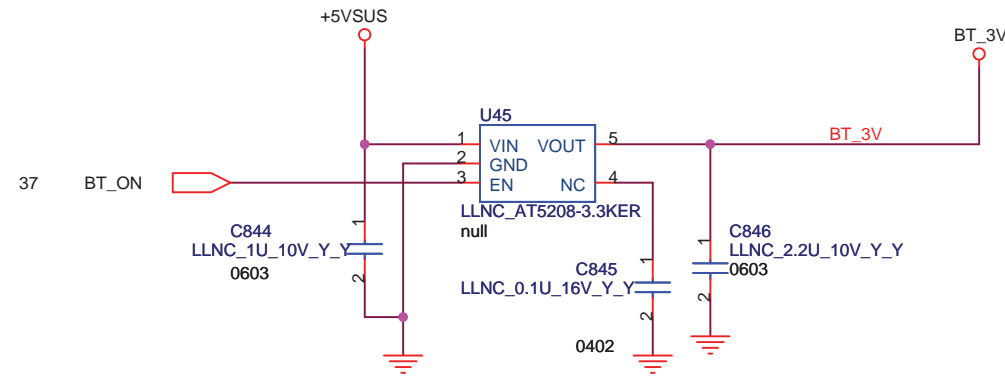
BOT Side

PVT

TP864 tpc40t_50	1	WIRELESS_CHCLK
TP865 tpc40t_50	1	BT_PRS#
TP866 tpc40t_50	1	BT_LED
TP867 tpc40t_50	1	BT_PP_SW_L
TP868 tpc40t_50	1	BT_PN_SW_L
TP869 tpc40t_50	1	BT_DATA
TP870 tpc40t_50	1	BT_3V_R

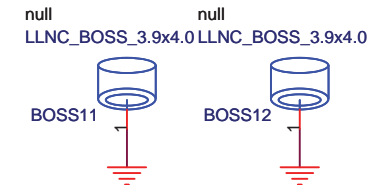


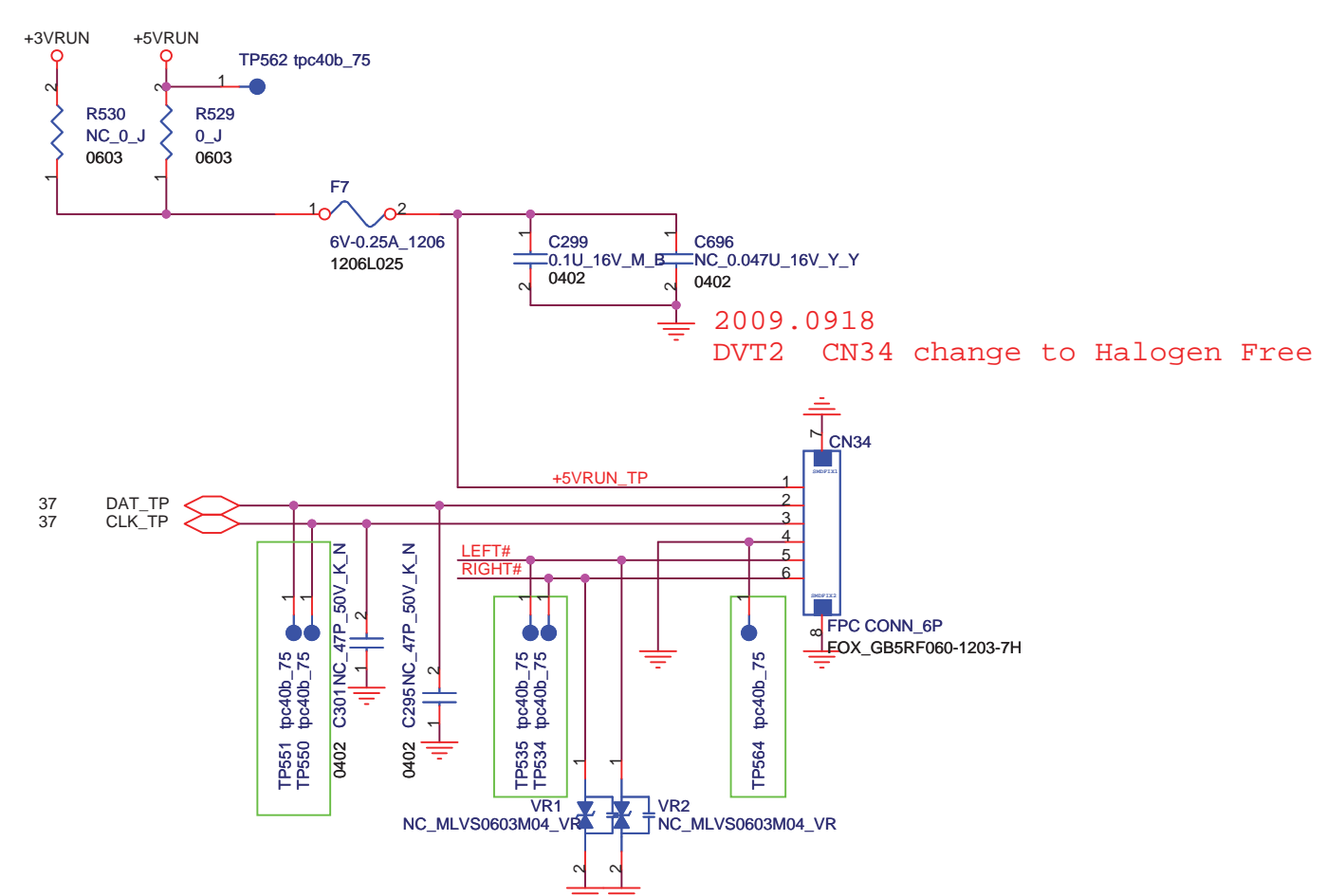
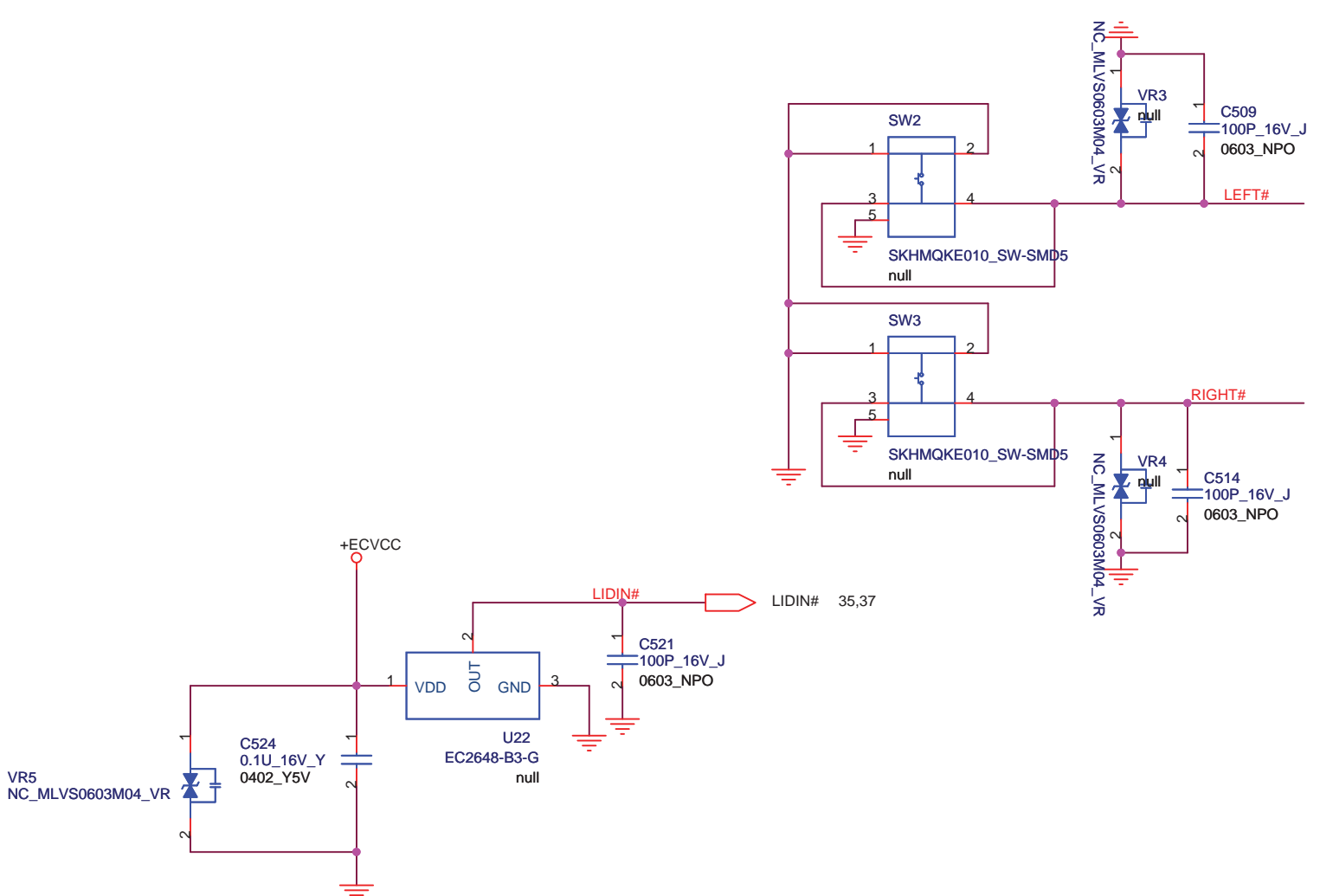
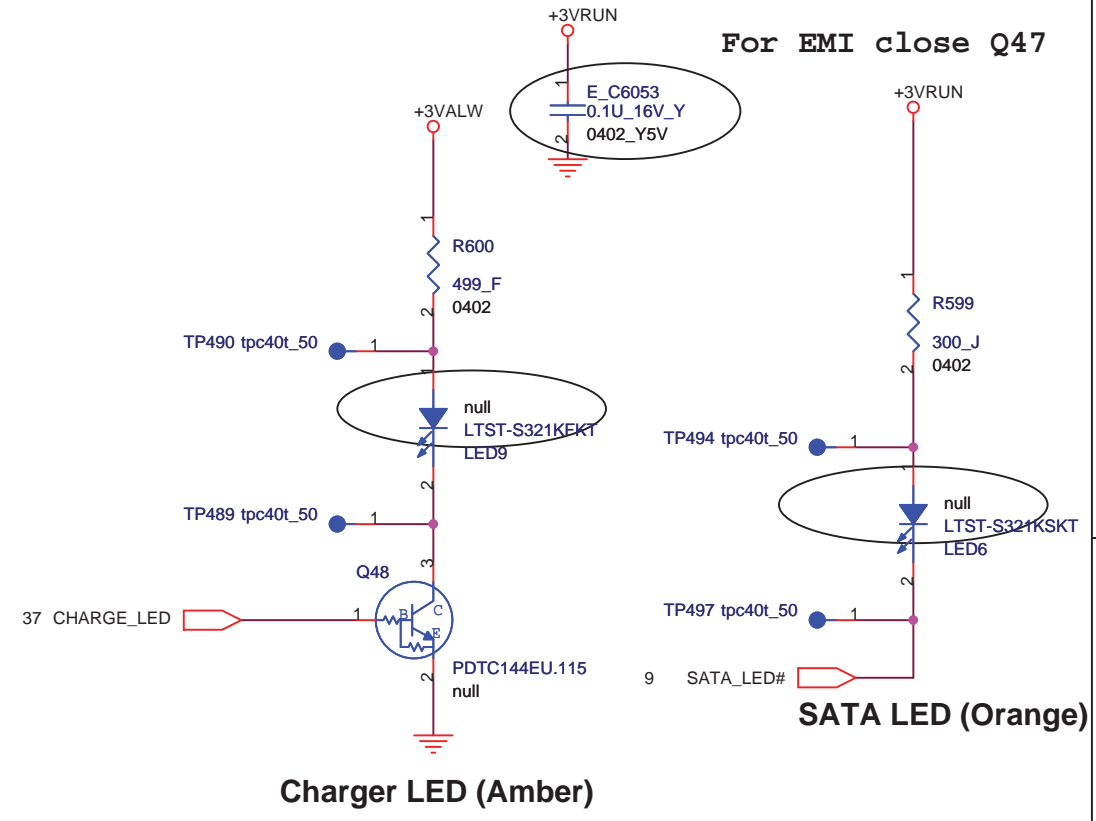
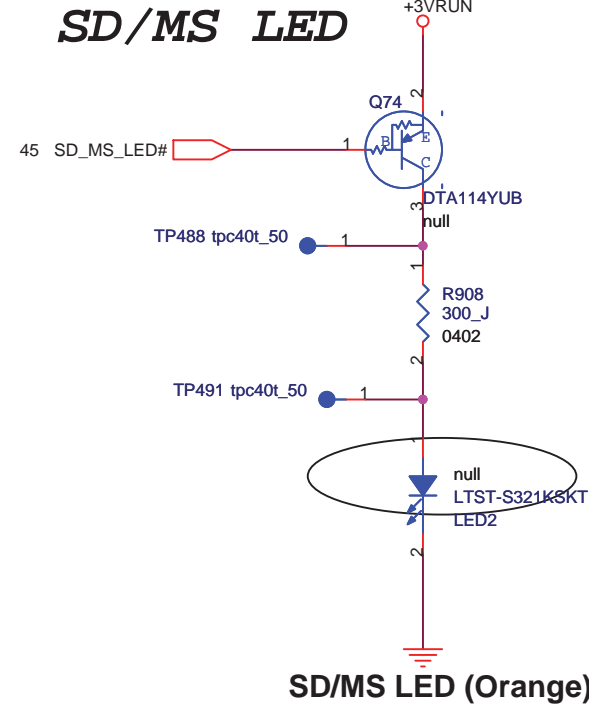
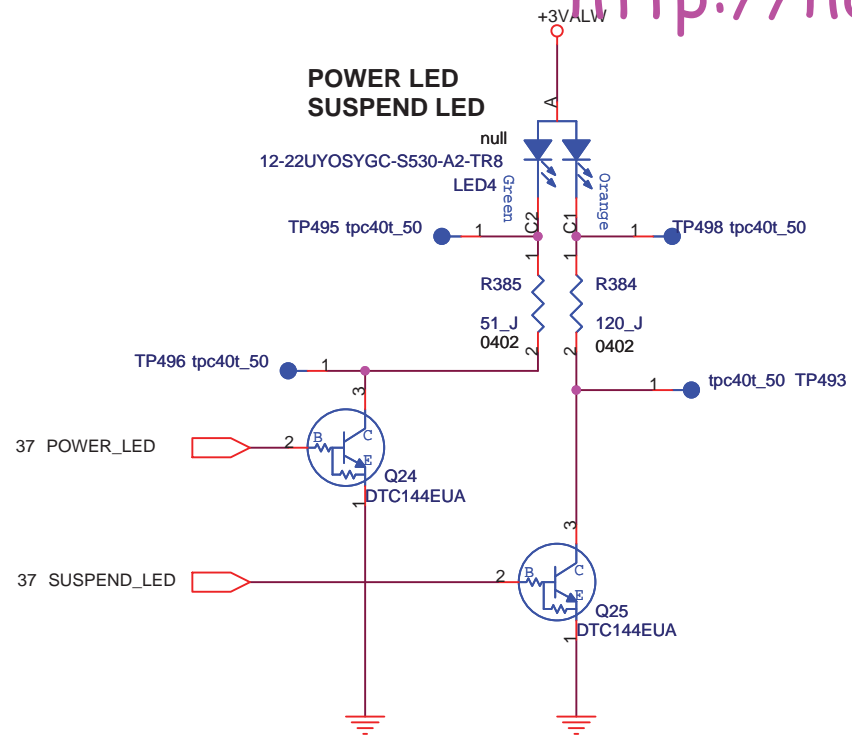
2009.0921
WIRELESS_DATA/WIRELESS_CHCLK follow M930



2009.11.19
Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

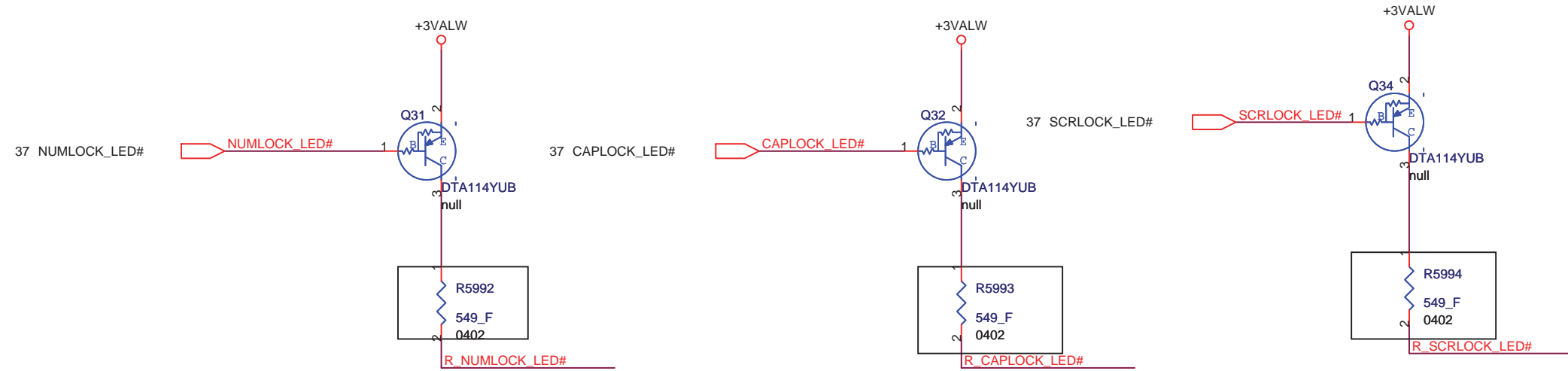
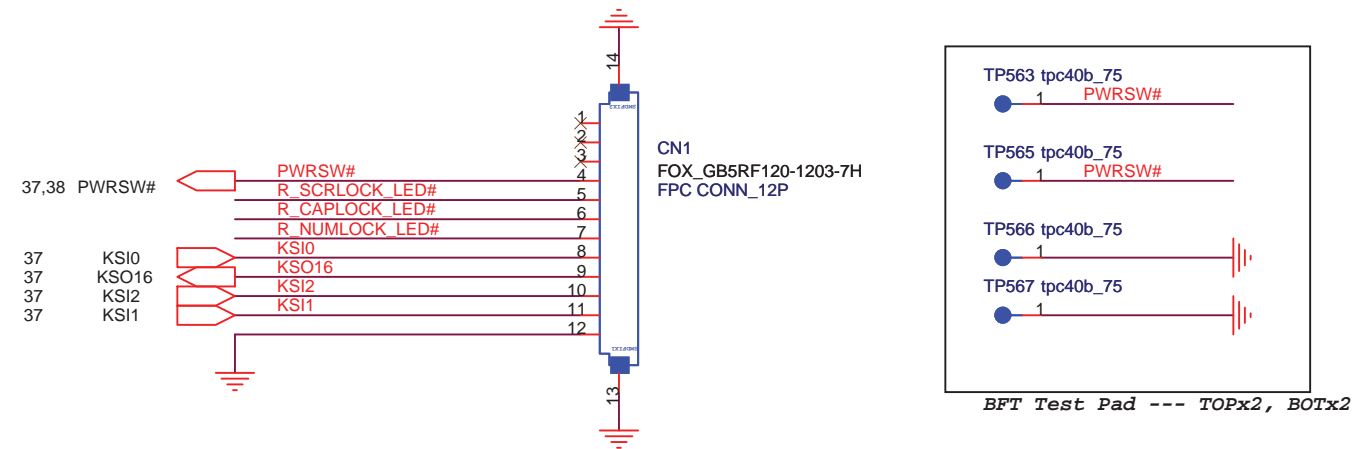
Bluetooth



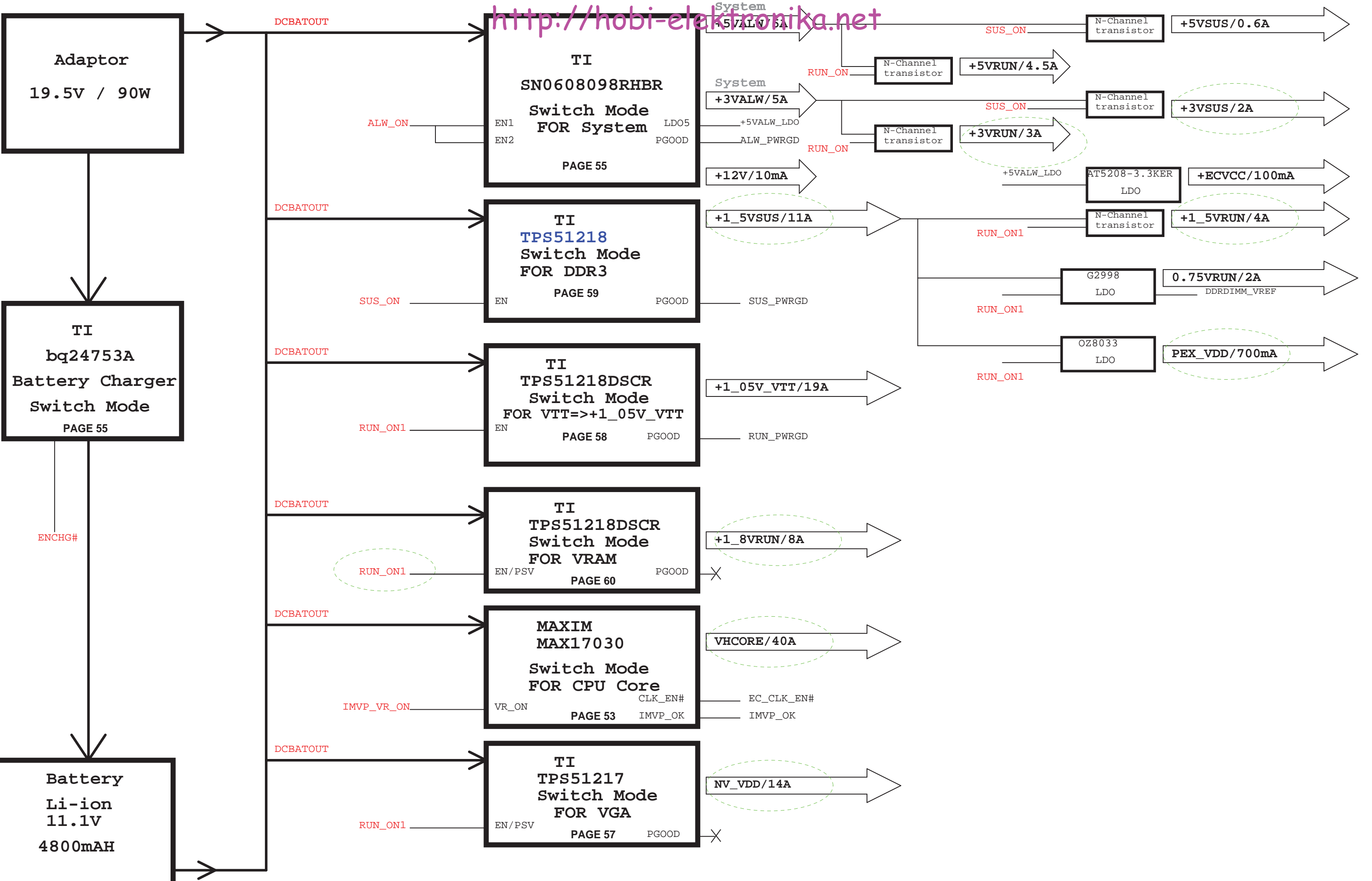


2009/09/10
Add test point for L6 TE request

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title LED & T/P & LID		CCPBG - R&D Division	
Size A3	Document Number M9A0_MP	Rev 1.1	
Date: Friday, October 23, 2009	Sheet 50	of 73	

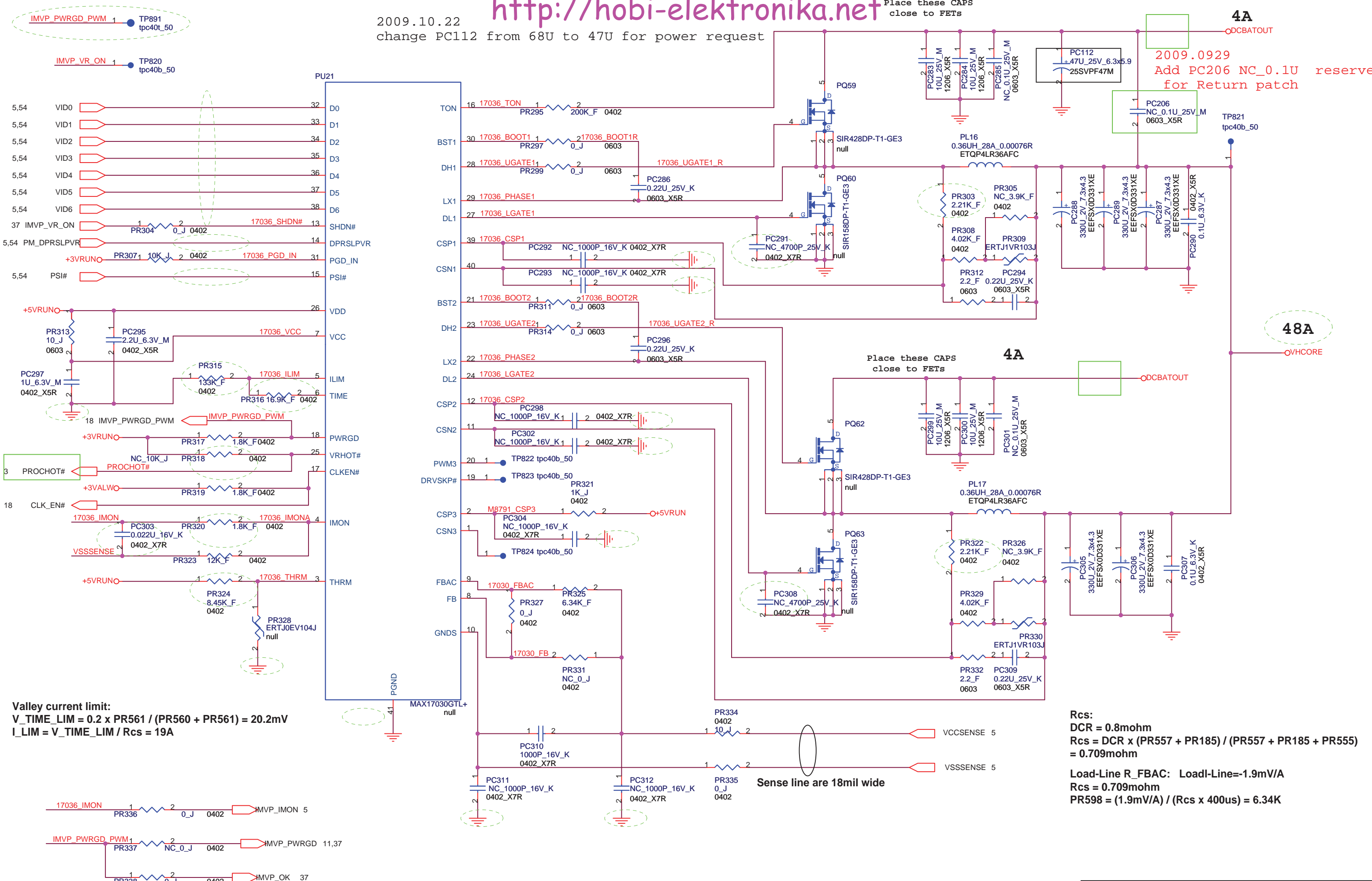


2009.10.30
change R5992,R5993,R5994 from 120ohm to 549ohm follow M870



2009.10.22
change PC112 from 68U to 47U for power request

2009.0929
Add PC206 NC_0.1U_25V_M reserve for Return patch



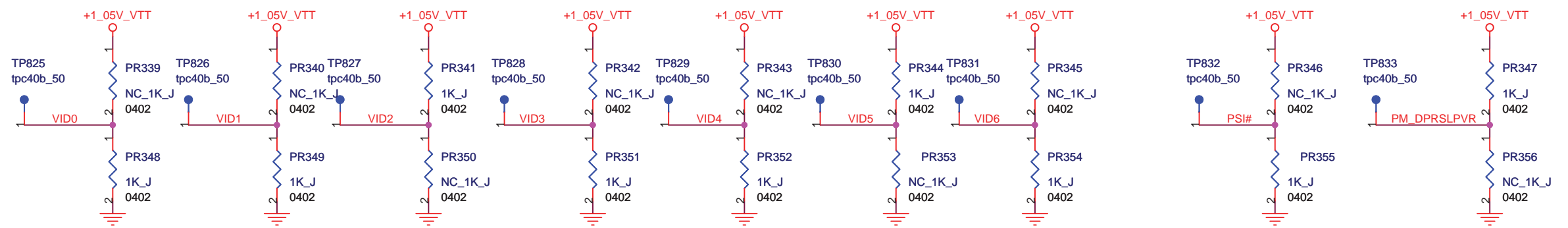
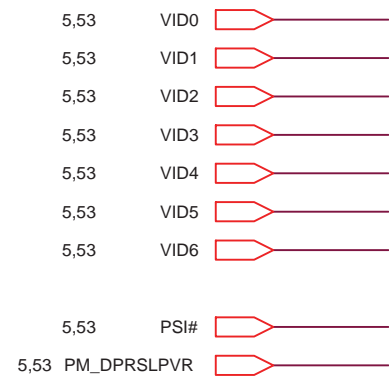
Valley current limit:
 $V_TIME_LIM = 0.2 \times PR561 / (PR560 + PR561) = 20.2mV$
 $I_LIM = V_TIME_LIM / Rcs = 19A$

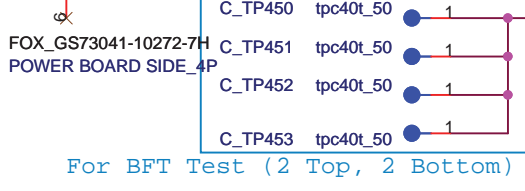
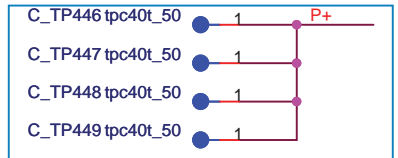
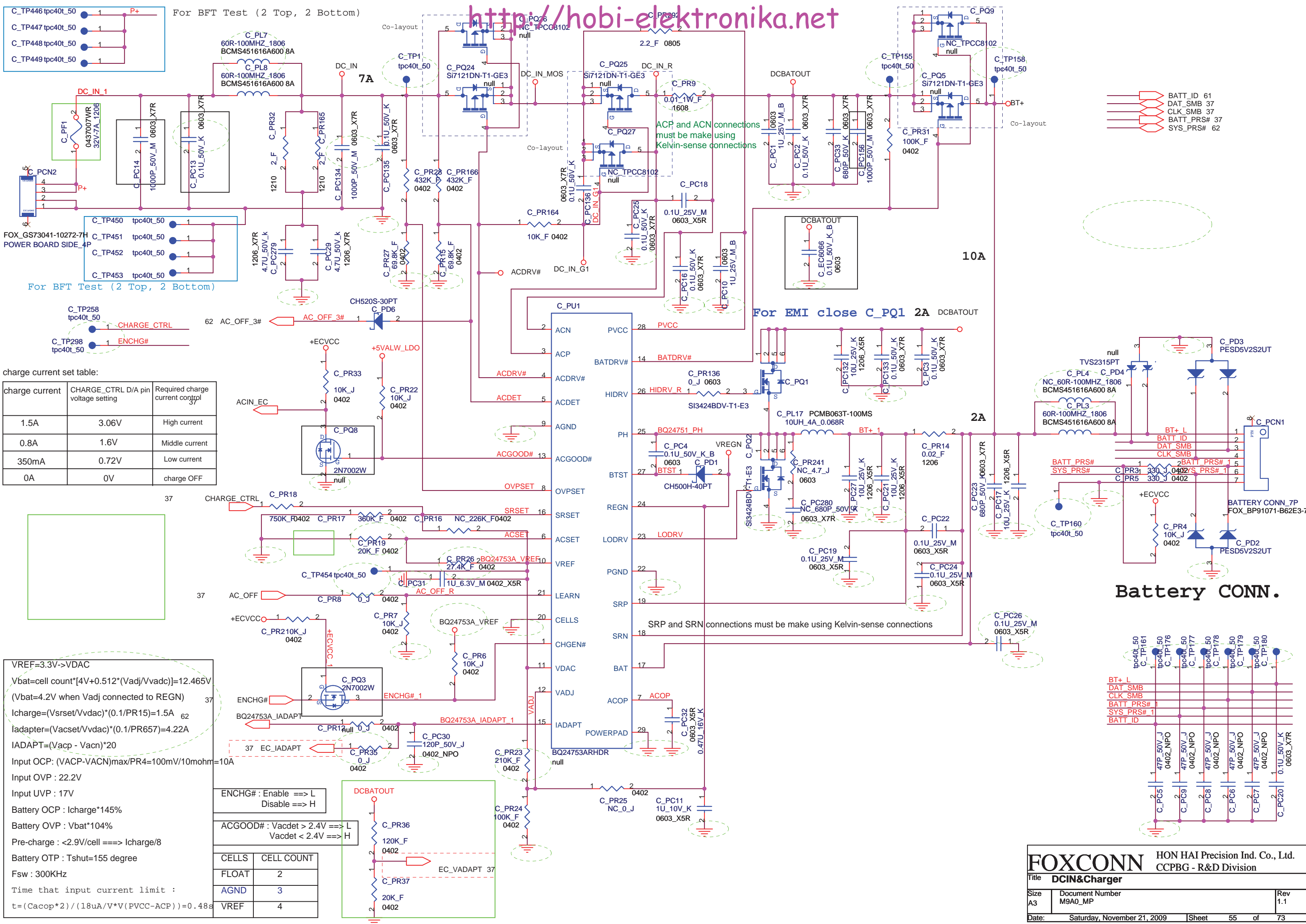
Rcs:
 $DCR = 0.8mohm$
 $Rcs = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm$
 Load-Line R_FBAC: Load-Line=-1.9mV/A
 $Rcs = 0.709mohm$
 $PR598 = (1.9mV/A) / (Rcs \times 400us) = 6.34K$

Sense line are 18mil wide

Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)
 - 416056_416056_Ard_EDS_Rev.1.1 - 403779_Clarksfield_MPG_Rev1.5





charge current set table:

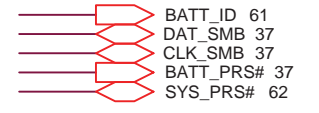
charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V->VDAC
 $V_{bat} = \text{cell count} * [4V + 0.512 * (V_{adj} / V_{vdc})] = 12.465V$
 (Vbat=4.2V when Vadj connected to REGN)
 $I_{charge} = (V_{srset} / V_{vdc}) * (0.1 / PR15) = 1.5A$
 $I_{adapter} = (V_{vacset} / V_{vdc}) * (0.1 / PR657) = 4.22A$
 $IADAPT = (V_{vacp} - V_{vacn}) * 20$
 Input OCP: $(V_{acp} - V_{acn})_{max} / PR4 = 100mV / 10mohm = 10A$
 Input OVP: 22.2V
 Input UVP: 17V
 Battery OCP: $I_{charge} * 145\%$
 Battery OVP: $V_{bat} * 104\%$
 Pre-charge: $< 2.9V / \text{cell} \implies I_{charge} / 8$
 Battery OTP: $T_{shut} = 155 \text{ degree}$
 Fsw: 300KHz
 Time that input current limit:
 $t = (C_{acop} * 2) / (18uA / V * V(PVCC - ACP)) = 0.48s$

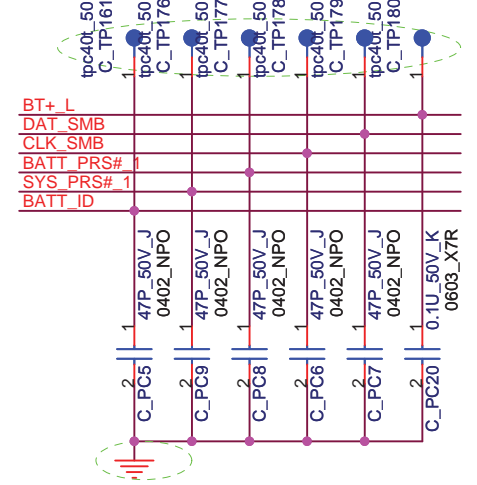
ENCHG#: Enable ==> L
 Disable ==> H

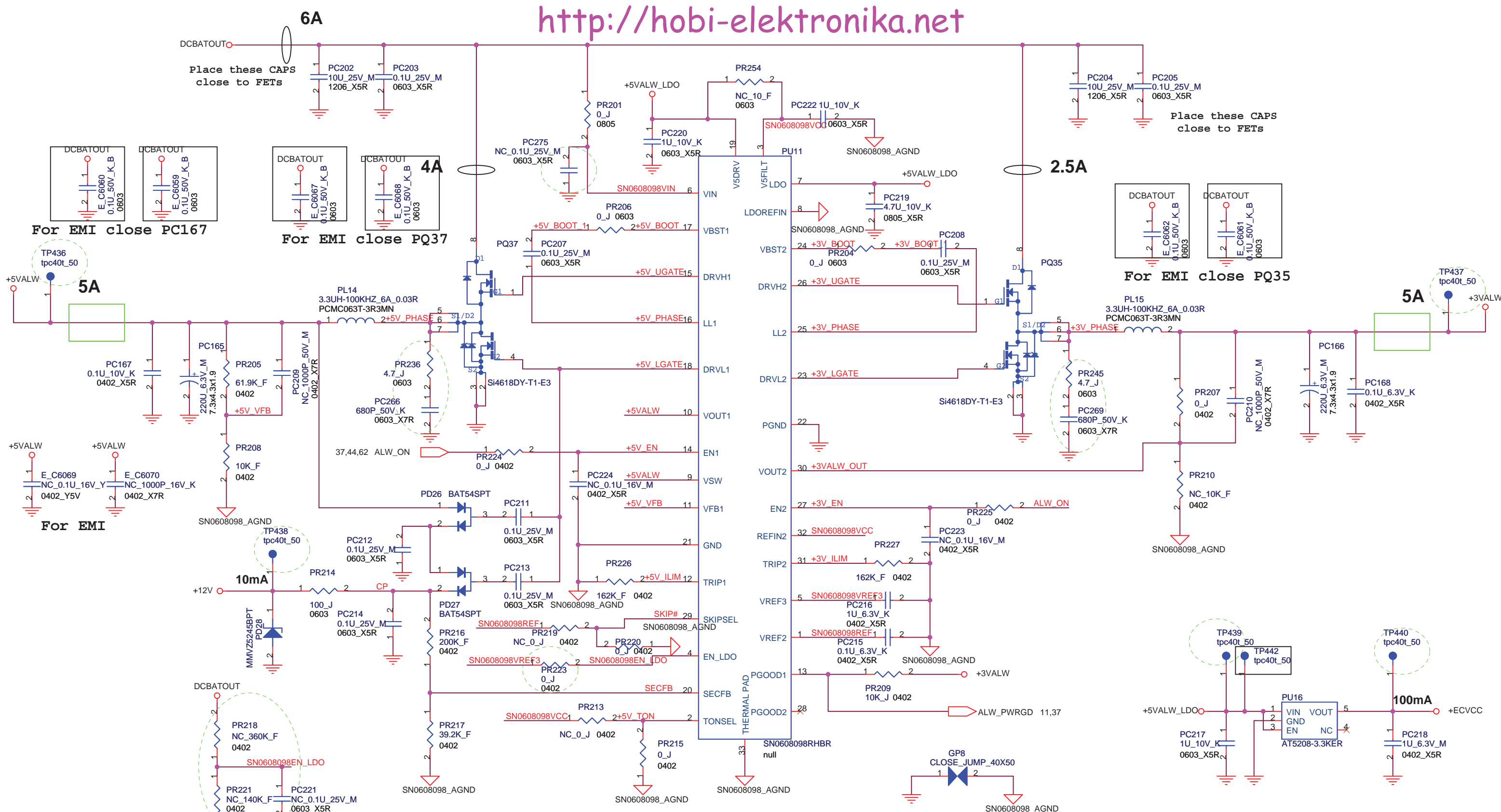
ACGOOD#: $V_{acdet} > 2.4V \implies L$
 $V_{acdet} < 2.4V \implies H$

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4



Battery CONN.





2009.0925
change PR245, PC269, PR236, PC266 from NC to mount for EMI request

TON	Operating Freqence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / ((VIN * f * LIR * ILOAD(MAX)))$$

$$Rocp = (Iocp - Iripple / 2) * (10 * Rds(on)) / 5u$$

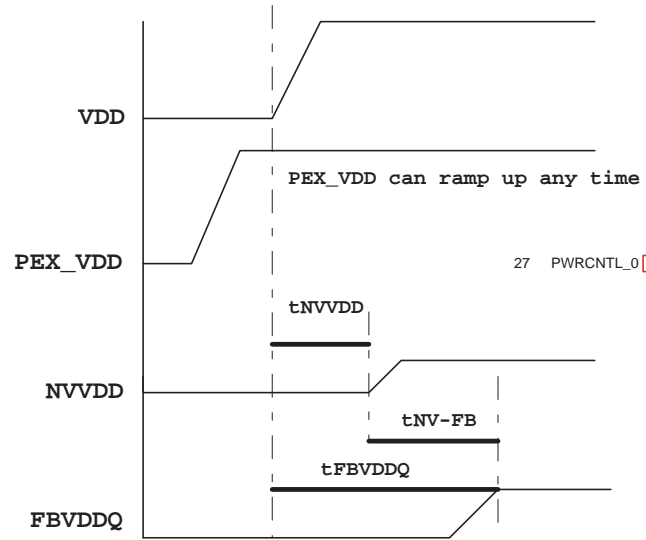
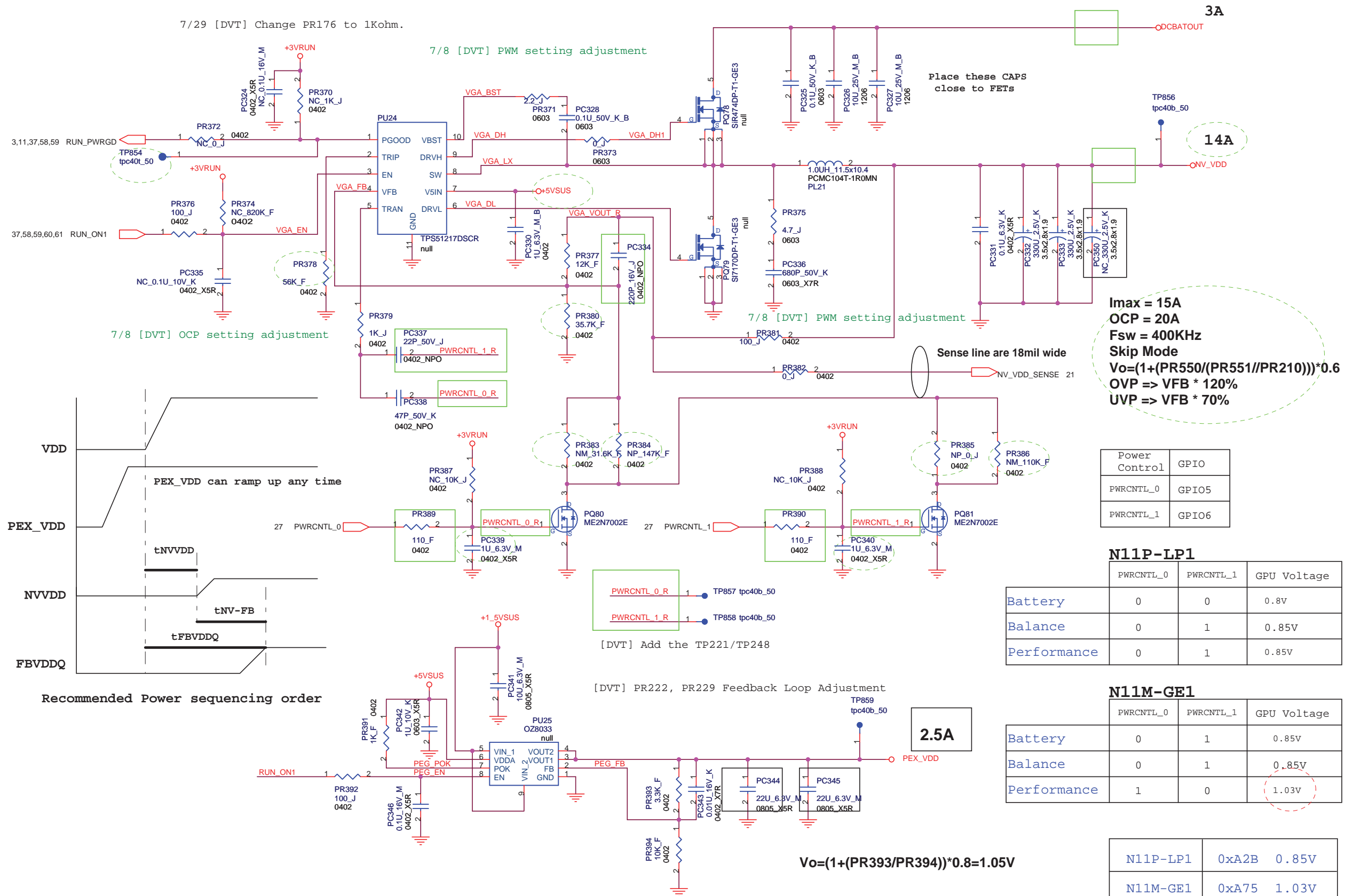
$$+5VALW = ((PR205 / PR208) + 1) * VFB1$$

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **SYS Power (+3_3V/+5V)**

Size A3	Document Number M9A0_MP	Rev 1.1
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Date: Wednesday, November 04, 2009 | Sheet 56 of 73



I_{max} = 15A
OCP = 20A
F_{sw} = 400KHz
Skip Mode
 $V_o = (1 + (PR550/(PR551//PR210))) * 0.6$
OVP => VFB * 120%
UVP => VFB * 70%

Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

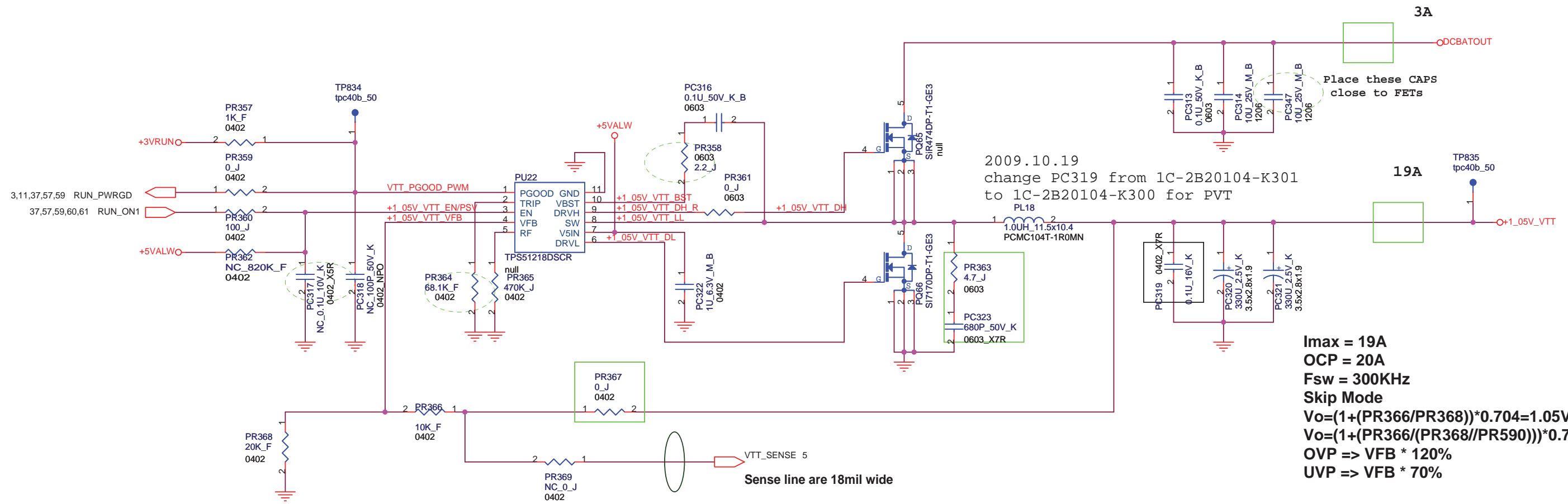
N11P-LP1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
Battery	0	0	0.8V
Balance	0	1	0.85V
Performance	0	1	0.85V

N11M-GE1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
Battery	0	1	0.85V
Balance	0	1	0.85V
Performance	1	0	1.03V

N11P-LP1	0xA2B	0.85V
N11M-GE1	0xA75	1.03V
P8		0.85 V
P12		0.8 V



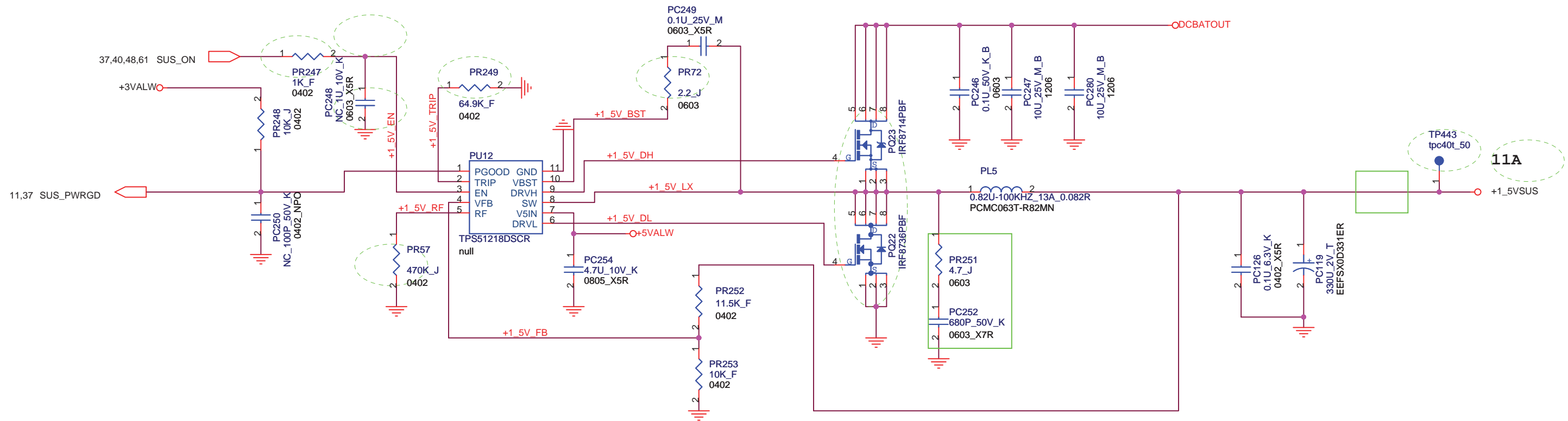
2009.10.19
change PC319 from 1C-2B20104-K301 to 1C-2B20104-K300 for PVT

Imax = 19A
OCP = 20A
Fsw = 300KHz
Skip Mode
 $V_o = (1 + (PR366/PR368)) * 0.704 = 1.05V$
 $V_o = (1 + (PR366/(PR368//PR590))) * 0.704 = 1.1V$
OVP => VFB * 120%
UVP => VFB * 70%

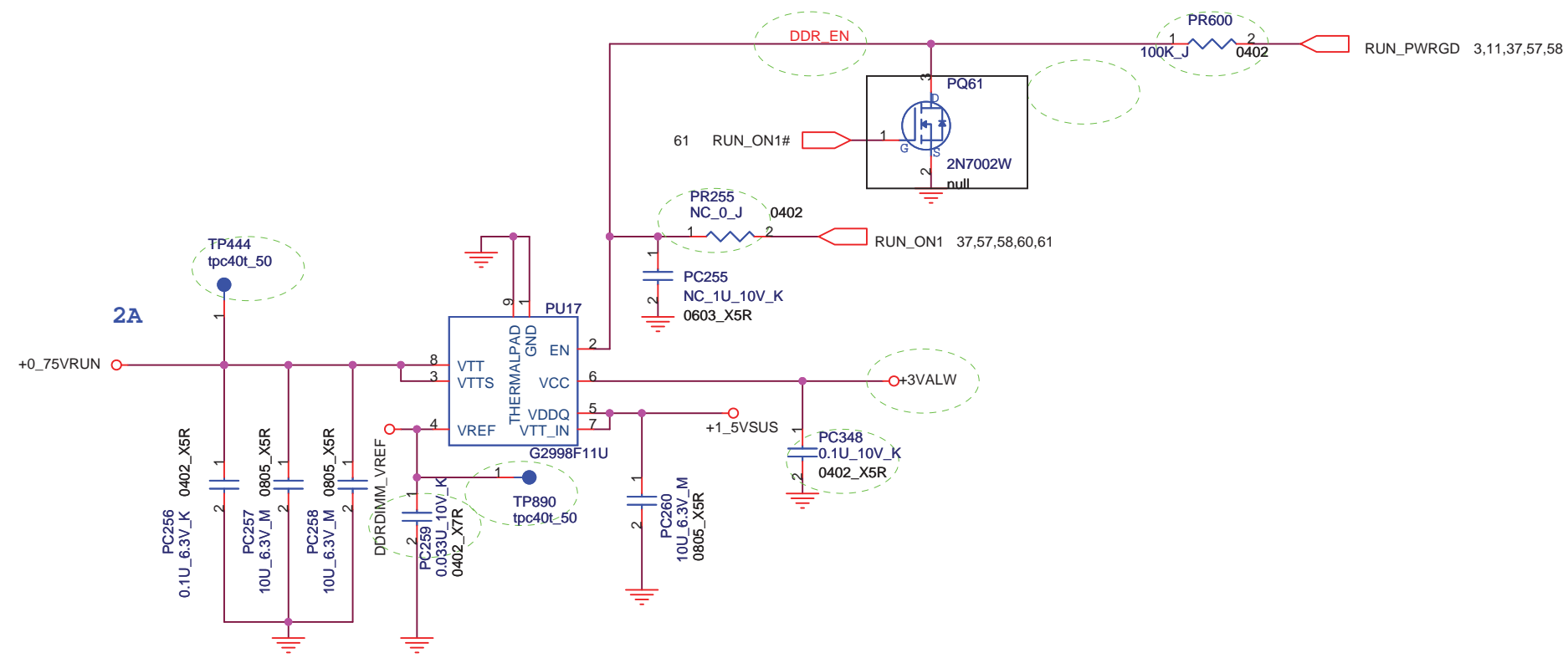
2009.0925
change PR363, PC323 from NC to mount for EMI request

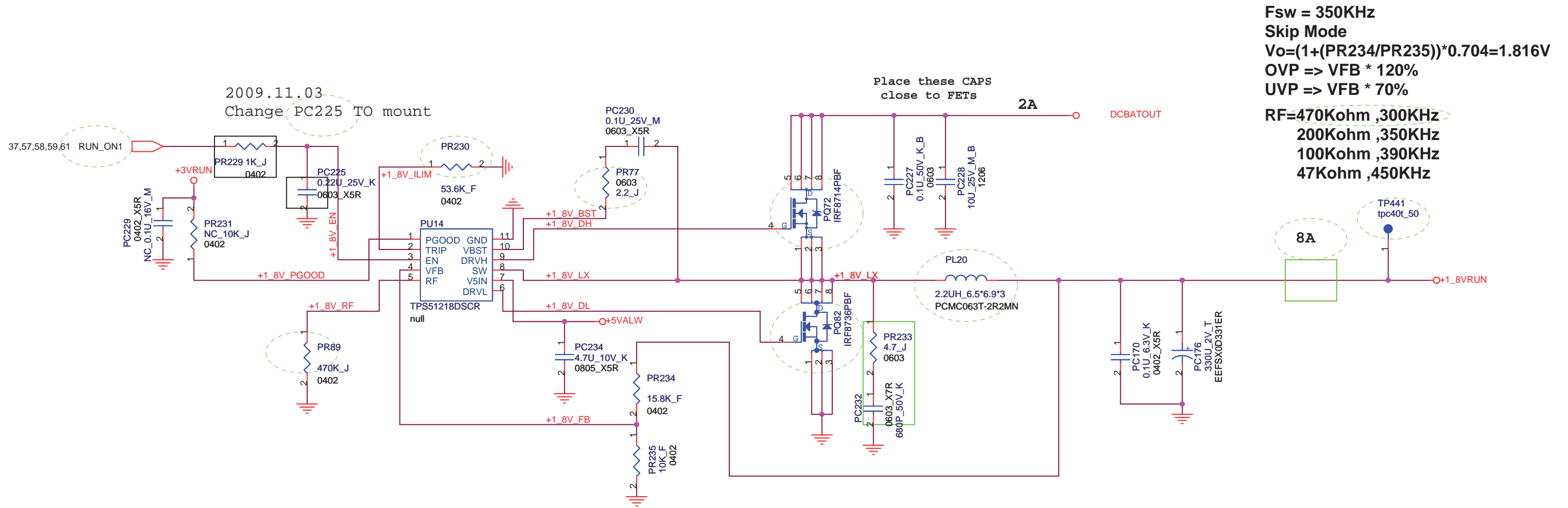
~~RF=470Kohm, 300KHz~~
200Kohm, 350KHz
100Kohm, 390KHz
47Kohm, 450KHz

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	DDR3 Power(+1.5V/+0.75V)		
Size	Document Number	Rev	
Custom	M9A0_MP	1.1	
Date:	Wednesday, November 04, 2009	Sheet	58 of 73



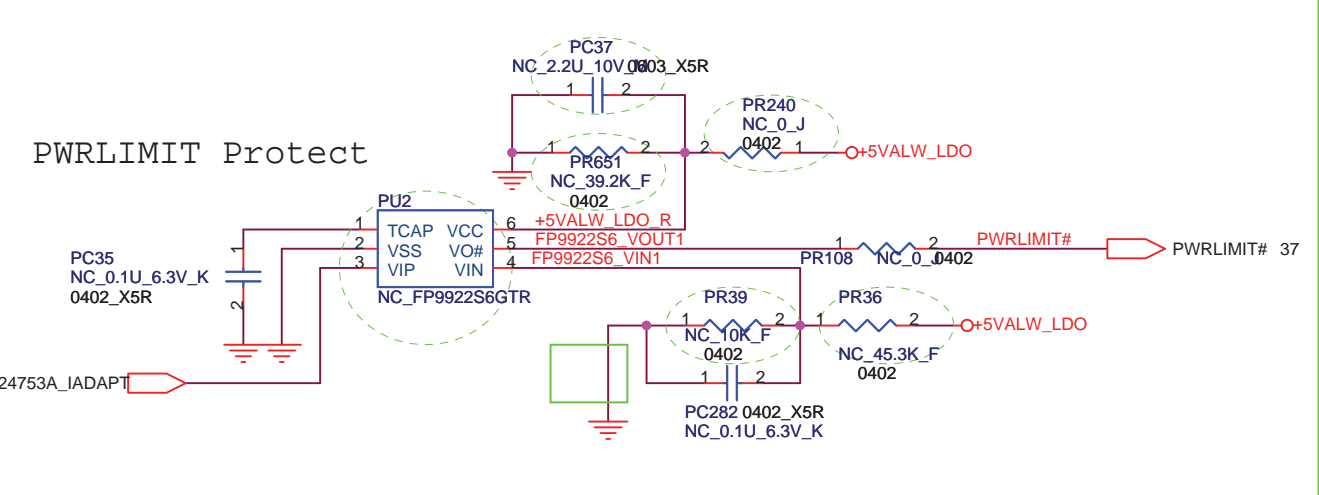
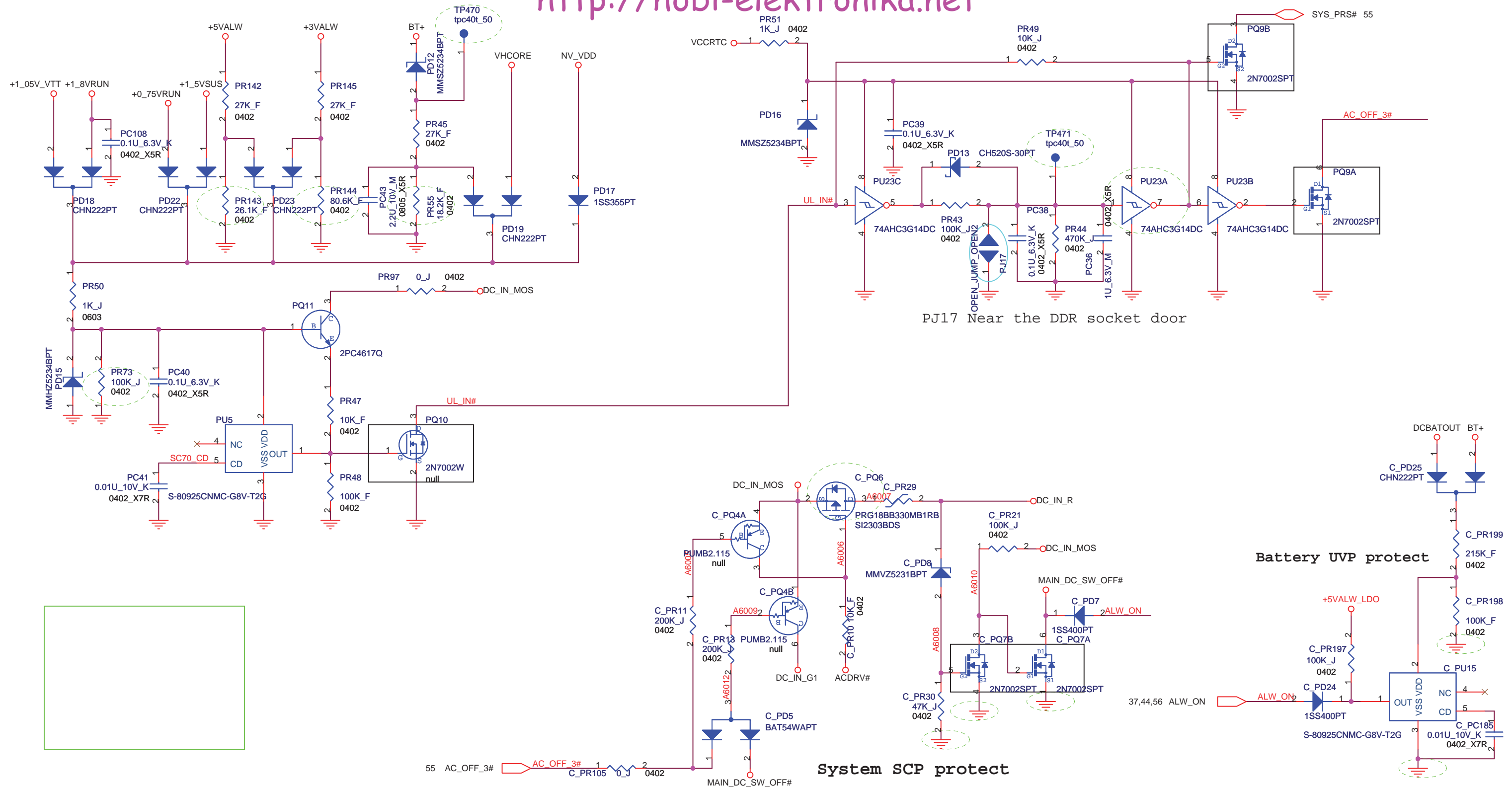
2009.0925
change PR251,PC252 from NC to mount for EMI request





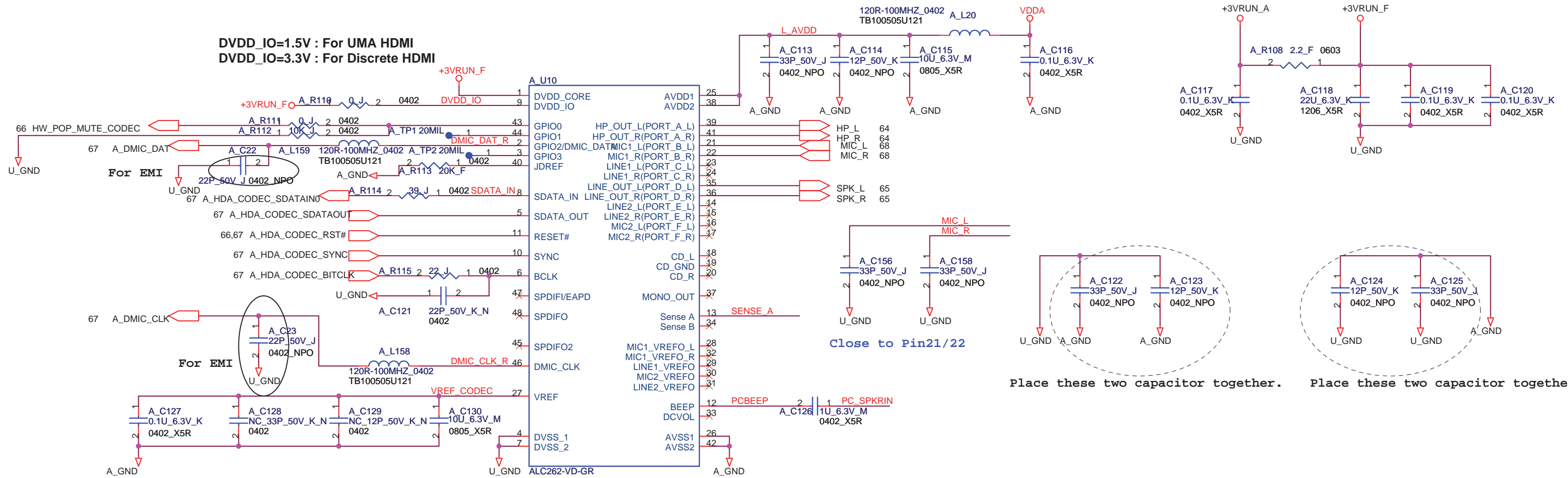
Fsw = 350KHz
Skip Mode
 $V_o = (1 + (PR234/PR235)) * 0.704 = 1.816V$
OVP => VFB * 120%
UVP => VFB * 70%
RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

2009.0925
 change PR233, PC232 from NC to mount for EMI request

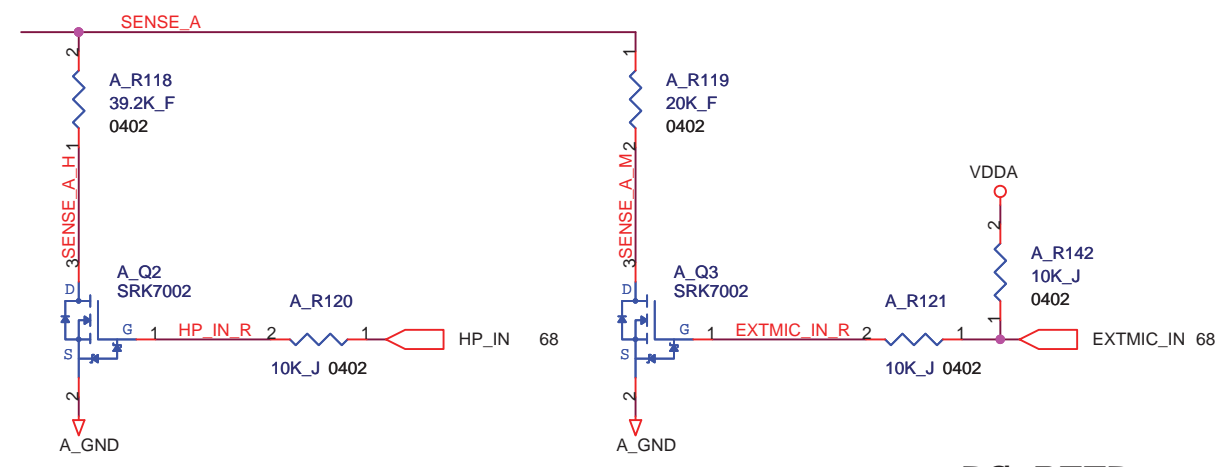


VIINP	90W adaptor
PWRLIMIT	1.3V/85W

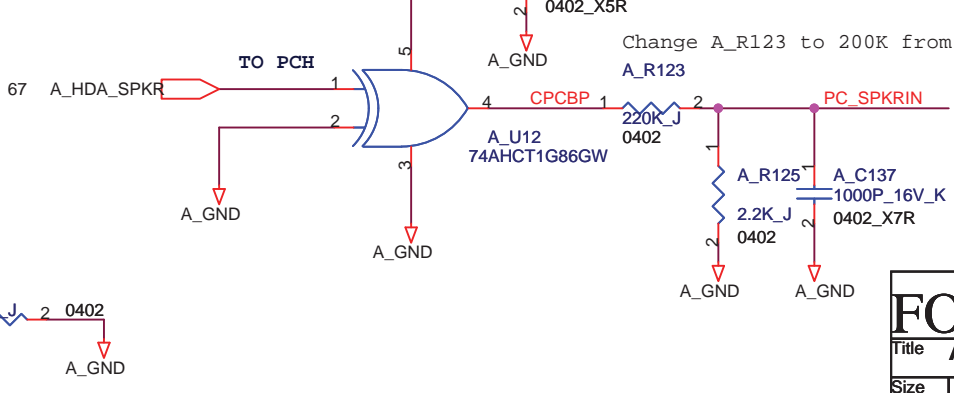
adapter max load : 5.7A/3000ms
adapter OCP : 7.5Amax



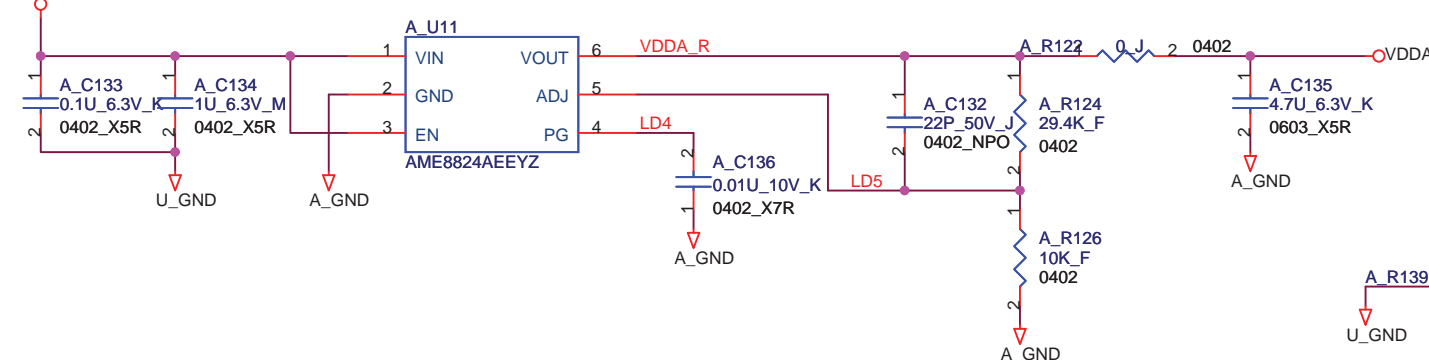
2009.11.03
change A_C23,A_C22 from 15PF to 22PF for EMI request

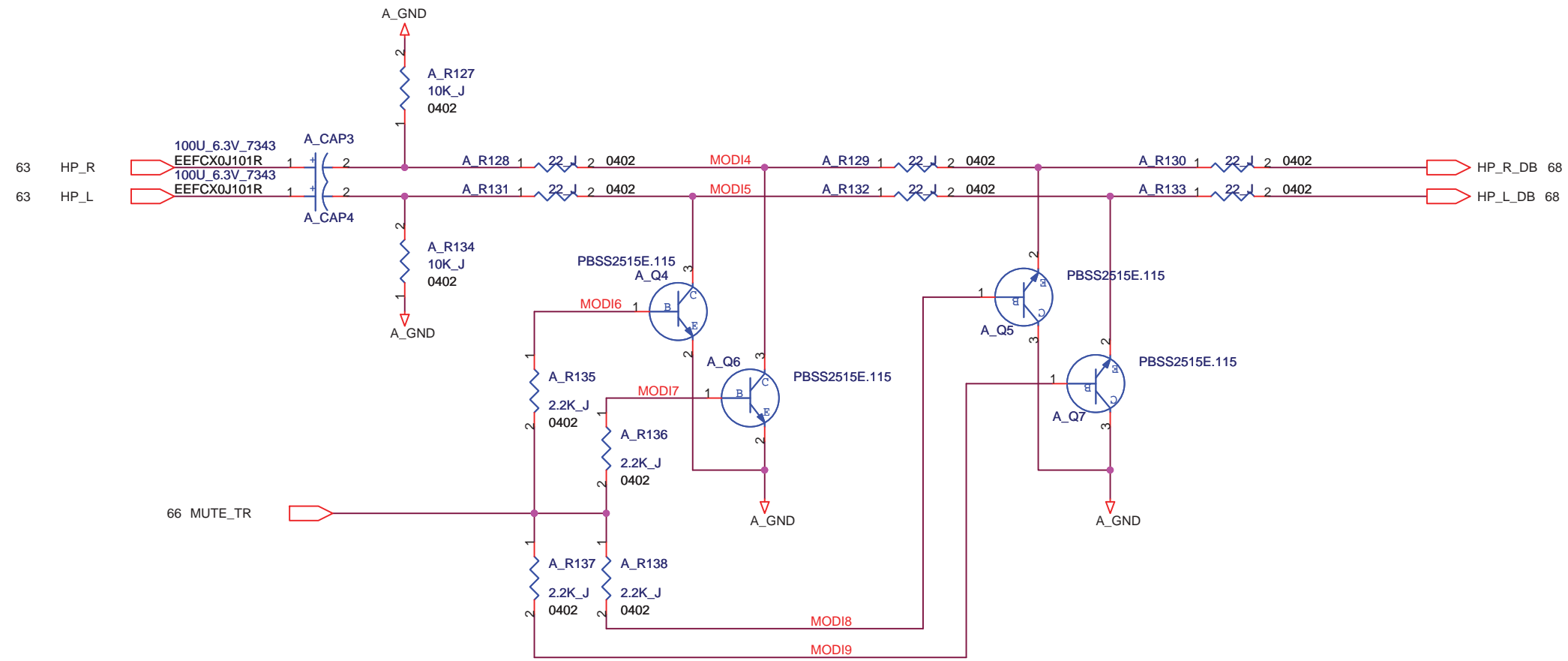


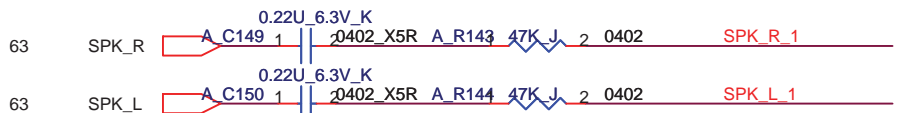
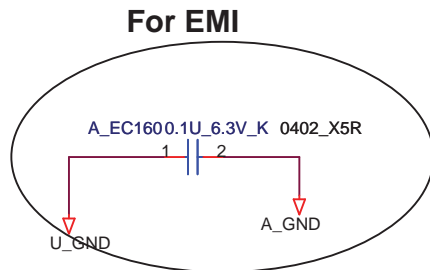
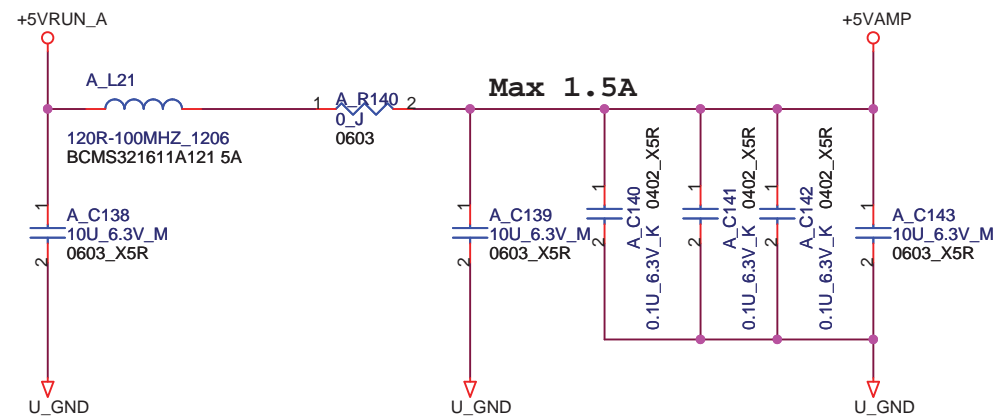
PC BEEP



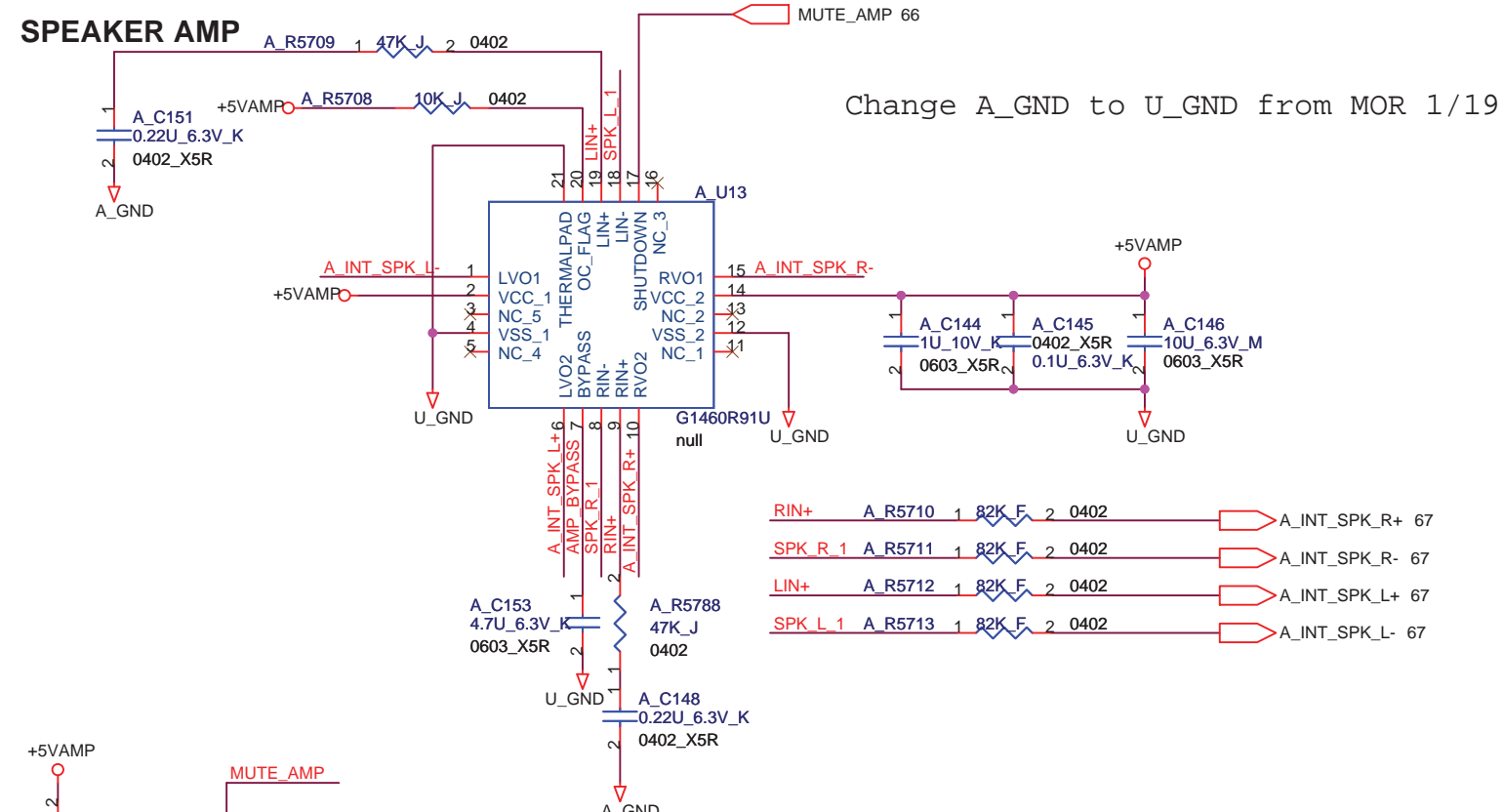
AUDIO POWER (4.75V/300mA)



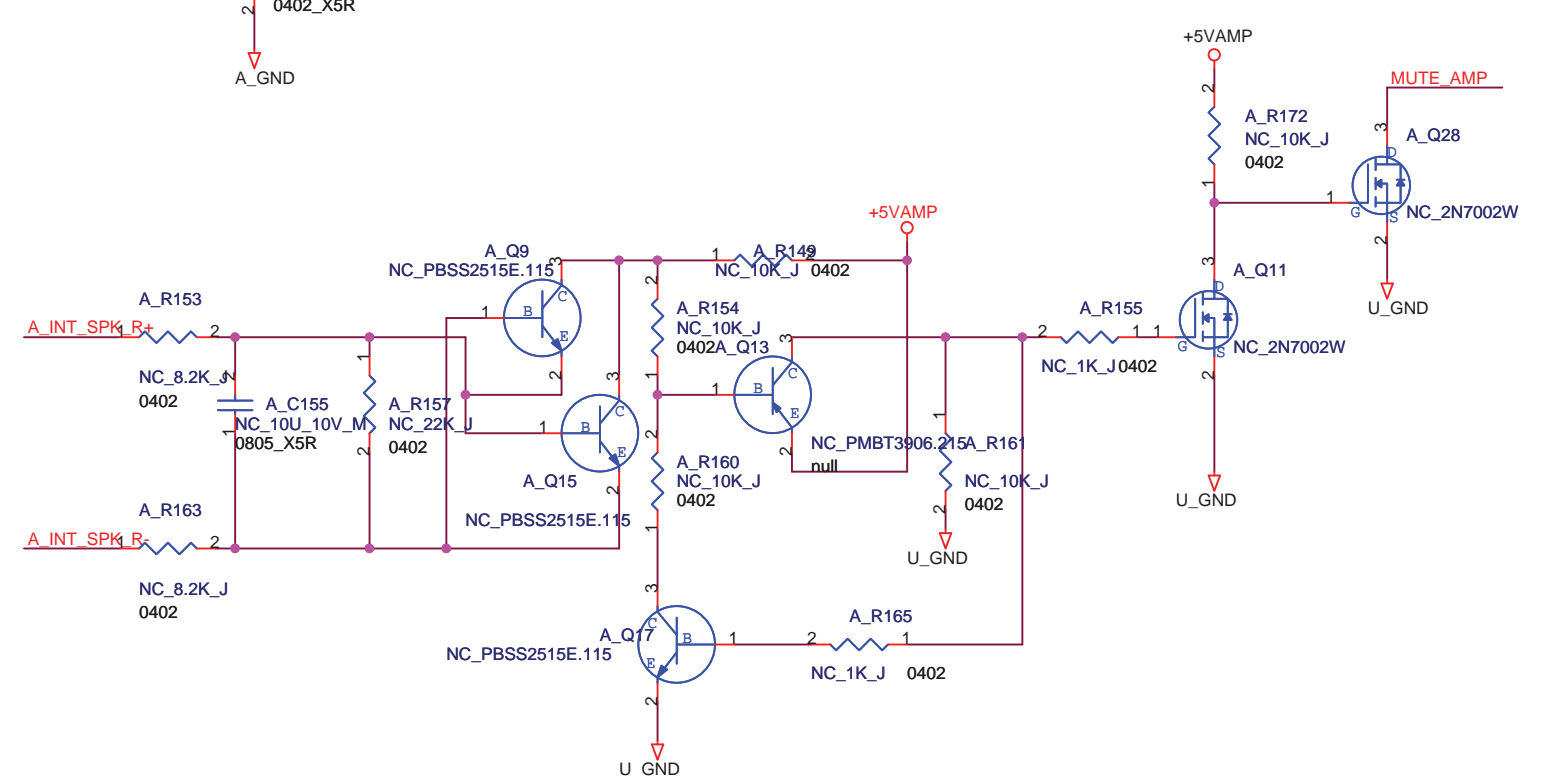
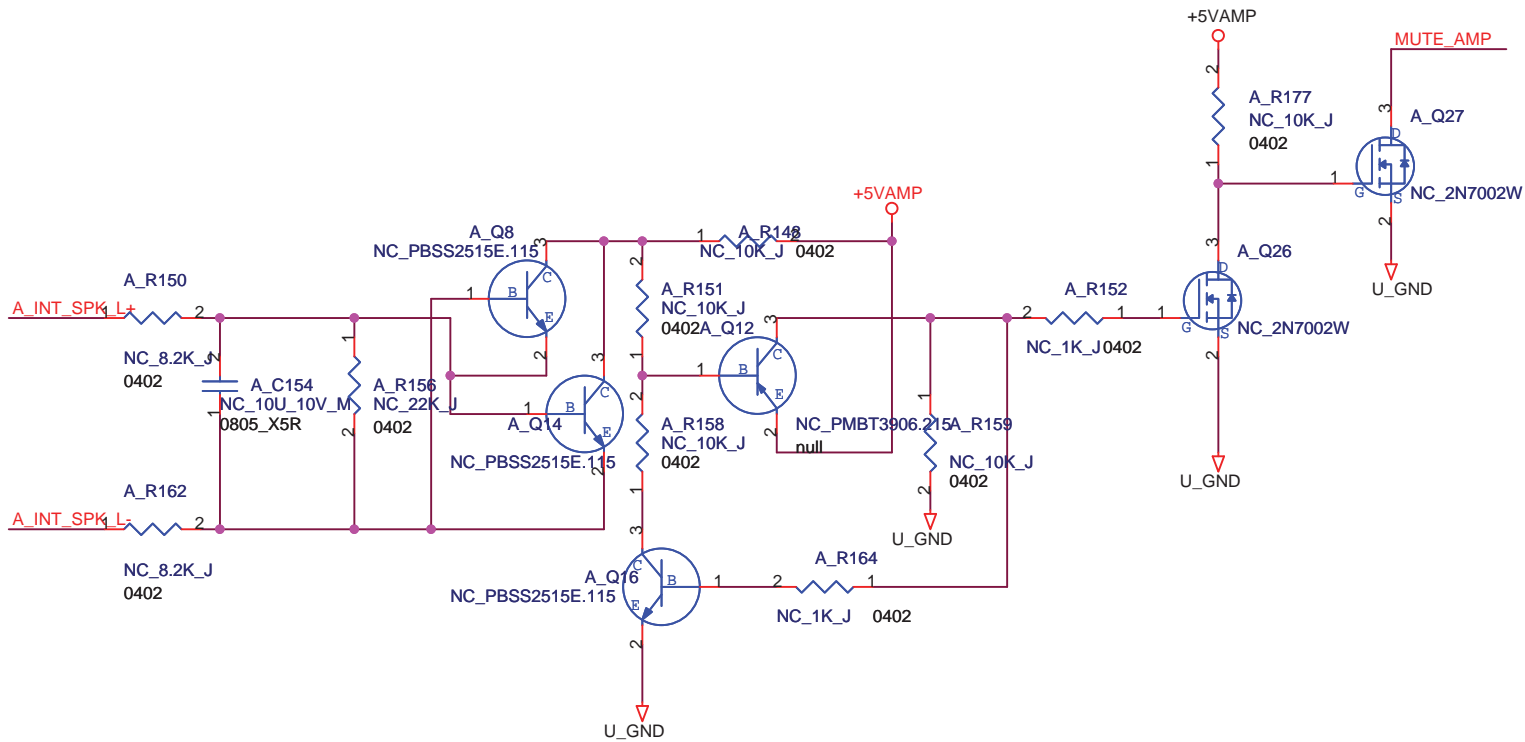




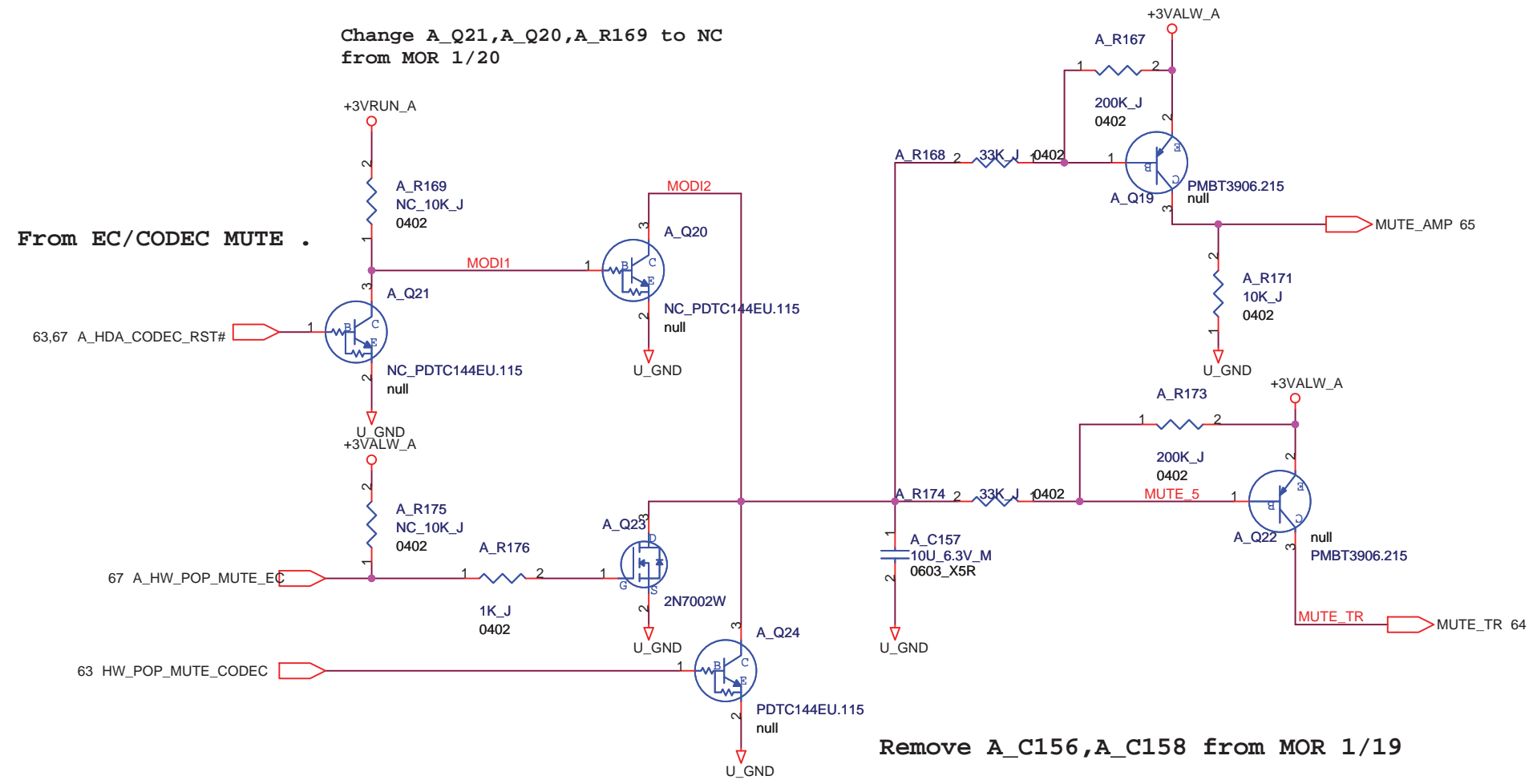
SPEAKER AMP



Change A_GND to U_GND from MOR 1/19

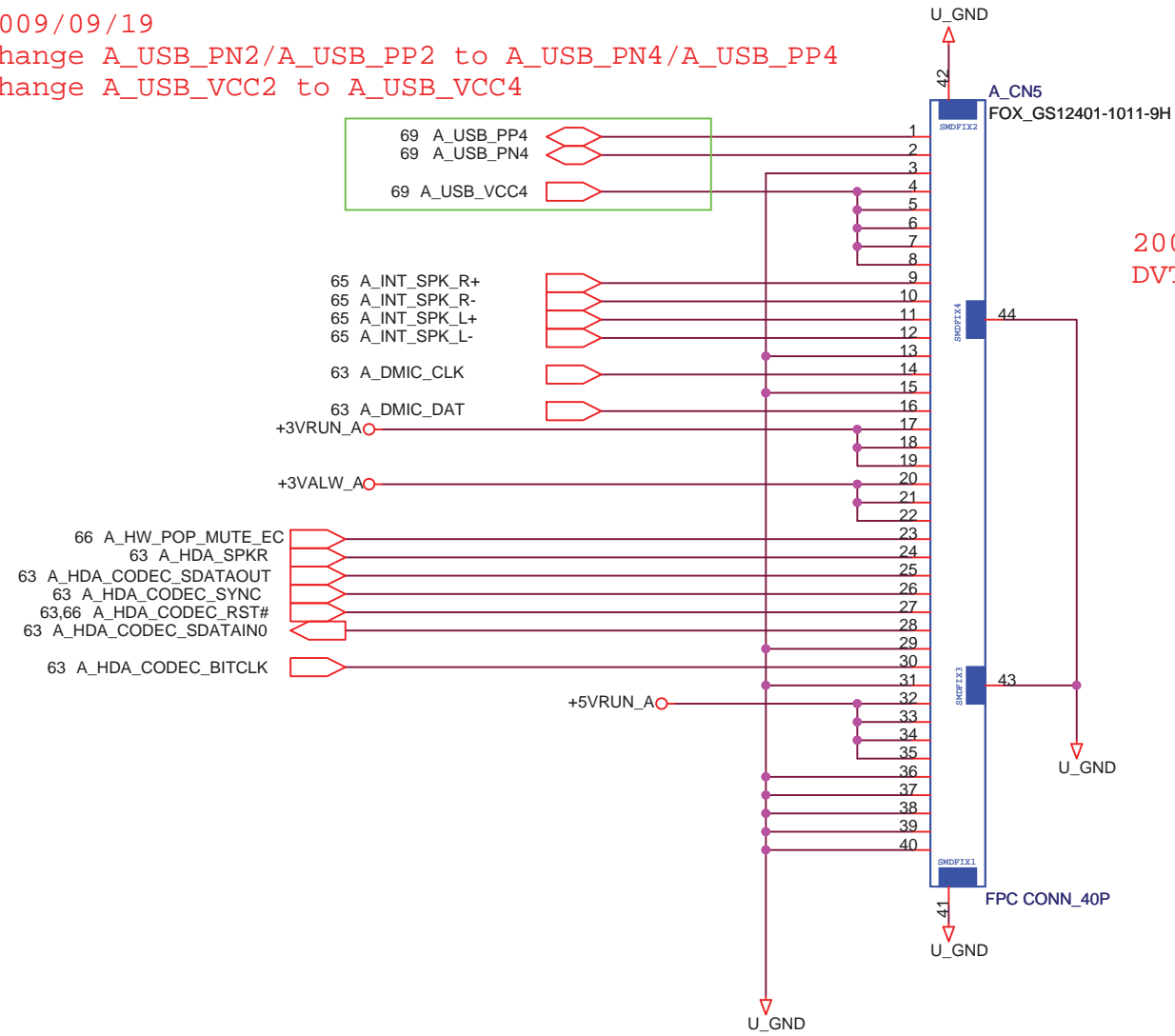


For Mor request, add the speaker cable short protection circuit

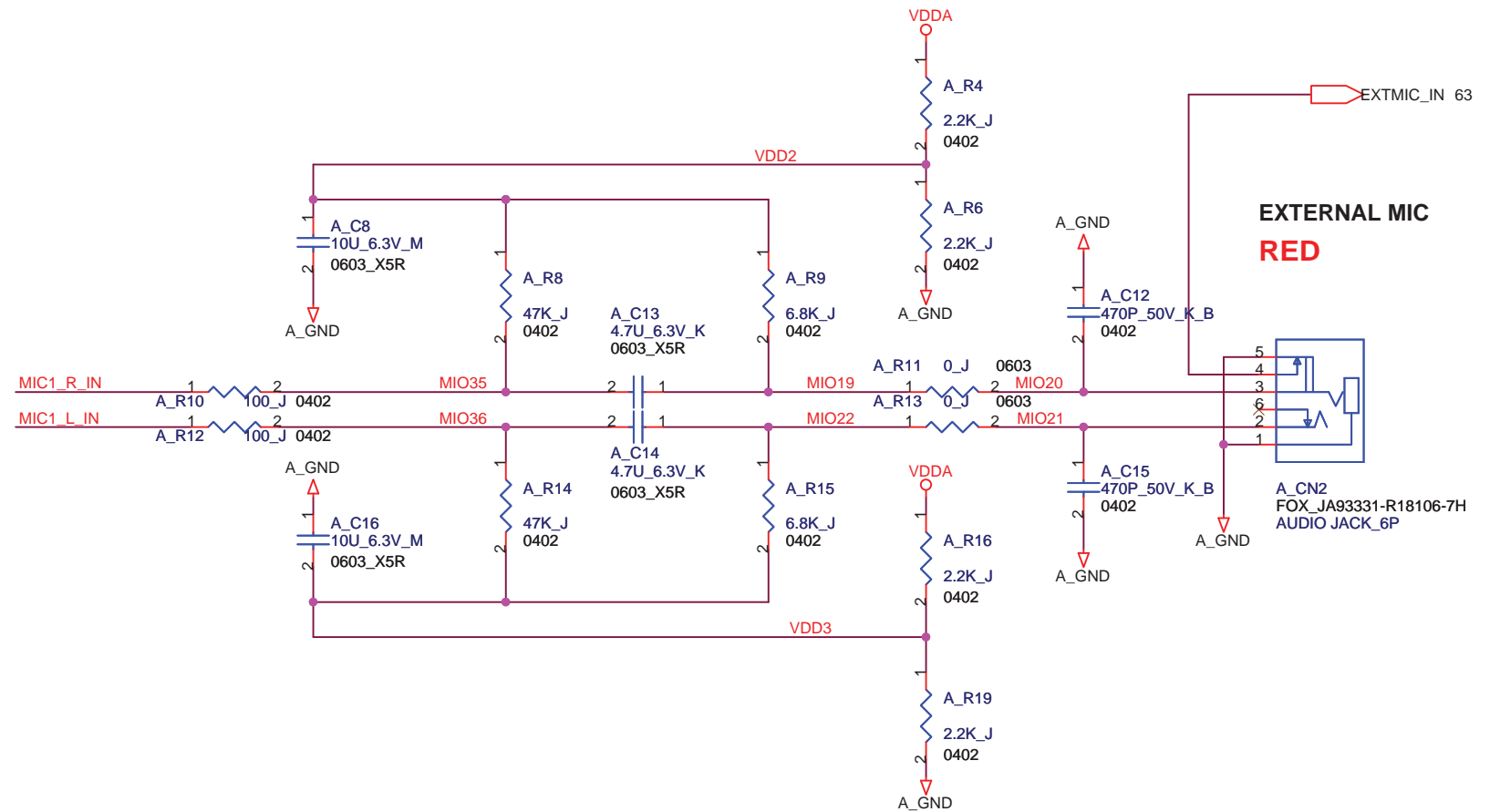
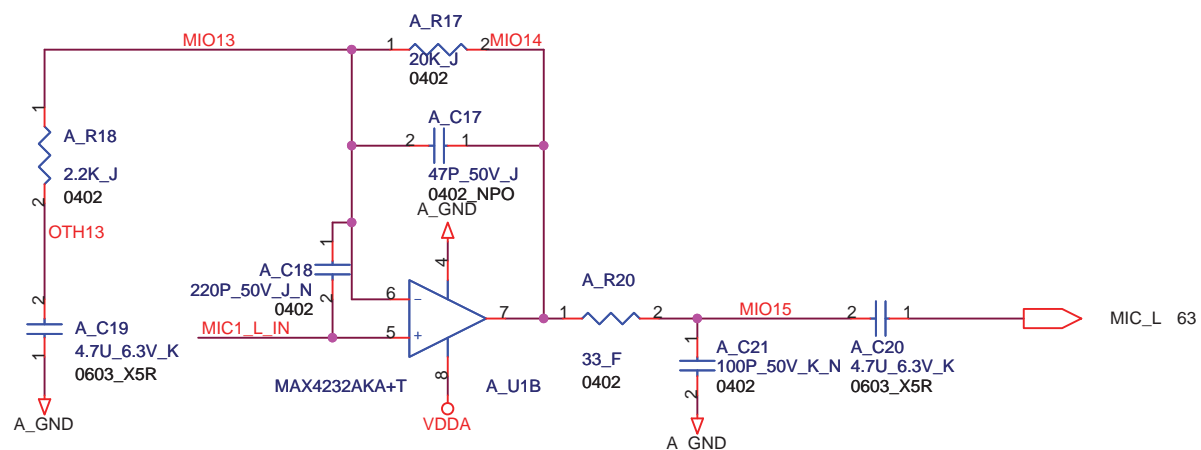
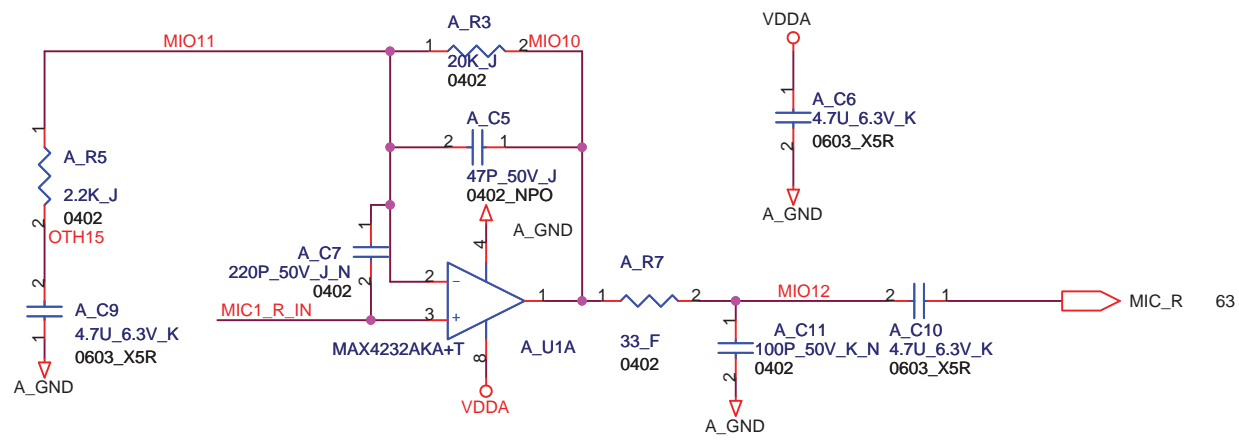
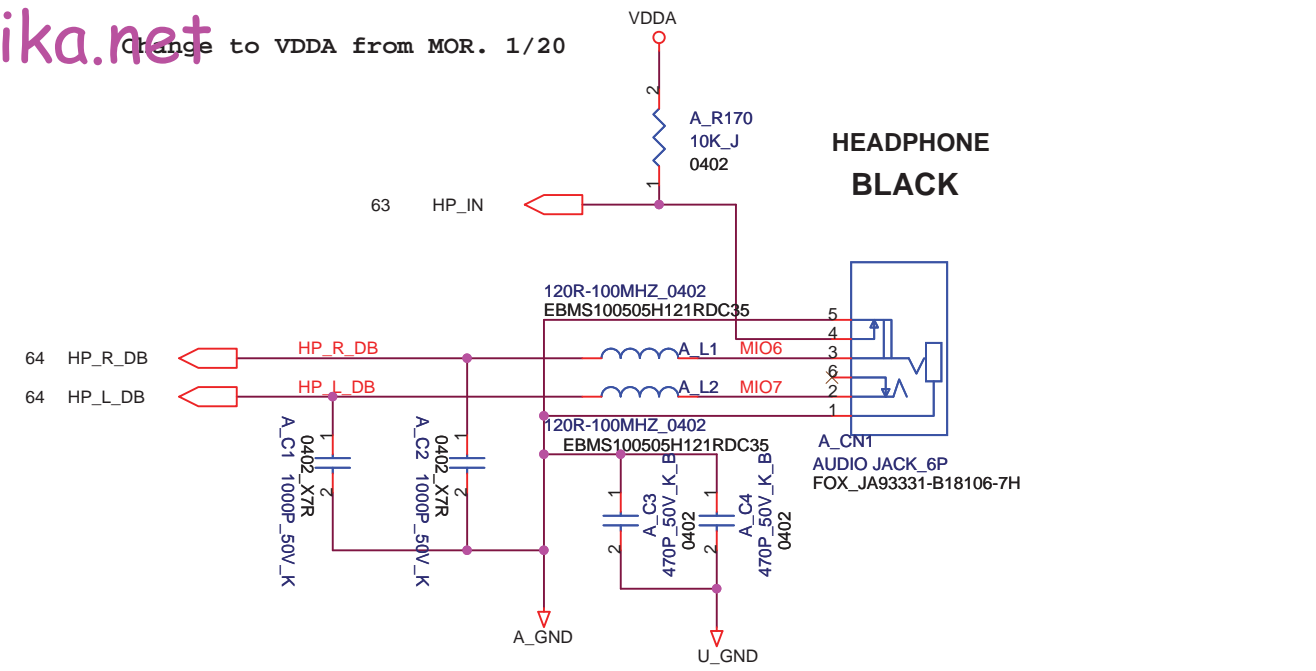


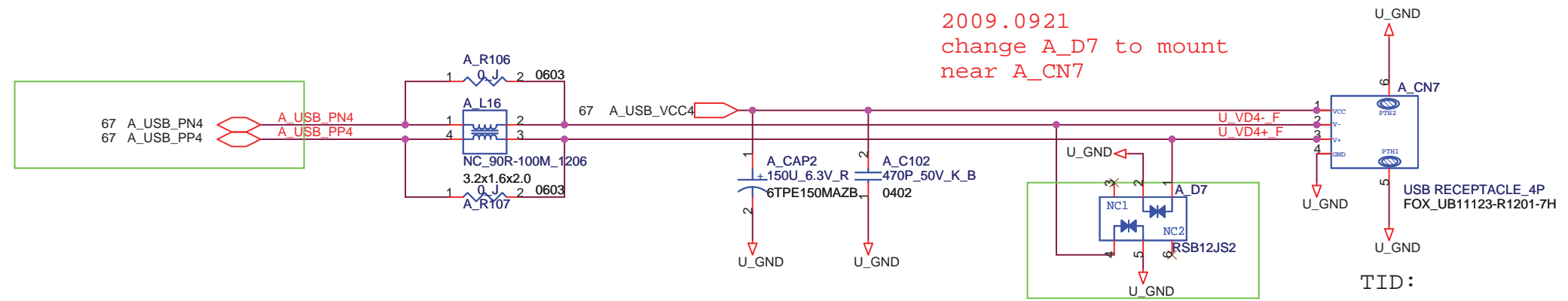
2009/09/19

Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4



2009.0918
DVT2 A_CN5 change to Halogen Free

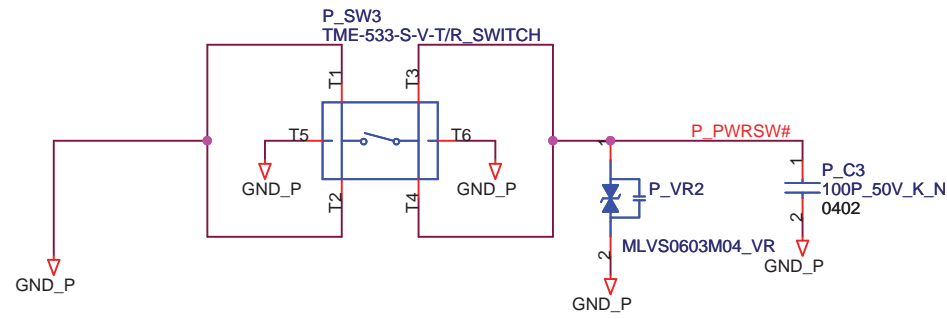




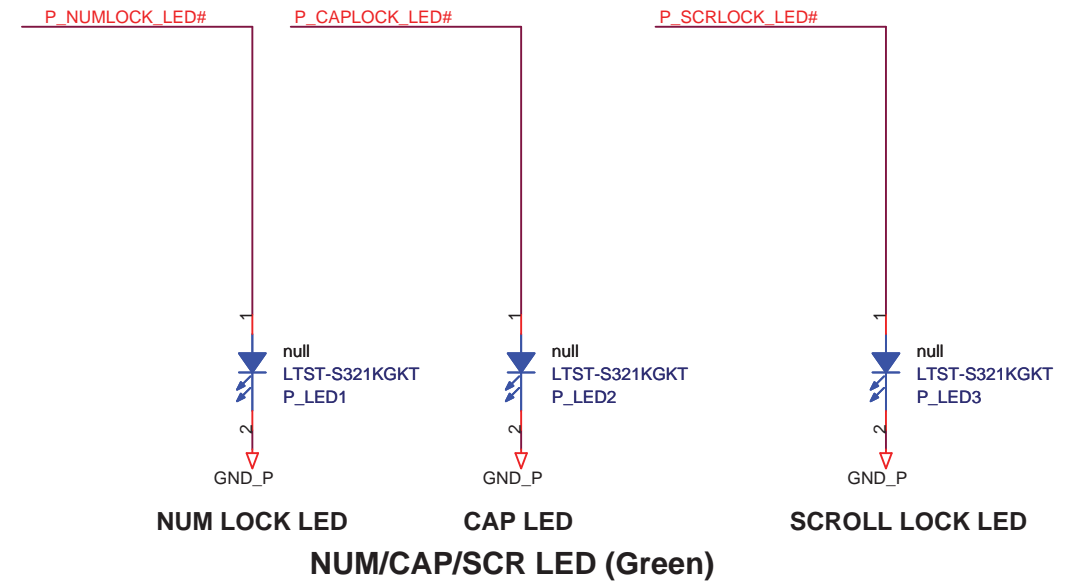
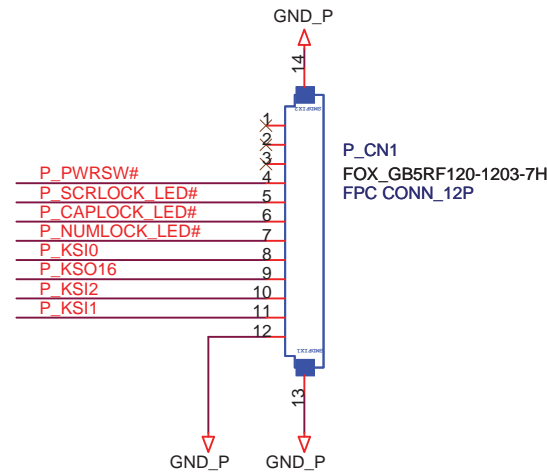
VespaCP no fingerprint function, so this page reserve

FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title FINGER PRINT			
Size A3	Document Number M9A0 MP		Rev 1.1
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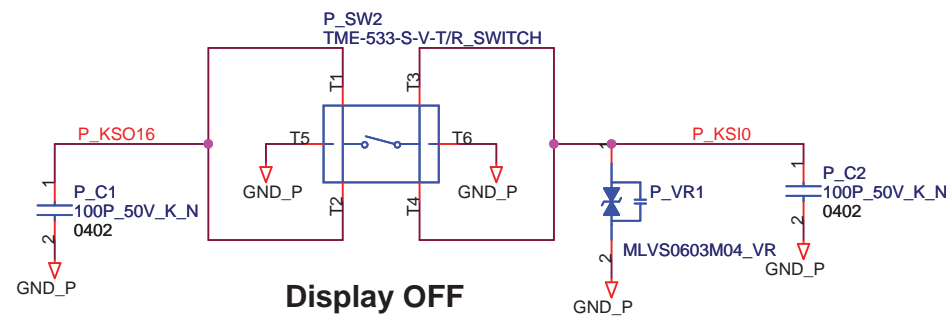
POWER BUTTON



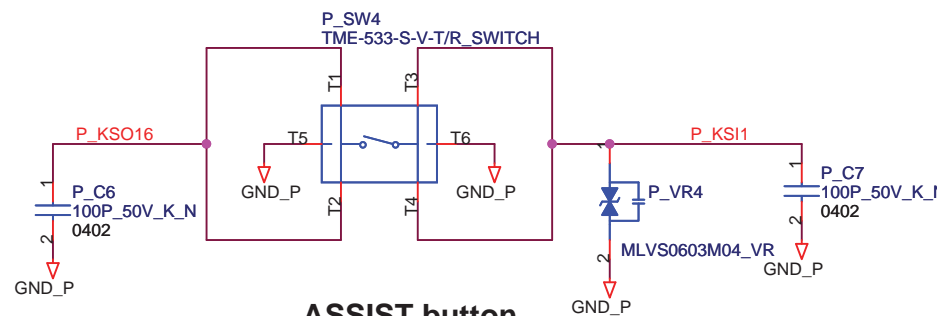
Power Button Board



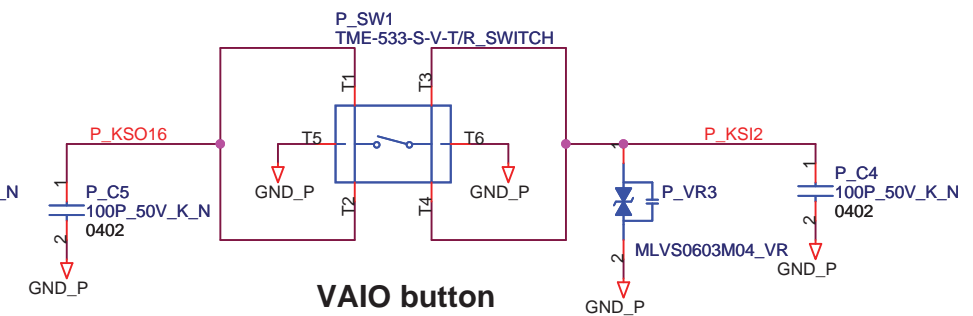
Display OFF

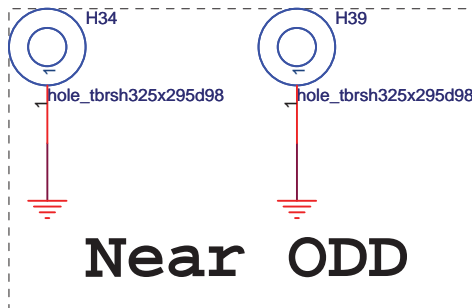
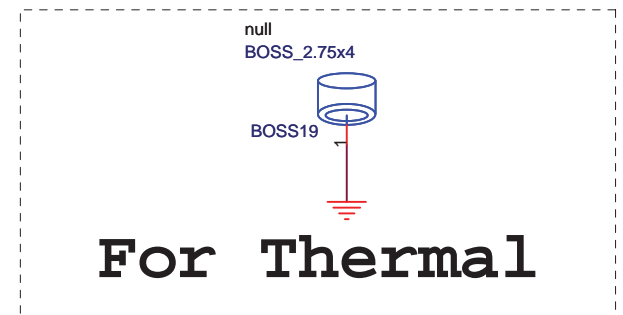
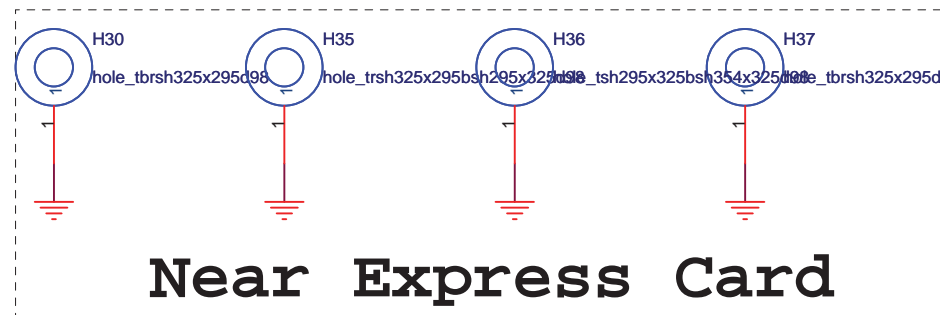
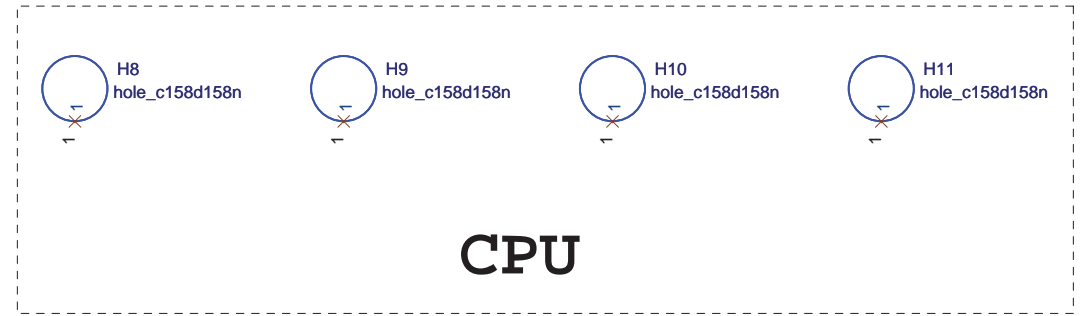
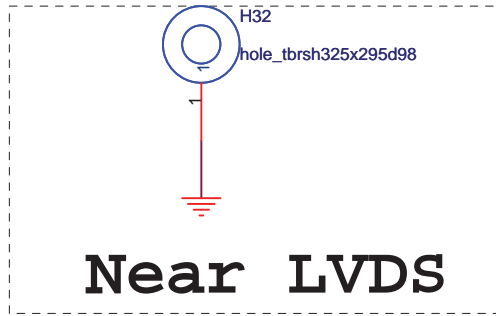
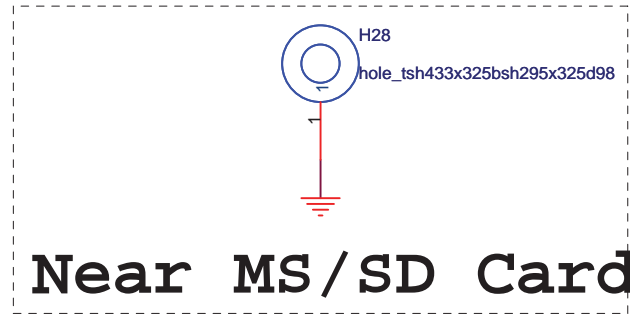
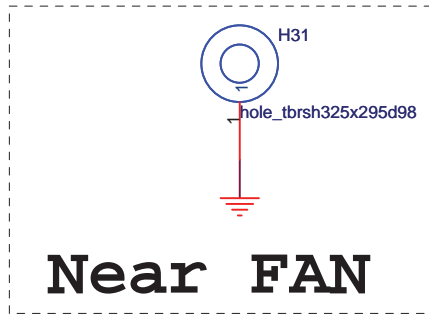
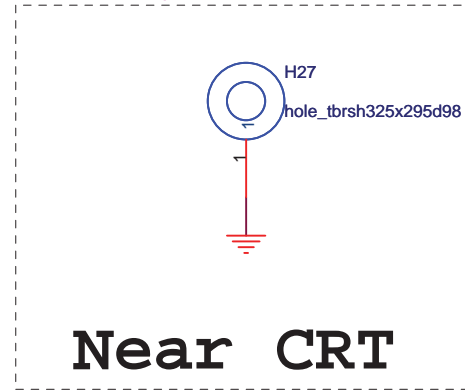
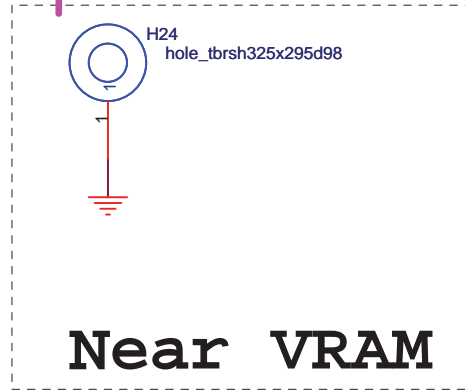
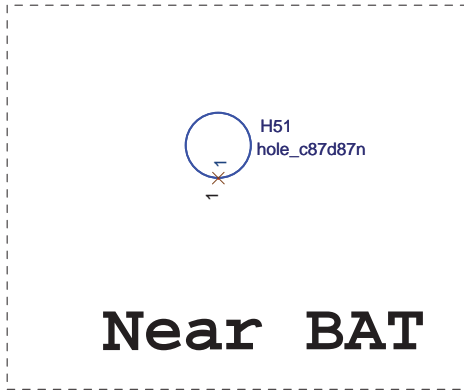


ASSIST button

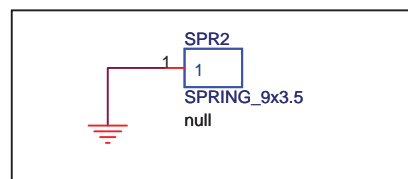
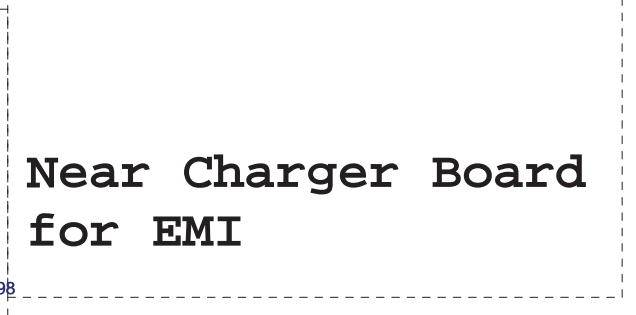
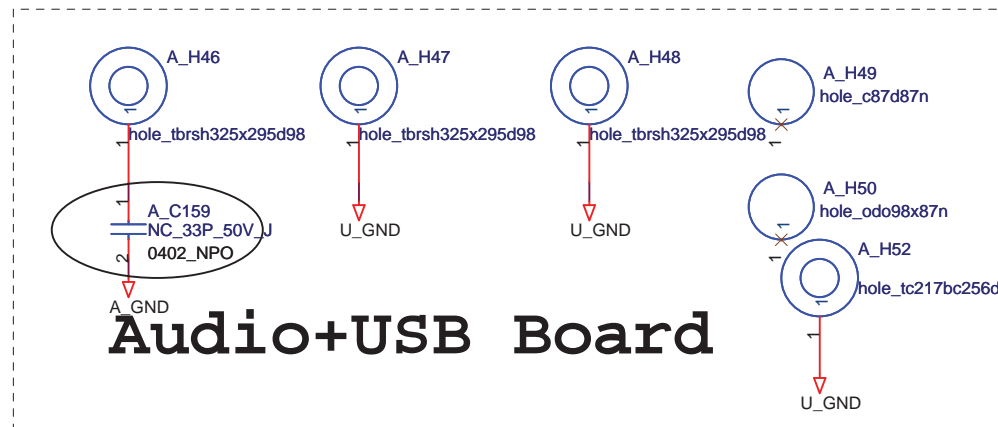
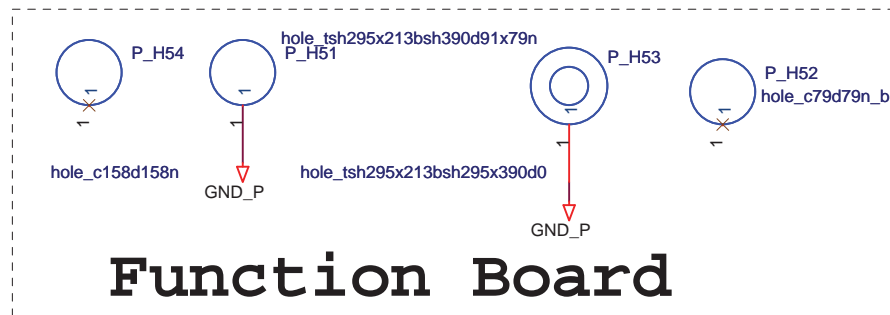
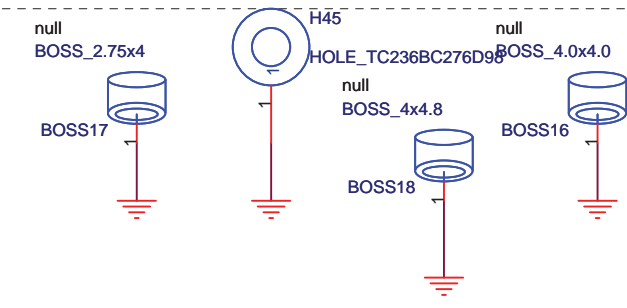
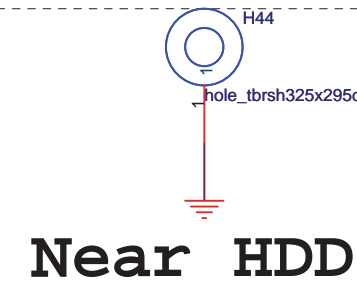
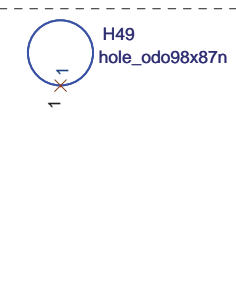


VAIO button





Del H42/H43, combine with CN25



2009.10.20
change SPR2 to 9 X3.5

2009/0910

1. Add S/D CARD test point for L6 TE request TP736

2. Add MS CARD test point for L6 TE request TP690, TP691, TP693, TP694, TP695, TP696, TP697 TP702, TP724, TP698, TP699, TP700, TP701, TP703

delete

3. Add I_LINK test point for L6 TE request TP512, TP513, TP514,TP515

4. Add TOUCHPAD test point for L6 TE request TP551, TP550, TP535, TP534 ,TP562, TP564

5.Delete R5893, R5887 and trace AC PRESENT, add R6007 to +3VALW in page 11, delete trace AC PRESENT, add test point TP186 in page 37. VespaCP use Ignition FW, no ACPRESENT function. Intel FAE suggest this pin can configure as GPIO.

6.change C6131 from NC_470P_16V_K to 0.047U_16V_K follow Intel suggest

7. Change trace (CLK-PCIE-EXPRESS#,CLK-PCIE-EXPRESS,EXPRESS-CLKREQ#) from U134(AH42,AH41,A8) to (AJ50,AJ52,H6) for DVT1 express card can't detect issue.

8. Change page 70 from finger print to reserve, VespaCP no this function.

2009/0912

9. Delete R5785 0ohm resistor for voltage drop problem

10. Change RP82 from NC to mount for SI test Change RP81 from mount to NC for SI test Change RP86 from NC to mount for SI test

2009/0914

11.delete finger print

12.delete TP417,link to gnd

13.CN16 PIN 15 LINK TO GND
14.CN35: change 0ohm to 33ohm

15.PCH: GNT0# and GNT1# change from pull high to +3vsus to pull low to gnd

16.DC_IN: DELETE C_PQ9 ,C_PR34 change C_PR36,C_PR37 from NC to mount C_PFI change to 0437007.WR

17.+1.05V: change PC319 from Y5V to X5R

18. VHCORE: change OVT_EC# to PROCHOT#

20.other: add PD31 change PR275 from 10K to 4.7K

21.OVP: DELETE PR78 ,PQ17 change PC35, PU2, PC37, PR240, PR108,PR39, PR36 from mount to NC

22.N11P-LP1+SANSUNG(H2) SKU and N11M-GE1 +SANSUANG(M2 SKU)need change BOM R5244 change from 1R-0004532-F200(45.3K) to 1R-0002492-F200(24.9K) for NVIDIA FAE suggest

2009.0918

23. CN11, CN18, CN34, CN9, CN12, A_CN7, A_CN5 change to Halogen Free

2009/09/19

1.Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4 Change A_USB_VCC2 to A_USB_VCC4 in page 67

2. Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4 Change A_USB_VCC2 to A_USB_VCC4 Change U_VD2+_F/U_VD2-_F to U_VD4+_F/U_VD4-_F in page 69

3.Change USB_VCC2 to USB_VCC4 Change USB_OC#0 to USB_OC#1 in page 48

4.Add USB_OC#1 Change USB_PN10/USB_PP10 to test point in page 13

5.Change USB_VCC2 to USB_VCC4 in page 43

2009.0921

Page 50
1.R531 Delete,then pull CN34 pin4 to GND.
2.Remove the Test point TP562 to +5VRUN.

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2009.0922

1.change R277,R273 from NC to mount
2.add R5313 for 10K_J
3.change R5916 TO NC
4.change D15,D21,A_D7 TO mount and place them near connector
5.WIRELESS_DATA/WIRELESS_CHCLK change please refer to page 49
6.ADD R5991 for 100K_J
7.change C476 TO NC_12P
8.change C1986 TO 12P
9.ADD R6010,R6011,R6012 to pull-down SPI0_CLK,SPI0_MOSI,SPI0_CS# in page 09
10.change CN25,CN29,CN30 TO Halogen Free
11.change D13,D11 TO 16-SSM22LL_PT00
12.change R5910,R5911 to NC_1K
13.DELETE TP498,TP491,TP490,TP495,TP494,TP509
14.CHANGE Q45 TO NC ,R5996 TO MOUNT
15.change CN21 TO 1N-1052000-0000 for ME request
16.change BOSS1,BOSS2 to 1M-1F40M20-1500 for ME request
17.page 57:change net PWRCNTL_0_R to PWRCNTL_1_R change net PWRCNTL_1_R to PWRCNTL_0_R change PR389,PR380 TO 110 ohm change PC334 to 220P_16V_J 0402 change PC337 to 220P_50V_J 0402 delete PJ23,PJ24,PJ25,PJ26

18.page 53:delete PJ18,PJ19
19.page 56:delete PJ1,PJ2
20.page 58:delete PJ20,PJ21,PJ22 ADD PR367/0 ohm
21.page 59:delete PJ5
22.page 60:delete PJ3
23.page 06:delete PJ43

2009.0923
ADD test point TP490,TP491,TP494,TP495,TP498,TP509

2009.0925
ADD C6260 NC_1000P_16V_K

2009.0925
For EMI request
1.Add Cap.C36 0.1U,C999 1000PF on net +1_05V_VTT
2.Add Cap.C37,C38 0.1U on net +1_8VRUN
3.Add Cap. C39 0.1U,C1000 1000PF on net +3VRUN
4.Add Cap.C53,C54,C61 0.1U on net DCBATOUT
5.Add SPR2

2009.0925
ADD C70,C71,C72 10P for RF request

2009.0925
change C6156,C6157 from 12p to 15p for vendor request

2009.0925
change PR245,PC269,PR236,PC266,PR363,PC323,PR251, PC252,PR233,PC232 from NC to mount for EMI request

2009.0926
For EMI request
1.Add PC62 0.1U on net +1_8V_LX ,place it near PQ72
2.change C539 from NC to 680P
3.Add C549 680P on net INV_BRADJ,place it near LVDS connector

2009.0928
For RF request
change C1264,C716,C532 to 47P

2009.0928
change R5376 to 100K follow design guide

2009.0928
change PC337 to 22P

2009.0928
Add Q7 for MOR request

2009.0929
Add PC206 NC_0.1U reserve for Return patch

2009.0929
change RP86 ,RP82 TO NC
change RP81 TO mount

2009.10.19
1.Change PC319 from 1C-2B20104-K301 To 1C-2B20104-K300.
2.change R5703 from 68ohm to 75 ohm
3 NC RP81 for 1R-1010000-JP00
4. MOUNT RP82, RP86 for 1R-1010000-JP00
5. change C5250 from 1C-2B20473-K300 to 1C-2B20102-K001
6. change C6256 from 1C-2B20102-K001 to 1C-2B20473-K300

2009.10.20
change SPR2 from 4x3 to 7x2.5

2009.10.22
PAGE37:delete C468, C513, U25, R76, R55, R41, R73, C60 (NC), TP871, TP872,TP873,TP876,TP878,TP880,TP874.TP875,TP877,TP879,TP881, TP882 for PVT
PAGE53:change PC112 from 68U to 47U for power request

2009.10.23
Page 35 : deleteJ2,J3
Page 38 : delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518
Page 05 : delete R5786
Page 37 : add TP690, TP690
PAGE 45,46:change net SD_WP# to SD_WP
Page 35 : Add test point TP897,TP898,TP899 for PVT

page 35 : add TP900,TP901 for +3VRUN

2009.10.28
page 57: Change PC344 to 1C-2B70226-M100.
Add PC345 1C-2B70226-M100.
Change PEX_VDD to 2.5A.

2009.10.30
page 55: Change C_PQ3,C_PQ8 to 17-2N7002W-0000.

page 59: Change PQ61 to 17-2N7002W-0000.

page 61: Change PQ58 to 17-2N7002S-PT00.

page 62: Change C_PQ7 to 17-2N7002S-PT00.
Change PQ10 to 17-2N7002W-0000.
Change PQ9 to 17-2N7002S-PT00.

Page 51:change R5992,R5993,R5994 from 120ohm to 549ohm follow M870

Page 36:change Q9 to 17-2N7002S-PT00.
Page 03:change Q179 to 17-2N7002S-PT00

Page 72 :change SPR2 to 9 X3.5

2009.10.31

page 57: Add PC350 1C-33U0337-KX00 NC_330U_2.5V_K.

Page 14 : add RP83 NC_0 to escape crosstalk

2009.11.3

Page60 : Change PC225 TO mount
page 60: Delete PC62.

page 60: Change PR229 to 1K_J.
Change PC225 to 0.22U_25V_K.

2009.11.03
Page 35:add C60,C62,C63,C64

For EMI request
1:Page 55 change C_PC14 to 4700pf
change C_PC13 to 0.1U
2: Page 55 change C_PC156 to 2200pf
3.Page 63 change A_C23,A_C22 from 15PF to 22PF

2009.11.4

Page 35:add C65,C66,C67,C73,C74 for FAN issue

page 55: Change C_EC6066 to 1C-2B30104-K000.

page 56: Add TP442.

page 56: Change E_C6060 to 1C-2B30104-K000.
Change E_C6059 to 1C-2B30104-K000.
Change E_C6067 to 1C-2B30104-K000.
Change E_C6068 to 1C-2B30104-K000.
Change E_C6062 to 1C-2B30104-K000.
Change E_C6061 to 1C-2B30104-K000.

2009.11.16
change C_PC14, C_PC156 to 1000P for EMI request

2009.11.19
Page49: Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

2009.11.19
Page 55: Add C_PQ26,C_PQ27,C_PQ9 NC_TPCC8102 for 2nd source.