

**Schematics Page Index (Title / Revision / Change Date)**

Page	Title of Schematics Page	Rev.	Page	Title of Schematics Page	Rev.
01	Schematics Page Index	1.0	43	Touch Pad Connector	1.0
02	Block Diagram	1.0	44	Audio/USB DB Conn.	1.0
03	ARD&CFD (DMI, PEG, FDI)	1.0	45	FAN	1.0
04	ARD&CFD (CLK, MISC, JTAG)	1.0	46	Thermal Sensor&Protection	1.0
05	ARD&CFD (DDR3)	1.0	47	Power Design Diagram	1.0
06	ARD&CFD (POWER)	1.0	48	DCIN&Charger	1.0
07	ARD&CFD (GRAPHICS POWER)	1.0	49	Discharge Circuit	1.0
08	ARD&CFD (GND)	1.0	50	SYS Power (+3 3V/+5V)	1.0
09	ARD&CFD (RESERVED)	1.0	51	VTT&PCH Power(+1 1/1 05V)	1.0
10	PCH (HDA, JTAG, SAT)	1.0	52	DDR3 Power(+1 5V/+0 75V)	1.0
11	PCH (PCI-E, SMBUS, CLK)	1.0	53	VRAM Power(+1 8V)	1.0
12	PCH (DMI, FDI, GPIO)	1.0	54	CPU Power VHCORE	1.0
13	PCH (LVDS, DDI)	1.0	55	CPU Power VID	1.0
14	PCH (PCI, USB, NVRAM)	1.0	56	VGFX Power GFXCORE	1.0
15	PCH (GPIO, VSS NCTF, RSVD)	1.0	57	VGA Power(NV VDD)	1.0
16	PCH (POWER) 1/2	1.0	58	Others power plane	1.0
17	PCH (POWER) 2/2	1.0	59	OVP protection	1.0
18	PCH (VSS)	1.0	60	INV CONNECTOR	1.0
19	CLOCK GEN	1.0	61	LVDS	1.0
20	DDRIII(SO-DIMM 0) 1/3	1.0	62	HDMI	1.0
21	DDRIII(SO-DIMM 1) 2/3	1.0	63	CRT	1.0
22	SO-DIMM VREF 3/3	1.0	64	Audio (CODEC)	1.0
23	EC+KBC (NPCE783L)	1.0	65	Audio (MUTE)	1.0
24	SPI Flash ROM	1.0	66	Audio (Power)	1.0
25	Debug Port	1.0	67	Audio (Speaker AMP)	1.0
26	Express Card	1.0	68	Audio (Speaker Connector)	1.0
27	Mini-PCIE Card (WLAN)	1.0	69	Mini-PCIE Card (Mach)	1.0
28	TV-Tuner Connector	1.0	70	VGA (PCI-E) 1/9	1.0
29	LAN (88E8057) 1/2	1.0	71	VGA (STRAP) 2/9	1.0
30	LAN (Transformer) 2/2	1.0	72	VGA (DDR) 3/9	1.0
31	SATA HDD	1.0	73	VGA (DDR) 4/9	1.0
32	SATA CD-ROM	1.0	74	VGA (CRT/eDP) 5/9	1.0
33	Braidwood Connector	1.0	75	VGA (LVDS/HDMI) 6/9	1.0
34	PCIE (MS&iLINK) 1/2	1.0	76	VGA (GPIO) 7/9	1.0
35	PCIE (SD) 2/2	1.0	77	VGA (XTAL) 8/9	1.0
36	Camera Connector	1.0	78	VGA (POWER/GND) 9/9	1.0
37	Felica Connector	1.0	79	VRAM (DDR3) 1/4	1.0
38	eDP&LVDS Connector	1.0	80	VRAM (DDR3) 2/4	1.0
39	Bluetooth Connector	1.0	81	VRAM (DDR3) 3/4	1.0
40	Modem Connector	1.0	82	VRAM (DDR3) 4/4	1.0
41	KB Connector	1.0	83	VRAM (BYPASS) 1/2	1.0
42	Status LED	1.0	84	VRAM (BYPASS) 2/2	1.0

**M931 BOM Control Table**

VALUE Head	CFD+PM55 N11P 1GVRAM-H	CFD+PM55 N11P 1GVRAM-S	CFD+PM55 N11M 512MVRAM-H	CFD+PM55 N11M 512MVRAM-S	ARD+PM55 N11P 1GVRAM-H	ARD+PM55 N11P 1GVRAM-S	ARD+PM55 N11M 512MVRAM-H	ARD+PM55 N11M 512MVRAM-S
NV_	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff
NP_	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy
NM_	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff
NVH_	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy
NVS_	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff
NC_	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy

**TJ\_ for T-JET SKU (CTO)**

85	LID Switch/eSATA COMBO	1.0
86	Identify IC	1.0
87	HOLE & AMI LABEL	1.0
88	USB & AUDIO Conn.	1.0
89	USB Port	1.0
90	HP Jack (S/PDIF)	1.0
91	Ext MIC Jack	1.0
92	Function SW & ALS	1.0

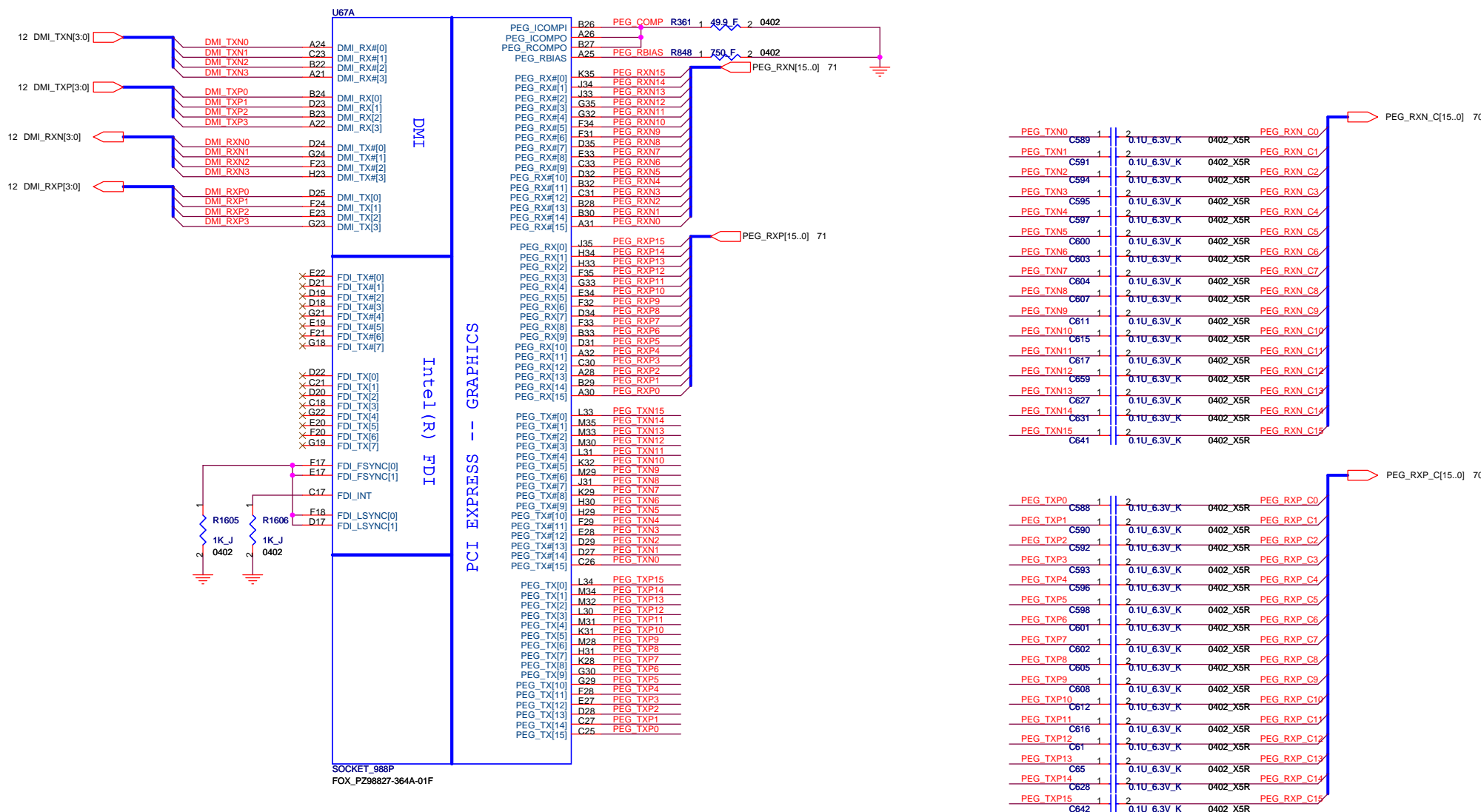
P. Leader	Check by	Design by

**Project Code & Schematics Subject:** M931 Main Board

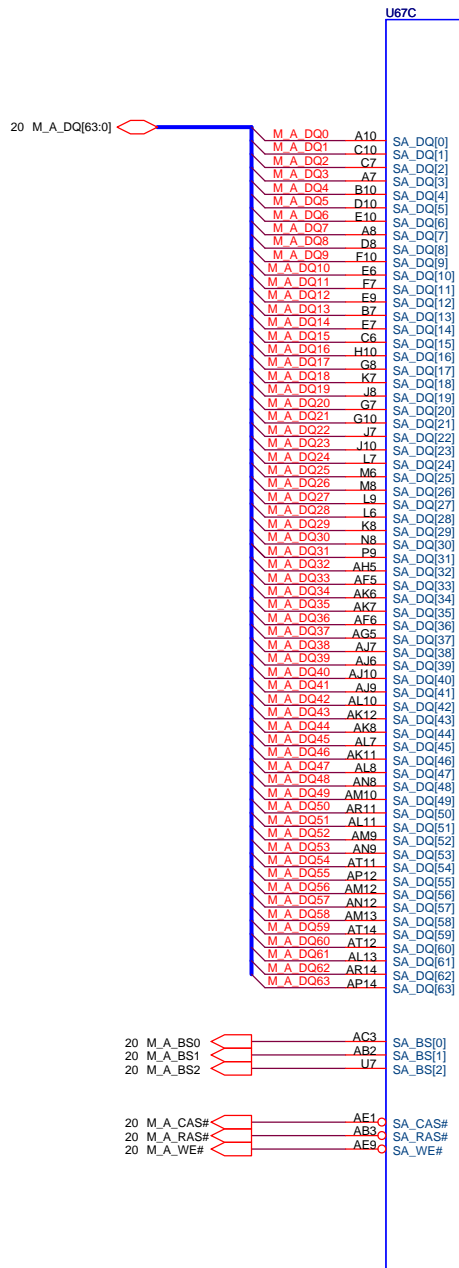
**PCB P/N:** (IRIS)  
(Hannstar)

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>Index Page</b>		
Size	Document Number		
Custom	<b>M931 (MBX-215)</b>		Rev <b>SA</b>
Date	Wednesday, January 06, 2010	Sheet 1	of 93

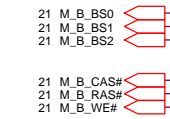
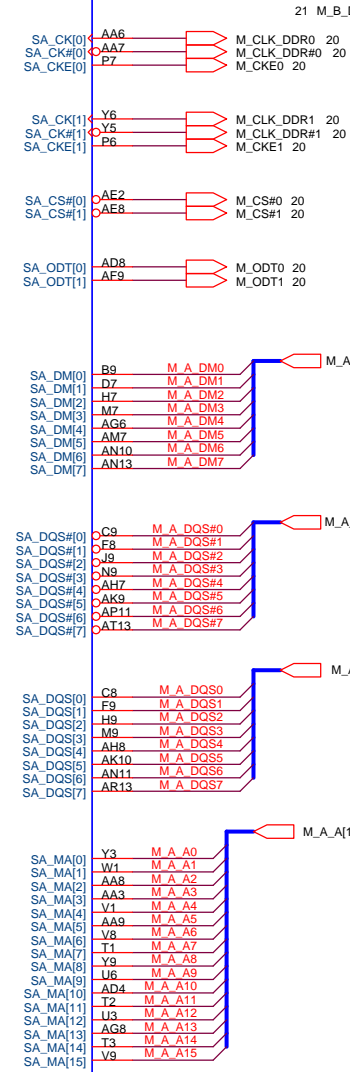




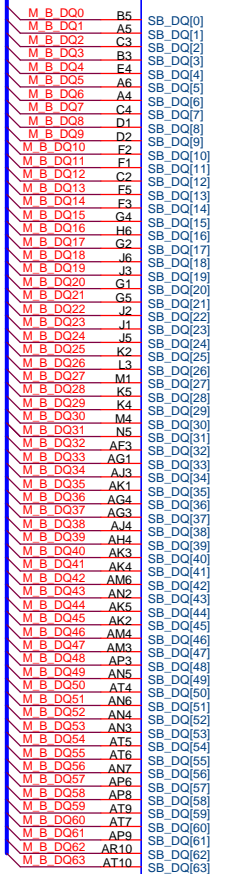




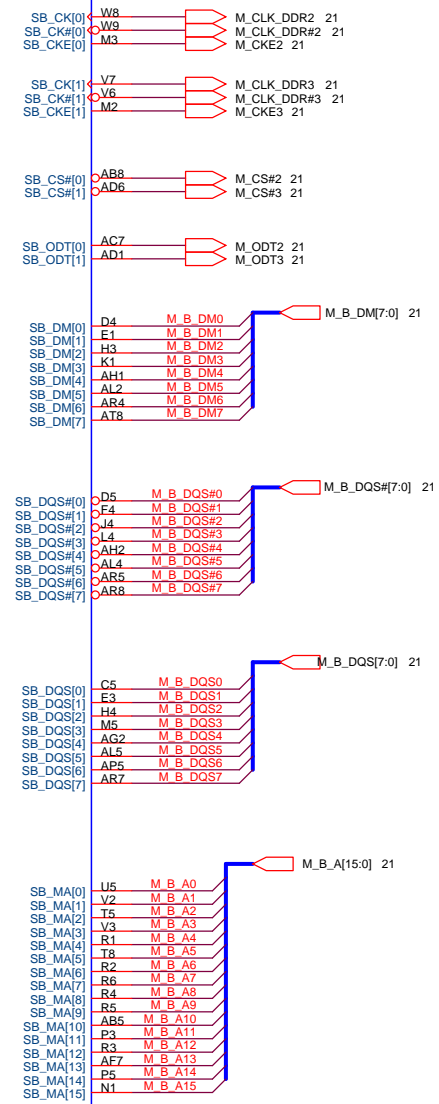
DDR SYSTEM MEMORY A



U67D



DDR SYSTEM MEMORY - B



**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **ARD&CFD (DDR3)**

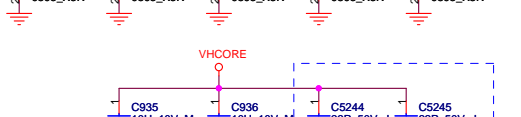
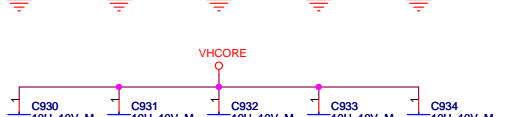
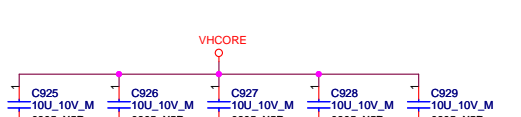
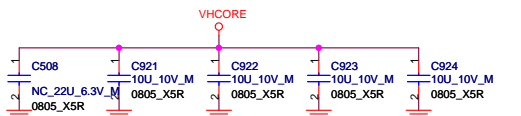
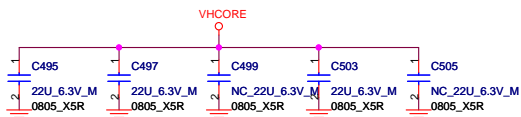
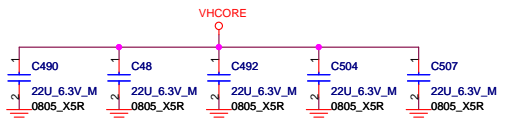
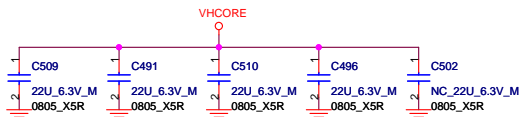
Size: A3  
Document Number: **M931 (MBX-215)**

Date: Wednesday, January 06, 2010

Rev: **SA**

Sheet 5 of 93

52A (CFD SV)



For RF Noise

VHCORE

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

SOCKET\_988P  
FOX\_P298827-364A-01F

1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

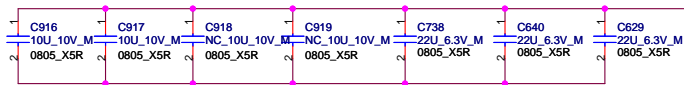
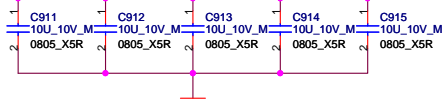
SENSE LINES

- VTT0\_1 AH14
- VTT0\_2 AH12
- VTT0\_3 AH11
- VTT0\_4 AH10
- VTT0\_5 J14
- VTT0\_6 J13
- VTT0\_7 H14
- VTT0\_8 H12
- VTT0\_9 G14
- VTT0\_10 G13
- VTT0\_11 G12
- VTT0\_12 G11
- VTT0\_13 F14
- VTT0\_14 F13
- VTT0\_15 F12
- VTT0\_16 F11
- VTT0\_17 E14
- VTT0\_18 E12
- VTT0\_19 D14
- VTT0\_20 D13
- VTT0\_21 D12
- VTT0\_22 D11
- VTT0\_23 C14
- VTT0\_24 C13
- VTT0\_25 C12
- VTT0\_26 B14
- VTT0\_27 B13
- VTT0\_28 B12
- VTT0\_29 A14
- VTT0\_30 A13
- VTT0\_31 A12
- VTT0\_32 A11

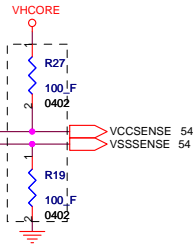
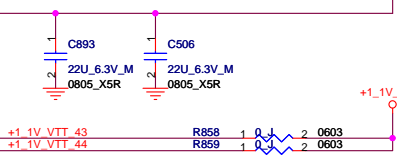
- PSI# AN33 PSI# 54,55
- VID[0] AK35 VID0 54,55
- VID[1] AK33 VID1 54,55
- VID[2] AK34 VID2 54,55
- VID[3] AL35 VID3 54,55
- VID[4] AL33 VID4 54,55
- VID[5] AM33 VID5 54,55
- VID[6] AM35 VID6 54,55
- PROC\_DPRSPLVPR AM34 PM\_DPRSPLVPR 54,55
- VTT\_SELECT G15 H\_VTTVID1 51

- ISENSE AN35 IMVP\_IMON 54
- VCC\_SENSE VCCSENSE AJ34 VCCSENSE
- VSS\_SENSE VSSSENSE AJ35 VSSSENSE
- VTT\_SENSE VTT\_SENSE B15 VTT\_SENSE 51
- VSS\_SENSE\_VTT VSS\_SENSE\_VTT A15 TP178 20MIL

18A(CFD SV) (VTT)

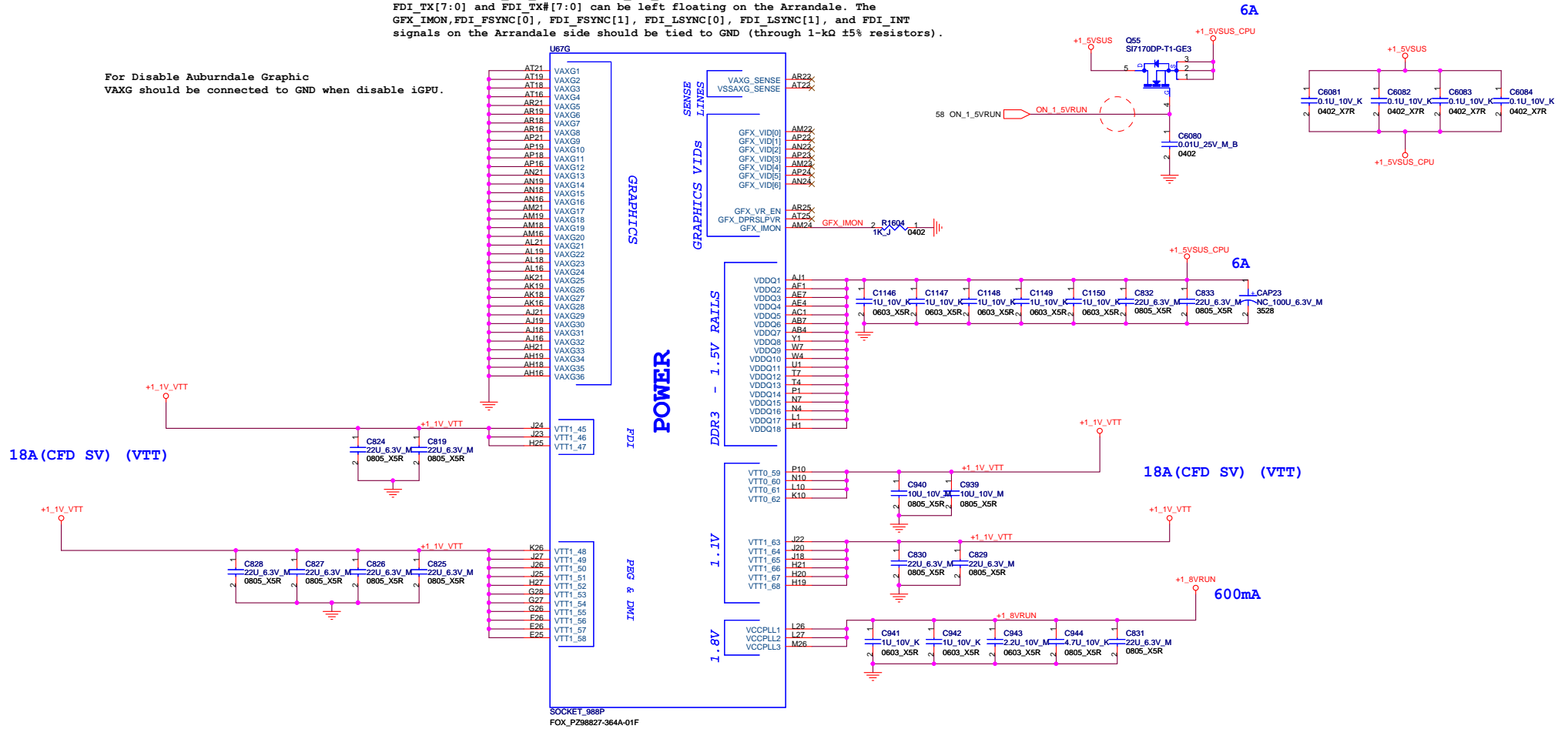


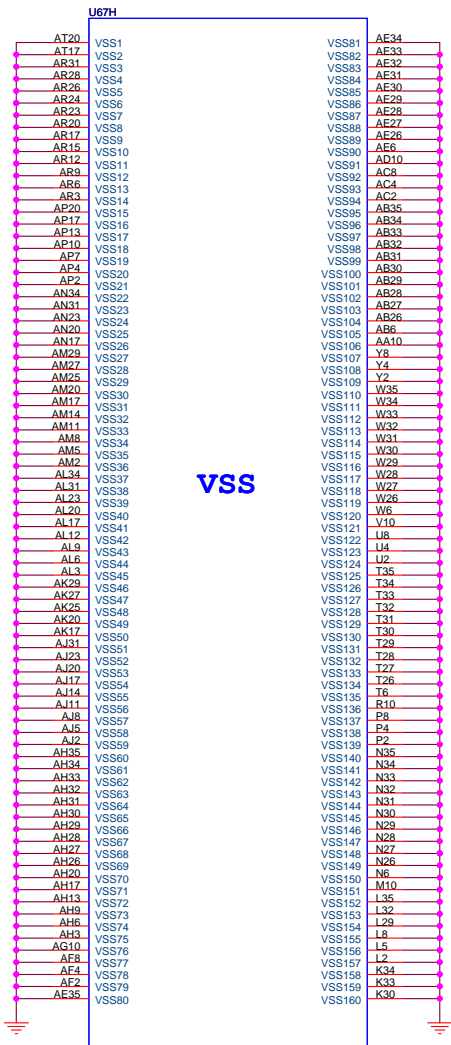
18A(CFD SV) (VTT)



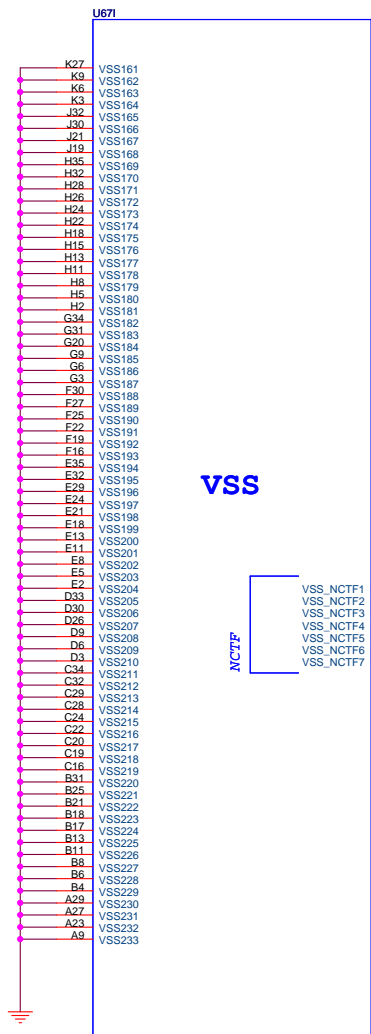
For Disable Auburndale Graphic  
 VAXG\_SENSE and VSSAXG\_SENSE on Arrandale can be left as no connect.  
 For Disable Auburndale Graphic  
 FDI\_RXN [7:0] and FDI\_RXP [7:0] can be left floating on the PCH.  
 FDI\_TX[7:0] and FDI\_TX#[7:0] can be left floating on the Arrandale. The  
 GFX\_IMON, FDI\_FSYNC[0], FDI\_FSYNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1], and FDI\_INT  
 signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

For Disable Auburndale Graphic  
 VAXG should be connected to GND when disable iGPU.

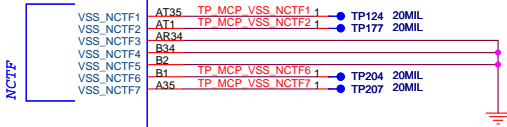




SOCKET\_988P  
FOX\_PZ98827-364A-01F

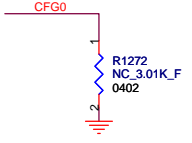


SOCKET\_988P  
FOX\_PZ98827-364A-01F

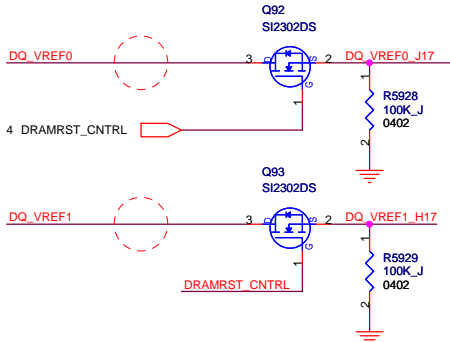
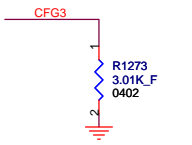




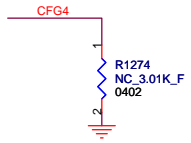
PCI Express Configuration Select  
 CFG0 1 : Single PEG  
 0 : Bifurcation enable



CFG3 PCI Express Static Lane Reversal  
 CFG3 1 : Normal Operation  
 0 : Lane Numbers Reversed  
 15 -> 0 , 14 -> 1 , ...

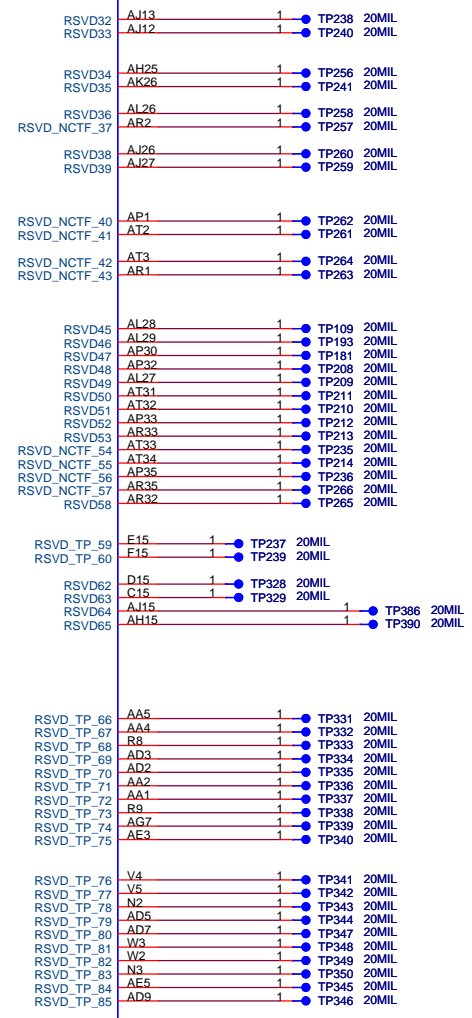
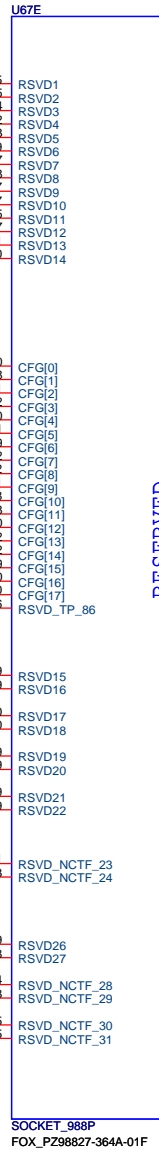
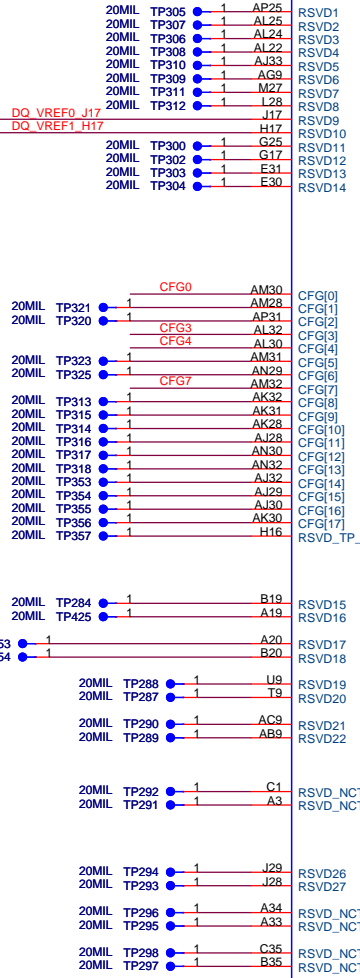
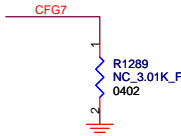


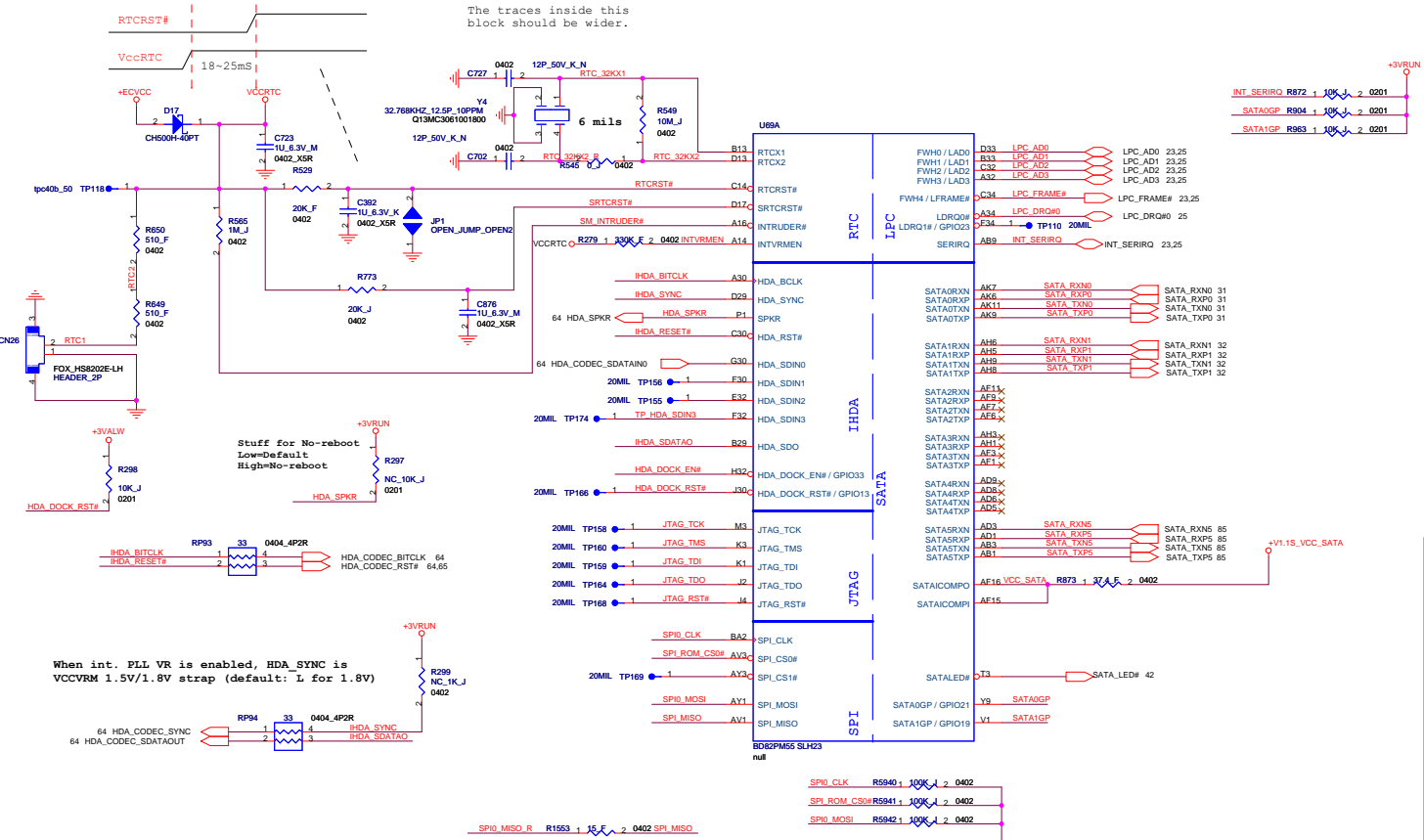
CFG4 Display Port Presence  
 CFG4 1 : Disabled ; No Physical Display Port  
 attached to Embedded Display Port  
 0 : Enable ; An external Display Port device  
 is connected to the Embedded Display Port



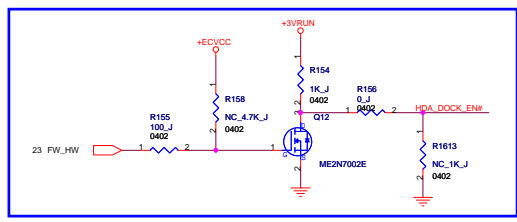
2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.

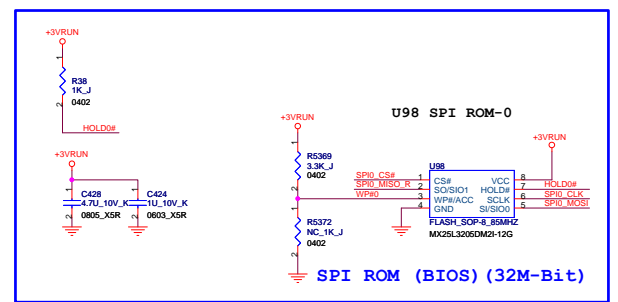
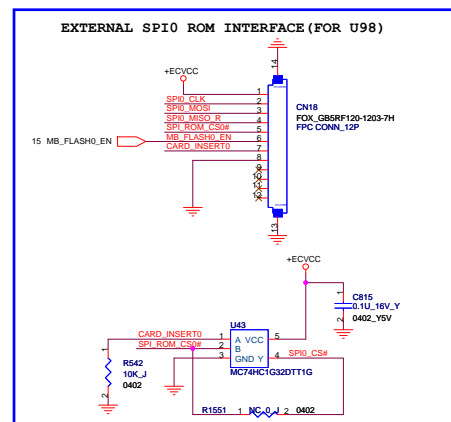




[HDA\_DOCK\_EN#/GPIO33]  
 Low (0) - Flash Descriptor Security will be overridden. Also, when this signal is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.  
 High (1) - Security measure defined in the Flash Descriptor will be enabled



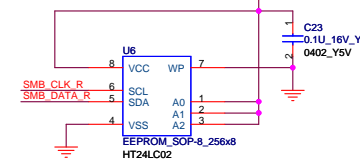
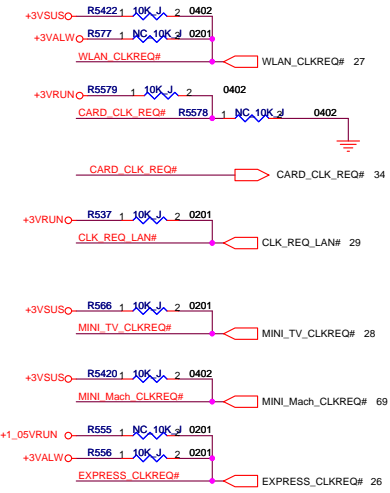
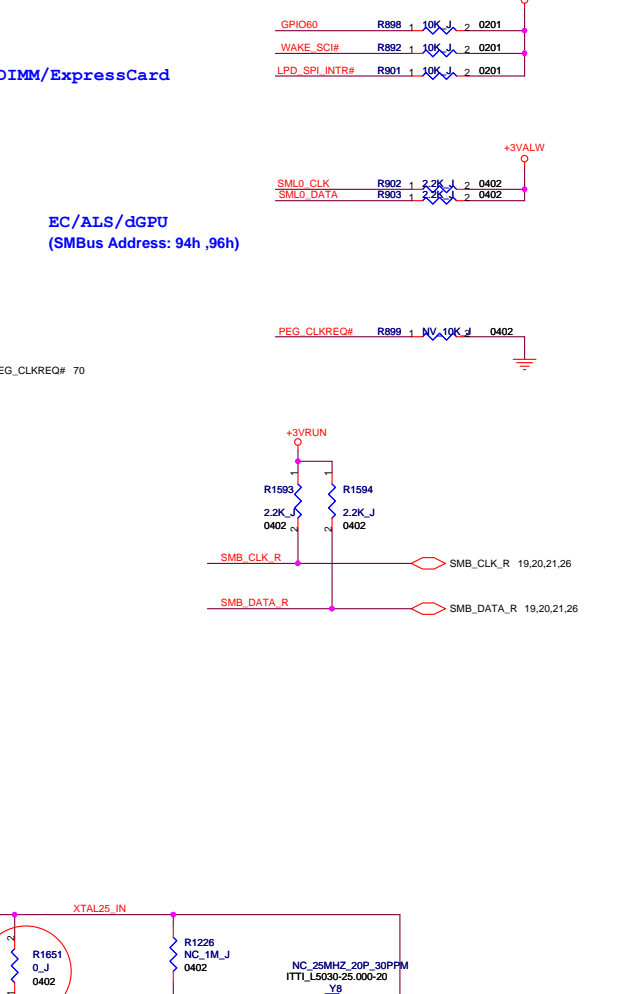
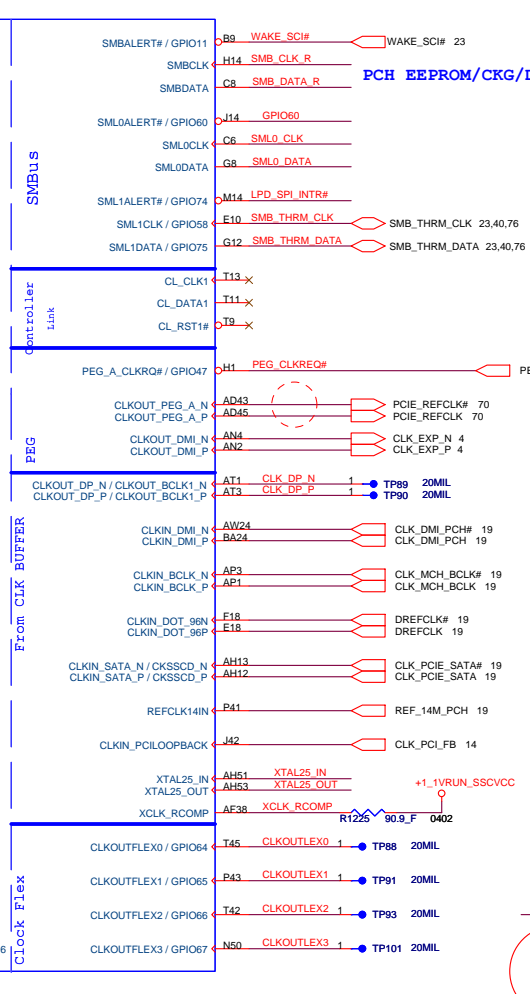
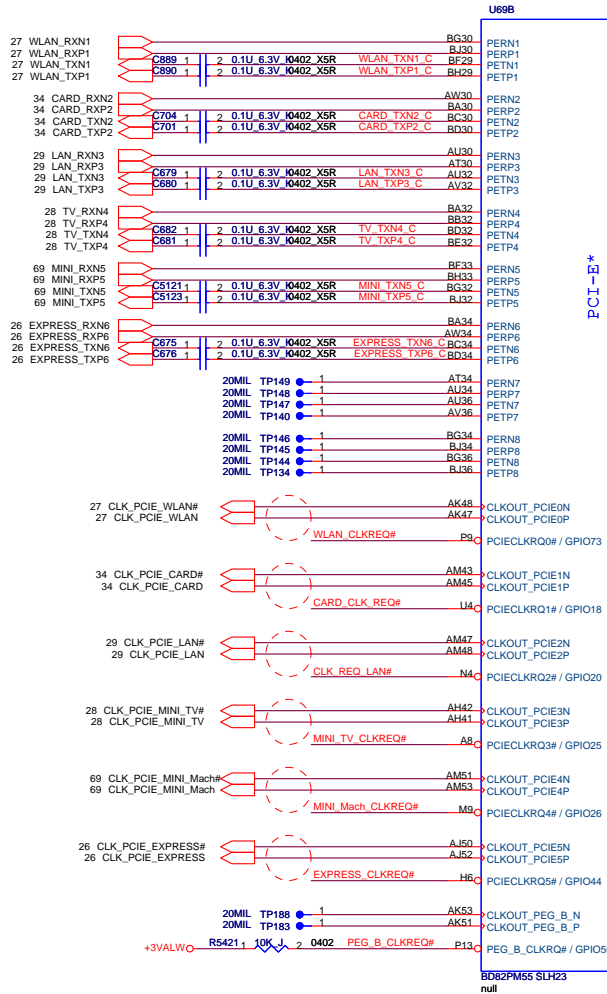
For MP, Dummy CN18, C815, U43, R542, Stuff R1551



When int. PLL VR is enabled, HDA\_SYNC is VCCVRM 1.5V/1.8V strap (default: L for 1.8V)

PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	ISDB-T Tuner (JP)
Port5	Mach
Port6	ExpressCard/34 (PCI-E)
Port7	NC
Port8	NC



Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044).  
XTAL\_IN should be pulled to GND via a 0ohm by default.  
This pull-down resistor on XTAL\_IN should only be un-stuffed when 25MHz crystal is used.

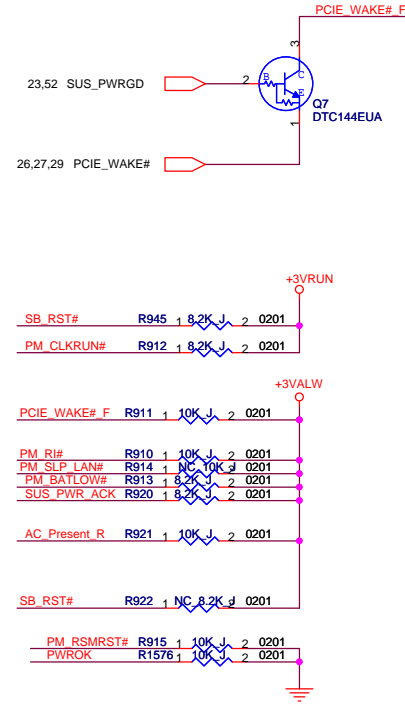
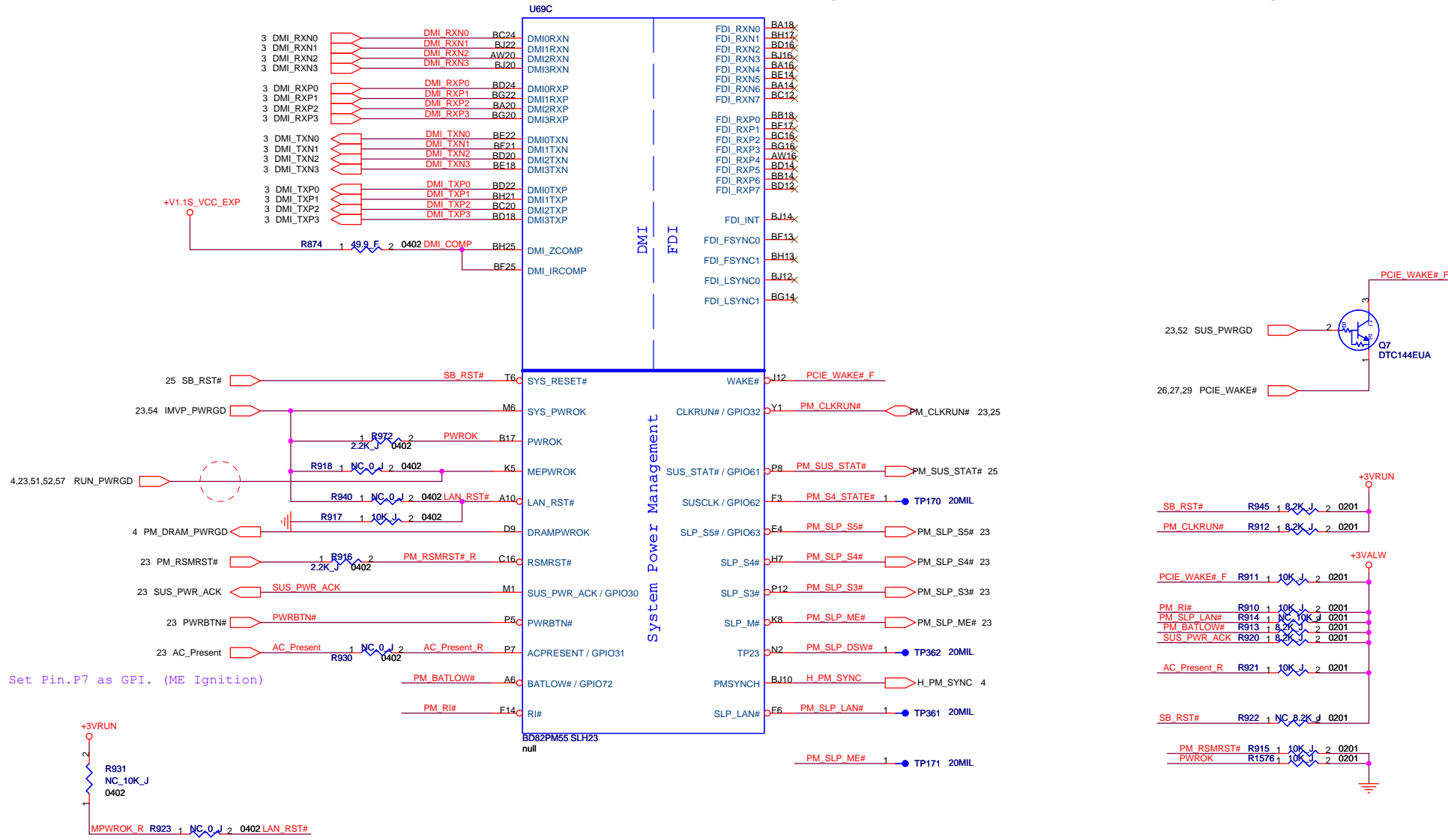
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **PCH (PCI-E, SMBUS, CLK)**

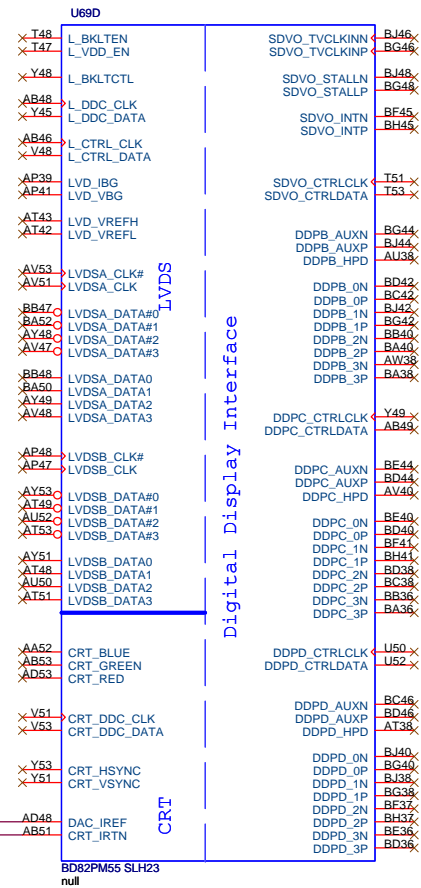
Size: Document Number  
Custom: **M931 (MBX-215)** Rev: **SA**

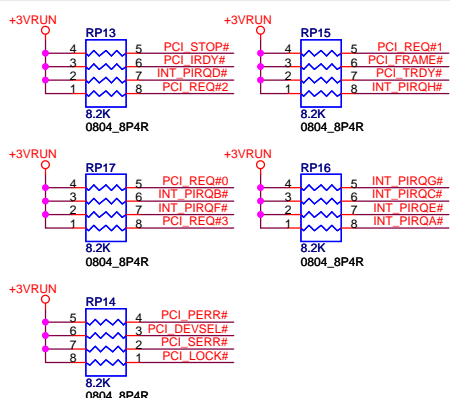
Date: Wednesday, January 06, 2010 | Sheet 11 of 93

For Disable Auburndale Graphic  
 In addition, FDI\_RXN\_[7:0] and FDI\_RXP\_[7:0] can be left floating on the PCH.  
 FDI\_TX\_[7:0] and FDI\_TX#\_[7:0] can be left floating on the Arrandale. The  
 GFX\_IMON, FDI\_FSYNC[0], FDI\_FSYNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1], and FDI\_INT  
 signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



Calpella Platform - Design Guide - Addendum  
 / Update - Rev. 1.52 (Doc #414044) .).





U69E

20MIL	TP182	1	H40	AD0
20MIL	TP167	1	N34	AD1
20MIL	TP186	1	C44	AD2
20MIL	TP194	1	A38	AD3
20MIL	TP187	1	C36	AD4
20MIL	TP199	1	J34	AD5
20MIL	TP201	1	A40	AD6
20MIL	TP200	1	D45	AD7
20MIL	TP202	1	E36	AD8
20MIL	TP319	1	H48	AD9
20MIL	TP247	1	F40	AD10
20MIL	TP322	1	M48	AD12
20MIL	TP363	1	M48	AD13
20MIL	TP324	1	M45	AD14
20MIL	TP426	1	F53	AD14
20MIL	TP428	1	M40	AD15
20MIL	TP427	1	M43	AD16
20MIL	TP429	1	J36	AD17
20MIL	TP431	1	F40	AD18
20MIL	TP430	1	K48	AD19
20MIL	TP432	1	C42	AD20
20MIL	TP434	1	K46	AD21
20MIL	TP433	1	M51	AD22
20MIL	TP435	1	J52	AD23
20MIL	TP437	1	L34	AD24
20MIL	TP436	1	K51	AD25
20MIL	TP438	1	F42	AD26
20MIL	TP440	1	J40	AD27
20MIL	TP439	1	G46	AD28
20MIL	TP441	1	F44	AD29
20MIL	TP443	1	M47	AD30
20MIL	TP442	1	H36	AD31
20MIL	TP446	1	J50	C/BE0#
20MIL	TP445	1	G42	C/BE1#
20MIL	TP447	1	H47	C/BE2#
20MIL	TP444	1	G34	C/BE3#

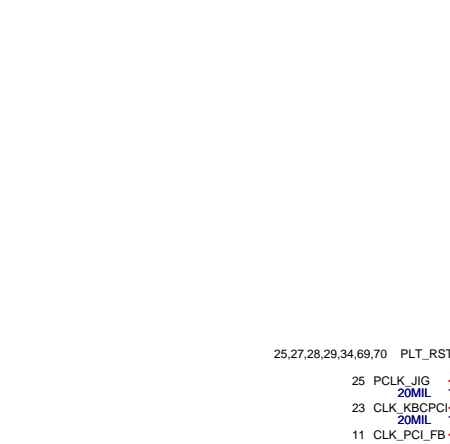
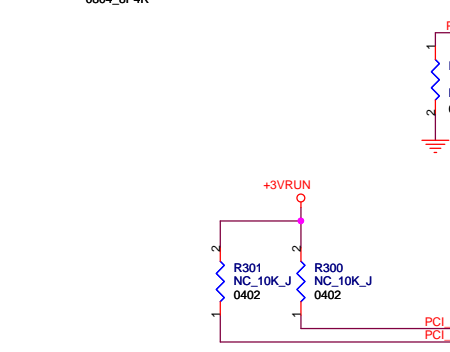
PCI

NVRAM

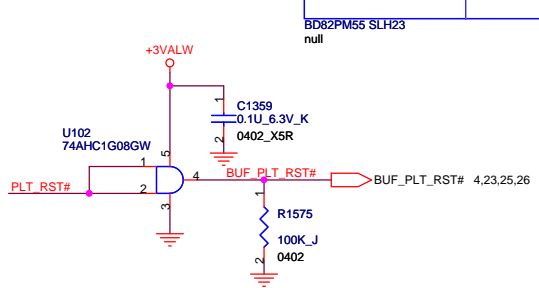
NV_CE#0	AY9
NV_CE#1	BD1
NV_CE#2	AP15
NV_CE#3	BD8
NV_DQS0	AV9
NV_DQS1	BG8
NV_DQ0 / NV_I00	AP7
NV_DQ1 / NV_I01	AP6
NV_DQ2 / NV_I02	AT6
NV_DQ3 / NV_I03	BBI
NV_DQ4 / NV_I04	AV6
NV_DQ5 / NV_I05	AD3
NV_DQ6 / NV_I06	BB3
NV_DQ7 / NV_I07	BA4
NV_DQ8 / NV_I08	BB4
NV_DQ9 / NV_I09	BD5
NV_DQ10 / NV_I010	BB6
NV_DQ11 / NV_I011	BB7
NV_DQ12 / NV_I012	BC8
NV_DQ13 / NV_I013	BJ8
NV_DQ14 / NV_I014	BJ6
NV_DQ15 / NV_I015	BG6
NV_ALE	BD3
NV_CLE	AY6
NV_RCOMP	AU2
NV_RB#	AVZ
NV_WR#0_RE#	AY8
NV_WR#1_RE#	AY5
NV_WE#_CK0	AV11
NV_WE#_CK1	BF5

USB

USBP0N	H18	USB P0	USB P0	85
USBP0P	J18	USB PP0	USB PP0	85
USBP1N	A18	USB PP1	USB PP1	44
USBP1P	C18	USB PP1	USB PP1	44
USBP2N	P20	USB PP2	TP450	20MIL
USBP2P	J20	USB PP2	TP451	20MIL
USBP3N	L20	USB PP3	USB PP3	26
USBP3P	F20	USB PP3	USB PP3	26
USBP4N	G20	USB PP4	USB PP4	44
USBP4P	A20	USB PP4	USB PP4	44
USBP5N	C20	USB PP5	TP326	20MIL
USBP5P	M22	USB PP6	TP358	20MIL
USBP6N	N22	USB PP6	TP299	20MIL
USBP6P	B21	USB PP7	TP301	20MIL
USBP7N	D21	USB PP7	TP352	20MIL
USBP7P	H22	USB PP8	TP359	20MIL
USBP8N	J22	USB PP8	TP360	20MIL
USBP8P	E22	USB PP9	TP449	20MIL
USBP9N	F22	USB PP9	USB PP9	36
USBP10N	A22	USB PP10	USB PP9	36
USBP10P	C22	USB PP10	USB PP10	28
USBP11N	G24	USB PP11	USB PP10	28
USBP11P	L24	USB PP11	USB PP11	37
USBP12N	M24	USB PP12	USB PP11	37
USBP12P	H24	USB PP12	USB PP12	27
USBP13N	A24	USB PP13	USB PP12	27
USBP13P	C24	USB PP13	USB PP13	39
USBRBIAS#	B25	USBRBIAS	R308	
USBRBIAS	D25		22.6_F 0402	
OC0# / GPIO59	N16	USB OC#0	USB OC#0	85
OC1# / GPIO40	H16	USB OC#1	USB OC#1	44
OC2# / GPIO41	E16	USB OC#2	USB OC#2	44
OC3# / GPIO42	L16	USB OC#3	USB OC#2	44
OC4# / GPIO43	E14	USB OC#4		
OC5# / GPIO8	G16	USB OC#5		
OC6# / GPIO10	F12	USB OC#6		
OC7# / GPIO14	I15	USB OC#7		

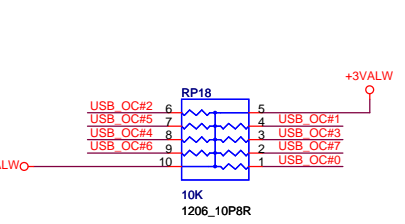


20MIL	TP163	1	F48	GNT0#				
			K45	GNT1# / GPIO51				
			F36	GNT2# / GPIO53				
			H53	GNT3# / GPIO55				
			B41	PIRQ# / GPIO2				
			K53	PIRQF# / GPIO3				
			A36	PIRQG# / GPIO4				
			A48	PIRQH# / GPIO5				
20MIL	TP130	1	K6	PCI_RST#				
			E44	SERR#				
			E50	PERR#				
20MIL	TP127	1	A42	PCI IRDY#				
			H44	PAR				
			F46	DEVSEL#				
			C46	PCI FRAME#				
			D49	PCI LOCK#				
20MIL	TP128	1	D41	PCI_STOP#				
			C48	PCI_TRDY#				
20MIL	TP126	1	M7	PME#_ICH				
			D5	PLTRST#				
25,27,28,29,34,69,70				PLT_RST#				
25	CLK_JIG	20MIL	TP132	1	R44	22_0402	CLK_PCI_JIG	P53
23	CLK_KBCPCI	20MIL	TP132	1	R56	22_0402	CLK_PCI_KBC	P46
11	CLK_PCI_FB	20MIL	TP129	1	R1223	22_0402	CLK_PCI_FB	P48



Buffer to reduce loading on PLT\_RST#.

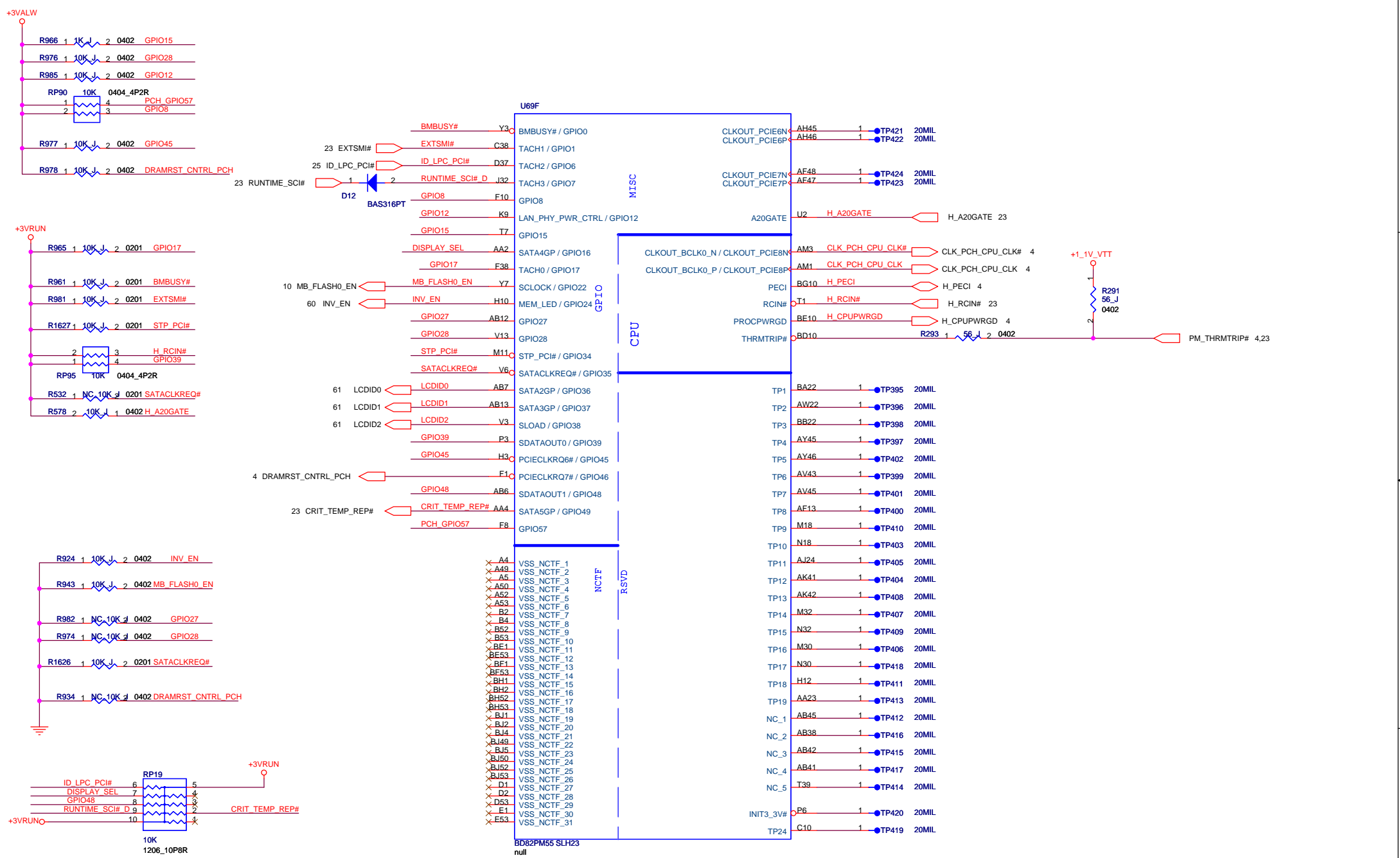
OC0# / GPIO59	N16	USB OC#0	USB OC#0	85
OC1# / GPIO40	H16	USB OC#1	USB OC#1	44
OC2# / GPIO41	E16	USB OC#2	USB OC#2	44
OC3# / GPIO42	L16	USB OC#3	USB OC#2	44
OC4# / GPIO43	E14	USB OC#4		
OC5# / GPIO8	G16	USB OC#5		
OC6# / GPIO10	F12	USB OC#6		
OC7# / GPIO14	I15	USB OC#7		



DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Intel Anti-Theft Technology Disabled when Low , NC R1616 Enabled when High , Stuff R1616

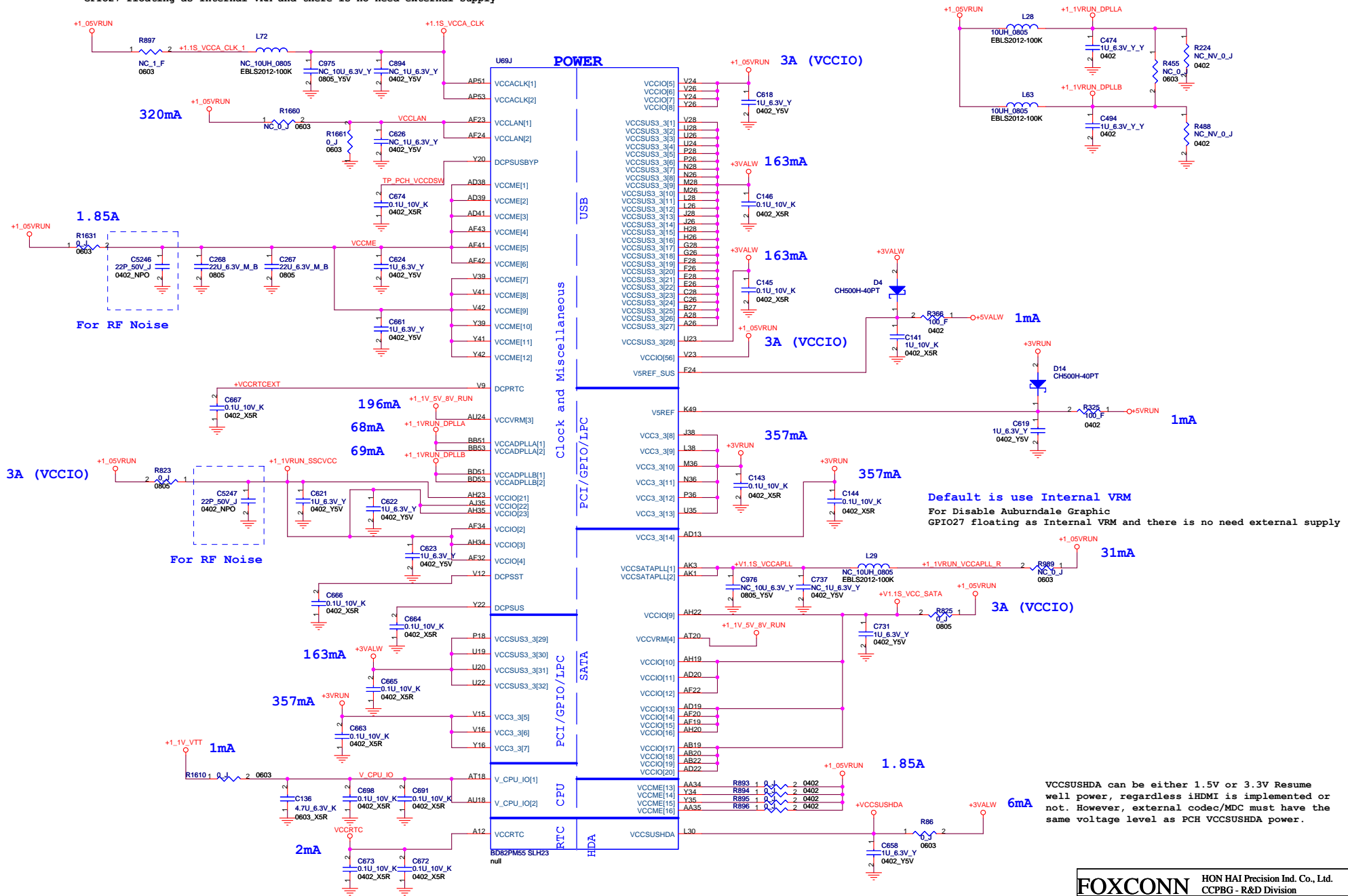
USB PORT	Function
PORT-0	On Board Port
PORT-1	External Port
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	IR Receiver (JP)
PORT-11	Felica
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth



SW1 for BFT JIG Reserved.

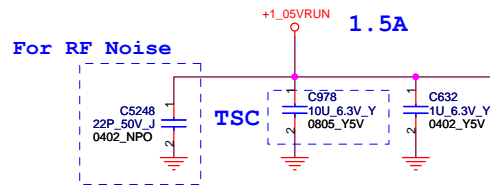
Default is use Internal VRM

For Disable Auburndale Graphic  
GPIO27 floating as Internal VRM and there is no need external supply



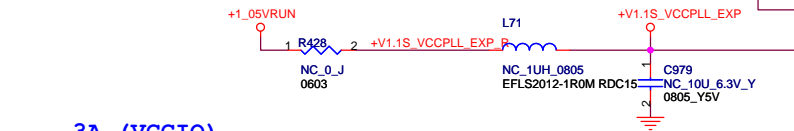
VCCSUSHDA can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.





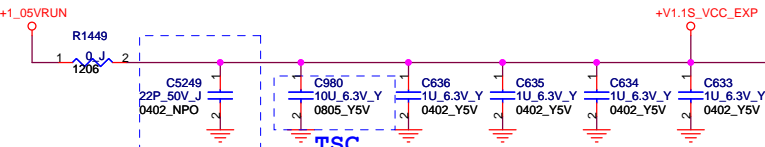
Default is use Internal VRM

For Disable Auburndale Graphic  
GPIO27 floating as Internal VRM and there is no need external supply



3A (VCCIO)

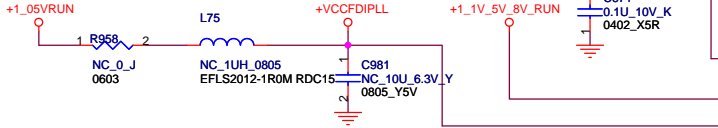
For RF Noise



37mA

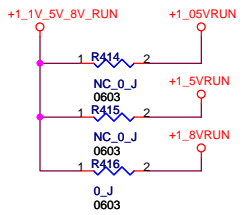
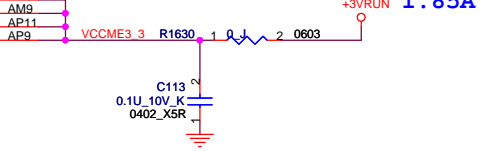
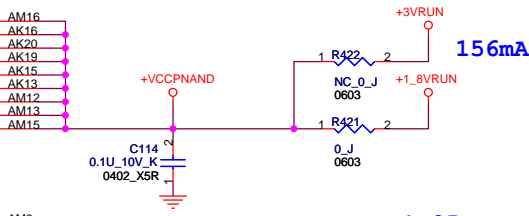
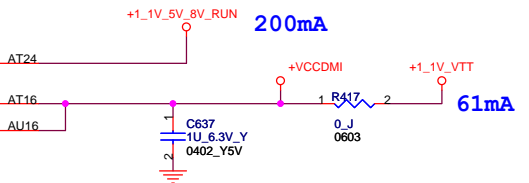
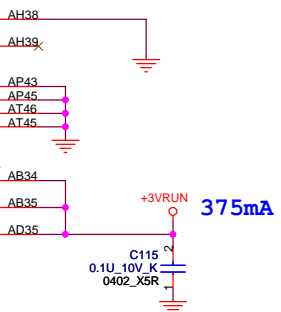
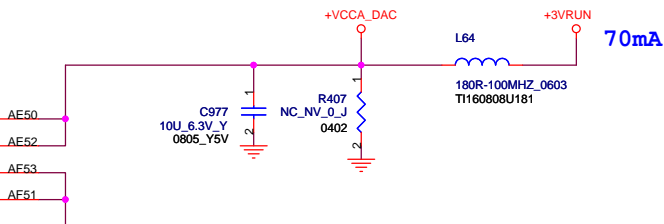
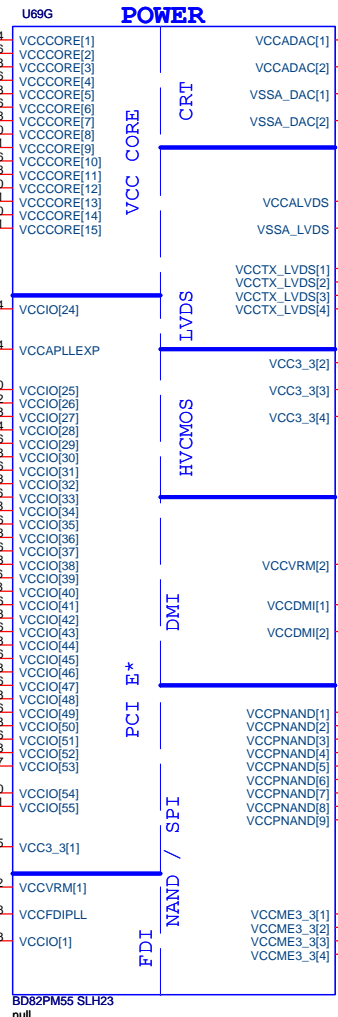
200mA

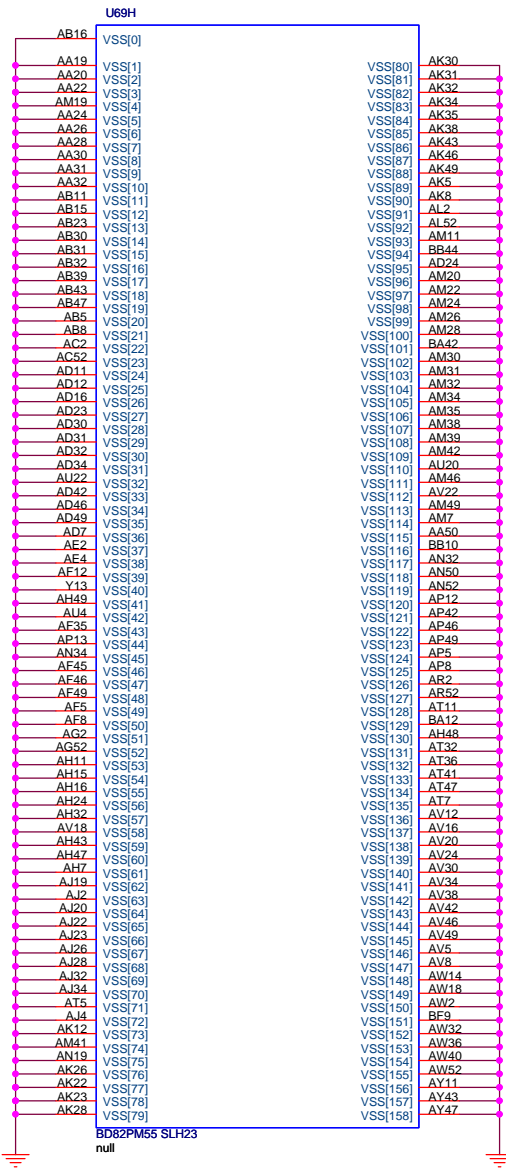
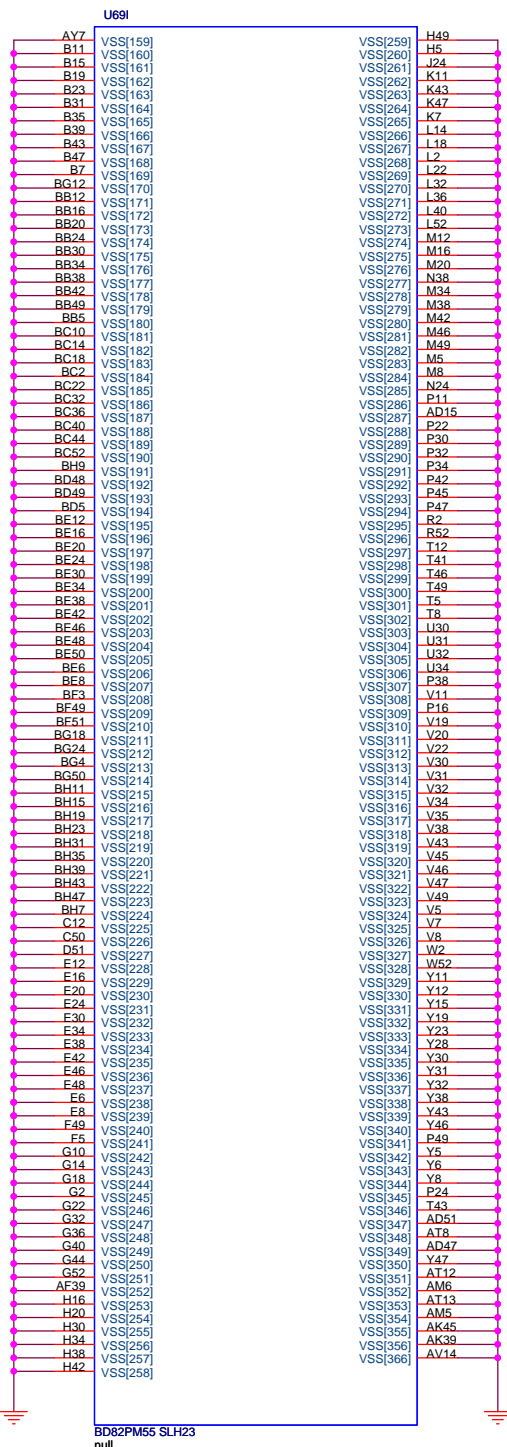
375mA



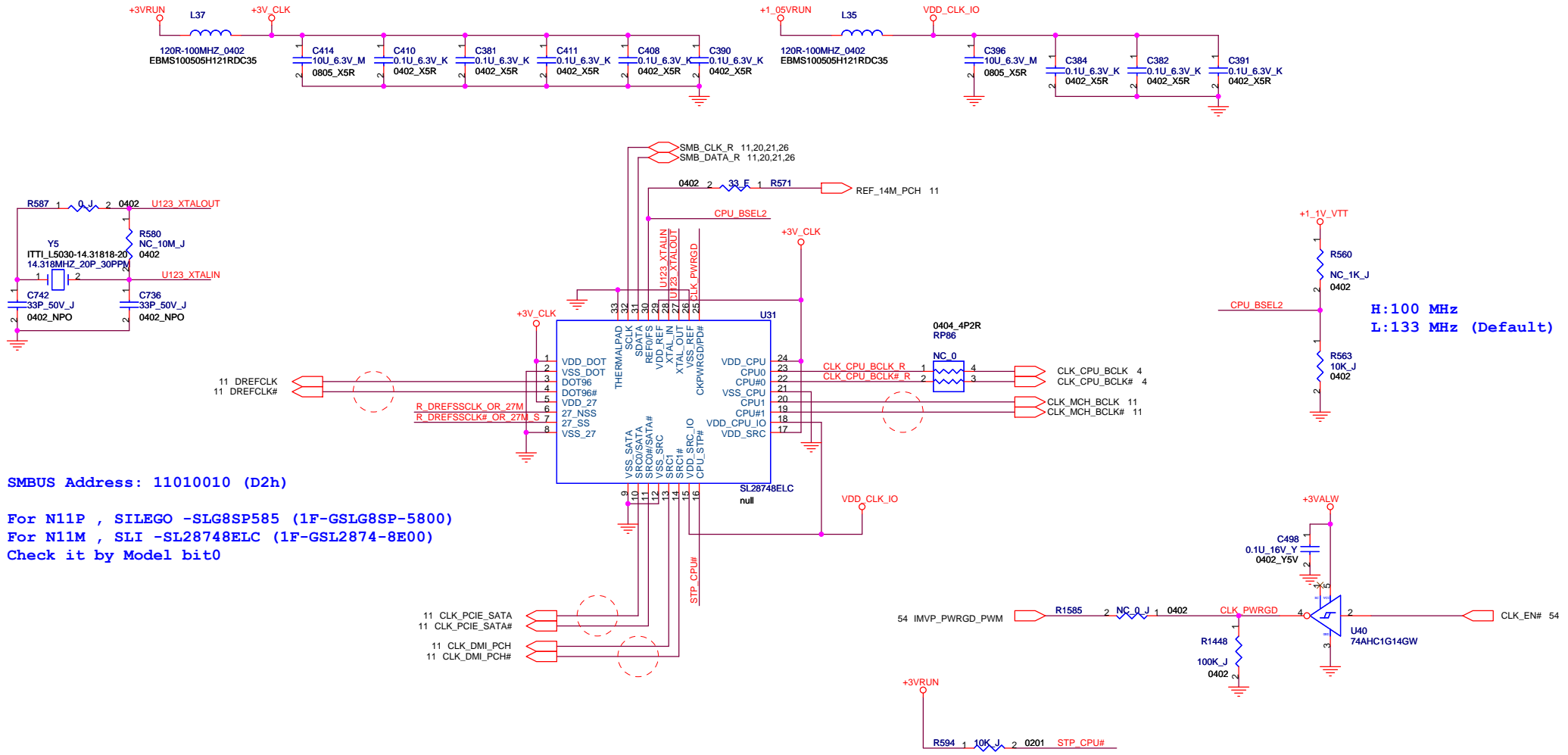
Default is use Internal VRM

For Disable Auburndale Graphic  
GPIO27 floating as Internal VRM and there is no need external supply





<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Title PCH (VSS)</b>			
Size A3	Document Number M931 (MBX-215)	Rev SA	
Date: Wednesday, January 06, 2010	Sheet 18	of 93	



H:100 MHz  
L:133 MHz (Default)





SMBUS Address: 11010010 (D2h)

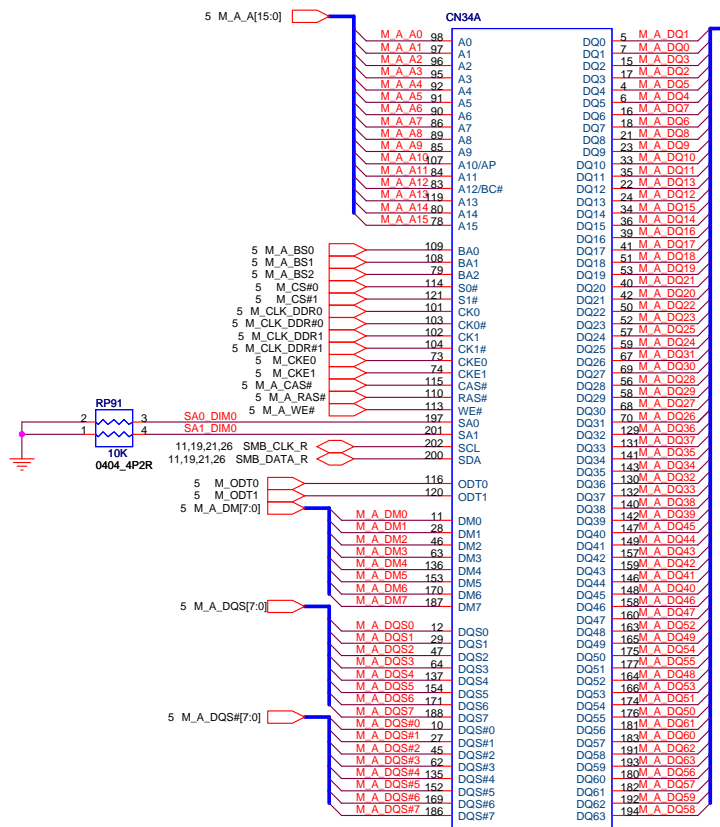
For N11P , SILEGO -SLG8SP585 (1F-GSLG8SP-5800)  
For N11M , SLI -SL28748ELC (1F-GSL2874-8E00)  
Check it by Model bit0

Frequency Select Pin (FS)

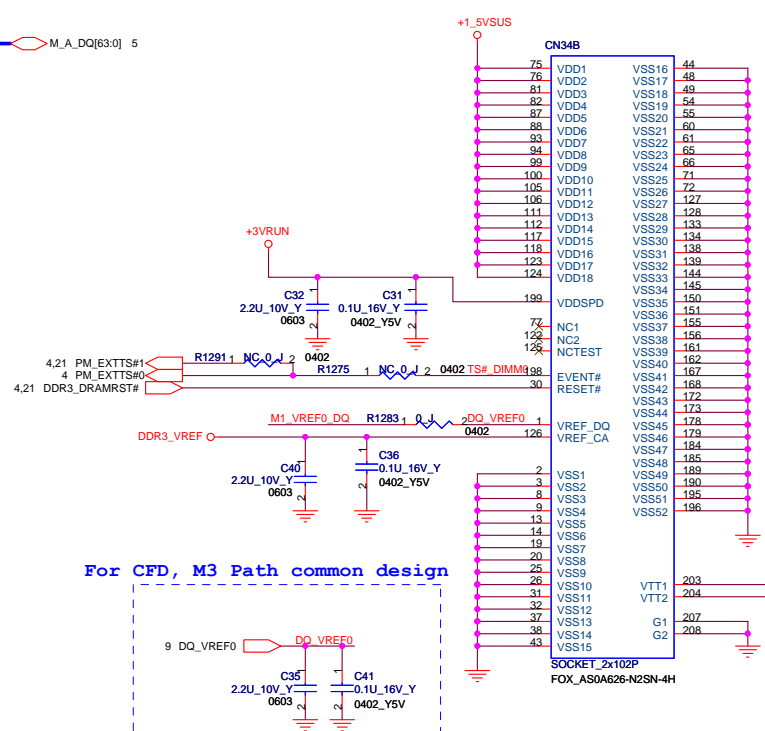
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						



 M\_A\_DM[0..7] 5  
 M\_A\_DQS[7..0] 5  
 M\_A\_DQS#[7..0] 5  
 M\_A\_A[0..14] 5

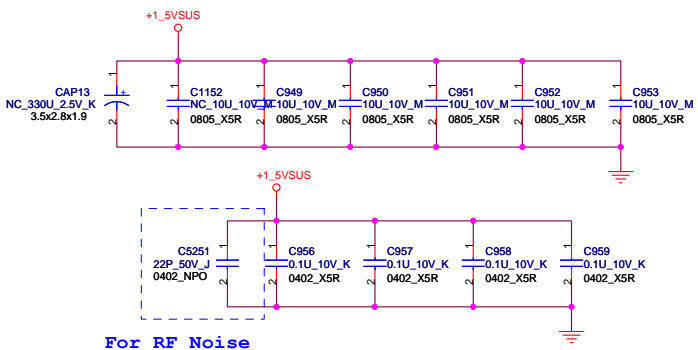
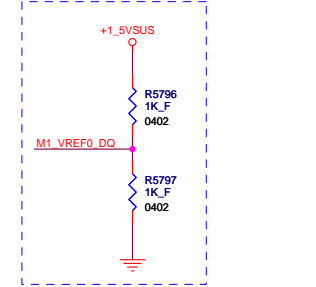


SOCKET\_2x102P  
FOX\_AS0A626-N2SN-4H  
**SBUS Address: A0H(W)/A1H(R)**

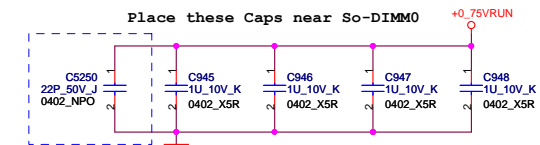


For CFD, M3 Path common design

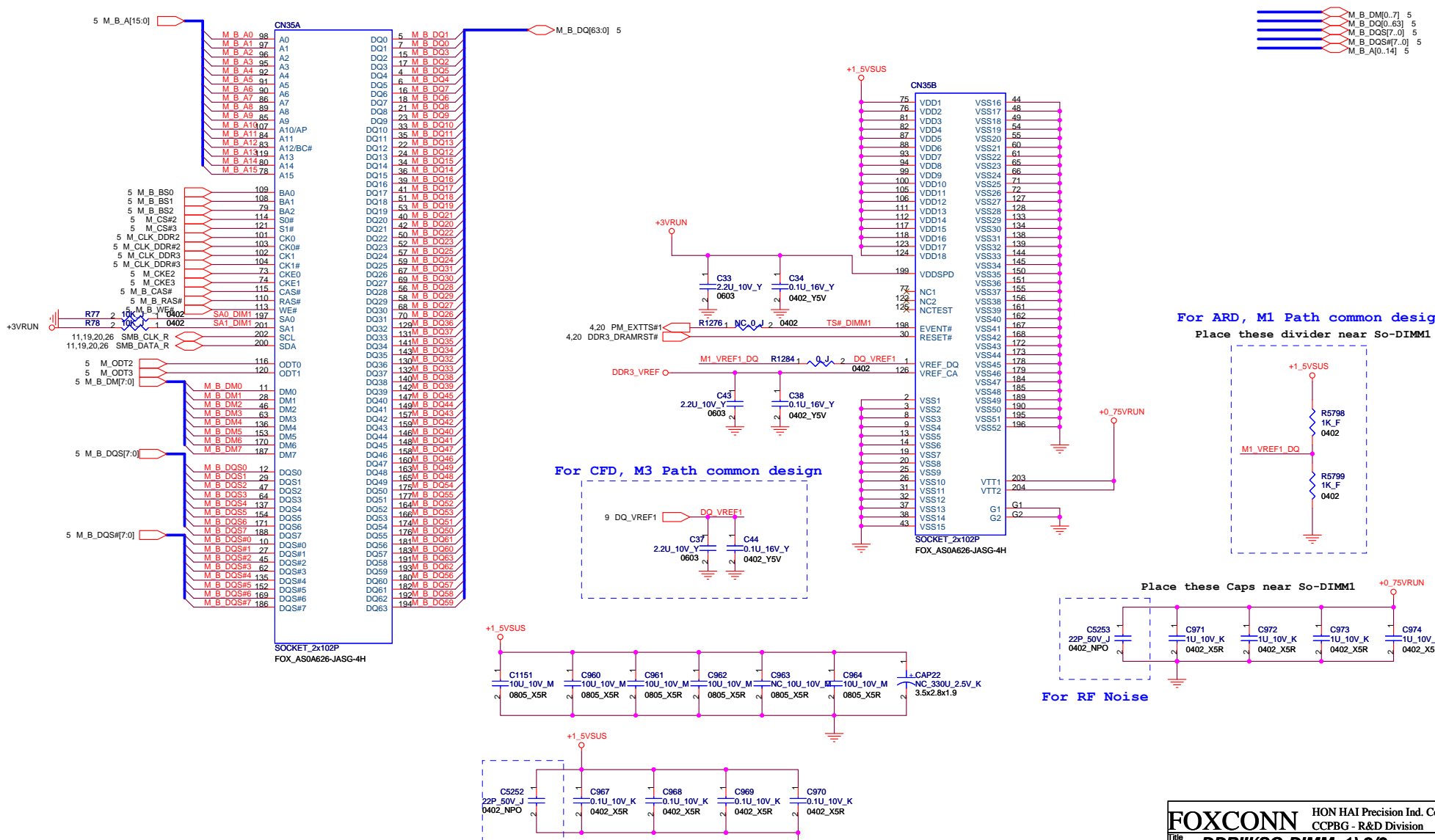
For ARD, M1 Path common design  
Place these divider near So-DIMM0



For RF Noise



Place these Caps near So-DIMM0



For ARD, M1 Path common design  
Place these divider near So-DIMM1

For CFD, M3 Path common design

Place these Caps near So-DIMM1

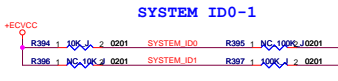
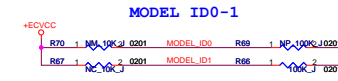
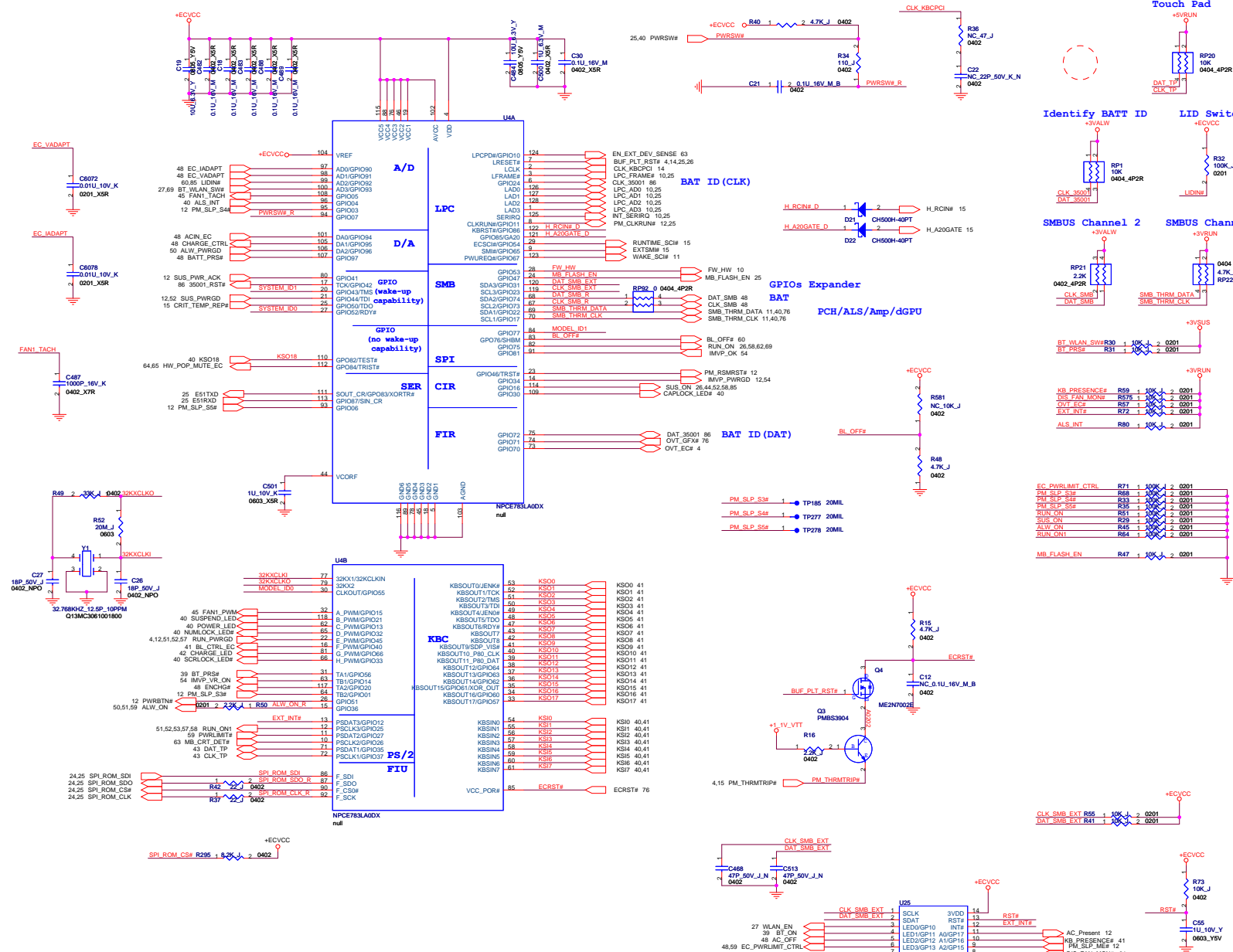
For RF Noise

For RF Noise

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Title <b>DDRIII(SO-DIMM 1) 2/3</b>			
Size	Document Number	Rev	SA
Custom	<b>M931 (MBX-215)</b>		
Date:	Wednesday, January 06, 2010	Sheet	21 of 93

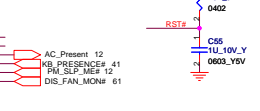
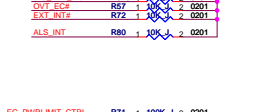
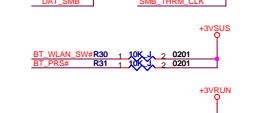
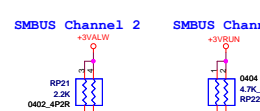
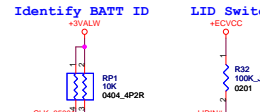
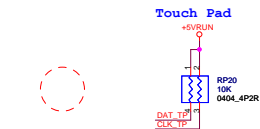
Delete M2 Path (Intel Revised)

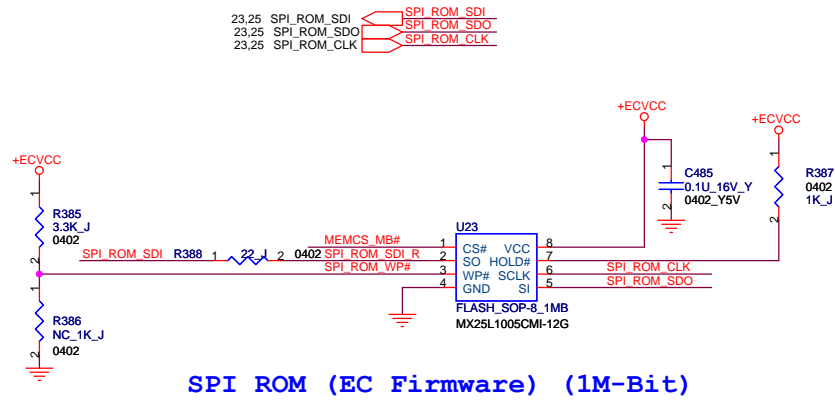
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
<b>SO-DIMM VREF 3/3</b>			
Size	Document Number	Rev	
A3	<b>M931 (MBX-215)</b>	<b>SA</b>	
Date:	Wednesday, January 06, 2010	Sheet	22 of 93



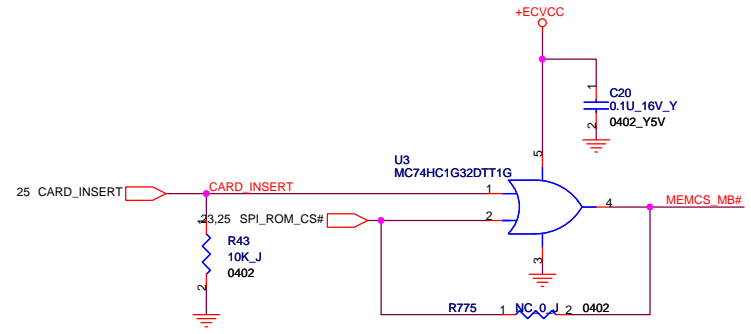
ID1 (Reserve)	ID0	SKU
0	0	SLI+H11P-GE1
0	1	SLIEGO+H11M-GE1
1	0	
1	1	

ID1	ID0	Model Name
0	0	M930
0	1	M931
1	0	Reserve
1	1	Reserve



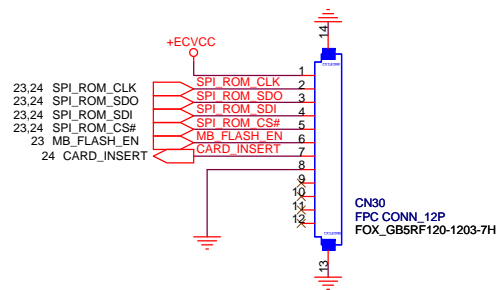


SPI ROM (EC Firmware) (1M-Bit)



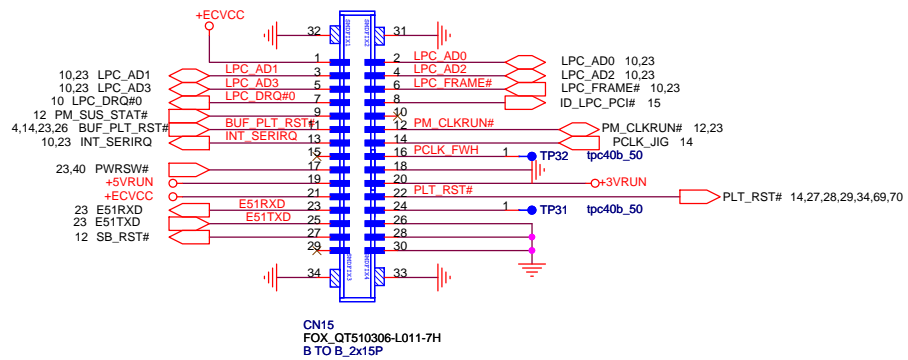
For MP, Dummy R43, C20, U3, CN30 and Stuff R775





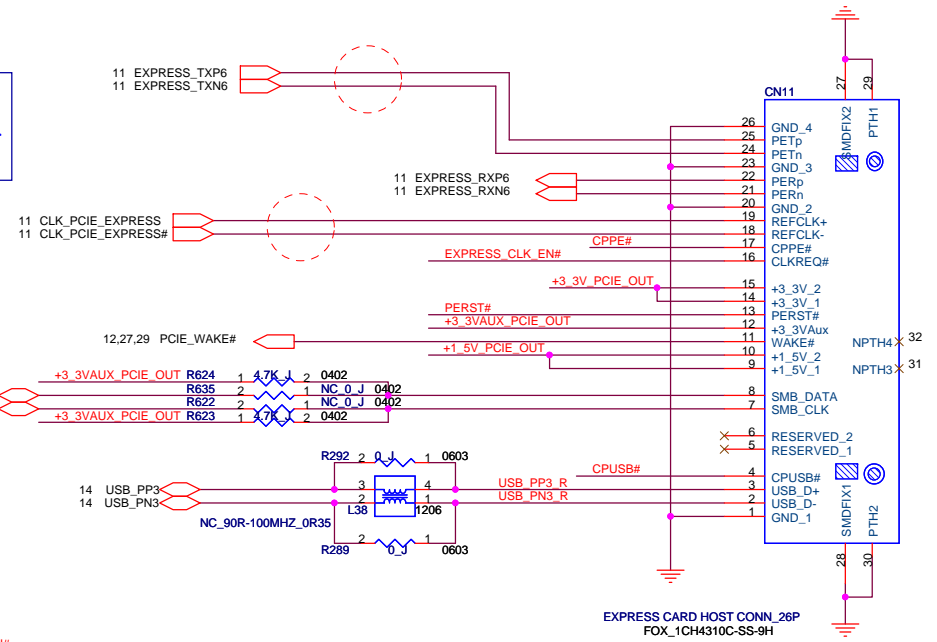
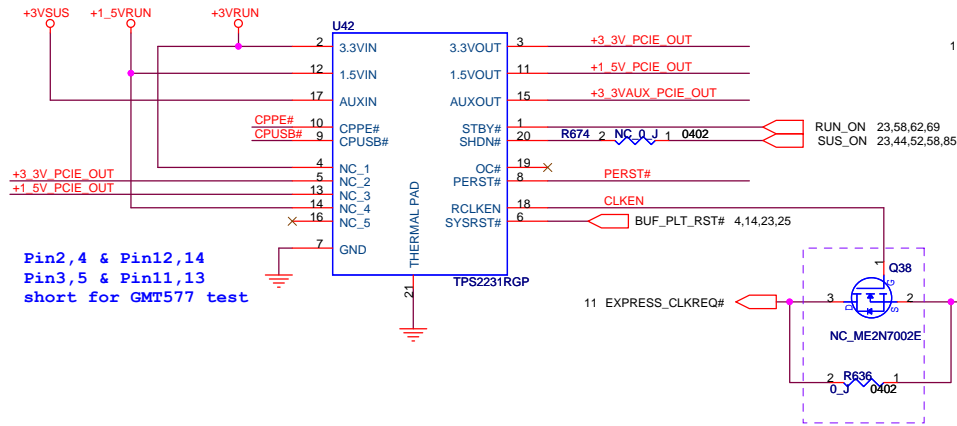
EXTERNAL SPI ROM INTERFACE (EC)

For MP, Dummy R43, C20 ,U3 ,CN30 and Stuff R775

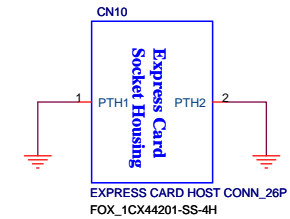
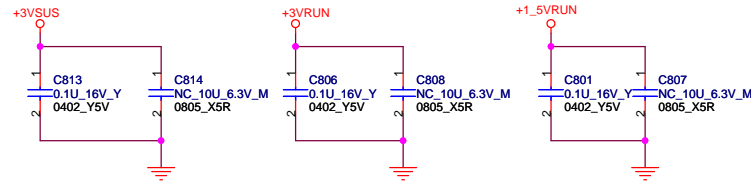


JIG-120

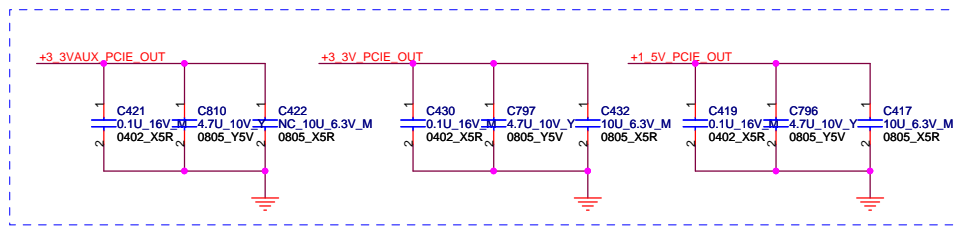
+1\_5V=>0.65A  
 +3\_3VAux=>0.275A  
 +3\_3V=>1.3A



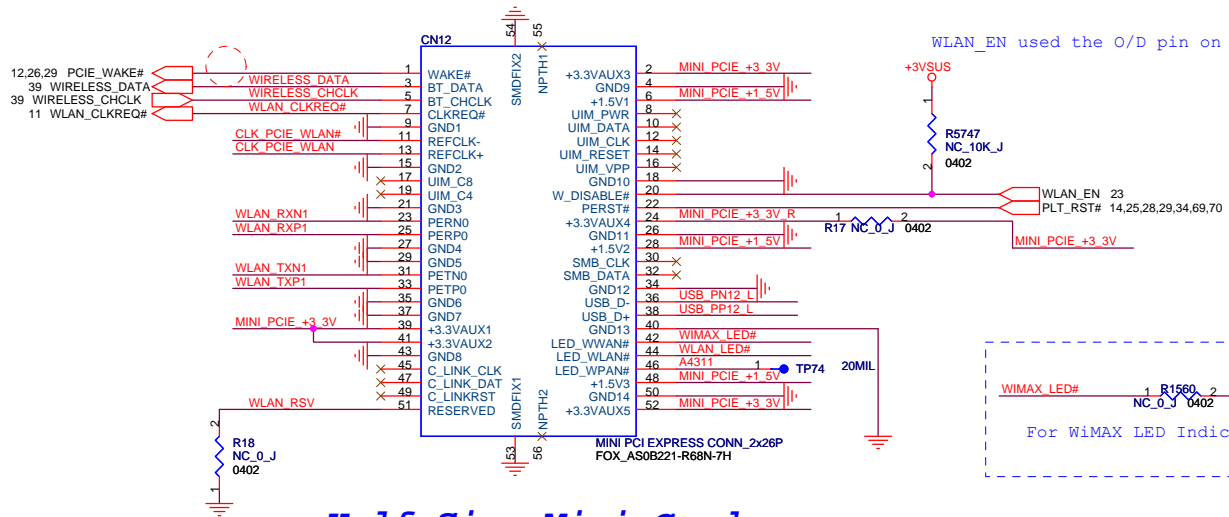
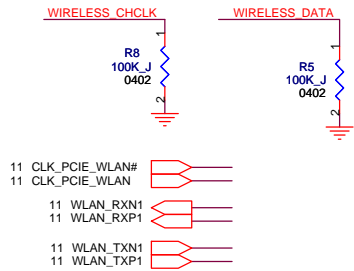
Express Card Slot.



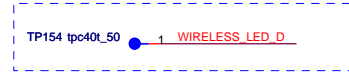
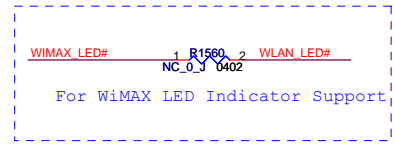
Express Card Housing.



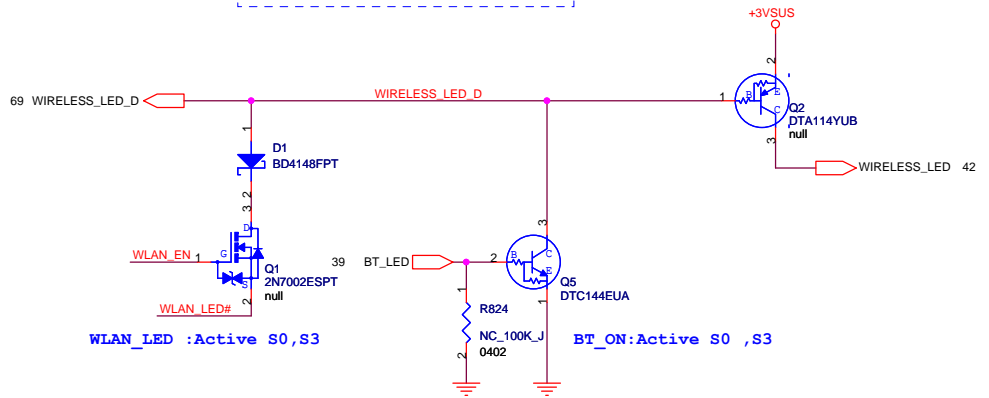
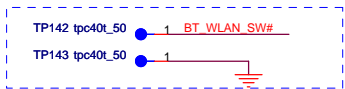
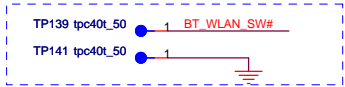
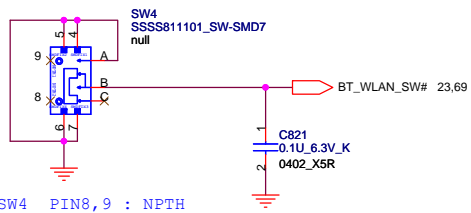
Place near by CN11 Pin.



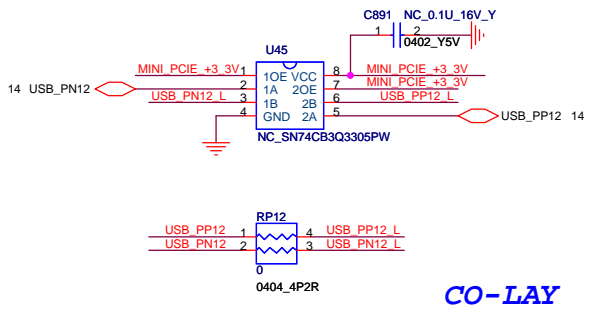
**Half Size Mini Card**



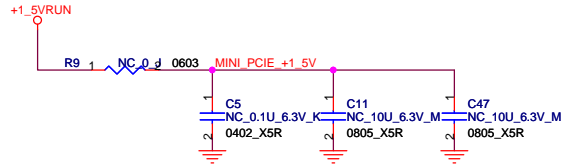
**WLAN Switch**



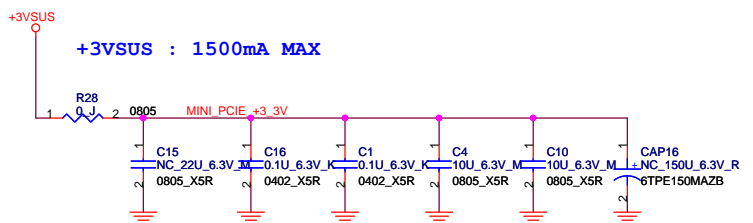
**USB I/F for Wi-MAX(Kilmer Peak)**

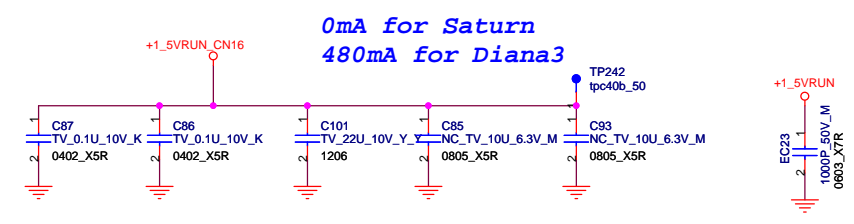
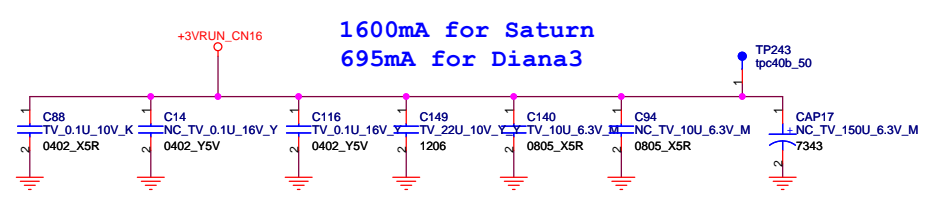
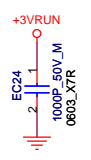
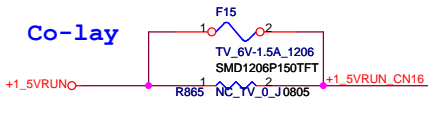
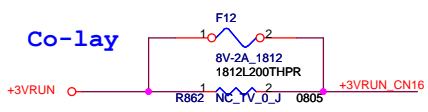


**+1\_5VRUN : 330mA MAX**  
Intel Puma Peak & Kilmer Peak nonsupport +1\_5VRUN

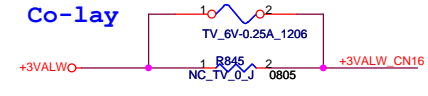
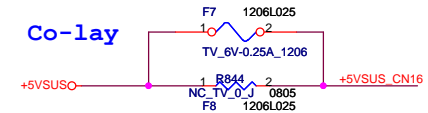
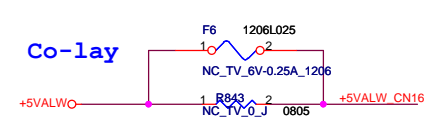
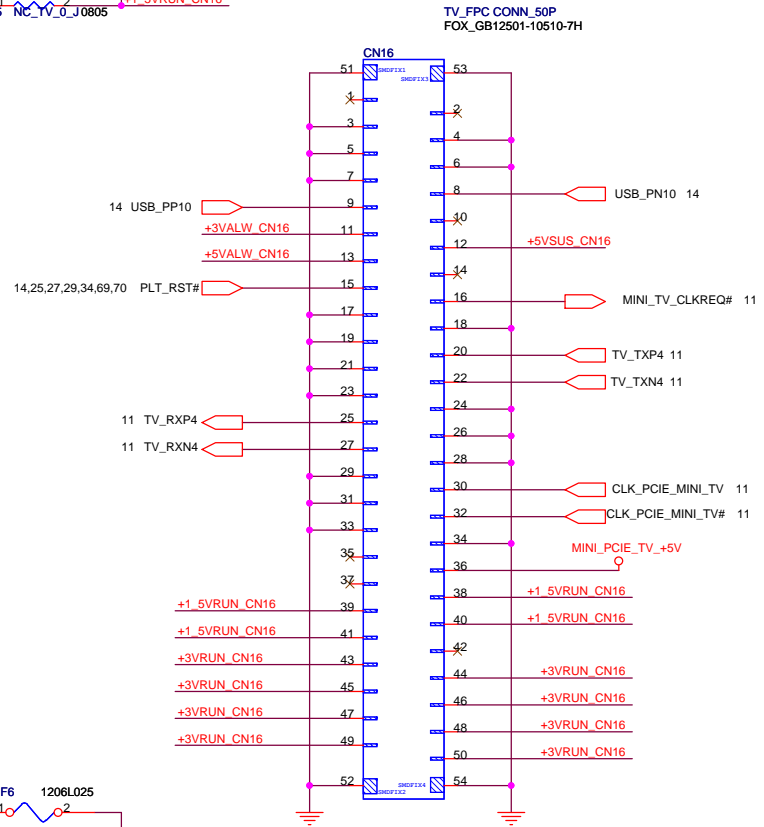
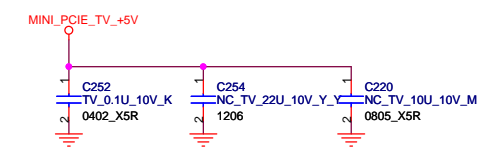
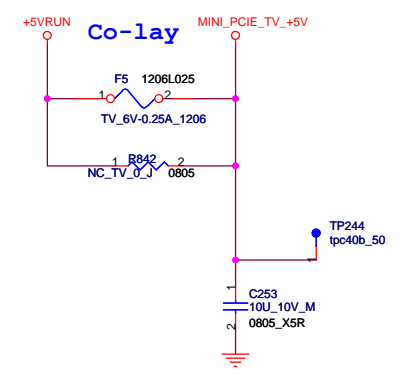


**+3VSUS : 1500mA MAX**

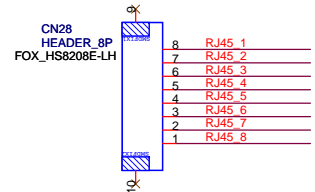
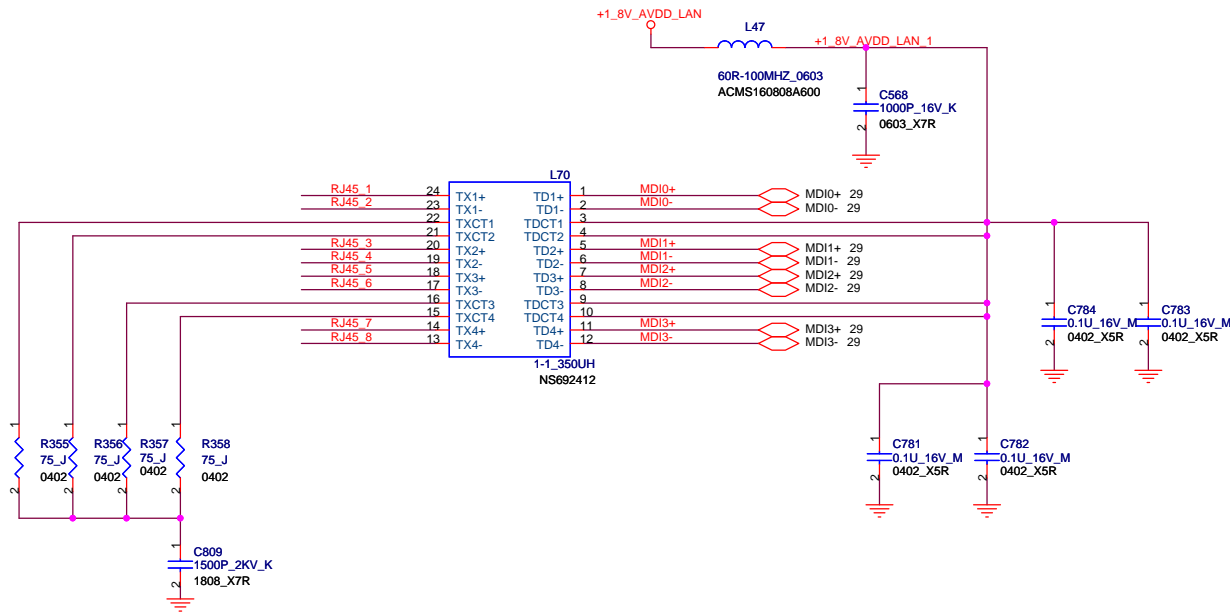




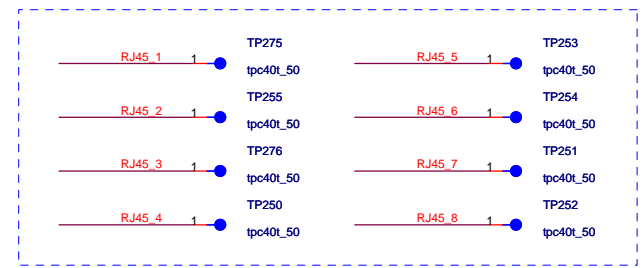
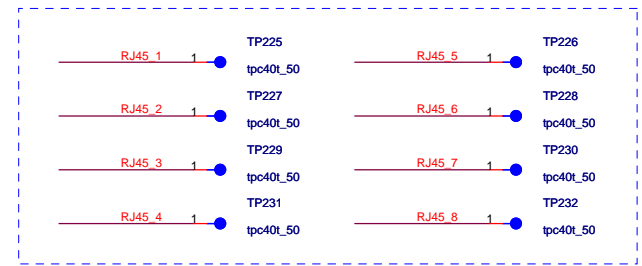
**20mA for Saturn  
20mA for Diana3**

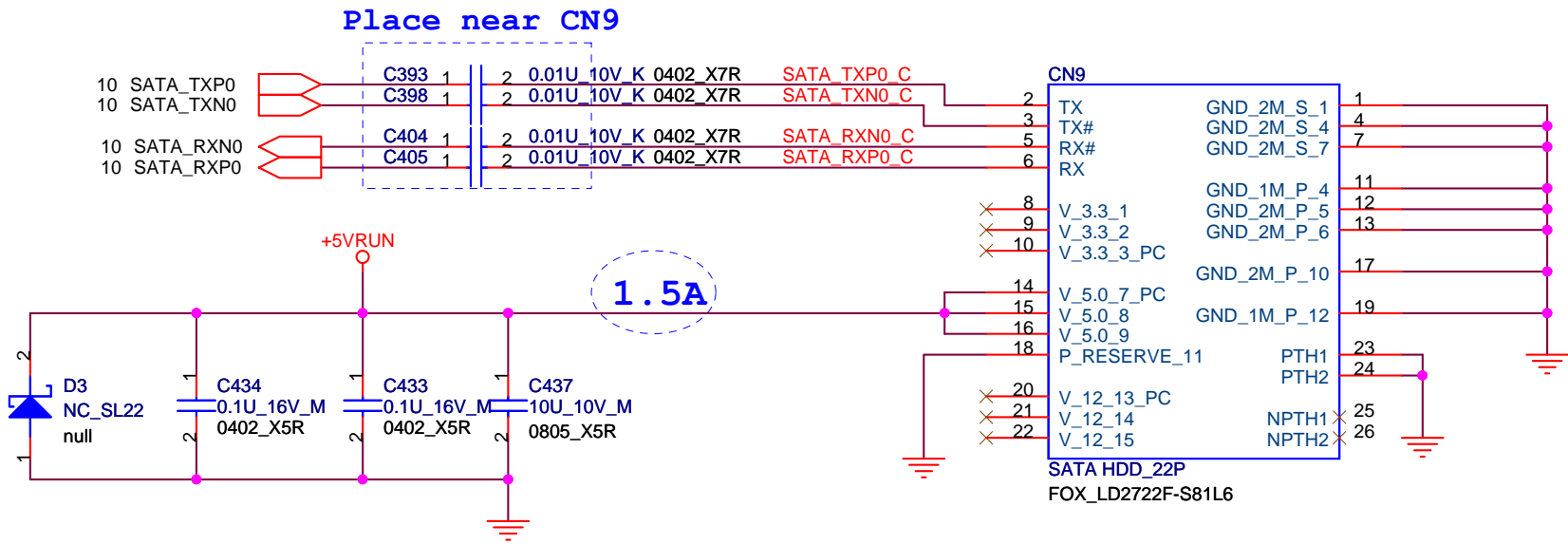






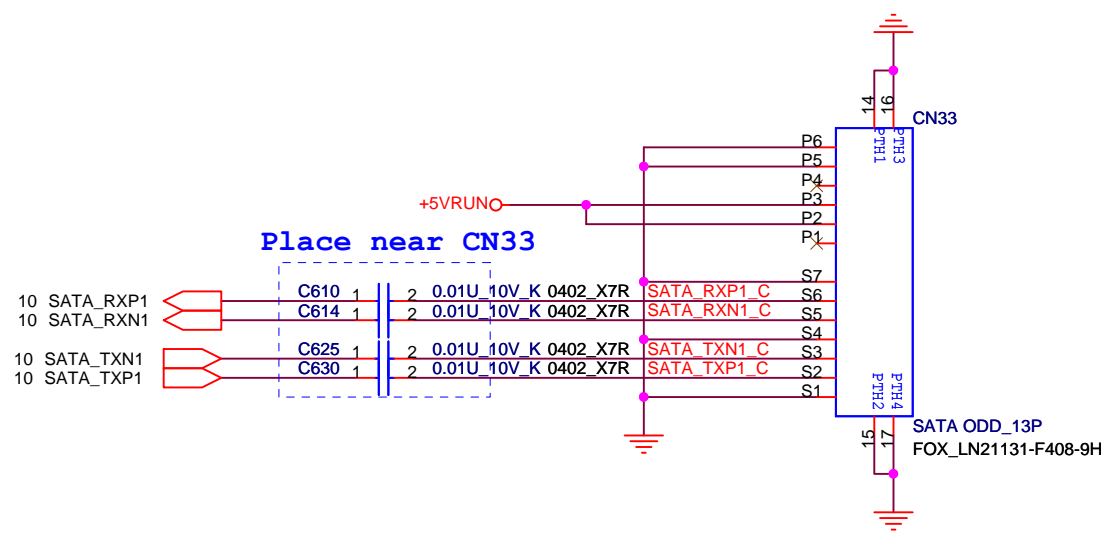
### RJ45



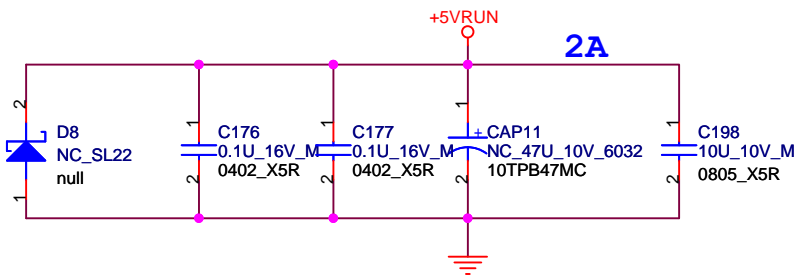


## SATA HDD CONN

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>SATA HDD</b>			
Size	Document Number		Rev
A	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	31 of 93



## SATA ODD CONN

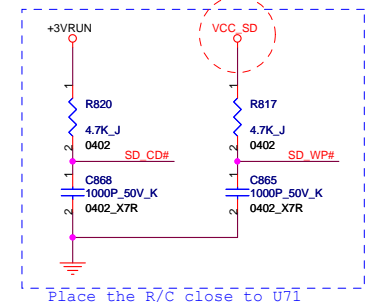
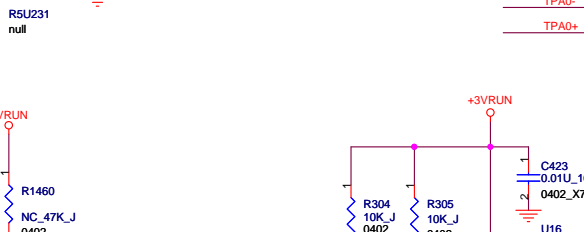
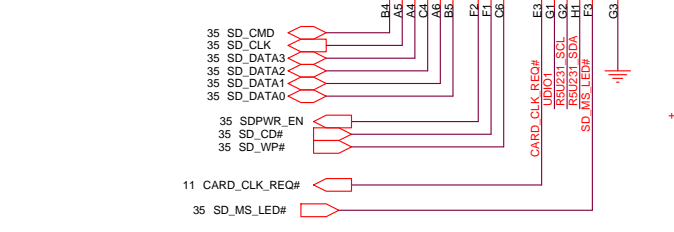
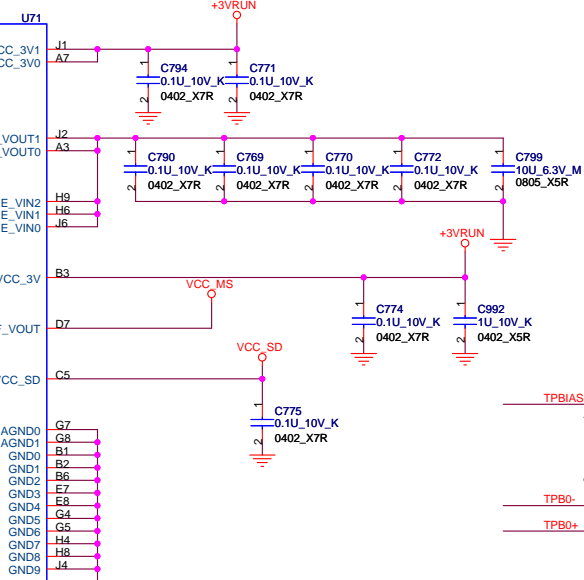
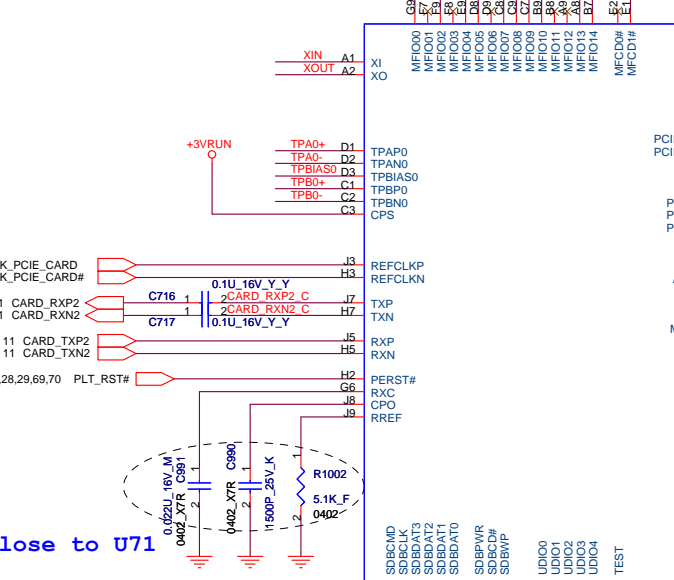
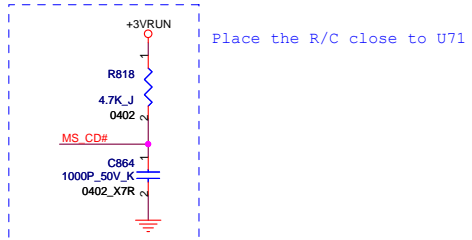
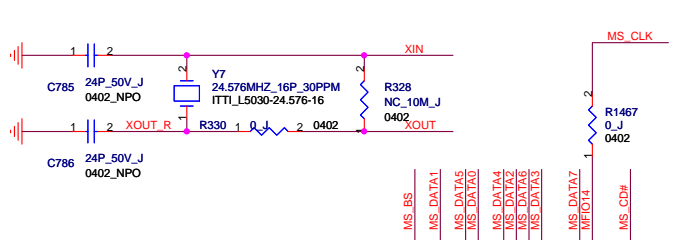


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>SATA ODD</b>			
Size	Document Number		Rev
A4	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	32 of 93



Remove Braidwood (Intel Updated and MOR confirmed)

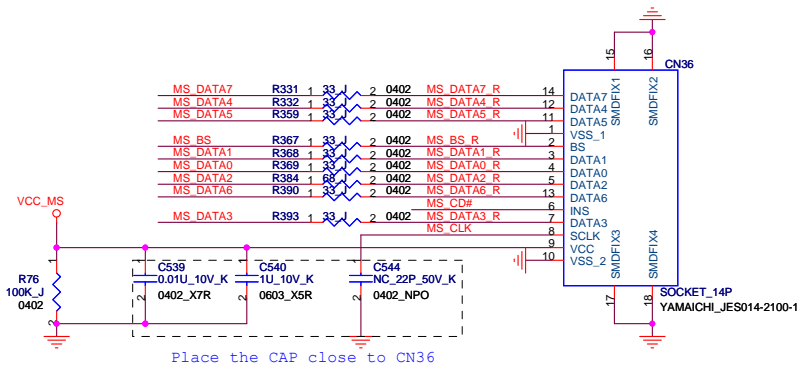
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>Braidwood Connector</b>			
Size	Document Number	Rev	
Custom	<b>M931 (MBX-215)</b>	<b>SA</b>	
Date:	Wednesday, January 06, 2010	Sheet	33 of 93



**SROM: UDIO1**  
 Pull-Hi: Disable  
 Pull-Lo: Enable (Default)

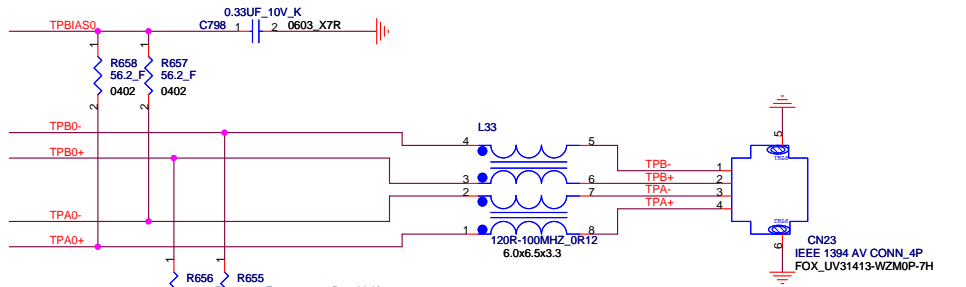
Place the R/C close to U71

Place the R/C close to U71

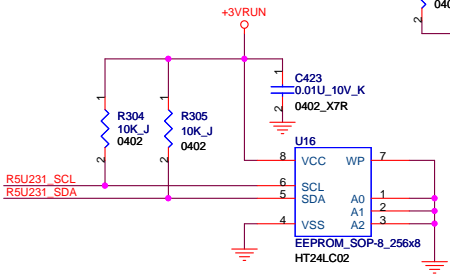


Place the CAP close to CN36

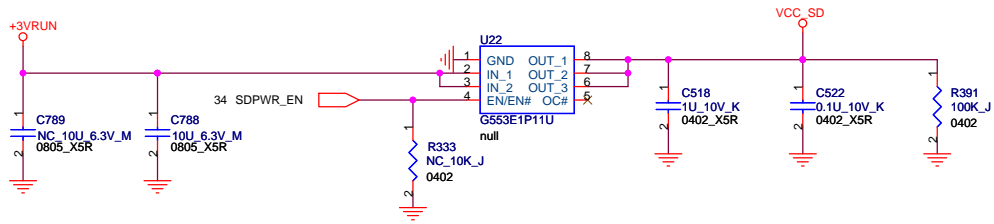
**MS HG-DUO CONN.**



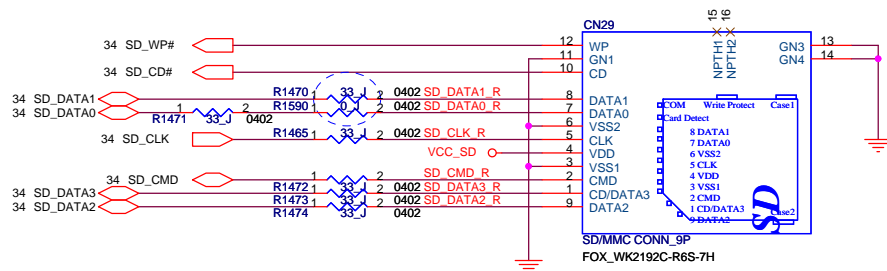
**i.Link CONN.**



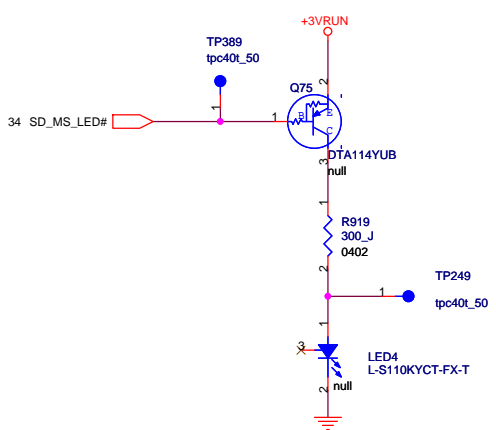
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>PCIE (MS&amp;iLink) 1/2</b>		
Size	Document Number		
Custom	<b>M931 (MBX-215)</b>		
Date:	Wednesday, January 06, 2010	Sheet	34 of 93
Rev	<b>SA</b>		



**SD POWER**



**SD CONN.**



**SD/MS LED**

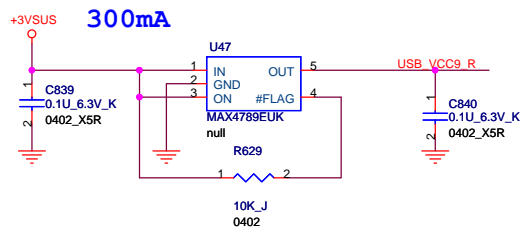
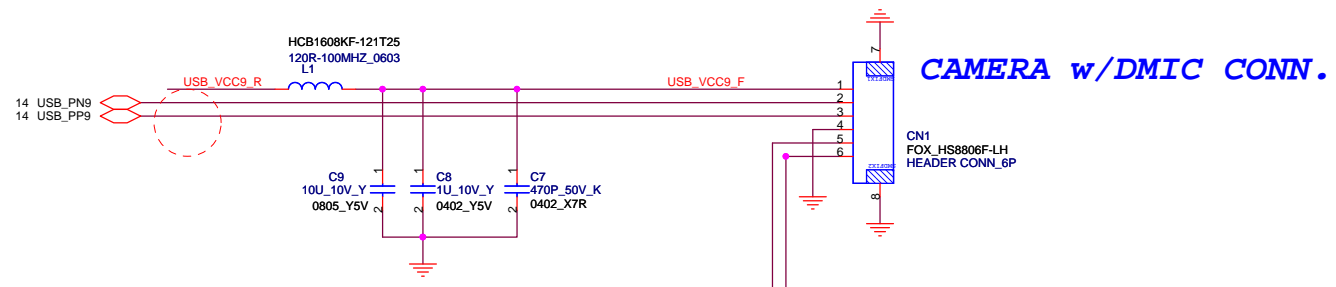


For EMI

- TP455 tpc40t\_50 SD\_WP#
- TP456 tpc40t\_50 SD\_CD#
- TP457 tpc40t\_50 SD\_DATA1\_R
- TP458 tpc40t\_50 SD\_DATA0\_R
- TP459 tpc40t\_50 SD\_CLK\_R
- TP460 tpc40t\_50 VCC\_SD
- TP469 tpc40t\_50 SD\_CMD\_R
- TP470 tpc40t\_50 SD\_DATA3\_R
- TP471 tpc40t\_50 SD\_DATA2\_R
- TP472 tpc40t\_50

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>PCIE (SD) 2/2</b>		CCPBG - R&D Division	
Size	Document Number	Date	Rev
Custom	<b>M931 (MBX-215)</b>	Wednesday, January 06, 2010	<b>SA</b>
		Sheet 35	of 93

- TP233 tpc40t\_50 1 DMIC\_CLK
- TP234 tpc40t\_50 1 DMIC\_DAT
- TP1 tpc40t\_50 1 USB\_VCC9\_F
- TP120 tpc40t\_50 1 USB\_PN9
- TP121 tpc40t\_50 1 USB\_PP9
- TP122 tpc40t\_50 1



**Current Limit Switch**

14 USB\_PN11  
14 USB\_PP11

L16 120R-100MHZ\_0603  
TB160808B121

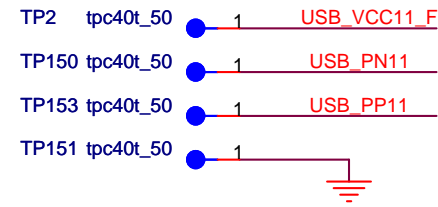
C152 10U\_10V\_M 0805\_X5R  
C142 NC\_1U\_10V\_Y 0603

C171 470P\_50V\_K 0402

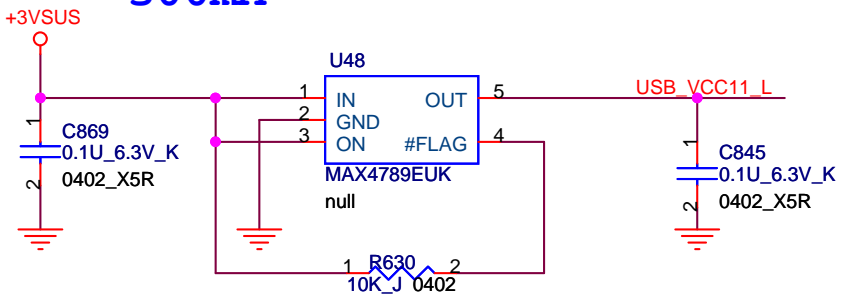
CN7 FPC CONN\_6P  
FOX\_GB5RF060-1203-7H

## Felica Conn.

Felica Vdd Spec. (3.15V to 3.45V)



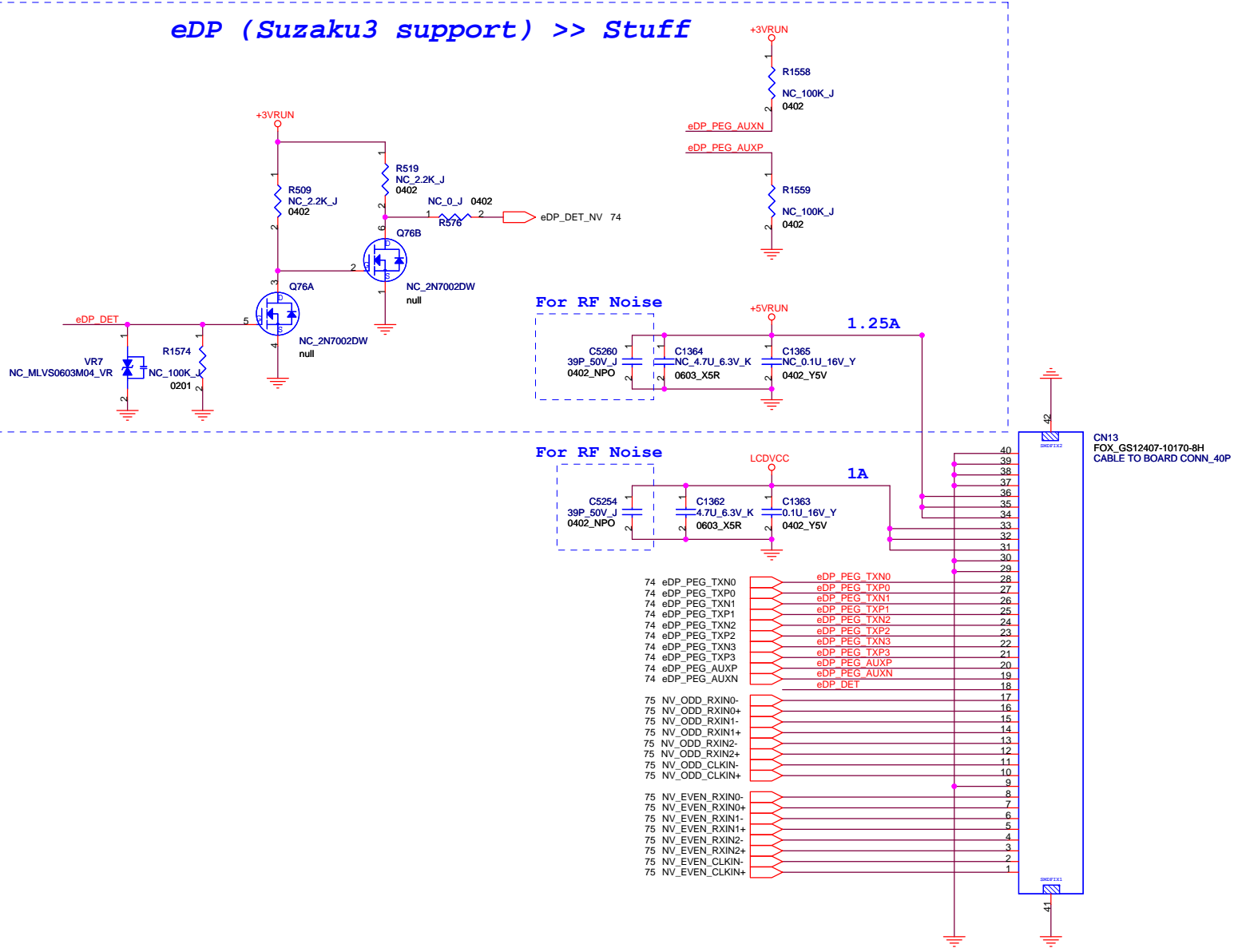
300mA



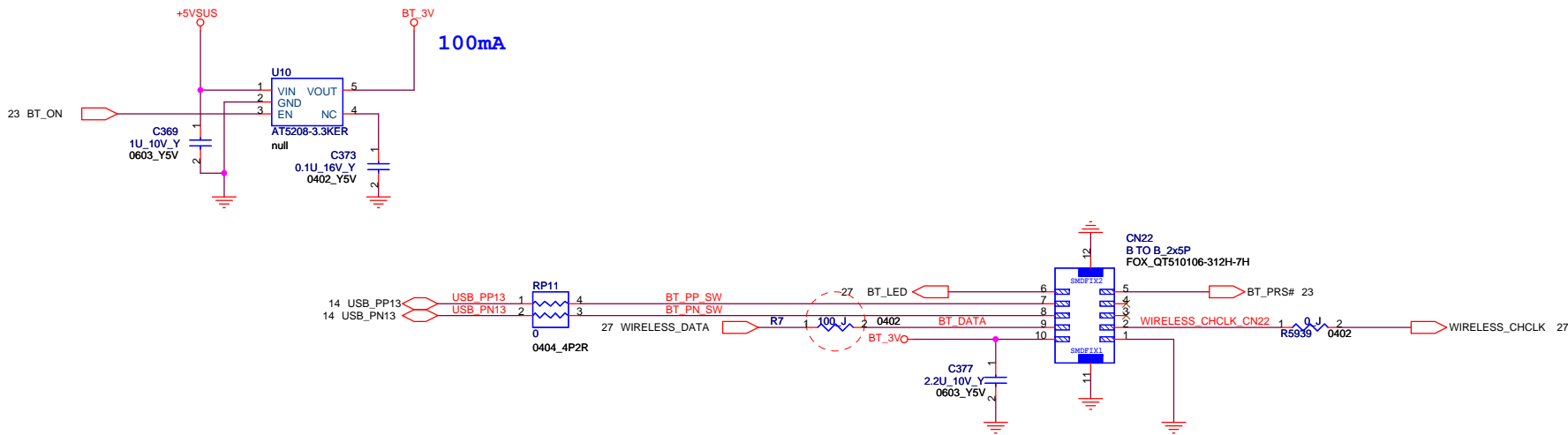
## Current Limit Switch

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>Felica Connector</b>			
Size A	Document Number <b>M931 (MBX-215)</b>	Rev <b>SA</b>	
Date:	Wednesday, January 06, 2010	Sheet	37 of 93

# eDP (Suzaku3 support) >> Stuff



## eDP & LVDS CONNECTOR

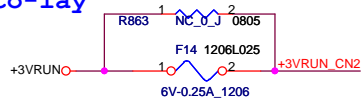


Place C377 close to CN22, Pin10

## Bluetooth CONN.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Bluetooth Connector</b>			
Size	Document Number		Rev
Custom	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	39 of 93

Co-lay



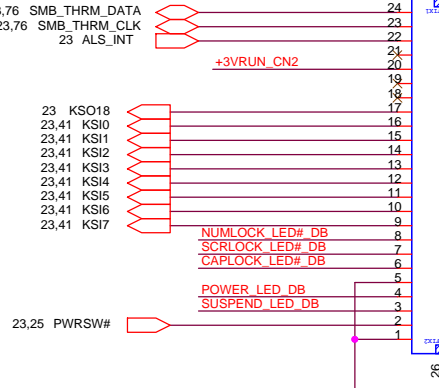
Light Sensor (EC)

11,23,76 SMB\_THRM\_DATA  
 11,23,76 SMB\_THRM\_CLK  
 23 ALS\_INT

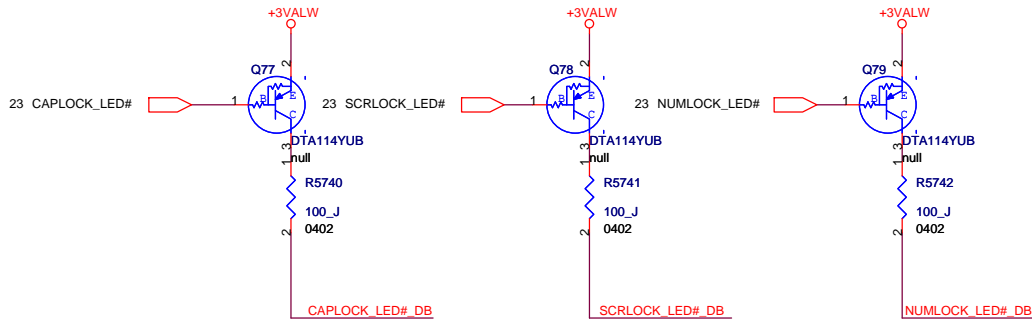
Switch Keyboard Matrix

Keyboard LED

Power Button



Switch DB Conn.



TP385 tpc40b\_50 1 PWSW#

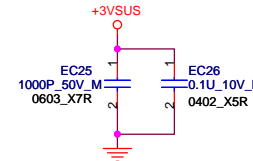
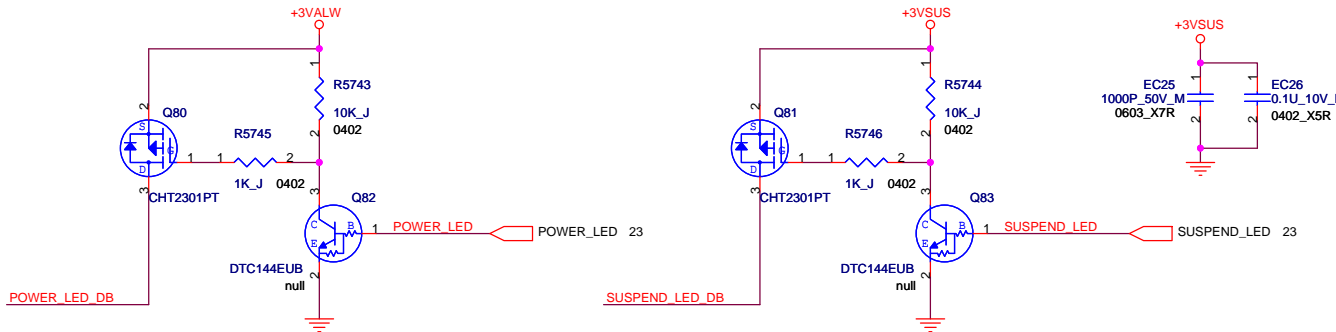
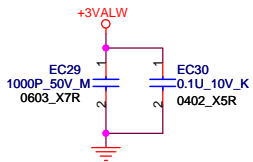
TP376 tpc40b\_50 1

Top side ,Closer together

TP462 tpc40b\_50 1 PWSW#

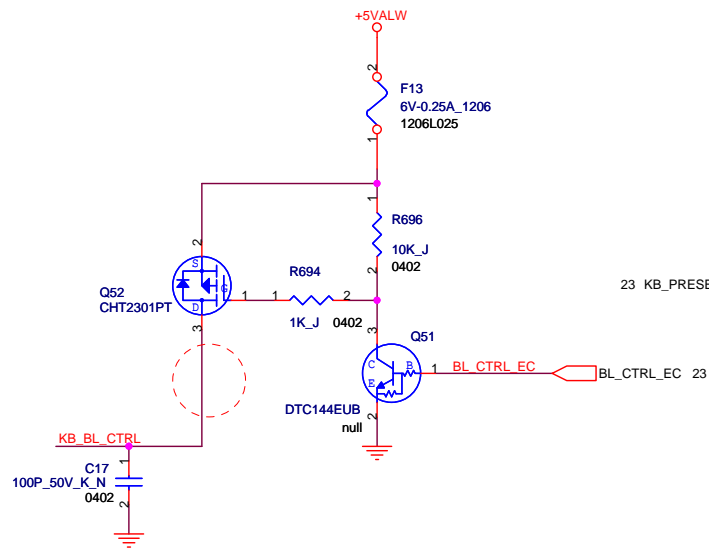
TP384 tpc40b\_50 1

Bot side ,Closer together

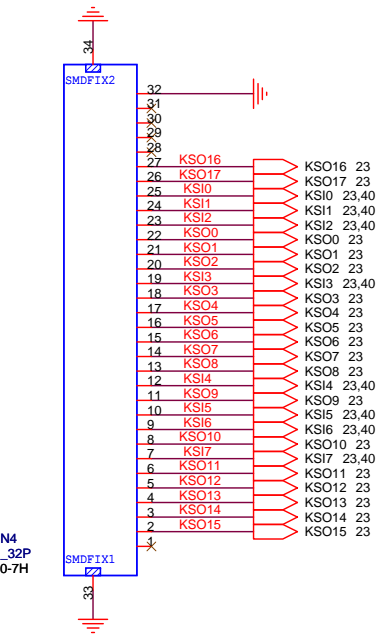
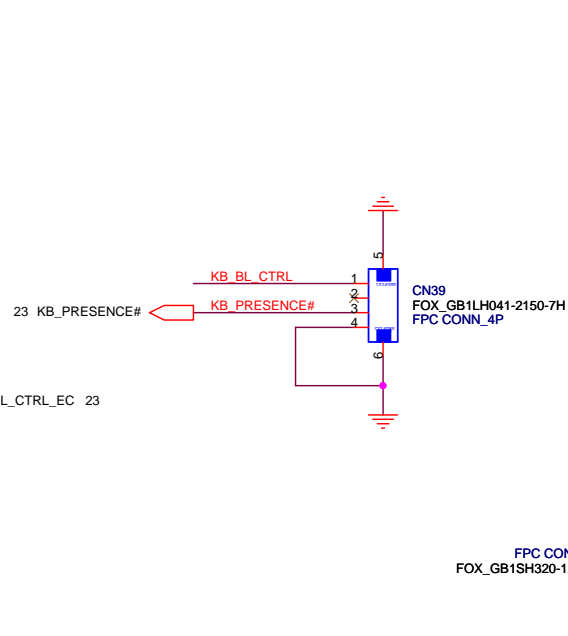


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>Switch DB Connector</b>		
Size	Document Number		Rev
Custom	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	40 of 93





**Backlit Power Conn**

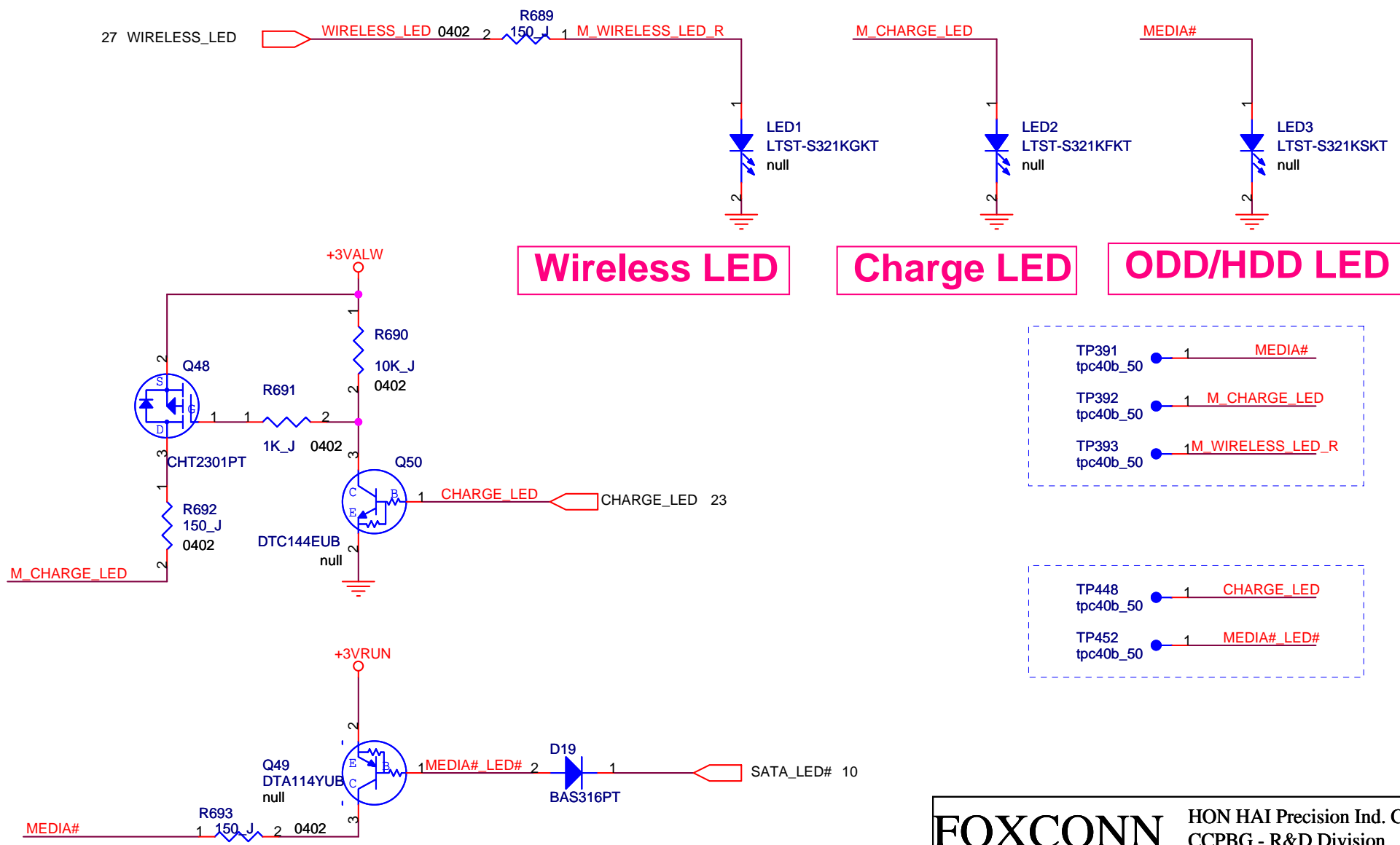


**KBC Conn**

KSI0	1	TP382	tpc40t_50
KSO10	1	TP381	tpc40t_50
KSI7	1	TP383	tpc40t_50
KSI2	1	TP394	tpc40t_50
KSO6	1	TP461	tpc40t_50

KSI0	1	TP280	tpc40t_50
KSO10	1	TP281	tpc40t_50
KSI7	1	TP282	tpc40t_50
KSI2	1	TP387	tpc40t_50
KSO6	1	TP388	tpc40t_50

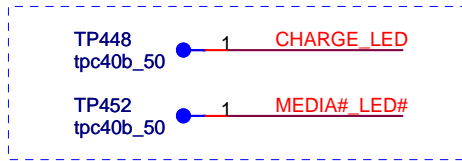
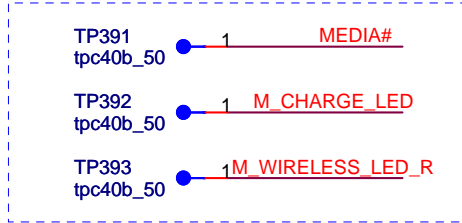
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>KB &amp; Backlit Connector</b>			
Size	Document Number		Rev
B	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	41 of 93



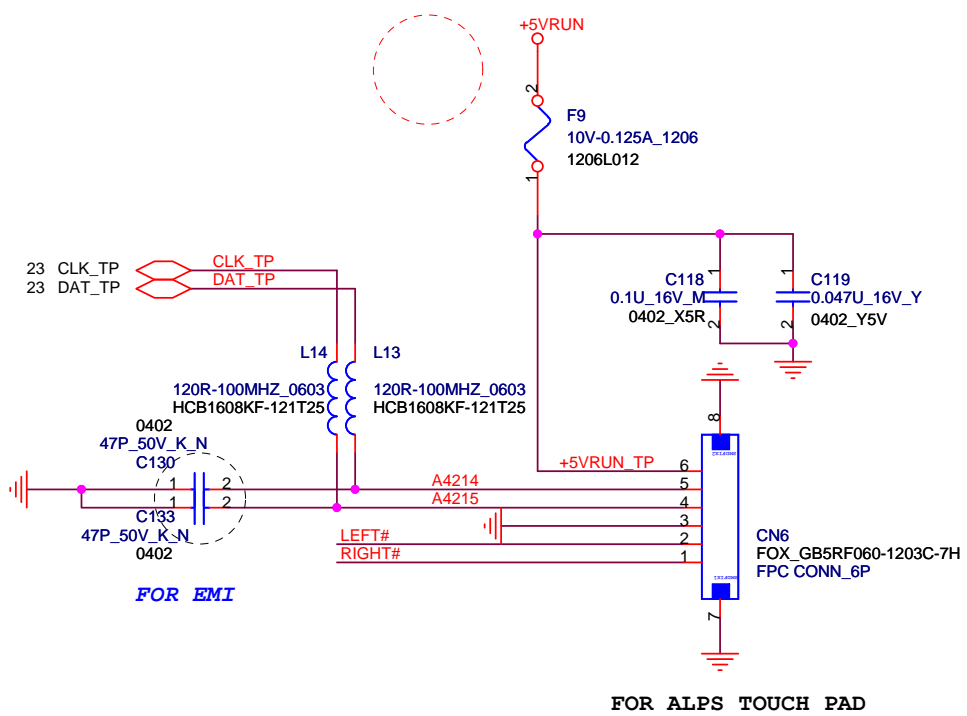
**Wireless LED**

**Charge LED**

**ODD/HDD LED**



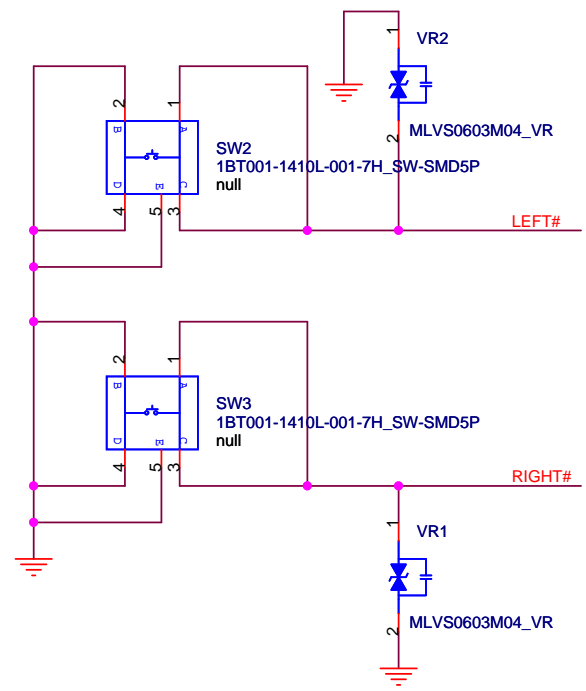
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Status LED</b>			
Size	Document Number		Rev
A	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	42 of 93



- +5VRUN\_TP 1 TP463 tpc40b\_50
- CLK\_TP 1 TP464 tpc40b\_50
- DAT\_TP 1 TP465 tpc40b\_50
- TP466 tpc40b\_50
- LEFT# 1 TP467 tpc40b\_50
- RIGHT# 1 TP468 tpc40b\_50

## Touch Pad Conn (Support Multi Touch)

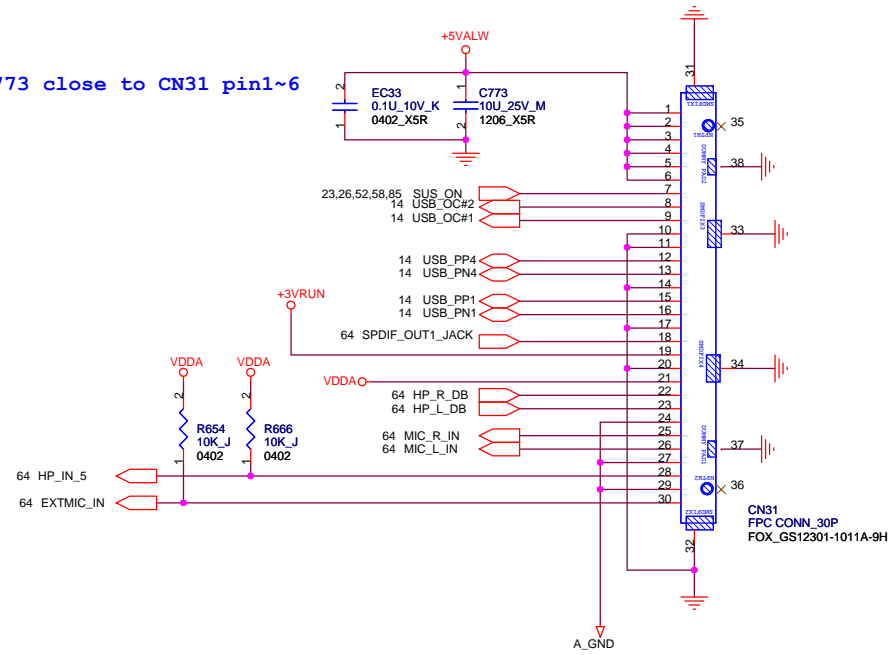
### TP\_LEFT Button



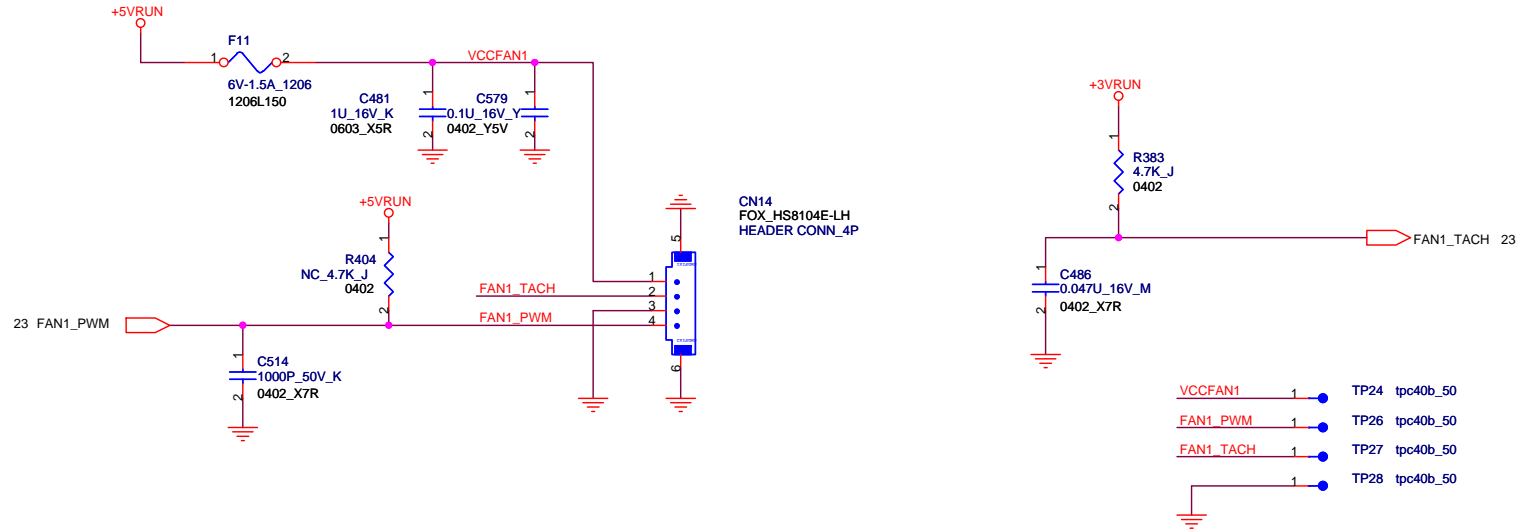
### TP\_Right Button

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title <b>Touch Pad</b>		
Size	Document Number	Rev
Custom	<b>M931 (MBX-215)</b>	<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet 43 of 93

Place C773 close to CN31 pin1~6



# Direct PWM FAN



A

B

C

D

E

4

4

3

3

2

2

1

1

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Title</b> <i>Thermal Sensor &amp; Protection</i>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	
A3	<b>M931 (MBX-215)</b>	<b>SA</b>	
<b>Date:</b>	Wednesday, January 06, 2010	<b>Sheet</b>	46 of 93

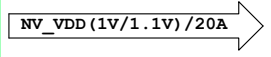
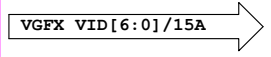
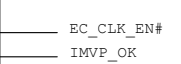
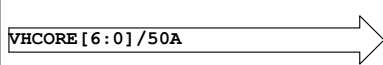
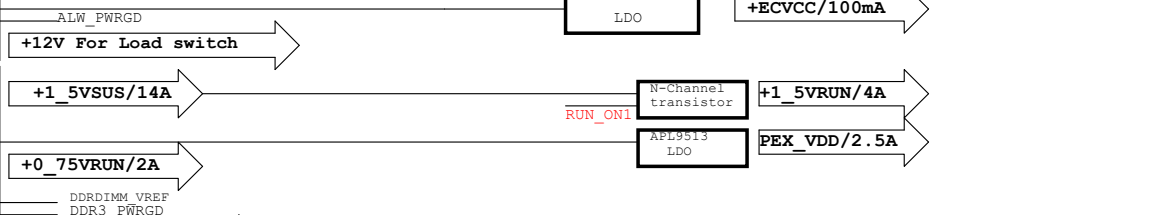
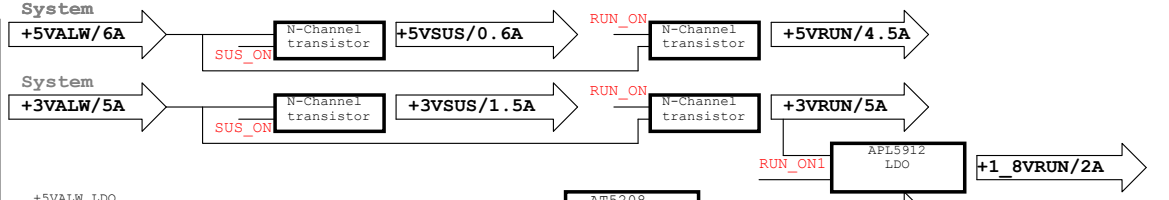
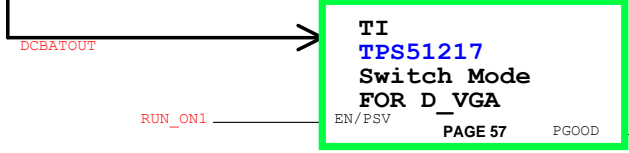
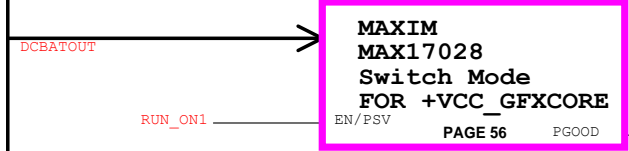
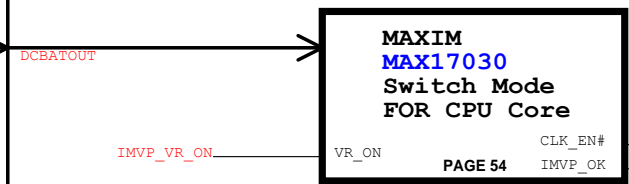
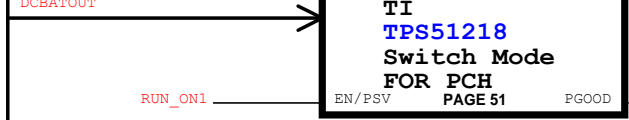
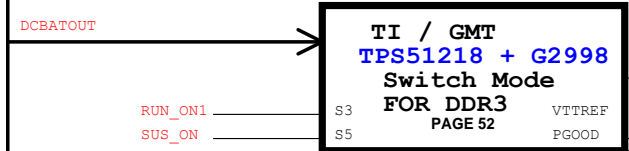
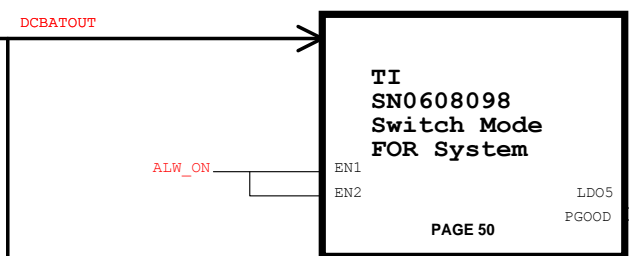
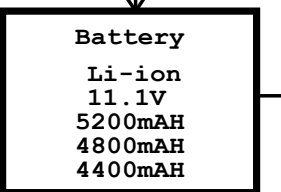
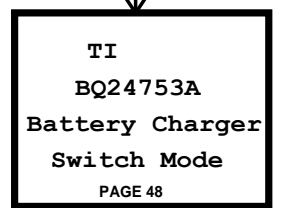
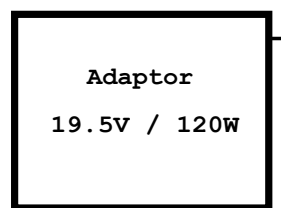
A

B

C

D

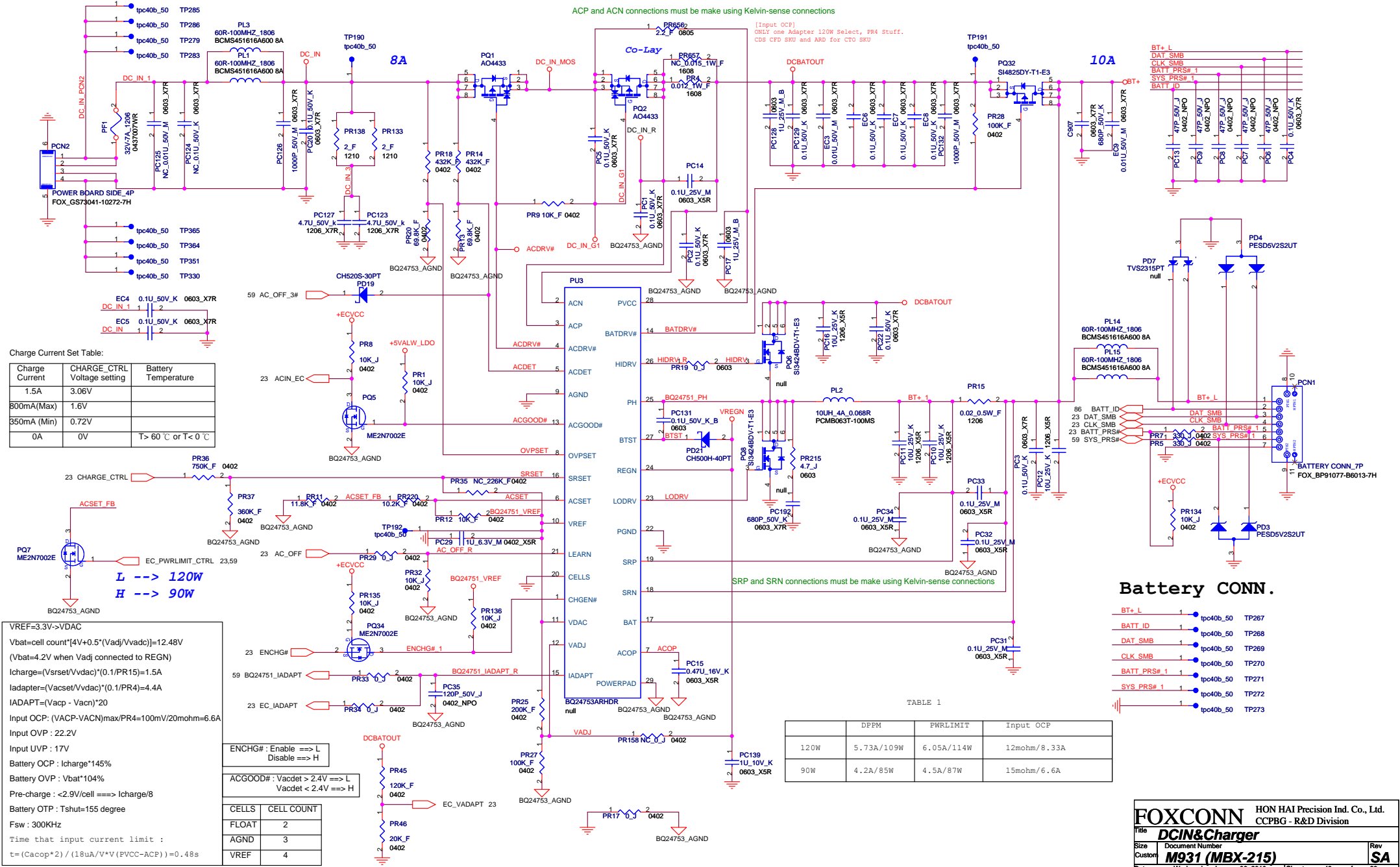
E



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Power Design Diagram</b>			
Title	Document Number	Rev	
Size	M931 (MBX-215)	SA	
Custom			
Date:	Wednesday, January 06, 2010	Sheet	47 of 93

ACP and ACN connections must be make using Kelvin-sense connections

ONLY one Adapter 120W Select, PR4 Stuff.  
CDS CPO SKU and ARD for CTO SKU



Charge Current Set Table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
800mA(Max)	1.6V	
350mA (Min)	0.72V	
0A	0V	T > 60 °C or T < 0 °C

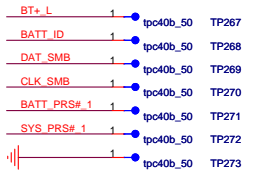
VREF=3.3V->VDAC  
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdac})] = 12.48V$   
 ( $V_{bat} = 4.2V$  when  $V_{adj}$  connected to REGN)  
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR15) = 1.5A$   
 $I_{adapter} = (V_{acset} / V_{vdac}) * (0.1 / PR4) = 4.4A$   
 $I_{ADAPT} = (V_{acp} - V_{vacn}) * 20$   
 Input OCP:  $(V_{ACP} - V_{ACN}) / \max(PR4) = 100mV / 20m\Omega = 6.6A$   
 Input OVP: 22.2V  
 Input UVP: 17V  
 Battery OCP:  $I_{charge} * 145\%$   
 Battery OVP:  $V_{bat} * 104\%$   
 Pre-charge:  $< 2.9V / \text{cell} \implies I_{charge} / 8$   
 Battery OTP:  $T_{shut} = 155 \text{ degree}$   
 Fsw: 300KHz  
 Time that input current limit :  
 $t = (C_{acop} * 2) / (18uA / V * V * (F_{VCC} - ACP)) = 0.48s$

ENCHG# : Enable ==> L Disable ==> H	
ACGOOD# : Vacdet > 2.4V ==> L Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

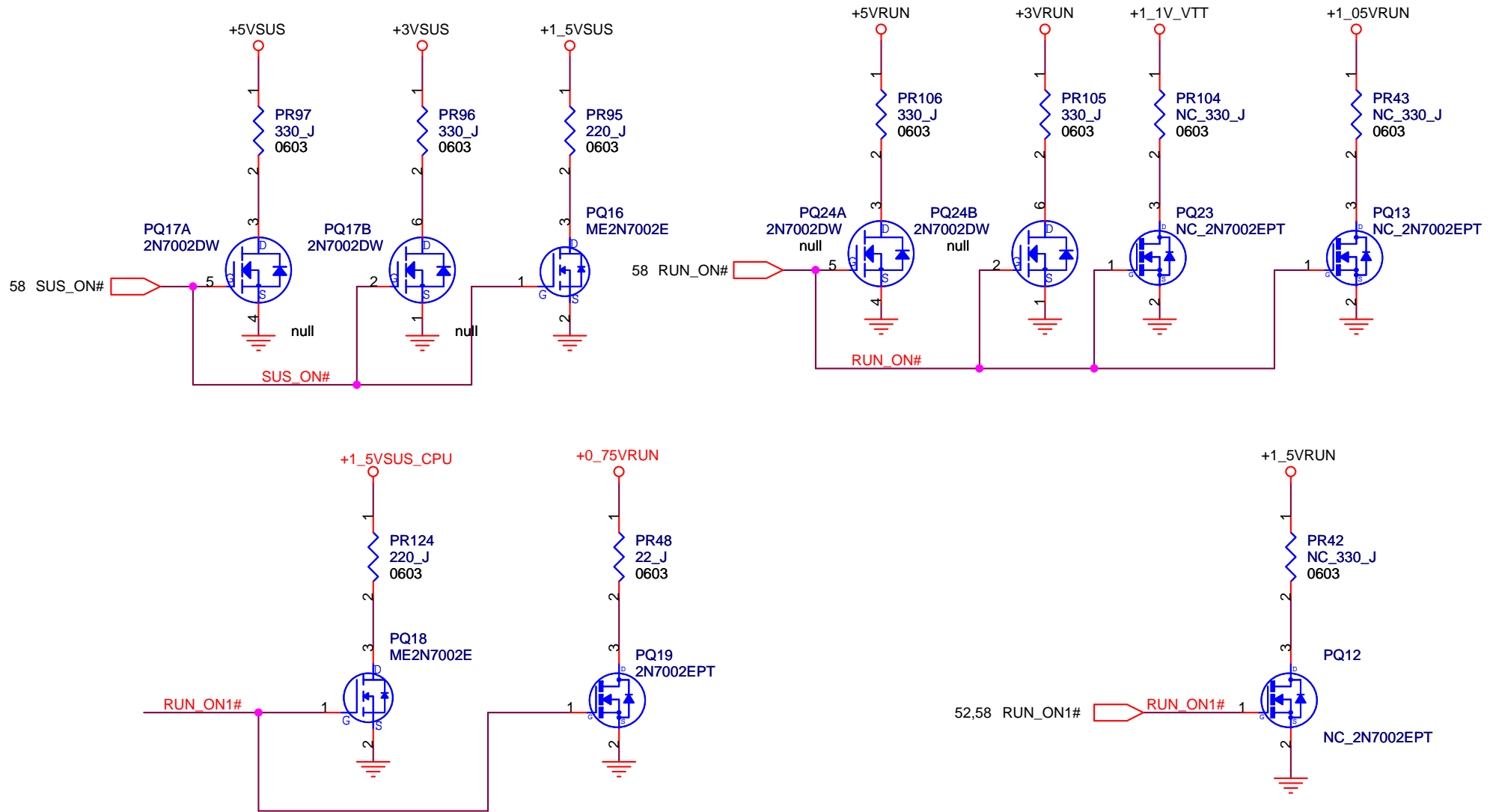
TABLE 1

	DFPM	PWRLIMIT	Input OCP
120W	5.73A/109W	6.05A/114W	12mohm/8.33A
90W	4.2A/85W	4.5A/87W	15mohm/6.6A

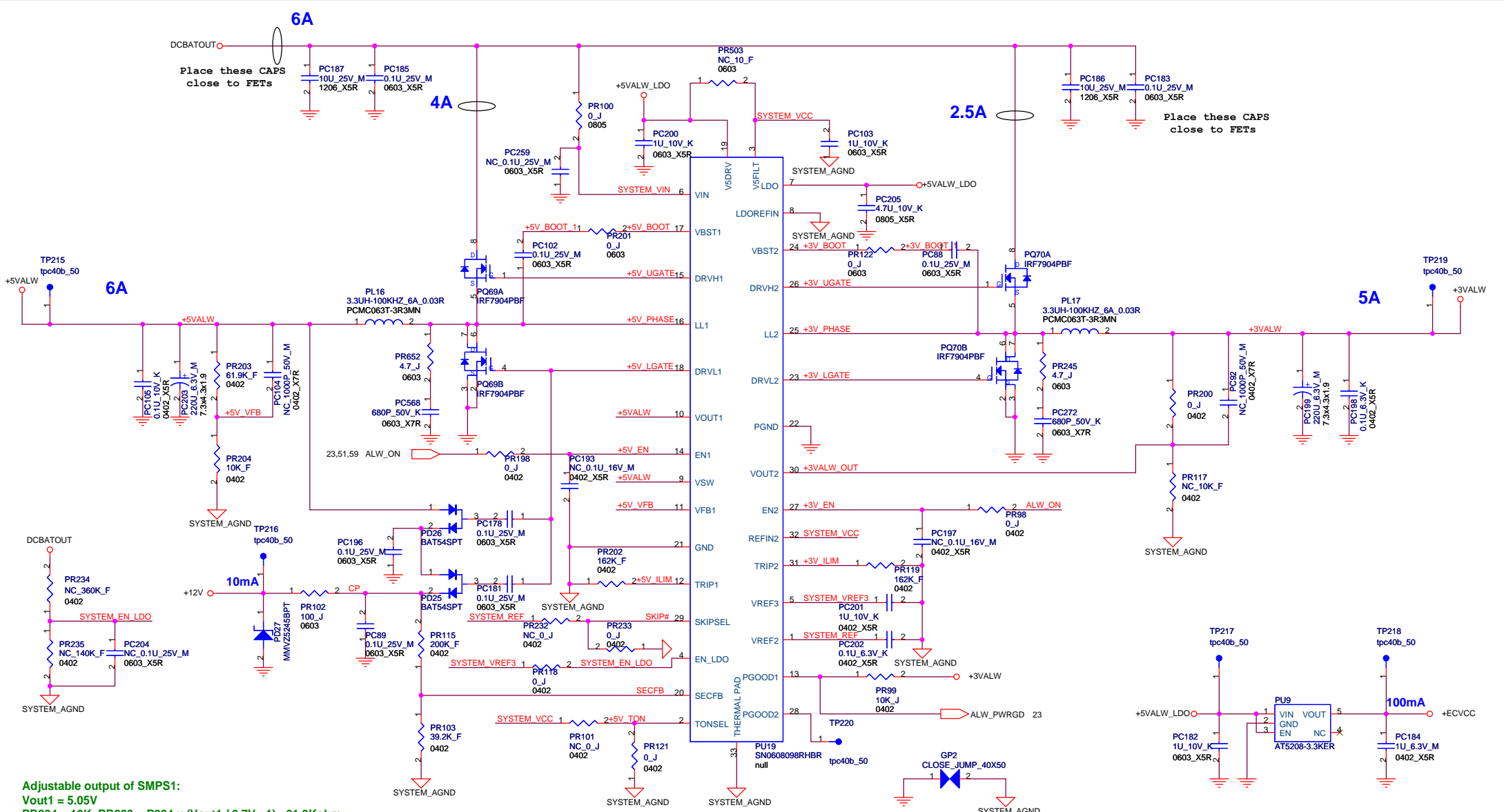
### Battery CONN.







<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>DISCHARGE CIRCUIT</b>			
Size	Document Number		Rev
A	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	49 of 93



Place these CAPS close to FETs

Place these CAPS close to FETs

**Adjustable output of SMPS1:**  
 $V_{out1} = 5.05V$   
 $PR204 = 10K, PR203 = P204 \times (V_{out1} / 0.7V - 1) = 61.9K\Omega$

**Second Feedback :**  
 $V_{out\_sec} = 12V, PR103 = 20K\Omega$   
 $PR115 = PR103 \times (V_{out\_sec} / 2V - 1) = 100K\Omega$

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = V_{OUT} (V_{IN} - V_{OUT}) / (V_{IN} \cdot f \cdot LIR \cdot I_{LOAD} (MAX))$$

$$R_{ocp} = (I_{ocp} - I_{ripple} / 2) \cdot (10 \cdot R_{ds} (on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) \cdot V_{FB1}$$

**Current limit resistor for SMPS1 :**  
 $I_{valley\_5} = 5.775A, R_{cs\_5} = R_{ds1} = 10.8m\Omega$   
 $PR202 = (10 \times I_{valley\_5} \times R_{cs\_5}) / 5uA = 162K$

**Current limit resistor for SMPS2 :**  
 $I_{valley\_3} = 5.525A, R_{cs\_3} = R_{ds2} = 10.8m\Omega$   
 $PR119 = (10 \times I_{valley\_3} \times R_{cs\_3}) / 5uA = 162K$

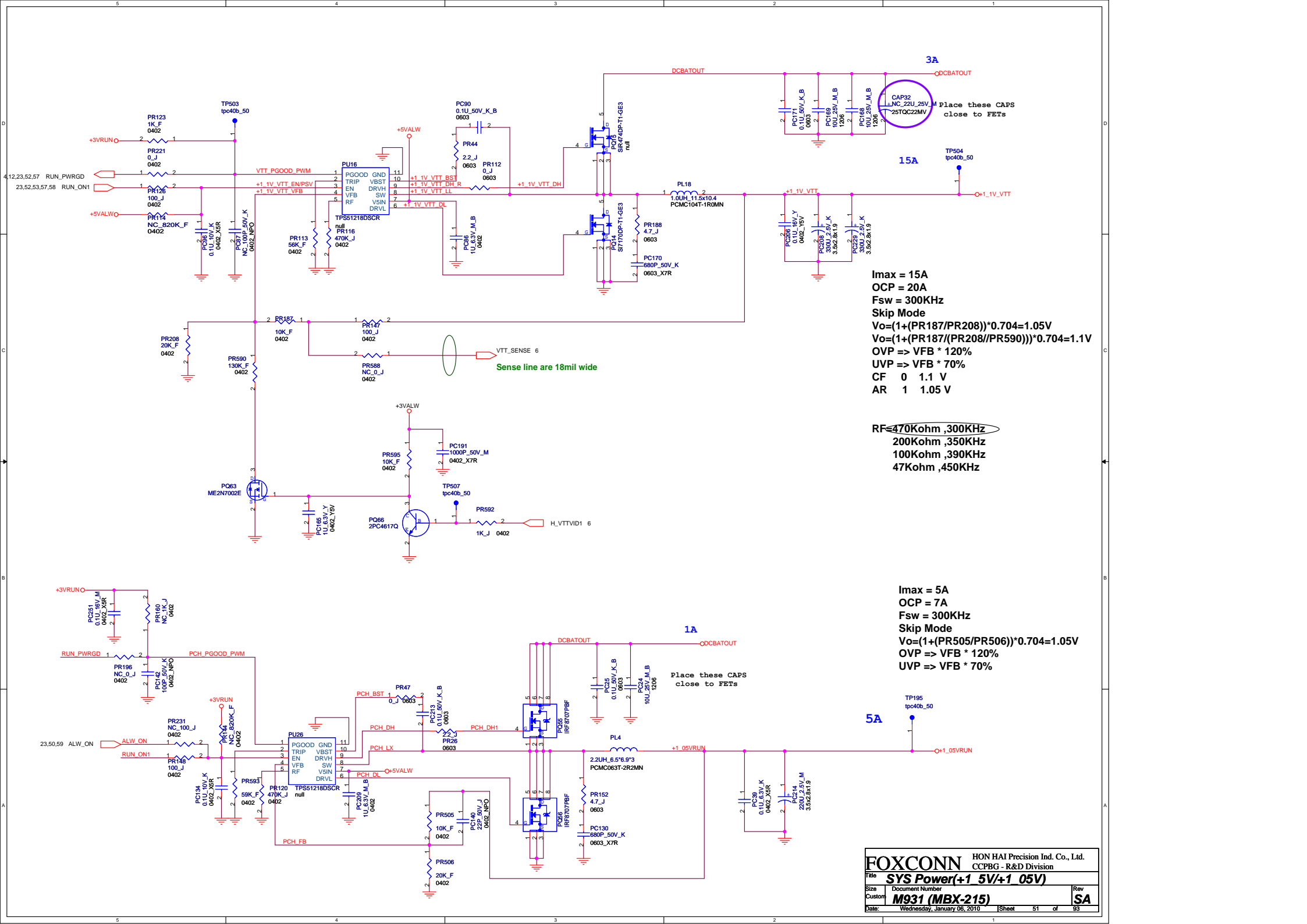
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **SYS Power (+3 3V/+5V)**

Size: Document Number  
 A3: **M931 (MBX-215)**

Date: Wednesday, January 06, 2010 Sheet 50 of 93

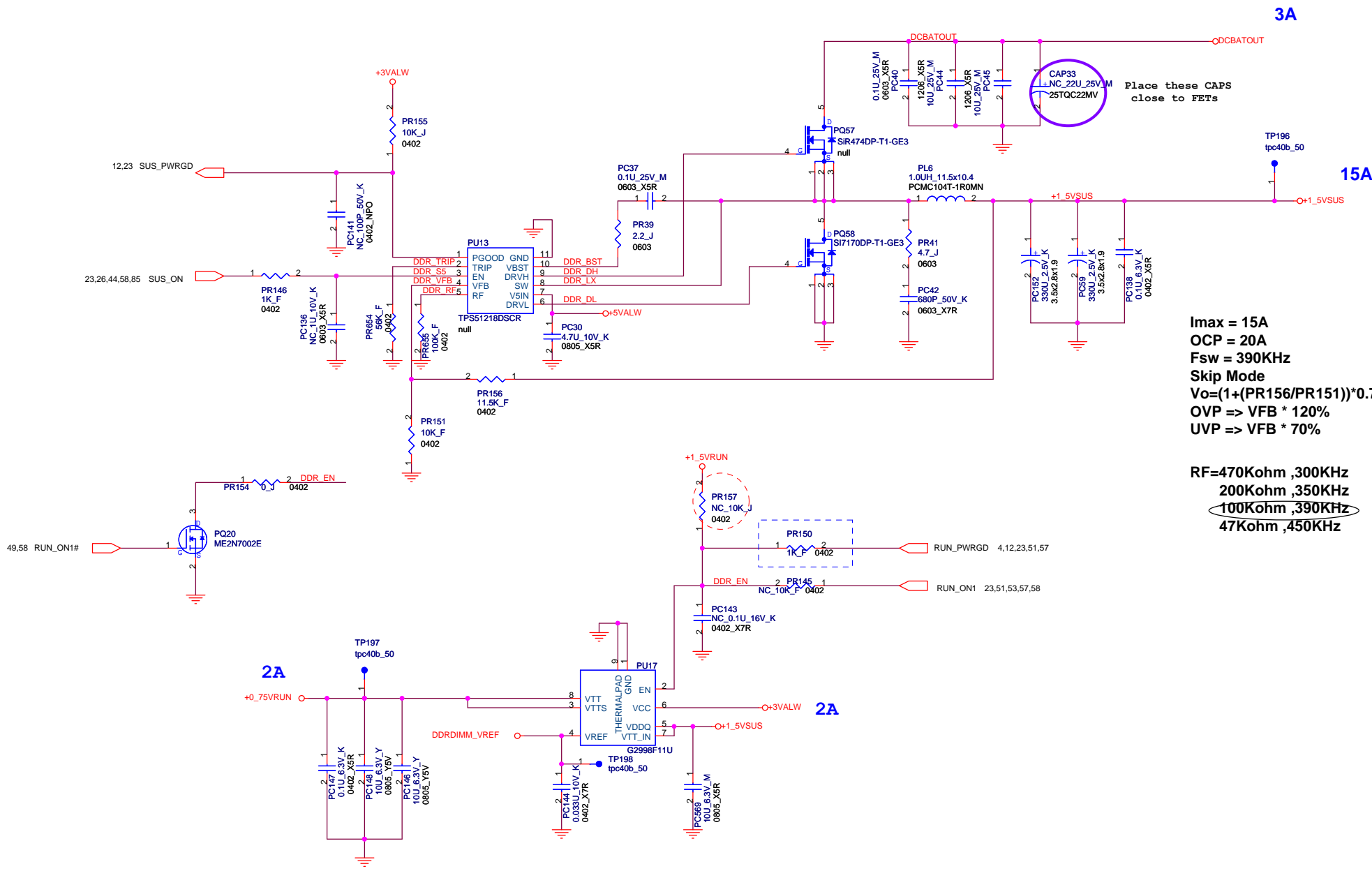
Rev: **SA**



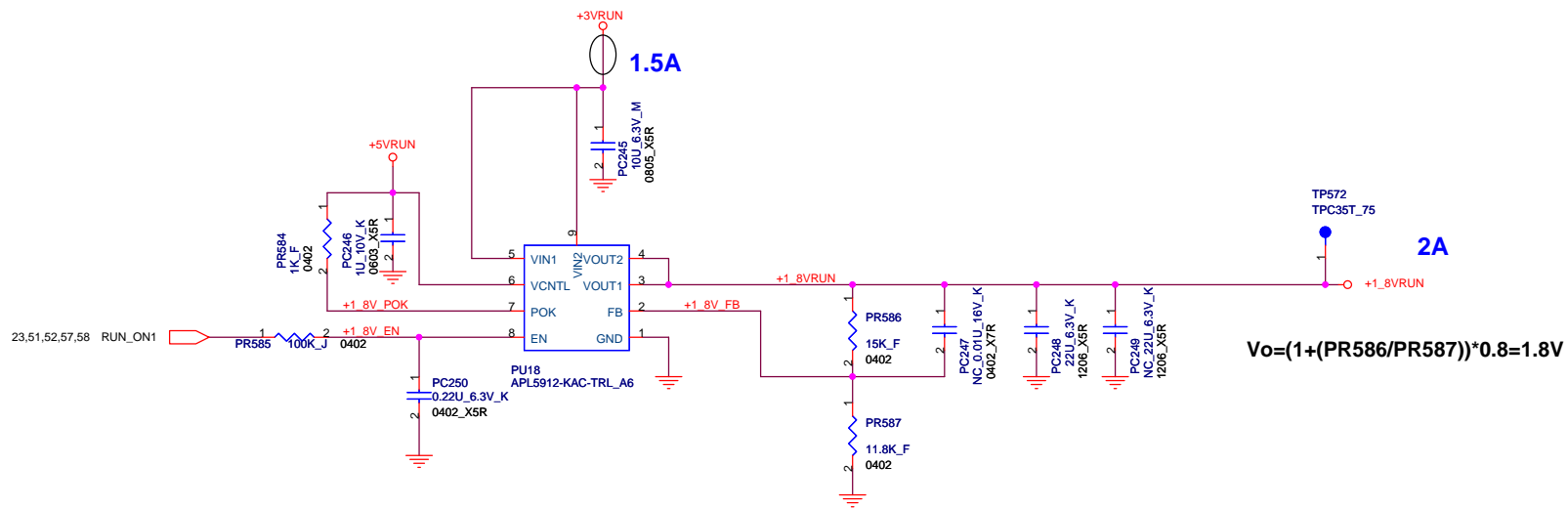
**Imax = 15A**  
**OCP = 20A**  
**Fsw = 300KHz**  
**Skip Mode**  
 $V_o = (1 + (PR187/PR208)) * 0.704 = 1.05V$   
 $V_o = (1 + (PR187/(PR208/PR590))) * 0.704 = 1.1V$   
**OVP => VFB \* 120%**  
**UVP => VFB \* 70%**  
**CF 0 1.1 V**  
**AR 1 1.05 V**

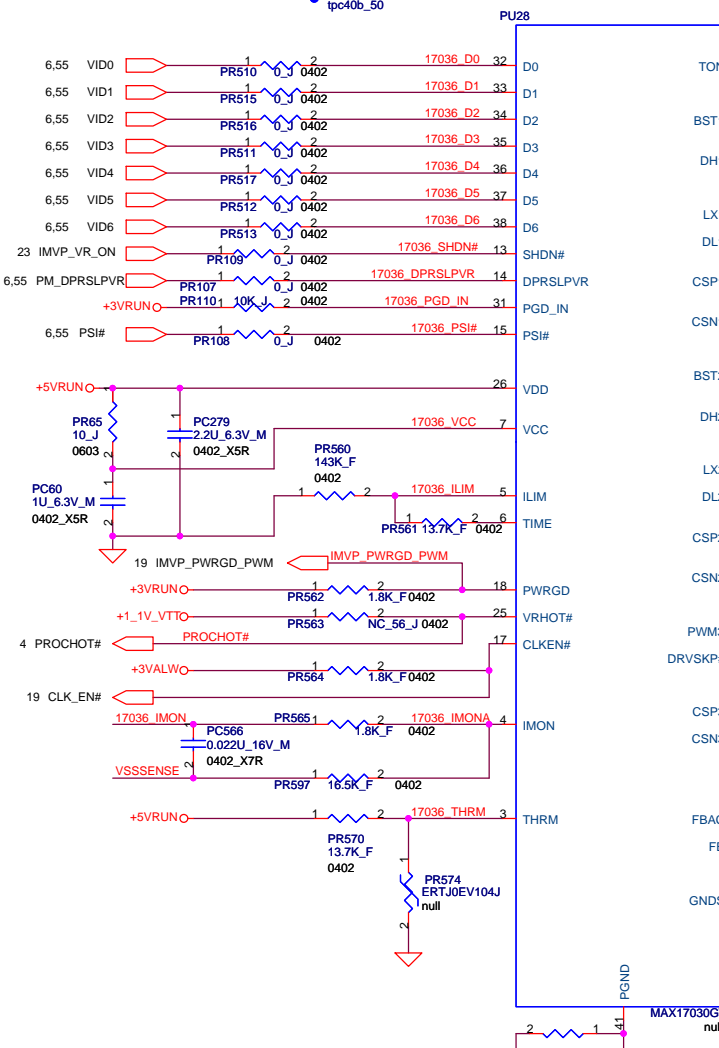
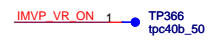
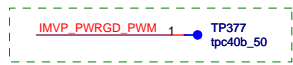
$RF = 470Kohm, 300KHz$   
 $200Kohm, 350KHz$   
 $100Kohm, 390KHz$   
 $47Kohm, 450KHz$

**Imax = 5A**  
**OCP = 7A**  
**Fsw = 300KHz**  
**Skip Mode**  
 $V_o = (1 + (PR505/PR506)) * 0.704 = 1.05V$   
**OVP => VFB \* 120%**  
**UVP => VFB \* 70%**

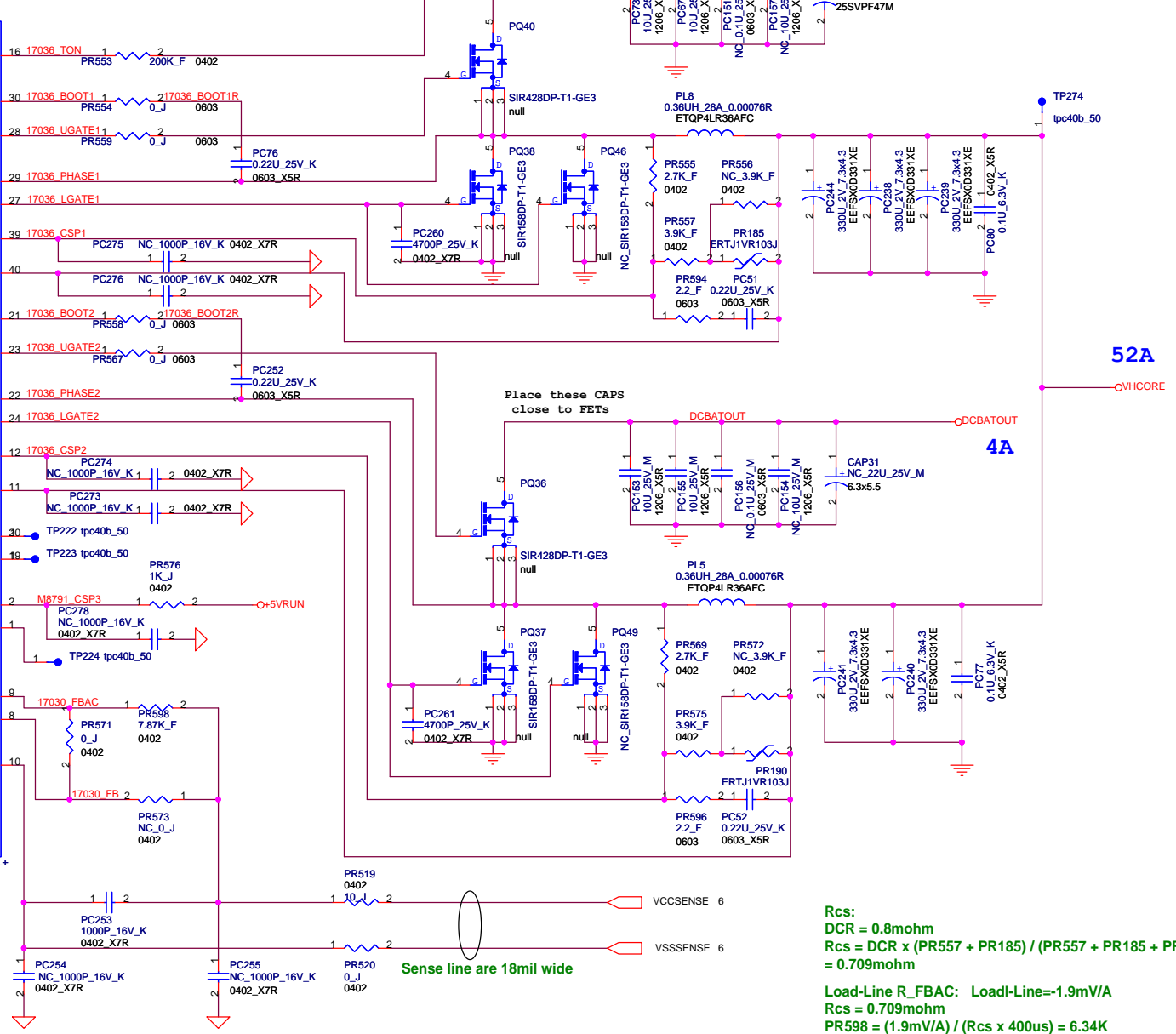
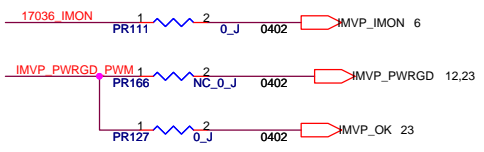


**3A**  
**15A**  
**Imax = 15A**  
**OCP = 20A**  
**Fsw = 390KHz**  
**Skip Mode**  
 $V_o = (1 + (PR156/PR151)) * 0.704 = 1.514V$   
**OVP => VFB \* 120%**  
**UVP => VFB \* 70%**  
**RF = 470Kohm, 300KHz**  
**200Kohm, 350KHz**  
**100Kohm, 390KHz**  
**47Kohm, 450KHz**





Valley current limit:  
 $V\_TIME\_LIM = 0.2 \times PR561 / (PR560 + PR561) = 20.2mV$   
 $I\_LIM = V\_TIME\_LIM / Rcs = 19A$



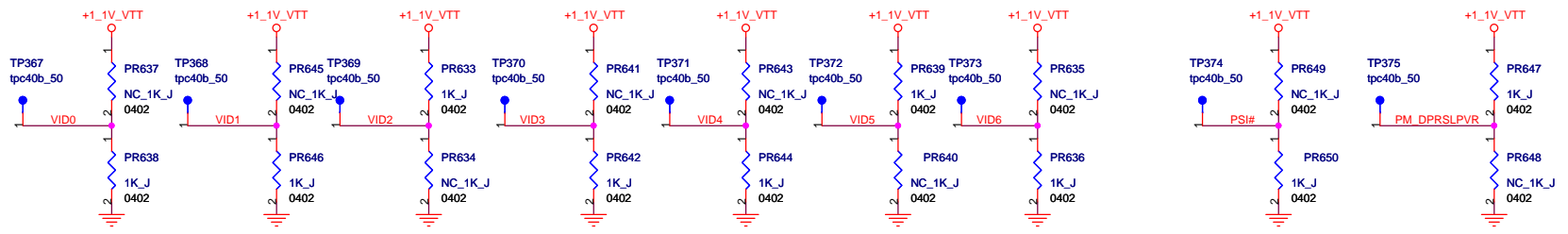
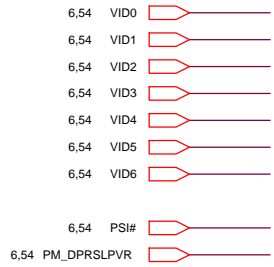
Sense line are 18mil wide

Rcs:  
 $DCR = 0.8mohm$   
 $Rcs = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm$   
 Load-Line R\_FBAC: Load-Line=-1.9mV/A  
 $Rcs = 0.709mohm$   
 $PR598 = (1.9mV/A) / (Rcs \times 400us) = 6.34K$

Default value of VID [6:0] = [ 0100100] , PSI# = 0 , PROC\_DPRSLPVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)

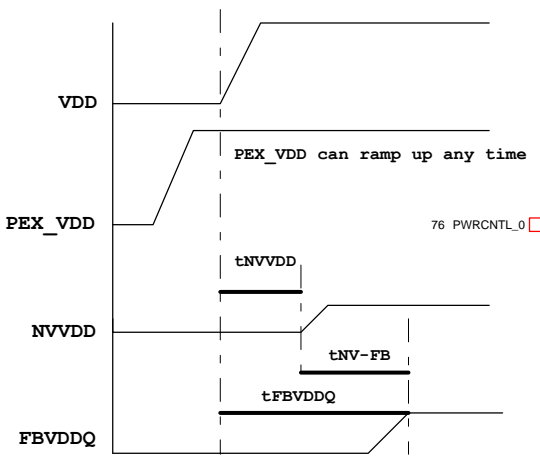
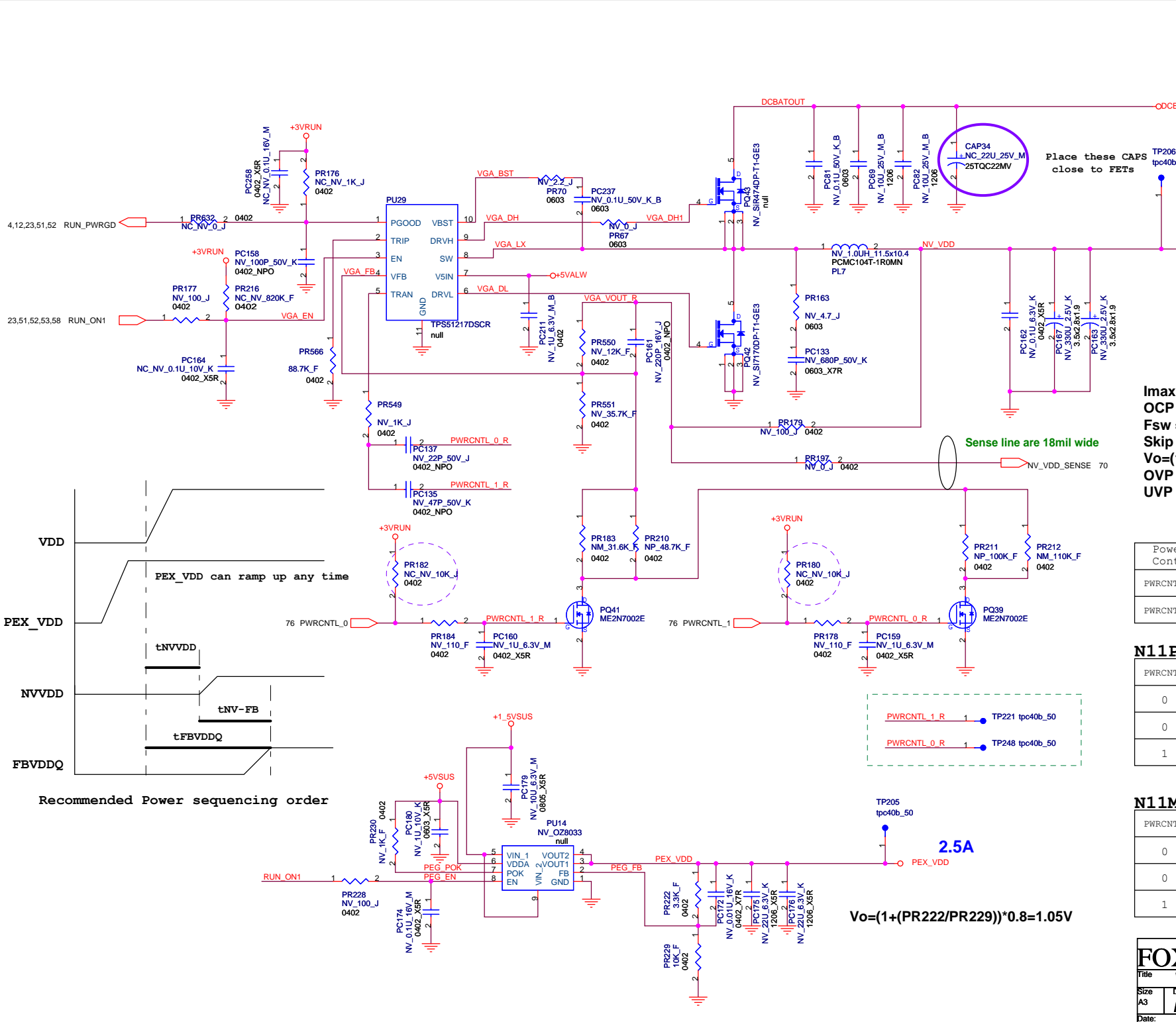
- 416056\_416056\_Ard\_EDS\_Rev.1.1
- 403779\_Clarksfield\_MPG\_Rev1.5



Delete iGPU Path on DVT for Cost Down

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>VGFX Power GFXCORE</b>			
Size A3	Document Number <b>M931 (MBX-215)</b>	Date: Wednesday, January 06, 2010	Rev <b>SA</b>
Sheet 56 of 93		1	





Recommended Power sequencing order

**Imax = 15A**  
**OCp = 20A**  
**Fsw = 400KHz**  
**Skip Mode**  
 $V_o = (1 + (PR550 / (PR551 / PR210))) * 0.6$   
**OVP => VFB \* 120%**  
**UVP => VFB \* 70%**

Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

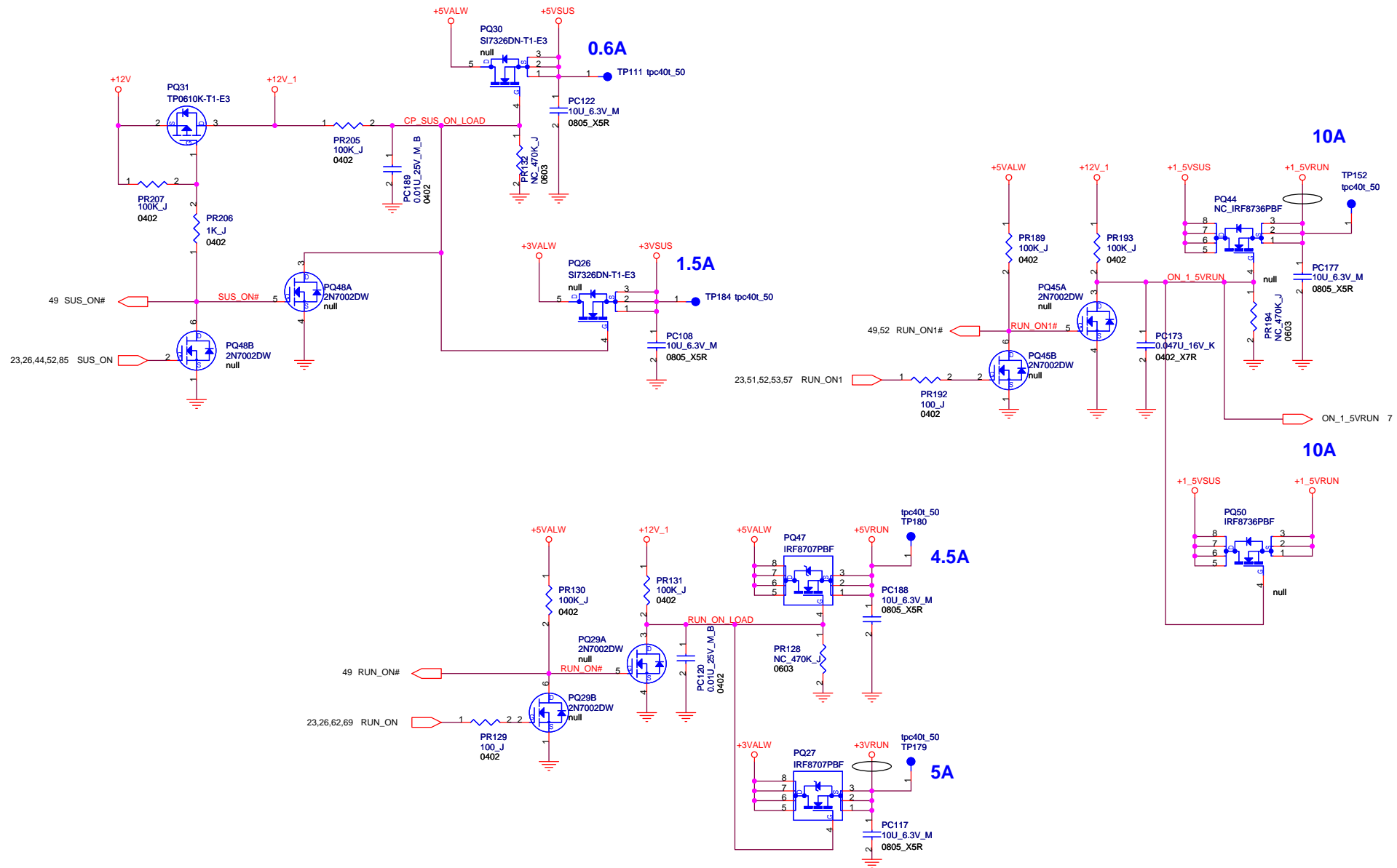
**N11P-GE1**

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.8V (P12)
0	1	0.85V (P8)
1	0	0.95V (P0)

**N11M-GE1**

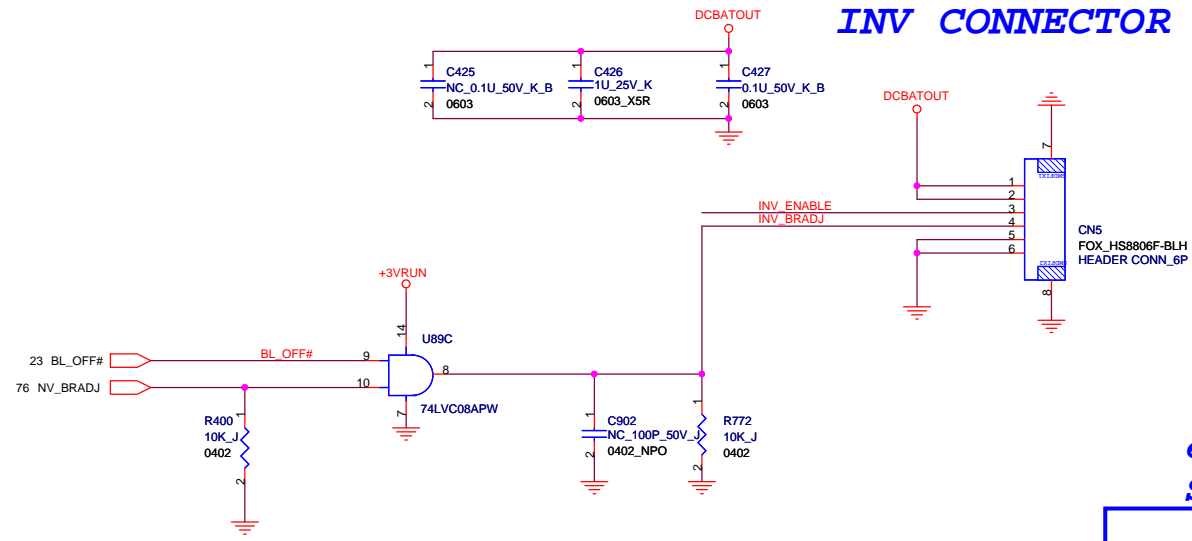
PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	1	0.85V (P12)
0	1	0.85V (P8)
1	0	1.03V (P0)

$V_o = (1 + (PR222 / PR229)) * 0.8 = 1.05V$

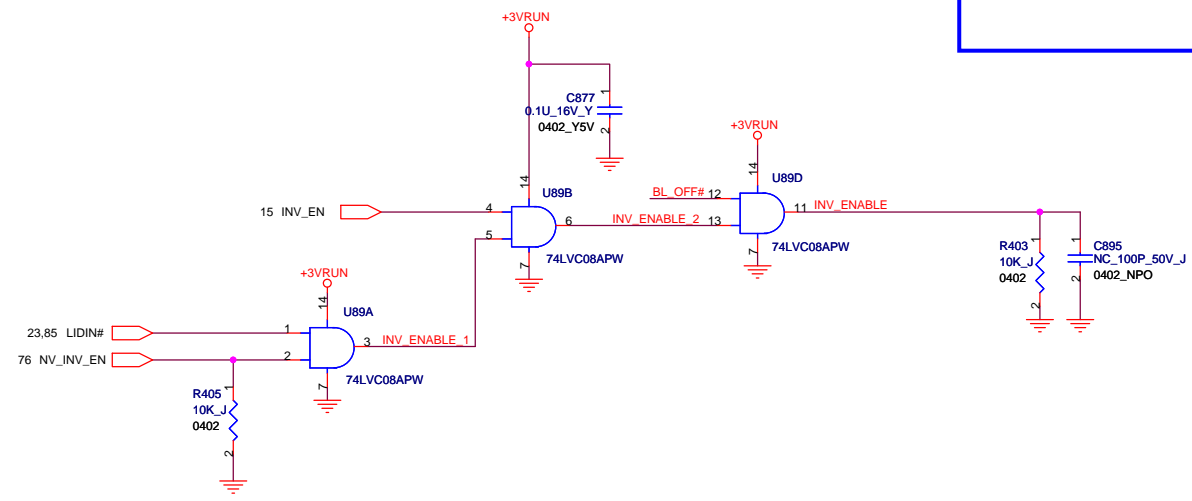
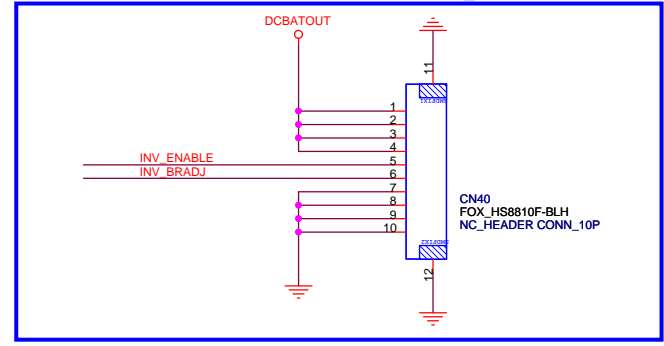




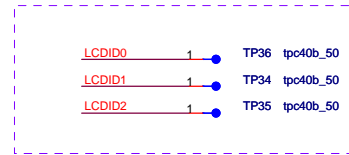
# INV CONNECTOR



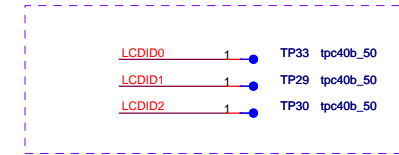
*eDP (Suzaku3 support) >>  
Stuff CN40 , Dummy CN5*



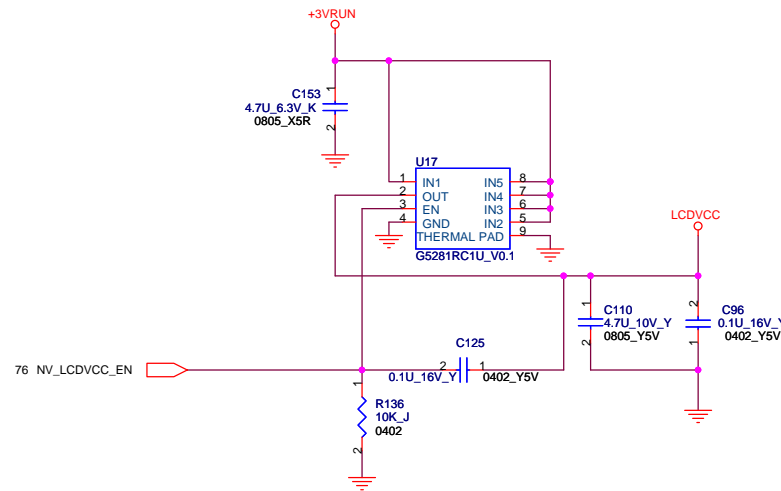
Bot-Side



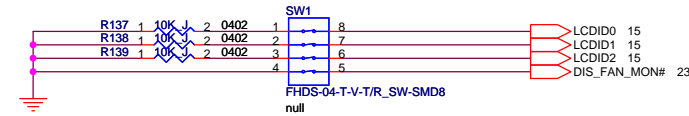
Top-Side



### LCDVCC Power

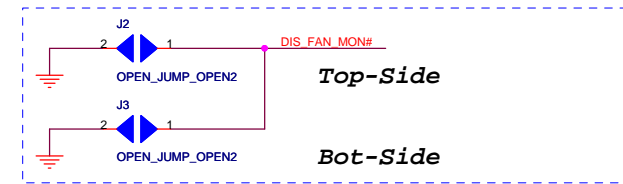


### PANEL ID

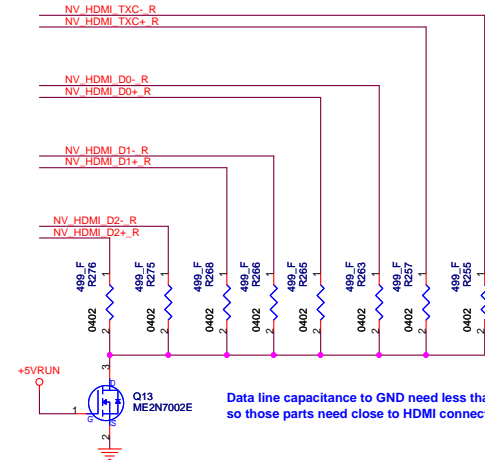
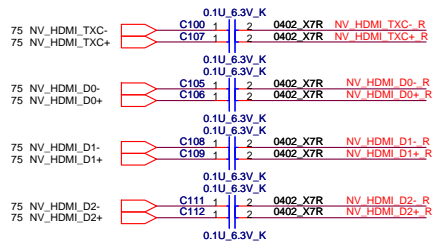


SW1 (Panel ID)	LCDID2	LCDID1	LCDID0	FAN Lock
CRT (No LCD)	0	0	0	ON: Disable OFF: Enable
EW1 (Sharp)	0	0	1	
RESERVED	0	1	0	
EW1 (LGD)	0	1	1	
EW3 (Sharp)	1	0	0	
RESERVED	1	1	0	
RESERVED	1	1	1	

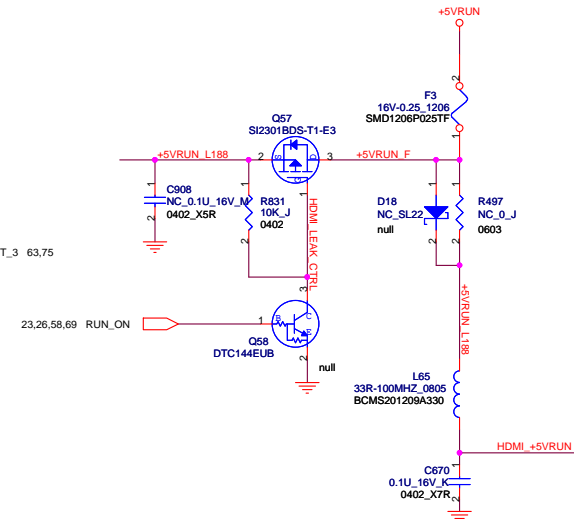
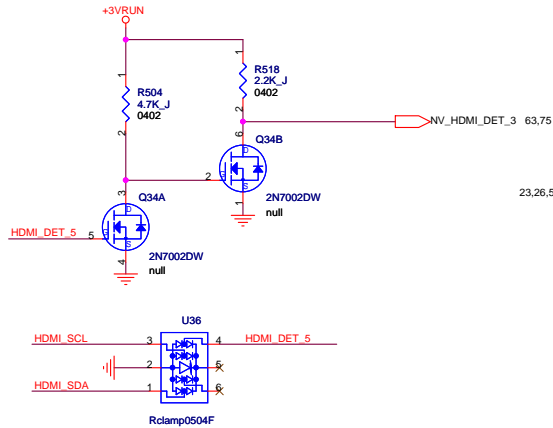
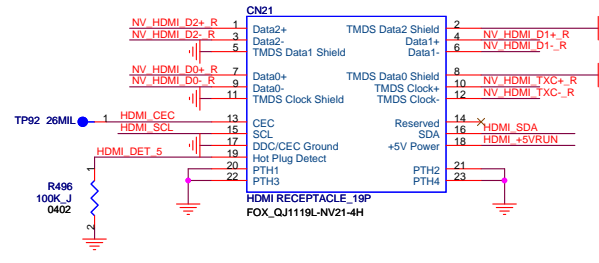
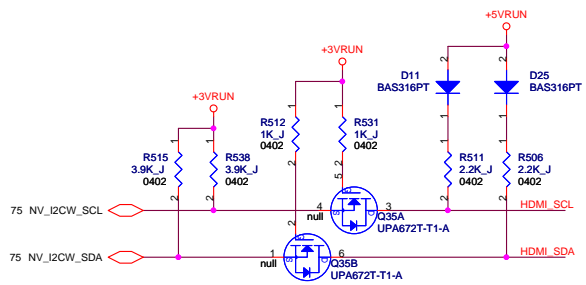
ON:0 , OFF:1

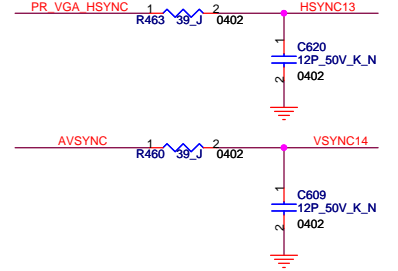
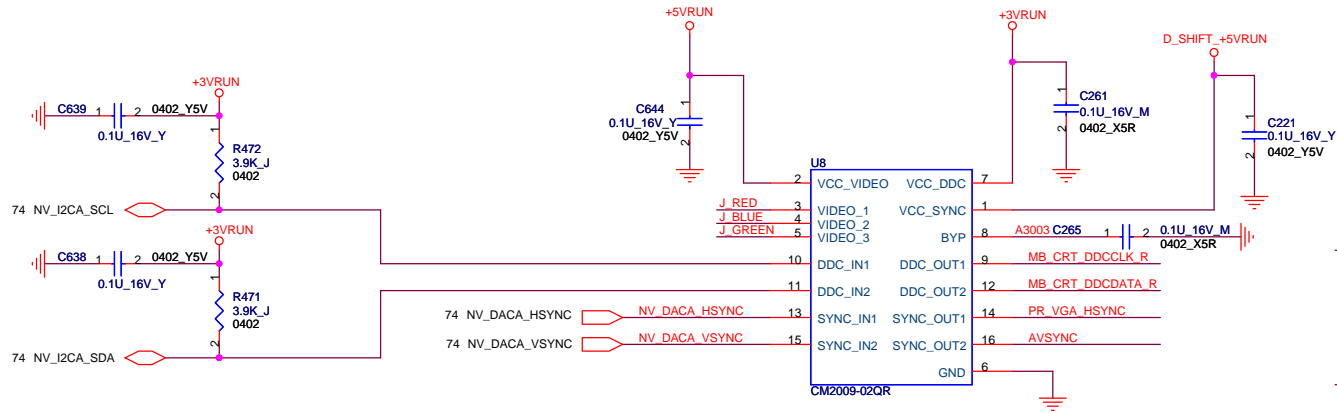


DIS\_FAN\_MON# for L6 BFT Test

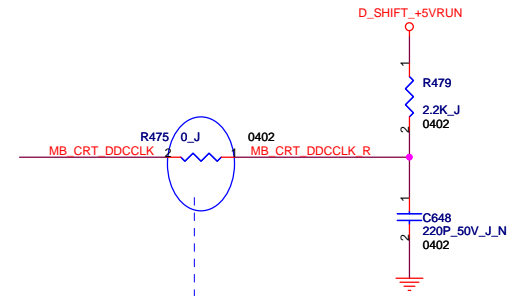
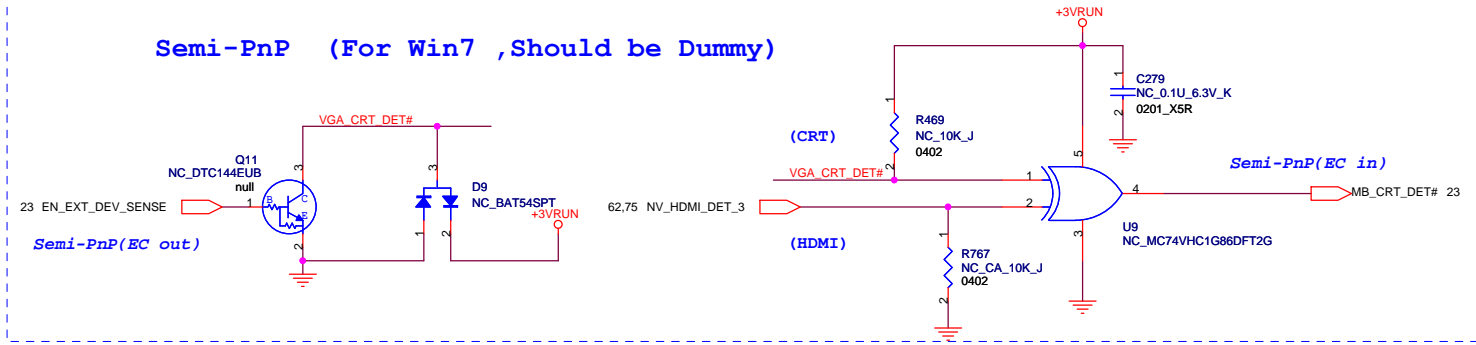


Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

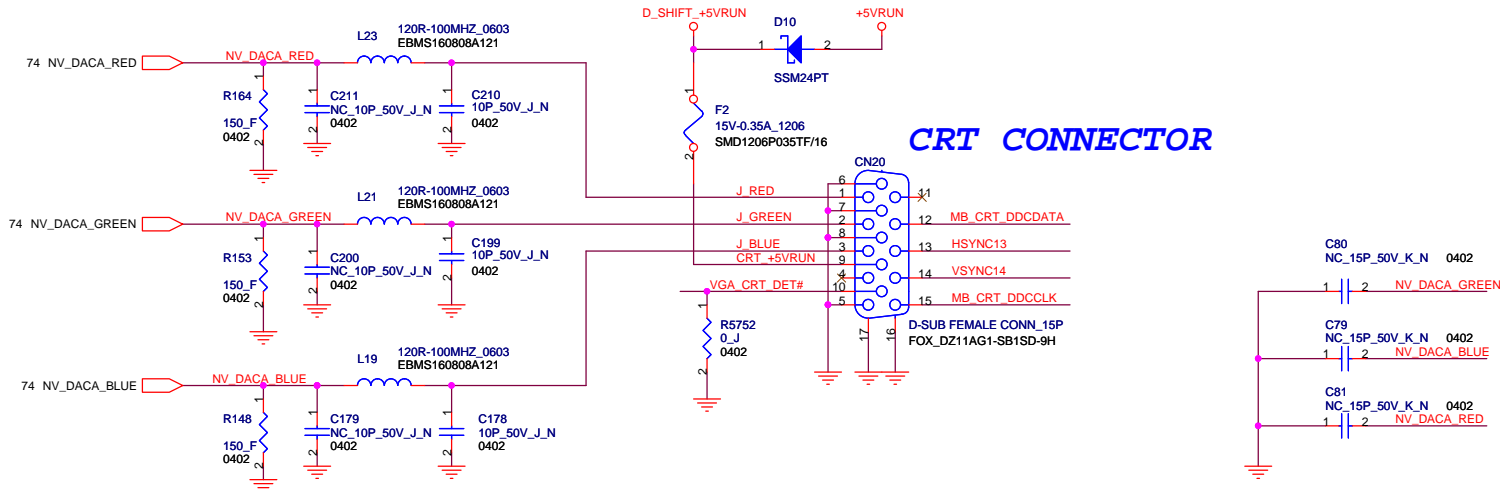
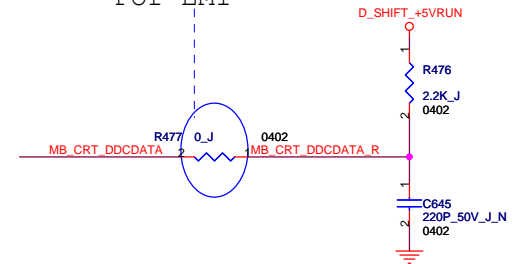




**Semi-PnP (For Win7 ,Should be Dummy)**



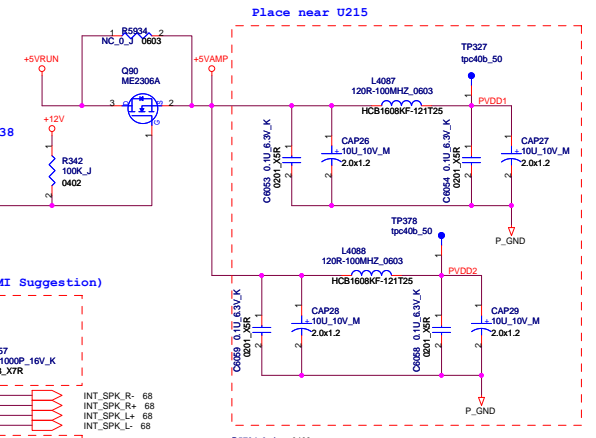
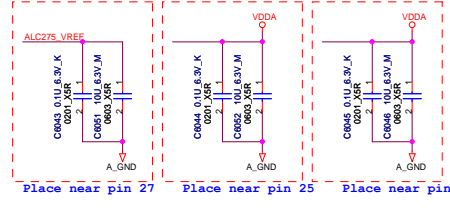
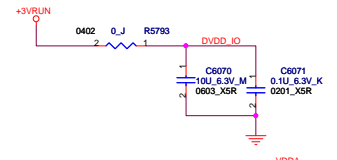
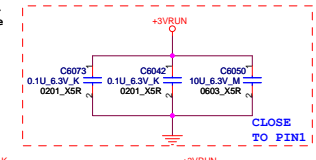
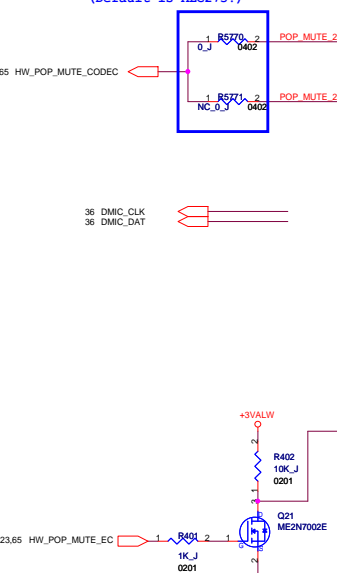
For EMI



**CRT CONNECTOR**

DVDD\_IO can be either 1.5V or 3.3V Resume wall power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.

BOM Option for ALC275 and ALC269 (Default is ALC275.)



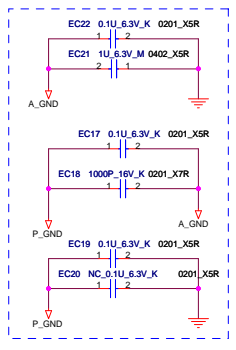
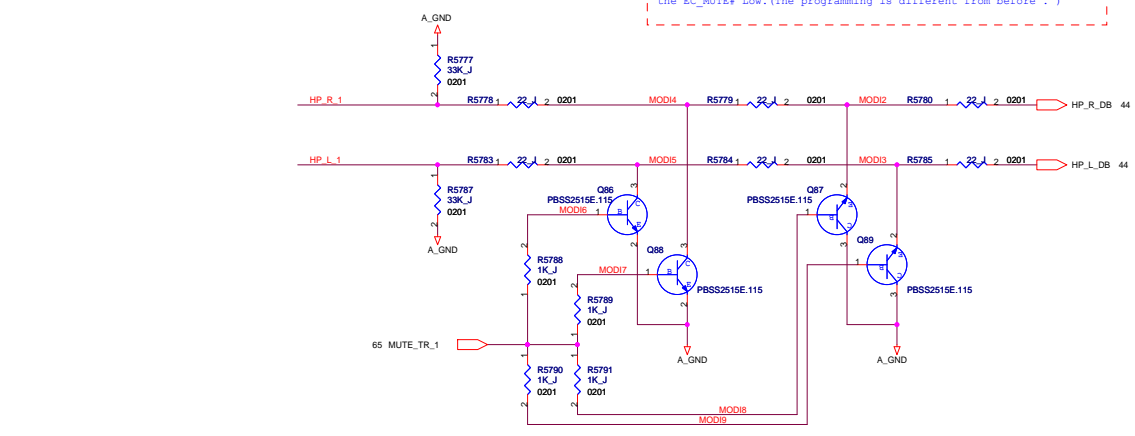
Place near JSFK1. (EMI Suggestion)

Place near JSFK1. (EMI Suggestion)

Place at one point only under the ALC275 or near the ALC275

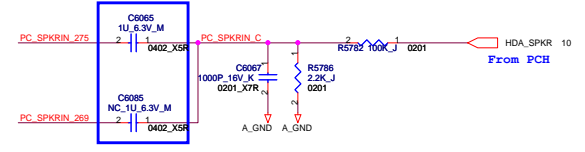
<<Attention>>  
For power on/off de-pop circuit and system booting warning signal! Please System BIOS Engineer Note :  
1. If you want the system make warning signal after power on , please let EC\_MUTE# High first.  
2. When you want to exit your Bios Programming Code, please let the EC\_MUTE# Low. (The programming is different from before .)

BOM Option for ALC275 and ALC269 (Default is ALC275.)

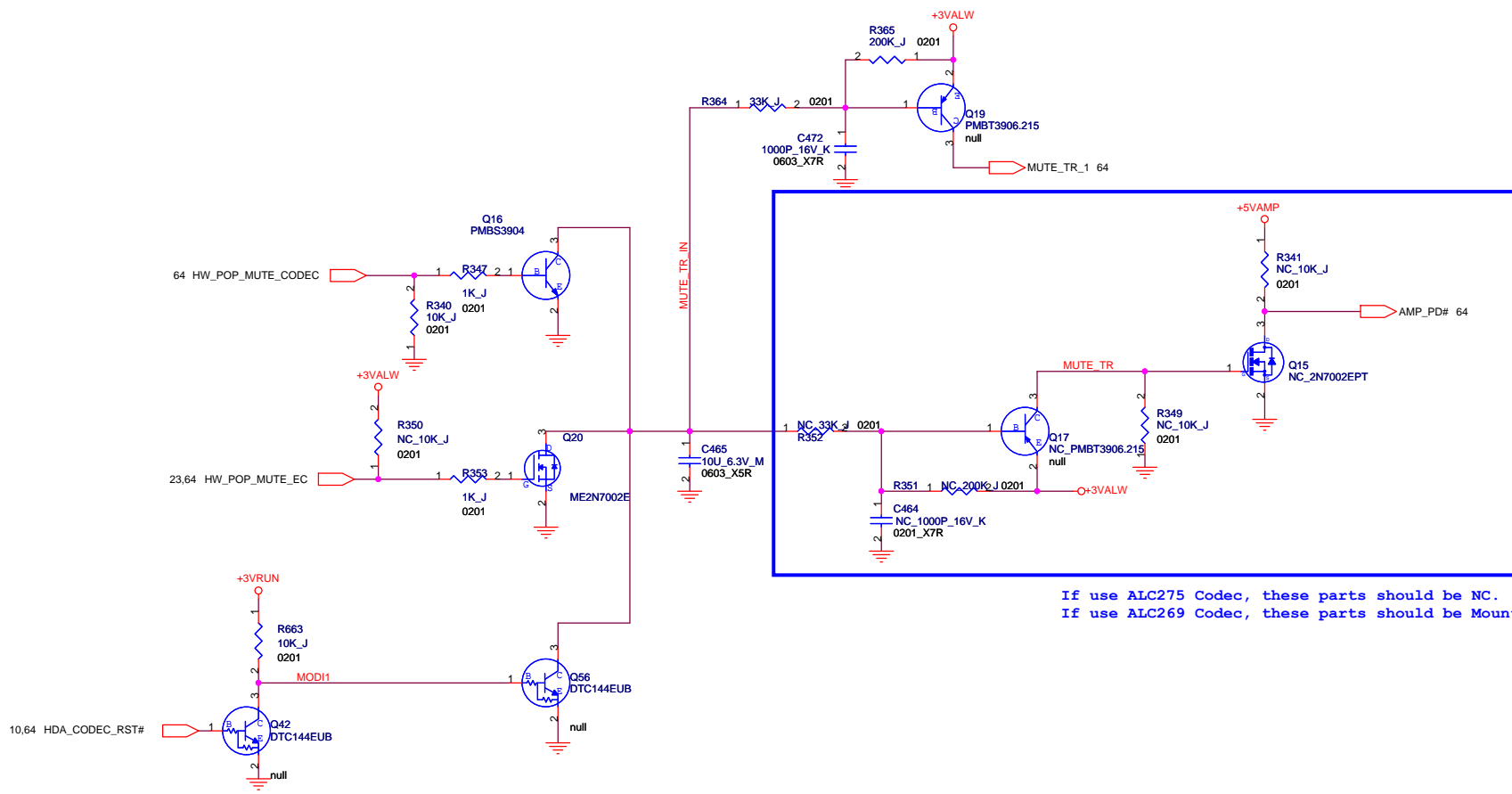


BOM Option for ALC275 and ALC269 (Default is ALC275.)

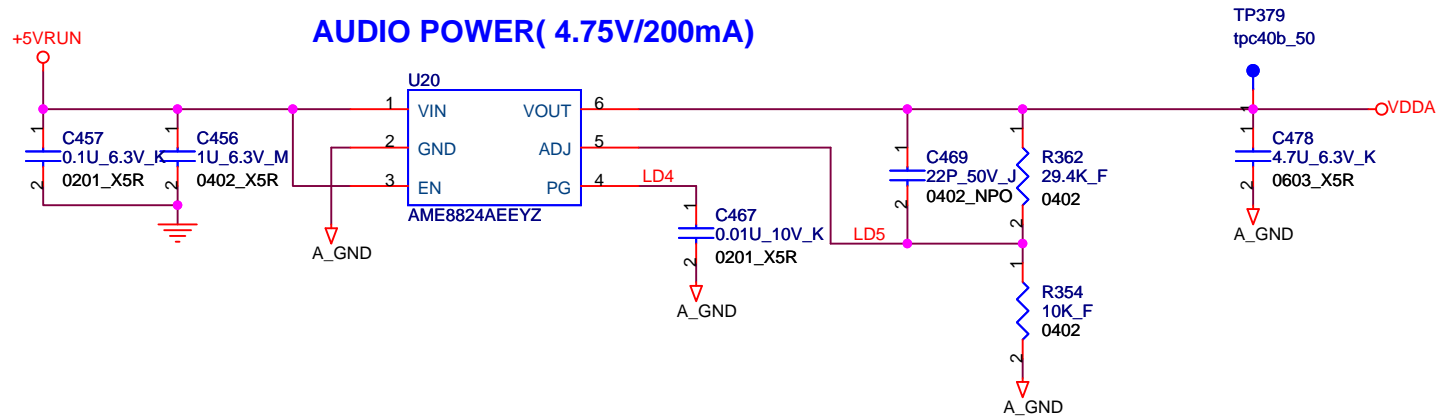
PC BEEP







If use ALC275 Codec, these parts should be NC.  
 If use ALC269 Codec, these parts should be Mount.

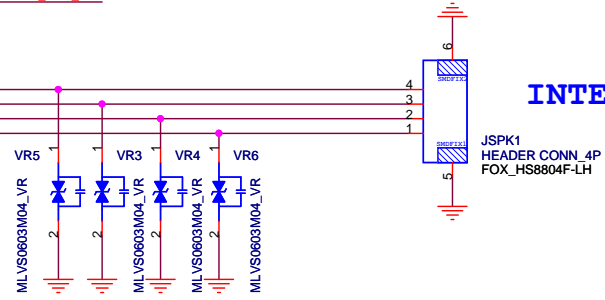


Delete Class D Amp. when implemented ALC275.

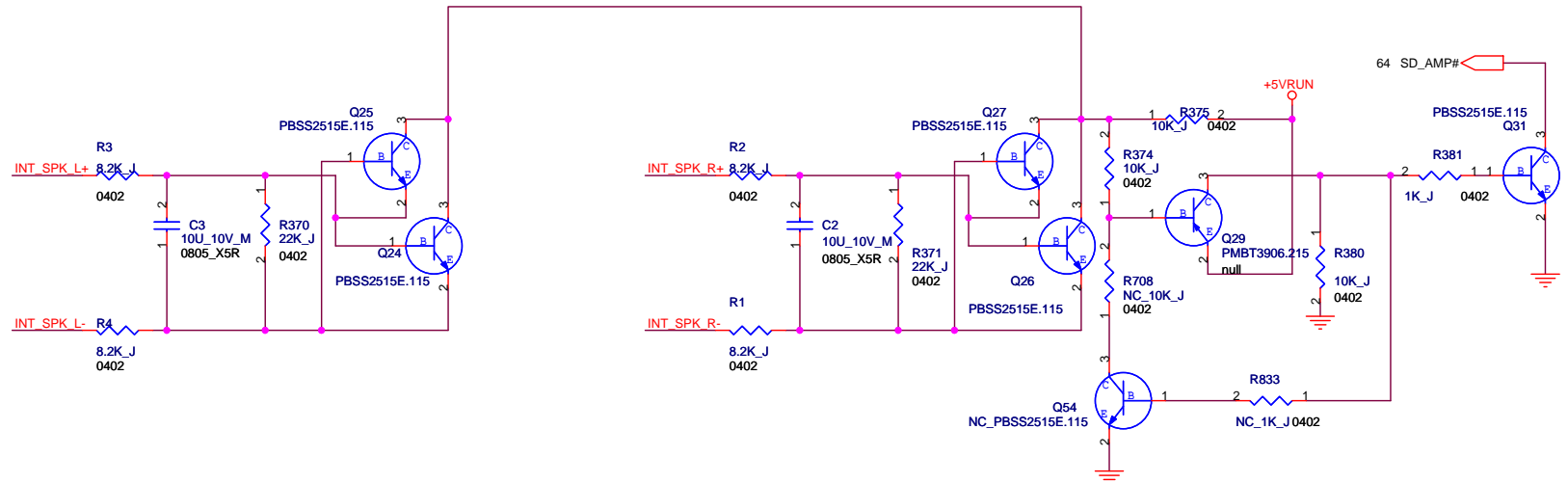
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title		<b>AUDIO SPEAKER AMP</b>	
Size	Document Number	Rev	
A3	<b>M931 (MBX-215)</b>	<b>SA</b>	
Date:	Wednesday, January 06, 2010	Sheet	67 of 93

- TP114 tpc40t\_50 1 INT\_SPK L+
- TP117 tpc40t\_50 1 INT\_SPK L-
- TP116 tpc40t\_50 1 INT\_SPK R+
- TP115 tpc40t\_50 1 INT\_SPK R-

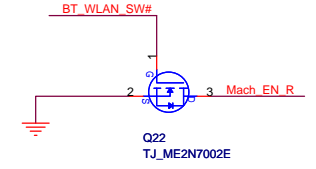
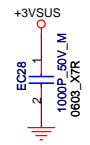
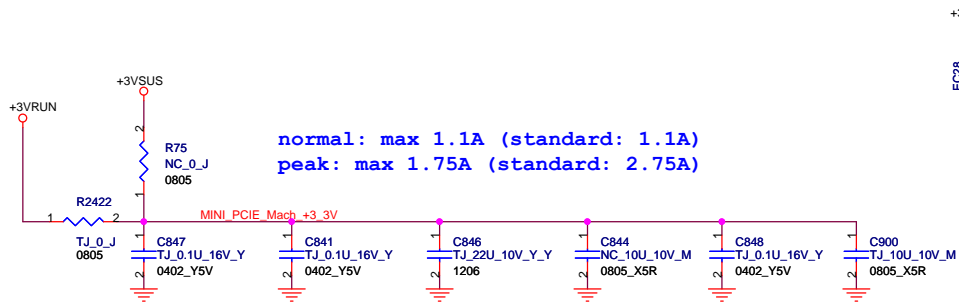
- 64 INT\_SPK L+ INT\_SPK L+
- 64 INT\_SPK L- INT\_SPK L-
- 64 INT\_SPK R+ INT\_SPK R+
- 64 INT\_SPK R- INT\_SPK R-



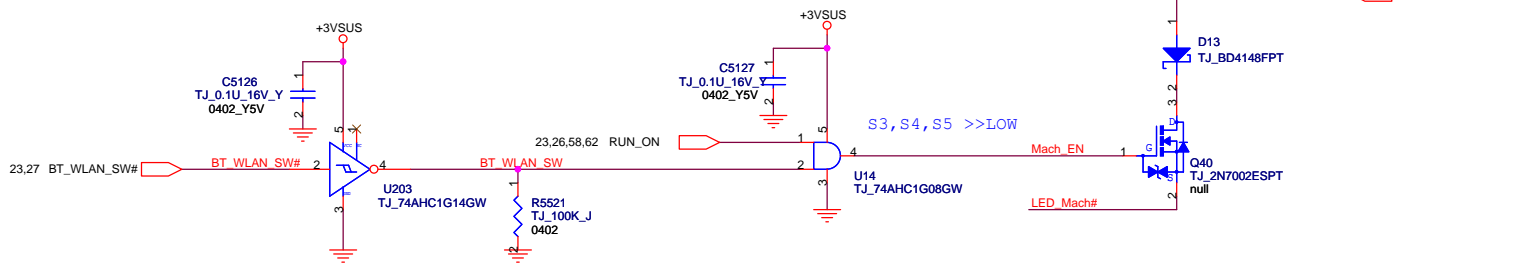
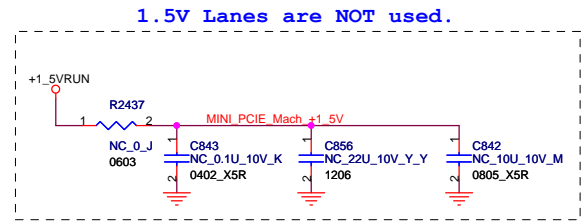
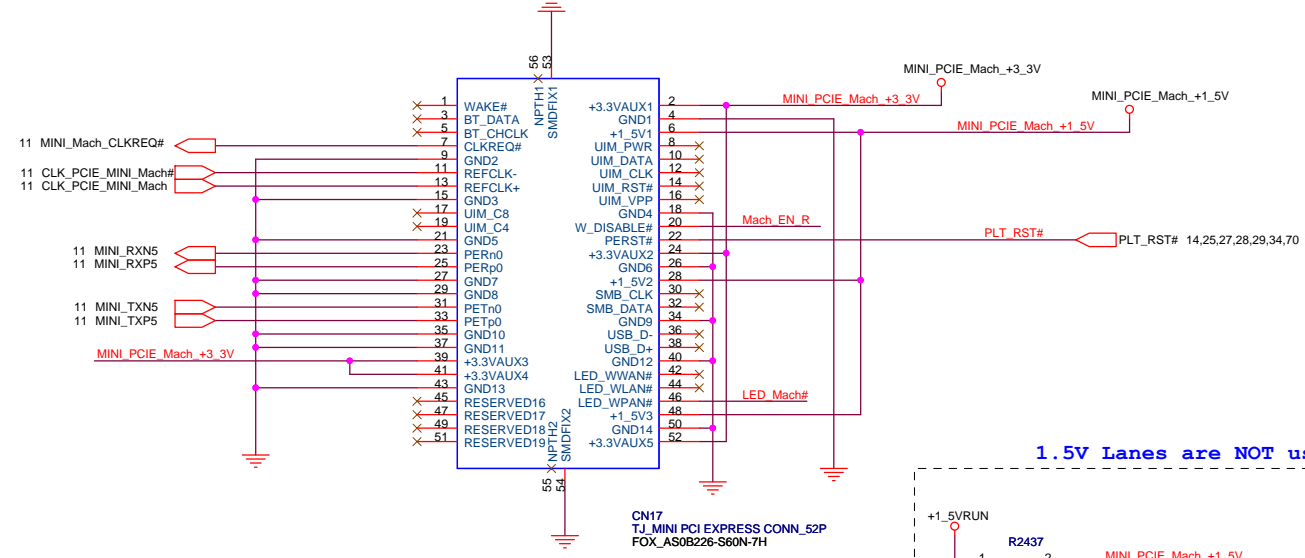
For Shut-down Codec Amp. power (PVDD1 and PVDD2)

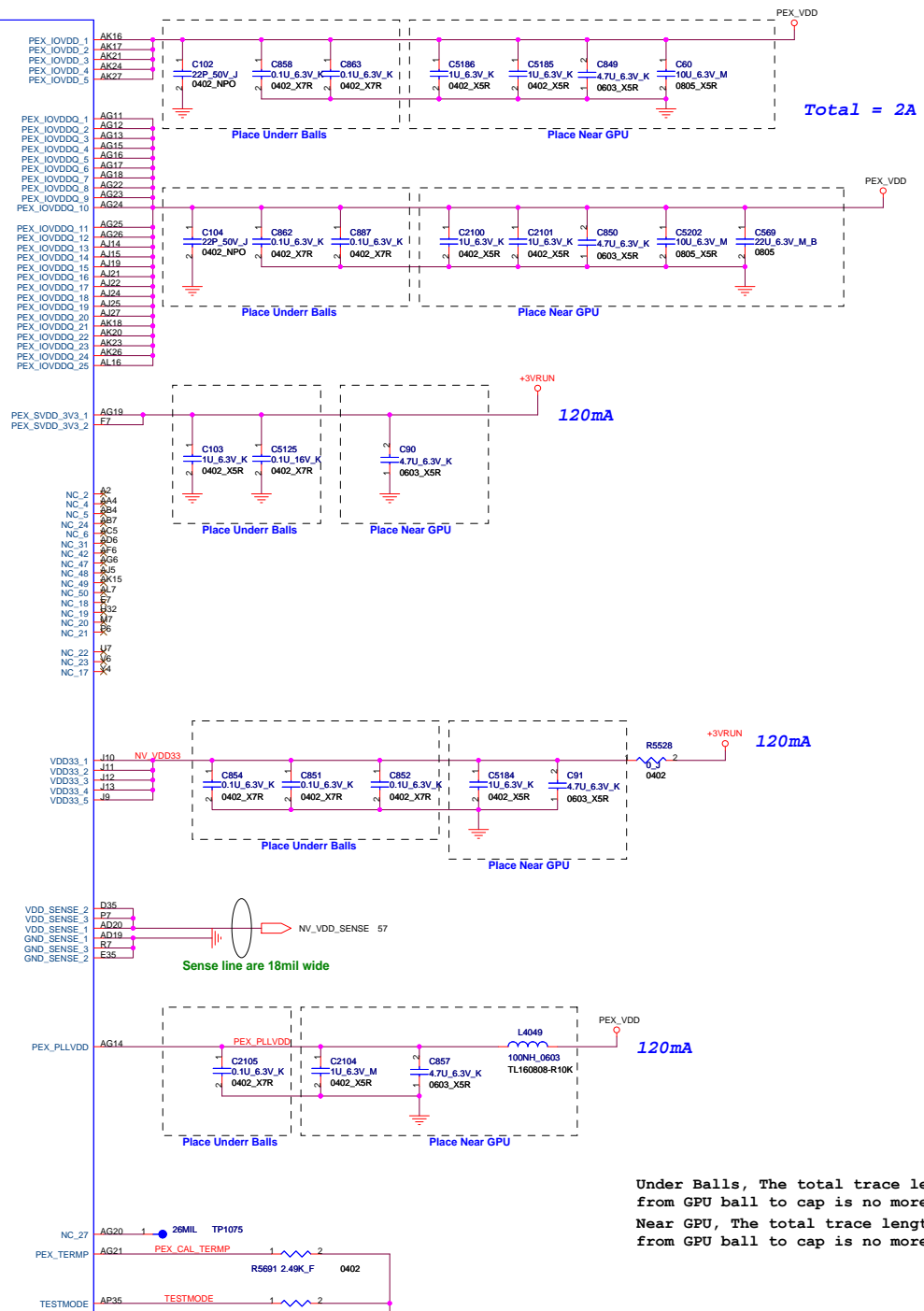
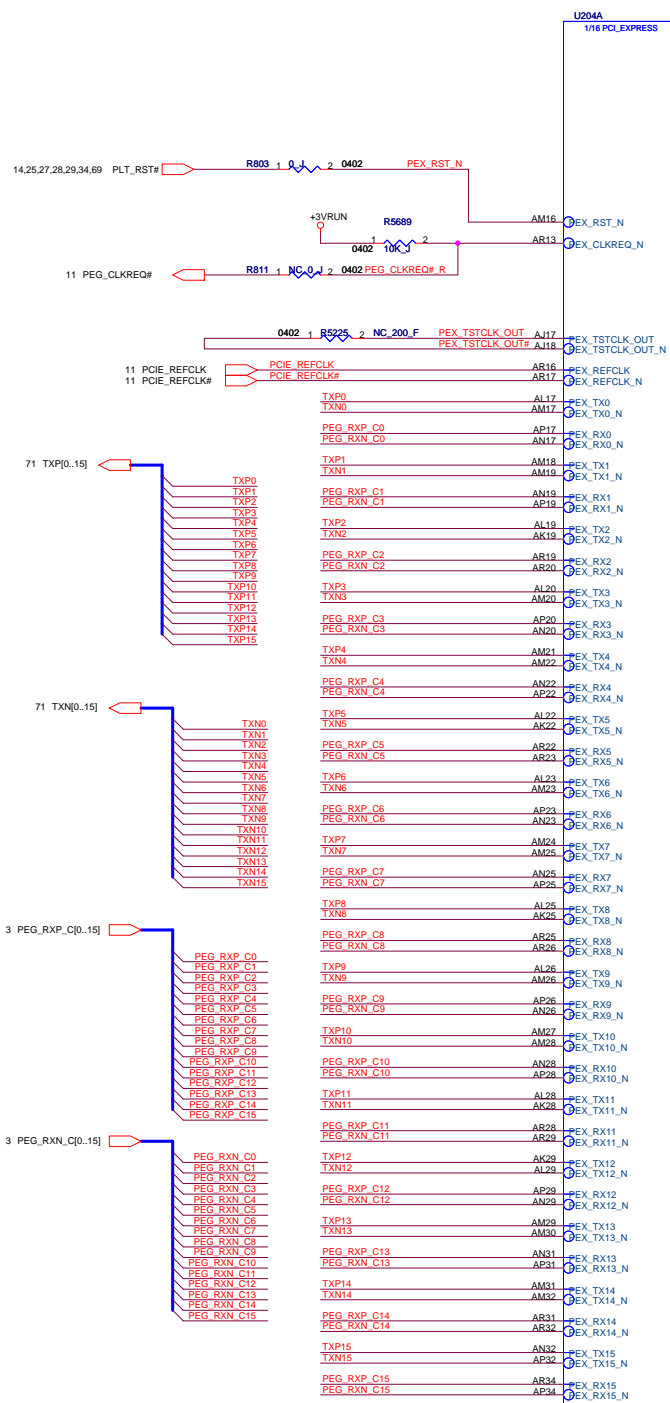


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Title</b> <b>AUDIO SPEAKER CONNECTOR</b>			
Size	Document Number		Rev
B	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	68 of 93



### Mach CONN





Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.  
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

File	VGA (PCI-E) 1/9		Rev
Size	Document Number		
Custom	M931 (MBX-215)		SA
Date:	Wednesday, January 06, 2010	Sheet	70 of 93



```

XCLK_417
0 (27M Hz)
1 (Reserved)
FB_0_BAR_SIZE
0 256MB
1 (Reserved)
SMB_ALT_ADDR
0 0x9E
1 0x9C(multi-GPU usage)
VGA_DEVICE
0 3D device(class code 302h)
1 VGA device(class code 300h)

SUB_VENDOR
0 (No vedio BIOS ROM)
1 (BIOS ROM is present)

SLOT_CLK_CFG
0 (GPU and MCH not share
a common reference clk)
1 (GPU and MCH share a
common reference clk)

PEX_PLL_EN_TERM
0 (Disable)
1 (Enable)

USER[3:0]
1000

N10x/N11x 3GIO_PADCFG[3:0]
0110

N11x PCI_DEVID[3:0]
N11P-GE1 1001b
N11M-GE1 0101b
PCI DEVICE IDs
N11P-GE1 (0x0A29)
N11M-GE1 (0x0A75)

ROM_SO
0001

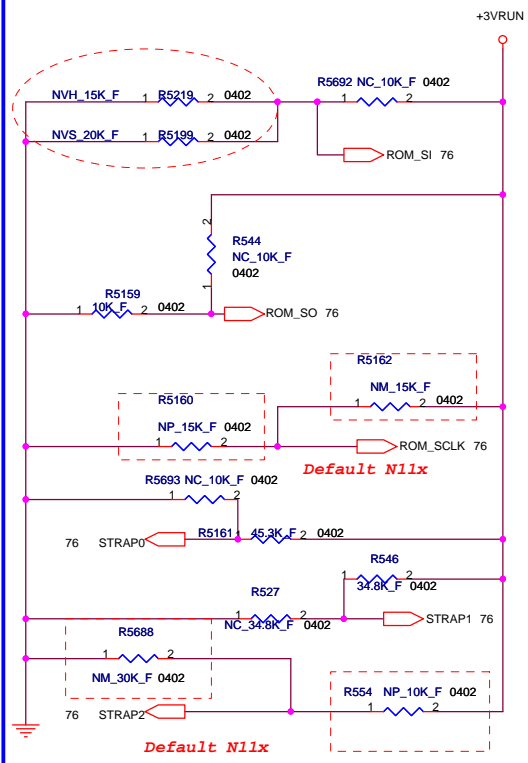
ROM_SCLK
N11P-GE1
0010
N11M-GE1
1010

STRAP0
(1111)

STRAP1
(1110)

Strap2
N11P-GE1
1001
N11M-GE1
0101

```



```

ROM_SI
0000 64-bit Reserved
0010 64Mx16 DDR3 - 96 ball 128-bit Hynix(13-H5T01G6-3000) 15K Pull Low.
0011 64Mx16 DDR3 - 96 ball 128-bit Samsung(13-K4W1G16-3000) 20K pull Low

```

**Logical Strap bit Mapping**

Resistor values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

**Strap Options**

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	BGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

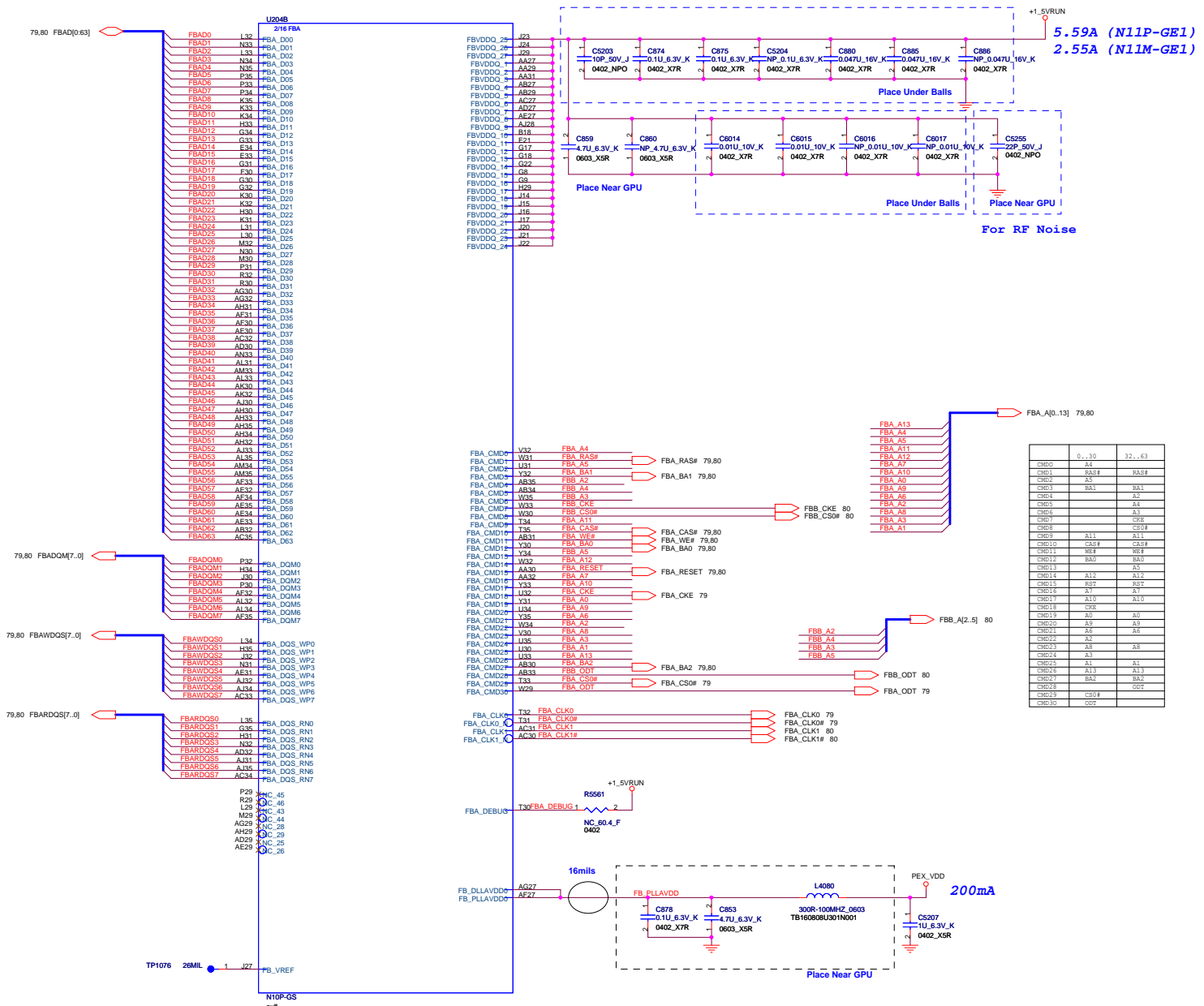
Refer to <GB1 Family Design Guide DG-04202-001\_v02\_secured>

**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title: **VGA (PCI-E BUS)Strap 2/9**

Size: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: \_\_\_\_\_  
 Custom: **M931 (MBX-215)** SA

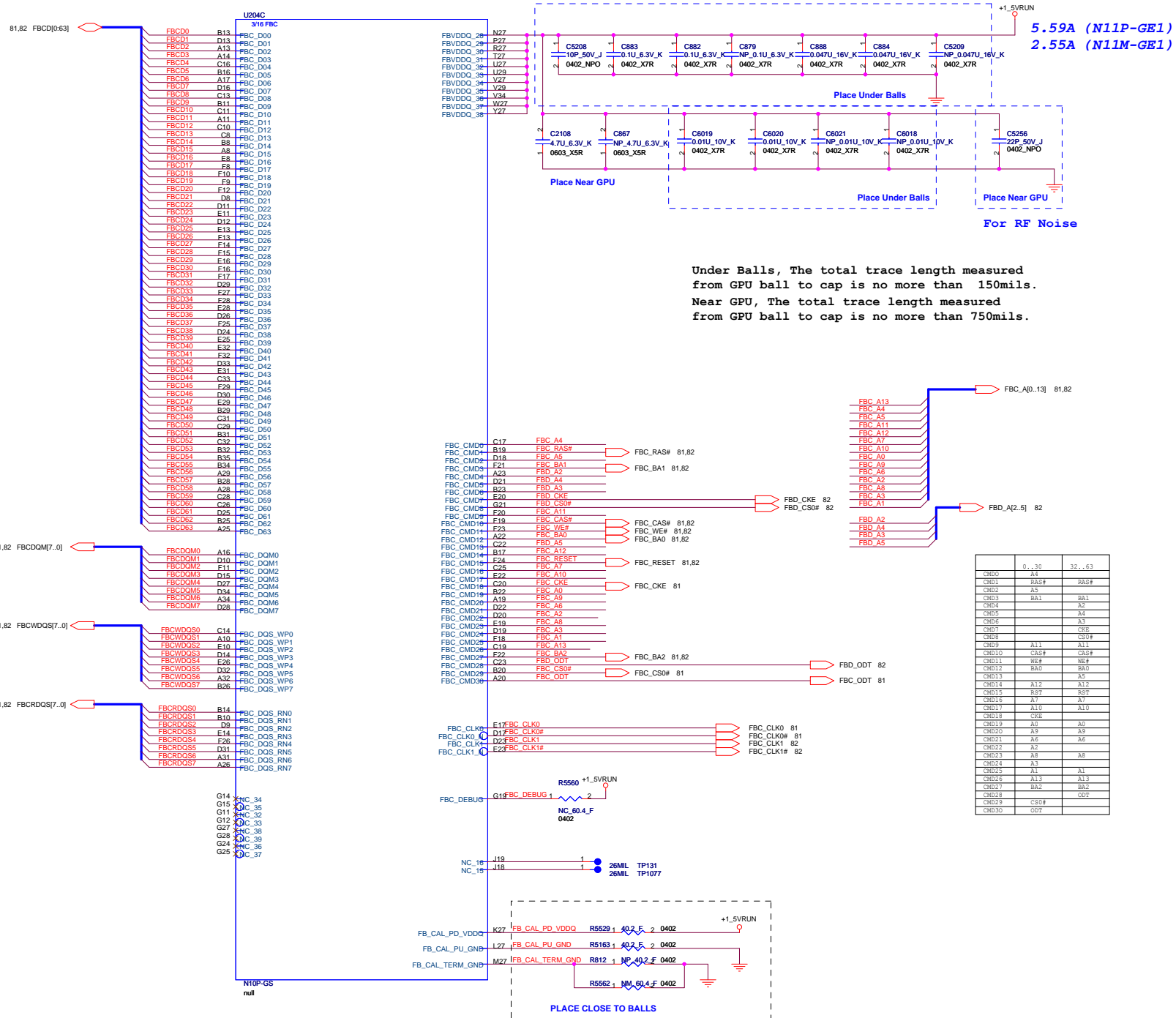
Date: Wednesday, January 06, 2010 Sheet 71 of 93



CM00	6..30	32..63
CM01	BA#	BA#
CM02	A5	BA1
CM03	BA1	A2
CM04	A2	A3
CM05	A3	CM06
CM06	CM07	CM08
CM07	CM08	CM09
CM08	CM09	CM10
CM09	CM10	CM11
CM10	CM11	CM12
CM11	CM12	CM13
CM12	CM13	CM14
CM13	CM14	CM15
CM14	CM15	CM16
CM15	CM16	CM17
CM16	CM17	CM18
CM17	CM18	CM19
CM18	CM19	CM20
CM19	CM20	CM21
CM20	CM21	CM22
CM21	CM22	CM23
CM22	CM23	CM24
CM23	CM24	CM25
CM24	CM25	CM26
CM25	CM26	CM27
CM26	CM27	CM28
CM27	CM28	CM29
CM28	CM29	CM30
CM29	CM30	CM31
CM30	CM31	CM32

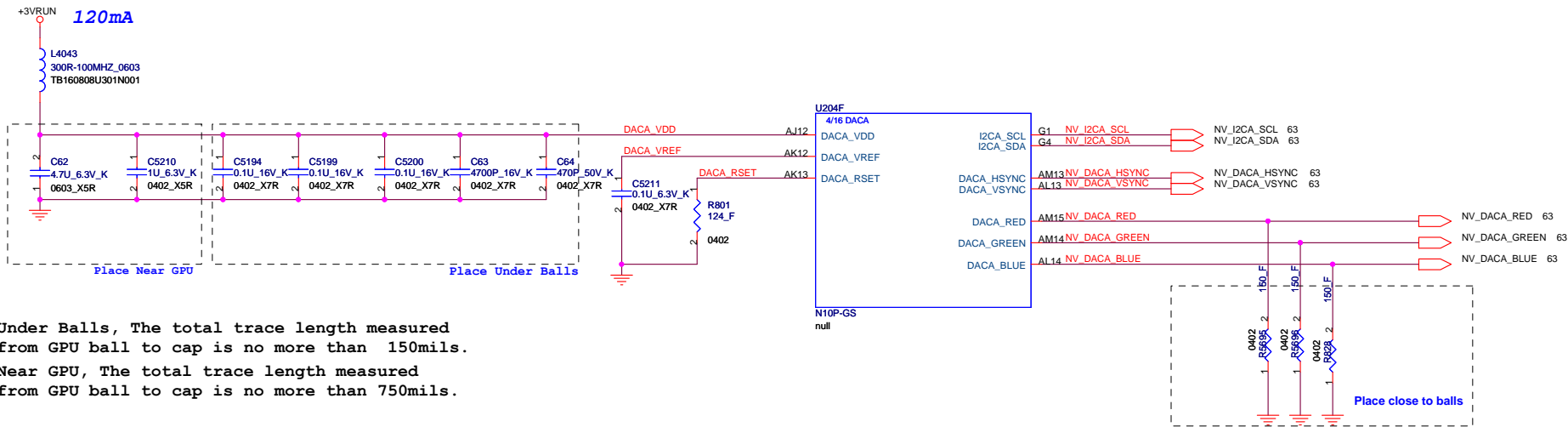
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.  
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.



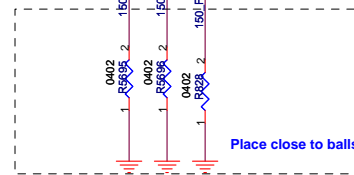


Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.  
 Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

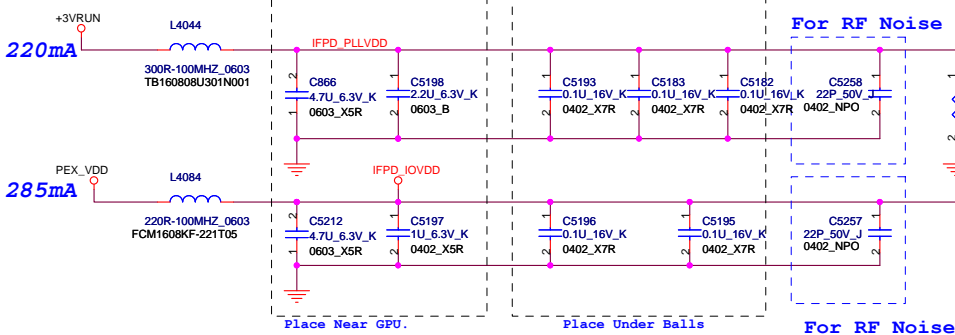
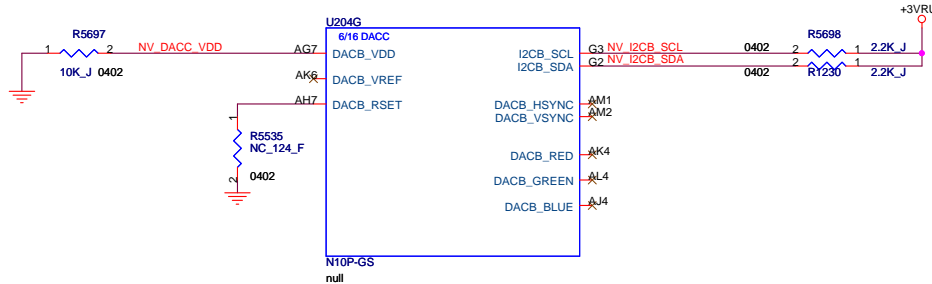
CMD0	0..30	32..63
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4	A2	
CMD5	A4	
CMD6	A3	
CMD7	CKE	
CMD8	CS0#	
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	
CMD14	A12	A12
CMD15	RS#	RS#
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A8	A8
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	BA2	BA2
CMD29	CS0#	CS0#
CMD30	ODT	



Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.  
 Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.



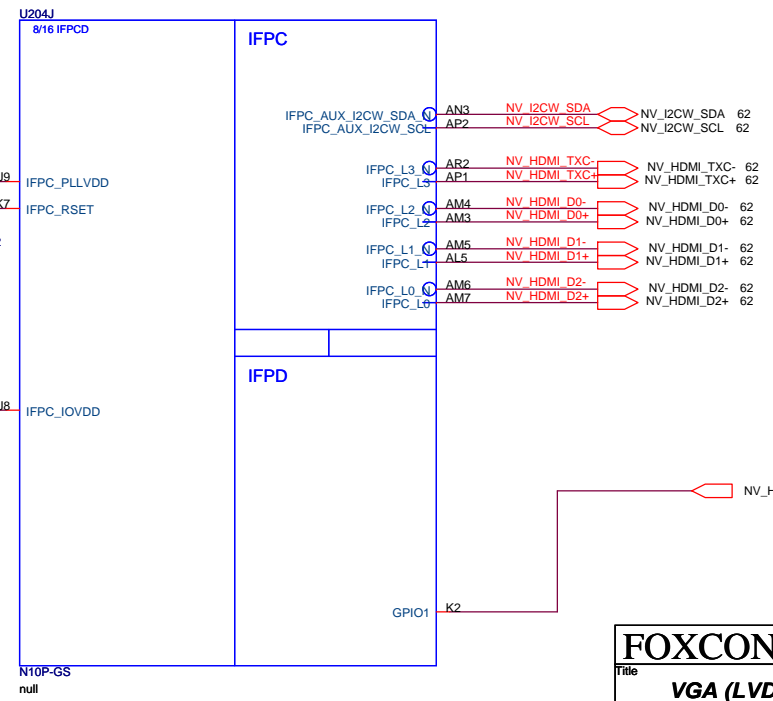
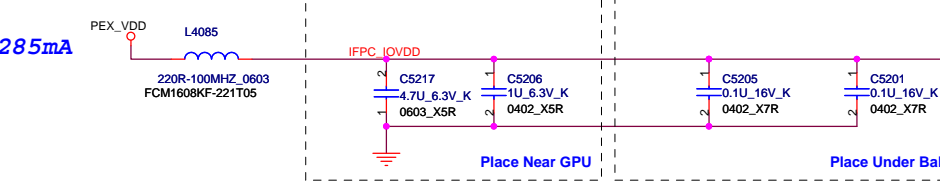
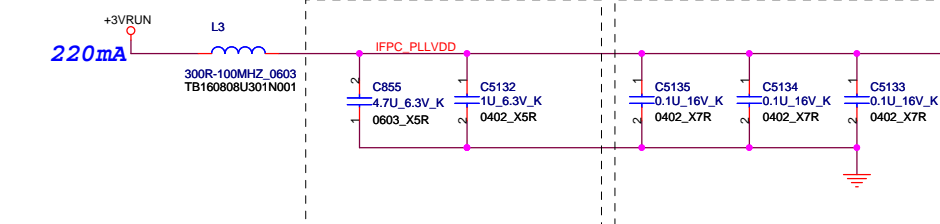
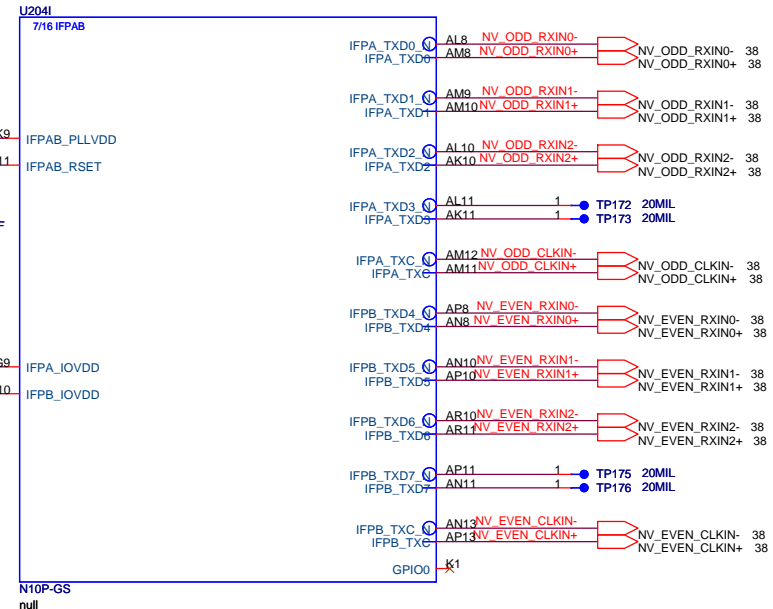
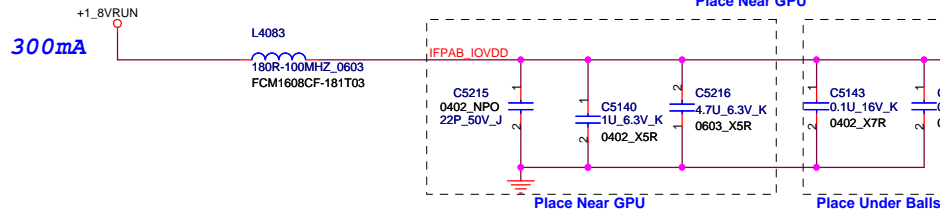
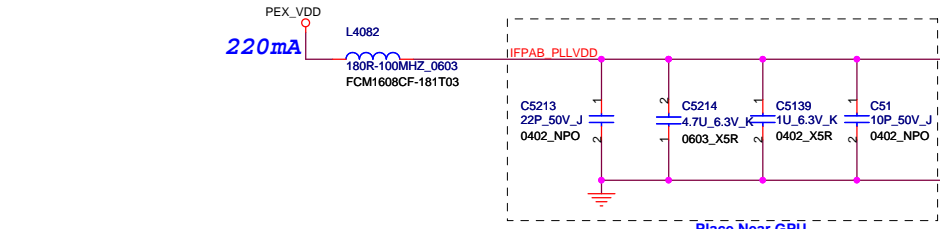
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DCCCLK	SCL
	VGA-DCCDATA	SDA



**eDP (Suzaku3 support) >> Stuff**

AN4 NV_PEG_AUXN	C835	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_AUXN	eDP_PEG_AUXN	38
AP4 NV_PEG_AUXP	C834	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_AUXP	eDP_PEG_AUXP	38
AR4 NV_PEG_TXN3	C837	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXN3	eDP_PEG_TXN3	38
AR5 NV_PEG_TXP3	C836	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXP3	eDP_PEG_TXP3	38
AP5 NV_PEG_TXN2	C800	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXN2	eDP_PEG_TXN2	38
AN5 NV_PEG_TXP2	C803	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXP2	eDP_PEG_TXP2	38
AN7 NV_PEG_TXN1	C793	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXN1	eDP_PEG_TXN1	38
AP7 NV_PEG_TXP1	C795	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXP1	eDP_PEG_TXP1	38
AR7 NV_PEG_TXN0	C725	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXN0	eDP_PEG_TXN0	38
AR8 NV_PEG_TXP0	C735	1	2	NC	0.1U	6.3V	K	0201	X5R	eDP_PEG_TXP0	eDP_PEG_TXP0	38
L7										eDP_DET_NV	eDP_DET_NV	38

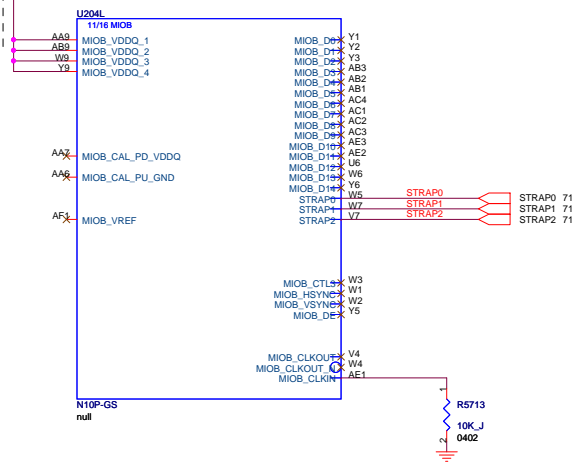
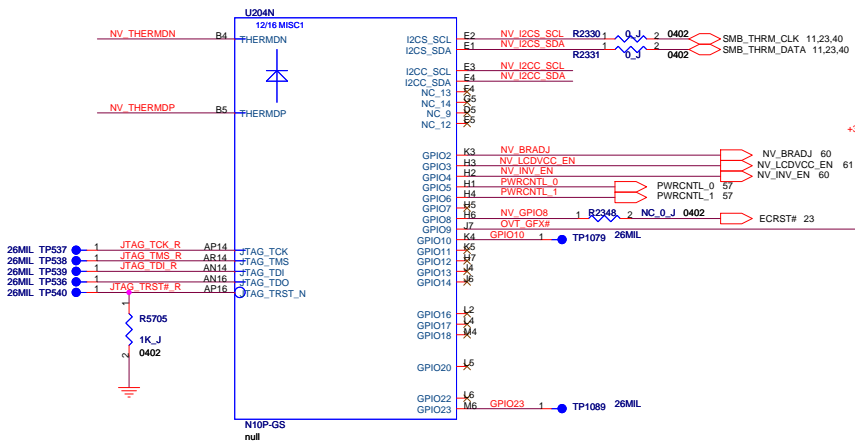
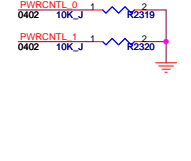
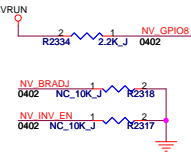
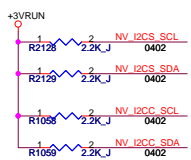
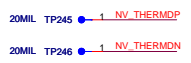
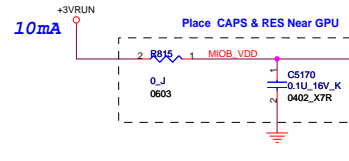
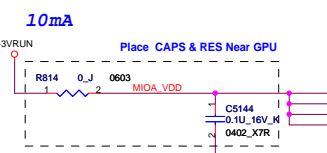
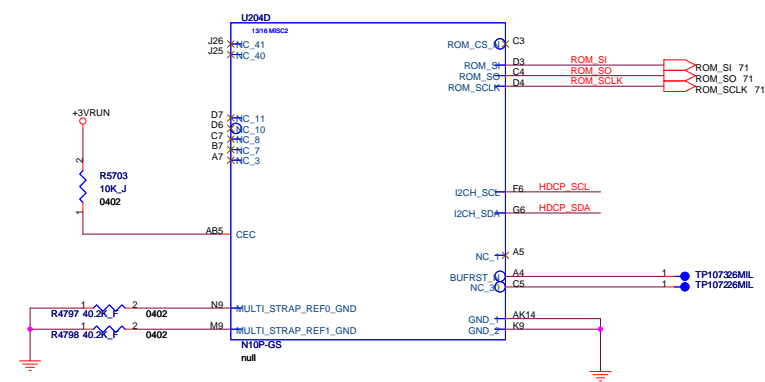
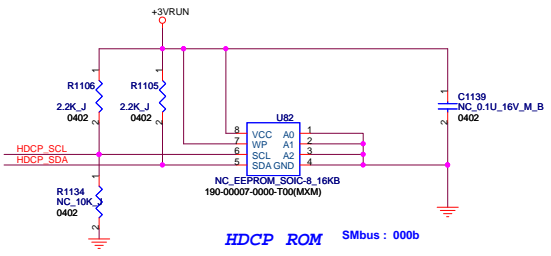
**To eDP CONN.**



To HDMI CONN.

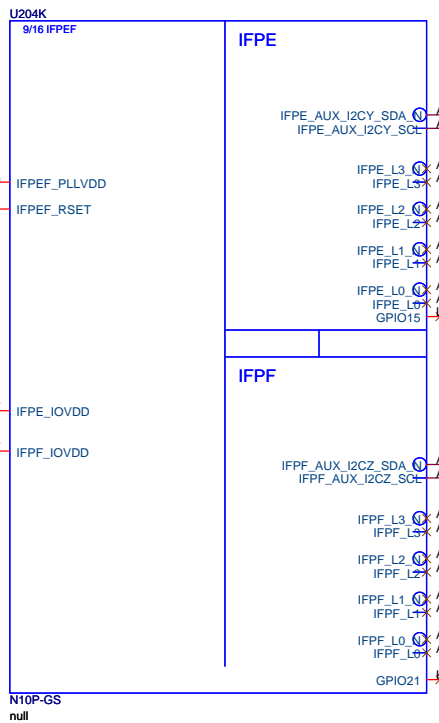
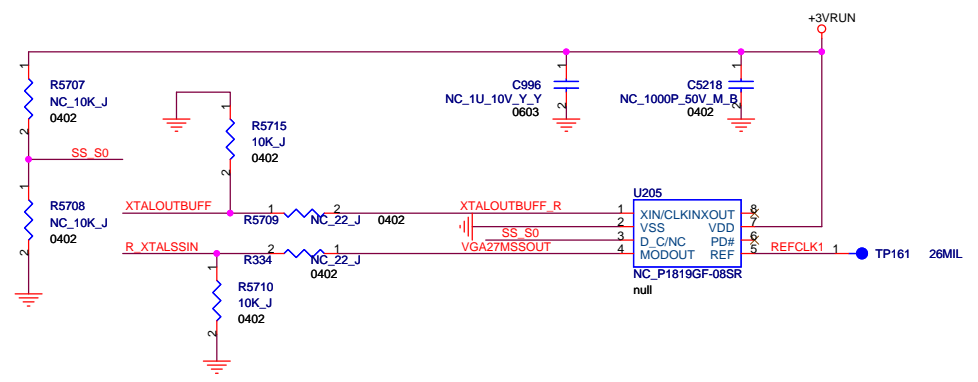
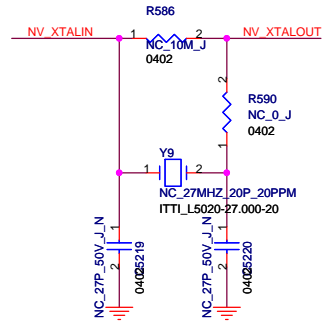
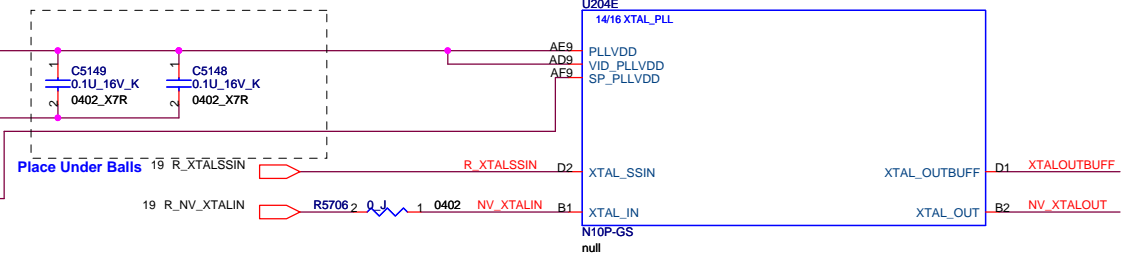
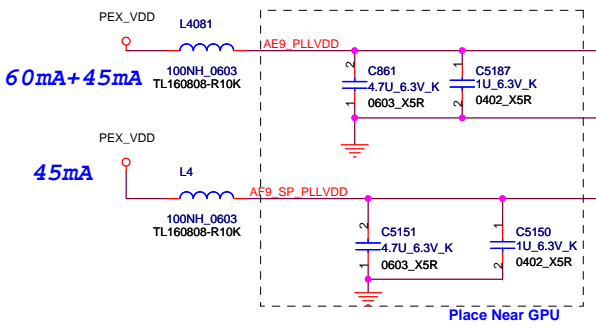
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.  
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

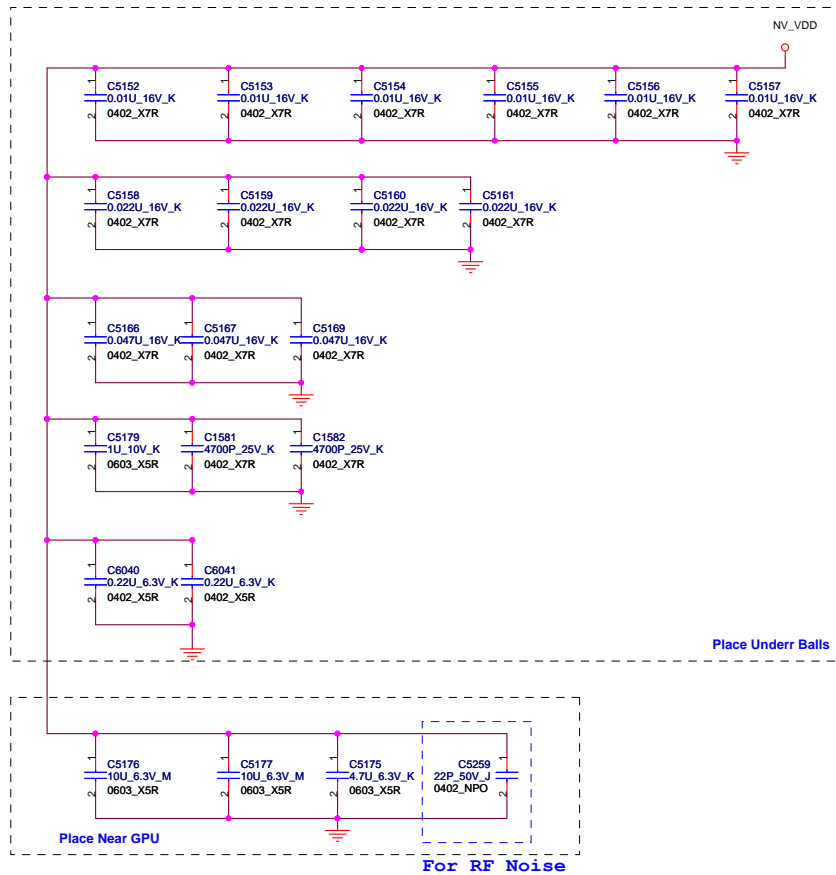
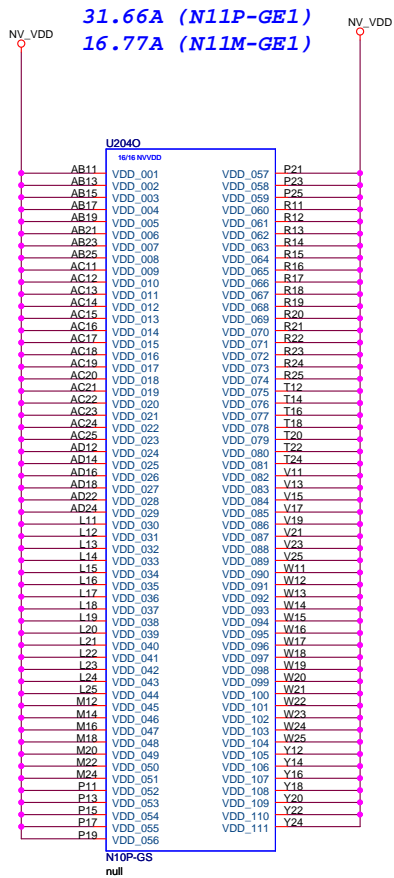
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title <b>VGA (LVDS/HDMI) 6/9</b>			
Size A3	Document Number <b>M931 (MBX-215)</b>		Rev <b>SA</b>
Date:	Wednesday, January 06, 2010		Sheet 75 of 93



GPIO	I/O	Internal pull low	GPIO TABLE
GPIO0	I	YES	
GPIO1	O	Yes	HDMI Hot Plug Detect 0 (HPD0) <b>Active High</b>
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_FWM) <b>Active High</b>
GPIO3	O	No	Panel Power(LCD0_VDD) <b>Active High</b>
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN) <b>Active High</b>
GPIO5	O	Yes	FOR Power Control NVDD <b>Active High or Low</b>
GPIO6	O	No	FOR Power Control NVDD <b>Active High or Low</b>
GPIO8	O	No	reserve for reset EC
GPIO9	I	No	System Power Limit Alert Input <b>Active Low</b>

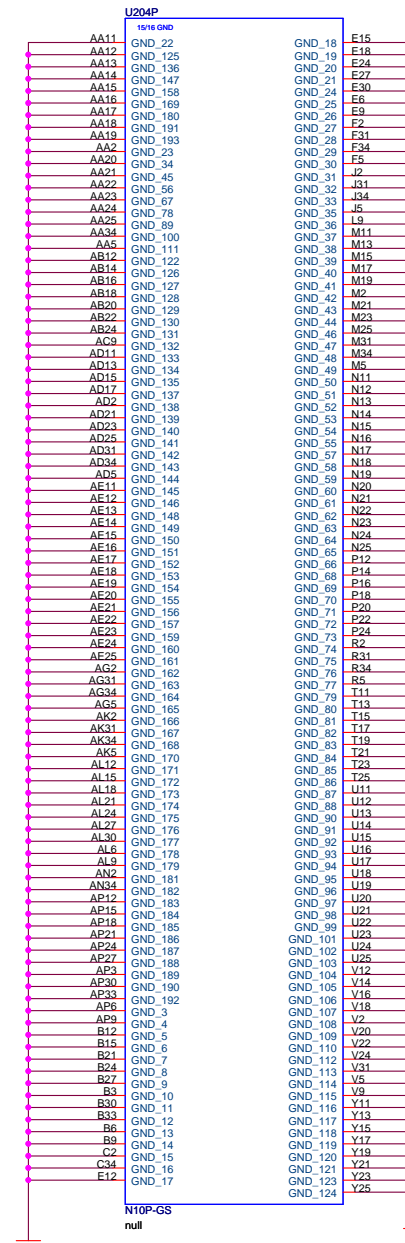
SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

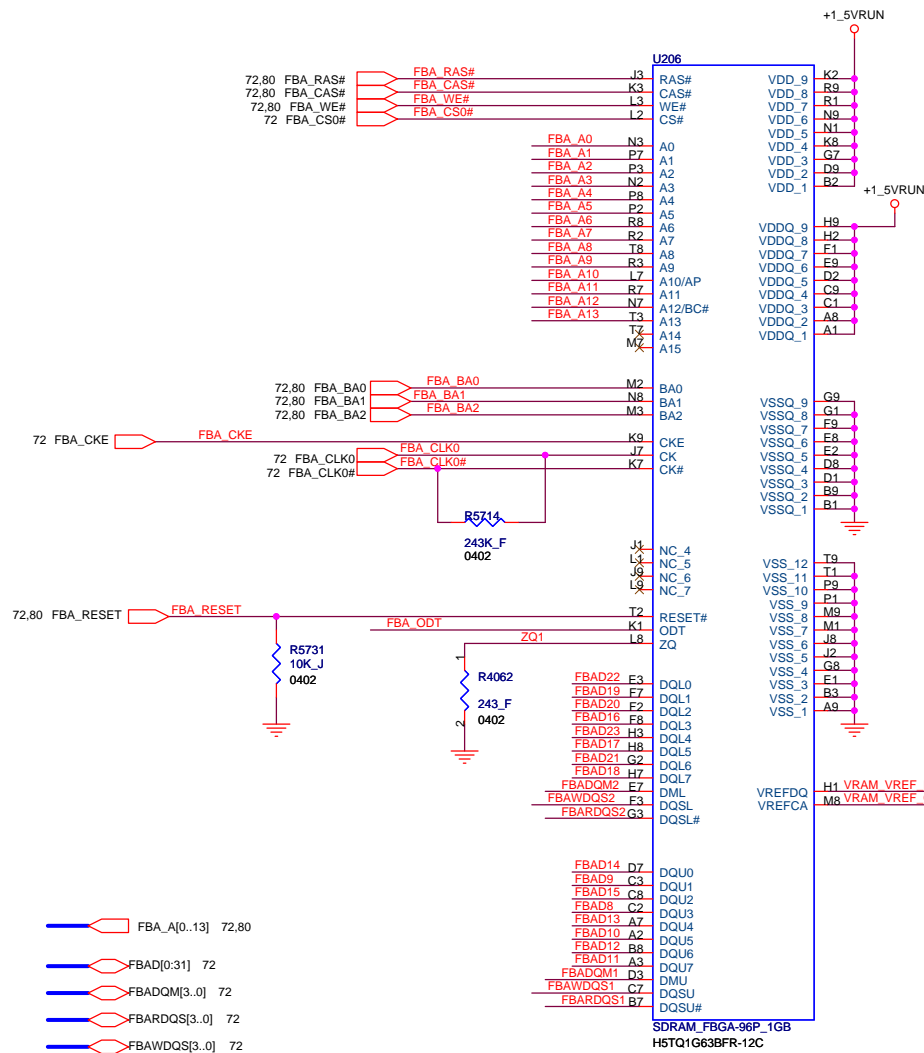




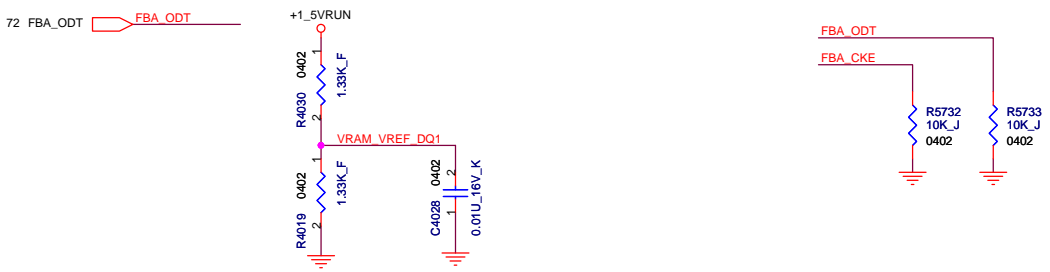
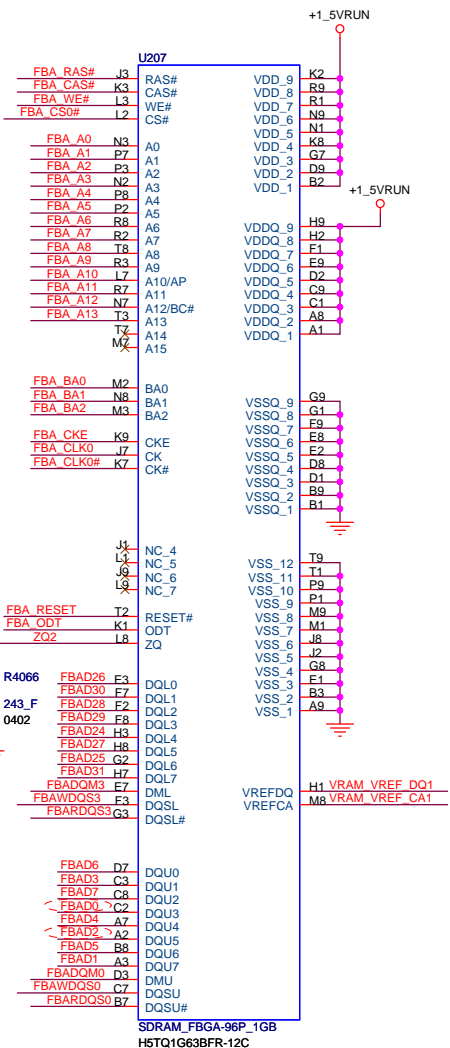
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

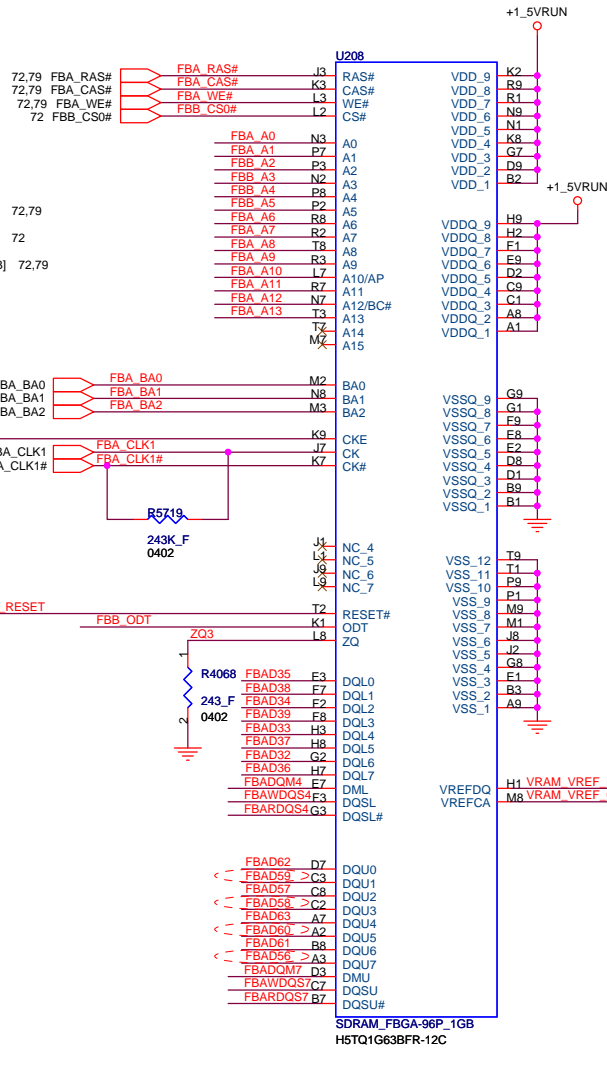
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.



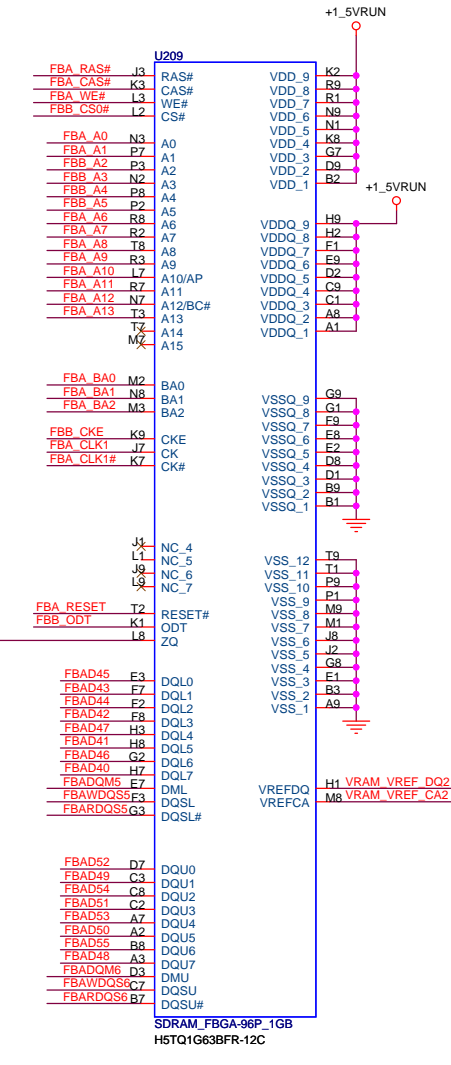


CMD0	0..30	32..63
CMD1	A4	
CMD2	RAS#	RAS#
CMD3	BA1	BA1
CMD4	A2	A2
CMD5	A4	A4
CMD6	A3	A3
CMD7	CKE	CKE
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	



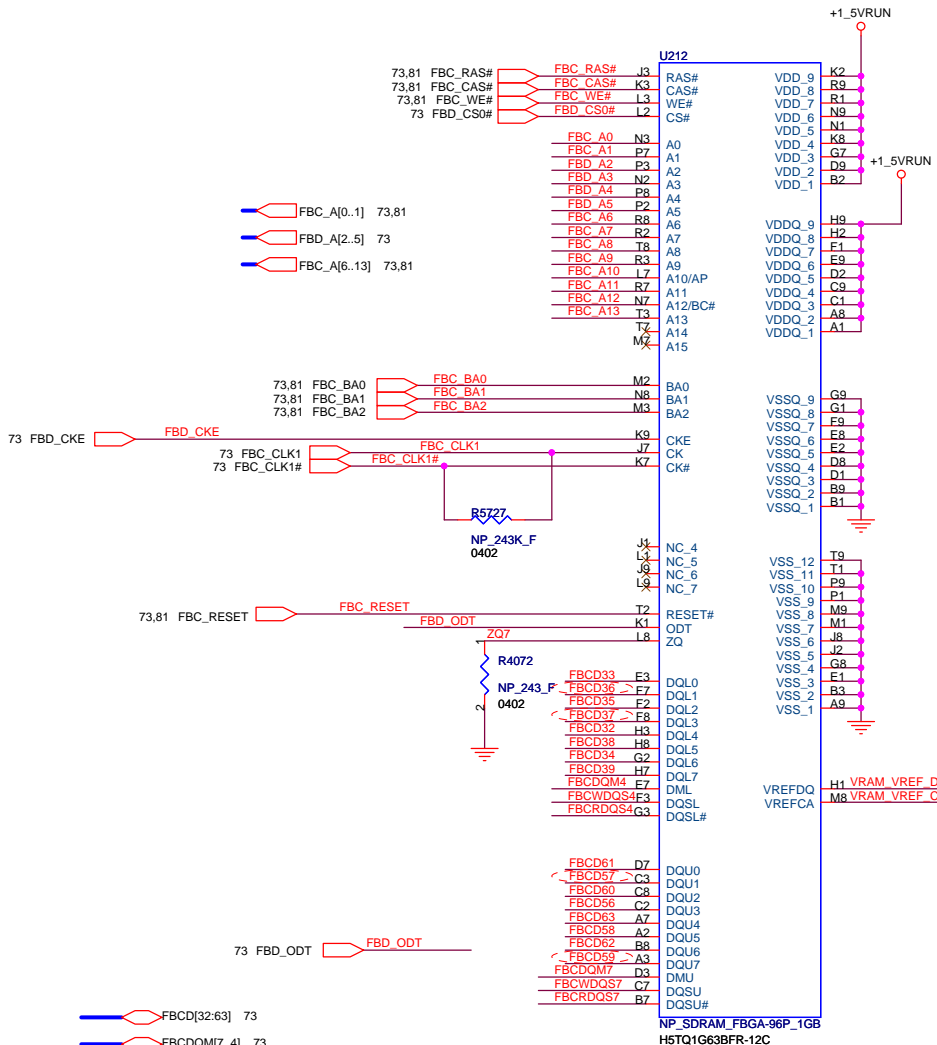


	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4	BA1	A2
CMD5	A4	A4
CMD6	A3	A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

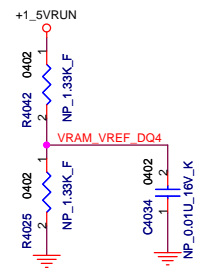
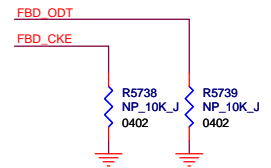
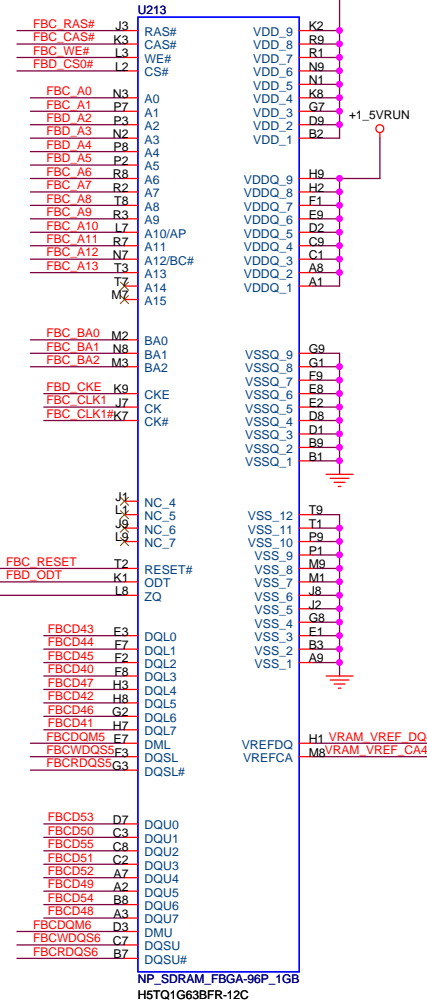








CMD0	A4	32..63
CMD1	RAS#	RAS#
CMD2	AS	AS
CMD3	BA1	BA1
CMD4	A2	A2
CMD5	A4	A4
CMD6	A3	A3
CMD7	CKE	CKE
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	ODT	ODT
CMD29	CS0#	CS0#
CMD30	ODT	ODT



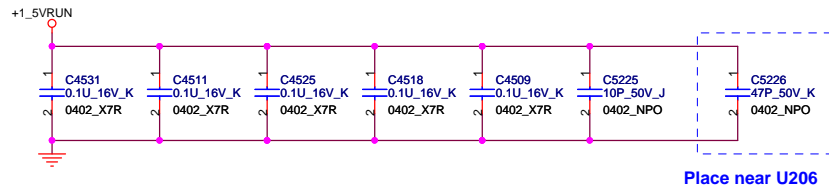
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title: **VRAM(DDR)# 4/4**

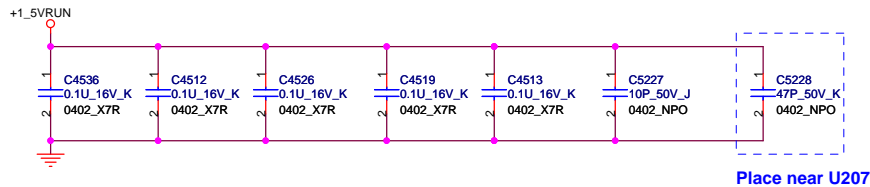
Size: Document Number **M931 (MBX-215)** Rev **SA**

Date: Wednesday, January 06, 2010 Sheet 82 of 93

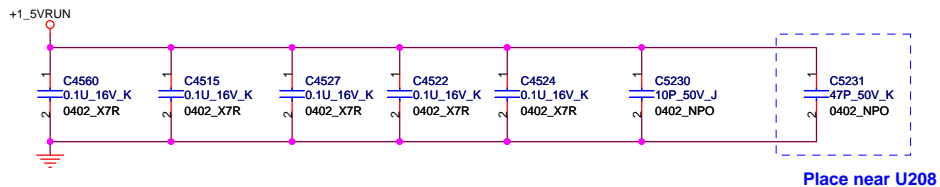
Place around the VRAM U206



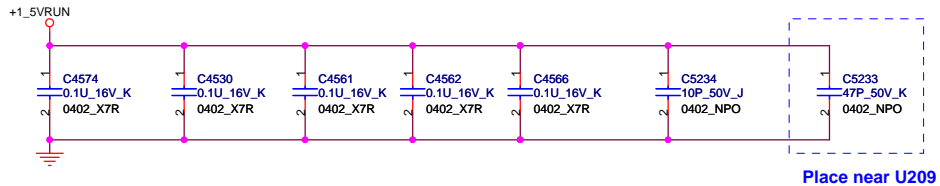
Place around the VRAM U207



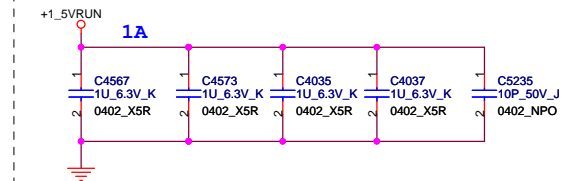
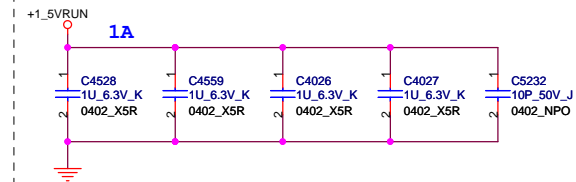
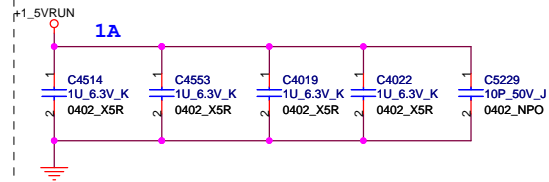
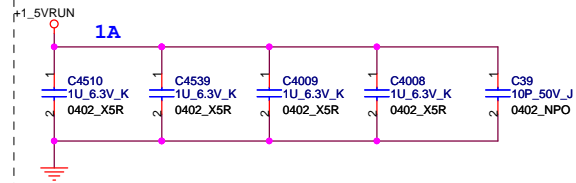
Place around the VRAM U208



Place around the VRAM U209

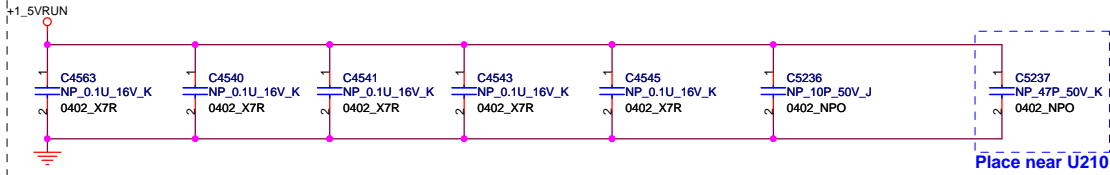


PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

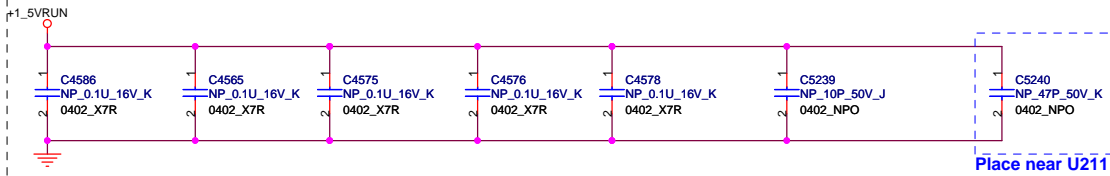


PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

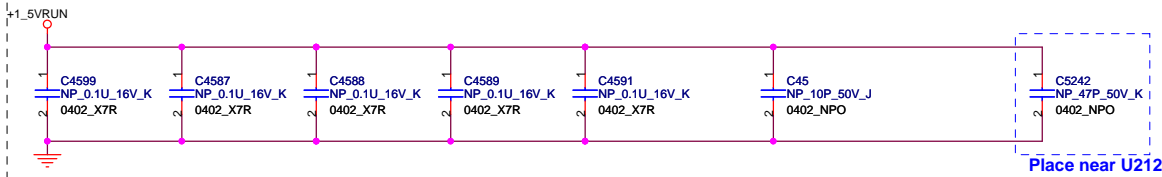
Place around the VRAM U210



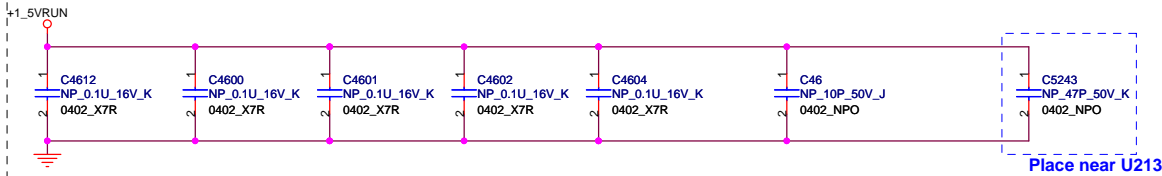
Place around the VRAM U211



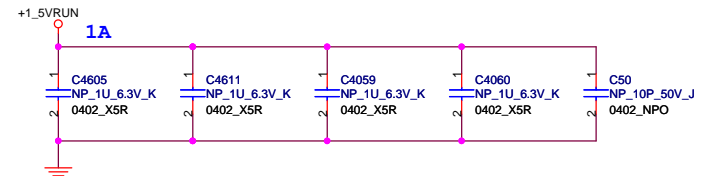
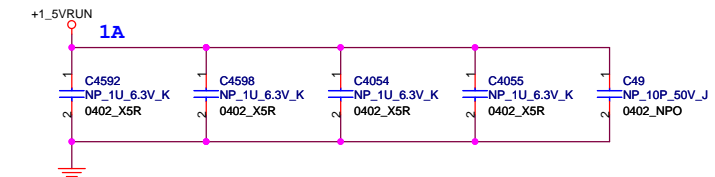
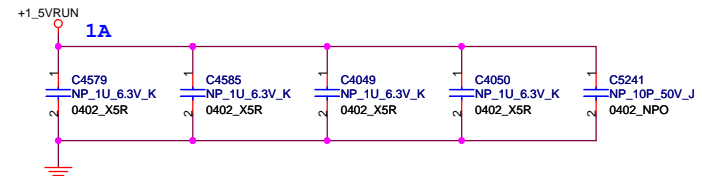
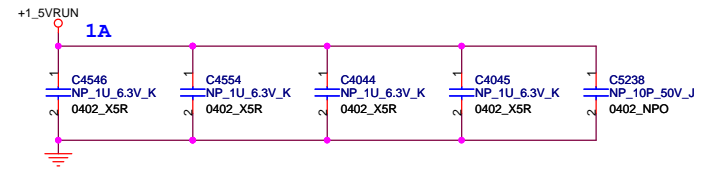
Place around the VRAM U212



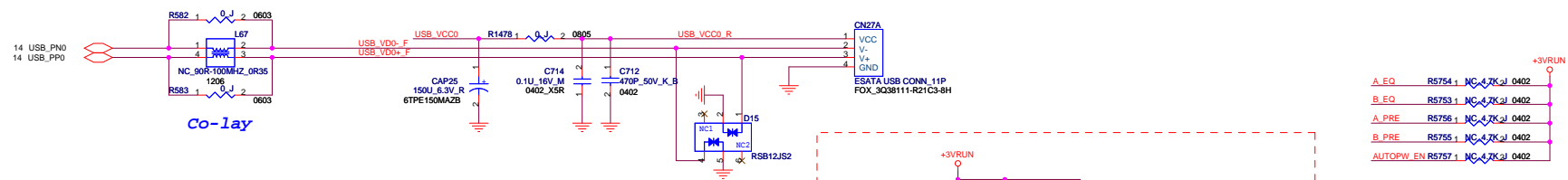
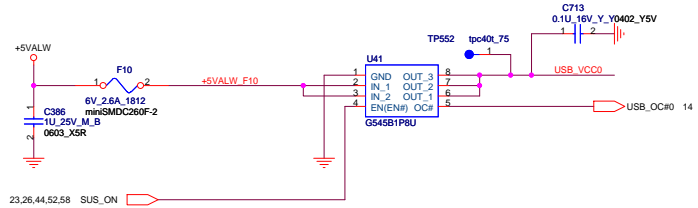
Place around the VRAM U213



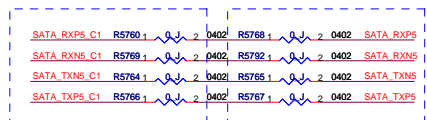
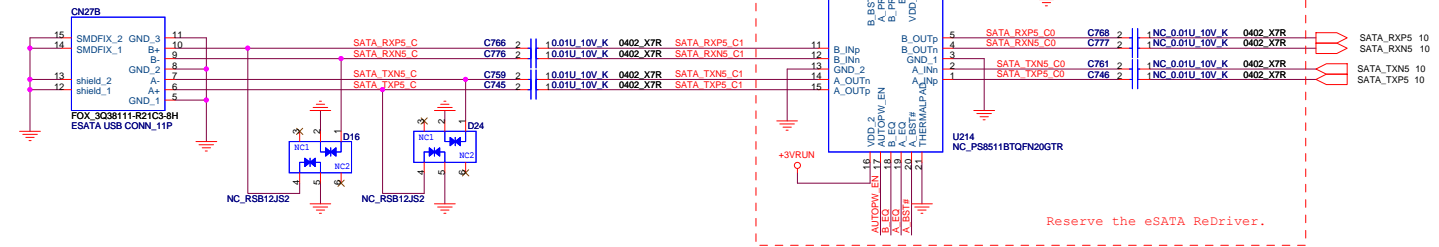
PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.



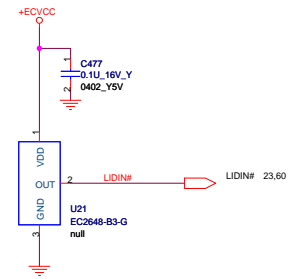
PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.



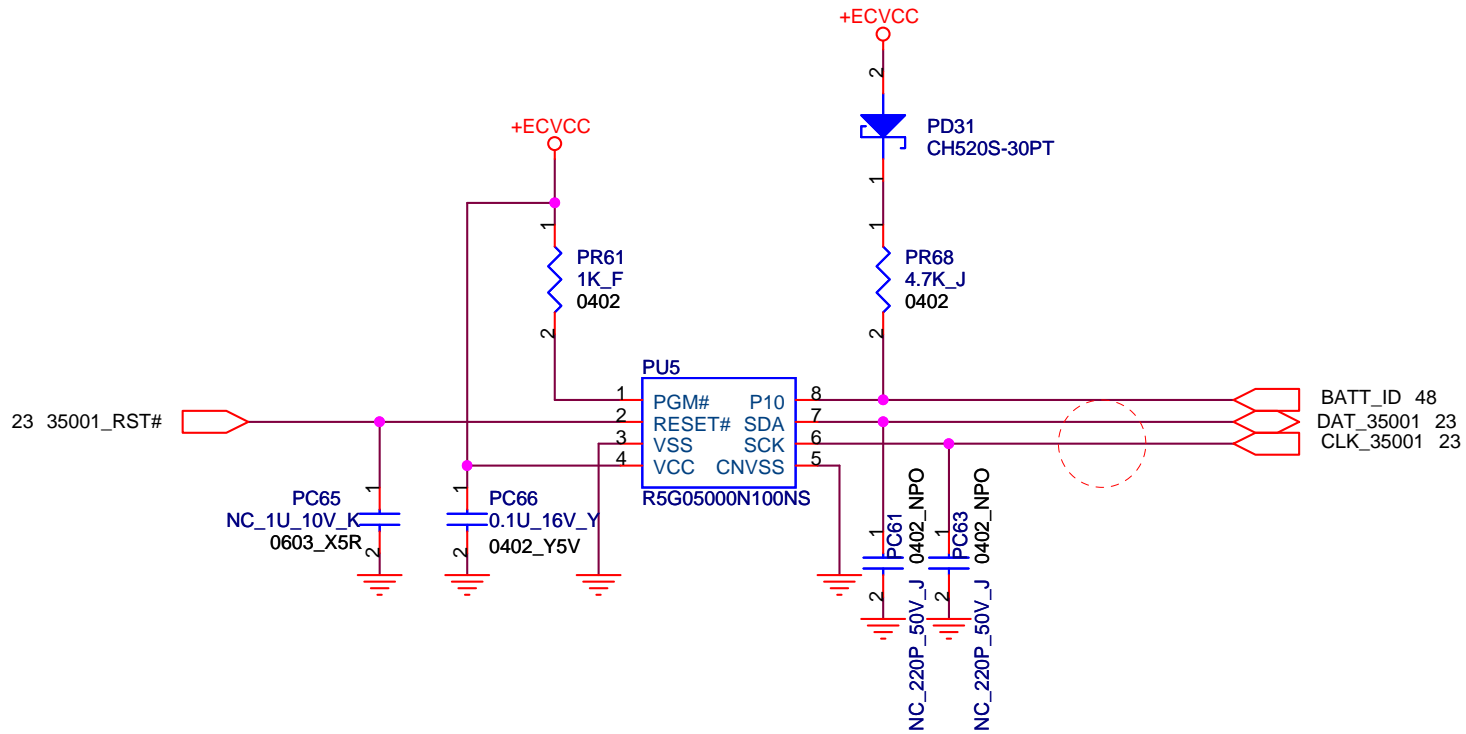
**USB/eSATA Combo**



Close to U124 ,Pin11 ,12 ,14 ,15      Close to U124 and C768 ,C777 ,C761 ,C746 Pin2

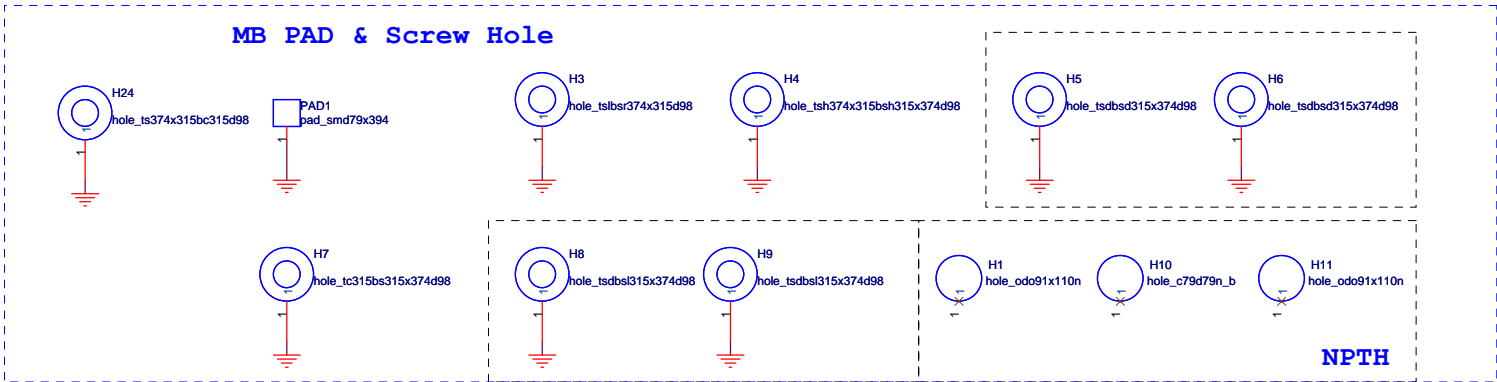


**LID Switch**



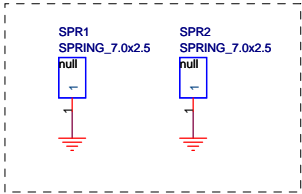
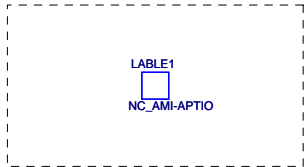
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Identify IC</b>			
Size	Document Number		Rev
A	<b>M931 (MBX-215)</b>		<b>SA</b>
Date:	Wednesday, January 06, 2010	Sheet	86 of 93

**MB PAD & Screw Hole**

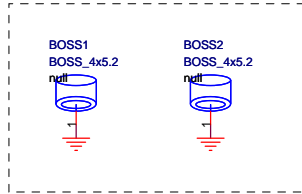


**NPTH**

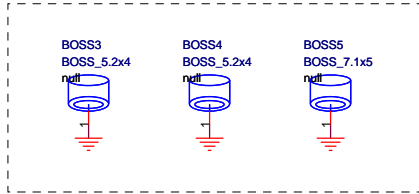
**AMI Label (For MP Only)**



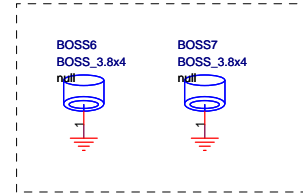
**EMI SPRING**



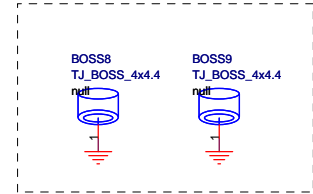
**WLAN Module**



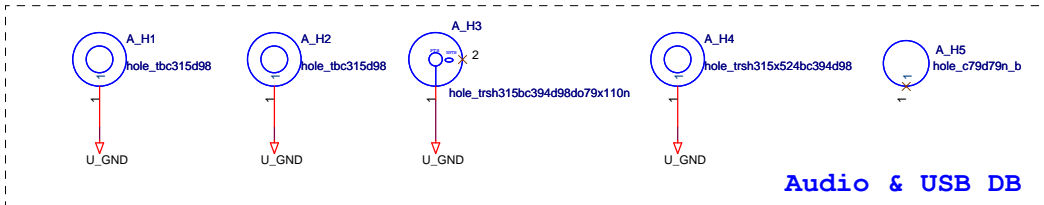
**Thermal Modul**



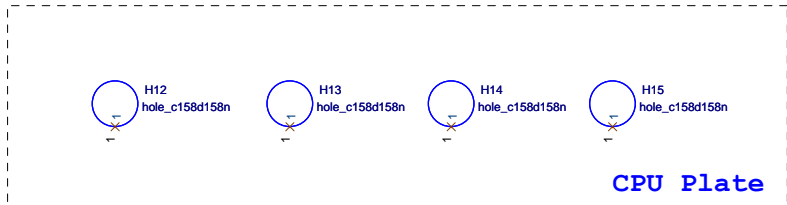
**Bluetooth Bracket**



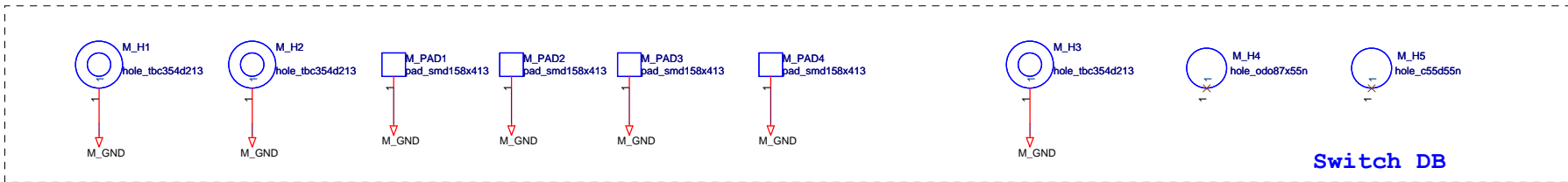
**T-jet (MACH)**



**Audio & USB DB**

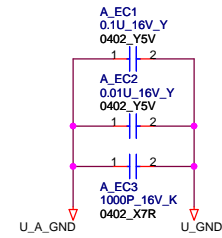
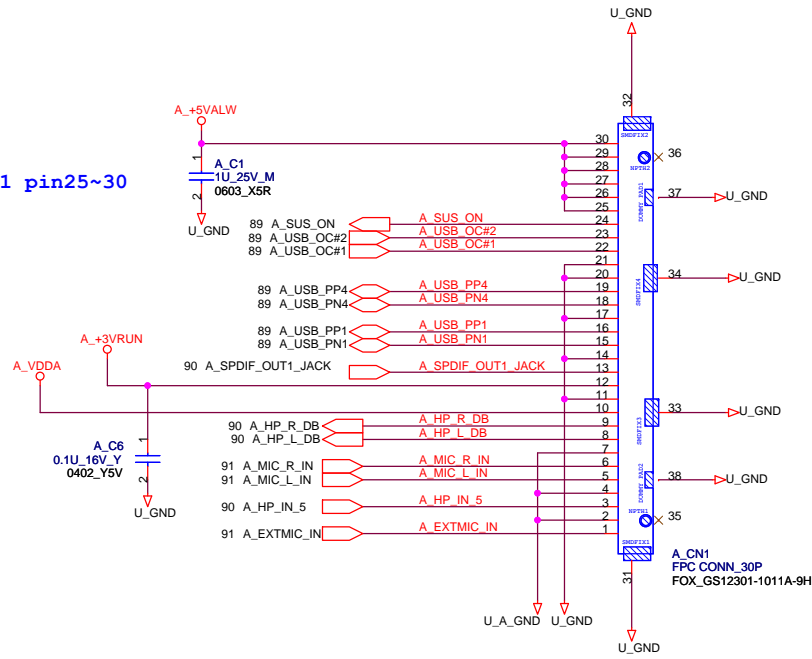


**CPU Plate**

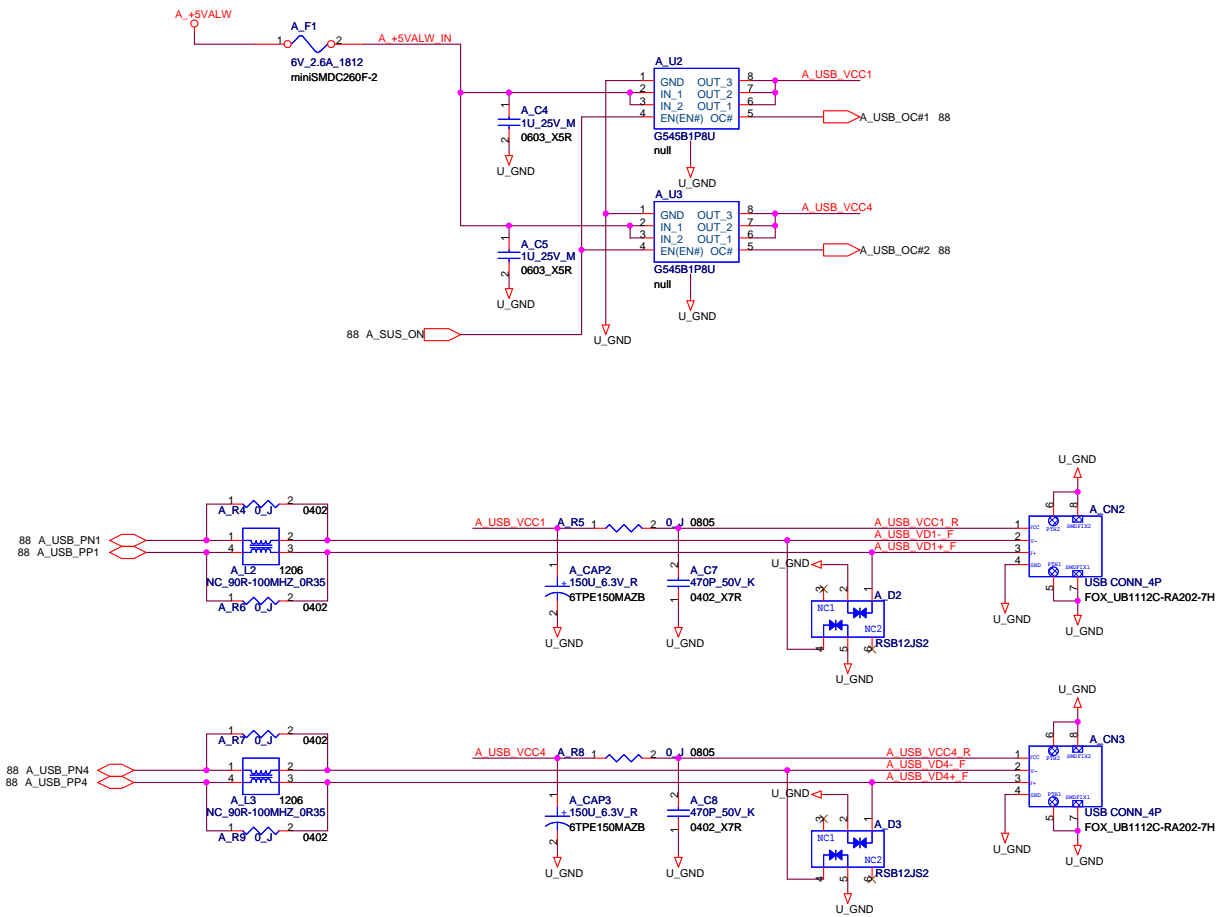


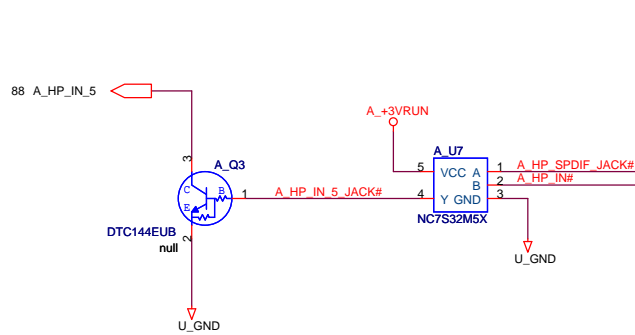
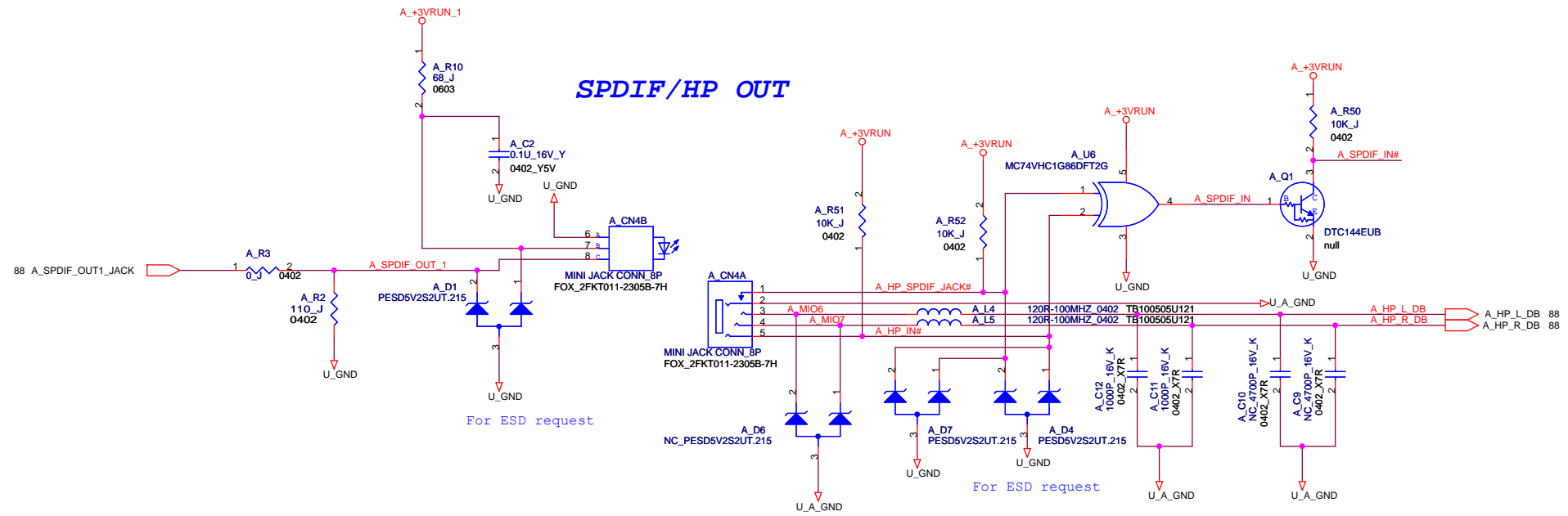
**Switch DB**

Place A\_C1 close to A\_CN1 pin25~30

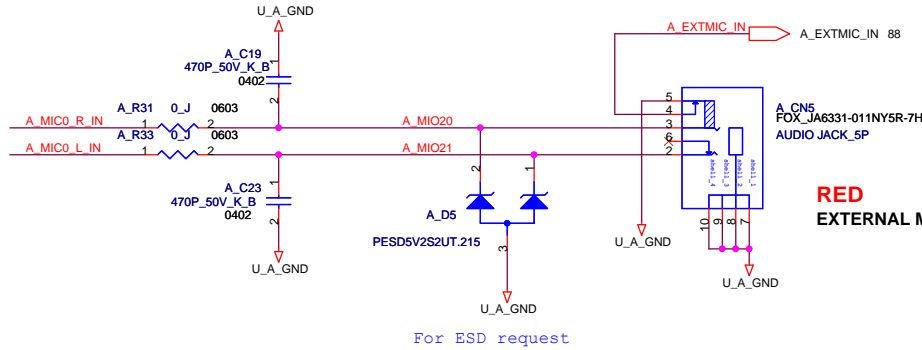
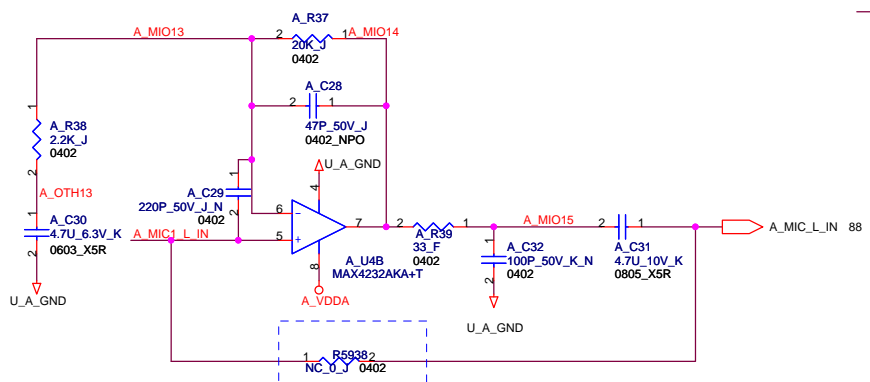
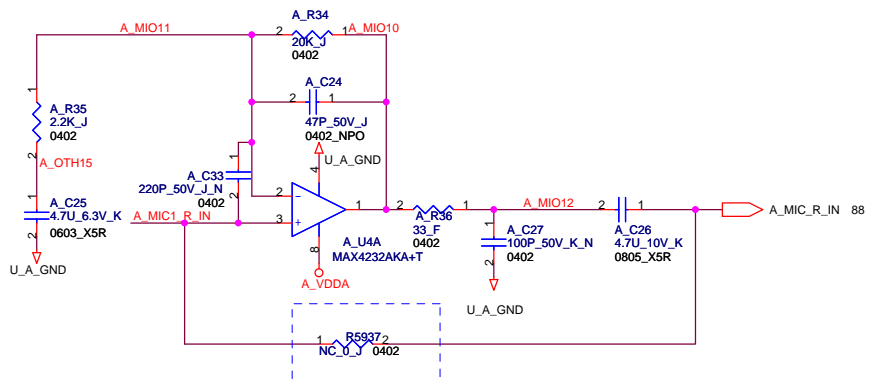




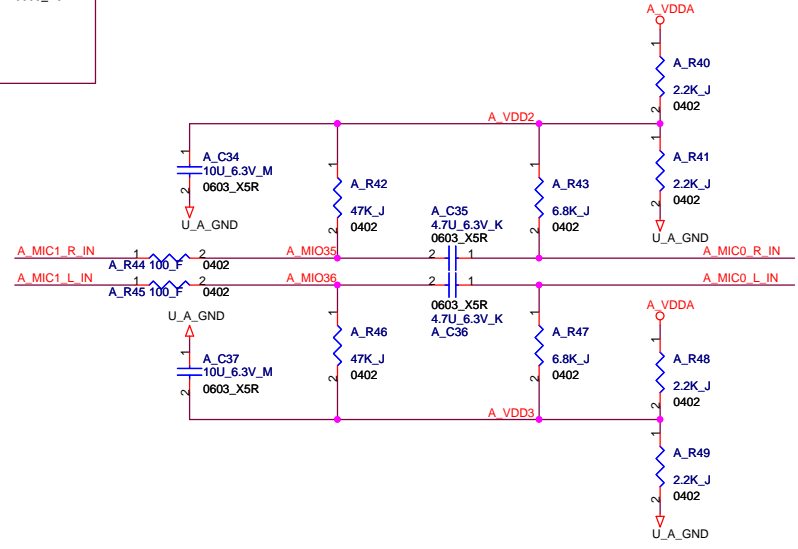
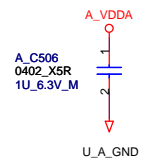


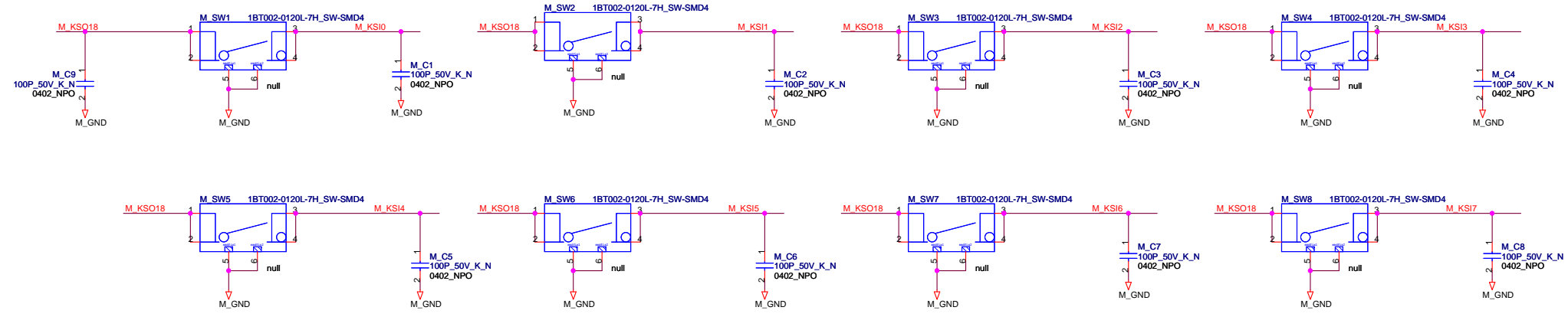
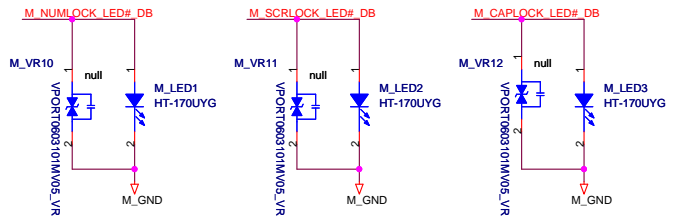
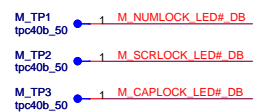
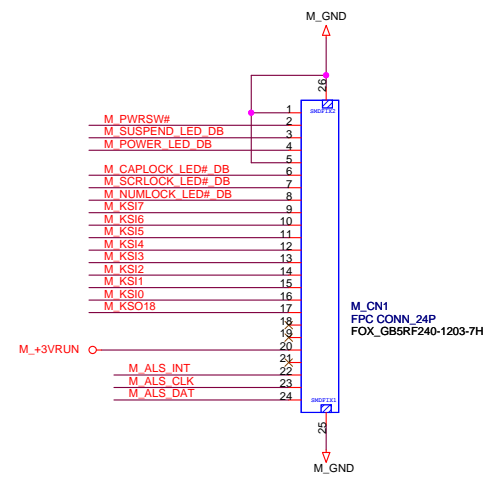
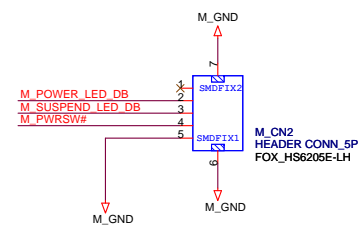
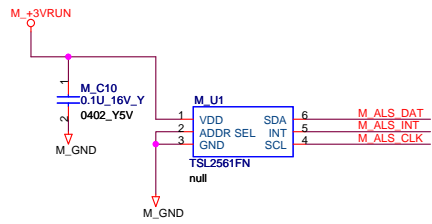


	Pin 1	Pin 5	A_LED SPDIF_IN#	A_HP_IN_5
HP	0	0	1 off	1
SPDIF	0	1	0 on	0
No plug	1	1	1 off	0



**RED**  
**EXTERNAL MIC**





**(2009/11/27) M930-MP ECN Changed**

- P.48 {DCIN} PR11 Change to SMD,RES,11.8K,1/16W,1%,0402
- P.48 {DCIN} PR12 Change to SMD,RES,10K,1/16W,1%,0402
- P.48 {DCIN} PR220 Change to SMD,RES,10.2K,1/16W,1%,0402
- P.57 {VGA Power} PR566 Change to SMD,RES,88.7K,1/16W,1%,0402
- P.51 {VTT Power} PR26 Change to SMD,RES,2.2ohm,1/10W,5%,0603
- P.51 {VTT Power} PR152 Change to SMD,RES,4.7ohm,1/10W,5%,0603
- P.51 {VTT Power} PC130 Change to SMD,MLCC,X7R,680pF,50V,10%,0603(0.8mm)
- P.12 {PCH} Delete D28, D29
- P.92 {DB} Delete M\_VR1,M\_VR2,M\_VR3,M\_VR4,M\_VR5,M\_VR6,M\_VR7,M\_VR8,M\_VR9
- P.92 {DB} Add M\_VR10,M\_VR11, M\_VR12
- P.23 {EC} Add C487 ,SMD,MLCC,X7R,1000pF,16V,10%,0402
- P.27 {WLAN} SW4 Change to ALPS,S55811101,Switch,SMD-7,Slide SW
- P.64 {CODEC} Change U215 vendor number from ALC275SQ-GR-A5 to ALC275SQ-GR

**(2009/12/02)**

- P.2 {Block Diagram} Revised Model Name and Feature
- P.4 {CPU} Short RP80
- P.7 {CPU} Short R1561
- P.9 {CPU} Short R1586, R1587
- P.11 {PCH} Short RP69 ,RP71 ,RP67 ,RP70 ,RP78 ,RP68 ,RP89
- P.12 {PCH} Short R927
- P.19 {CLK} Short RP9 ,RP84 ,RP85 ,RP79
- P.23 {EC} Delete RP23
- P.26 {ExpressCard} Short R343, R337 ,Delete L40
- P.27 {WLAN} Short R22
- P.36 {Camera} Short R376 ,R377 ,Delete L46
- P.37 {Felica} Short R192 ,R193 ,Delete L25
- P.39 {BT} Change R7 to 100ohm as RF team Request.
- P.39 {BT} Delete U1 ,R6 ,C6 ,U12
- P.41 {KB} Short R695
- P.43 {TP} Short R533 ,Delete R530
- P.46 {Thermal} Delete D20 ,C547 ,C534 ,U26 ,R946 ,R61
- P.46 {Thermal} Delete U5 ,R65 ,C42 ,R54 ,R53 ,R60
- P.62 {HDMI} Delete L57 ,L60 ,L74 ,L76 ,Short R495 ,R483 ,R487 ,R492 ,R489 ,R498 ,R499 ,R494
- P.64 {Audio} Short R5767.
- P.85 {eSATA} Reserved C768 ,C777 ,C761 ,C746 ,U214
- P.85 {eSATA} Delete L62 ,L66 ,Short R589 ,R588 ,R592 ,R591
- P.86 {BAT ID} Short PR125

**(2009/12/18)**

- P.57 {VGA Power} Change PR182 to PWR\_CNTL\_0 Net.
- P.57 {VGA Power} Change PR180 to PWR\_CNTL\_1 Net.
- P.11 {PCH} U69 P/N :12-1BEXPEA-0004 (INTEL,BD82PM55 SLH23,BGA-1071,Intel Platform Controller Hub)
- P.35 {SD} Reserve the R1590 for SD Slot (CN29) Dampning.
- P.52 {0.75VPower} Change PC143 to 1C-2B20104-K300 (0.1uF/X7R/10%)

**(2009/12/23)**

- P.76 {VGA} Reserve the TP245 and TP246
- P.52 {DDR3 Power} Reserve the PR150 /PR157 Path

**(2009/12/29)**

- P.51 {VTTV Power} Reserve the CAP32 for Power Noise Reduce
- P.52 {1.5V Power} Reserve the CAP33 for Power Noise Reduce
- P.57 {VGA Power} Reserve the CAP34 for Power Noise Reduce

**(2010/01/06)**

- P.34 {SD} Revise R817 pull-up connection from +3VRUN to VCC\_SD