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21	DDRIII(SO-DIMM_1) 2/3	1.0	63	CRT	1.0
22	SO-DIMM_VREF 3/3	1.0	64	Audio (CODEC)	1.0
23	EC+KBC (NPCE783L)	1.0	65	Audio (MUTE)	1.0
24	SPI Flash ROM	1.0	66	Audio (Power)	1.0
25	Debug Port	1.0	67	Audio (Speaker AMP)	1.0
26	Express Card	1.0	68	Audio (Speaker Connector)	1.0
27	Mini-PCIE Card (WLAN)	1.0	69	Mini-PCIE Card (Mach)	1.0
28	TV-Tuner Connector	1.0	70	VGA (PCI-E) 1/9	1.0
29	LAN (88E8057) 1/2	1.0	71	VGA (STRAP) 2/9	1.0
30	LAN (Transformer) 2/2	1.0	72	VGA (DDR) 3/9	1.0
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35	PCIE (SD) 2/2	1.0	77	VGA (XTAL) 8/9	1.0
36	Camera Connector	1.0	78	VGA (POWER/GND) 9/9	1.0
37	Felica Connector	1.0	79	VRAM (DDR3) 1/4	1.0
38	eDP&LVDS Connector	1.0	80	VRAM (DDR3) 2/4	1.0
39	Bluetooth Connector	1.0	81	VRAM (DDR3) 3/4	1.0
40	Modem Connector	1.0	82	VRAM (DDR3) 4/4	1.0
41	KB Connector	1.0	83	VRAM (BYPASS) 1/2	1.0
42	Status LED	1.0	84	VRAM (BYPASS) 2/2	1.0

M931 BOM Control Table

VALUE Head	CFD+PM55 N11P 1GVRAM-H	CFD+PM55 N11P 1GVRAM-S	CFD+PM55 N11M 512MVRAM-H	CFD+PM55 N11M 512MVRAM-S	ARD+PM55 N11P 1GVRAM-H	ARD+PM55 N11P 1GVRAM-S	ARD+PM55 N11M 512MVRAM-H	ARD+PM55 N11M 512MVRAM-S
NV_	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff
NP_	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy
NM_	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff
NVH_	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy
NVS_	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff
NC_	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy

TJ_ for T-JET SKU (CTO)

85	LID Switch/eSATA COMBO	1.0
86	Identify IC	1.0
87	HOLE & AMI LABEL	1.0
88	USB & AUDIO Conn.	1.0
89	USB Port	1.0
90	HP Jack (S/PDIF)	1.0
91	Ext MIC Jack	1.0
92	Function SW & ALS	1.0

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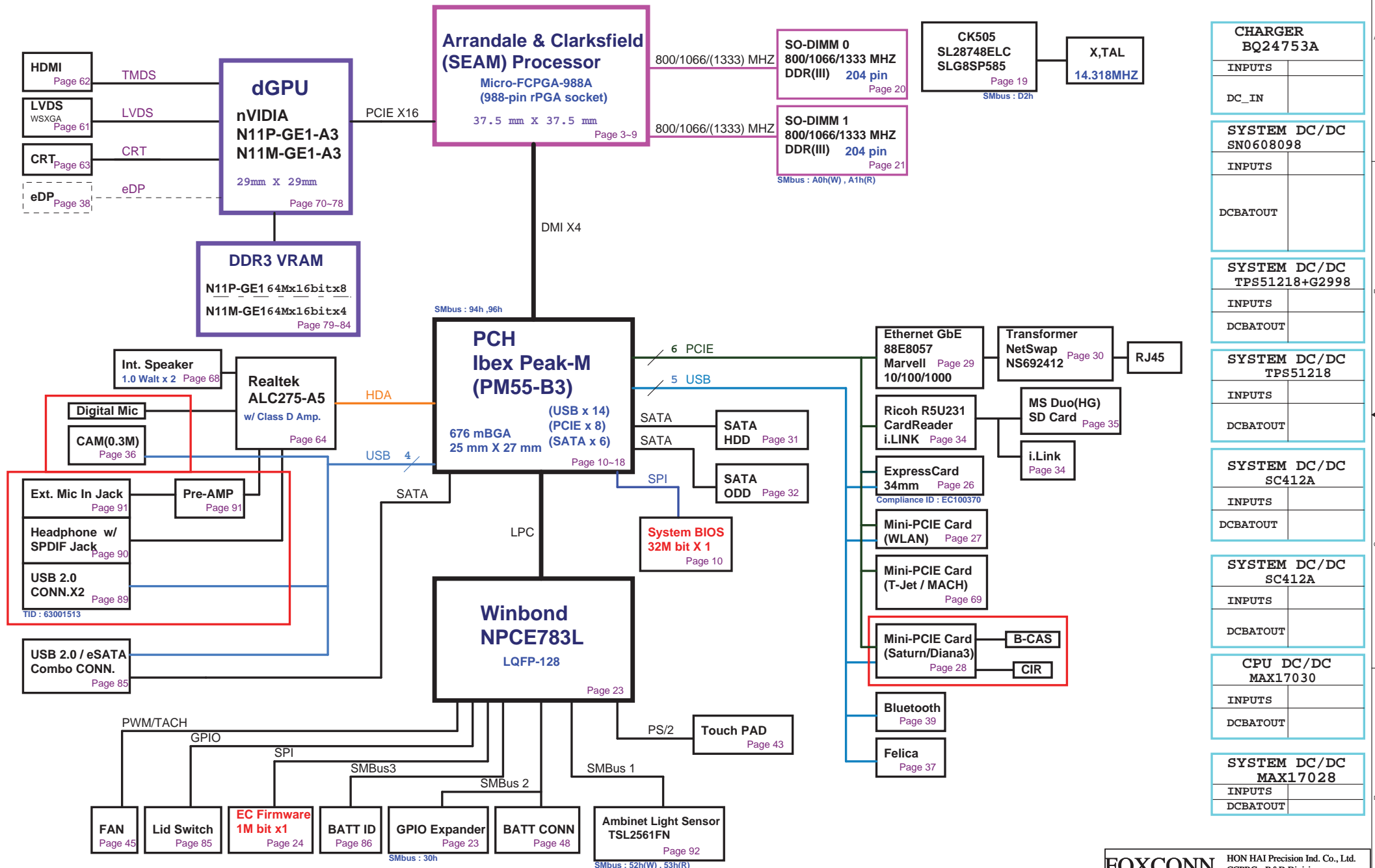
P. Leader	Check by	Design by

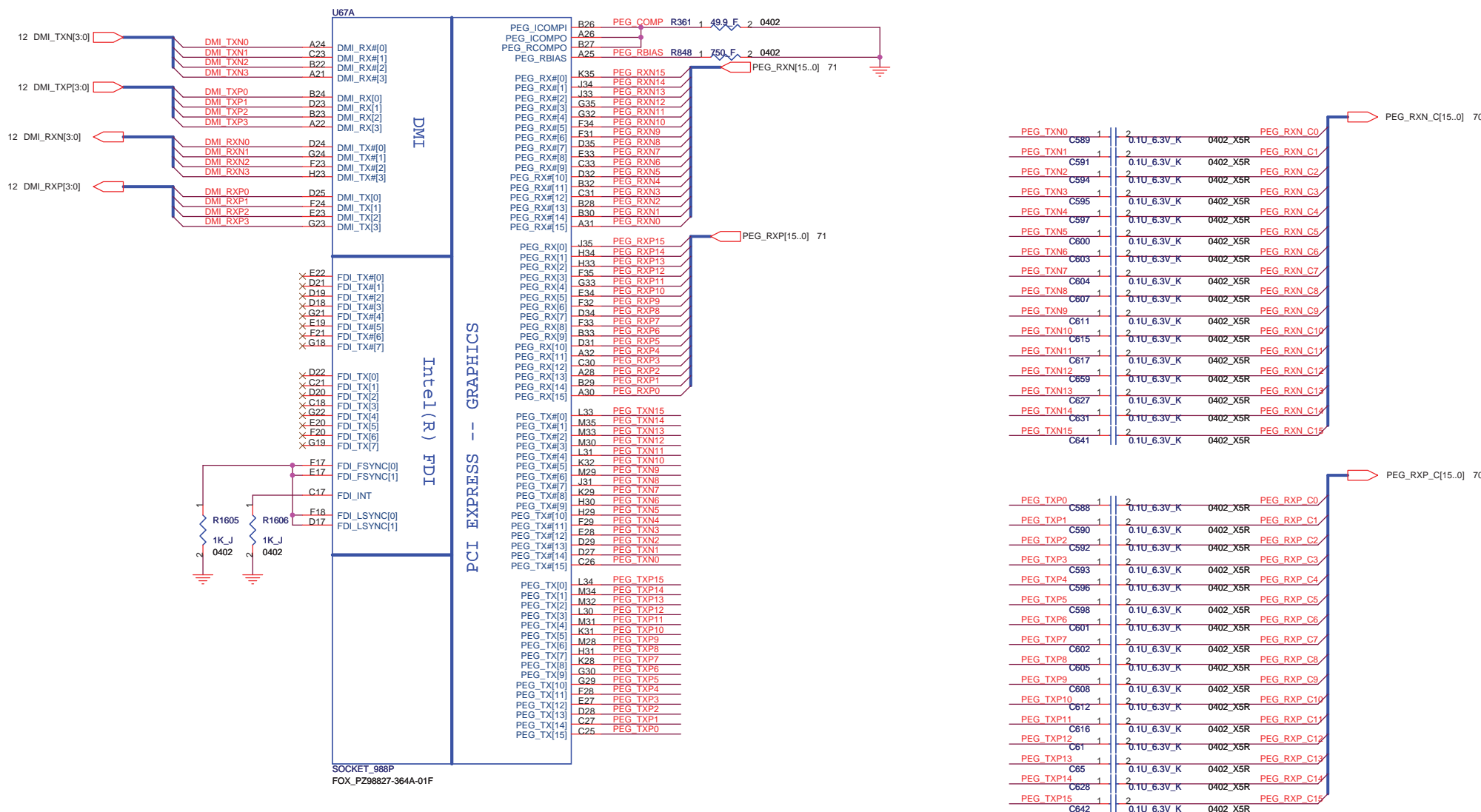
Project Code & Schematics Subject: M931 Main Board

PCB P/N: (IRIS)
(Hannstar)

FOXCONN		HON HAI Precision Ind. Co., Ltd.
		CCPBG - R&D Division
Title	Index Page	
Size	Document Number	
Custom	M931 (MBX-215)	Rev SA
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M931 (IRX-5300) Calpella Platform+ nVIDIA N11P/M Discrete Graphic

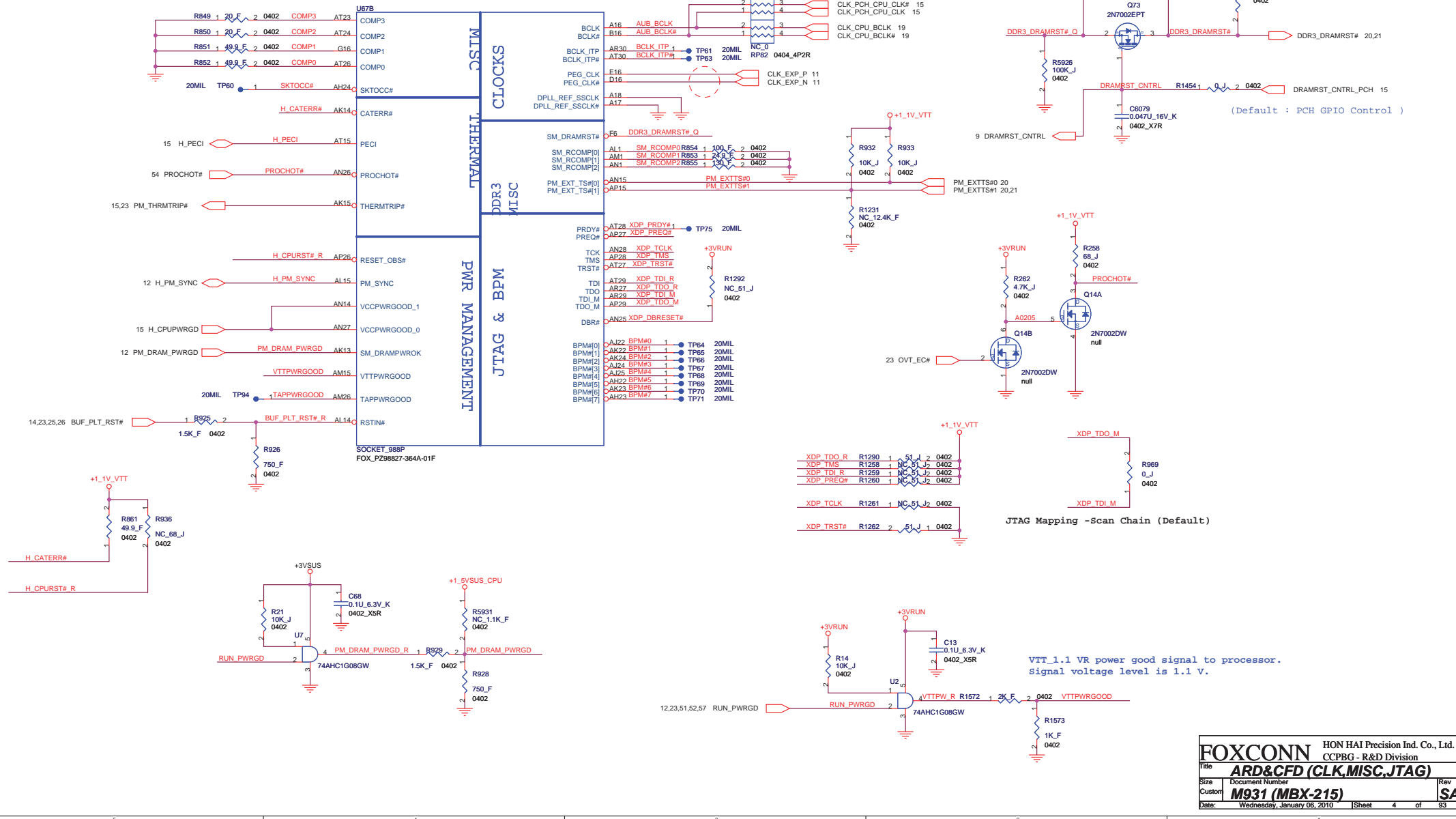




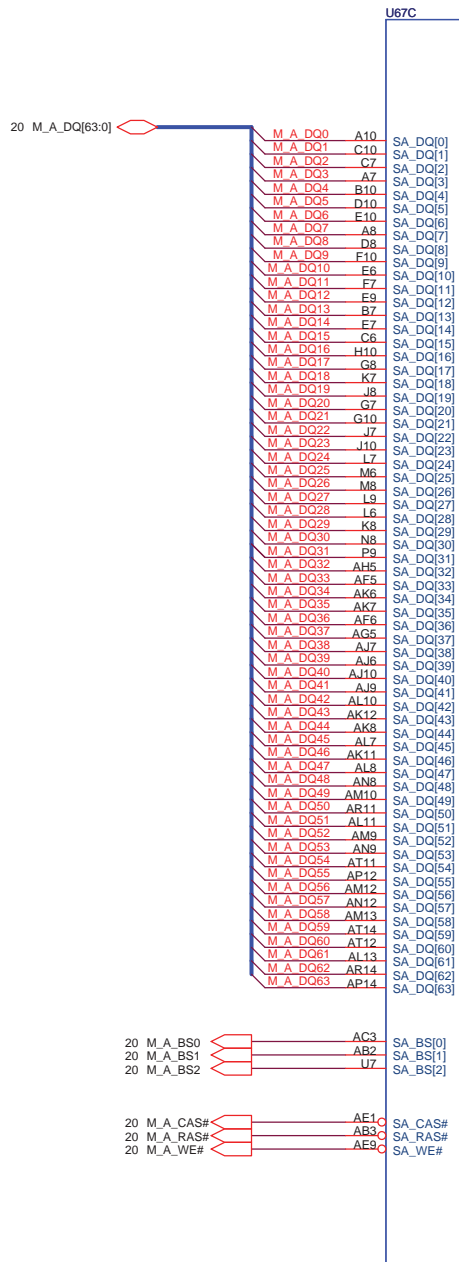
Layout Note:
 In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils (0.254-mm) wide trace for routing less than 500 mils (12.7 mm), or 20-mils (0.508-mm) wide trace for routing between 500 mils (12.7 mm) and 1000 mils(25.4 mm). Keep 20-mils (0.508-mm) spacing to any other signals in order to minimize crosstalk.

For Disable Auburndale Graphic
 DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics.

<http://laptop-motherboard-schematic.blogspot.com/>

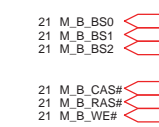
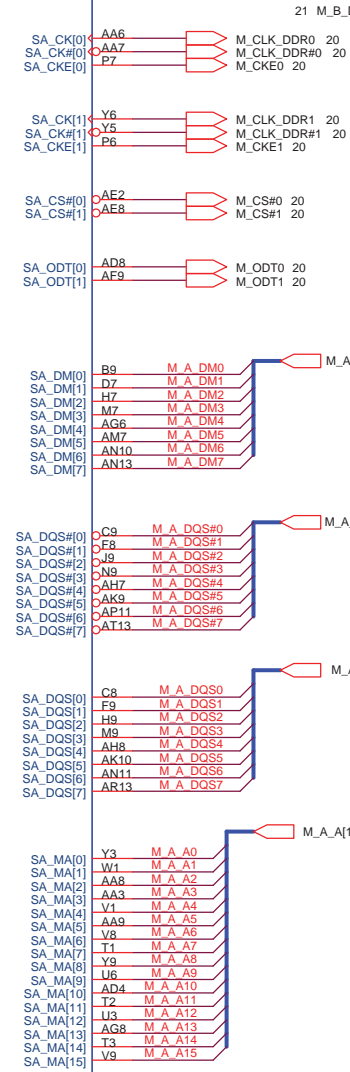


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ARD&CFD (CLK,MISC,JTAG)		
Size	Document Number		Rev
Custom	M931 (MBX-215)		SA
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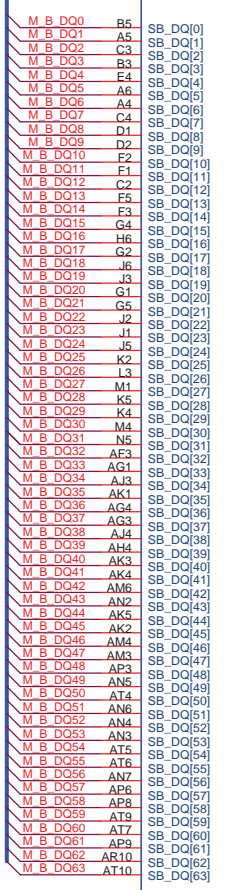


DDR SYSTEM MEMORY A

SOCKET_988P
FOX_PZ98827-364A-01F

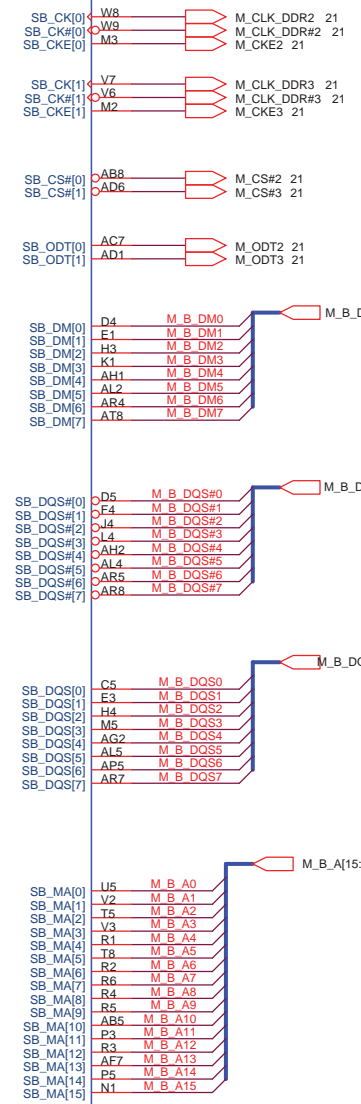


U67D



DDR SYSTEM MEMORY - B

SOCKET_988P
FOX_PZ98827-364A-01F



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **ARD&CFD (DDR3)**

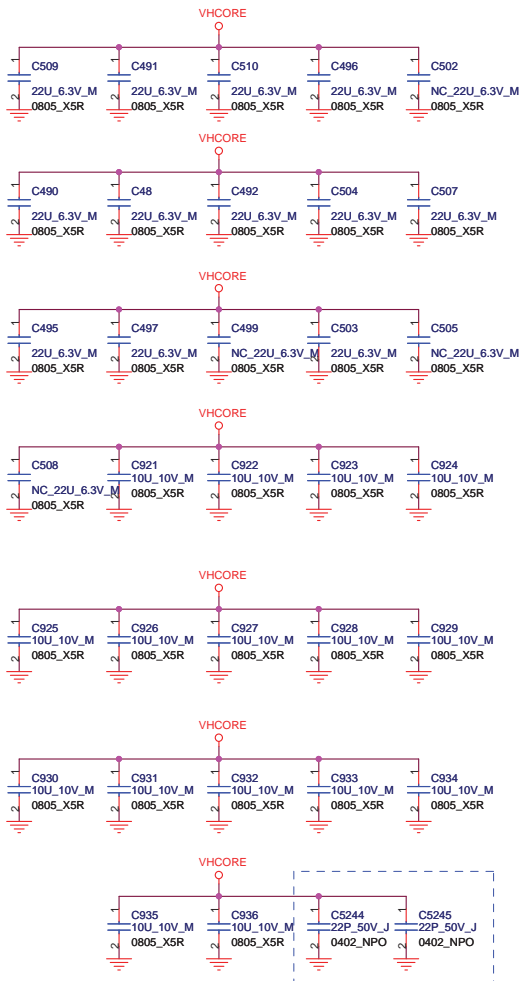
Size: A3
Document Number: **M931 (MBX-215)**

Date: Wednesday, January 06, 2010

Rev: **SA**

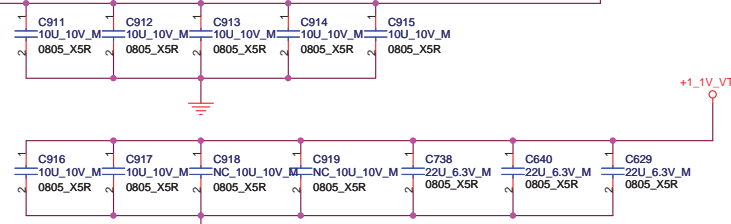
Sheet 5 of 93

52A (CFD SV)

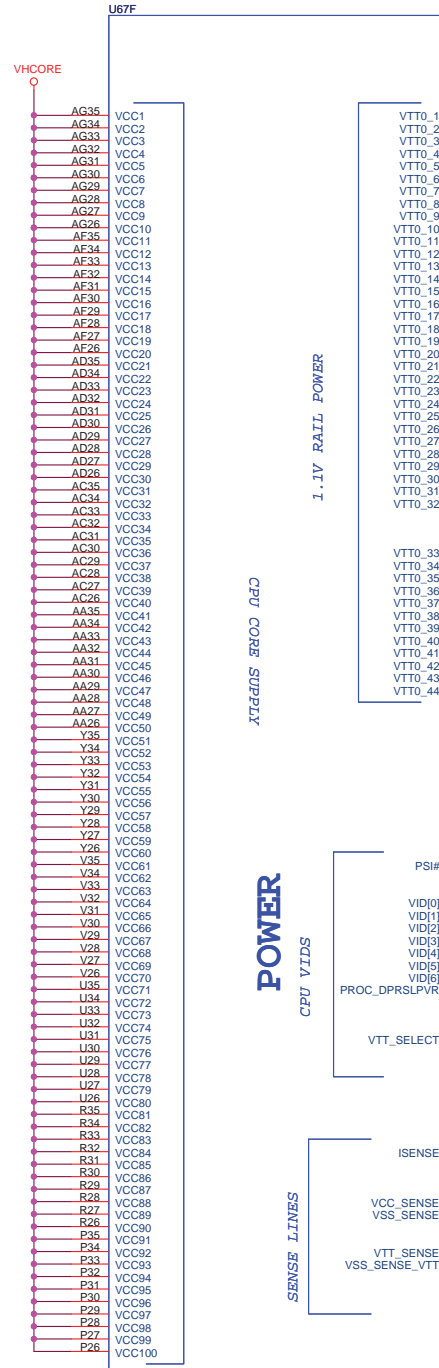
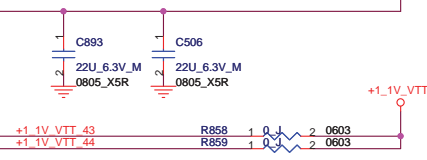


For RF Noise

18A(CFD SV) (VTT)



18A(CFD SV) (VTT)

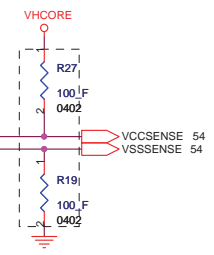
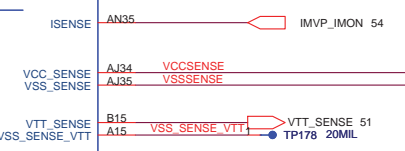
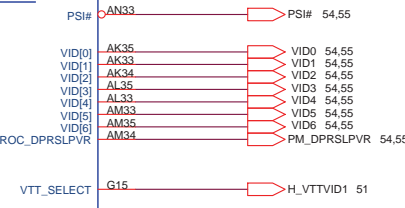
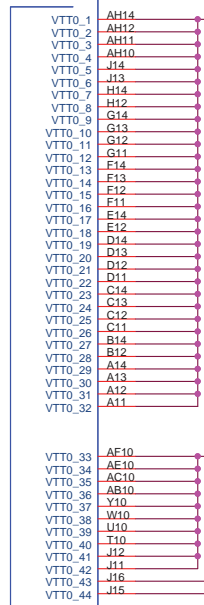


1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

SENSE LINES

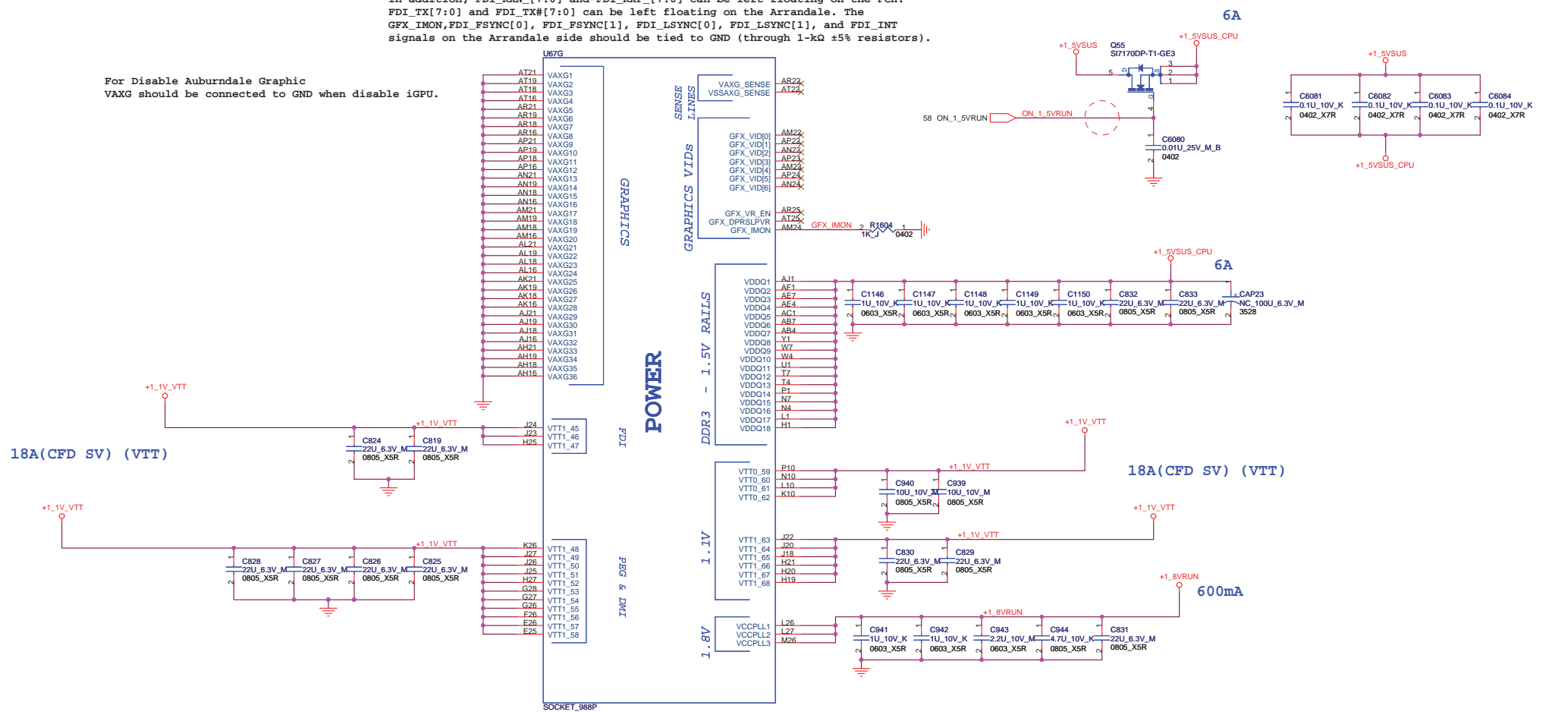


SOCKET_988P
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FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		ARD&CFD (POWER)	
Size	Document Number	Rev	
Custom	M931 (MBX-215)	SA	
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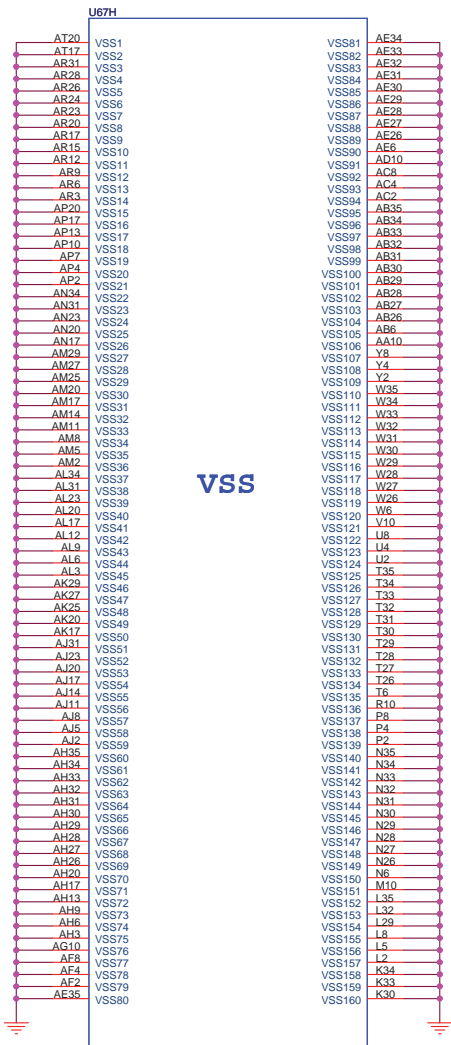
For Disable Auburndale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as not connect.
For Disable Auburndale Graphic
In addition, FDI_RXN[7:0] and FDI_RXP[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

For Disable Auburndale Graphic
VAXG should be connected to GND when disable iGPU.

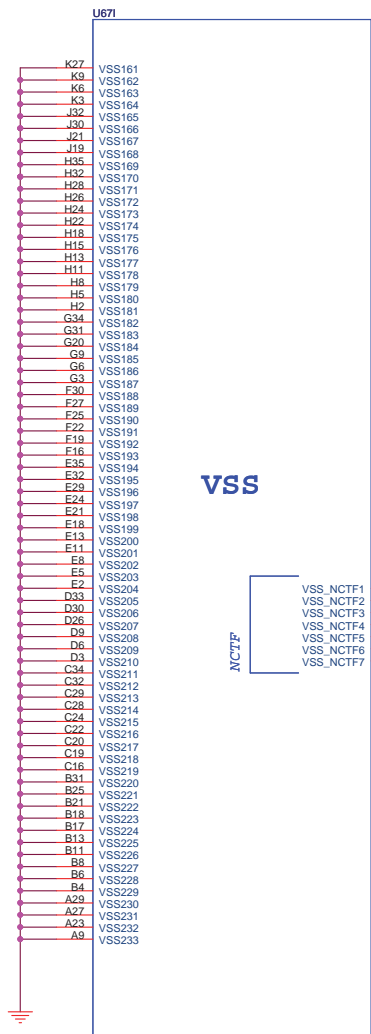


SOCKET_988P
FOX_PZ8827-364A-01F

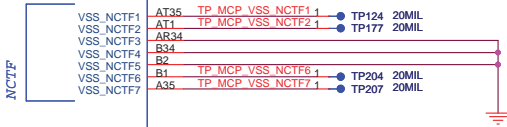
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ARD&FD (GRAPHICS POWER)		
Size	Document Number	Rev	
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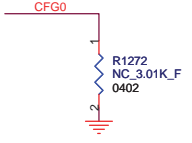
SOCKET_988P
FOX_PZ98827-364A-01F



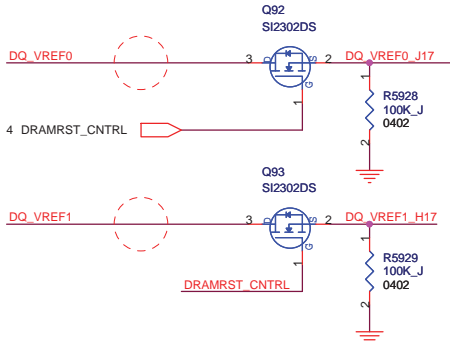
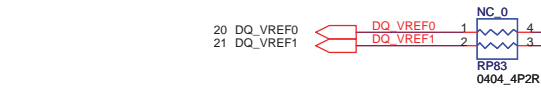
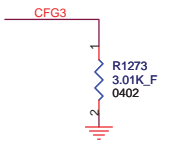
SOCKET_988P
FOX_PZ98827-364A-01F



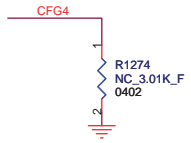
PCI Express Configuration Select
 CFG0 1 : Single PEG
 0 : Bifurcation enable



CFG3 PCI Express Static Lane Reversal
 CFG3 1 : Normal Operation
 0 : Lane Numbers Reversed
 15 -> 0 , 14 -> 1 , ...

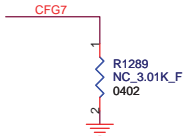


CFG4 Display Port Presence
 CFG4 1 : Disabled ; No Physical Display Port
 attached to Embedded Display Port
 0 : Enable ; An external Display Port device
 is connected to the Embedded Display Port



2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



- 20MIL TP305 ● 1 AP25
- 20MIL TP307 ● 1 AL25
- 20MIL TP306 ● 1 AL24
- 20MIL TP308 ● 1 AL22
- 20MIL TP310 ● 1 AJ33
- 20MIL TP309 ● 1 AG9
- 20MIL TP311 ● 1 M27
- 20MIL TP312 ● 1 L28
- 20MIL TP300 ● 1 G25
- 20MIL TP302 ● 1 G17
- 20MIL TP303 ● 1 E31
- 20MIL TP304 ● 1 E30

- 20MIL TP321 ● 1 CFG0
- 20MIL TP320 ● 1 CFG1
- 20MIL TP323 ● 1 CFG2
- 20MIL TP325 ● 1 CFG3
- 20MIL TP313 ● 1 AM30
- 20MIL TP315 ● 1 AM28
- 20MIL TP316 ● 1 AL30
- 20MIL TP317 ● 1 AN29
- 20MIL TP318 ● 1 AN32
- 20MIL TP354 ● 1 AK32
- 20MIL TP355 ● 1 AK31
- 20MIL TP356 ● 1 AK30
- 20MIL TP357 ● 1 AK32

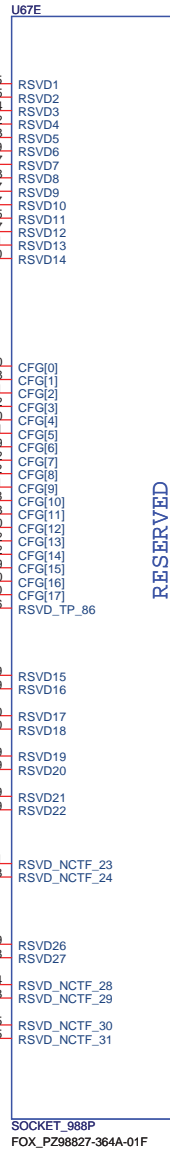
- 20MIL TP284 ● 1 B19
- 20MIL TP425 ● 1 A19
- 20MIL TP453 ● 1 A20
- 20MIL TP454 ● 1 B20

- 20MIL TP288 ● 1 U9
- 20MIL TP287 ● 1 T9
- 20MIL TP290 ● 1 AC9
- 20MIL TP289 ● 1 AB9

- 20MIL TP292 ● 1 C1
- 20MIL TP291 ● 1 A3

- 20MIL TP294 ● 1 J29
- 20MIL TP293 ● 1 J28
- 20MIL TP296 ● 1 A34
- 20MIL TP295 ● 1 A33

- 20MIL TP298 ● 1 C35
- 20MIL TP297 ● 1 B35



RESERVED

- RSVD32 ● 1 AJ13
- RSVD33 ● 1 TP238
- RSVD34 ● 1 AH25
- RSVD35 ● 1 TP256
- RSVD36 ● 1 AL26
- RSVD37 ● 1 TP258
- RSVD38 ● 1 AR2
- RSVD39 ● 1 TP257
- RSVD38 ● 1 AJ26
- RSVD39 ● 1 TP260
- RSVD38 ● 1 AJ27
- RSVD39 ● 1 TP259
- RSVD_NCTF_40 ● 1 AP1
- RSVD_NCTF_41 ● 1 TP262
- RSVD_NCTF_42 ● 1 AT2
- RSVD_NCTF_43 ● 1 TP261
- RSVD_NCTF_42 ● 1 AT3
- RSVD_NCTF_43 ● 1 TP264
- RSVD_NCTF_43 ● 1 AR1
- RSVD_NCTF_43 ● 1 TP263
- RSVD45 ● 1 AL28
- RSVD46 ● 1 TP109
- RSVD47 ● 1 AL29
- RSVD48 ● 1 TP193
- RSVD49 ● 1 AP30
- RSVD50 ● 1 TP181
- RSVD51 ● 1 AL27
- RSVD52 ● 1 TP208
- RSVD53 ● 1 AP32
- RSVD54 ● 1 TP209
- RSVD55 ● 1 AT31
- RSVD56 ● 1 TP211
- RSVD57 ● 1 AT32
- RSVD58 ● 1 TP210
- RSVD59 ● 1 AP33
- RSVD60 ● 1 TP212
- RSVD61 ● 1 AR33
- RSVD62 ● 1 TP213
- RSVD63 ● 1 AT33
- RSVD64 ● 1 TP235
- RSVD65 ● 1 AT34
- RSVD66 ● 1 TP214
- RSVD67 ● 1 AP35
- RSVD68 ● 1 TP236
- RSVD69 ● 1 AR35
- RSVD70 ● 1 TP266
- RSVD71 ● 1 AR32
- RSVD72 ● 1 TP265
- RSVD_TP_59 ● 1 E15
- RSVD_TP_60 ● 1 TP237
- RSVD_TP_60 ● 1 TP239
- RSVD62 ● 1 D15
- RSVD63 ● 1 TP328
- RSVD64 ● 1 C15
- RSVD65 ● 1 TP329
- RSVD66 ● 1 AJ15
- RSVD67 ● 1 TP386
- RSVD68 ● 1 AH15
- RSVD69 ● 1 TP390
- RSVD_TP_66 ● 1 AA5
- RSVD_TP_67 ● 1 TP331
- RSVD_TP_68 ● 1 R8
- RSVD_TP_69 ● 1 TP332
- RSVD_TP_70 ● 1 AD3
- RSVD_TP_71 ● 1 TP333
- RSVD_TP_72 ● 1 AD2
- RSVD_TP_73 ● 1 TP334
- RSVD_TP_74 ● 1 AA1
- RSVD_TP_75 ● 1 TP335
- RSVD_TP_76 ● 1 AA2
- RSVD_TP_77 ● 1 TP336
- RSVD_TP_78 ● 1 AA1
- RSVD_TP_79 ● 1 TP337
- RSVD_TP_80 ● 1 AG7
- RSVD_TP_81 ● 1 TP338
- RSVD_TP_82 ● 1 AE3
- RSVD_TP_83 ● 1 TP340
- RSVD_TP_84 ● 1 V4
- RSVD_TP_85 ● 1 TP341
- RSVD_TP_86 ● 1 V5
- RSVD_TP_87 ● 1 TP342
- RSVD_TP_88 ● 1 N2
- RSVD_TP_89 ● 1 TP343
- RSVD_TP_90 ● 1 AD5
- RSVD_TP_91 ● 1 TP344
- RSVD_TP_92 ● 1 AD7
- RSVD_TP_93 ● 1 TP347
- RSVD_TP_94 ● 1 W3
- RSVD_TP_95 ● 1 TP348
- RSVD_TP_96 ● 1 W2
- RSVD_TP_97 ● 1 TP349
- RSVD_TP_98 ● 1 N3
- RSVD_TP_99 ● 1 TP350
- RSVD_TP_100 ● 1 AE5
- RSVD_TP_101 ● 1 TP345
- RSVD_TP_102 ● 1 AD9
- RSVD_TP_103 ● 1 TP346

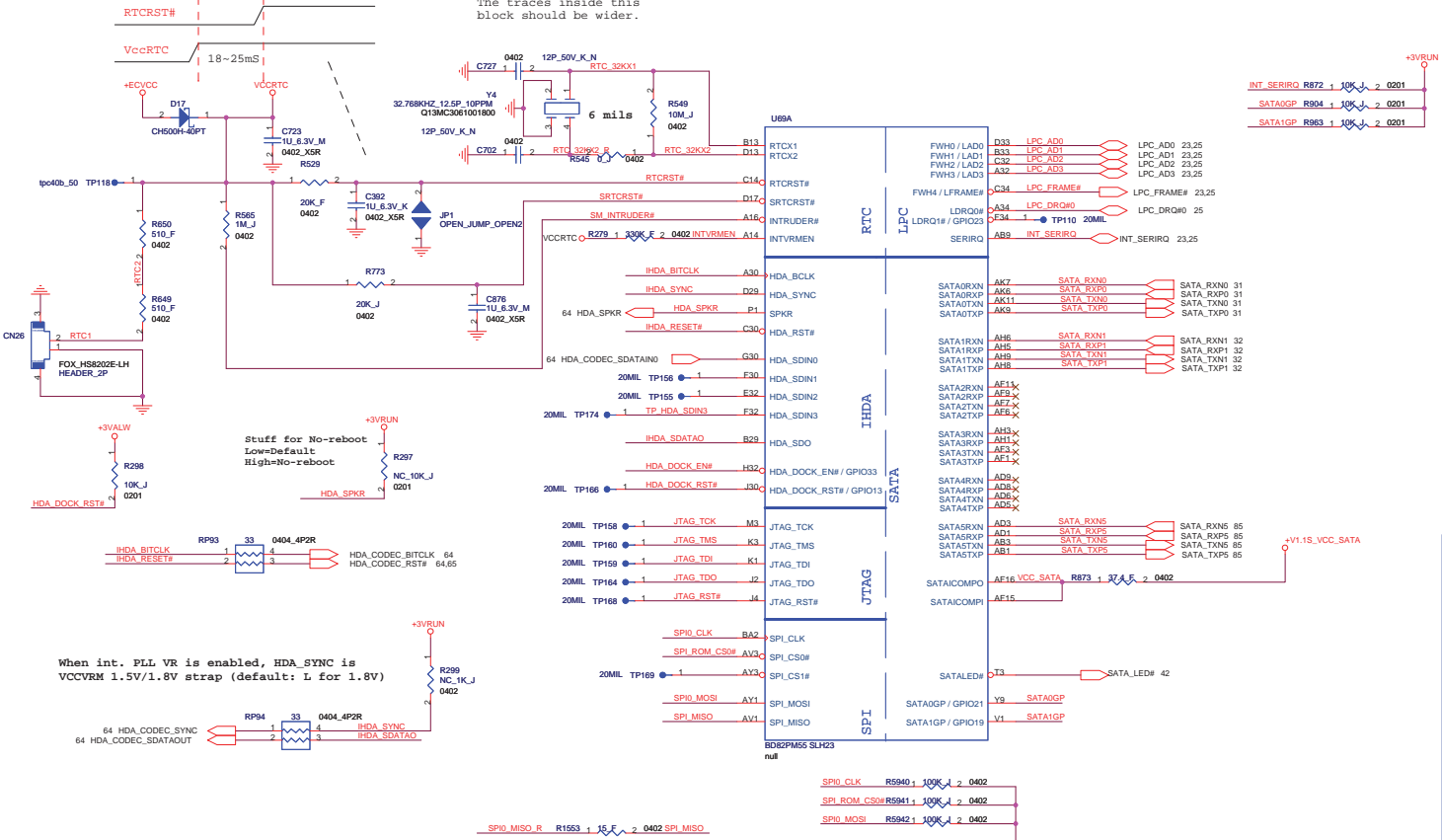
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **ARD&CFD (RESERVED)**

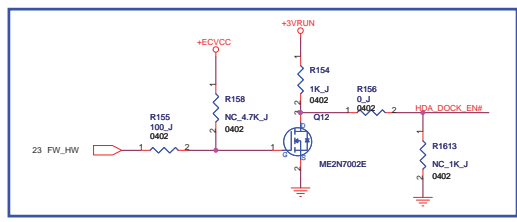
Size: A3 Document Number: **M931 (MBX-215)** Rev: **SA**

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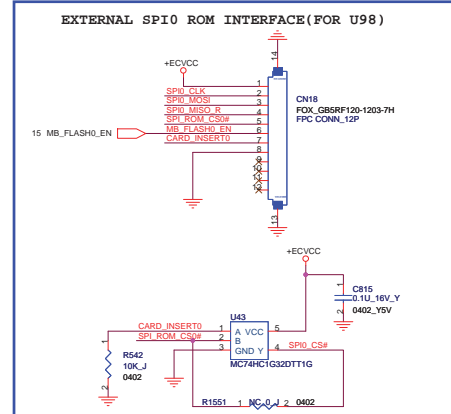
The traces inside this block should be wider.



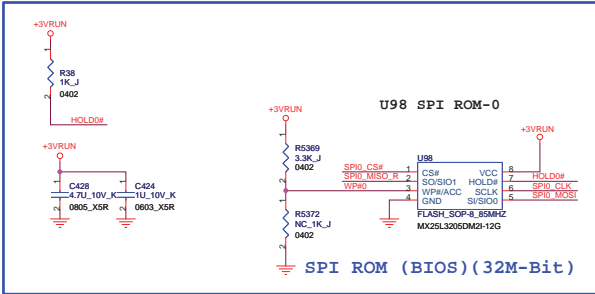
[HDA_DOCK_EN#/GPIO33]
 Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
 High (1) - Security measure defined in the Flash Descriptor will be enabled



For MP, Dummy CN18, C815, U43, R542, Stuff R1551

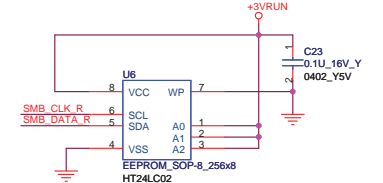
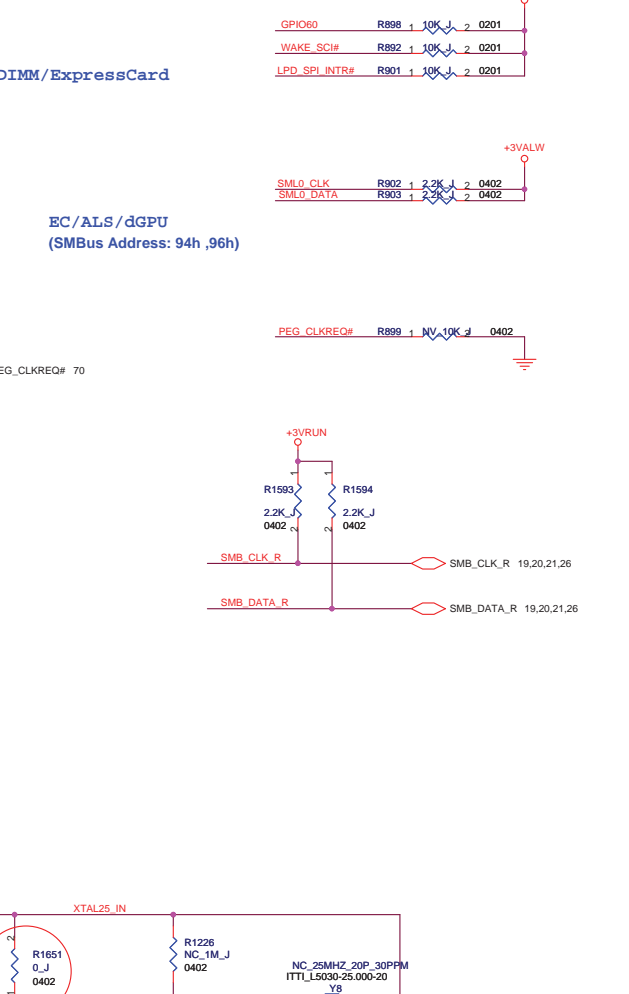
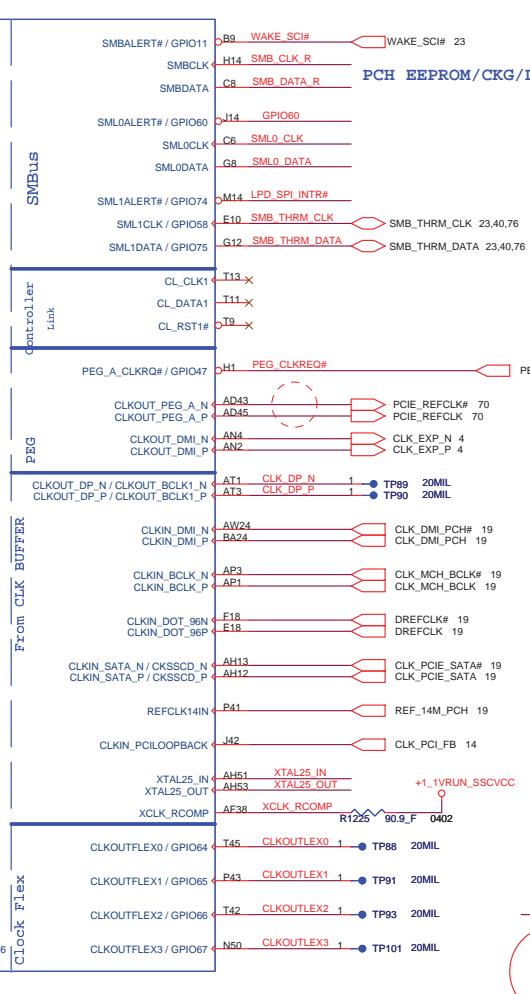
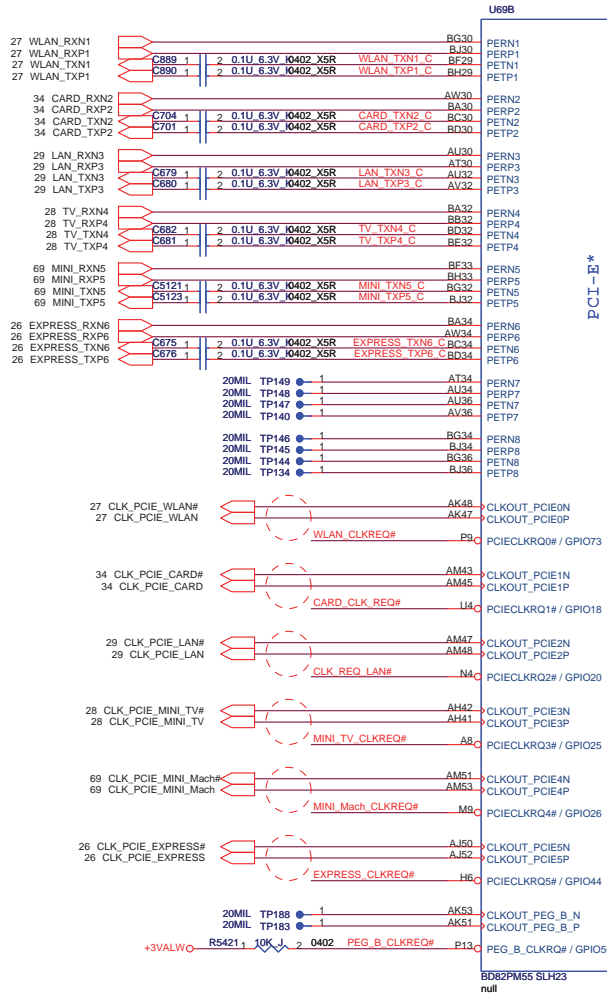


<http://laptop-motherboard-schematic.blogspot.com/>



PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	ISDB-T Tuner (JP)
Port5	Mach
Port6	ExpressCard/34 (PCI-E)
Port7	NC
Port8	NC



Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044).
XTAL_IN should be pulled to GND via a 0ohm by default.
This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **PCH (PCI-E,SMBUS,CLK)**

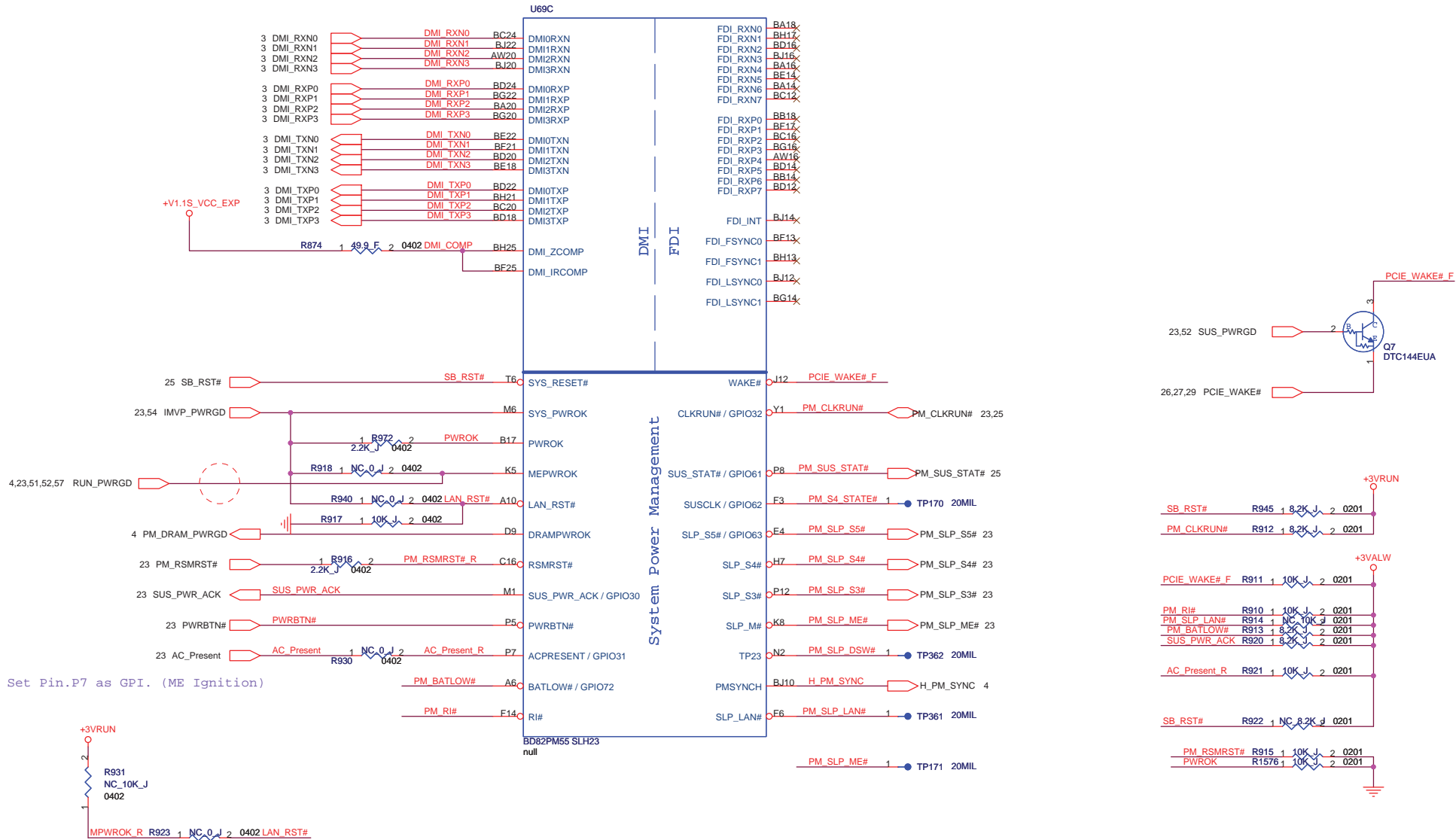
Size: Document Number

Custom: **M931 (MBX-215)**

Date: Wednesday, January 06, 2010 | Sheet 11 of 93

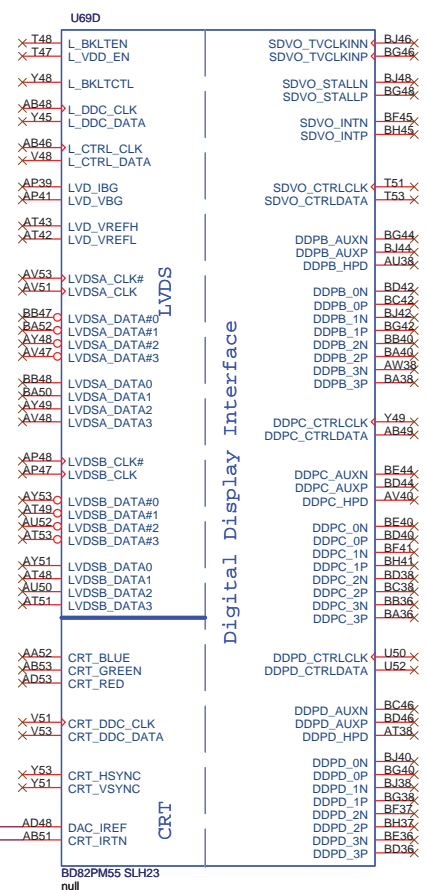
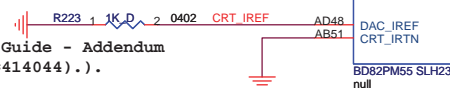
Rev: **SA**

For Disable Auburndale Graphic
 In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
 FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
 GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
 signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

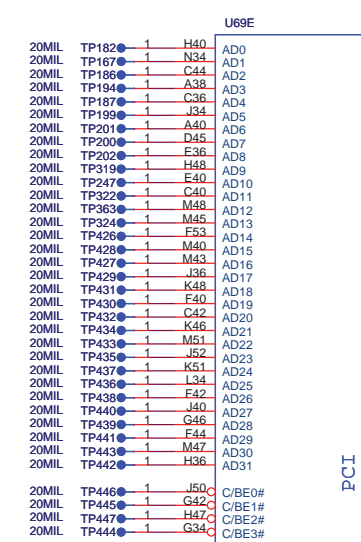
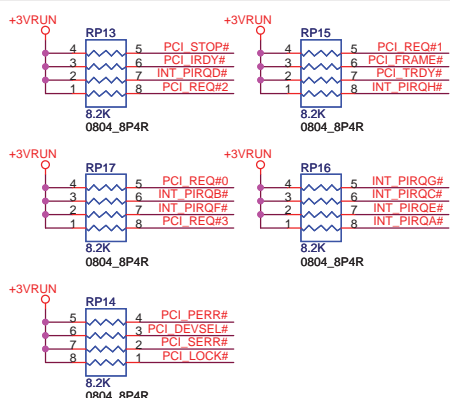


Set Pin.P7 as GPI. (ME Ignition)

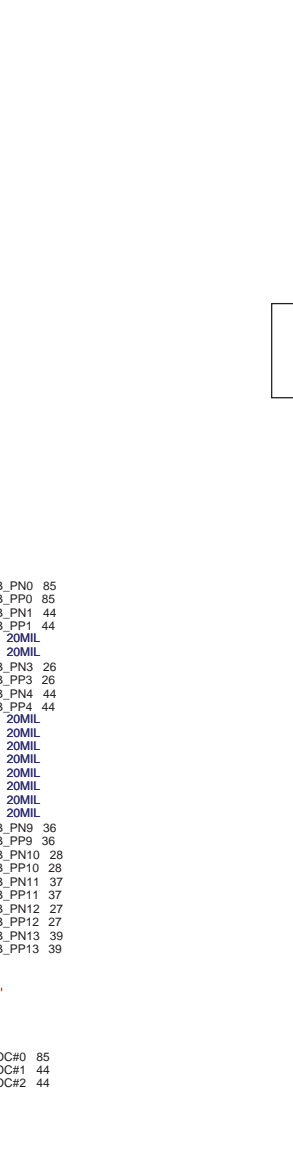
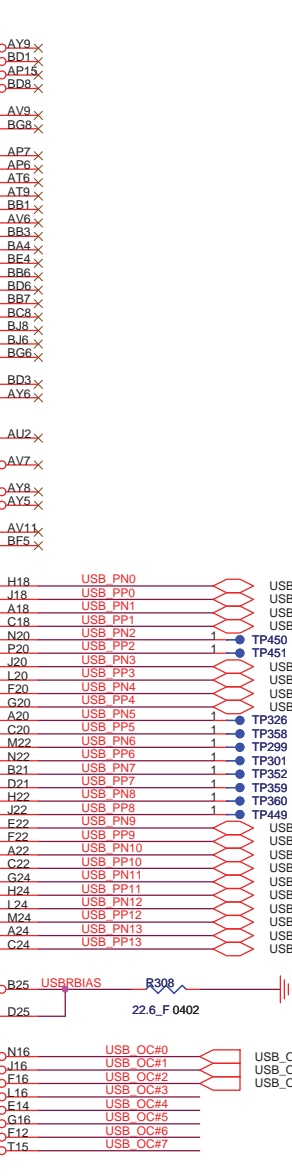
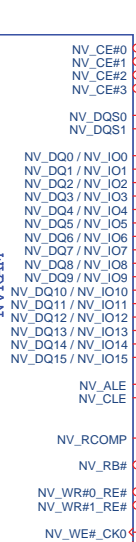
Calpella Platform - Design Guide - Addendum
 / Update - Rev. 1.52 (Doc #414044)..



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title PCH (LVDS, DDI)			
Size	Document Number		Rev
Custom	M931 (MBX-215)		SA
Date:	Wednesday, January 06, 2010	Sheet	13 of 93



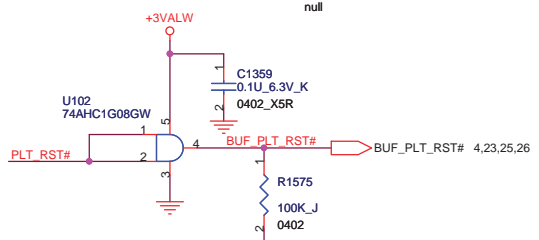
U69E
BD82PM55 SLH23
null



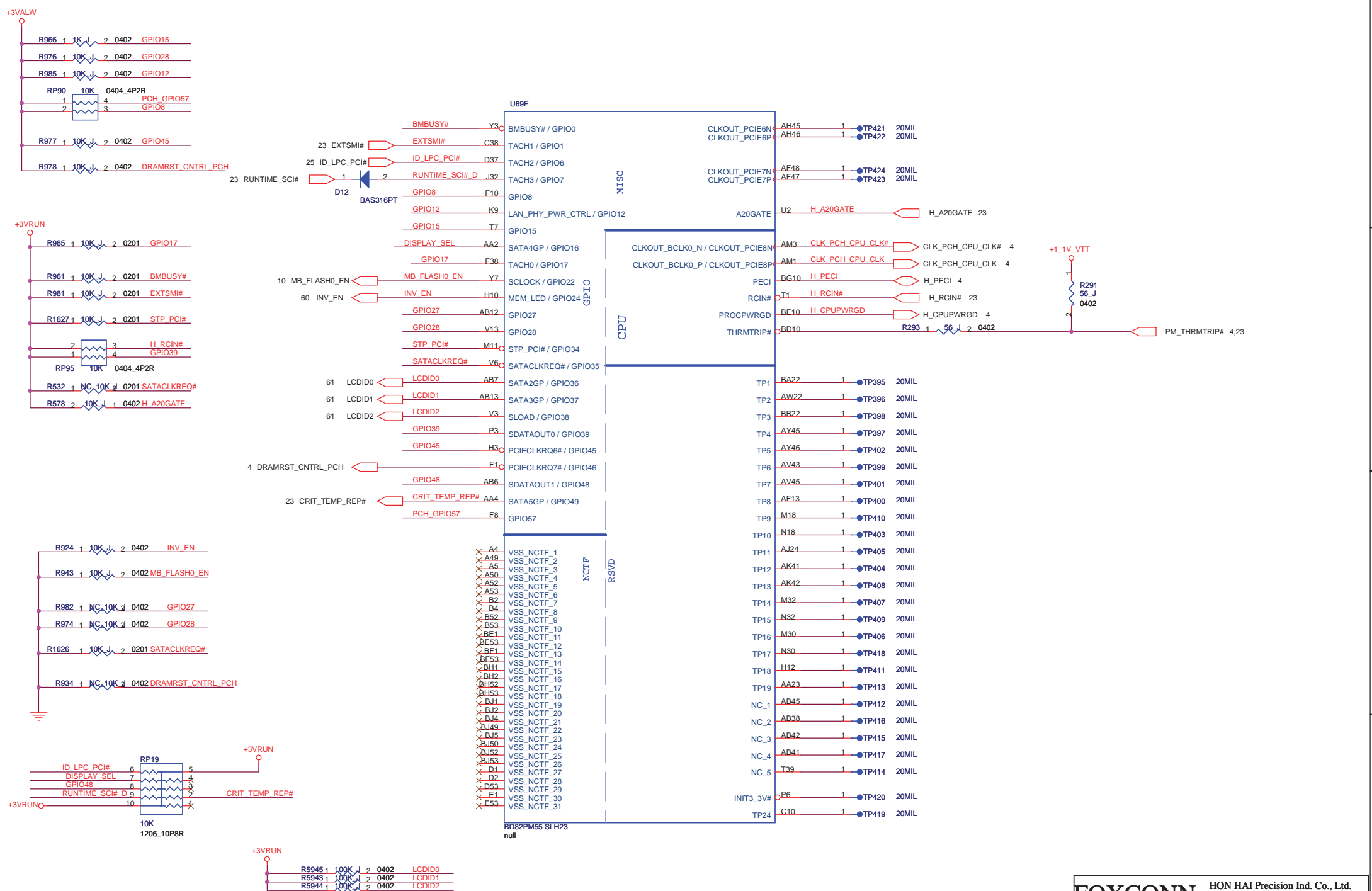
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Intel Anti-Theft Technology
Disabled when Low , NC R1616
Enabled when High , Stuff R1616

USB PORT	Function
PORT-0	On Board Port
PORT-1	External Port
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	IR Receiver (JP)
PORT-11	Felica
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth



Buffer to reduce loading on PLT_RST#.

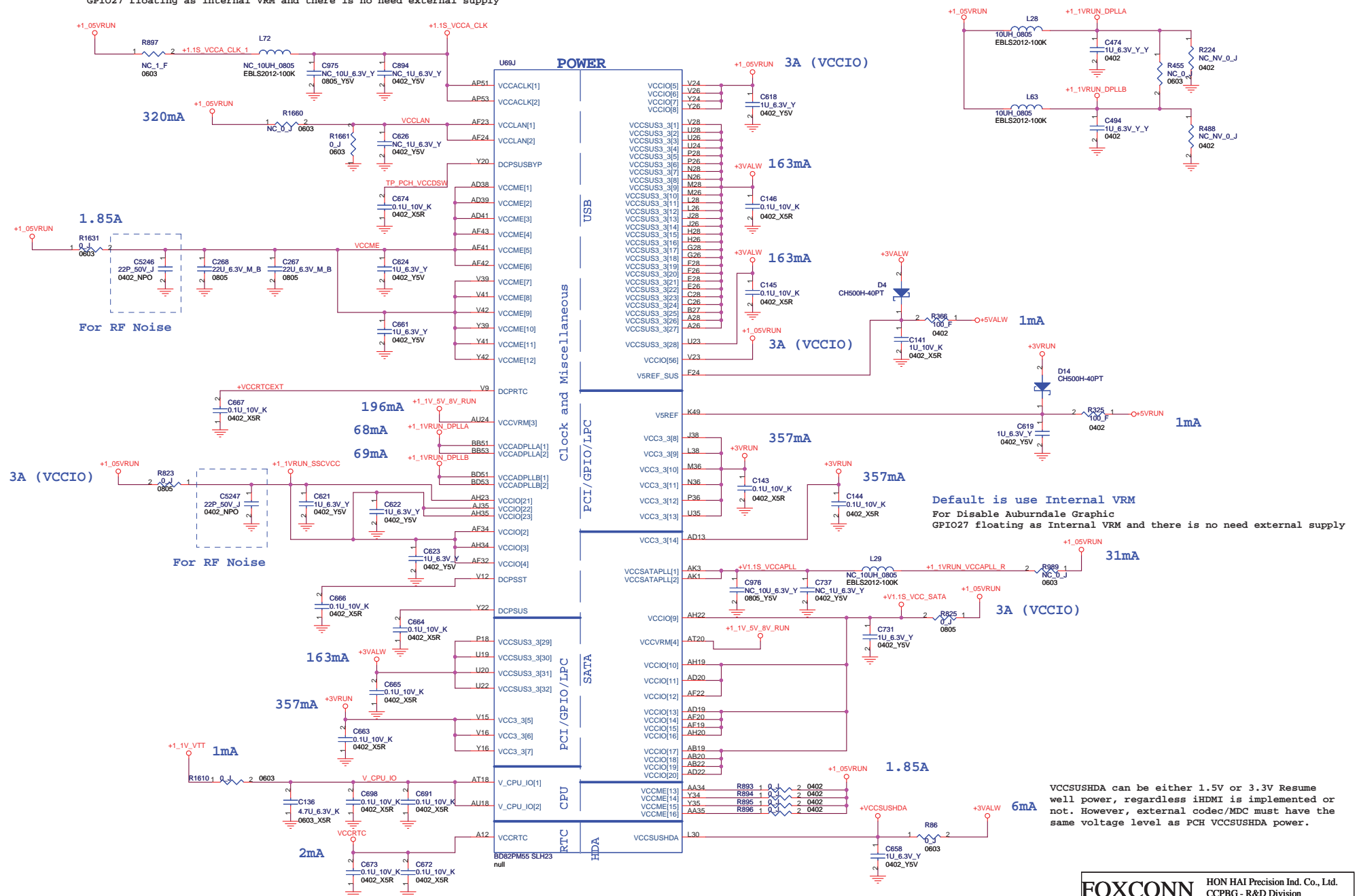


SW1 for BFT JIG Reserved.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title PCH (GPIO, VSS NCTF, RSVD)			
Size A3	Document Number	Rev SA	
Date	M931 (MBX-215)	Wednesday, January 06, 2010	Sheet 15 of 93

Default is use Internal VRM

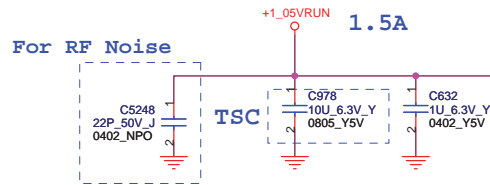
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



Default is use Internal VRM
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply

VCCSUSHDA can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.

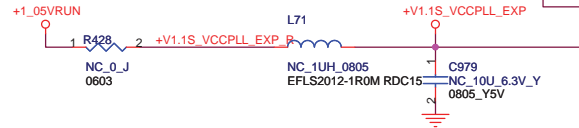
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
File	PCH (POWER) 1/2		
Size	Document Number		
Custom	M931 (MBX-215)		
Date:	Wednesday, January 06, 2010	Sheet	16 of 93
			Rev SA



3A (VCCIO)

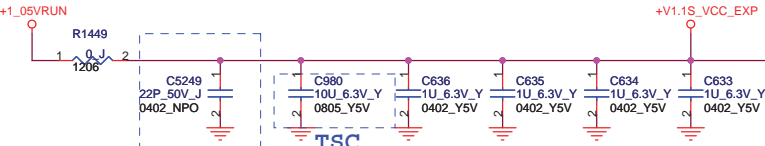
Default is use Internal VRM

For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



3A (VCCIO)

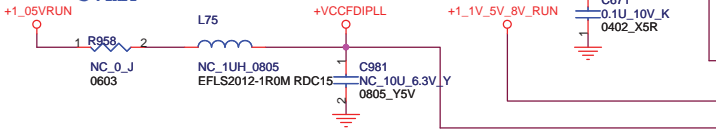
For RF Noise



37mA

200mA

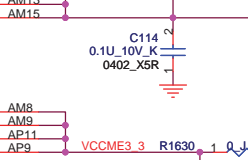
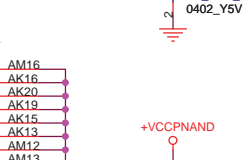
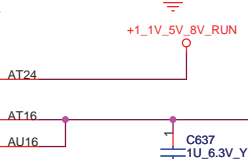
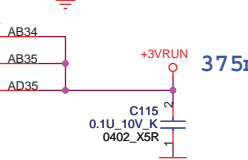
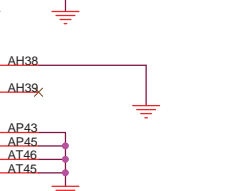
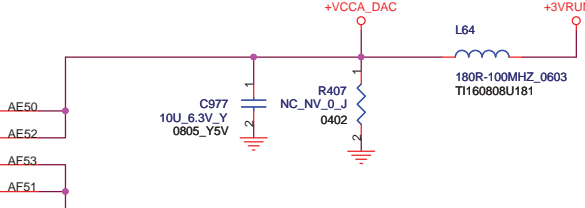
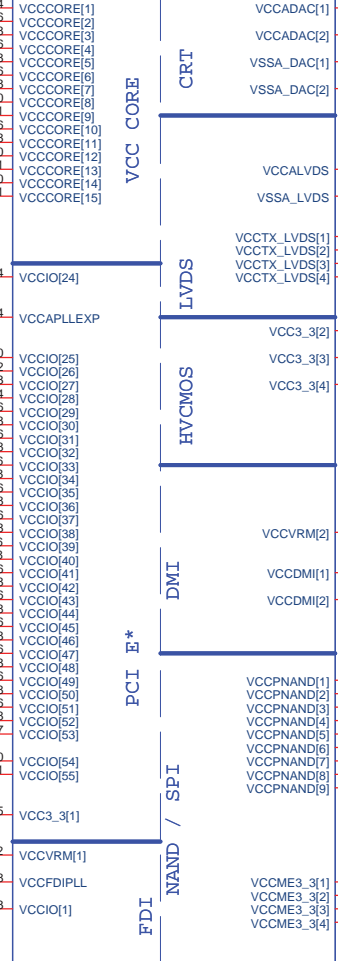
375mA



Default is use Internal VRM

For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply

POWER



+VCCA_DAC
+3VRUN 70mA



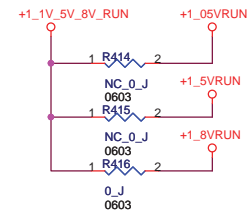
375mA

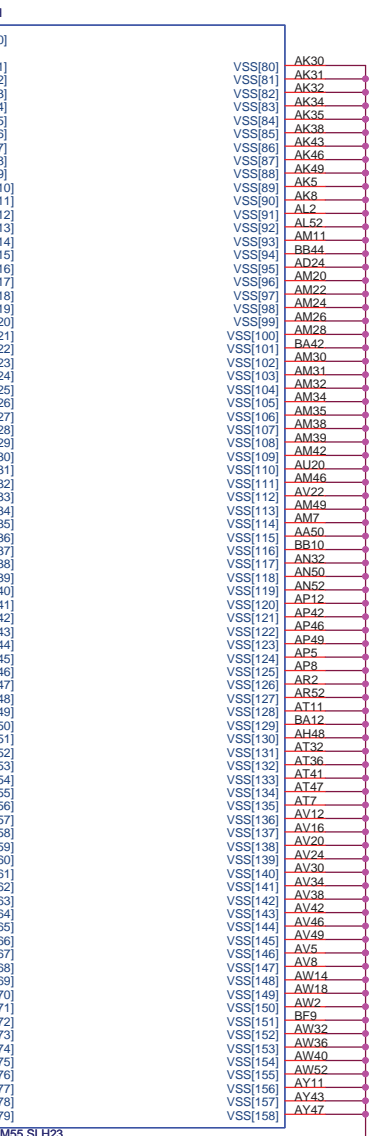
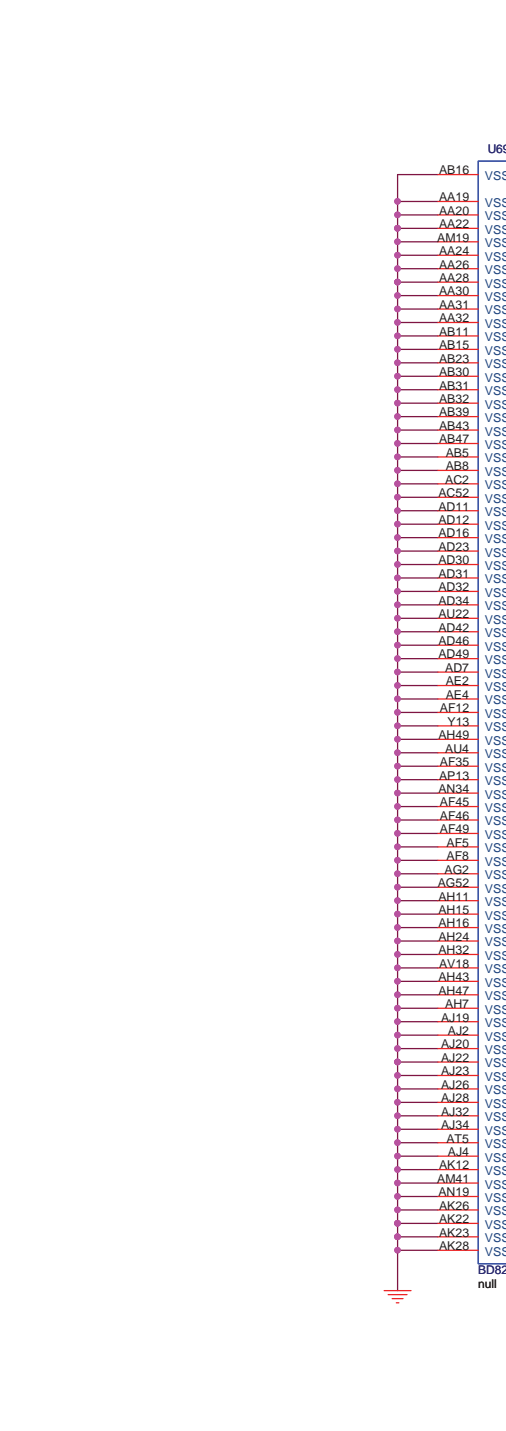
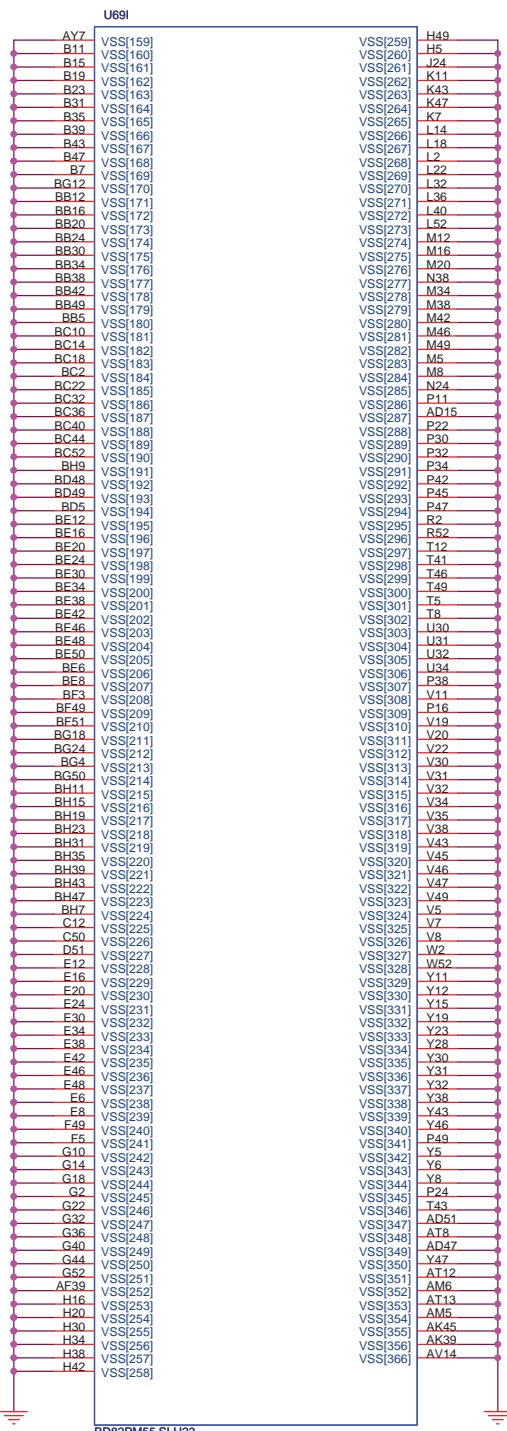
200mA

61mA

156mA

1.85A

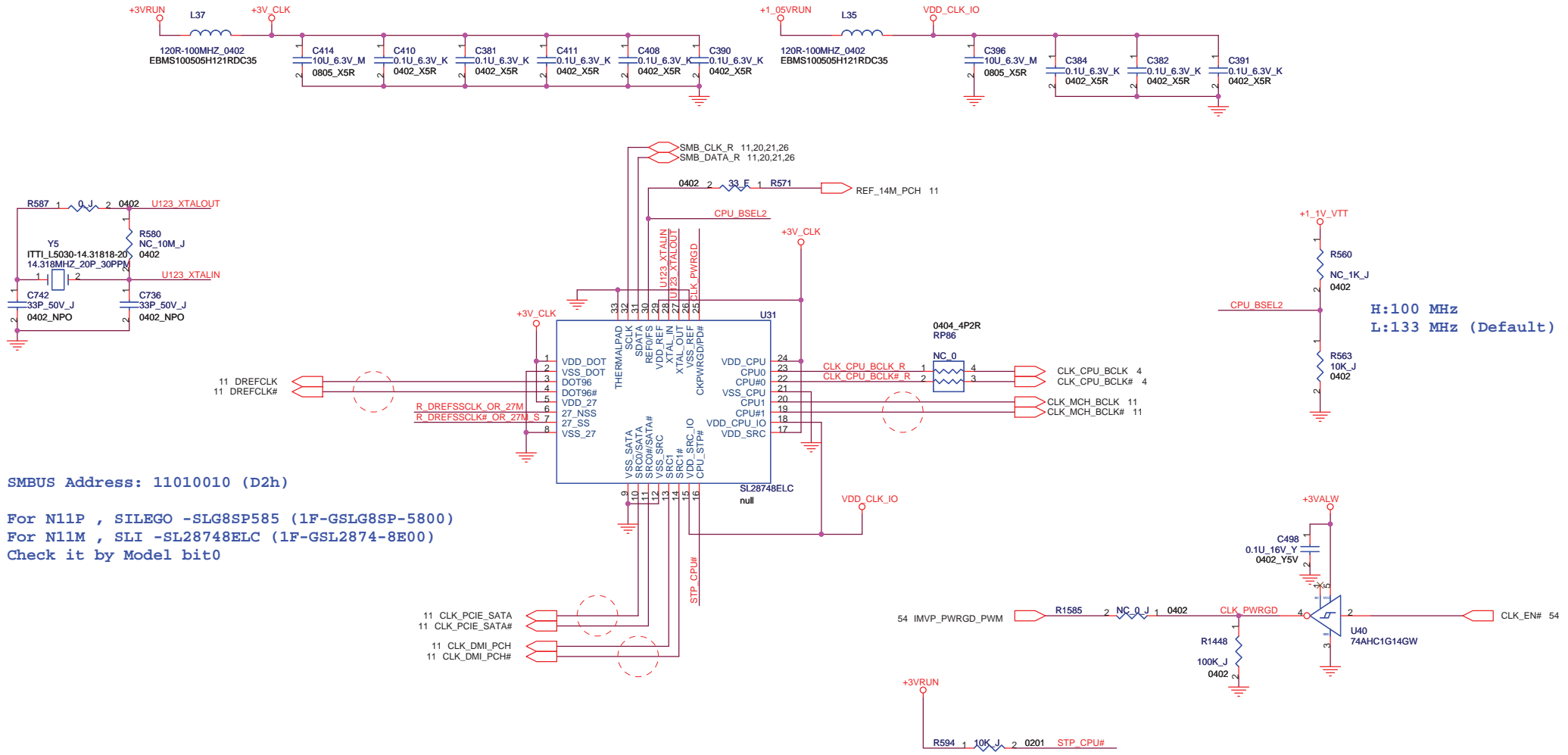




BD82PM55 SLH23
null

BD82PM55 SLH23
null

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title PCH (VSS)			
Size A3	Document Number M931 (MBX-215)	Rev SA	
Date: Wednesday, January 06, 2010	Sheet 18	of 93	



H:100 MHz
L:133 MHz (Default)

SMBUS Address: 11010010 (D2h)

For N11P , SILEGO -SLG8SP585 (1F-GSLG8SP-5800)
For N11M , SLI -SL28748ELC (1F-GSL2874-8E00)
Check it by Model bit0

Frequency Select Pin (FS)

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						







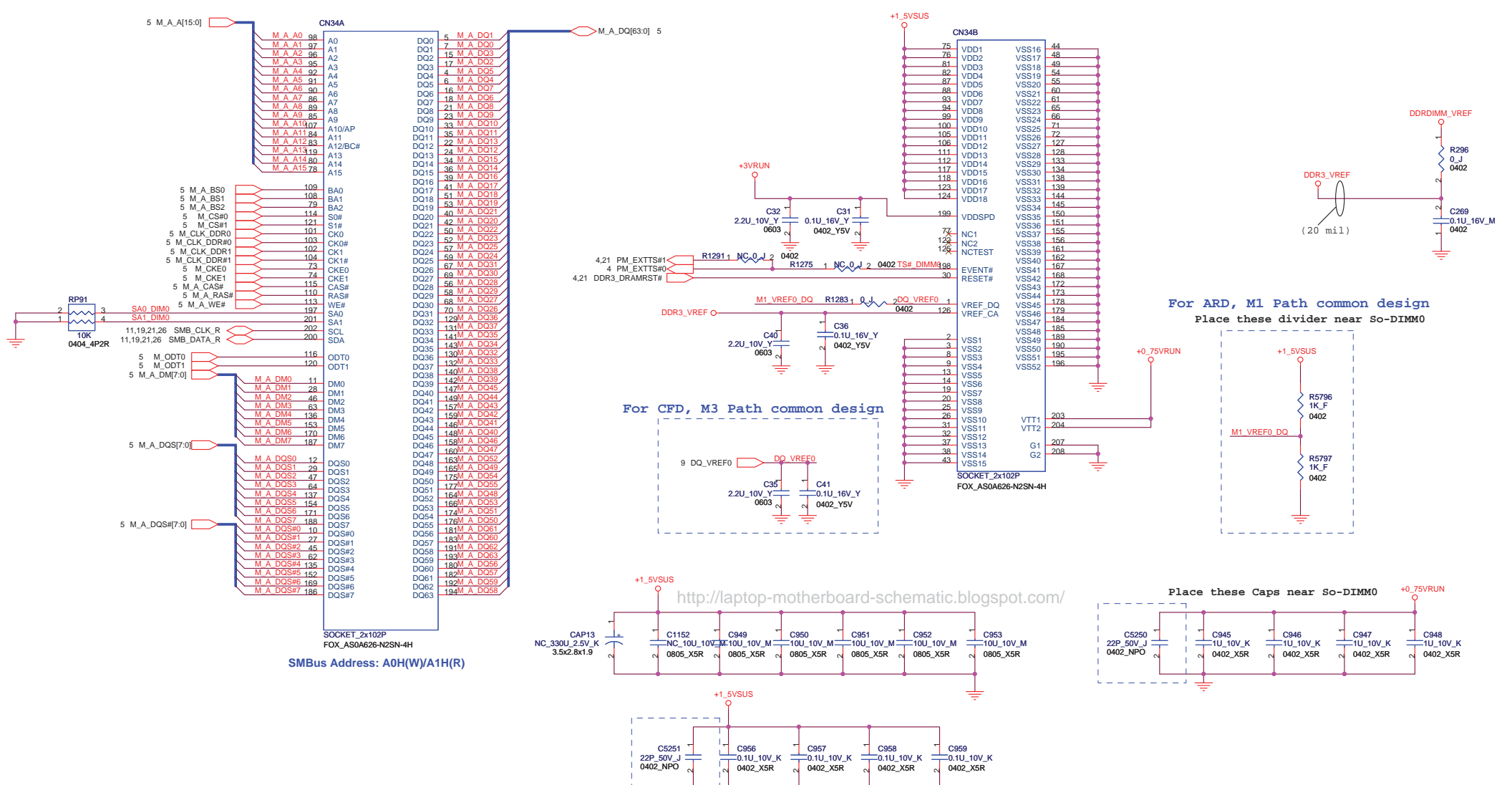
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **CLOCK GEN**

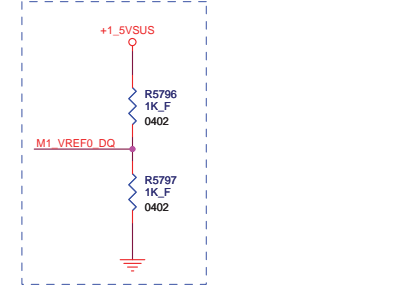
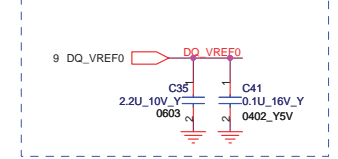
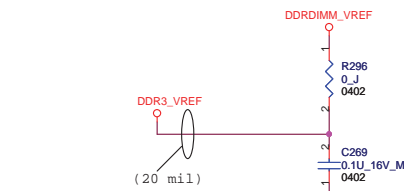
Size: Document Number
A3: **M931 (MBX-215)** Rev: **SA**

Date: Wednesday, January 06, 2010 | Sheet 19 of 93

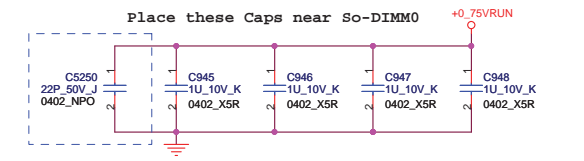
 M_A_DM[0..7] 5
 M_A_DQS[7..0] 5
 M_A_DQS# [7..0] 5
 M_A_A[0..14] 5



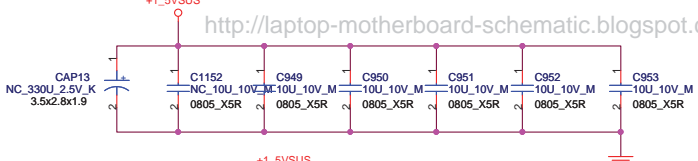
For ARD, M1 Path common design
Place these divider near So-DIMM0



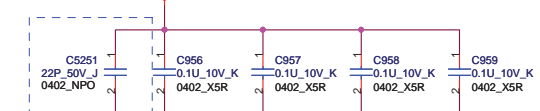
Place these Caps near So-DIMM0



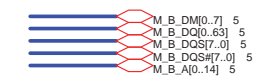
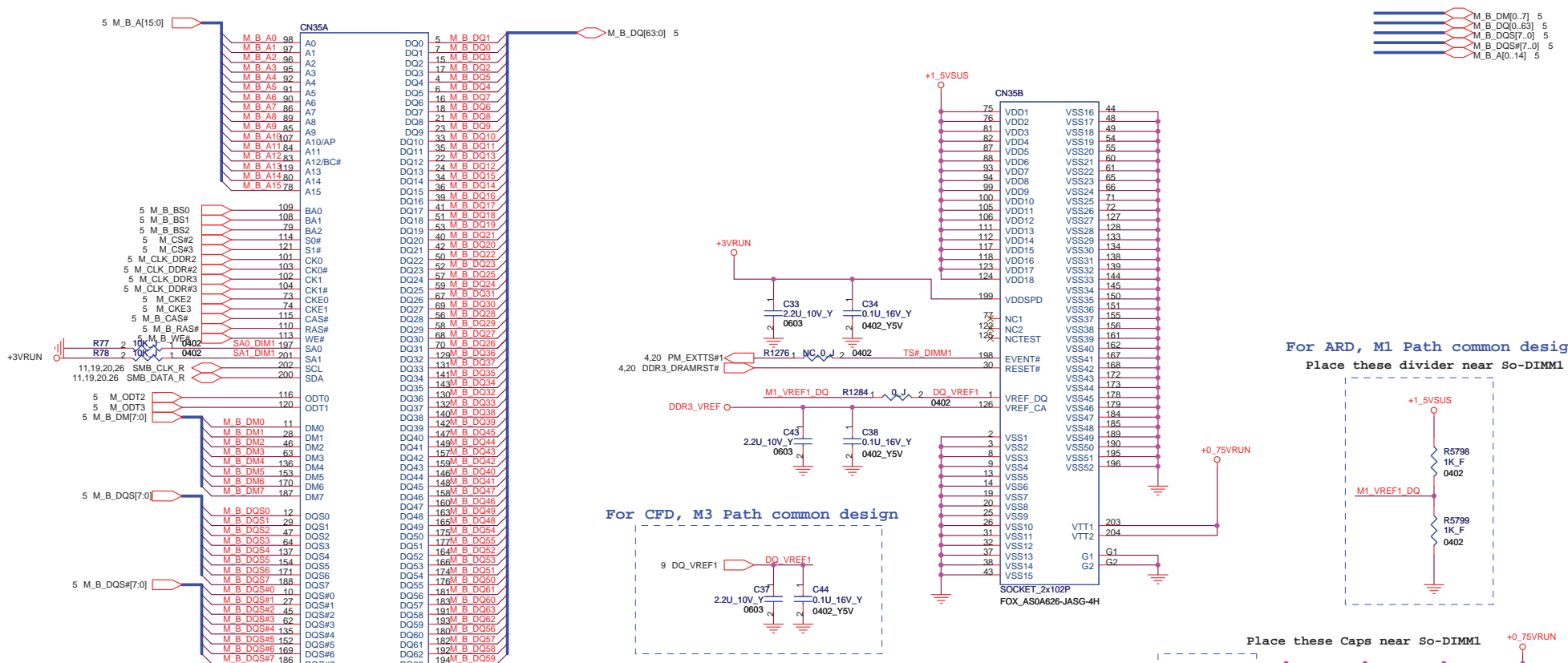
<http://laptop-motherboard-schematic.blogspot.com/>



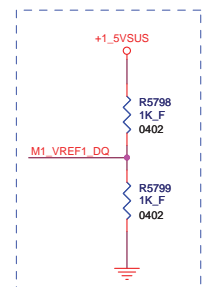
For RF Noise



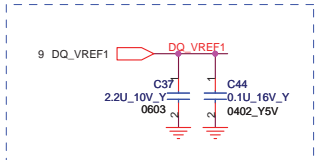
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R & D Division	
DDR3(SO-DIMM 0) 1/3			
Size	Document Number	Rev	
Custom	M931 (MBX-215)	SA	
Date:	Wednesday, January 06, 2010	Sheet	20 of 93



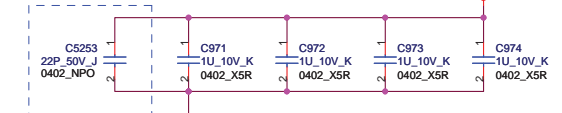
For ARD, M1 Path common design
Place these divider near So-DIMM1



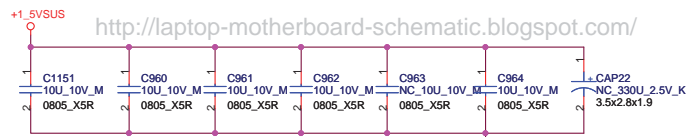
For CFD, M3 Path common design



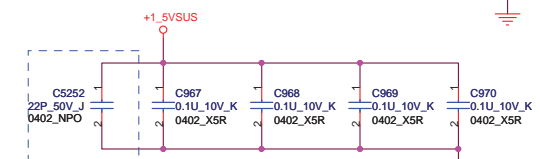
Place these Caps near So-DIMM1



For RF Noise



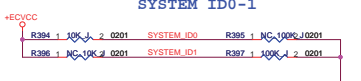
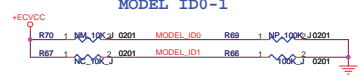
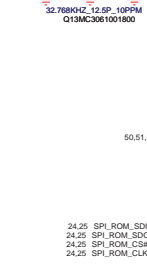
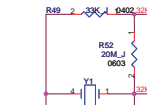
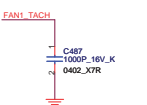
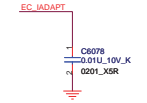
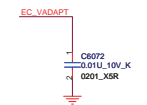
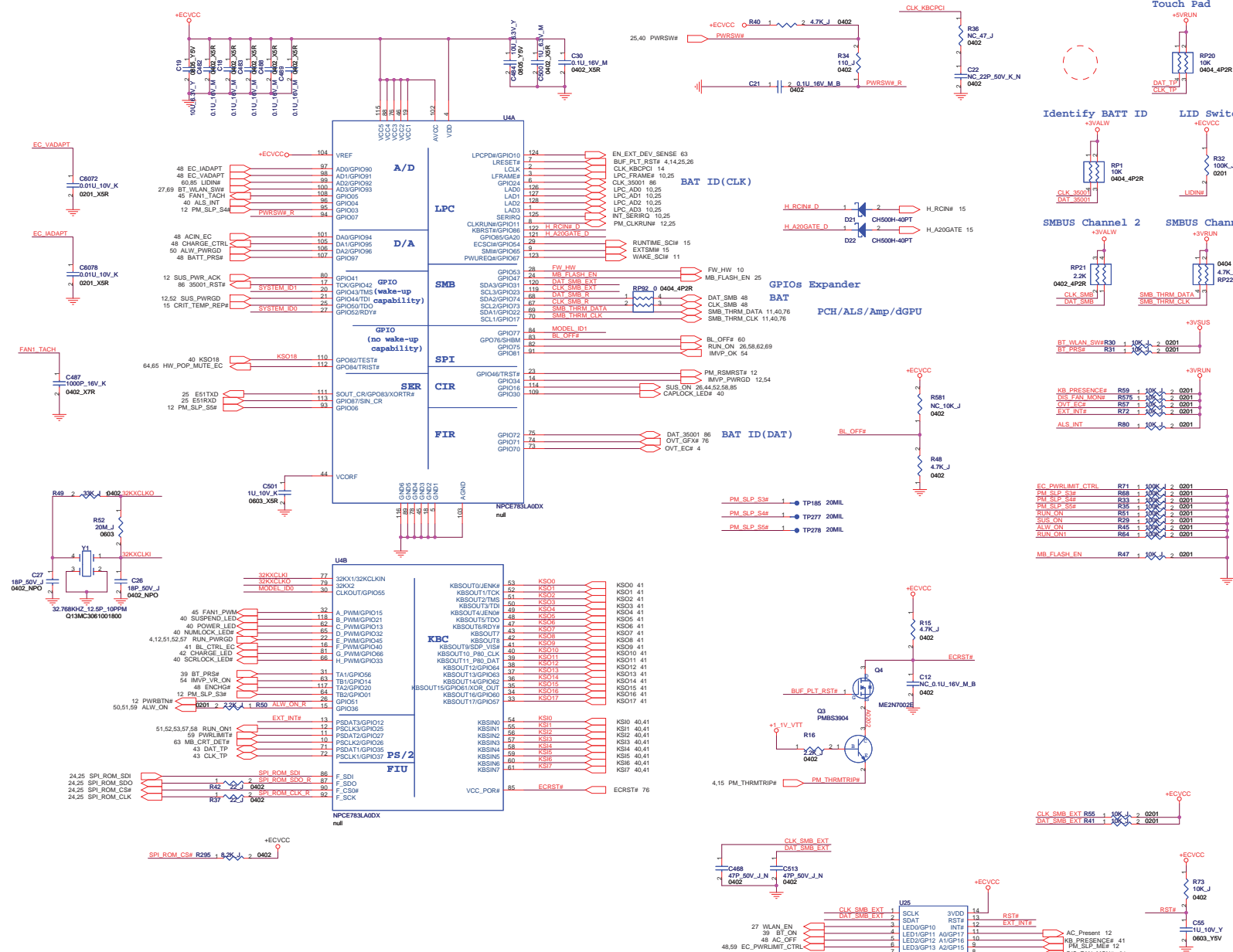
For RF Noise



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DDRIII(SO-DIMM 1) 2/3			
Size	Document Number		Rev
Custom	M931 (MBX-215)		SA
Date:	Wednesday, January 06, 2010	Sheet	21 of 93

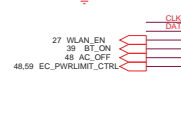
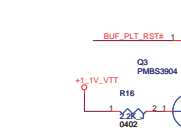
Delete M2 Path (Intel Revised)

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title		SO-DIMM VREF 3/3	
Size	Document Number	Rev	
A3	M931 (MBX-215)	SA	
Date:	Wednesday, January 06, 2010	Sheet	22 of 93

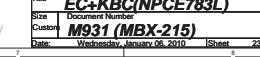
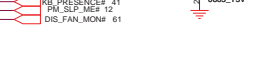
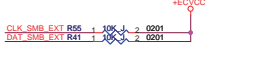
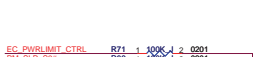
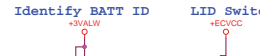
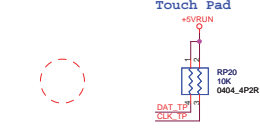


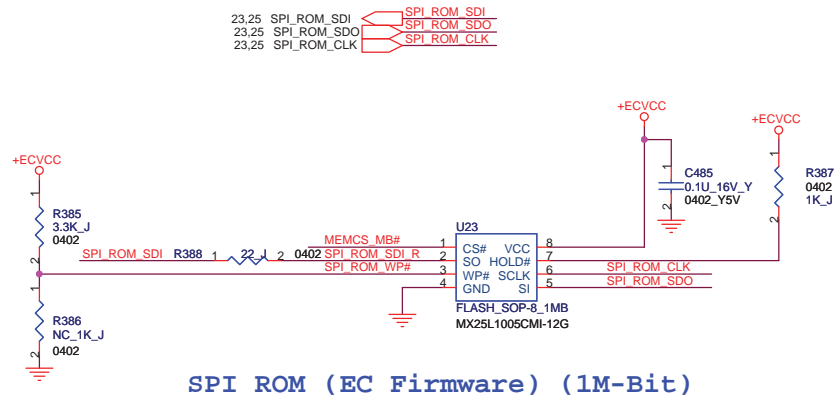
ID1 (Reserve)	ID0	SKU
0	0	SLI+N11P-GE1
0	1	SILEGO+N11M-GE1
1	0	
1	1	

ID1	ID0	Model Name
0	0	M930
0	1	M931
1	0	Reserve
1	1	Reserve

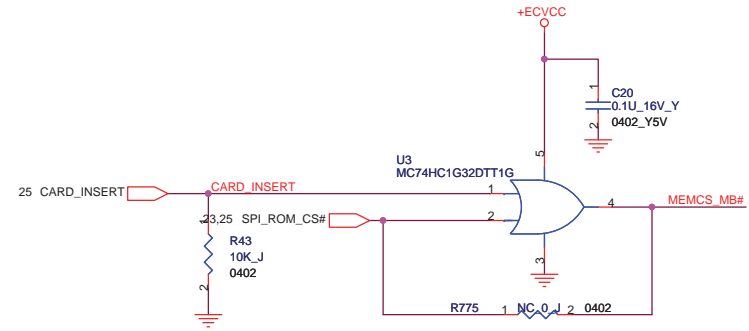


SMBus Address: 0x30h

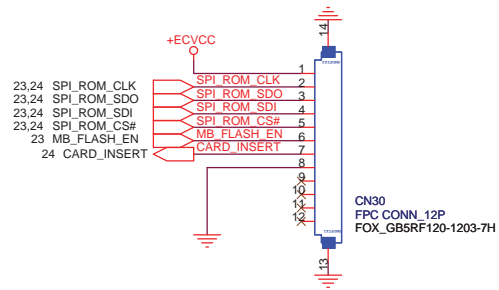




SPI ROM (EC Firmware) (1M-Bit)

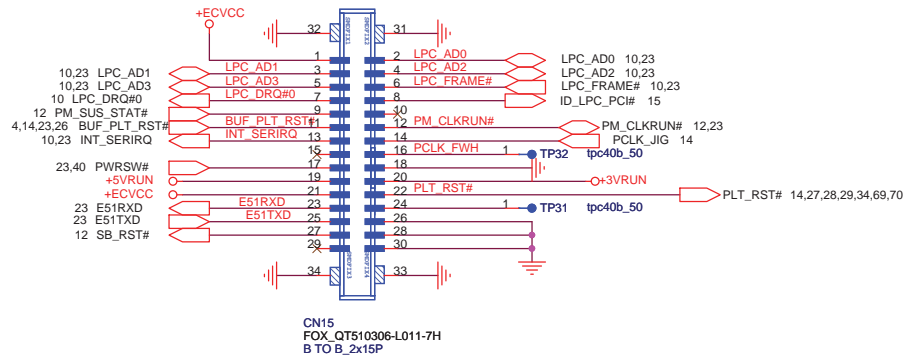


For MP, Dummy R43, C20 ,U3 ,CN30 and Stuff R775



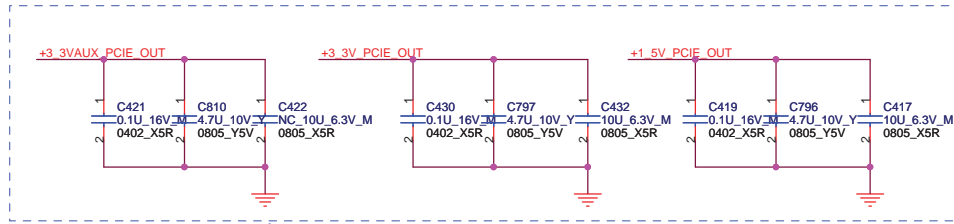
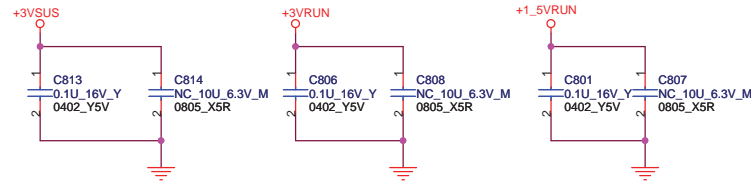
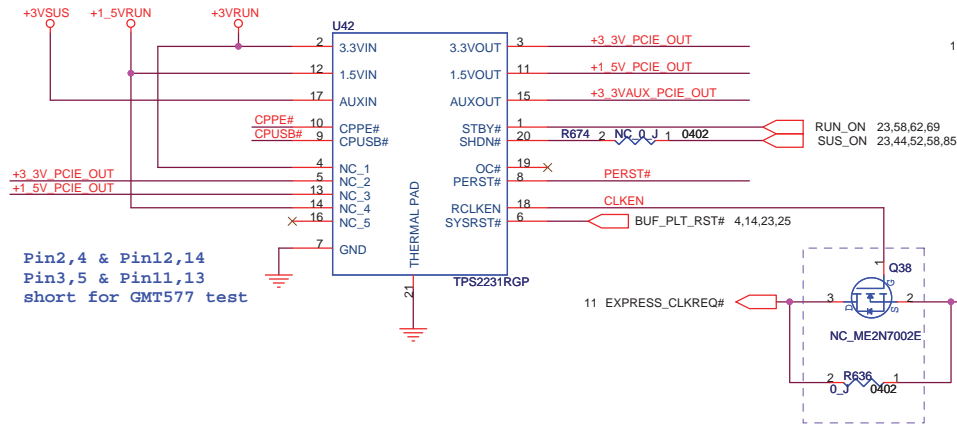
EXTERNAL SPI ROM INTERFACE (EC)

For MP, Dummy R43, C20 ,U3 ,CN30 and Stuff R775

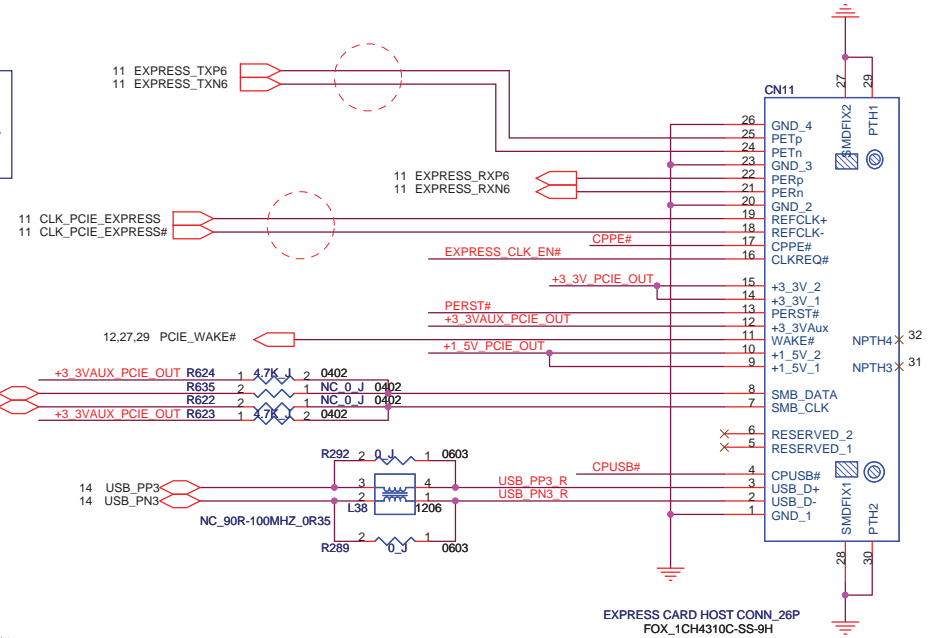


JIG-120

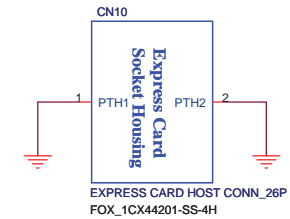
+1_5V=>0.65A
 +3_3VAux=>0.275A
 +3_3V=>1.3A



Place near by CN11 Pin.

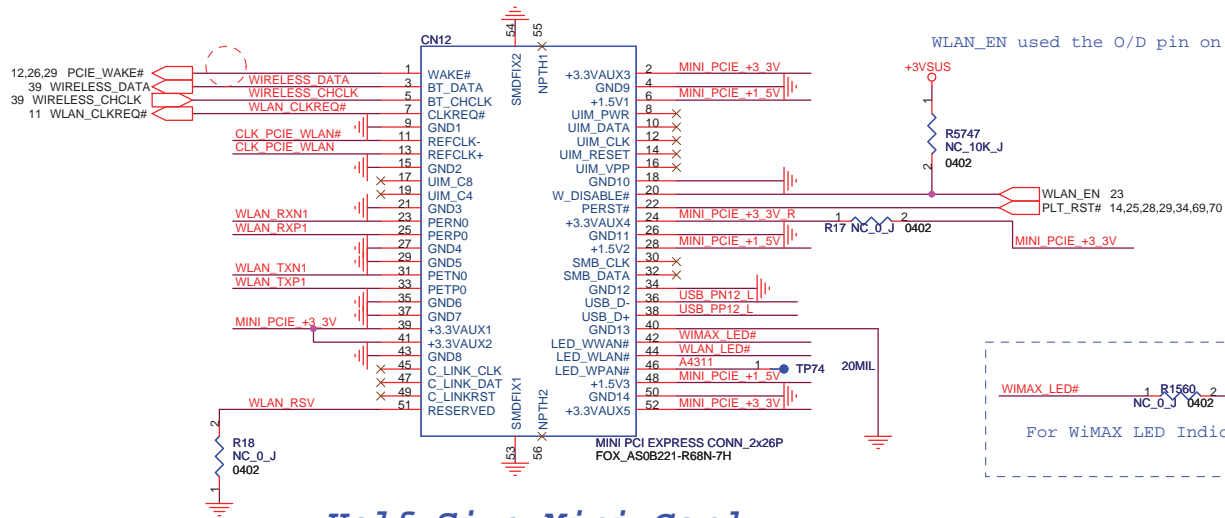
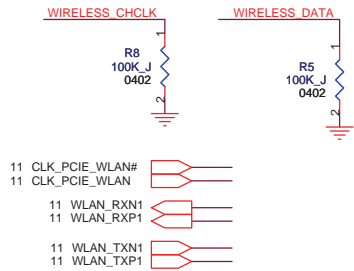


Express Card Slot.

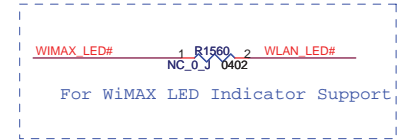


Express Card Housing.

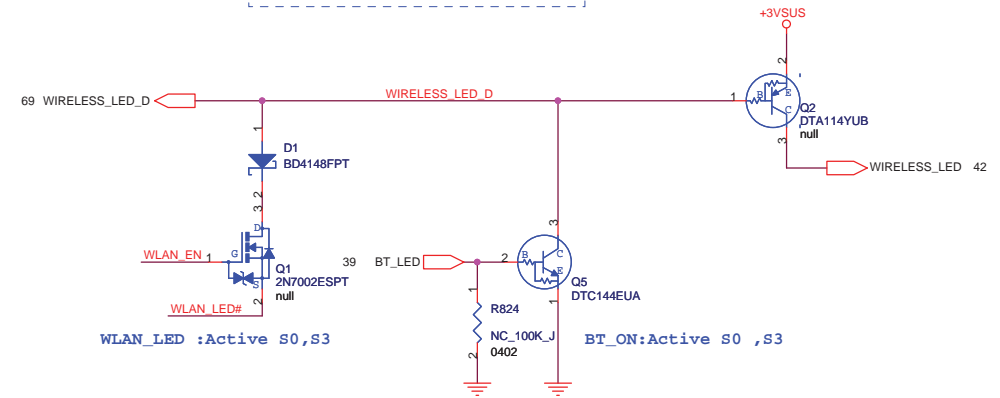
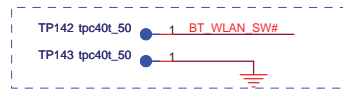
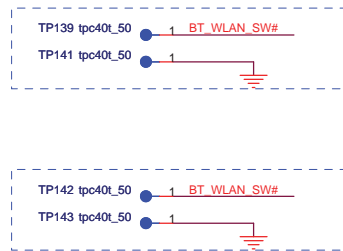
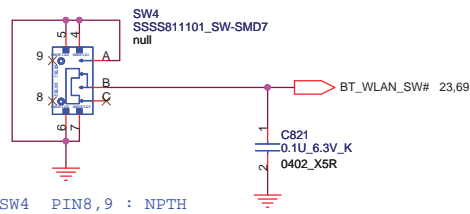
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	EXPRESS CARD		
Size	Document Number	Rev	
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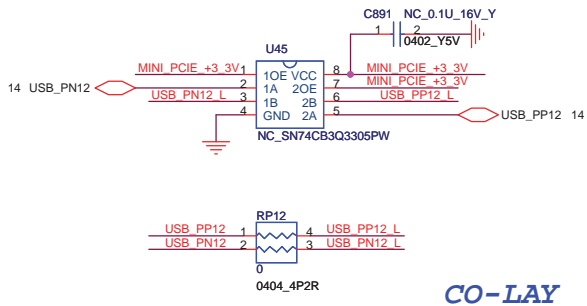
Half Size Mini Card



WLAN Switch

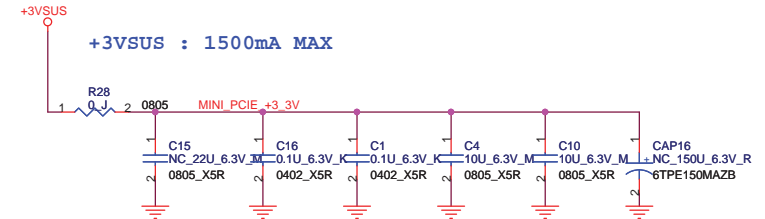
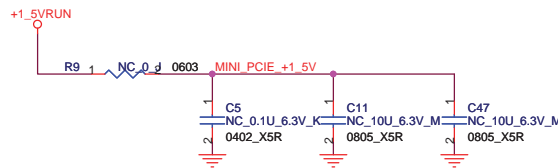


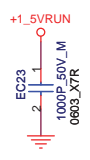
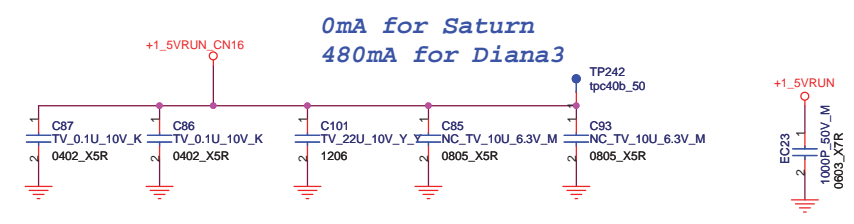
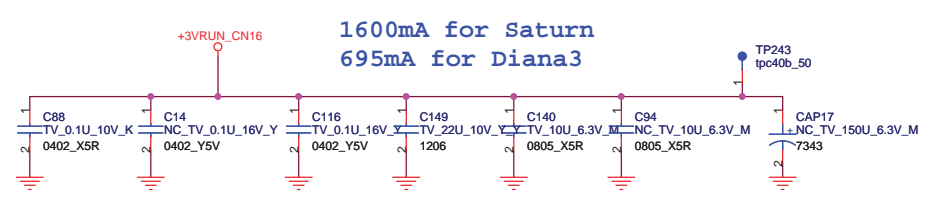
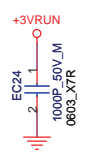
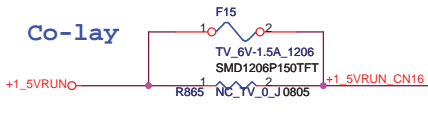
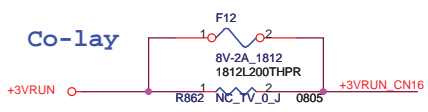
USB I/F for Wi-MAX(Kilmer Peak)



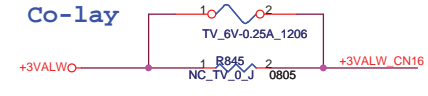
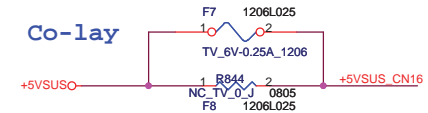
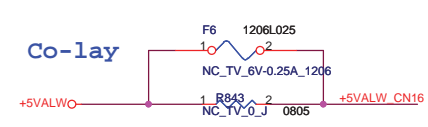
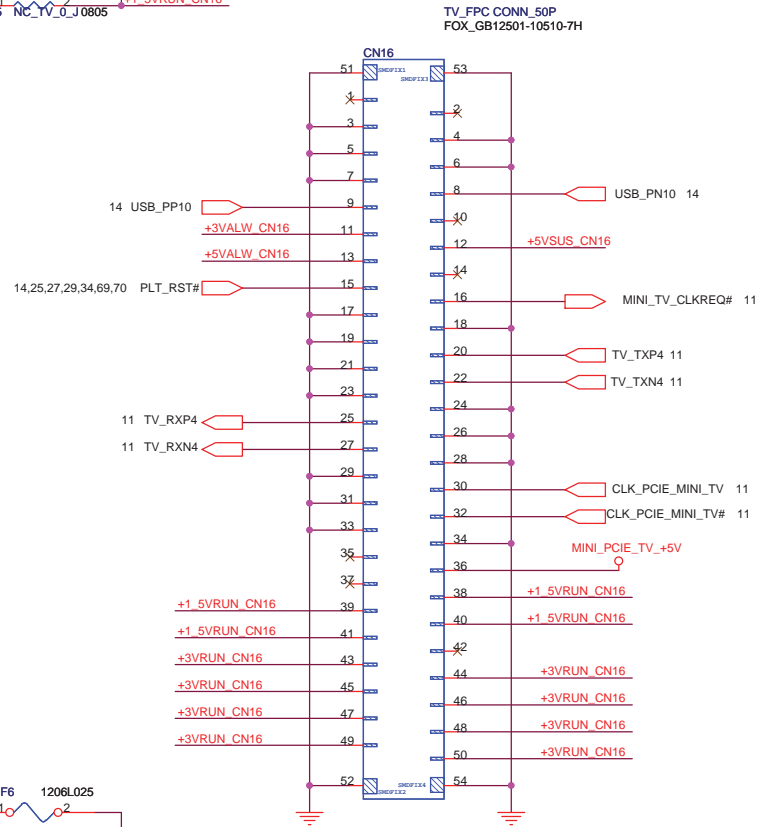
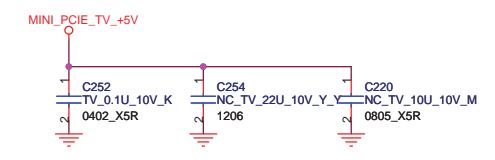
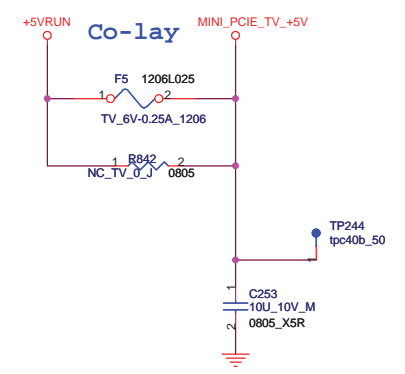
CO-LAY

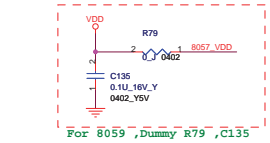
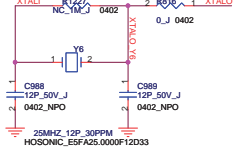
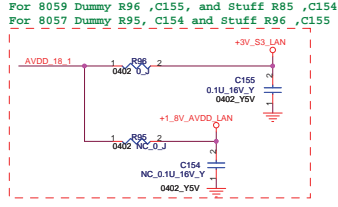
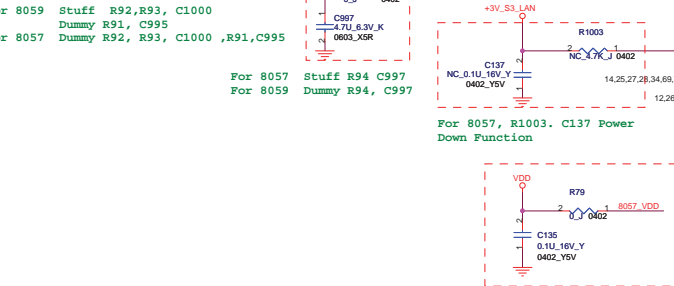
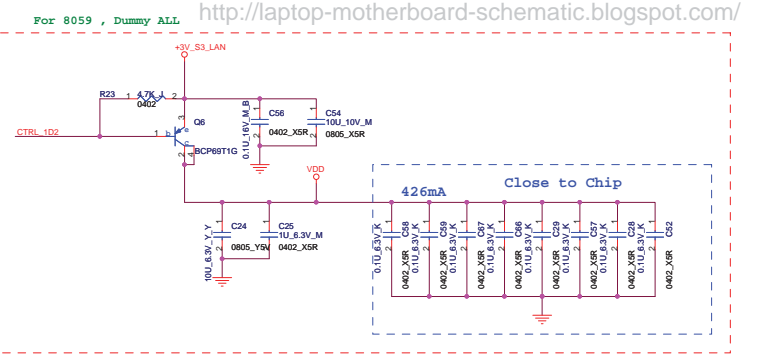
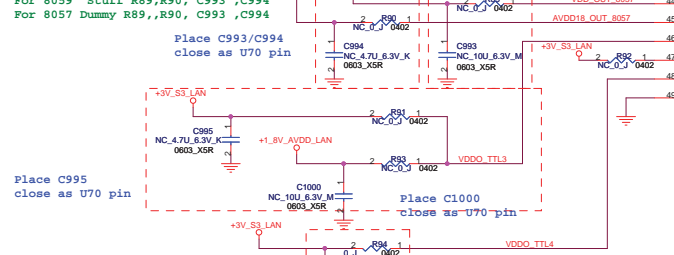
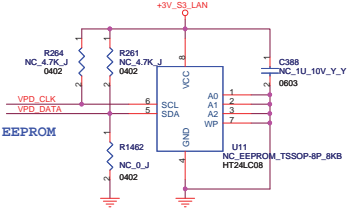
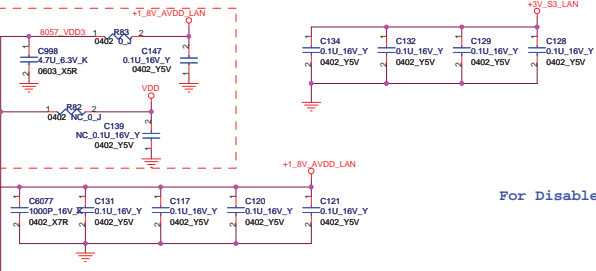
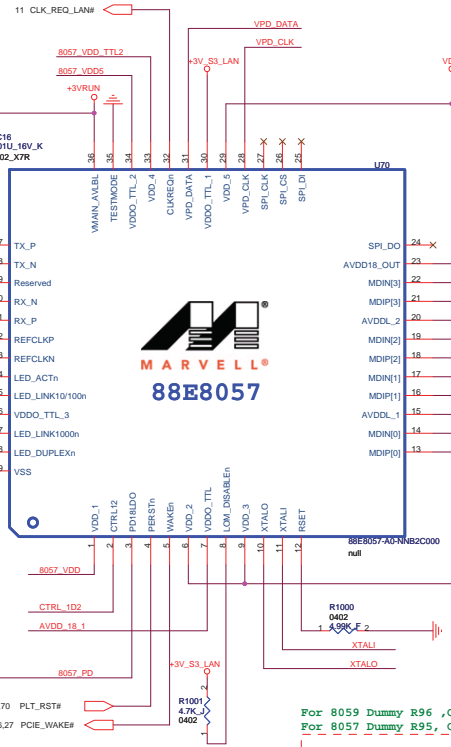
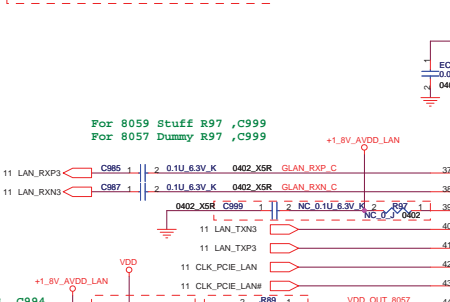
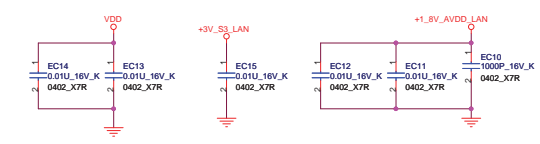
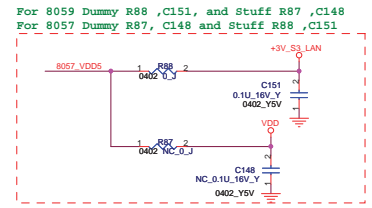
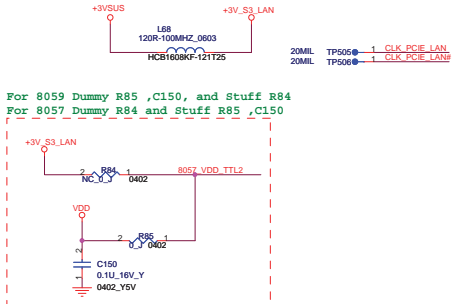
+1_5VRUN : 330mA MAX
Intel Puma Peak & Kilmer Peak nonsupport +1_5VRUN



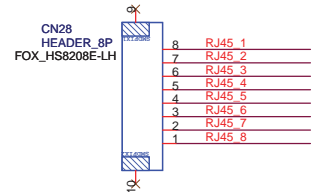
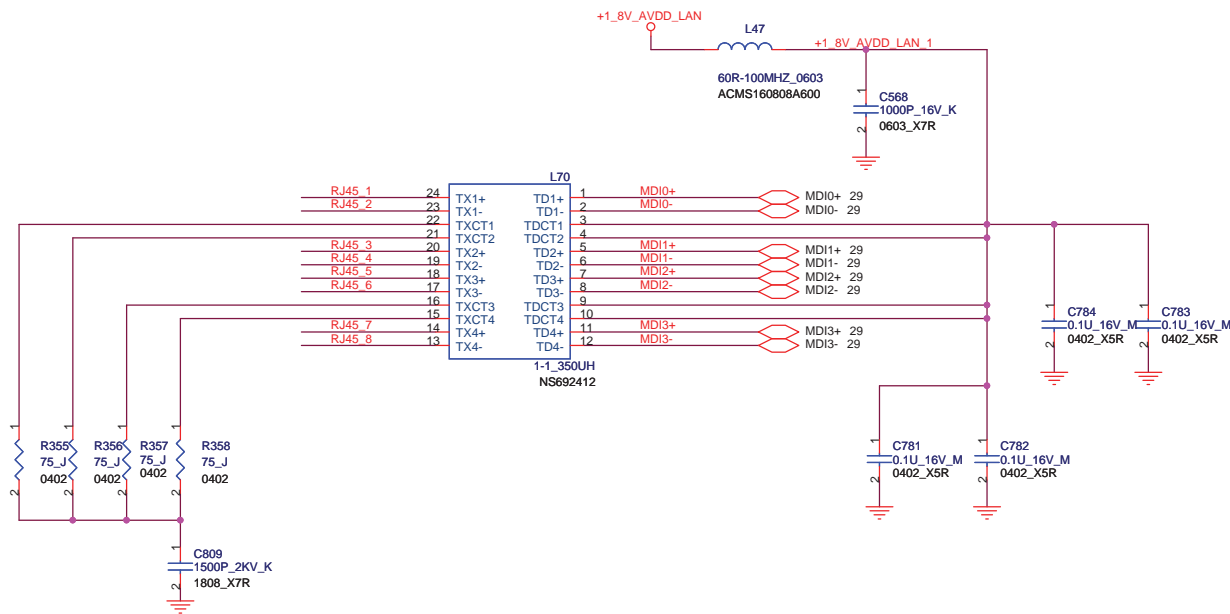


**20mA for Saturn
20mA for Diana3**

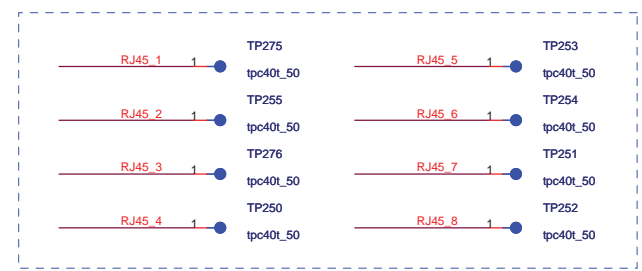
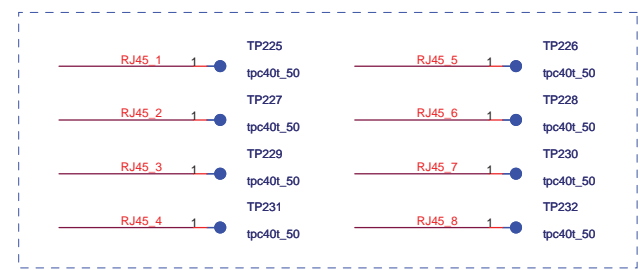


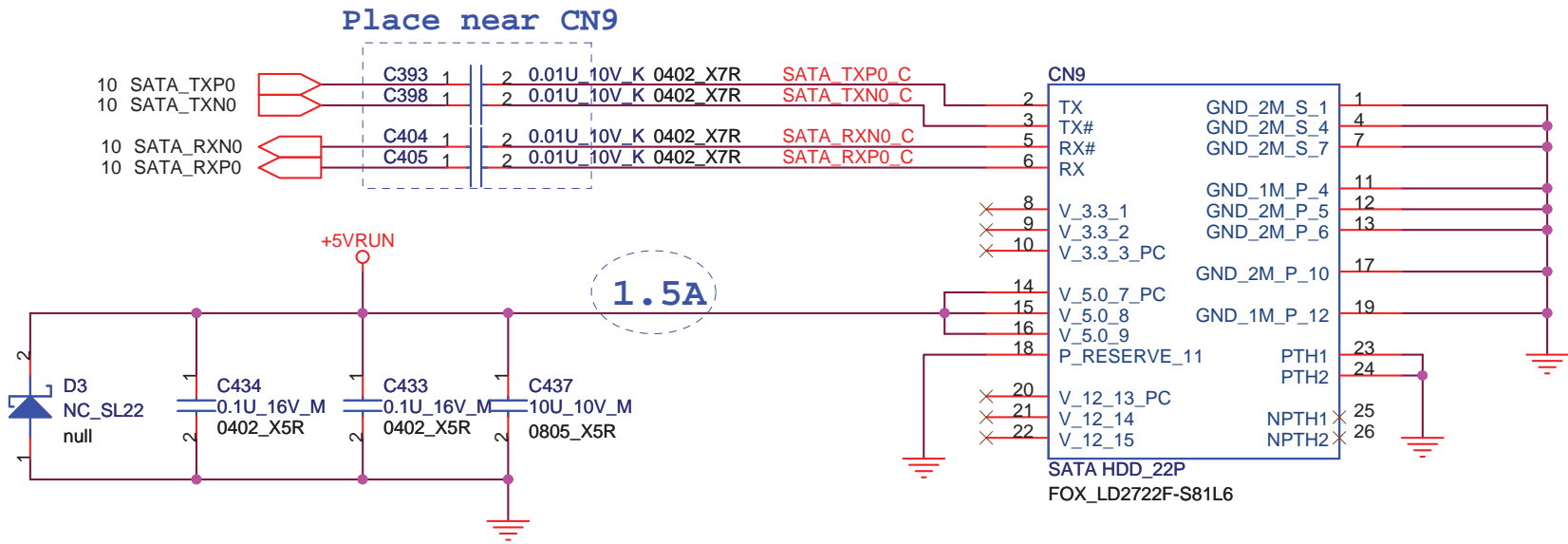


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division			
Title: LAN (88E8057) /12			
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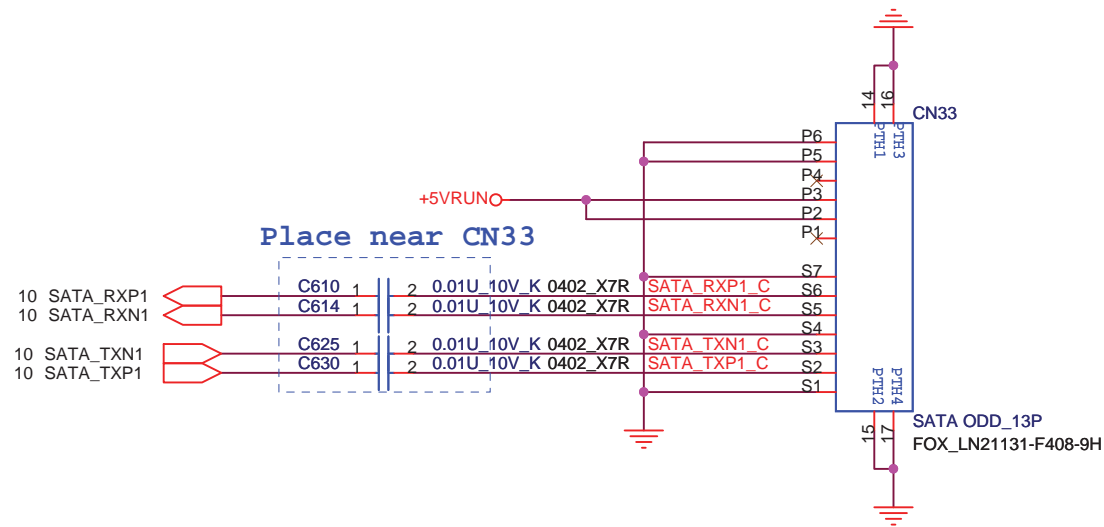
RJ45



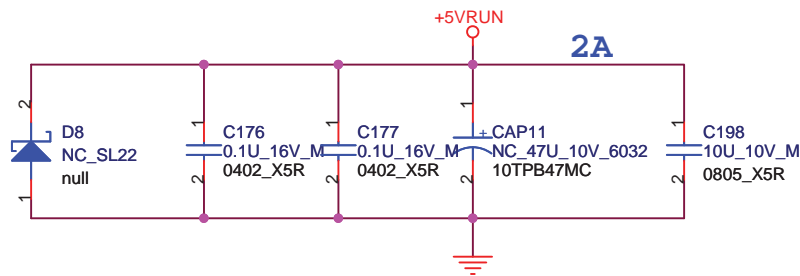


SATA HDD CONN

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title SATA HDD			
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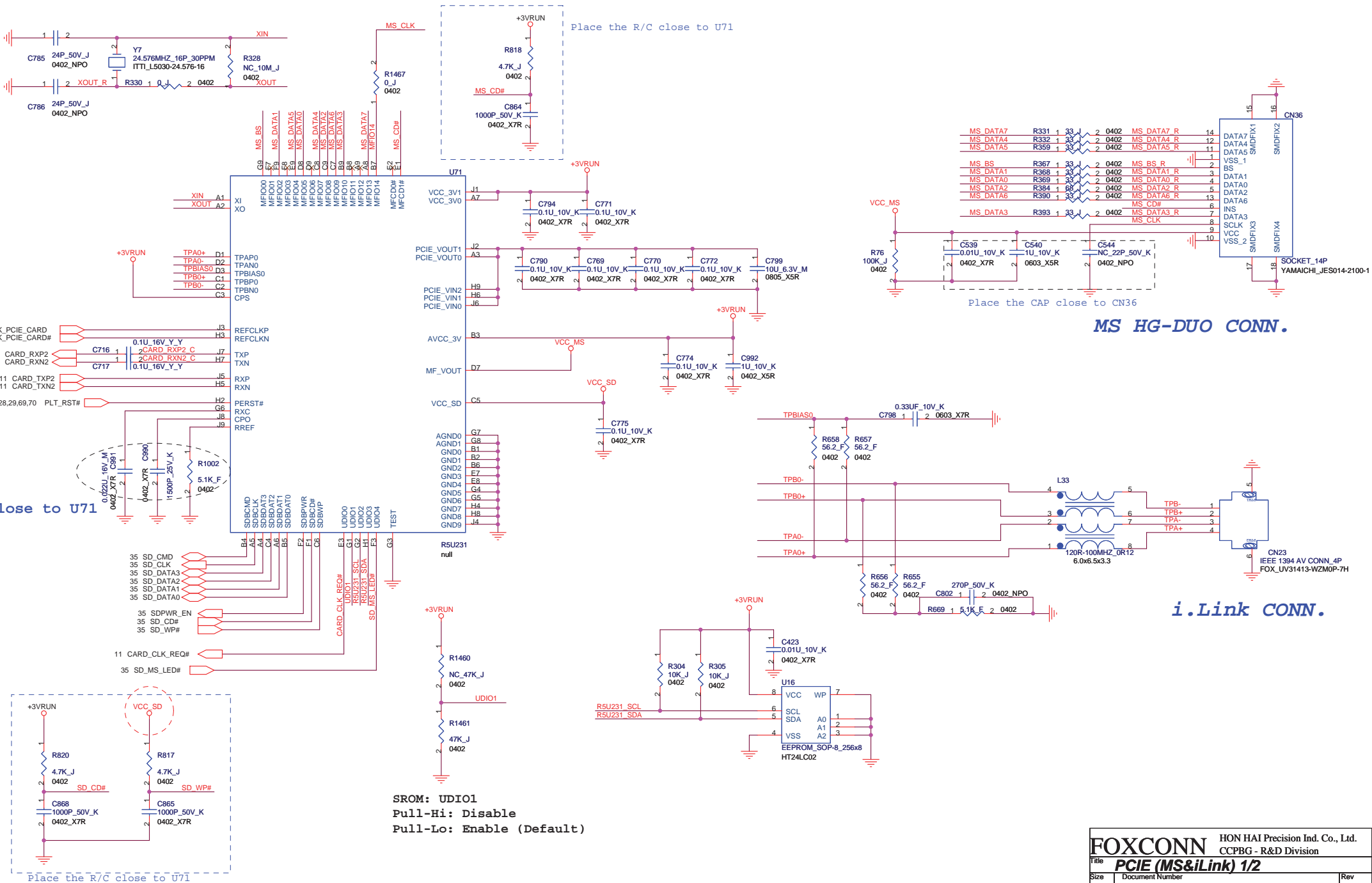


SATA ODD CONN

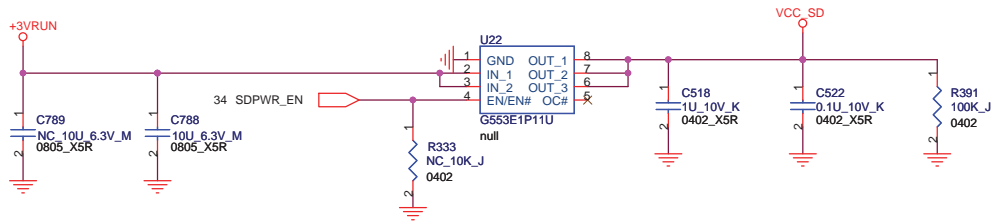


Remove Braidwood (Intel Updated and MOR confirmed)

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Braidwood Connector			
Size	Document Number		Rev
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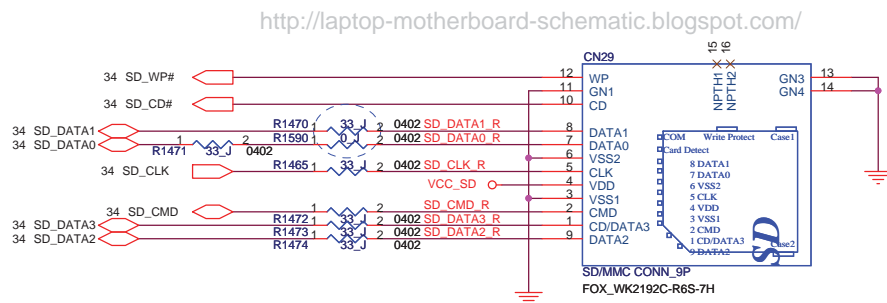
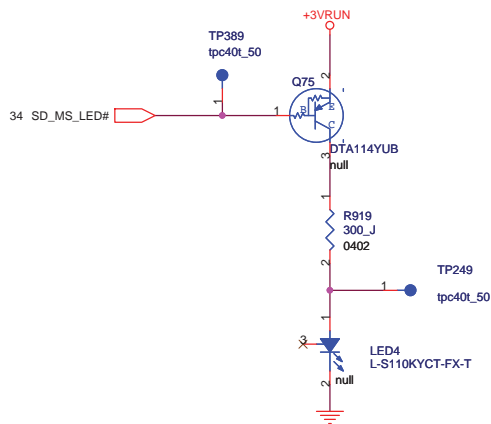


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCIE (MS&iLink) 1/2	
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SD POWER

SD/MS LED



SD CONN.

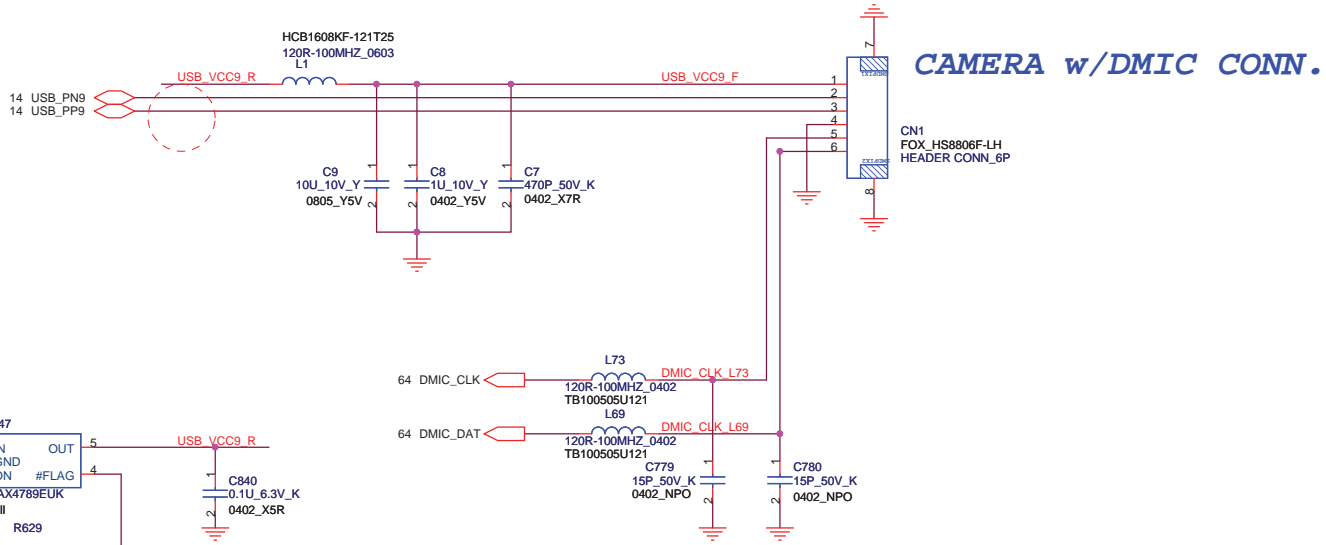


For EMI

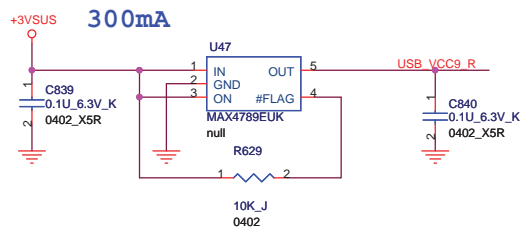
- TP455 tpc40t_50 SD_WP#
- TP456 tpc40t_50 SD_CD#
- TP457 tpc40t_50 SD_DATA1_R
- TP458 tpc40t_50 SD_DATA0_R
- TP459 tpc40t_50 SD_CLK_R
- TP460 tpc40t_50 VCC_SD
- TP469 tpc40t_50 SD_CMD_R
- TP470 tpc40t_50 SD_DATA3_R
- TP471 tpc40t_50 SD_DATA2_R
- TP472 tpc40t_50

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title PCIE (SD) 2/2		CCPBG - R&D Division	
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- TP233 tpc40t_50 1 DMIC_CLK
- TP234 tpc40t_50 1 DMIC_DAT
- TP1 tpc40t_50 1 USB_VCC9_F
- TP120 tpc40t_50 1 USB_PN9
- TP121 tpc40t_50 1 USB_PP9
- TP122 tpc40t_50 1



CAMERA w/DMIC CONN.



Current Limit Switch

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Camera w/DMIC Connector			
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14 USB_PN11
14 USB_PP11

L16 120R-100MHZ_0603
TB160808B121

USB_VCC11_L

USB_VCC11_F
USB_PN11
USB_PP11

C152 10U_10V_M
0805_X5R

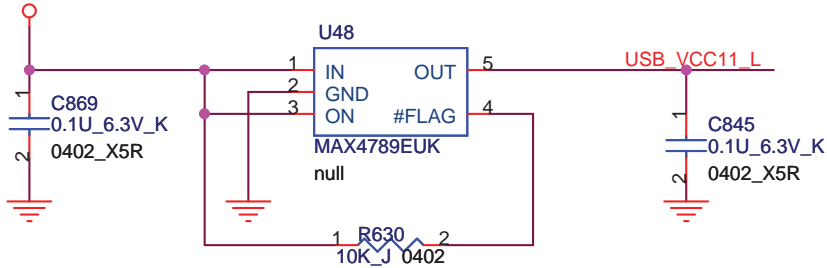
C142 NC_1U_10V_Y
0603

C171 470P_50V_K
0402

CN7
FPC CONN_6P
FOX_GB5RF060-1203-7H

300mA

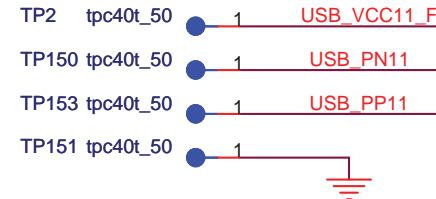
+3VSUS



Current Limit Switch

Felica Conn.

Felica Vdd Spec. (3.15V to 3.45V)



FOXCONN

HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title **Felica Connector**

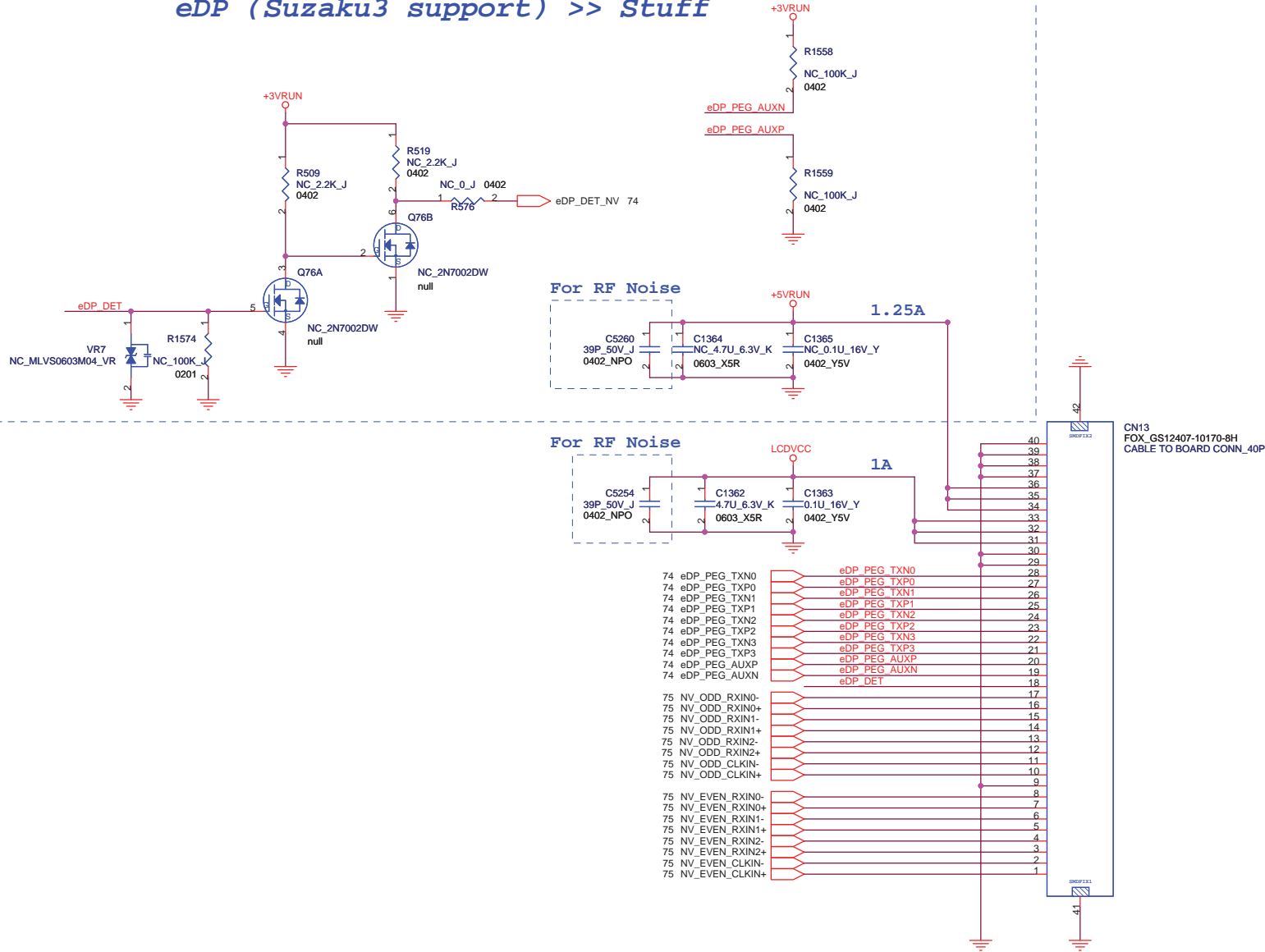
Size Document Number

A **M931 (MBX-215)**

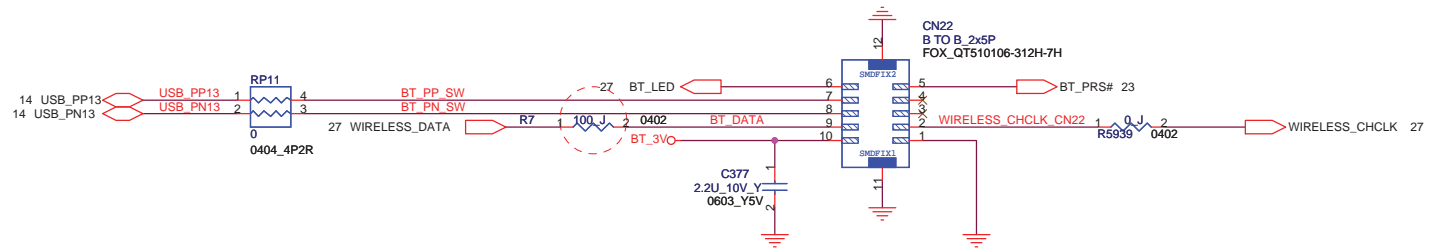
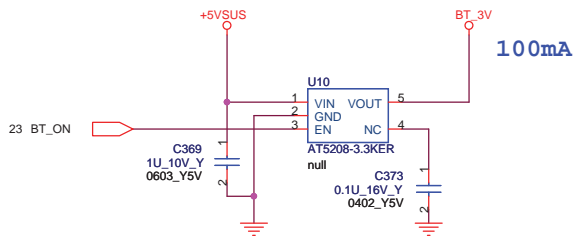
Rev

SA

eDP (Suzaku3 support) >> Stuff



eDP & LVDS CONNECTOR

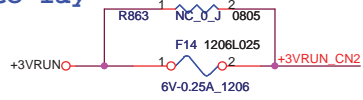


Place C377 close to CN22, Pin10

Bluetooth CONN.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Bluetooth Connector			
Size: Custom	Document Number: M931 (MBX-215)	Rev: SA	
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Co-lay



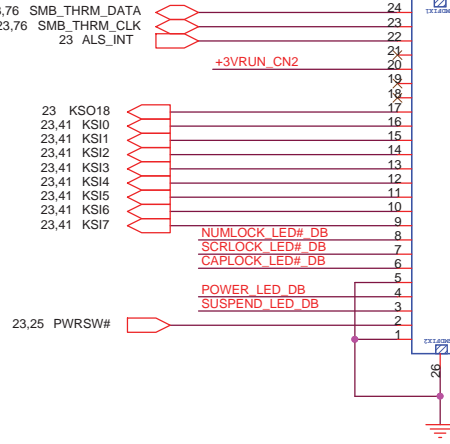
Light Sensor (EC)

Switch Keyboard Matrix

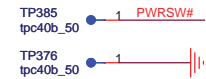
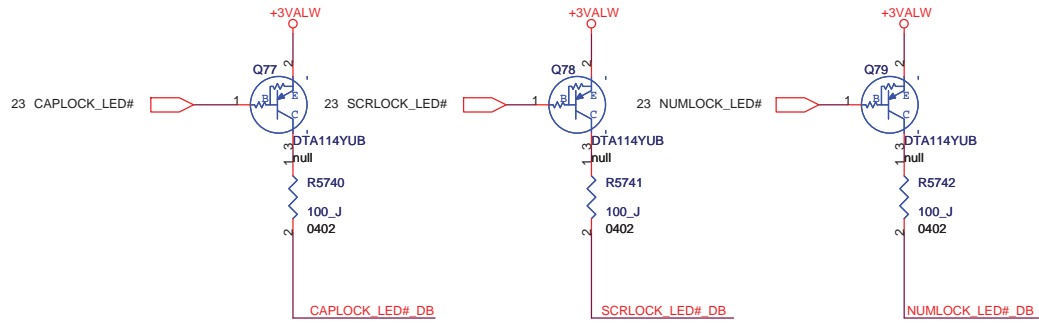
Keyboard LED

Power Button

11,23,76 SMB_THRM_DATA
11,23,76 SMB_THRM_CLK
23 ALS_INT

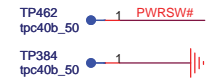


Switch DB Conn.

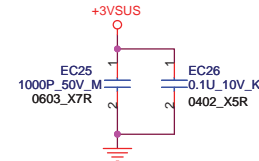
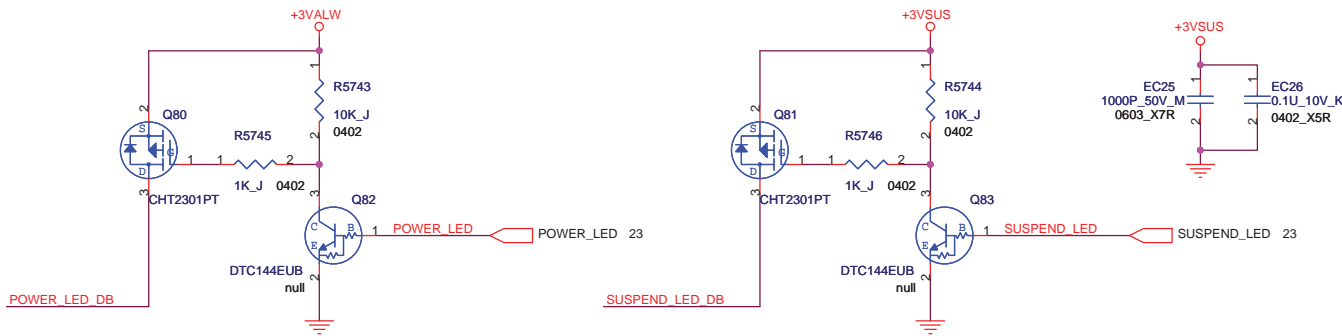
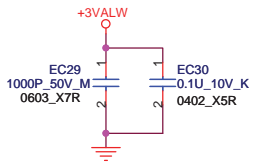


Top side ,Closer together

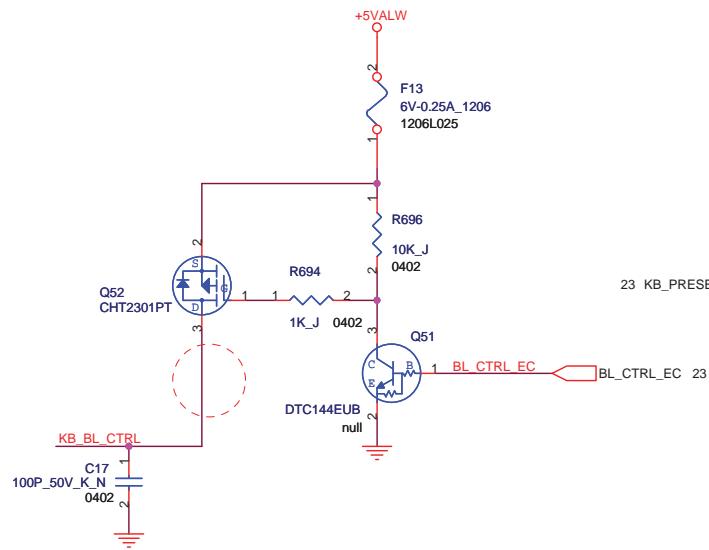
<http://laptop-motherboard-schematic.blogspot.com/>



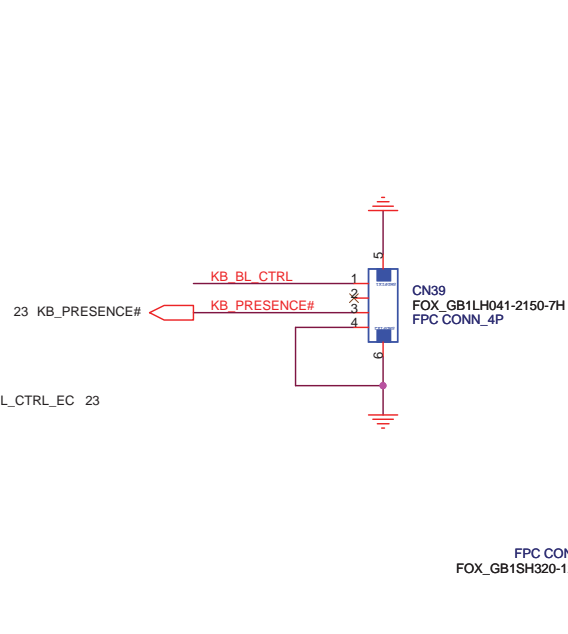
Bot side ,Closer together



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Switch DB Connector		
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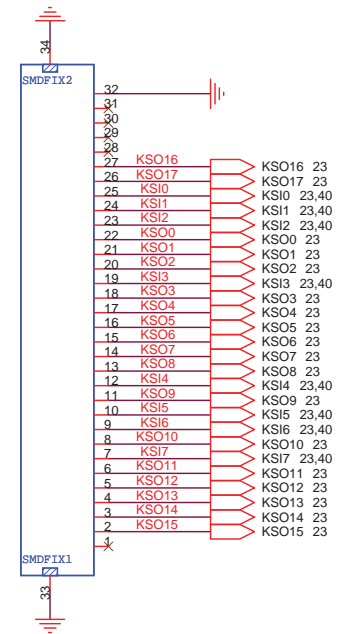


Backlit Power Conn



KBC Conn

CN4
FPC CONN_32P
FOX_GB1SH320-1280-7H

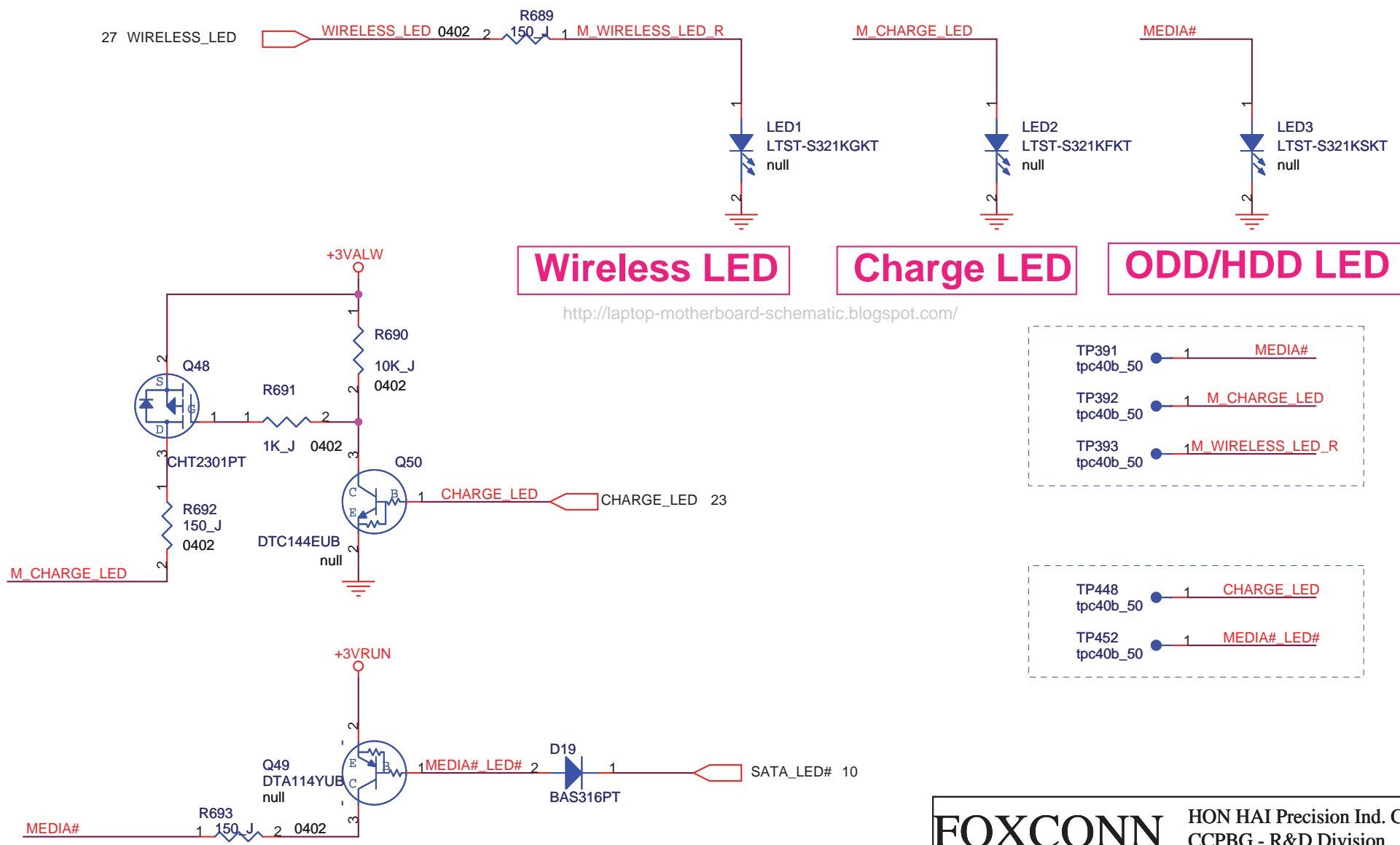


<http://laptop-motherboard-schematic.blogspot.com/>

KSI0	1	TP382	tpc40t_50
KSO10	1	TP381	tpc40t_50
KSI7	1	TP383	tpc40t_50
KSI2	1	TP394	tpc40t_50
KSO6	1	TP461	tpc40t_50

KSI0	1	TP280	tpc40t_50
KSO10	1	TP281	tpc40t_50
KSI7	1	TP282	tpc40t_50
KSI2	1	TP387	tpc40t_50
KSO6	1	TP388	tpc40t_50

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title KB & Backlit Connector			
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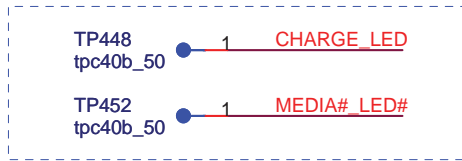
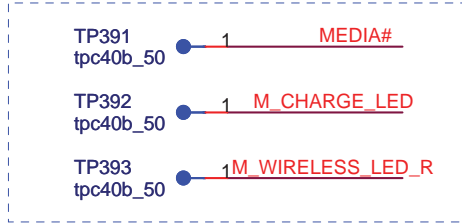


Wireless LED

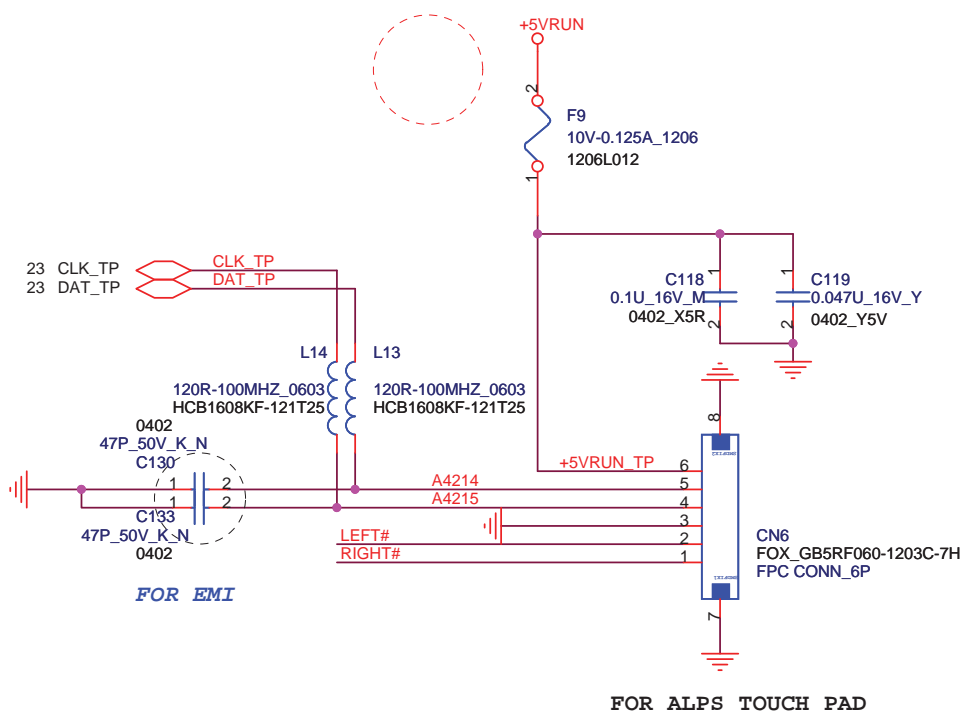
Charge LED

ODD/HDD LED

<http://laptop-motherboard-schematic.blogspot.com/>



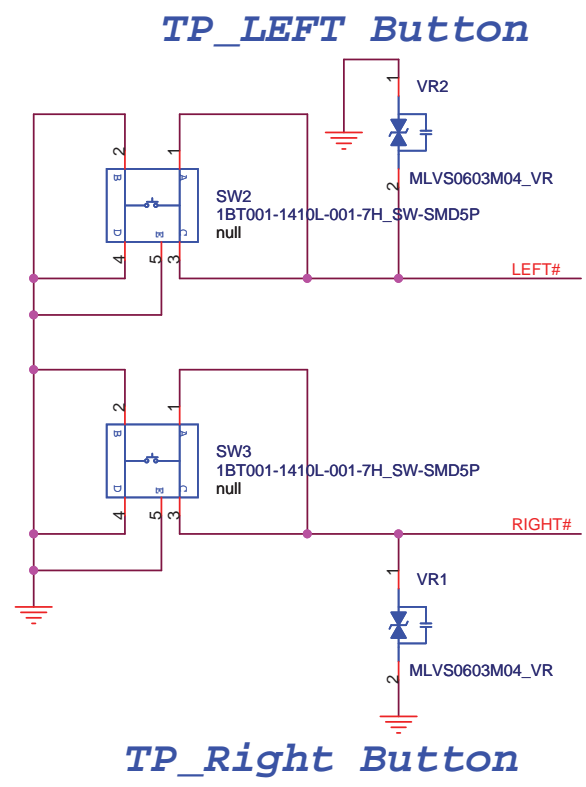
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Status LED			
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- +5VRUN_TP 1 TP463 tpc40b_50
- CLK_TP 1 TP464 tpc40b_50
- DAT_TP 1 TP465 tpc40b_50
- 1 TP466 tpc40b_50
- LEFT# 1 TP467 tpc40b_50
- RIGHT# 1 TP468 tpc40b_50

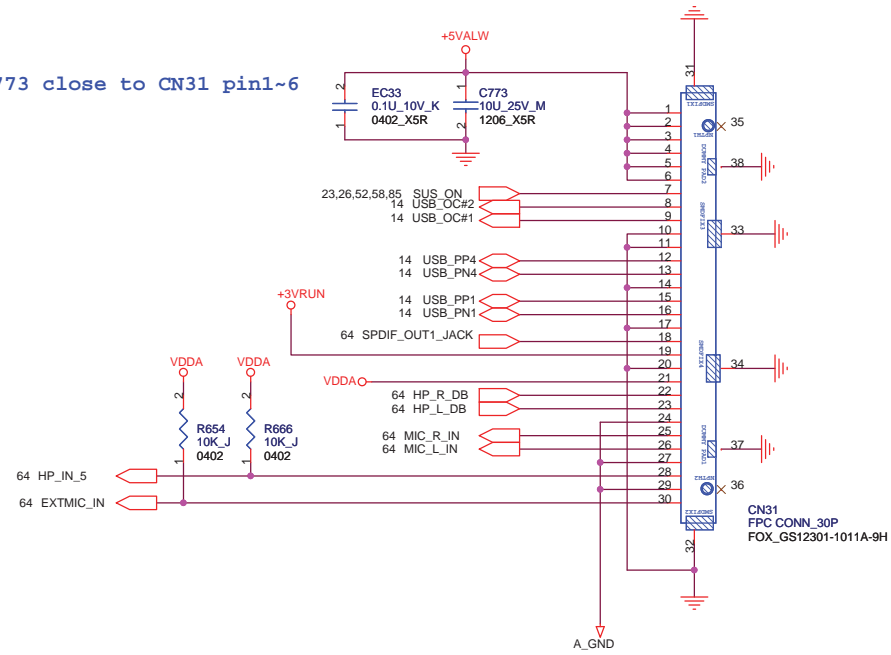
Touch Pad Conn (Support Multi Touch)

<http://laptop-motherboard-schematic.blogspot.com/>

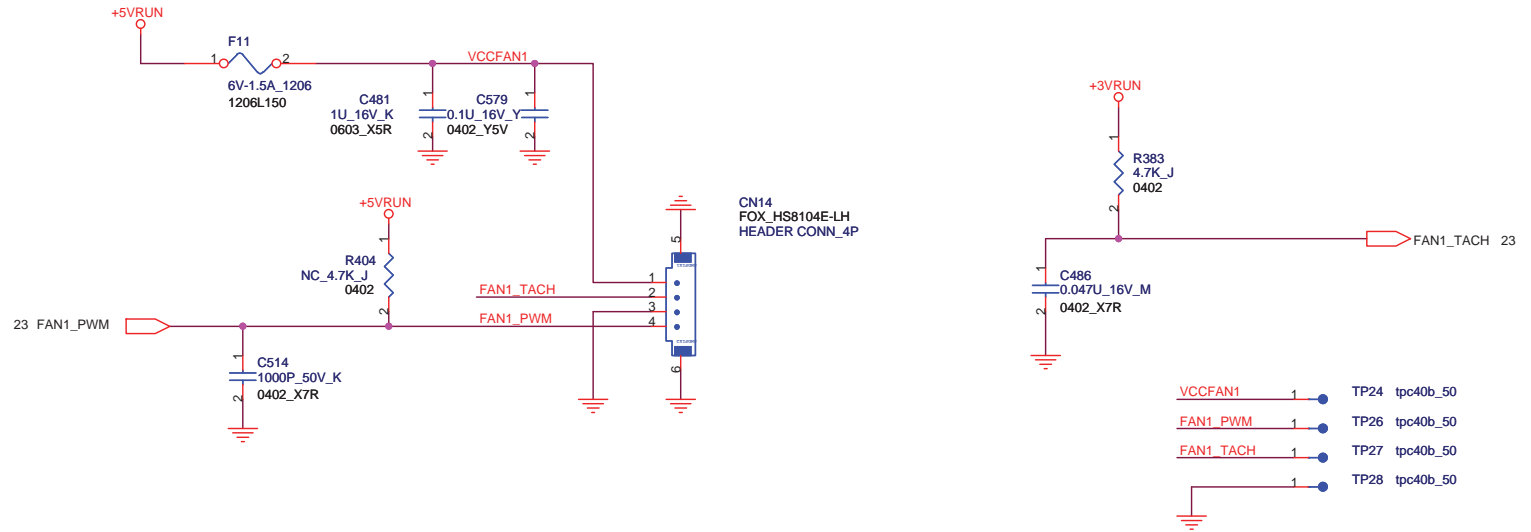


FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title Touch Pad		
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Place C773 close to CN31 pin1~6



Direct PWM FAN



- VCCFAN1 1 TP24 tpc40b_50
- FAN1_PWM 1 TP26 tpc40b_50
- FAN1_TACH 1 TP27 tpc40b_50
- 1 TP28 tpc40b_50

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN		
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A

B

C

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4

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3

2

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1

1

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Thermal Sensor & Protection			
Size A3	Document Number M931 (MBX-215)	Rev SA	
Date:	Wednesday, January 06, 2010	Sheet	46 of 93

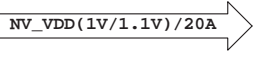
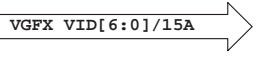
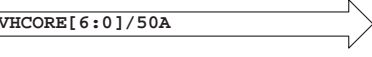
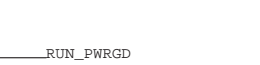
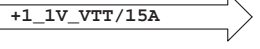
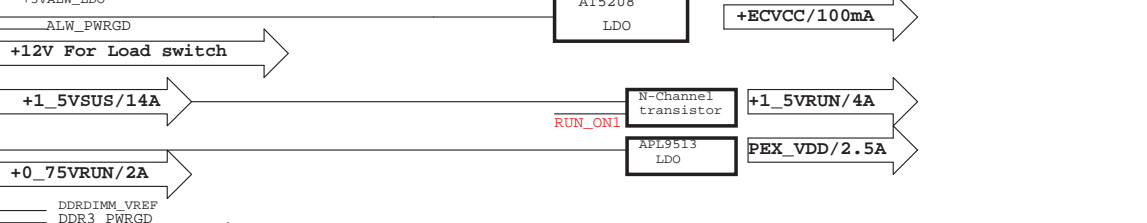
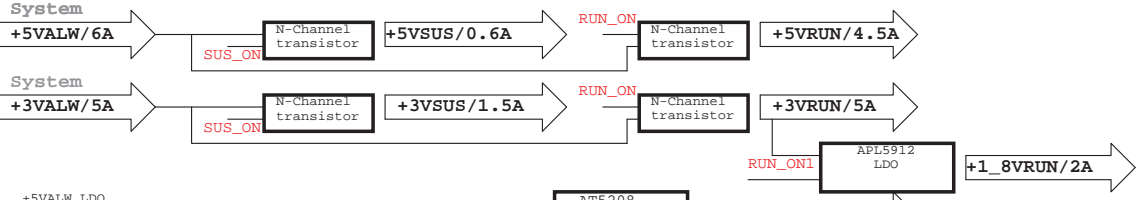
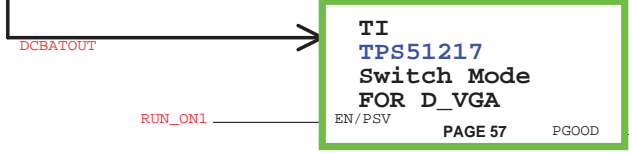
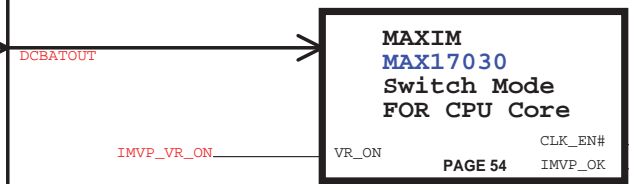
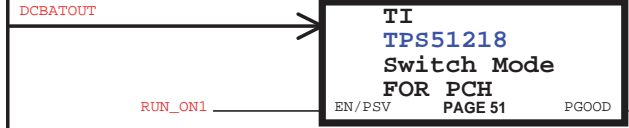
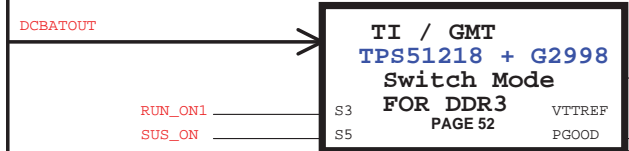
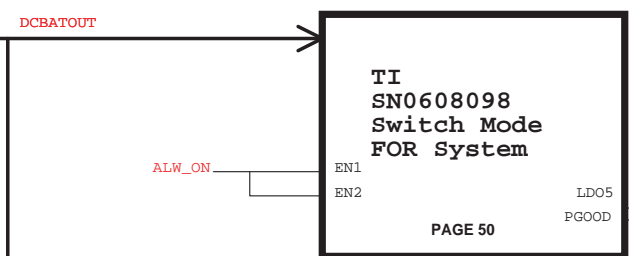
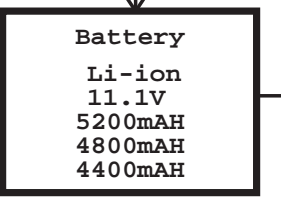
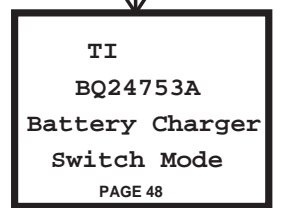
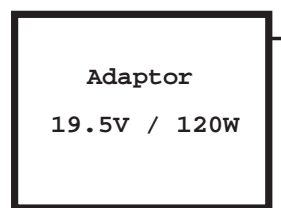
A

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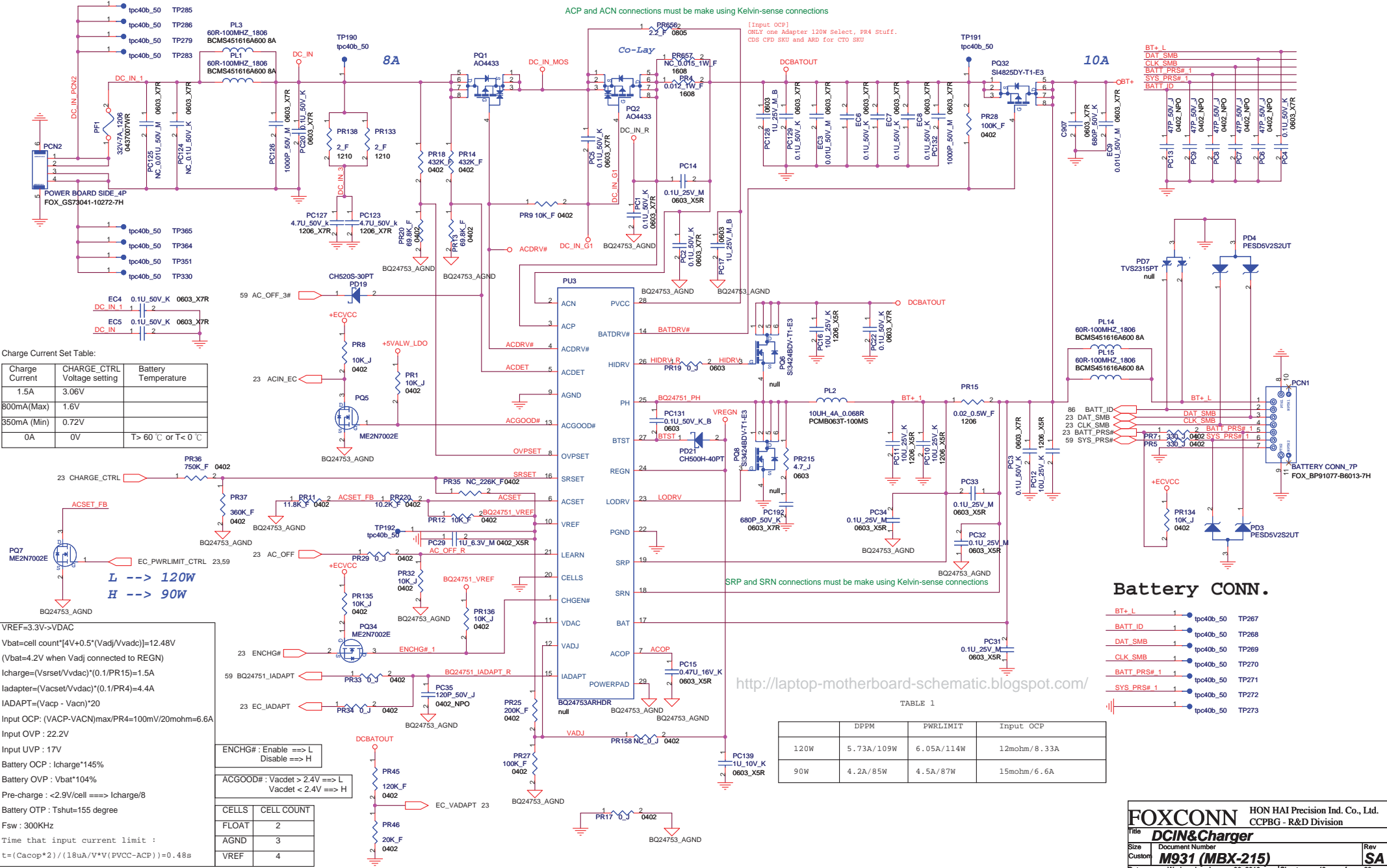


<http://laptop-motherboard-schematic.blogspot.com/>

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Power Design Diagram			
Size	Document Number	Rev	
Custom	M931 (MBX-215)	SA	
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ACP and ACN connections must be make using Kelvin-sense connections

ONLY one Adapter 120W Select. PR4 Stuff.
CDS CPD SKU and ARD for CTO SKU



Charge Current Set Table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
800mA(Max)	1.6V	
350mA (Min)	0.72V	
0A	0V	T > 60 °C or T < 0 °C

L ---> 120W
H ---> 90W

VREF=3.3V->VDAC
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{dac})] = 12.48V$
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to REGN})$
 $I_{charge} = (V_{srset} / V_{dac}) * (0.1 / PR15) = 1.5A$
 $I_{adapter} = (V_{acset} / V_{dac}) * (0.1 / PR4) = 4.4A$
 $IADAPT = (V_{acp} - V_{vacn}) * 20$
 Input OCP: $(V_{ACP} - V_{ACN}) / \max(PR4) = 100mV / 20m\Omega = 6.6A$
 Input OVP: 22.2V
 Input UVP: 17V
 Battery OCP: $I_{charge} * 145\%$
 Battery OVP: $V_{bat} * 104\%$
 Pre-charge: $< 2.9V / \text{cell} \implies I_{charge} / 8$
 Battery OTP: $T_{shut} = 155 \text{ degree}$
 Fsw: 300KHz
 Time that input current limit:
 $t = (C_{acop} * 2) / (18\mu A / V * V(PVCC - ACP)) = 0.48s$

ENCHG#: Enable ==> L
Disable ==> H

ACGOOD#: Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

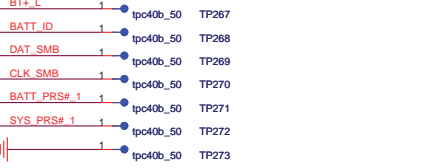
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

<http://laptop-motherboard-schematic.blogspot.com/>

TABLE 1

DPPM	PWRLIMIT	Input OCP
120W	5.73A/109W	6.05A/114W
90W	4.2A/85W	4.5A/87W
		15mohm/6.6A

Battery CONN.



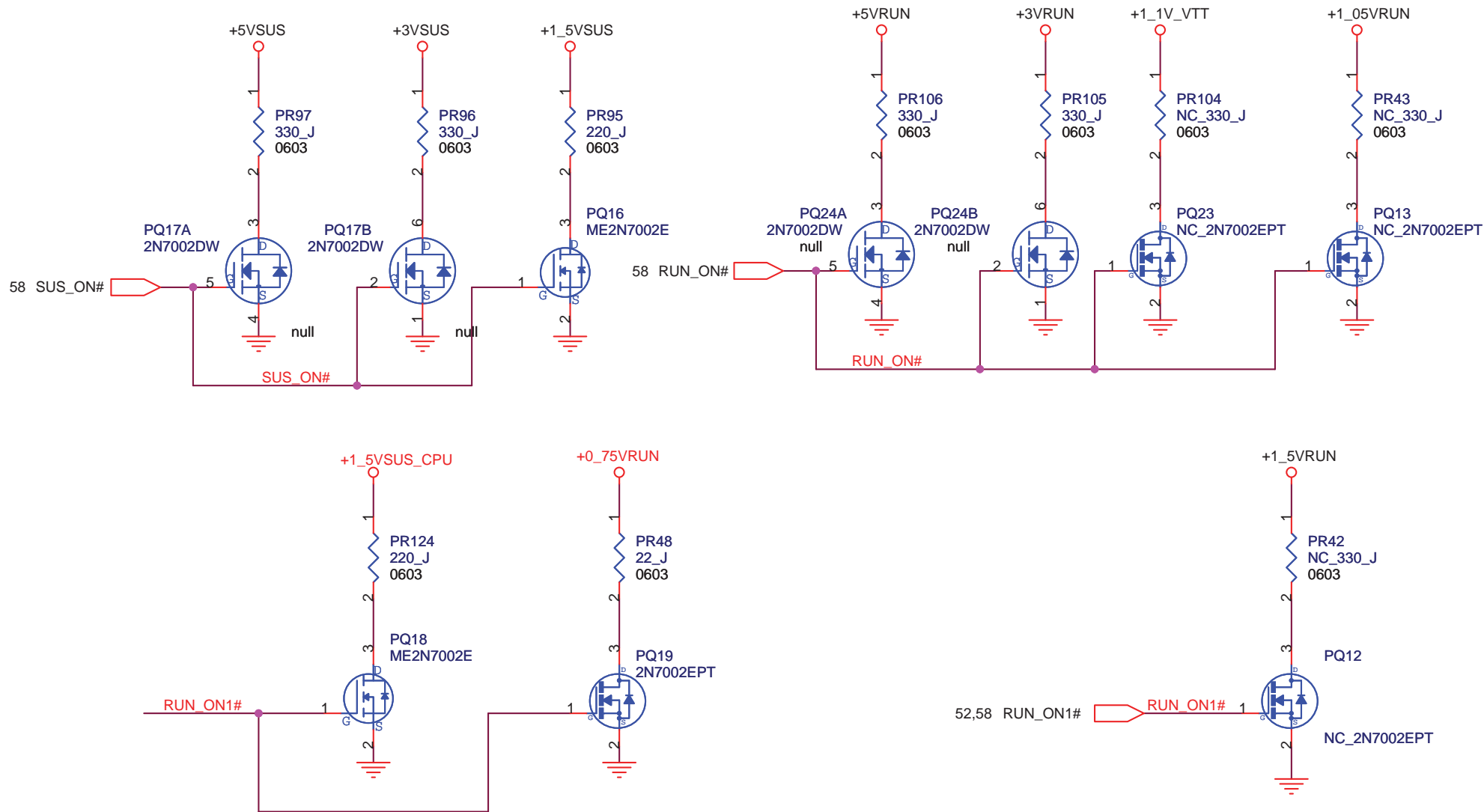
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **DCIN&Charger**

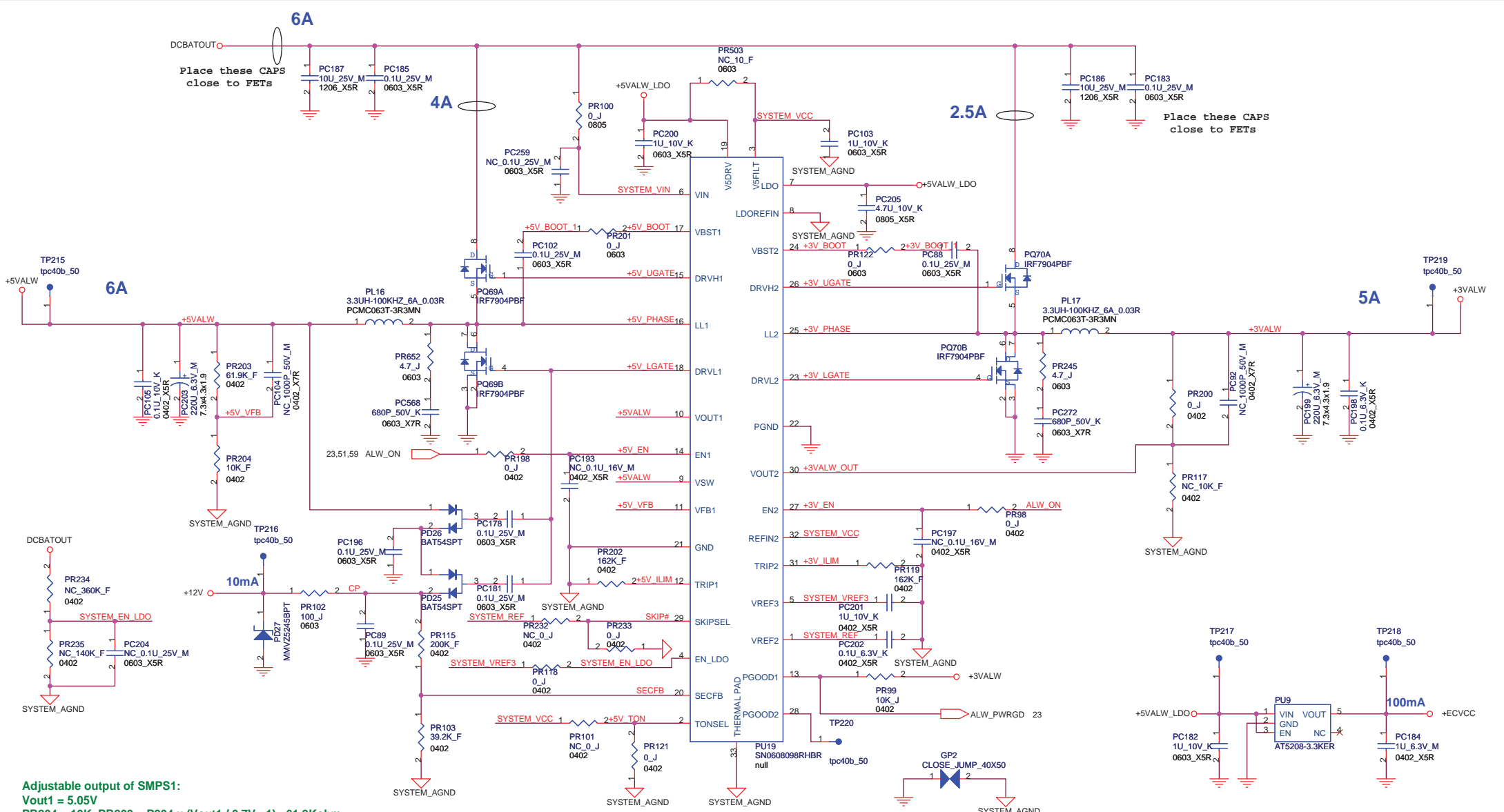
Size: Document Number
Customer: **M931 (MBX-215)**

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Rev: **SA**



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DISCHARGE CIRCUIT			
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Place these CAPS close to FETs

Place these CAPS close to FETs

Adjustable output of SMPS1:
 $V_{out1} = 5.05V$
 $PR204 = 10K, PR203 = P204 \times (V_{out1} / 0.7V - 1) = 61.9K\Omega$

Second Feedback :
 $V_{out_sec} = 12V, PR103 = 20K\Omega$
 $PR115 = PR103 \times (V_{out_sec} / 2V - 1) = 100K\Omega$

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = V_{OUT} (V_{IN} - V_{OUT}) / (V_{IN} * F * LIR * I_{LOAD} (MAX))$$

$$R_{ocp} = (I_{ocp} - I_{ripple} / 2) * (10 * R_{ds} (on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) * V_{FB1}$$

Current limit resistor for SMPS1 :
 $I_{valley_5} = 5.775A, R_{cs_5} = R_{ds1} = 10.8m\Omega$
 $PR202 = (10 \times I_{valley_5} \times R_{cs_5}) / 5uA = 162K$

Current limit resistor for SMPS2 :
 $I_{valley_3} = 5.525A, R_{cs_3} = R_{ds2} = 10.8m\Omega$
 $PR119 = (10 \times I_{valley_3} \times R_{cs_3}) / 5uA = 162K$

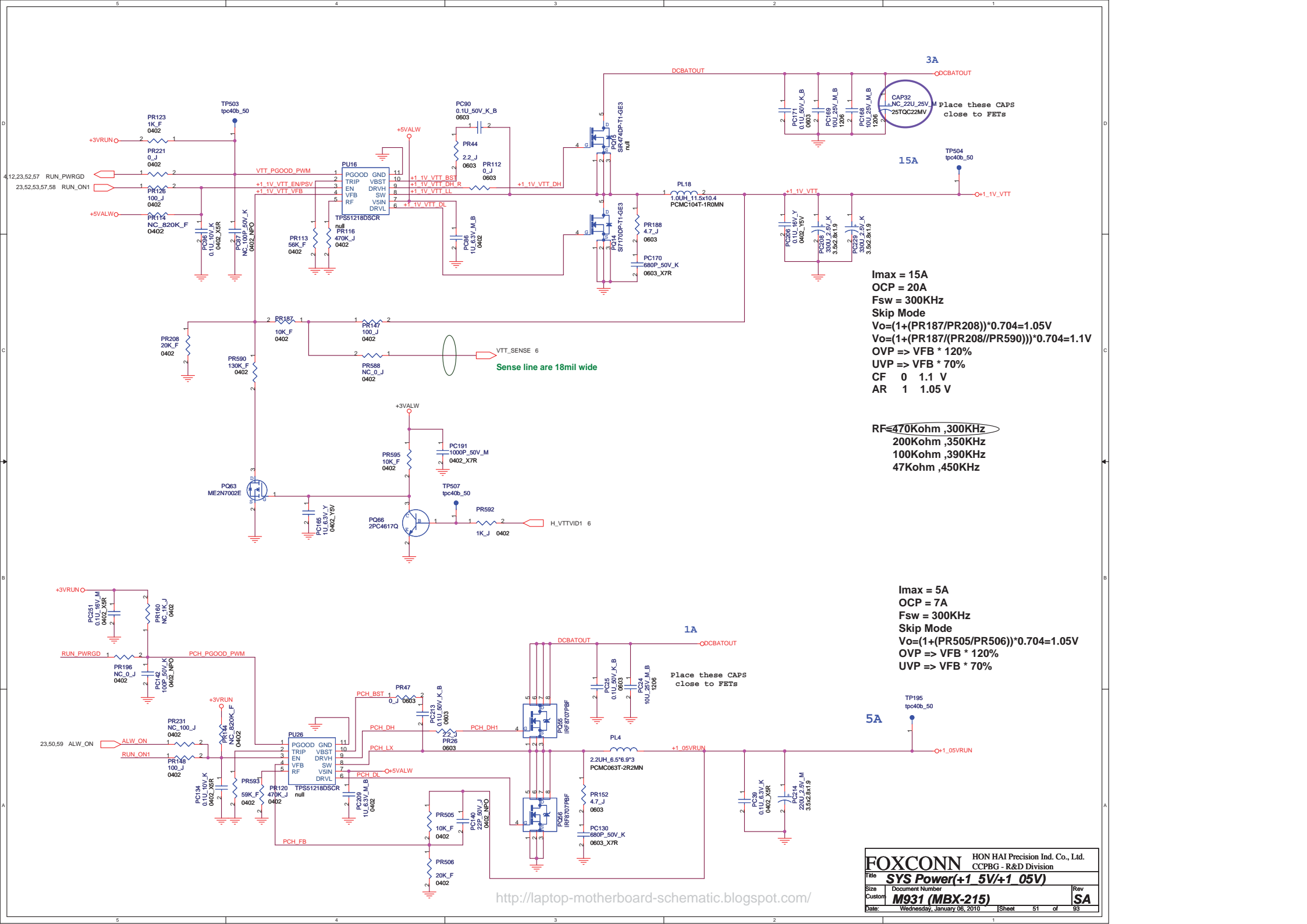
<http://laptop-motherboard-schematic.blogspot.com/>

FOXCONN HON HAI Precision Ind. Co., Ltd.
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Title: **SYS Power (+3 3V/+5V)**

Size: Document Number
 A3: **M931 (MBX-215)** Rev: **SA**

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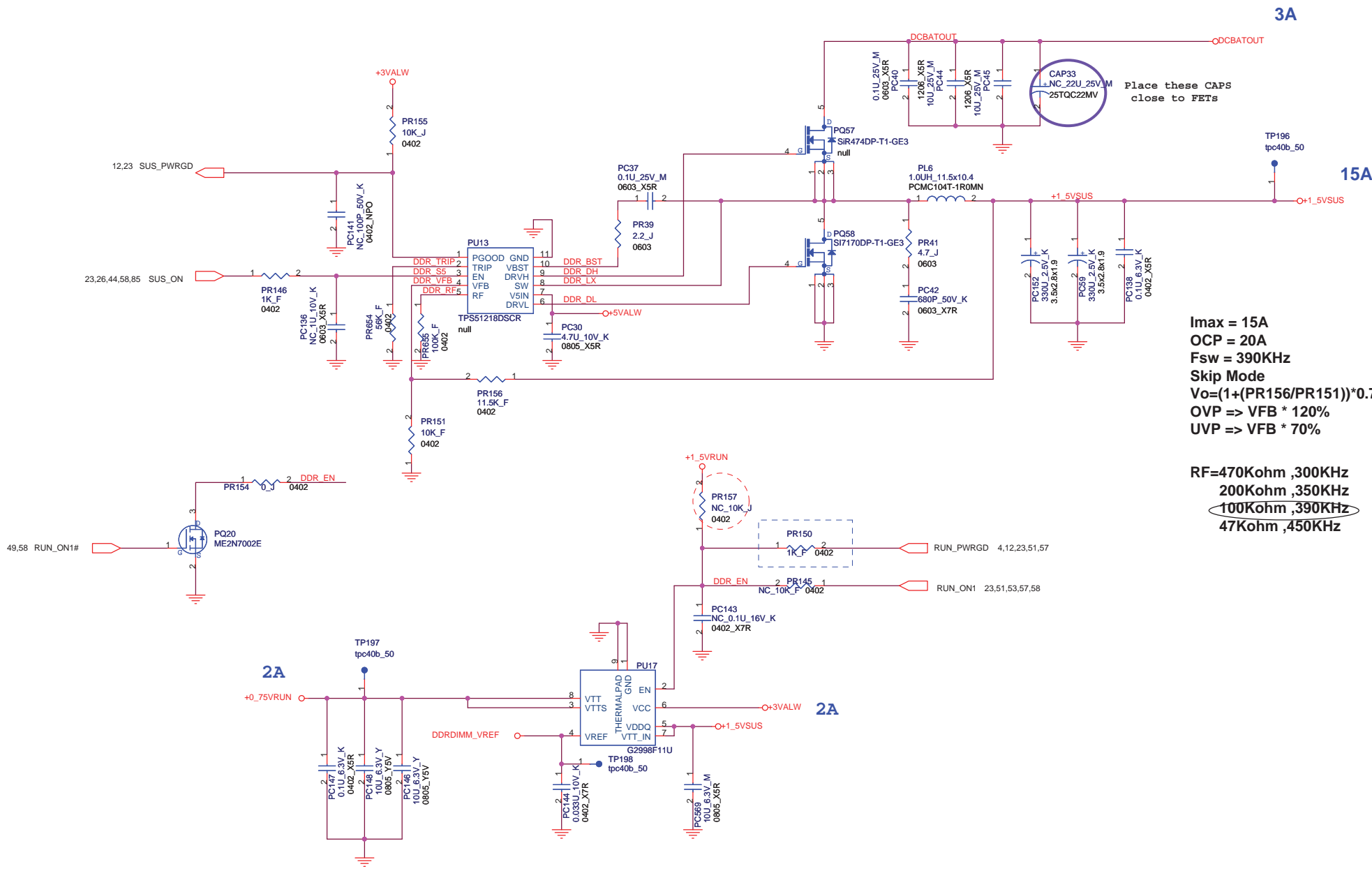


Imax = 15A
OCP = 20A
Fsw = 300KHz
Skip Mode
 $V_o = (1 + (PR187/PR208)) * 0.704 = 1.05V$
 $V_o = (1 + (PR187/(PR208/PR590))) * 0.704 = 1.1V$
OVP => VFB * 120%
UVP => VFB * 70%
CF 0 1.1 V
AR 1 1.05 V

RF = 470Kohm , 300KHz
200Kohm , 350KHz
100Kohm , 390KHz
47Kohm , 450KHz

Imax = 5A
OCP = 7A
Fsw = 300KHz
Skip Mode
 $V_o = (1 + (PR505/PR506)) * 0.704 = 1.05V$
OVP => VFB * 120%
UVP => VFB * 70%

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		CCPBG - R&D Division	
File SYS Power(+1.5V/+1.05V)			
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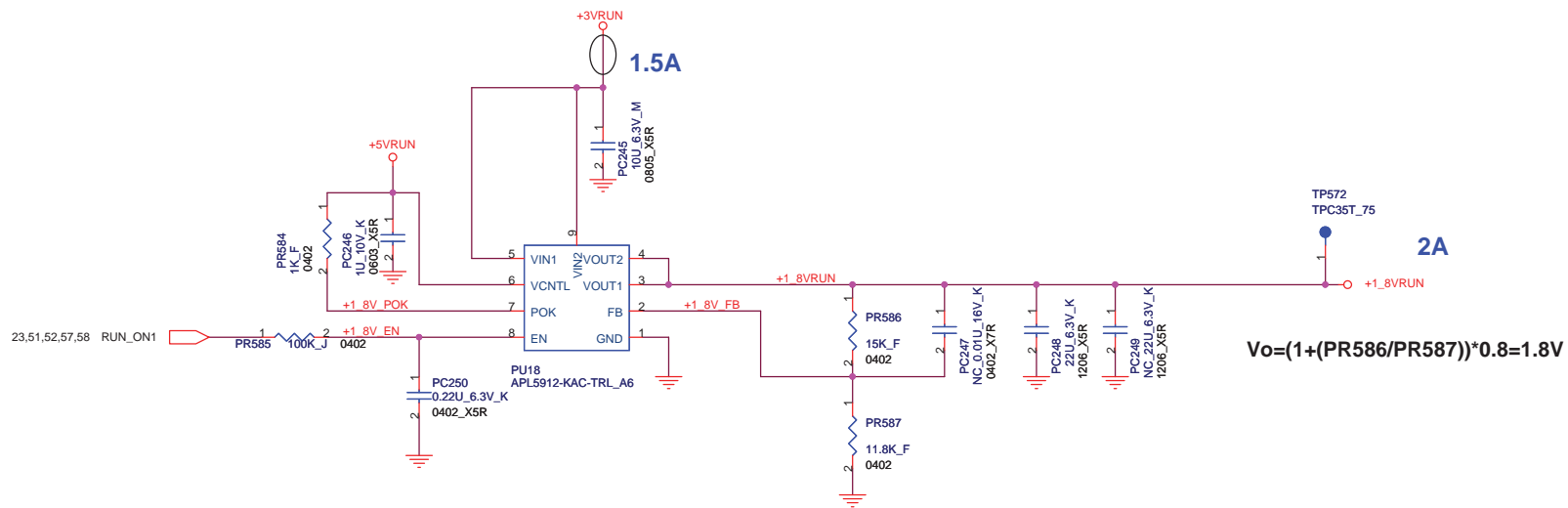


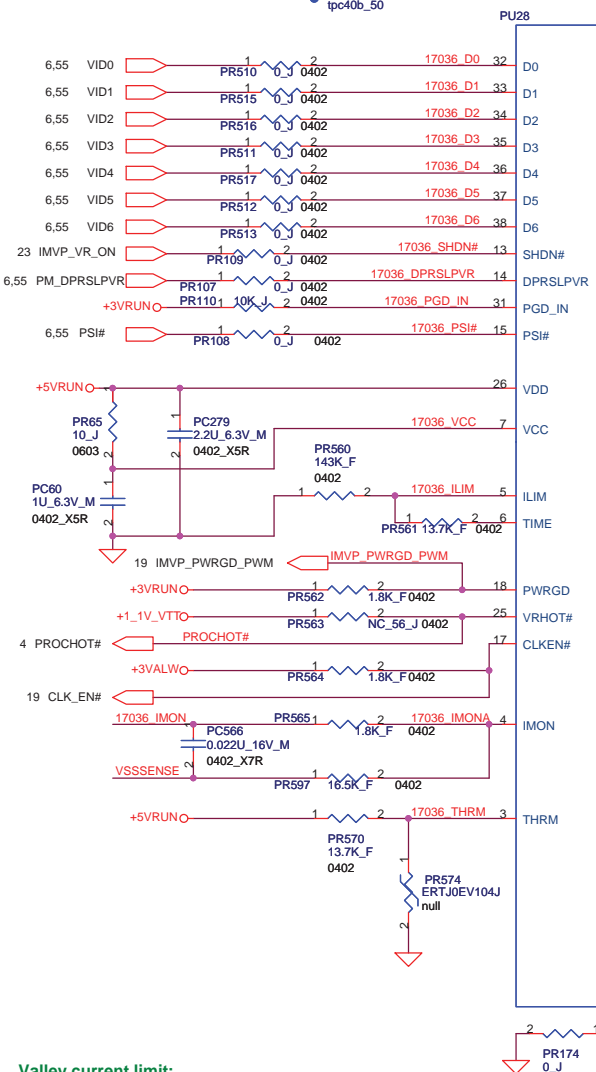
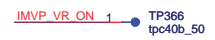
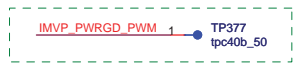
Place these CAPS close to FETs

Imax = 15A
OCP = 20A
Fsw = 390KHz
Skip Mode
 $V_o = (1 + (PR156/PR151)) * 0.704 = 1.514V$
OVP => VFB * 120%
UVP => VFB * 70%

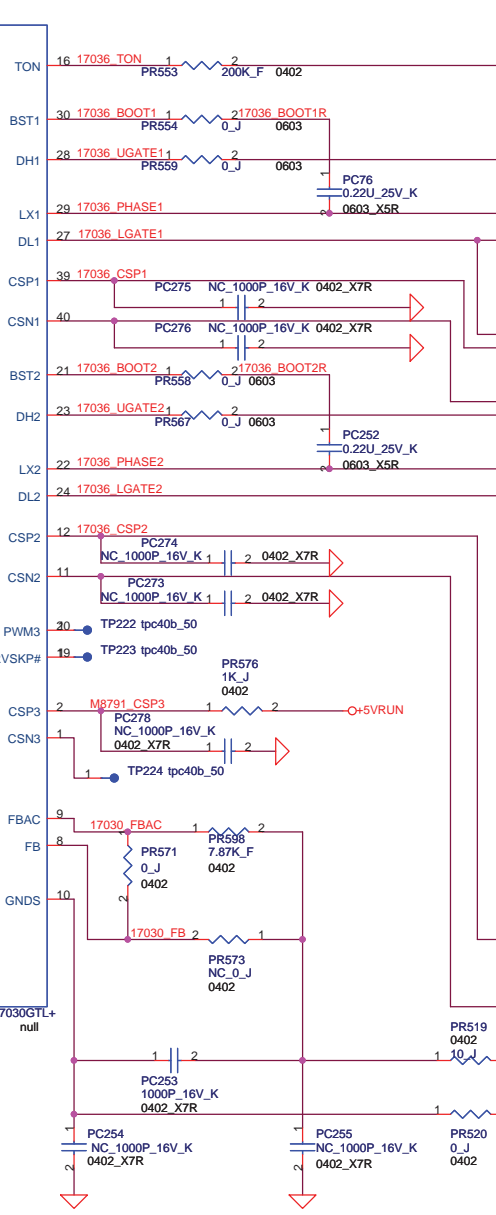
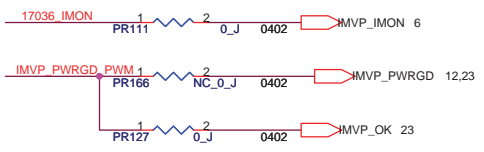
RF = 470Kohm, 300KHz
200Kohm, 350KHz
100Kohm, 390KHz
47Kohm, 450KHz

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
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Title DDR3 Power(+1.5V/+0.75V)			
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Valley current limit:
 $V_TIME_LIM = 0.2 \times PR561 / (PR560 + PR561) = 20.2mV$
 $I_LIM = V_TIME_LIM / Rcs = 19A$



Sense line are 18mil wide

Place these CAPS close to FETs

Place these CAPS close to FETs

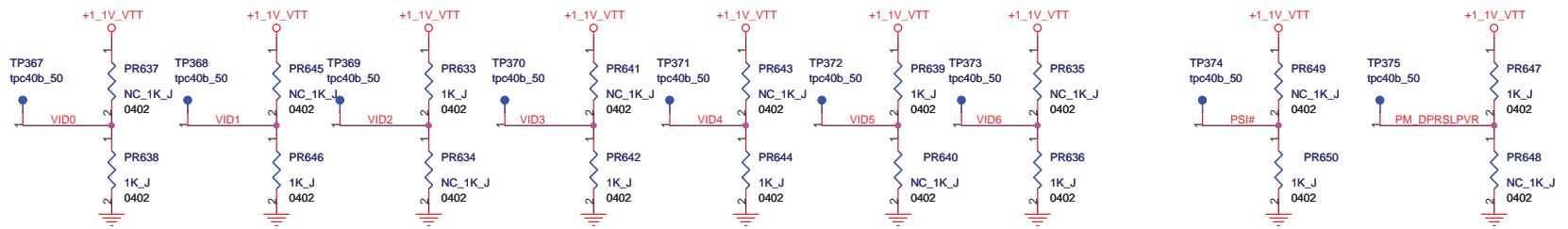
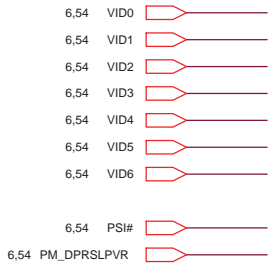
Rcs:
 $DCR = 0.8m\Omega$
 $Rcs = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709m\Omega$
 Load-Line R_FBAC: Load-Line=-1.9mV/A
 $Rcs = 0.709m\Omega$
 $PR598 = (1.9mV/A) / (Rcs \times 400us) = 6.34K$

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
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Title: CPU Power VHCORE			
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Default value of VID [6:0] = [0100100] , PSI# = 0 , PROC_DPRSLPVR = 1

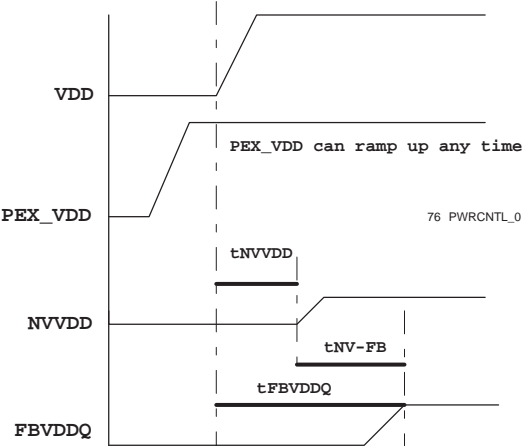
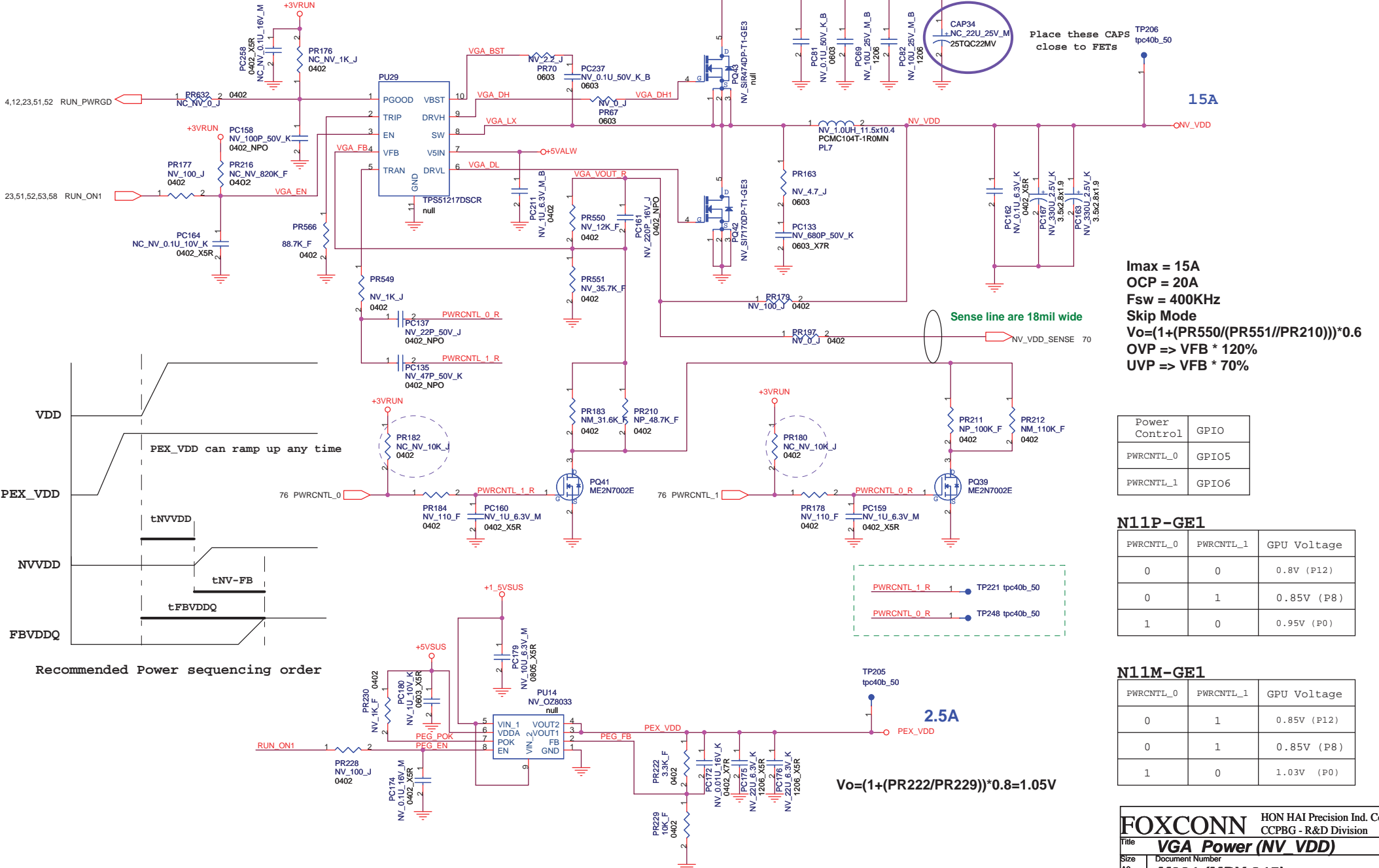
Market Segment Selection MSID[2:0] = [100] (SV)

- 416056_416056_Ard_EDS_Rev.1.1
- 403779_Clarksfield_MPG_Rev1.5



Delete iGPU Path on DVT for Cost Down

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title VGFX Power GFXCORE			
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3A
15A

Place these CAPS close to FETs

Imax = 15A
 OCP = 20A
 Fsw = 400KHz
 Skip Mode
 $V_o = (1 + (PR550 / (PR551 / PR210))) * 0.6$
 OVP => VFB * 120%
 UVP => VFB * 70%

Power Control	GPIO
PWRCTRL_0	GPIO5
PWRCTRL_1	GPIO6

N11P-GE1

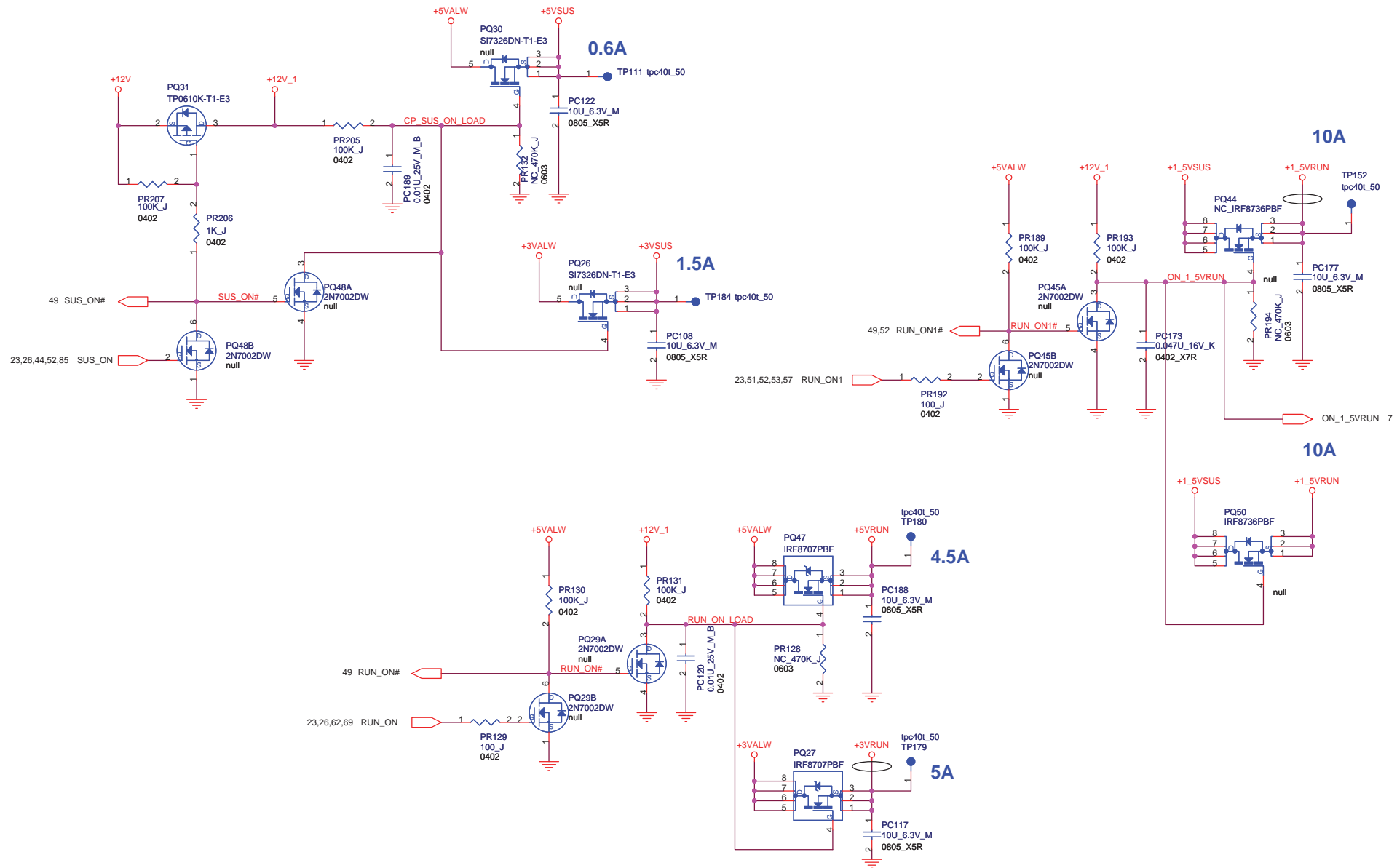
PWRCTRL_0	PWRCTRL_1	GPU Voltage
0	0	0.8V (P12)
0	1	0.85V (P8)
1	0	0.95V (P0)

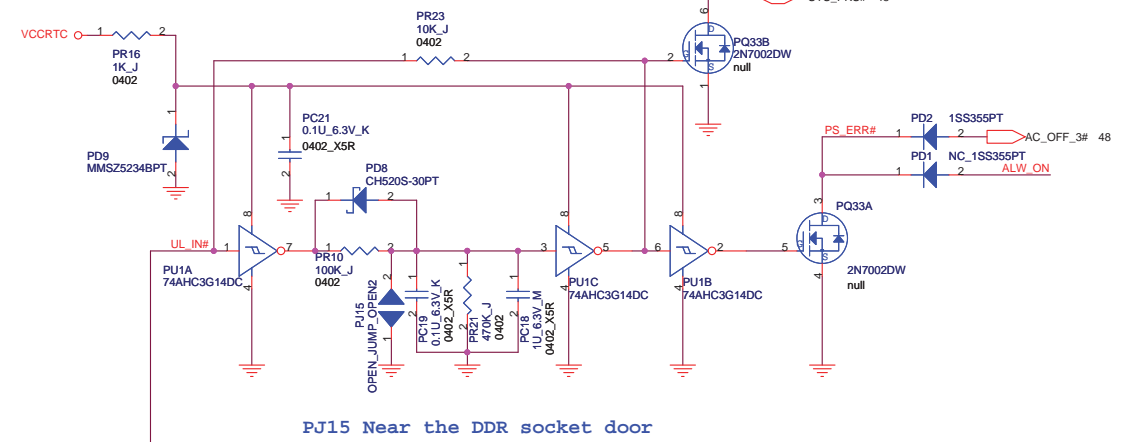
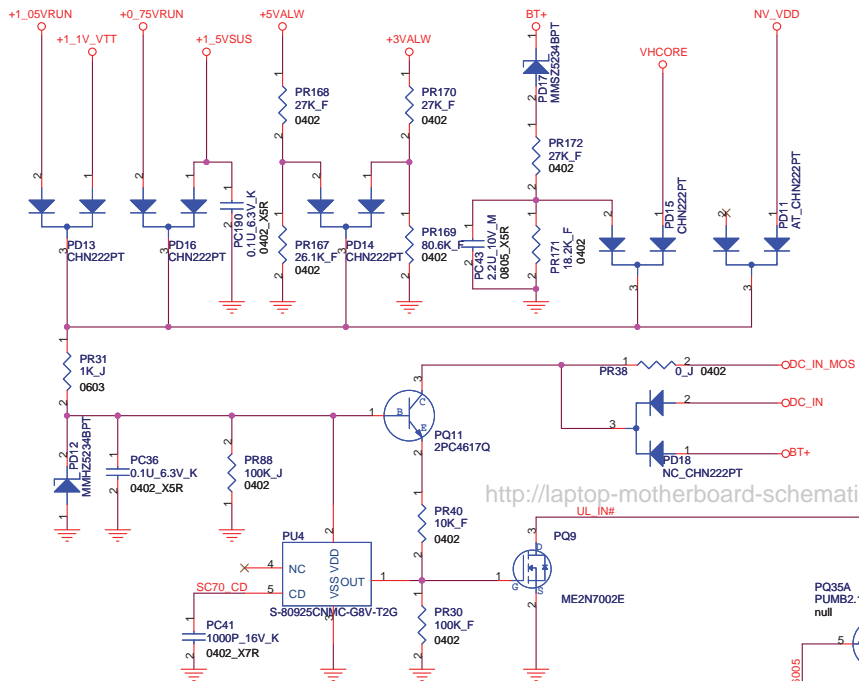
N11M-GE1

PWRCTRL_0	PWRCTRL_1	GPU Voltage
0	1	0.85V (P12)
0	1	0.85V (P8)
1	0	1.03V (P0)

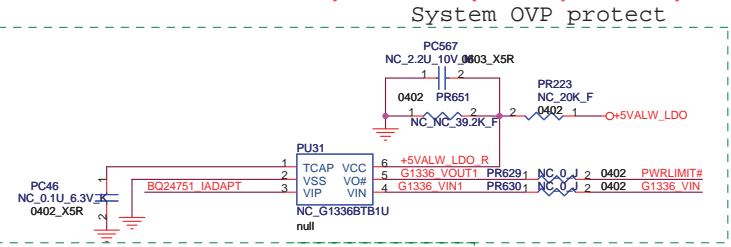
2.5A

$V_o = (1 + (PR222 / PR229)) * 0.8 = 1.05V$

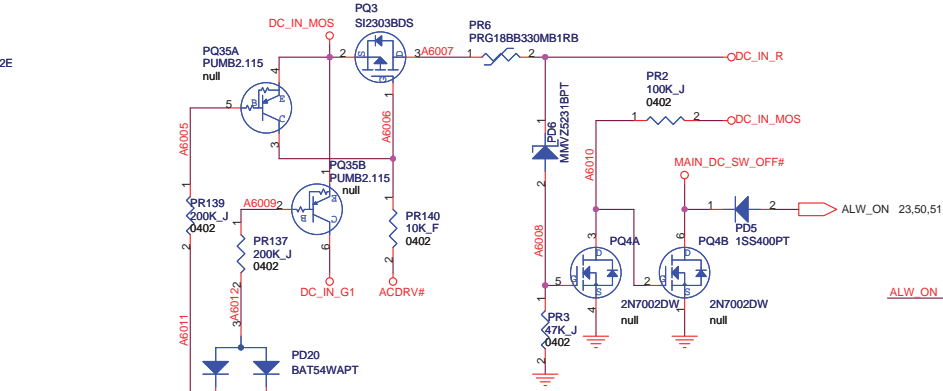




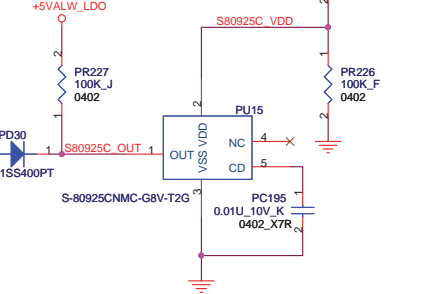
PJ15 Near the DDR socket door



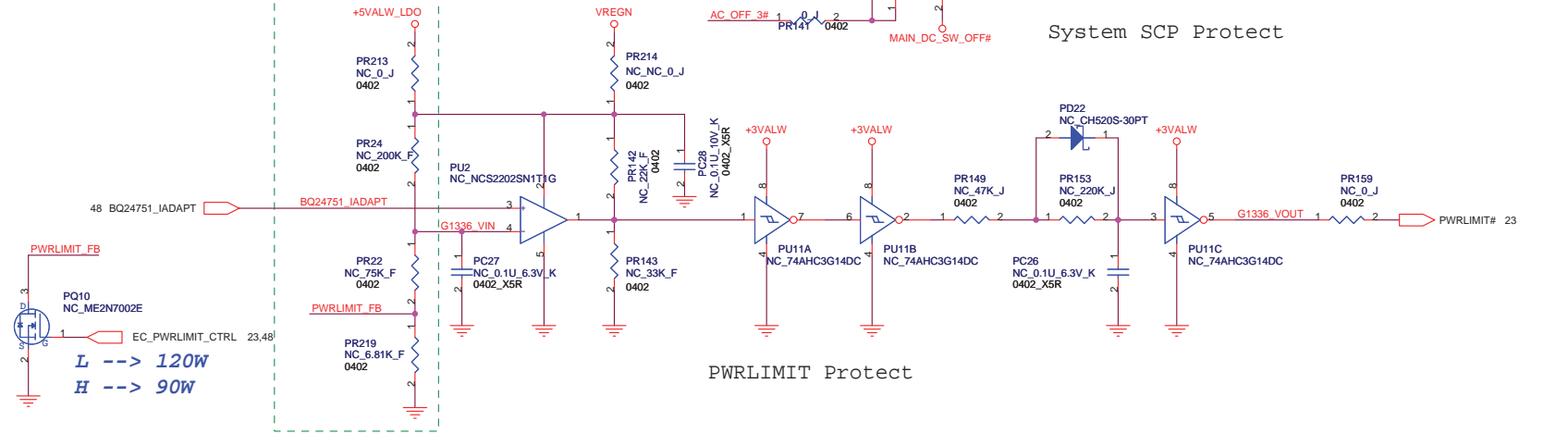
System OVP protect



System SCP Protect



Battery UVP Protect



PWRLIMIT Protect

L --> 120W
H --> 90W

VIINP	90W adaptor	120W adaptor
PWRLIMIT	4.5A 87W	6.05A 114W

adaptor max load : 5.7A/3000ms
adaptor OCP : 7.5Amax

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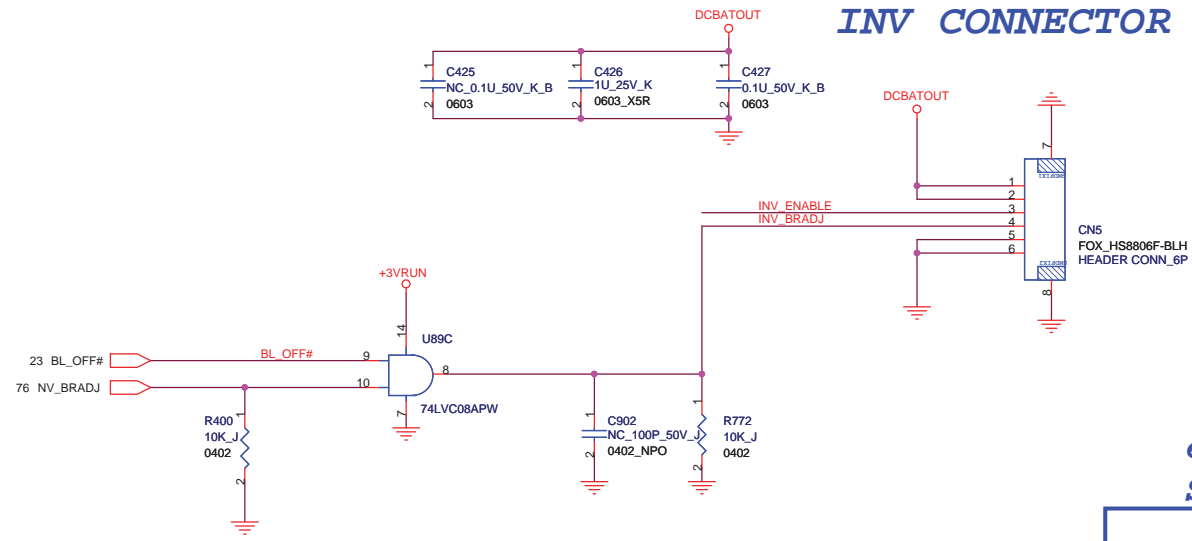
Title: **OVP protection**

Size: Document Number

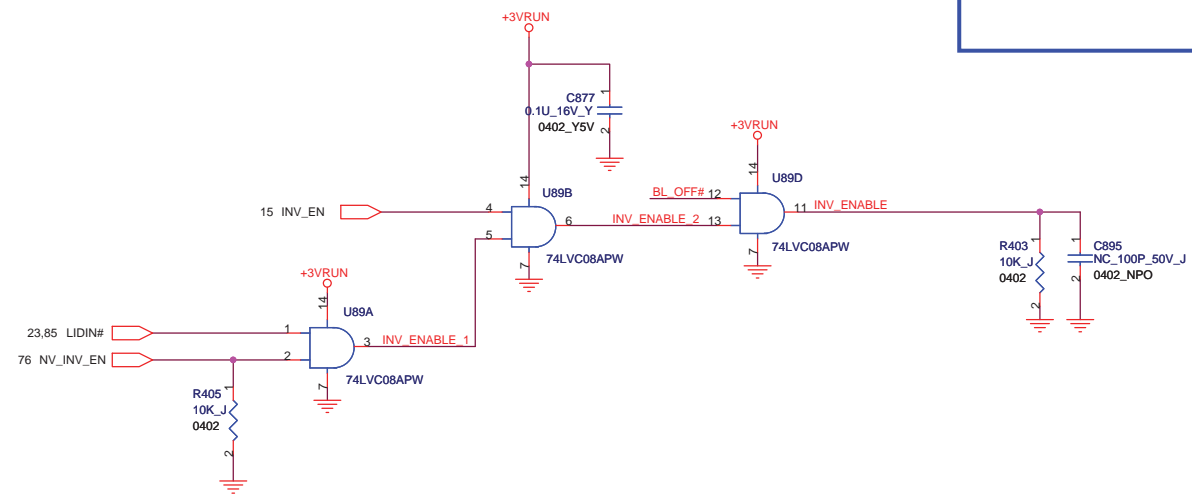
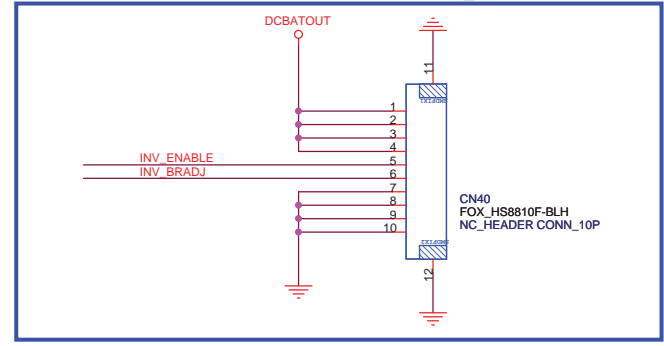
Custom: **M931 (MBX-215)** Rev: **SA**

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INV CONNECTOR

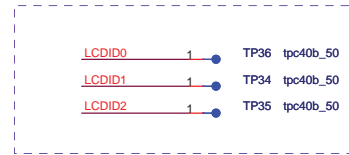


eDP (Suzaku3 support) >>
 Stuff CN40 , Dummy CN5

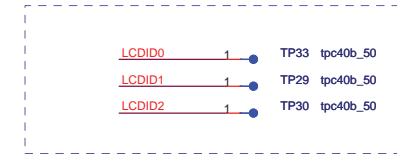


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Title INV CONNECTOR			
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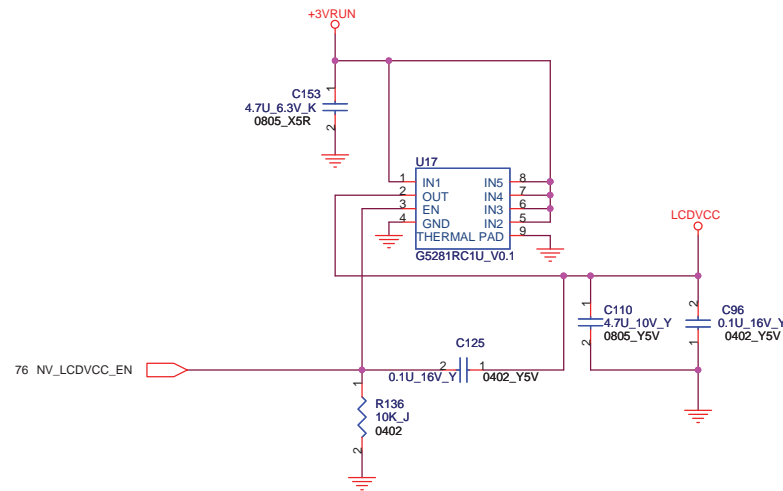
Bot-Side



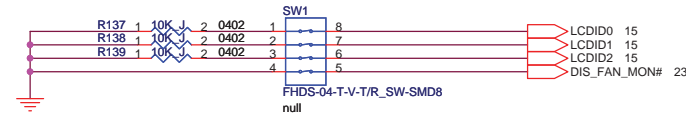
Top-Side



LCDVCC Power

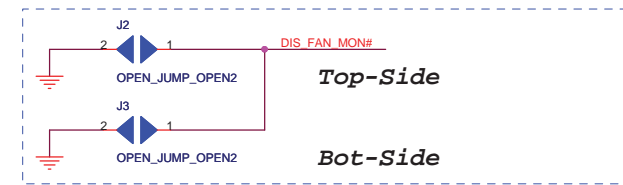


PANEL ID

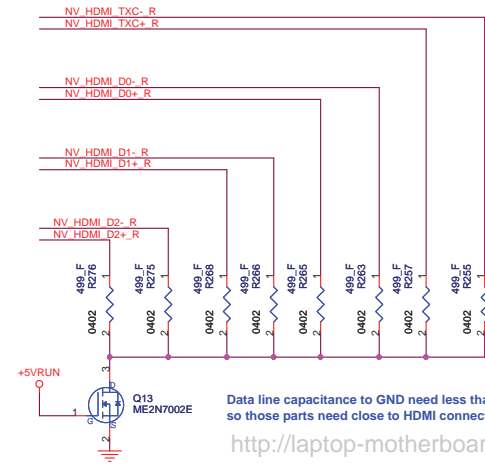
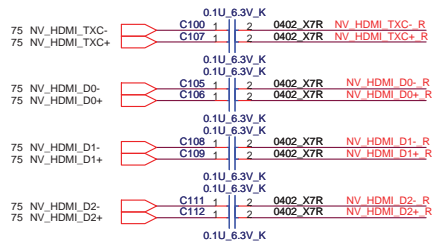


SW1 (Panel ID)	LCDID2	LCDID1	LCDID0	FAN Lock
CRT (No LCD)	0	0	0	ON: Disable OFF: Enable
EW1 (Sharp)	0	0	1	
RESERVED	0	1	0	
EW1 (LGD)	0	1	1	
EW3 (Sharp)	1	0	0	
RESERVED	1	1	0	
RESERVED	1	1	1	

ON:0 , OFF:1

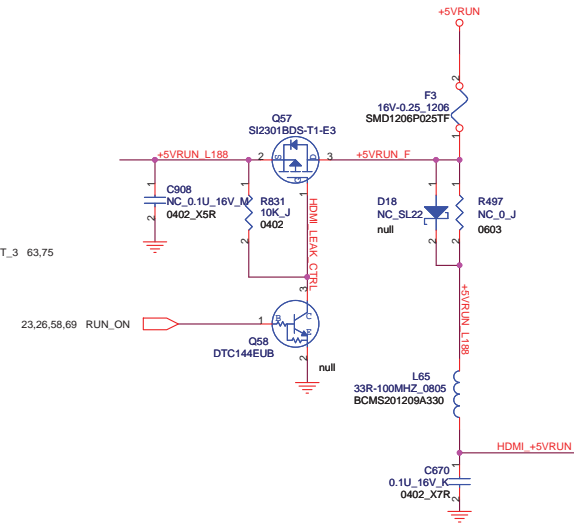
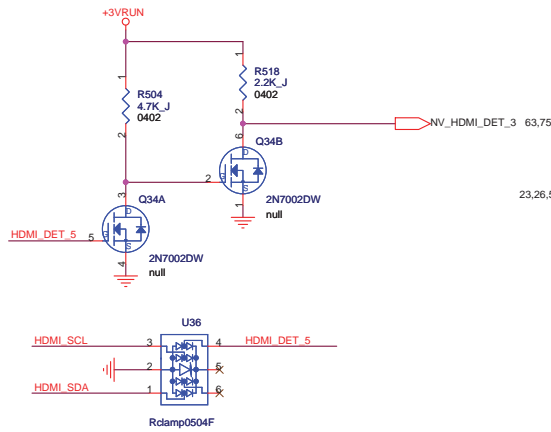
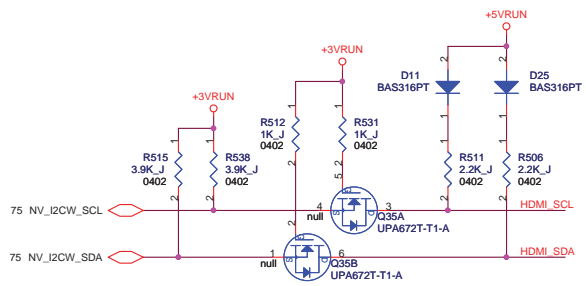
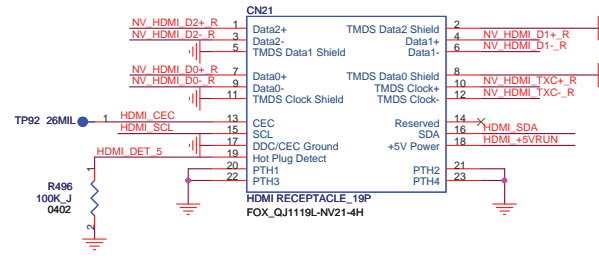


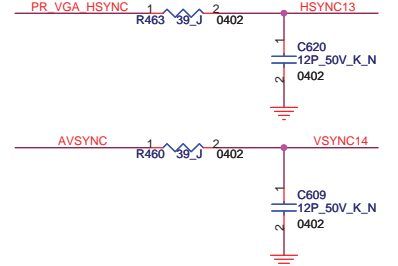
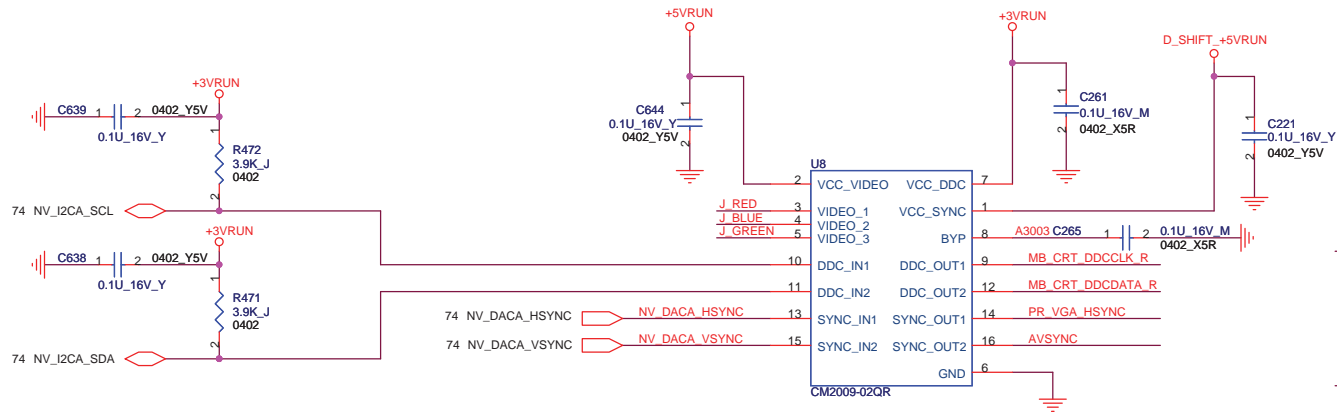
DIS_FAN_MON# for L6 BFT Test



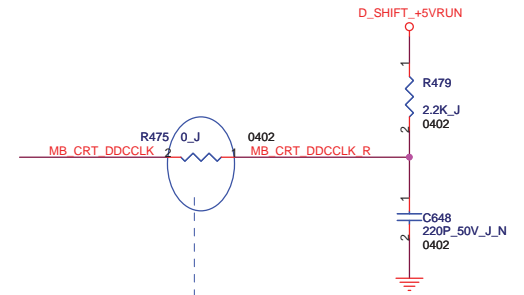
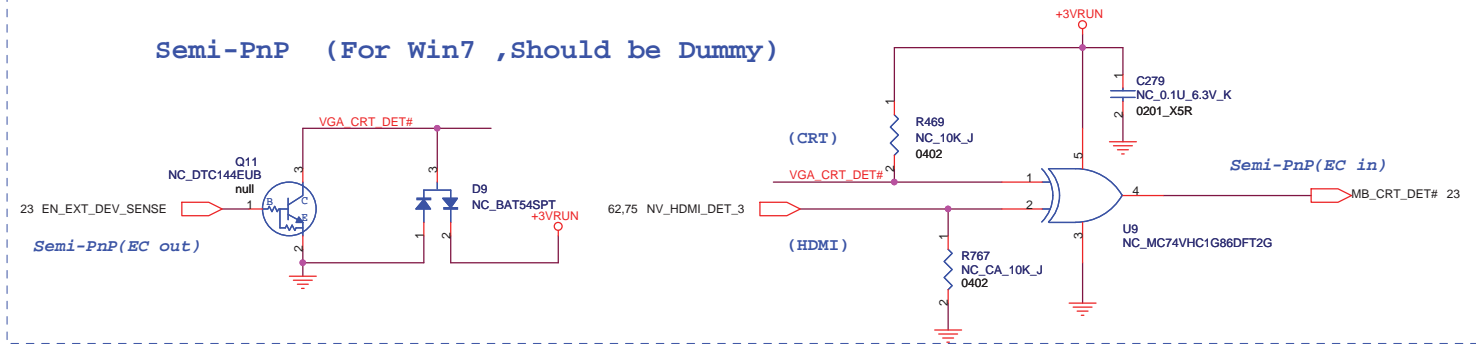
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

<http://laptop-motherboard-schematic.blogspot.com/>

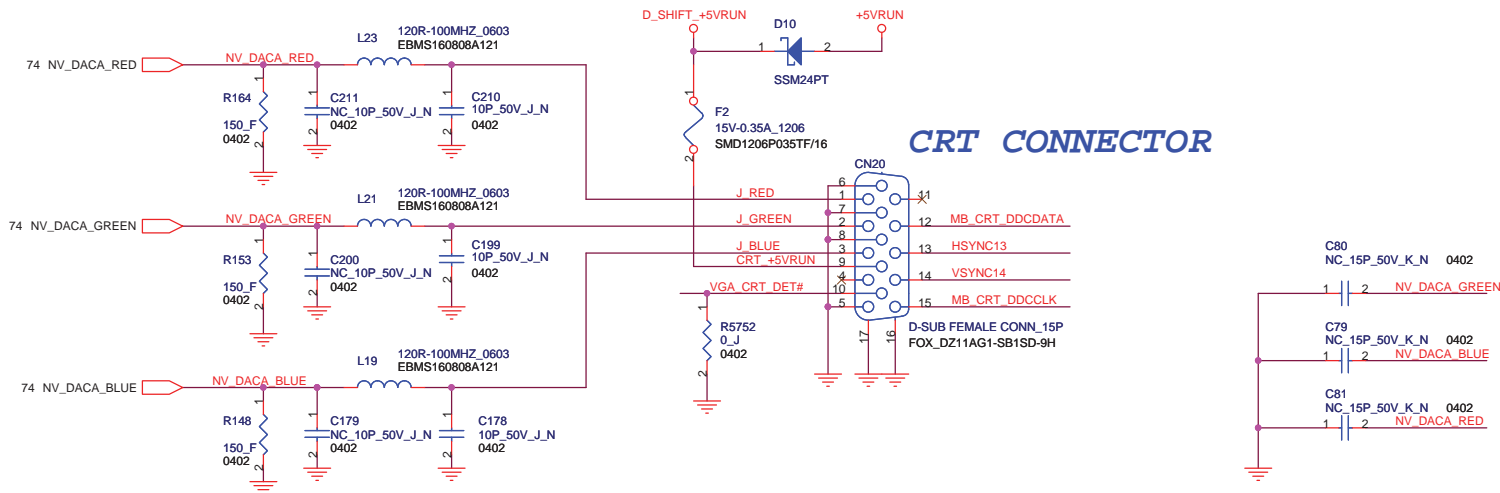




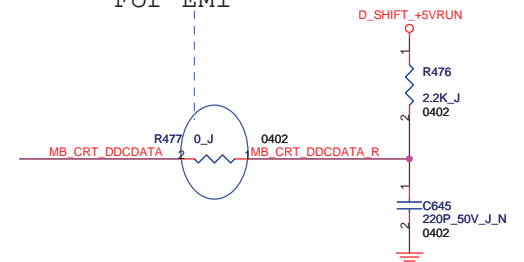
Semi-PnP (For Win7 ,Should be Dummy)



For EMI

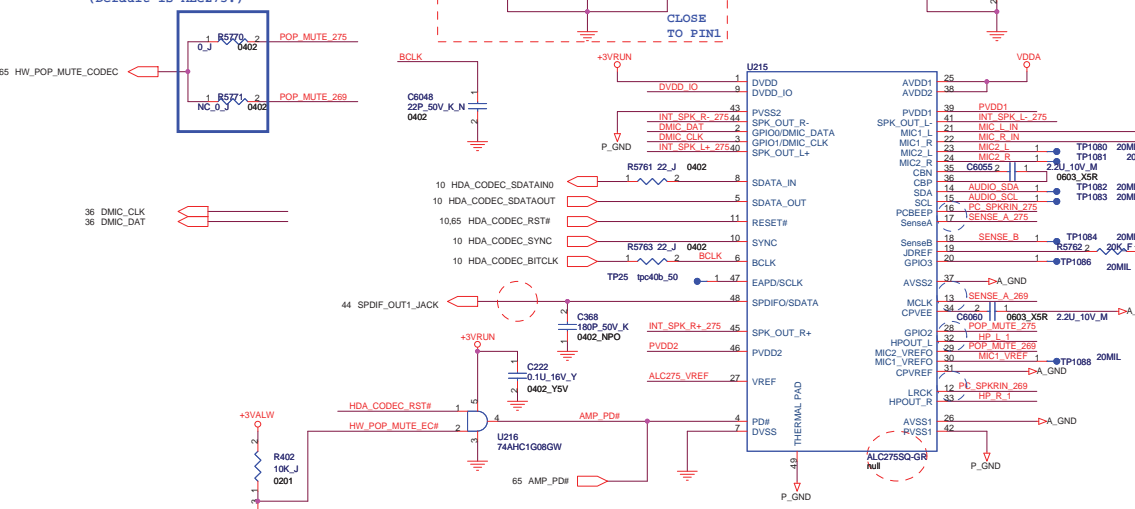


CRT CONNECTOR



DVDD_IO can be either 1.5V or 3.3V Resume wall power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as FCH VCCSUSHDA power.

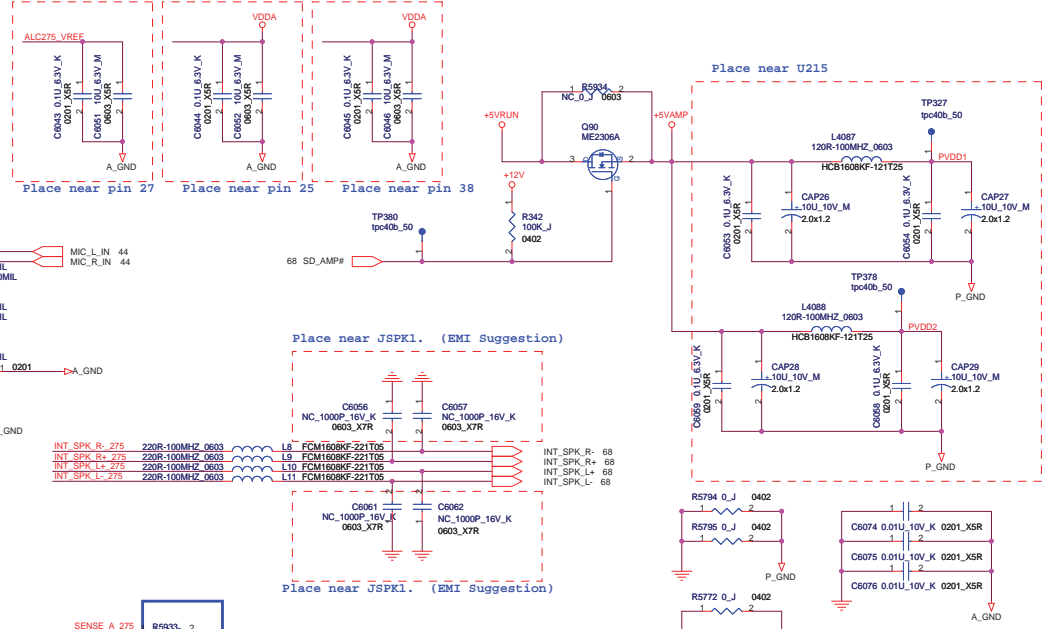
BOM Option for ALC275 and ALC269
(Default is ALC275.)



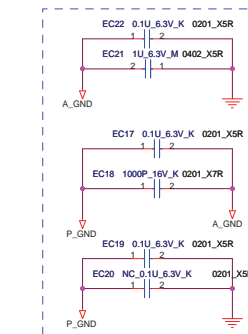
<http://laptop-motherboard-schematic.blogspot.com/>

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal! Please System BIOS Engineer Note
1. If you want the system make warning signal after power on, please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before. .)

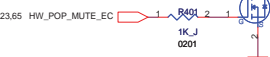
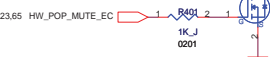
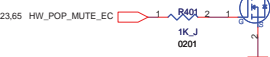
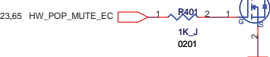
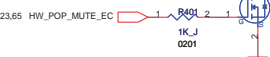
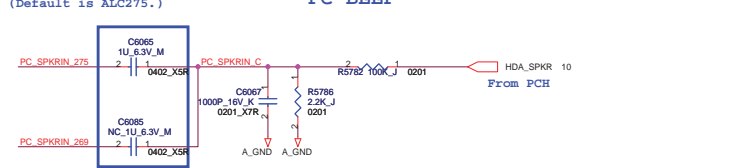
BOM Option for ALC275 and ALC269
(Default is ALC275.)

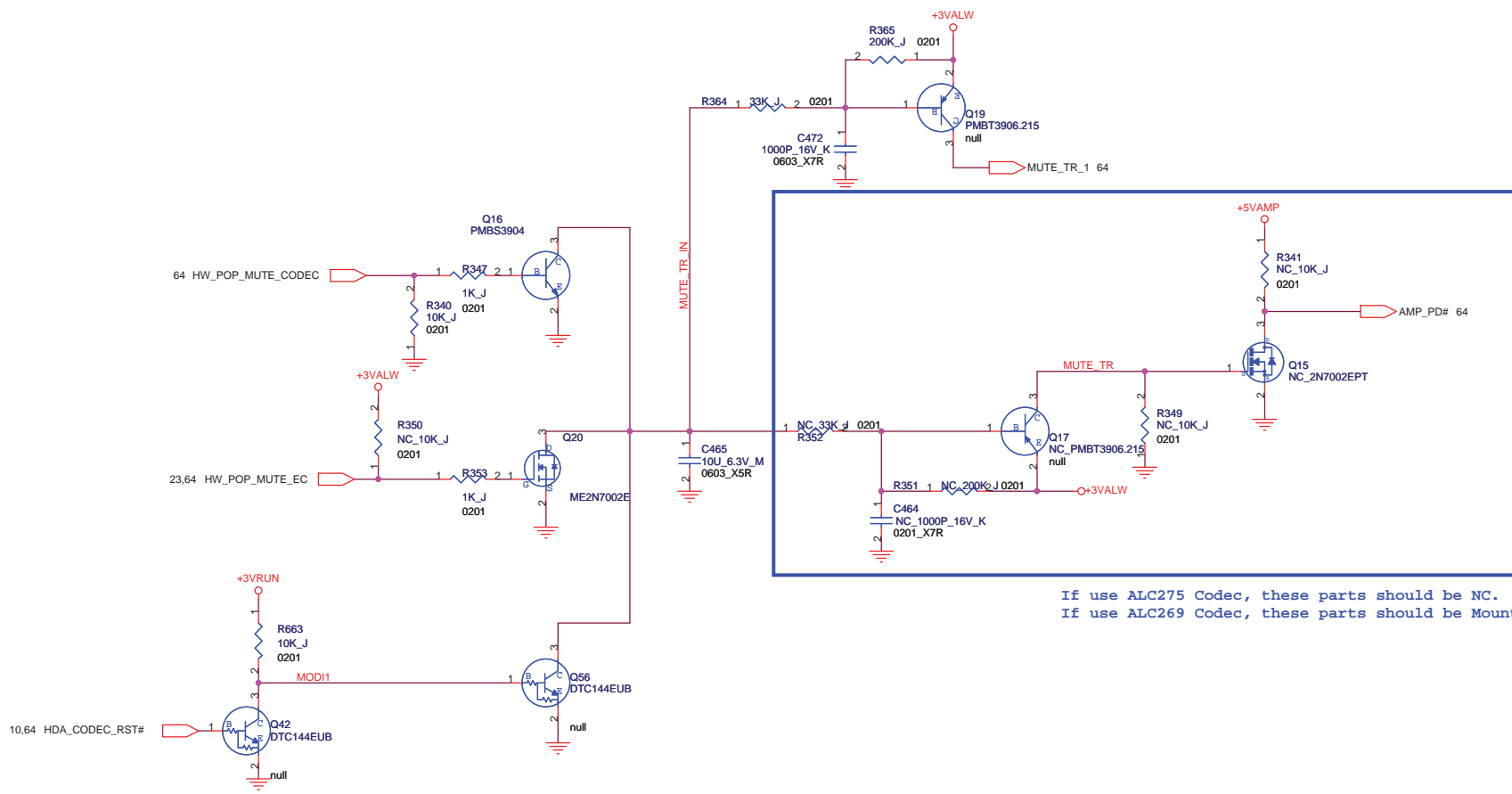


BOM Option for ALC275 and ALC269
(Default is ALC275.)

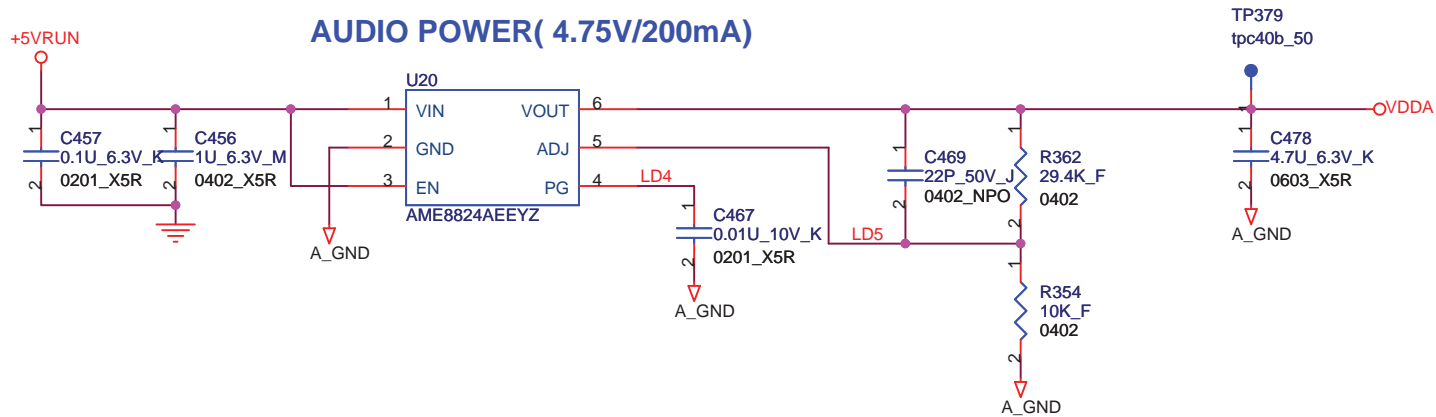


BOM Option for ALC275 and ALC269
(Default is ALC275.)





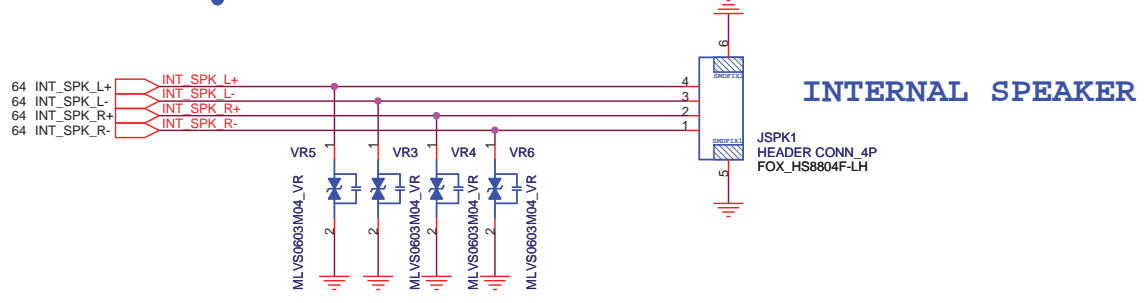
If use ALC275 Codec, these parts should be NC.
 If use ALC269 Codec, these parts should be Mount.



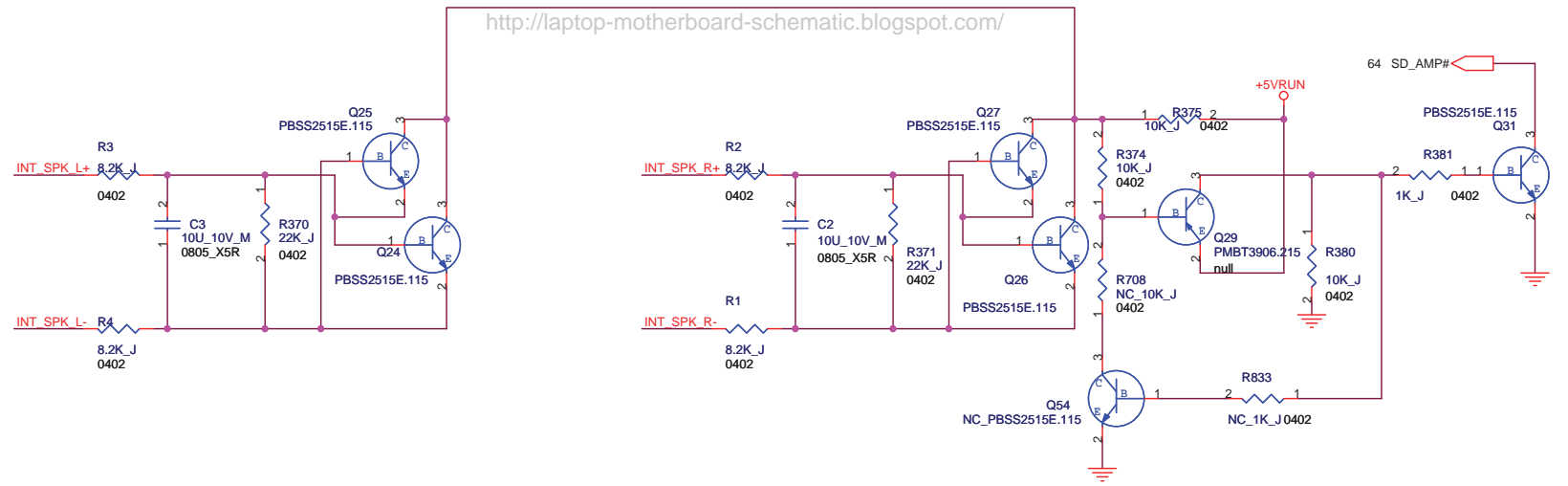
Delete Class D Amp. when implemented ALC275.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title		AUDIO SPEAKER AMP	
Size	Document Number	Rev	
A3	M931 (MBX-215)	SA	
Date:	Wednesday, January 06, 2010	Sheet	67 of 93

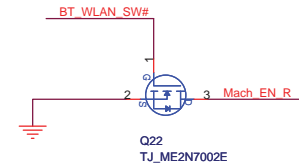
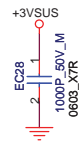
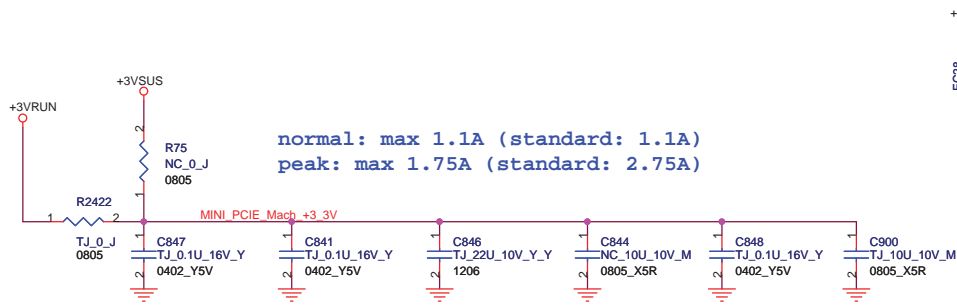
- TP114 tpc40t_50 1 INT_SPK L+
- TP117 tpc40t_50 1 INT_SPK L-
- TP116 tpc40t_50 1 INT_SPK R+
- TP115 tpc40t_50 1 INT_SPK R-



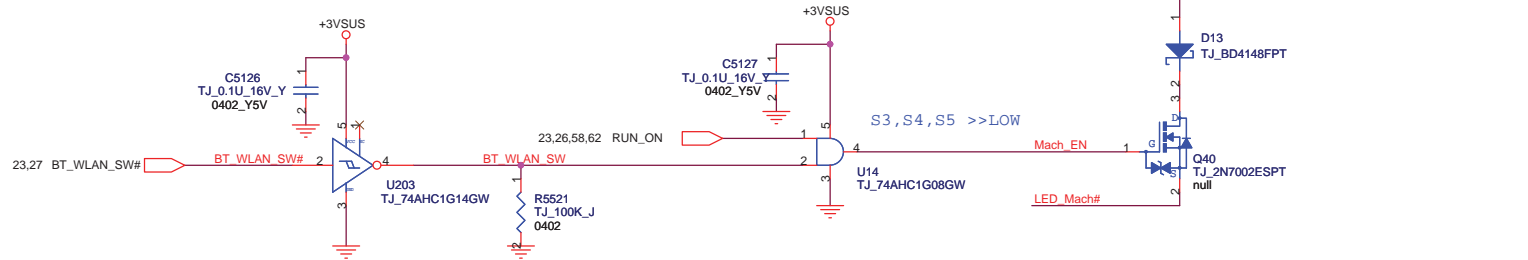
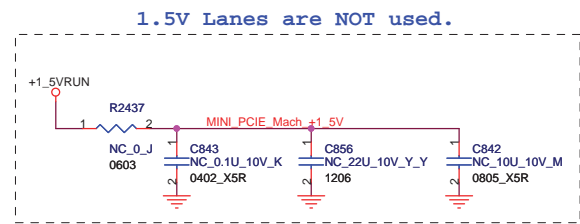
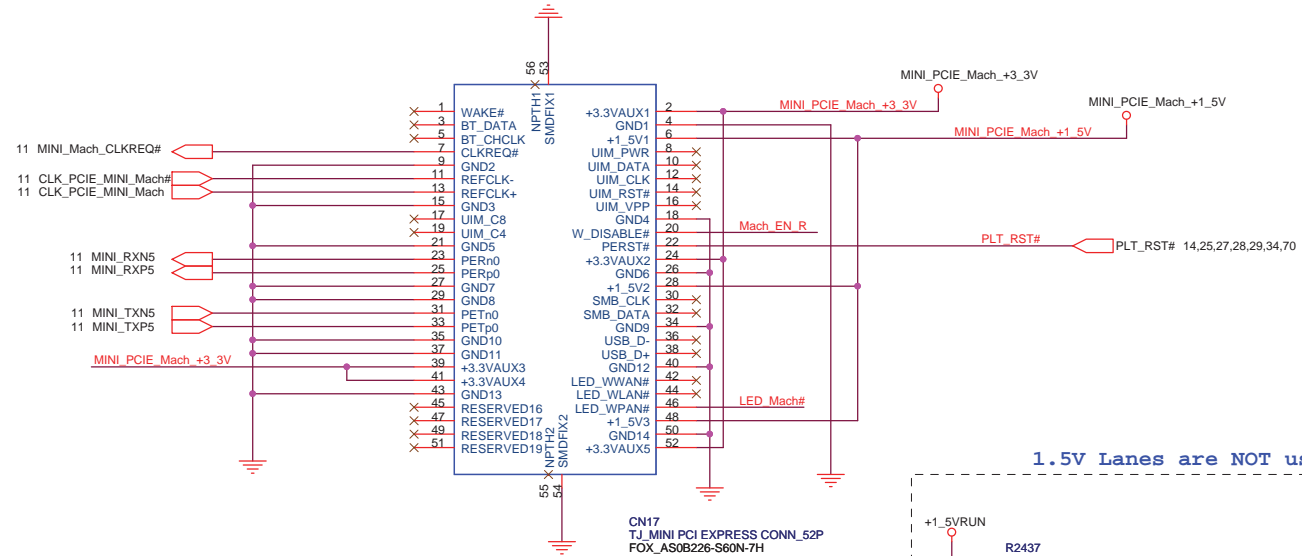
For Shut-down Codec Amp. power (PVDD1 and PVDD2)

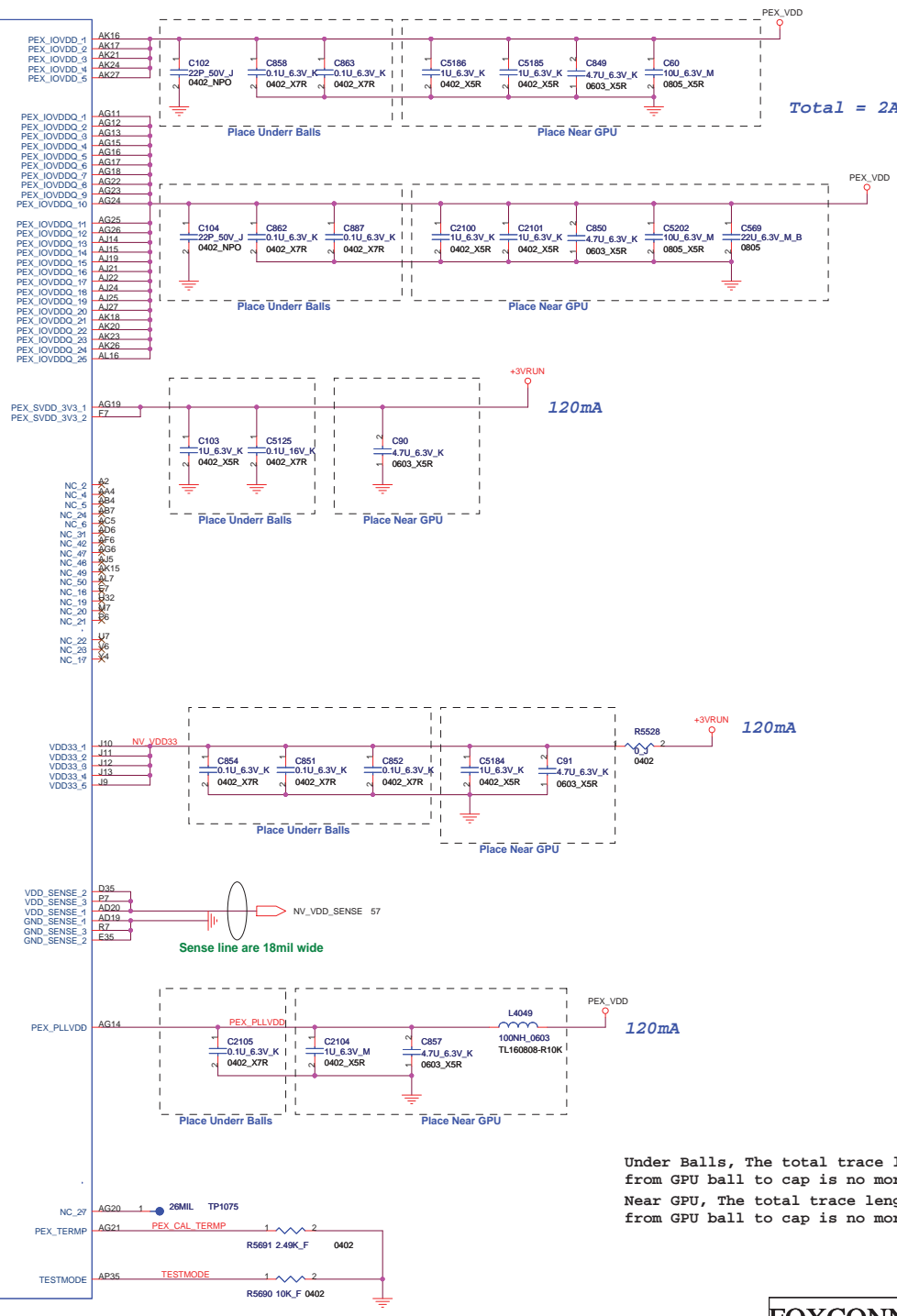
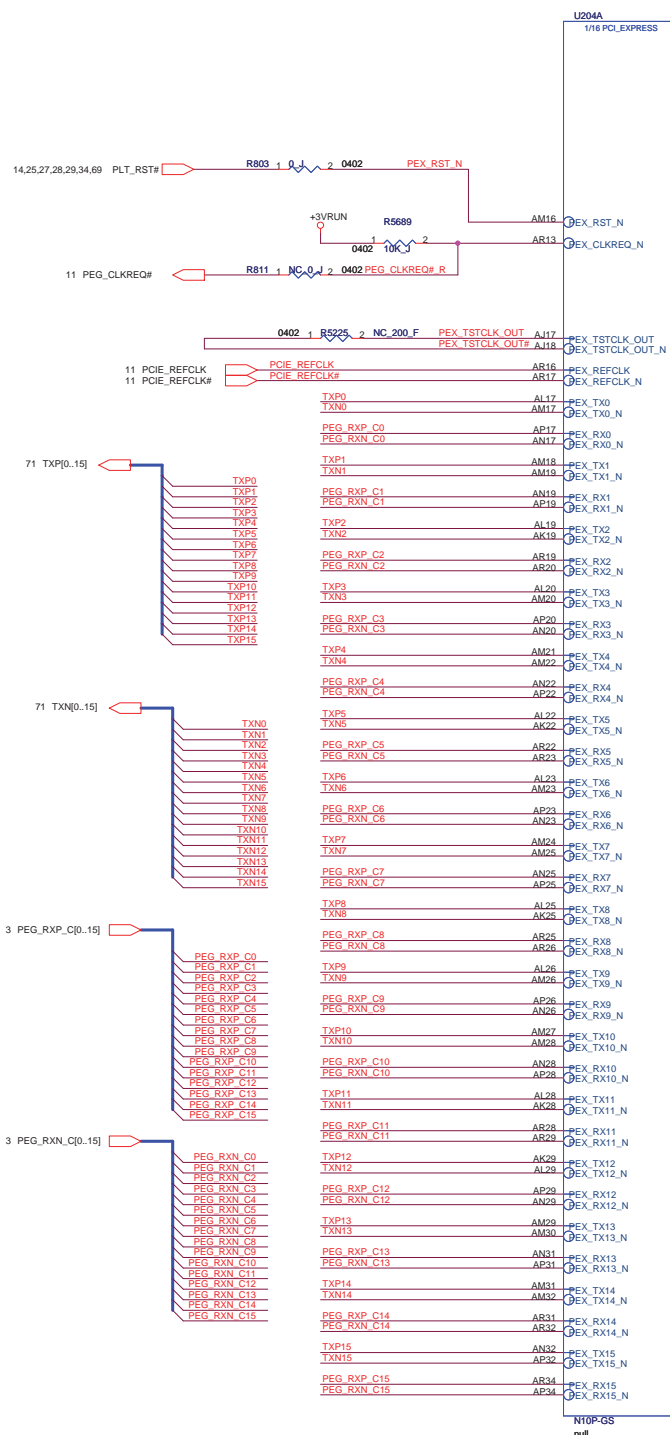


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title AUDIO SPEAKER CONNECTOR			
Size	Document Number		Rev
B	M931 (MBX-215)		SA
Date:	Wednesday, January 06, 2010	Sheet	68 of 93



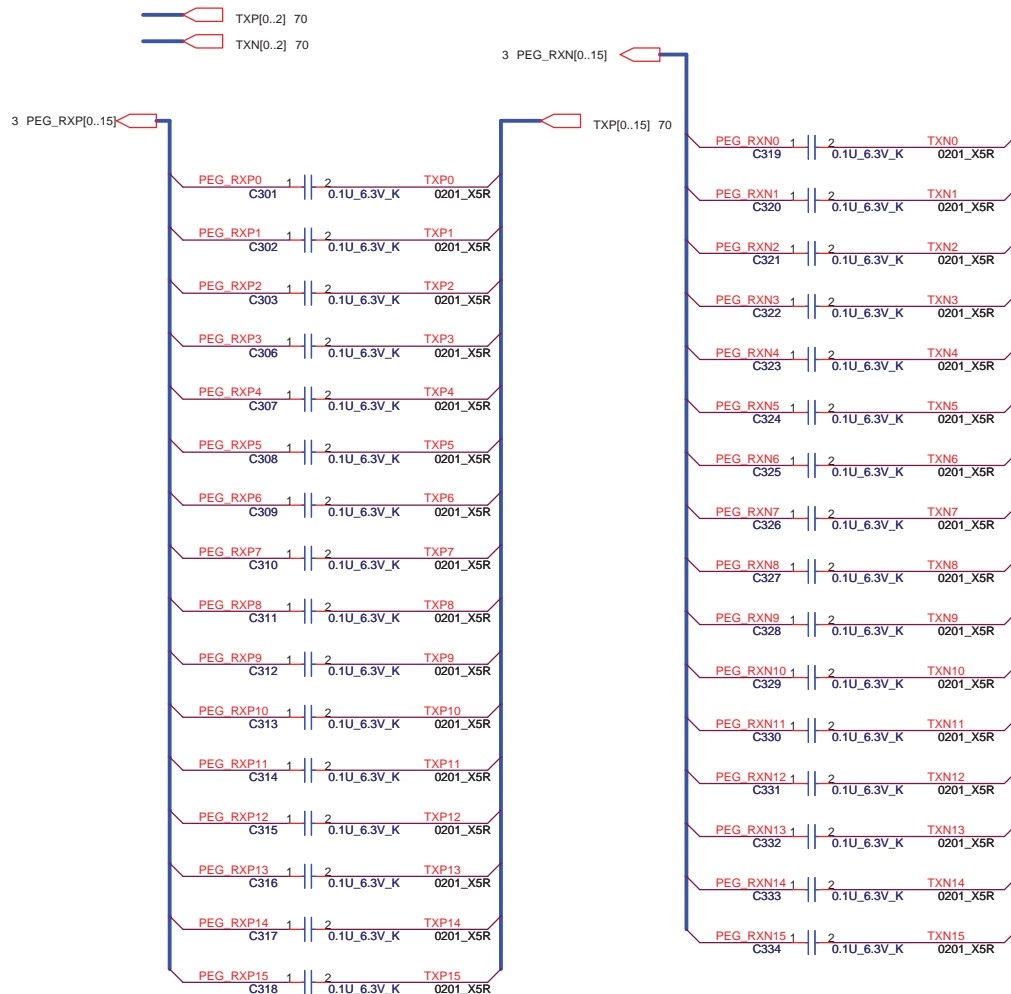
Mach CONN





Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
File	VGA (PCI-E) 1/9		
Size	Document Number		
Custom	M931 (MBX-215)		
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```

XCLK_417
0 (27M Hz)
1 (Reserved)
FB_0_BAR_SIZE
0 256MB
1 (Reserved)
SMB_ALT_ADDR
0 0x9E
1 0x9C(multi-GPU usage)
VGA_DEVICE
0 3D device(class code 302h)
1 VGA device(class code 300h)

SUB_VENDOR
0 (No vedio BIOS ROM)
1 (BIOS ROM is present)

SLOT_CLK_CFG
0 (GPU and MCH not share
a common reference clk)
1 (GPU and MCH share a
common reference clk)

PEX_PLL_EN_TERM
0 (Disable)
1 (Enable)

USER[3:0]
1000

N10x/N11x 3GIO_PADCFG[3:0]
0110

N11x PCI_DEVID[3:0]
N11P-GE1 1001b
N11M-GE1 0101b
PCI DEVICE IDs
N11P-GE1 (0x0A29)
N11M-GE1 (0x0A75)

```

```

ROM_SO
0001

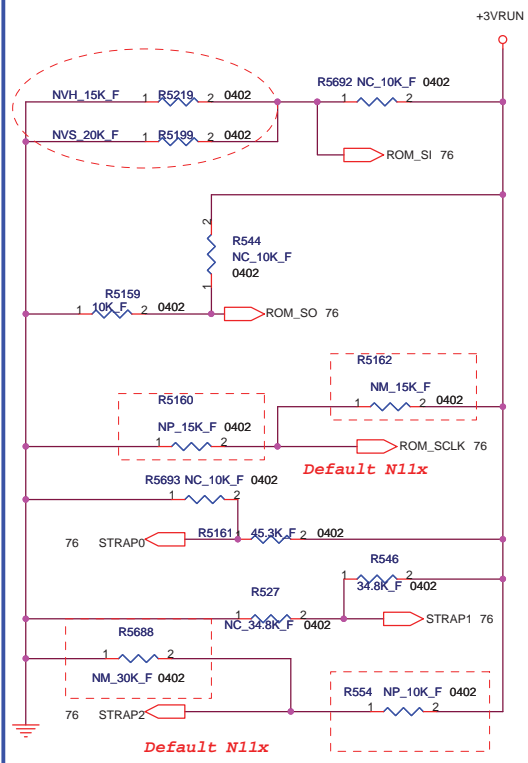
ROM_SCLK
N11P-GE1
0010
N11M-GE1
1010

STRAP0
(1111)

STRAP1
(1110)

Strap2
N11P-GE1
1001
N11M-GE1
0101

```



ROM_SI <http://laptop-motherboard-schematic.blogspot.com/>
0000 64-bit Reserved
0010 64Mx16 DDR3 - 96 ball 128-bit Hynix(13-H5T01G6-3000) 15K Pull Low.
0011 64Mx16 DDR3 - 96 ball 128-bit Samsung(13-K4W1G16-3000) 20K pull Low

Logical Strap bit Mapping

Resistor values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	BGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

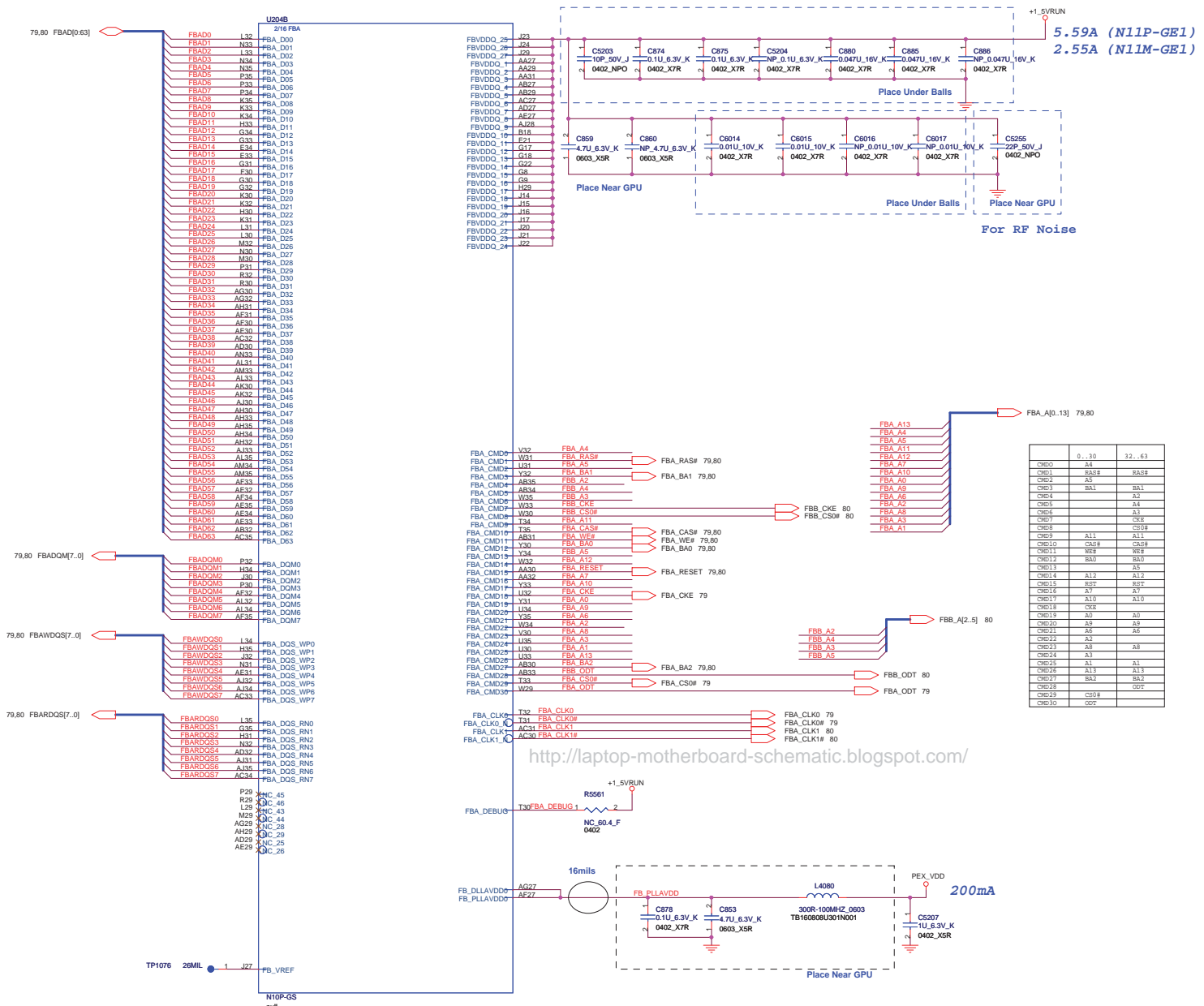
Refer to <GB1 Family Design Guide DG-04202-001_v02_secured>

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Title: **VGA (PCI-E BUS) Strap 2/9**

Size: _____ Document Number: _____ Rev: _____
Customer: **M931 (MBX-215)** SA

Date: **Wednesday, January 06, 2010** Sheet **71** of **93**



5.59A (N11P-GE1)
2.55A (N11M-GE1)

MEM0	0...30	32...63
MEM0	A4	
MEM1	BA5#	BA8#
MEM2	A5	BA1
MEM3	BA1	A2
MEM4	A2	A3
MEM5	A3	A4
MEM6	A4	A5
MEM7	CA8	CA9
MEM8	CA8	CA9
MEM9	BA11	BA11
MEM10	CA9#	CA9#
MEM11	BA8	BA8
MEM12	BA0	BA0
MEM13	A5	A5
MEM14	A12	A12
MEM15	RST	RST
MEM16	A7	A7
MEM17	A10	A10
MEM18	CA8	CA8
MEM19	A0	A0
MEM20	A9	A9
MEM21	A6	A6
MEM22	A2	A2
MEM23	A8	A8
MEM24	A3	A3
MEM25	A1	A1
MEM26	A11	A11
MEM27	BA2	BA2
MEM28	ODT	ODT
MEM29	CA9	CA9
MEM30	ODT	

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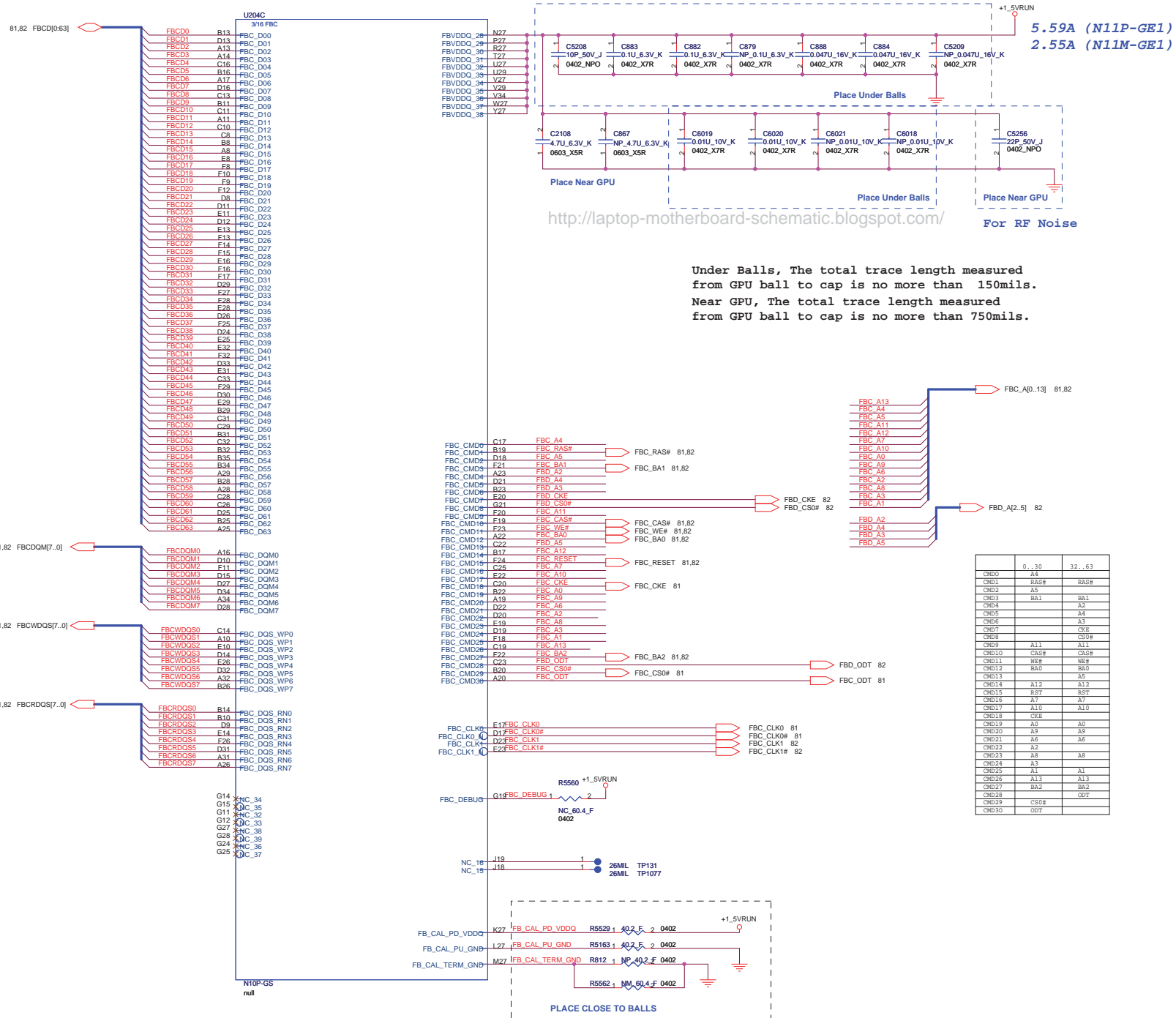
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN HON HAI PRECISION IND. CO., LTD.
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File: **VGA(DDR)# 3/9**

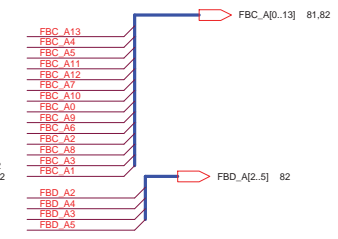
Docu: Document Number
Customer: **M931 (MBX-215)**

Date: Wednesday, January 06, 2010 Sheet 72 of 93



<http://laptop-motherboard-schematic.blogspot.com/> For RF Noise

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.



CMD0	0..30	31..63
CMD0	RAS#	RAS#
CMD1	AS	AS
CMD2	BA1	BA1
CMD3	A2	A2
CMD4	A4	A4
CMD5	A3	A3
CMD6	CKE	CKE
CMD7	CSD#	CSD#
CMD8	A11	A11
CMD9	CAS#	CAS#
CMD10	WE#	WE#
CMD11	BA0	BA0
CMD12	A5	A5
CMD13	A12	A12
CMD14	A7	A7
CMD15	A10	A10
CMD16	A0	A0
CMD17	A9	A9
CMD18	A6	A6
CMD19	A2	A2
CMD20	A8	A8
CMD21	A1	A1
CMD22	A13	A13
CMD23	BA2	BA2
CMD24	ODT	ODT
CMD25	A3	A3
CMD26	A4	A4
CMD27	A6	A6
CMD28	A7	A7
CMD29	A11	A11
CMD30	A5	A5

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File: **VGA(DDR)# 4/9**

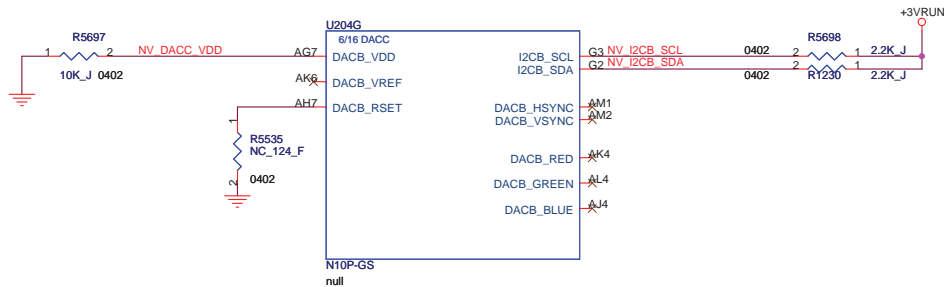
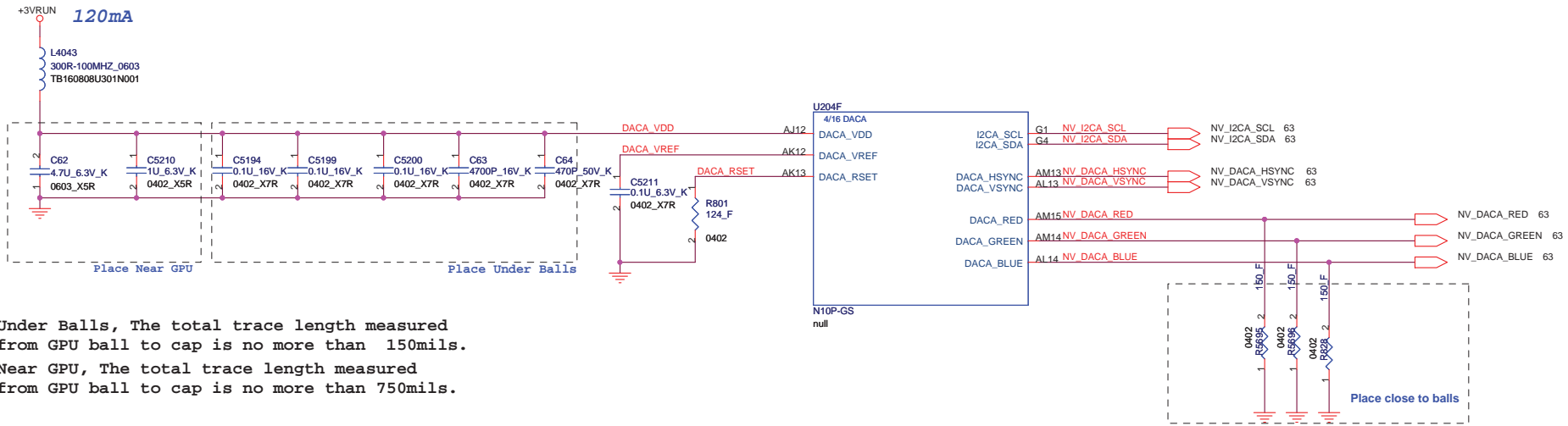
Size: Document Number

Customer: **M931 (MBX-215)**

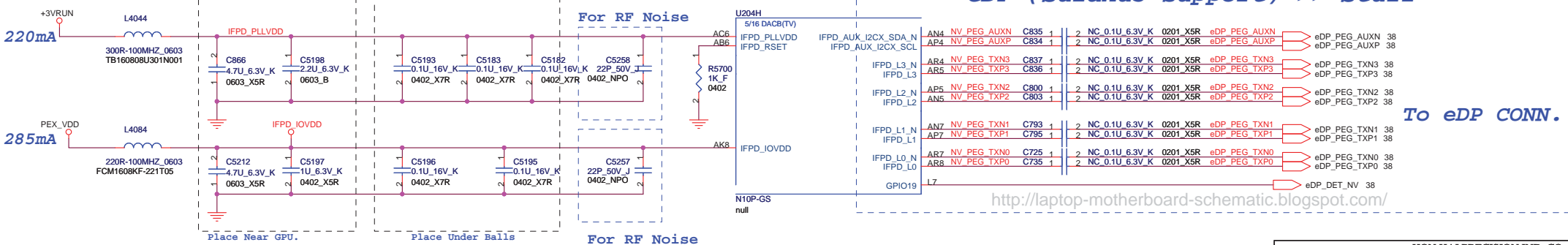
Date: Wednesday, January 06, 2010

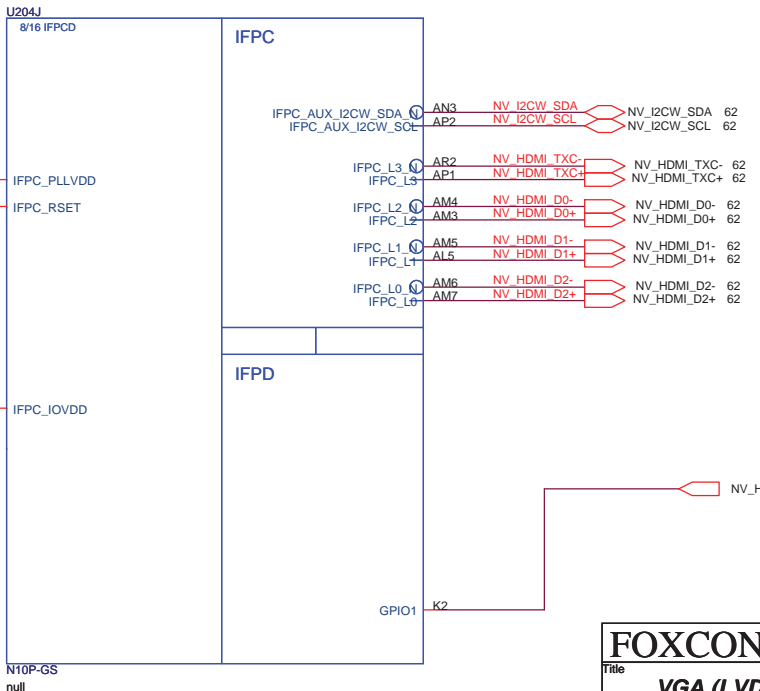
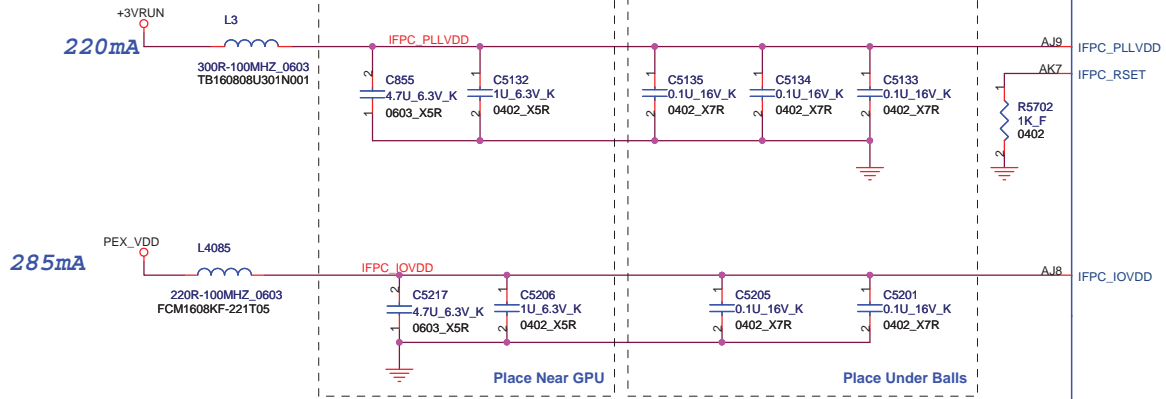
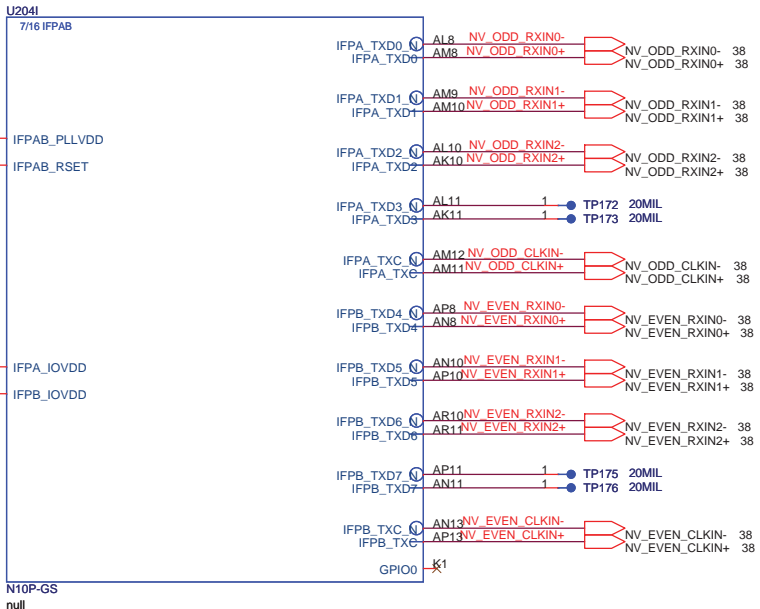
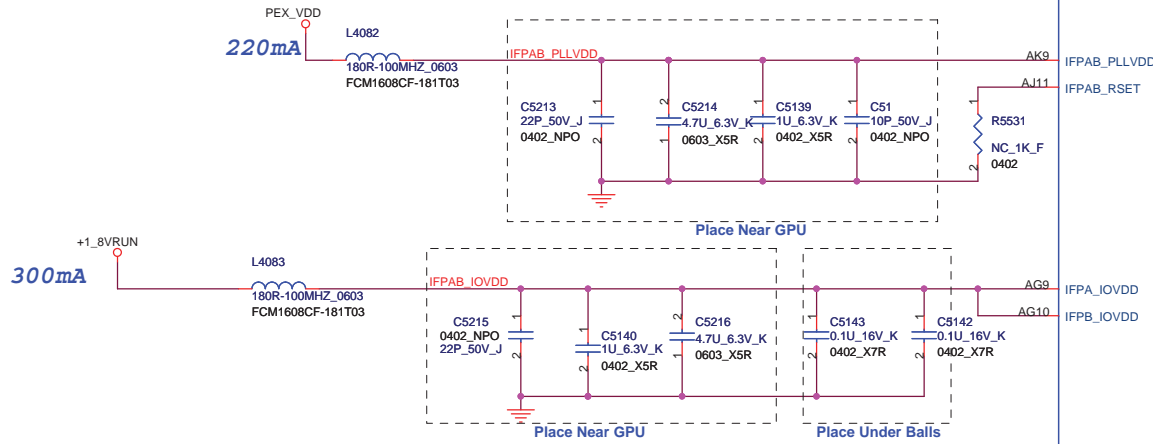
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Rev **SA**



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

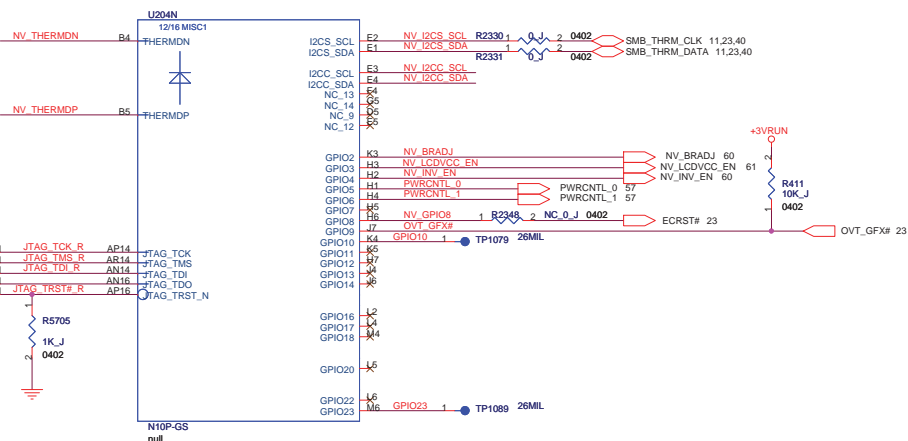
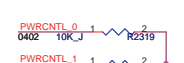
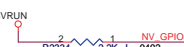
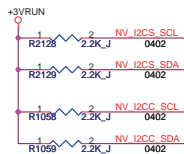
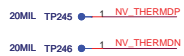
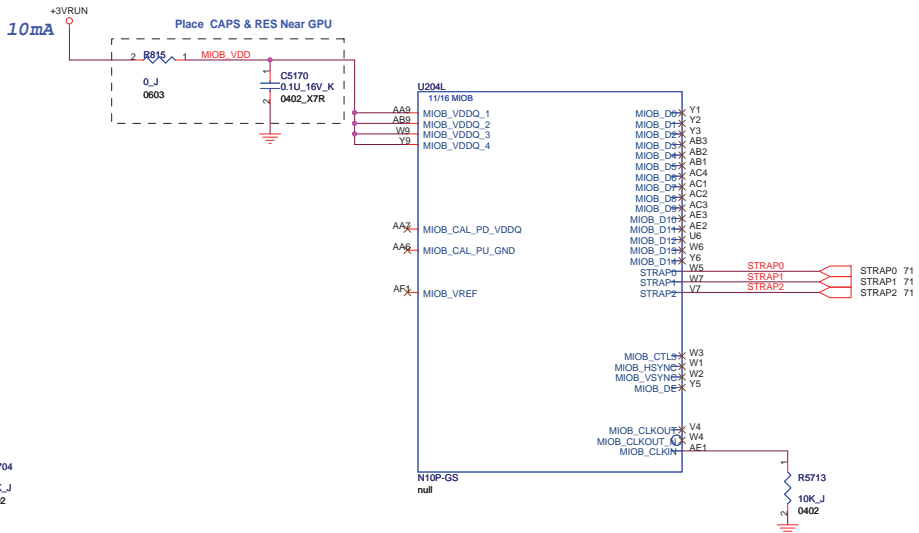
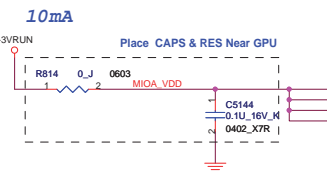
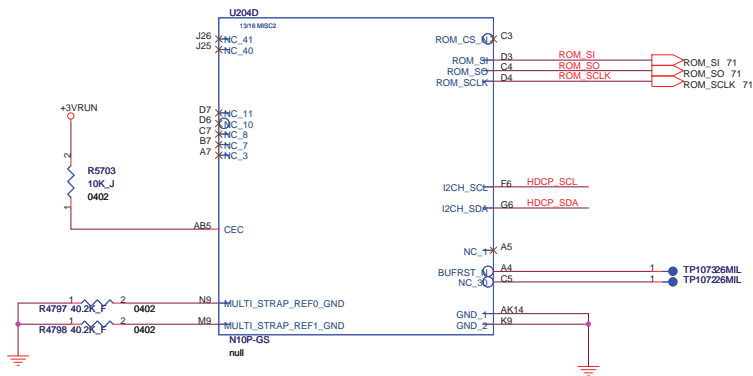
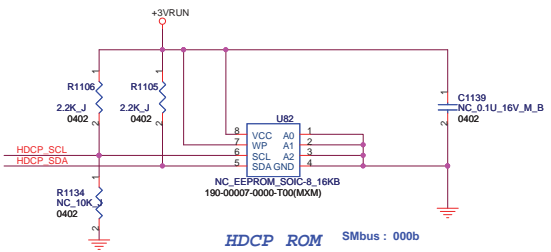




To HDMI CONN.

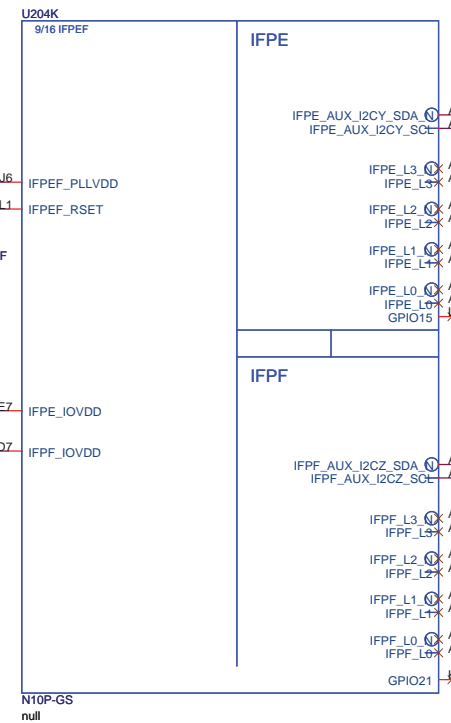
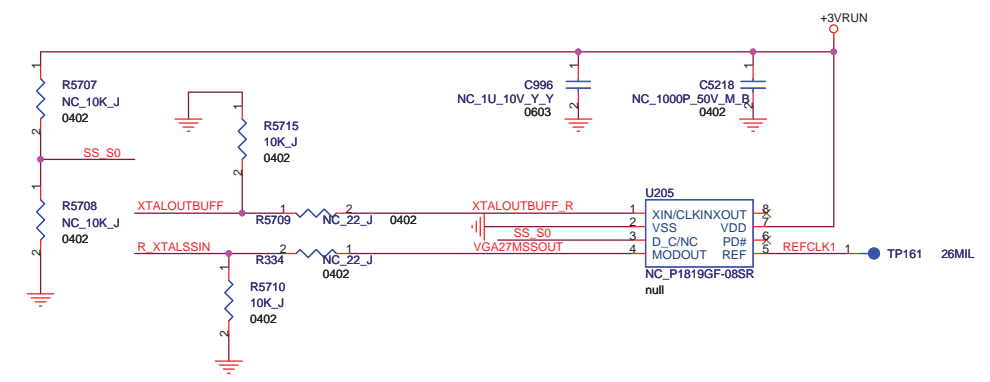
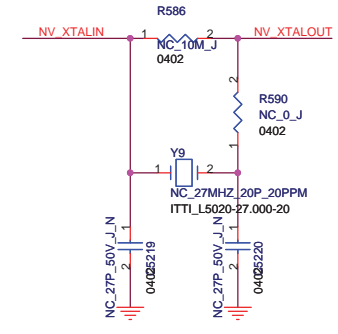
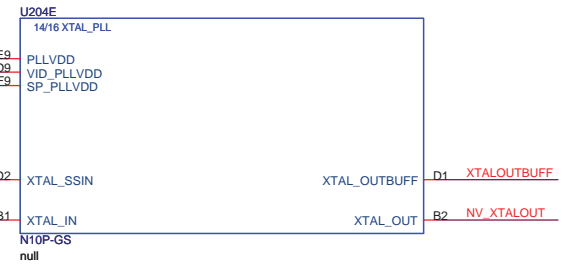
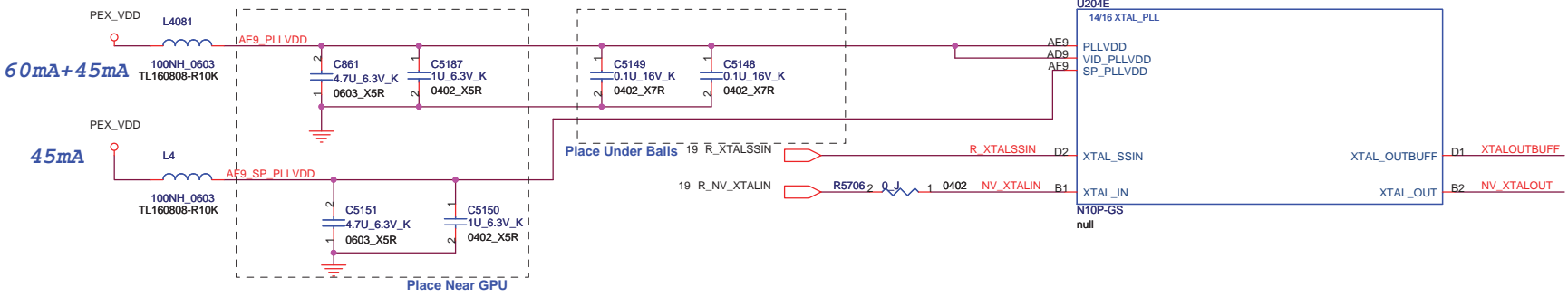
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title VGA (LVDS/HDMI) 6/9	
Size A3	Document Number M931 (MBX-215)
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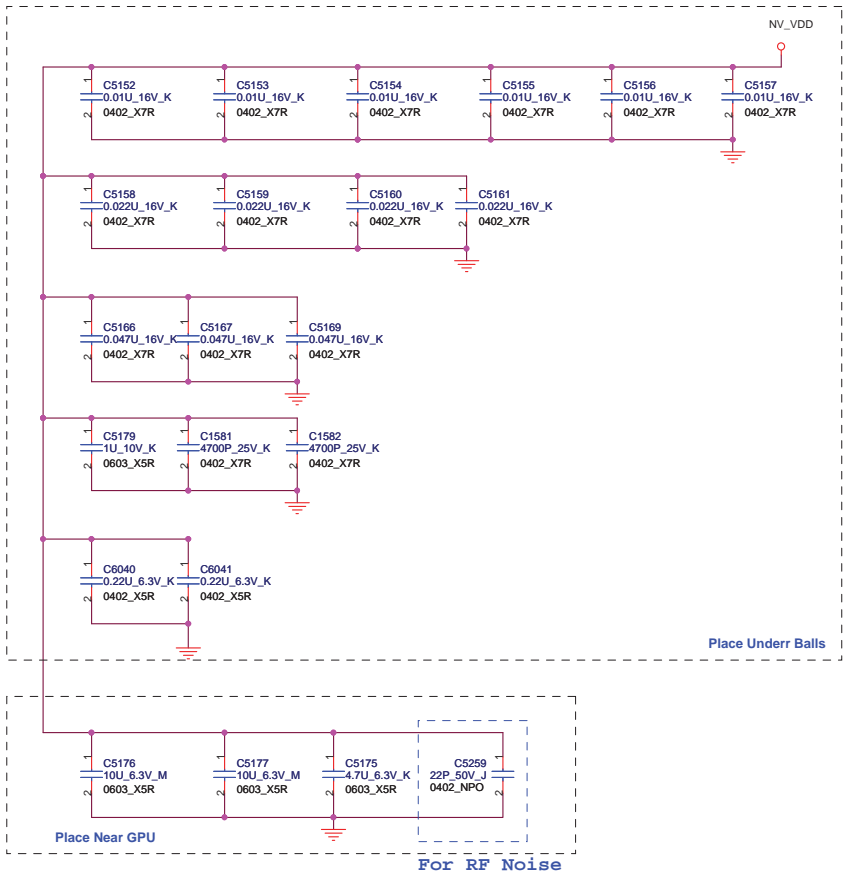
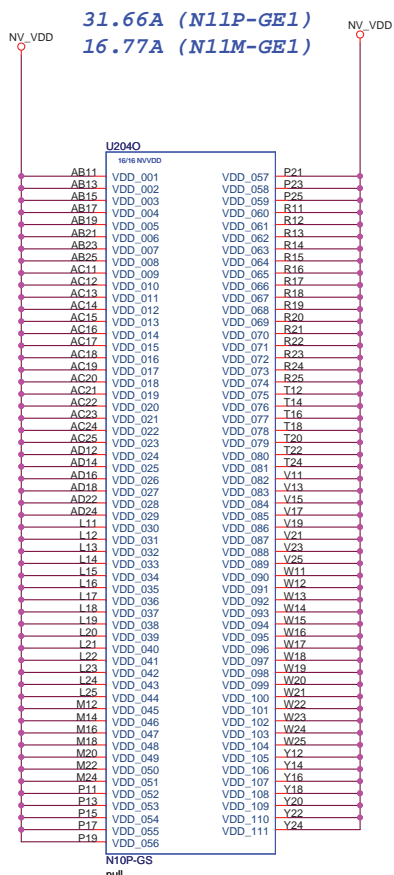
GPIO	I/O	Internal pull low	GPIO TABLE
GPIO0	I	YES	
GPIO1	O	Yes	HDMI Hot Plug Detect 0 (HPD0) Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM) Active High
GPIO3	O	No	Panel Power(LCD0_VDD) Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN) Active High
GPIO5	O	Yes	FOR Power Control NVDD Active High or Low
GPIO6	O	No	FOR Power Control NVDD Active High or Low
GPIO8	O	No	reserve for reset EC
GPIO9	I	No	System Power Limit Alert Input Active Low

SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor



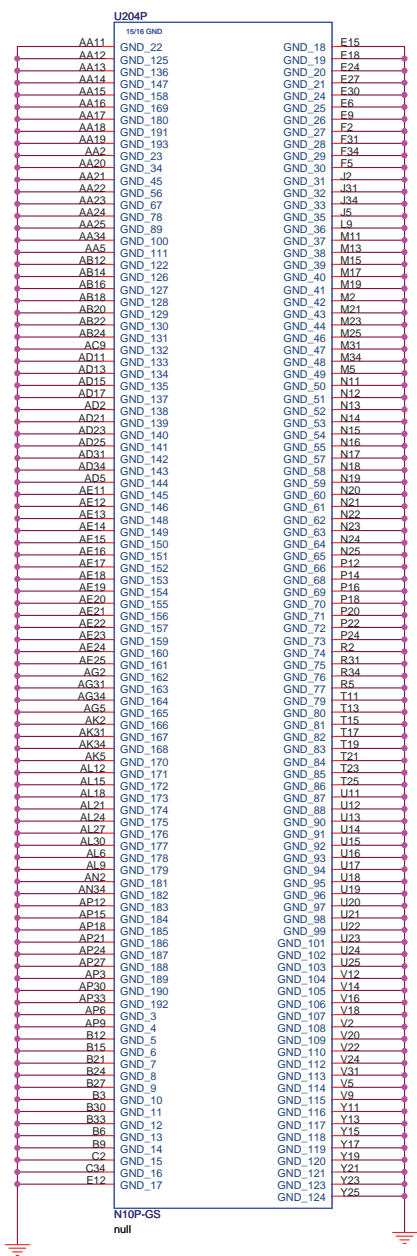
<http://laptop-motherboard-schematic.blogspot.com/>

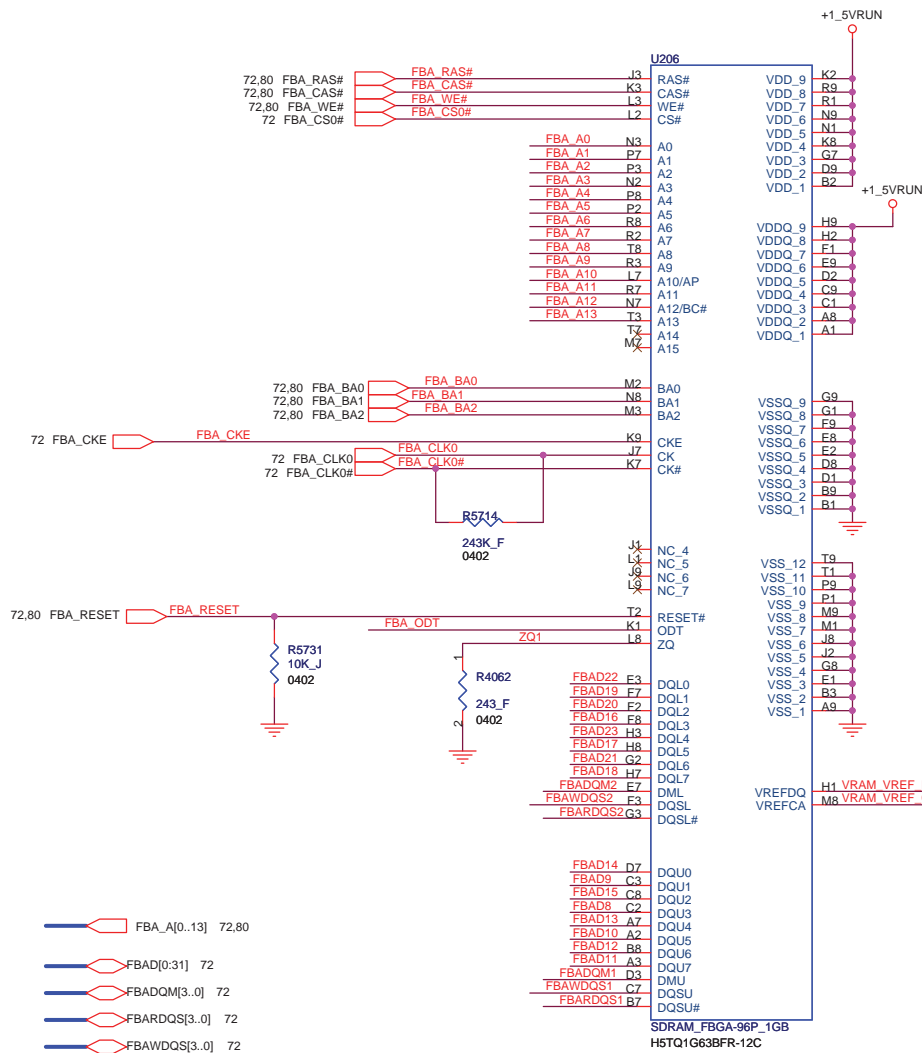
FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title	VGA (XTAL) 8/9
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A3	M931 (MBX-215)
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Rev	SA



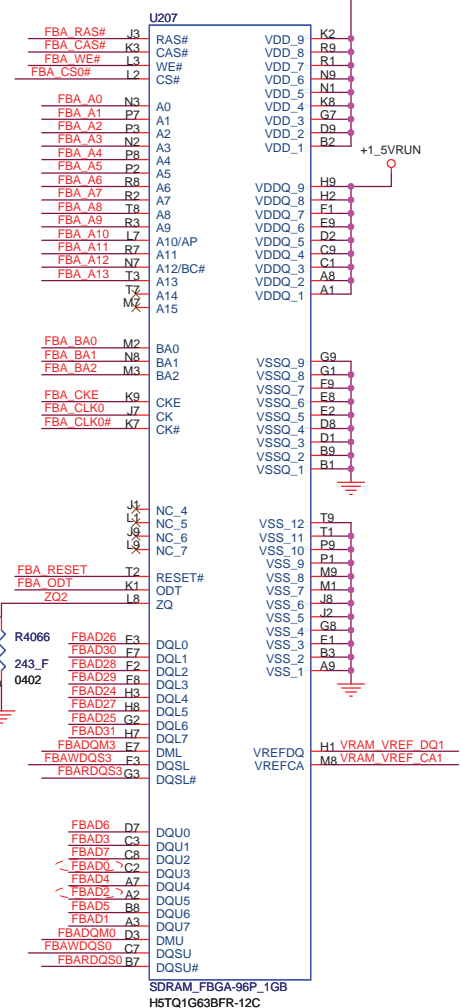
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

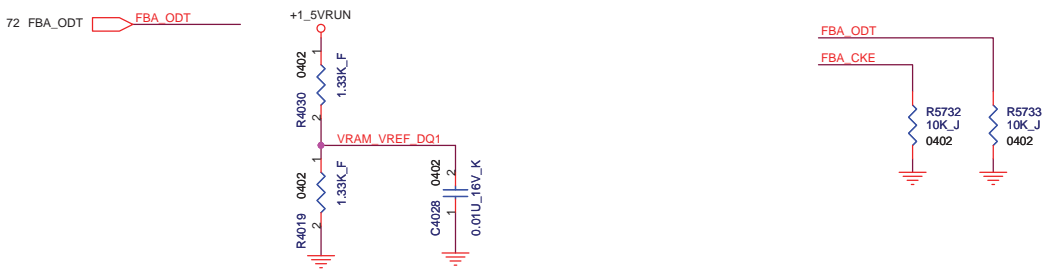




CMD0	0..30	32..63
CMD1	RAS#	RAS#
CMD2	A5	BA1
CMD3	BA1	BA1
CMD4	A2	A4
CMD5	A4	A3
CMD6	A3	A3
CMD7	CKE	CKE
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	CS0#
CMD30	ODT	ODT



- FBA_A[0..13] 72.80
- FBAD[0..31] 72
- FBADQM[3..0] 72
- FBARDQS[3..0] 72
- FBAWDQS[3..0] 72

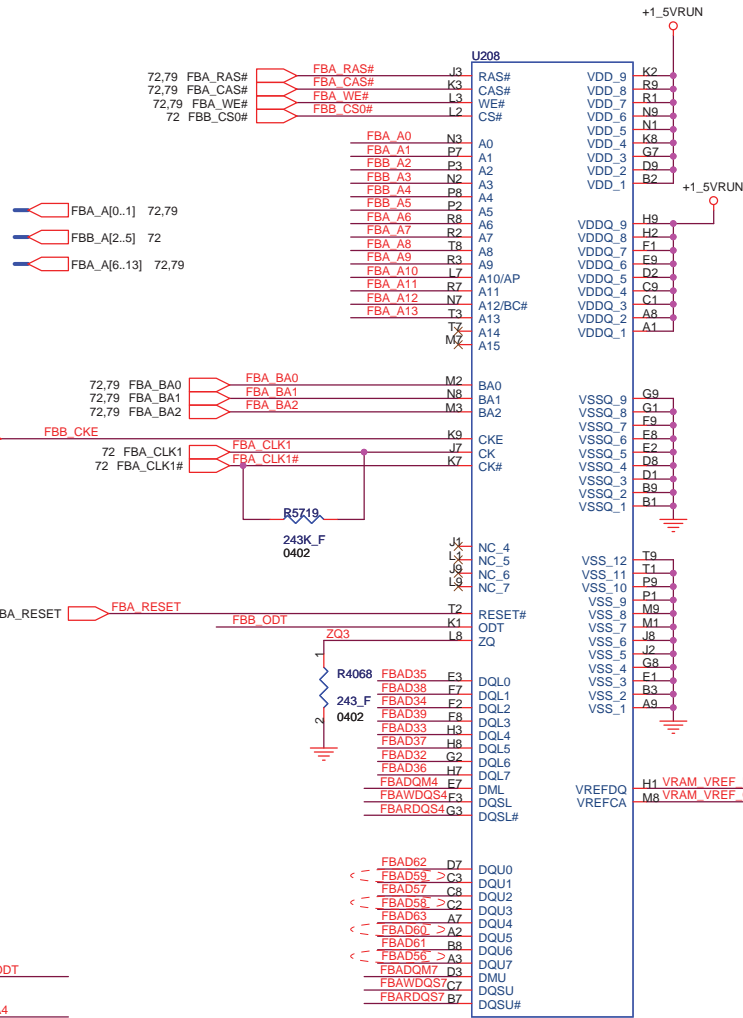


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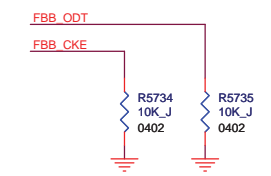
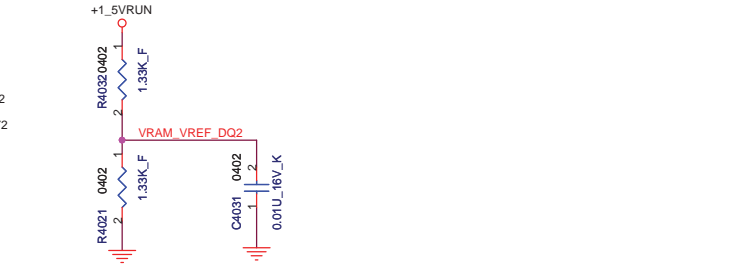
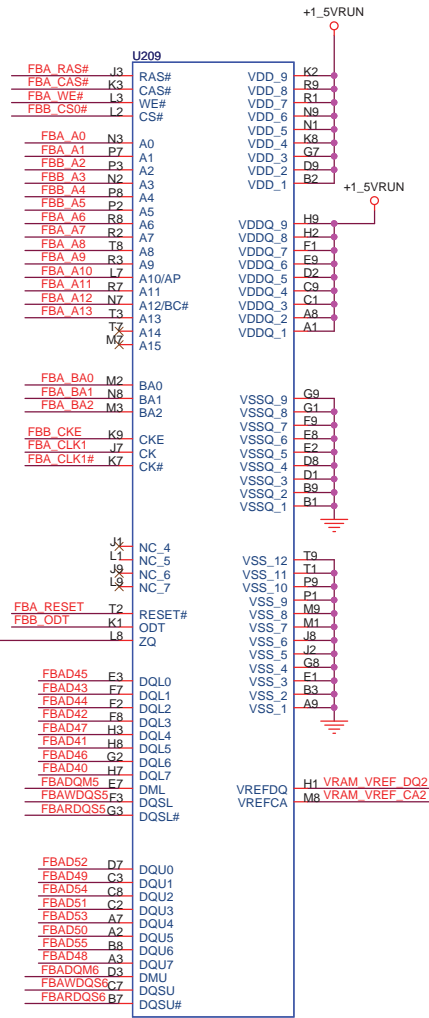
Title: **VRAM(DDR)# 1/4**

Size: Document Number **M931 (MBX-215)** Rev **SA**

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CMD0	0..30	32..63
CMD1	RAS#	RAS#
CMD2	A5	BA1
CMD3	BA1	BA2
CMD4	BA1	A2
CMD5	BA0	A4
CMD6	BA0	A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	BA2
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

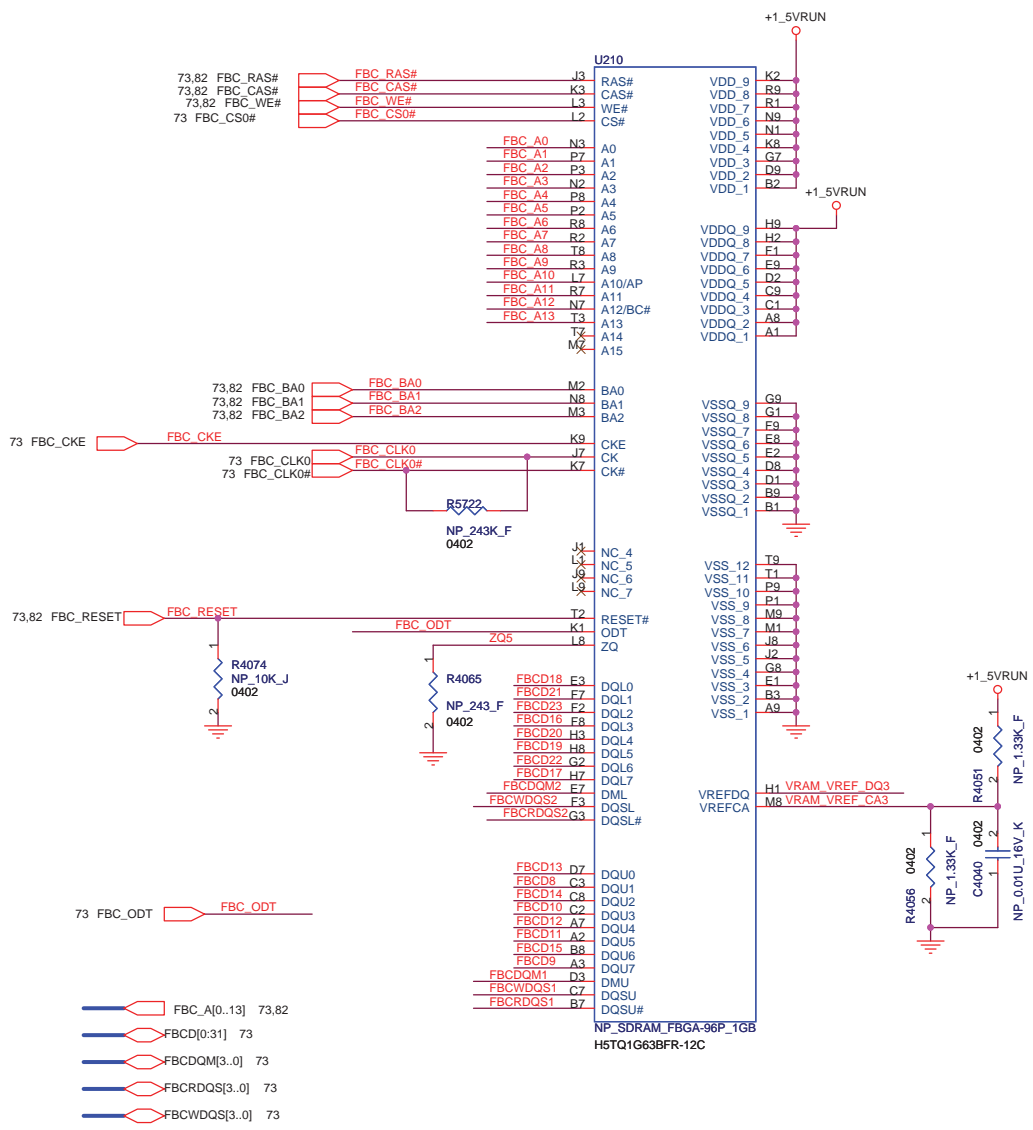


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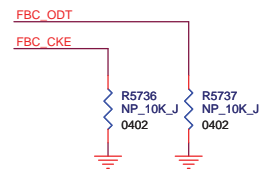
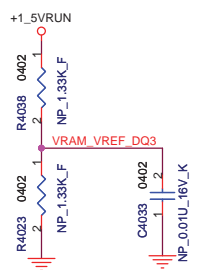
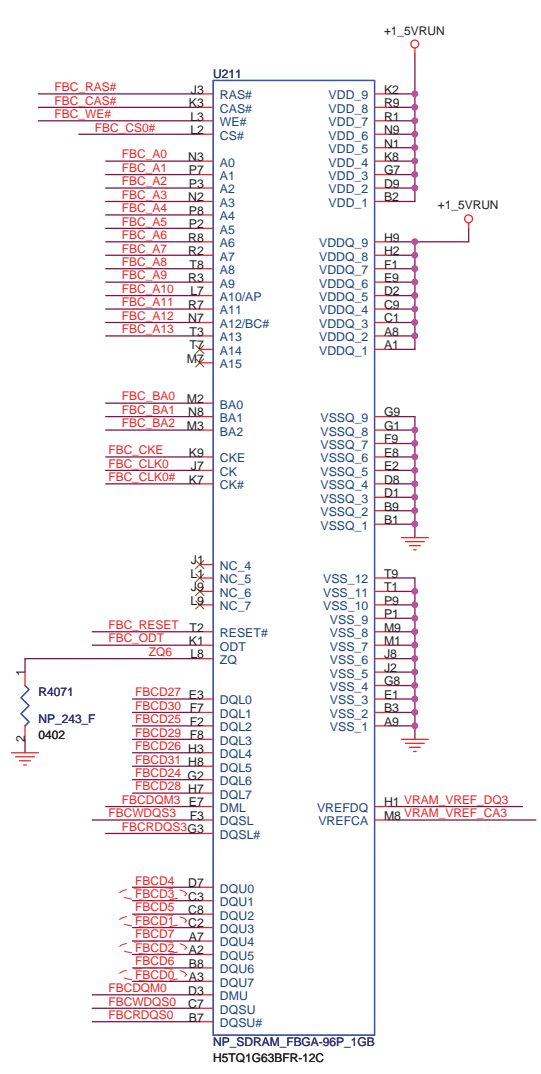
File: **VRAM(DDR)# 2/4**

Size: A3 Document Number: **M931 (MBX-215)** Rev: **SA**

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	0..30	32..63
CMD0	A4	RAS#
CMD1	RAS#	RAS#
CMD2	A5	CS#
CMD3	BA1	BA1
CMD4	A2	A2
CMD5	A4	A4
CMD6	A3	A3
CMD7	CKE	CKE
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	ODT	ODT
CMD29	CS0#	CS0#
CMD30	ODT	ODT

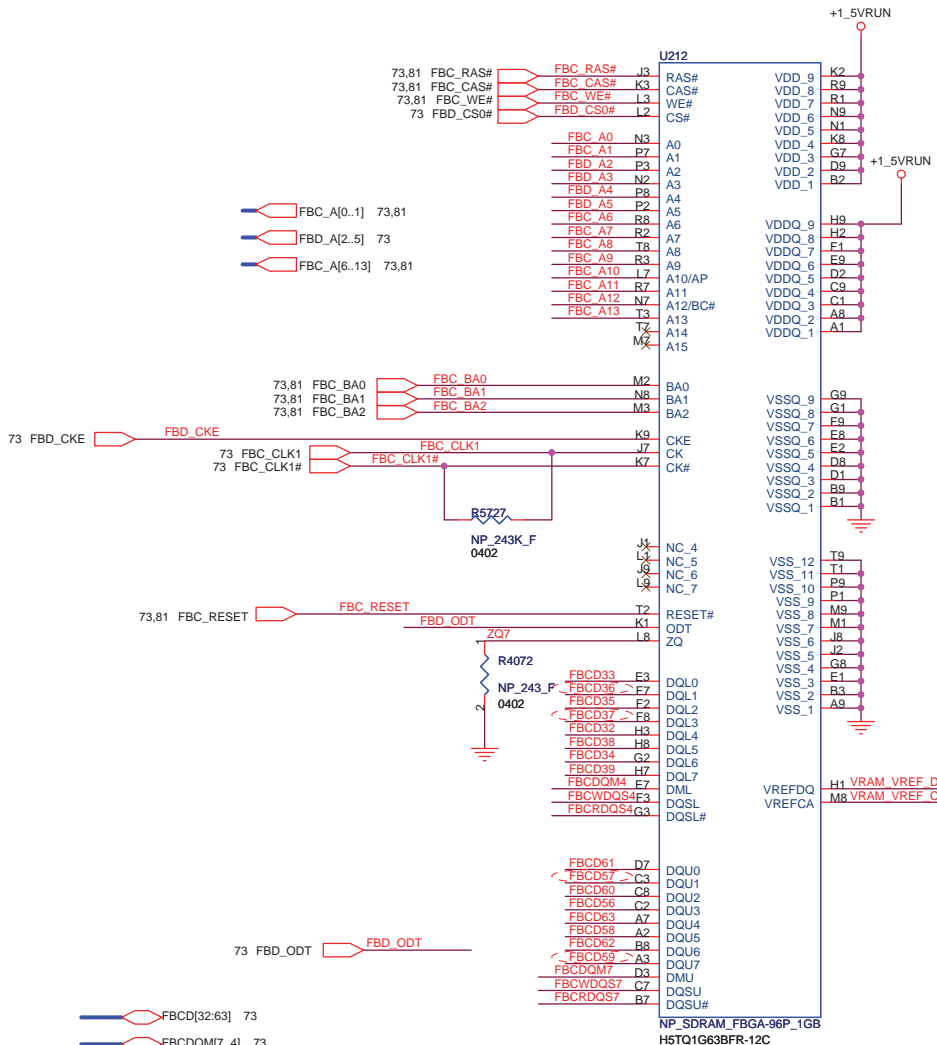


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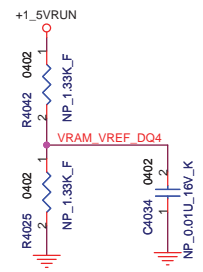
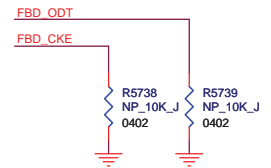
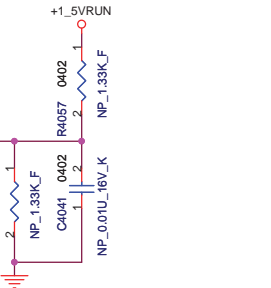
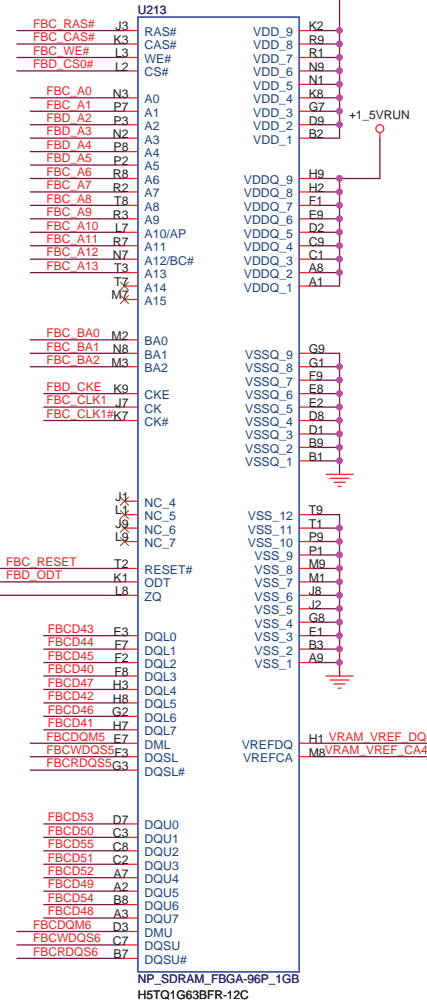
Title: **VRAM(DDR)# 3/4**

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	0..30	32..63
CMD0	A4	RAS#
CMD1	RAS#	RAS#
CMD2	A5	BA1
CMD3	BA1	BA1
CMD4	A2	A2
CMD5	A4	A4
CMD6	A3	A3
CMD7	A7	CKE
CMD8	A6	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	ODT	ODT
CMD29	CS0#	CS0#
CMD30	ODT	ODT



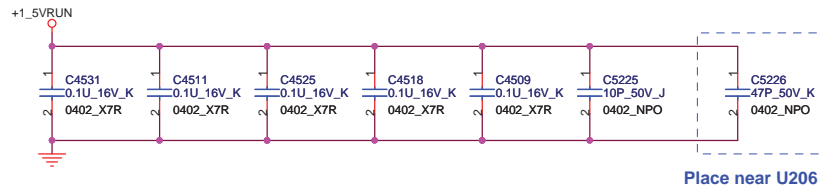
FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: **VRAM(DDR)# 4/4**

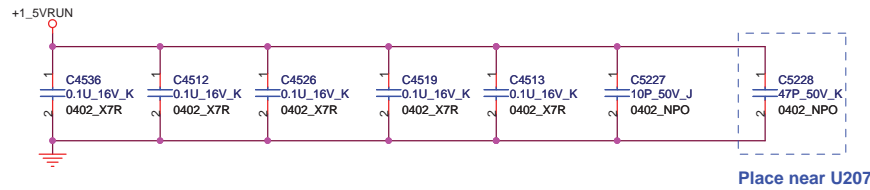
Size: Document Number **M931 (MBX-215)** Rev **SA**

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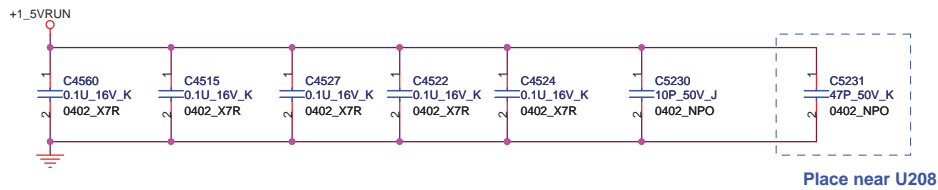
Place around the VRAM U206



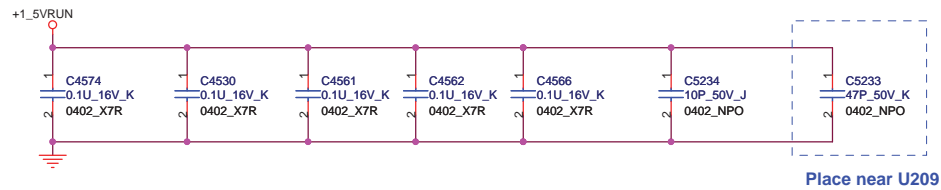
Place around the VRAM U207



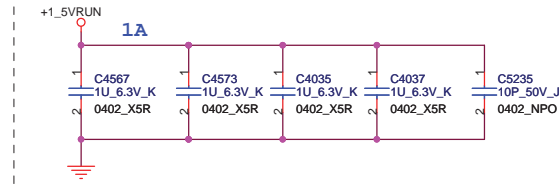
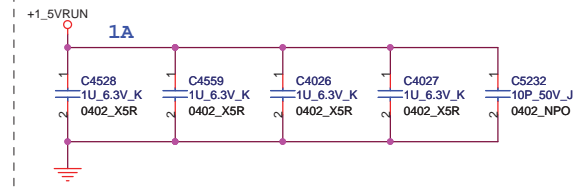
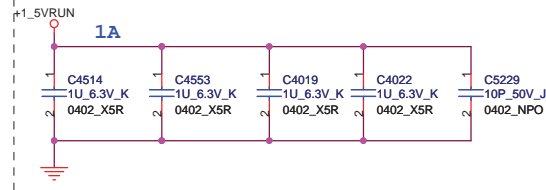
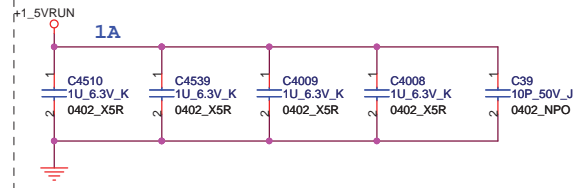
Place around the VRAM U208



Place around the VRAM U209



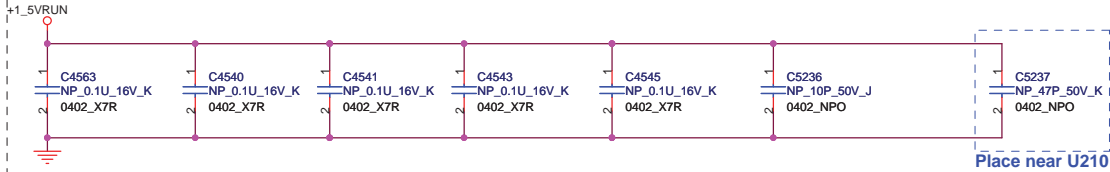
PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.



PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

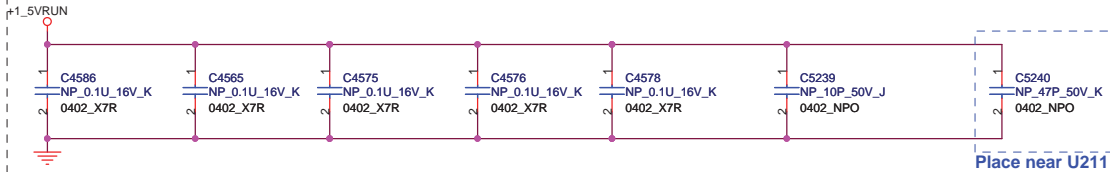
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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Place around the VRAM U210



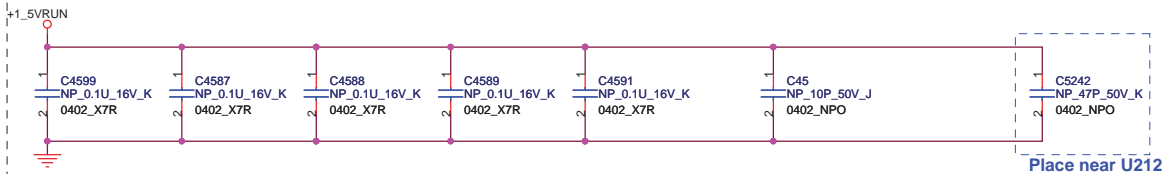
Place near U210

Place around the VRAM U211



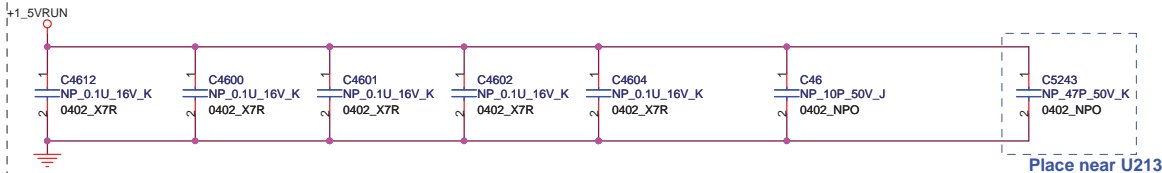
Place near U211

Place around the VRAM U212



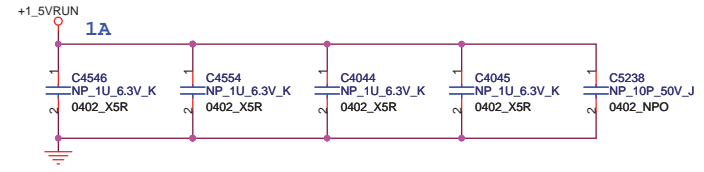
Place near U212

Place around the VRAM U213

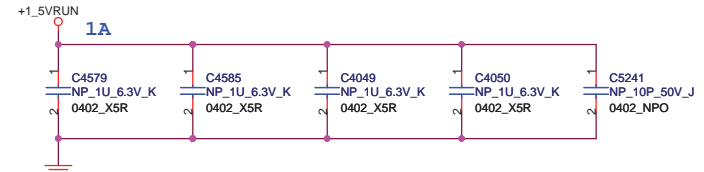


Place near U213

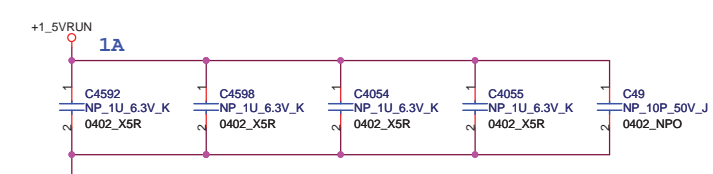
PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.



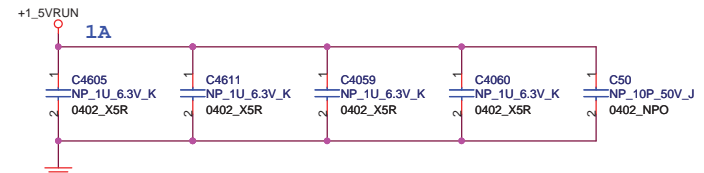
1A



1A



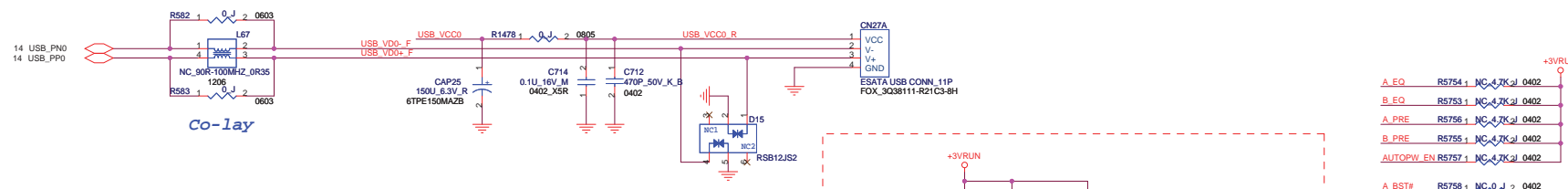
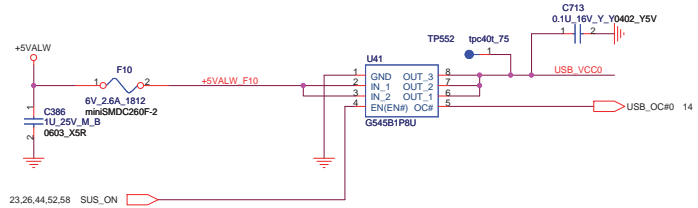
1A



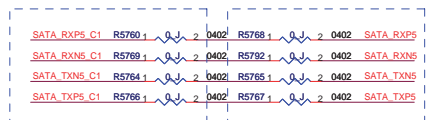
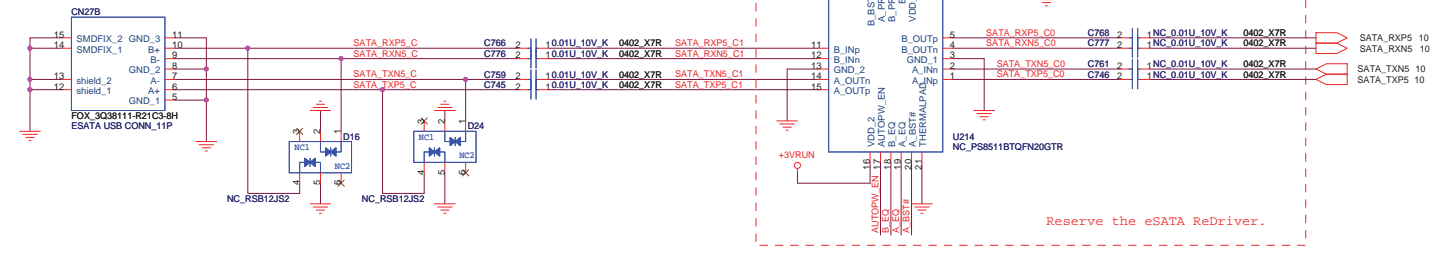
1A

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

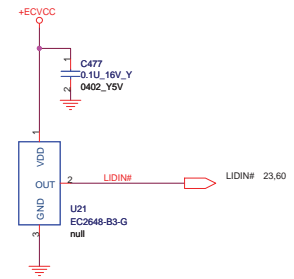
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VRAM(N11P BYPASS) 2/2	
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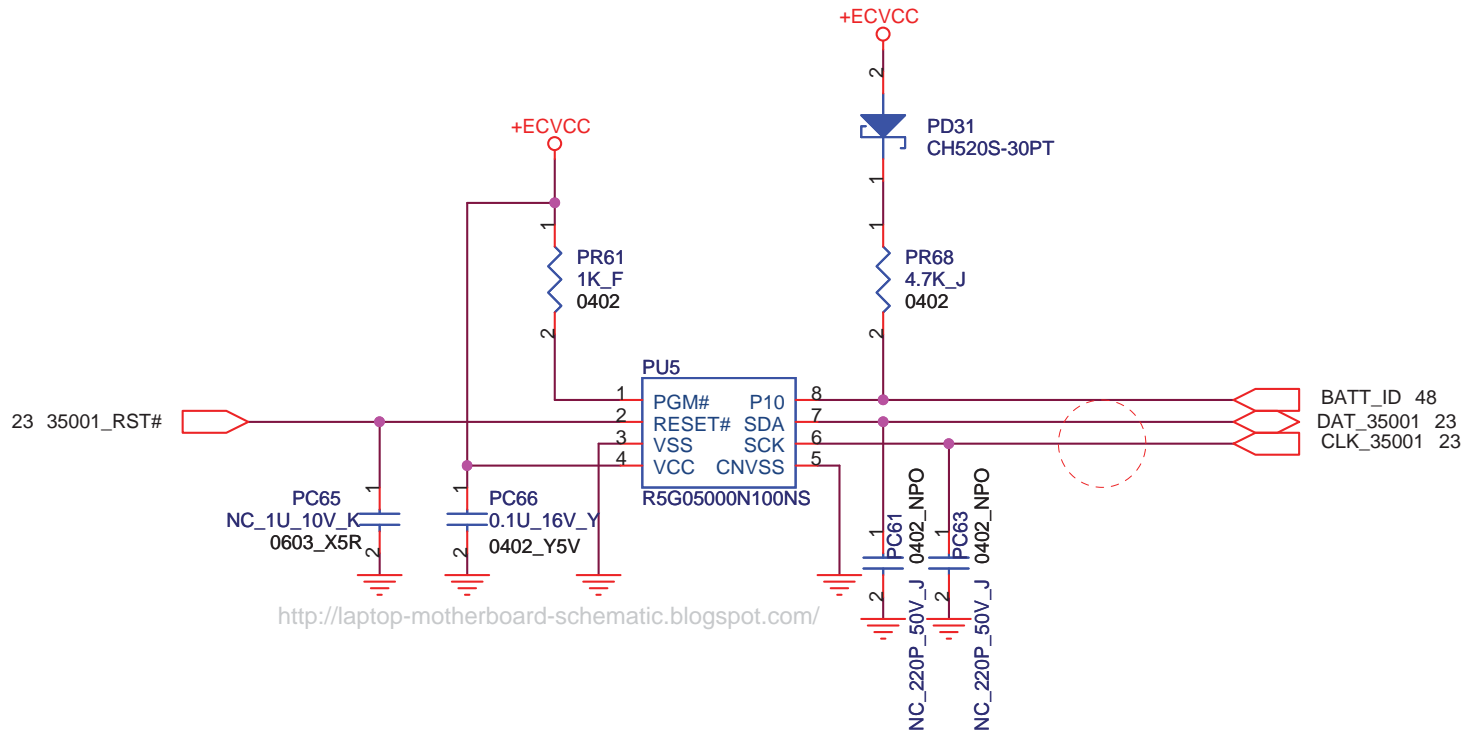
USB/eSATA Combo



Close to U124 ,Pin11 ,12 ,14 ,15 Close to U124 and C768 ,C777 ,C761 ,C746 Pin2

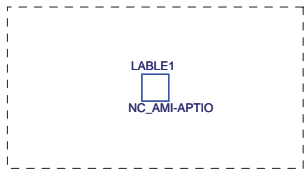


LID Switch

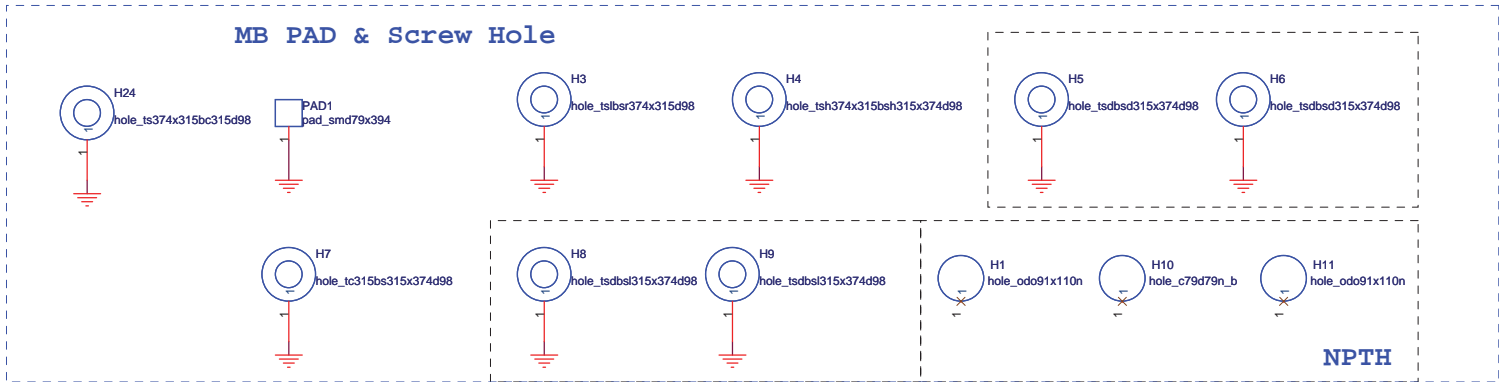


FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Identify IC			
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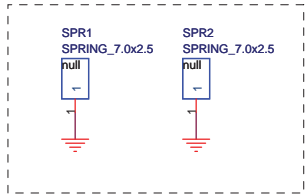
MB PAD & Screw Hole



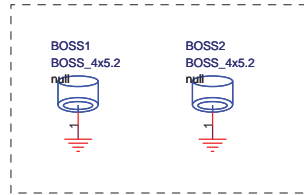
AMI Label (For MP Only)



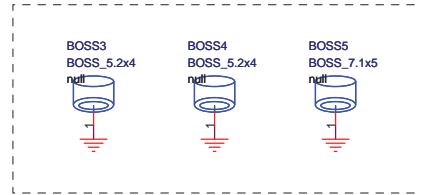
NPTH



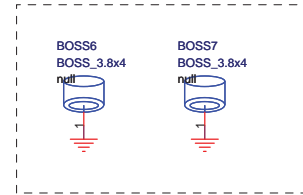
EMI SPRING



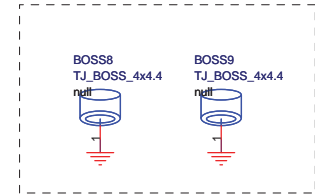
WLAN Module



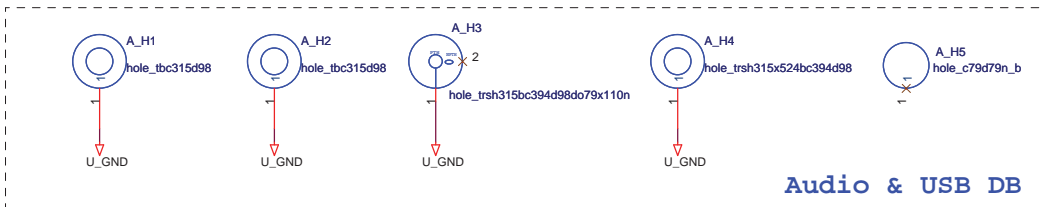
Thermal Modul



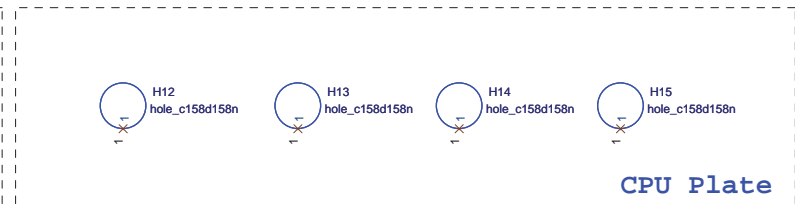
Bluetooth Bracket



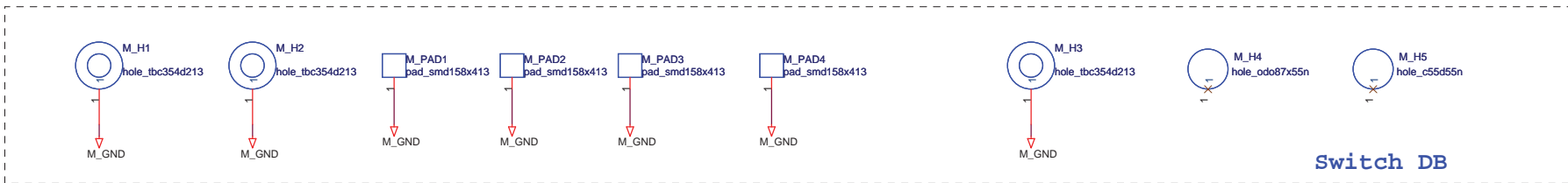
T-jet (MACH)



Audio & USB DB

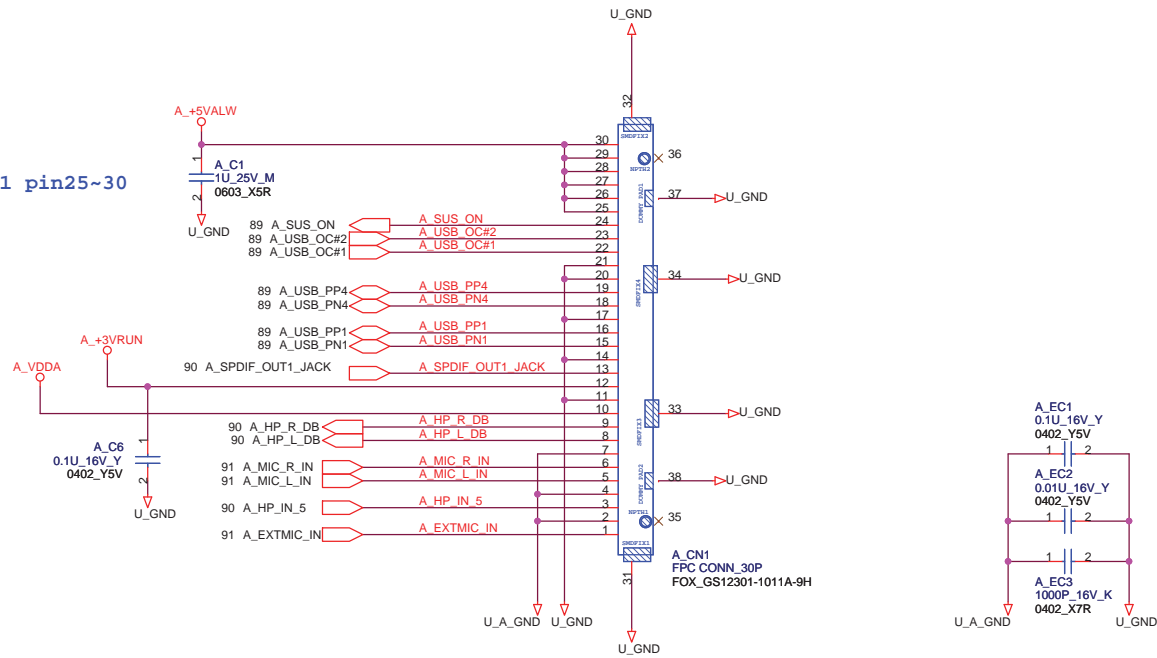


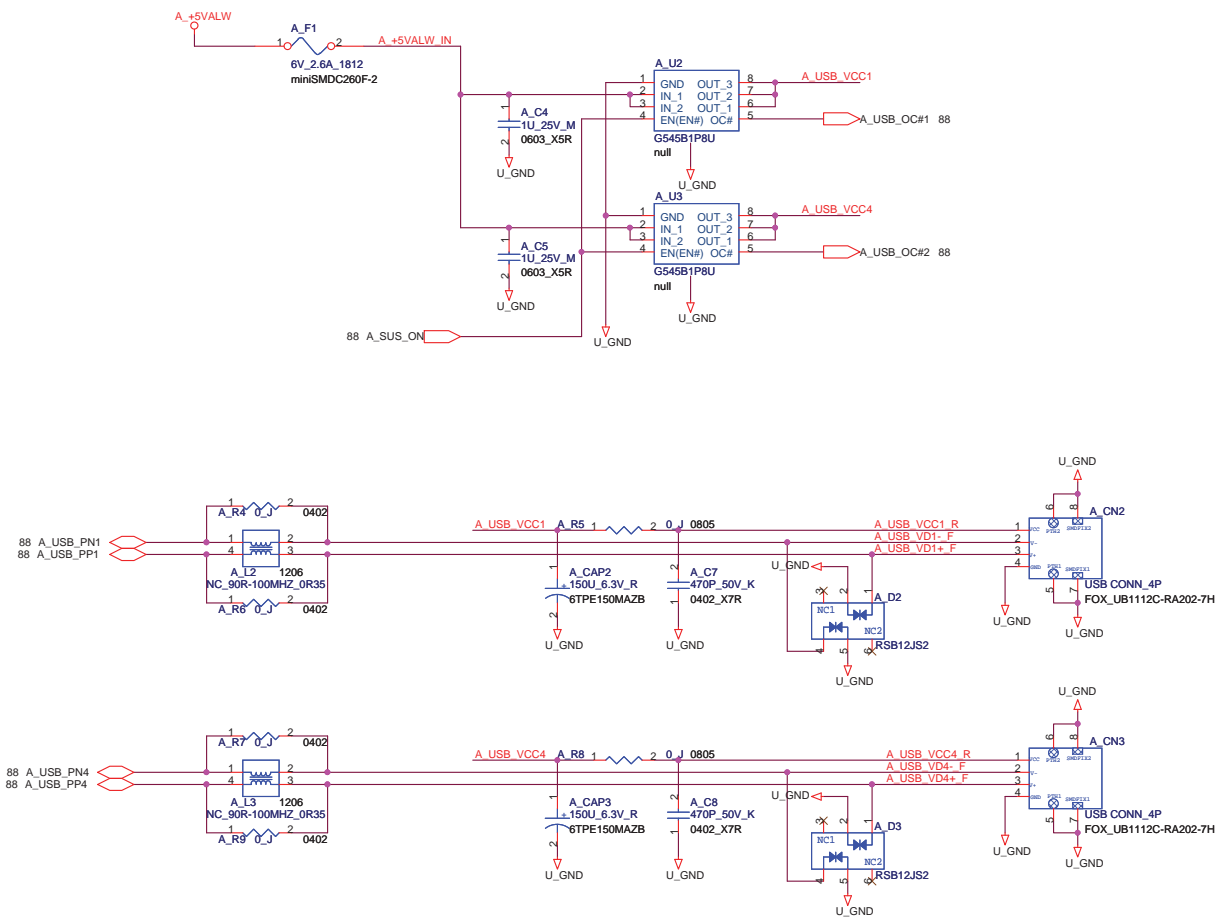
CPU Plate

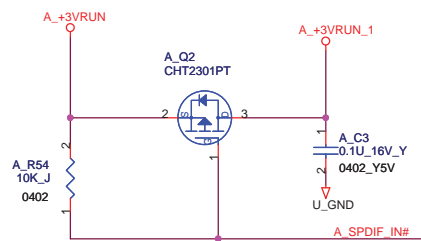
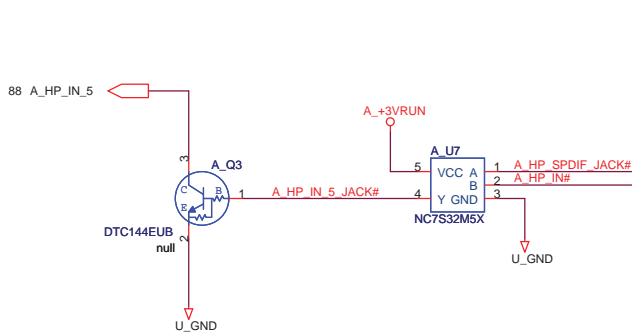
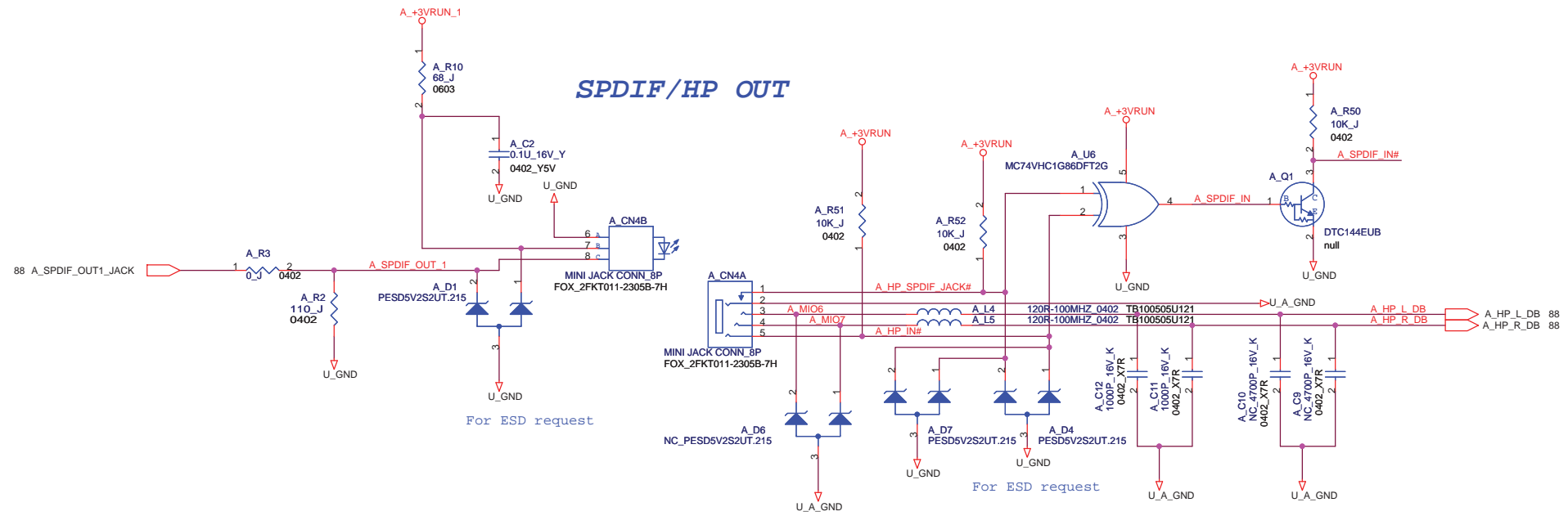


Switch DB

Place A_C1 close to A_CN1 pin25-30

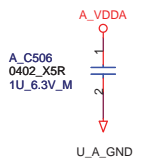
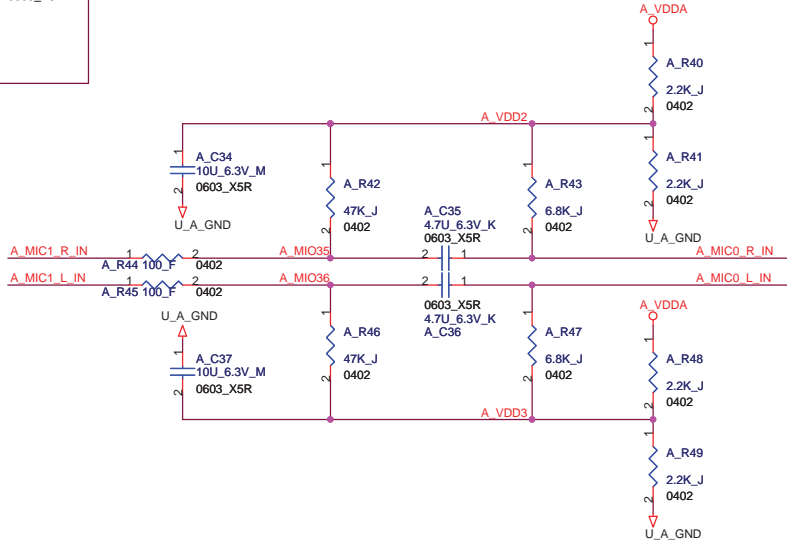
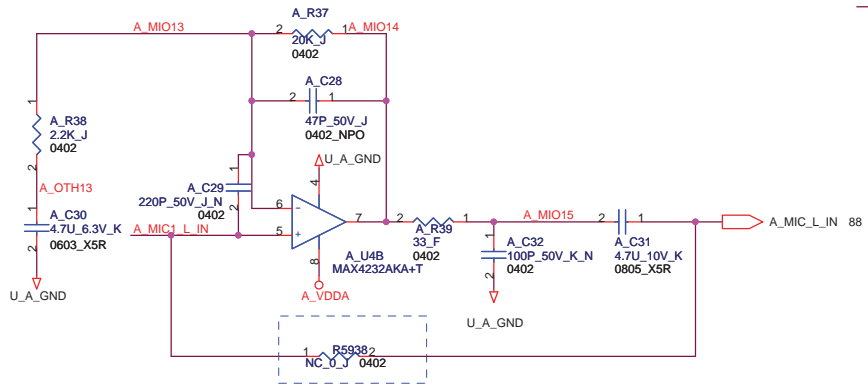
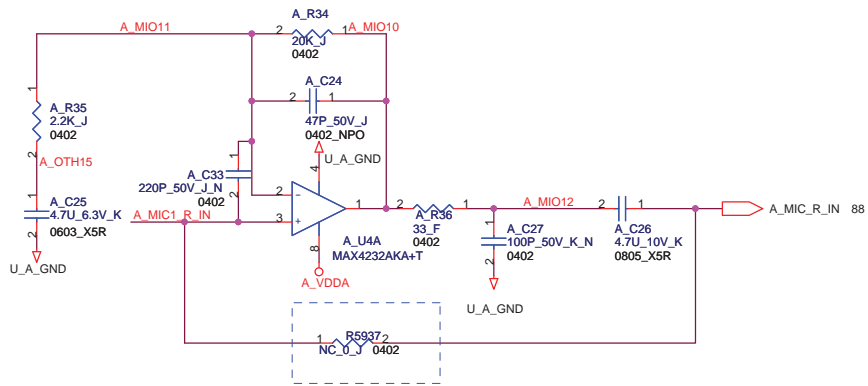




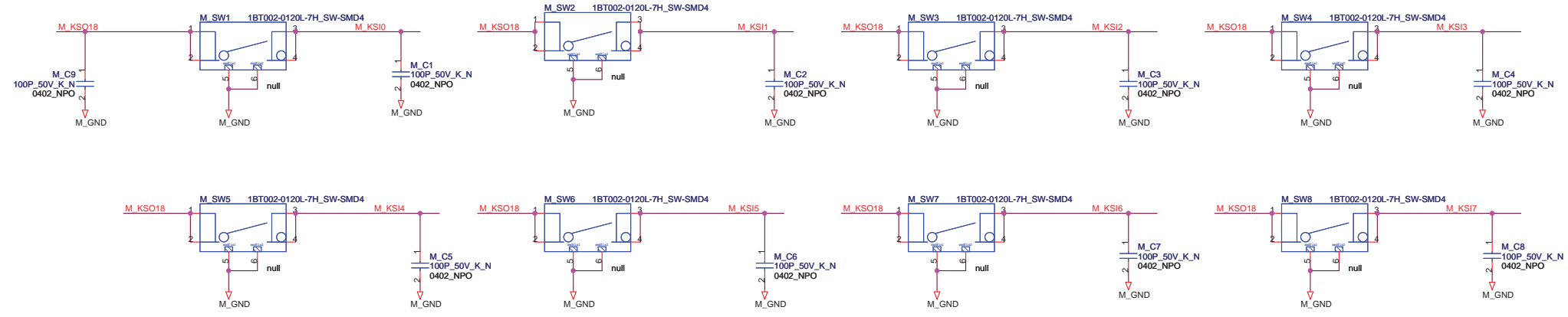
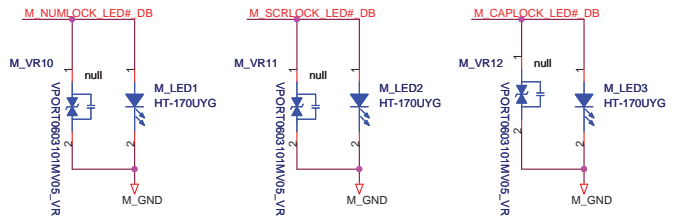
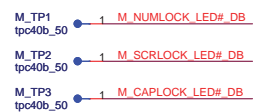
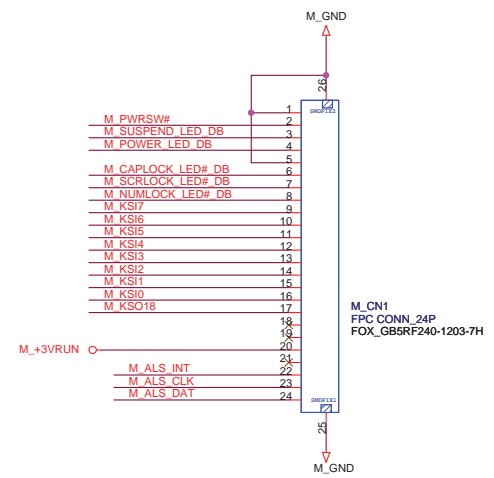
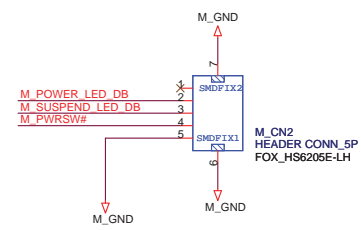
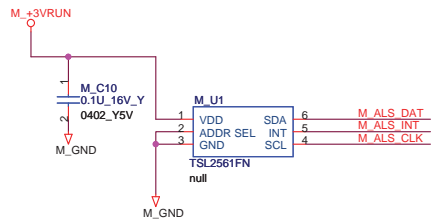


LED status

	Pin 1	Pin 5	LED A_SPDIF_IN#	A_HP_IN_5
HP	0	0	1 off	1
SPDIF	0	1	0 on	0
No plug	1	1	1 off	0



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Ext MIC Jack			
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(2009/11/27) M930-MP ECN Changed

- P.48 {DCIN} PR11 Change to SMD,RES,11.8K,1/16W,1%,0402
- P.48 {DCIN} PR12 Change to SMD,RES,10K,1/16W,1%,0402
- P.48 {DCIN} PR220 Change to SMD,RES,10.2K,1/16W,1%,0402
- P.57 {VGA Power} PR566 Change to SMD,RES,88.7K,1/16W,1%,0402
- P.51 {VTT Power} PR26 Change to SMD,RES,2.2ohm,1/10W,5%,0603
- P.51 {VTT Power} PR152 Change to SMD,RES,4.7ohm,1/10W,5%,0603
- P.51 {VTT Power} PC130 Change to SMD,MLCC,X7R,680pF,50V,10%,0603(0.8mm)
- P.12 {PCH} Delete D28, D29
- P.92 {DB} Delete M_VR1,M_VR2,M_VR3,M_VR4,M_VR5,M_VR6,M_VR7,M_VR8,M_VR9
- P.92 {DB} Add M_VR10,M_VR11, M_VR12
- P.23 {EC} Add C487 ,SMD,MLCC,X7R,1000pF,16V,10%,0402
- P.27 {WLAN} SW4 Change to ALPS,S55811101,Switch,SMD-7,Slide SW
- P.64 {CODEC} Change U215 vendor number from ALC275SQ-GR-A5 to ALC275SQ-GR

(2009/12/02)

- P.2 {Block Diagram} Revised Model Name and Feature
- P.4 {CPU} Short RP80
- P.7 {CPU} Short R1561
- P.9 {CPU} Short R1586, R1587
- P.11 {PCH} Short RP69 ,RP71 ,RP67 ,RP70 ,RP78 ,RP68 ,RP89
- P.12 {PCH} Short R927
- P.19 {CLK} Short RP9 ,RP84 ,RP85 ,RP79
- P.23 {EC} Delete RP23
- P.26 {ExpressCard} Short R343, R337 ,Delete L40
- P.27 {WLAN} Short R22
- P.36 {Camera} Short R376 ,R377 ,Delete L46
- P.37 {Felica} Short R192 ,R193 ,Delete L25
- P.39 {BT} Change R7 to 100ohm as RF team Request.
- P.39 {BT} Delete U1 ,R6 ,C6 ,U12
- P.41 {KB} Short R695
- P.43 {TP} Short R533 ,Delete R530
- P.46 {Thermal} Delete D20 ,C547 ,C534 ,U26 ,R946 ,R61
- P.46 {Thermal} Delete U5 ,R65 ,C42 ,R54 ,R53 ,R60
- P.62 {HDMI} Delete L57 ,L60 ,L74 ,L76 ,Short R495 ,R483 ,R487 ,R492 ,R489 ,R498 ,R499 ,R494
- P.64 {Audio} Short R5767.
- P.85 {eSATA} Reserved C768 ,C777 ,C761 ,C746 ,U214
- P.85 {eSATA} Delete L62 ,L66 ,Short R589 ,R588 ,R592 ,R591
- P.86 {BAT ID} Short PR125

(2009/12/18)

- P.57 {VGA Power} Change PR182 to PWRCNTL_0 Net.
- P.57 {VGA Power} Change PR180 to PWRCNTL_1 Net.
- P.11 {PCH} U69 P/N :12-1BEXPEA-0004 (INTEL,BD82PM55 SLH23,BGA-1071,Intel Platform Controller Hub)
- P.35 {SD} Reserve the R1590 for SD Slot (CN29) Damppling.
- P.52 {0.75VPower} Change PC143 to 1C-2B20104-K300 (0.1uF/X7R/10%)

(2009/12/23)

- P.76 {VGA} Reserve the TP245 and TP246
- P.52 {DDR3 Power} Reserve the PR150 /PR157 Path

(2009/12/29)

- P.51 {VTTV Power} Reserve the CAP32 for Power Noise Reduce
- P.52 {1.5V Power} Reserve the CAP33 for Power Noise Reduce
- P.57 {VGA Power} Reserve the CAP34 for Power Noise Reduce

(2010/01/06)

- P.34 {SD} Revise R817 pull-up connection from +3VRUN to VCC_SD