Schematics Page Index (Title / Revision / Change Date)

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09	ARD&CFD (RESERVED)	SB		51	VTT&PCH Power(+1_1/1_05V)	SB
10	PCH (HDA,JTAG,SAT)	SB		52	DDR3 Power(+1_5V/+0_75V)	SB
11	PCH (PCI-E,SMBUS,CLK)	SB		53	VRAM Power(+1_8V)	SB
12	PCH (DMI,FDI,GPIO)	SB		54	CPU Power_VHCORE	SB
13	PCH (LVDS,DDI)	SB		55	CPU Power_VID	SB
14	PCH (PCI,USB,NVRAM)	SB		56	VGFX Power_GFXCORE	SB
15	PCH (GPIO,VSS_NCTF,RSVD)	SB		57	VGA Power(NV VDD)	SB
16	PCH (POWER) 1/2	SB		58	Others power plane	SB
17	PCH (POWER) 2/2	SB		59	OVP protection	SB
18	PCH (VSS)	SB		60	INV CONNECTOR	SB
19	CLOCK GEN	SB		61	LVDS	SB
20	DDRIII(SO-DIMM_0) 1/3	SB		62	HDMI	SB
21	DDRIII(SO-DIMM_1) 2/3	SB		63	CRT	SB
22	SO-DIMM_VREF 3/3	SB		64	Audio (CODEC)	SB
23	EC+KBC (NPCE783L)	SB		65	Audio (MUTE)	SB
24	SPI Flash ROM	SB		66	Audio (Power)	SB
25	Debug Port	SB		67	Audio (Speaker AMP)	SB
26	Express Card	SB		68	Audio (Speaker Connector)	SB
27	Mini-PCIE Card (WLAN)	SB		69	Mini-PCIE Card (Mach)	SB
28	TV-Tuner Connector	SB		70	VGA (PCI-E) 1/9	SB
29	LAN (88E8057) 1/2	SB		71	VGA (STRAP) 2/9	SB
30	LAN (Transformer) 2/2	SB		72	VGA (DDR) 3/9	SB
31	SATA HDD	SB		73	VGA (DDR) 4/9	SB
32	SATA CD-ROM	SB		74	VGA (CRT/eDP) 5/9	SB
33	Braidwood Connector	SB		75	VGA (LVDS/HDMI) 6/9	SB
34	PCIE (MS&iLINK) 1/2	SB		76	VGA (GPIO) 7/9	SB
35	PCIE (SD) 2/2	SB		77	VGA (XTAL) 8/9	SB
36	Camera Connector	SB		78	VGA (POWER/GND) 9/9	SB
37	Felica Connector	SB		79	VRAM (DDR3) 1/4	SB
38	eDP&LVDS Connector	SB		80	VRAM (DDR3) 2/4	SB
39	Bluetooth Connector	SB		81	VRAM (DDR3) 3/4	SB
40	Modem Connector	SB		82	VRAM (DDR3) 4/4	SB
41	KB Connector	SB		83	VRAM (BYPASS) 1/2	SB
42	Status LED	SB		84	VRAM (BYPASS) 2/2	SB

M930 BOM Control Table

VALUE Head	CFD+PM55 N11P 1GVRAM-H	CFD+PM55 N11P 1GVRAM-S	CFD+PM55 N11M 512MVRAM-H	CFD+PM55 N11M 512MVRAM-S	ARD+SSKU N11P 1GVRAM-H	ARD+SSKU N11P 1GVRAM-S	ARD+SSKU N11M 512MVRAM-H	ARD+SSKU N11M 512MVRAM-S
CF_	Stuff	Stuff	Stuff	Stuff	Dummy	Dummy	Dummy	Dummy
AR_	Dummy	Dummy	Dummy	Dummy	Stuff	Stuff	Stuff	Stuff
NV_	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff
NP_	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy
NM_	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff
NVH_	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy
NVS_	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff
NC_	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy

85	LID Switch/eSATA COMBO	SB
86	Identify IC	SB
87	HOLE & AMI LABEL	SB
88	USB & AUDIO Conn.	SB
89	USB Port	SB
90	HP Jack (S/PDIF)	SB
91	Ext MIC Jack	SB
92	Function SW & ALS	SB

P. Leader	Check by	Design by

Project Code & Schematics Subject: M930 Main Board

PCB P/N: (IRIS)
(Hannstar)

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

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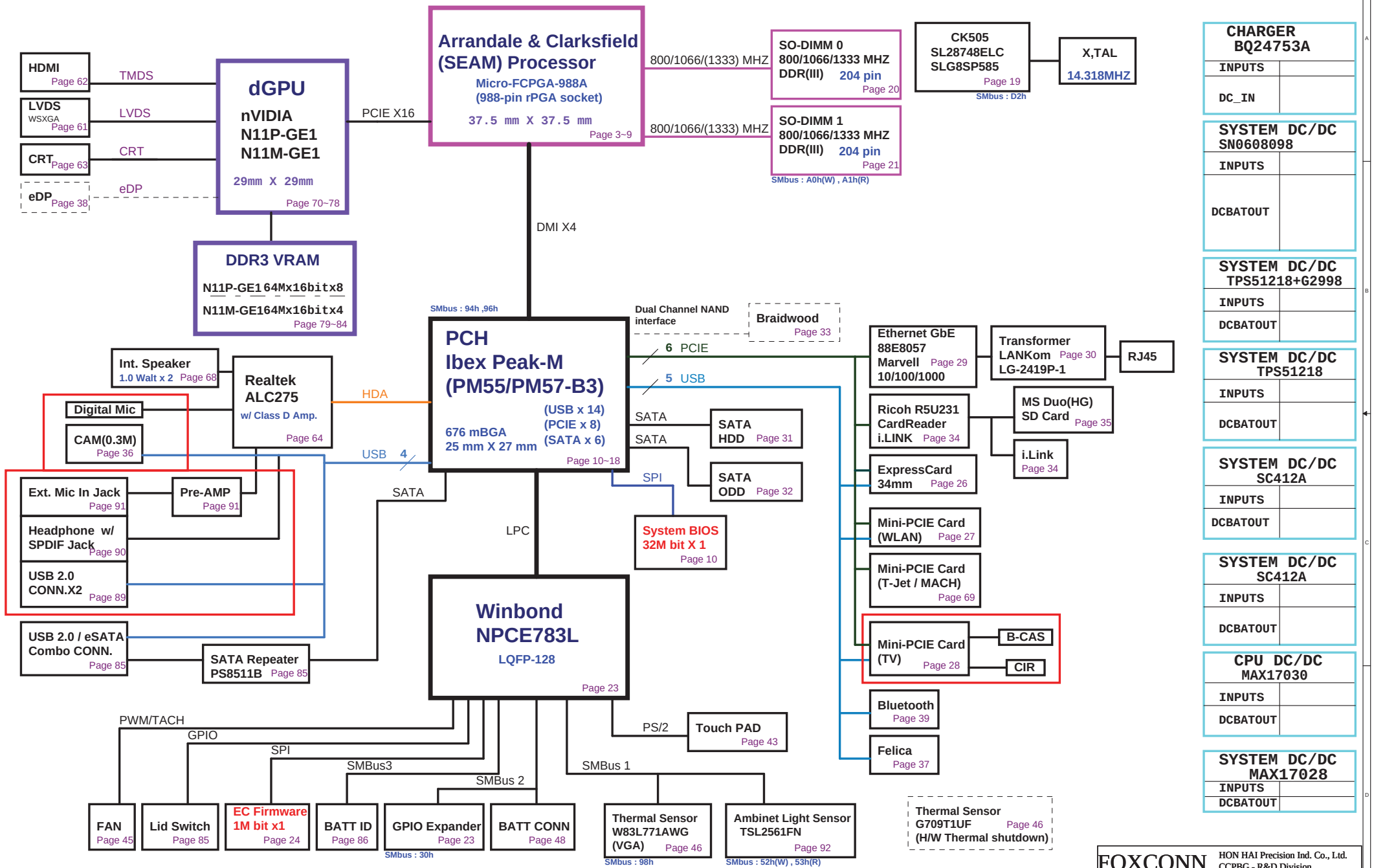
M930 (IRX-5100) Calpella Platform+ nVIDIA N11P/M Discrete Graphic



CHARGER BQ24753A	
INPUTS	
DC_IN	

SYSTEM DC/DC SN0608098	
INPUTS	
DCBATOUT	

SYSTEM DC/DC TPS51218+G2998	
INPUTS	
DCBATOUT	

SYSTEM DC/DC TPS51218	
INPUTS	
DCBATOUT	

SYSTEM DC/DC SC412A	
INPUTS	
DCBATOUT	

SYSTEM DC/DC SC412A	
INPUTS	
DCBATOUT	

CPU DC/DC MAX17030	
INPUTS	
DCBATOUT	

SYSTEM DC/DC MAX17028	
INPUTS	
DCBATOUT	

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Title: **Block Diagram**

Size: Custom | Document Number: **M930 (MBX-215)** | Rev: SB

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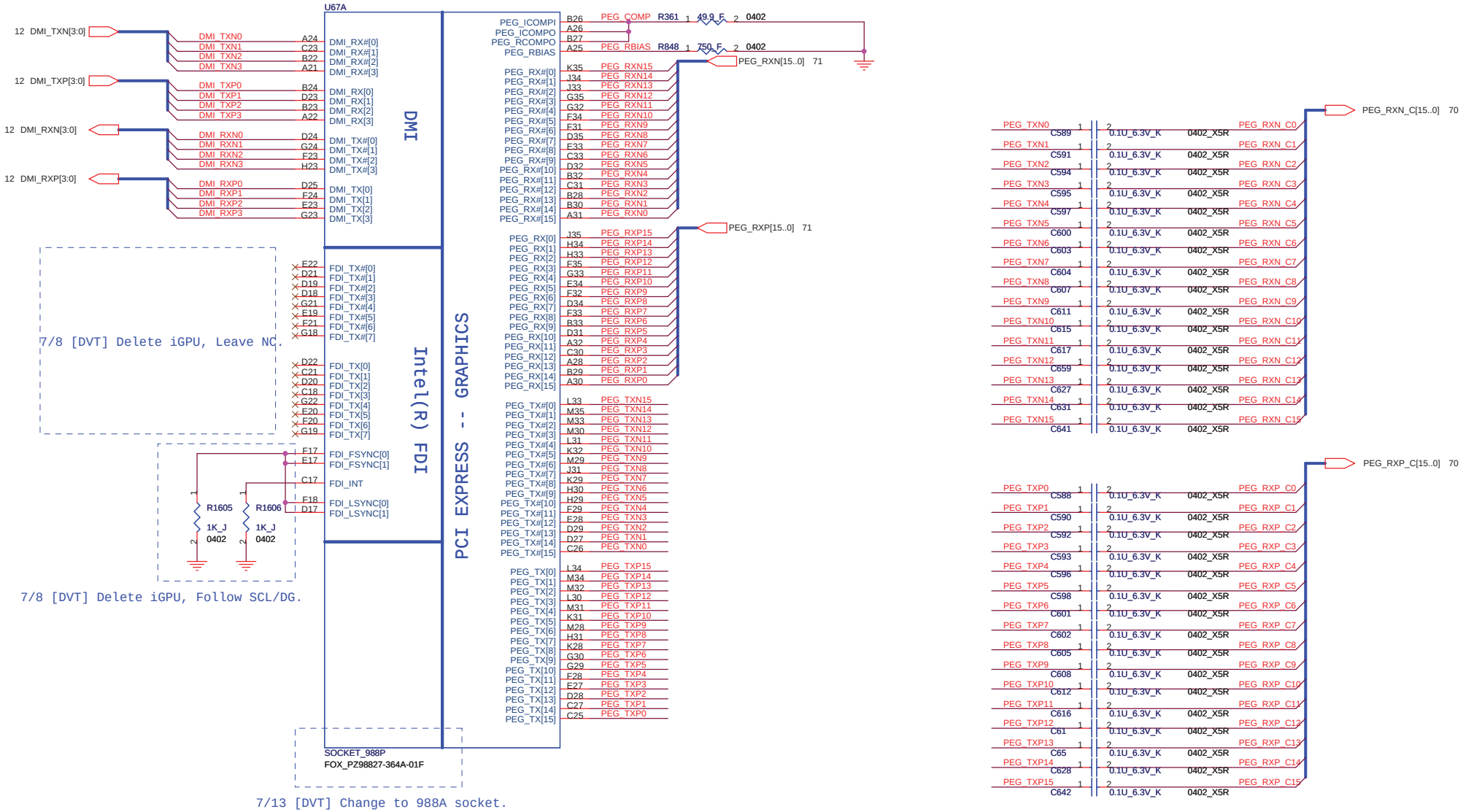

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Title	ARD&CFD (DMI,PEG,FDI)	
Size A3	Document Number M930 (MBX-215)	Rev SB
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Layout Note:
In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils (0.254-mm) wide trace for routing less than 500 mils (12.7 mm), or 20-mils (0.508-mm) wide trace for routing between 500 mils (12.7 mm) and 1000 mils(25.4 mm). Keep 20-mils (0.508-mm) spacing to any other signals in order to minimize crosstalk.

For Disable Auburndale Graphic
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics.

7/24 [DVT] Change to Array for C/D.

U67B

MISC THERMAL — CLOCKS — DDR3 MISC — PWR MANAGEMENT — JTAG & BPM

COMP3 AT23 · COMP2 AT24 · COMP1 G16 · COMP0 AT26 · SKTOCC# AH24 · CATERR# AK14 · PECI AT15 · PROCHOT# AN26 · THERMTRIP# AK15 · RESET_OBS# AP26 · PM_SYNC AL15 · VCCPWRGOOD_1 AN14 · VCCPWRGOOD_0 AN27 · SM_DRAMPWROK AK13 · VTTPWRGOOD AM15 · TAPPWRGOOD AM26 · RSTIN# AL14

SOCKET_988P
FOX_PZ98827-364A-01F

BCLK AUB_BCLK / BCLK# AUB_BCLK# · BCLK_ITP BCLK_ITP# · PEG_CLK CLK_EXP_P_R / CLK_EXP_N_R · DPLL_REF_SSCLK A18 / DPLL_REF_SSCLK# A17

RP81 0404_4P2R: CLK_PCH_CPU_CLK# 15 / CLK_PCH_CPU_CLK 15
RP82 0404_4P2R: CLK_CPU_BCLK 19 / CLK_CPU_BCLK# 19
RP80 0404_4P2R: CLK_EXP_P 11 / CLK_EXP_N 11

7/8 [DVT] Delete iGPU, Short to GND.

SM_DRAMRST# F6 DDR3_DRAMRST#_Q
SM_RCOMP[0] AL1 SM_RCOMP0 R854 100_F 0402
SM_RCOMP[1] AM1 SM_RCOMP1 R853 24.9_F 0402
SM_RCOMP[2] AN1 SM_RCOMP2 R855 130_F 0402
PM_EXT_TS#[0] AN15 PM_EXTTS#0 · PM_EXT_TS#[1] AP15 PM_EXTTS#1
PM_EXTTS#0 20,46 · PM_EXTTS#1 20,21

+1_1V_VTT: R932 10K_J 0402 · R933 10K_J 0402 · R1231 NC_12.4K_F 0402

PRDY# AT28 XDP_PRDY# TP75 20MIL · PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK · TMS AP28 XDP_TMS · TRST# AT27 XDP_TRST#
TDI AT29 XDP_TDI_R · TDO AR27 XDP_TDO_R · TDI_M AR29 XDP_TDI_M · TDO_M AP29 XDP_TDO_M
DBR# AN25 XDP_DBRESET#
+3VRUN: R1292 NC_51_J 0402

BPM#[0] AJ22 BPM#0 TP64 · BPM#[1] AK22 BPM#1 TP65 · BPM#[2] AK24 BPM#2 TP66 · BPM#[3] AJ24 BPM#3 TP67 · BPM#[4] AJ25 BPM#4 TP68 · BPM#[5] AH22 BPM#5 TP69 · BPM#[6] AK23 BPM#6 TP70 · BPM#[7] AH23 BPM#7 TP71
(20MIL)

R849–R852 20_F 0402 COMP3 / COMP2 / 49.9_F COMP1 / COMP0
20MIL TP60 SKTOCC#
H_CATERR# AK14
15 H_PECI AT15
54 PROCHOT# AN26
15,23 PM_THRMTRIP# AK15
H_CPURST#_R AP26
12 H_PM_SYNC AL15
15 H_CPUPWRGD AN27
12 PM_DRAM_PWRGD AK13
VTTPWRGOOD AM15
20MIL TP94 TAPPWRGOOD AM26
14,23,25,26 BUF_PLT_RST# R925 1.5K_F 0402 → BUF_PLT_RST#_R AL14
R926 750_F 0402

7/13 [DVT] Change to 988A socket.

+1_5VSUS
R1456 NC_0_J 0402 · Q73 2N7002EPT · R5925 1K_J 0402
DDR3_DRAMRST# Q → DDR3_DRAMRST# 20,21
R5926 100K_J 0402 · DRAMRST_CNTRL
R1455 NC_0_J 0402 → DRAMRST_CNTRL_EC 23
R1454 0_J 0402 → DRAMRST_CNTRL_PCH 15
C6079 470P_50V_K 0402_X7R
9 DRAMRST_CNTRL

(Default : PCH GPIO Control)

7/24 [DVT] INTEL S3 Power Reduction Solution.

+3VRUN: R262 4.7K_J 0402 · A0205 · Q14B 2N7002DW null
+1_1V_VTT: R258 68_J 0402 · PROCHOT# · Q14A 2N7002DW null
23 OVT_EC#

+1_1V_VTT
XDP_TDO_R R1290 · XDP_TMS R1258 · XDP_TDI_R R1259 · XDP_PREQ# R1260 · XDP_TCLK R1261 · XDP_TRST# R1262
51_J 0402

XDP_TDO_M → R969 0_J 0402 → XDP_TDI_M

JTAG Mapping -Scan Chain (Default)

7/24 [DVT] Change R1261 to Stuff as MOR request.

+1_1V_VTT: R861 49.9_F 0402 · R936 NC_68_J 0402
H_CATERR#
H_CPURST#_R

+3VALW: R21 10K_J 0402 · C68 0.1U_6.3V_K 0402_X5R
U7 74AHC1G08GW
RUN_PWRGD
PM_DRAM_PWRGD_R → R928 1.5K_F 0402 → PM_DRAM_PWRGD
+1_5VSUS_CPU: R5931 NC_1.1K_F 0402 · R928 750_F 0402

7/24 [DVT] INTEL S3 Power Reduction Solution.

+3VRUN: R14 10K_J 0402 · C13 0.1U_6.3V_K 0402_X5R
U2 74AHC1G08GW
12,23,51,52,57 RUN_PWRGD
VTTPW_R R1572 2K_F 0402 → VTTPWRGOOD
R1573 1K_F 0402

VTT_1.1 VR power good signal to processor.
Signal voltage level is 1.1 V.

FOXCONN — HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title	ARD&CFD (CLK,MISC,JTAG)	
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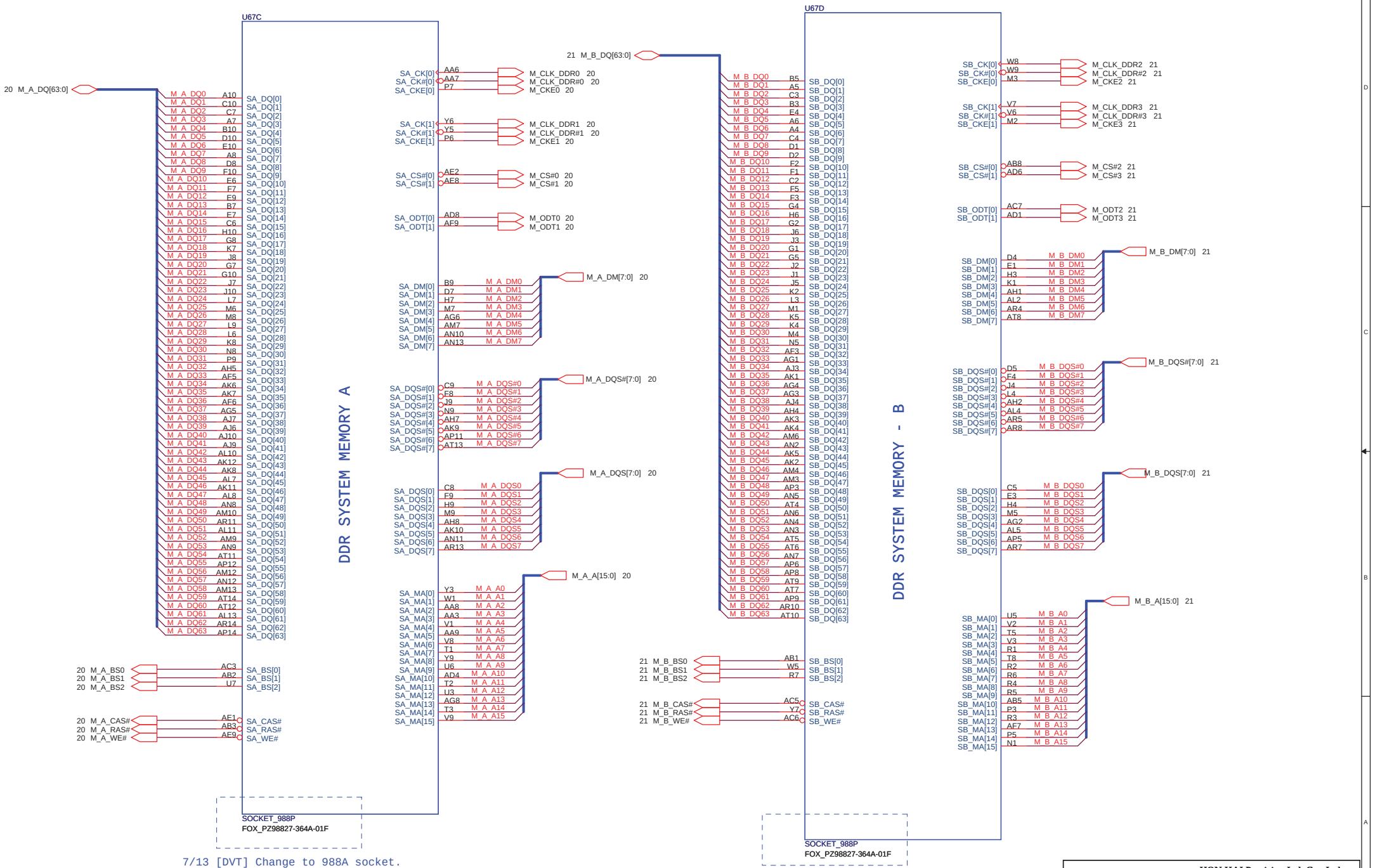
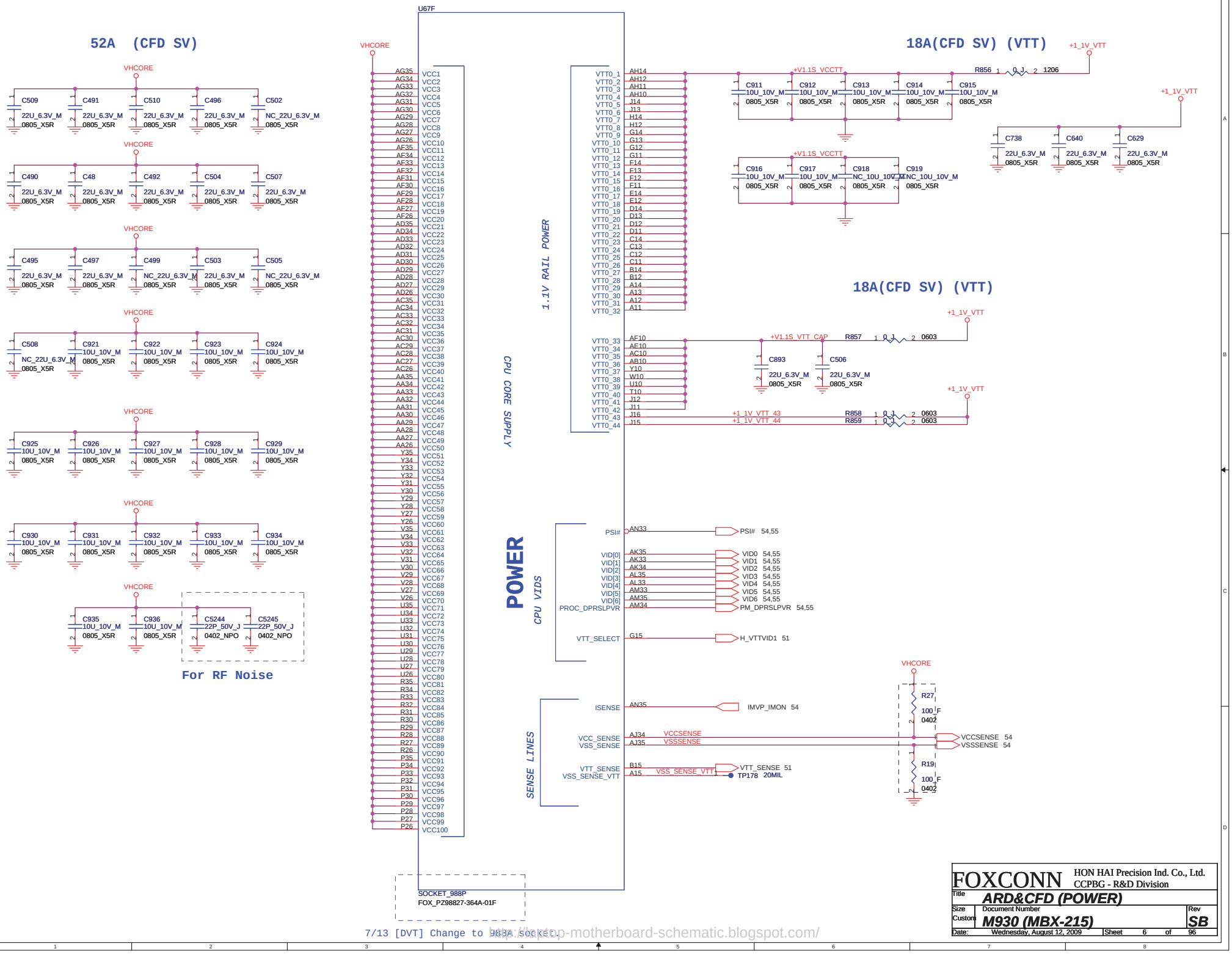


7/13 [DVT] Change to 988A socket.

7/13 [DVT] Change to 988A socket.

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ARD&CFD (DDR3)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 5 of 96	



7/13 [DVT] Change to 988A socket.

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ARD&CFD (POWER)	
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For Disable Auburndale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as no connect.
For Disable Auburndale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

For Disable Auburndale Graphic
VAXG should be connected to GND when disable iGPU.

7/8 [DVT] Delete iGPU, Short to GND.

7/8 [DVT] Delete iGPU,
Leave to NC.

8/12 [DVT] INTEL White Paper0.9 Check List Request of Q55 6A

8/12 [DVT] INTEL S3 White Paper0.9 Update.

7/24 [DVT] INTEL S3 Power Reduction Solution.

U67G

GRAPHICS POWER

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

FDI

PEG & DMI

1.1V

1.8V

18A(CFD SV) (VTT)

18A(CFD SV) (VTT)

6A

600mA

SOCKET_988P
FOX_PZ98827-364A-01F

7/13 [DVT] Change to 988A socket.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	ARD&CFD (GRAPHICS POWER)
Size: Custom	Document Number: M930 (MBX-215)
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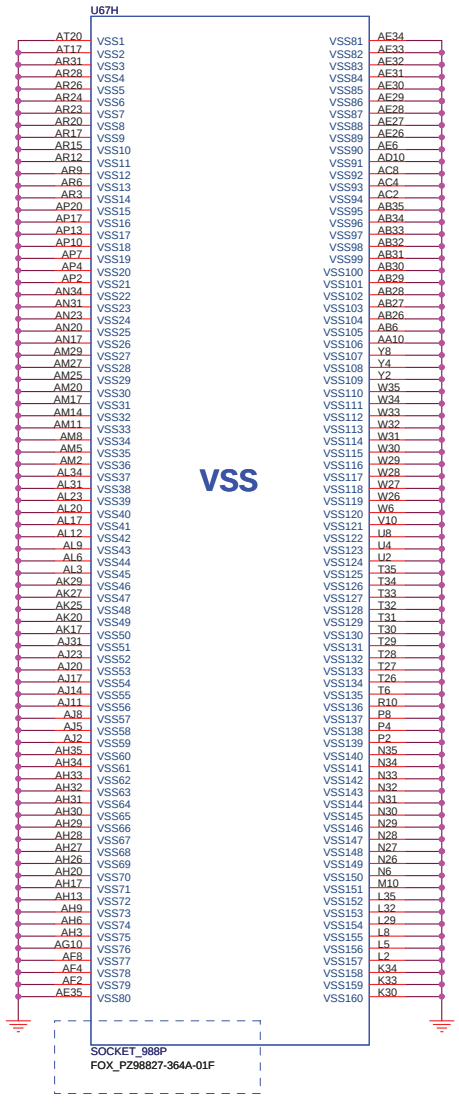
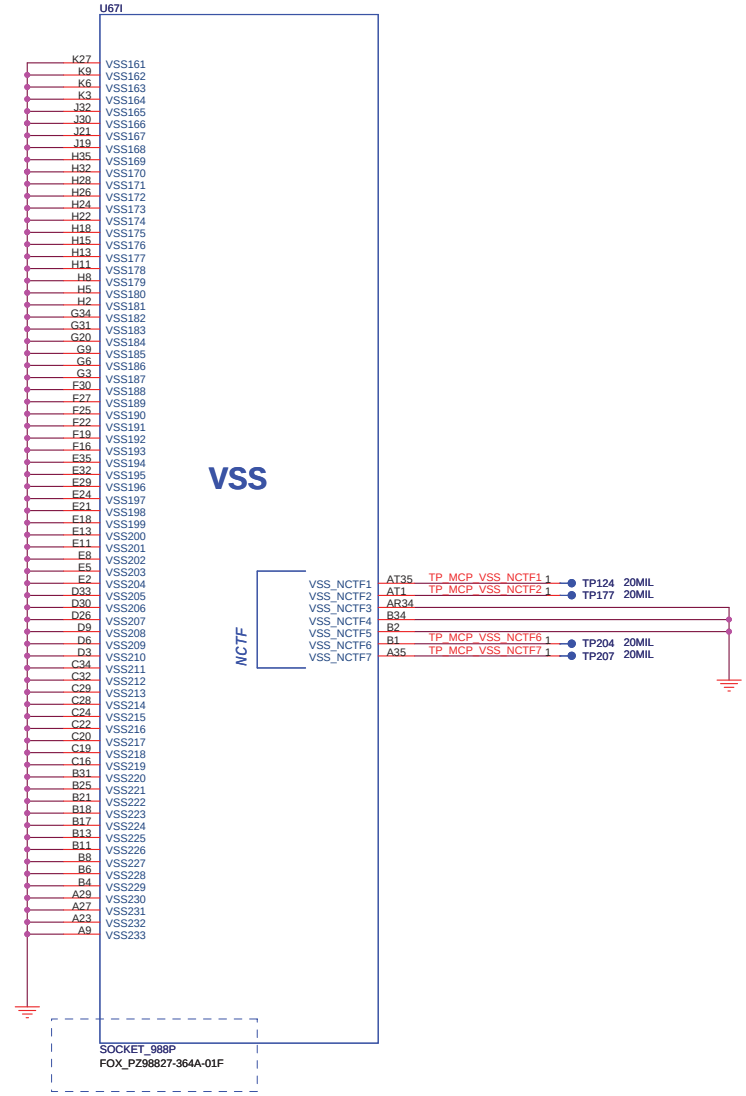


7/13 [DVT] Change to 988A socket.



7/13 [DVT] Change to 988A socket.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD&CFD (GND)	
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PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enable

CFG0
R1272
NC_3.01K_F
0402

CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 ->0 , 14-> 1 , ...

CFG3
R1273
3.01K_F
0402

CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port
attached to Embedded Display Port
0 : Enable ; An external Display Port device
is connected to the Embedded Display Port

CFG4
R1274
NC_3.01K_F
0402

2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down).
Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.

CFG7
R1289
NC_3.01K_F
0402

Place RP83 Close to So-DIMM Slot

20 DQ_VREF0
21 DQ_VREF1
DQ_VREF0
DQ_VREF1
NC_0
RP83
0404_4P2R
DQ_VREF0_J17
DQ_VREF1_H17

7/8 [DVT] Support M1/M3 Common Motherboard Design

Q92
SI2302DS
DQ_VREF0
R1586
0_J 0402
DIMM0
DQ_VREF0_J17
R5928
100K_J
0402
4 DRAMRST_CNTRL
Q93
SI2302DS
DQ_VREF1
R1587
0_J 0402
DIMM1
DQ_VREF1_H17
R5929
100K_J
0402
DRAMRST_CNTRL

7/24 [DVT] INTEL S3 Power Reduction Solution.

U67E

20MIL TP305	AP25	RSVD1	RSVD32	AJ13 — TP238 20MIL
20MIL TP307	AL25	RSVD2	RSVD33	AJ12 — TP240 20MIL
20MIL TP306	AL24	RSVD3		
20MIL TP308	AL22	RSVD4	RSVD34	AH25 — TP256 20MIL
20MIL TP310	AJ33	RSVD5	RSVD35	AK26 — TP241 20MIL
20MIL TP309	AG9	RSVD6		
20MIL TP311	M27	RSVD7	RSVD36	AL26 — TP258 20MIL
20MIL TP312	L28	RSVD8	RSVD_NCTF_37	AR2 — TP257 20MIL
	J17	RSVD9		
	H17	RSVD10	RSVD38	AJ26 — TP260 20MIL
20MIL TP300	G25	RSVD11	RSVD39	AJ27 — TP259 20MIL
20MIL TP302	G17	RSVD12		
20MIL TP303	E31	RSVD13	RSVD_NCTF_40	AP1 — TP262 20MIL
20MIL TP304	E30	RSVD14	RSVD_NCTF_41	AT2 — TP261 20MIL
			RSVD_NCTF_42	AT3 — TP264 20MIL
			RSVD_NCTF_43	AR1 — TP263 20MIL
			RSVD45	AL28 — TP109 20MIL
			RSVD46	AL29 — TP193 20MIL
			RSVD47	AP30 — TP181 20MIL
			RSVD48	AP32 — TP208 20MIL
			RSVD49	AL27 — TP209 20MIL
			RSVD50	AT31 — TP211 20MIL
			RSVD51	AT32 — TP210 20MIL
			RSVD52	AP33 — TP212 20MIL
			RSVD53	AR33 — TP213 20MIL
			RSVD_NCTF_54	AT33 — TP235 20MIL
			RSVD_NCTF_55	AT34 — TP214 20MIL
			RSVD_NCTF_56	AP35 — TP236 20MIL
			RSVD_NCTF_57	AR35 — TP266 20MIL
			RSVD58	AR32 — TP265 20MIL
			RSVD_TP_59	F15 — TP237 20MIL
			RSVD_TP_60	F15 — TP239 20MIL
			RSVD62	D15 — TP328 20MIL
			RSVD63	C15 — TP329 20MIL
			RSVD64	AJ15
			RSVD65	AH15
				RP87 0 0404_4P2R
			RSVD_TP_66	AA5 — TP331 20MIL
			RSVD_TP_67	AA4 — TP332 20MIL
			RSVD_TP_68	R8 — TP333 20MIL
			RSVD_TP_69	AD3 — TP334 20MIL
			RSVD_TP_70	AD2 — TP335 20MIL
			RSVD_TP_71	AA2 — TP336 20MIL
			RSVD_TP_72	AA1 — TP337 20MIL
			RSVD_TP_73	R9 — TP338 20MIL
			RSVD_TP_74	AG7 — TP339 20MIL
			RSVD_TP_75	AE3 — TP340 20MIL
			RSVD_TP_76	V4 — TP341 20MIL
			RSVD_TP_77	V5 — TP342 20MIL
			RSVD_TP_78	N2 — TP343 20MIL
			RSVD_TP_79	AD5 — TP344 20MIL
			RSVD_TP_80	AD7 — TP347 20MIL
			RSVD_TP_81	W3 — TP348 20MIL
			RSVD_TP_82	W2 — TP349 20MIL
			RSVD_TP_83	N3 — TP350 20MIL
			RSVD_TP_84	AE5 — TP345 20MIL
			RSVD_TP_85	AD9 — TP346 20MIL
			VSS	AP34

CFG0 CFG[0]
CFG[1]
CFG[2]
CFG3 CFG[3]
CFG4 CFG[4]
CFG[5]
CFG[6]
CFG7 CFG[7]
CFG[8]
CFG[9]
CFG[10]
CFG[11]
CFG[12]
CFG[13]
CFG[14]
CFG[15]
CFG[16]
CFG[17]
RSVD_TP_86

RESERVED

20MIL TP321	AM30	CFG[0]	
20MIL TP320	AM28	CFG[1]	
	AP31	CFG[2]	
	AL32	CFG[3]	
	AL30	CFG[4]	
20MIL TP323	AM31	CFG[5]	
20MIL TP325	AN29	CFG[6]	
	AM32	CFG[7]	
20MIL TP313	AK32	CFG[8]	
20MIL TP315	AK31	CFG[9]	
20MIL TP314	AK28	CFG[10]	
20MIL TP316	AJ28	CFG[11]	
20MIL TP317	AN30	CFG[12]	
20MIL TP318	AN32	CFG[13]	
20MIL TP353	AJ32	CFG[14]	
20MIL TP354	AJ29	CFG[15]	
20MIL TP355	AJ30	CFG[16]	
20MIL TP356	AK30	CFG[17]	
20MIL TP357	H16	RSVD_TP_86	
20MIL TP284	B19	RSVD15	
20MIL TP425	A19	RSVD16	
R1583 0_J 0201	A20	RSVD17	
R1584 0_J 0201	B20	RSVD18	
20MIL TP288	U9	RSVD19	
20MIL TP287	T9	RSVD20	
20MIL TP290	AC9	RSVD21	
20MIL TP289	AB9	RSVD22	
20MIL TP292	C1	RSVD_NCTF_23	
20MIL TP291	A3	RSVD_NCTF_24	
20MIL TP294	J29	RSVD26	
20MIL TP293	J28	RSVD27	
20MIL TP296	A34	RSVD_NCTF_28	
20MIL TP295	A33	RSVD_NCTF_29	
20MIL TP298	C35	RSVD_NCTF_30	
20MIL TP297	B35	RSVD_NCTF_31	

SOCKET_988P
FOX_PZ98827-364A-01F

7/13 [DVT] Change to 988A socket.

R1582
0_J
0402

8/3 [DVT] Stuff R1582

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ARD&CFD (RESERVED)	
Size A3	Document Number M930 (MBX-215)	Rev SB
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The traces inside this block should be wider.

RTCRST#

VccRTC

18~25mS

[HDA_DOCK_EN#/GPIO33]
Low (0) – Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) – Security measure defined in the Flash Descriptor will be enabled

Stuff for No-reboot
Low=Default
High=No-reboot

7/28 [DVT] Reduce the BOM Q'ty for C/D.

When int. PLL VR is enabled, HDA_SYNC is VCCVRM 1.5V/1.8V strap (default: L for 1.8V)

7/28 [DVT] Reduce the BOM Q'ty for C/D.

For MP, Dummy CN18, C815, U43 ,R542, Stuff R1551

EXTERNAL SPI0 ROM INTERFACE(FOR U98)

U98 SPI ROM-0

SPI ROM (BIOS)(4M-Bit)

7/15 [DVT] Change U98 to MX25L3205DM2I-12G.

FET Switch For SPI Bus Isolation

For SW Debug

Strap for PCH SPI Program (SW5)	
X	Normal Operation
2 - 3 (ON)	Programing SPI0 (U98)

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: PCH (HDA,JTAG,SAT)

Size: Custom | Document Number: M930 (MBX-215) | Rev: SB

Date: Wednesday, August 12, 2009 | Sheet 10 of 98

PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	ISDB-T Tuner (JP)
Port5	Mach/Tsubaki
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC

U69B

PCI-E* — SMBus — Controller Link — PEG — From CLK BUFFER — Clock Flex

PCH EEPROM/CKG/DIMM/ExpressCard

6/24 [DVT] - Change to ALW Power Rail as DG and SCL.

EC/THM/ALS/dGPU
(SMBus Address: 94h ,96h)

7/8 [DVT] Delete Dummy Parts and Change Net name.

SMBus Address: AEH

Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).
XTAL_IN should be pulled to GND via a 0ohm by default.
This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	PCH (PCI-E,SMBUS,CLK)
Size / Custom	Document Number: M930 (MBX-215)
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Date: Wednesday, August 12, 2009	Sheet 11 of 96

For Disable Auburndale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH. FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

U69C

DMI

DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP

FDI

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

System Power Management

SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_ACK / GPIO30
PWRBTN#
ACPRESENT / GPIO31
BATLOW# / GPIO72
RI#

WAKE#
CLKRUN# / GPIO32
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SLP_S5# / GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN#

3 DMI_RXN0 3 DMI_RXN1 3 DMI_RXN2 3 DMI_RXN3 → DMI_RXN0 BC24, DMI_RXN1 BJ22, DMI_RXN2 AW20, DMI_RXN3 BJ20
3 DMI_RXP0 3 DMI_RXP1 3 DMI_RXP2 3 DMI_RXP3 → DMI_RXP0 BD24, DMI_RXP1 BG22, DMI_RXP2 BA20, DMI_RXP3 BG20
3 DMI_TXN0 3 DMI_TXN1 3 DMI_TXN2 3 DMI_TXN3 → DMI_TXN0 BE22, DMI_TXN1 BF21, DMI_TXN2 BD20, DMI_TXN3 BE18
3 DMI_TXP0 3 DMI_TXP1 3 DMI_TXP2 3 DMI_TXP3 → DMI_TXP0 BD22, DMI_TXP1 BH21, DMI_TXP2 BC20, DMI_TXP3 BD18

+V1.1S_VCC_EXP
R874 1 49.9_F 2 0402 DMI_COMP → BH25 DMI_ZCOMP, BF25 DMI_IRCOMP

FDI_RXN0 BA18, FDI_RXN1 BH17, FDI_RXN2 BD16, FDI_RXN3 BJ16, FDI_RXN4 BA16, FDI_RXN5 BE14, FDI_RXN6 BA14, FDI_RXN7 BC12
FDI_RXP0 BB18, FDI_RXP1 BF17, FDI_RXP2 BC16, FDI_RXP3 BG16, FDI_RXP4 AW16, FDI_RXP5 BD14, FDI_RXP6 BB14, FDI_RXP7 BD12
FDI_INT BJ14
FDI_FSYNC0 BE13
FDI_FSYNC1 BH13
FDI_LSYNC0 BJ12
FDI_LSYNC1 BG14

7/8 [DVT] Delete iGPU, Leave NC.

7/31 [DVT] Add the Q7 as MOR request.

23,52 SUS_PWRGD → Q7 DTC144EUA → PCIE_WAKE# F
26,27,29 PCIE_WAKE#

25 SB_RST# → SB_RST# T6
23,54 IMVP_PWRGD → M6
R972 2.2K_J 0402 → PWROK B17
4,23,51,52,57 RUN_PWRGD → R927 1 0_J 2 0402 → R918 1 NC_0_J 2 0402 → MPWROK_R K5
R940 1 NC_0_J 2 0402 LAN_RST# → A10
R917 1 10K_J 2 0402
4 PM_DRAM_PWRGD → D9
23 PM_RSMRST# → R916 2.2K_J 0402 → PM_RSMRST# R C16
23 SUS_PWR_ACK → SUS_PWR_ACK M1
23 PWRBTN# → PWRBTN# P5
23 AC_Present → AC_Present R930 1 0_J 2 0402 → AC_Present_R P7
PM_BATLOW# A6
PM_RI# F14

WAKE# J12 → PCIE_WAKE# F
CLKRUN# / GPIO32 Y1 → PM_CLKRUN# → PM_CLKRUN# 23,25
SUS_STAT# / GPIO61 P8 → PM_SUS_STAT# → PM_SUS_STAT# 25
SUSCLK / GPIO62 F3 → PM_S4_STATE# 1 → TP170 20MIL
SLP_S5# / GPIO63 E4 → PM_SLP_S5# → PM_SLP_S5# 23
SLP_S4# H7 → PM_SLP_S4# → PM_SLP_S4# 23
SLP_S3# P12 → PM_SLP_S3# → PM_SLP_S3# 23
SLP_M# K8 → PM_SLP_ME# → PM_SLP_ME# 23
TP23 N2 → PM_SLP_DSW# 1 → TP362 20MIL
PMSYNCH BJ10 → H_PM_SYNC → H_PM_SYNC 4
SLP_LAN# F6 → PM_SLP_LAN# 1 → TP361 20MIL

7/24 [DVT] Change R911 to 10Kohm as MOR request.

+3VRUN
SB_RST# R945 1 8.2K_J 2 0201
PM_CLKRUN# R912 1 8.2K_J 2 0201

+3VALW
PCIE_WAKE# F R911 1 10K_J 2 0201
PM_RI# R910 1 10K_J 2 0201
PM_SLP_LAN# R914 1 NC_10K_J 2 0201
PM_BATLOW# R913 1 8.2K_J 2 0201
SUS_PWR_ACK R920 1 8.2K_J 2 0201
AC_Present R921 1 NC_10K_J 2 0201
SB_RST# R922 1 NC_8.2K_J 2 0201
PM_RSMRST# R915 1 10K_J 2 0201
PWROK R1576 1 10K_J 2 0201

+3VRUN
R931 NC_10K_J 0402
MPWROK_R R923 1 NC_0_J 2 0402 LAN_RST#

7/28 [DVT] Reserve R930 for Leakage Check

PM_SLP_ME# 1 → TP171 20MIL

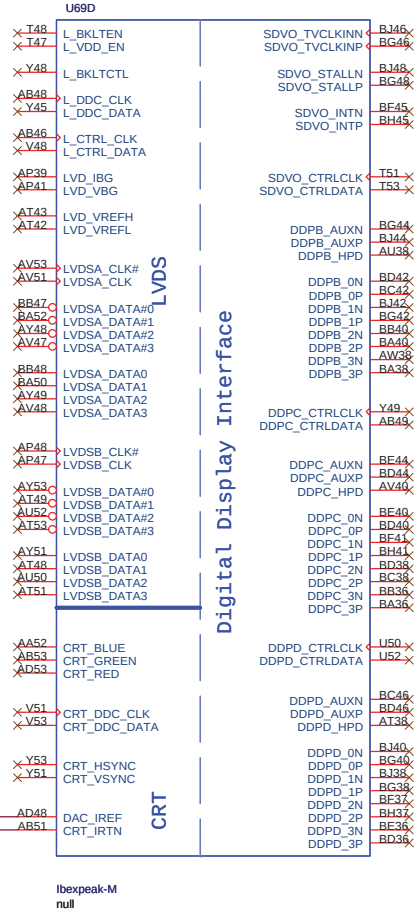
7/27 [DVT] Dummy the R921 for ME function support and avoid the leakge concern.
(Optional if Intel ME FW is IntelR ME Ignition Firmware)

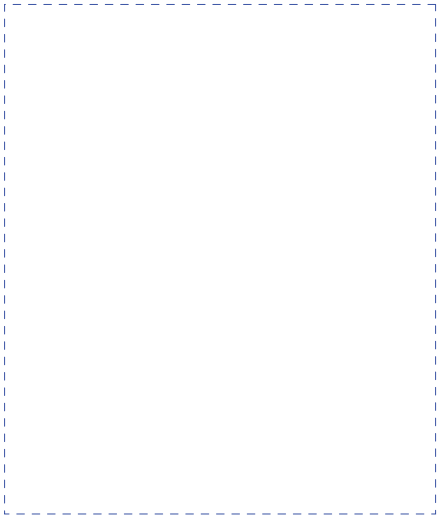
PM_RSMRST# R 2 → D28 BAS316PT → ALW_PWRGD 23,50
PWROK 2 → D29 BAS316PT

ibexpeak-M
null

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (DMI,FDI,GPIO)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 12 of 96	

7/8 [DVT] Delete iGPU, Leave NC.

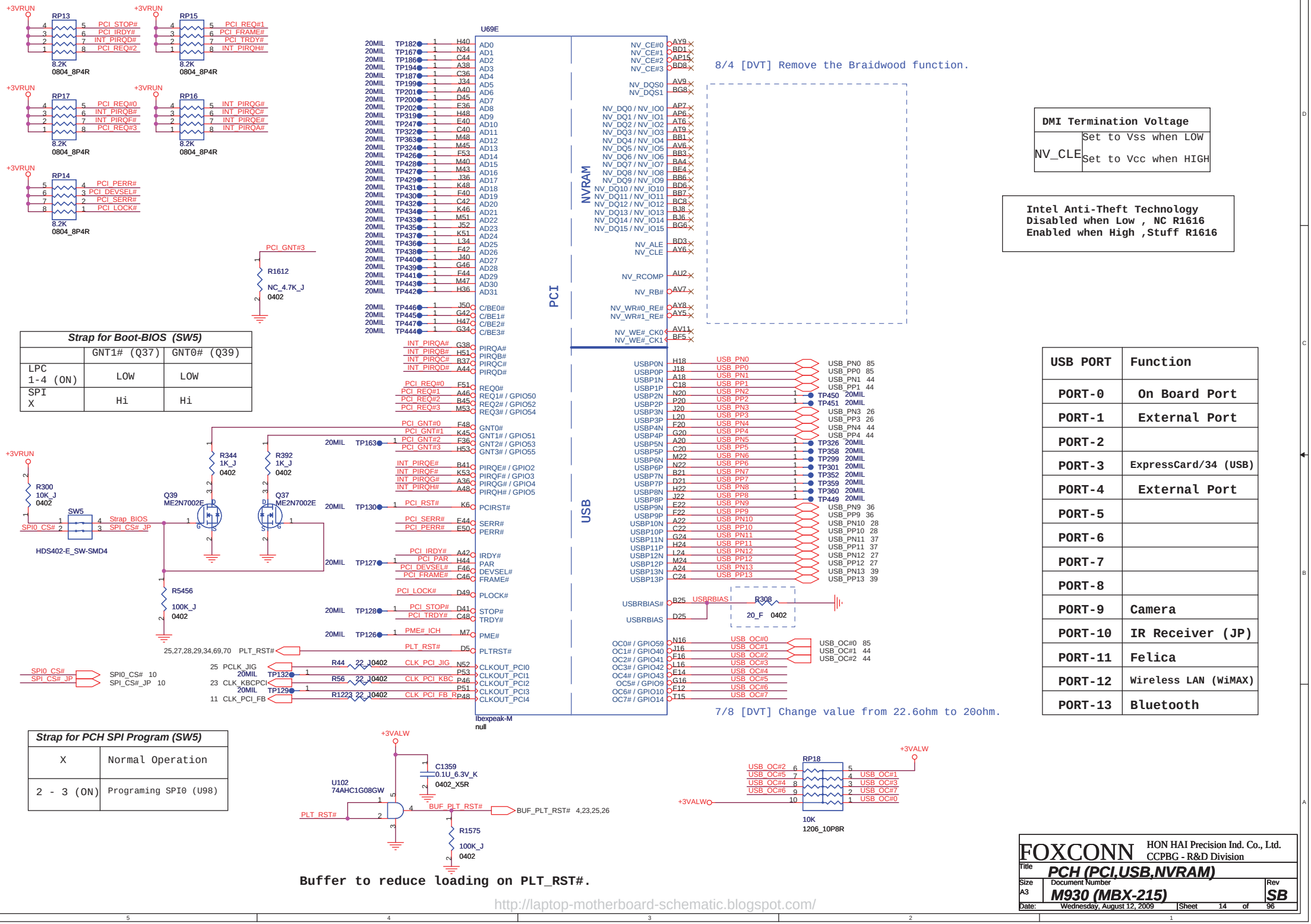




7/8 [DVT] Delete iGPU, Leave NC.

Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (LVDS,DDI)	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 13 of 96	



Strap for Boot-BIOS (SW5)		
	GNT1# (Q37)	GNT0# (Q39)
LPC 1-4 (ON)	LOW	LOW
SPI X	Hi	Hi

Strap for PCH SPI Program (SW5)	
X	Normal Operation
2 - 3 (ON)	Programing SPI0 (U98)

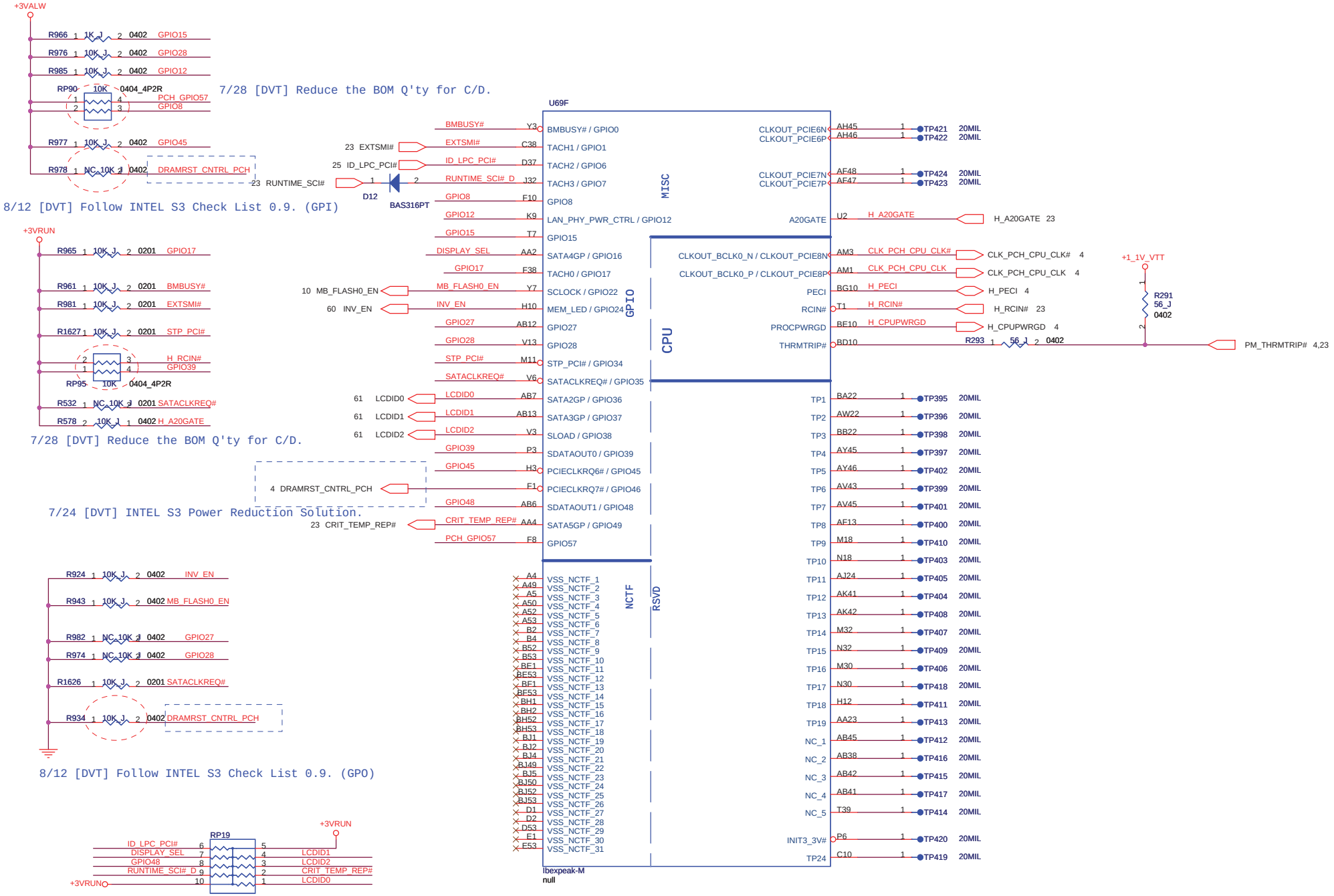
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Intel Anti-Theft Technology
Disabled when Low , NC R1616
Enabled when High ,Stuff R1616

USB PORT	Function
PORT-0	On Board Port
PORT-1	External Port
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	IR Receiver (JP)
PORT-11	Felica
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth

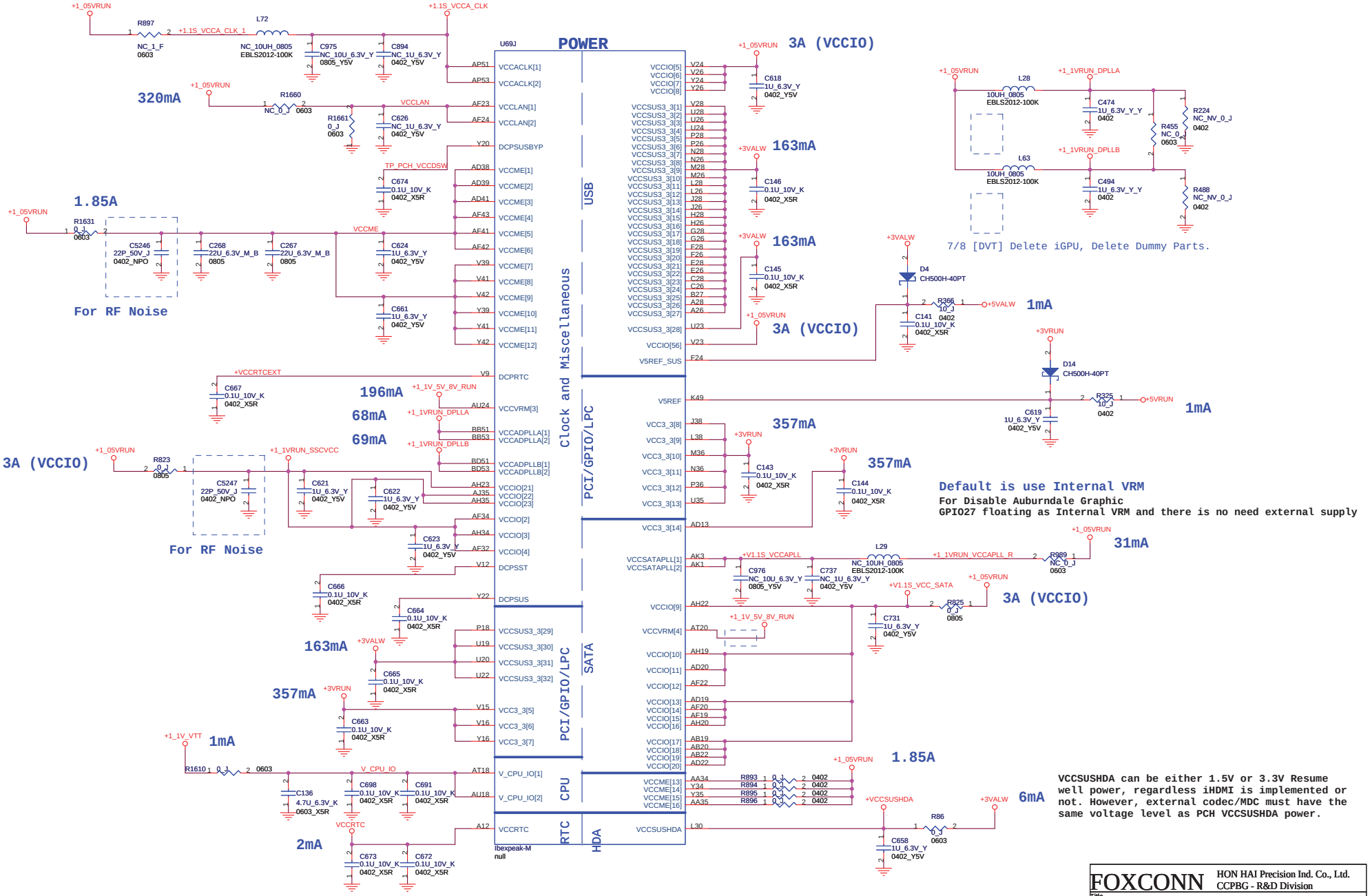
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: PCH (PCI,USB,NVRAM)
Size: A3 | Document Number: M930 (MBX-215) | Rev: SB
Date: Wednesday, August 12, 2009 | Sheet 14 of 96



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (GPIO,VSS_NCTF,RSVD)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 15 of 96	

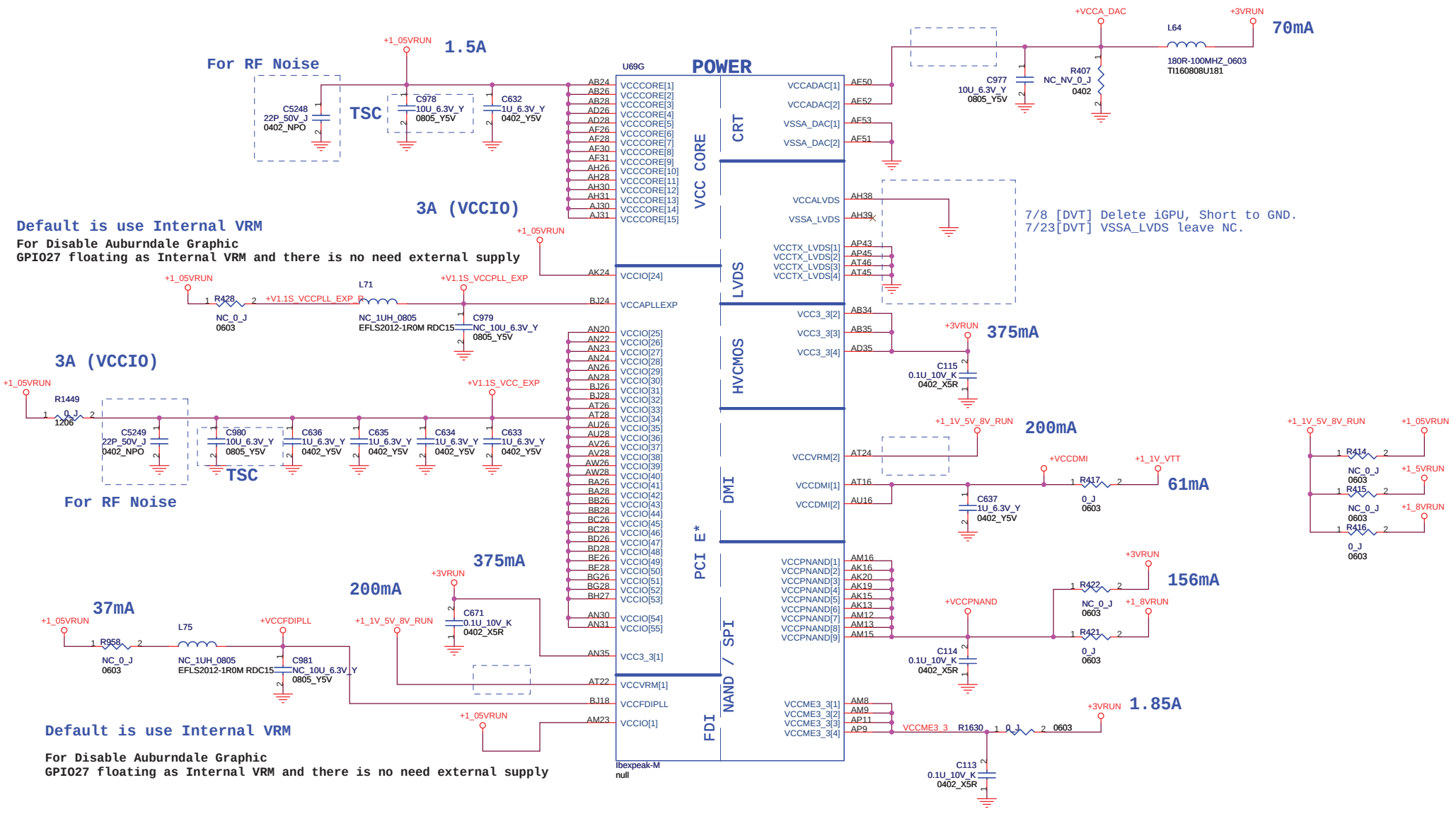
Default is use Internal VRM
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



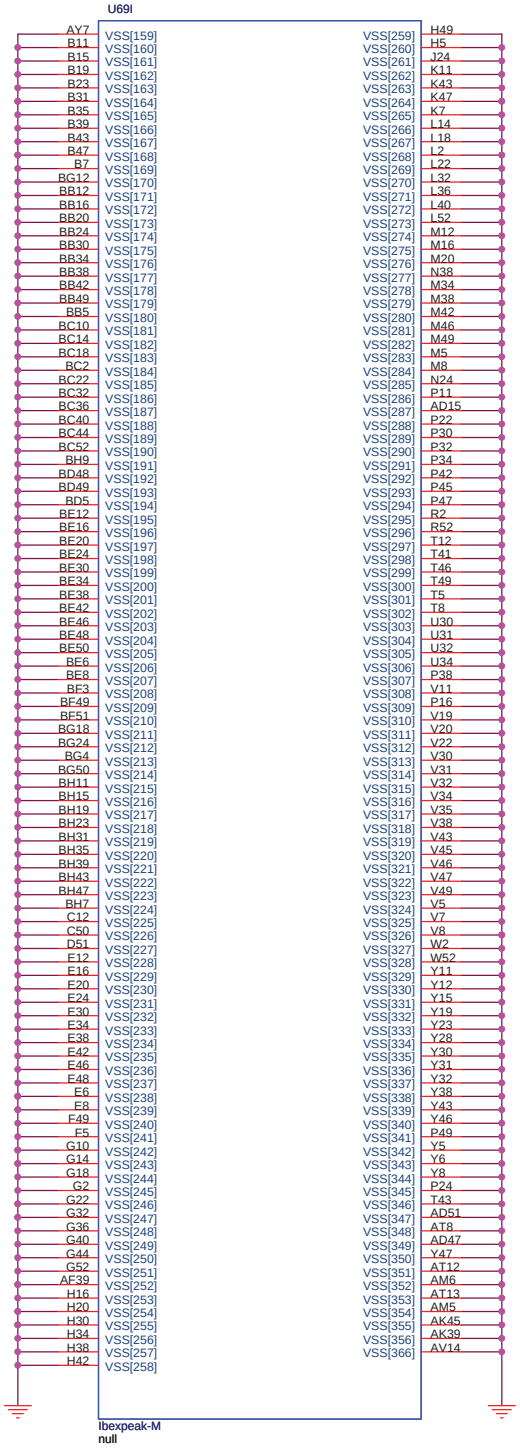
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

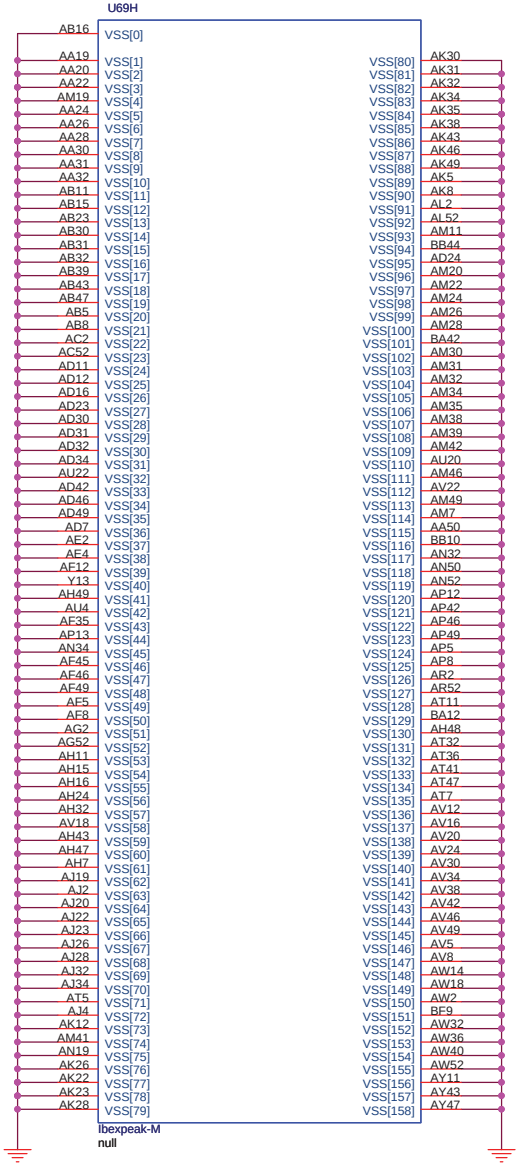
Title	PCH (POWER) 1/2	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 16 of 96	

7/8 [DVT] Delete iGPU, Delete Dummy Parts.



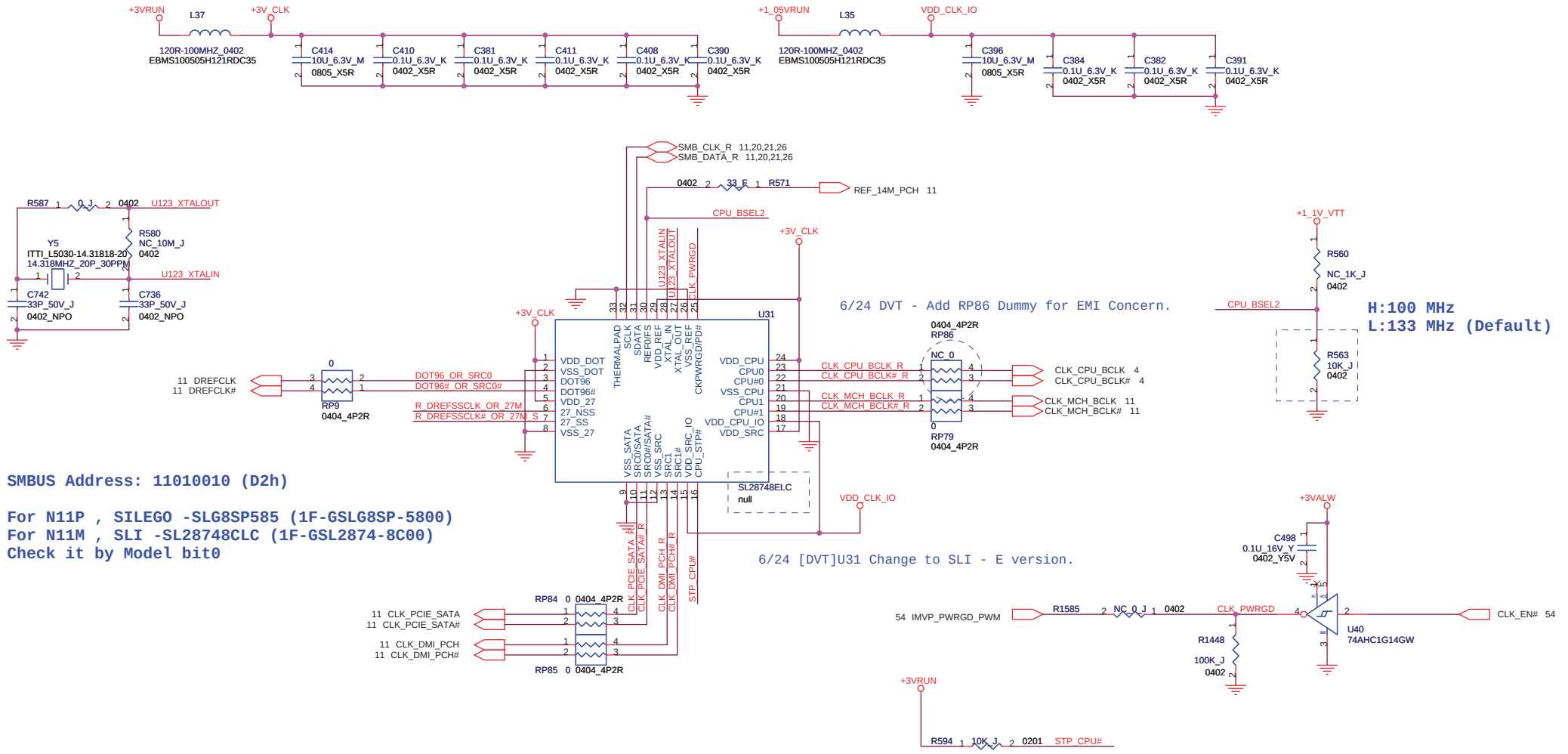
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 2/2	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 17 of 96	





FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	PCH (VSS)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 18 of 96	



Frequency Select Pin (FS)

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	CLOCK GEN	
Size A3	Document Number M930 (MBX-215)	Rev SB
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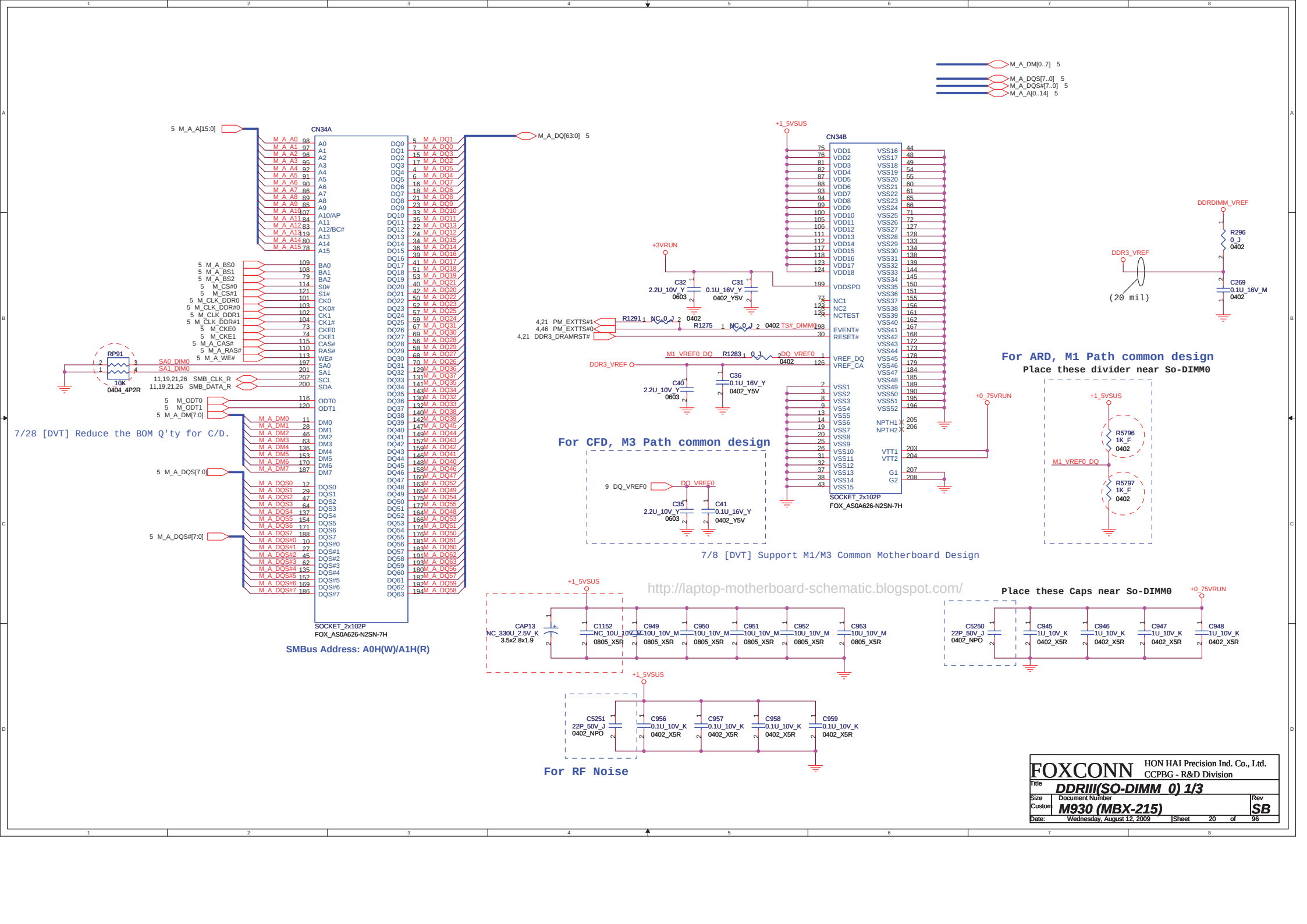
M_A_DM[0..7] 5
M_A_DQS[7..0] 5
M_A_DQS#[7..0] 5
M_A_A[0..14] 5
CN34A
5 M_A_A[15:0]
M_A_DQ[63:0] 5
SOCKET_2x102P
FOX_AS0A626-N2SN-7H
SMBus Address: A0H(W)/A1H(R)
RP91
10K
0404_4P2R
SA0_DIM0
SA1_DIM0
11,19,21,26 SMB_CLK_R
11,19,21,26 SMB_DATA_R
7/28 [DVT] Reduce the BOM Q'ty for C/D.
CN34B
+1_5VSUS
+3VRUN
4,21 PM_EXTTS#1
4,46 PM_EXTTS#0
4,21 DDR3_DRAMRST#
TS#_DIMM0
M1_VREF0_DQ
DQ_VREF0
DDR3_VREF
+0_75VRUN
For CFD, M3 Path common design
9 DQ_VREF0
7/8 [DVT] Support M1/M3 Common Motherboard Design
For ARD, M1 Path common design
Place these divider near So-DIMM0
DDRDIMM_VREF
(20 mil)
http://laptop-motherboard-schematic.blogspot.com/
Place these Caps near So-DIMM0
For RF Noise
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
DDRIII(SO-DIMM_0) 1/3
Size
Custom
Document Number
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SB
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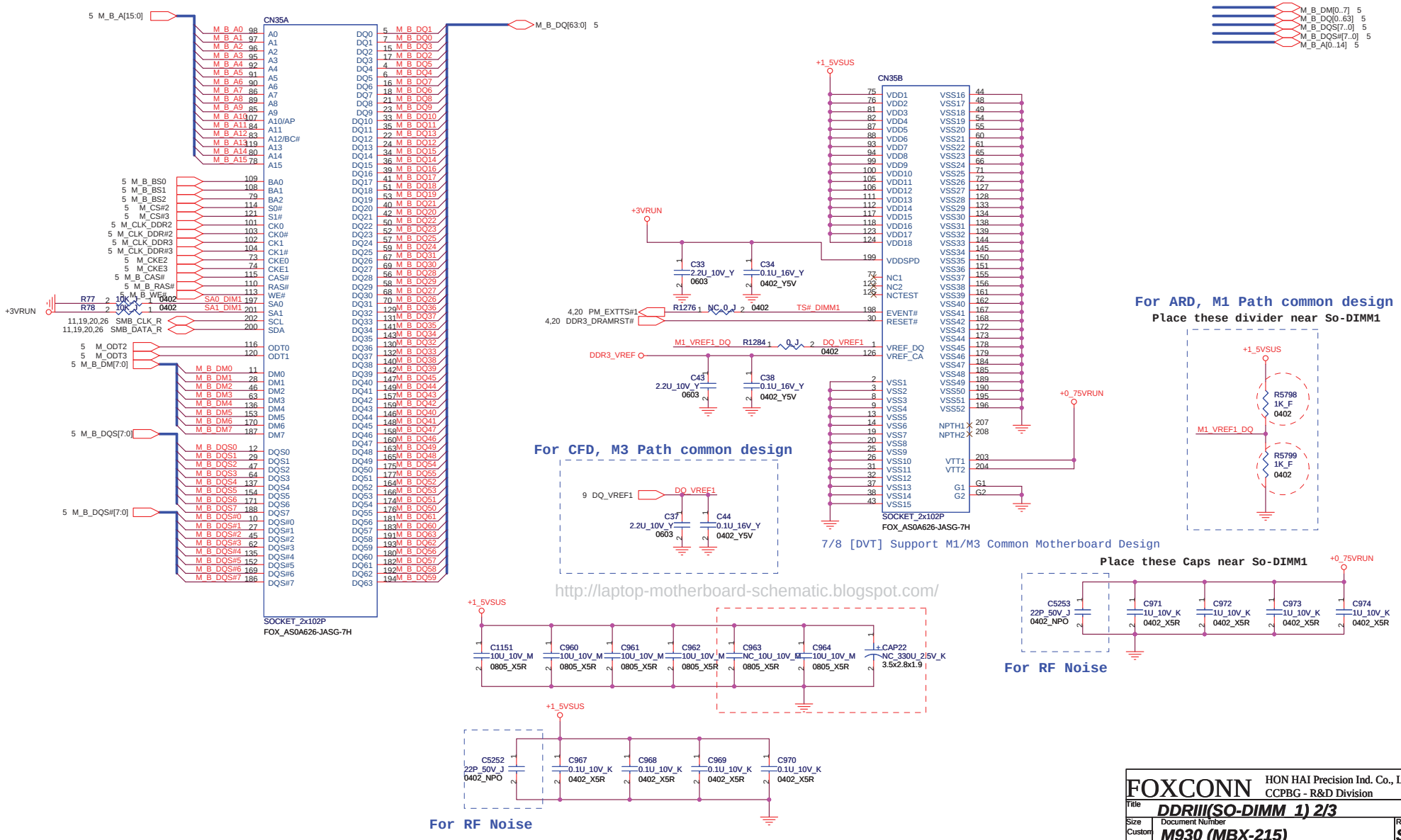
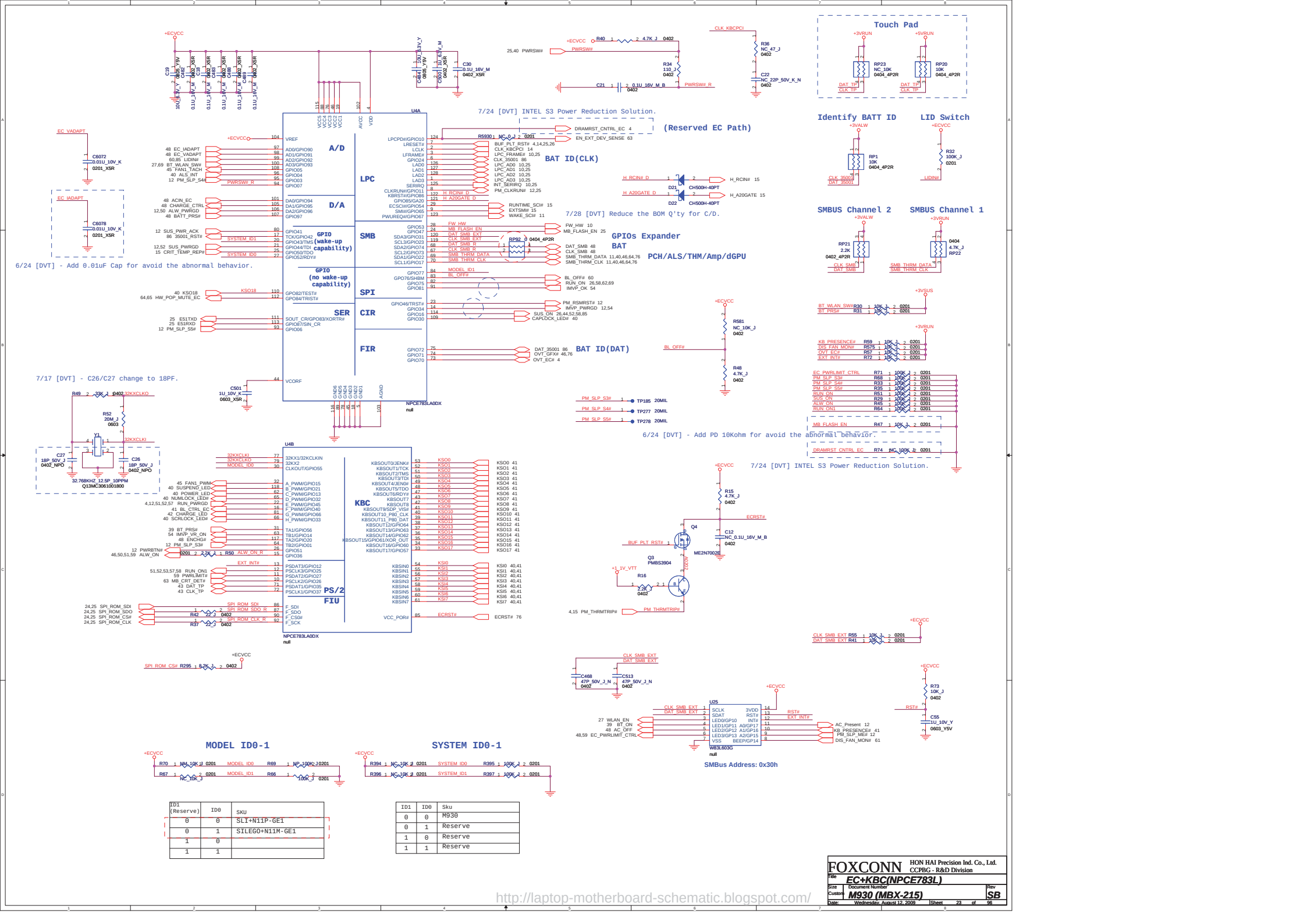


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	DDRIII(SO-DIMM_1) 2/3		
Size: Custom	Document Number: M930 (MBX-215)		Rev: SB
Date: Wednesday, August 12, 2009	Sheet 21 of 96		

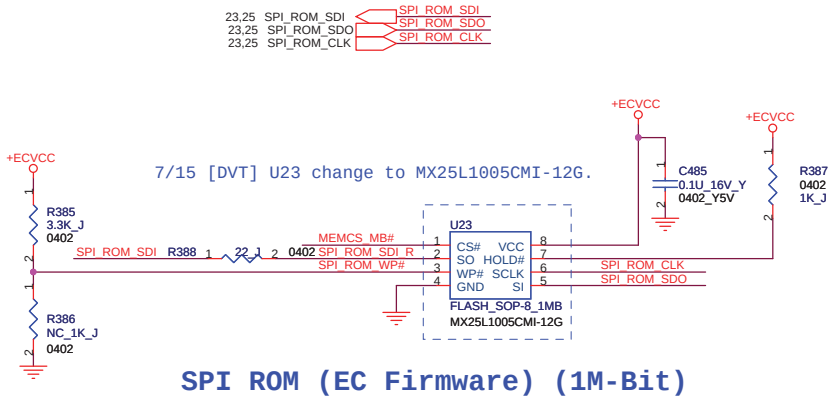
Delete M2 Path (Intel Revised)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SO-DIMM VREF 3/3	
Size: A3	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 22 of 96	

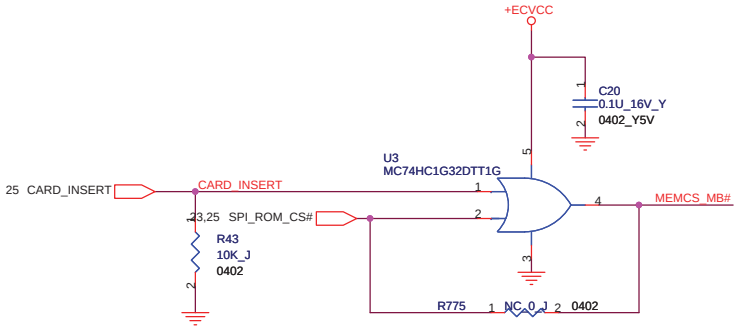


ID1 (Reserve)	ID0	SKU
0	0	SLI+N11P-GE1
0	1	SILEGO+N11M-GE1
1	0	
1	1	

ID1	ID0	Sku
0	0	M930
0	1	Reserve
1	0	Reserve
1	1	Reserve

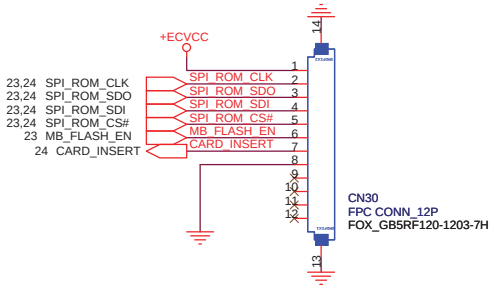


SPI ROM (EC Firmware) (1M-Bit)

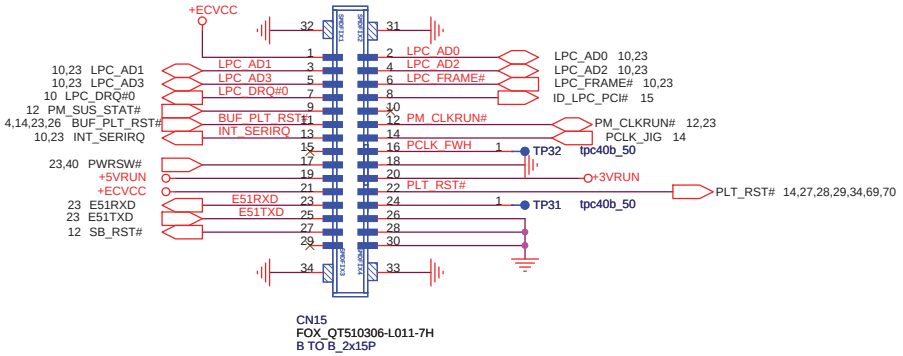


For MP, Dummy R43, C20 ,U3 ,CN30 and Stuff R775

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SPI Flash ROM	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 24 of 96	



EXTERNAL SPI ROM INTERFACE (EC)



JIG-120

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***Debug Port***	
Size A3	Document Number ***M930 (MBX-215)***	Rev ***SB***
Date: Wednesday, August 12, 2009	Sheet 25 of 96	

+1_5V=>0.65A
+3_3VAux=>0.275A
+3_3V=>1.3A

7/24 [DVT] Short R677,R683,R682,R685.

Pin2,4 & Pin12,14
Pin3,5 & Pin11,13
short for GMT577 test

7/23 [DVT] Add R345 for MOR request. (Reserve)

8/10 [DVT] Add R636 for MOR request. (Reserve)

Place near by CN11 Pin.

Express Card Slot.

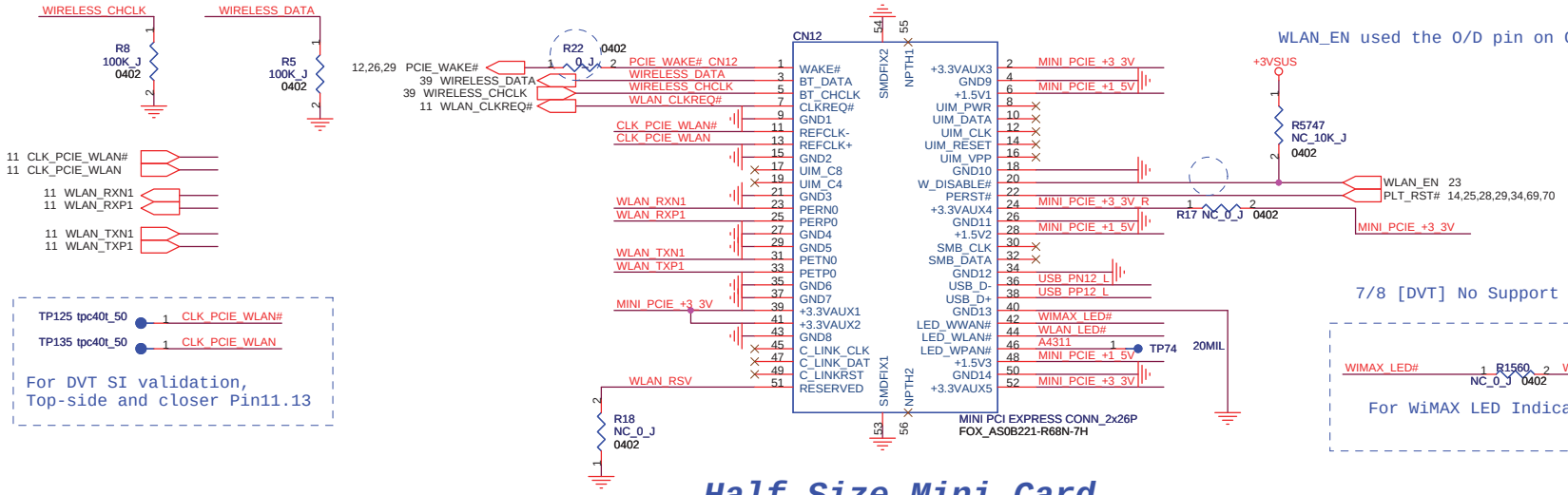
7/8 [DVT] Change the CN10 Footprint symbol for Screw PAD.

Express Card Housing.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EXPRESS CARD	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 26 of 96	

8/3 [DVT] Reserve R22 as MOR request. (WoWLAN Function)

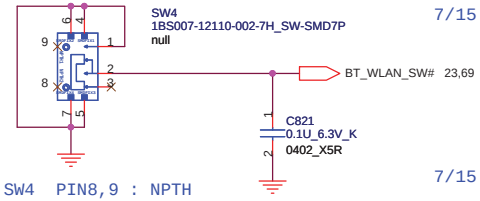
WLAN_EN used the O/D pin on GPIOs Expander (U25)



7/8 [DVT] No Support WiMAX Feature

Half Size Mini Card

WLAN Switch



SW4 PIN8,9 : NPTH

TP139 tpc40t_50 BT_WLAN_SW#
TP141 tpc40t_50

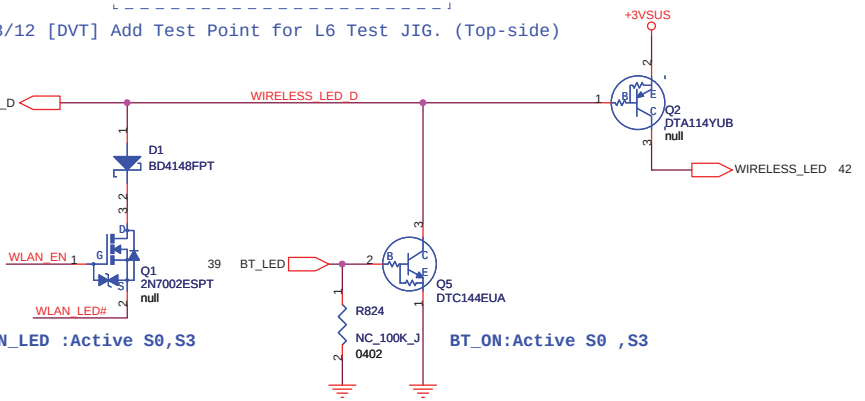
7/15 [DVT] Add Test Point for L6 Test JIG. (Top-side)

TP142 tpc40t_50 BT_WLAN_SW#
TP143 tpc40t_50

7/15 [DVT] Add Test Point for L6 Test JIG. (Bot-side)

TP154 tpc40t_50 WIRELESS_LED_D

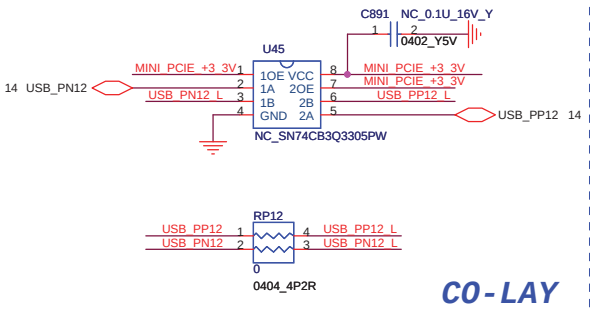
8/12 [DVT] Add Test Point for L6 Test JIG. (Top-side)



WLAN_LED :Active S0,S3

BT_ON:Active S0 ,S3

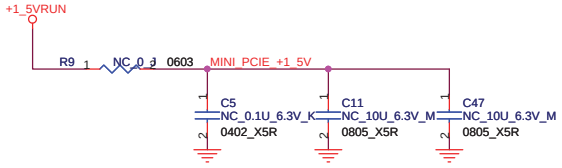
USB I/F for Wi-MAX(Kilmer Peak)



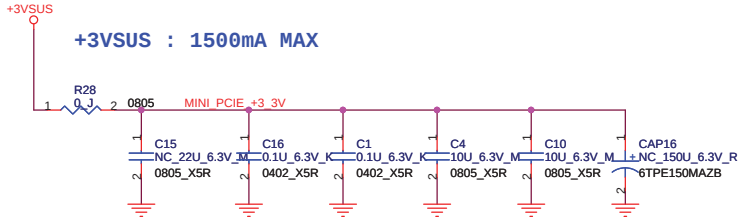
CO-LAY

+1_5VRUN : 330mA MAX

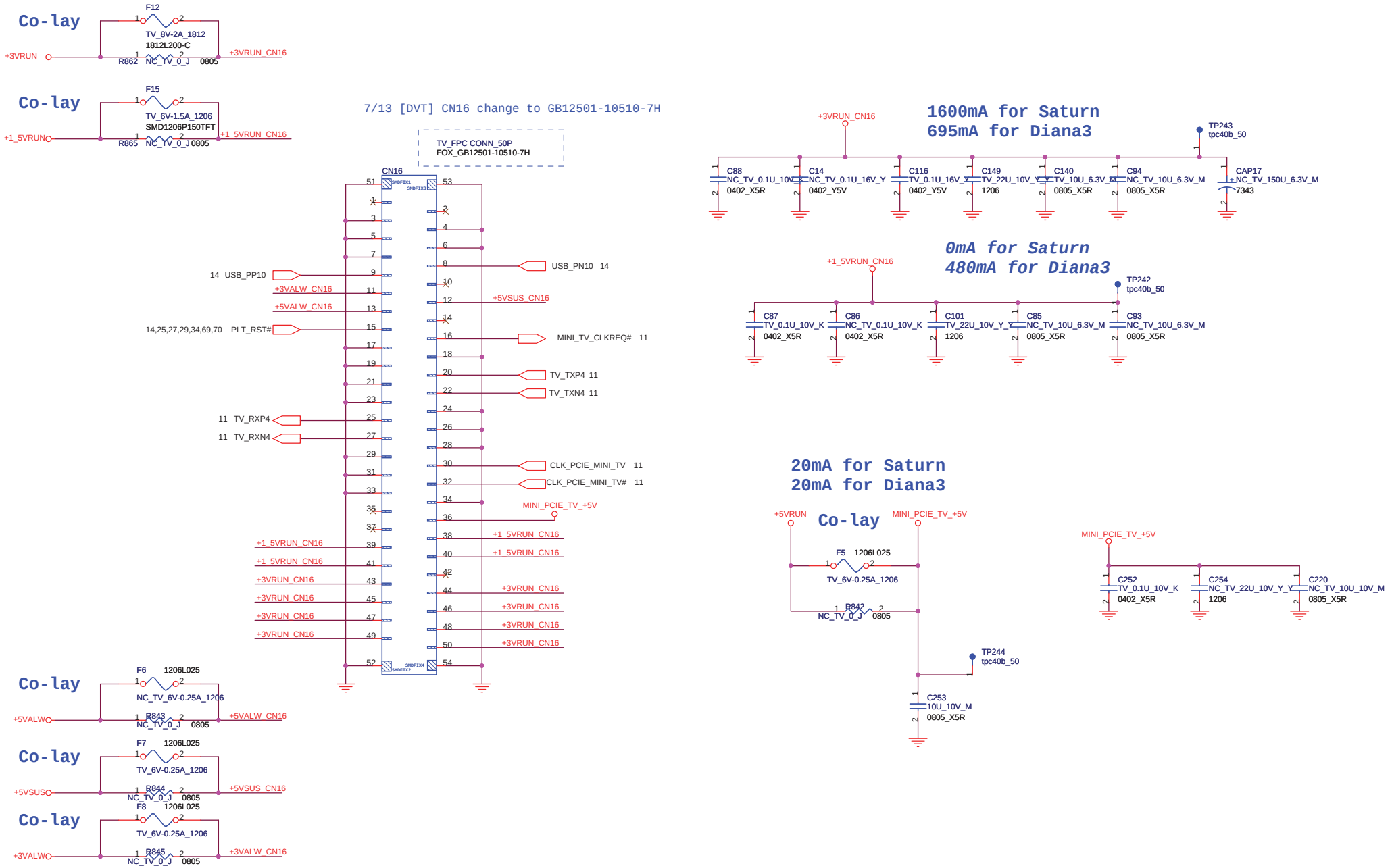
Intel Puma Peak & Kilmer Peak nonsupport +1_5VRUN



+3VSUS : 1500mA MAX



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Mini-PCIE Card (WLAN)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 27 of 96	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	TV-Tuner connector	
Size A3	Document Number M930 (MBX-215)	Rev SB
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8/5 [DVT]Add EC10~EC15 for EMI Solution.

For 8059 Dummy R88 ,C151, and Stuff R87 ,C148
For 8057 Dummy R87, C148 and Stuff R88 ,C151

For 8059 Dummy R85 ,C150, and Stuff R84
For 8057 Dummy R84 and Stuff R85 ,C150

For 8059 Dummy R83 ,C147, and Stuff R82 ,C139
For 8057 Dummy R82, C139 and Stuff R83 ,C147

8/5 [DVT]Add EC16 for EMI Solution.

For 8059 Stuff R97
For 8057 Dummy R97

For 8059 Z0 version ONLY,
It's LDO Power-Up Issue workround.

For Disable EEPROM

http://laptop-motherboard-schematic.blogspot.com/

Dummy all when use 88E8059 (A0/Z0)

Place C993/C994
close as U70 pin

For 8059 Stuff R89,R90, C993 ,C994
For 8057 Dummy R89,,R90, C993 ,C994

426mA

Close to Chip

Power Down of 8057
Stuff R1003.

For 8057 Stuff R94 C997
For 8059 Dummy R94, C997

For 8059 Z0 version ONLY , Dummy R1003
For 8059 A0 version ONLY, Stuff R1003

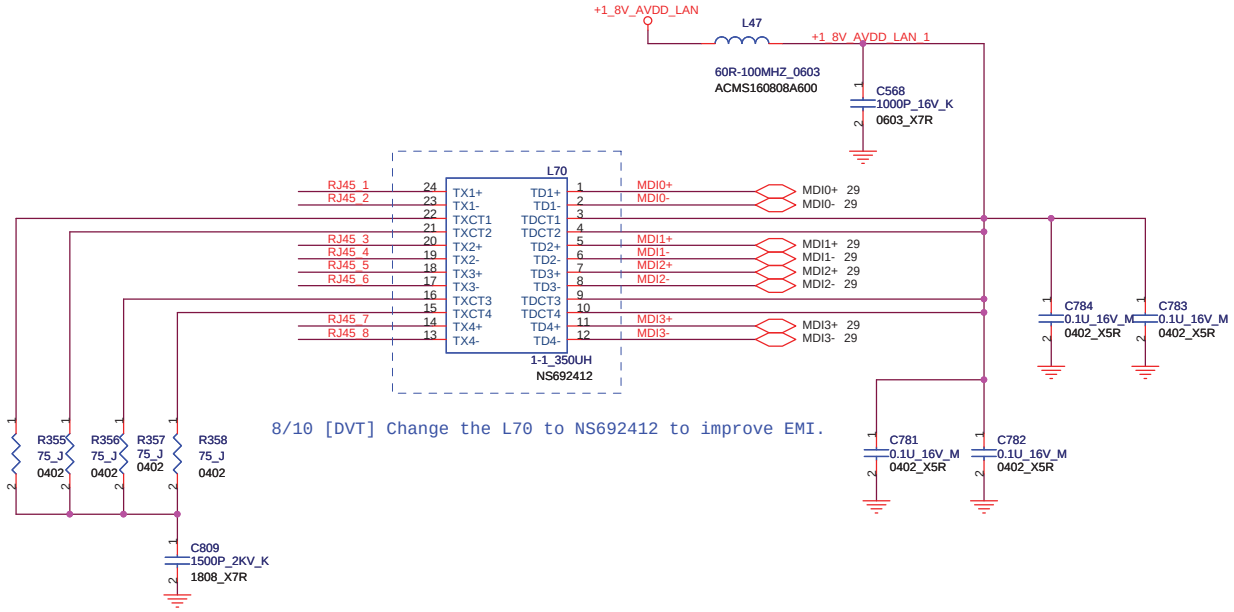
For 8059 Dummy R96 ,C155, and Stuff R85 ,C154
For 8057 Dummy R95, C154 and Stuff R96 ,C155

Dummy all when use 88E8059 (A0/Z0)

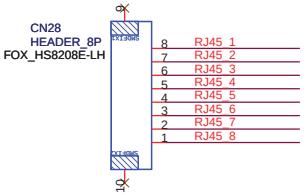
7/17 [DVT]Change the Y6 to 25MHZ_12P_30PPM.
8/12 [DVT]Change the Y6 to E5FA25.0000F12D33.

7/8 [DVT] Change the C988, C989 CL value to 12P.

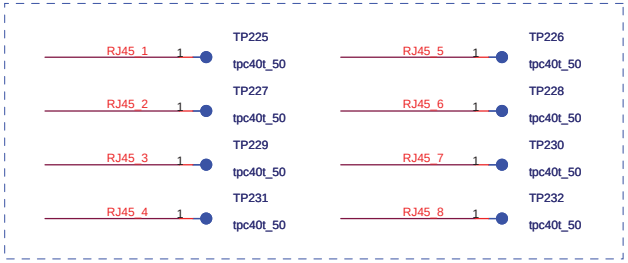
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	LAN (88E8057) 1/2
Size: Custom	Document Number: M930 (MBX-215)
Rev	SB
Date: Wednesday, August 12, 2009	Sheet 29 of 96



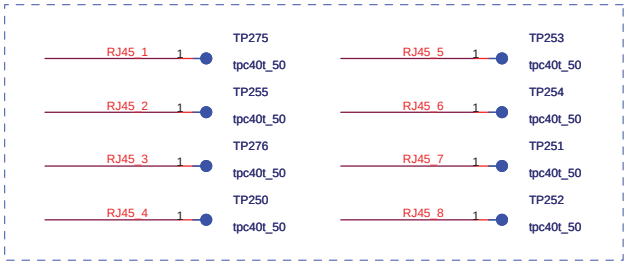
8/10 [DVT] Change the L70 to NS692412 to improve EMI.



RJ45

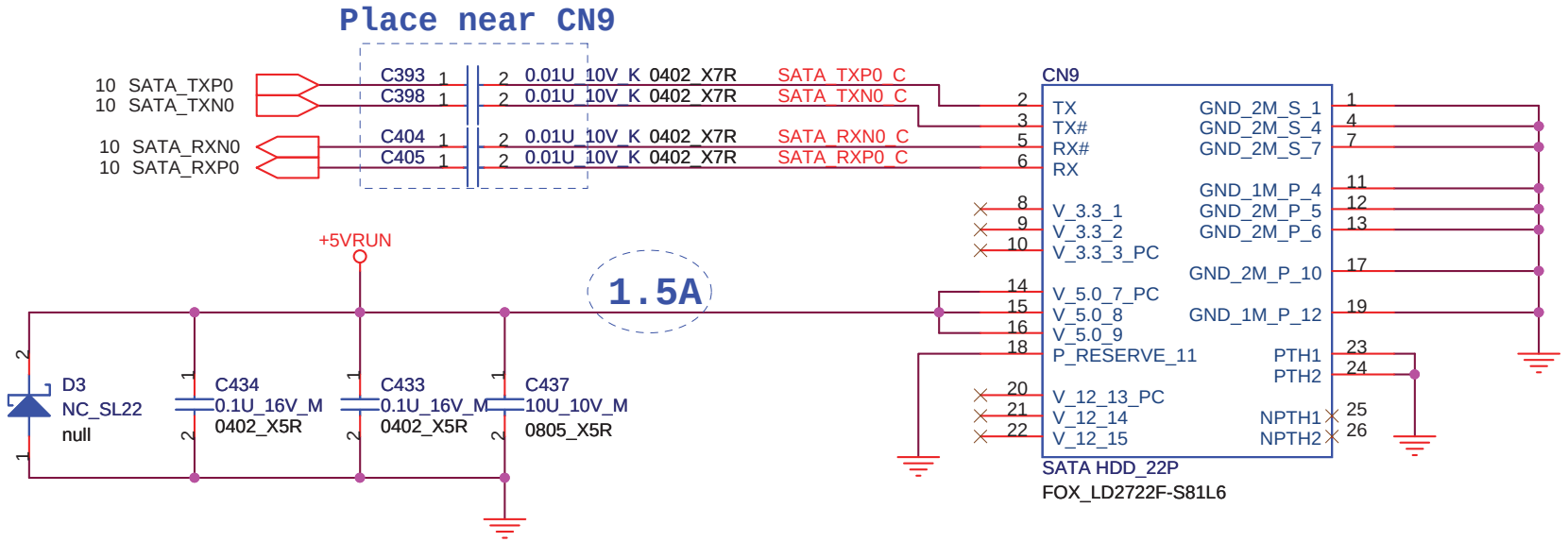


7/15 [DVT] Add Test Point for L6 Test JIG. (Top-side)



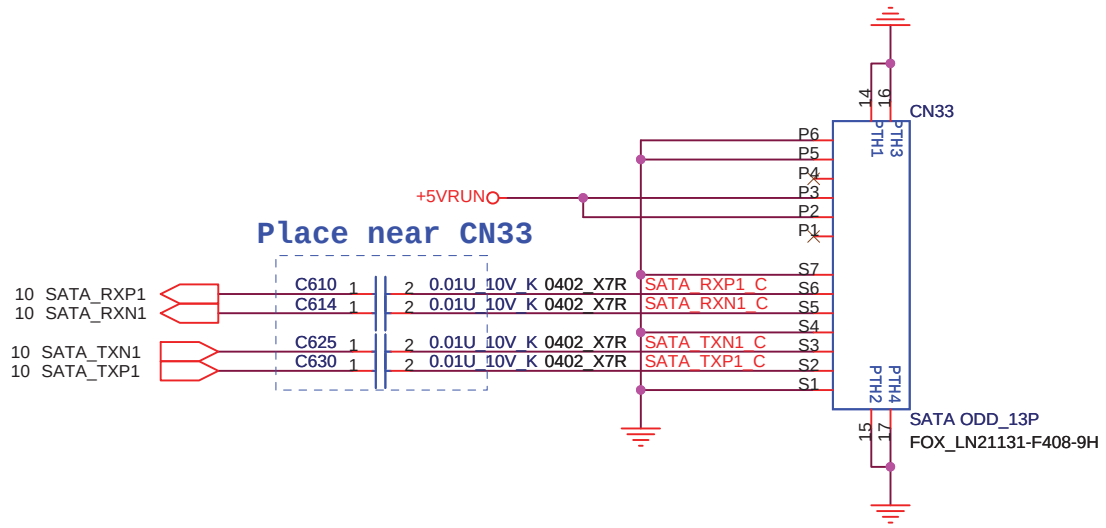
7/15 [DVT] Add Test Point for L6 Test JIG. (Bot-side)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN (Transfomer)(2/2)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 30 of 96	

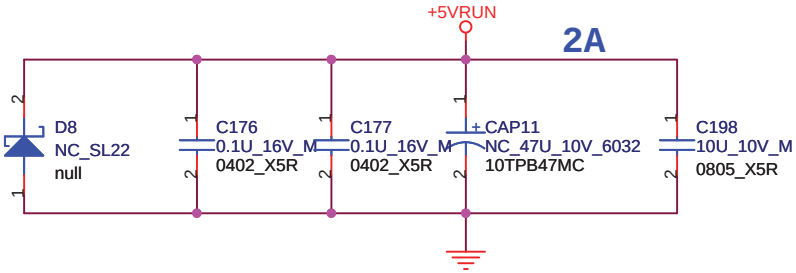


SATA HDD CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD		
Size: A	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 31 of 96	



SATA ODD CONN



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA ODD		
Size: A4	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 32 of 96	

Remove Braidwood (Intel Updated and MOR confirmed)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Braidwood Connector		
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 33 of 96	

7/9 [DVT] Change C785/C786 value to 24P depends on Cystal report.

Place the R/C close to U71

7/8 [DVT] Change Damping value to fix the OS/US issue.

Place the damping close to U71

Place the CAP close to CN36

MS HG-DUO CONN.

i.Link CONN.

Close to U71

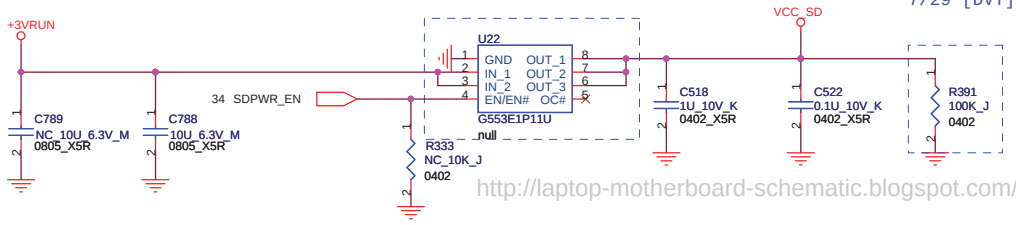
SROM: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)

Place the R/C close to U71

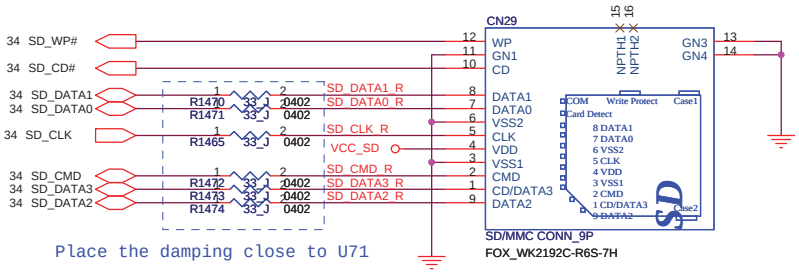
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCIE (MS&iLink) 1/2		
Size: Custom	Document Number: M930 (MBX-215)		Rev: SB
Date: Wednesday, August 12, 2009	Sheet 34 of 96		

7/9 [DVT] U22 Change to G553E1P11U.

7/29 [DVT] Change R391 to 100K as VEDS.



SD POWER

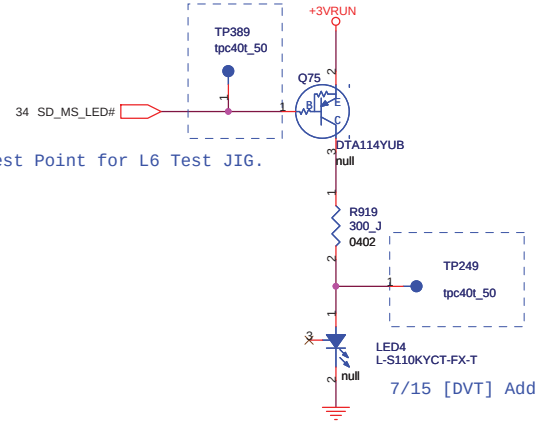


Place the damping close to U71

7/8 [DVT] Change Damping value to fix the OS/US issue.

SD CONN.

SD/MS LED



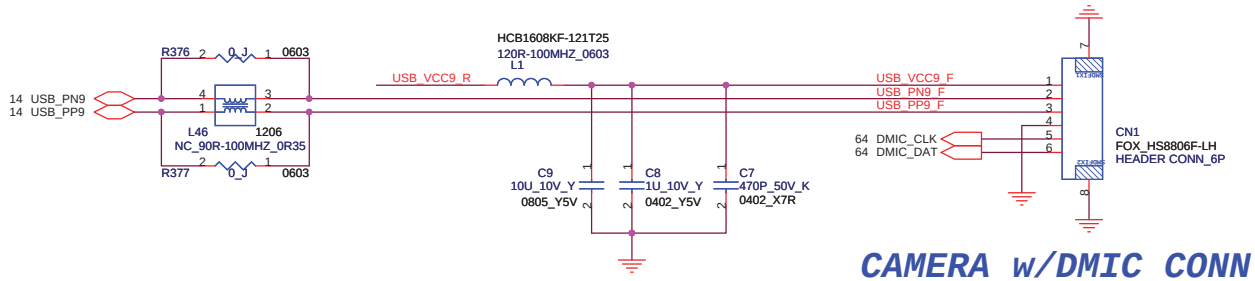
8/12 [DVT] Add Test Point for L6 Test JIG.

7/15 [DVT] Add Test Point for L6 Test JIG.

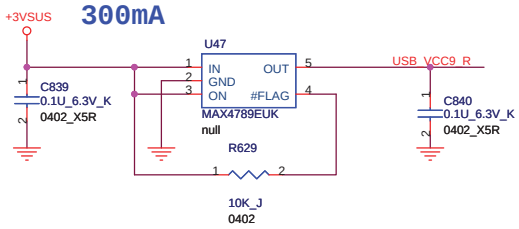
8/5 [DVT] Dummy C767 and Change R1465 to 33ohm.

For EMI

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: PCIE (SD) 2/2		
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 35 of 96	



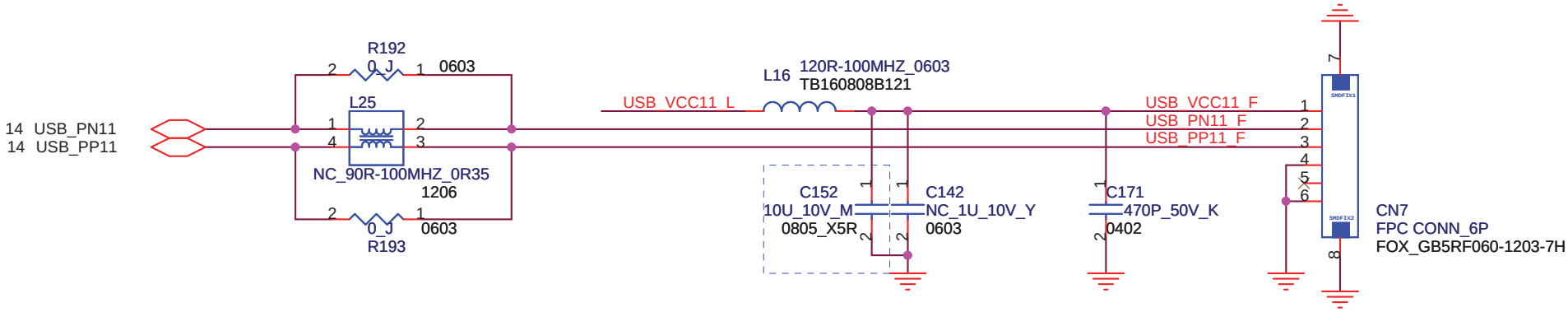
CAMERA w/DMIC CONN.



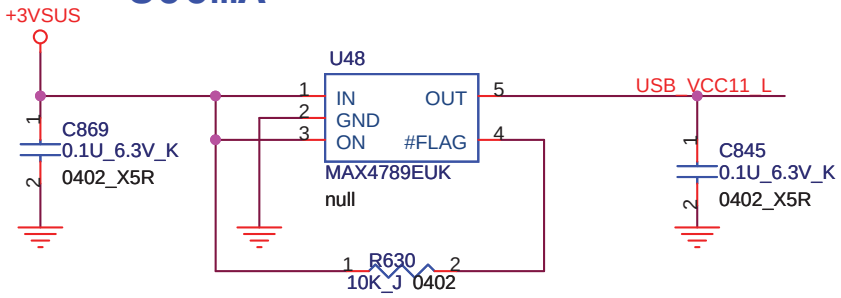
300mA

Currert Limit Switch

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Camera w/DMIC Connector	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 36 of 96	



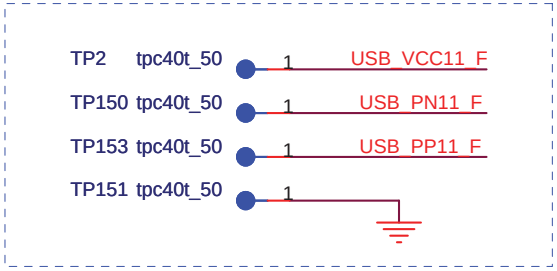
300mA



Felica Conn.

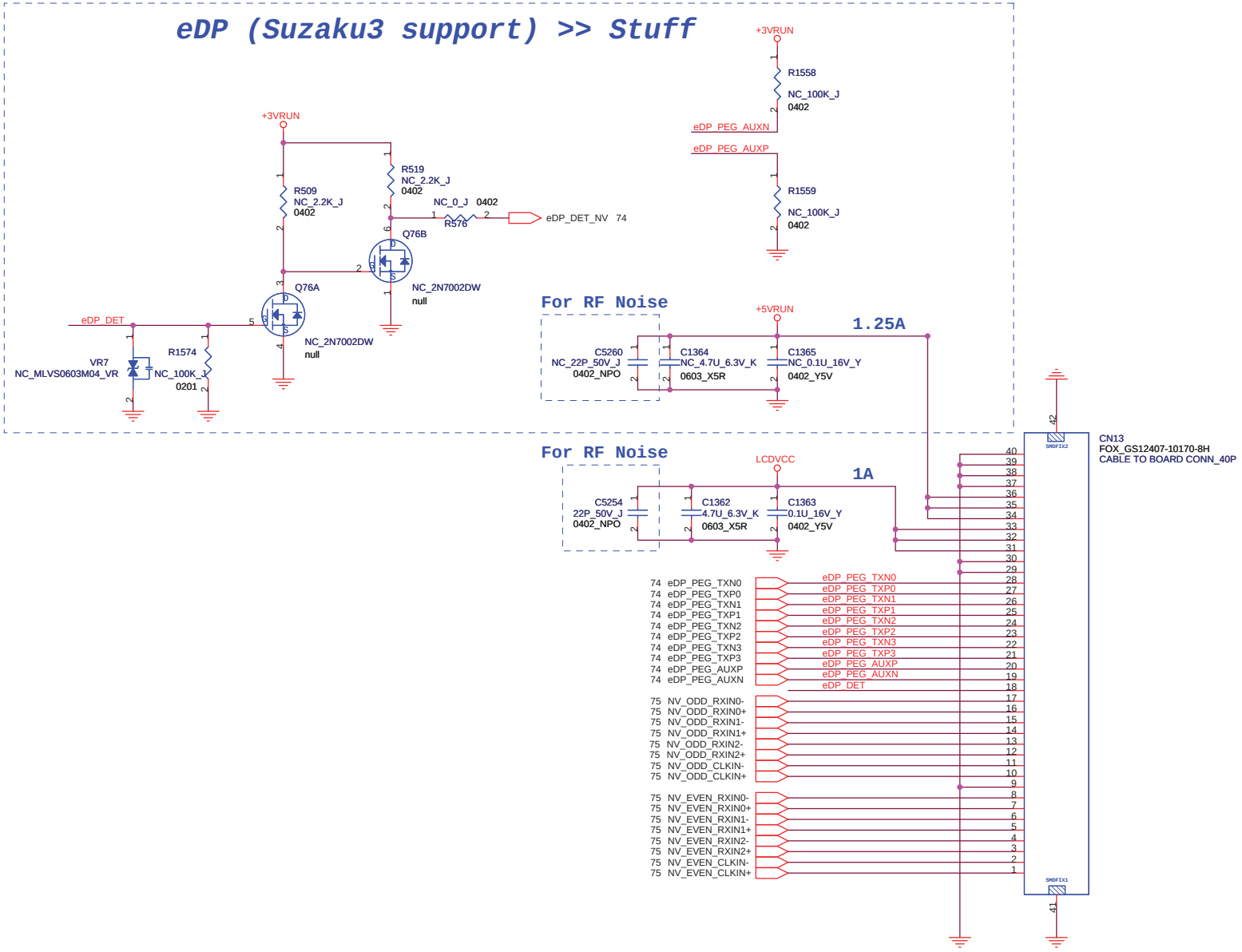
Felica Vdd Spec. (3.15V to 3.45V)

Currert Limit Switch

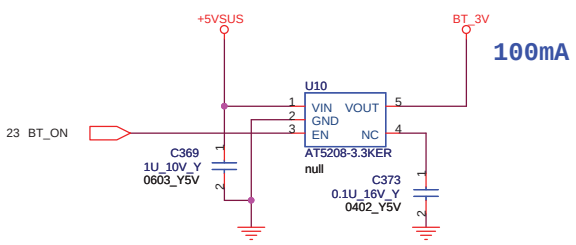


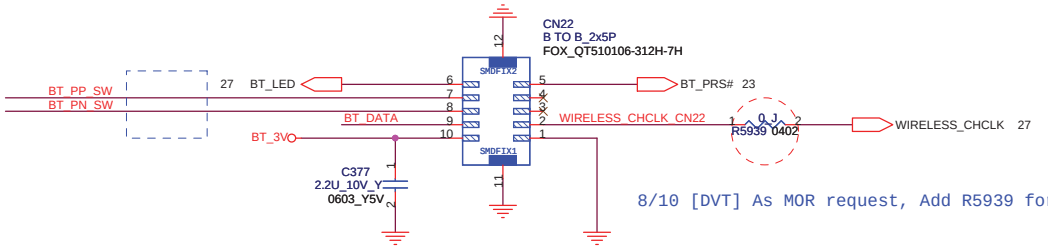
7/15 [DVT] Add Test Point for L6 JIG.(Top-side)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Felica Connector	
Size A	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 37 of 96	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	eDP&LVDS Connector	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 38 of 96	

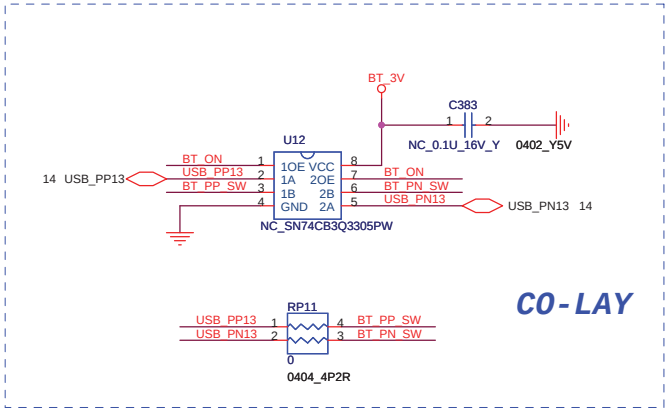


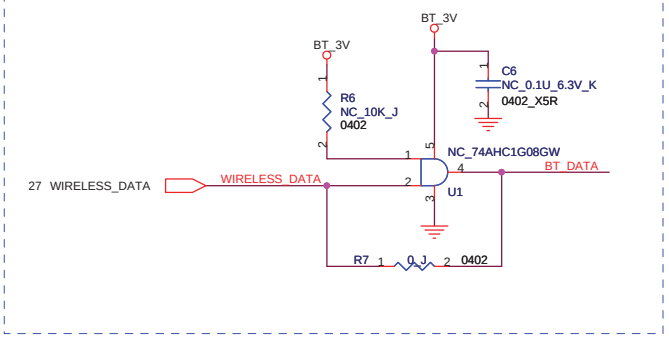


8/10 [DVT] As MOR request, Add R5939 for Clock.

Place C377 close to CN22, Pin10

Bluetooth CONN.





8/10 [DVT] As MOR request, Stuff the R7 Path.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Bluetooth Connector	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 39 of 96	

Co-lay

R863 NC_0_J 0805

F14 1206L025

+3VRUN — +3VRUN_CN2

6V-0.25A_1206

Light Sensor (EC)

11,23,46,64,76 SMB_THRM_DATA
11,23,46,64,76 SMB_THRM_CLK
23 ALS_INT

Switch Keyboard Matrix

23 KSO18
23,41 KSI0
23,41 KSI1
23,41 KSI2
23,41 KSI3
23,41 KSI4
23,41 KSI5
23,41 KSI6
23,41 KSI7

Keyboard LED

NUMLOCK_LED# DB
SCRLOCK_LED# DB
CAPLOCK_LED# DB

Power Button

POWER_LED_DB
SUSPEND_LED_DB
23,25 PWRSW#

+3VRUN_CN2

CN2
FPC CONN_24P
FOX_GB5RF240-1203-7H

Switch DB Conn.

TP385 tpc40b_50 — PWRSW#
TP376 tpc40b_50

Top side ,Closer together

TP462 tpc40b_50 — PWRSW#
TP384 tpc40b_50

Bot side ,Closer together

+3VALW

23 CAPLOCK_LED# — Q77 DTA114YUB null — 23 SCRLOCK_LED# — Q78 DTA114YUB null — 23 NUMLOCK_LED# — Q79 DTA114YUB null

R5740 75_J 0402 — CAPLOCK_LED# DB
R5741 75_J 0402 — SCRLOCK_LED# DB
R5742 75_J 0402 — NUMLOCK_LED# DB

+3VALW

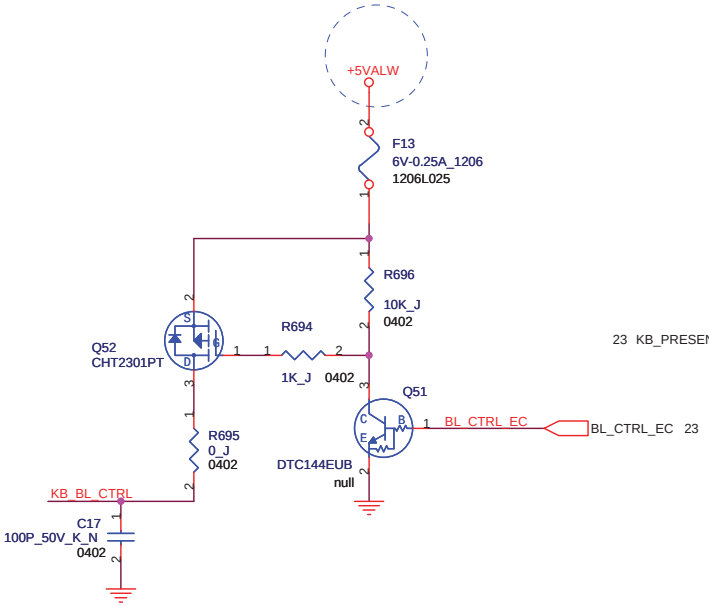
Q80 CHT2301PT
R5743 10K_J 0402
R5745 1K_J 0402
Q82 DTC144EUB null
POWER_LED — POWER_LED 23
POWER_LED_DB

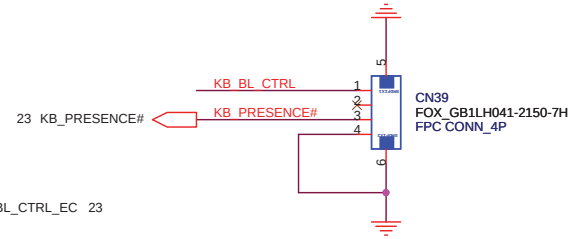
+3VSUS

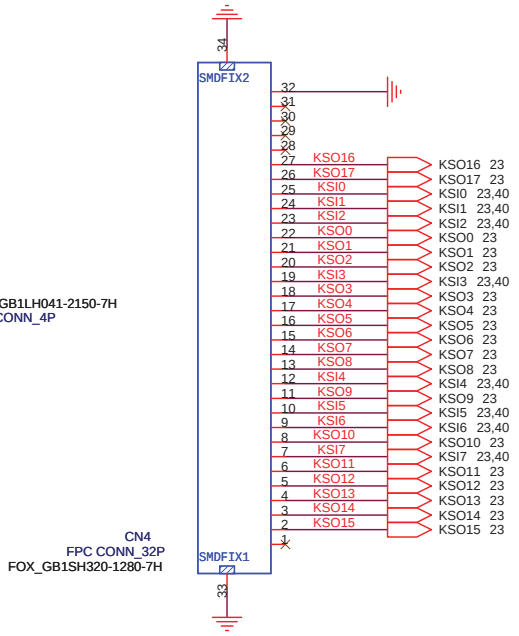
Q81 CHT2301PT
R5744 10K_J 0402
R5746 1K_J 0402
Q83 DTC144EUB null
SUSPEND_LED — SUSPEND_LED 23
SUSPEND_LED_DB

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Switch DB Connector	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 40 of 96	

6/24 [DVT] - EC Engineer Request, for Backlit conctrol well.

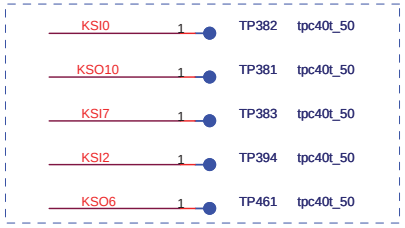




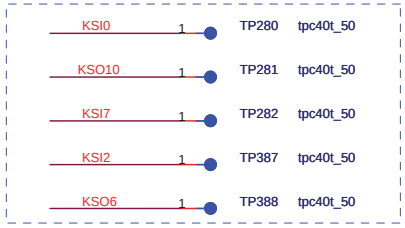


Backlit Power Conn

KBC Conn (Refer to the M780)



7/15 [DVT] Add Test Point for L6 Test JIG. (Bot-side)



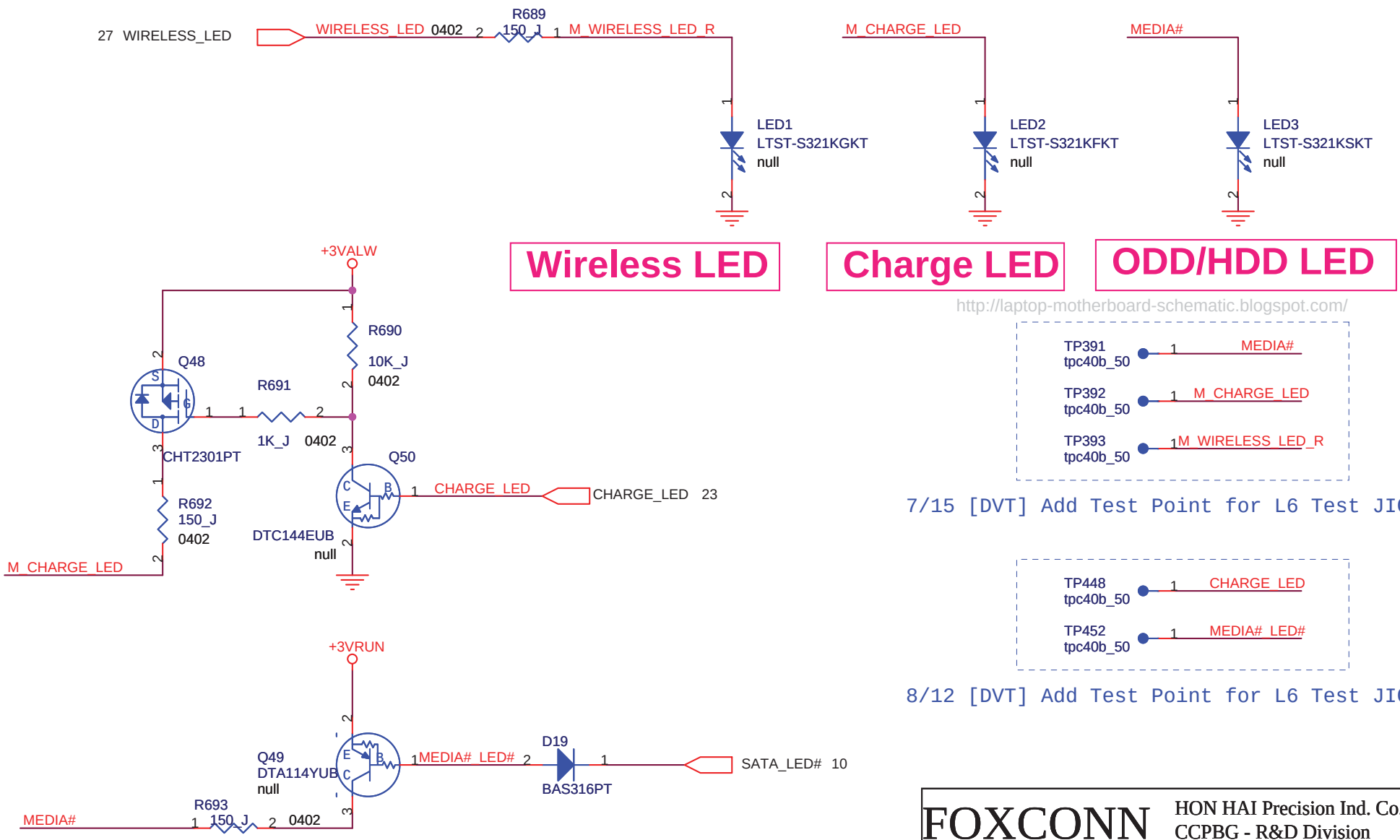
7/15 [DVT] Add Test Point for L6 Test JIG. (Top-side)

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: KB & Backlit Connector

Size: B | Document Number: M930 (MBX-215) | Rev: SB

Date: Wednesday, August 12, 2009 | Sheet 41 of 96



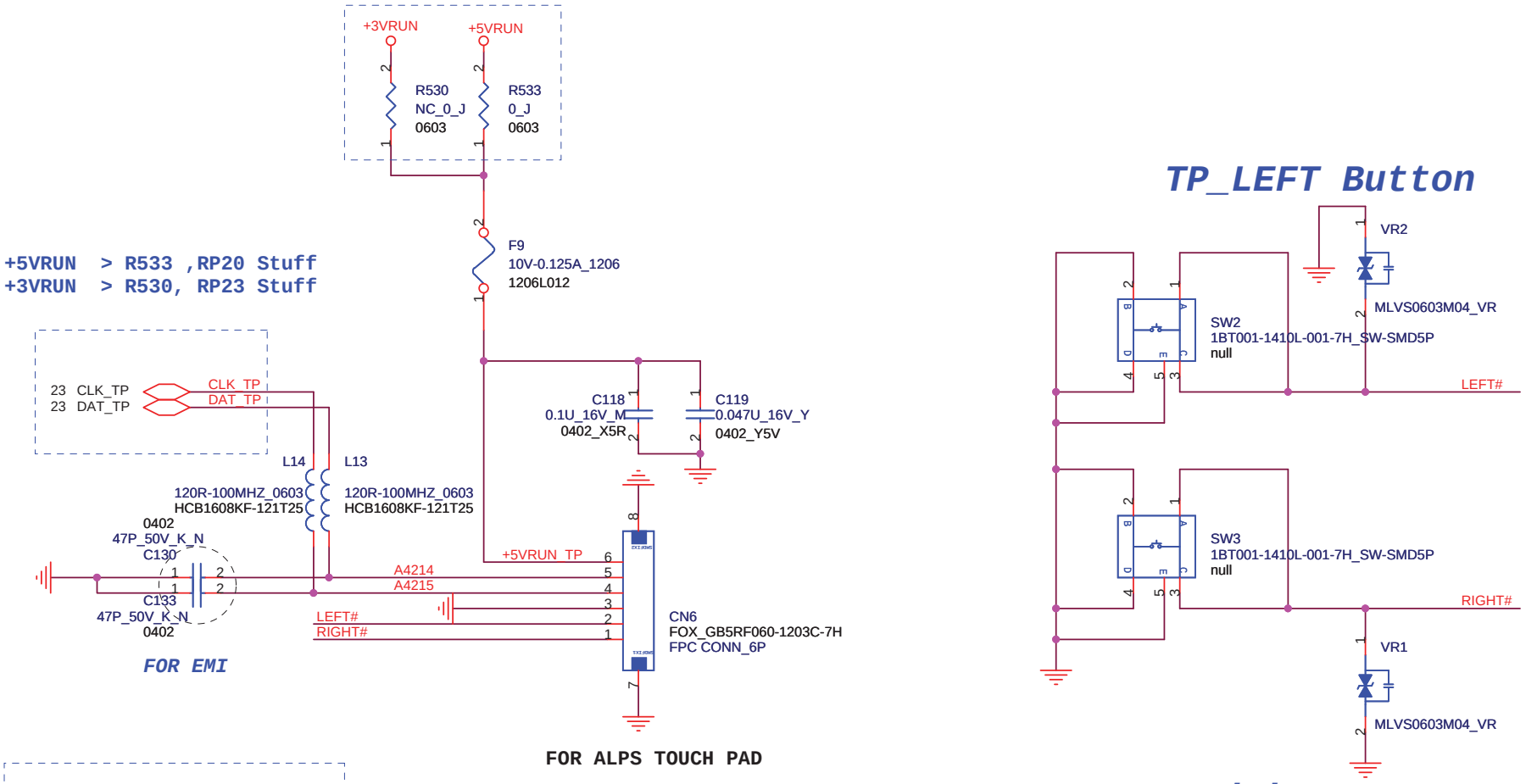
TP391 tpc40b_50 — MEDIA#
TP392 tpc40b_50 — M_CHARGE_LED
TP393 tpc40b_50 — M_WIRELESS_LED_R

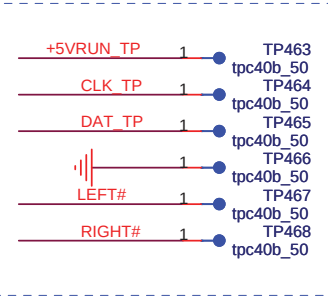
7/15 [DVT] Add Test Point for L6 Test JIG.

TP448 tpc40b_50 — CHARGE_LED
TP452 tpc40b_50 — MEDIA# LED#

8/12 [DVT] Add Test Point for L6 Test JIG.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Status LED**	
Size: A	Document Number: **M930 (MBX-215)**	Rev: **SB**
Date: Wednesday, August 12, 2009	Sheet 42 of 96	

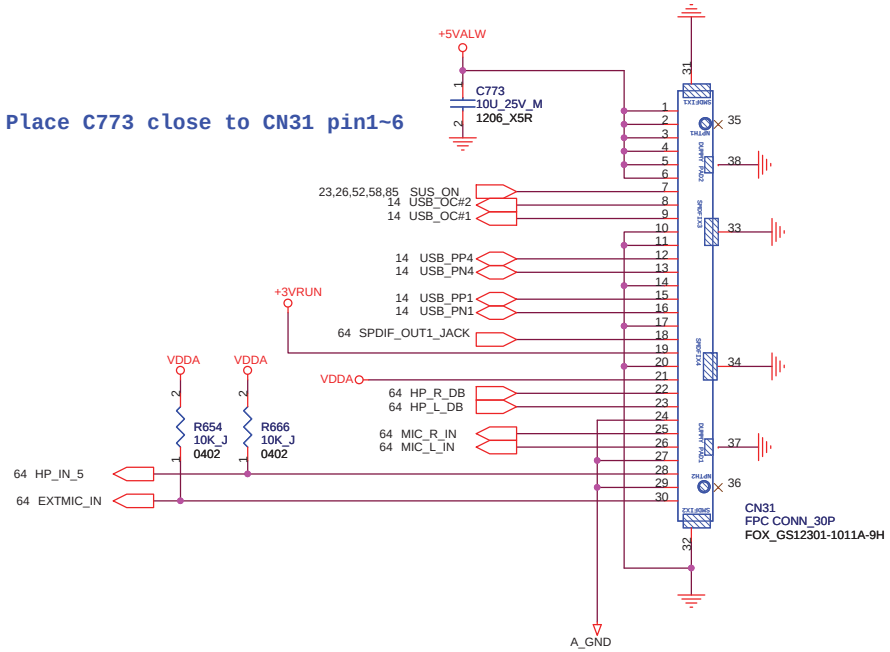




Touch Pad Conn (Support Multi Touch)

7/15 [DVT] Add Test Point for L6 JIG.(Bot-side)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Touch Pad		
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 43 of 96	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	*Audio/USB DB Conn.*	
Size A3	Document Number *M930 (MBX-215)*	Rev *SB*
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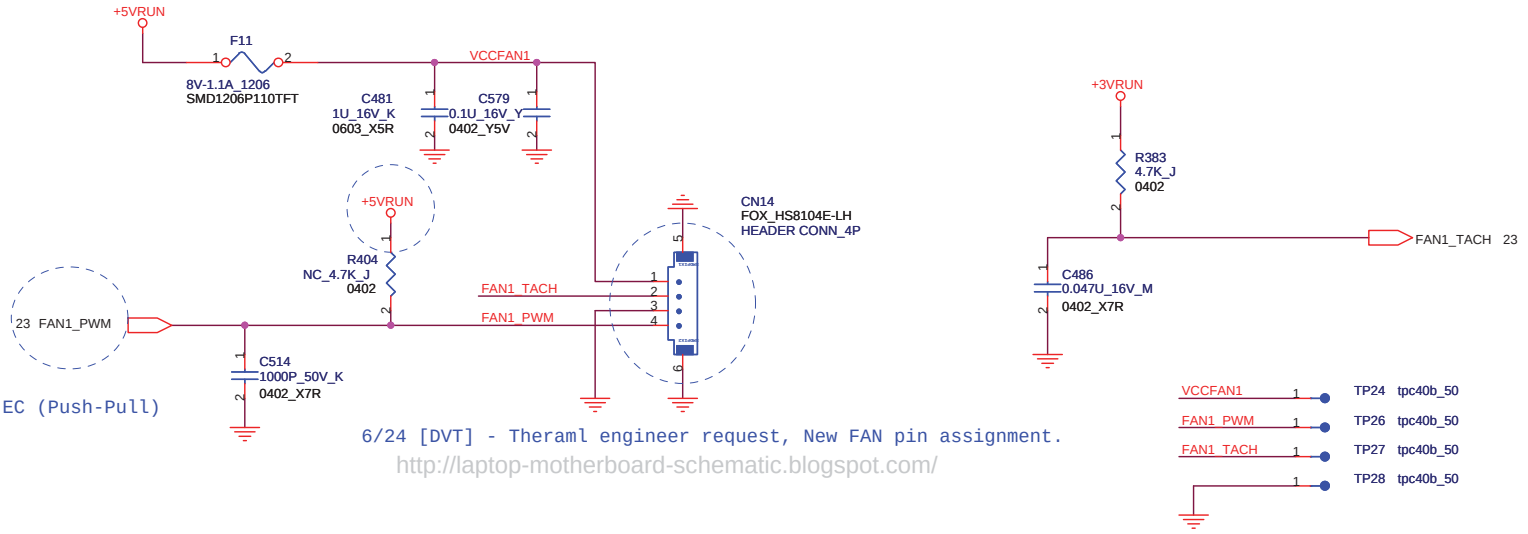
Direct PWM FAN

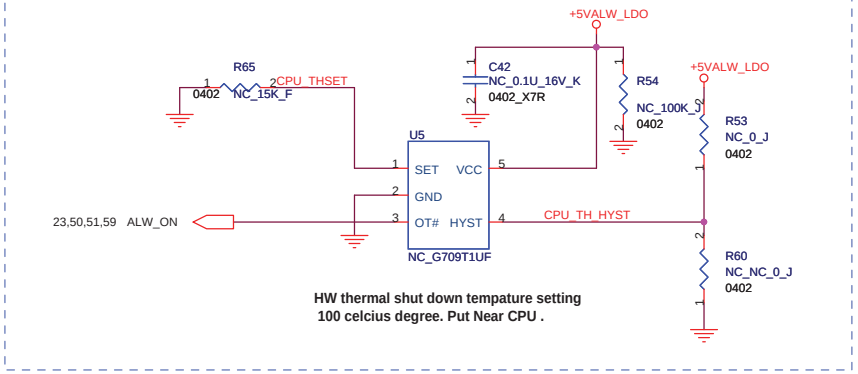


7/7 [DVT] - Direct FAN Drive from EC (Push-Pull)

6/24 [DVT] - Theraml engineer request, New FAN pin assignment.

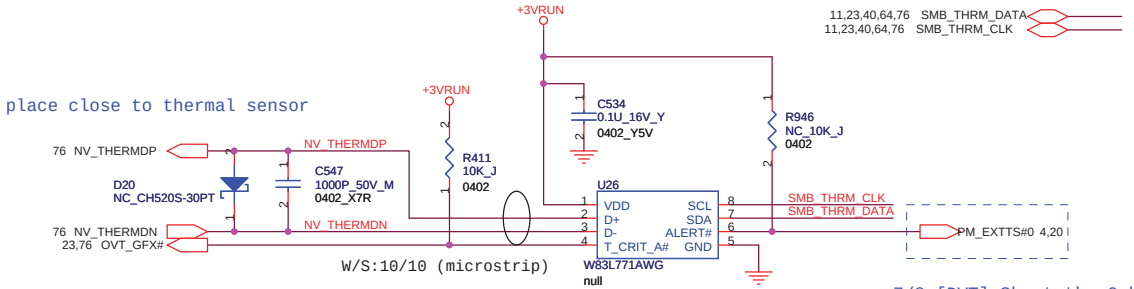
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: FAN		
Size: B	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 45 of 96	

HW THERMAL PROTECTION



7/8 [DVT] Dummy the HW Thermal Protection for C/D.

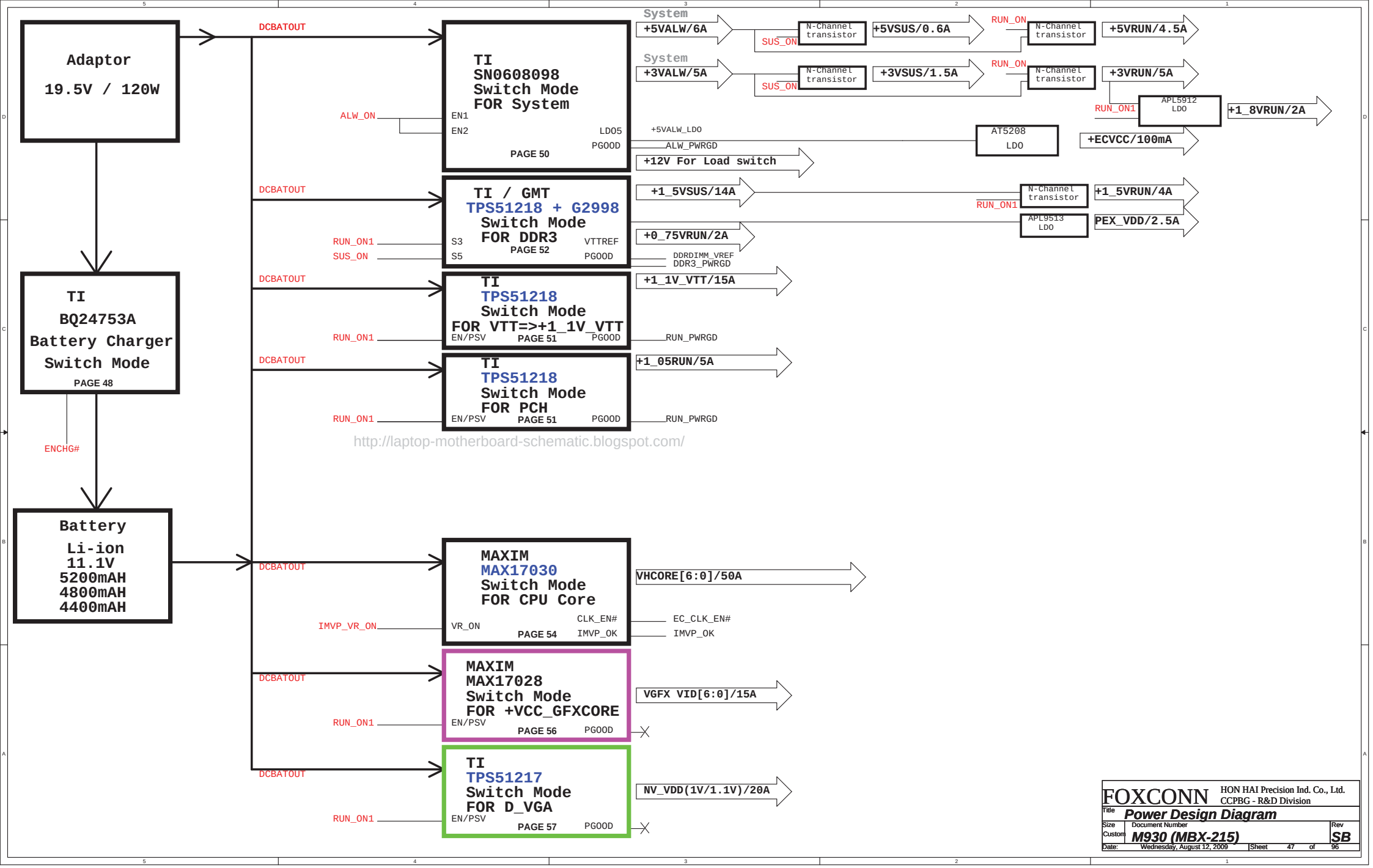
VGA Thermal SENSOR
W83L771AWG



7/8 [DVT] Short the 0ohm ,Change the Net Name.

Place Thermal-Sensor near VGA

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Thermal Sensor & Protection	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 46 of 96	


Adaptor
19.5V / 120W
TI
BQ24753A
Battery Charger
Switch Mode
PAGE 48
ENCHG#
Battery
Li-ion
11.1V
5200mAH
4800mAH
4400mAH
DCBATOUT
TI
SN0608098
Switch Mode
FOR System
ALW_ON
EN1
EN2
LDO5
PGOOD
PAGE 50
System
+5VALW/6A
SUS_ON
N-Channel transistor
+5VSUS/0.6A
RUN_ON
N-Channel transistor
+5VRUN/4.5A
System
+3VALW/5A
SUS_ON
N-Channel transistor
+3VSUS/1.5A
RUN_ON
N-Channel transistor
+3VRUN/5A
RUN_ON1
APL5912 LDO
+1_8VRUN/2A
+5VALW_LDO
AT5208 LDO
+ECVCC/100mA
ALW_PWRGD
+12V For Load switch
TI / GMT
TPS51218 + G2998
Switch Mode
FOR DDR3
RUN_ON1
SUS_ON
S3
S5
VTTREF
PGOOD
PAGE 52
+1_5VSUS/14A
N-Channel transistor
RUN_ON1
+1_5VRUN/4A
APL9513 LDO
PEX_VDD/2.5A
+0_75VRUN/2A
DDRDIMM_VREF
DDR3_PWRGD
TI
TPS51218
Switch Mode
FOR VTT=>+1_1V_VTT
RUN_ON1
EN/PSV
PGOOD
PAGE 51
+1_1V_VTT/15A
RUN_PWRGD
TI
TPS51218
Switch Mode
FOR PCH
RUN_ON1
EN/PSV
PGOOD
PAGE 51
+1_05RUN/5A
RUN_PWRGD
http://laptop-motherboard-schematic.blogspot.com/
MAXIM
MAX17030
Switch Mode
FOR CPU Core
IMVP_VR_ON
VR_ON
CLK_EN#
IMVP_OK
PAGE 54
VHCORE[6:0]/50A
EC_CLK_EN#
IMVP_OK
MAXIM
MAX17028
Switch Mode
FOR +VCC_GFXCORE
RUN_ON1
EN/PSV
PGOOD
PAGE 56
VGFX VID[6:0]/15A
TI
TPS51217
Switch Mode
FOR D_VGA
RUN_ON1
EN/PSV
PGOOD
PAGE 57
NV_VDD(1V/1.1V)/20A
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
Power Design Diagram
Size
Custom
Document Number
M930 (MBX-215)
Rev
SB
Date:
Wednesday, August 12, 2009
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47
of
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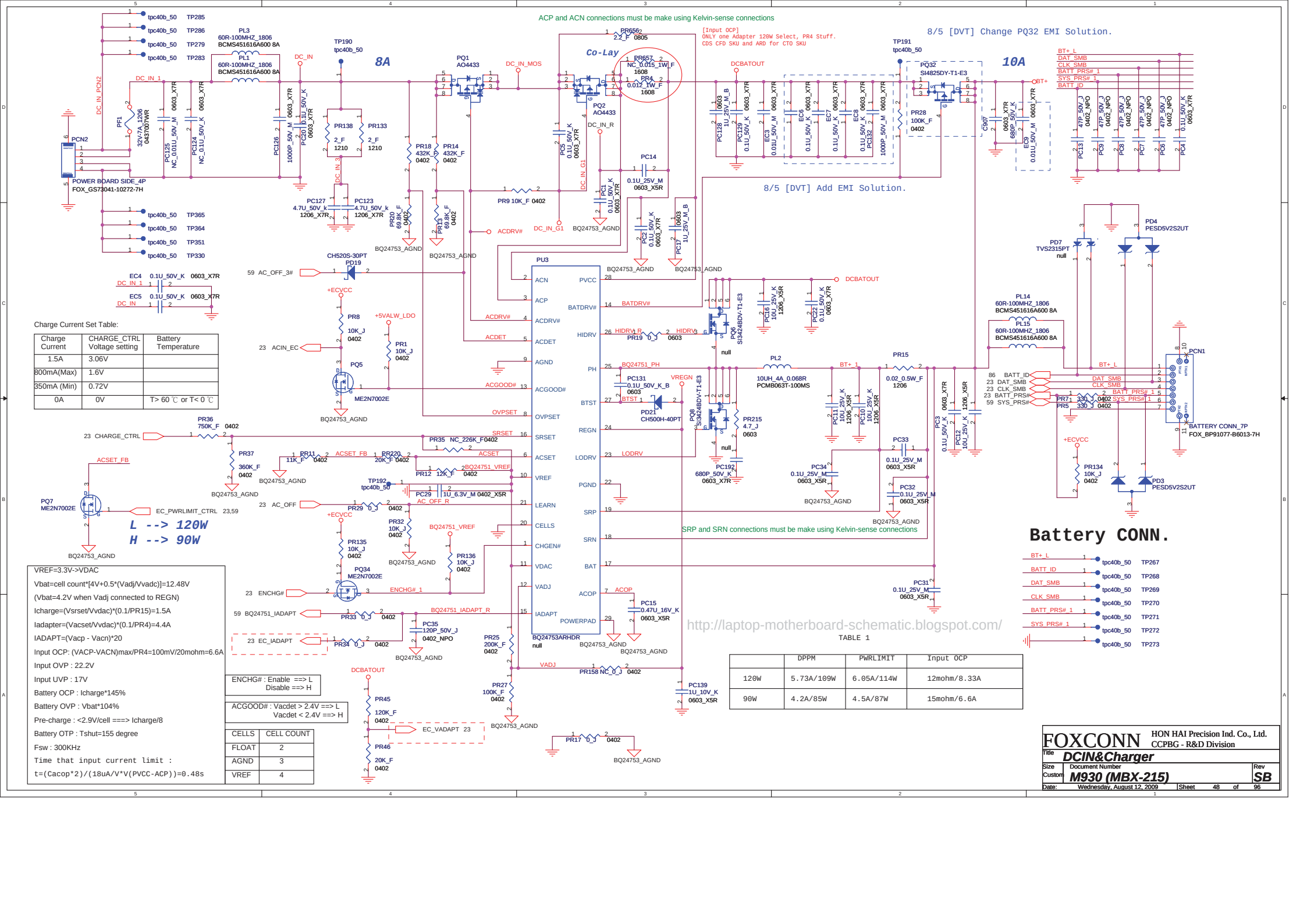
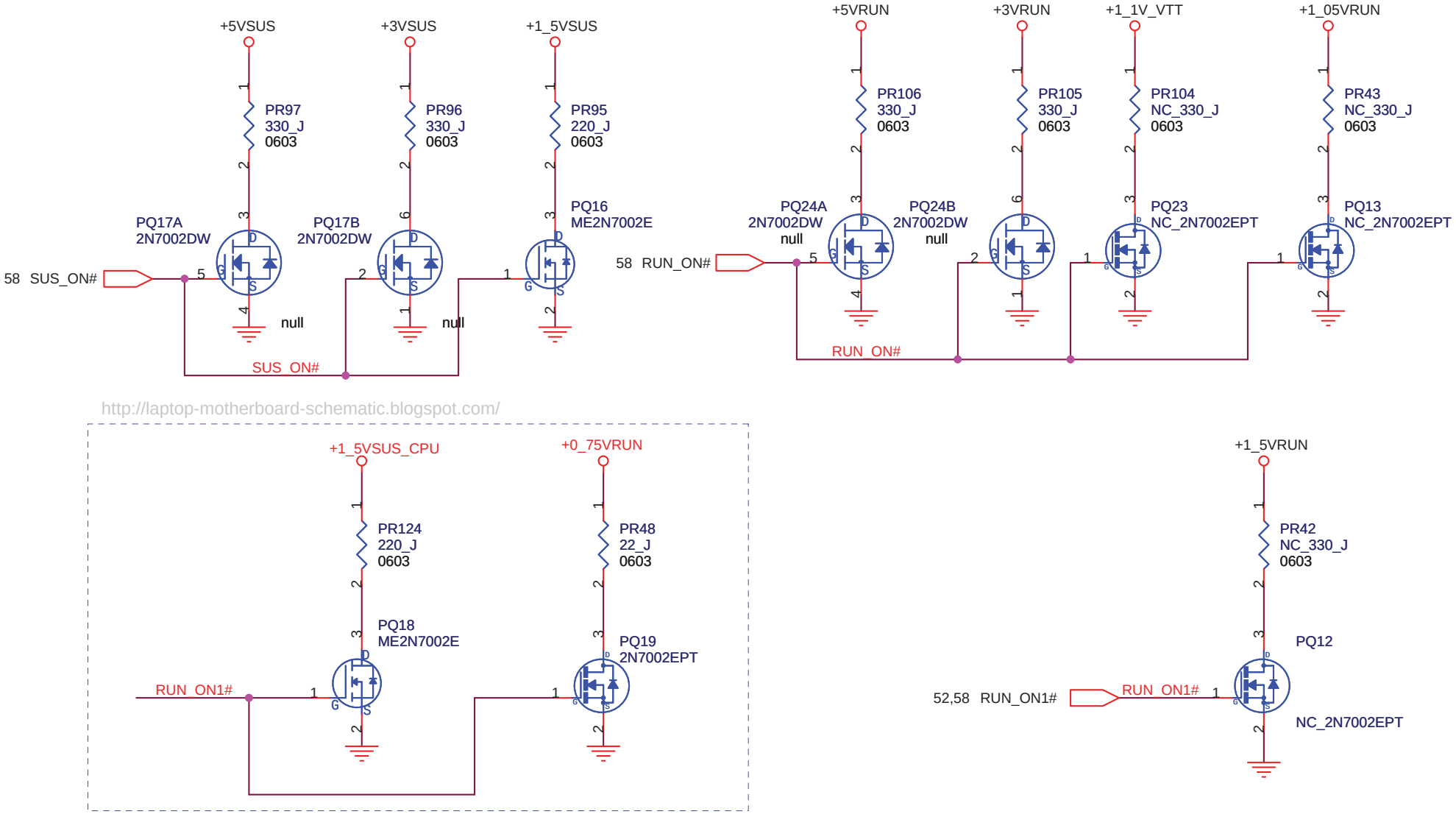


Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
800mA(Max)	1.6V	
350mA (Min)	0.72V	
0A	0V	T> 60 ℃ or T< 0 ℃

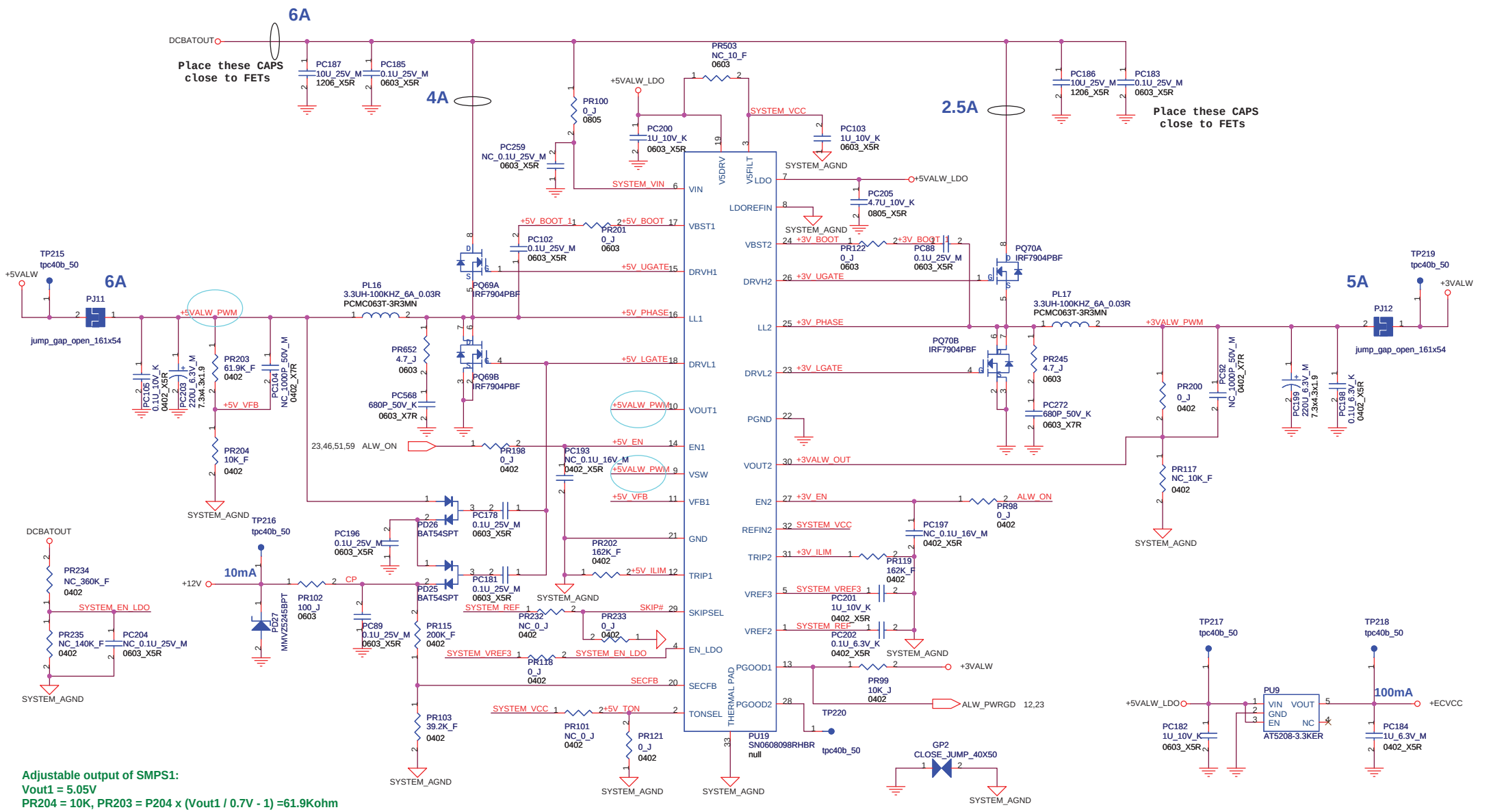
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

	DPPM	PWRLIMIT	Input OCP
120W	5.73A/109W	6.05A/114W	12mohm/8.33A
90W	4.2A/85W	4.5A/87W	15mohm/6.6A



7/24 [DVT] INTEL S3 Power Reduction Solution.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**DISCHARGE CIRCUIT**	
Size A	Document Number **M930 (MBX-215)**	Rev **SB**
Date: Wednesday, August 12, 2009	Sheet 49 of 96	



Adjustable output of SMPS1:
Vout1 = 5.05V
PR204 = 10K, PR203 = P204 x (Vout1 / 0.7V - 1) =61.9Kohm

Second Feedback :
Vout_sec = 12V, PR103 = 20Kohm
PR115 = PR103 x (Vout_sec / 2V - 1) =100Kohm

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

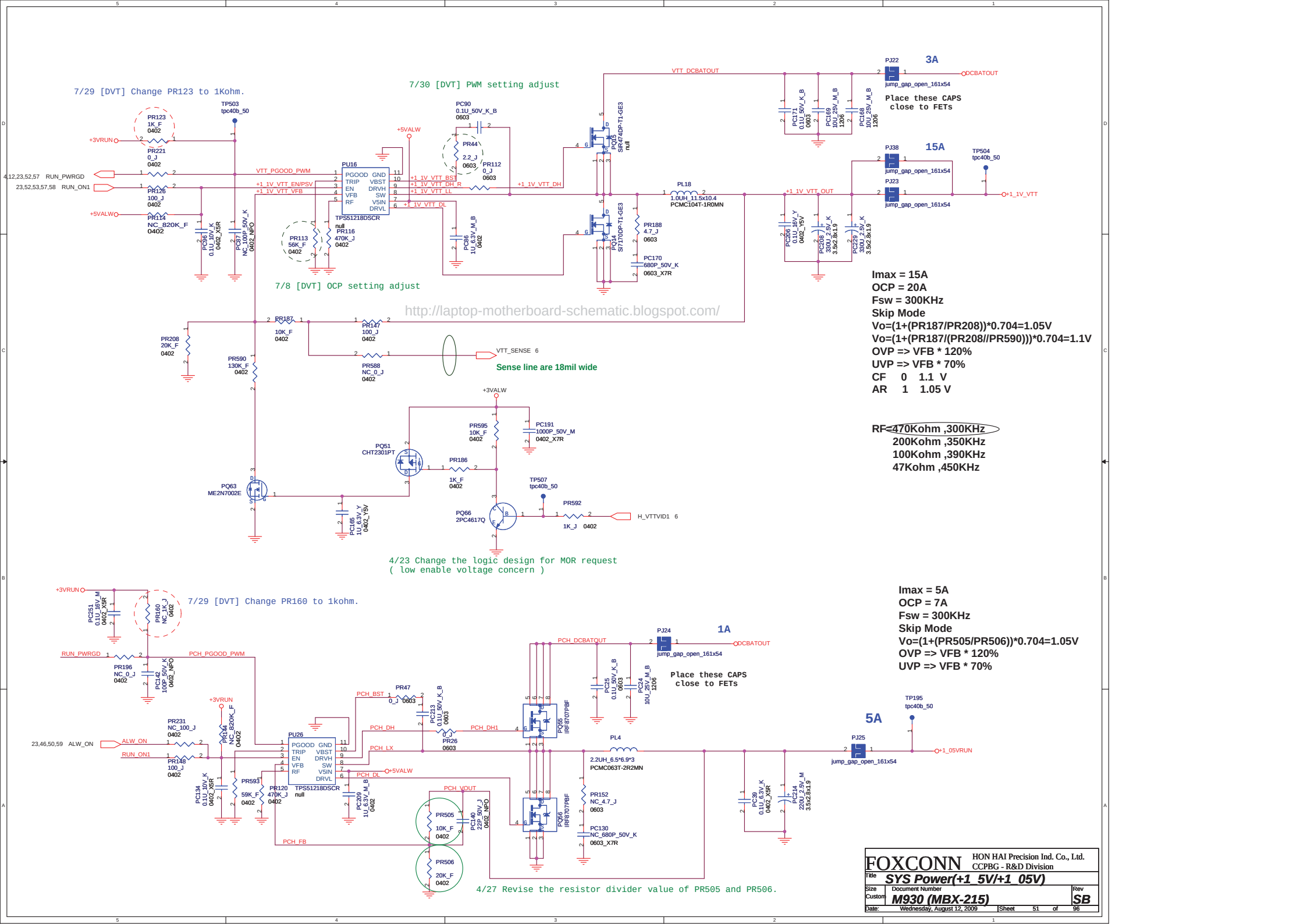
L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u
+5VALW=((PR186/PR188)+1)*VFB1

Current limit resistor for SMPS1 :
Ivalley_5 = 5.775A, Rcs_5 = Rds1 = 10.8mohm
PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

Current limit resistor for SMPS2 :
Ivalley_3 = 5.525A, Rcs_3 = Rds2 = 10.8mohm
PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	SYS Power (+3_3V/+5V)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 50 of 96	


7/29 [DVT] Change PR123 to 1Kohm.
7/30 [DVT] PWM setting adjust
7/8 [DVT] OCP setting adjust
http://laptop-motherboard-schematic.blogspot.com/
Sense line are 18mil wide
4/23 Change the logic design for MOR request
(low enable voltage concern)
7/29 [DVT] Change PR160 to 1kohm.
4/27 Revise the resistor divider value of PR505 and PR506.
Place these CAPS close to FETs
Place these CAPS close to FETs
3A
15A
1A
5A
Imax = 15A
OCP = 20A
Fsw = 300KHz
Skip Mode
Vo=(1+(PR187/PR208))*0.704=1.05V
Vo=(1+(PR187/(PR208//PR590)))*0.704=1.1V
OVP => VFB * 120%
UVP => VFB * 70%
CF 0 1.1 V
AR 1 1.05 V
RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz
Imax = 5A
OCP = 7A
Fsw = 300KHz
Skip Mode
Vo=(1+(PR505/PR506))*0.704=1.05V
OVP => VFB * 120%
UVP => VFB * 70%
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
SYS Power(+1_5V/+1_05V)
M930 (MBX-215)
SB
Wednesday, August 12, 2009
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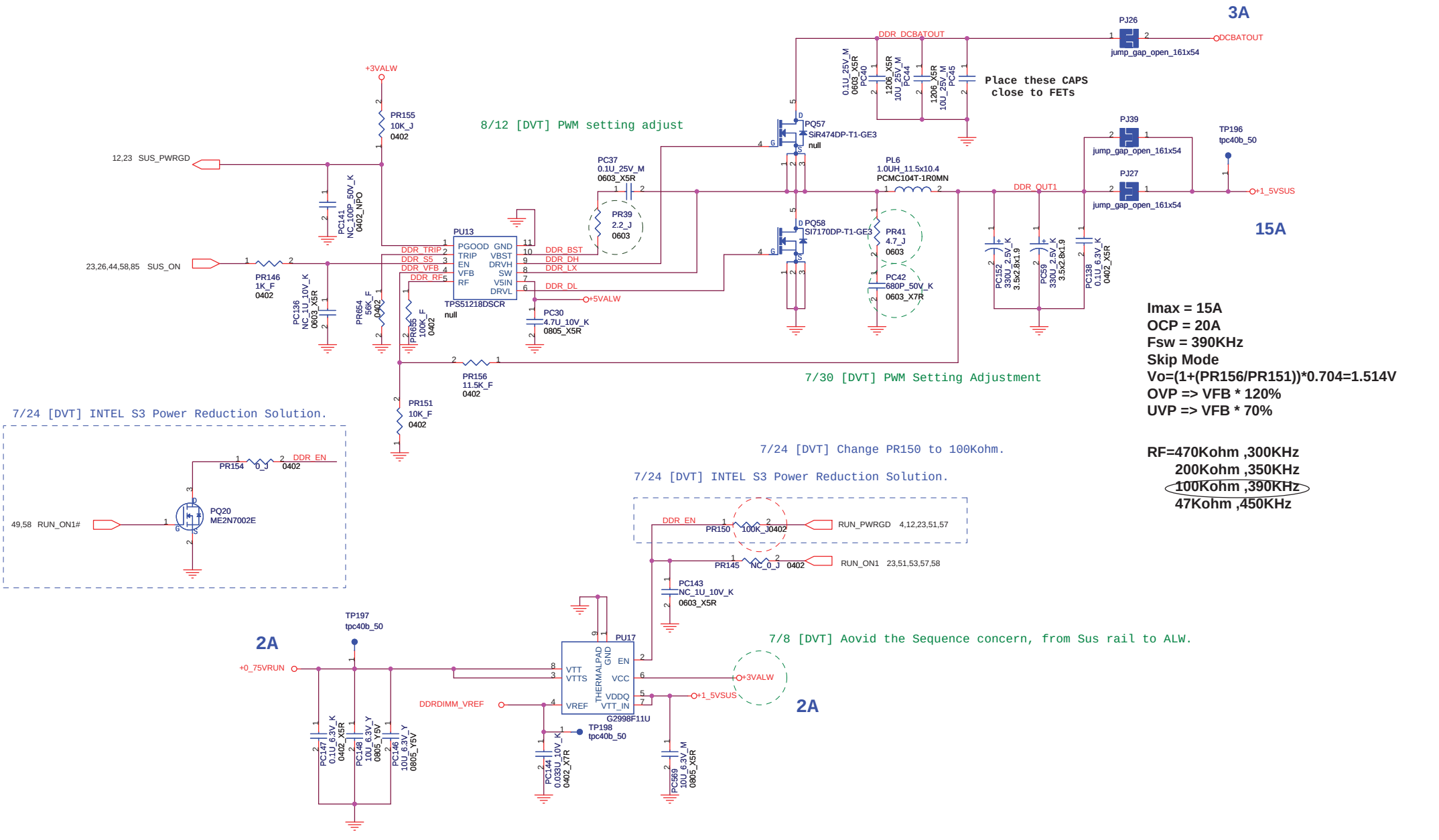
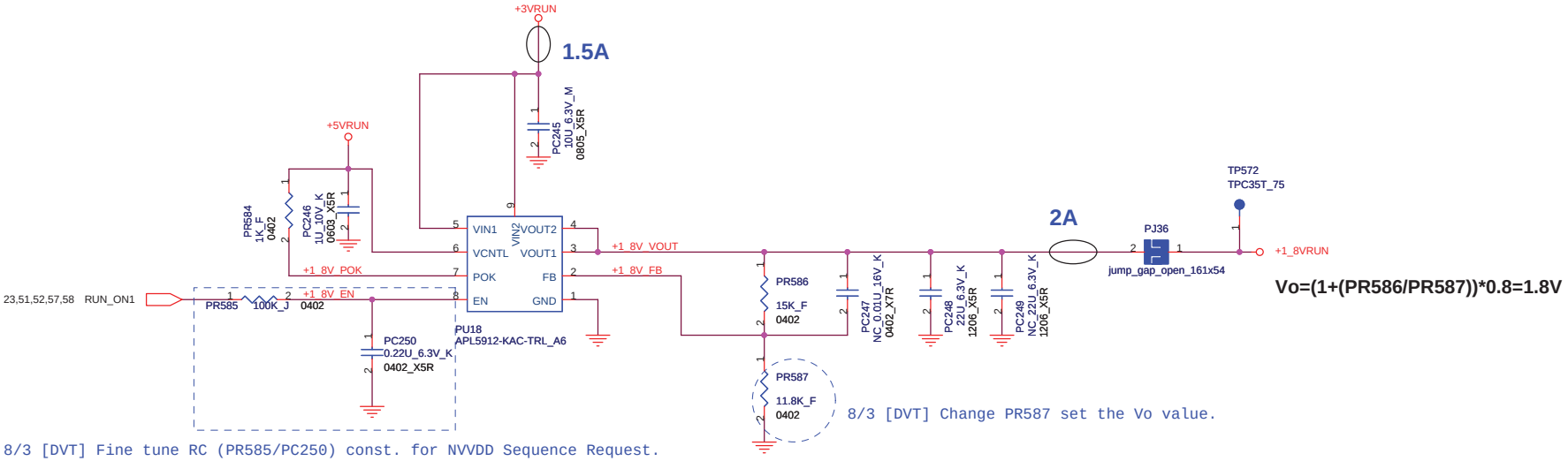


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	DDR3 Power(+1_5V/+0_75V)		
Size A3	Document Number M930 (MBX-215)		Rev SB
Date: Wednesday, August 12, 2009	Sheet 52 of 96		

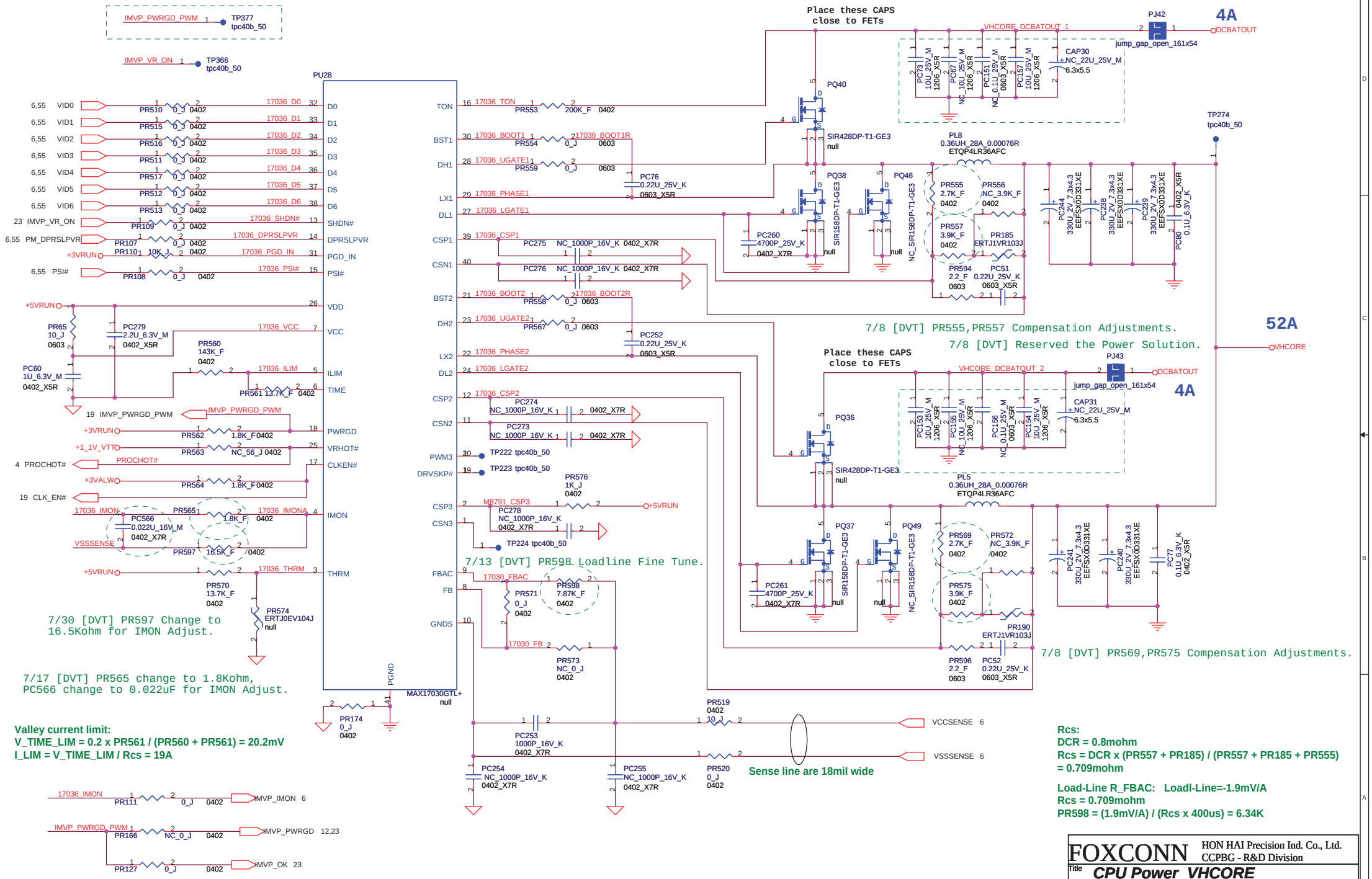


Vo=(1+(PR586/PR587))*0.8=1.8V

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_8V)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 53 of 96	

7/13 [DVT] For L6 Power Test Station usage (Top-side)

7/8 [DVT] Reserved the Power Solution.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	CPU Power_VHCORE
Size A3	Document Number M930 (MBX-215) Rev SB
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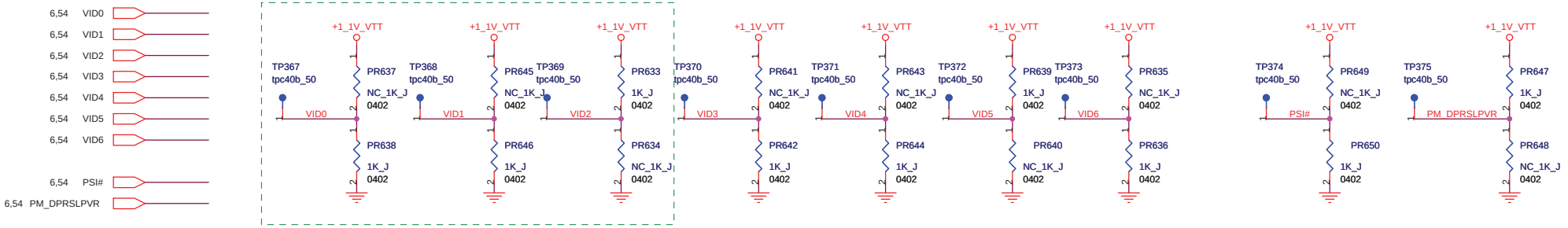
Default value of VID [6:0] = [0100100] , PSI# = 0 , PROC_DPRSLPVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)
- 416056_416056_Ard_EDS_Rev.1.1
- 403779_Clarksfield_MPG_Rev1.5



7/8 [DVT] Follow the ARD/CFD EDS Setting to set as SV type.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CPU Power_VID	
Size A3	Document Number M930 (MBX-215)	Rev SB
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Delete iGPU Path on DVT for Cost Down

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: VGFX Power_GFXCORE		
Size: A3	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 56 of 96	

7/29 [DVT] Change PR176 to 1Kohm.

7/8 [DVT] PWM setting adjustment

Place these CAPS close to FETs

3A

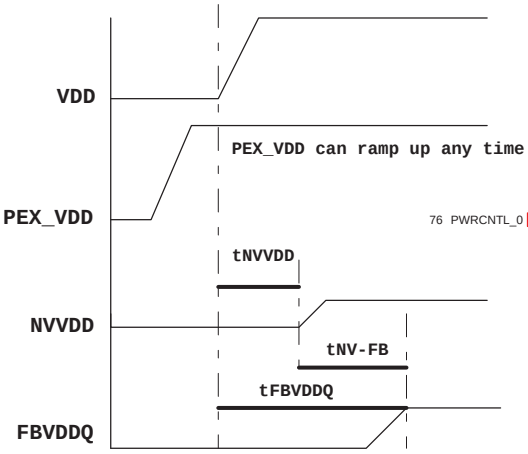
15A

7/8 [DVT] OCP setting adjustment

7/8 [DVT] PWM setting adjustment

Sense line are 18mil wide

Imax = 15A
OCP = 20A
Fsw = 400KHz
Skip Mode
Vo=(1+(PR550/(PR551//PR210)))*0.6
OVP => VFB * 120%
UVP => VFB * 70%



Recommended Power sequencing order

Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

N11P-GE1

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.8V (P12)
0	1	0.85V (P8)
1	0	0.95V (P0)

8/3 [DVT] Revise the Table for DVT.

N11M-GE1

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.8V (P12)
0	1	0.85V (P8)
1	0	1.03V (P0)

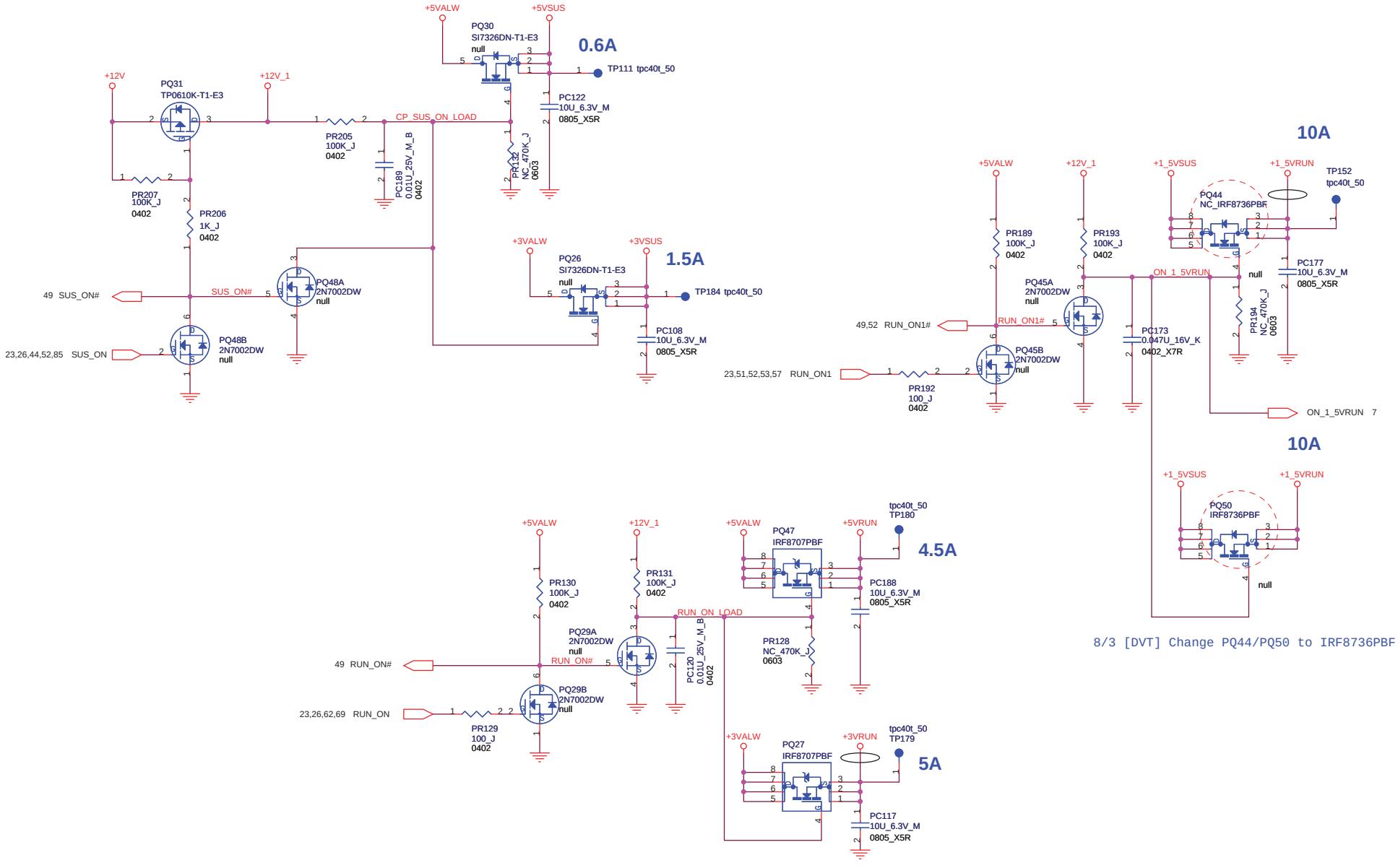
7/13 [DVT] Add the TP221/TP248

7/8 [DVT] PR222, PR229 Feedback Loop Adjustment

2.5A

Vo=(1+(PR222/PR229))*0.8=1.05V

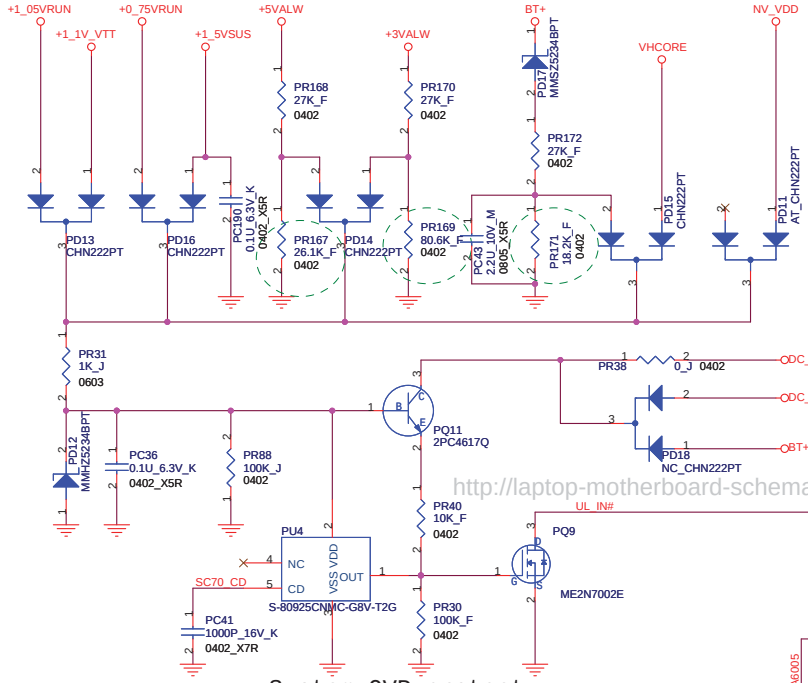
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	VGA_Power (NV_VDD)
Size A3	Document Number M930 (MBX-215) Rev SB
Date: Wednesday, August 12, 2009	Sheet 57 of 96



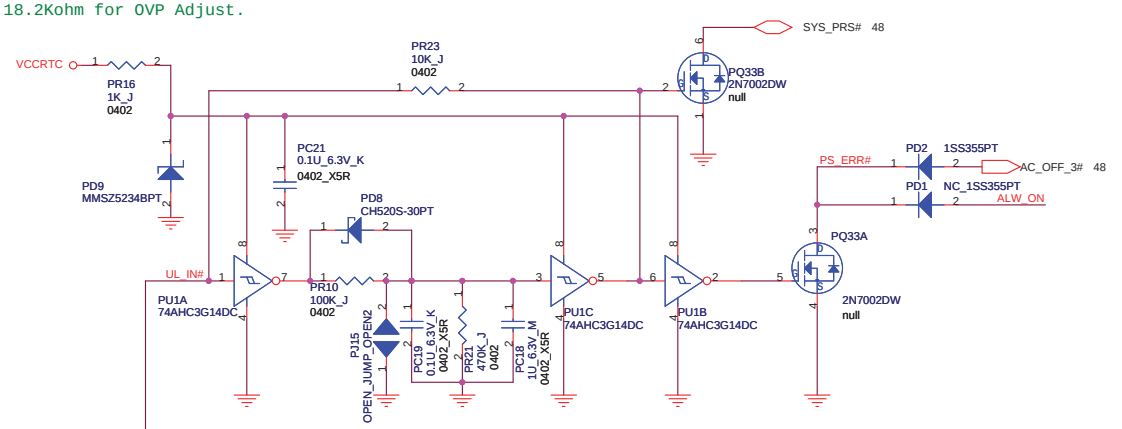
8/3 [DVT] Change PQ44/PQ50 to IRF8736PBF.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Others power plan		
Size: A3	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 58 of 96	

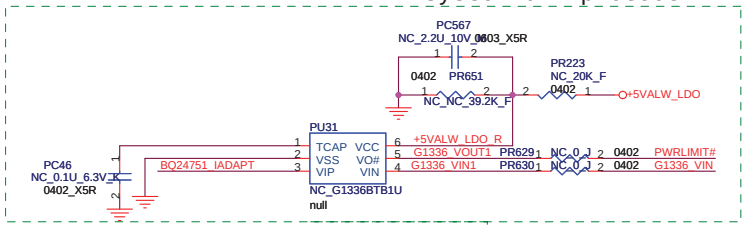
7/17 [DVT] PR167 change to 26.1Kohm, PR169 change to 80.6Kohm ,PR171 change to 18.2Kohm for OVP Adjust.

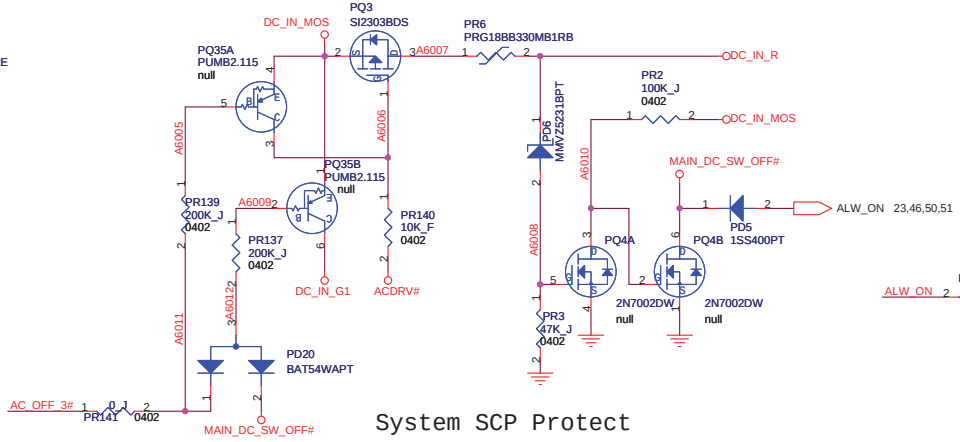


System OVP protect

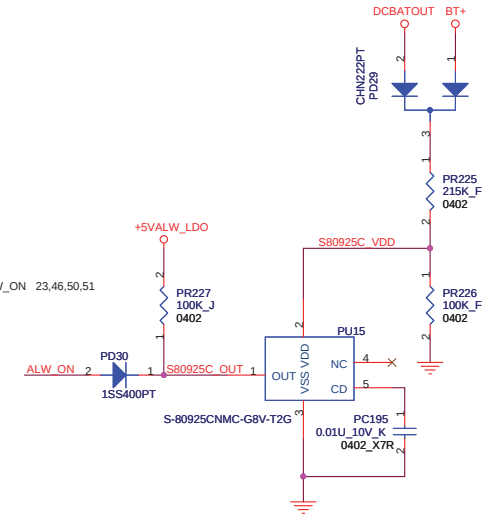


PJ15 Near the DDR socket door



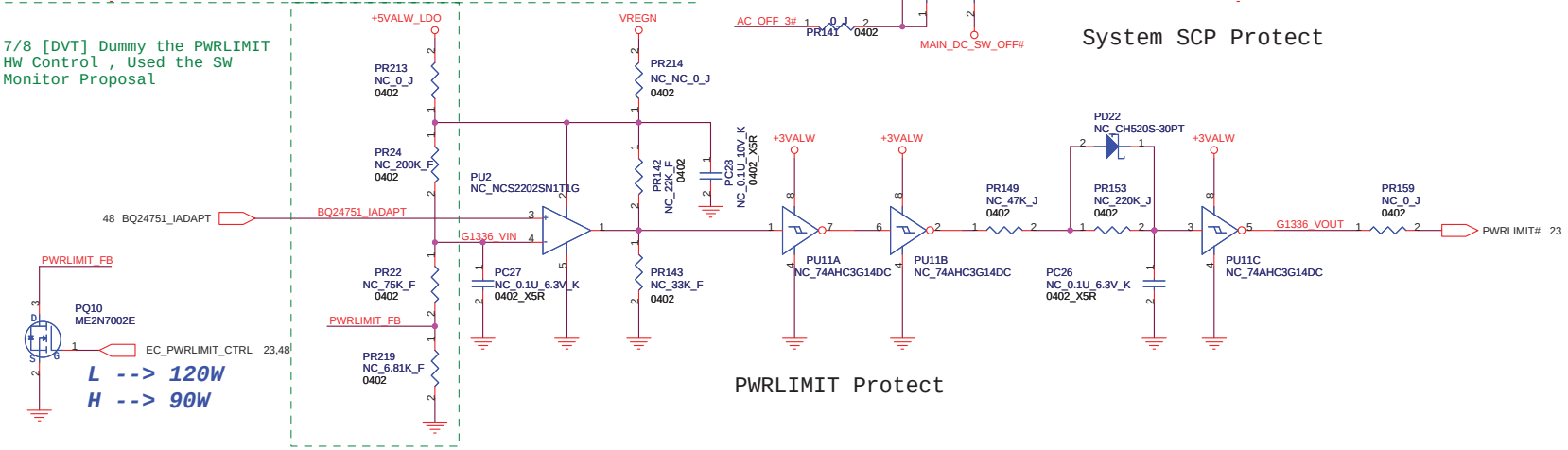


System SCP Protect



Battery UVP Protect

7/8 [DVT] Dummy the PWRLIMIT HW Control , Used the SW Monitor Proposal



PWRLIMIT Protect

VIINP	90W adaptor	120W adaptor
PWRLIMIT	4.5A 87W	6.05A 114W

adapter max load : 5.7A/3000ms
adapter OCP : 7.5Amax

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: OVP protection

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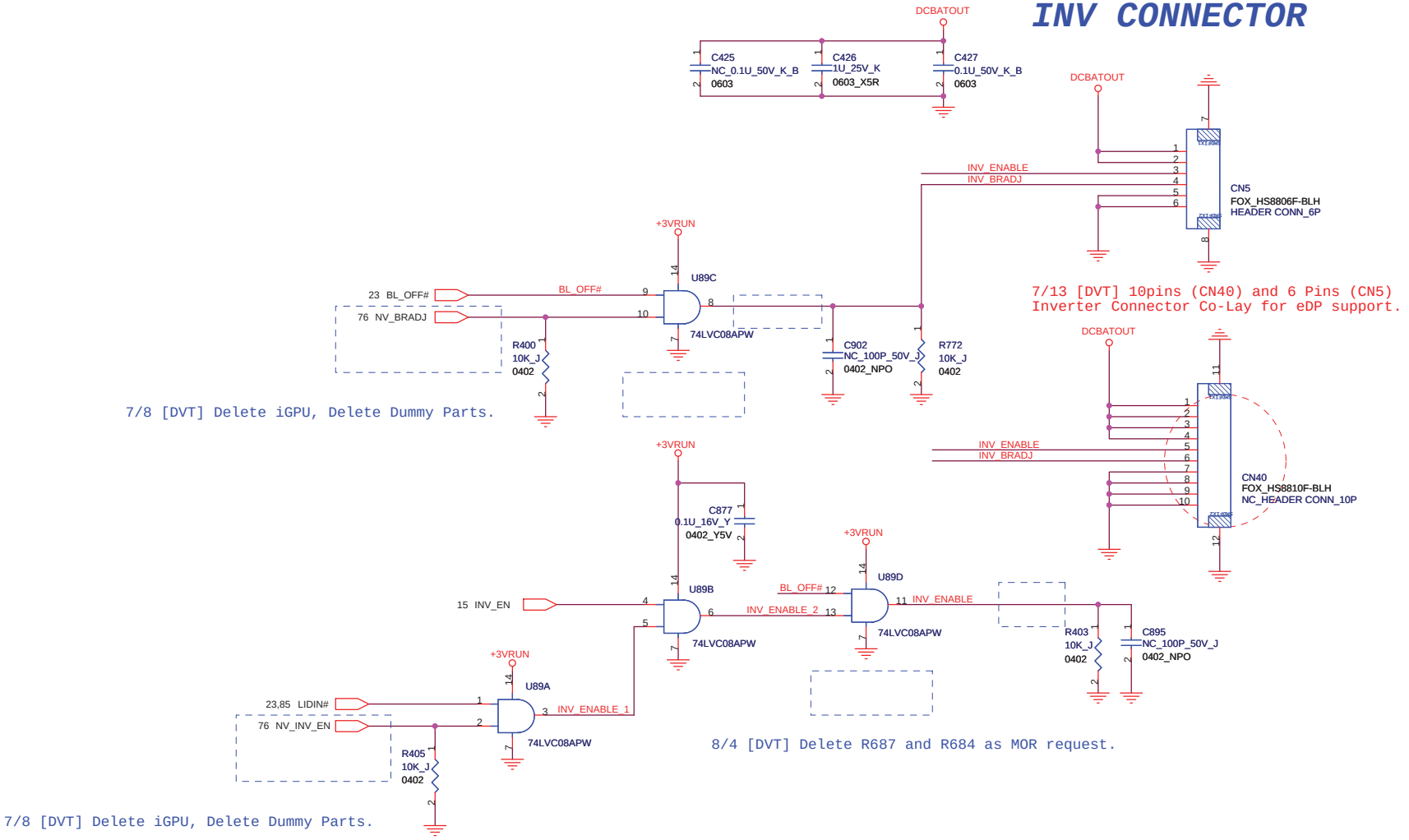
INV CONNECTOR



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	INV CONNECTOR	
Size A3	Document Number M930 (MBX-215)	Rev SB
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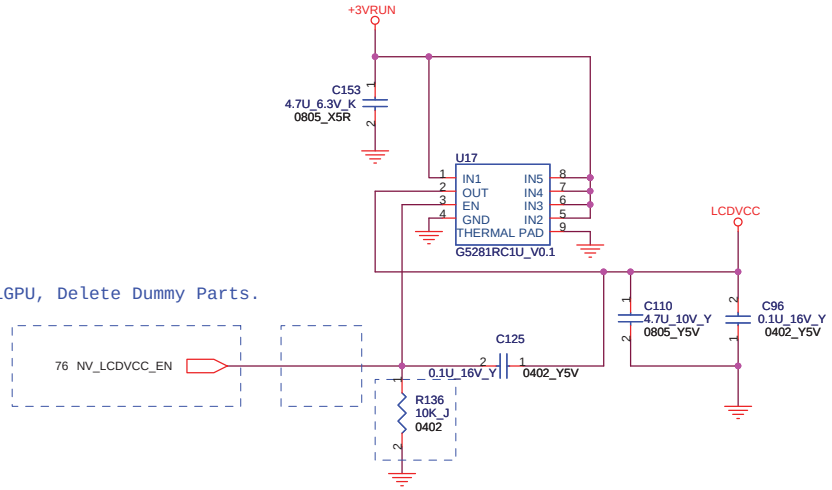
LCDVCC Power

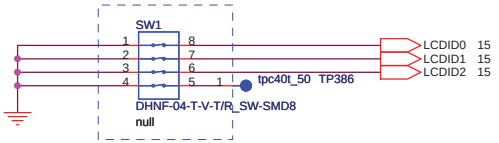


7/8 [DVT] Delete iGPU, Delete Dummy Parts.

7/15 [DVT] Delete U46 to fix the DISPLAY OFF function issue.

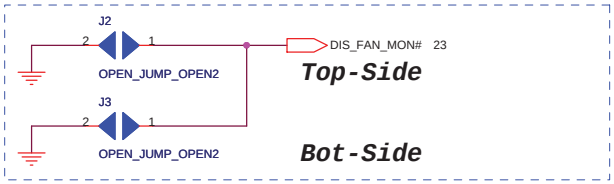
7/15 [DVT] Change R136 from 100Kohm to 10Kohm.

PANEL ID



SW1 (Panel ID)	LCDID2	LCDID1	LCDID0
CRT (No LCD)	0	0	0
EW1 (Sharp)	0	0	1
EW1 (AUO)	0	1	0
EW1 (LGD)	0	1	1
EW3 (Sharp)	1	0	0
RESERVED	1	0	1
RESERVED	1	1	0
RESERVED	1	1	1

ON:0 , OFF:1



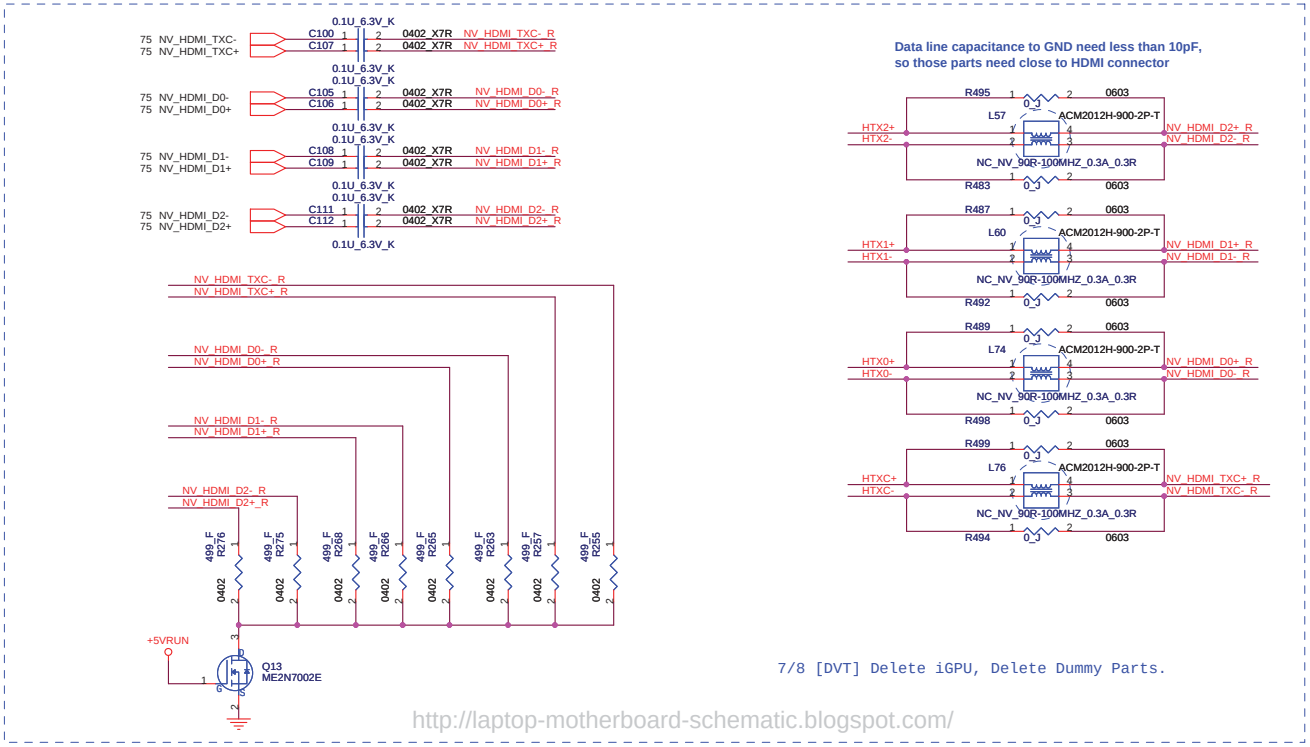
DIS_FAN_MON# for L6 BFT Test

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: LVDS(Panel ID/PWR)

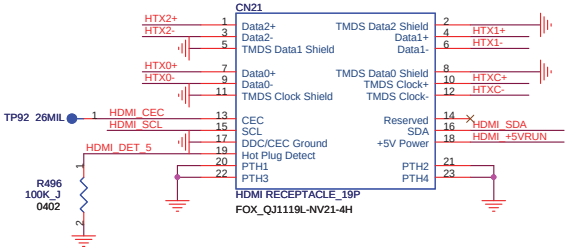
Size: A3 | Document Number: M930 (MBX-215) | Rev: SB

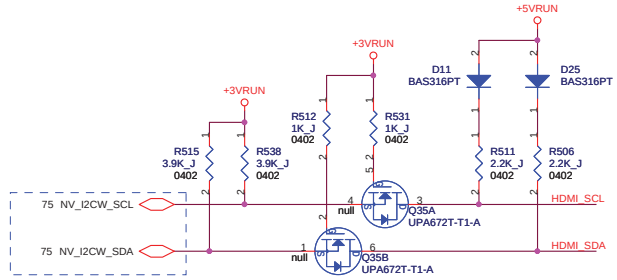
Date: Wednesday, August 12, 2009 | Sheet 61 of 96



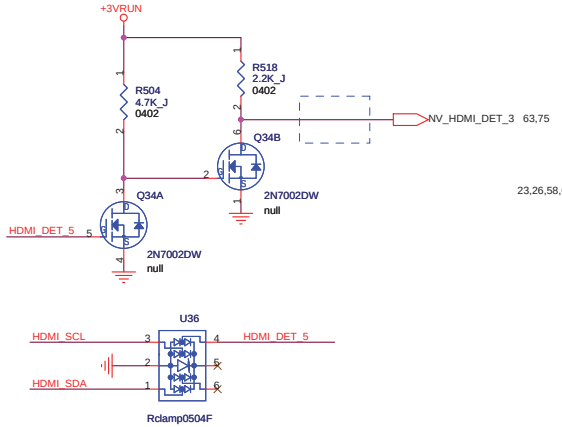
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

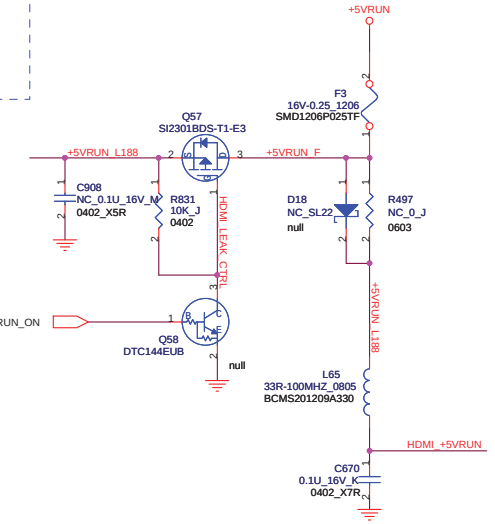
7/8 [DVT] Delete iGPU, Delete Dummy Parts.





7/8 [DVT] Delete iGPU, Change the Net name.





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA (STRAP) 2 OF 6	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
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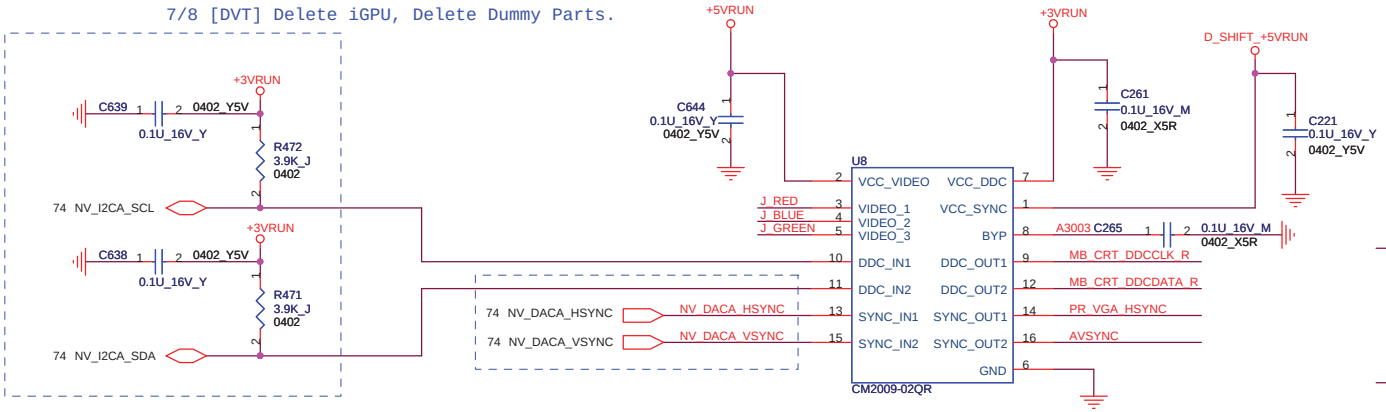
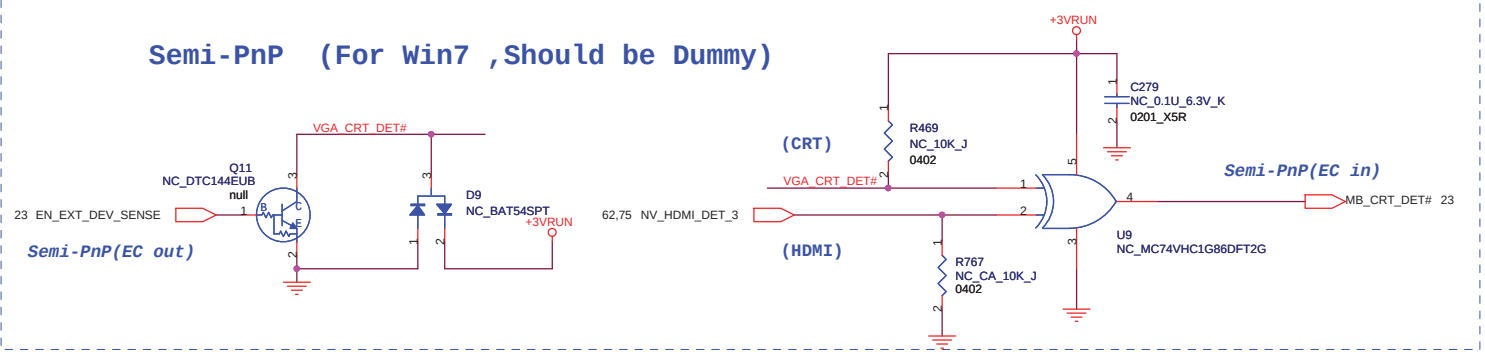
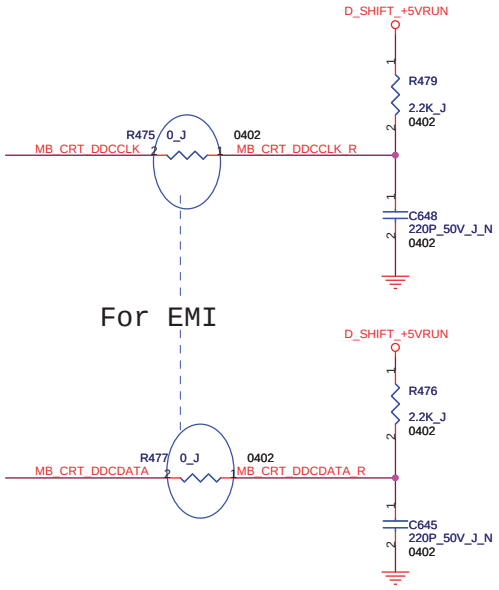
7/8 [DVT] Delete iGPU, Delete Dummy Parts.



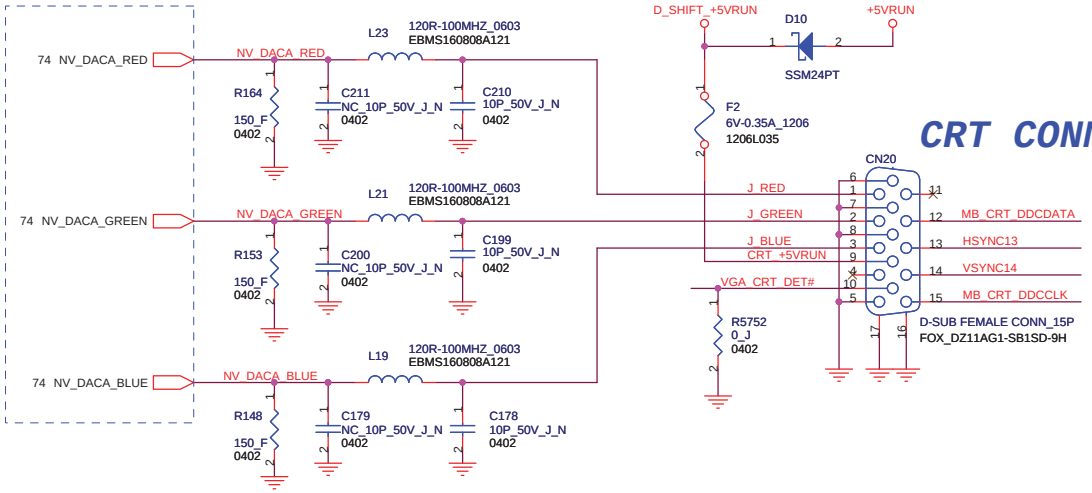
Semi-PnP (For Win7 ,Should be Dummy)

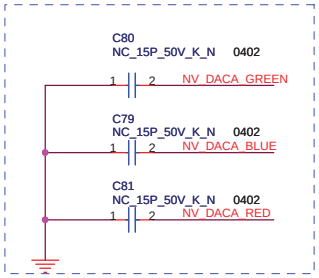




7/8 [DVT] Delete iGPU, Change Net name.

CRT CONNECTOR





7/8 [DVT] Delete iGPU, Change Net name.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CRT	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 63 of 96	

DVDD_IO can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.

BOM Option for ALC275 and ALC269
(Default is ALC275.)

8/10 [DVT] Delete the U215 SMB Connection.

7/8 [DVT] Change to AND gate for AMP_PD# works.

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2.When you want to exit your Bios Programming Code, please let the EC_MUTE# Low.(The programming is different from before .)

Place near pin 27

Place near pin 25

Place near pin 38

8/10 [DVT] Reserve the R5934 for C/D as MOR request.

7/13 [DVT] Add Test Point TP327 ,TP378 ,TP380 Place near U215

7/23 [DVT] Change PH Power Plane to avoid Q90 abnormal behavior.

Place near U215

Tied at one point only under the ALC275 or near the ALC275

BOM Option for ALC275 and ALC269
(Default is ALC275.)

8/10 [DVT] Dummy U217 and C6063 for C/D as MOR request.

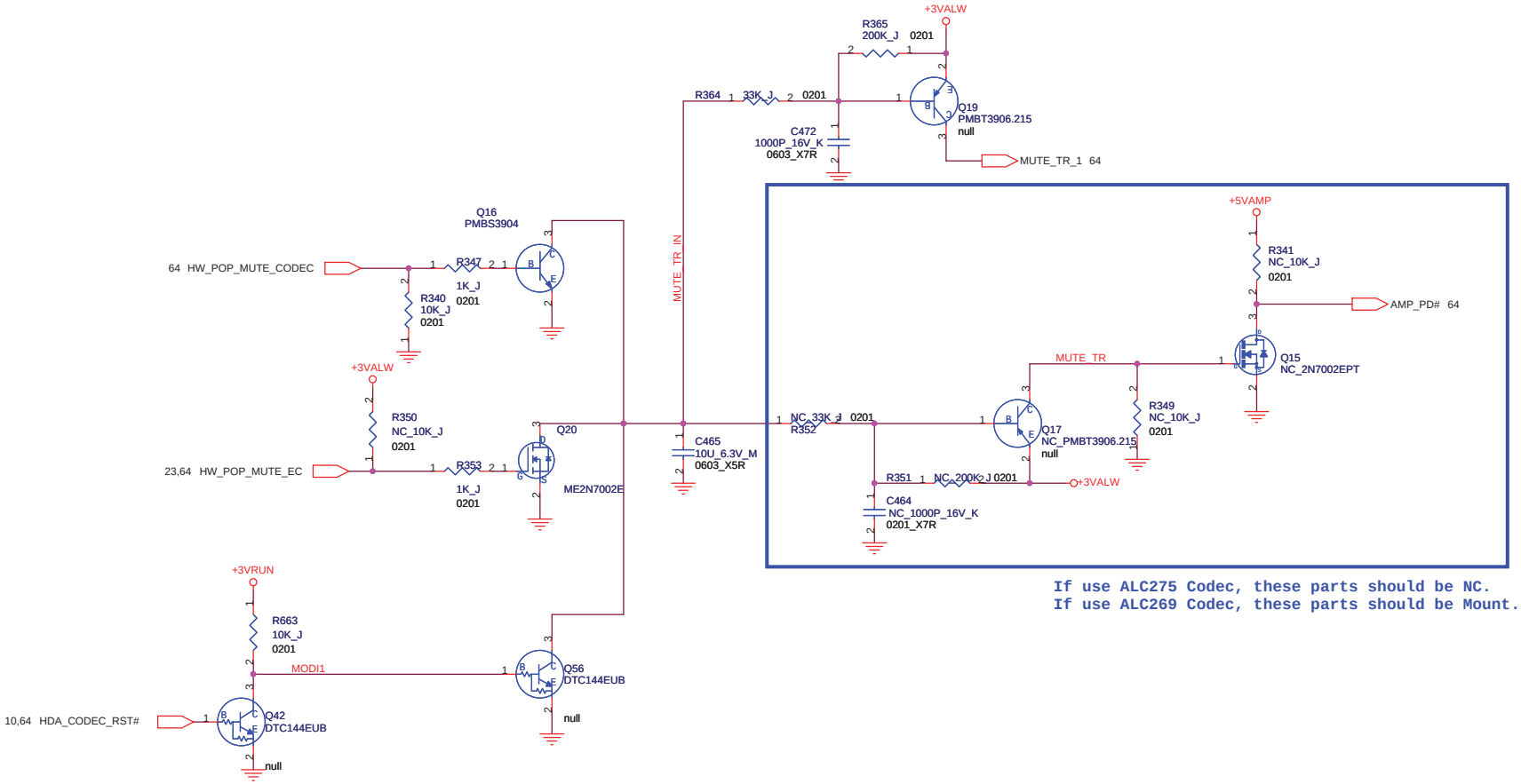
8/10 [DVT] Add EC17 and EC19 ,EC21,EC22 for EMI Solution.

BOM Option for ALC275 and ALC269
(Default is ALC275.)

PC BEEP

8/10 [DVT] Change R5782 to 100kohm to decrease and BEEP sound level as MOR request.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: AUDIO(CODEC)		
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 64 of 96	

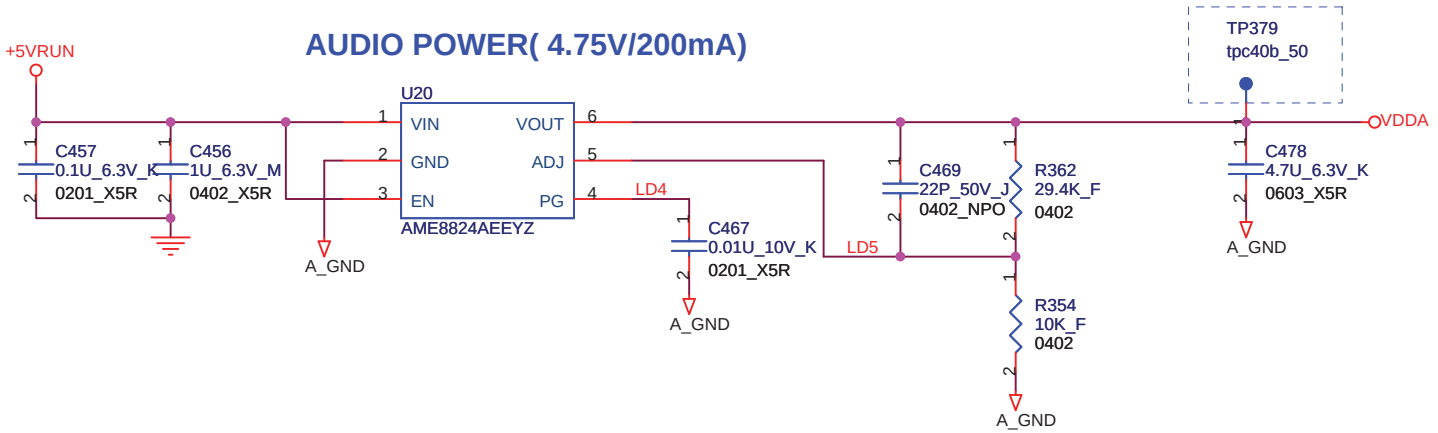


If use ALC275 Codec, these parts should be NC.
If use ALC269 Codec, these parts should be Mount.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO (MUTE)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 65 of 96	

7/13 [DVT] Add Test Point TP379

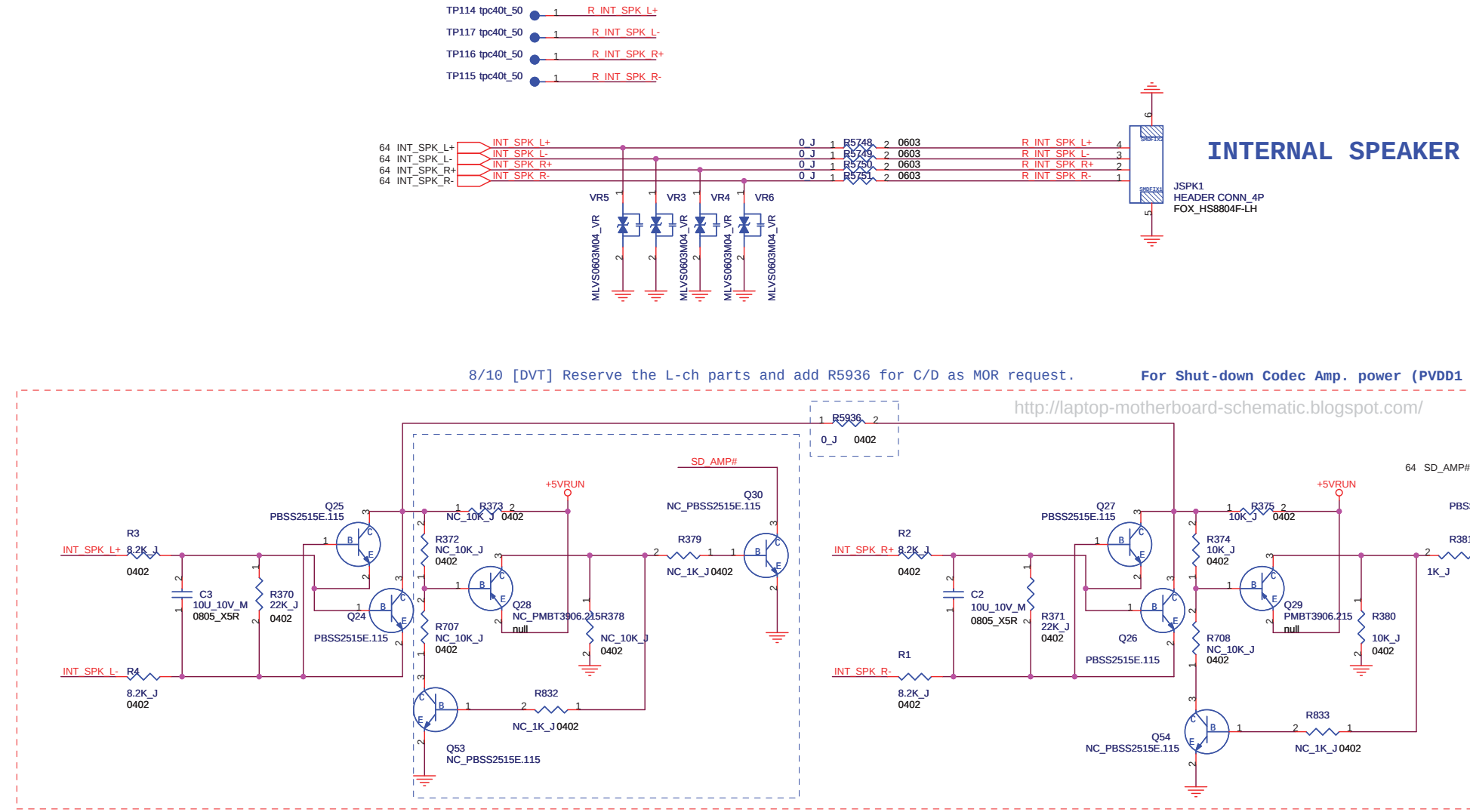
AUDIO POWER(4.75V/200mA)



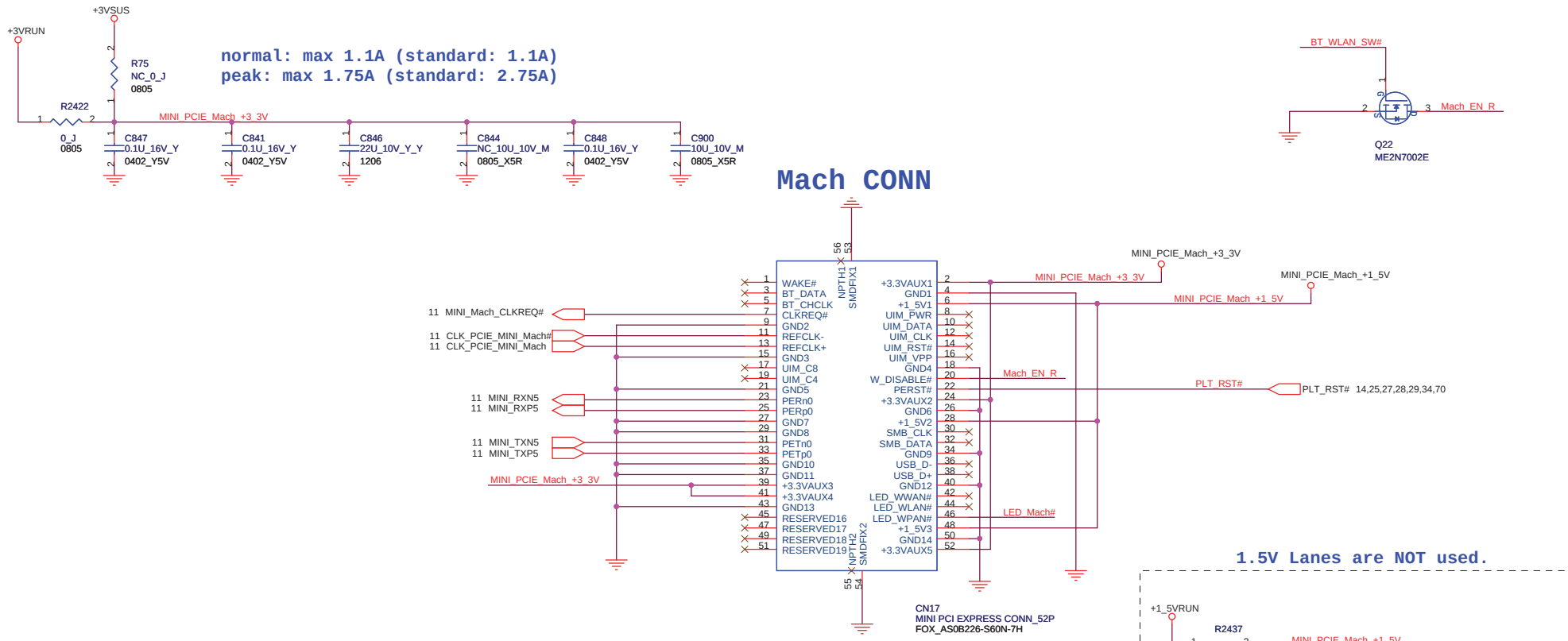
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**AUDIO POWER**	
Size A4	Document Number **M930 (MBX-215)**	Rev **SB**
Date: Wednesday, August 12, 2009	Sheet 66 of 96	

Delete Class D Amp. when implemented ALC275.

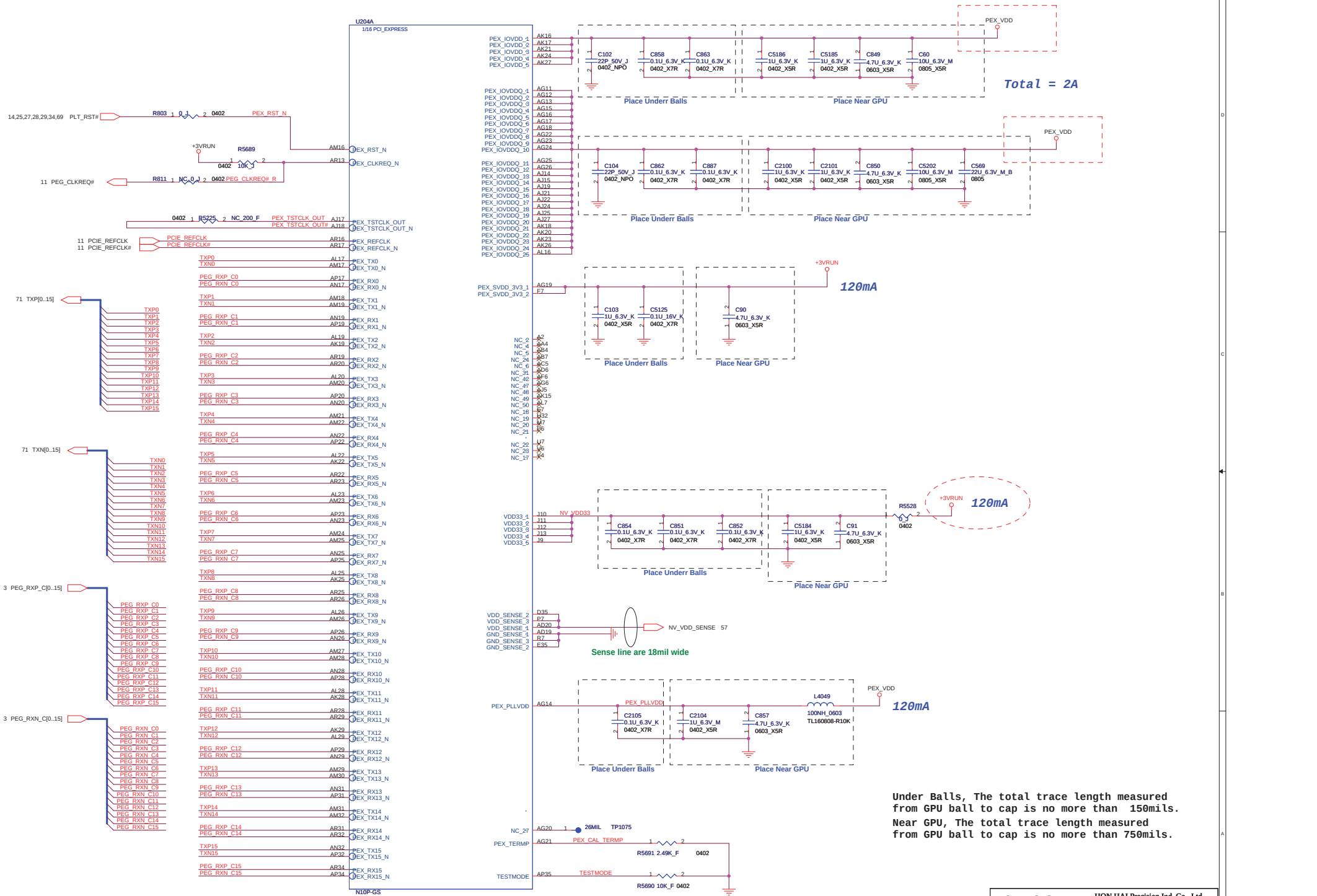
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO SPEAKER AMP	
Size: A3	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 67 of 96	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO SPEAKER CONNECTOR	
Size B	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 68 of 96	



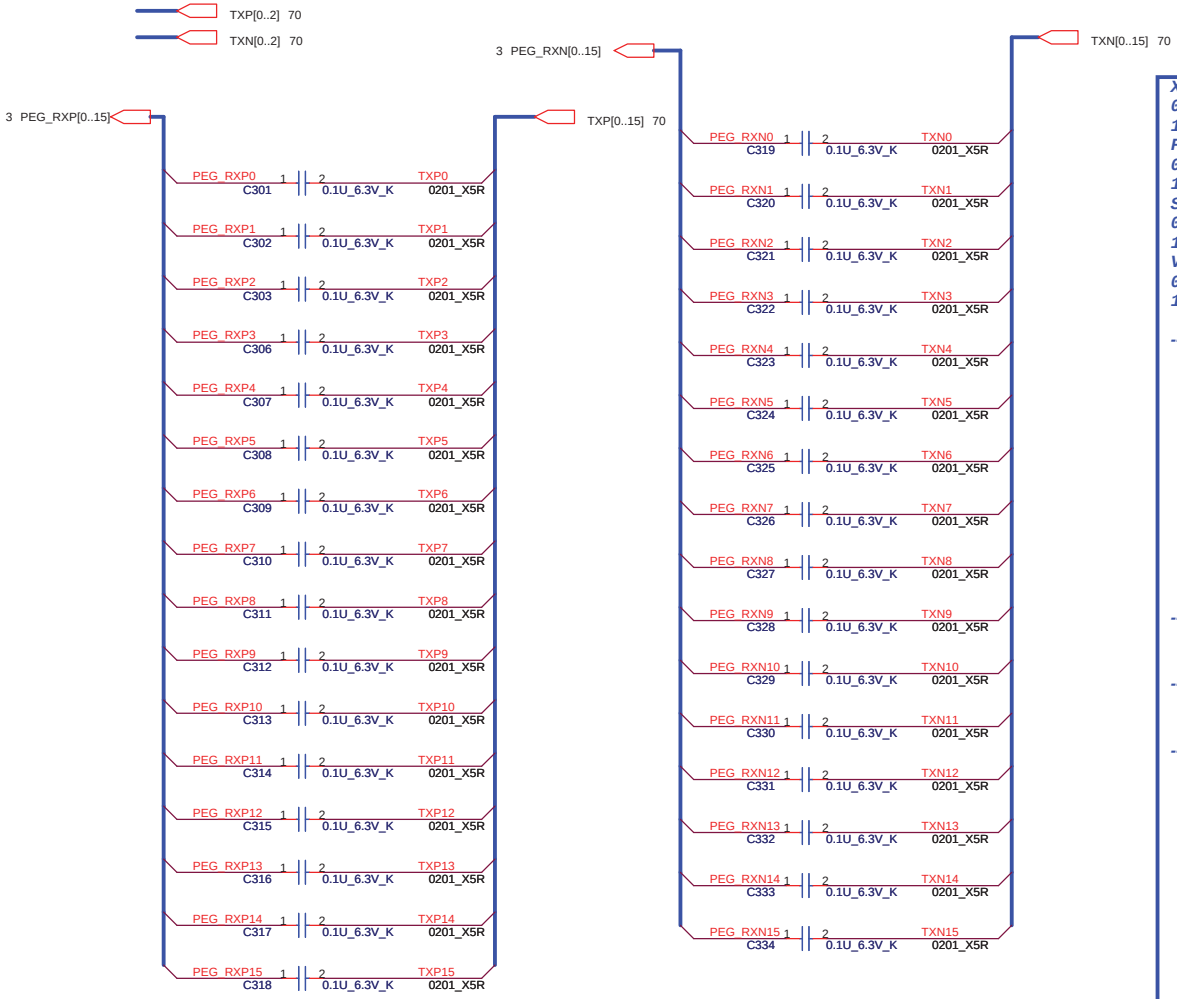
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Mini-PCIE Card(Mach)	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 69 of 96	



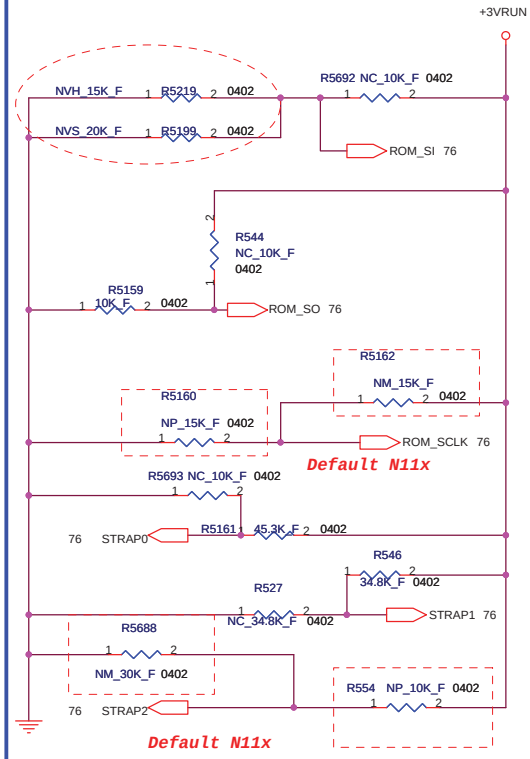
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VGA (PCI-E) 1/9	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 70 of 96	

8/3 [DVT] Revise the Strap Pin value as FAEprovided for DVT Sample.
- N11P-GE1 x0A29
- N11M-GE1 x0A75



XCLK_417 0 (27M Hz) 1 (Reserved) FB_0_BAR_SIZE 0 256MB 1 (Reserved) SMB_ALT_ADDR 0 0x9E 1 0x9C(multi-GPU usage) VGA_DEVICE 0 3D device(class code 302h) 1 VGA device(class code 300h)	ROM_SO 0001
SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present) SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk) PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	ROM_SCLK N11P-GE1 0010 N11M-GE1 1010
USER[3:0] 1000	STRAP0 (1111)
N10x/N11x 3GIO_PADCFG[3:0] 0110	STRAP1 (1110)
N11X PCI_DEVID[3:0] N11P-GS1 1001b N11M-GE1 0101b PCI DEVICE IDs N11P-GE1 (0x0A29) N11M-GE1 (0x0A75)	Strap2 N11P-GE1 1001 N11M-GE1 0101



ROM_SI 0000 64-bit Reserved 0010 64Mx16 DDR3 - 96 ball 128-bit Hynix(13-H5T01G6-3000) 15K Pull Low. 0011 64Mx16 DDR3 - 96 ball 128-bit Samsung(13-K4W1G16-3000) 20K pull Low

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

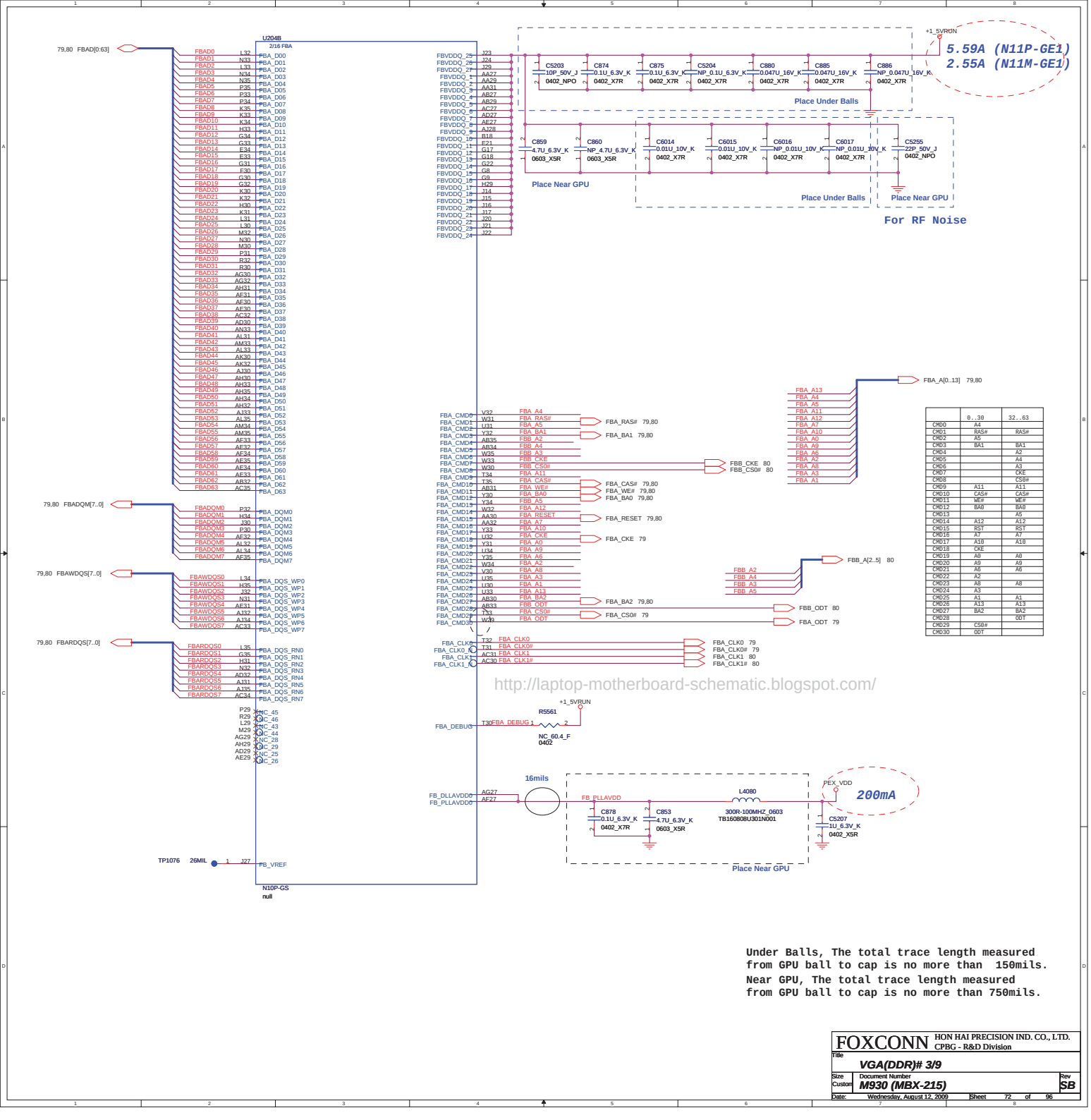
Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	BGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04202-001_v02_secured>

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

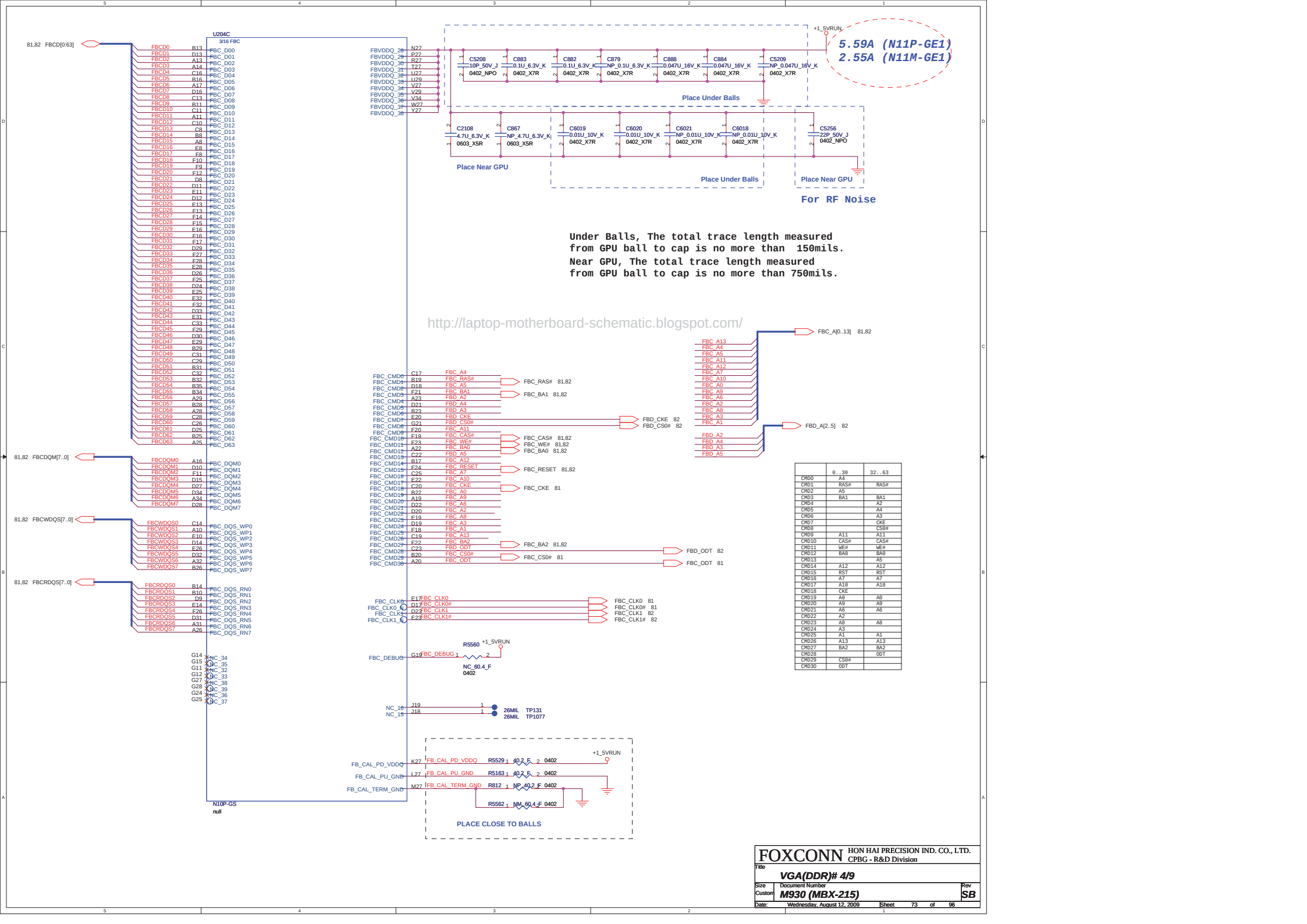
Title: VGA (PCI-E BUS)Strap 2/9
Size: Custom | Document Number: M930 (MBX-215) | Rev: SB
Date: Wednesday, August 12, 2009 | Sheet 71 of 96



	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A9	A9
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(DDR)# 3/9	
Size: Custom	Document Number: M930 (MBX-215)	Rev: SB
Date: Wednesday, August 12, 2009	Sheet 72 of 96	


U204C
3/16 FBC
N10P-GS
null
81,82 FBCD[0:63]
FBCD0 B13 FBC_D00
FBCD1 D13 FBC_D01
FBCD2 A13 FBC_D02
FBCD3 A14 FBC_D03
FBCD4 C16 FBC_D04
FBCD5 B16 FBC_D05
FBCD6 A17 FBC_D06
FBCD7 D16 FBC_D07
FBCD8 C13 FBC_D08
FBCD9 B11 FBC_D09
FBCD10 C11 FBC_D10
FBCD11 A11 FBC_D11
FBCD12 C10 FBC_D12
FBCD13 C8 FBC_D13
FBCD14 B8 FBC_D14
FBCD15 A8 FBC_D15
FBCD16 E8 FBC_D16
FBCD17 F8 FBC_D17
FBCD18 F10 FBC_D18
FBCD19 F9 FBC_D19
FBCD20 F12 FBC_D20
FBCD21 D8 FBC_D21
FBCD22 D11 FBC_D22
FBCD23 E11 FBC_D23
FBCD24 D12 FBC_D24
FBCD25 F13 FBC_D25
FBCD26 E13 FBC_D26
FBCD27 F14 FBC_D27
FBCD28 F15 FBC_D28
FBCD29 E16 FBC_D29
FBCD30 F16 FBC_D30
FBCD31 F17 FBC_D31
FBCD32 D29 FBC_D32
FBCD33 F27 FBC_D33
FBCD34 E28 FBC_D34
FBCD35 E28 FBC_D35
FBCD36 D26 FBC_D36
FBCD37 F25 FBC_D37
FBCD38 D24 FBC_D38
FBCD39 E25 FBC_D39
FBCD40 E32 FBC_D40
FBCD41 F32 FBC_D41
FBCD42 D33 FBC_D42
FBCD43 E31 FBC_D43
FBCD44 C33 FBC_D44
FBCD45 F29 FBC_D45
FBCD46 D30 FBC_D46
FBCD47 E29 FBC_D47
FBCD48 B29 FBC_D48
FBCD49 C31 FBC_D49
FBCD50 C29 FBC_D50
FBCD51 B31 FBC_D51
FBCD52 C32 FBC_D52
FBCD53 B32 FBC_D53
FBCD54 B35 FBC_D54
FBCD55 B34 FBC_D55
FBCD56 A29 FBC_D56
FBCD57 B28 FBC_D57
FBCD58 A28 FBC_D58
FBCD59 C28 FBC_D59
FBCD60 C26 FBC_D60
FBCD61 D25 FBC_D61
FBCD62 B25 FBC_D62
FBCD63 A25 FBC_D63
81,82 FBCDQM[7..0]
FBCDQM0 A16 FBC_DQM0
FBCDQM1 D10 FBC_DQM1
FBCDQM2 F11 FBC_DQM2
FBCDQM3 D15 FBC_DQM3
FBCDQM4 D27 FBC_DQM4
FBCDQM5 D34 FBC_DQM5
FBCDQM6 A34 FBC_DQM6
FBCDQM7 D28 FBC_DQM7
81,82 FBCWDQS[7..0]
FBCWDQS0 C14 FBC_DQS_WP0
FBCWDQS1 A10 FBC_DQS_WP1
FBCWDQS2 E10 FBC_DQS_WP2
FBCWDQS3 D14 FBC_DQS_WP3
FBCWDQS4 E26 FBC_DQS_WP4
FBCWDQS5 D32 FBC_DQS_WP5
FBCWDQS6 A32 FBC_DQS_WP6
FBCWDQS7 B26 FBC_DQS_WP7
81,82 FBCRDQS[7..0]
FBCRDQS0 B14 FBC_DQS_RN0
FBCRDQS1 B10 FBC_DQS_RN1
FBCRDQS2 D9 FBC_DQS_RN2
FBCRDQS3 E14 FBC_DQS_RN3
FBCRDQS4 F26 FBC_DQS_RN4
FBCRDQS5 D31 FBC_DQS_RN5
FBCRDQS6 A31 FBC_DQS_RN6
FBCRDQS7 A26 FBC_DQS_RN7
G14 NC_34
G15 NC_35
G11 NC_32
G12 NC_33
G27 NC_38
G28 NC_39
G24 NC_36
G25 NC_37
FBVDDQ_28 N27
FBVDDQ_29 P27
FBVDDQ_30 R27
FBVDDQ_31 T27
FBVDDQ_32 U27
FBVDDQ_33 U29
FBVDDQ_34 V27
FBVDDQ_35 V29
FBVDDQ_36 V34
FBVDDQ_37 W27
FBVDDQ_38 Y27
+1_5VRUN
C5208 10P_50V_J 0402_NPO
C883 0.1U_6.3V_K 0402_X7R
C882 0.1U_6.3V_K 0402_X7R
C879 NP_0.1U_6.3V_K 0402_X7R
C888 0.047U_16V_K 0402_X7R
C884 0.047U_16V_K 0402_X7R
C5209 NP_0.047U_16V_K 0402_X7R
Place Under Balls
5.59A (N11P-GE1)
2.55A (N11M-GE1)
C2108 4.7U_6.3V_K 0603_X5R
C867 NP_4.7U_6.3V_K 0603_X5R
C6019 0.01U_10V_K 0402_X7R
C6020 0.01U_10V_K 0402_X7R
C6021 NP_0.01U_10V_K 0402_X7R
C6018 NP_0.01U_10V_K 0402_X7R
C5256 22P_50V_J 0402_NPO
Place Near GPU
Place Under Balls
Place Near GPU
For RF Noise
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.
http://laptop-motherboard-schematic.blogspot.com/
FBC_A[0..13] 81,82
FBC_A13
FBC_A4
FBC_A5
FBC_A11
FBC_A12
FBC_A7
FBC_A10
FBC_A0
FBC_A9
FBC_A6
FBC_A2
FBC_A8
FBC_A3
FBC_A1
FBD_A[2..5] 82
FBD_A2
FBD_A4
FBD_A3
FBD_A5
FBC_CMD0 C17 FBC_A4
FBC_CMD1 B19 FBC_RAS# FBC_RAS# 81,82
FBC_CMD2 D18 FBC_A5
FBC_CMD3 F21 FBC_BA1 FBC_BA1 81,82
FBC_CMD4 A23 FBC_A2
FBC_CMD5 D21 FBD_A4
FBC_CMD6 B23 FBD_A3
FBC_CMD7 E20 FBD_CKE FBD_CKE 82
FBC_CMD8 G21 FBD_CS0# FBD_CS0# 82
FBC_CMD9 E20 FBC_A11
FBC_CMD10 F19 FBC_CAS# FBC_CAS# 81,82
FBC_CMD11 F23 FBC_WE# FBC_WE# 81,82
FBC_CMD12 A22 FBC_BA0 FBC_BA0 81,82
FBC_CMD13 C22 FBD_A5
FBC_CMD14 B17 FBC_A12
FBC_CMD15 F24 FBC_RESET FBC_RESET 81,82
FBC_CMD16 C25 FBC_A7
FBC_CMD17 E22 FBC_A10
FBC_CMD18 C20 FBC_CKE FBC_CKE 81
FBC_CMD19 B22 FBC_A0
FBC_CMD20 A19 FBC_A9
FBC_CMD21 D22 FBC_A6
FBC_CMD22 D20 FBC_A2
FBC_CMD23 E19 FBC_A8
FBC_CMD24 D19 FBC_A3
FBC_CMD25 F18 FBC_A1
FBC_CMD26 C19 FBC_A13
FBC_CMD27 F22 FBC_BA2 FBC_BA2 81,82
FBC_CMD28 C23 FBD_ODT FBD_ODT 82
FBC_CMD29 B20 FBC_CS0# FBC_CS0# 81
FBC_CMD30 A20 FBC_ODT FBC_ODT 81
FBC_CLK0 E17 FBC_CLK0 FBC_CLK0 81
FBC_CLK0_Q D17 FBC_CLK0# FBC_CLK0# 81
FBC_CLK1 D23 FBC_CLK1 FBC_CLK1 82
FBC_CLK1_Q E23 FBC_CLK1# FBC_CLK1# 82
R5560 +1_5VRUN
FBC_DEBUG G19 FBC_DEBUG
NC_60.4_F 0402
NC_16 J19 26MIL TP131
NC_15 J18 26MIL TP1077
FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R5529 40.2_F 0402 +1_5VRUN
FB_CAL_PU_GND L27 FB_CAL_PU_GND R5163 40.2_F 0402
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R812 NP_40.2_F 0402
R5562 NM_60.4_F 0402
PLACE CLOSE TO BALLS
0..30 32..63
CMD0 A4
CMD1 RAS# RAS#
CMD2 A5
CMD3 BA1 BA1
CMD4 A2
CMD5 A4
CMD6 A3
CMD7 CKE
CMD8 CS0#
CMD9 A11 A11
CMD10 CAS# CAS#
CMD11 WE# WE#
CMD12 BA0 BA0
CMD13 A5
CMD14 A12 A12
CMD15 RST RST
CMD16 A7 A7
CMD17 A10 A10
CMD18 CKE
CMD19 A0 A0
CMD20 A9 A9
CMD21 A6 A6
CMD22 A2
CMD23 A8 A8
CMD24 A3
CMD25 A1 A1
CMD26 A13 A13
CMD27 BA2 BA2
CMD28 ODT
CMD29 CS0#
CMD30 ODT
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
VGA(DDR)# 4/9
Size Custom
Document Number
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+3VRUN **120mA**

L4043
300R-100MHZ_0603
TB160808U301N001

C62 4.7U_6.3V_K 0603_X5R
C5210 1U_6.3V_K 0402_X5R
Place Near GPU

C5194 0.1U_16V_K 0402_X7R
C5199 0.1U_16V_K 0402_X7R
C5200 0.1U_16V_K 0402_X7R
C63 4700P_16V_K 0402_X7R
C64 470P_50V_K 0402_X7R
Place Under Balls

DACA_VDD
DACA_VREF
DACA_RSET
C5211 0.1U_6.3V_K 0402_X7R
R801 124_F 0402

U204F
4/16 DACA
DACA_VDD AJ12
DACA_VREF AK12
DACA_RSET AK13
I2CA_SCL G1 NV_I2CA_SCL
I2CA_SDA G4 NV_I2CA_SDA
DACA_HSYNC AM13 NV_DACA_HSYNC
DACA_VSYNC AL13 NV_DACA_VSYNC
DACA_RED AM15 NV_DACA_RED
DACA_GREEN AM14 NV_DACA_GREEN
DACA_BLUE AL14 NV_DACA_BLUE
N10P-GS
null

NV_I2CA_SCL 63
NV_I2CA_SDA 63
NV_DACA_HSYNC 63
NV_DACA_VSYNC 63
NV_DACA_RED 63
NV_DACA_GREEN 63
NV_DACA_BLUE 63

150_F 0402 R5695
150_F 0402 R5696
150_F 0402 R5697
Place close to balls

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

R5697 10K_J 0402 NV_DACC_VDD

U204G
6/16 DACC
DACB_VDD AG7
DACB_VREF AK6
DACB_RSET AH7
I2CB_SCL G3 NV_I2CB_SCL
I2CB_SDA G2 NV_I2CB_SDA
DACB_HSYNC AM1
DACB_VSYNC AM2
DACB_RED AK4
DACB_GREEN AL4
DACB_BLUE AJ4
N10P-GS
null

R5535 NC_124_F 0402

+3VRUN
R5698 0402 2.2K_J
R1230 0402 2.2K_J

DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

eDP (Suzaku3 support) >> Stuff

+3VRUN **220mA**
L4044
300R-100MHZ_0603
TB160808U301N001
C866 4.7U_6.3V_K 0603_X5R
C5198 2.2U_6.3V_K 0603_B
IFPD_PLLVDD

PEX_VDD **285mA**
L4084
220R-100MHZ_0603
FCM1608KF-221T05
C5212 4.7U_6.3V_K 0603_X5R
C5197 1U_6.3V_K 0402_X5R
IFPD_IOVDD
Place Near GPU.

C5193 0.1U_16V_K 0402_X7R
C5183 0.1U_16V_K 0402_X7R
C5182 0.1U_16V_K 0402_X7R
C5196 0.1U_16V_K 0402_X7R
C5195 0.1U_16V_K 0402_X7R
Place Under Balls

For RF Noise
C5258 22P_50V_J 0402_NPO
C5257 22P_50V_J 0402_NPO
For RF Noise

R5700 1K_F 0402

U204H
5/16 DACB(TV)
IFPD_PLLVDD AC6
IFPD_RSET AB6
IFPD_IOVDD AK8
IFPD_AUX_I2CX_SDA_N
IFPD_AUX_I2CX_SCL
IFPD_L3_N
IFPD_L3
IFPD_L2_N
IFPD_L2
IFPD_L1_N
IFPD_L1
IFPD_L0_N
IFPD_L0
GPIO19
N10P-GS
null

AN4 NV_PEG_AUXN C835 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_AUXN
AP4 NV_PEG_AUXP C834 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_AUXP
AR4 NV_PEG_TXN3 C837 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXN3
AR5 NV_PEG_TXP3 C836 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXP3
AP5 NV_PEG_TXN2 C800 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXN2
AN5 NV_PEG_TXP2 C803 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXP2
AN7 NV_PEG_TXN1 C793 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXN1
AP7 NV_PEG_TXP1 C795 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXP1
AR7 NV_PEG_TXN0 C725 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXN0
AR8 NV_PEG_TXP0 C735 NC_0.1U_6.3V_K 0201_X5R eDP_PEG_TXP0
L7 eDP_DET_NV

eDP_PEG_AUXN 38
eDP_PEG_AUXP 38
eDP_PEG_TXN3 38
eDP_PEG_TXP3 38
eDP_PEG_TXN2 38
eDP_PEG_TXP2 38
eDP_PEG_TXN1 38
eDP_PEG_TXP1 38
eDP_PEG_TXN0 38
eDP_PEG_TXP0 38

To eDP CONN.

7/8 [DVT] Change to NC, when support eDP stuffed.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA(CRT/eDP) 5/9
Size: Custom
Document Number: M930 (MBX-215)
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Date: Wednesday, August 12, 2009
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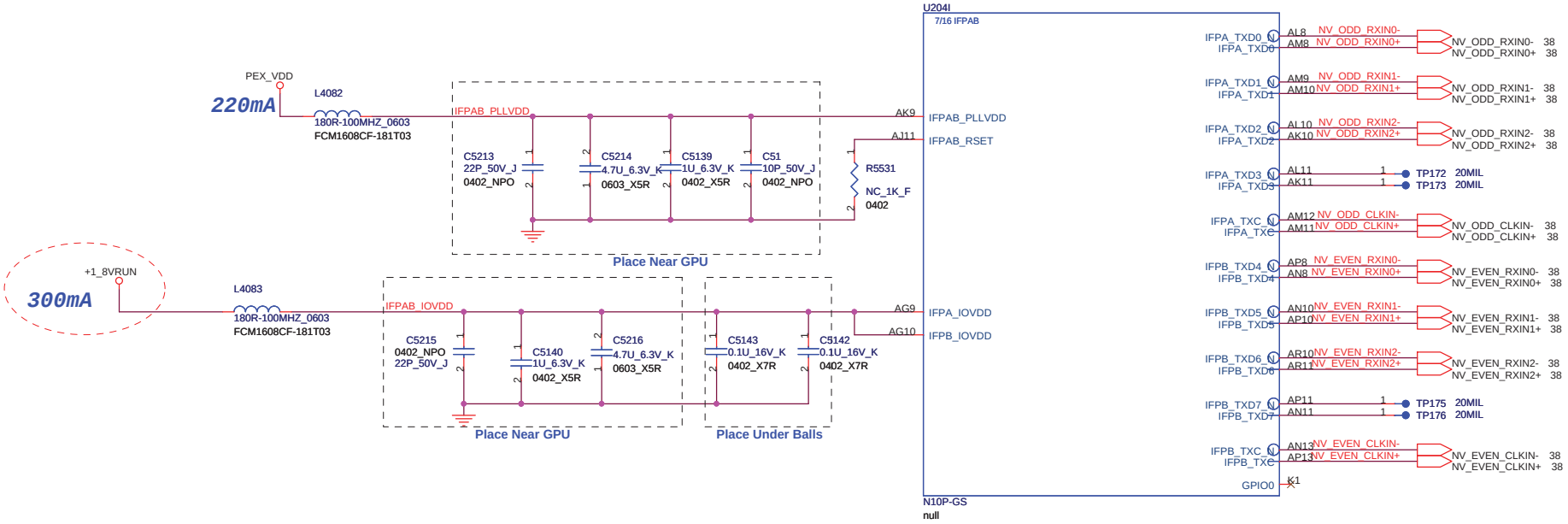
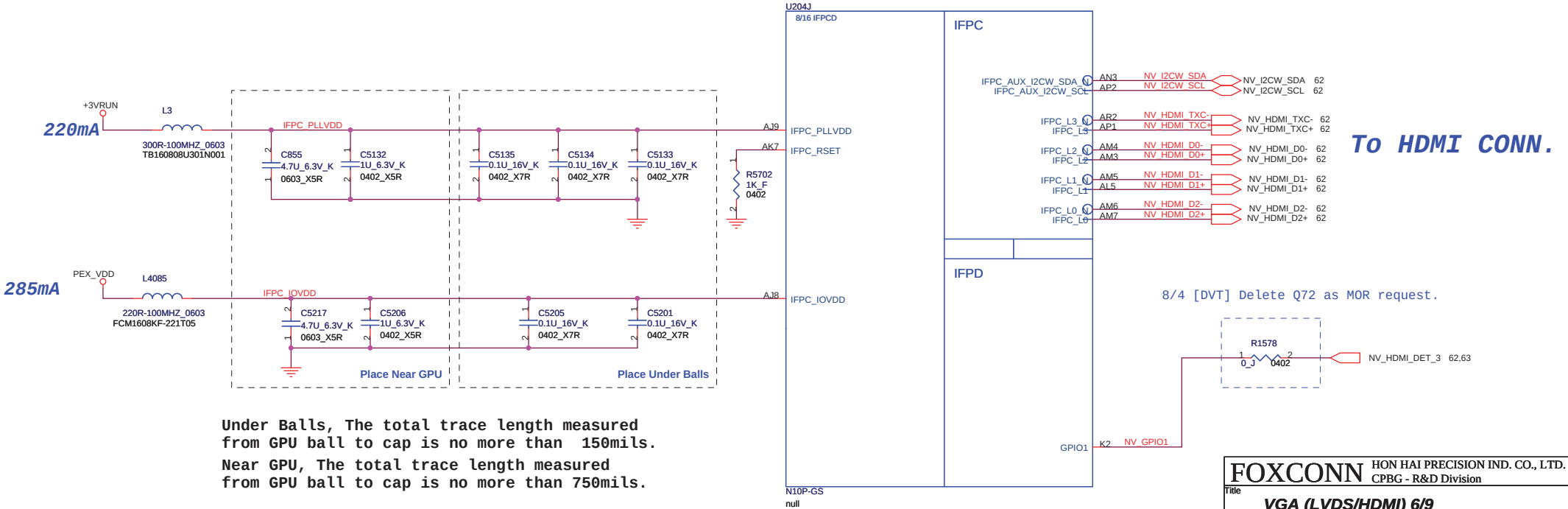




Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

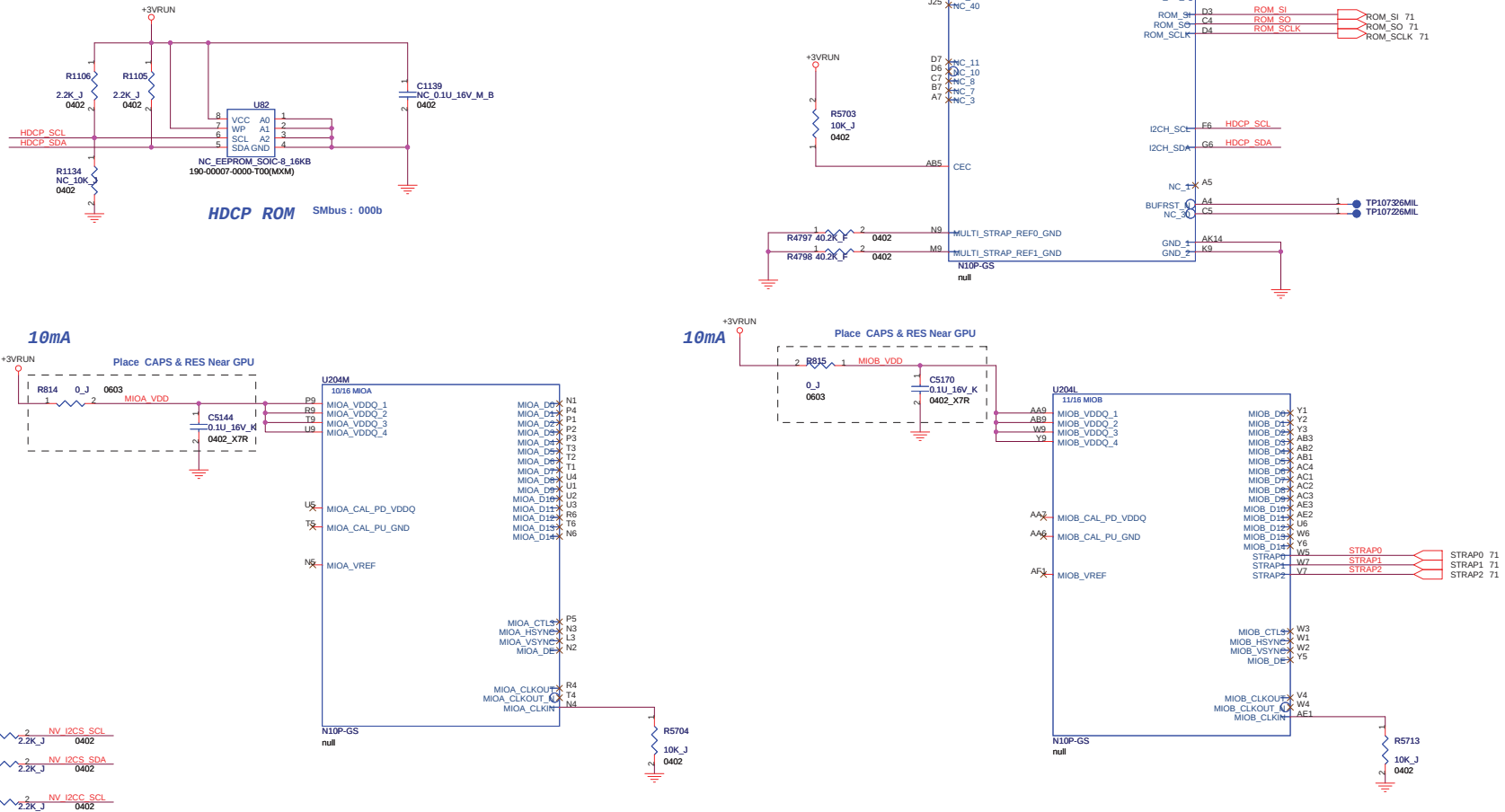
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (LVDS/HDMI) 6/9

Size: A3 | Document Number: M930 (MBX-215) | Rev: SB

Date: Wednesday, August 12, 2009 | Sheet 75 of 96



GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	YES		
GPIO1	I	Yes	HDMI Hot Plug Detect 0(HPD0)	Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	Yes	FOR Power Control NVDD	Active High or Low
GPIO6	O	No	FOR Power Control NVDD	Active High or Low
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	Active Low

SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermial I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

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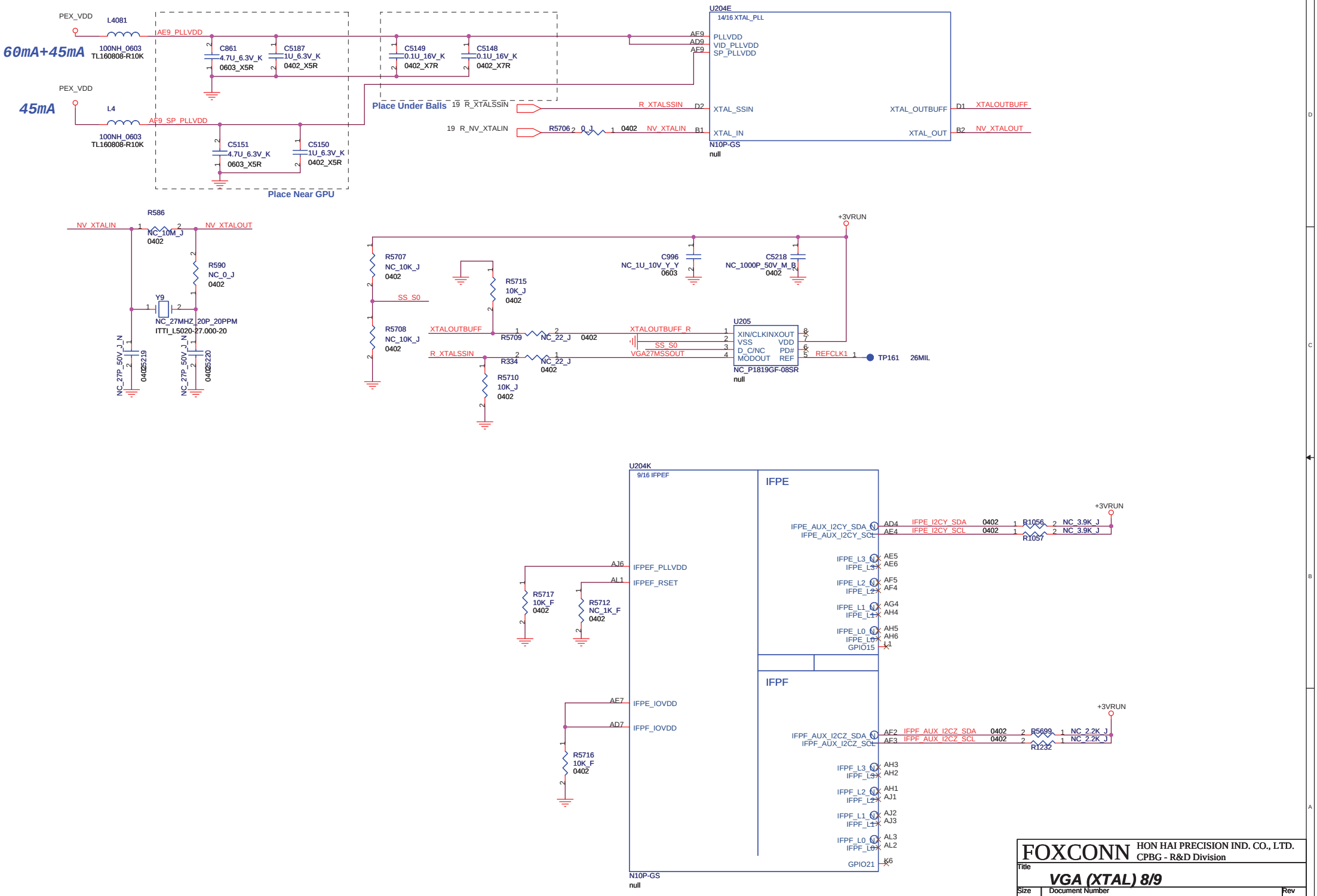
Title: VGA (XTAL/GPIO) 7/9

Size: Custom | Document Number: M930 (MBX-215) | Rev: SB

Date: Wednesday, August 12, 2009 | Sheet 76 of 96

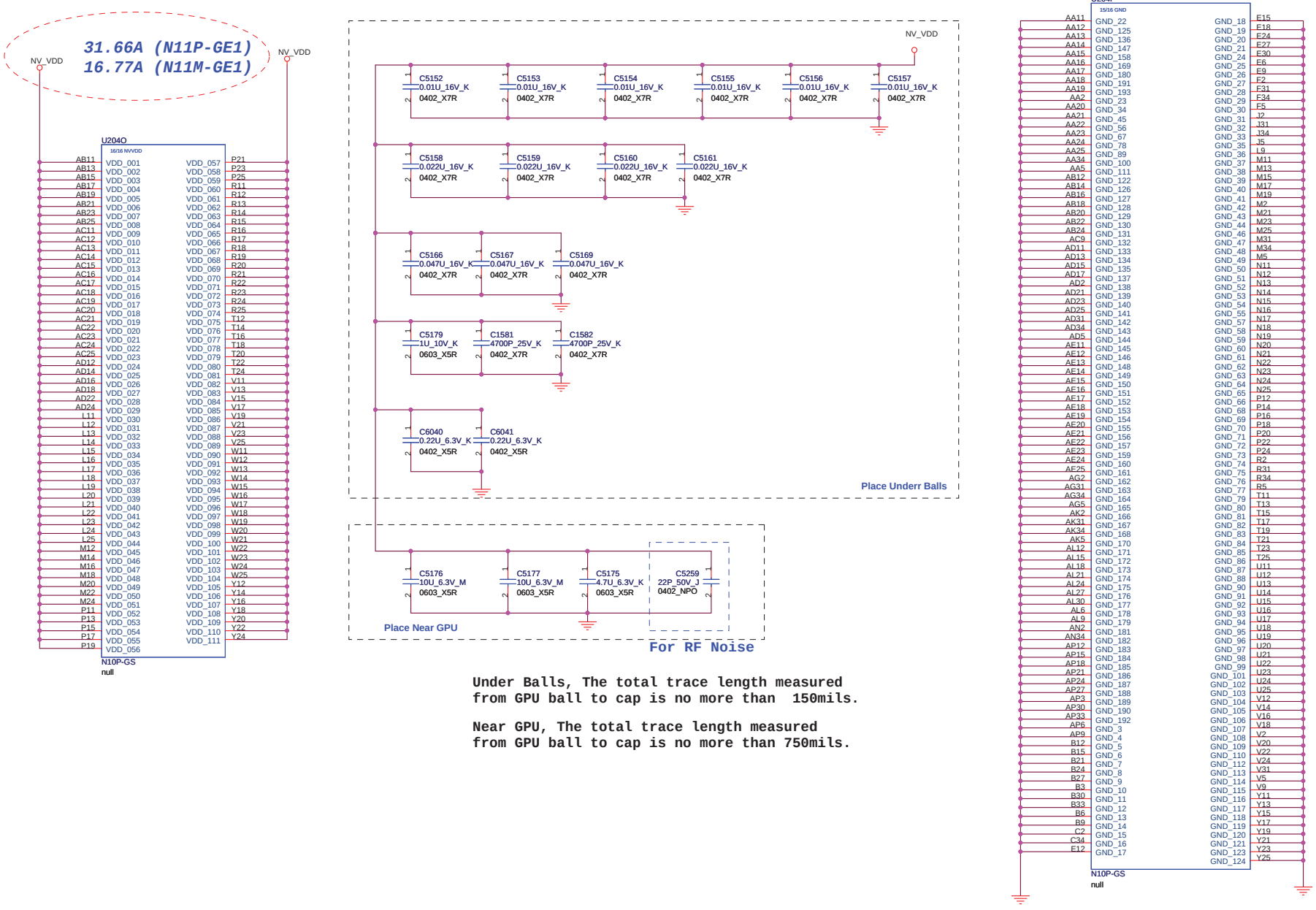


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (XTAL) 8/9

Size: A3 | Document Number: M930 (MBX-215) | Rev: SB

Date: Wednesday, August 12, 2009 | Sheet 77 of 96



Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VGA(POWER/GROUND) 9/9		
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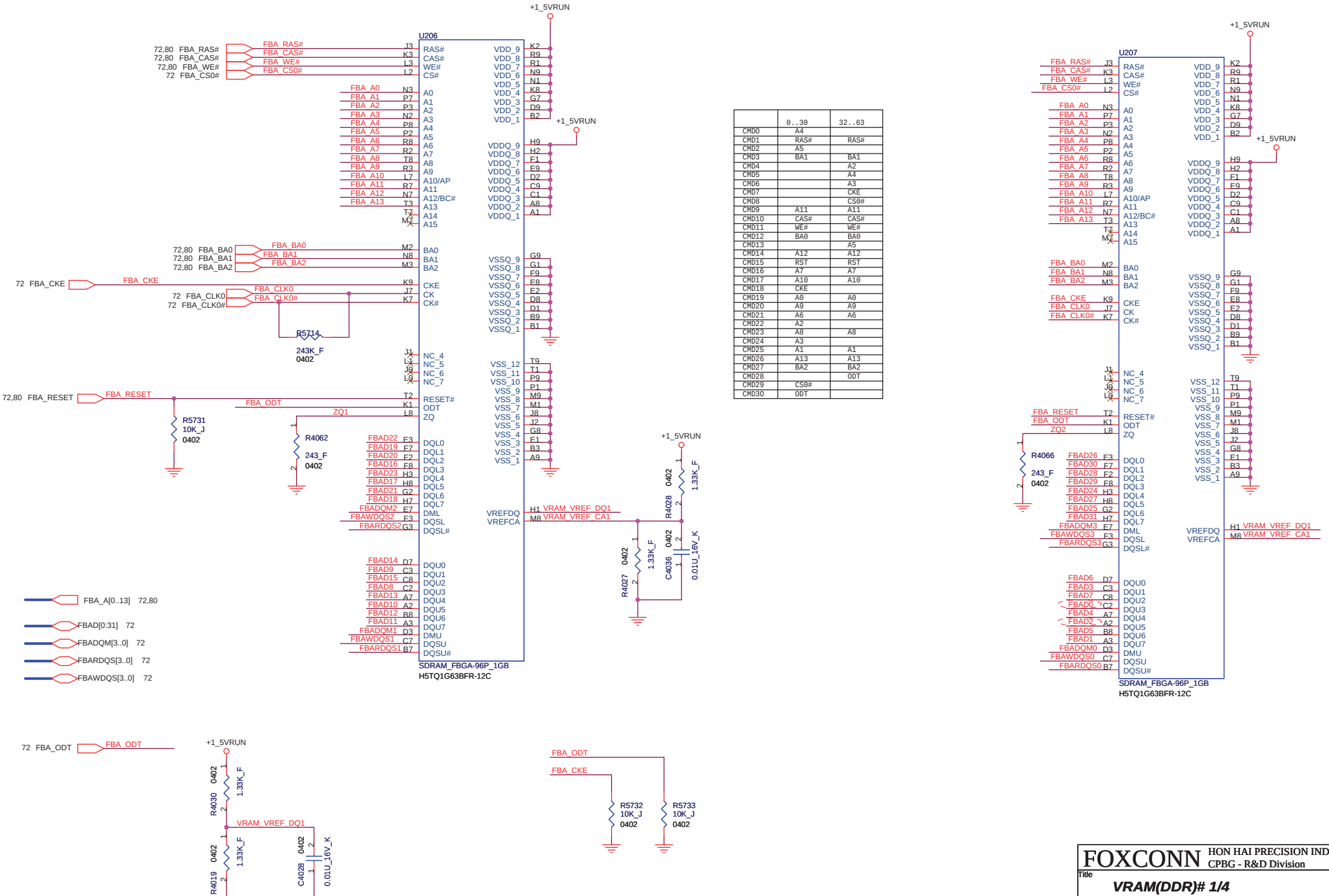

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM(DDR)# 1/4

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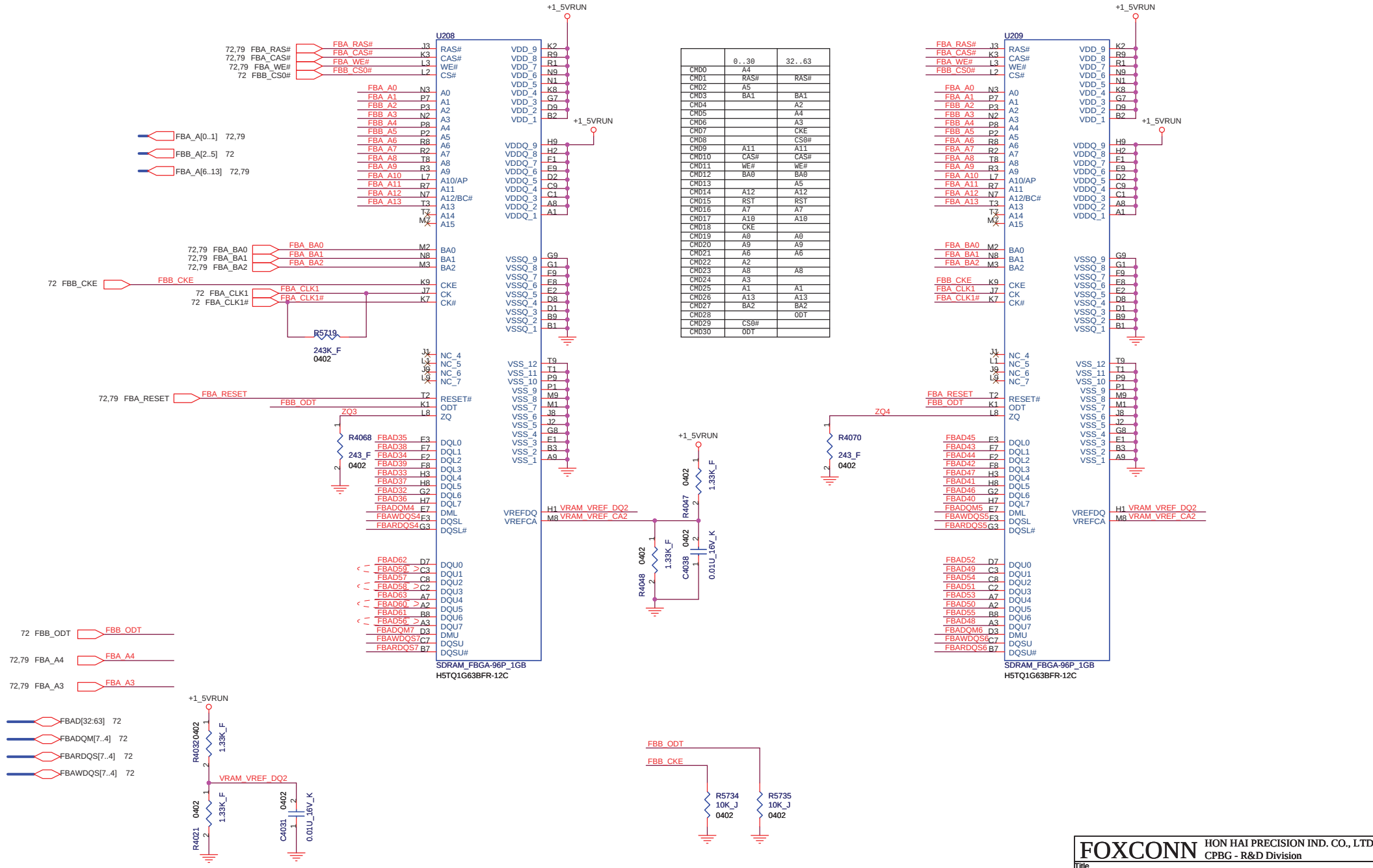

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM(DDR)# 2/4
Size A3	Document Number M930 (MBX-215)
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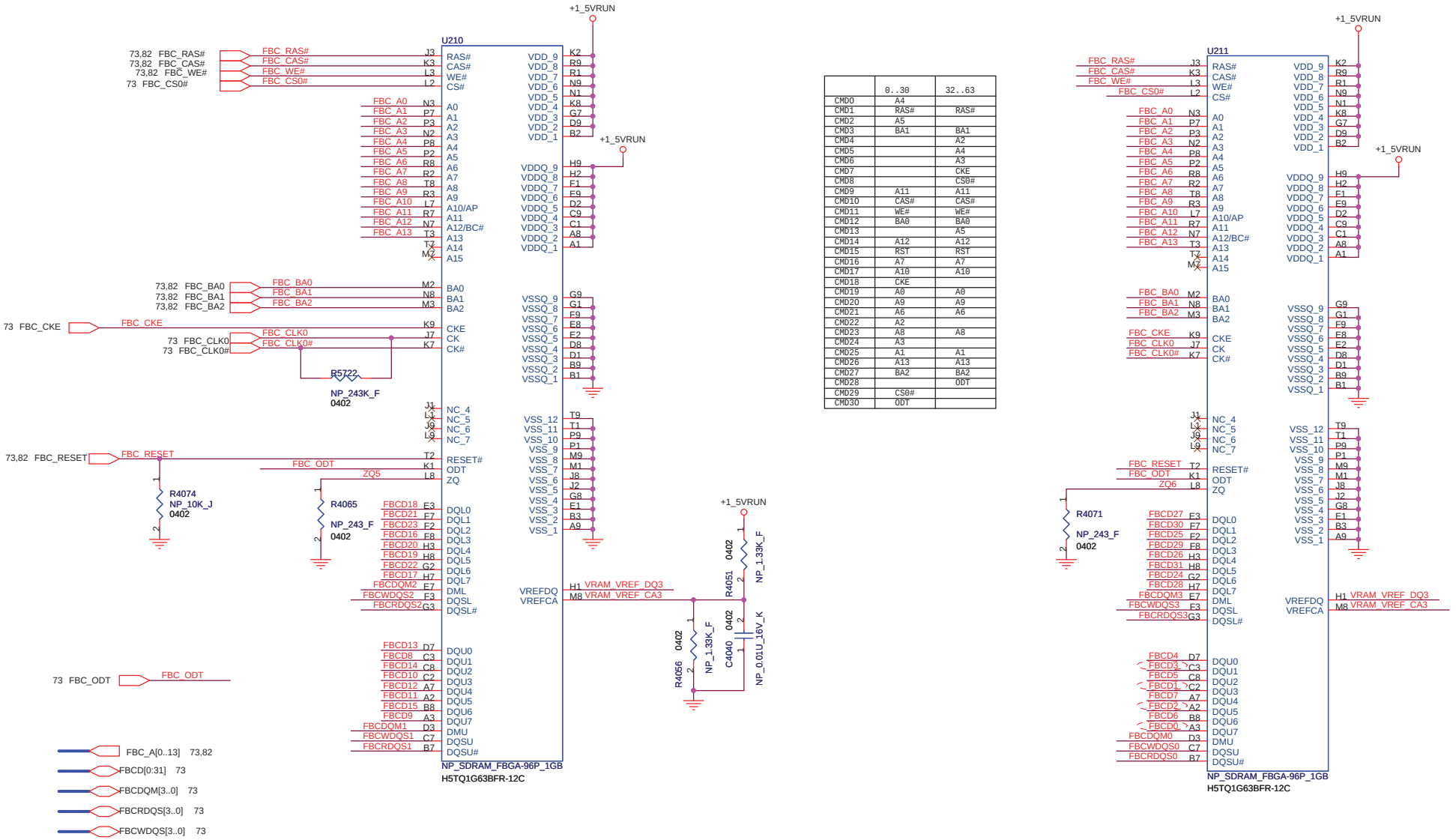


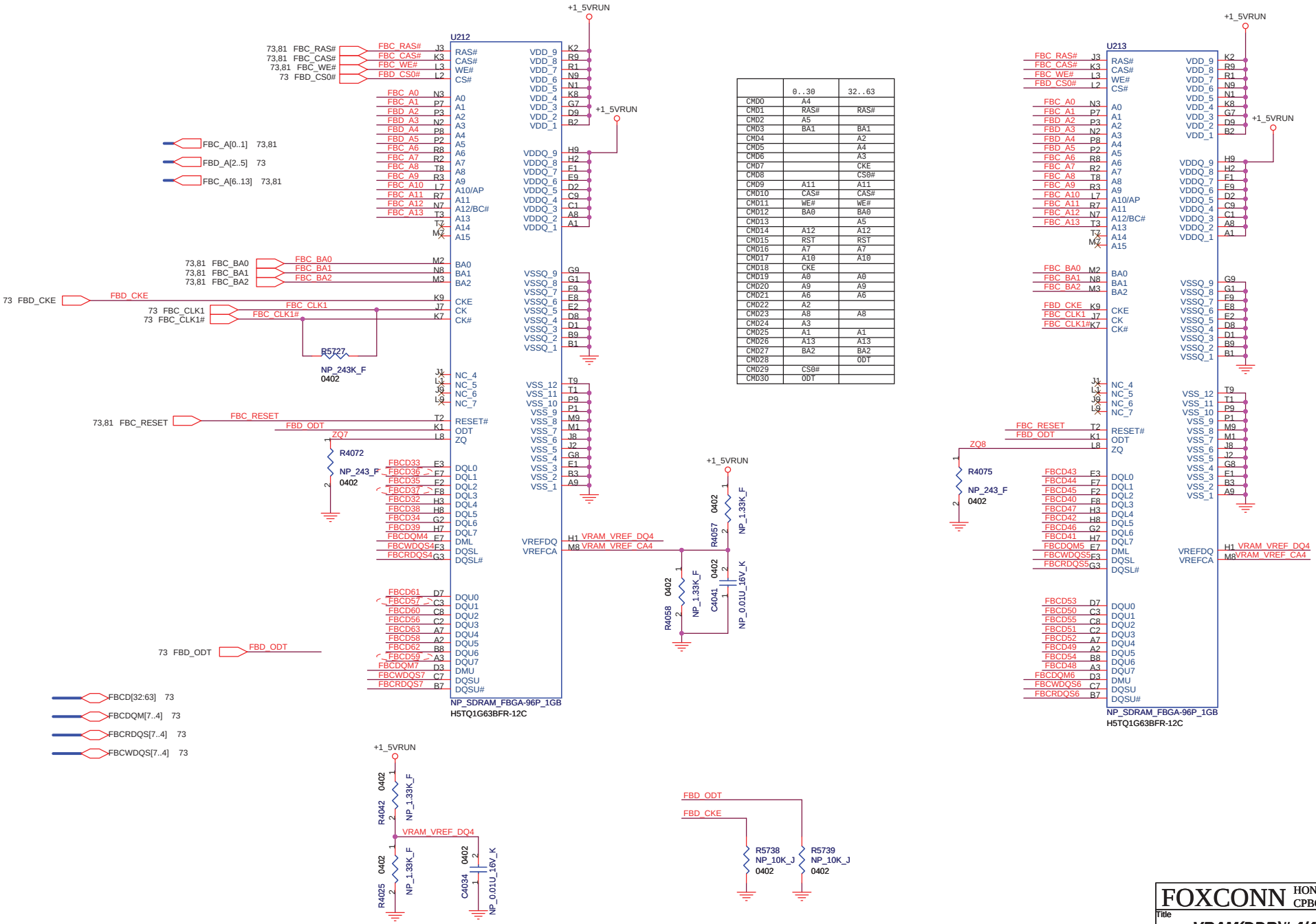
	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A3
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM(DDR)# 3/4

Size: A3 | Document Number: M930 (MBX-215) | Rev: SB

Date: Wednesday, August 12, 2009 | Sheet 81 of 96



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM(DDR)# 4/4

Size: A3 | Document Number: M930 (MBX-215) | Rev: SB

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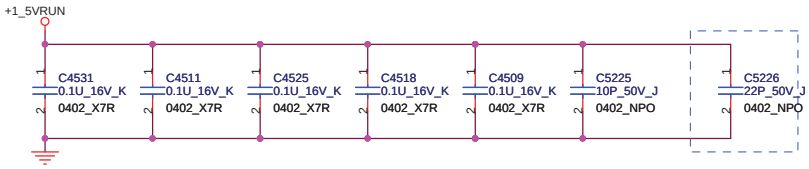
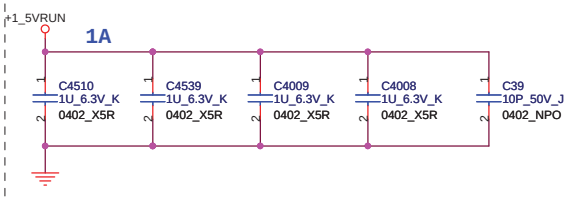
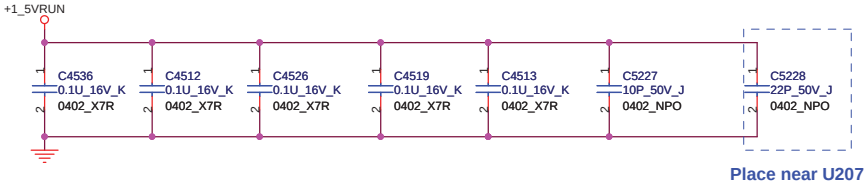
Place around the VRAM U206



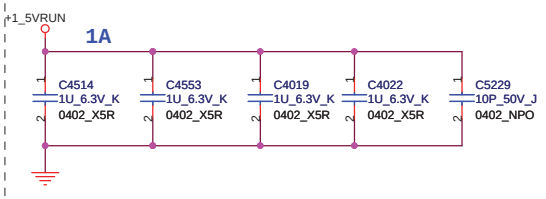
Place near U206



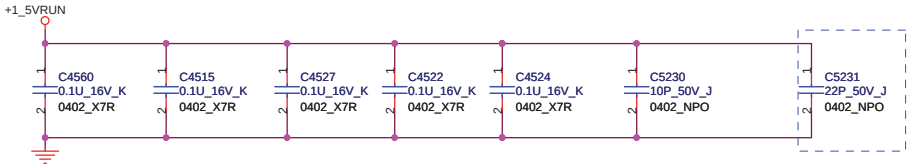
Place around the VRAM U207



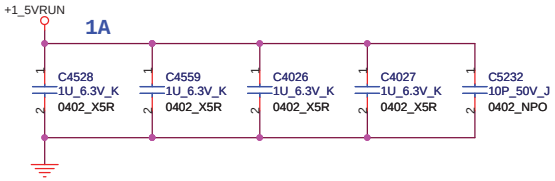
Place near U207



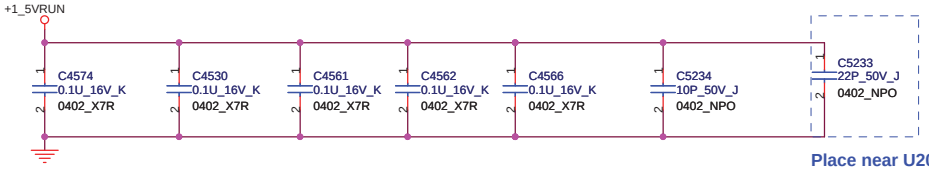
Place around the VRAM U208



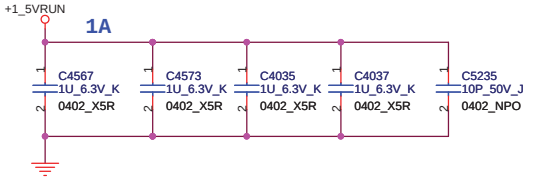
Place near U208



Place around the VRAM U209



Place near U209



PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM(N11M BYPASS) 1/2
Size A3	Document Number M930 (MBX-215)
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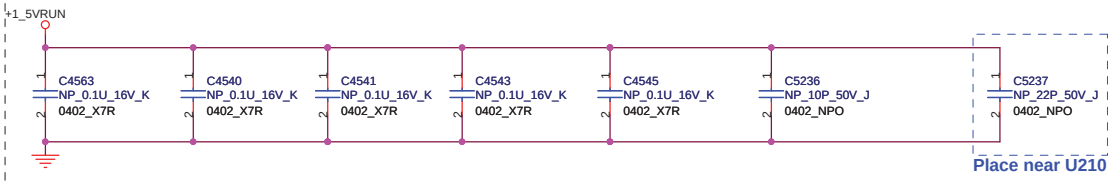
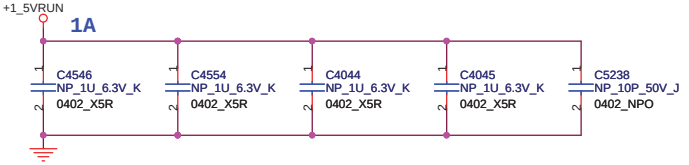
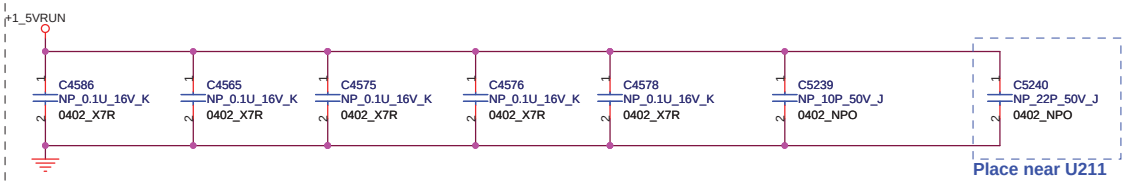
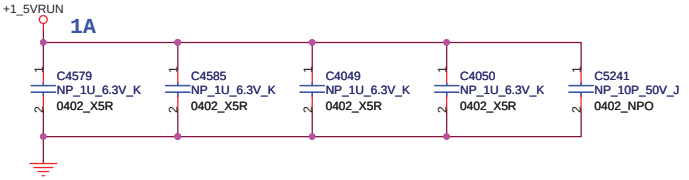
Place around the VRAM U210



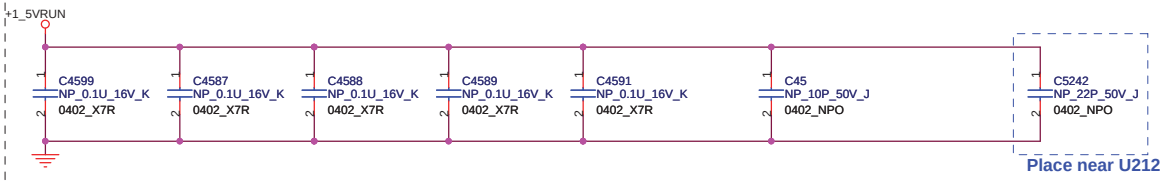


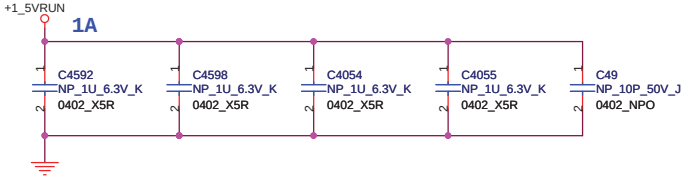
Place around the VRAM U211



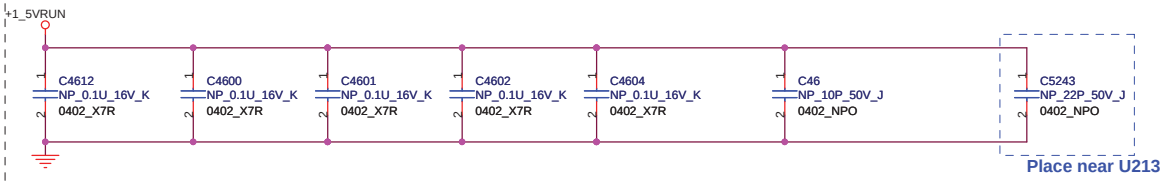


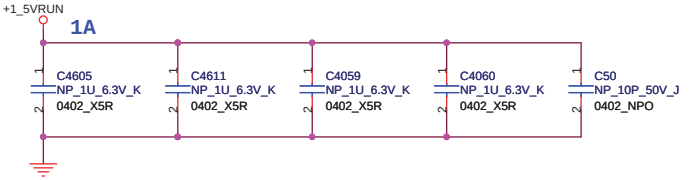
Place around the VRAM U212





Place around the VRAM U213

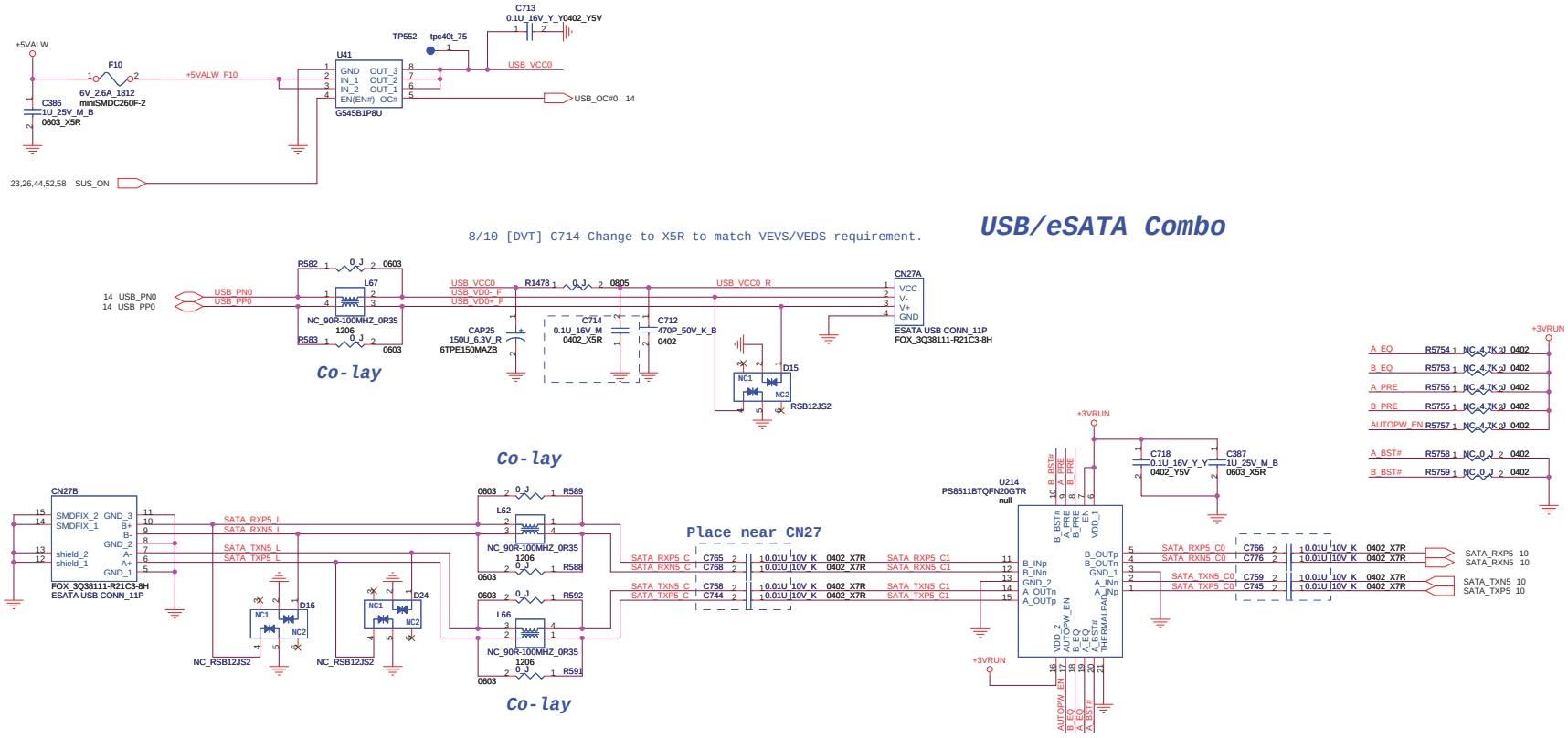




PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(N11P BYPASS) 2/2	
Size A3	Document Number M930 (MBX-215)	Rev SB
Date: Wednesday, August 12, 2009	Sheet 84 of 96	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LID SWITCH & USB/eSATA Combo	
Size C	Document Number M930 (MBX-215)	Rev SB
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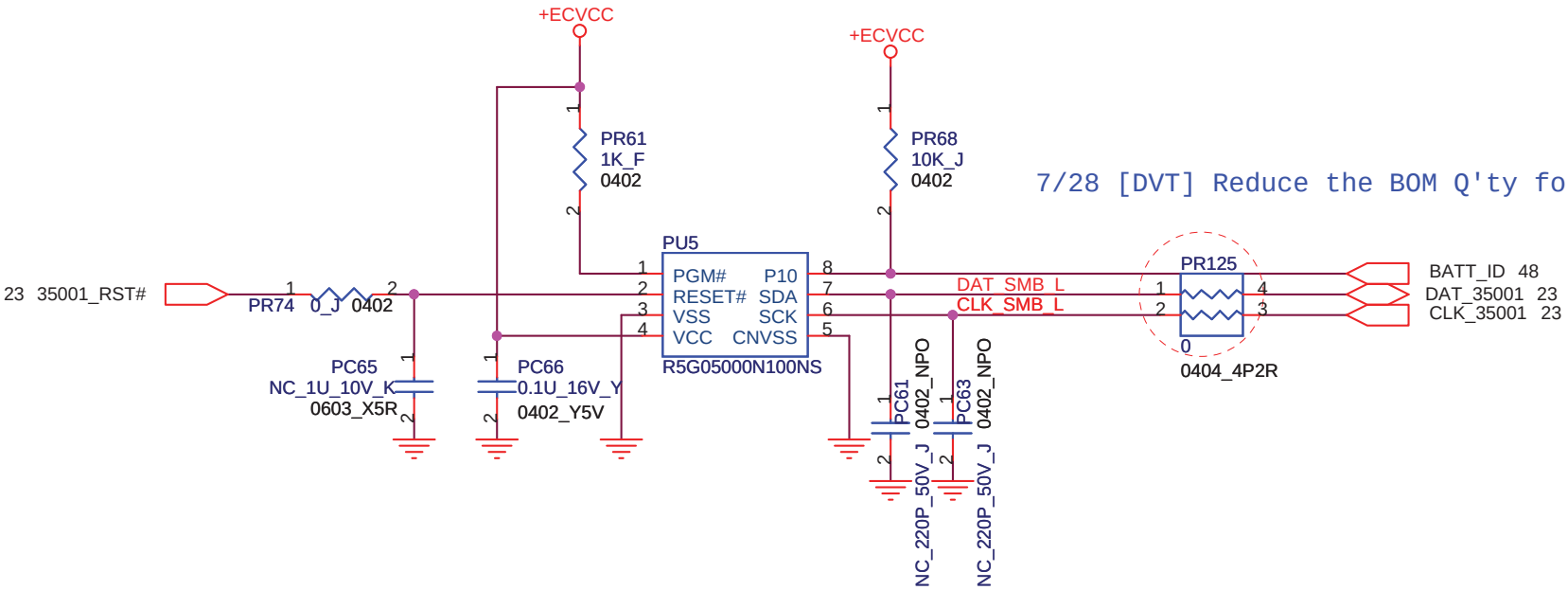
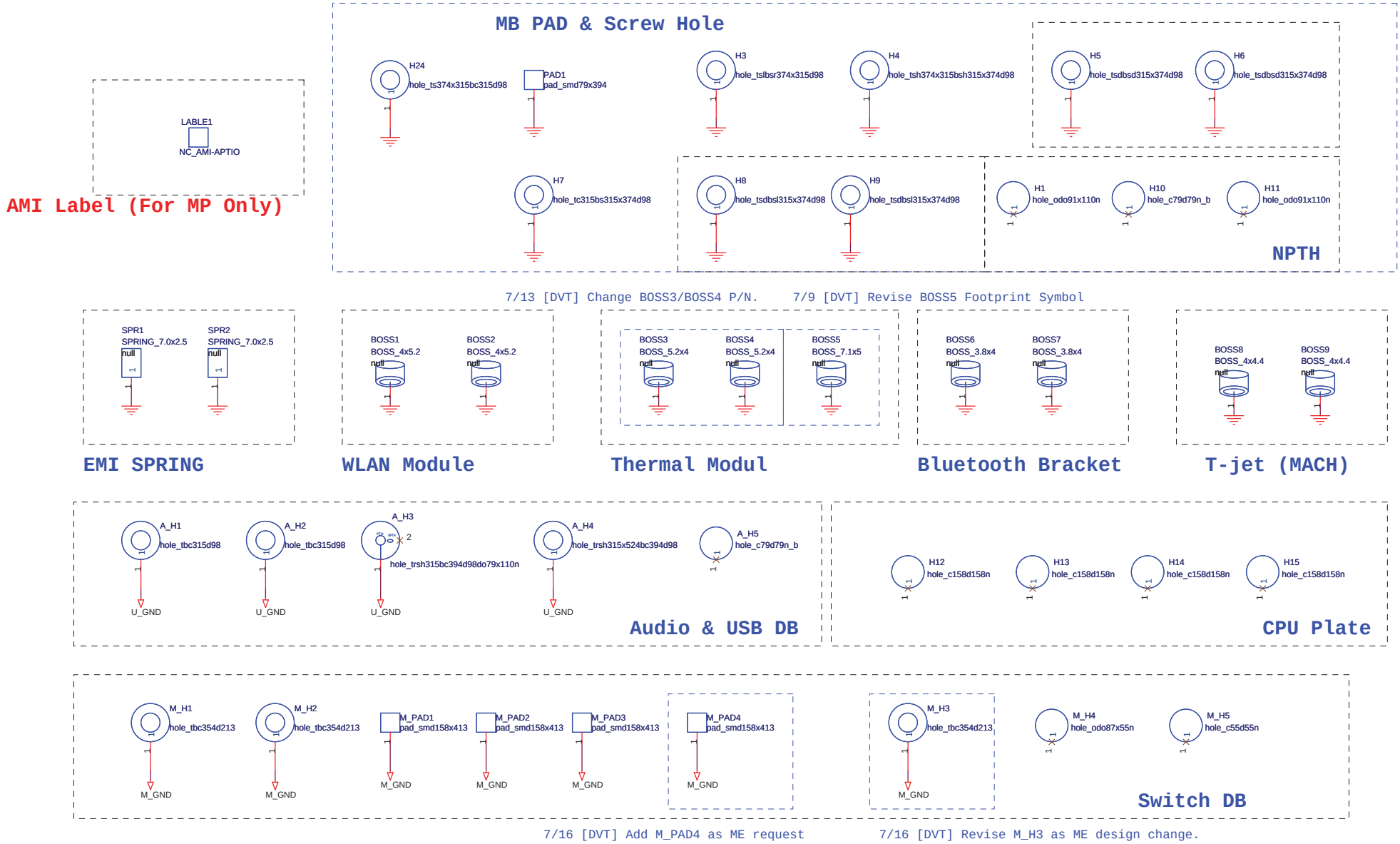


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Identify IC**	
Size A	Document Number **M930 (MBX-215)**	Rev **SB**
Date: Wednesday, August 12, 2009	Sheet 86 of 96	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE&AMI Label&BOSS	
Size A3	Document Number M930 (MBX-215)	Rev SB
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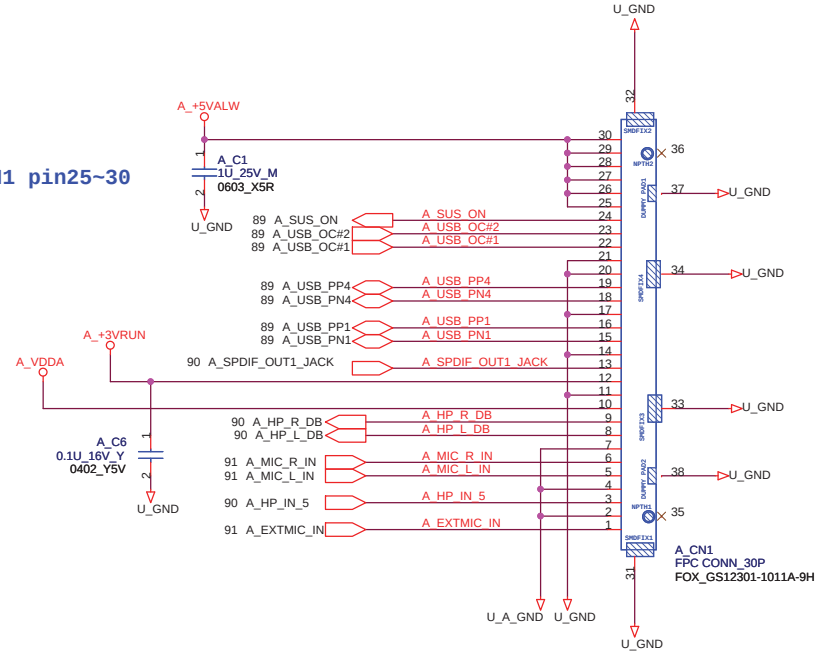
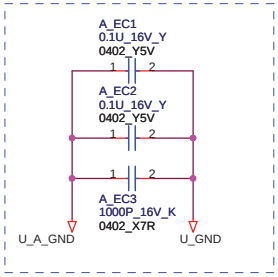
Place A_C1 close to A_CN1 pin25~30



8/5 [DVT] Add EMI Solution A_EC1~3.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB & AUDIO Conn.	
Size A3	Document Number M930 (CNX-448)	Rev SB
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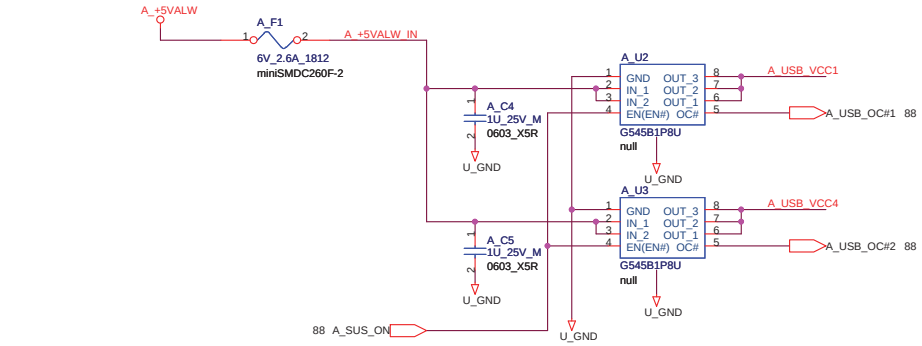
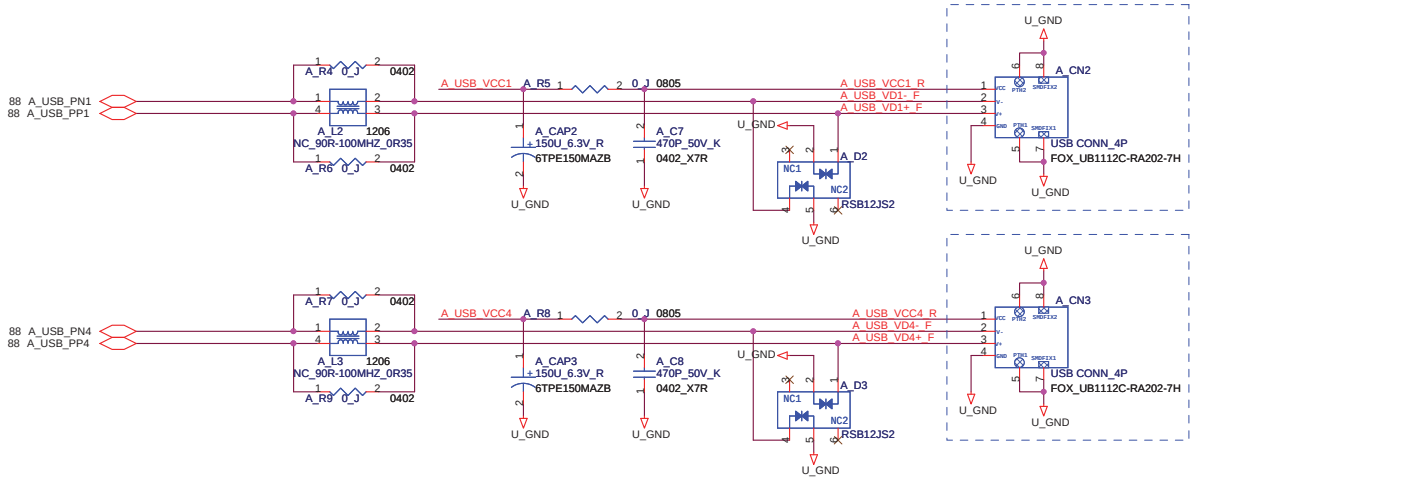


7/13 [DVT] Change A_CN2/A_CN3 to UB1112C-RA202-7H.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: USB Port		
Size: Custom	Document Number: M930 (CNX-448)	Rev: SB
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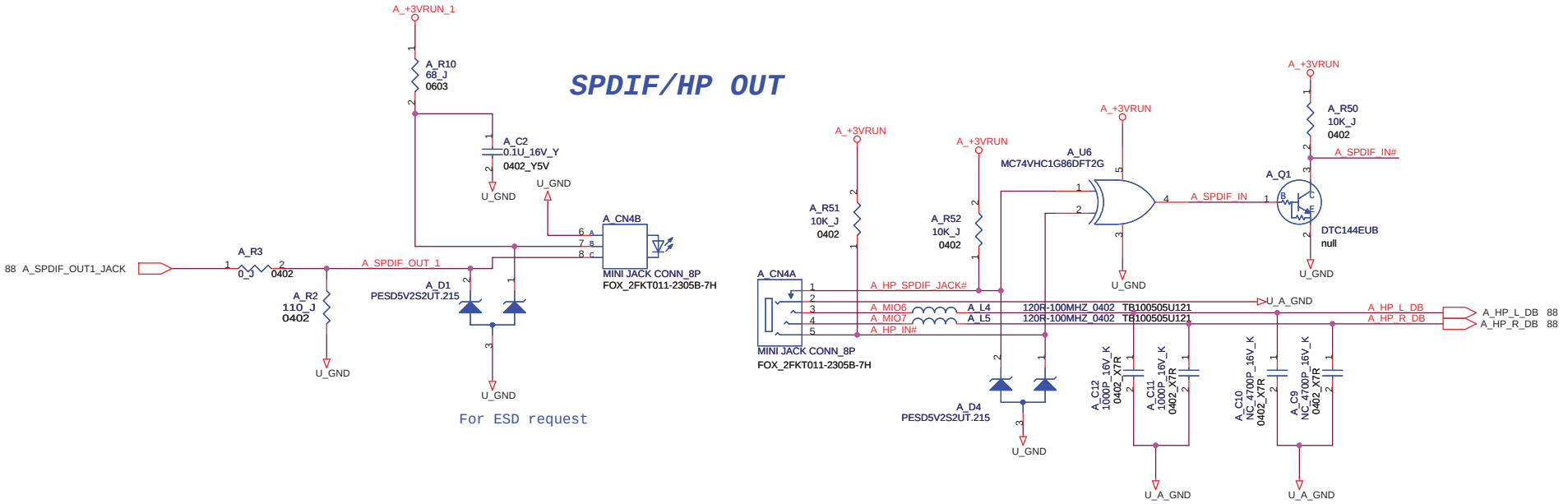
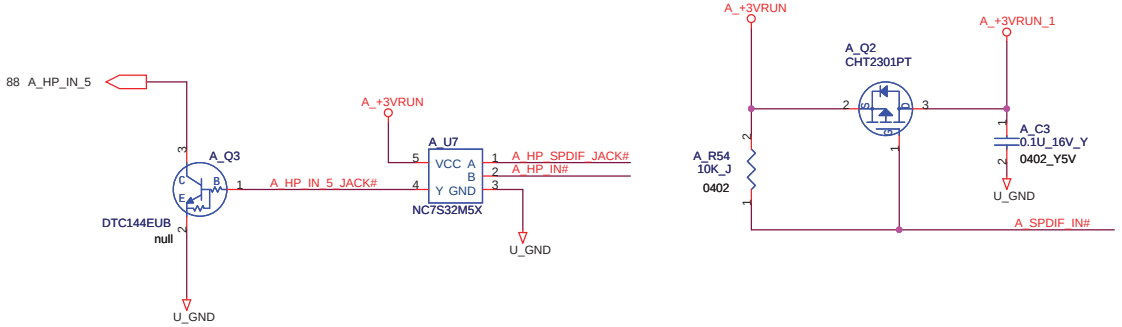
SPDIF/HP OUT





LED status

	Pin 1	Pin 5	LED A_SPDIF_IN#	A_HP_IN_5
HP	0	0	1 off	1
SPDIF	0	1	0 on	0
No plug	1	1	1 off	0

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: HP Jack (SPDIF)

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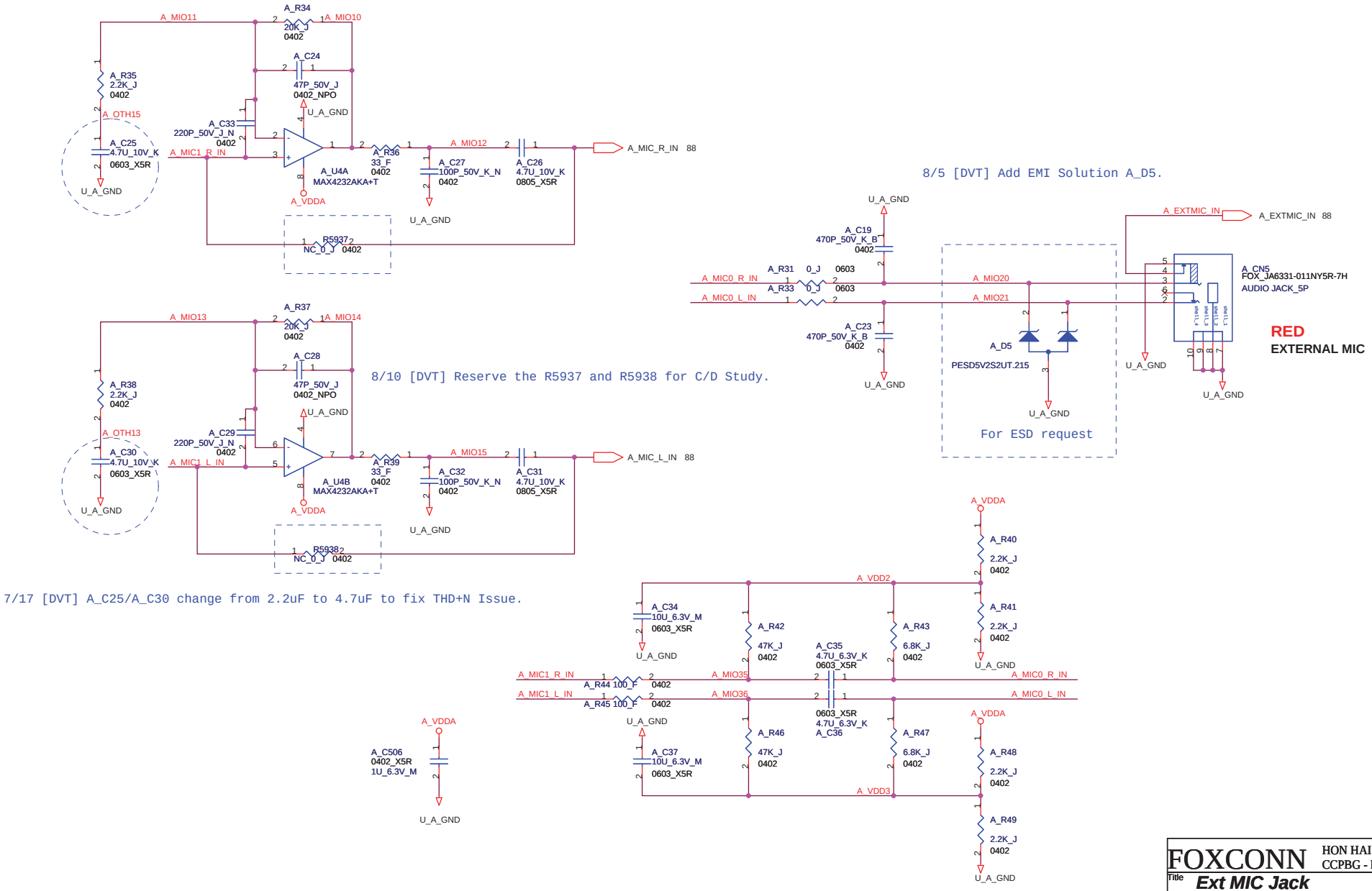

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Ext MIC Jack	
Size A3	Document Number M930 (CNX-448)	Rev SB
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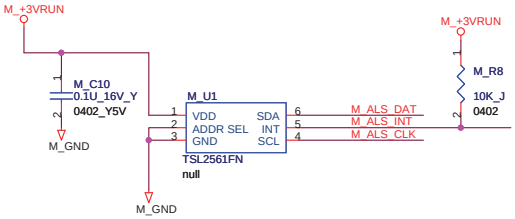
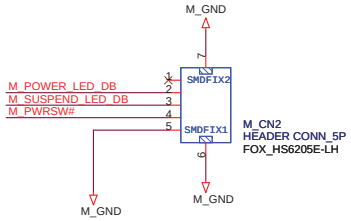


Ambinet Light Sensor (TAOS)

Slave Addr: 52h(W) , 53h(R)
(Pin2 ,Addr Select :GND)



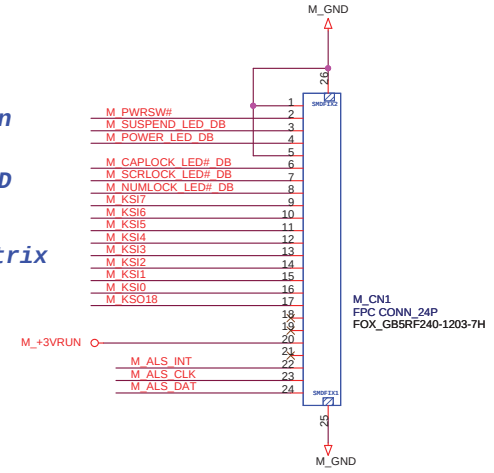
Power Button Conn

Power Button

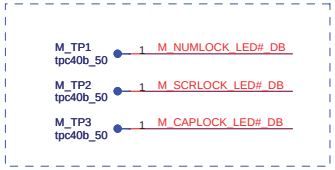
Keyboard LED

Switch Keyboard Matrix

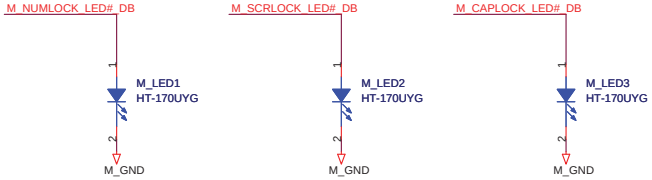
Light Sensor



Switch DB Conn

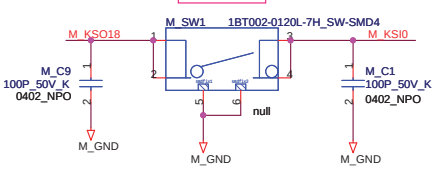


8/12 [DVT] Add Test Point for L6 Test JIG.

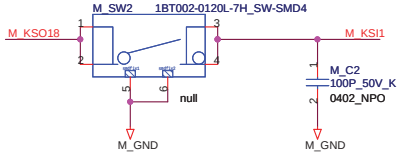


Keyboard LED

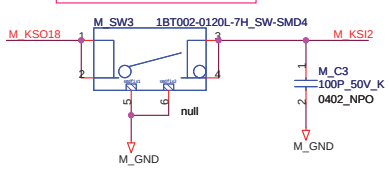
S1



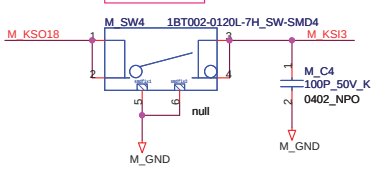
ASSIST / S2



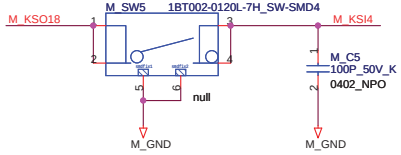
Display OFF



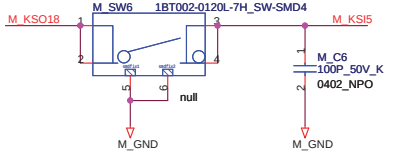
STOP



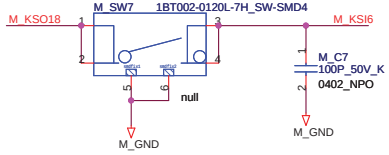
PLAY/PAUSE



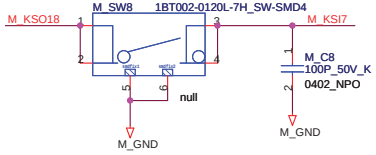
FR



FF



VAIO / S3



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(2009/04/21)
P.87 {HOLE} Add Audio&USB DB PAD
P.11 {PCH} Add R5421 PH 10Kohm to +3VALW
P.90 {SPDIF} Revise LED Status Table

(2009/04/22)
P.71 {VGA Strap} ROM_SI Table Revised
P.71 {VGA Strap} Revise R5219 value to NVH_
Revise R5199 value to NVS_
P.01 {Index} Revise M930 BOM Control Table
P.34 {PCIE(SD)} Add R820/R817 and C868/C865 for VEDS_I/F_Memory Card
P.34 {PCIE(SD)} Revise net name from SD_WP to SD_WP#
P.87 {HOLE} Add CPU Plate NPTH Hole, H12, H13 ,H14 ,H15
P.01 {Index} Add MB PCB P/N
P.41 {Backlit Conn} Revise PWM by +5VRUN
P.41 {Backlit Conn} Revise CN39 Pin2 as KB_PRESENCE
P.41 {Backlit Conn} Revise R695 from 150ohm to 0ohm

(2009/04/23)
P.91 {Ext MIC} Change A_C35,A_C36 to 4.7uF/X5R
P.10 {PCH} Change R158 from Stuff to Dummy
P.10 {PCH} Change R156 from 1Kohm to 0ohm
P.51 {VTT POWER} Change design the PQ66 logic for MOR request
(low enable voltage concern)
P.09 {MCP} Change R1272 to Dummy_3.01Kohm
P.20 {DIMM} Add CAP13_330uF for +1_5VSUS
Change CAP12 100uF to 330uF

(2009/04/24)
P.29 {LAN} Change GbE Solution to 88E8059 (7x7mm)
P.23 {EC} Add Test Point , TP185, TP277 ,TP287

(2009/04/27)
P.34 {PCIE(MS)} Add R1467 damping resistor for MS_CLK as FAE suggestion
P.34 {PCIE(MS)} Dummy R76 of SDMSXD_VCC as FAE suggestion
P.34 {PCIE(MS)} Change C540 from 1uF to 10uF as FAE suggestion
P.28 {TV} Revised PC84 location to C85
P.53 {SYS Power} Revised U85 location to PU18
P.74 {Graphic} Add Net Name for U204 ,Pin AC6 ,AK8
P.75 {Graphic} Add Net Name for U204 ,Pin AK9, AG9 ,AJ9 ,AJ8
P.77 {Graphic} Add Net Name for U204 ,Pin AE9 ,AF9
P.37 {Felica} Add Current Limit IC (U48) for MOR request.
P.67 {Audio AMP} Revise the R360 and R363 from 47Kohm to 1Kohm.
P.68 {Audio AMP} Revise the R1,R2 ,R3 ,R4 from 3.3Kohm to 8.2Kohm as MOR revised.
P.68 {Audio AMP} Add the P_GND for AMP to isolate the AMP GND plane.
P.28 {TV} Update Saturn information from MOR. Change Pin definition as Doraemon.
P.43 {Touch Pad} CN6 Swap Pin Definition for ME design review w/FFC.
P.41 {Backlit KB} CN39 Swap Pin Definition for ME design review w/FFC.
P.30 {Transformer} Delete C811 and C812 ,Change C809 GND_TR to GND.
P.85 {USB/eSATA} Add D15 and D16, D24 for signals ESD protection.
P.23 {EC} Add C418/C513 (47P) for GPIOs Expander SMbus.
P.92 {Switch DB} Add M_SW9 for ASSIST.
P.23 {EC} Change R63/R64 from 100ohm to 0ohm.
P.34 {PCIE(MS/SD)} Add 0ohm damping on the MS/SD bus and close to U71.
P.51 {VTT POWER} Revise the resistor divider value of PR505 and PR506.
P.34 {PCIE(MS/SD)} Revise the MS/SD Power Netname as MS_VDD and SD_VCC.
P.19 {CLK GEN} Delete RP86 and use 2 resistors(R584/R595)for NV_27MHz.
P.62 {HDMI} Delete RP46
P.74 {Graphic} Dummy R5694/R1229, there are the PH on Page63 already.
P.63 {CRT} Leave NC for Semi-PNP Circuit.
P.72 {Graphic} Leave NC R5560.
P.73 {Graphic} Leave NC R5561.
P.77 {Graphic} Delete R5711
P.11 {PCH} R1593 and R1594 revise to 2.2Kohm.
P.16 {PCH Power} R823 change from 0603 to 1206 for VCCIO(3A).
P.43 {Touch Pad} Change F9 to 1M-F10V0A1-F000 as MOR request (0.12A)
P.43 {Touch Pad} Reserve the +3VRUN Power Source path for Synaptics.
P.76 {Graphic} Stuff R1105 and R1106 for U204, I2C Bus.
P.45 {FAN} Revise the Direct PWM circuit. (Refer to M860)
P.74 {Graphic} As FAE suggestion, revised eDP to IFPD port.
P.77 {Graphic} As FAE suggestion, revised HDMI to IFPE port.

(2009/04/28)
P.23 {EC} Add U25 GPIOs expander and revised the GPIOs pin assignment.
P.92 {Switch DB} Add M_SW9 ,and Change the M_CN1 Pin Assignment (KSO18/KSO19).
P.40 {Switch Conn.} Change the CN2 Pin Assignment (KSO18/KSO19).

(2009/04/29)
P.35 {SD} Change the C518/C522 from Y5V to X5R.
P.28 {TV} Add the C88 and C94 for +3VRUN_CN16 ,Add C87 for +1_5VRUN_CN16 as MOR request.
P.27 {WLAN} Delete C-Link Bus as MOR request.
P.27 {WLAN} Dummy R17, Pin #24 is defined as NC on PumaPeak/KilmerPeak/Atheros modules. (MOR side comment)
P.27 {WLAN} Stuff R1560 and Remove R1557 then short to GND.
P.27 {WLAN} Leave NC U45 and C891 then add RP12 Jumper.
P.27 {WLAN} Change D1 to BD4148FPT.
P.27 {WLAN} Change Q5 to from FET to BJT(DTC144EUA).
P.61 {LVDS} Add C97 for U46 Power supply.
P.39 {BT} Change BT connector CN22 to FOX_QT510106-312H-7H.
P.4 {MCP} Change R262 from 2.2Kohm to 4.7Kohm as MOR request.
P.62 {HDMI} Change R504 from 2.2Kohm to 4.7Kohm as MOR request.
P.77 {Graphic} Add PH resistor R5699 and R1232 Bus Mater of IFPF.
P.72 {Graphic} Delete J27 pin circuit and leave NC.
P.77 {Graphic} Add Bead/Caps for IFPE Power (+3VRUN/PEX_VDD)(HDMI).
P.76 {Graphic} Leave NC R1779 as FAE suggestion.
P.71 {Graphic} R577 for Strap1 revise to 35Kohm setting (0110) as FAE PUN revised. (PUN-04335-001_v08.pdf)
P.76 {Graphic} Delete R5252 as FAE Suggestion.
P.57 {NV_VDD} Swap PWRCNTL_0 and PWRCNTL_1 Signal.
P.48 {DCIN&CHARGER} PR12 change from 51K to 59Kohm for 90W DPPM(4.2A)Revised.
P.68 {SPK} Change Bead to 0ohm for FAE Suggestion.
P.61 {LVDS} Revise PANEL_ID Table by SW Requirement.
P.70 {Graphic} Revised the U204, Pin AG19,Pin F7 from NV_VDD33 to +3VRUN as FAE suggestion.

(2009/04/30)
P.28 {TV} Add CN16, Pin1/Pin2 from EC control CIR module (Reset#/Wake#).
P.23 {EC} Add CIR Control Signal(RST# and Wake#) and Swap GPIOs Pins.
P.65 {AUDIO} Add comment when implement ALC275.
P.67 {AUDIO} Add comment when implement ALC275.
P.68 {AUDIO} Add comment when implement ALC275.

(2009/05/01)
P.11 {PCH} Revise the R566/R5420 PH Power plane to +3VSUS.

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(2009/05/04)
P.59 {OVP} Stuff PR88 and Change PC41 to 1000pF as MOR suggestion.
P.12 {PCH} Add the R927 for the MEPWROK Path (RUN_PWRGD) and Dummy R918.
393353_393353_Calpella_Power_Seq_Spec_Rev1.1 requirement.
P.87 {HOLE} Add the HOLE P/N for Switch DB.

(2009/05/05)
P.76 {Graphic} Add R2319/R2320 10Kohm PD for GPIO5 ,GPIO6.
P.All {All} Review Test Point for the BFT/Power Test and Debug usage.

(2009/05/06)
P.59 {OVP} Add PQ10 for EC Control to reduce SKU. (EVT evaluation usage)
P.48 {DCIN&CHARGER} Add PQ7 for EC Control to reduce SKU. (EVT evaluation usage)
P.23 {EC} Add R71 PD for EC_PWRLIMIT_CTRL. (U4, Pin113)
P.61 {LVDS} Add J2 and J3 for DIS_FAN_MON#. (BFT Test Usage)

(2009/05/07) - Pre-BOM 0.70
P.35 {MS/SD} Change the LED4 from Side View to Front View as ME request.
P.63 {CRT} Add R5752 for VGA_CRT_DET# for MOR Request.
P.62 {HDMI} Change R515 and R538 from 2.2Kohm to 3.9Kohm for MOR Request.
P.63 {CRT} Change R471 and R472 from 2.2Kohm to 3.9Kohm for MOR Request.
P.76 {GRAPHIC} Leave NC for R2317.
P.60 {INV Conn} Change R405 from 100Kohm to 10Kohm.
P.41 {KB} Revise the Net name from KB_PRESENCE to KB_PRESENCE#.
P.23 {EC} Revise the Net name from KB_PRESENCE to KB_PRESENCE#.
P.23 {EC} Reserve the RP23 for +3VRUN Path for Touch Pad.

(2009/05/08)
P.87 {HOLE} Revise the H1 as MERD Request
P.92 {Switch DB} Revise the M_CN1 Pin Definition as MERD Connector Design Changed.
P.75 {GRAPHIC} Leave NC for R1056,R1057.
P.75 {GRAPHIC} Leave NC for R5699,R1232.

(2009/05/11)
P.85 {USB/eSATA Combo} Add CN27A Pin1 Net Name as USB_VCC0_R.
P.48 {DCIN&CHARGER} PCN1 Connector Pin8 and Pin9 Change NPTH to PTH Grounding usage.
P.39 {BT} Add U1,R6,C6 for BT Module leakage protection.
P.23 {SODIMM VREF} Delete M2 Path as Intel Update
P.9 {MCP} Leave RP83 as NC as MOR Suggestion.
P.4 {MCP} Revised the COMP Signals Layout Notices
P.28 {TV} Change F12 from 1.5A to 2A (1812L200-C) as MOR Suggestion.
P.38 {LVDS/eDP} Add the +5VRUN Power Source for eDP requirement and add the C1364,C1365,C5260
P.10 {PCH} Add R298 the +3VALW Power for GPIO13/ GPI default usage.
P.26 {ExpressCard} L38,L39,L40 Net Swap for Layout Routing Requirement.

(2009/05/12)
P.87 {HOLE} Add PAD1 as MERD Request
P.38 {LVDS/eDP} Change C1362/C1364 from 0805 to 0603.
P.87 {HOLE} Revise the H4 as MERD Request.
P.23 {EC} Add R55/R41 PH for GPIOs Expander SMbus.
P.23 {EC} Add R57 PH for OVT_EC#
P.23 {EC} Add R59 PH for KB_PRESENCE#
P.23 {EC} Add R72 PH for EXT_INT#
P.92 {SW DB} Revise the SW Table Description and Delete M_SW9.
P.35 {SD} Change NET name SD_CLK to SD_CLK_R on C767.

(2009/05/13)
P.10 {PCH} Change CN26 Symbol of RTC BAT.
P.71 {GRAPHIC} Add N11P/N11M Device ID, 0CAF/0A75.
P.23 {EC} Delete HARD_RST#/CIR_WAKE# and Swap GPIOs
P.85 {USB/eSATA Combo} Add U214 SATA Reapter for Total Length Issue.
P.23 {EC} Add EC_IADAPT for Power Current Monitor (Reserve for EVT evaluation)
P.48 {DCIN&CHARGER} Add PR34 for EC Power Current Monitor (Reserve for EVT evaluation)
P.48~57 {Power} Change the Power Jump 1X-JUMP000-0031 as Power RD Request.

(2009/05/14)
P.87 {HOLE} Add the HOLE P/N H16~H19 for BAT/ODD Connector.
P.87 {HOLE} Add the HOLE P/N H20~H23 for ExpressCard Connector.
P.87 {HOLE} Add the HOLE P/N H24 for MB Screw.

(2009/05/15) -M930_EVT_MB_ALC275_0515-1030
P.64 {CODEC} Change Solution to ALC275 as MOR Request.
P.90 {S/PDIF} Change A_C9/A_C10 from 1206 to 0402 as Same 0.047u/X7R/0402 (NC).
P.77 {Graphic} As FAE suggestion, Connector U204K,pin AE7 and AD7 as IFPE_IOVDD.
P.75 {Graphic} As FAE suggestion, Connector U204J,pin AJ8 as IFPD_IOVDD (AK8).
Delete L2, C66,C5138,C5137,C5136
P.87 {HOLE} Update A_H3, A_H4 for USB DB PAD revised as MERD Request.
P.62 {HDMI} Delete R513 and add D25 as FAE suggestion.
P.70 {Graphic} Add C91 for NV_VDD33 as DG_v0.4.
P.63 {CRT} Change F2 to 6V-0.35A_1206 for MOR Request.
P.71 {GRAPHIC} Review the Strap Table for N10x/N11x support.

(2009/05/16)
P.48 {DCIN&CHARGER} Change PF1 to 32V-7A_1206 as PUR Suggestion.
P.10 {PCH} Delete R302 and Change R1553 to 150ohm.
P.17 {PCH} Add R1617 PH Resistor (NC).
P.10 {PCH} Add R1557 for +3VRUN Jump and D23 Leave NC on EVT evluation.
P.48 {DCIN&CHARGER} Add PR45,PR46 for EC_VADAPT for EC Power Monitor. (Reserve for EVT evaluation)
P.23 {EC} Add C6072 for EC_VADAPT Signal.
P.68 {SPK} Revise the Comment for the Cable Short circuit.
P.9 {MCP} Add NET Name for RP83, DQ_VREF0_J17 and DQ_VREF1_H17.

(2009/05/18)
P.64 {CODEC} Add R5794/R5795 for P_GND Isolation as MOR Request.
P.75 {GRAPHIC} Change the HDMI port to C as FAE Revised.
P.77 {GRAPHIC} Change the HDMI port to C and Disbale the Port E.
P.64 {CODEC} Add Q90 for Switch +5VAMP (PVDD1/PVVD2 Power Down) as MOR Request.

(2009/05/19)
P.64 {CODEC} Revise the Thermal PAD to P_GND Isolation as MOR Request.
P.64 {CODEC} Add some comment for Placement as MOR Request.
P.64 {CODEC} Change C6056/C6057/C6061/C6062 as DGND to P_GND as MOR/FAE Request.
P.64 {CODEC} Add Q90 for PVDD1/PVDD2 Power Switch when Cbale Short as MOR Request.
P.64 {CODEC} Add C368 for S/PDIF EMI concern as FAE Suggestion.
P.64 {CODEC} Add C6073 for DVDD as MOR Request.
P.65 {MUTE} Revise Q15,Pin3 as AMP_PD# from MOR Request.
P.62 {HDMI} Delete RP55/RP57/RP59/RP61 and RP72/RP73/RP74/RP75
to reduce VIAs and add the common mode filter for dGPU as MOR
Request.
P.75 {Graphic} Change IFPC port as HDMI as FAE revised.

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(2009/05/20)

P.64 {CODEC} Change U215 HW_POP_MUTE_CODEC to Pin28 (GPIO2) as MOR Request.
P.69 {TSUB/MACH} Add Q22 for the Module Leakage Concern as MOR Request. (Revised)
P.62 {HDMI} Delete RP53 to avoid the Stub as MOR suggestion.
P.45 {FAN} Reserve the R404 PH resistor.

(2009/05/21)

P.All {All} Change/Review All the Connector to Halogen Free.
P.95 {NV_VDD} Change the PU29 Solution to TPS51217DSCR.
P.51 {PCH Power} Change the PU26 Solution to TPS51218DSCR.
P.23 {EC} Revise the Model_ID Table.
P.23 {EC} Set Model ID to N11x Default.
P.71 {Graphic Strap} Set Strap2 to N11x Default. (Need to Change R value when used N10x.

(2009/05/22)

P.29 {LAN} Change the GbE Solution to Co-Lay 88E8057 and 88E8059 (7mmx7mm)
P.35 {SD} Change the SD LED4 Part.
P.42 {Status LED} Change the LED1, LED2 ,LED3 Part.

(2009/05/23)

P.60 {INV} Change R400 to 10Kohm and Stuff.
P.76 {VGA} Change R2318 to Dummy.

(2009/05/23)

P.90 {HP} Change A_C11 and A_C12 from 0.015uF to 1000pF as MOR suggestion.
P.90 {HP} Change A_C9 and A_C10 from 0.047uF to 4700pF as MOR suggestion.

(2009/05/27)

P.71 {VGA} Revised the N11P/M Device ID for ES Sample ONLY .
N11P-GS1 (ES) : 0A3D
N11M-GE1 (ES) : 0A7D

(2009/06/04)

P.34 {MS} BOM Change R76 as Mount and C540 change to 1uF (1C-2B30105-K002).
P.71 {VGA} Revised the N11P/M Device ID for ES Sample ONLY .
N11P-GS1 (ES) : 0CAD
Revised the N10x/N11x 3GPIO as 1110.

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(2009/06/24)
P.23 {EC}Add 0.01uF C6078 for EC_IADAPT.
P.23 {EC}Add R47/10Kohm for MB_FLASH_EN.
P.41 {Backlit}EC Engineer Request, for Backlit conctrol well (+5VALW).
P.19 {CLK}U31 Change to SLI - E version.

(2009/07/08)
P.3 {MCP}Delete iGPU, Leave FDI BUS NC.
P.3 {MCP}Delete iGPU, Tied the FDI_SYNC 1Kohm to GND.
P.3 {MCP}Delete iGPU, Set the FDI_INT 1Kohm to GND.
P.4 {MCP}Delete iGPU, Set U67, A17/A18 pin to GND.
P.7 {MCP}Delete iGPU, Set VAXG to GND.
P.7 {MCP}Delete iGPU, Set SENSE and Graphice VIDs as NC.
P.9 {MCP}Support M1/M3 Path for Common Motherboard Deisgn and Stuff RP83.
P.11 {PCH}Change R902/R903 PH Power Rail to ALW.
P.11 {PCH}Delete the Dummy parts and short 0ohm. Change the U69, Pin C8/H14 Net name.
P.12 {PCH}Delete iGPU, Leave FDI BUS NC.
P.13 {PCH}Delete iGPU, Leave LVDS/CRT/DDI BUS NC.
P.14 {PCH}Change R308 from 22.6ohm to 20ohm to fix the USB Eye Diagram Issue.(BIOS: Long Topology)
P.16 {PCH}Delete iGPU, Delete CA_ Dummy Parts.
P.17 {PCH}Delete iGPU, Delete CA_ Dummy Parts.
P.17 {PCH}Delete iGPU, LVDS I/F Short to GND.
P.20 {DDR3}Support M1/M3 Common Motherboard Design
P.21 {DDR3}Support M1/M3 Common Motherboard Design
P.26 {ExpressCard}Short 0ohm for C/D.
P.27 {WLAN}Dummy R1560.
P.34 {CardReader} CN36 ,Change Damping value to fix the OS/US issue.
P.35 {CardReader} CN29 ,Change Damping value to fix the OS/US issue.
P.37 {Felica} C152, Change from 1206 to 0805 for Placement issue.
P.38 {eDP/LVDS} As MOR request, Defined the NEW Pin-out.
P.45 {FAN} Change the FAN Pin-Out Definition.
P.45 {FAN} Drive Out the PWM by EC Directly.
P.46 {Thermal} Dummy HW Thermal Protection G709 Function.
P.46 {Thermal} Change the U26,Pin6 Net name.
P.51 {VTT&PCH Power} Change OCP setting adjust PR113 to 56Kohm.
P.52 {DDR3 Power} Aovid the Sequence concern, from Sus rail to ALW.
P.54 {CPU VHCORE} Reserved CAP30/31 for Power Solution.
P.54 {CPU VHCORE} PR555,PR557 Compensation Adjustments.
P.54 {CPU VHCORE} PR569,PR575 Compensation Adjustments.
P.55 {CPU VID} Follow the ARD/CFD EDS Setting to set as SV type.
P.56 {VGFX Power} Delete iGPU, Delete Dummy Parts.
P.57 {VGAPower} Change OCP setting adjust PR566 to 56Kohm.
P.57 {VGAPower} PR222, PR229 Feedback Loop Adjustment
P.59 {OVP} Dummy the PWRLIMIT HW Control , Used the SW Monitor Proposal
P.60 {INV} Delete iGPU, Delete Dummy Parts.
P.61 {LVDS} Delete iGPU, Delete Dummy Parts.
P.62 {HDMI} Delete iGPU, Delete Dummy Parts.
P.63 {CRT} Delete iGPU, Delete Dummy Parts.
P.64 {Audio} Change U126 from OR gate to AND gate.
P.69 {T-JET} Add C5127 Cap.
P.74 {VGA} Change to NC, when support eDP stuffed.
P.74 {VGA} Short 0ohm , R2319,R2320 Change Net name.
P.85 {LID} Change U21 to EC2648-B3-G.

(2009/07/09)
P.26 {Expresscard}Revise the CN10 Footprint symbol for Screw PAD.
P.29 {LAN}Change the C988, C989 CL value to 12P.
P.87 {BOSS}Revise BOSS5 Footprint Symbol
P.35 {CardReader} U22 Change to G553E1P11U.
P.34 {CardReader} Change C785/C786 value to 24P depends on Cystal report.

(2009/07/13)
P.4 {MCP}Change U67 Socket to 988A(PZ98827-364A-01F)
P.54 {CPU VHCORE} PR598 Loadline Fine Tune.
P.54 {CPU VHCORE} Add TP377 for L6 Power Test Usage.
P.89 {USB} Change A_CN2/A_CN3 to UB1112C-RA202-7H.
P.28 {TV} CN16 change to GB12501-10510-7H
P.87 {BOSS} Change BOSS3/BOSS4 P/N as ME request.
P.66 {Audio} Add Test Point TP379.
P.64 {Audio} Add Test Point TP327 ,TP378 ,TP380.
P.60 {INV}10pins (CN40) and 6 Pins (CN5) Inverter Connector Co-Lay for eDP support.
P.57 {VGAPower} Add the TP221/TP248.

(2009/07/15)
P.10 {PCH}Change U98 to MX25L3205DM2I-12G.
P.61 {LVDS} Delete U46 to fix the DISPLAY OFF function issue.
P.61 {LVDS} Change R136 from 100Kohm to 10Kohm.
P.24 {SPI} U23 change to MX25L1005CMI-12G.

(2009/07/17)
P.91 {Audio} A_C25/A_C30 change from 2.2uF to 4.7uF to fix crosstalk issue.
P.59 {OVP} PR167 change to 26.1Kohm, PR169 change to 80.6Kohm
,PR171 change to 18.2Kohm for OVP Adjust.

P.54 {CPU VHCORE}PR565 change to 1.8Kohm, PC566 change to 0.022uF for IMON Adjust.
P.87 {HOLE}Revise M_H3 as ME design change.
P.87 {HOLE}Add M_PAD4 as ME request.
P.29 {LAN} Change the Y6 to 25MHZ_12P_30PPM.
P.23 {EC}C26/C27 change to 18pF.

(2009/07/23)
P.91 {Audio} Change R342 PH Power Plane to avoid Q90 abnormal behavior.
P.17 {PCH} VSSA_LVDS leave NC.
P.26 {ExpressCard} Add R345 for MOR request. (Reserve)

(2009/07/24)
P.4 {MCP}Change R1261 to Stuff as MOR request.
P.4 {MCP}INTEL S3 Power Reduction Solution Implement.
P.7 {MCP}INTEL S3 Power Reduction Solution Implement.
P.9 {MCP}INTEL S3 Power Reduction Solution Implement.
P.15 {PCH}INTEL S3 Power Reduction Solution Implement.
P.49 {Discharge} INTEL S3 Power Reduction Solution Implement.
P.52 {DDR3 Power} INTEL S3 Power Reduction Solution Implement.
P.12 {PCH}Change R911 to 10Kohm as MOR request.
P.4 {MCP}RP81, RP82 change to Array for C/D.
P.26 {ExpressCard}Short R677,R683,R682,R685 0ohm for C/D.

(2009/07/27)
P.12 {PCH}Dummy the R921 for ME function support and avoid the leakge concern.

(2009/07/28)
P.79 {VRAM} U207 ,Data Pin Swap
P.80 {VRAM} U208 ,Data Pin Swap
P.81 {VRAM} U211 ,Data Pin Swap
P.82 {VRAM} U212 ,Data Pin Swap
P.15 {PCH}RP90, RP95 ,RP96 for Reduce BOM Q'ty.
P.10 {PCH}RP93, RP94 for Reduce BOM Q'ty.
P.20 {DDR3}RP91 for Reduce BOM Q'ty.
P.23 {EC}RP92 for Reduce BOM Q'ty.
P.86 {Identify IC}PR125 for Reduce BOM Q'ty.
P.12 {PCH}Reserve R930 for Leakage Check.
P.7 {MCP}INTEL S3 Power Reduction Solution Implement Revised.
P.49 {Discharge} INTEL S3 Power Reduction Solution Implement Revised.

(2009/07/29)
P.35 {CardReader} Change R391 to 100K as VEDS.
P.27 {WLAN}Short R20.
P.49 {Discharge} INTEL S3 Power Reduction Solution Implement Revised.
P.51 {VTT&PCH Power} Change PR123 to 1Kohm
P.51 {VTT&PCH Power} Change PR160 to 1Kohm (NC)
P.57 {VGAPower} Change PR176 to 1Kohm (NC)
P.20 {DDR3} INTEL S3 Power Reduction Solution Implement Revised.
P.21 {DDR3} INTEL S3 Power Reduction Solution Implement Revised.

(2009/07/30)
P.51 {VTT&PCH Power} Change PR44 to 2.2ohm.
P.52 {DDR3 Power} Add PR41 and PC42 for PWM Setting.
P.57 {VGAPower} PR70 Change to 2.2ohm for PWM setting.
P.57 {VGAPower} Add PR163 and PC133 for PWM Setting.
P.54 {CPU VHCORE} Change PR597 to 16.5Kohm for IMON Fine Tune.
P.48 {DCIN&CHARGER} Delete PR657.

(2009/07/31)
P.12 {PCH}Add Q7 as MOR request.

(2009/08/03)
P.09 {MCP} Stuff R1582.
P.27 {WLAN}Reserve R22 for MOR request.
P.74 {VGA} Revise the Strap Pin value as FAEprovided for DVT Sample.
- N11P-GE1 x0A29
- N11M-GE1 x0A75

P.53 {+1_8V SYSPower}Fine tune RC (PR585/PC250) const.
for NVVDD Sequence Request.
P.64 {Audio} Reserve the ALC275/ALC269 BOM Mount Option.
P.57 {VGAPower} Set the P-state for N11P-GE1/N11M-GE1 QS Sample Requirement.
P.53 {+1_8V SYSPower}Change PR587 set the Vo value.
P.58 {Other Power}Change PQ44/PQ50 to IRF8736PBF.

(2009/08/04) - Pre-BOM 0.80
P.60 {INV} Delete R687 and R684 as MOR request.
P.76 {VGA} Add Test Point for eDP.
P.76 {VGA} Change R2330/R2331 for C/D thermal sensor.(DVT Verify)
P.75 {VGA} Delete Q72 as MOR request.
P.14 {PCH} Remove Braidwood (Intel Updated and MOR confirmed)
P.33 {Braidwood} Remove Braidwood (Intel Updated and MOR confirmed)

(2009/08/05)
P.76 {VGA} Stuff R5705 as FAE Request.
P.35 {CardReader}Dummy C767 and Change R1465 to 33ohm.
P.48 {DCIN&CHARGER} Add EC6~9 for EMI Solution.
P.29 {LAN} Add EC10~16 for EMI Solution.
P.88 {DB Connector} Add A_EC1~3 for EMI Solution.
P.91 {Audio} Add A_D5 for EMI Solution.
P.48 {DCIN&CHARGER} Change PQ32 EMI Solution.

(2009/08/10)
P.30 {LAN} Change the L70 to NS692412 to improve EMI.
P.64 {Audio}Add EC17 and EC19 ,EC21,EC22 for EMI Solution.
P.64 {Audio} Change R5782 to 100kohm to decrease and BEEP sound level as MOR request.
P.64 {Audio} Dummy U217 and C6063 for C/D as MOR request.
P.64 {Audio} Reserve the R5934 for C/D as MOR request.
P.64 {Audio} Delete the U215 SMB Connection.
P.65 {Audio} Add the comment for " If use ALC269 Codec, these parts should be Mount."
P.68 {Audio} Reserve the L-ch parts and add R5936 for C/D as MOR request.
P.85 {USB} C714 Change to X5R to match VEVS/VEDS requirement.
P.26 {ExpressCard}Add R636 for MOR request. (Reserve)
P.39 {BT} As MOR request, Stuff the R7 Path.
P.39 {BT}As MOR request, Add R5939 for Clock.

(2009/08/12)
P.4 {MCP}Stuff R5926 to avoid the Q73 Floating.
P.7 {MCP} Add R1561 0ohm and change C6080 to 0.01uF as INTEL update.
P.7 {MCP}INTEL White Paper0.9 Check List Request of Q55.
P.15 {PCH}Add R934 ,Follow INTEL S3 Check List 0.9. (GPO)
P.52 {DDR3 Power} Change PR39 for PWM Setting.
P.58 {Other Power}Dummy PQ44 to IRF8736PBF.
P.29 {LAN} Change the Y6 to E5FA25.0000F12D33.

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CCPBG - R&D Division
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