Schematics Page Index (Title / Revision / Change Date)

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03	Penryn(HOST BUS) 1/3	1.0	09'02'26	38	Audio (CODEC & POWER)	1.0	09'02'26
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11	Cantiga (POWER,VCC) 5/7	1.0	09'02'26	46	CAMERA/Int MIC.	1.0	09'02'26
12	Cantiga (VCC CORE) 6/7	1.0	09'02'26	47	Felica & Modem	1.0	09'02'26
13	Cantiga (VSS) 7/7	1.0	09'02'26	48	USB2.0	1.0	09'02'26
14	DDRII(SO-DIMM_0) 1/2	1.0	09'02'26	49	Bluetooth	1.0	09'02'26
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16	VGA (PCI-E) 1/6	1.0	09'02'26	51	Power Board MB CONN	1.0	09'02'26
17	VGA (Strap) 2/6	1.0	09'02'26	52	HOLE	1.0	09'02'26
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19	VGA (Memory BUS) 4/6	1.0	09'02'26	54	DCIN&Charger	1.0	09'02'26
20	VGA (LVDS) 5/6	1.0	09'02'26	55	SYS Power (+3_3V/+5V)	1.0	09'02'26
21	VGA (Power) 6/6	1.0	09'02'26	56	SYS Power(+1_5V/+1_05V)	1.0	09'02'26
22	VRAM (GDDR3) 1/2	1.0	09'02'26	57	DDR2 Power(+1_8V/+0_9V)	1.0	09'02'26
23	VRAM (BYPASS) 2/2	1.0	09'02'26	58	CPU_Vcore---ISL6266A	1.0	09'02'26
24	CRT	1.0	09'02'26	59	Others power plane	1.0	09'02'26
25	LVDS	1.0	09'02'26	60	OVP protection	1.0	09'02'26
26	HDMI	1.0	09'02'26	61	VGA Power(ATI VDD)	1.0	09'02'26
27	ICH9-M (PCI/USB) 1/5	1.0	09'02'26	62	Audio+USB DB CONN	1.0	09'02'26
28	ICH9-M (LPC,IDE,SATA) 2/5	1.0	09'02'26	63	Audio (HP, MIC Jack)	1.0	09'02'26
29	ICH9-M (GPIO) 3/5	1.0	09'02'26	64	Power Board DB & CONN	1.0	09'02'26
30	ICH9-M (POWER) 4/5	1.0	09'02'26	65	USB DB	1.0	09'02'26
31	ICH9-M (GND) 5/5	1.0	09'02'26	66	History (1)	1.0	09'02'26
32	SATA HDD/ODD	1.0	09'02'26	67	History (2)	1.0	09'02'26
33	EC+KBC (WPCE775L)	1.0	09'02'26	68	History (3)	1.0	09'02'26
34	Flash ROM/SPI	1.0	09'02'26	69	History (4)	1.0	09'02'26
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Project Code & Schematics Subject: M850 Main Board_8L

PCB P/N:	1P-0094J00-8011(IRIS) 1P-0094500-8011(HANNSTAR)
A+U/B P/N:	1P-1094J01-8011(IRIS) 1P-1094501-8011(HANNSTAR)
P/B P/N:	1P-1094J00-8011(IRIS) 1P-1094500-8011(HANNSTAR)

P. Leader	Check by	Design by

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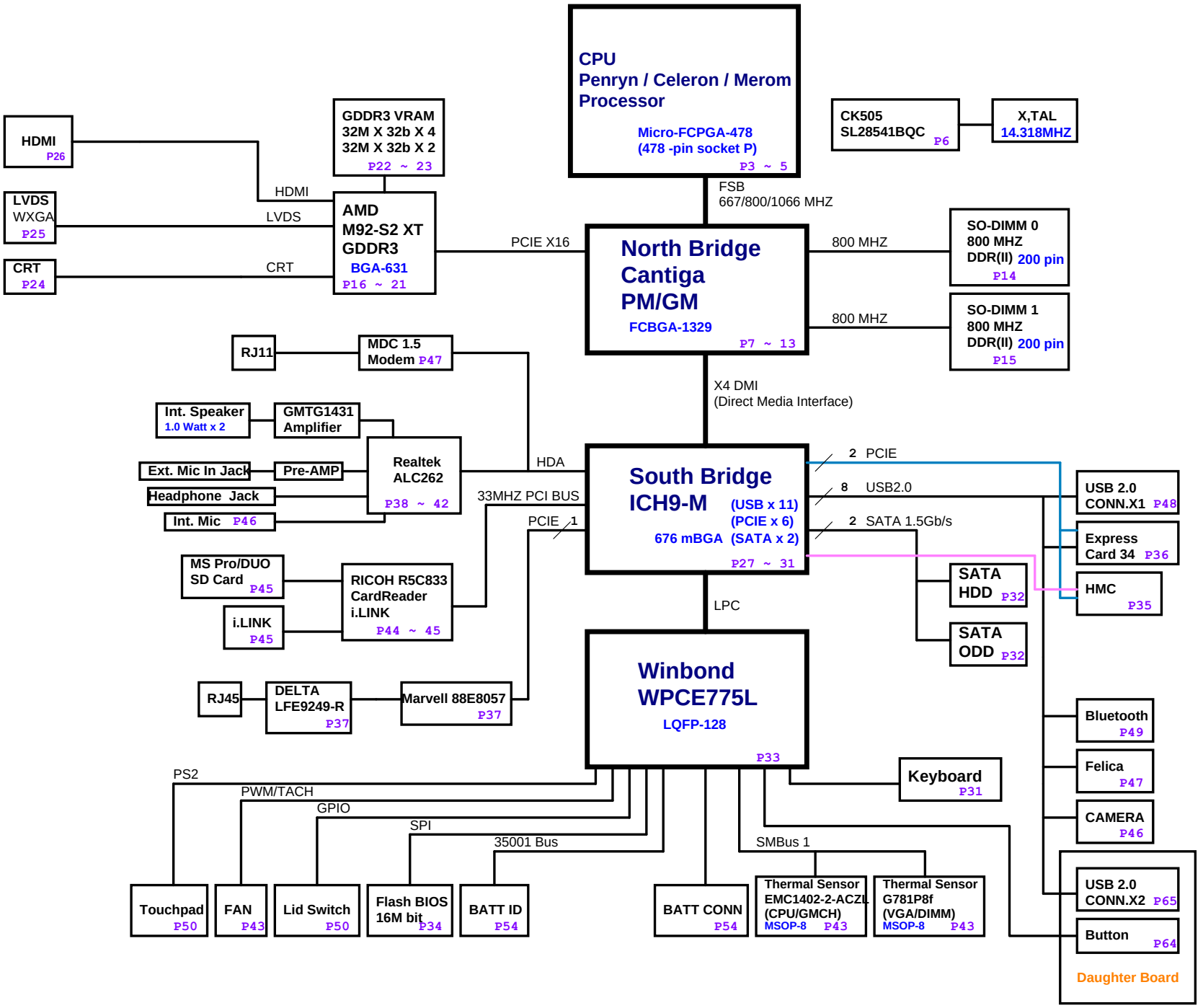
M851(Montevina + M92-S2 XT)

AT_ External Graphic



TI CHARGER BQ24751 P.54

	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC TPS51125RGER P.55

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +1.5V_ALW

SYSTEM DC/DC SC411 P.56

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM

SYSTEM DC/DC TPS51116RGER P.57

INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS +0_9VSUS

CPU DC/DC ISL6262A P.58

INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC APL5913 P.61

INPUTS	OUTPUTS
+1_5VRUN	PEX_VDD

SYSTEM DC/DC SC411MLTRT P.70

INPUTS	OUTPUTS
DCBATOUT	AT_VDD

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Title: Block Diagram

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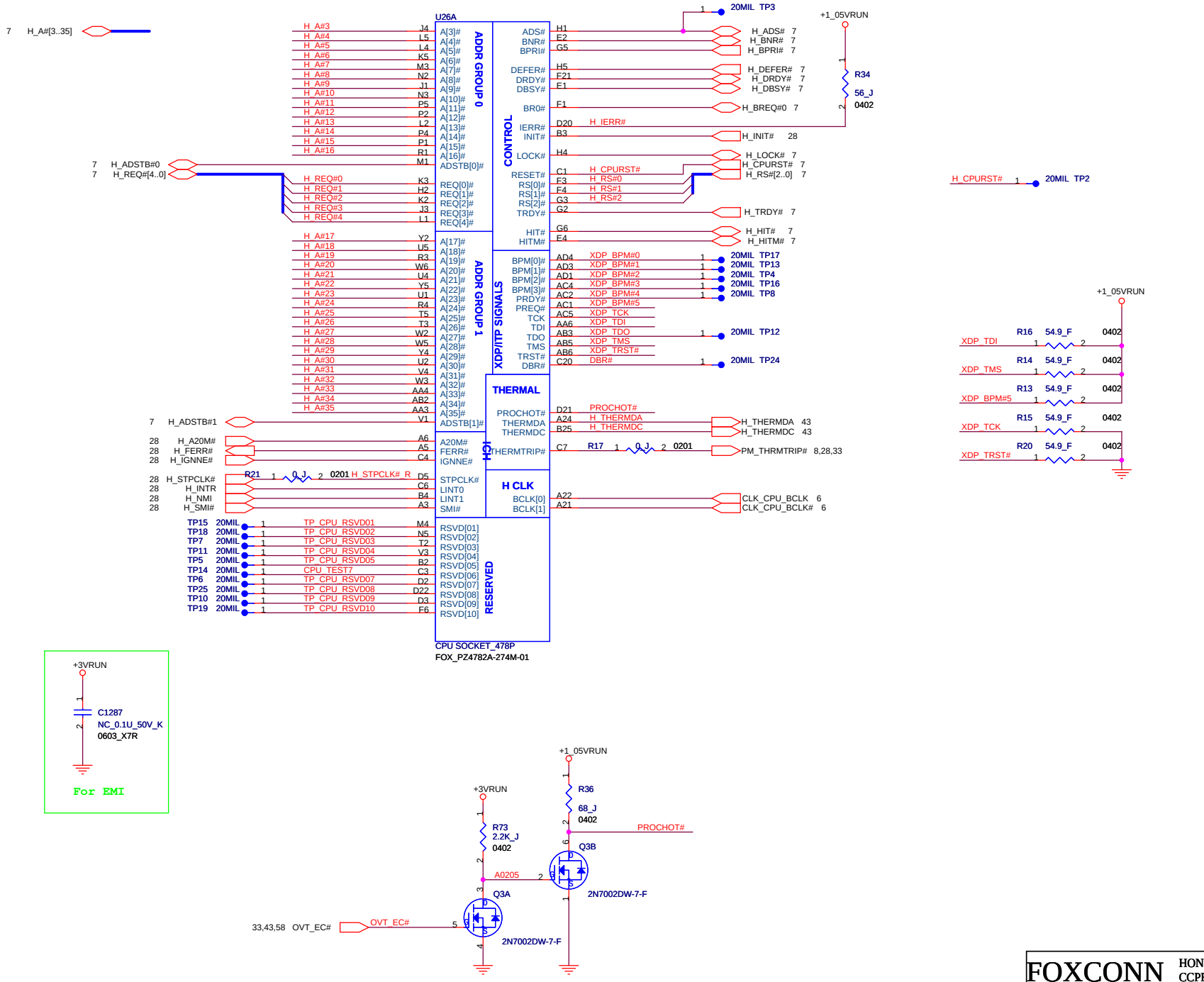
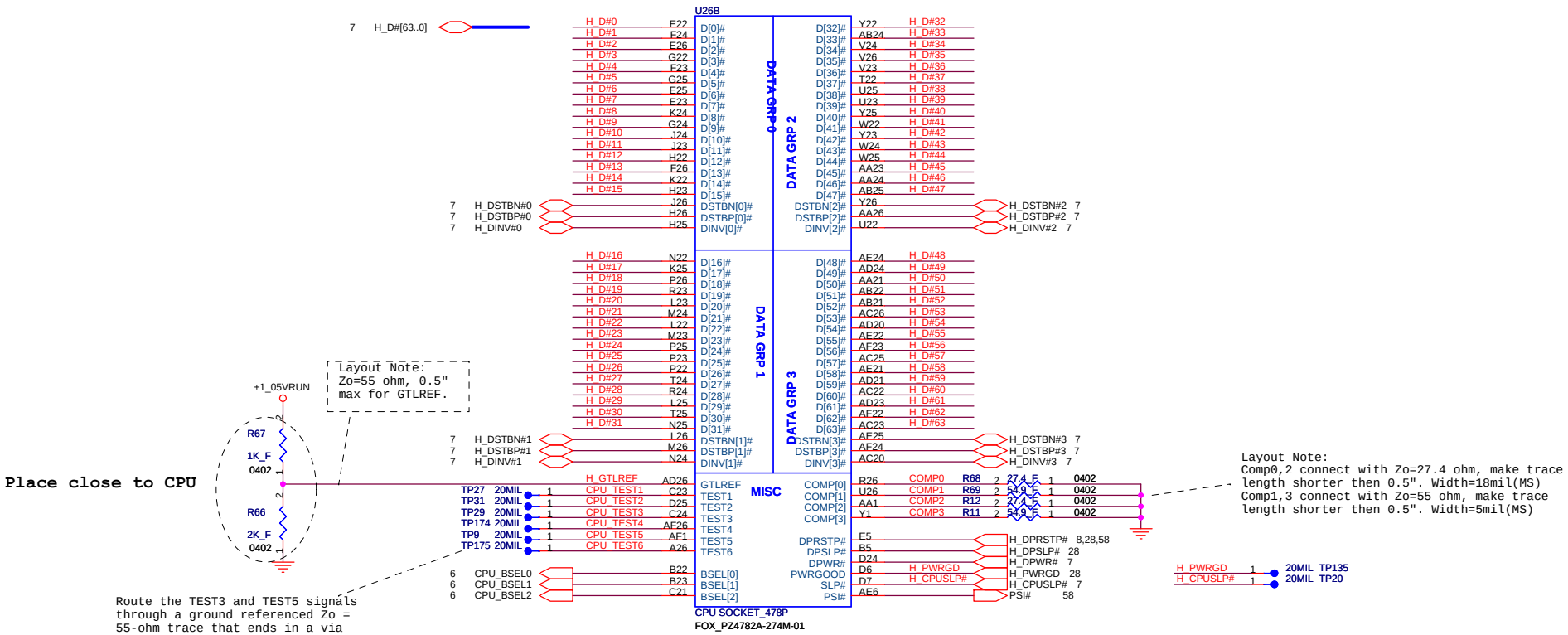


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Penryn (HOST BUS) 1/3	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 3 of 69	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Penryn (HOST BUS) 2/3	
Size A3	Document Number M850-1-01	Rev 1.0
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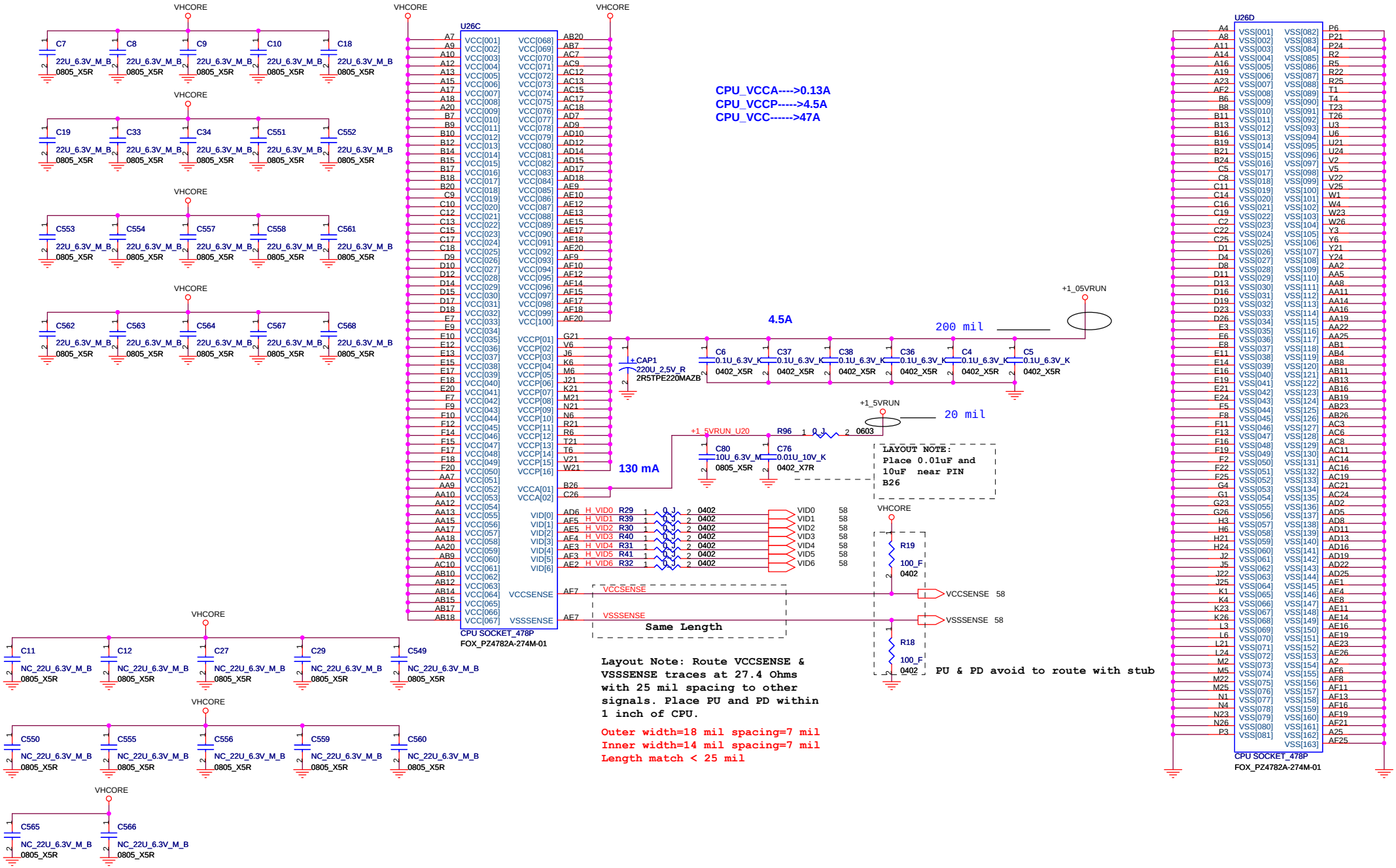

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Penryn (POWER/GROUND) 3/3	
Size A3	Document Number M850-1-01	Rev 1.0
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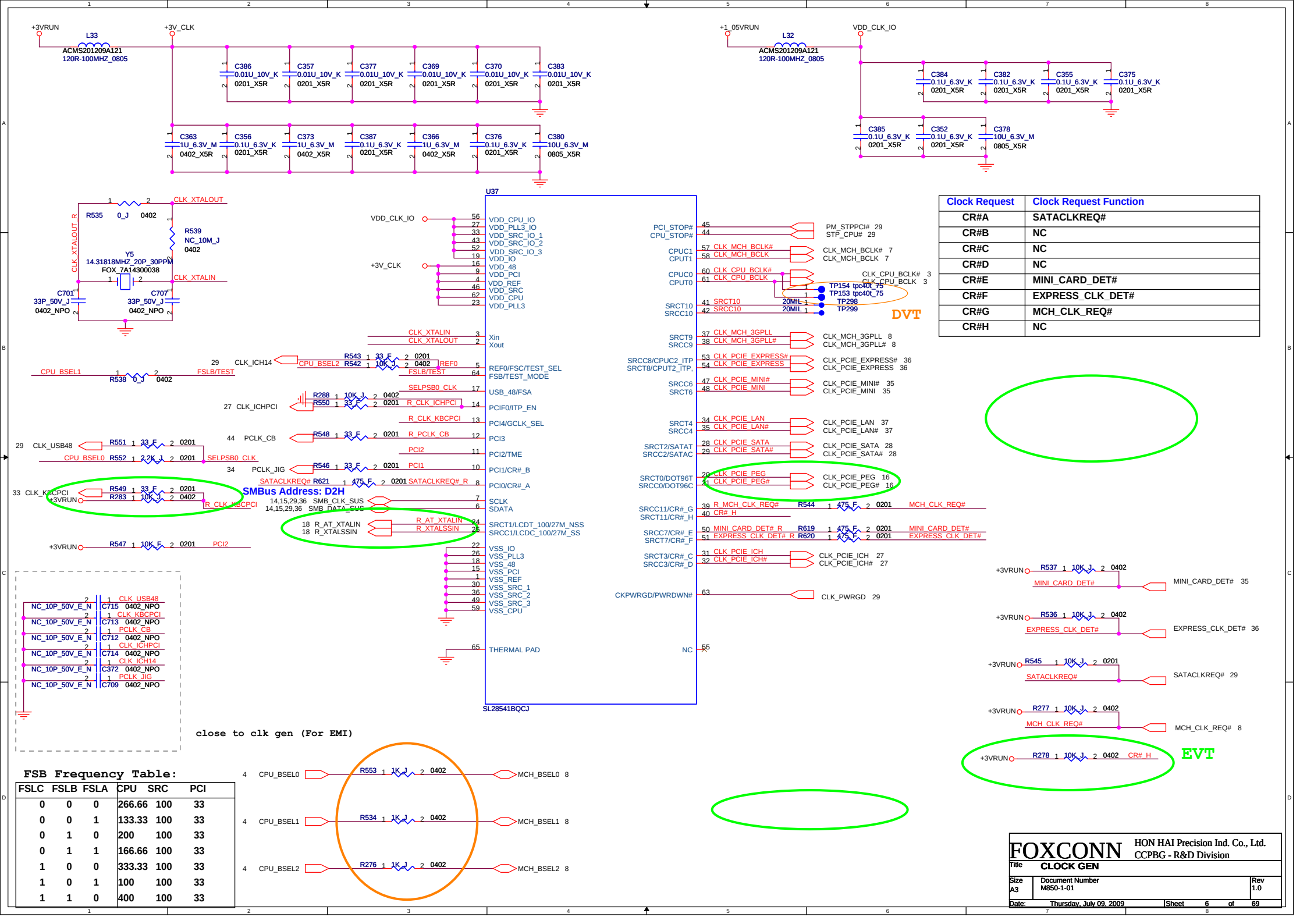

Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	NC
CR#C	NC
CR#D	NC
CR#E	MINI_CARD_DET#
CR#F	EXPRESS_CLK_DET#
CR#G	MCH_CLK_REQ#
CR#H	NC

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

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Title: CLOCK GEN

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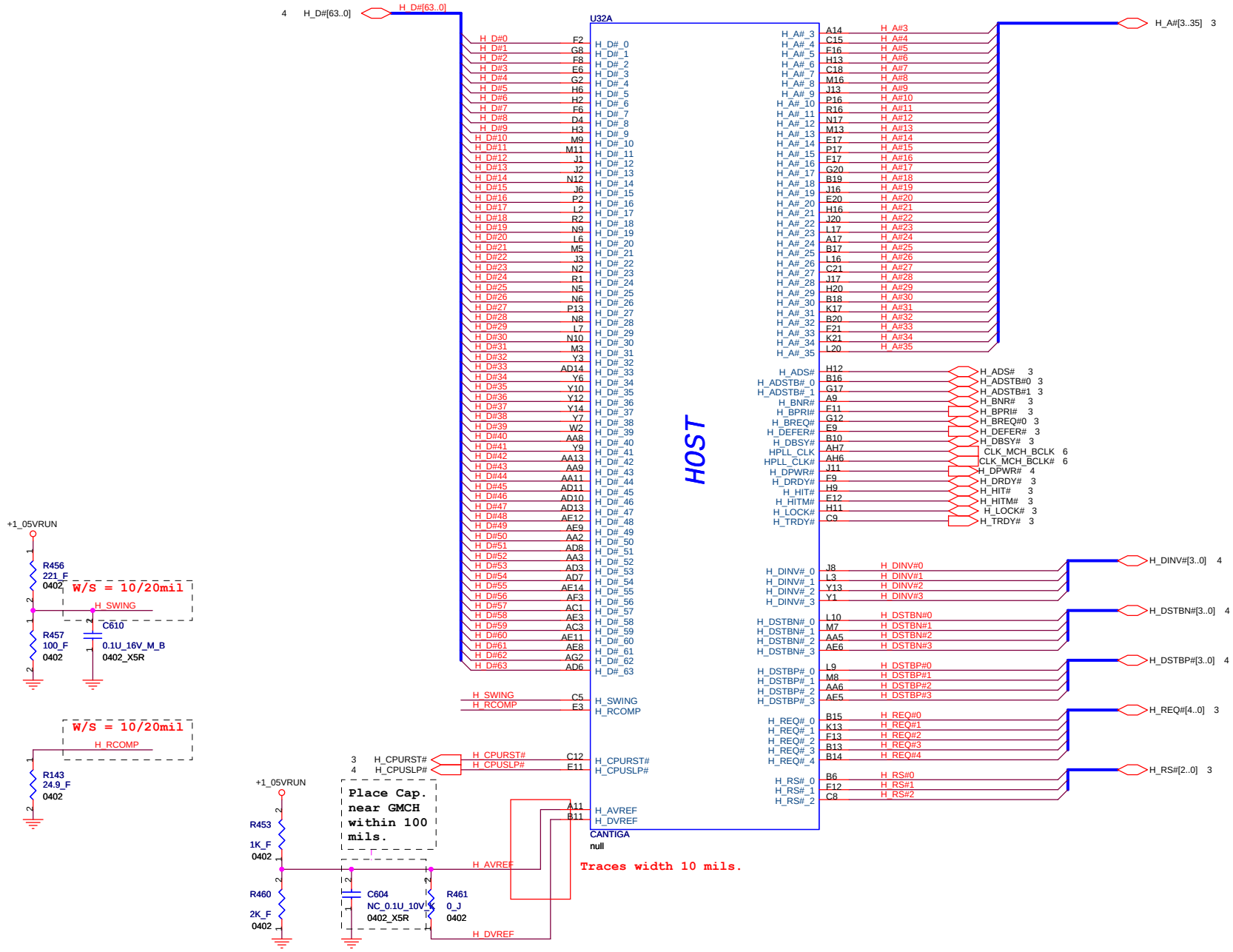

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Cantiga (HOST) 1/7		
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MCH_CFG_0~2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3~4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIE Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIE Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14~15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17~18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

U32B

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
GRAPHICS VID
MISC
NC
HDA

CFG[17:3] internal pull-up
CFG[20:18] internal pull-down

CANTIGA

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Title	Cantiga (DMI) 2/7		
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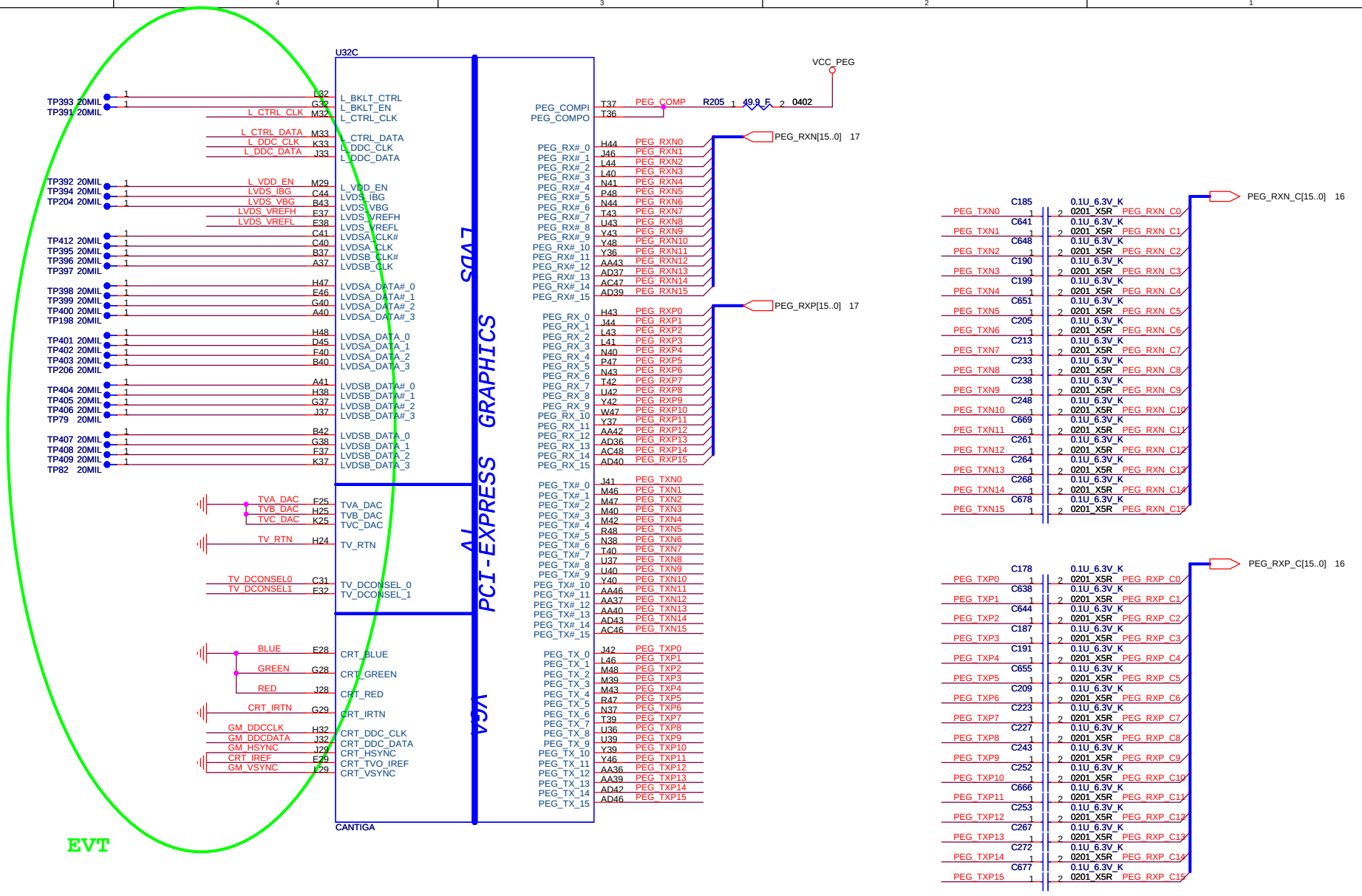

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	Cantiga (GRAPHIC) 3/7
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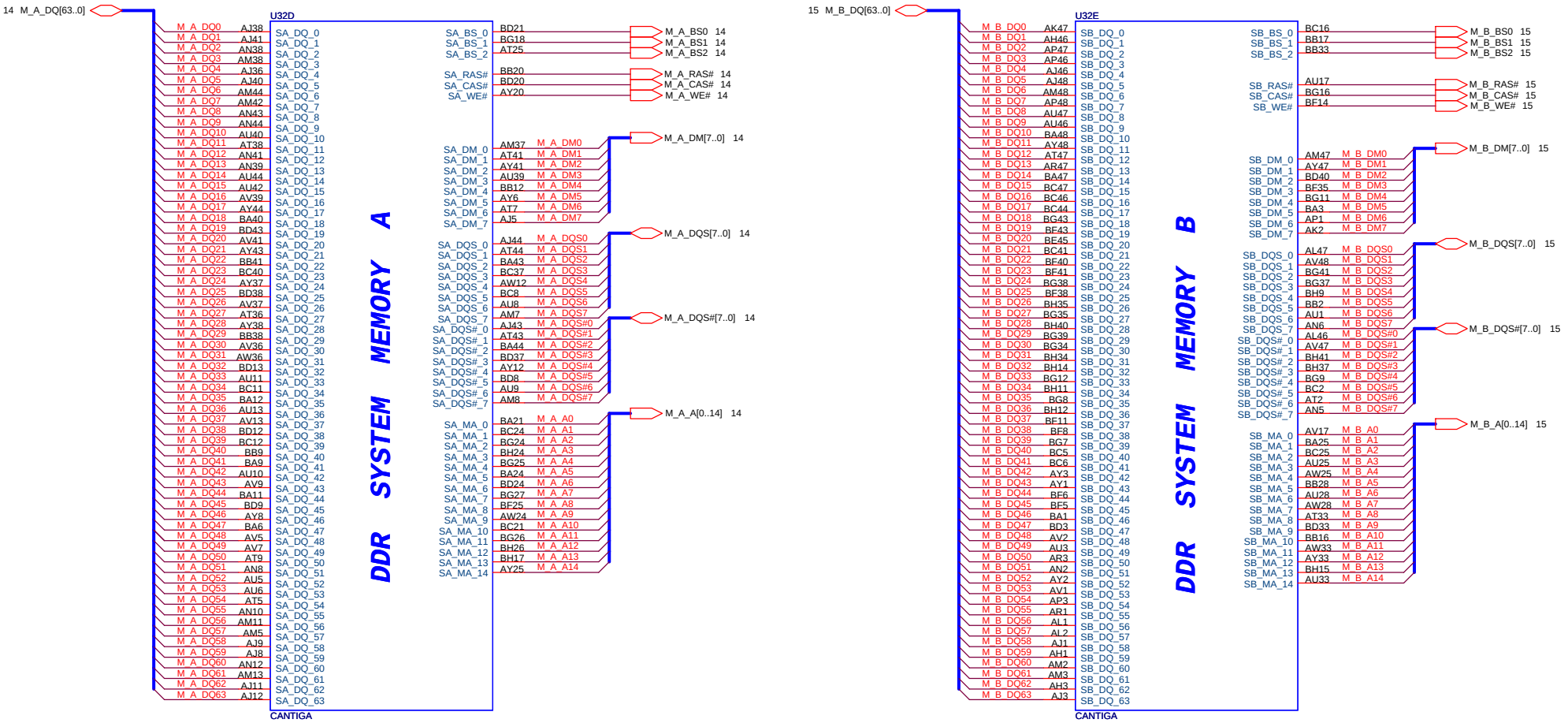

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Title	Cantiga (DDRII) 4/7	
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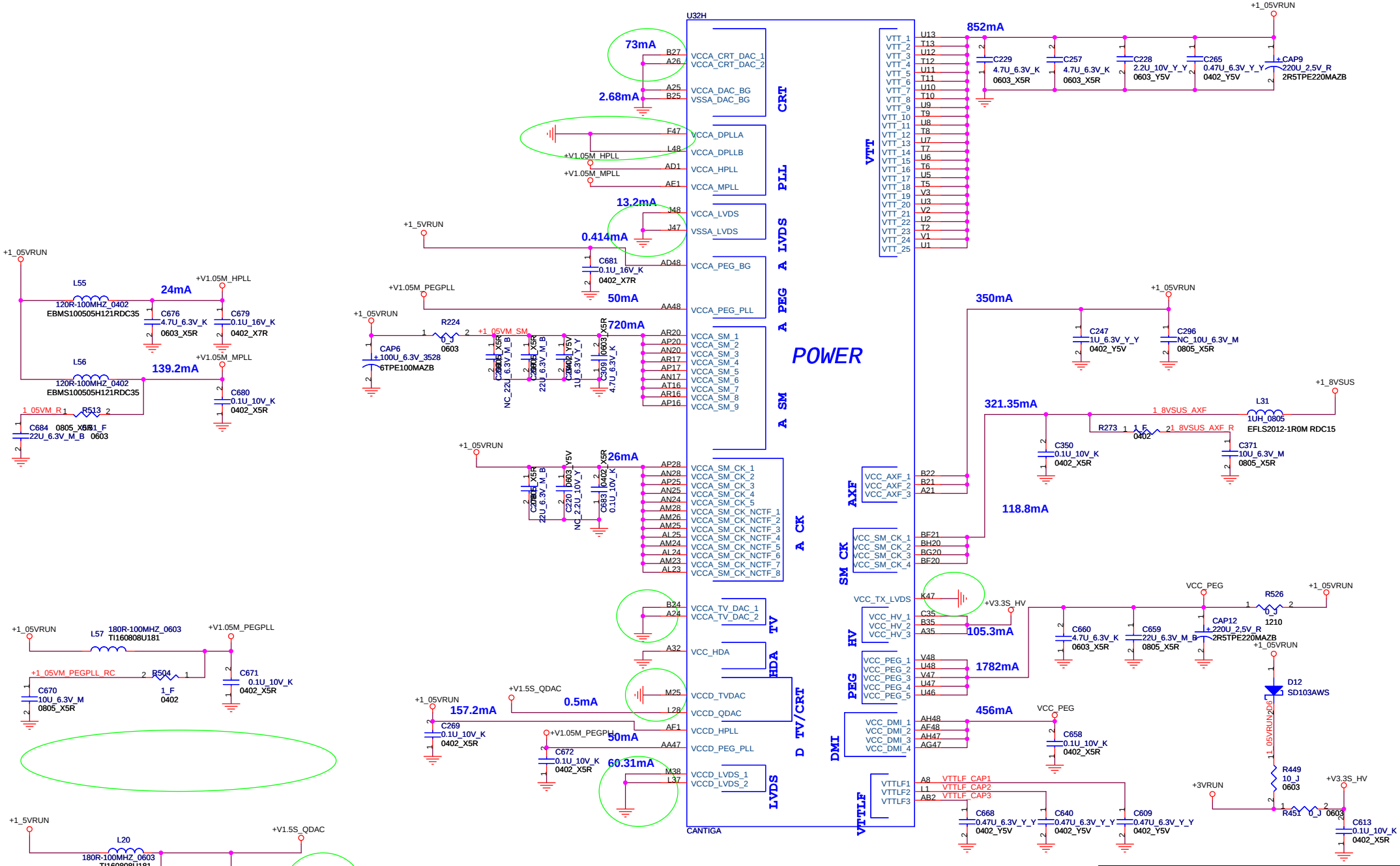

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (POWER,VCC) 5/7	
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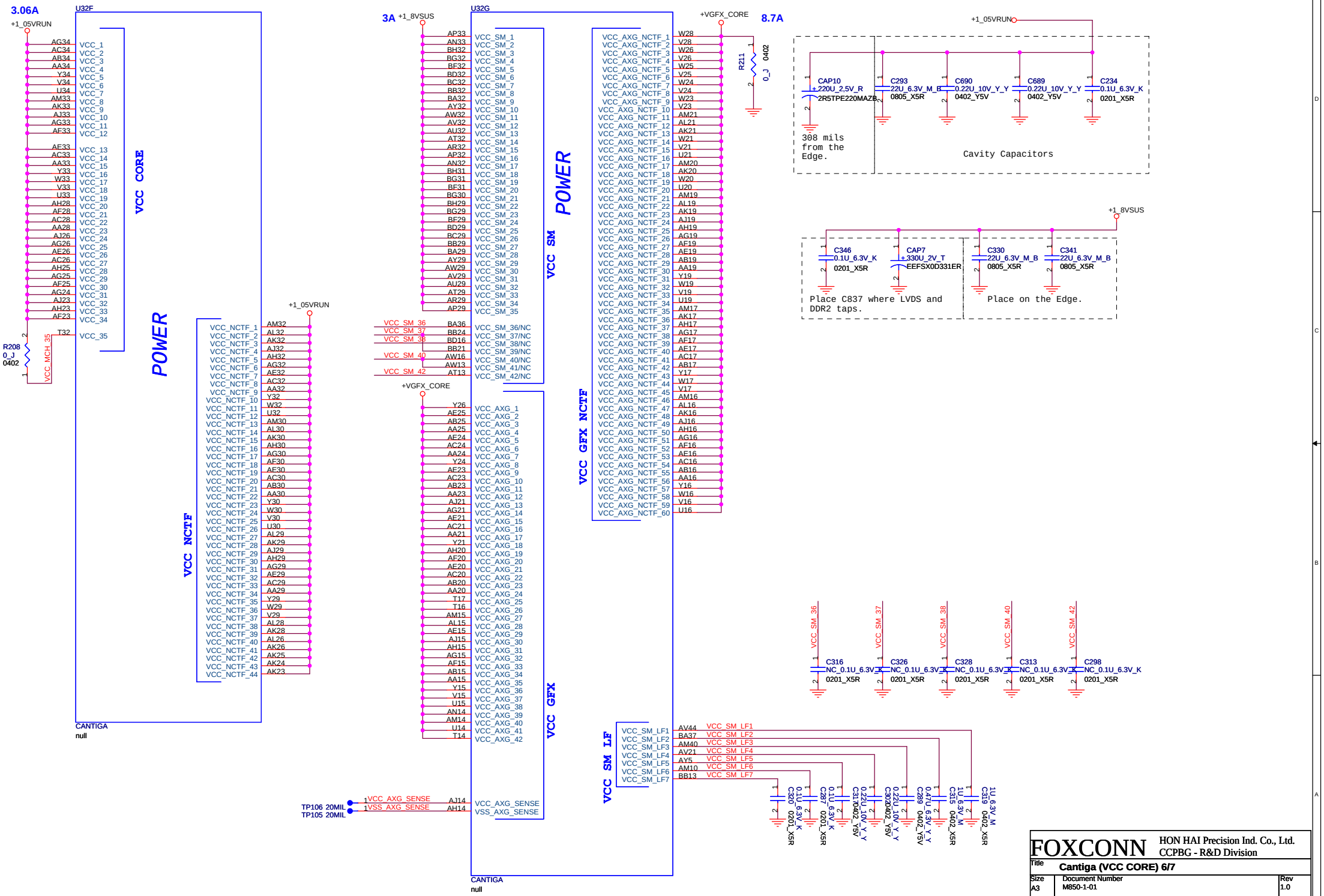

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (VCC CORE) 6/7	
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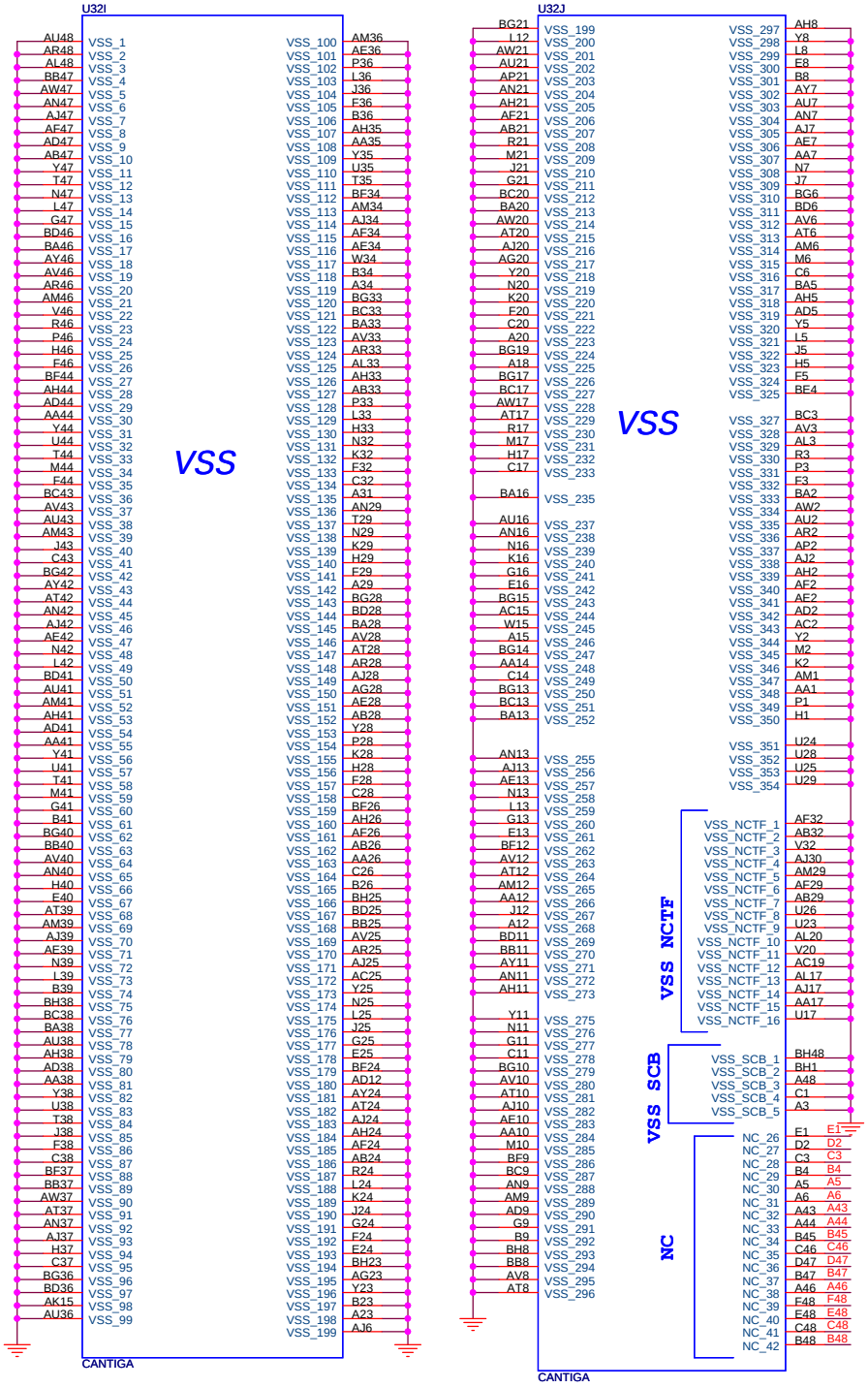

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Cantiga (VSS) 7/7		
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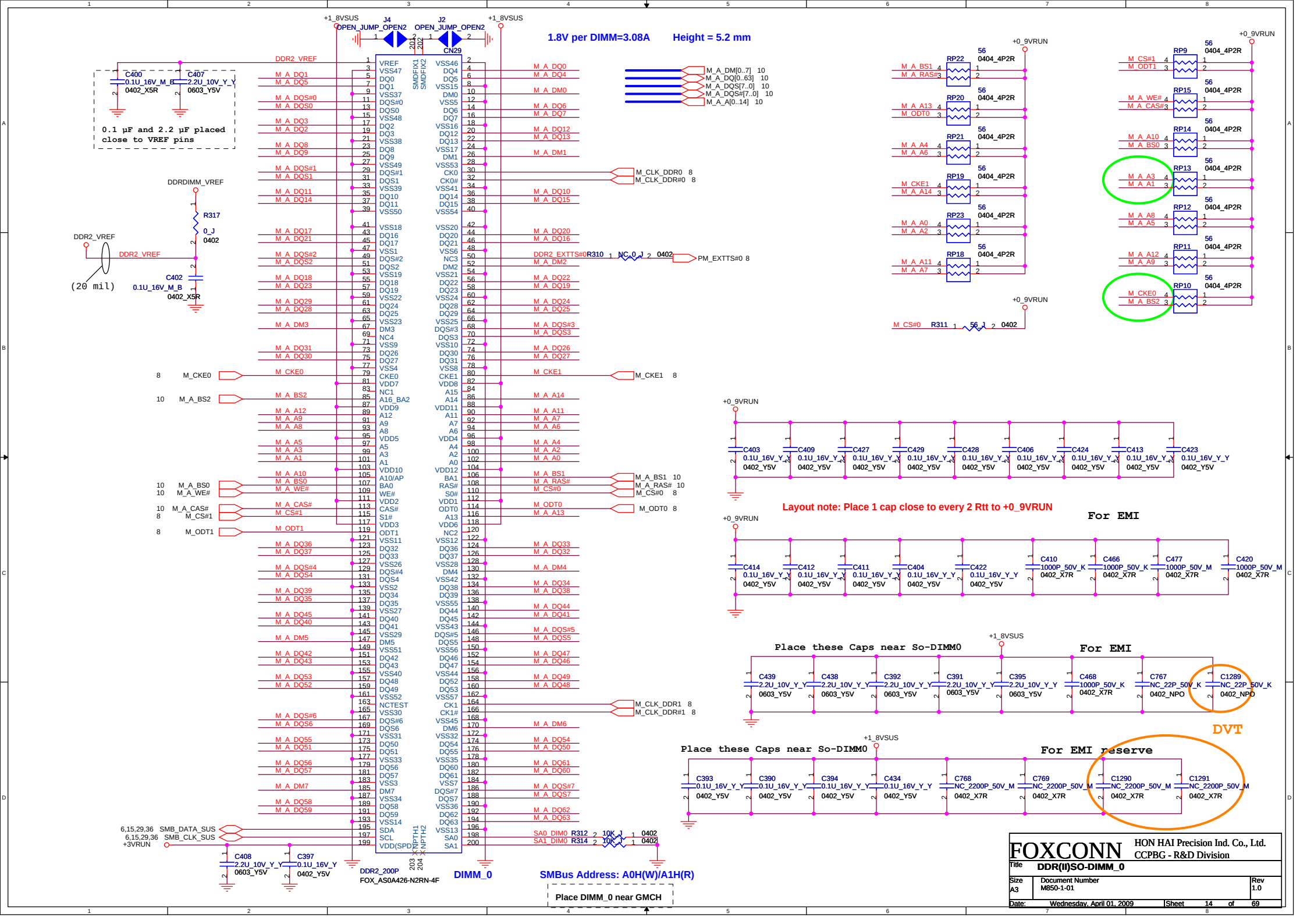
1.8V per DIMM=3.08A
Height = 5.2 mm
+1_8VSUS
OPEN_JUMP_OPEN2
J4
J2
CN29
DDR2_VREF
C400 0.1U_16V_M_B 0402_X5R
C407 2.2U_10V_Y_Y 0603_Y5V
0.1 µF and 2.2 µF placed close to VREF pins
DDRDIMM_VREF
R317 0_J 0402
C402 0.1U_16V_M_B 0402_X5R
(20 mil)
M_A_DM[0..7] 10
M_A_DQ[0..63] 10
M_A_DQS[7..0] 10
M_A_DQS#[7..0] 10
M_A_A[0..14] 10
M_CLK_DDR0 8
M_CLK_DDR#0 8
DDR2_EXTTS#0 R310 NC_0_J 0402
PM_EXTTS#0 8
M_CKE0 8
M_CKE1 8
M_A_BS2 10
M_A_BS0 10
M_A_WE# 10
M_A_CAS# 10
M_CS#1 8
M_ODT1 8
M_A_BS1 10
M_A_RAS# 10
M_CS#0 8
M_ODT0 8
M_CLK_DDR1 8
M_CLK_DDR#1 8
6,15,29,36 SMB_DATA_SUS
6,15,29,36 SMB_CLK_SUS
+3VRUN
C408 2.2U_10V_Y_Y 0603_Y5V
C397 0.1U_16V_Y 0402_Y5V
DDR2_200P
FOX_AS0A426-N2RN-4F
DIMM_0
SA0_DIMM0 R312 10K_J 0402
SA1_DIMM0 R314 10K_J 0402
SMBus Address: A0H(W)/A1H(R)
Place DIMM_0 near GMCH
+0_9VRUN
RP22 RP20 RP21 RP19 RP23 RP18
M_A_BS1 M_A_RAS# M_A_A13 M_ODT0 M_A_A4 M_A_A6 M_CKE1 M_A_A14 M_A_A0 M_A_A2 M_A_A11 M_A_A7
56 0404_4P2R
M_CS#0 R311 56_J 0402
RP9 RP15 RP14 RP13 RP12 RP11 RP10
M_CS#1 M_ODT1 M_A_WE# M_A_CAS# M_A_A10 M_A_BS0 M_A_A3 M_A_A1 M_A_A8 M_A_A5 M_A_A12 M_A_A9 M_CKE0 M_A_BS2
C403 C409 C427 C429 C428 C406 C424 C413 C423
0.1U_16V_Y_Y 0402_Y5V
Layout note: Place 1 cap close to every 2 Rtt to +0_9VRUN
For EMI
C414 C412 C411 C404 C422
C410 1000P_50V_K 0402_X7R
C466 1000P_50V_K 0402_X7R
C477 1000P_50V_M 0402_X7R
C420 1000P_50V_M 0402_X7R
Place these Caps near So-DIMM0
C439 C438 C392 C391 C395 2.2U_10V_Y_Y 0603_Y5V
C468 1000P_50V_K 0402_X7R
C767 NC_22P_50V_K 0402_NPO
C1289 NC_22P_50V_K 0402_NPO
DVT
For EMI reserve
C393 C390 C394 C434 0.1U_16V_Y_Y 0402_Y5V
C768 C769 C1290 C1291 NC_2200P_50V_M 0402_X7R
FOXCONN
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Title DDR(II)SO-DIMM_0
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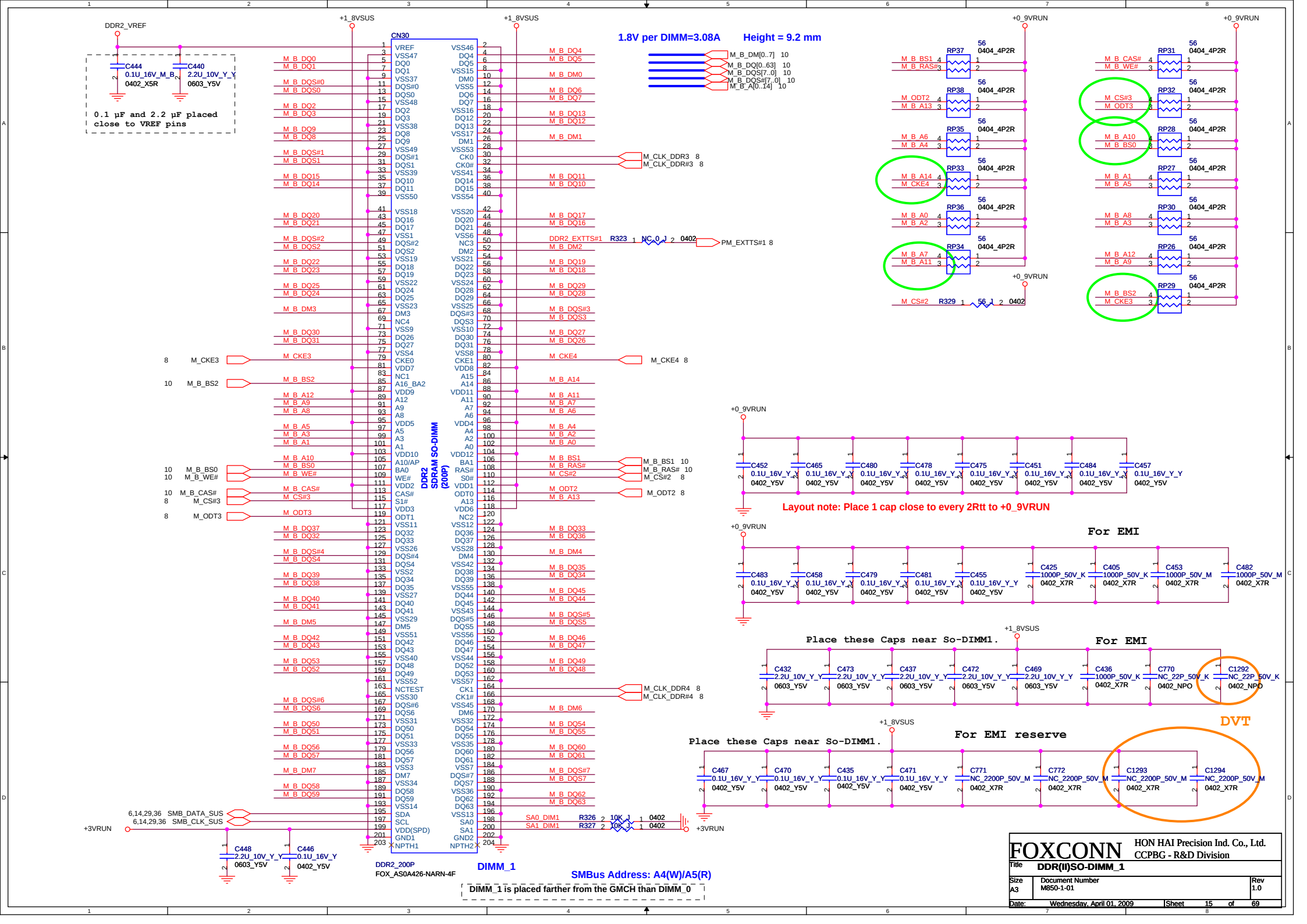
DDR2_VREF
+1_8VSUS
CN30
C444 0.1U_16V_M_B 0402_X5R
C440 2.2U_10V_Y_Y 0603_Y5V
0.1 µF and 2.2 µF placed close to VREF pins
1.8V per DIMM=3.08A
Height = 9.2 mm
M_B_DM[0..7] 10
M_B_DQS[0..63] 10
M_B_DQS#[7..0] 10
M_B_A[0..14] 10
DDR2 SDRAM SO-DIMM (200P)
M_CLK_DDR3 8
M_CLK_DDR#3 8
M_CLK_DDR4 8
M_CLK_DDR#4 8
DDR2_EXTTS#1 R323 NC_0_J 0402
PM_EXTTS#1 8
M_CKE3 8
M_CKE4 8
M_B_BS2 10
M_B_BS1 10
M_B_RAS# 10
M_B_CS#2 8
M_ODT2 8
M_ODT3 8
M_B_BS0 10
M_B_WE# 10
M_B_CAS# 10
M_CS#3 8
SMB_DATA_SUS 6,14,29,36
SMB_CLK_SUS 6,14,29,36
+3VRUN
SA0_DIM1 R326 10K_J 0402
SA1_DIM1 R327 10K_J 0402
DDR2_200P
FOX_AS0A426-NARN-4F
DIMM_1
SMBus Address: A4(W)/A5(R)
DIMM_1 is placed farther from the GMCH than DIMM_0
+0_9VRUN
RP37 RP38 RP35 RP33 RP36 RP34 RP31 RP32 RP28 RP27 RP30 RP26 RP29
56 0404_4P2R
M_CS#2 R329 56_J 0402
Layout note: Place 1 cap close to every 2Rtt to +0_9VRUN
For EMI
Place these Caps near So-DIMM1.
For EMI reserve
DVT
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title DDR(II)SO-DIMM_1
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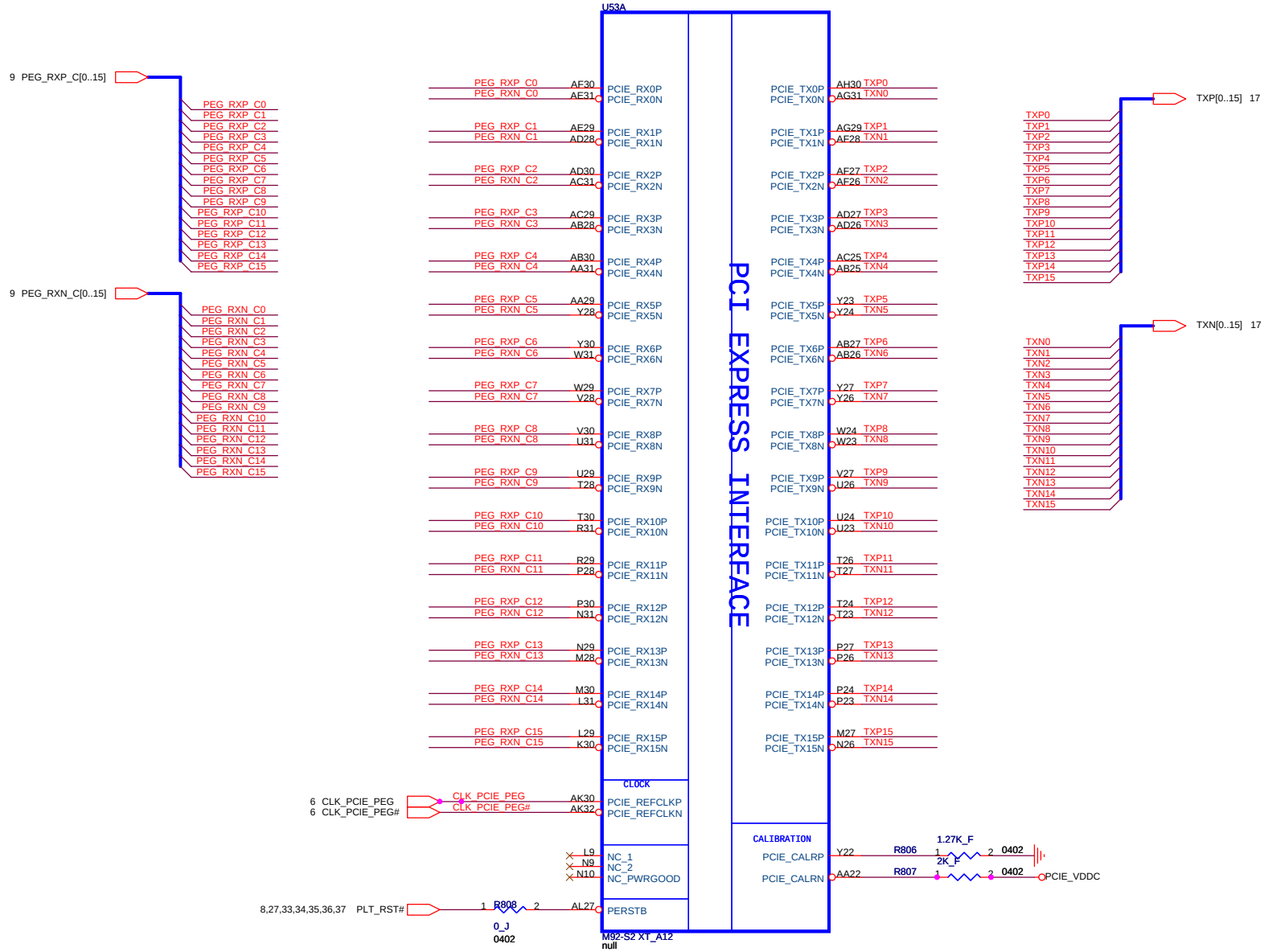

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA (PCI-E) 1/5	
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	Mount	NC
Hynix-256MB H5RS1H23MFR-11C	R812,R809	R910,R911, R811,R810
Hynix-512MB H5RS1H23MFR-11C	R910 R812,R809	R911 R811,R810

	Mount	NC
Samsung-256MB K4J10324QD-HC12	R812,R810	R910,R911, R811,R809
Qimonda-256MB HYB18H1G321A2F-10	R811,R810	R910,R911, R812,R809

	Mount	NC
Samsung-512MB K4J10324QD-HC12	R910 R812,R810	R911 R811,R809
Qimonda-512MB HYB18H1G321A2F-10	R910 R811,R810	R911 R812,R809

DVT

9 PEG_RXP[0..15]

TXP[0..15] 16

9 PEG_RXN[0..15]

TXN[0..15] 16

0.1U_6.3V_K

PEG_RXP0	C1078	0201_X5R	TXP0	PEG_RXN0 C1079 0201_X5R TXN0
PEG_RXP1	C1080	0201_X5R	TXP1	PEG_RXN1 C1081 0201_X5R TXN1
PEG_RXP2	C1082	0201_X5R	TXP2	PEG_RXN2 C1083 0201_X5R TXN2
PEG_RXP3	C1084	0201_X5R	TXP3	PEG_RXN3 C1085 0201_X5R TXN3
PEG_RXP4	C1086	0201_X5R	TXP4	PEG_RXN4 C1087 0201_X5R TXN4
PEG_RXP5	C1088	0201_X5R	TXP5	PEG_RXN5 C1089 0201_X5R TXN5
PEG_RXP6	C1090	0201_X5R	TXP6	PEG_RXN6 C1091 0201_X5R TXN6
PEG_RXP7	C1092	0201_X5R	TXP7	PEG_RXN7 C1093 0201_X5R TXN7
PEG_RXP8	C1094	0201_X5R	TXP8	PEG_RXN8 C1095 0201_X5R TXN8
PEG_RXP9	C1096	0201_X5R	TXP9	PEG_RXN9 C1097 0201_X5R TXN9
PEG_RXP10	C1098	0201_X5R	TXP10	PEG_RXN10 C1099 0201_X5R TXN10
PEG_RXP11	C1100	0201_X5R	TXP11	PEG_RXN11 C1101 0201_X5R TXN11
PEG_RXP12	C1102	0201_X5R	TXP12	PEG_RXN12 C1103 0201_X5R TXN12
PEG_RXP13	C1104	0201_X5R	TXP13	PEG_RXN13 C1105 0201_X5R TXN13
PEG_RXP14	C1106	0201_X5R	TXP14	PEG_RXN14 C1107 0201_X5R TXN14
PEG_RXP15	C1108	0201_X5R	TXP15	PEG_RXN15 C1109 0201_X5R TXN15

DVT

Strap for GDDR3-136ball
ATI_DVPDATA[1:0:21:20]

0001 32Mx32 Qimonda-256MB
0010 32Mx32 Hynix-256MB
0011 32Mx32 Samsung-256MB
0101 32Mx32 Qimonda-512MB
0110 32Mx32 Hynix-512MB
0111 32Mx32 Samsung-512MB

+1_8VRUN

MEM_ID0	R809	NC_10K_J 0402	AT_MEM_ID0	R810 10K_J 0201
MEM_ID1	R811	NC_10K_J 0201	AT_MEM_ID1	R812 10K_J 0201
MEM_ID2	R813	NC_10K_J 0201	AT_MEM_ID2	R814 NC_10K_J 0201
MEM_ID3	R815	NC_10K_J 0201	AT_MEM_ID3	R816 NC_10K_J 0201
			AT_MEM_ID2_1	R910 10K_J 0201
			AT_MEM_ID3_1	R911 NC_10K_J 0201

If no ROM attached, GPIO[13:12:11] ;
CONFIG{2:0}
controls the memory aperture size.

64MB	010
128MB	000
256MB	001
512MB	001

+3V_DELAY

MEM_SIZE2	R819	10K_J 0201	AT_GPIO13	R820 NC_10K_J 0201
MEM_SIZE1	R821	10K_J 0201	AT_GPIO12	R822 NC_10K_J 0201
MEM_SIZE0	R823	NC_10K_J 0201	AT_GPIO11	R824 10K_J 0201

HSYNC , VSYNC
AUD[1] , AUD[0]

0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

18,24	AT_DACA_HSYNC	R825 10K_J 0402
18,24	AT_DACA_VSYNC	R826 10K_J 0402
18	AT_GPIO2	R882 NC_10K_J 0402
18	AT_GPIO1	R883 NC_10K_J 0402
18	AT_GPIO0	R884 NC_10K_J 0402

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED

18 AT_MEM_ID0	AT_MEM_ID0
18 AT_MEM_ID1	AT_MEM_ID1
18 AT_MEM_ID2	AT_MEM_ID2
18 AT_MEM_ID3	AT_MEM_ID3
18 AT_MEM_ID2_1	AT_MEM_ID2_1
18 AT_MEM_ID3_1	AT_MEM_ID3_1

For AMD verification

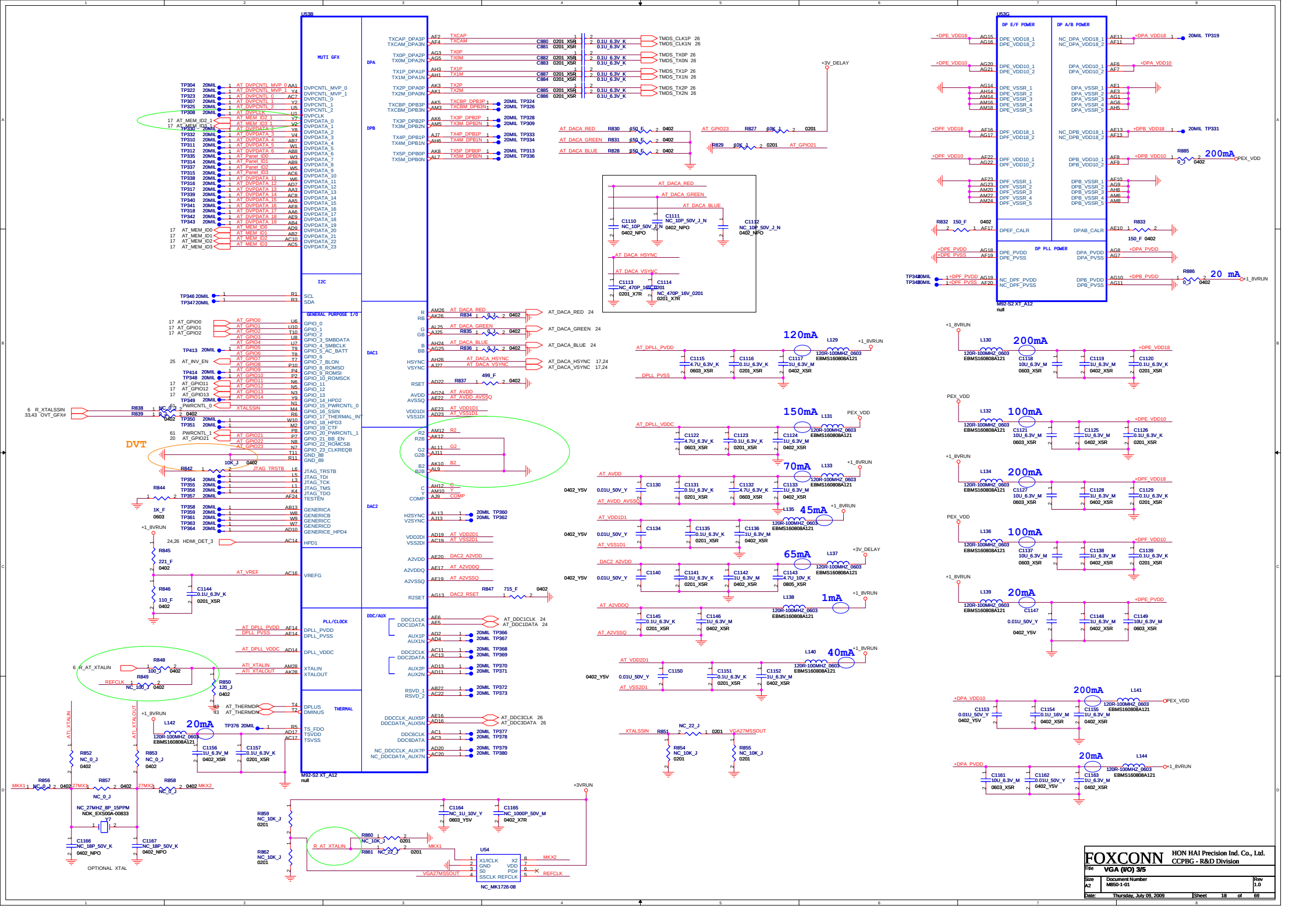
18 AT_GPIO11	AT_GPIO11
18 AT_GPIO12	AT_GPIO12
18 AT_GPIO13	AT_GPIO13

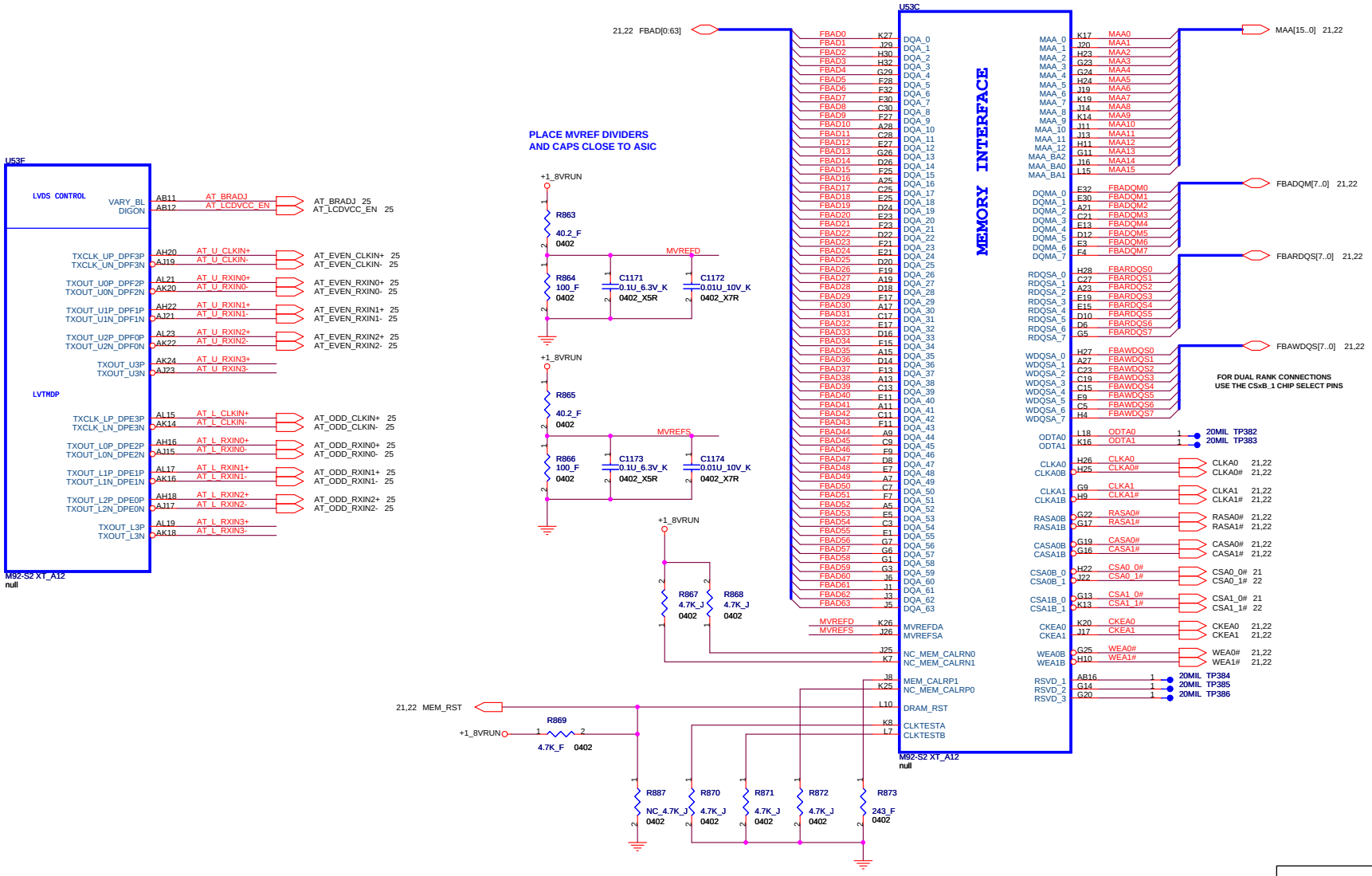
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: VGA (Strap) 2/5

Size: A3 | Document Number: M850-1-01 | Rev: 1.0

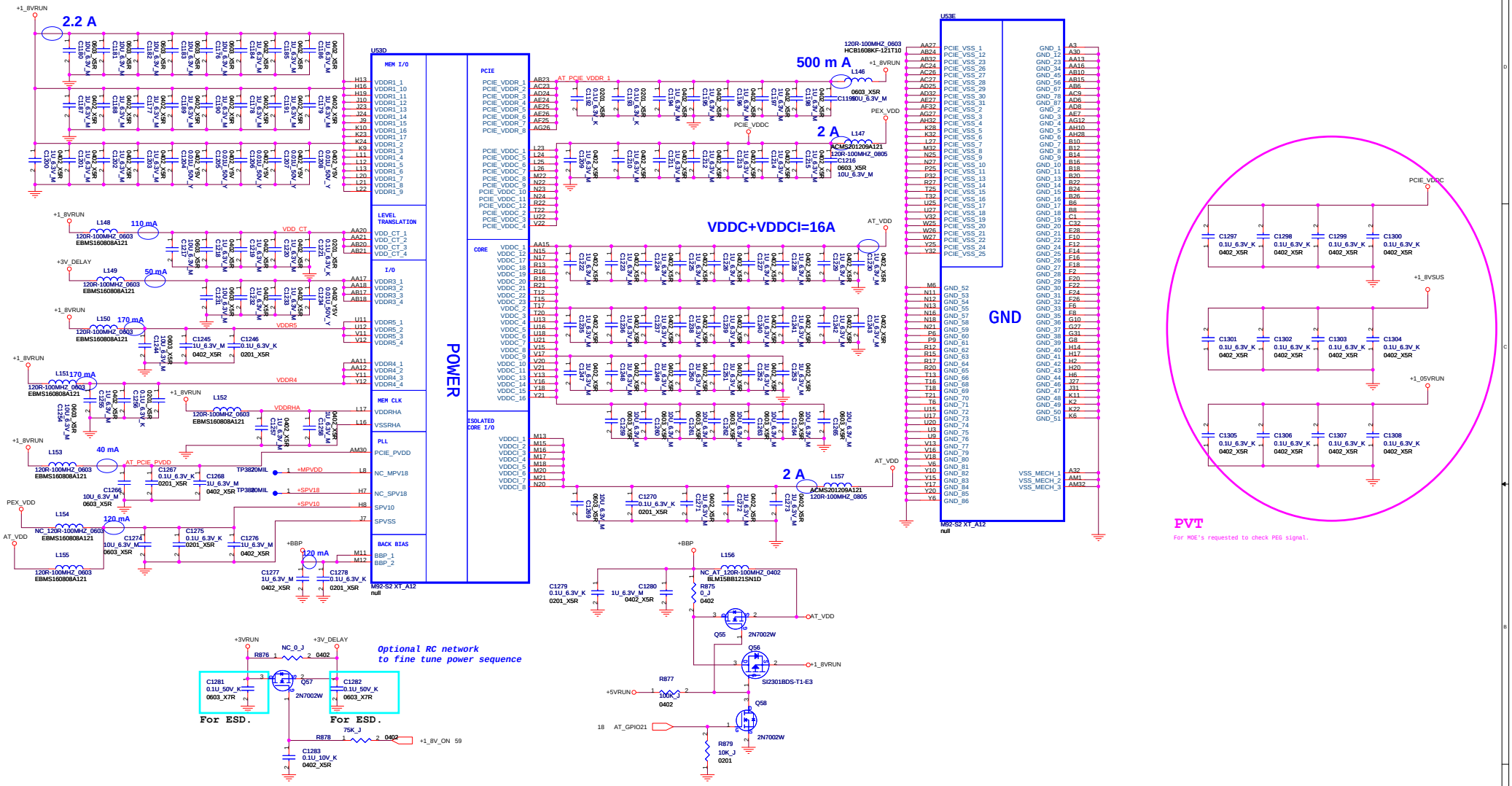
Date: Thursday, July 09, 2009 | Sheet 17 of 69

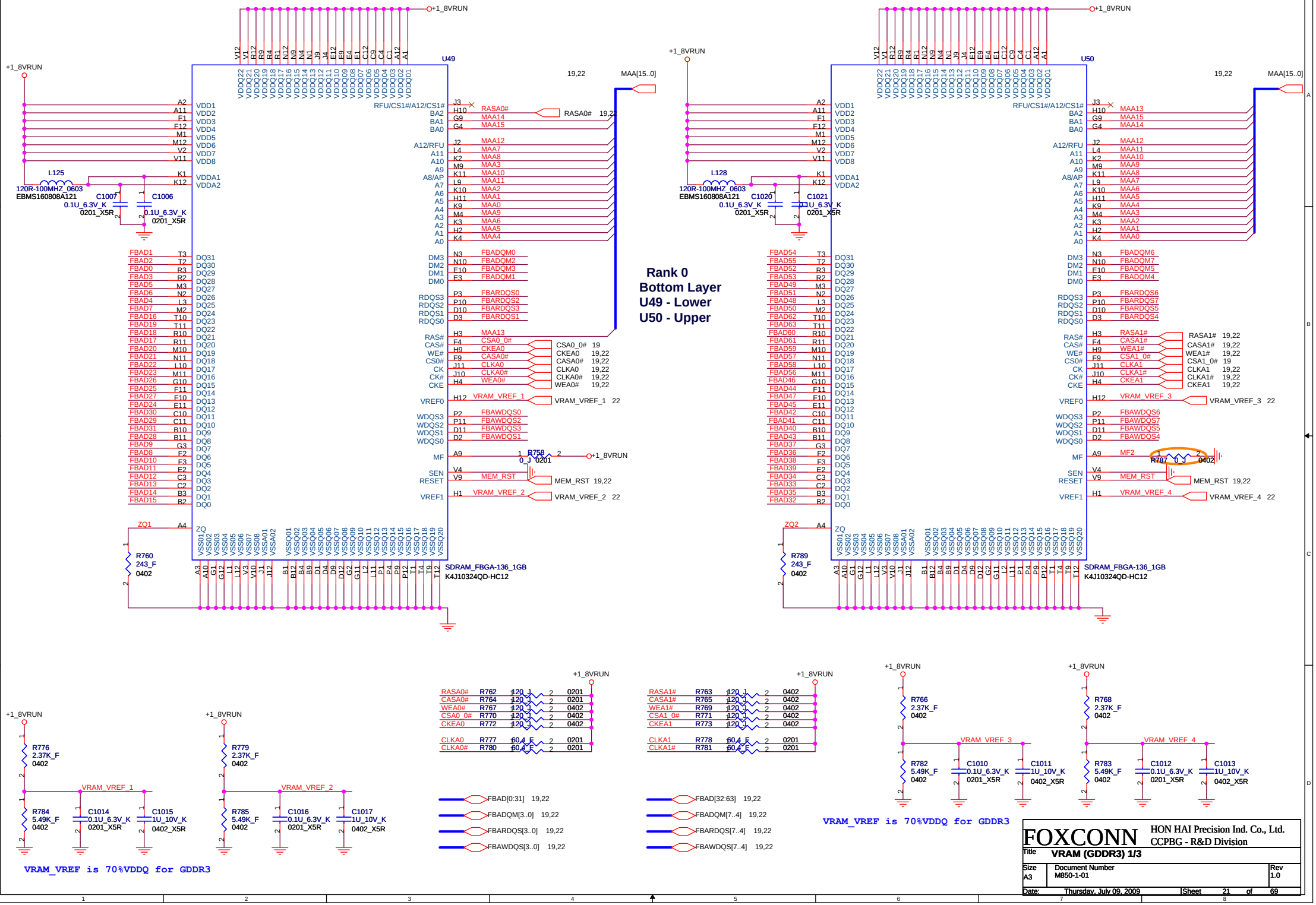

U53B
MUTI GFX
DPA
DPB
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
M92-S2 XT_A12
null
U53G
DP E/F POWER
DP A/B POWER
DP PLL POWER
M92-S2 XT_A12
null
DVT
OPTIONAL XTAL
NC_MK1726-08
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
VGA (I/O) 3/5
Size
A2
Document Number
M850-1-01
Rev
1.0
Date:
Thursday, July 09, 2009
Sheet
18
of
69



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

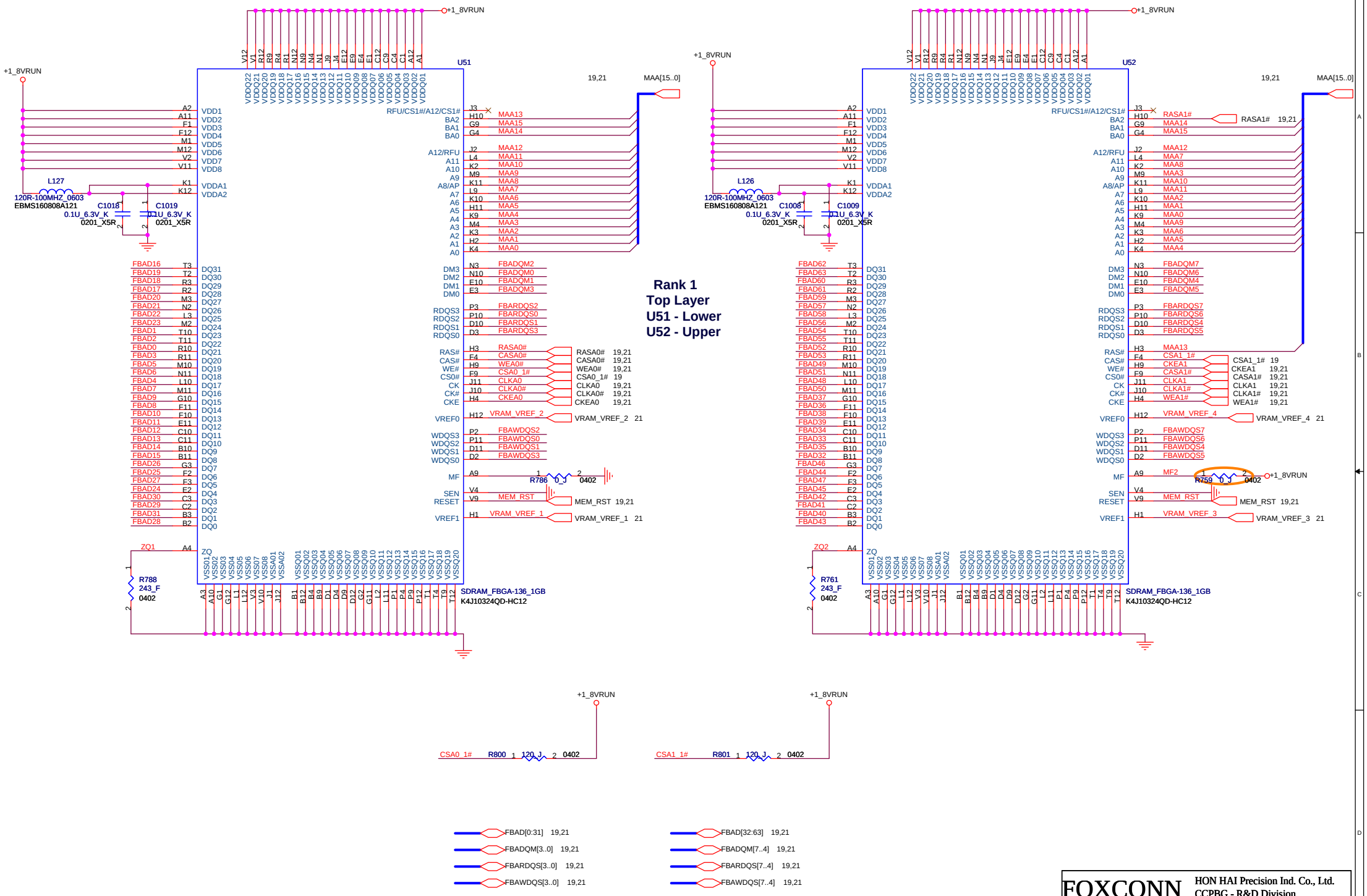
Title	VGA (Memory BUS) 4/5	
Size: Custom	Document Number: M850-1-01	Rev: 1.0
Date: Wednesday, April 01, 2009	Sheet 19 of 69	


2.2 A
500 m A
2 A
VDDC+VDDCI=16A
2 A
POWER
GND
U53D
U53E
PCIE
CORE
ISOLATED CORE I/O
MEM I/O
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
Optional RC network to fine tune power sequence
For ESD.
For ESD.
PVT
For MOE's requested to check PEG signal.
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
VGA (Power) 5/5
Document Number M850-1-01
Rev 1.0
Wednesday, April 01, 2009
Sheet 20 of 69



FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VRAM (GDDR3) 1/3	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 21 of 69	



FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: VRAM (GDDR3) 2/3		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 22 of 69	

+1_8VRUN

Place around the VRAM U49 **1.2A**

C1022 10U_6.3V_M 0805_X5R	C1023 0.1U_6.3V_K 0201_X5R	C1024 0.1U_6.3V_K 0201_X5R	C1025 0.1U_6.3V_K 0201_X5R	C1026 0.1U_6.3V_K 0201_X5R	C1027 0.1U_6.3V_K 0201_X5R	C1028 0.1U_6.3V_K 0201_X5R	C1029 1000P_16V_K 0201_X7R	C1030 1000P_16V_K 0201_X7R	C1031 0.1U_6.3V_K 0201_X5R	C1032 0.1U_6.3V_K 0201_X5R	C1033 0.1U_6.3V_K 0201_X5R	C1034 0.1U_6.3V_K 0201_X5R	C1035 1000P_16V_K 0201_X7R

+1_8VRUN

Place around the VRAM U50 **1.2A**

C1036 10U_6.3V_M 0805_X5R	C1037 0.1U_6.3V_K 0201_X5R	C1038 0.1U_6.3V_K 0201_X5R	C1039 0.1U_6.3V_K 0201_X5R	C1040 0.1U_6.3V_K 0201_X5R	C1041 0.1U_6.3V_K 0201_X5R	C1042 0.1U_6.3V_K 0201_X5R	C1043 1000P_16V_K 0201_X7R	C1044 1000P_16V_K 0201_X7R	C1045 0.1U_6.3V_K 0201_X5R	C1046 0.1U_6.3V_K 0201_X5R	C1047 0.1U_6.3V_K 0201_X5R	C1048 0.1U_6.3V_K 0201_X5R	C1049 1000P_16V_K 0201_X7R

+1_8VRUN

Place around the VRAM U51 **1.2A**

C1050 10U_6.3V_M 0805_X5R	C1051 0.1U_6.3V_K 0201_X5R	C1052 0.1U_6.3V_K 0201_X5R	C1053 0.1U_6.3V_K 0201_X5R	C1054 0.1U_6.3V_K 0201_X5R	C1055 0.1U_6.3V_K 0201_X5R	C1056 0.1U_6.3V_K 0201_X5R	C1057 1000P_16V_K 0201_X7R	C1058 1000P_16V_K 0201_X7R	C1059 0.1U_6.3V_K 0201_X5R	C1060 0.1U_6.3V_K 0201_X5R	C1061 0.1U_6.3V_K 0201_X5R	C1062 0.1U_6.3V_K 0201_X5R	C1063 1000P_16V_K 0201_X7R

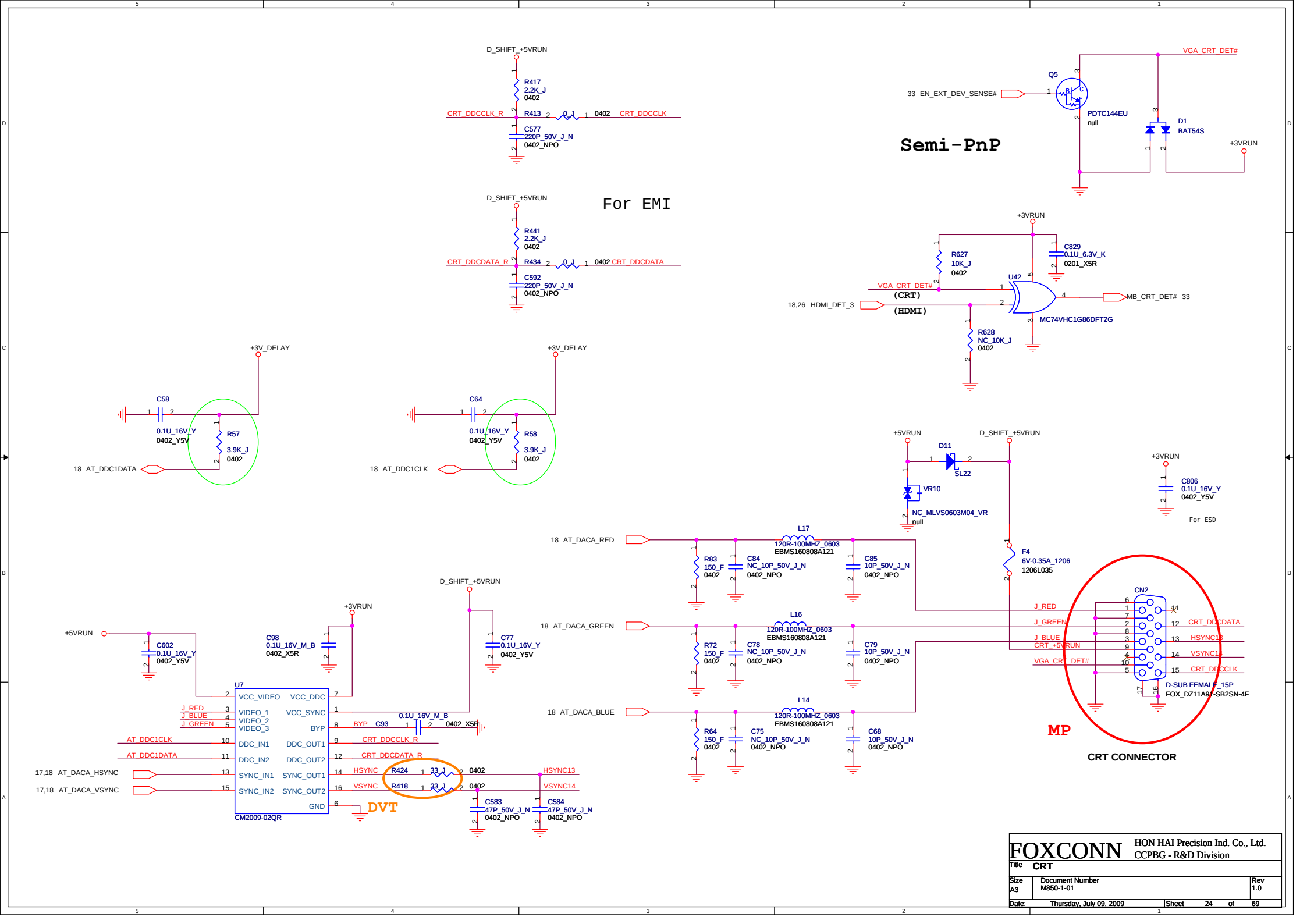
+1_8VRUN

Place around the VRAM U52 **1.2A**

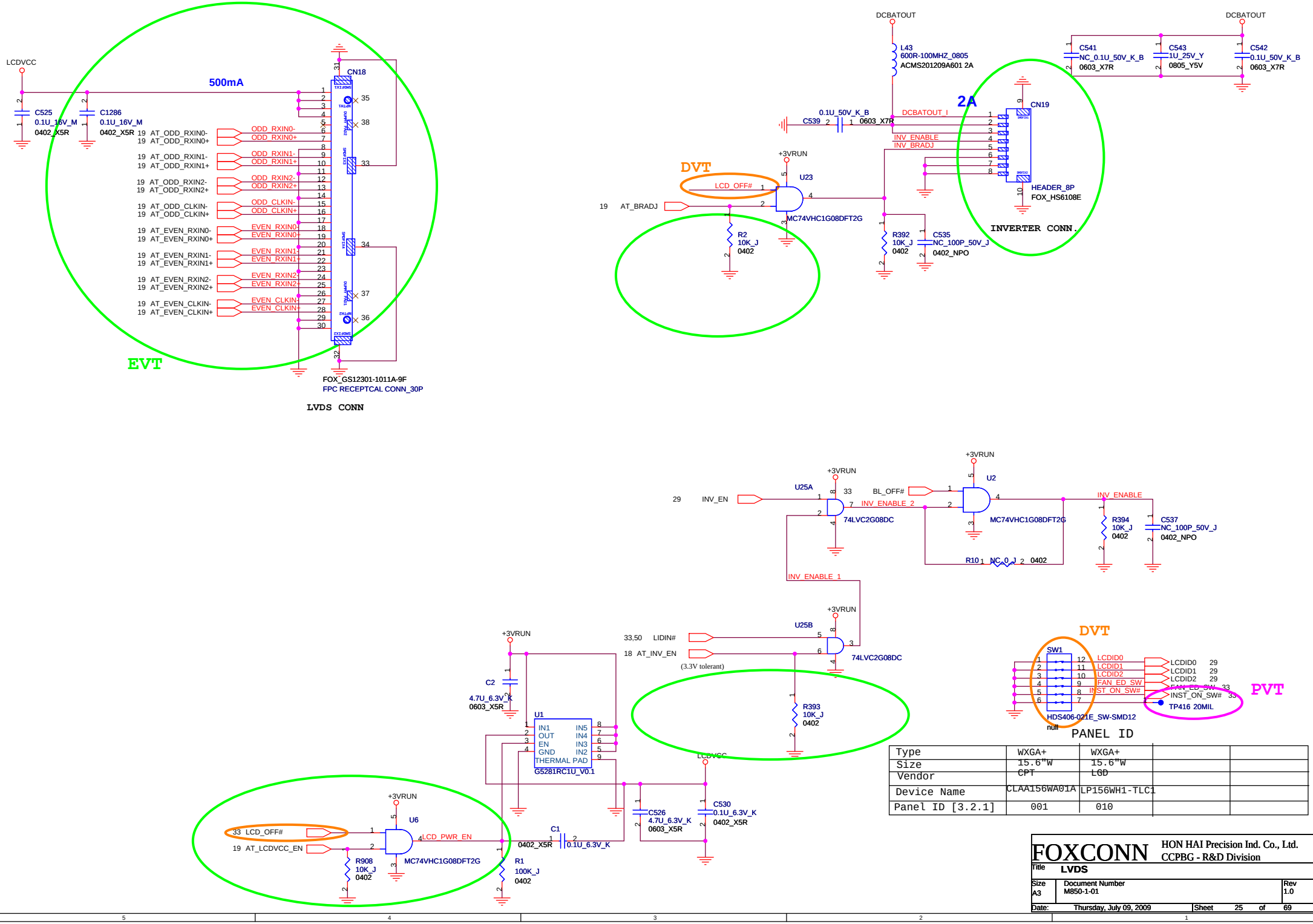
C1064 10U_6.3V_M 0805_X5R	C1065 0.1U_6.3V_K 0201_X5R	C1066 0.1U_6.3V_K 0201_X5R	C1067 0.1U_6.3V_K 0201_X5R	C1068 0.1U_6.3V_K 0201_X5R	C1069 0.1U_6.3V_K 0201_X5R	C1070 0.1U_6.3V_K 0201_X5R	C1071 1000P_16V_K 0201_X7R	C1072 1000P_16V_K 0201_X7R	C1073 0.1U_6.3V_K 0201_X5R	C1074 0.1U_6.3V_K 0201_X5R	C1075 0.1U_6.3V_K 0201_X5R	C1076 0.1U_6.3V_K 0201_X5R	C1077 1000P_16V_K 0201_X7R

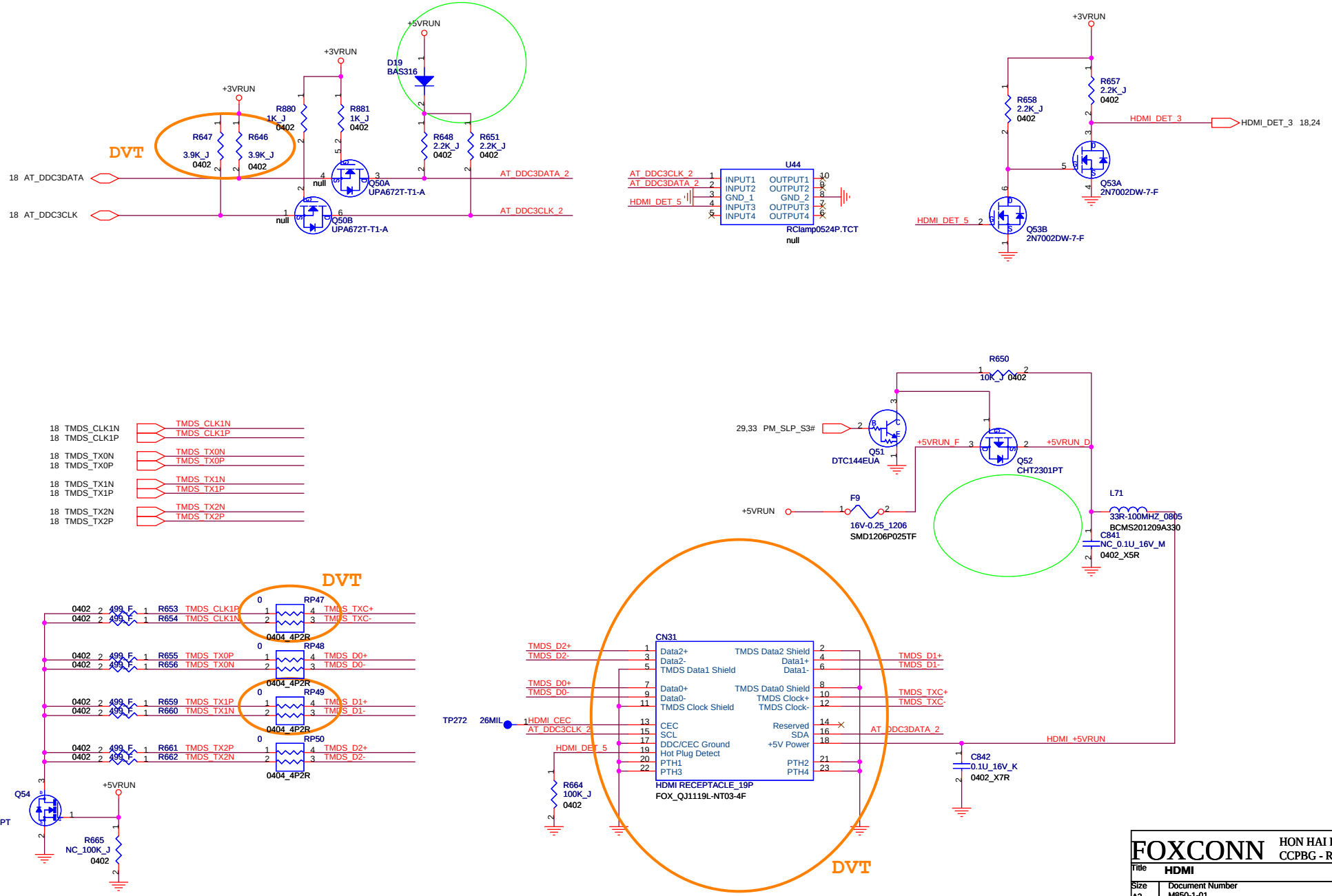
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: VRAM (BYPASS) 3/3		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Thursday, February 26, 2009	Sheet 23 of 69	

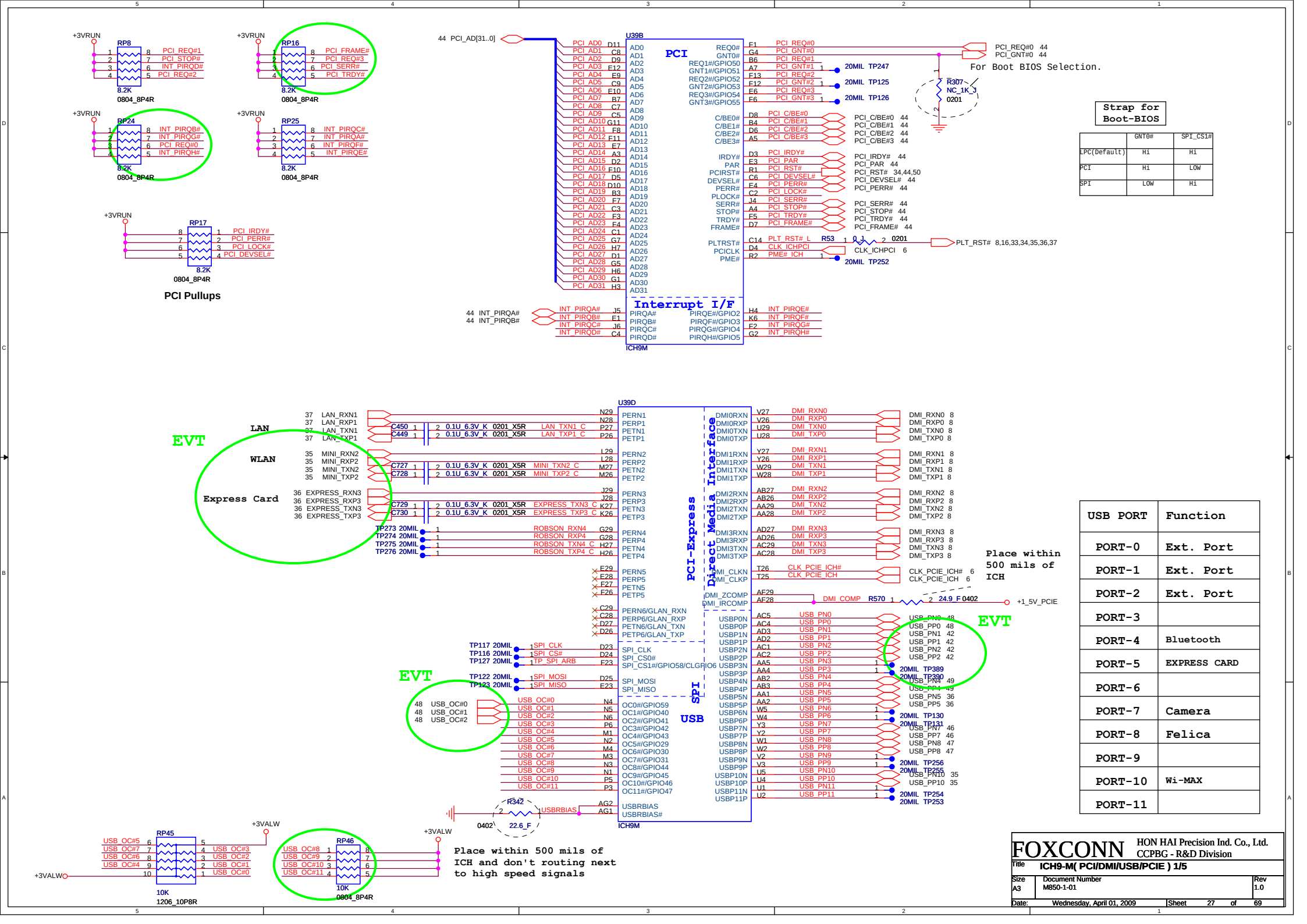


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 24 of 69	


LCDVCC
C525
0.1U_16V_M
0402_X5R
C1286
0.1U_16V_M
0402_X5R
500mA
CN18
FOX_GS12301-1011A-9F
FPC RECEPTCAL CONN_30P
EVT
LVDS CONN
ODD_RXIN0-
ODD_RXIN0+
ODD_RXIN1-
ODD_RXIN1+
ODD_RXIN2-
ODD_RXIN2+
ODD_CLKIN-
ODD_CLKIN+
EVEN_RXIN0-
EVEN_RXIN0+
EVEN_RXIN1-
EVEN_RXIN1+
EVEN_RXIN2-
EVEN_RXIN2+
EVEN_CLKIN-
EVEN_CLKIN+
DCBATOUT
L43
600R-100MHZ_0805
ACMS201209A601 2A
C541
NC_0.1U_50V_K_B
0603_X7R
C543
1U_25V_Y
0805_Y5V
C542
0.1U_50V_K_B
0603_X7R
C539
0.1U_50V_K_B
0603_X7R
DCBATOUT_I
2A
CN19
HEADER_8P
FOX_HS6108E
INVERTER CONN.
INV_ENABLE
INV_BRADJ
DVT
LCD_OFF#
U23
MC74VHC1G08DFT2G
19 AT_BRADJ
R2
10K_J
0402
R392
10K_J
0402
C535
NC_100P_50V_J
0402_NPO
+3VRUN
U25A
74LVC2G08DC
29 INV_EN
BL_OFF#
INV_ENABLE_2
U2
MC74VHC1G08DFT2G
R394
10K_J
0402
C537
NC_100P_50V_J
0402_NPO
R10
NC_0_J
0402
INV_ENABLE_1
U25B
74LVC2G08DC
33,50 LIDIN#
18 AT_INV_EN
(3.3V tolerant)
R393
10K_J
0402
C2
4.7U_6.3V_K
0603_X5R
U1
IN1
OUT
EN
GND
IN5
IN4
IN3
IN2
THERMAL PAD
G5281RC1U_V0.1
C526
4.7U_6.3V_K
0603_X5R
C530
0.1U_6.3V_K
0402_X5R
C1
0.1U_6.3V_K
0402_X5R
LCDVCC
U6
33 LCD_OFF#
19 AT_LCDVCC_EN
LCD_PWR_EN
MC74VHC1G08DFT2G
R908
10K_J
0402
R1
100K_J
0402
SW1
HDS406-021E_SW-SMD12
null
LCDID0
LCDID1
LCDID2
FAN_ED_SW
INST_ON_SW#
TP416 20MIL
PVT
PANEL ID
Type WXGA+ WXGA+
Size 15.6"W 15.6"W
Vendor CPT LGD
Device Name CLAA156WA01A LP156WH1-TLC1
Panel ID [3.2.1] 001 010
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title LVDS
Size A3
Document Number M850-1-01
Rev 1.0
Date: Thursday, July 09, 2009
Sheet 25 of 69



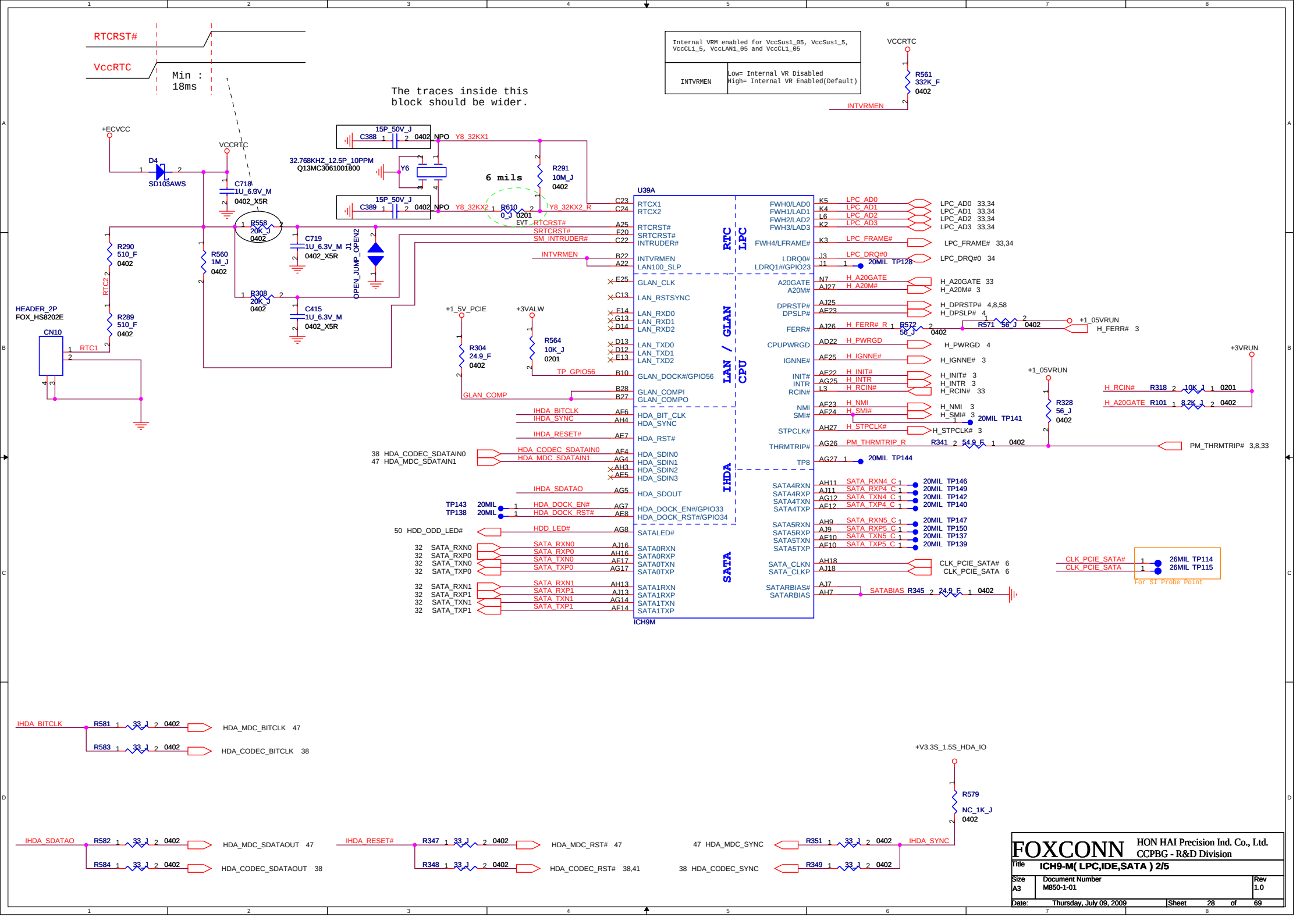
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 26 of 69	

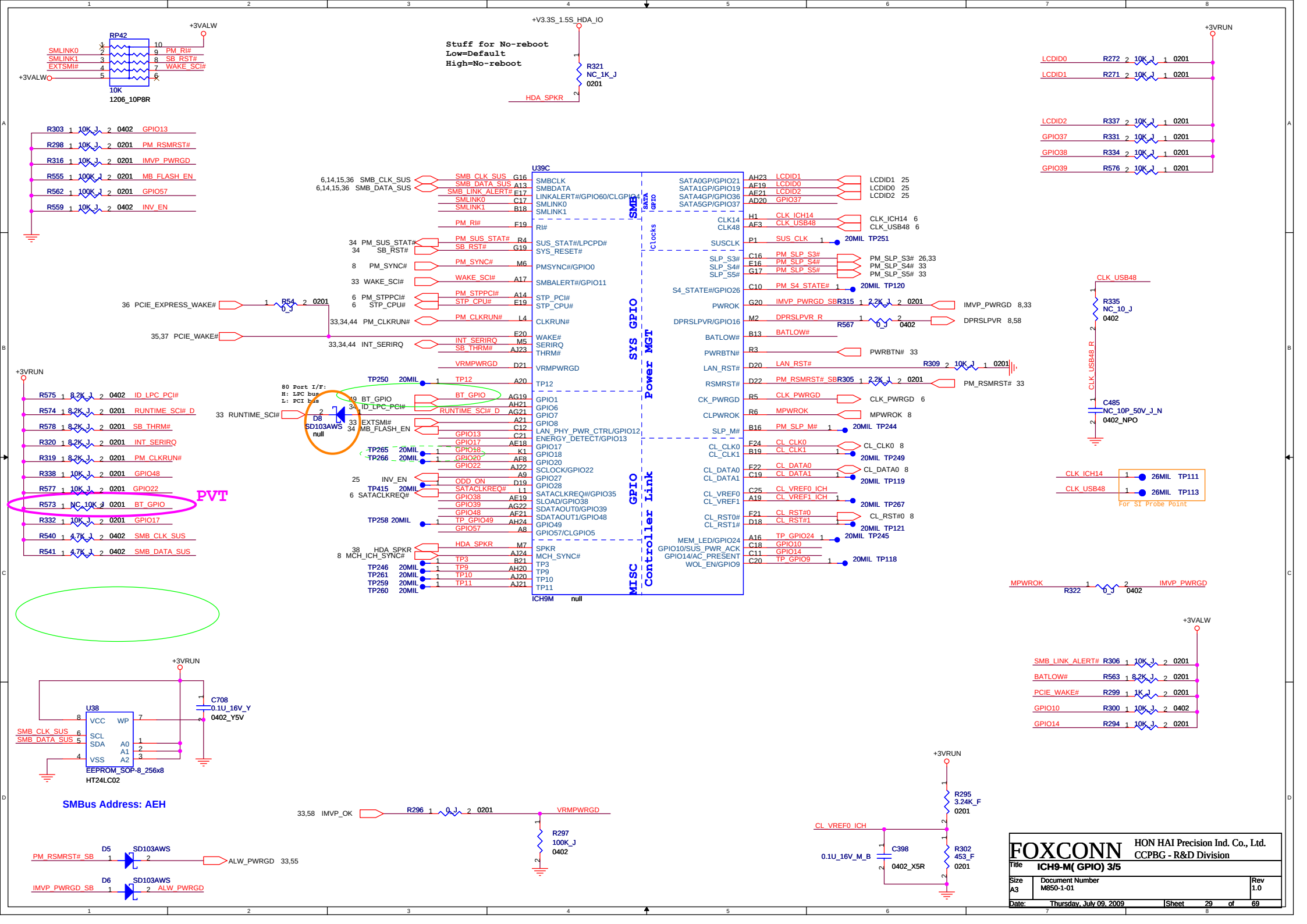


USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	Ext. Port
PORT-3	
PORT-4	Bluetooth
PORT-5	EXPRESS CARD
PORT-6	
PORT-7	Camera
PORT-8	Felica
PORT-9	
PORT-10	Wi-MAX
PORT-11	

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ICH9-M(PCI/DMI/USB/PCIE) 1/5	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 27 of 69	


RTCRST#
VccRTC
Min : 18ms
The traces inside this block should be wider.
Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05
INTVRMEN
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
VCCRTC
R561 332K_F 0402
INTVRMEN
+ECVCC
D4 SD103AWS
C718 1U_6.3V_M 0402_X5R
15P_50V_J C388 0402 NPO Y8_32KX1
32.768KHZ_12.5P_10PPM Q13MC3061001800 Y6
15P_50V_J C389 0402 NPO Y8_32KX2
6 mils
R291 10M_J 0402
R610 0_J 0201 EVT
Y8_32KX2_R
R558 20K_J 0402
R290 510_F 0402
R560 1M_J 0402
R308 20K_J 0402
C719 1U_6.3V_M 0402_X5R
C415 1U_6.3V_M 0402_X5R
OPEN_JUMP_OPEN2
HEADER_2P FOX_HS8202E
CN10
RTC1
RTC2
R289 510_F 0402
+1_5V_PCIE
+3VALW
R304 24.9_F 0402
R564 10K_J 0201
GLAN_COMP
TP_GPIO56
U39A
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_AD0 33,34
LPC_AD1 33,34
LPC_AD2 33,34
LPC_AD3 33,34
LPC_FRAME# 33,34
LPC_DRQ#0 34
20MIL TP128
H_A20GATE 33
H_A20M# 3
H_DPRSTP# 4,8,58
H_DPSLP# 4
H_FERR# 3
+1_05VRUN
H_PWRGD 4
H_IGNNE# 3
H_INIT# 3
H_INTR 3
H_RCIN# 33
H_NMI 3
H_SMI# 3
20MIL TP141
H_STPCLK# 3
PM_THRMTRIP# 3,8,33
20MIL TP144
+3VRUN
H_RCIN# R318 10K_J 0201
H_A20GATE R101 8.2K_J 0402
R328 56_J 0402
SATA_RXN4_C 20MIL TP146
SATA_RXP4_C 20MIL TP149
SATA_TXN4_C 20MIL TP142
SATA_TXP4_C 20MIL TP140
SATA_RXN5_C 20MIL TP147
SATA_RXP5_C 20MIL TP150
SATA_TXN5_C 20MIL TP137
SATA_TXP5_C 20MIL TP139
CLK_PCIE_SATA# 6
CLK_PCIE_SATA 6
SATABIAS R345 24.9_F 0402
CLK_PCIE_SATA#
CLK_PCIE_SATA
26MIL TP114
26MIL TP115
For SI Probe Point
38 HDA_CODEC_SDATAIN0
47 HDA_MDC_SDATAIN1
IHDA_BITCLK
IHDA_SYNC
IHDA_RESET#
IHDA_SDATAO
TP143 20MIL
TP138 20MIL
HDA_DOCK_EN#
HDA_DOCK_RST#
50 HDD_ODD_LED#
HDD_LED#
32 SATA_RXN0
32 SATA_RXP0
32 SATA_TXN0
32 SATA_TXP0
32 SATA_RXN1
32 SATA_RXP1
32 SATA_TXN1
32 SATA_TXP1
IHDA_BITCLK R581 33_J 0402 HDA_MDC_BITCLK 47
R583 33_J 0402 HDA_CODEC_BITCLK 38
+V3.3S_1.5S_HDA_IO
R579 NC_1K_J 0402
IHDA_SDATAO R582 33_J 0402 HDA_MDC_SDATAOUT 47
R584 33_J 0402 HDA_CODEC_SDATAOUT 38
IHDA_RESET# R347 33_J 0402 HDA_MDC_RST# 47
R348 33_J 0402 HDA_CODEC_RST# 38,41
47 HDA_MDC_SYNC R351 33_J 0402 IHDA_SYNC
38 HDA_CODEC_SYNC R349 33_J 0402
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title ICH9-M(LPC,IDE,SATA) 2/5
Size A3
Document Number M850-1-01
Rev 1.0
Date: Thursday, July 09, 2009
Sheet 28 of 69


RP42
+3VALW
SMLINK0
SMLINK1
EXTSMI#
PM_RI#
SB_RST#
WAKE_SCI#
10K
1206_10P8R
+V3.3S_1.5S_HDA_IO
Stuff for No-reboot
Low=Default
High=No-reboot
R321
NC_1K_J
0201
HDA_SPKR
+3VRUN
LCDID0
LCDID1
LCDID2
GPIO37
GPIO38
GPIO39
R272
R271
R337
R331
R334
R576
R303
R298
R316
R555
R562
R559
GPIO13
PM_RSMRST#
IMVP_PWRGD
MB_FLASH_EN
GPIO57
INV_EN
U39C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP12
GPIO1
GPIO6
GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP9
TP10
TP11
SMB
SATA GPIO
CLocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M
null
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
MEM_LED/GPIO24
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
WOL_EN/GPIO9
LCDID1
LCDID0
LCDID2
GPIO37
CLK_ICH14
CLK_USB48
SUS_CLK
PM_SLP_S3#
PM_SLP_S4#
PM_SLP_S5#
PM_S4_STATE#
IMVP_PWRGD_SB
DPRSLPVR_R
BATLOW#
PWRBTN#
LAN_RST#
PM_RSMRST#_SB
CK_PWRGD
MPWROK
PM_SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST#0
CL_RST#1
TP_GPIO24
GPIO10
GPIO14
TP_GPIO9
R309
R305
R315
R567
R335
NC_10_J
0402
C485
NC_10P_50V_J_N
0402_NPO
CLK_USB48_R
CLK_ICH14
CLK_USB48
26MIL
TP111
TP113
For SI Probe Point
MPWROK
IMVP_PWRGD
R322
PCIE_EXPRESS_WAKE#
R54
PCIE_WAKE#
PM_CLKRUN#
INT_SERIRQ
SB_THRM#
PM_STPPCI#
STP_CPU#
PM_SYNC#
WAKE_SCI#
PM_SUS_STAT#
SB_RST#
SMB_CLK_SUS
SMB_DATA_SUS
SMB_LINK_ALERT#
SMLINK0
SMLINK1
PM_RI#
RUNTIME_SCI#
ID_LPC_PCI#
BT_GPIO
TP250
TP265
TP266
TP415
TP258
TP246
TP261
TP259
TP260
TP3
TP9
TP10
TP11
ODD_ON
SATACLKREQ#
TP_GPIO49
HDA_SPKR
MCH_ICH_SYNC#
D8
SD103AWS
80 Port I/F:
H: LPC bus
L: PCI bus
R575
R574
R578
R320
R319
R338
R577
R573
R332
R540
R541
SMB_CLK_SUS
SMB_DATA_SUS
GPIO48
GPIO22
GPIO17
PVT
U38
VCC
WP
SCL
SDA
A0
A1
A2
VSS
EEPROM_SOP-8_256x8
HT24LC02
C708
0.1U_16V_Y
0402_Y5V
SMBus Address: AEH
IMVP_OK
R296
VRMPWRGD
R297
100K_J
0402
D5
D6
PM_RSMRST#_SB
IMVP_PWRGD_SB
ALW_PWRGD
R295
3.24K_F
0201
C398
0.1U_16V_M_B
0402_X5R
R302
453_F
BATLOW#
R563
PCIE_WAKE#
R299
R300
R294
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
ICH9-M(GPIO) 3/5
Size
A3
Document Number
M850-1-01
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1.0
Date:
Thursday, July 09, 2009
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29
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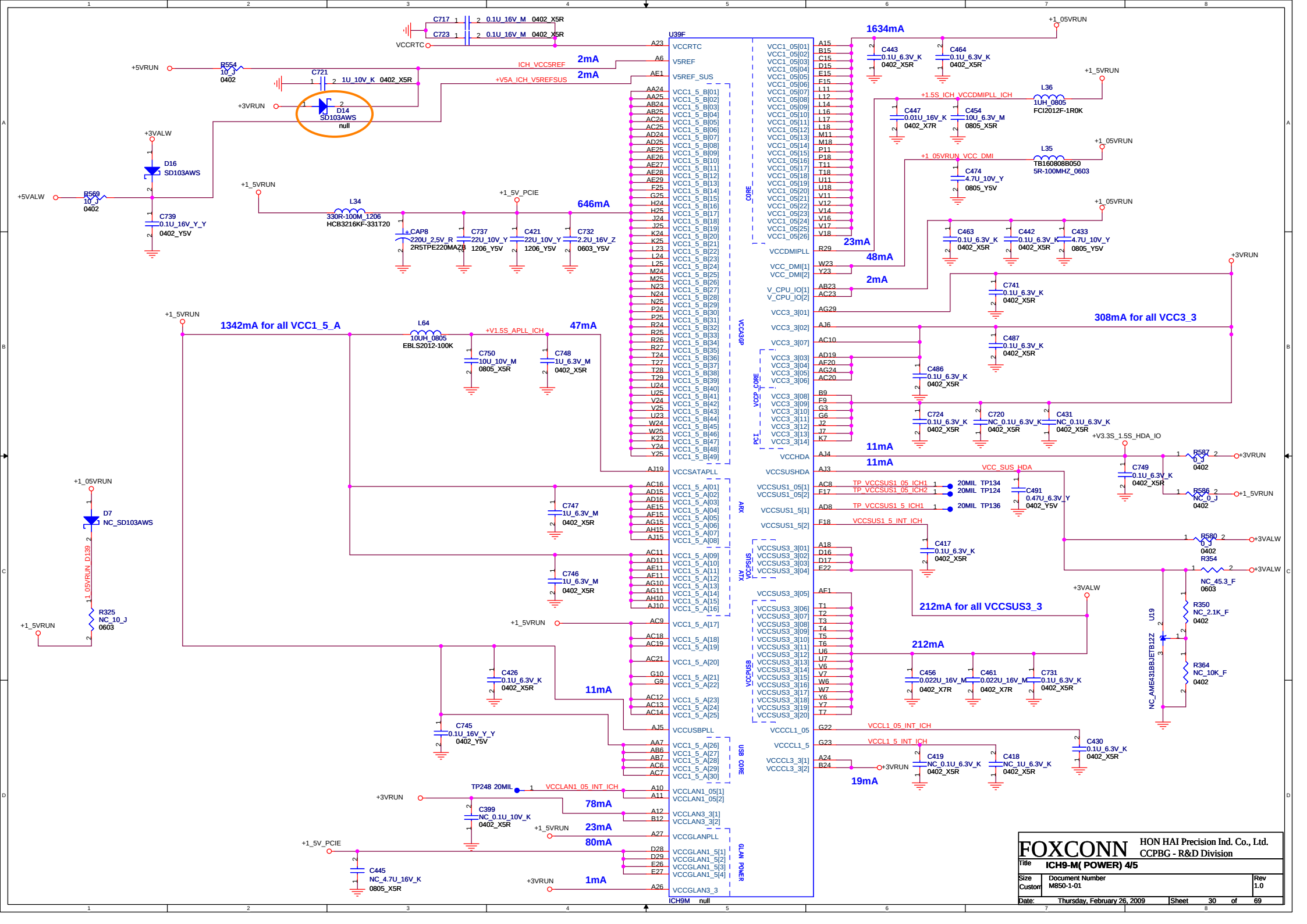
69



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	ICH9-M(POWER) 4/5
Size: Custom	Document Number: M850-1-01
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Date:	Thursday, February 26, 2009
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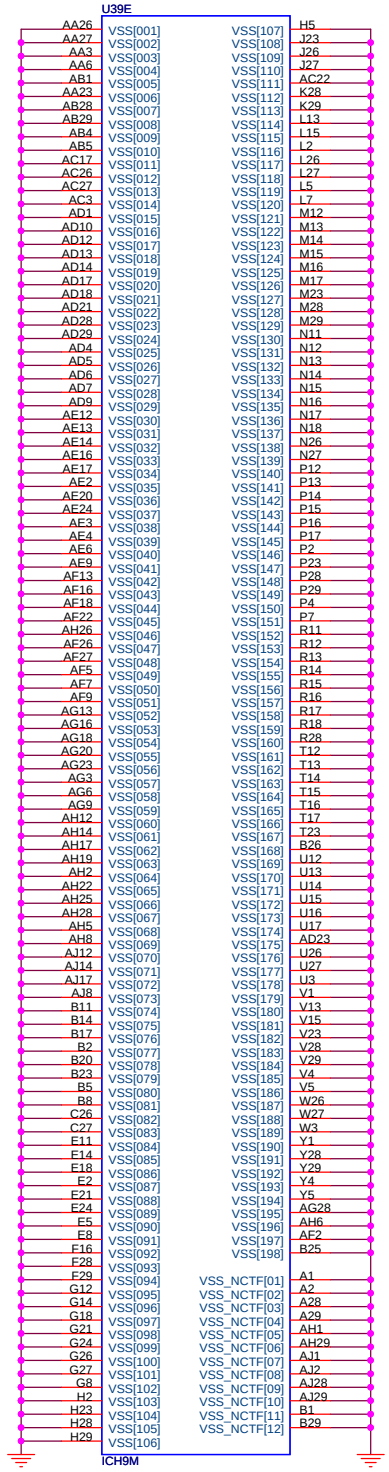
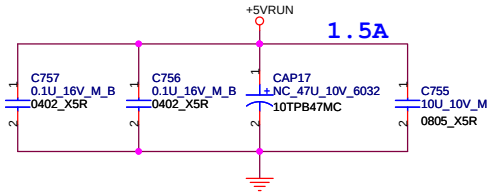
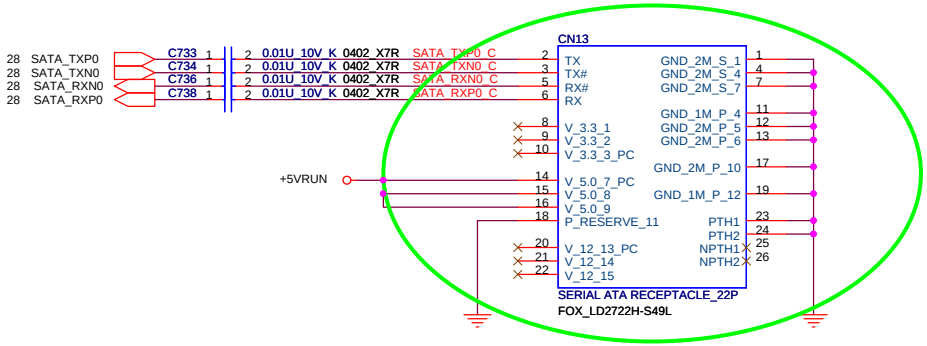


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ICH9-M(GND) 5/5	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, February 26, 2009	Sheet 31 of 69	

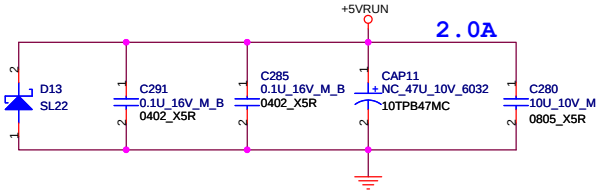
SATA HDD CONN

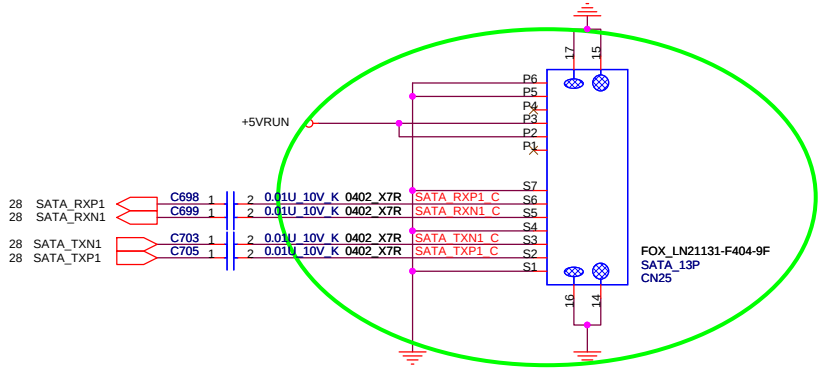


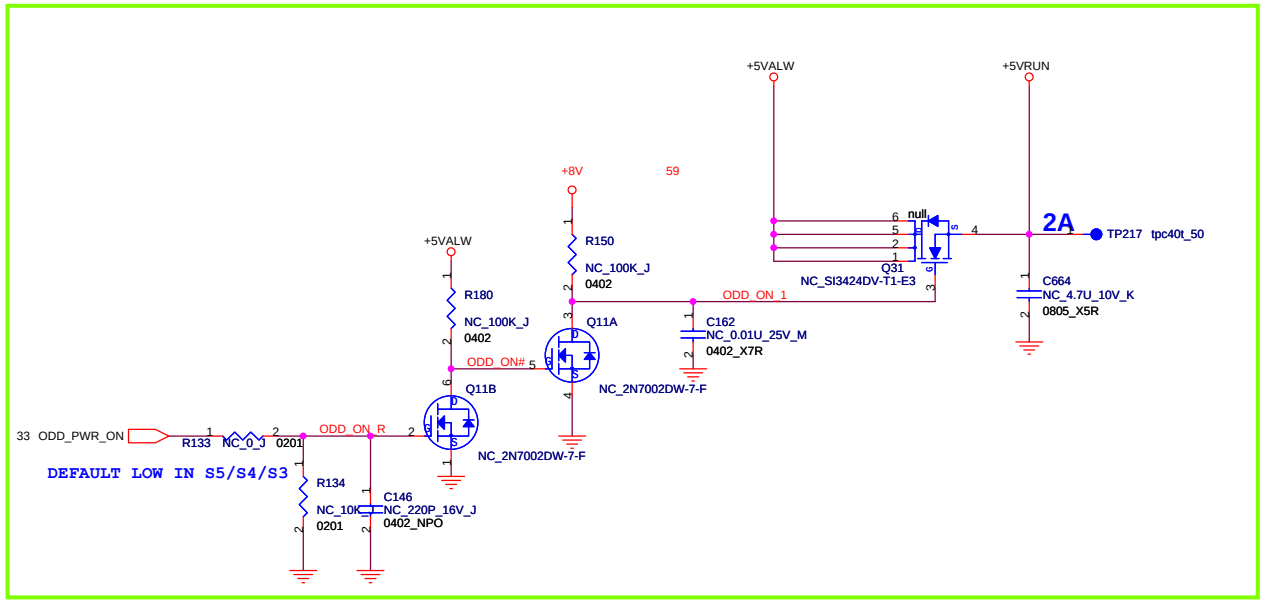


EVT

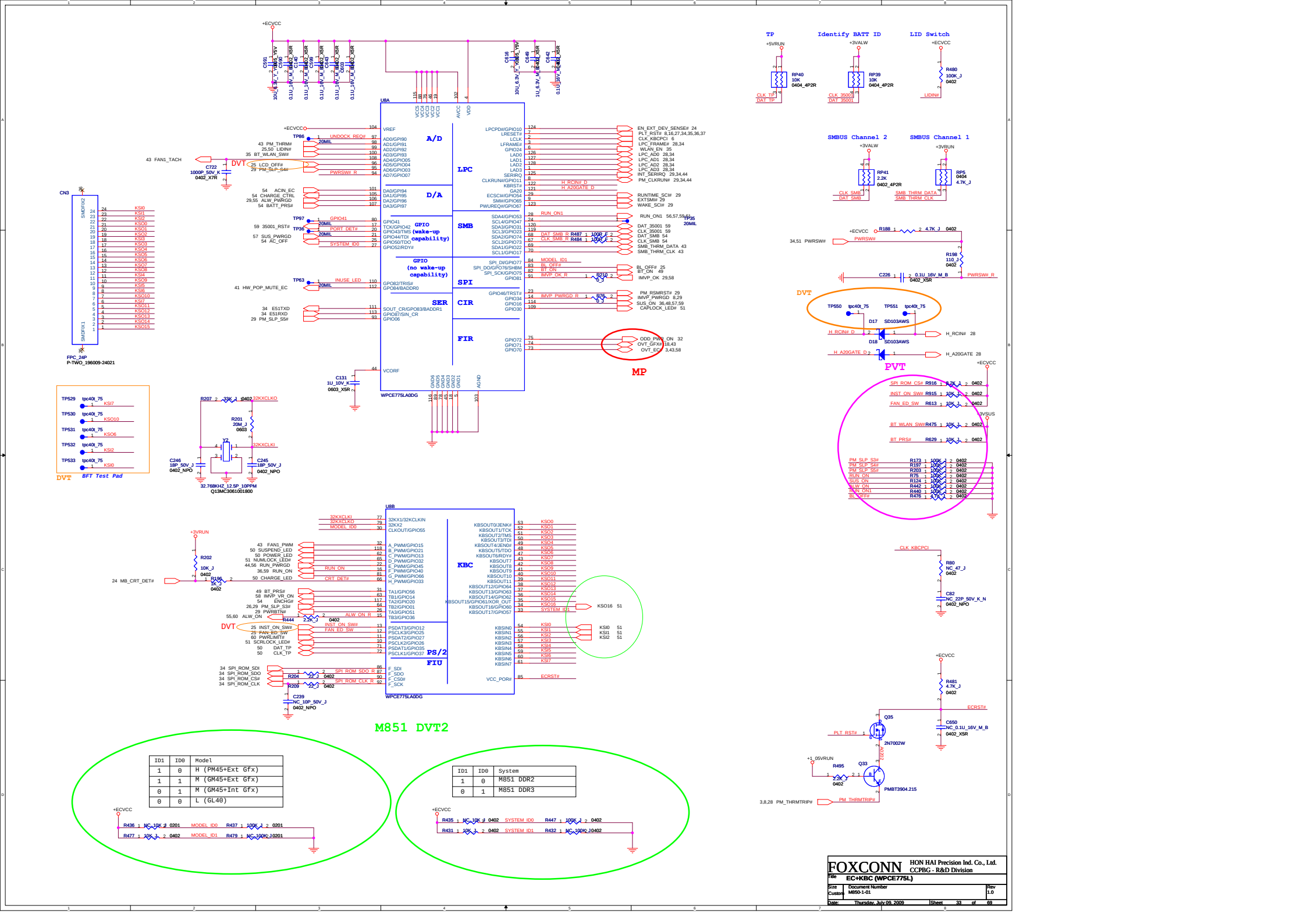
SATA ODD CONN







FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD/ODD		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Thursday, July 09, 2009	Sheet 32 of 69	


TP
Identify BATT ID
LID Switch
SMBUS Channel 2
SMBUS Channel 1
DVT
PVT
MP
BFT Test Pad
U8A
WPCE775LA0DG
U8B
WPCE775LA0DG
A/D
LPC
D/A
SMB
GPIO (wake-up capability)
GPIO (no wake-up capability)
SPI
SER
CIR
FIR
KBC
PS/2 FIU
M851 DVT2
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
EC+KBC (WPCE775L)
Thursday, July 09, 2009
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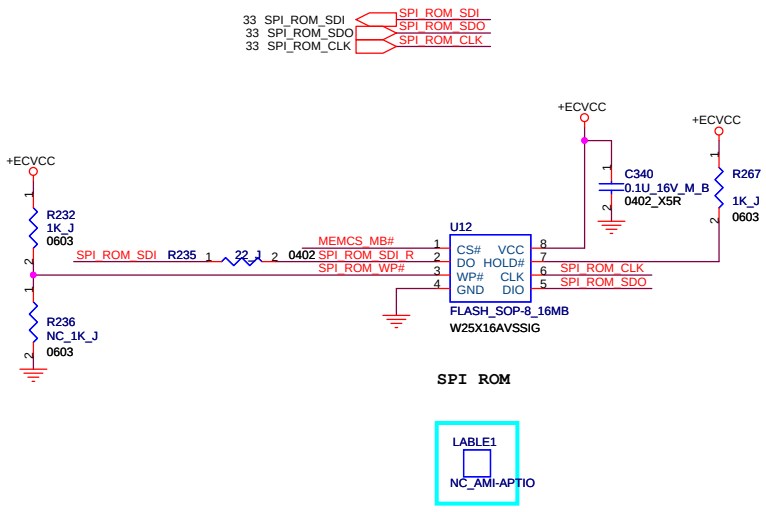
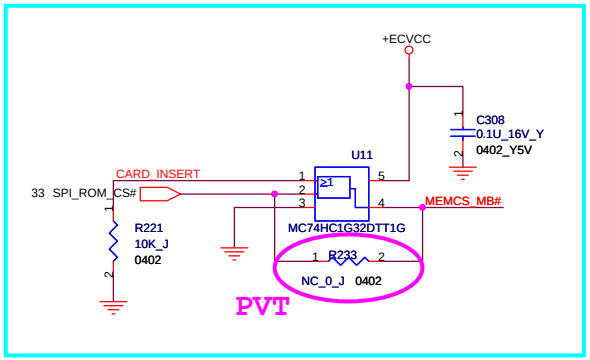
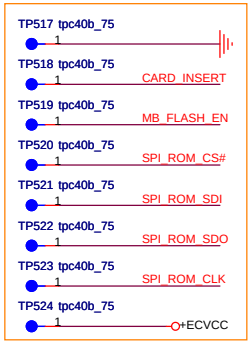
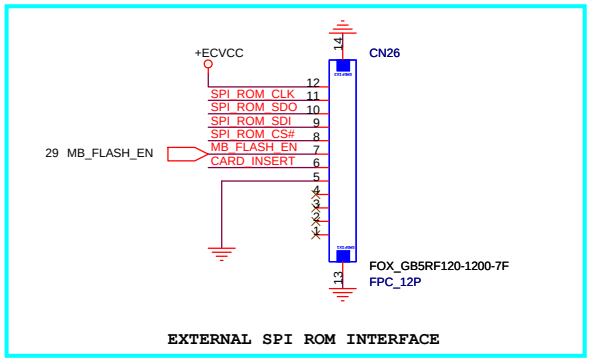
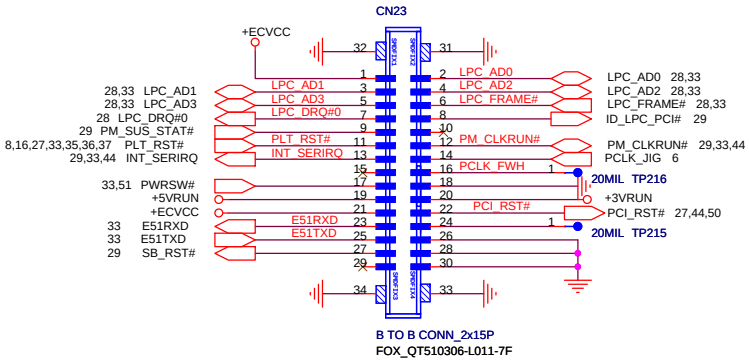






DVT *BFT Test Pad*





FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Flash ROM/SPI	
Size A3	Document Number M850-1-01	Rev 1.0
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BOSS2
BOSS_4x5.2

BOSS1
BOSS_4x5.2

Half Mini Card

+1_5V=>0.5A Peak/0.375A Normal
+3_3VAux=>2.75A Peak/1.1A Normal

WLAN ON/OFF Switch

BT_WLAN_SW# → BT_WLAN_SW# 33

1BS007-12110-002-7F_SW_SMD7
SW4

CN21

29,37 PCIE_WAKE#		1	WAKE#	+3.3Vaux_1	2		MINI_PCIE_+3_3V
49 WIRELESS_DATA	WIRELESS_DATA	3	BT_DATA	GND_1	4		MINI_PCIE_+1_5V
49 WIRELESS_CHCLK	WIRELESS_CHCLK	5	BT_CHCLK	NC_1	6		
6 MINI_CARD_DET#	MINI_CARD_DET#	7	CLKREQ#	NC_2	8		
		9	GND_2	NC_3	10		
6 CLK_PCIE_MINI#		11	REFCLK-	NC_4	12		
6 CLK_PCIE_MINI		13	REFCLK+	NC_5	14		
		15	GND_3	NC_6	16		
		17	NC_7	GND_4	18		
		19	NC_8	W_DISABLE#	20		
27 MINI_RXN2		21	GND_5	PERST#	22	PLT_RST# 8,16,27,33,34,36,37	
27 MINI_RXP2		23	PETn0	+3.3Vaux_2	24		MINI_PCIE_+3_3V
		25	PETp0	GND_6	26		MINI_PCIE_+1_5V
		27	GND_7	NC_9	28		
		29	GND_8	NC_10	30		
27 MINI_TXN2		31	PERn0	NC_11	32		
27 MINI_TXP2		33	PERp0	GND_9	34		
		35	GND_10	NC_12	36		USB_PN10_L
		37	GND_11	NC_13	38		USB_PP10_L
MINI_PCIE_+3_3V		39	+3.3Vaux_3	NC_14	40		
		41	+3.3Vaux_4	NC_15	42		
		43	GND_12	LED_WLAN#	44		MINI_CARD_LED#
		45	C-Link_CLK	NC_16	46	A4311 1	20MIL TP159
		47	C-Link_DAT	NC_17	48		MINI_PCIE_+1_5V
		49	C-Link_RST	GND_13	50		
		51	NC_18	+3.3Vaux_5	52		MINI_PCIE_+3_3V

SMDFIX1 (53, 55) NPTH1
SMDFIX2 (54, 56) NPTH2

MINI PCI CONN_2x26P
FOX_AS0B226_S68N_7F

Half Mini Card
WLAN

for RF team test VEDS, MP will delete

R914 0_J 0402: WLAN_EN 33 ↔ PLT_RST#

Q21 SRK7002 · D22 BAS316PT · Q20 DTA114YUA · +3VSUS

WLAN_EN

R386 120_J 0402

TP180 tpc40t_75 · TP184 tpc40t_75

49 BT_LED

R630 NC_100K_J 0402 · Q49 DTC144EUA

LED3 HT-110UYG null

M851 PVT

WIRELESS LED

TURN WIRELSS LED ON WHEN EITHER WLAN OR BT IS ENABLED.

+3VSUS

R387 0_J 0805 · MINI_PCIE_+3_3V

C538 NC_22U_6.3V_M 0805_X5R
C531 0.1U_16V_Y 0402_Y5V
C546 0.1U_16V_Y 0402_Y5V
C529 10U_10V_M 0805_X5R
C548 10U_10V_M 0805_X5R

C534 NC_0.1U_16V_Y 0402_Y5V

U24 NC_SN74CB3Q3305PW

27 USB_PN10 ↔ USB_PN10_L
USB_PP10_L ↔ USB_PP10 27

+1_5VRUN

R396 0_J 0603 · MINI_PCIE_+1_5V

C545 0.1U_10V_K 0402_X5R
C544 NC_10U_10V_M 0805_X5R
C536 NC_10U_10V_M 0805_X5R

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	Half Mini Card
Size A3	Document Number M850-1-01 · Rev 1.0
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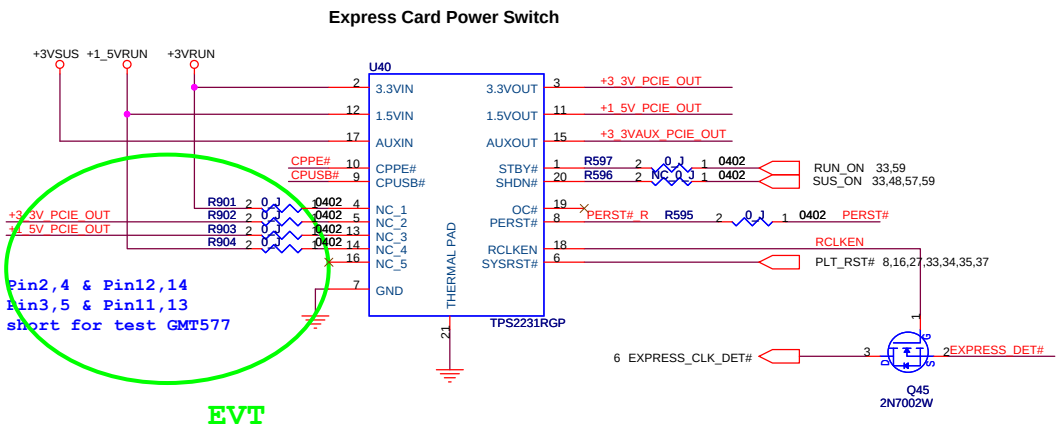
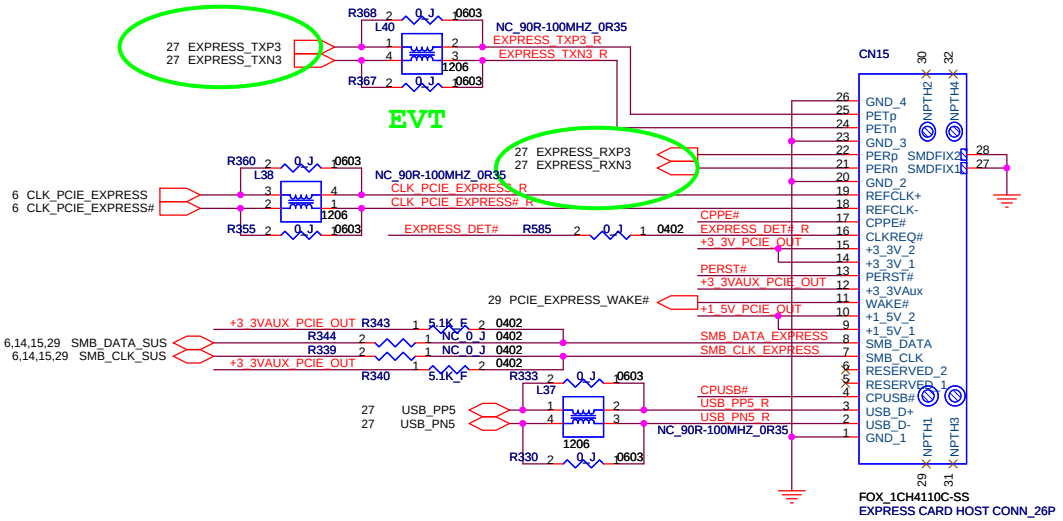
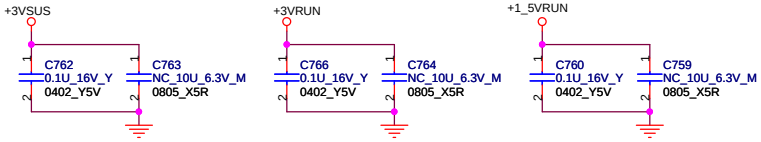
+1_5V=>1.3A
+3_3VAux=>0.6A
+3_3V=>2.5A

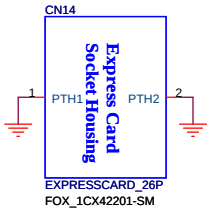
Express Card Power Switch

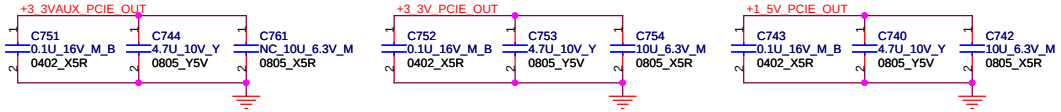




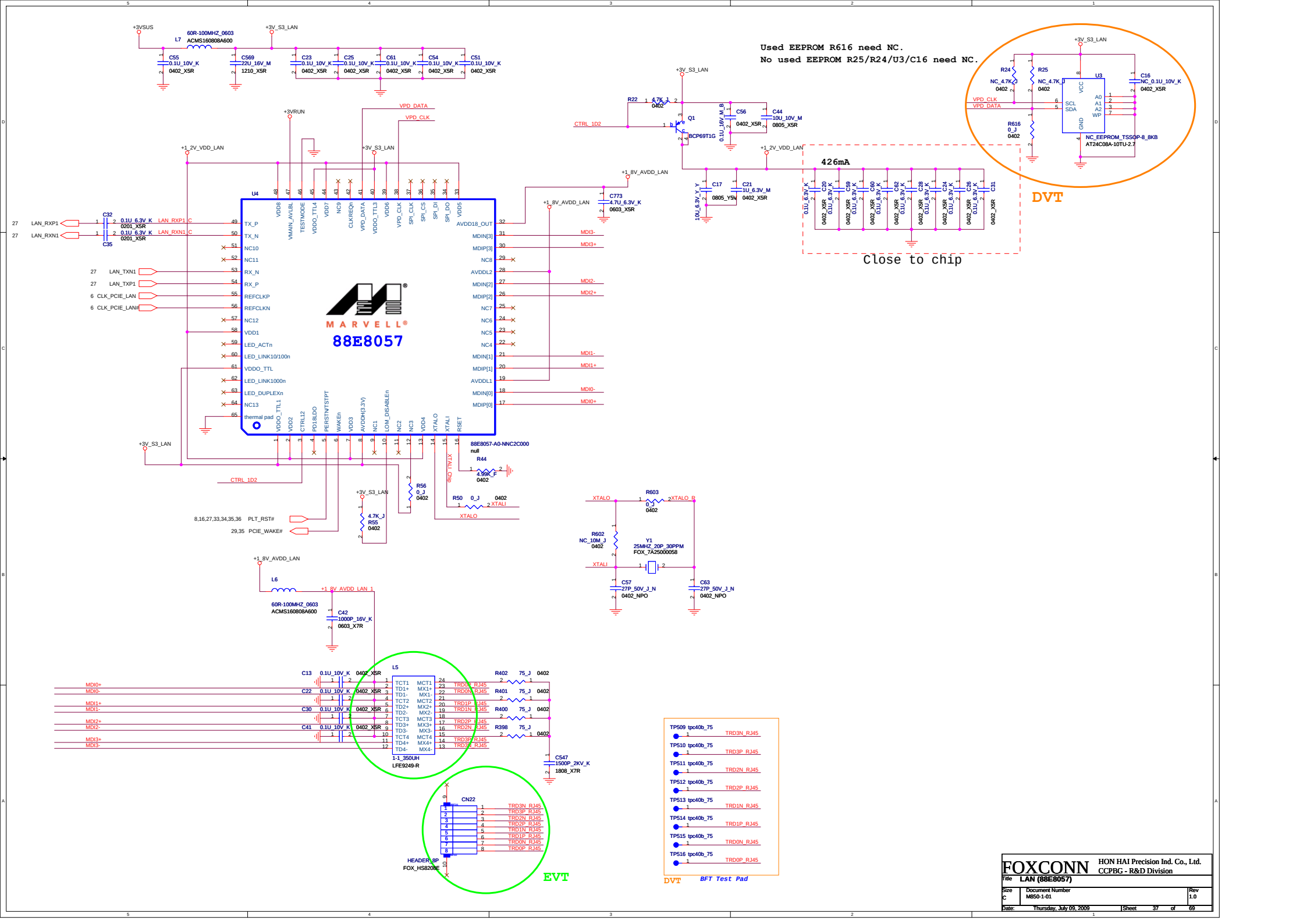
Express Card Slot.

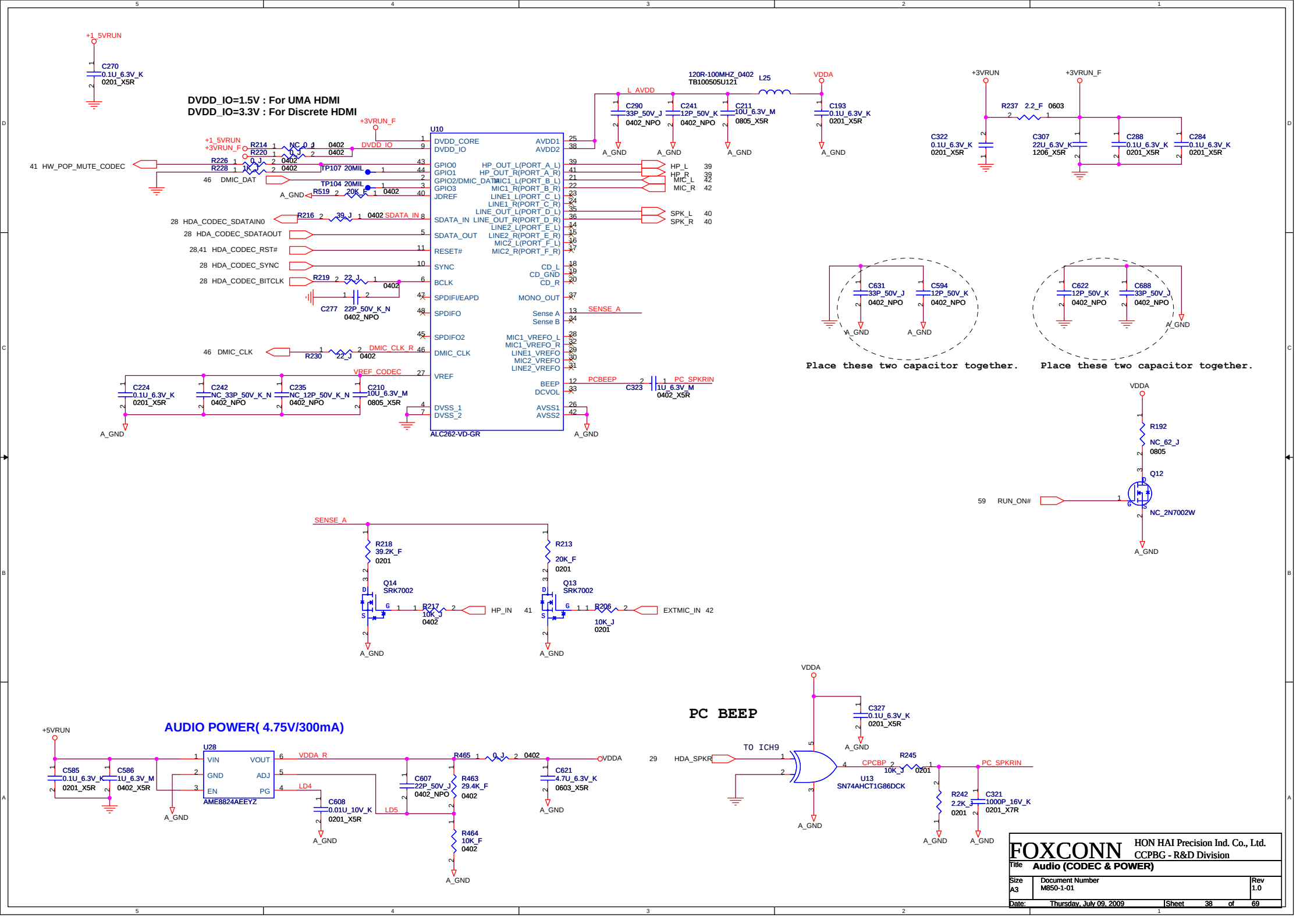






FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: EXPRESS CARD		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Wednesday, April 01, 2009	Sheet 36 of 69	


Used EEPROM R616 need NC.
No used EEPROM R25/R24/U3/C16 need NC.
DVT
426mA
Close to chip
88E8057
MARVELL
EVT
DVT
BFT Test Pad
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title LAN (88E8057)
Size C
Document Number M850-1-01
Rev 1.0
Date: Thursday, July 09, 2009
Sheet 37 of 69


DVDD_IO=1.5V : For UMA HDMI
DVDD_IO=3.3V : For Discrete HDMI
U10
ALC262-VD-GR
Place these two capacitor together.
Place these two capacitor together.
AUDIO POWER(4.75V/300mA)
U28
AME8824AEEYZ
PC BEEP
TO ICH9
U13
SN74AHCT1G86DCK
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
Audio (CODEC & POWER)
Size
A3
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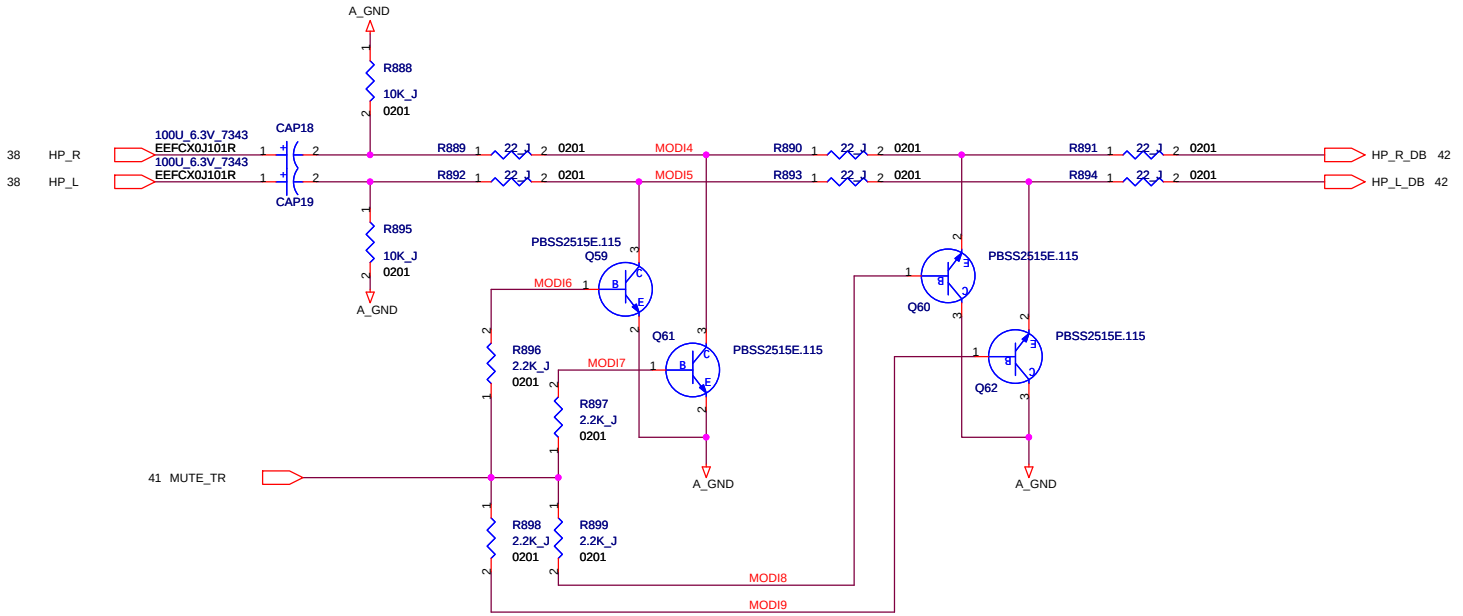
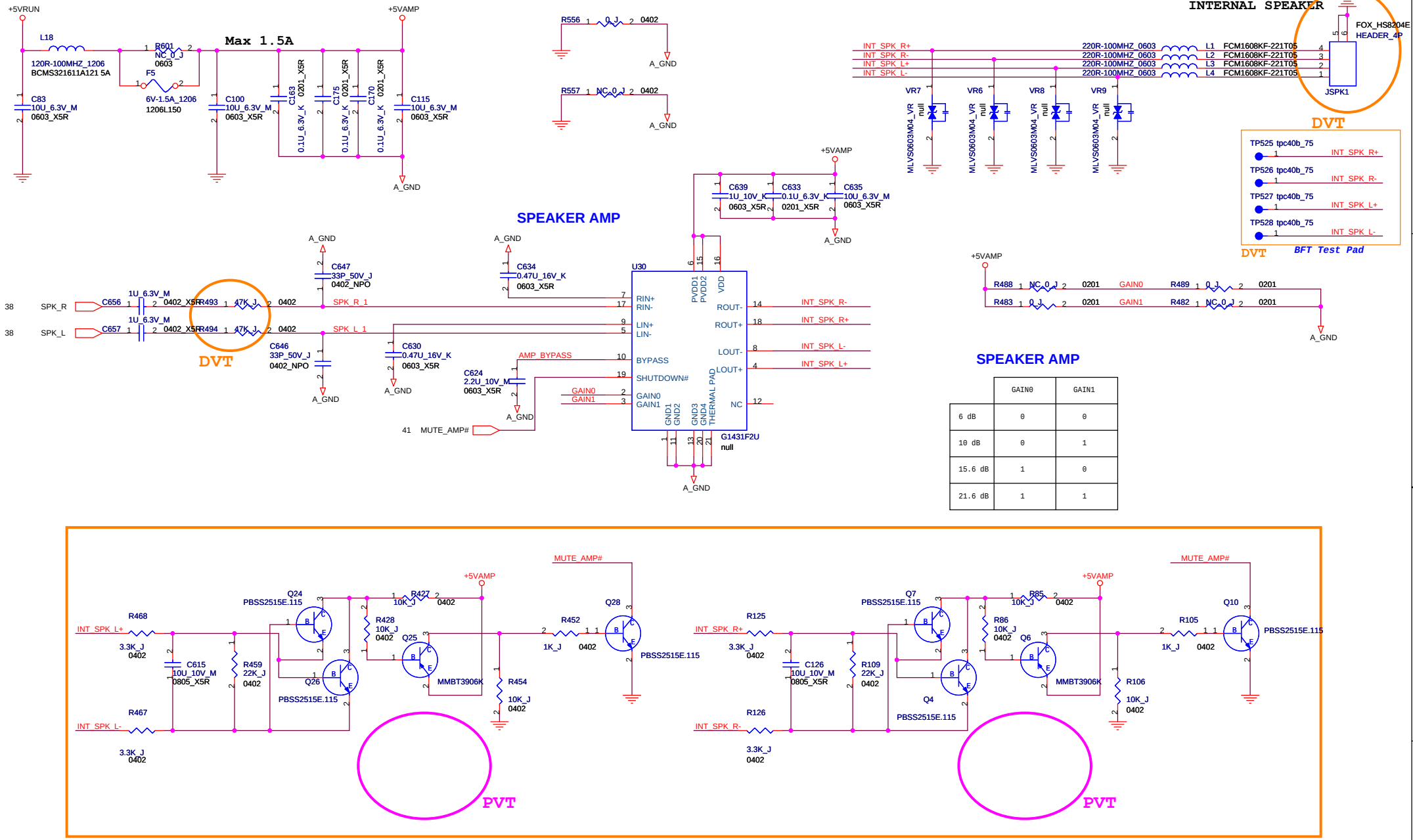


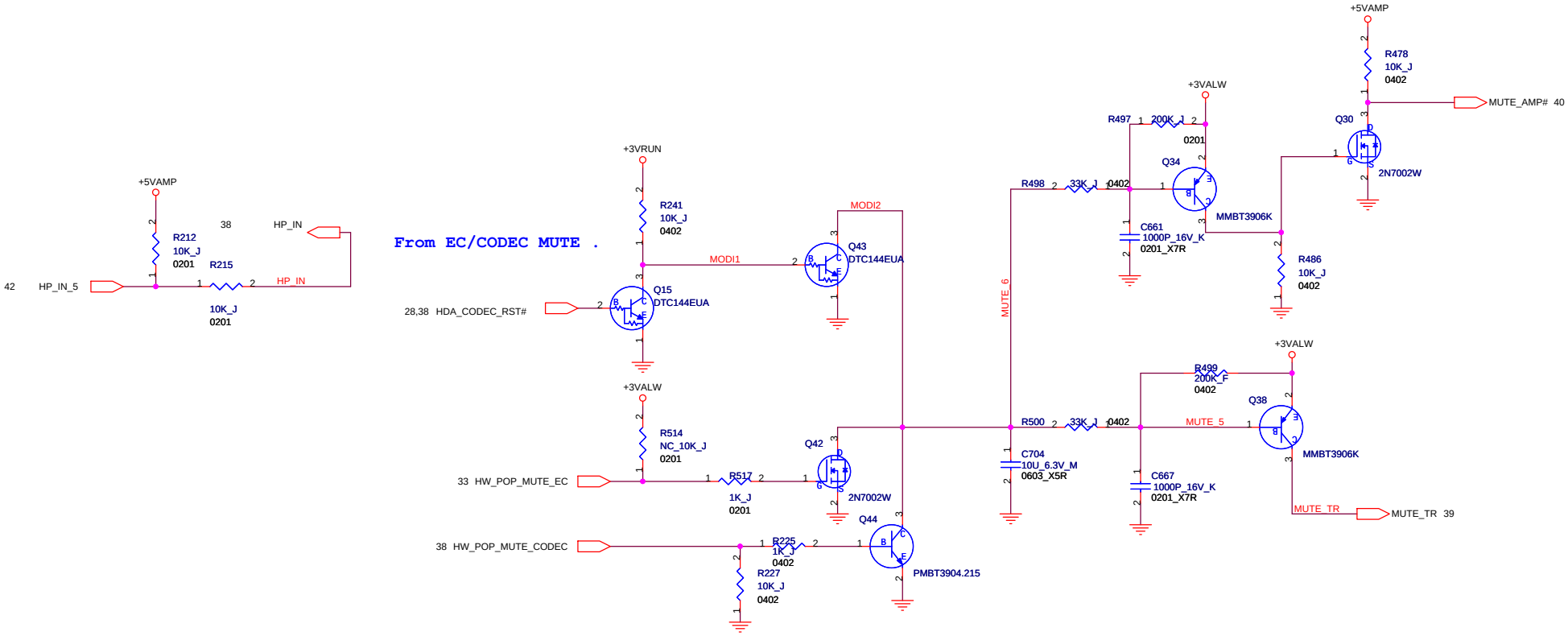
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (HP)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Monday, July 13, 2009	Sheet 39 of 69	



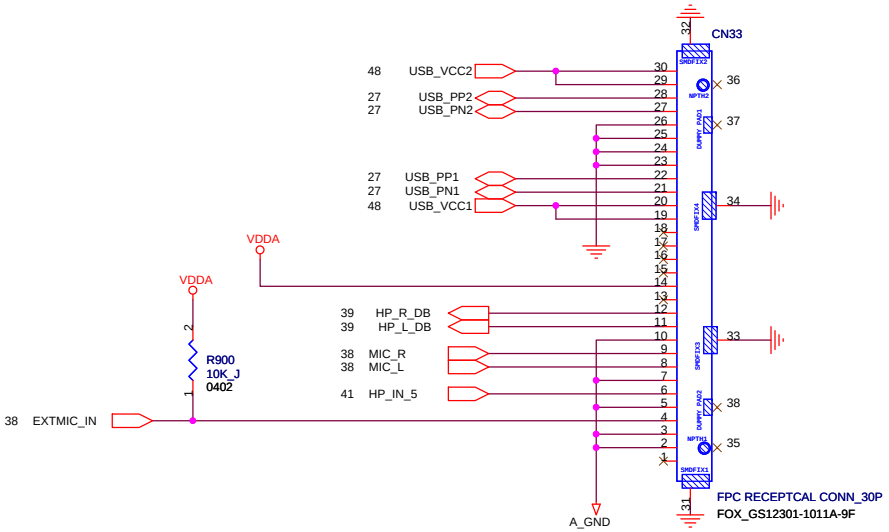
	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

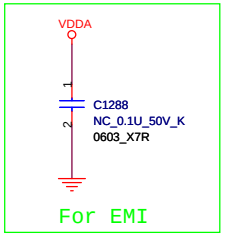
FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Audio (SPKR)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 40 of 69	

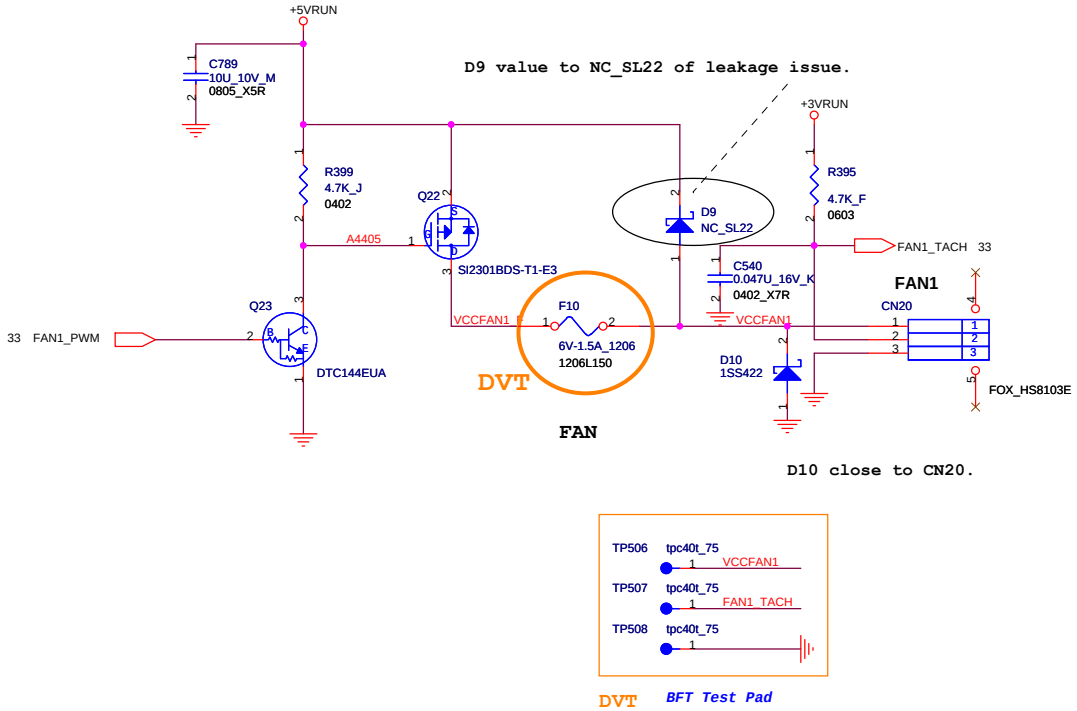


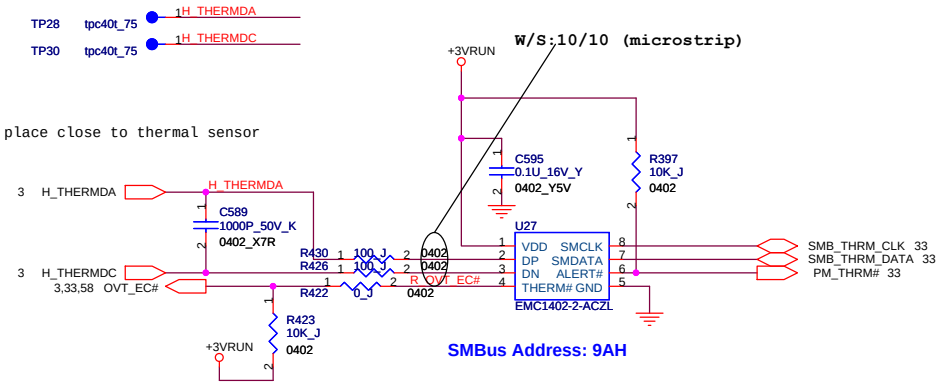
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (MUTE)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 41 of 69	

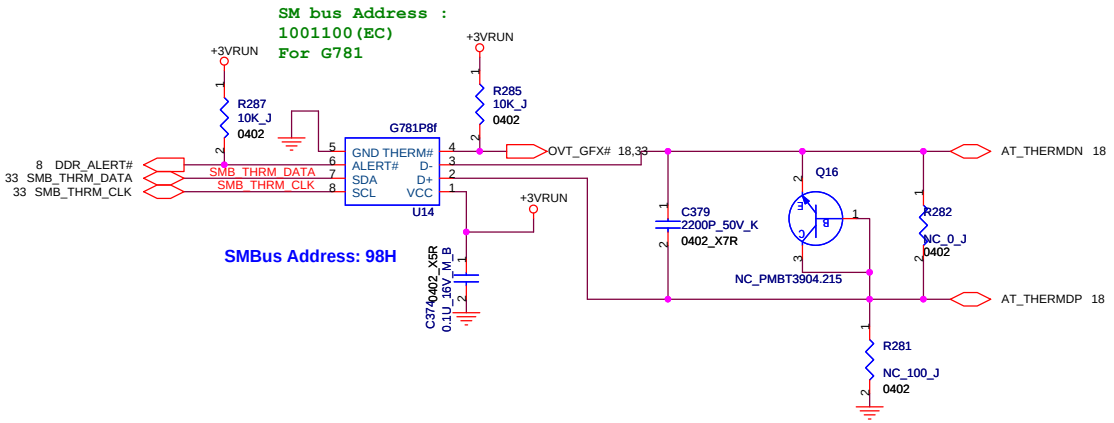




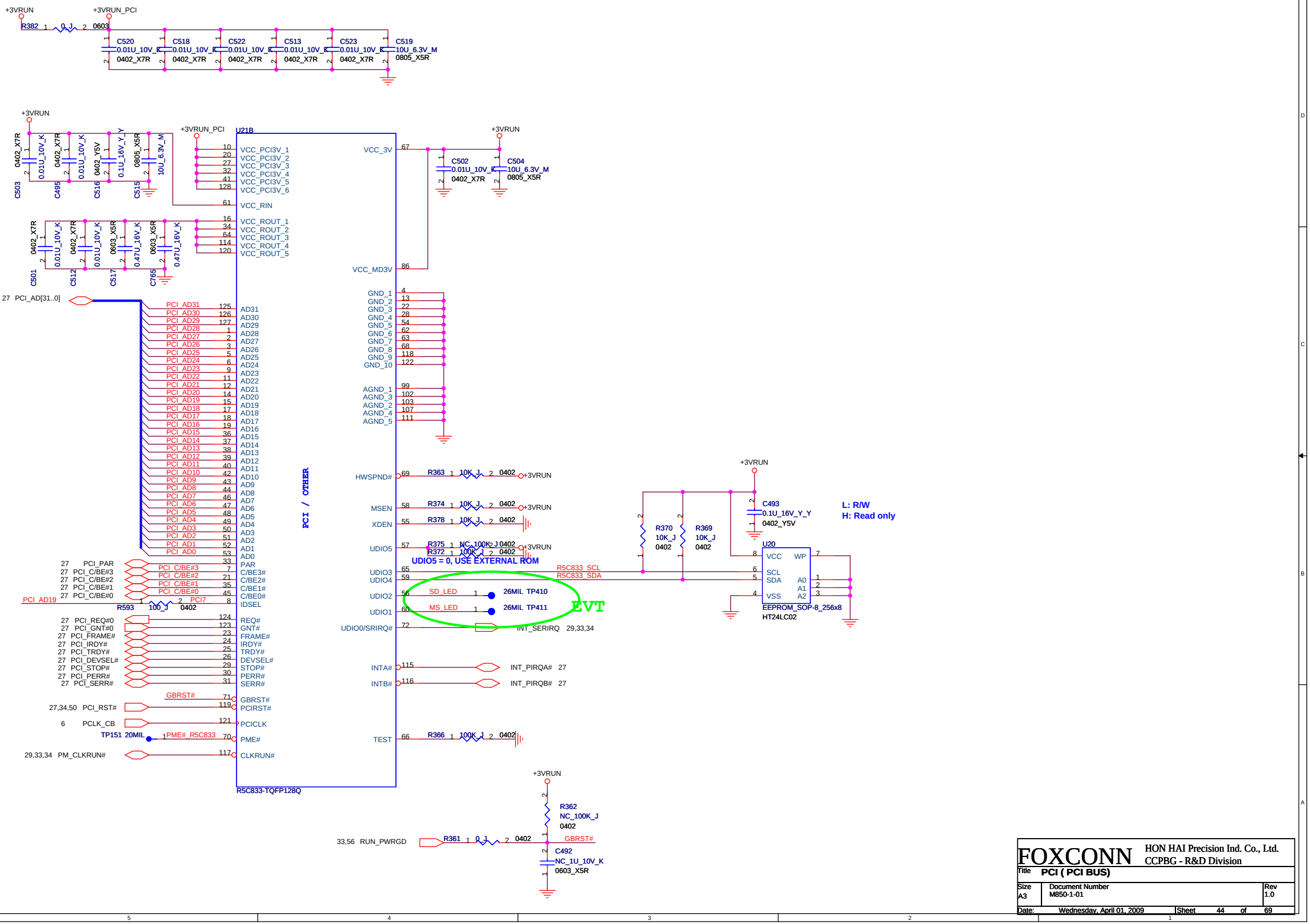
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: **Audio+USB MB CONN**		
Size: A3	Document Number: **M850-1-01**	Rev: **1.0**
Date: Wednesday, April 01, 2009	Sheet 42 of 69	



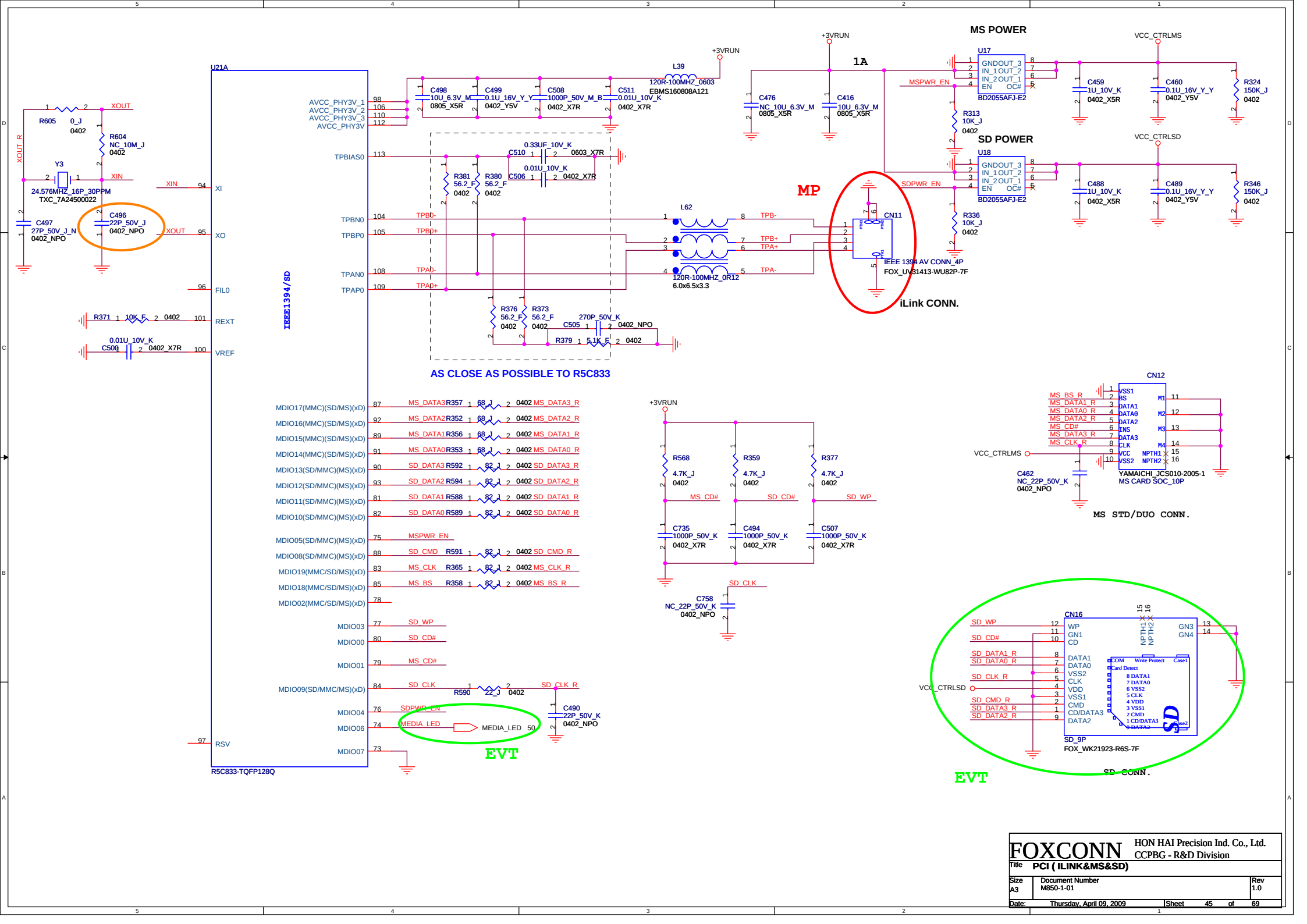


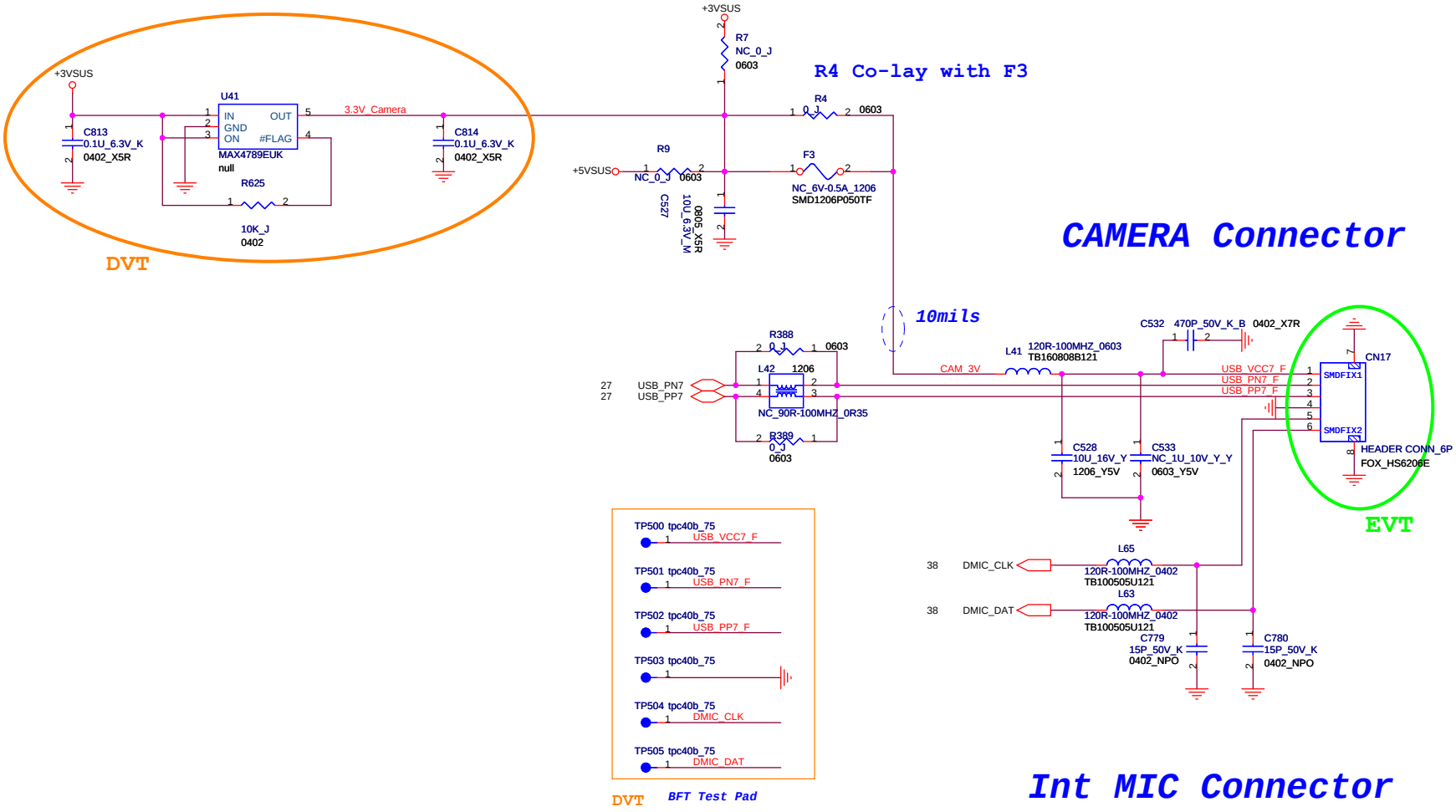


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: FAN/Thermal		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Wednesday, April 01, 2009	Sheet 43 of 69	

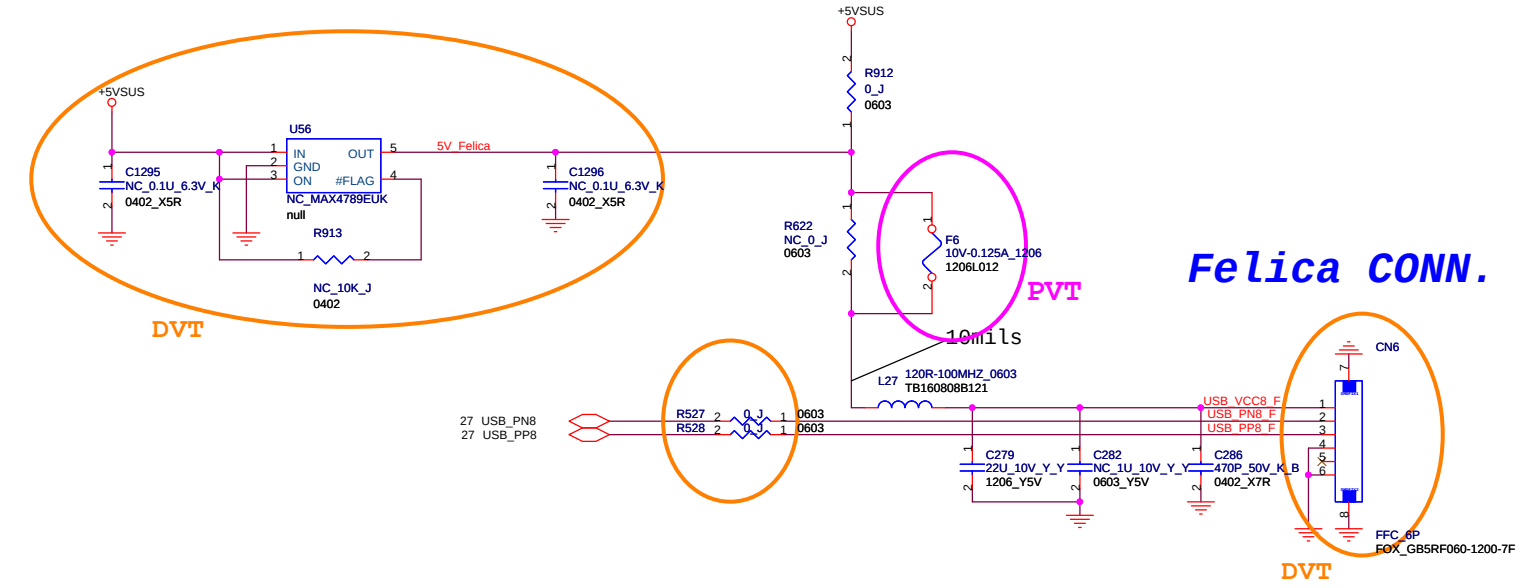


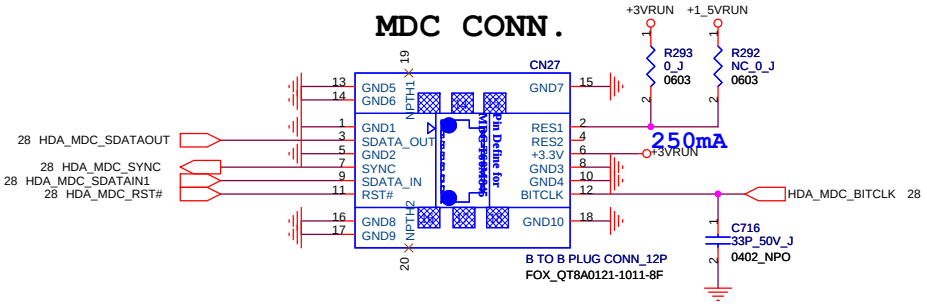
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (PCI BUS)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 44 of 69	

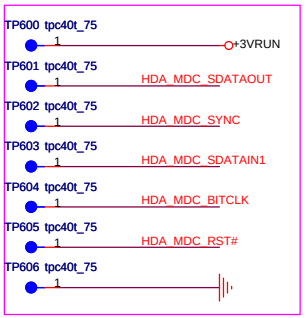

MS POWER
SD POWER
MP
iLink CONN.
AS CLOSE AS POSSIBLE TO R5C833
EVT
EVT
MS STD/DUO CONN.
SD CONN.
IEEE1394/SD
R5C833-TQFP128Q
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
PCI (ILINK&MS&SD)
Document Number M850-1-01
Rev 1.0
Thursday, April 09, 2009
Sheet 45 of 69

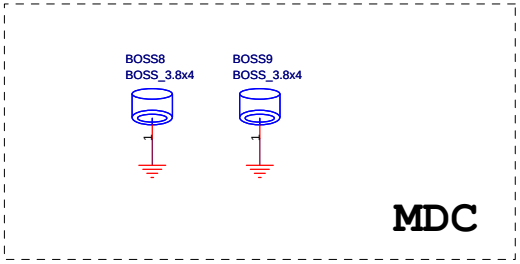


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CAMERA/Int MIC.	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 46 of 69	

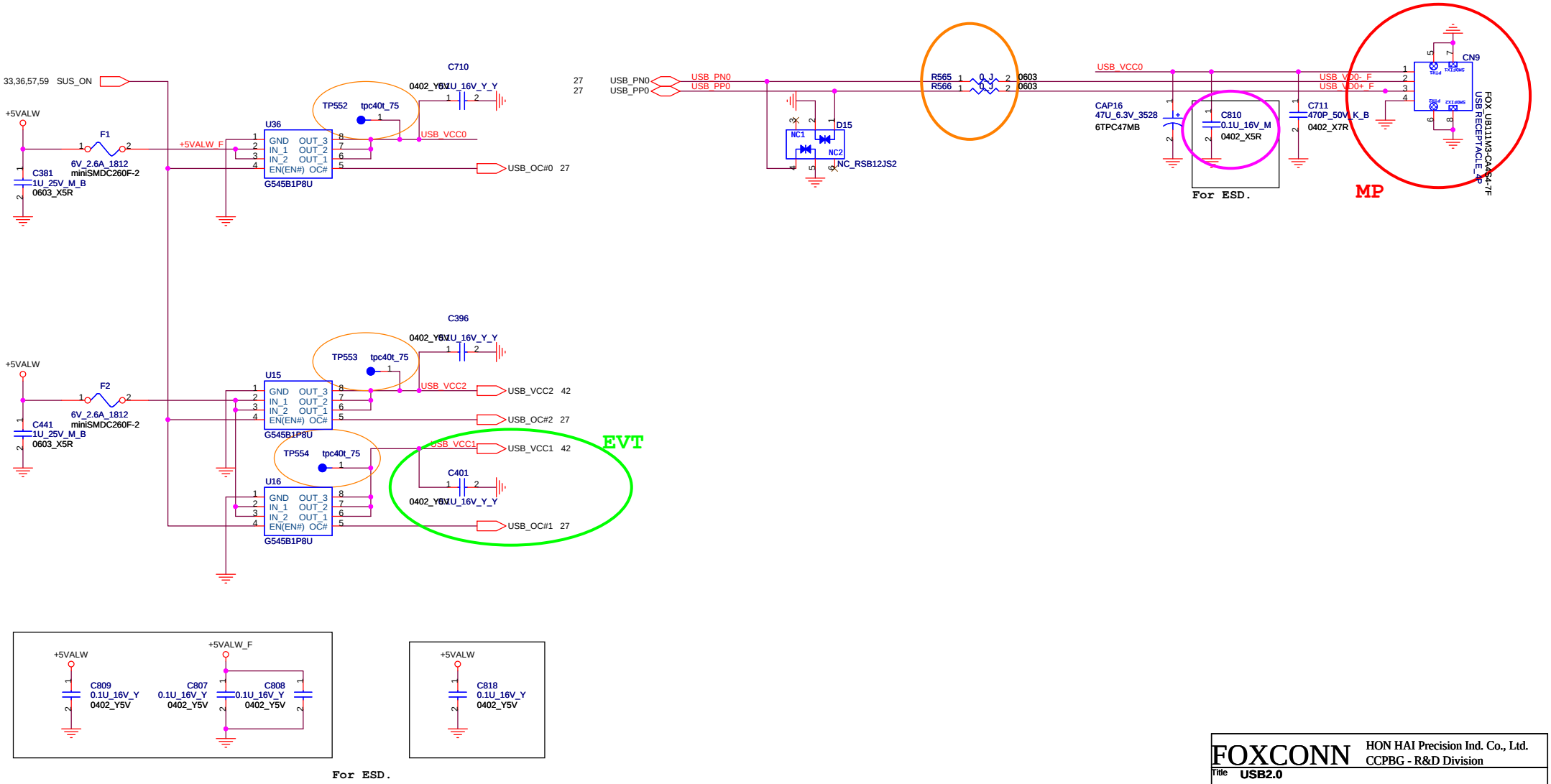






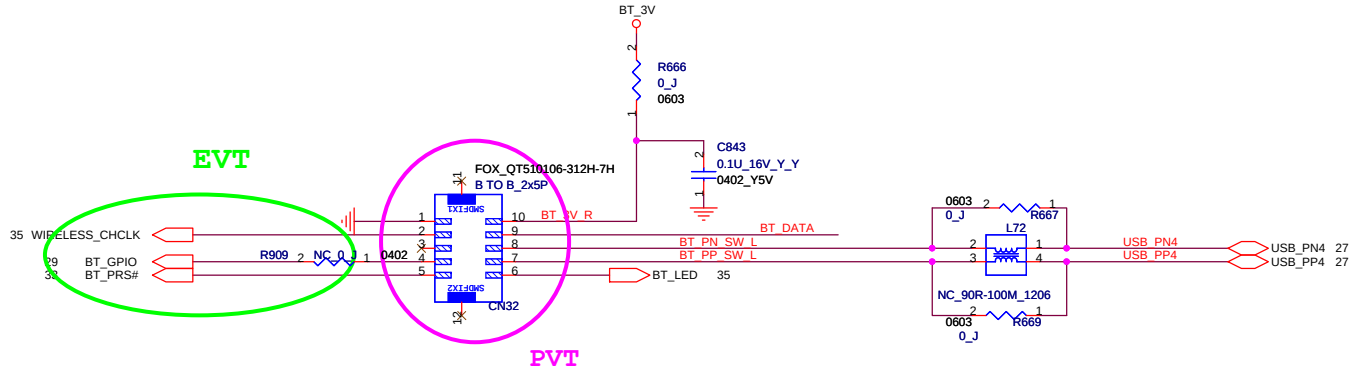


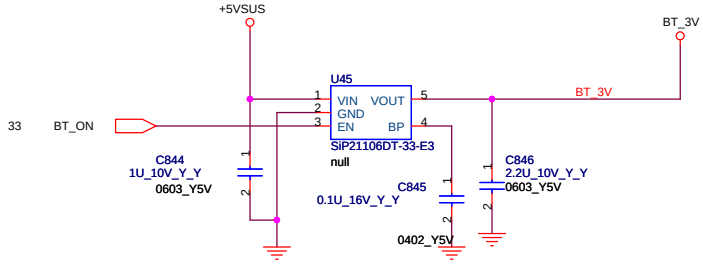
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Felica & Modem	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 47 of 69	

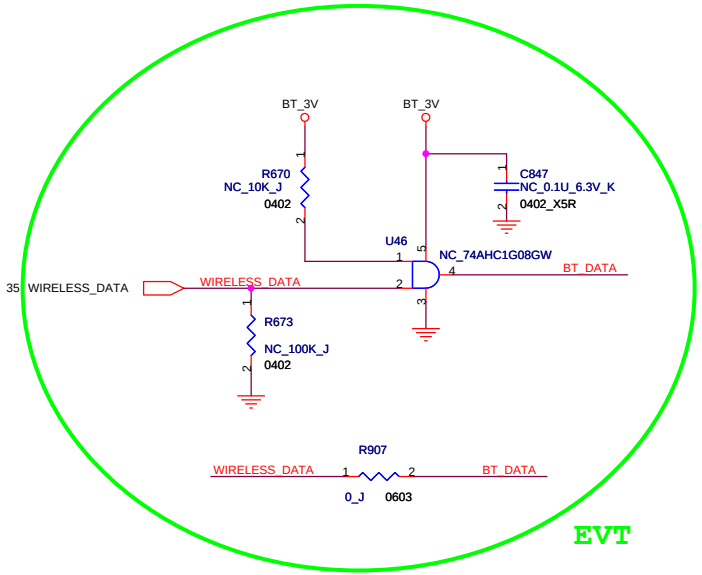


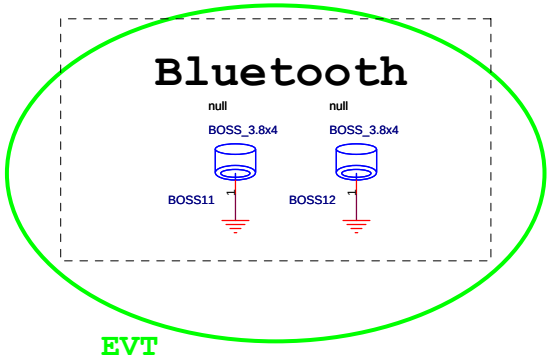
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB2.0	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 08, 2009	Sheet 48 of 69	

Bluetooth connector

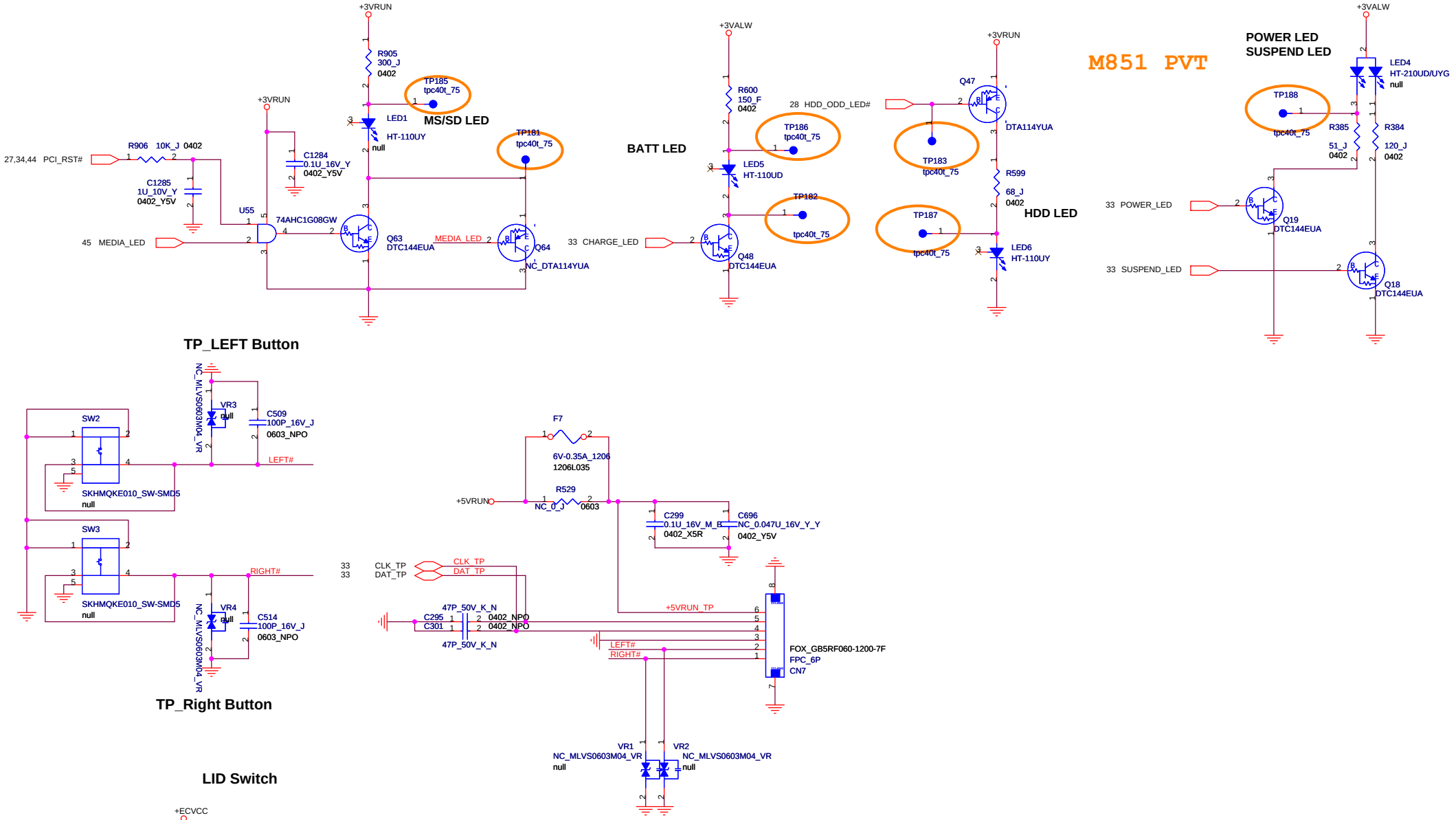




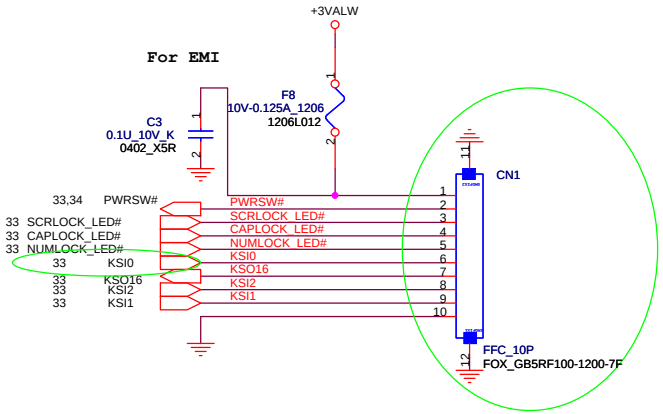


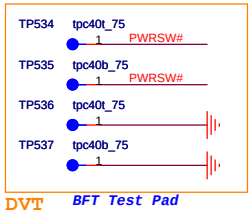


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Bluetooth		
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Wednesday, April 01, 2009	Sheet 49 of 69	



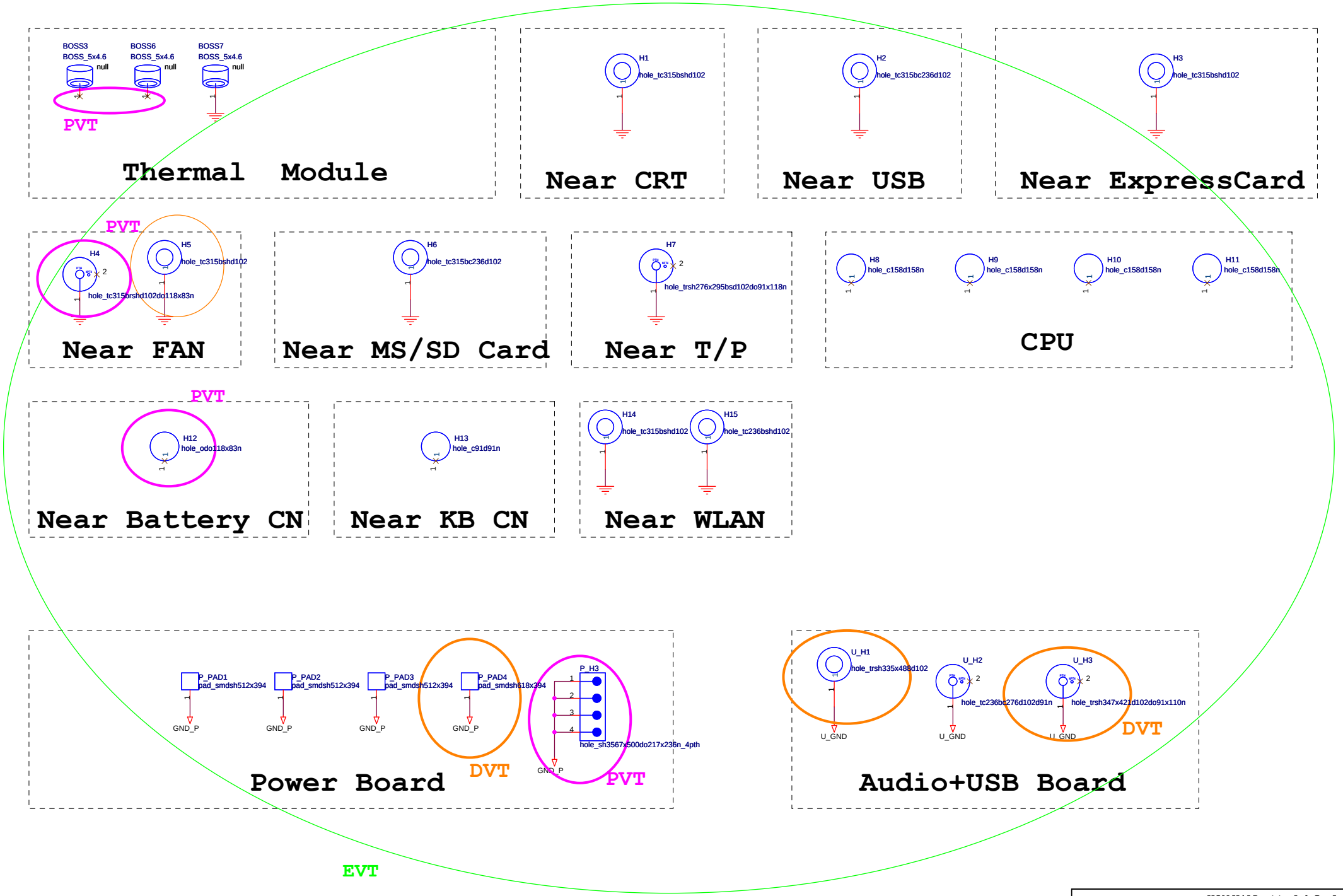
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED & T/P & LID	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 50 of 69	



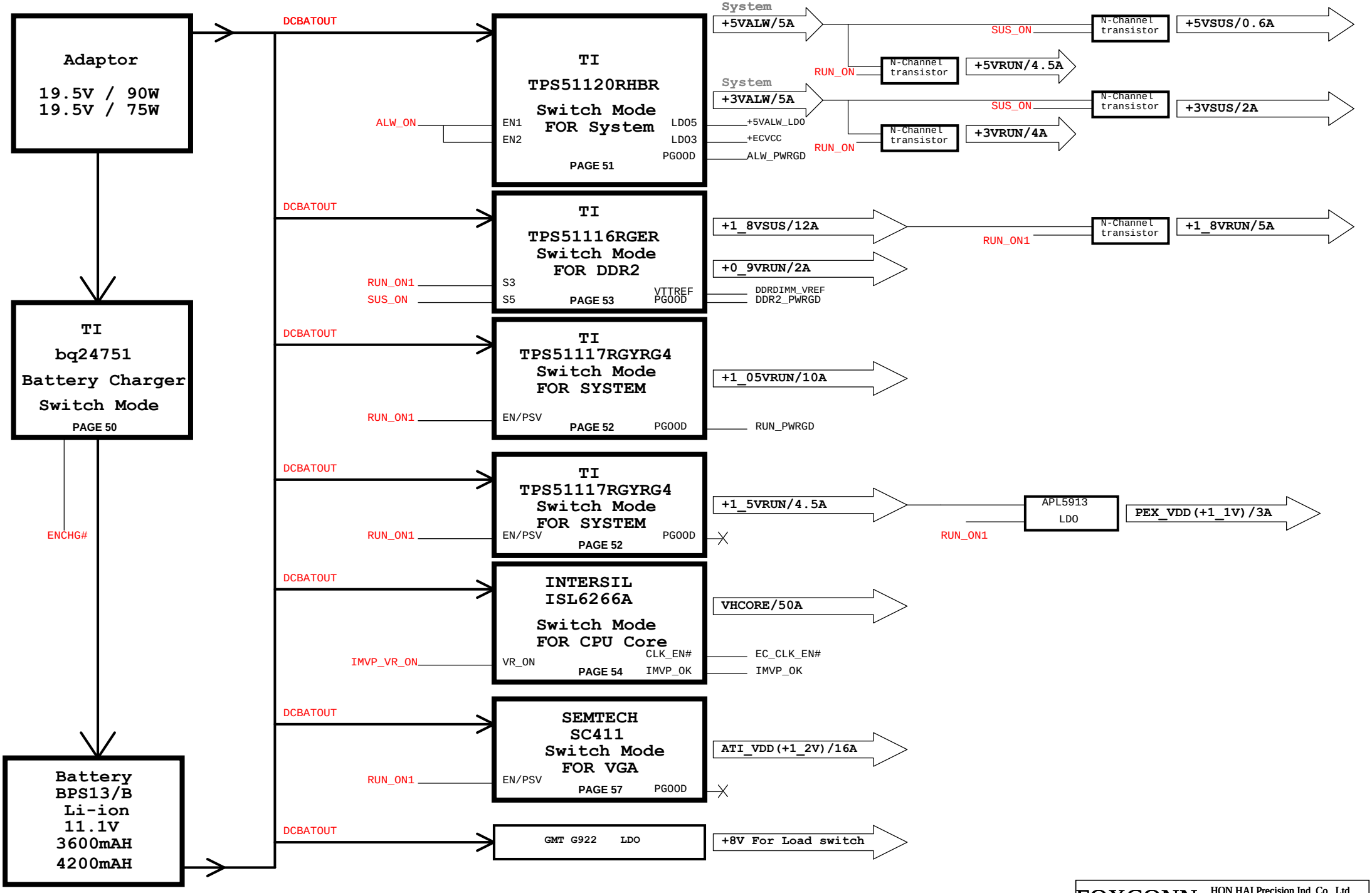


DVT *BFT Test Pad*

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Power Board MB CONN**	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 51 of 69	

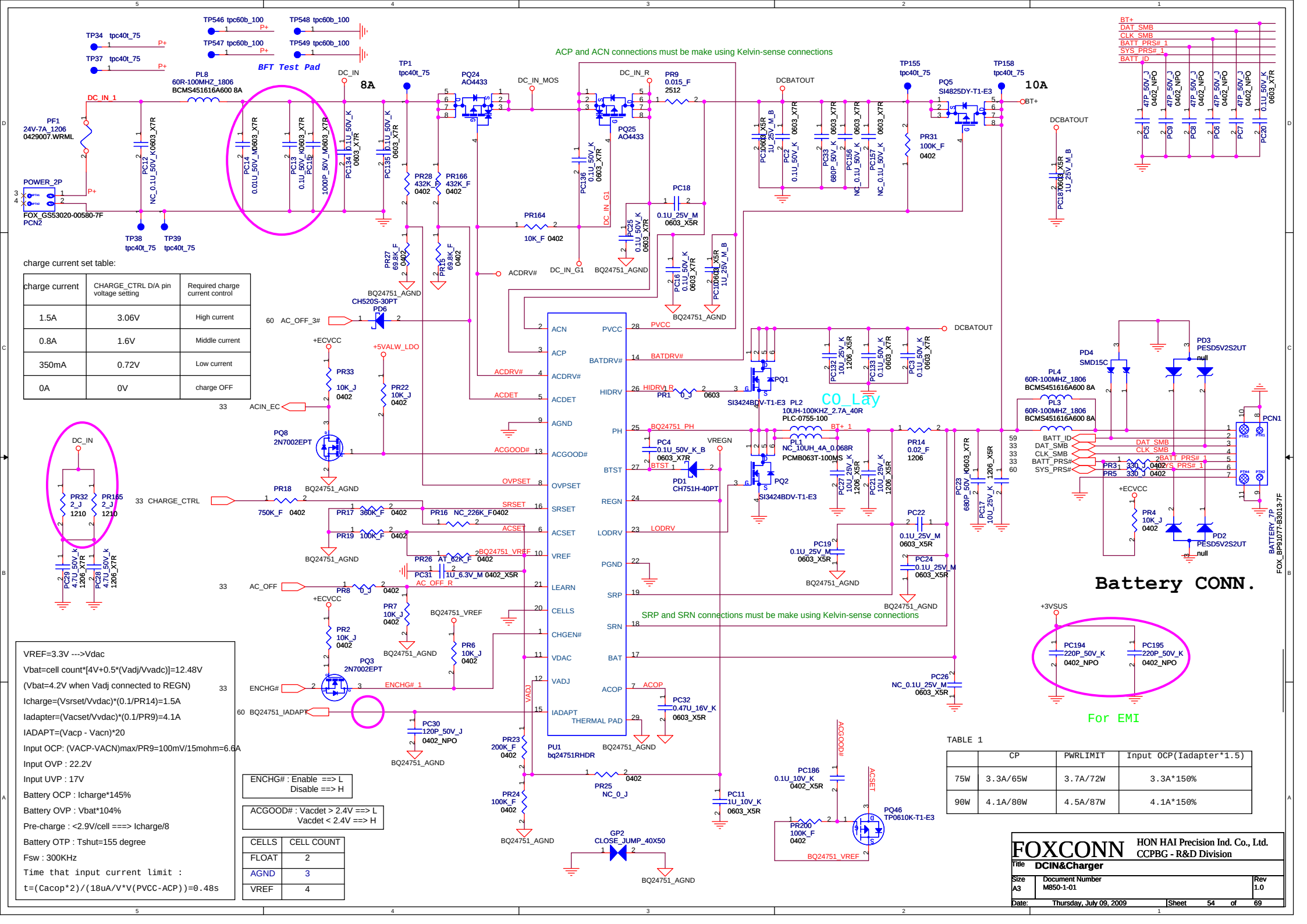


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, February 26, 2009	Sheet 52 of 69	



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Power Design Diagram	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, February 26, 2009	Sheet 53 of 69	


ACP and CN connections must be make using Kelvin-sense connections
BFT Test Pad
8A
10A
CO_Lay
Battery CONN.
SRP and SRN connections must be make using Kelvin-sense connections
For EMI
charge current set table:
charge current | CHARGE_CTRL D/A pin voltage setting | Required charge current control
1.5A | 3.06V | High current
0.8A | 1.6V | Middle current
350mA | 0.72V | Low current
0A | 0V | charge OFF
VREF=3.3V ---->Vdac
Vbat=cell count*[4V+0.5*(Vadj/Vvadc)]=12.48V
(Vbat=4.2V when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR14)=1.5A
Iadapter=(Vacset/Vvdac)*(0.1/PR9)=4.1A
IADAPT=(Vacp - Vacn)*20
Input OCP: (VACP-VACN)max/PR9=100mV/15mohm=6.6A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz
Time that input current limit :
t=(Cacop*2)/(18uA/V*V(PVCC-ACP))=0.48s
ENCHG# : Enable ==> L
Disable ==> H
ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H
CELLS | CELL COUNT
FLOAT | 2
AGND | 3
VREF | 4
TABLE 1
 | CP | PWRLIMIT | Input OCP(Iadapter*1.5)
75W | 3.3A/65W | 3.7A/72W | 3.3A*150%
90W | 4.1A/80W | 4.5A/87W | 4.1A*150%
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title DCIN&Charger
Size A3
Document Number M850-1-01
Rev 1.0
Date: Thursday, July 09, 2009
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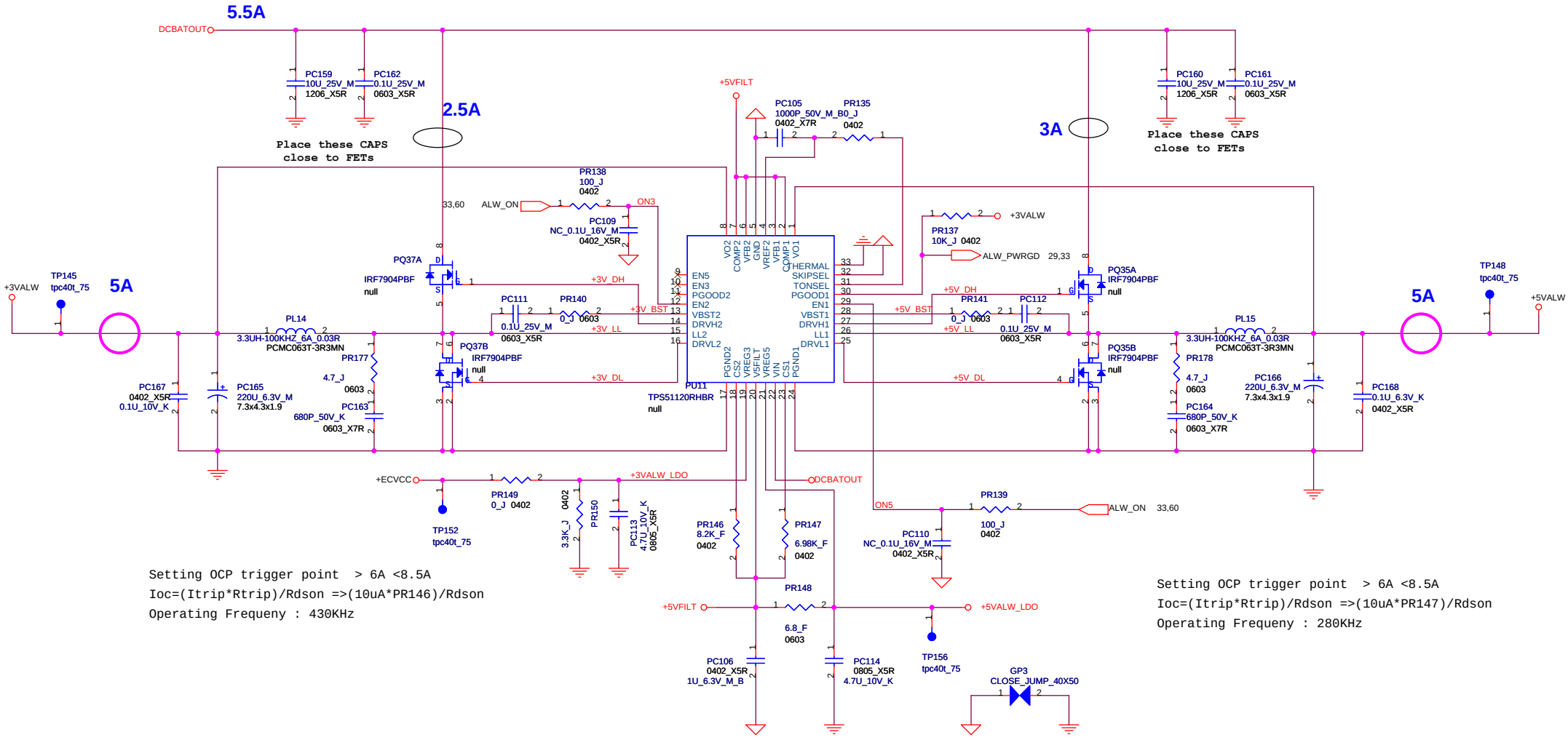
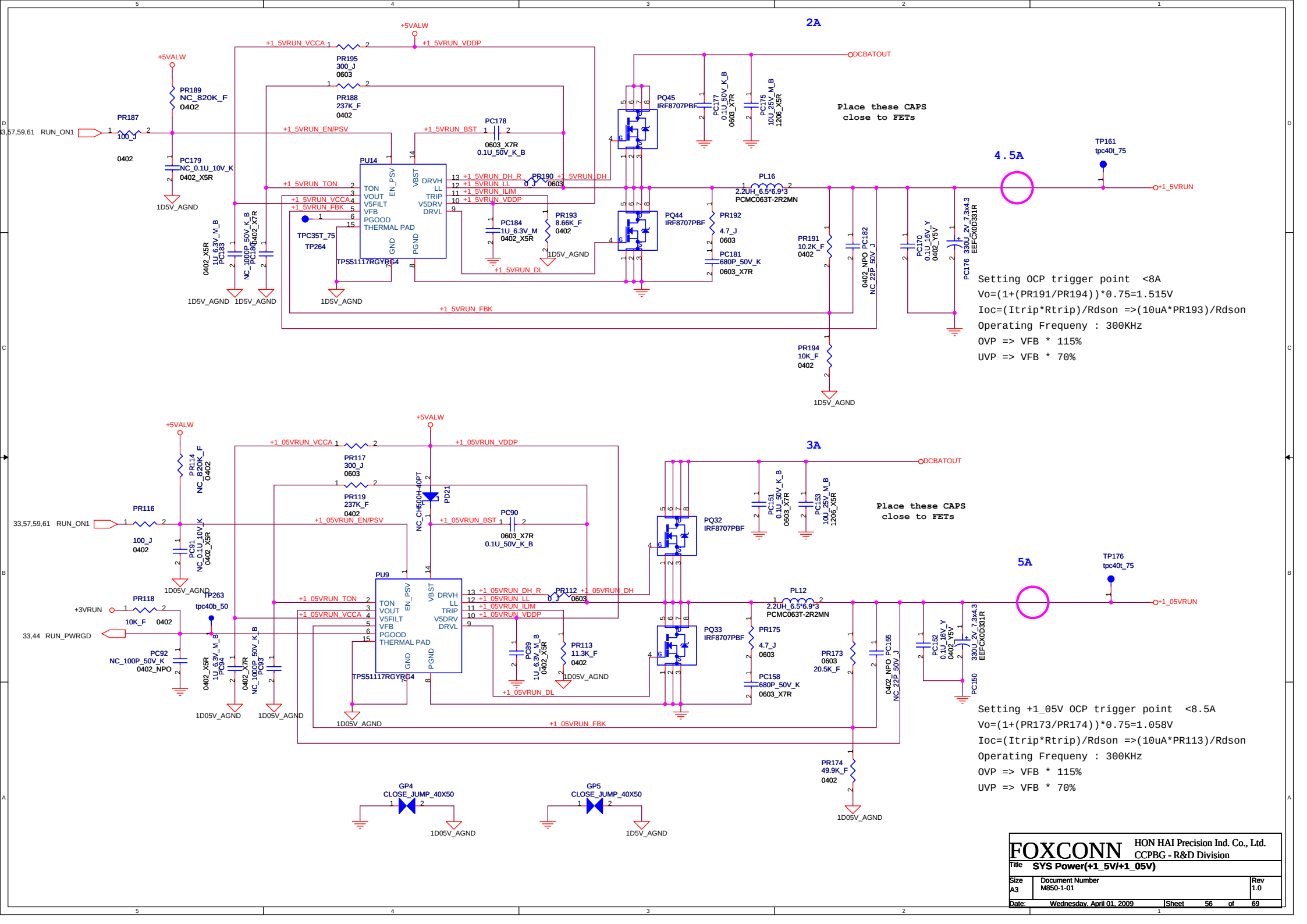


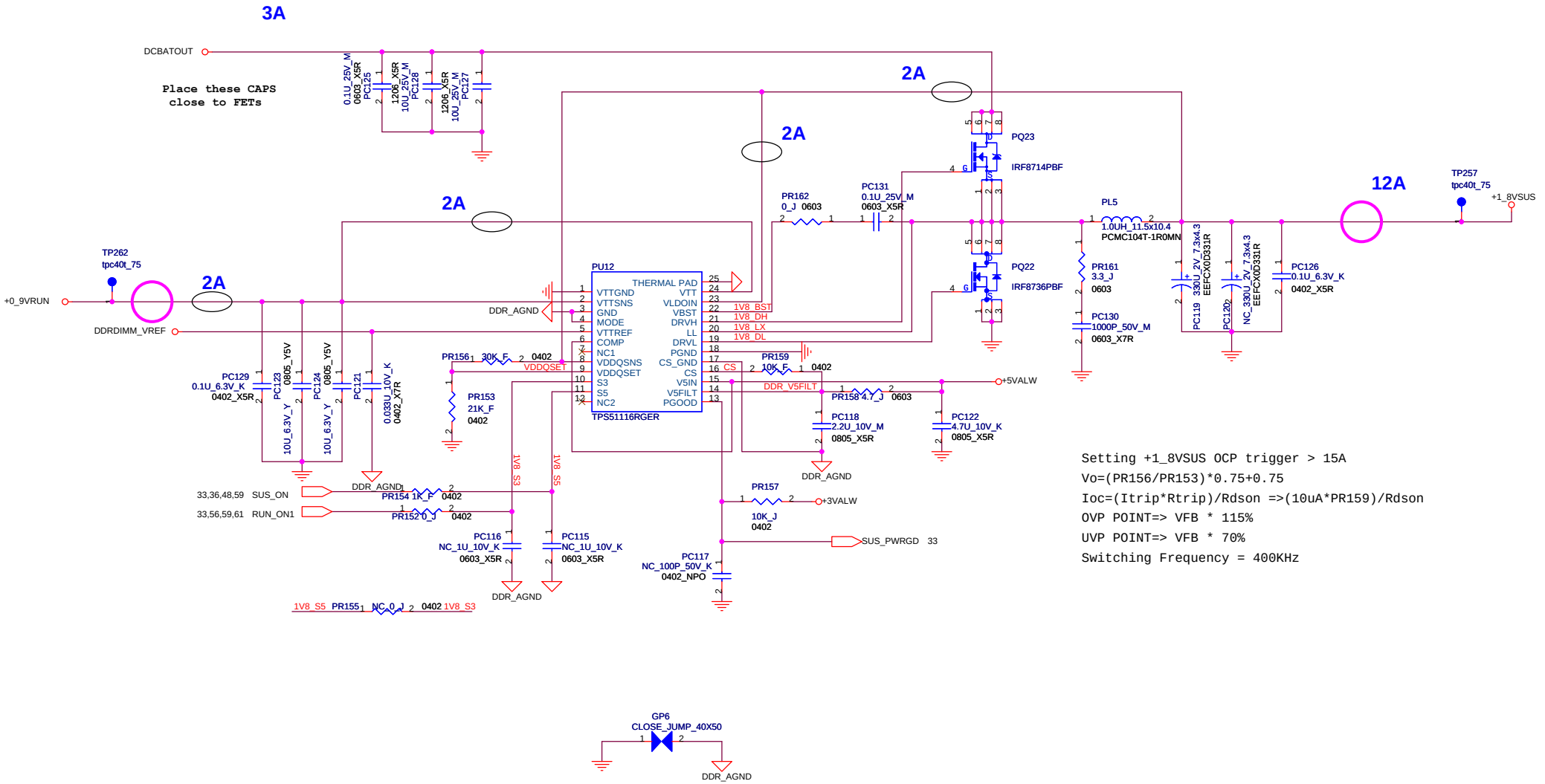
Setting OCP trigger point > 6A <8.5A
Ioc=(Itrip*Rtrip)/Rdson =>(10uA*PR146)/Rdson
Operating Frequeny : 430KHz

Setting OCP trigger point > 6A <8.5A
Ioc=(Itrip*Rtrip)/Rdson =>(10uA*PR147)/Rdson
Operating Frequeny : 280KHz

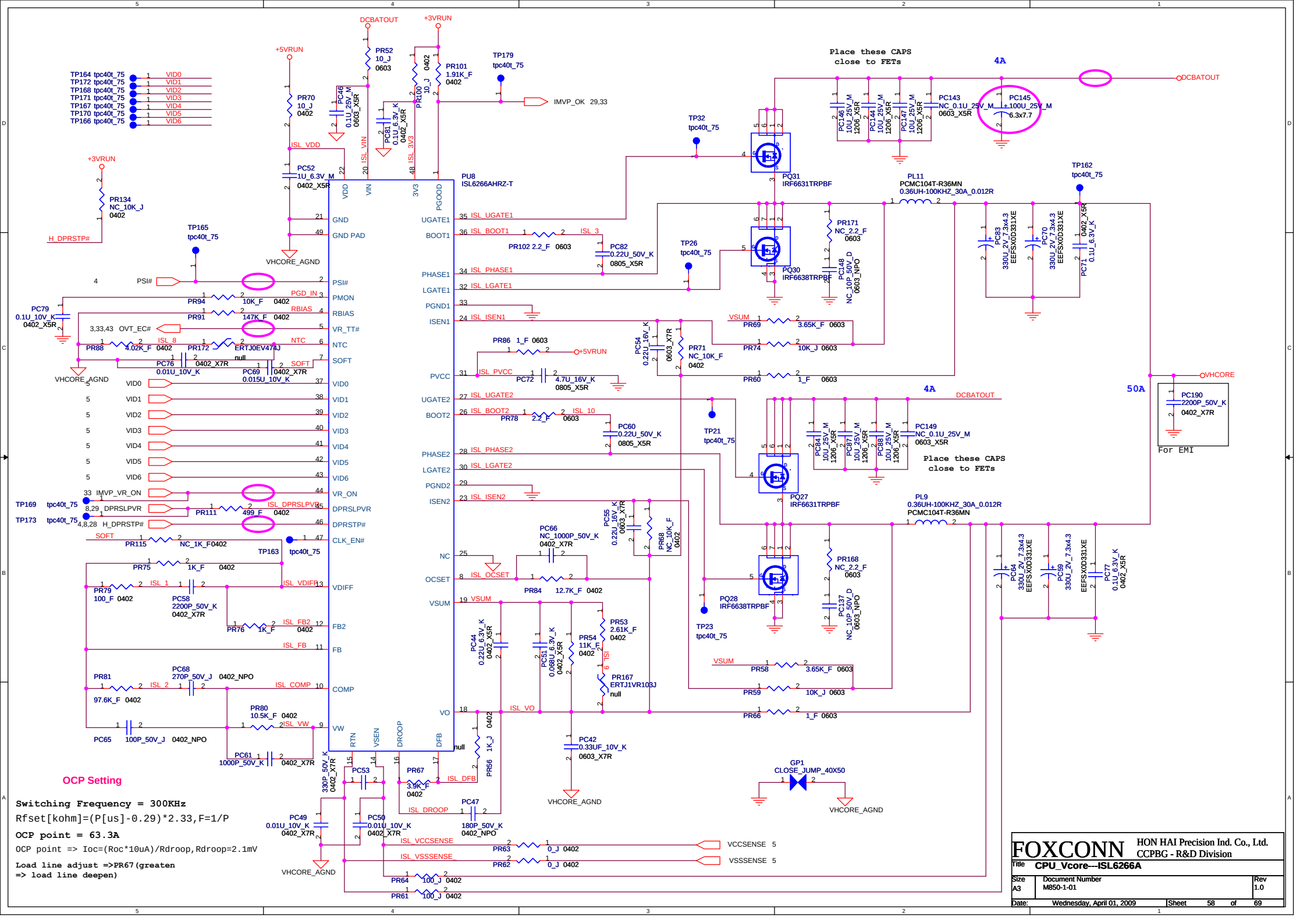
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power (+3_3V/+5V)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 55 of 69	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_5V/+1_05V)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 56 of 69	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR2 Power(+1_8V/+0_9V)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 57 of 69	


PU8
ISL6266AHRZ-T
Place these CAPS close to FETs
4A
50A
DCBATOUT
VHCORE
For EMI
+5VRUN
+3VRUN
VHCORE_AGND
IMVP_OK 29,33
PSI#
H_DPRSTP#
OVT_EC#
DPRSLPVR
DPRSTP#
IMVP_VR_ON
CLK_EN#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PQ31 IRF6631TRPBF
PQ30 IRF6638TRPBF
PQ27 IRF6631TRPBF
PQ28 IRF6638TRPBF
PL11 PCMC104T-R36MN 0.36UH-100KHZ_30A_0.012R
PL9 0.36UH-100KHZ_30A_0.012R PCMC104T-R36MN
GP1 CLOSE_JUMP_40X50
VCCSENSE 5
VSSSENSE 5
OCP Setting
Switching Frequency = 300KHz
Rfset[kohm]=(P[us]-0.29)*2.33,F=1/P
OCP point = 63.3A
OCP point => Ioc=(Roc*10uA)/Rdroop,Rdroop=2.1mV
Load line adjust =>PR67(greaten
=> load line deepen)
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title CPU_Vcore---ISL6266A
Size A3
Document Number M850-1-01
Rev 1.0
Date: Wednesday, April 01, 2009
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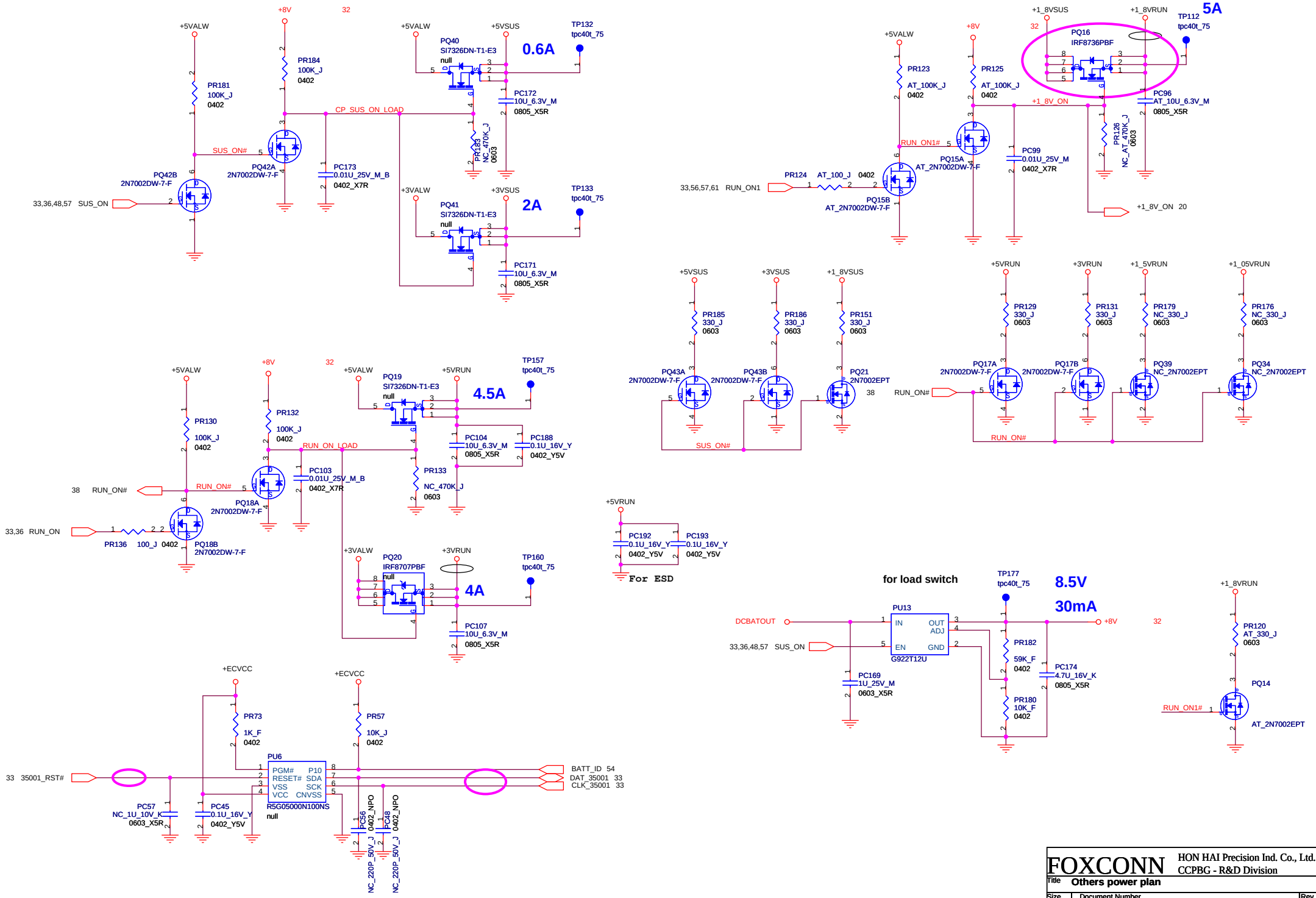
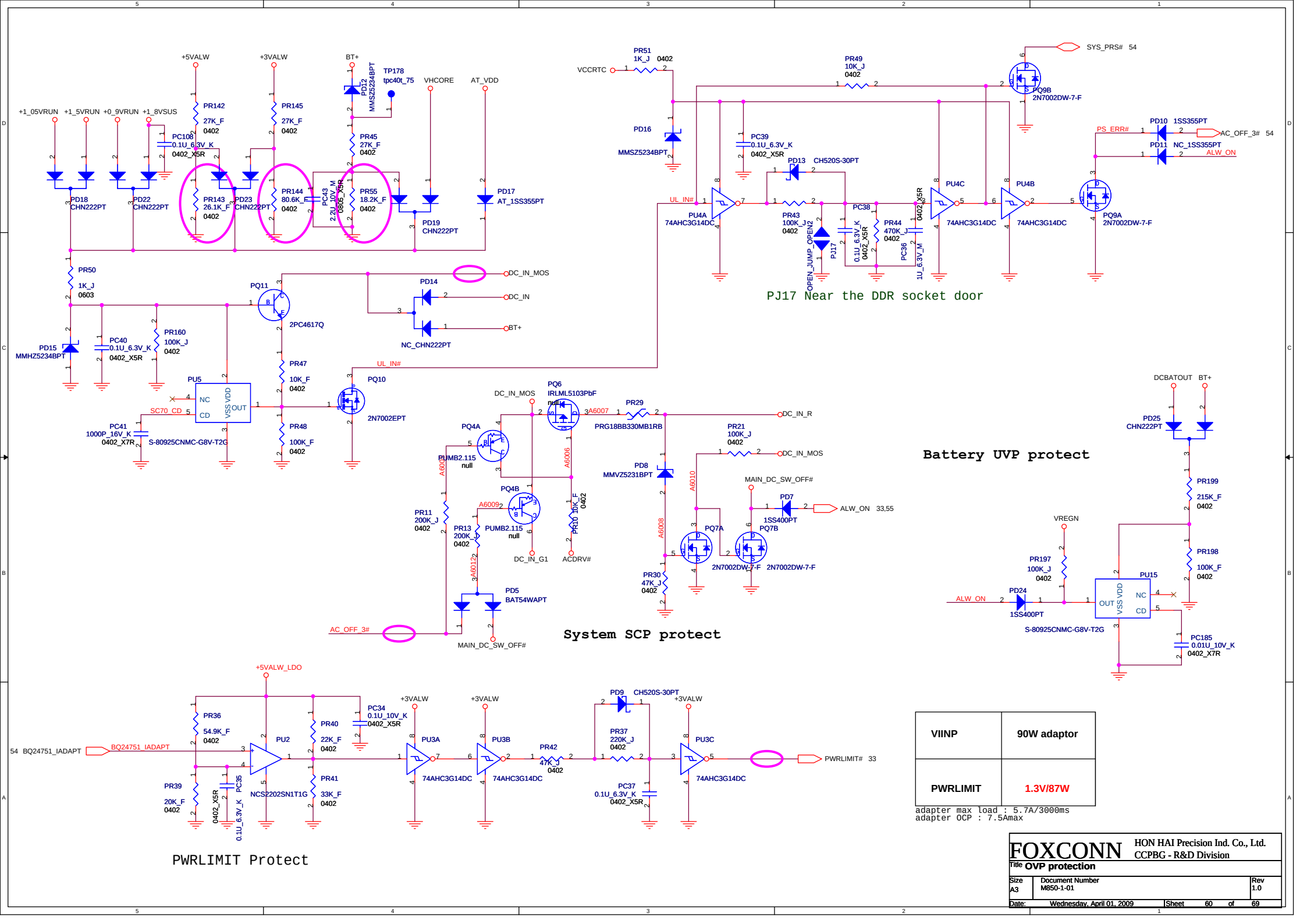


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 59 of 69	



VIINP	90W adaptor
PWRLIMIT	1.3V/87W

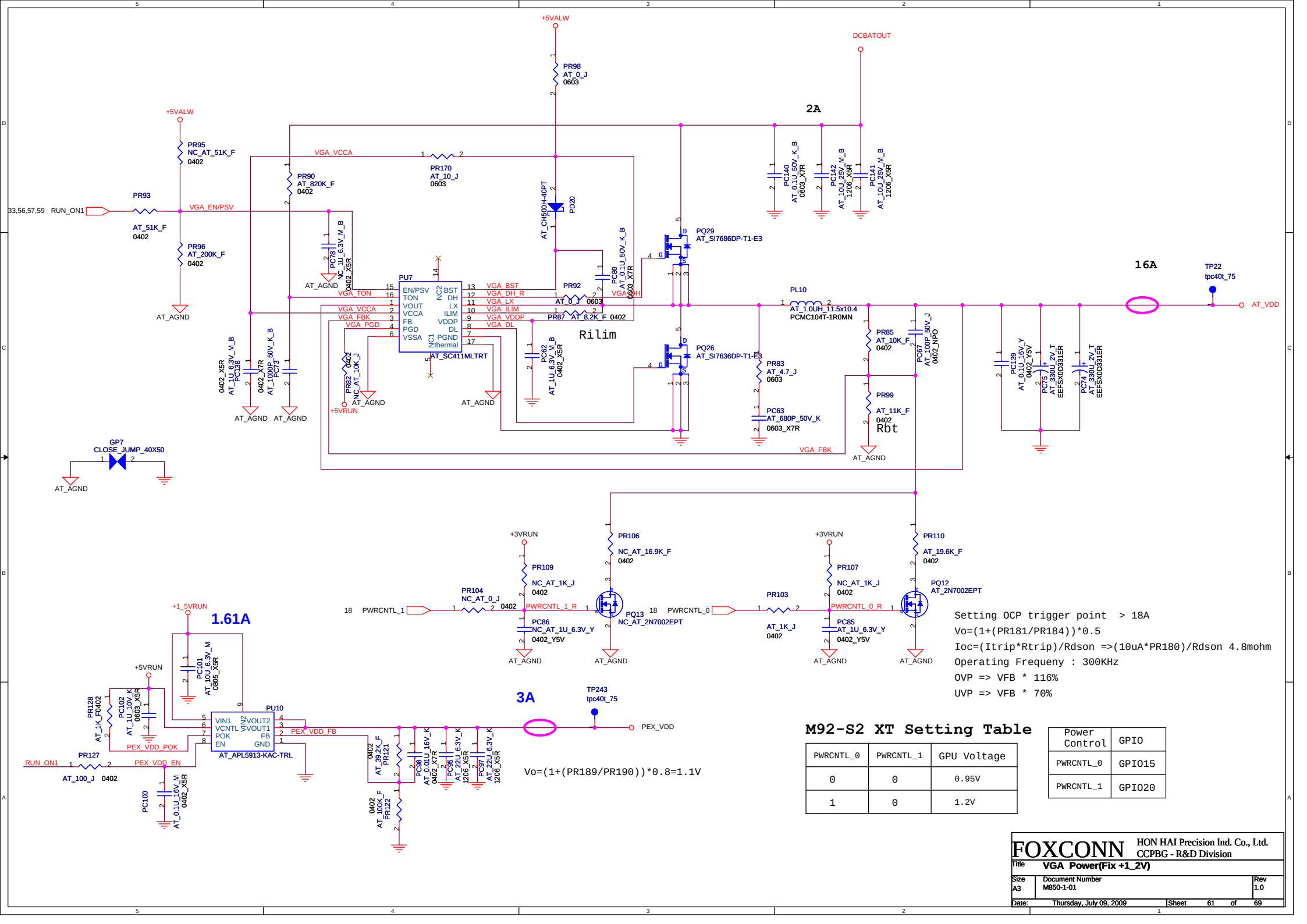
adapter max load : 5.7A/3000ms
adapter OCP : 7.5Amax

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: OVP protection

Size	Document Number	Rev
A3	M850-1-01	1.0

Date: Wednesday, April 01, 2009 Sheet 60 of 69



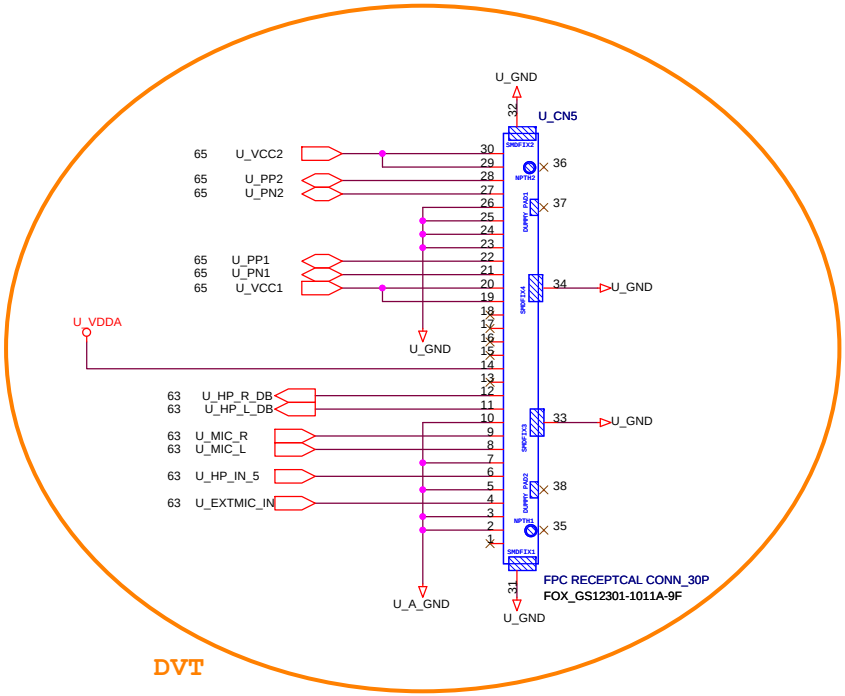
M92-S2 XT Setting Table

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.95V
1	0	1.2V

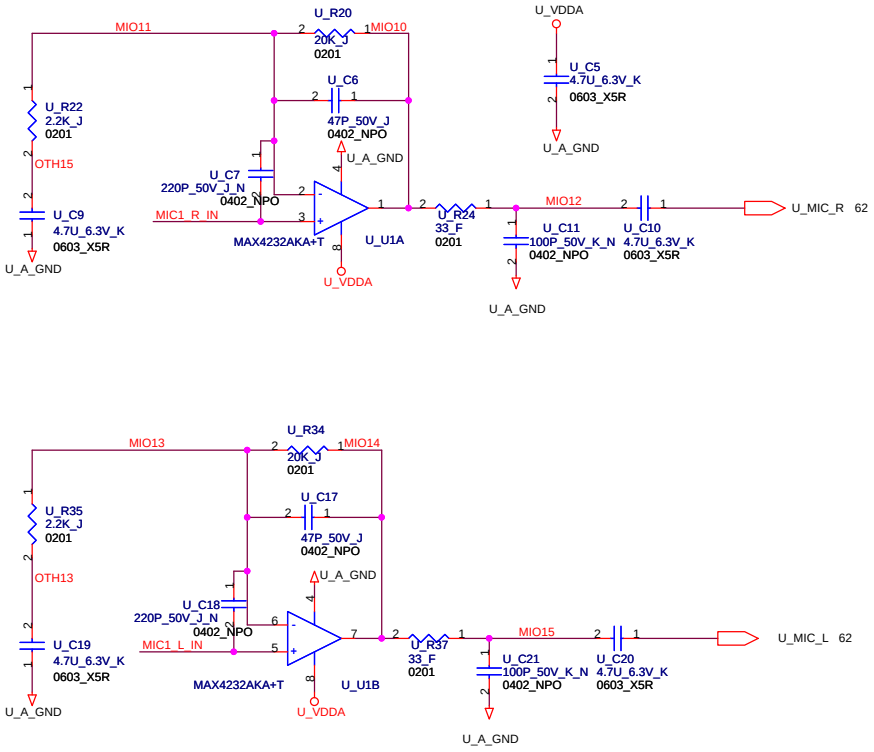
Power Control	GPIO
PWRCNTL_0	GPIO15
PWRCNTL_1	GPIO20

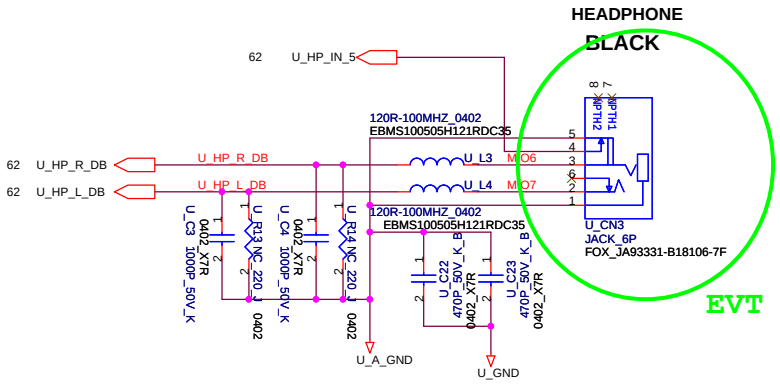
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

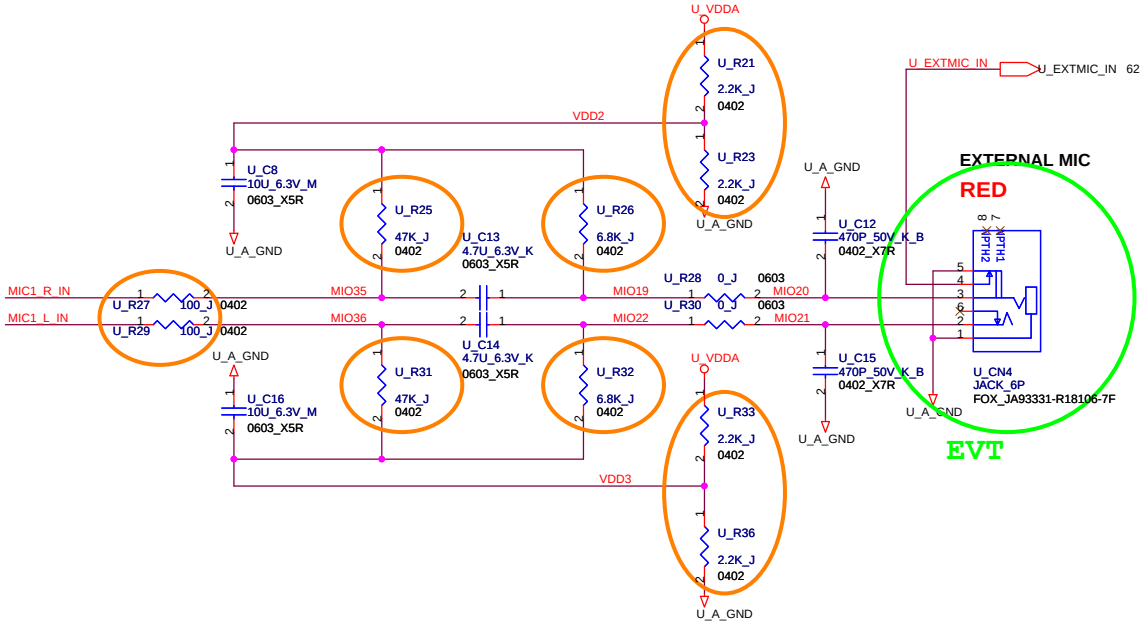
Title	VGA Power(Fix +1_2V)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 61 of 69	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***Audio+USB DB CONN***	
Size A3	Document Number ***M850-1-01***	Rev ***1.0***
Date: Wednesday, April 01, 2009	Sheet 62 of 69	



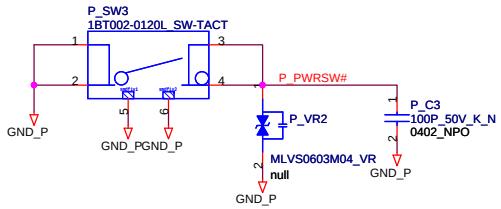


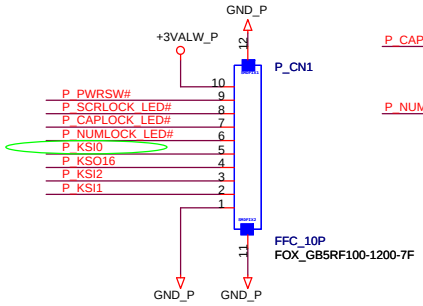


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (HP, MIC Jack)	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 01, 2009	Sheet 63 of 69	

Power Button Board

POWER BUTTON

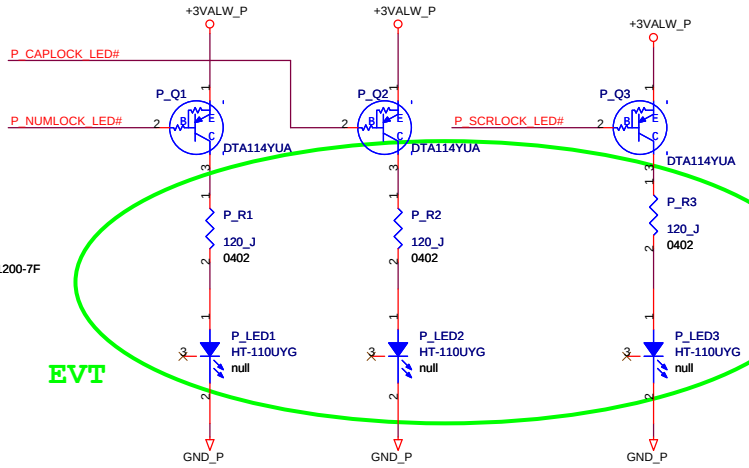




NUM LOCK LED

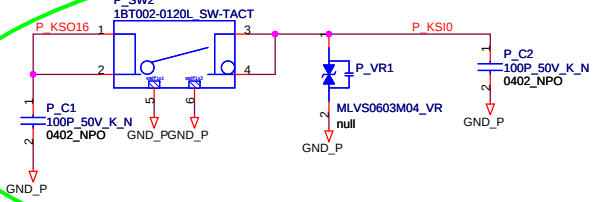
CAP LED

SCROLL LOCK LED

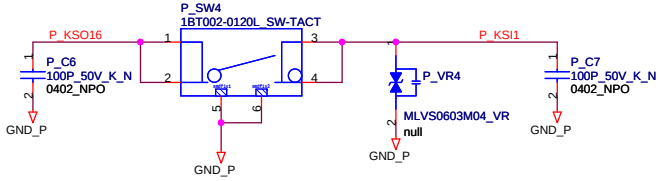


EVT

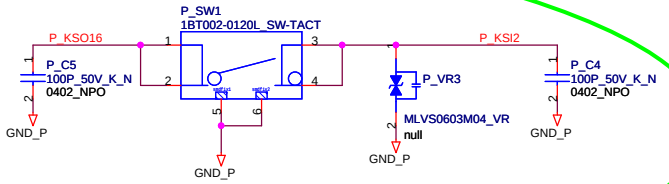
Instant ON



Mute

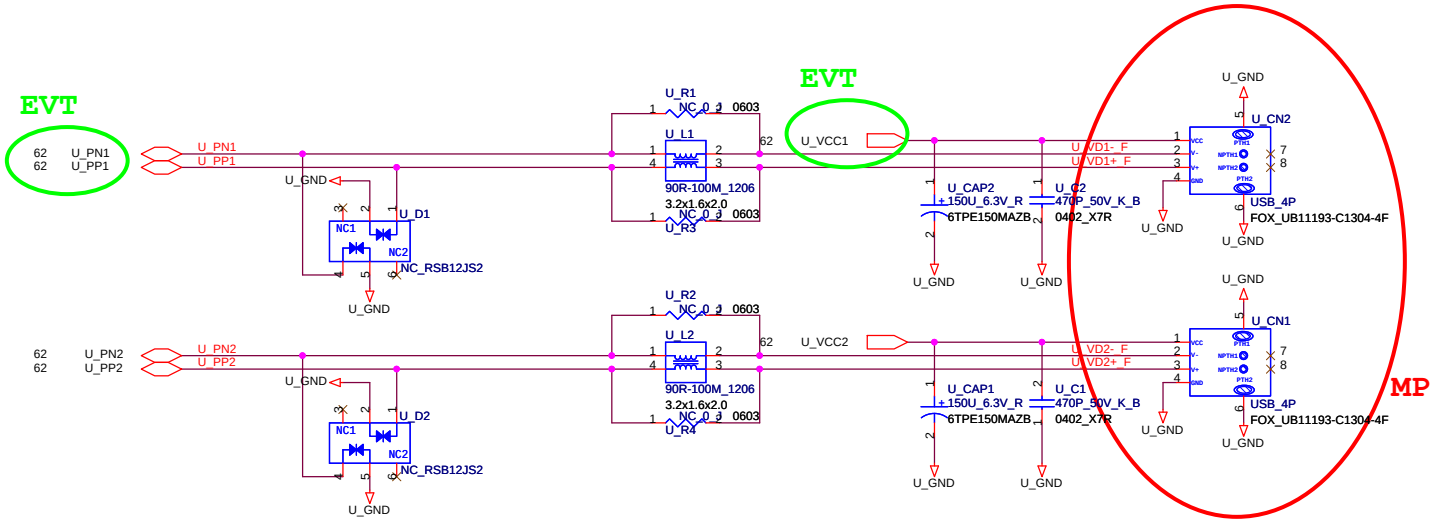


Display OFF



EVT

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Board DB & CONN	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, February 26, 2009	Sheet 64 of 69	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB DB	
Size A3	Document Number M850-1-01	Rev 1.0
Date: Wednesday, April 08, 2009	Sheet 65 of 69	

M850 EVT

(2008/08/29)

P.45 Change CN16 from WK21923-S6P-7F to WK21923-R6S-7F for ME request.
P.32 Change CN25 from LN27131-A403-4F to LN21131-F404-9F for ME request.
P.32 Change CN13 from LD2722F-SR6L to LD2722H-S49L for ME request.
P.25 Change CN18 from HT1310F to GS12201-1011-9F for ME request.
P.46 Change CN17 from HS6106E to HS6206E for ME request.
P.37 Change CN22 from HS6108E to HS8208E for ME request.
P.33 Change CN3 from GB21240-0002-7F to 196009-24021 for ME request.
P.49 Change CN32 from QT510106-111H-7F to QT510106-311H-7F for ME request.
P.35 Change SW4 from 1BS007-12120-002-7F to 1BS007-12110-002-7F for ME request.
P.39 Change U_CN4 from JA9333L-R5S7-7F to JA93331-R18106-7F for ME request.
P.39 Change U_CN3 from JA9333L-B5S7-7F to JA93331-B18106-7F for ME request.
P.51 Change U_CN1 and U_CN2 from UB11193-C1314-4F to UB11193-C1308-4F for ME request.
P.52 Add BOSS11 and BOSS12 for ME request.

(2008/08/29)

P.45 Change CN11 form UV31413-GR56P-7F to UV31413-WZ03P-7F for ME request.
P.24 Change CN2 from DZ11A91-MA2SY-4F to DZ11A91-SB281-4F for ME request.
P.26 Change CN31 from QJ5119L-NT03-4F to QJ5119L-NK03-4F for ME request.
P.48 Change CN9 from UB11193-C1314-4F to UB1112C-CA501-7F for ME request.

(2008/09/01)

P.55 Change PR146 from 6.98K_F to 8.2K_F for OCP setting.
P.55 Change PR147 from 6.19K_F to 6.98K_F for OCP setting.
P.56 Change PR193 from 5.49K_F to 8.66K_F for OCP setting.
P.56 Change PR113 from 8.66K_F to 11.3K_F for OCP setting.
P.61 Change PR87 from 6.8K_F to 8.2K_F for OCP setting.
P.61 Change PR99 from 8.2K_F to 6.98K_F for AT_VDD voltage setting to 1.2V.

(2008/09/02)

P.25 Change CN18 from GS12201-1011-9F to GS12301-1011A-9F for support Dual-LVDS.
P.25 Add RP51,RP52,RP53 and RP54 for support Dual-LVDS.

(2008/09/19)

P.35 Delete R611&R612 for MOR's requested
P.35 Add D22 for MOR's requested
P.27,42,48,51 Change external USB port from USBP3N/USBP3P to USBP1N/USBP1P for MOR's requested
P.27,35,36 Change PCIE port from Express Card #2, WLAN #3 to WLAN #2, Express Card #3 for MOR's requested
P.54 Change PCN1 from BP91077-B2013-7F to BP91077-B3013-7F for ME's requested
P.37 Change U4 from 88E8055 to 88E8057 for MOR's requested
P.49 Delete R668,674,672,671 for MOR's requested
P.35 Change C538,C544,C536 to NC for MOR's requested

(2008/09/22)

P.45 Change CN11 from UV31413-WZ03P-7F to UV31413-RU81P-7F for ME's requested

(2008/09/24)

P.48 Change CN9 from UB1112C-CA501-7F to UB1112C-CA207-7F for ME's requested

(2008/09/26)

P.65 [Power board DB button] Add P_SW4,P_C6,P_C7,P_VR4 for add mute button
P.25 [Inverter CONN] Change CN19 from HS6106E to HS6108E for support LED backlight function
P.25 [Panel ID Switch] Change SW1 from HDS404-E to FHDS-04-T-V-T/R for shortage issue

(2008/10/02)

P.36 [ExpressCard] Add R901,R902,R903,R904 for test GMT577 ExpressCard power switch
P.37 [GLAN]Change L5 from NS682403P to LFE9249-R for PUR's suggestion
P.26 [HDMI] Change CN31 from QJ5119L-NK03-4F to QJ5119L-NT03-4F for ME's ID concern
P.52 [Thermal Module Nut] Change BOSS3,BOSS6,BOSS7 form F50M20-501130BS to EMI_F50M20_351130BS for ME's concern
P.21,22 [VRAM] Change U49,U50,U51,U52 from K4J10324QD-HC14 to K4J10324QD-HC12 for support 800MHz
P.50 [TouchPad] Change CN7 from GB5RF120-1200-7F to GB5RF060-1200-7F for change to 6-pin solution
P.60 [OVP protection]Delete PR35 CA_69.8K_F for 8L version unnecessary resister.
P.50 [MS/SD LED] Combine MS/SD LED for MOR's requested
P.65 [Caps/Num/Scroll lock LED] Change from HT-150YG to HT-110UYG for ME's ID concern
P.14 [DDR2] Swap RP13,RP10 pin assignment for layout convenient
P.15 [DDR2] Swap RP33,RP34,RP32,RP28,RP29 pin assignment for layout convenient
P.25 [LVDS] Change L98 from EBMS160808A121(400mA) to HCB1608KF-121T10(1A) for Panel max current is 500mA

(2008/10/06)

P.27 [ICH9] Swap RP46,RP24,RP16 pin assignment for layout convenient
P.50 [TP] Reserved 12pin TP solution in EVT

(2008/10/07)

P.49 [BT]NC U46,R673,R670,C847 and add R907 for BT module has internal protection schematics for BT_DATA pin.
P.35 [WLAN]Change Q49 from FET to transistor for a little cost down.
P.54 [DCIN&Charger]Delete PR34 for 8L version unnecessary resister.
P.52 [HOLE]Update HOLE for ME's requested.
P.11 [Cantiga] Delete R121,R151 for 8L version unnecessary resister.

(2008/10/08)

P.11 [Cantiga]Delete C202,C225 for VCCD_TVDAC can be connected to GND form Intel DG mention.
P.18 [VGA]REFCLK jumper R849.2pin should be connected to R848.1pin side not R848.2pin side. In case if you use REFCLK, It's voltage should be deviced also.
P.18 [VGA]Delete R840,R841,R843 and connect R2B,G2B,B2B to GND directly.
P.24 [CRT]Change DDC 3V pull-up R57,R58 from 2.2k to 3.9k to meet E-DDC spec.
P.25 [LVDS]Add R908 for AT_LCDVCC_EN need 10k pull-down as AMD Check list 8-1 mention.
P.26 [HDMI]Delete R649 for HDMI DDC need back drive protection so cannot use R649.
P.26 [HDMI]Delete D21 and R652 for if using diode, HDMI_+5VRUN voltage cannot meet spec. And HDMI_+5VRUN need back drive protection.
P.25 [LVDS]Change R393 from 10k to 100k to meet desing guide.

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(2008/10/09)

P.21 [VRAM]Change R770,R771 from 82.5ohm to 120ohm for AMD suggestion
P.33,51,64 [Button]Delte KSO15 and add KSI0 control signal for SW request
P.49 [BT]Add R909(NC) for new BT module reserved
P.11 [Cantiga]Delete R116 for useless
P.33 [EC]Change R477,R437 to mount and R479,R436 to NC for H model ID change to "10"
P.25 [LVDS]Change back R393 from 100k to 10k to meet AMD check list 8-8.

(2008/10/10)

P.62 [Audio+USB CONN]Swap pin assignment for cable routing smooth.
P.03 [Penryn]Add C1287(NC) for EMI verification.
P.33 [EC]Add R910~R933 for EMI verification.
P.51 [Power Board CONN]Add C1288~C1295(NC) for EMI verification.
P.17 [VGA]Delete R817,R818 for GPIO9 is VGA_DIS strap.

(2008/10/11)

P.52 [HOLE]Update all holes for ME's requested

(2008/10/13)

P.33 [EC]Delete R910~R933 for layout space not enough
P.51 [Power Board CONN]Delete C1288~C1295 for layout space not enough.
P.48 [USB]Change CN9 from UB1112C-CA207-7F to UB11123-CA301-7F
for ME's concerned.
P.54 [DCIN&Charger]Add PC194,PC195(NC) for EMI verification

(2008/10/14)

P.52 [HOLE]Delete H16,H17,H18 for ME's requested.
P.17 [VGA]Add R910,R911 for AMD confirm pin DVPDATA_22 and DVPDATA_23 function
P.29 [ICH9]Delete R301 for needless
P.48 [USB]Change CN9 from UB11123-CA301-7F to UB111M3-CA4S4-7F for ME's requested

(2008/10/15)

P.16 [VGA]Change R849 from 0ohm to 100ohm and Net for R861.1&R860.1
changed to R_AT_XTALIN for MOR's comment
P.42 [Audio]Add C1288(NC) for EMI verification

(2008/10/16)

P.50 [T/P]Reverse CONN for ME's requested

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(2008/11/13)

P.40 [Audio]Reverse JSPK1 pin definiens for ME's cable routing concern
P.62 [Audio+USB DB]Reverse U_CN5 pin definiens for ME's cable routing concern
P.47 [Felica]Reverse CN6 pin definiens for ME's cable routing concern
P.50 [T/P]Reverse CN7 pin definiens for ME's cable routing concern
P.18 [VGA]Connect U53.T11&R11 to GND for ATI updated
P.17 [VGA]Change R815,R814 to NC and R910 to mount for
ATI DVPDATA[23,22] failure issue

(2008/11/15)

P.50 [T/P]Delete CN34,R530,R531 for cancel 12pin T/P solution

(2008/11/17)

P.26 [HDMI]Change CN31 from QJ5119L-NT03-4F to QJ1119L-NT03-4F(Dip type)
for CONN issue

(2008/11/19)

P.26 [HDMI]Swap RP47 and RP49 for layout convenient
P.52 [HOLE]Change U_H3 size for ME's requested
P.52 [HOLE]Delete P_PAD5 and add P_H3 for ME's requested
P.52 [HOLE]Change P_PAD4 size for ME's requested
P.52 [HOLE]Delete P_H1 and P_H2 for ME's requested

(2008/11/24)

P.55 [SYS Power (+3_3V/+5V)] Add test point TP152, TP156
P.56 [SYS Power(+1_5V/+1_05V))] Add test point TP161, TP176
P.58 [CPU_Vcore---ISL6266A] Add test point TP179
P.59 [Others power plane] Add test point TP132, TP133, TP157, TP160, TP177
P.60 [OVP protection] Add test point TP178

(2008/12/01)

P.54 [DCIN&Charger] Add test point TP34, TP37, TP38, TP39
P.54 [DCIN&Charger] Change PQ5 from AO4433 to SI4825DY-T1-E3 for EMI Issue
P.58 [CPU_Vcore---ISL6266A] Add PJ11 for power test

(2008/12/02)

P.62 Change U_CN5 pin33 and Pin34 to connect U_GND
P.06 [Clock Gen] Change test point type of TP153,TP154 for L6 requested
P.63 [Audio]Change U_R21,U_R23,U_R33,U_R36,U_R27,U_R29,U_R25,U_R26,U_R31
and U_R32 from 0201 to 0402 for L6 requested
P.33 [EC,LVDS] Add LED_OFF#(GPIO04) signal to U6.1 and U23.1 for Display Off issue.
P.25 [LVDS] Change SW1 from 8pin to 12pin for add Instant ON function

(2008/12/04)

P.50 [T/P Buttom] Change SW2 and SW3 from 1BT001-1420L-001(160g) to
1BT001-1410L-001(100g) for ME's requested
P.26 [HDMI] Swap RP47 and RP49 for layout convenience

(2008/12/05)

P.52 [HOLE] Change U_H3 from 1X-HOLE000-0935 to 1X-HOLE000-0959 for ME's requested
P.52 [HOLE] Change U_H1 from 1X-HOLE000-0905 to 1X-HOLE000-0958 for ME's requested
P.52 [HOLE] Change P_H3 from 1X-HOLE000-0936 to 1X-HOLE000-0960 for ME's requested

(2008/12/10)

P.33,34,37,40,43,46,51,54 [Test Pad] Add TP500~TP549 for BFT test pad
P.54 [DCIN] Delete PL6 for safety concern
P.37 [GLAN]NC R24,R25,U3,C16 and mount R616 for using M8057 internal EEPROM.
P.17 [VGA]Update VRAM strp for add Hynix VRAM
P.33 [EC]Add TP550,TP551 for detect D17 reverse from L6's suggestion
P.48 [USB]Add TP552~TP554 for detect USB power switch leakage from L6's suggestion

(2008/12/12)

P.59 [Other power plane]Change PQ40,PQ41 from SI2316DS-T1-E3 to SI7326DN-T1-E3
for overload test issue.
P.26 [HDMI]Change R647 and R646 to 3.9k ohm for meet E-DDC spec.
P.49 [BT]Change CN32 from QT510106-311H-7F to QT510106-312H-7F for ME's requested.

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(2008/12/15)

P.54 [DCIN&Charger] Change PC194, PC195 from NC_0.1U_50V_K 0603 to 220P_50V_K 0603 for EMI request

P.61 [VGA Power] Change PR99 from 6.98K_F 0402 to 11K_F 0402 for AMD M92 Power-Play function

P.61 [VGA Power] Change PR110 from NC_49.9K_F 0402 to 19.6K_F 0402 for AMD M92 Power-Play function

P.61 [VGA Power] Change PQ12 from NC to mount for AMD M92 Power-Play function

P.61 [VGA Power] Change PC85 from NC to mount for AMD M92 Power-Play function

P.61 [VGA Power] Change PR103 from 0_J 0402 to 1K_J 0402 for AMD M92 Power-Play function

(2008/12/18)

P.54 [DCIN&Charger] Change PC28, PC29 from 4.7U_25V_K 0805 to 4.7U_50V_K 1206 for reducing DC_IN inrush voltage.

P.54 [DCIN&Charger] Parallel PR32 and PR165 for reducing DC_IN inrush voltage.

P.54 [DCIN&Charger] Change PL1 from SPD8D43PT100M to PCMB063T-100MS for 2nd source implement.

P.50 [LED] Change R385 from 33ohm to 51ohm for LED brightness issue

(2008/12/19)

P.60 [OVP Protection] Add PR160 100K_J 0402 for MOR request.

P.46 [CAM]Change U41 to MAX4789EUK and delete C815,C816,R626 for VEDS current limit requested.

P.43 [FAN]Add F10 for prevent FAN sorot issue of MOR requested

P.24 [CRT]Change R418 and R424 from 22ohm to 33ohm for improve VEDS AGRB issue.

P.24 [CRT]Change CN2 from DZ11A91-SB281-4F to DZ11A91-SB2SN-4F for ME's requested.

(2008/12/20)

P14,15 [DDR2]Add C1289,C1290,C1291,C1292,C1293,C1294 (NC) for EMI concern and MOR requested

P.50 [TP]Change F7 from 0.5A to 0.35A for MOR's requested

P.47 [Felica]Change F6 from 0.5A to 0.35A for MOR's requested

P.47 [Felica]Add U56,C1295,C1296,R913 (NC) and R912 for reserve power switch for MOR's requested

P.40 [Audio]Change R493,R494 from 1k to 47k for Pi-Pi noise issue

(2008/12/22)

P.35 [Half Mini Card]Add R914 for RF team test VEDS,MP will delete it.

P.54 [DCIN&Charger]Change TP546~TP549 from 40mil to 60mil for BFT side requested.

P.23,33 [EC]Change signal name "LED_OFF#" to "LCD_OFF#" for MOR's suggestion.

P.60 [OVP]Change PC41 from 0.01uF to 1nF for Power_Abnormal_Conditions issue.

P.47 [Felica]Delete L60 for needless and SMT requested

P.48 [USB]Delete L61 for needless and SMT requested

(2008/12/23)

P.37 [Marvell GLAN]Delete TP538~TP545 for layout space concern

P.45 [PCI]Change C496 from 27p to 22p for improve crytal accuracy

P.29 [ICH9]Change footprint of D8 for SMT requested

P.30 [ICH9]Change footprint of D14 for SMT requested

(2008/12/24)

P.52 [HOLE]Change H5 from 1X-HOLE000-0925 to 1X-HOLE000-0913 for ME's requested

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(2008/12/26)

P.33 [EC] Add R915 for updating Instand On function.

(2009/02/09)

P.50 [T/P]Update the connection of SW2 and SW3 to correct T/P function

P.35 [WLAN]Update the connection of WLAN Switch to meet ME's requested

(2009/02/10)

P.54 [DCIN&Charger] Change PR32, PR165 from 1_J 1210 to 2_J 1210 for reducing DC_IN inrush voltage.

P.54 [DCIN&Charger] Change PC194, PC195 from 220P_50V_K 0603_NPO to 220P_50V_K 0402_NPO for PUR convenient.

P.54 [DCIN&Charger] Delete PR12 for unnecessary.

P.55 [SYS Power(+3_3V/+5V)] Delete PJ1, PJ2 for unnecessary.

P.56 [SYS Power(+1_5V/+1_05V)] Delete PJ3, PJ4 for unnecessary.

P.57 [DDR2 Power(+1_8V/+0_9V)] Delete PJ5, PJ8 for unnecessary.

P.58 [CPU_Vcore---ISL6266A] Delete PR20, PR38, PR46, PR65, PJ11 for unnecessary.

P.58 [CPU_Vcore---ISL6266A] Change PC145 from MATSUSHITA, EEEFK1E101XP to CHEMI-CON, EMVE250ADA101MF80G for MOR request.

P.59 [Others power plane] Delete PR72, PR77, PR89 for unnecessary.

P.60 [OVP protection] Delete PR97, PR105, PR108 for unnecessary.

P.61 [VGA Power(ATI VDD)] Delete PJ7, PJ9, PJ10 for unnecessary.

(2009/02/13)

P.29 [ICH9]Change R573 from mount to NC because BT_GPIO is not used for M850.

P.25 [LVDS]Change signal name "INST_ON_SW" to "INST_ON_SW#" because it's low active.

P.33 [EC]Change signal name "INST_ON_SW" to "INST_ON_SW#" because it's low active.

(2009/02/19)

P.50 [LED]Change R600 from 120ohm to 150ohm to satisfy brightness requested.

P.47 [Felica]Change F6 from 0.35A to 0.25A for felica module heated concern.

P.33 [EC]Add R916 for SPI ROM datasheet updated.

P.52 [HOLE]Change H4 from 1X-HOLE000-0926 to 1X-HOLE000-1052 for ME's requested.

P.52 [HOLE]Change H12 from 1X-HOLE000-0915 to 1X-HOLE000-1051 for ME's requested.

P.65 [USB]Change U_CN1 and U_CN2 form UB11193-C1308-4F to UB111S3-C1GS6-4H for ME's requested.

(2009/02/20)

P.59 [Others power plane] Change PQ16 from IRF8714PBF to IRF8736PBF for +1_8VRUN voltage drop issue.

P.60 [OVP protection] Change PR55 from 14.7K_F 0402 to 18.2K_F 0402 for BT+ OVP setting.

P.60 [OVP protection] Change PR143 from 20K_F 0402 to 26.1K_F 0402 for +5VALW OVP setting.

P.60 [OVP protection] Change PR144 from 47K_F 0402 to 80.6K_F 0402 for +3VALW OVP setting.

P.24 [CRT] Change CN2 from DZ11A91-SB2SN-4F to DZ11A91-SA2SN-4H for ME's requested.

P.47 [Felica]Change F6 from 0.25A to 0.125A for felica module heated concern.

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(2009/02/23)

P.50 [TP]Change SW2 and SW3 from 19-1BT0011-1003 to 19-SKHM0KE-1000 for ME's requested.

P.54 [DCIN]Move PC13,PC14,PC15 to the another side of PL8 for improving EMC.

P.52 [HOLE]Change BOSS3,BOSS6 from connect to GND to NC for improving EMC.

P.49 [BT]Change CN32 from QT510106-312H-7F to QT510106-312H-7H for ME's requested.

P.45 [ILINK]Change CN11 from UV31413-RU81P-7F to UV31413-RU82P-7H for ME's requested.

P.20 [VGA]Add C1297~C1308 for MOR's requested to check PEG signal.

(2009/02/24)

P.48 [USB]Change CN9 from UB111M3-CA4S4-7F to UB111M3-CAGS4-7H for MOR's requested.

(2009/02/25)

P.52 [HOLE]Change P_H3 from 1X-HOLE000-0960 to 1X-HOLE000-1054 for EMC's requested.

P.33 [EC]Change R915,R613,R475,R629,R435,R431(10K) from 0201 to 0402 for SMT's requested.

P.33 [EC]Change R173,R197,R203,R75,R124,R442,R440,R447,R432(100K) from 0201 to 0402 for SMT's requested.

P.33 [EC]Change R476(4.7K) from 0201 to 0402 for SMT's requested.

P.34 [Flash ROM]Change R233(0) from 0201 to 0402 for SMT's requested.

(2009/02/25b)

P.47 [Modem]Add TP600~TP606 for BFT test requested.

(2009/02/26)

P.48 [USB]Change C810 from Y5V to X5R for MOR VEDS requested.

P.40 [Audio]Delete Q27,R450,R614,Q8,R98,R615 for unnecessary to improve BFT test point.

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(2009/04/01)

P.33 [EC]Signal symbol "OVT_GFX#" change to two-way type for avoiding confusion from SW's suggestion.

(2009/04/08)

P.24 [CRT]Change CN2 from FOX_DZ11A91-SA2SN-4H to FOX_DZ11A91-SB2SN-4F (same as DVT used) for CONN discoloration issue.

P.48 [USB2.0]Change CN9 from FOX_UB111M3-CAGS4-7H to FOX_UB111M3-CA4S4-7F (same as DVT used) for CONN discoloration issue.

P.65 [USB DB]Change U_CN1 and U_CN2 from FOX_UB111S3-C1GS6-4H to FOX_UB11193-C1304-4F for CONN discoloration issue.

(2009/04/09)

P.45 [ILINK]Change CN11 from UV31413-RU82P-7H to UV31413-WU82P-7F for CONN discoloration issue.

M851 PVT

(2009/07/08)

P.35 [Half Mini Card]Add TP180,TP184 for LED test in L6.

P.50 [LED&T/P&LID]Add TP181,TP182,TP183 TP185,TP186,TP187,TP188 for LED test in L6.

(2009/07/09)

P.06 [Half Mini Card]Change R542,R276,R283,R288,R553,R277,R278,R536,R537,R538, R534 from 0201 to 0402 for SMT's request.

P.08 [Cantiga (DMI)]Change R286,R231,R193,R195 from 0201 to 0402 for SMT's request.

P.12 [Cantiga (VCC CORE)]Change R208 from 0201 to 0402 for SMT's request.

P.17 [VGA (Strap)]Change R809,R825,R826 from 0201 to 0402 for SMT's request.

P.18 [VGA (I/O)]Change R830,R831,R828 from 0201 to 0402 for SMT's request.

P.21 [VRAM (GDDR3)]Change R787,R763,R769,R765,R773,R771,RR772,R767,R770 from 0201 to 0402 for SMT's request.

P.22 [VRAM (GDDR3)]Change R801,R786,R800 from 0201 to 0402 for SMT's request.

P.28 [ICH9-M (LPC,IDE,SATA)]Change R101 from 0201 to 0402 for SMT's request.

P.29 [ICH9-M (GPIO)]Change R541,R540,R567, R322,R575,R300,R297,R303 from 0201 to 0402 for SMT's request.

P.33 [EC+KBC (WPCE775L)]Change R444,R477 from 0201 to 0402 for SMT's request.

P.38 [Audio (CODEC & POWER)]Change R230,R217 from 0201 to 0402 for SMT's request.

P.39 [Audio (HP)]Change R893,R894 from 0201 to 0402 for SMT's request.

P.41 [Audio (MUTE)]Change R241,R499,R227,R225,R486,R498,R500,R478 from 0201 to 0402 for SMT's request.

(2009/07/13)

P.39 [Audio (HP)]Change R893,R894 to 0201 again for avoiding side effect.

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