

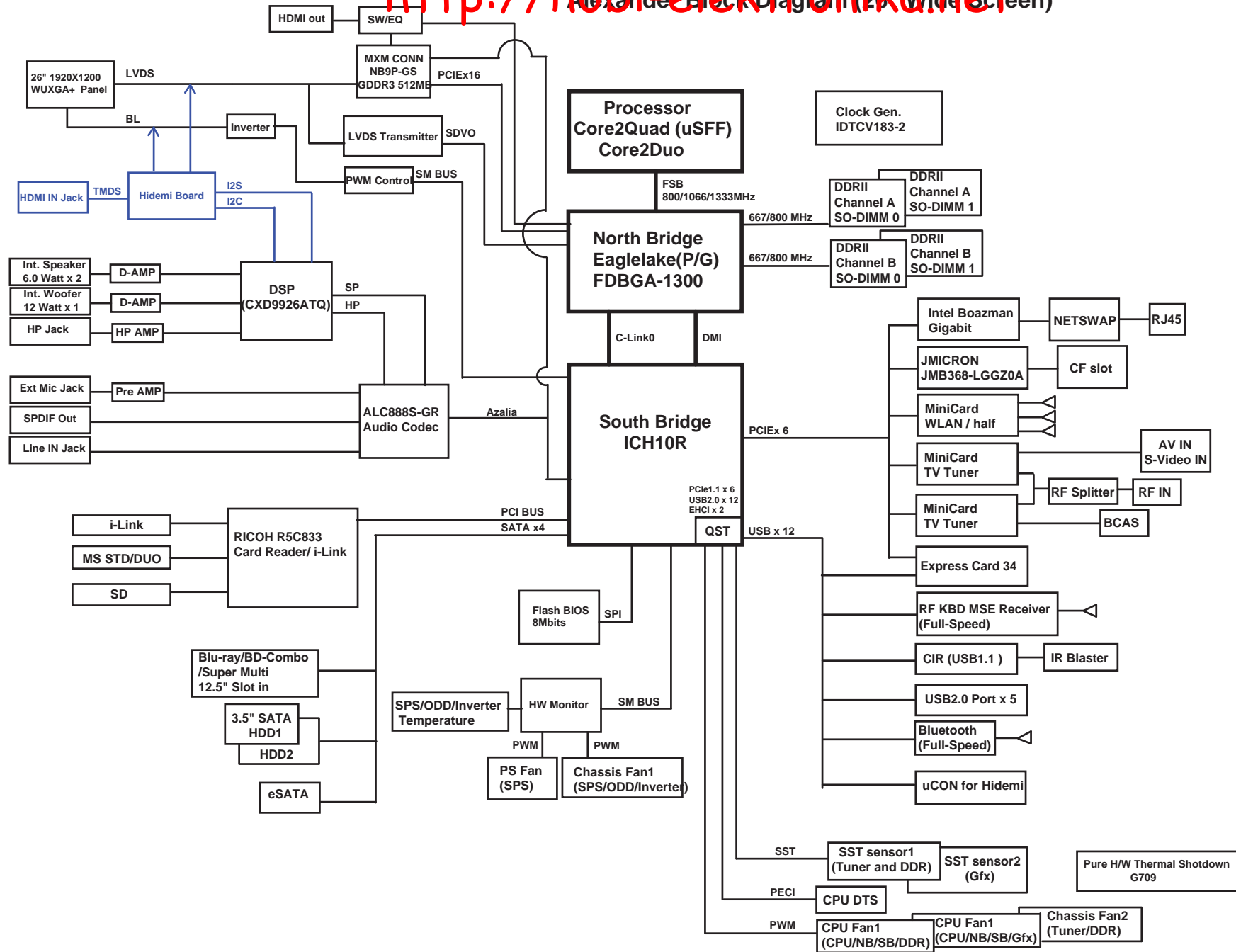
Schematics Page Index (Title / Revision / Change Date)

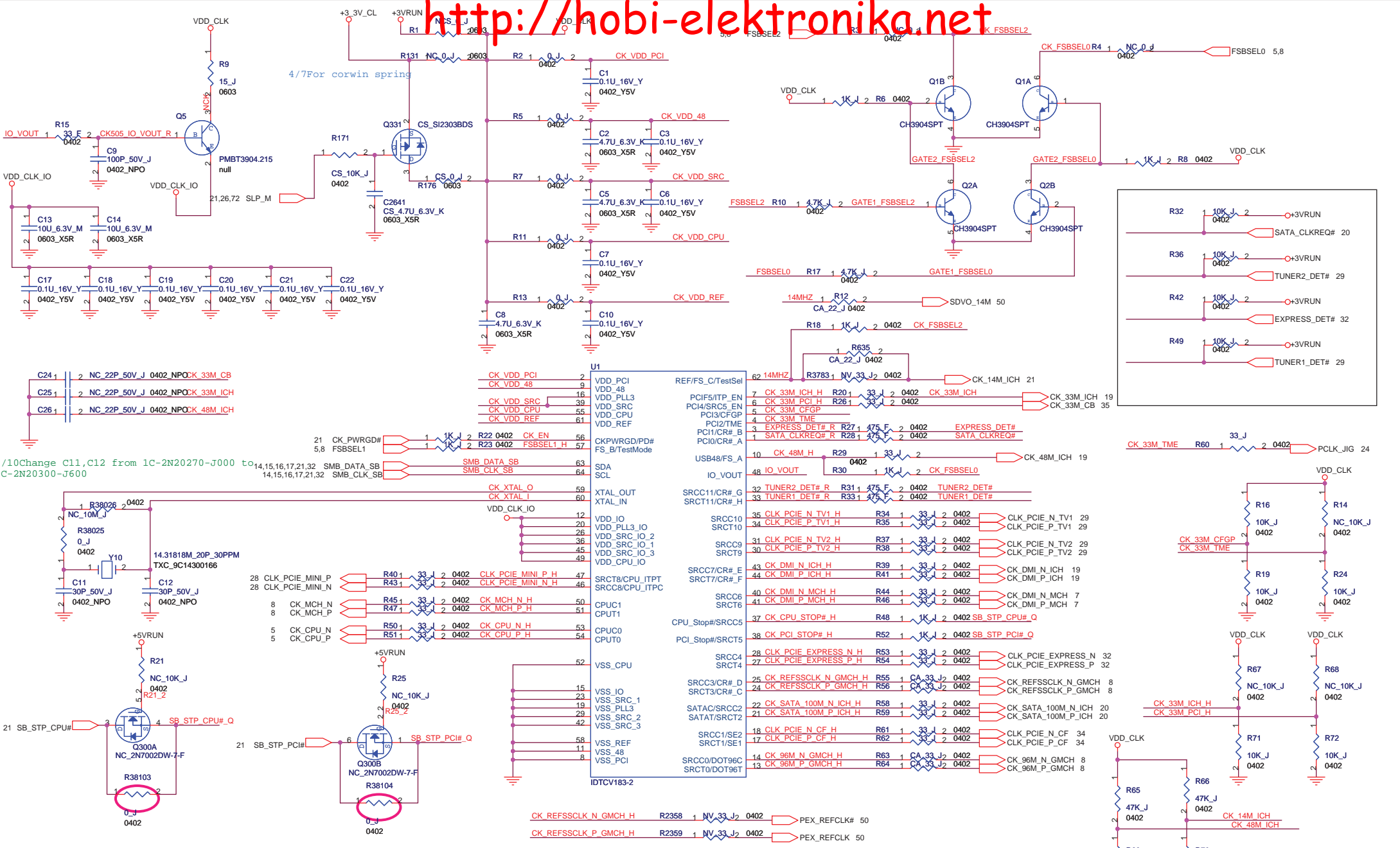
Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Index Page	0.1		49	VGA PCIE BUS	0.1	
02	Block Diagram (System)	0.1		50	VGA MXM CONN PCEI	0.1	
03	CLOCK GEN	0.1		51	VGA MXM CONN OUT	0.1	
04	CPU HOST 1/3	0.1		52	VGA MXM CONN POWER	0.1	
05	CPU THERMAL 2/3	0.1		53	VGA MB TO HIDEMI CONN	0.1	
06	CPU POWER 3/3	0.1		54	AUDIO(CODEC & POWER)	0.1	
07	Eaglelake HOST/PCI-E 1/7	0.1		55	AUDIO DSP	0.1	
08	Eaglelake VGA/MISC 2/7	0.1		56	AUDIO(HP)	0.1	
09	Eaglelake DDR CH A 3/7	0.1		57	AUDIO(SP AMP)	0.1	
10	Eaglelake DDR CH B 4/7	0.1		58	AUDIO(SW AMP)	0.1	
11	Eaglelake POWER 5/7	0.1		59	AUDIO(EXTMIC&LINE IN)	0.1	
12	Eaglelake POWER 6/7	0.1		60	AUDIO (MUTE)	0.1	
13	Eaglelake GND 7/7	0.1		61	Power Block Diagram	0.1	
14	DDRII(CHANNEL A) 1/4	0.1		62	DCIN	0.1	
15	DDRII(CHANNEL A) 2/4	0.1		63	CPU_DCIN	0.1	
16	DDRII(CHANNEL B) 3/4	0.1		64	SYSPWR(+3V/+5V)	0.1	
17	DDRII(CHANNEL B) 4/4	0.1		65	DDR2PWR(+1_8V/+0_9V)	0.1	
18	DDRII Termination	0.1		66	SYSPWR(+1_1V/+1_5V)	0.1	
19	ICH10R (PCIe/USB/PCI) 1/5	0.1		67	SYSPWR(+1_2V)	0.1	
20	ICH10R (HOST/SATA) 2/5	0.1		68	VH CORE (1) -- ISL6334A	0.1	
21	ICH10R (PM/LAN/HDA) 3/5	0.1		69	VH CORE (2) -- ISL6208	0.1	
22	ICH10R (Power) 4/5	0.1		70	OVP Protect	0.1	
23	ICH10R (Ground) 5/5	0.1		71	Others PWR Plane	0.1	
24	Flash ROM & DEBUG	0.1		72	Corwin spring(3_3/1_1V_CL)	0.1	
25	Power Sequence 1/2	0.1		73	HOLES & BOSS	0.1	
26	Power Sequence 2/2	0.1		74	Power Sequence Timing	0.1	
27	INTEL GLAN Boazman	0.1		75	Revision History(1)	0.1	
28	PCIe WLAN	0.1		76	Revision History(2)	0.1	
29	TV-TUNER1&TUNER2	0.1		77	Revision History(3)	0.1	
30	AVIN/SVIDEO IN/RF Splitter	0.1					
31	B-CAS	0.1					
32	ExpressCard	0.1					
33	PCIe(CF Card)	0.1					
34	CF Card CLCOK BUFFER	0.1					
35	PCI BUS(Bridge) 1/2	0.1					
36	PCI BUS(MS&SD&iLink) 2/2	0.1					
37	SATA HDD/SATA ODD/e-SATA	0.1					
38	e-SATA	0.1					
39	USB Port & CONN	0.1					
40	CIR&BT	0.1					
41	RF KB CONN	0.1					
42	Thermal & BL	0.1					
43	FAN	0.1					
44	LED	0.1					
45	DB CONN (Pswitch/PSP/IO)	0.1					
46	VGA CRT (FOR DEBUG)	0.1					
47	VGA LVDS	0.1					
48	VGA HDMI OUT	0.1					

FUBAI PCB P/N: 1P-0089J00-80SA

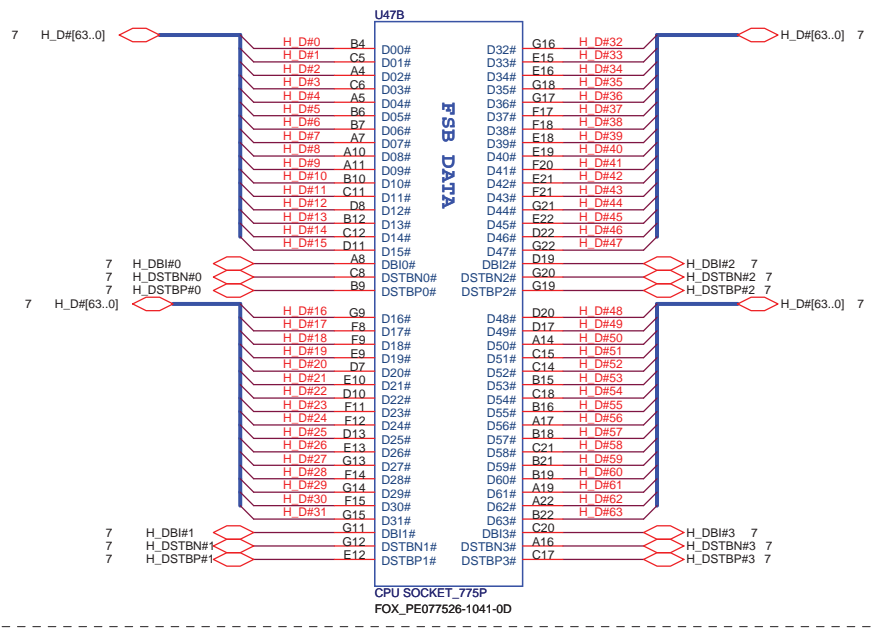
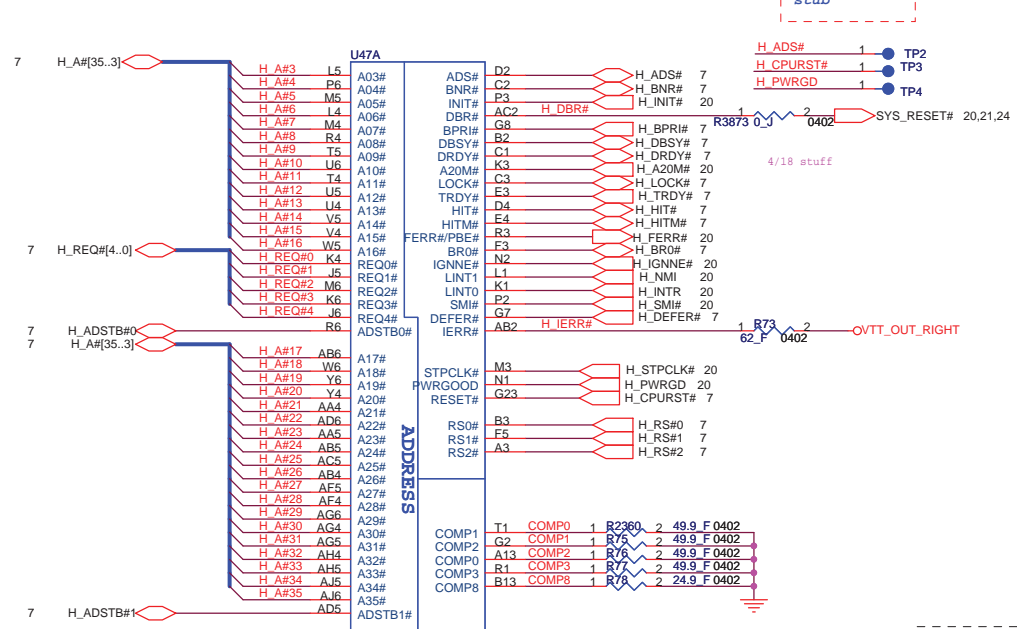
P. Leader	Check by	Design by

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title Index Page			
Size	Document Number	Rev	
A3	M841 DVT		
Date:	Tuesday, September 23, 2008	Sheet	1 of 77





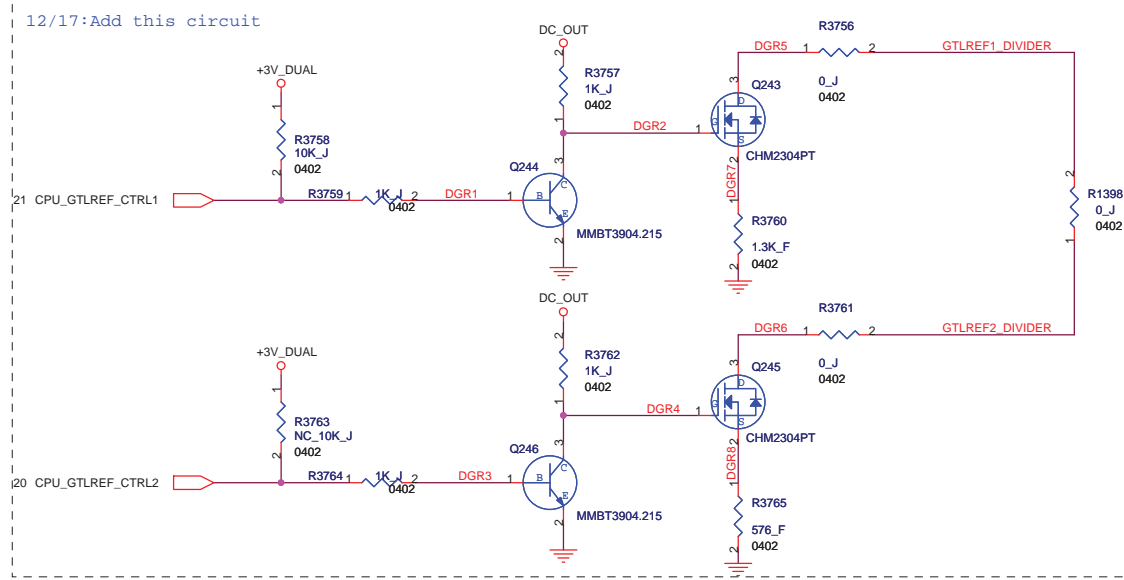
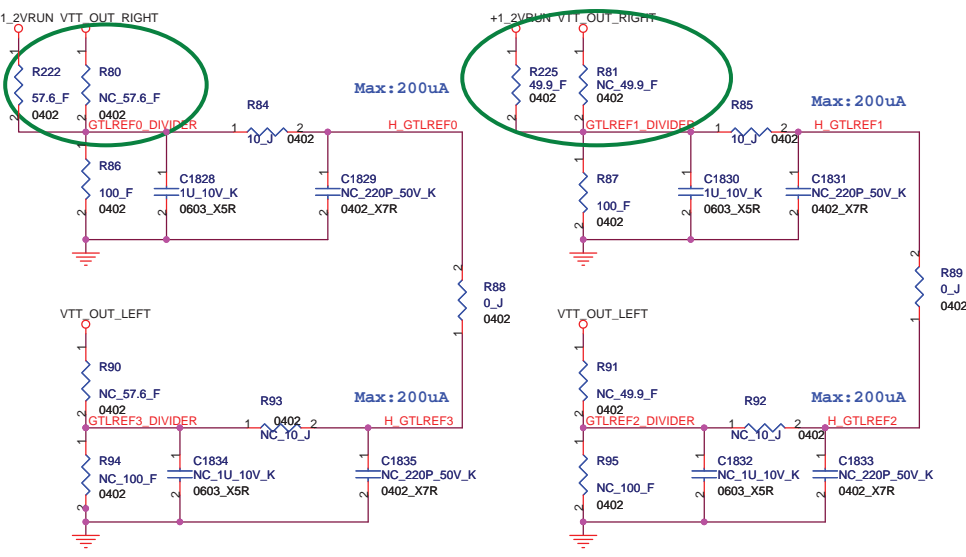
Connect test point with no stub



CPU SIGNAL TERMINATION



Layout note : Please near the processor



GTLREF FUNCTION TABLE

CPU_GTLREF_CTRL2	CPU_GTLREF_CTRL1	Ratio Set
0	0	0.615 X VTT
0	1	0.63 X VTT
1	0	0.65 X VTT
1	1	0.67 X VTT

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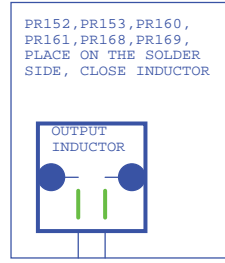
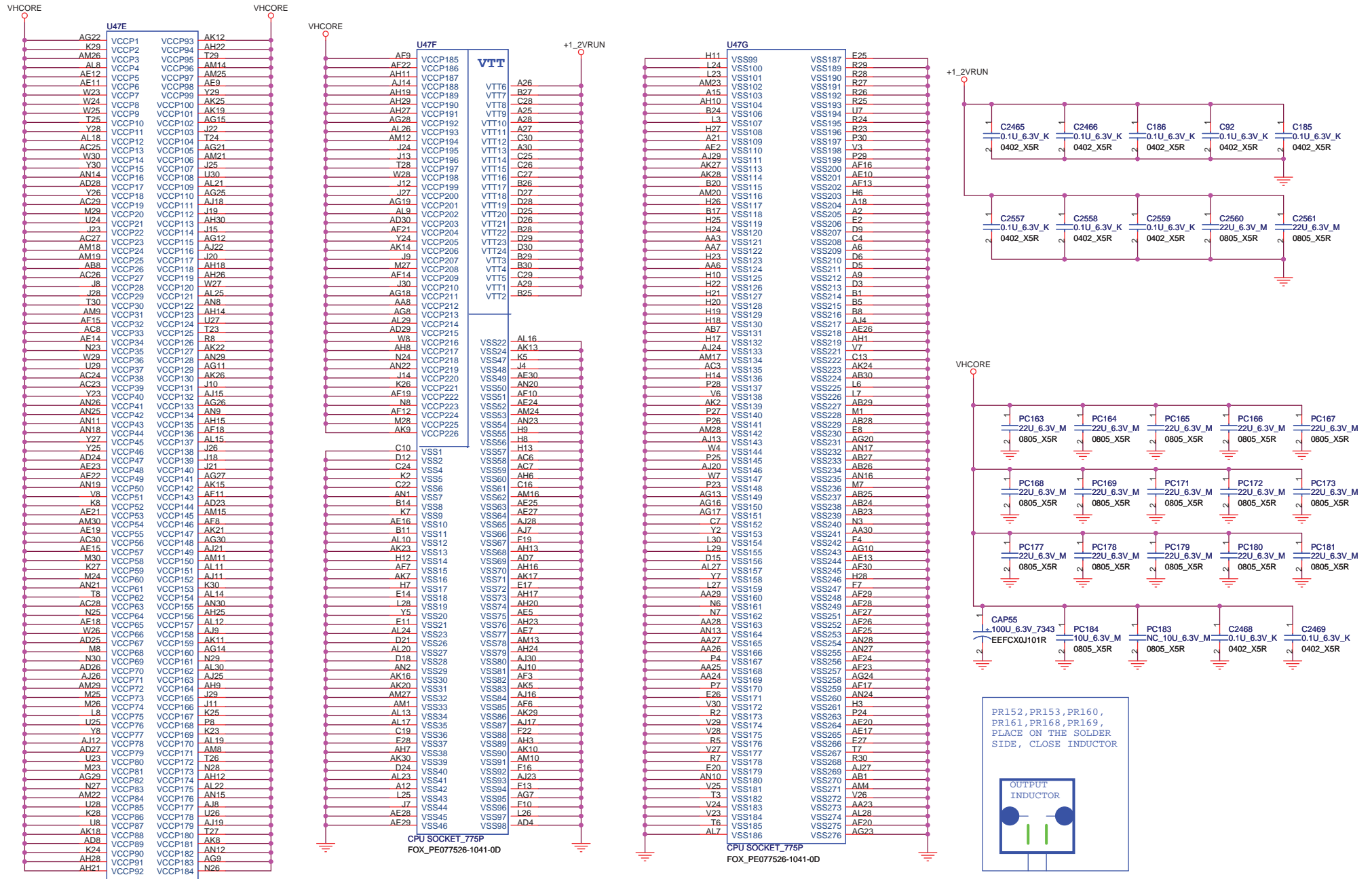
File: **CPU HOST**

Size: A3 Document Number: **M841 DVT** Rev: 0.1

Date: Saturday, September 13, 2008 Sheet 4 of 77

VHOCORE(0.85V-1.45V,VCC_BOOT=1.1V):
 Wolfdale--max 75A
 Yorkfied--max 125A

<http://hobi-elektronika.net>

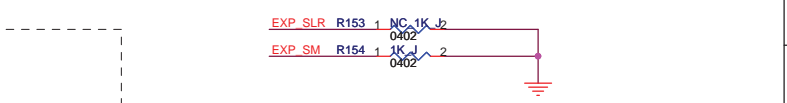
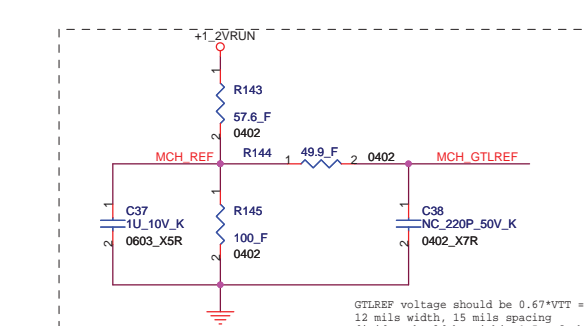
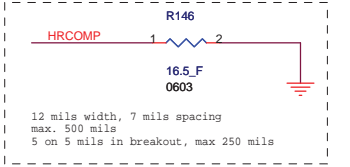
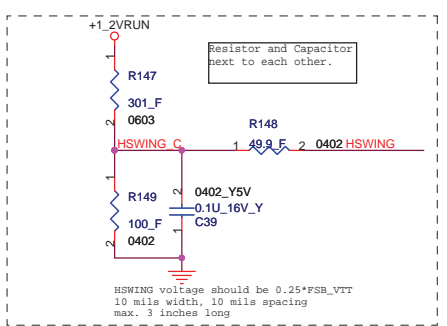
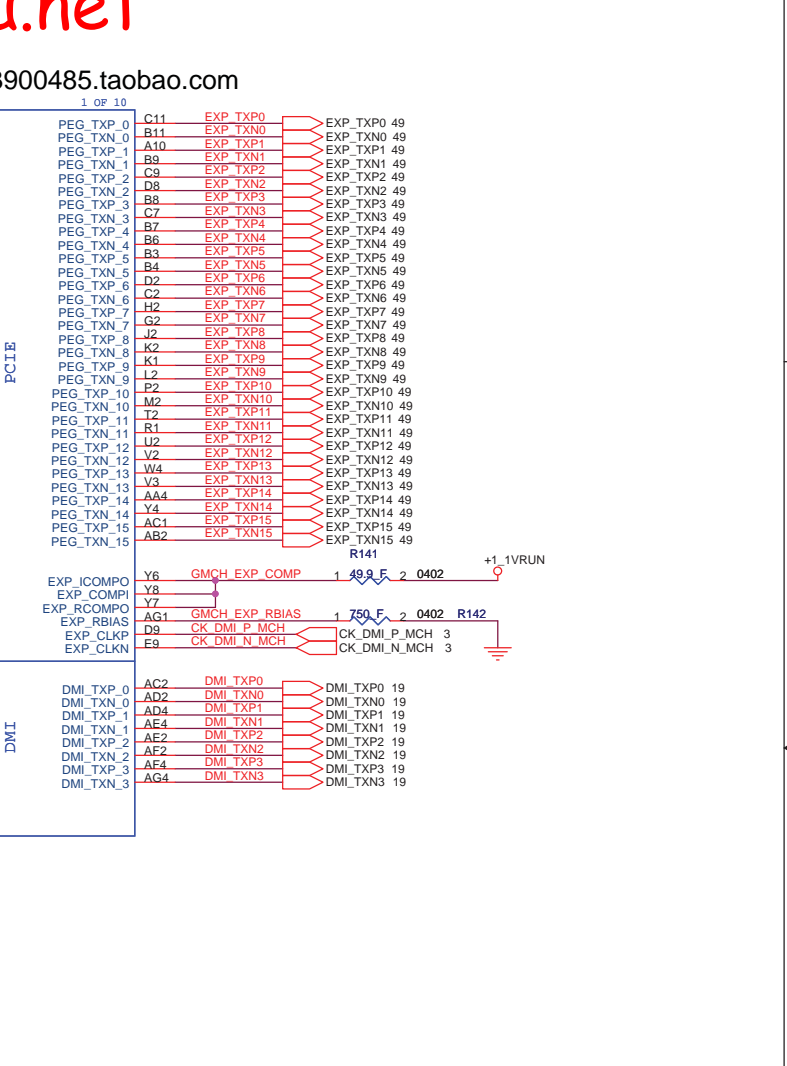
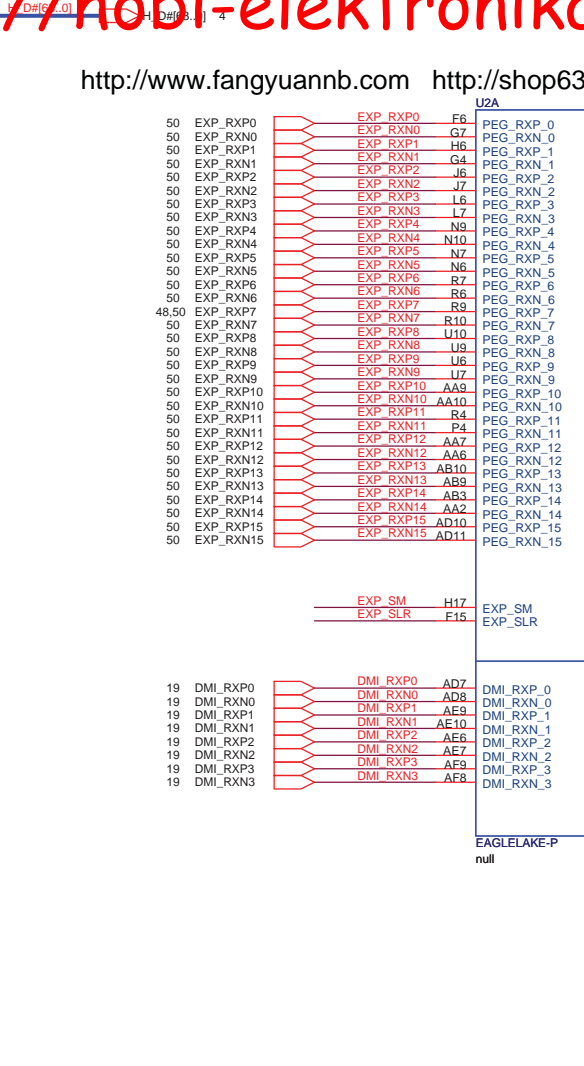
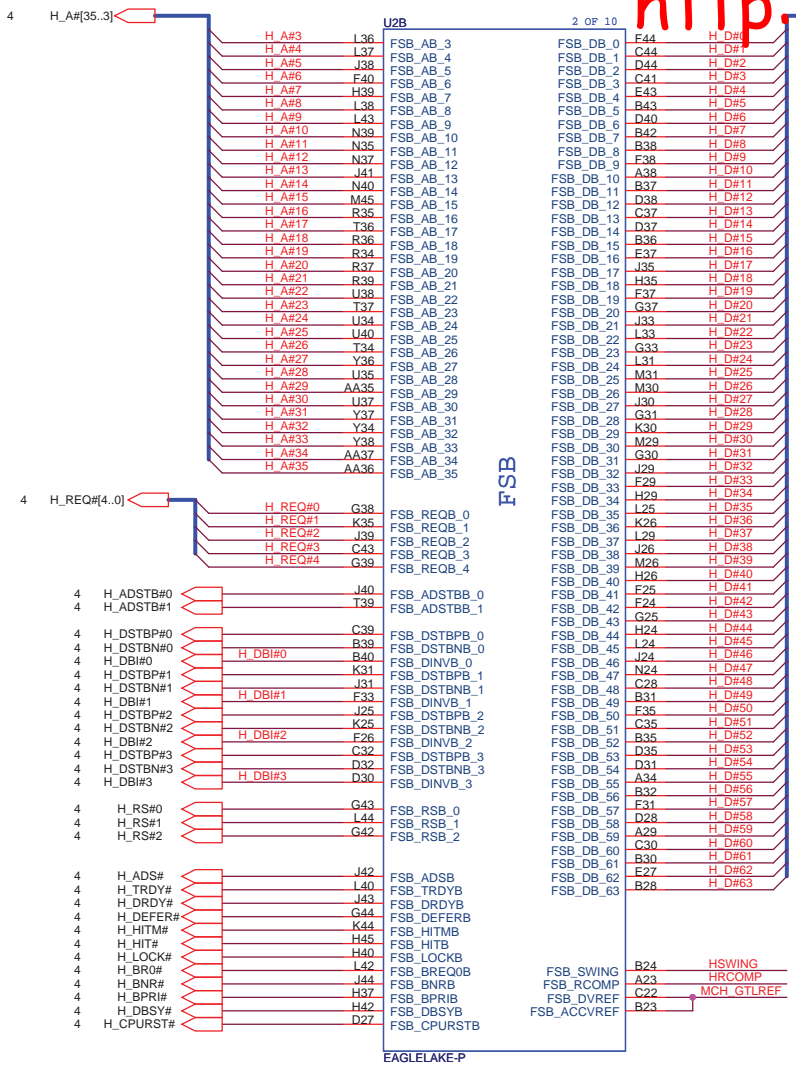


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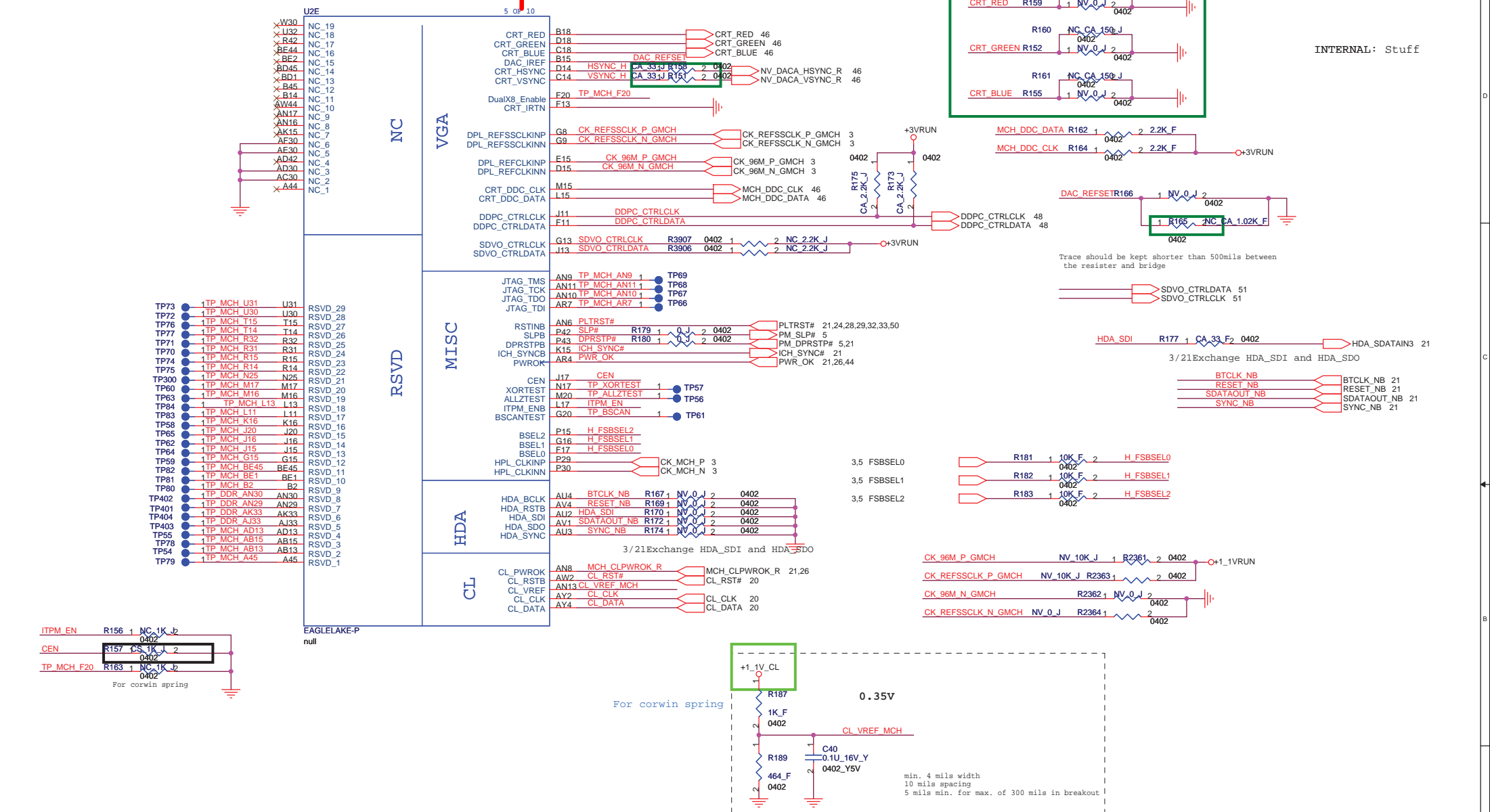
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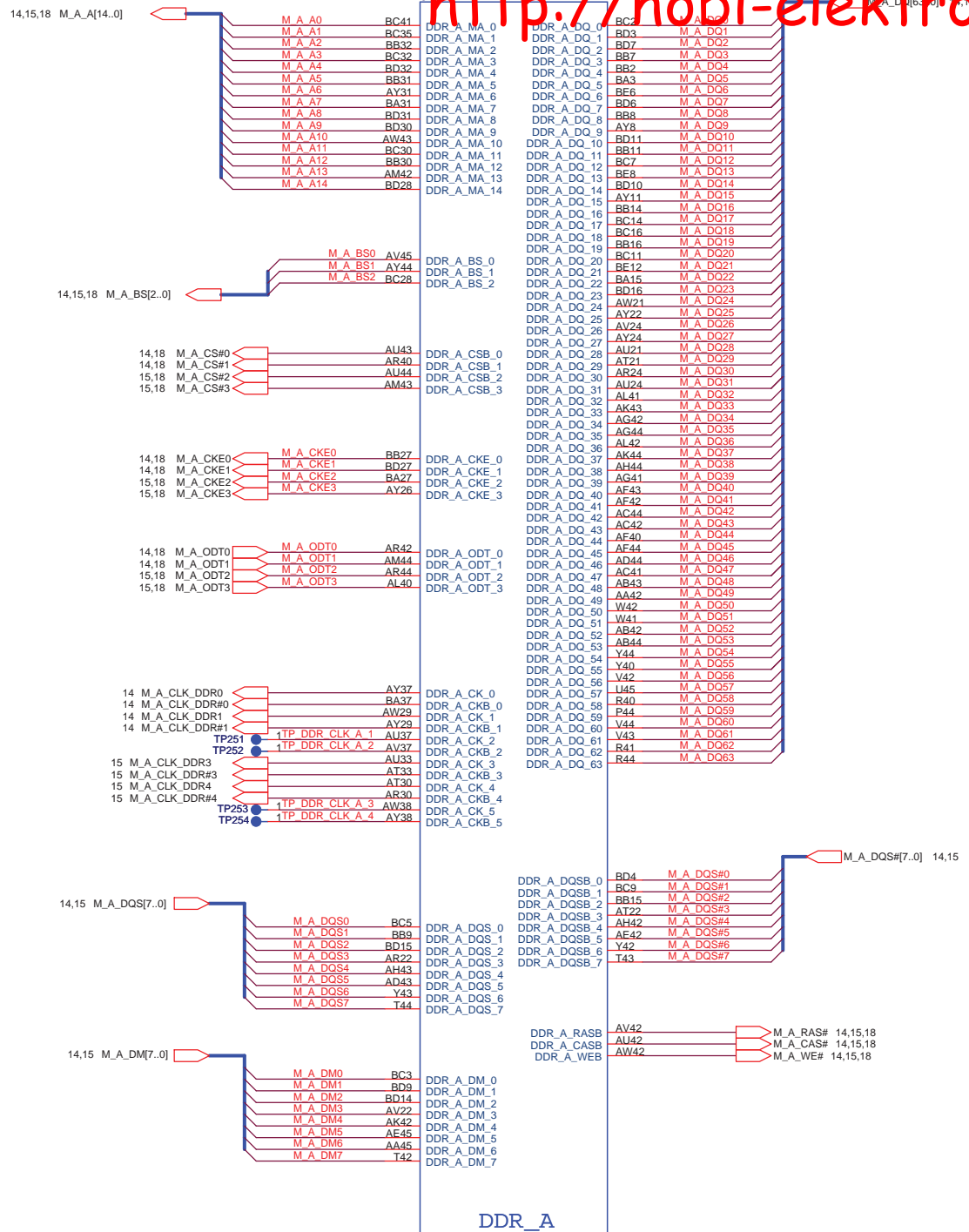
Size A3 Document Number **M841 DVT** Rev 0.1

Date: Thursday, September 11, 2008 Sheet 6 of 77



INTERNAL: Stuff

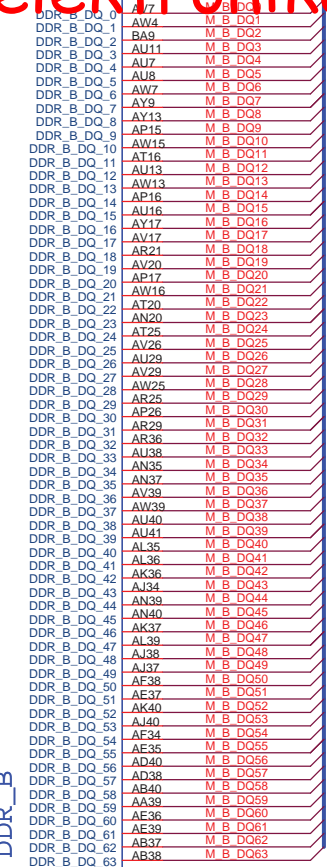
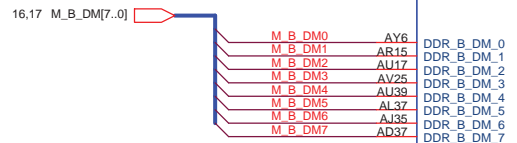
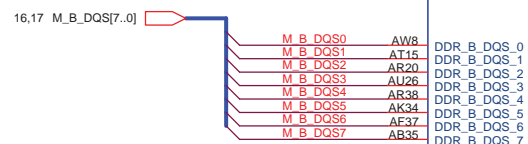
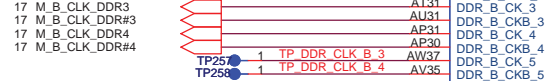
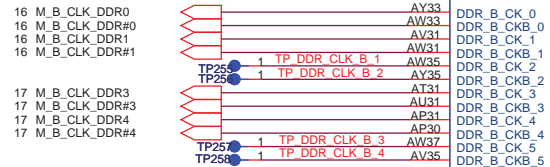
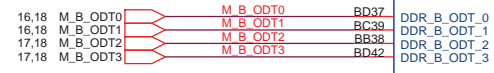
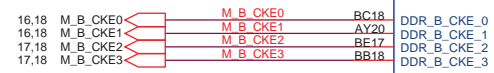
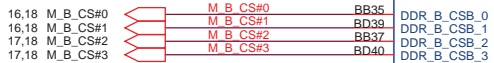
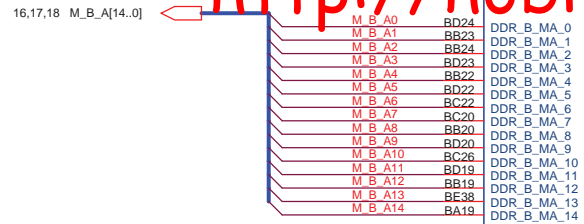




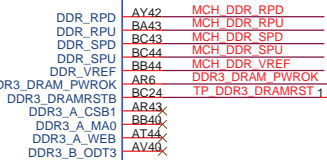
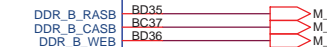
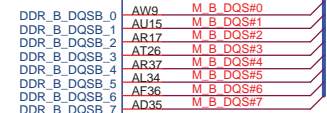
DDR_A

EAGLELAKE-P
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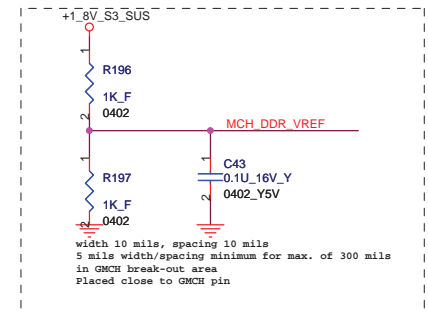
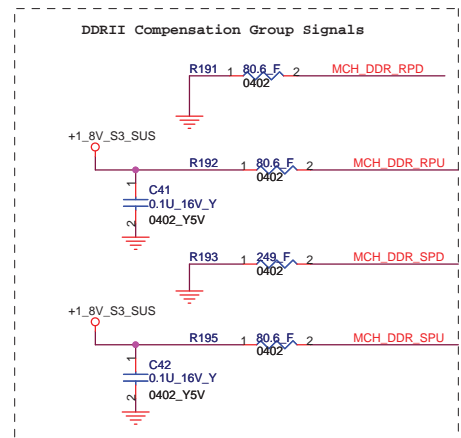
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File: Eaglelake DDR CH A 3/7		
Size	Document Number	Rev
A3	M841 DVT	0.1
Date:	Saturday, September 13, 2008	Sheet 9 of 77



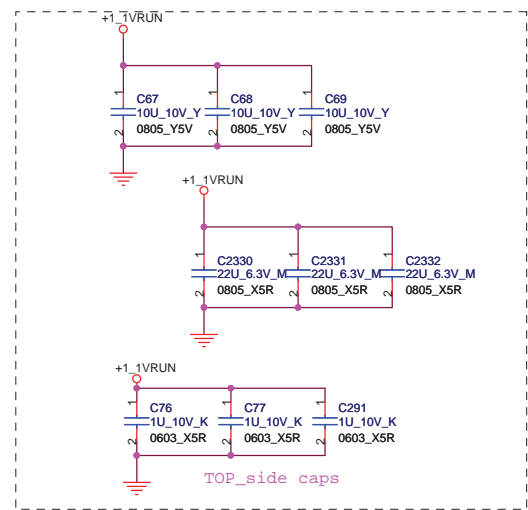
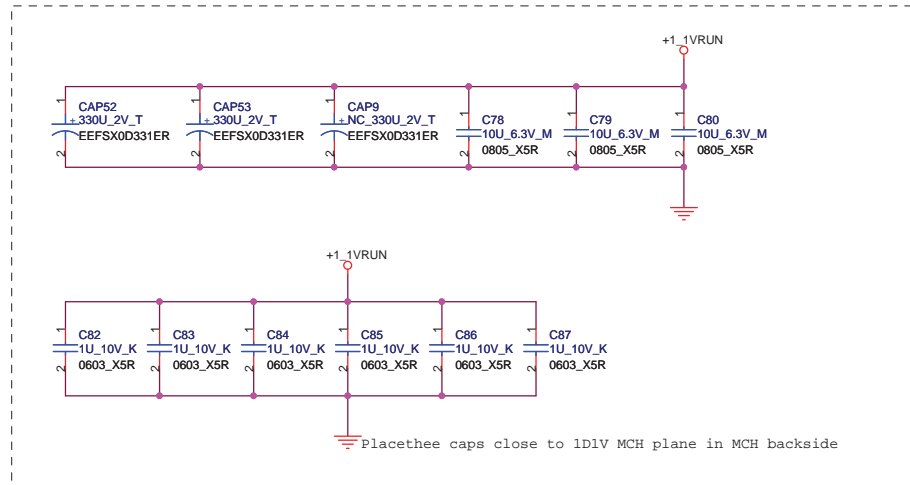
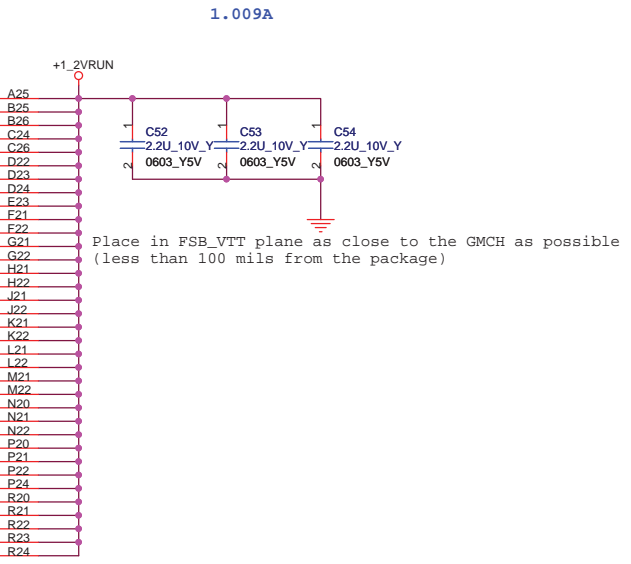
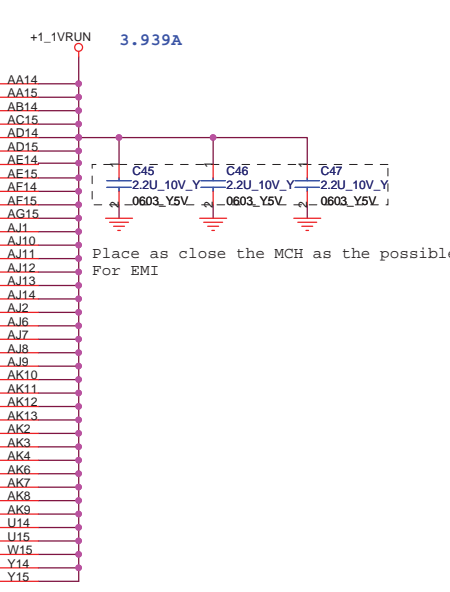
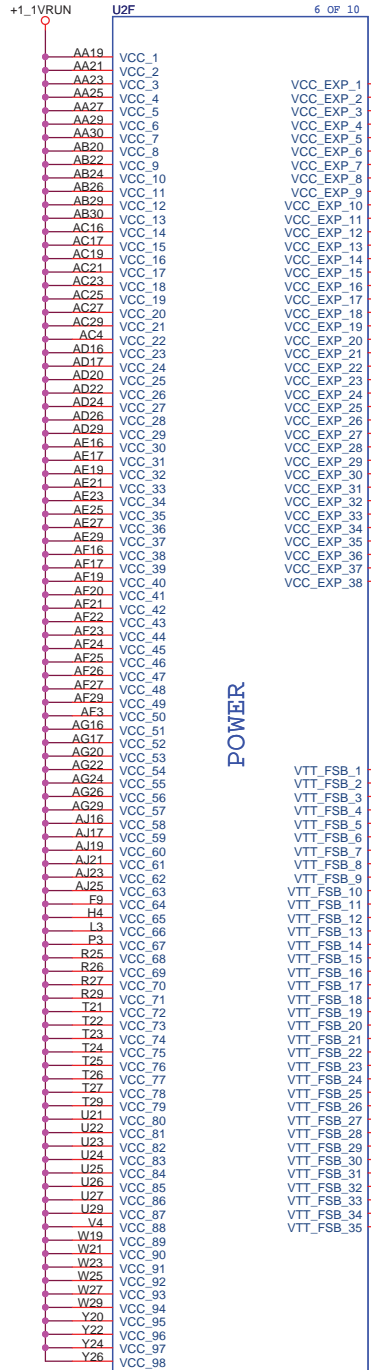
DDR_B



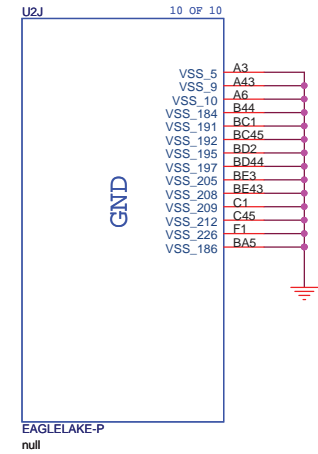
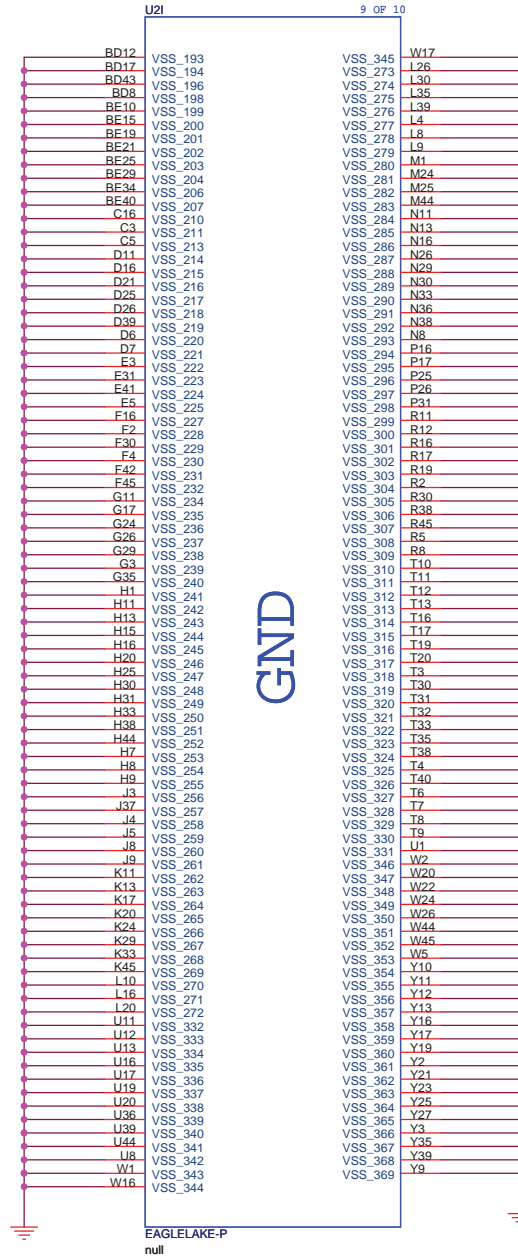
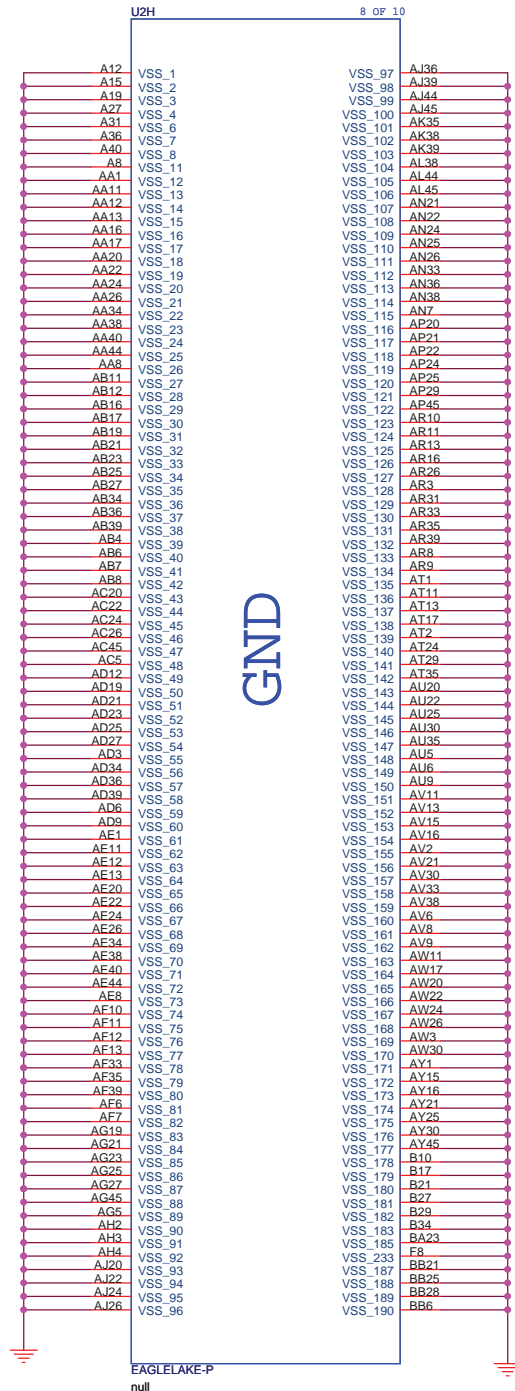
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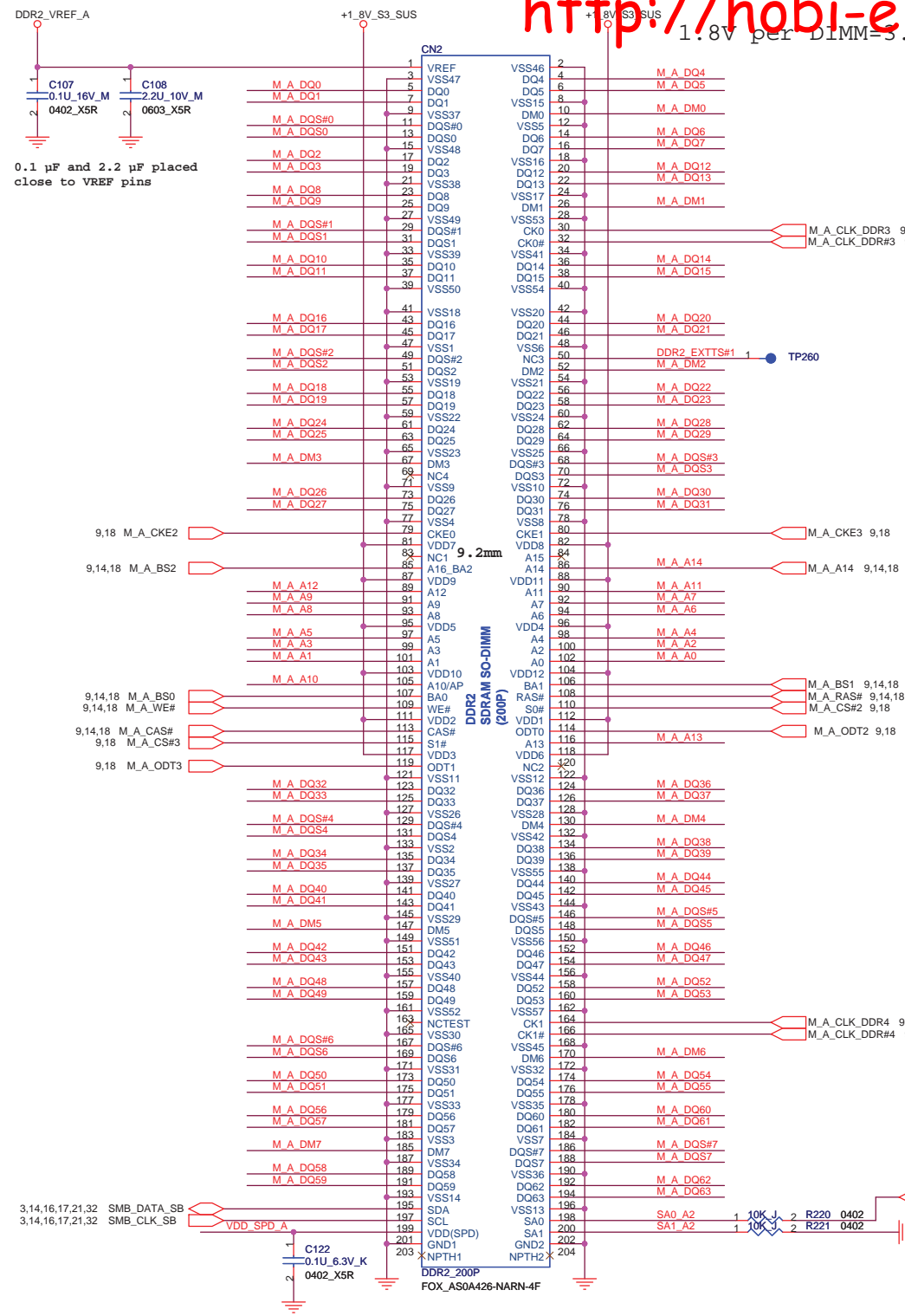
26.40A



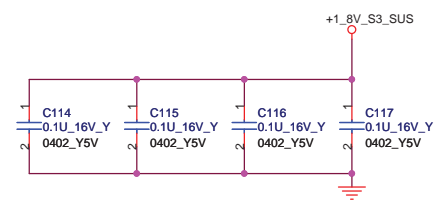
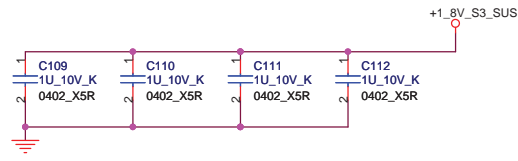
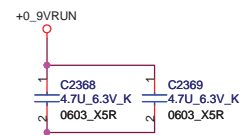
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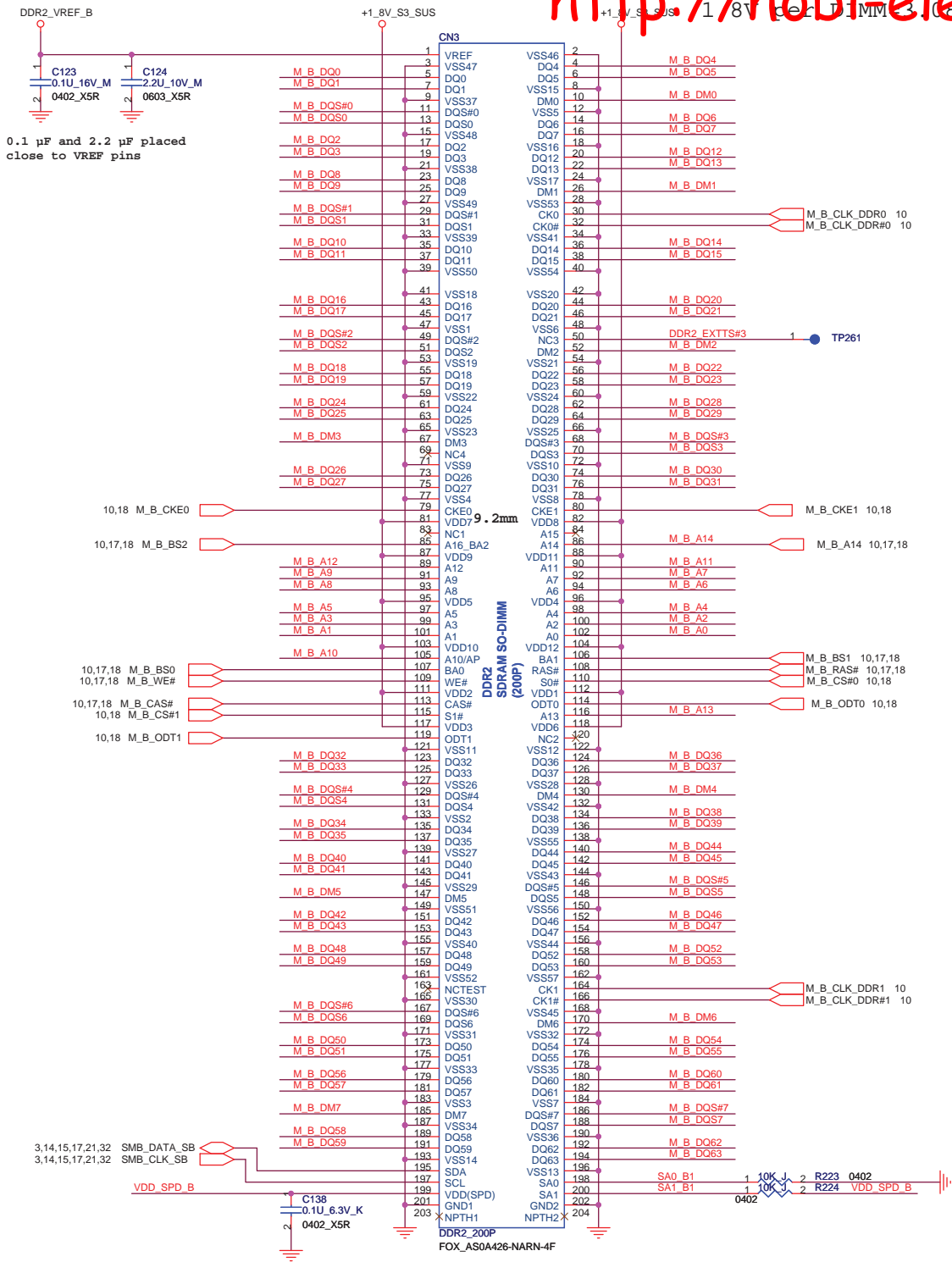
1.8V per DIMM=3.06A

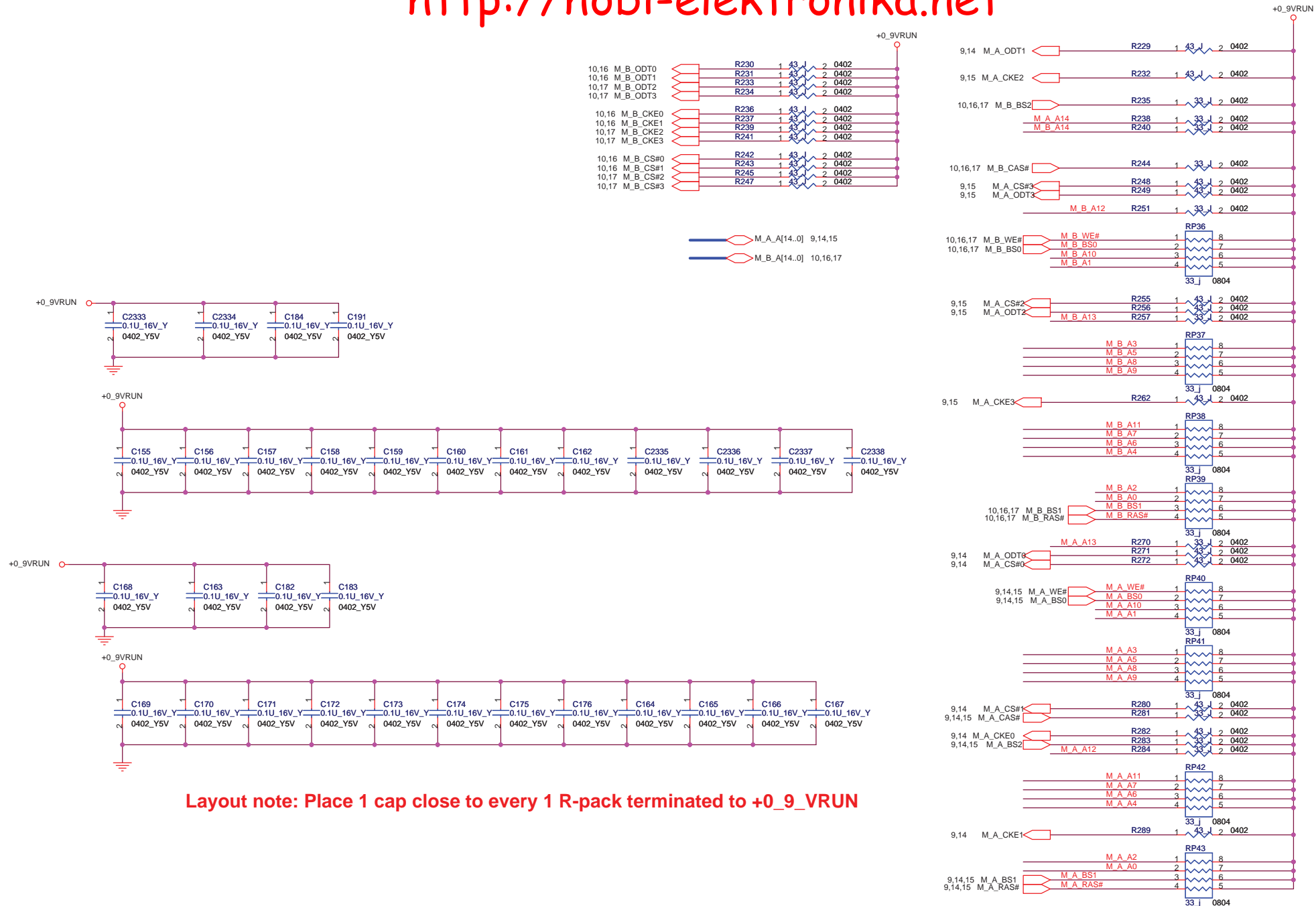


- M_A_DM[7..0] 9,14
- M_A_DQ[63..0] 9,14
- M_A_DQS[7..0] 9,14
- M_A_DQS#[7..0] 9,14
- M_A_A[14..0] 9,14,18



FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
File DDRII(CHANNEL A)		
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 15 of 77	





Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9_VRUN

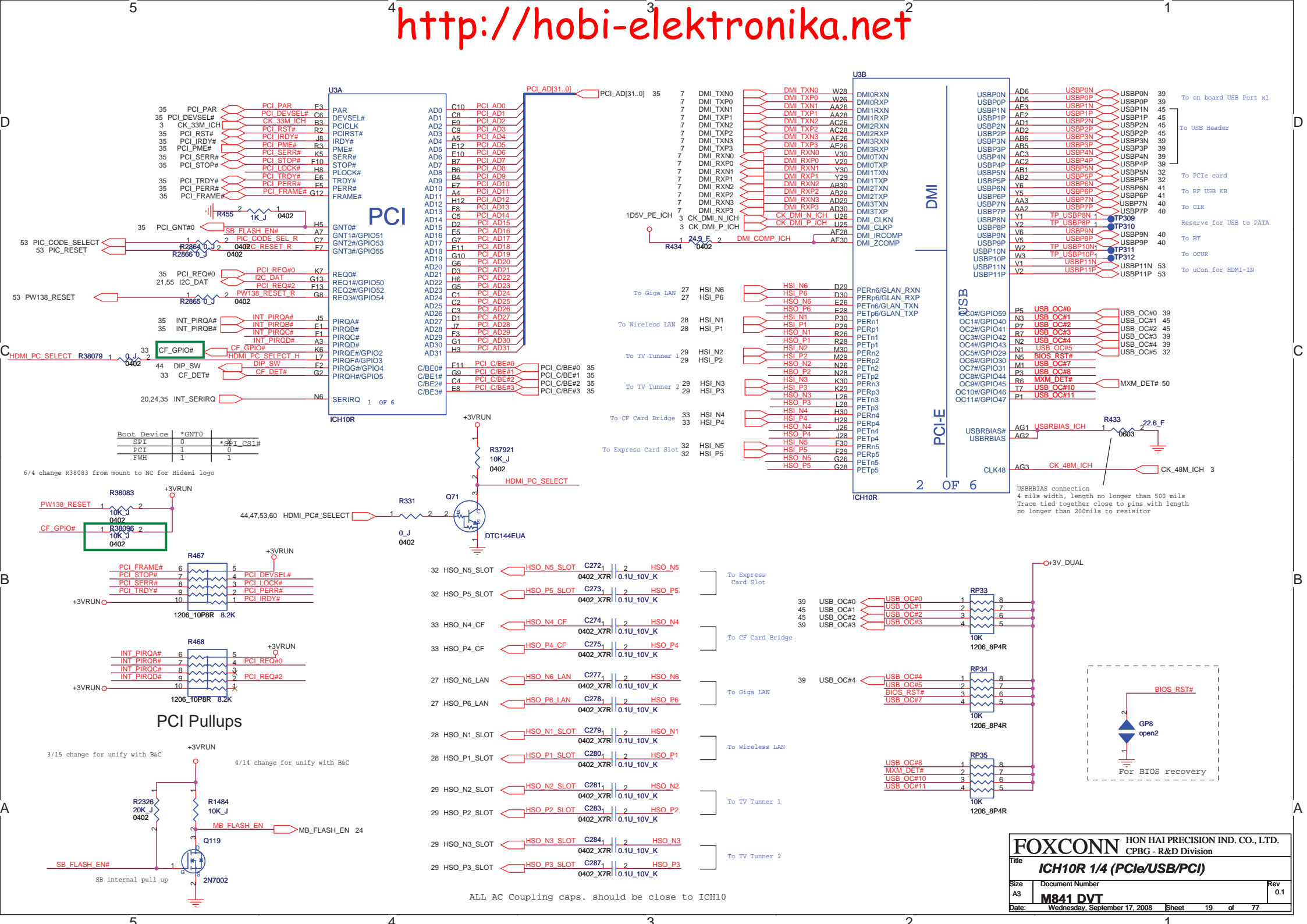


Table with 3 columns: Boot Device, *GNT0, *GNT CS1#. Rows include SPI, PCI, and FWH.

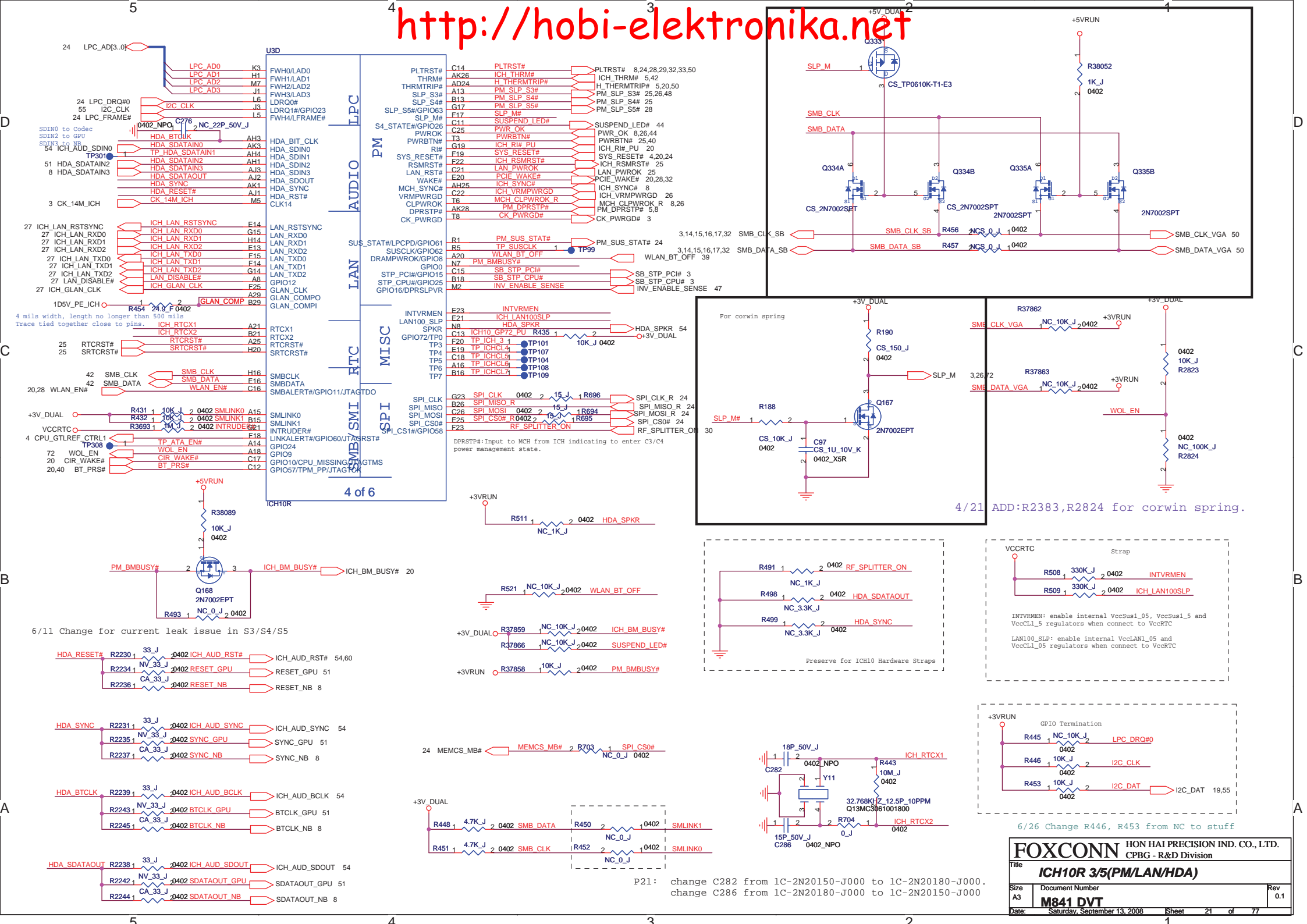
6/4 change R38083 from mount to NC for Hidemi logo

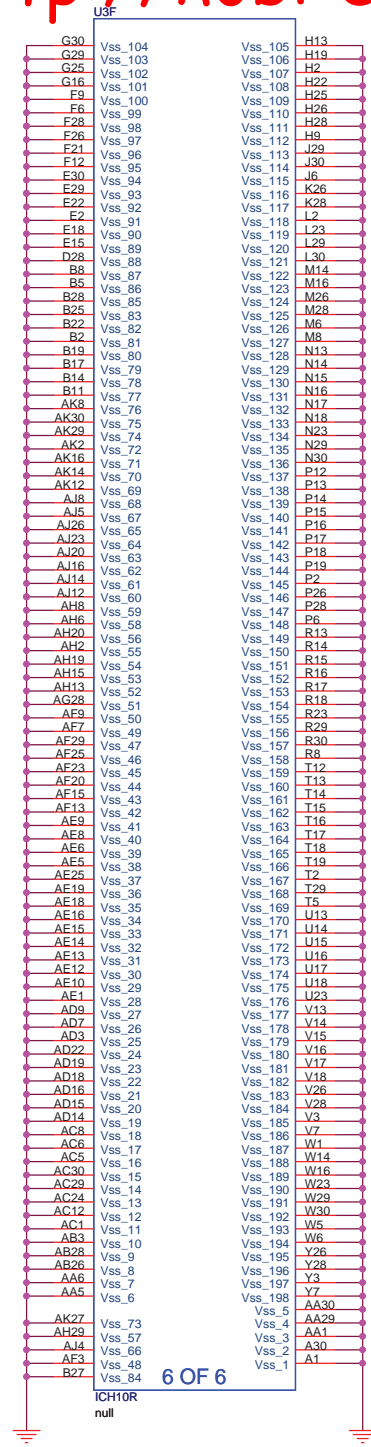
PCI Pullups

3/15 change for unify with B&C

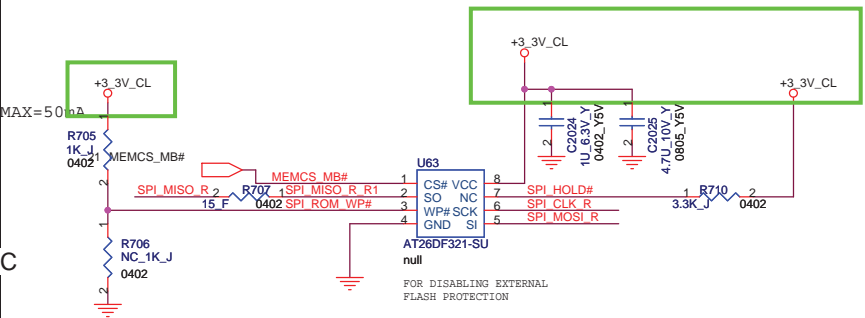
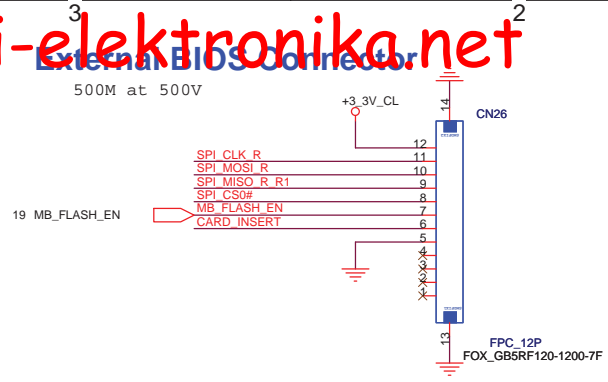
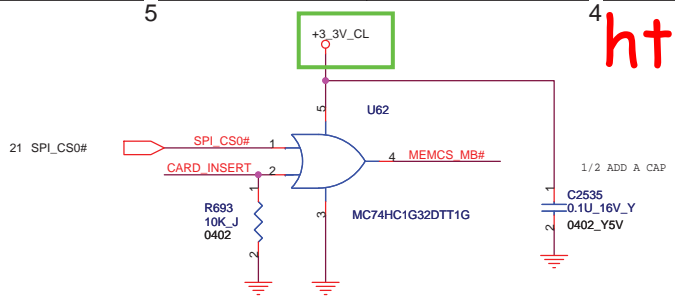
4/14 change for unify with B&C

FOXCONN HON HAI PRECISION IND. CO., LTD. ICH10R 1/4 (PCIe/USB/PCI) M841 DVT. Includes date, sheet number, and revision info.

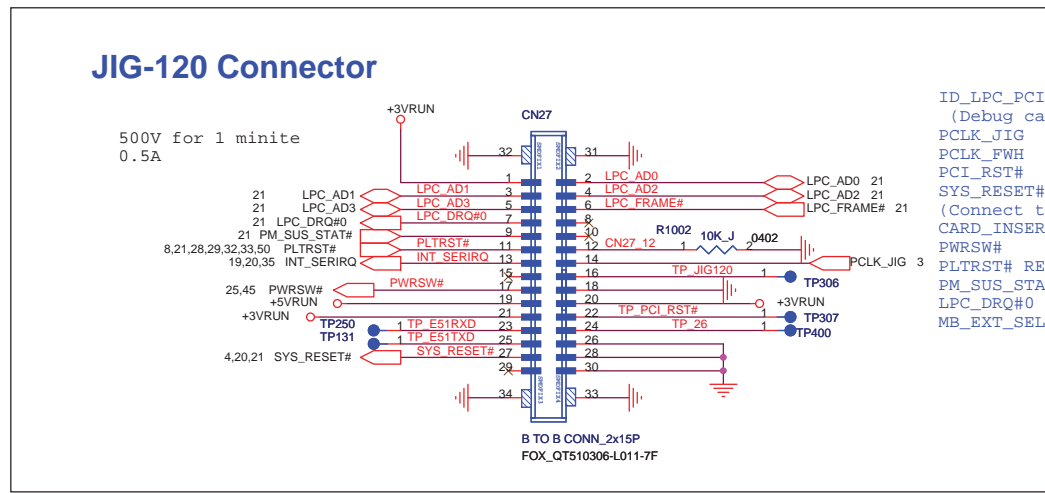




FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title ICH10R 5/5(Ground)	
Size A3	Document Number M841 DVT
Date: Thursday, September 11, 2008	Sheet 23 of 77
Rev 0.1	

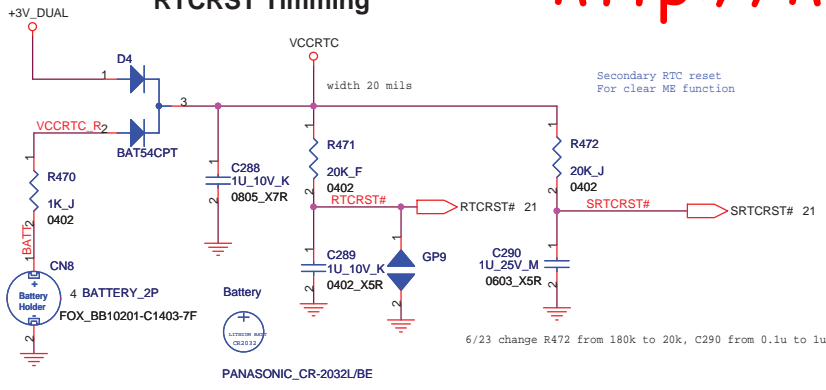


SPI Interface BIOS



ID_LPC_PCI#:Detect 80 port by LPC or PCI bus.
 (Debug card did not use this signal right now)
 PCLK_JIG
 PCLK_FWH
 PCI_RST#
 SYS_RESET#General SMI# from JIG-120
 (Connect through a switch to GND on debug card)
 CARD_INSERT
 PWRSW#
 PLTRST# RESET外設
 PM_SUS_STAT# LPC power down
 LPC_DRQ#0
 MB_EXT_SEL

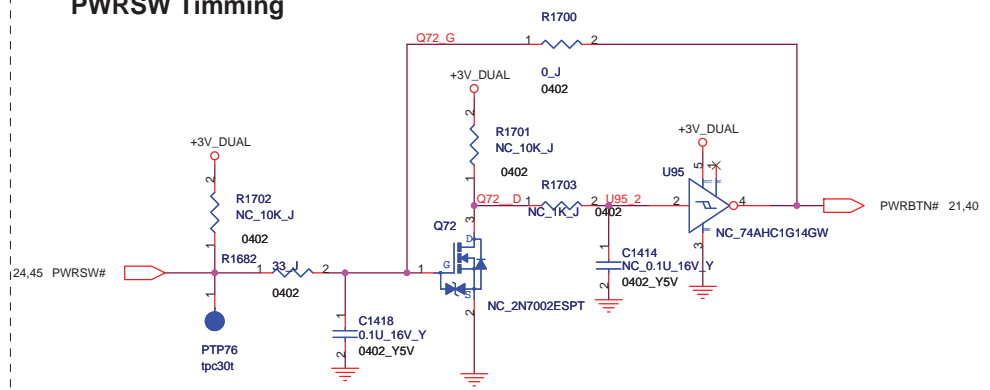
RTCST Timming



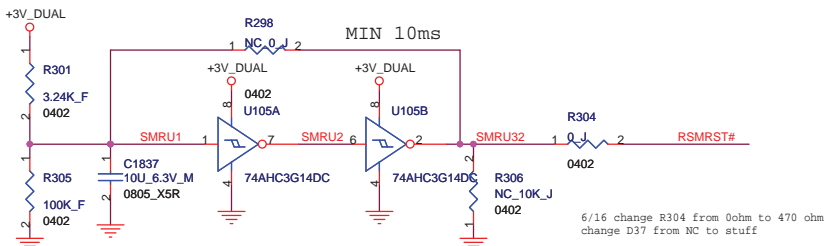
6/23 change R472 from 180k to 20k, C290 from 0.1u to 1u

PANASONIC_CR-2032L/BE

PWRSW Timming



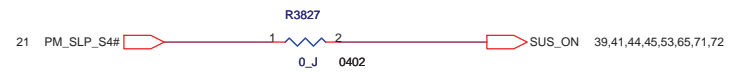
RSMRST Timming



6/16 change R304 from 0ohm to 470 ohm
change D37 from NC to stuff

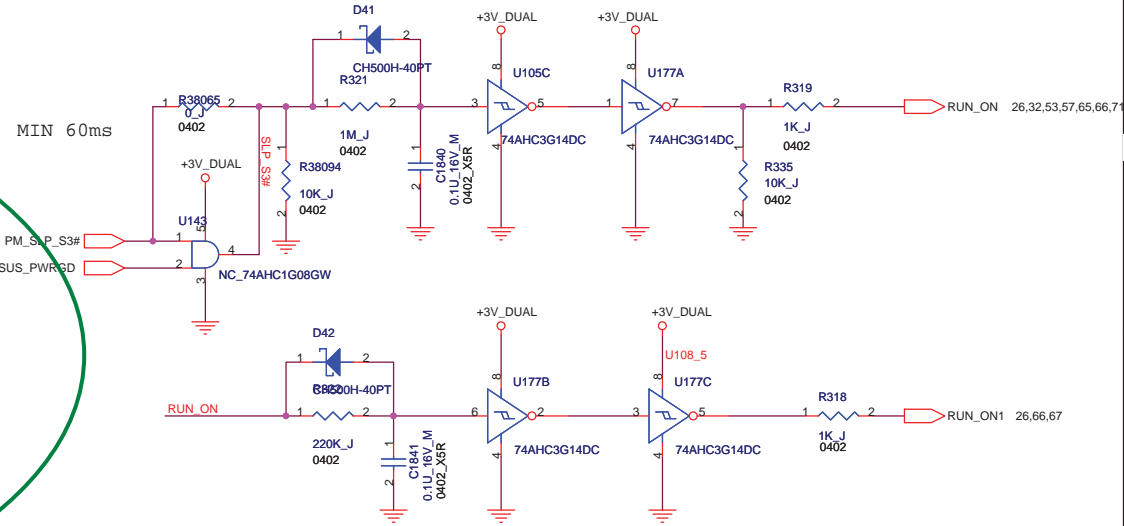
RSMRET# falling edge must transition to 0.8 V or less before +3V_DUAL drops to 2.1V

SLP_S4#

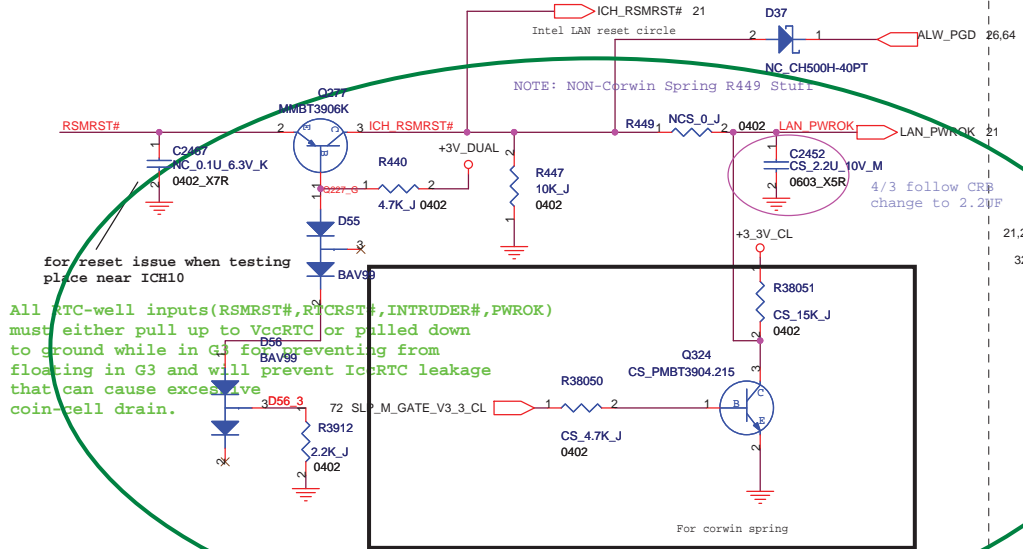


P25: Change R38094 form NC to 1R-0000103-J200

SLP_S3# --> RUN_ON



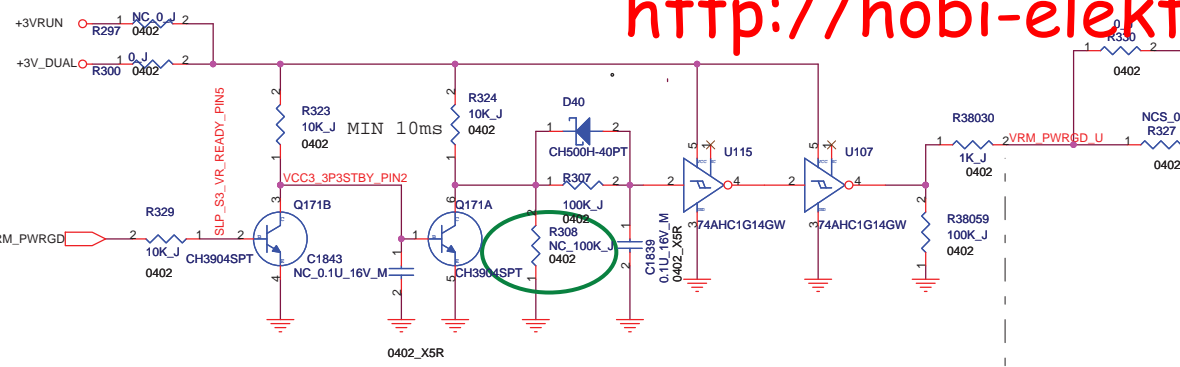
6/6 unify sequence circuit with B&C



All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#, PWROK) must either pull up to VccRTC or pulled down to ground while in G3 for preventing from floating in G3 and will prevent IccRTC leakage that can cause excessive coin-cell drain.

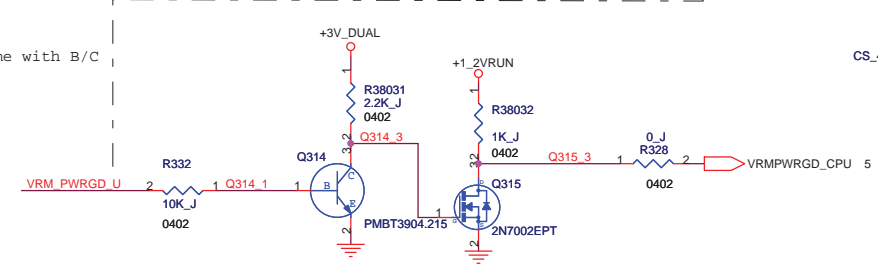
for reset issue when testing place near ICH10

For corwin spring

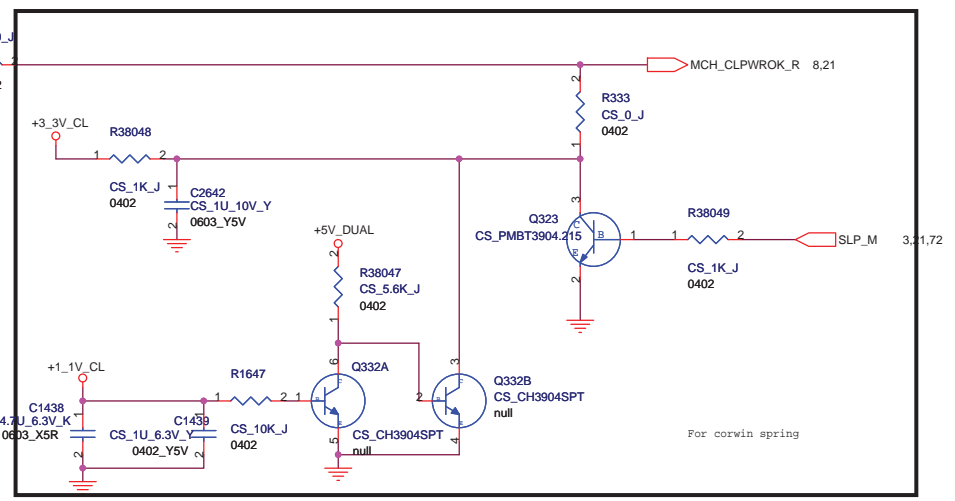


6/6 unify sequence circuit with B&C

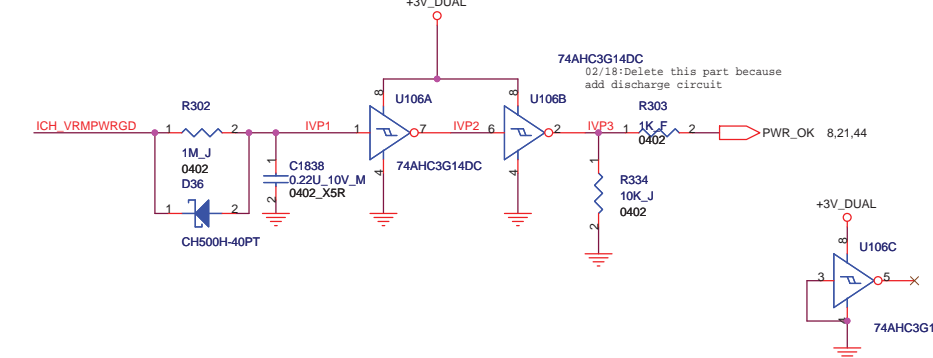
03/11 Change this circuit to keep same with B/C



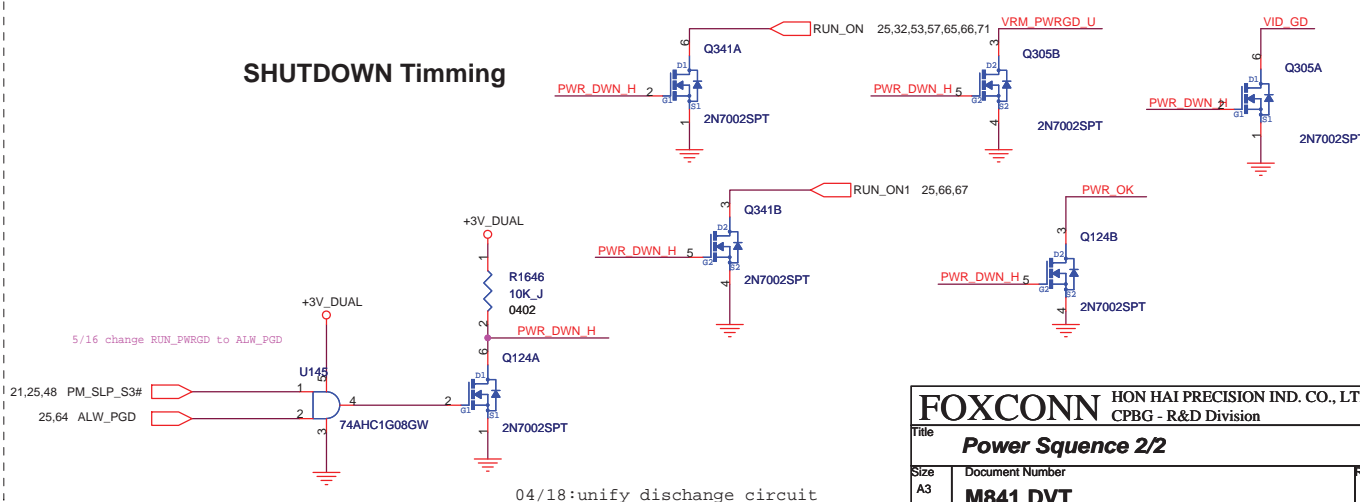
RUN_PWRGD --> VID_GD



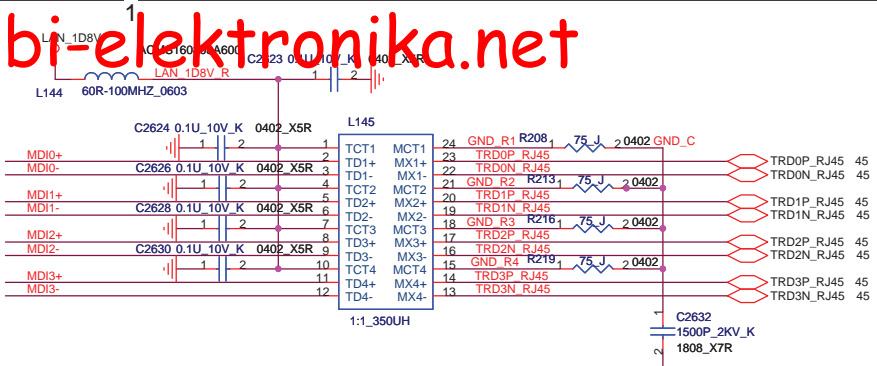
VRMPWRGD --> PWR_OK



SHUTDOWN Timing

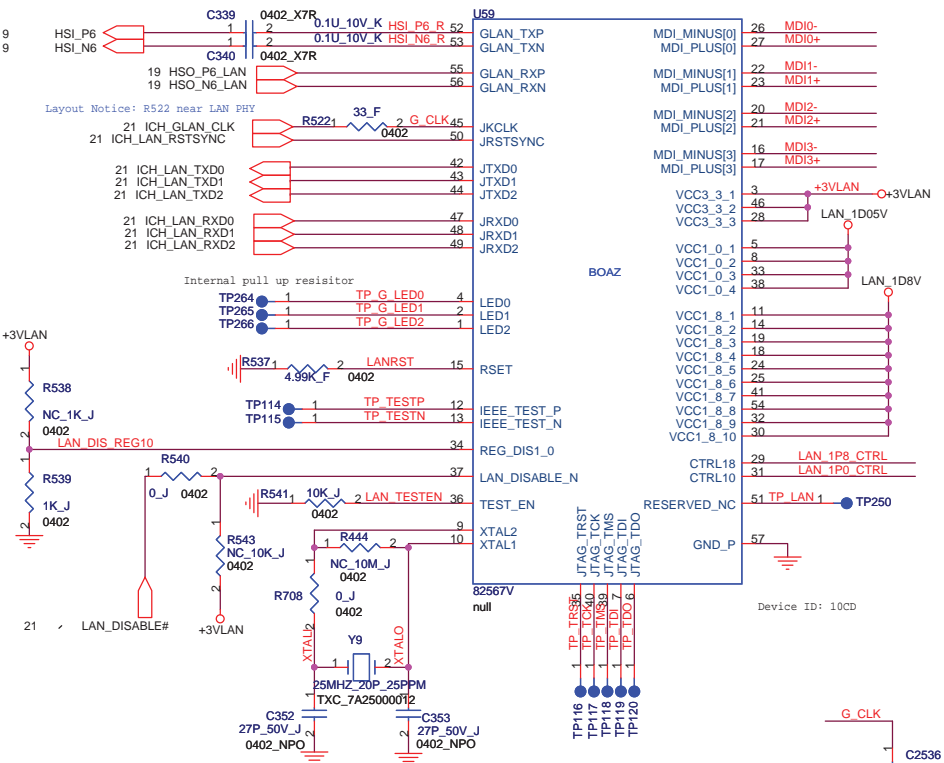


In 1000 Mb/s mode, JKCLK frequency is 62.5 MHz.
 In 100 Mb/s mode, JKCLK frequency is 50 MHz.
 In 10 Mb/s mode, JKCLK frequency is 5 MHz.
 In power down mode, JKCLK frequency is 0 MHz.



9/12 L145 main source change 1T-INS6824-0300 to 1T-130F50L-0000(height:2.9mm),second source 1T-130F500-0000(height:2.5mm)

Pls split a ground plane beneath the magnetics module(L61).



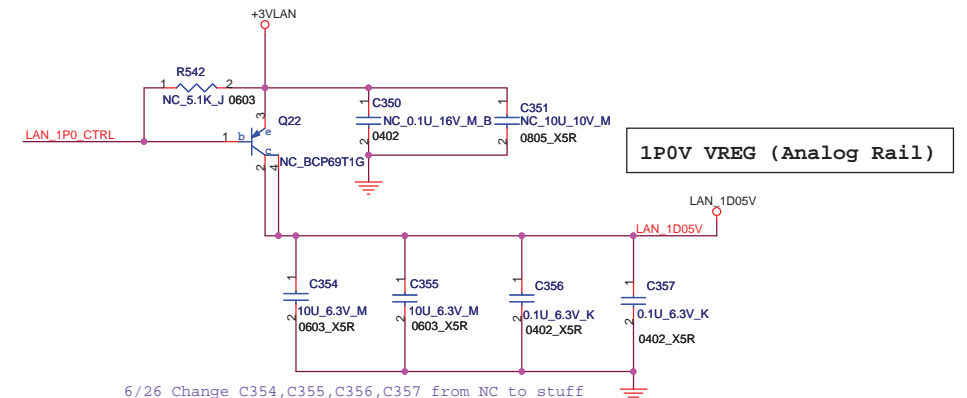
Layout Notice: R522 near LAN PHY

Internal pull up resistor

LAN DIS REG10

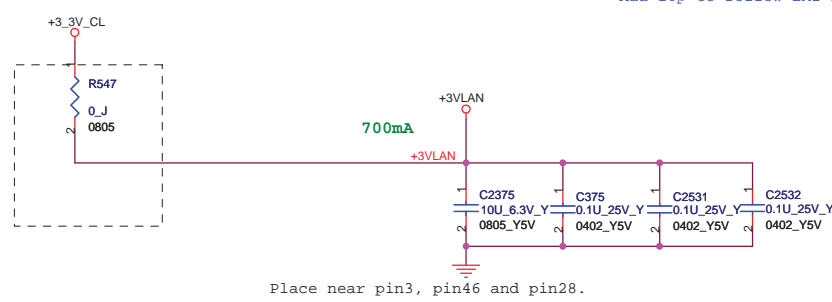
LAN_DISABLE#

0103
Add 10p to follow EMI suggest



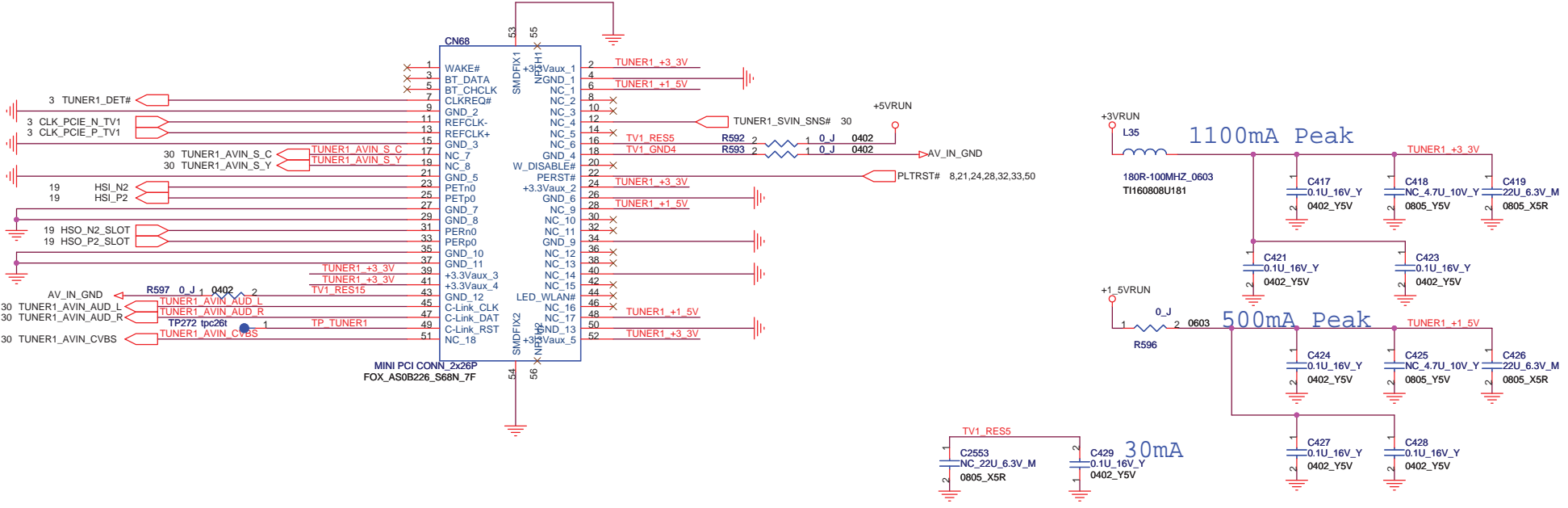
6/26 Change C354,C355,C356,C357 from NC to stuff

Close to chip

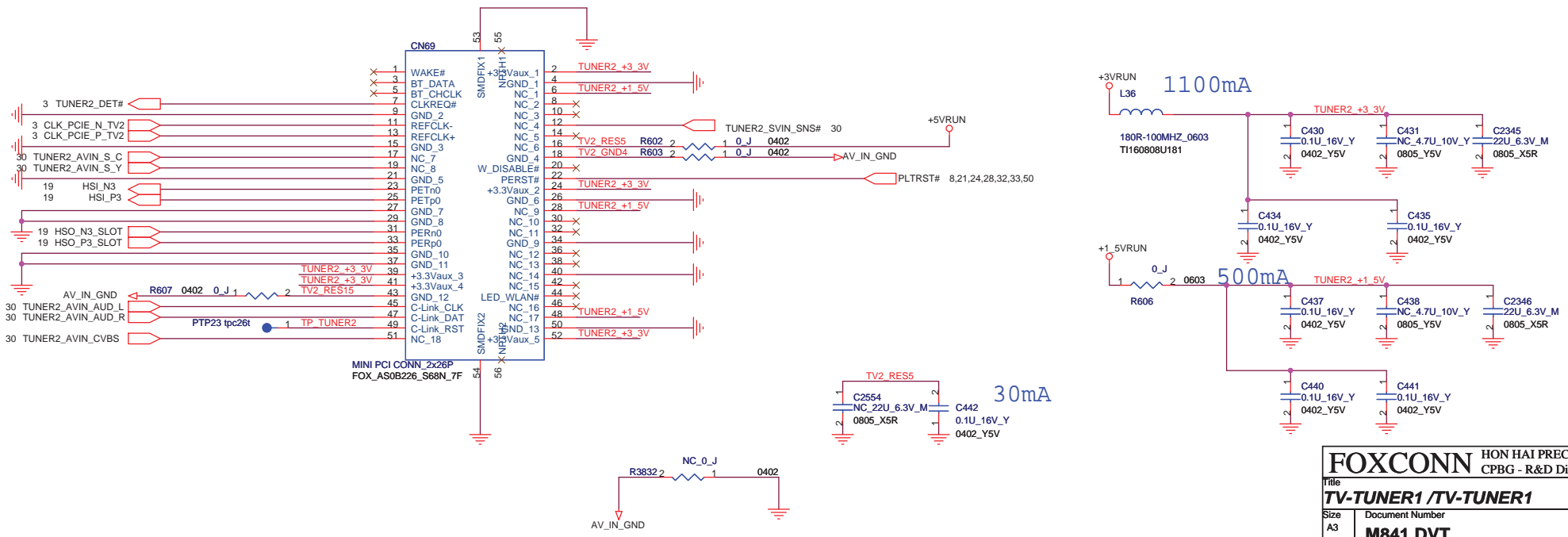


Place near pin3, pin46 and pin28.

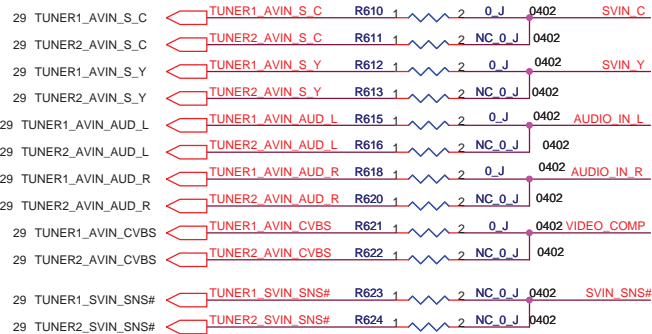
Mini-PCIE TUNER1 connector



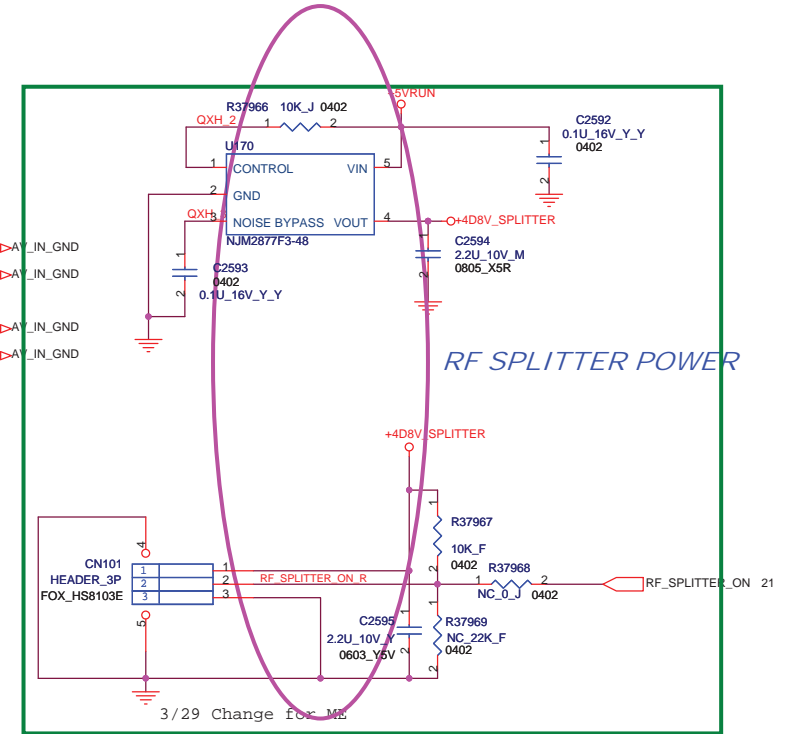
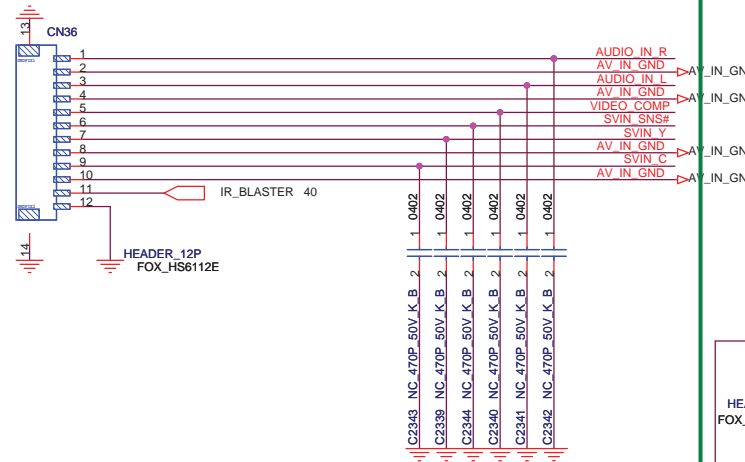
Mini-PCIE TUNER2 connector



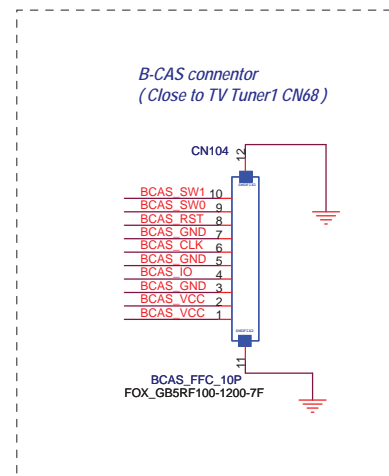
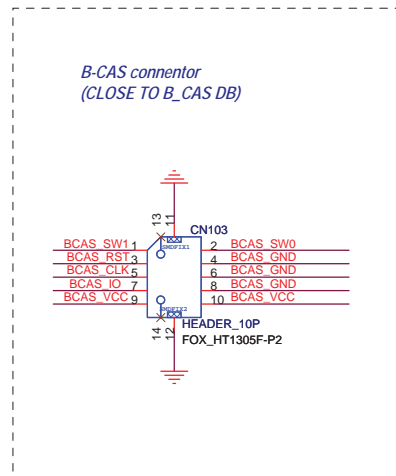
9/12 Change this circuit from NC to stuff for EU TV tuner evaluation



AV_IN/SVIDEO IN/RF Splitter Power

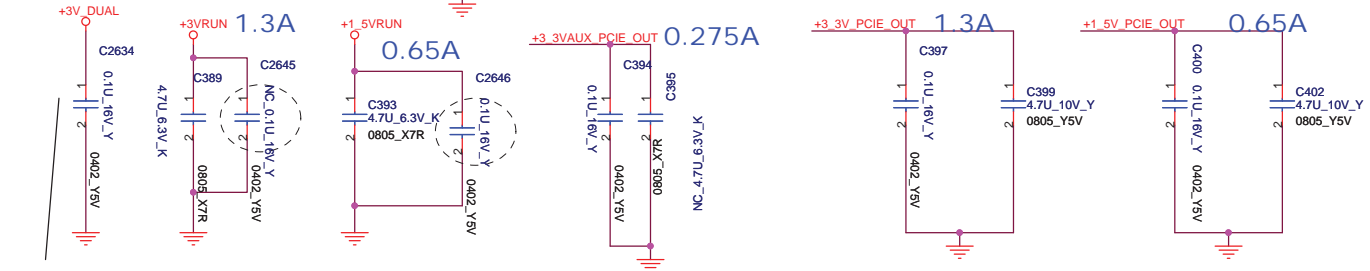
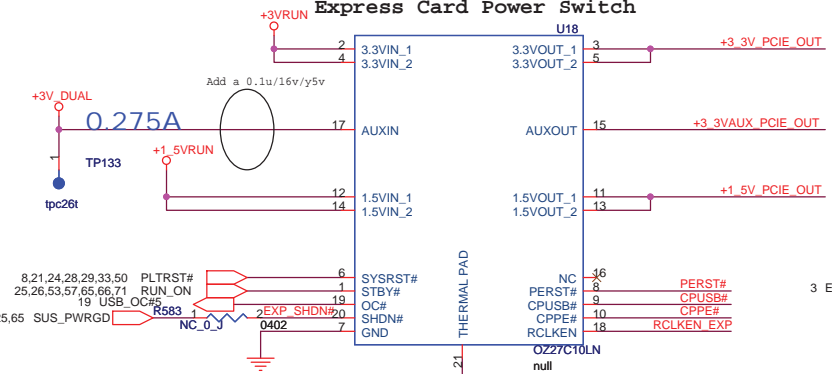


3/29 Change for ML



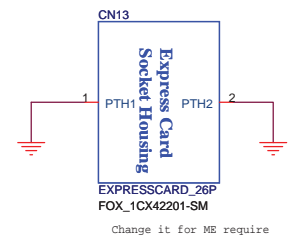
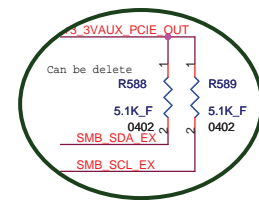
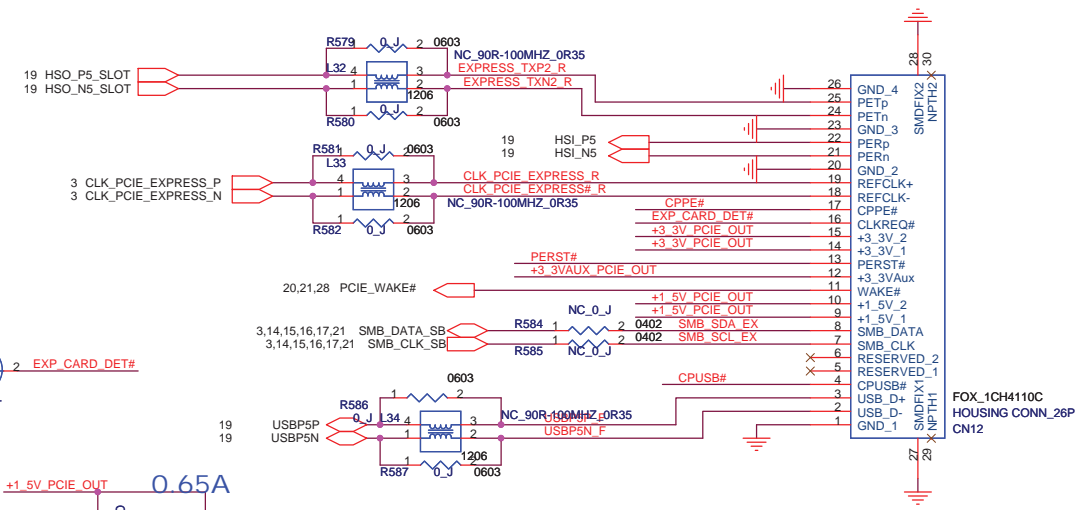
	VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
	AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	1	GND	GND	GND	No Card
On	On	On	1	0	0	0	On	Off	Off	Standby
On	On	On	1	1	0	0	On	On	On	Card Inserted

Express Card Power Switch

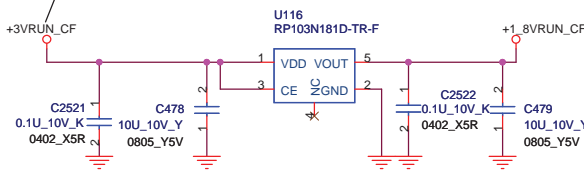


CLOSE U18 PIN 17

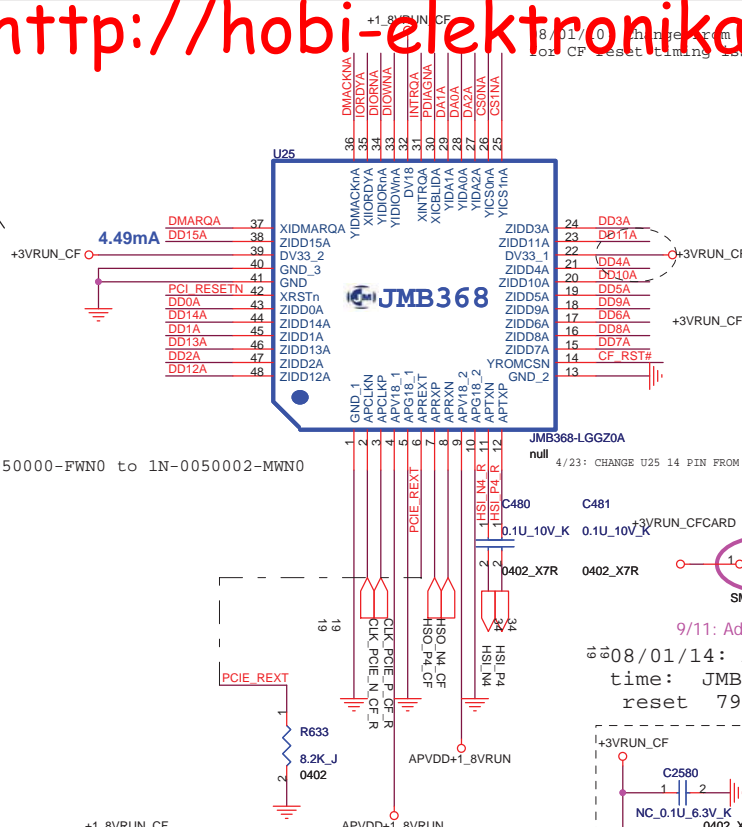
4/28
We add C2645 C2646 base on ShiBa Sche.



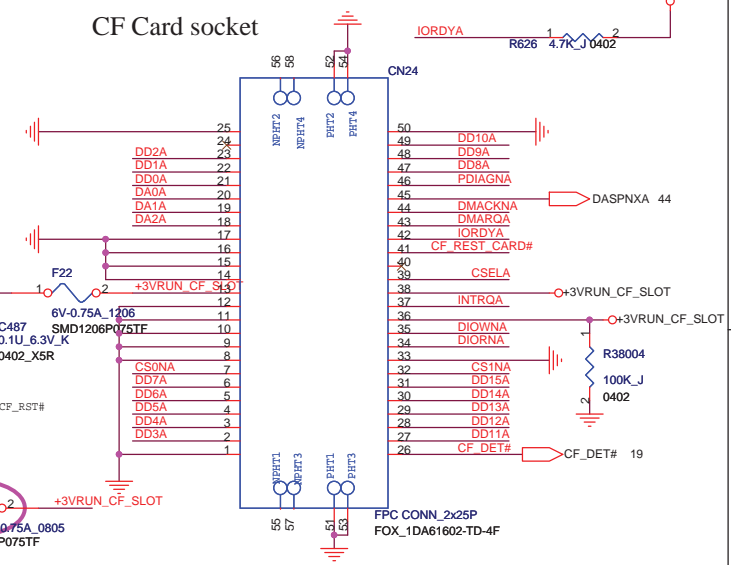
08/01/10: Change from +3VRUN power to +3VRUN_CF power for CF reset timing issue.



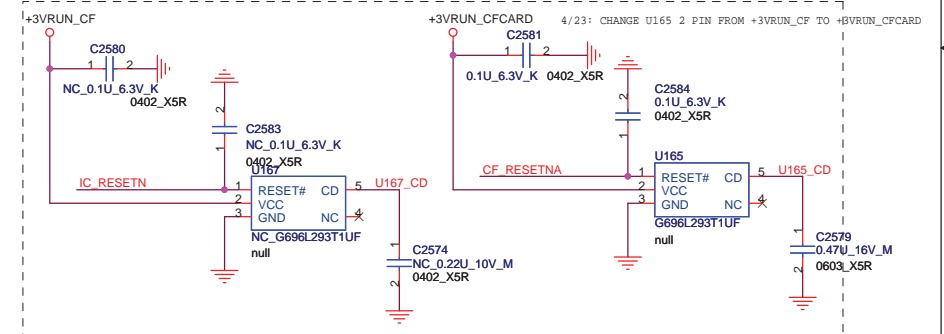
P21: Change CN24 from 1N-0050000-FWN0 to 1N-0050002-MWN0



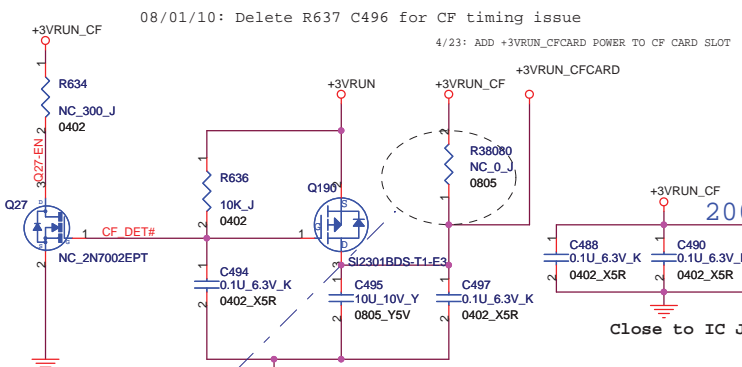
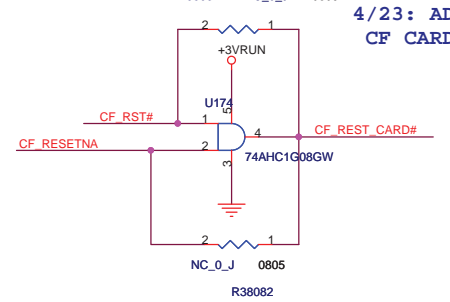
CF Card socket



08/01/14: Add those two RESET IC to control the delay time: JMB368 reset 370ms after CF CARD inset, CF CARD reset 792ms after JMB368 reset.

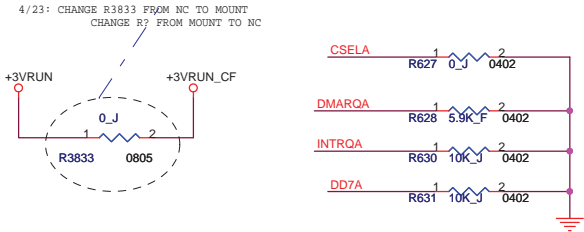


4/23: ADD THIS CIRCUIT FOR CF CARD RESET

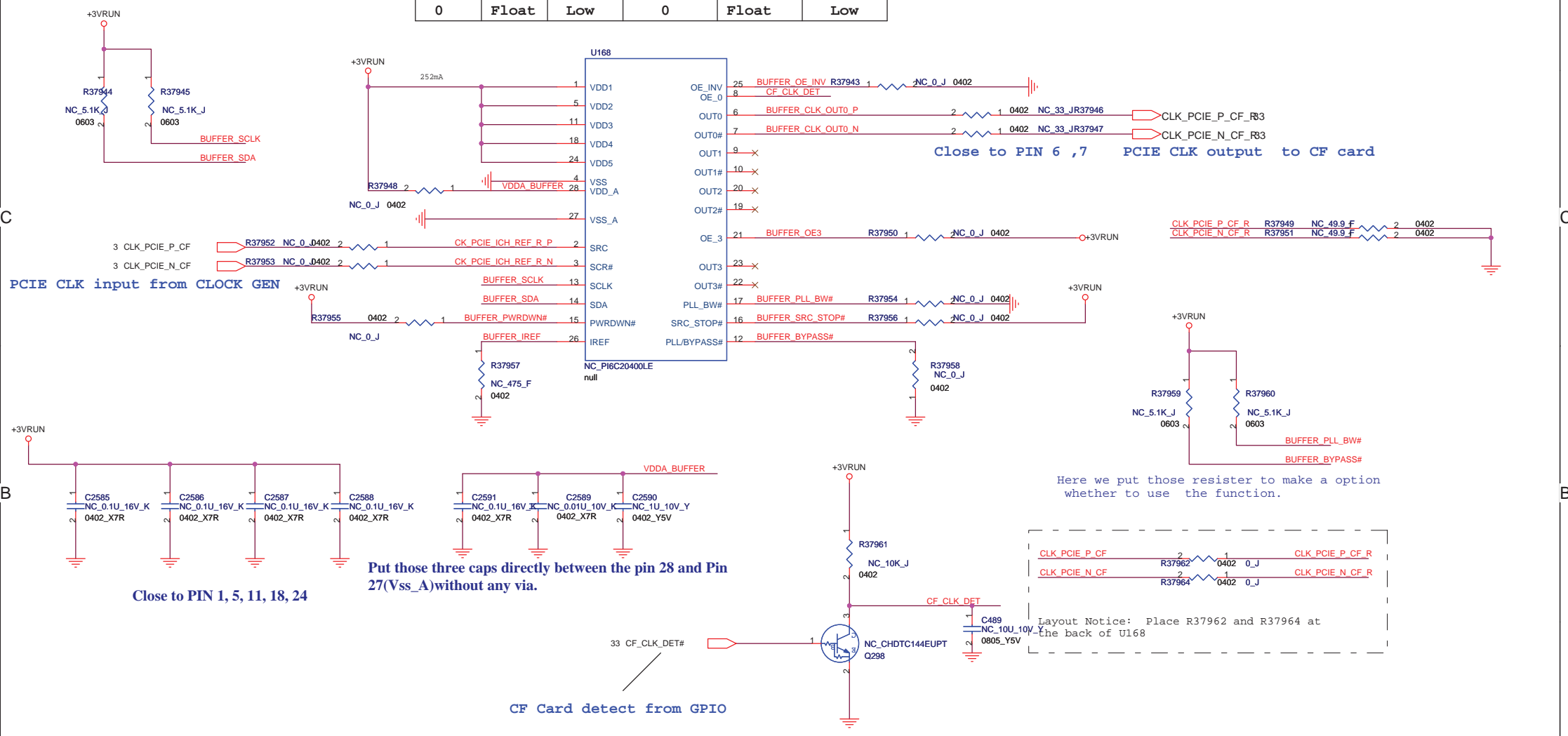


CompactFlash power circuit

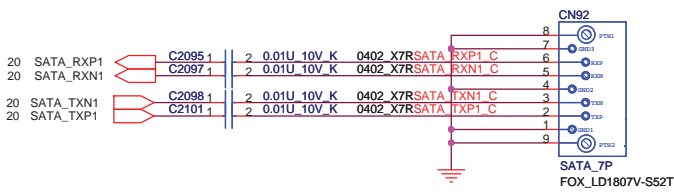
Here we make a option if JMB368 is NOT powered ON without CF media.



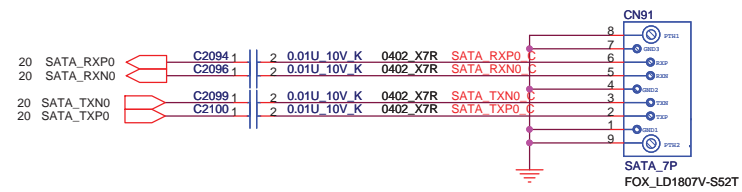
PWRDWN#	OUT	OUT#	SRC_STOP#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	Float	Low	0	Float	Low



HDD2

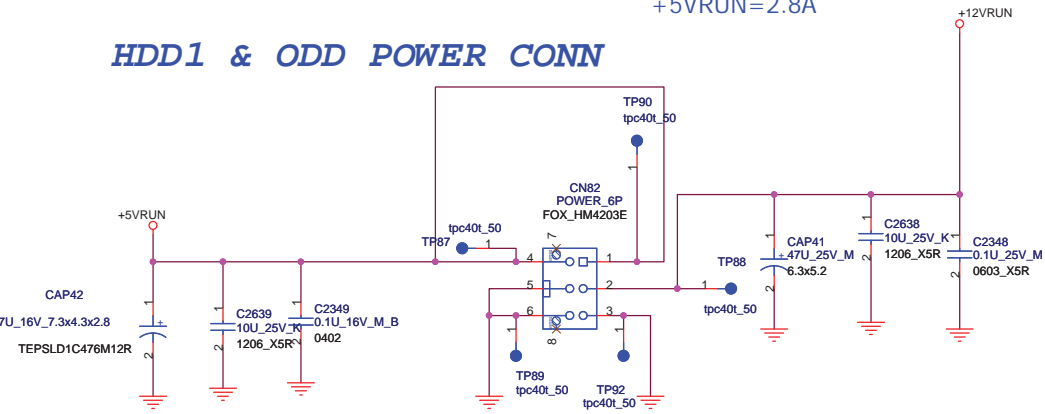


HDD1



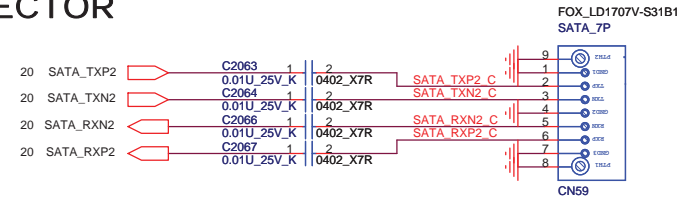
HDD1 & ODD POWER CONN

Power Budget
 +12VRUN=4A, PEAK,4SECONDS
 +5VRUN=2.8A



4/28 :change pin 2 from +12VRUN to GND, chane pin 5 from GND to +5VRUN

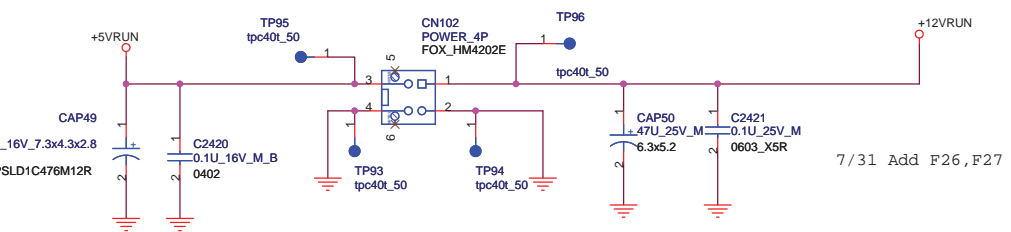
SATA ODD CONNECTOR



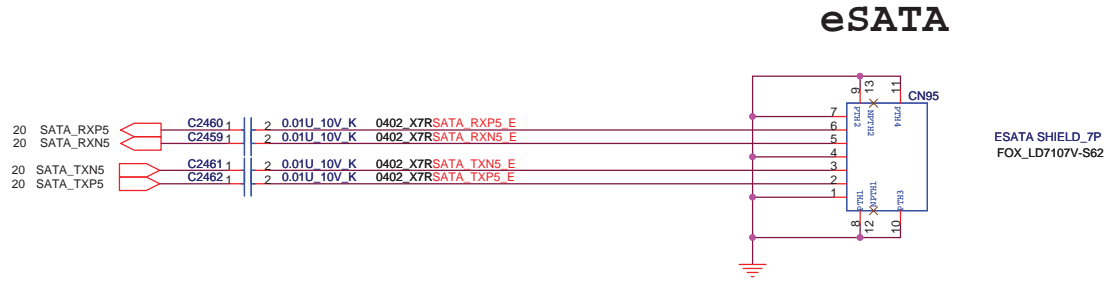
SATA ODD and SATA HDD share the same POWER CONN.

HDD2 POWER CONN

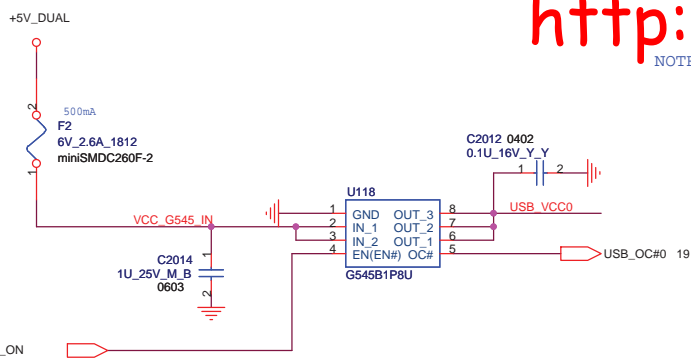
Power Budget
 +12VRUN=4A, PEAK,4SECONDS
 +5VRUN=0.8A



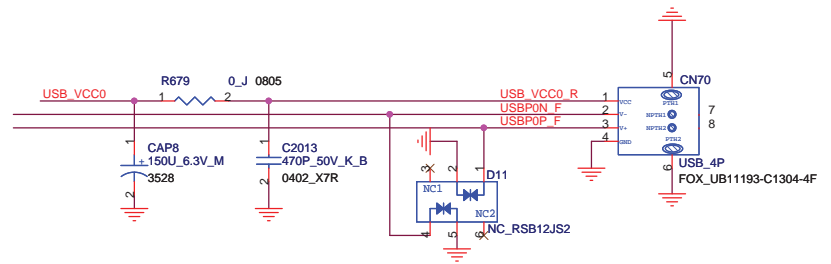
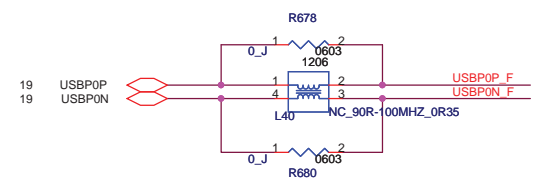
7/31 Add F26, F27



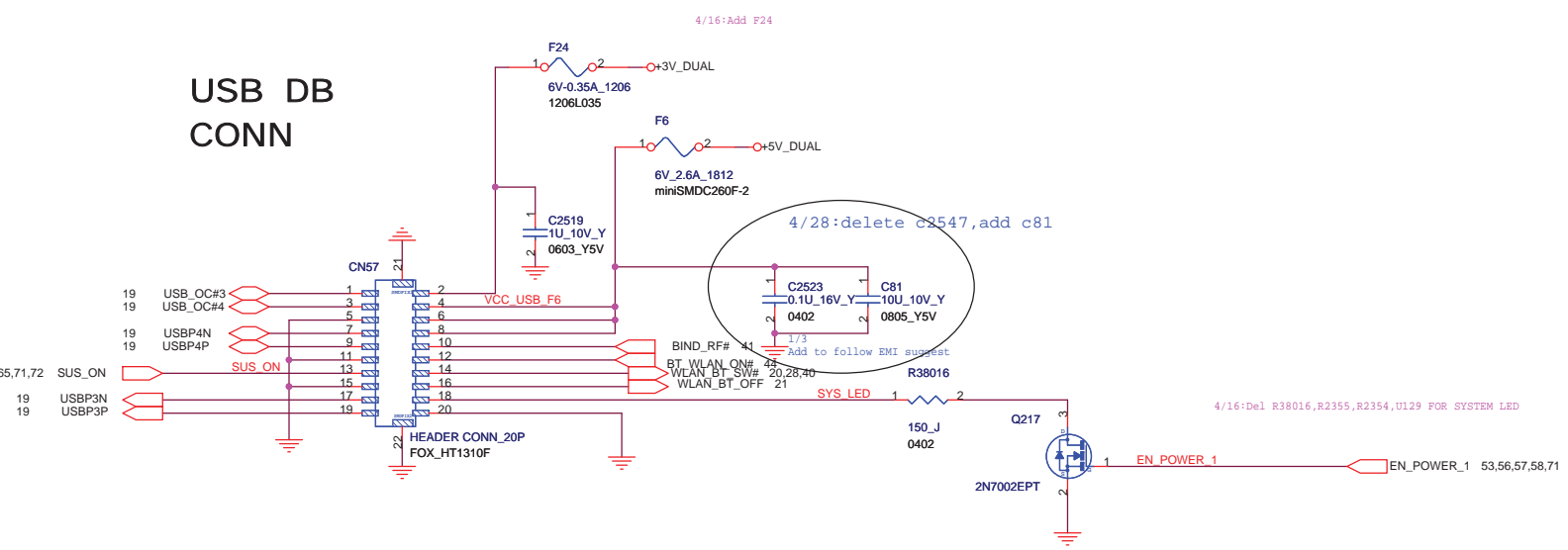
NOTE: S0, S1, S3



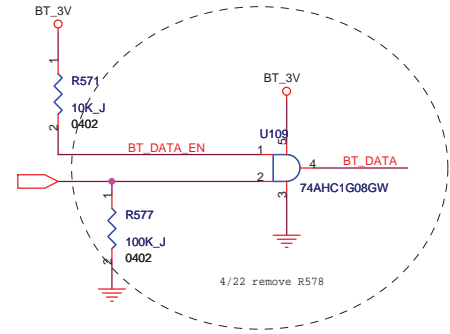
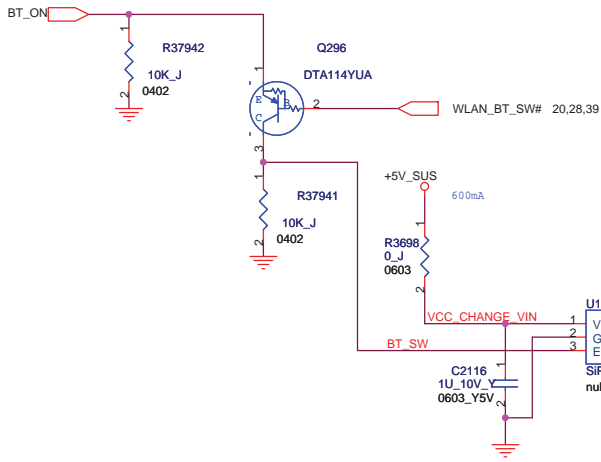
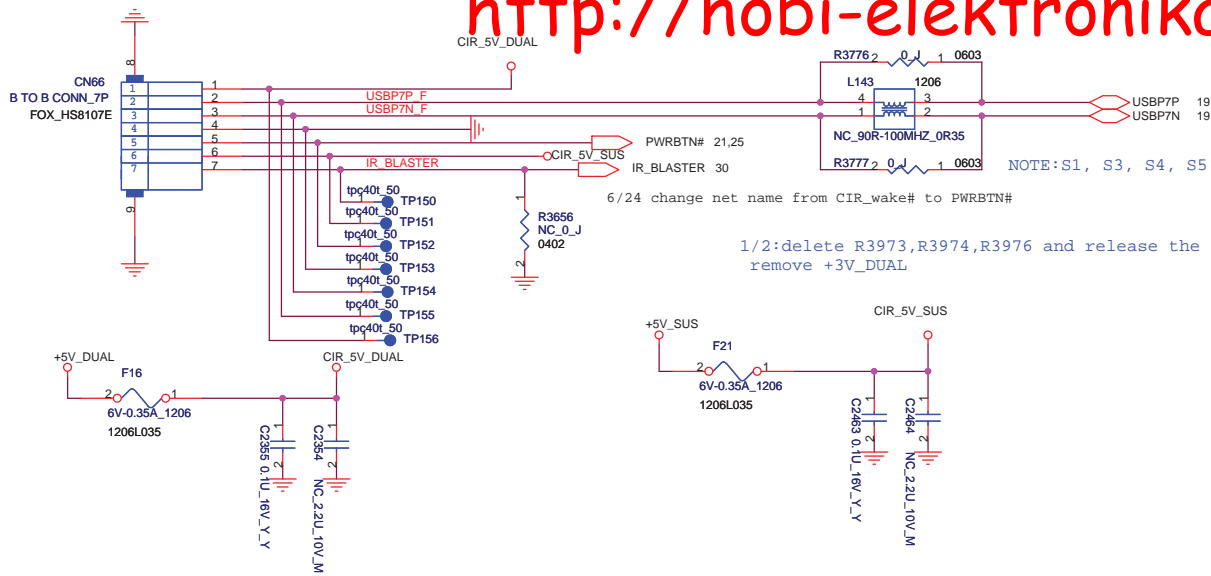
USB Port on Board



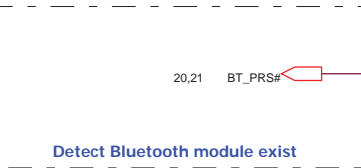
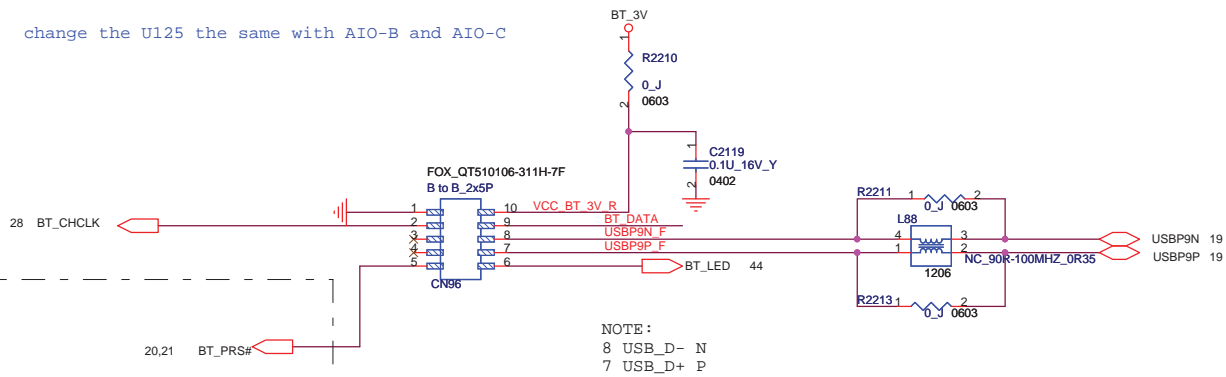
USB DB CONN



CIR



change the U125 the same with AIO-B and AIO-C

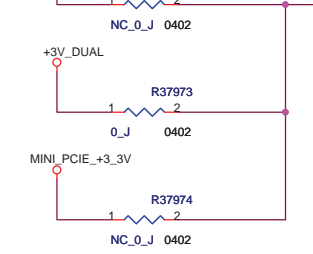


Bluetooth connector

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title CIR&BT	
Size A3	Document Number M841 DVT
Date: Saturday, September 13, 2008	Rev 0.1
Sheet 40	of 77

INVERTER

SPS

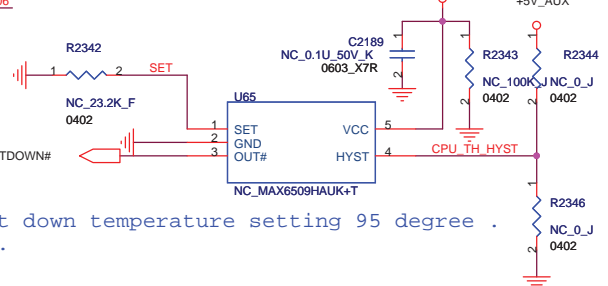


caps C2182, C2184 and C2186, 2200pF is 470pF would be a good value and be placed close to the EMC2106 pins

NOTE:PWM4 configurations for PWM4 as backlight control
 - set Reg0E0h B[6:5]="11b" to select pin5 as PWM4
 - config Reg2Bh B[7:6] to select PWM4 base freq
 - config Reg2Fh for PWM4 Divide for exact freq
 - set Reg2Eh for PWM4 duty cycle
 SHDN_SEL (pin22) and SYS_SHDN# (pin 9), you may leave them as NC

2007/12/31
 delete R2355/R2336/R2357/R3341 10K resistor

HW THERMAL PROTECTION



HW thermal shut down temperature setting 95 degree .
 Put Near CPU .

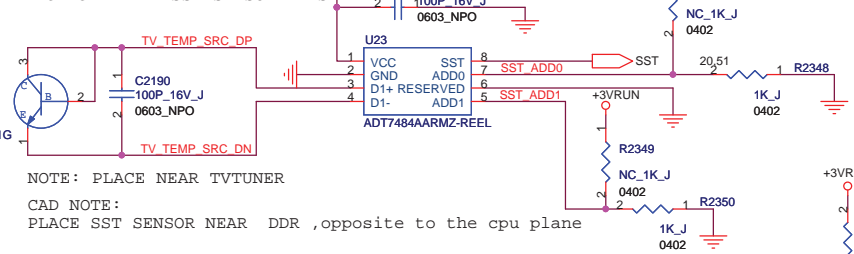
PIN1 SET:Temperature Set Point. Connect an external 1% resistor from SET to GND to set trip point.
 To set the temperature trip point from 0°C to +125°C, use the following equation:
 $RSET = [(8.3793 \cdot 104) / T] - 211.3569 + [(1.2989 \cdot 105) / T2] = 289k$
 where T is the trip temperature in Kelvin.

The THRM# signal is used as a status input for a thermal sensor. Based on the THRM# signal going active, the ICH10 generates an SMI# or SCI (depending on SCI_EN).

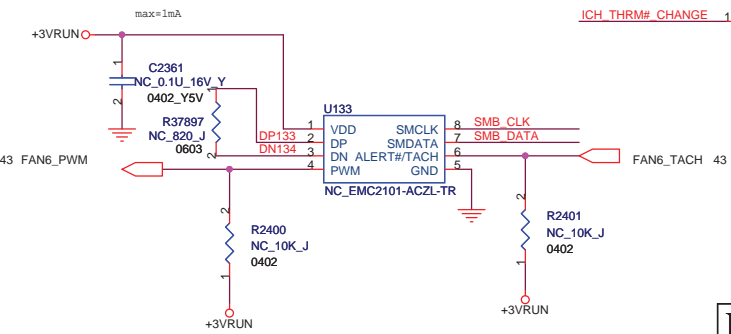
DDR & TVTUNERTEMP SENSOR Address
 ADD0 ADD1 0x48
 MXM THERMAL SENSOR ADDRESS
 ADD1 ADD0 ADDRESS
 FLOAT HIGH OX4D

DESIGN NOTE:
 DDR & TVTUNERTEMP SENSOR

CAD NOTE:
 PLACE CAP NEAR SST SENSOR PINS

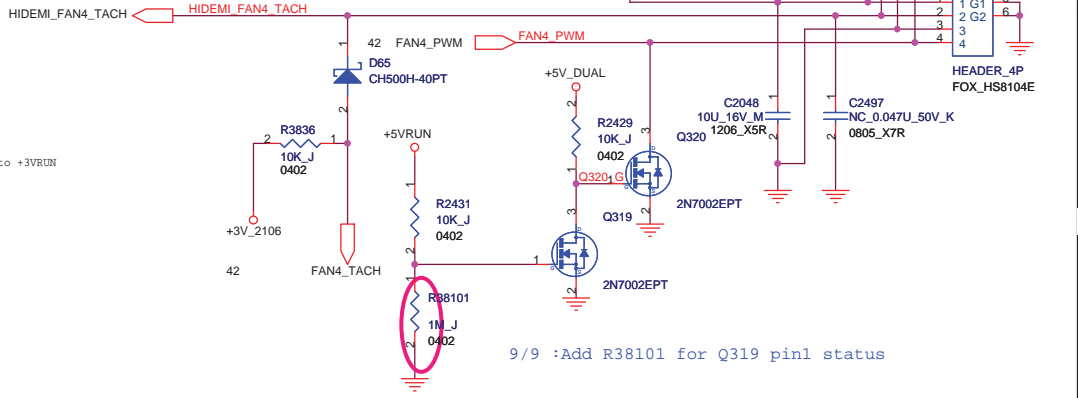
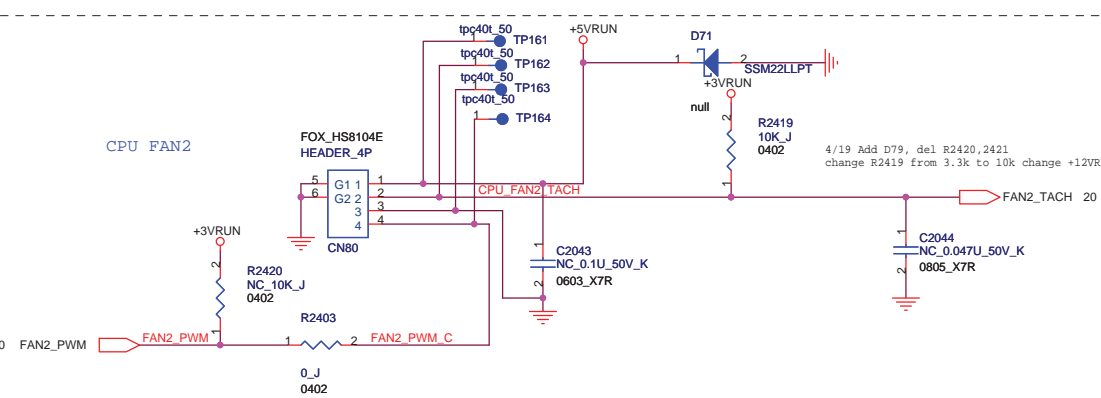
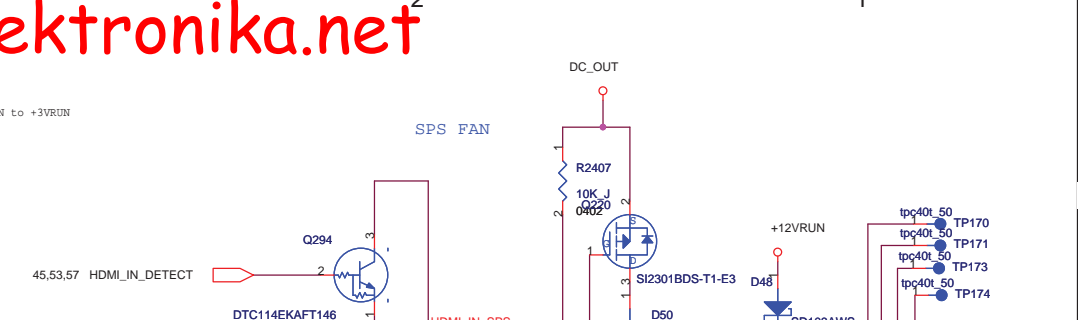
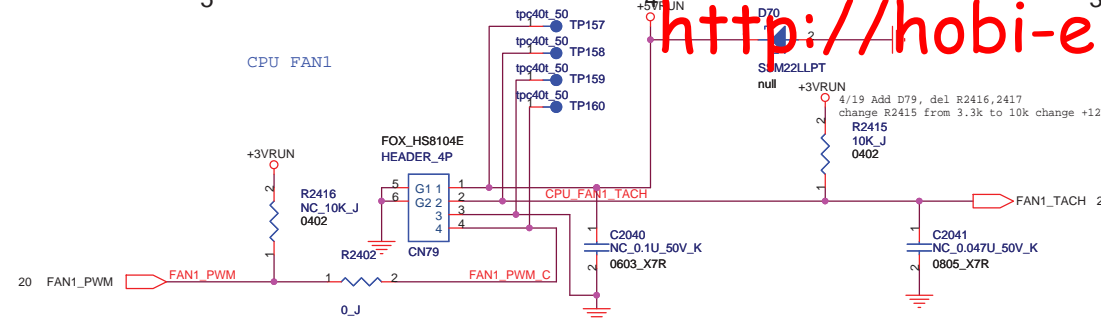


NOTE: PLACE NEAR TVTUNER
 PLACE SST SENSOR NEAR DDR ,opposite to the cpu plane

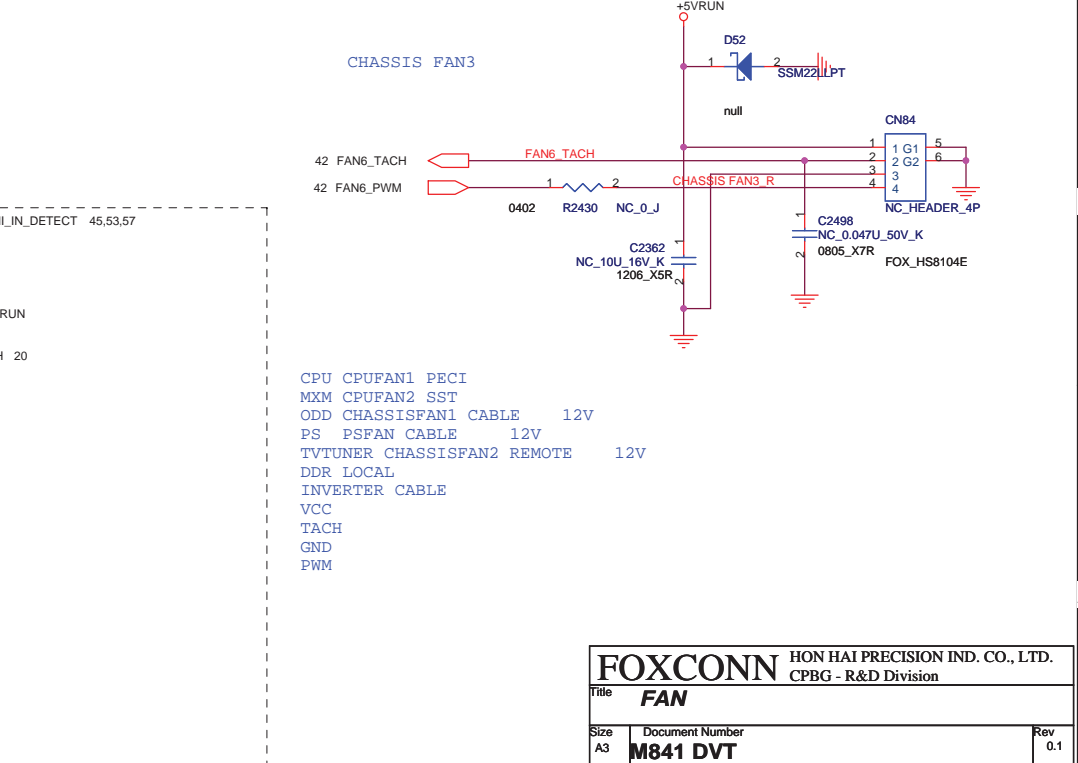
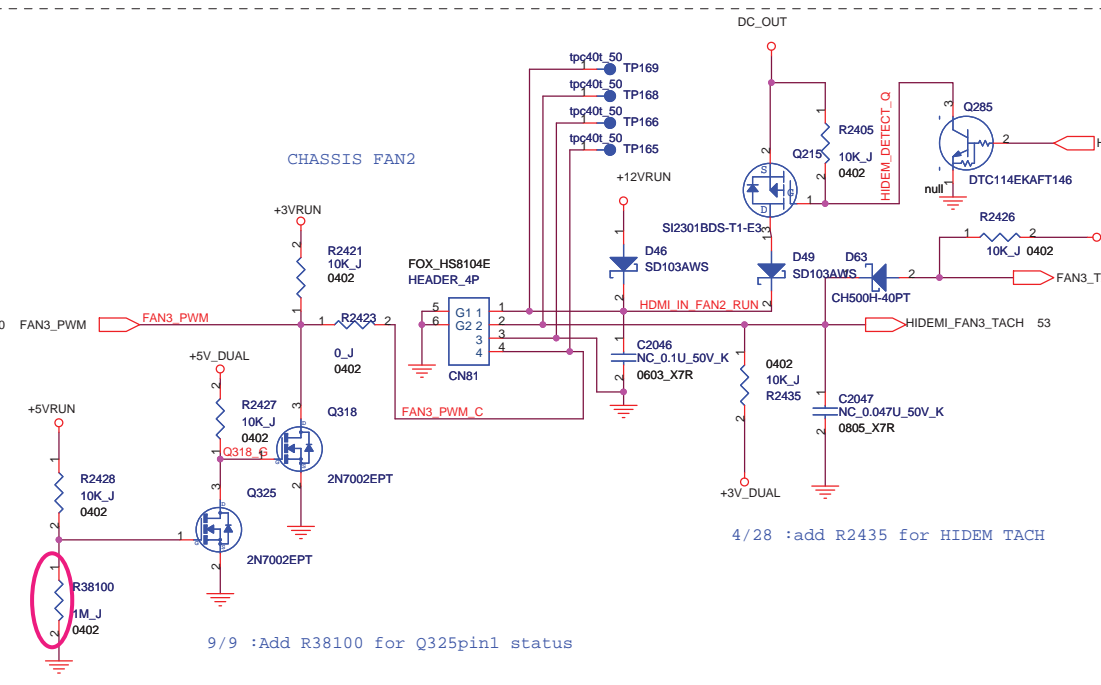


The EMC2101 is addressed on the SMBus as 100_1100b.

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title: Thermal & BL			
Size A3	Document Number	Rev 0.1	
	M841 DVT		
Date:	Saturday, September 13, 2008	Sheet	42 of 77

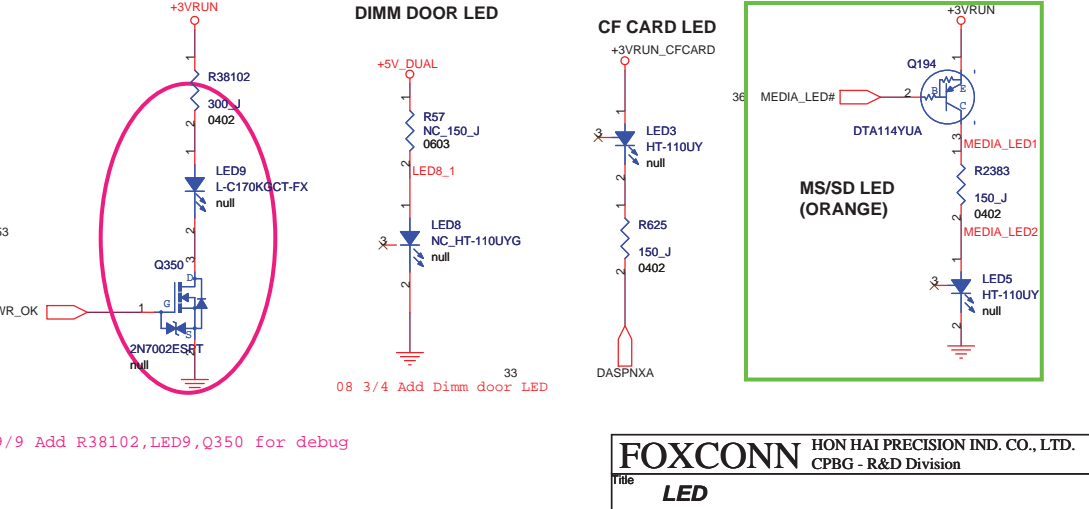
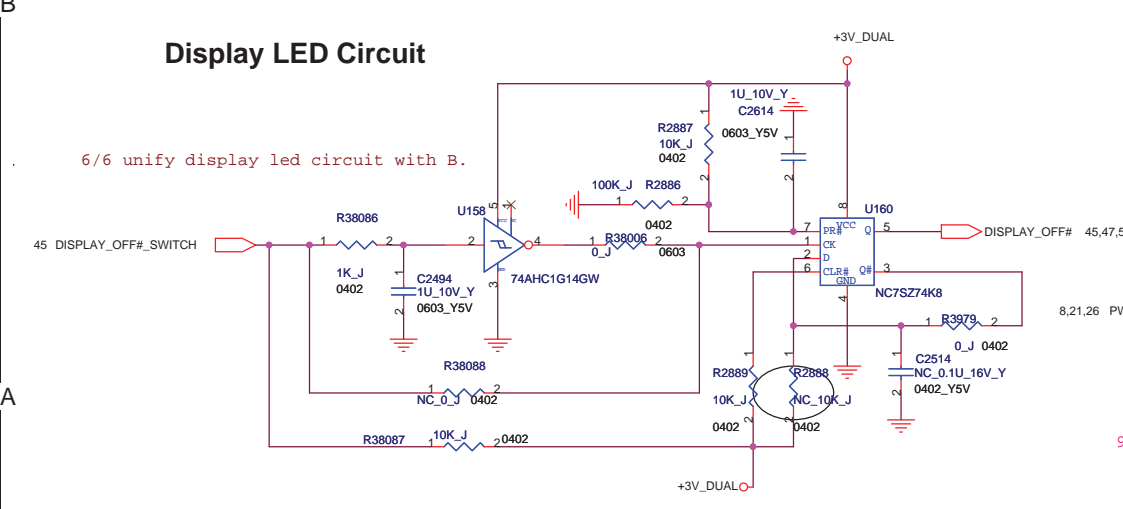
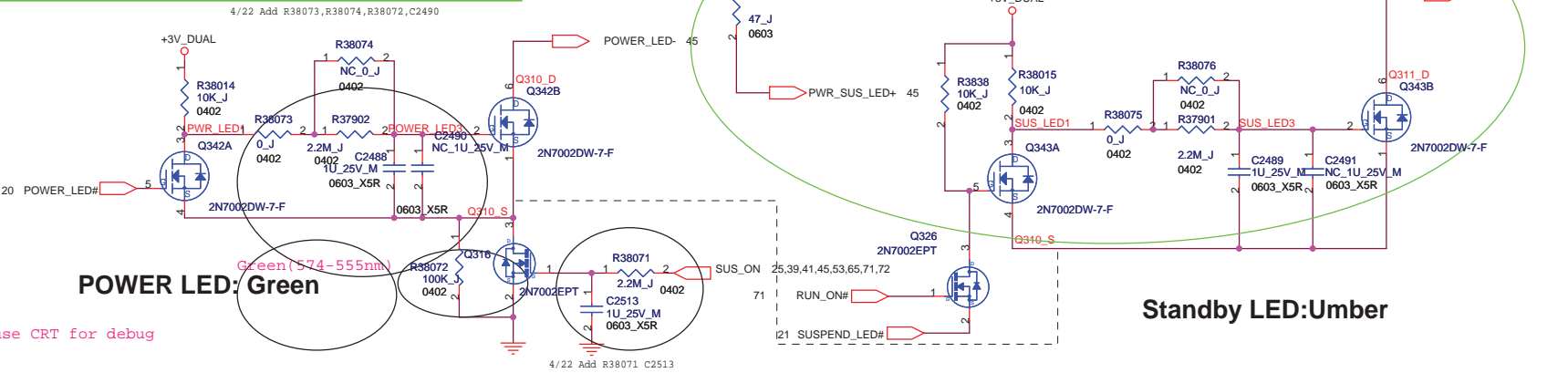
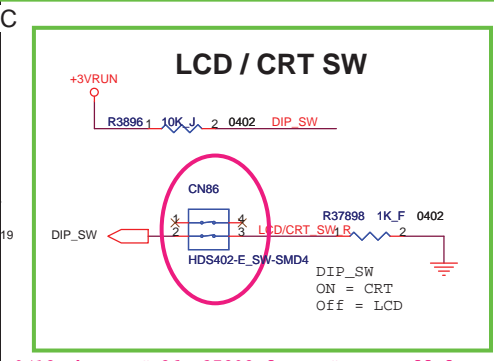
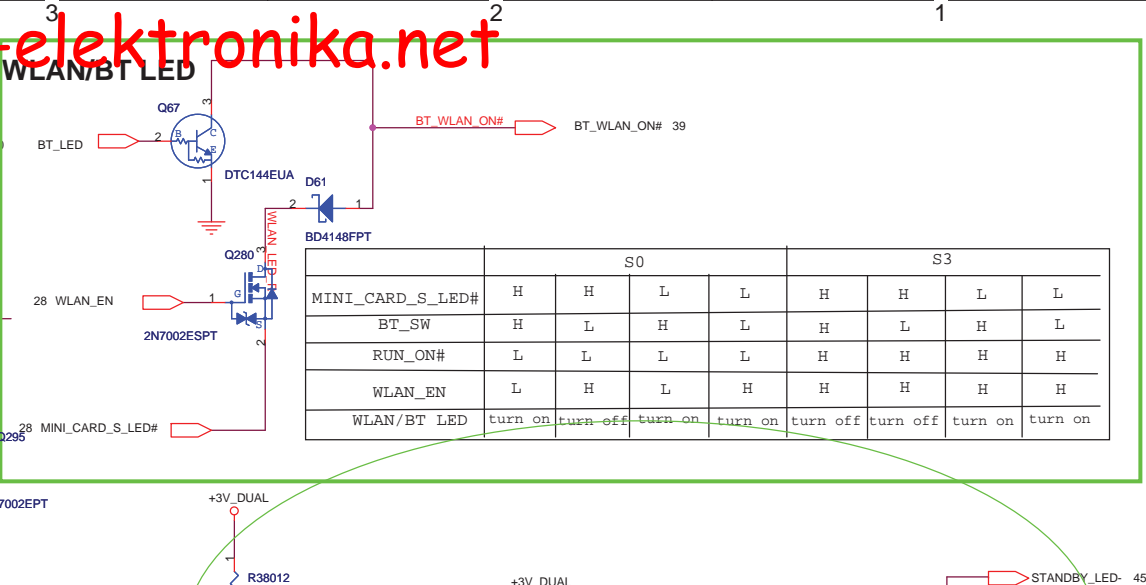
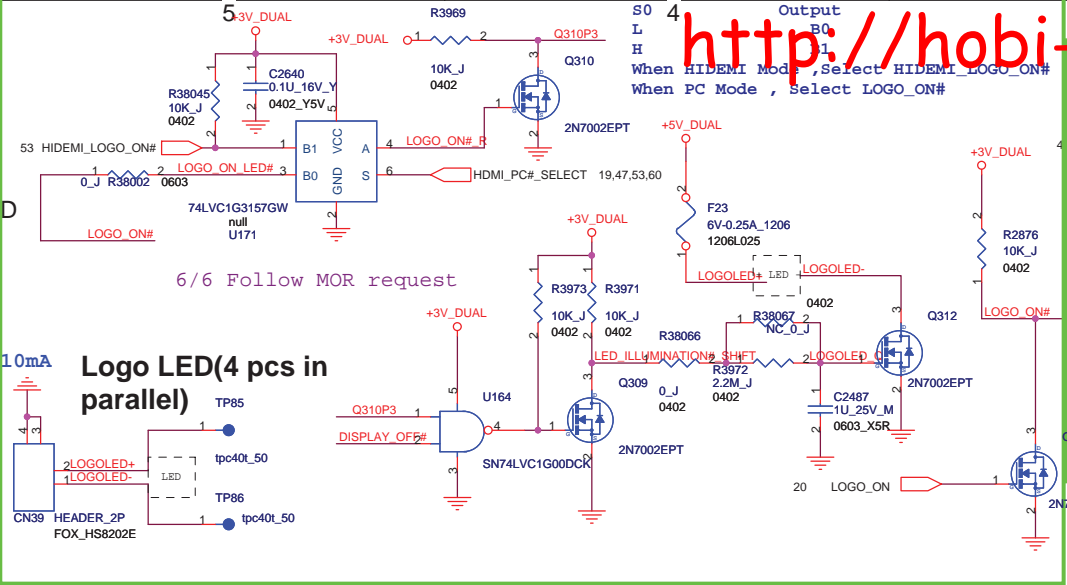


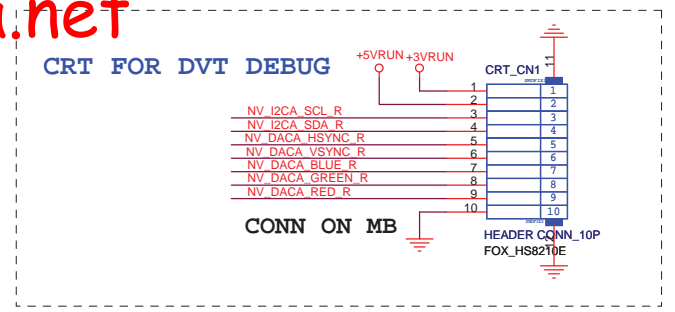
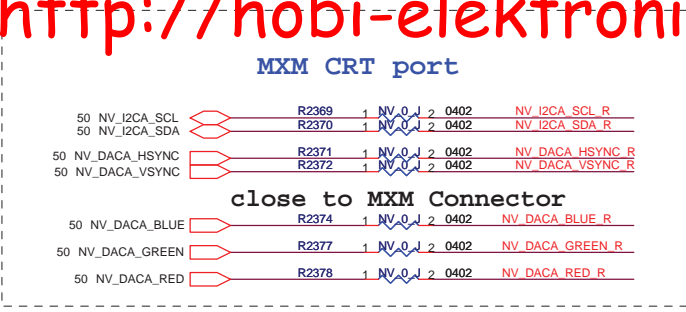
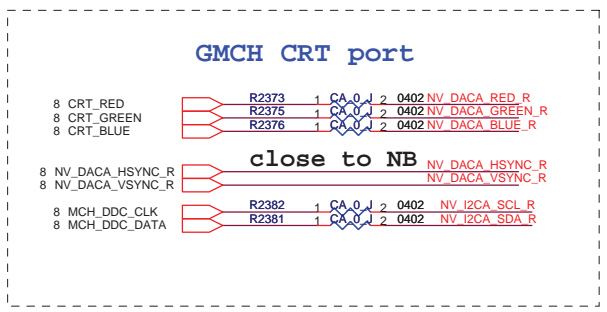
http://www.fangyuannb.com http://shop63900485.taobao.com



- CPU CPUFAN1 PECE
- MXM CPUFAN2 SST
- ODD CHASSISFAN1 CABLE 12V
- PS PSFAN CABLE 12V
- TVTUNER CHASSISFAN2 REMOTE 12V
- DDR LOCAL
- INVERTER CABLE
- VCC
- TACH
- GND
- PWM

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Title	FAN
Size	Document Number
A3	M841 DVT
Date:	Wednesday, September 17, 2008 Sheet 43 of 77
Rev	0.1





Change history of VGA portion from page 46 to page 53 (base on M840 MP)

DVT

0821

1, Stuff CRT

2, Change NV_thermal_alert connect from AC_OFF_3# to ICH_H_THERMTRIP#

0909

1, Change CN53 pin assignment for HIDE MI, change pin 14 from GND to SUS_ON; change Pin 18 from GND to INV_BRADJ; change Pin 40 from TP to INV_ENABLE1; change Pin 39 from GND to HIDE MI_DETECT; Add R38108 1M ohm for HIDE MI_DETECT PD.

2, change page 46 LVDS SW selector from HDMI_PC#_SELECT to HIDE MI_DETECT

0911

1, Page 53 add Back up circuit for HIDE MI2 compatibility with HIDE MI 1 FW.

2, CN53 change Pin 32 from gnd to LCDVCC_EN;

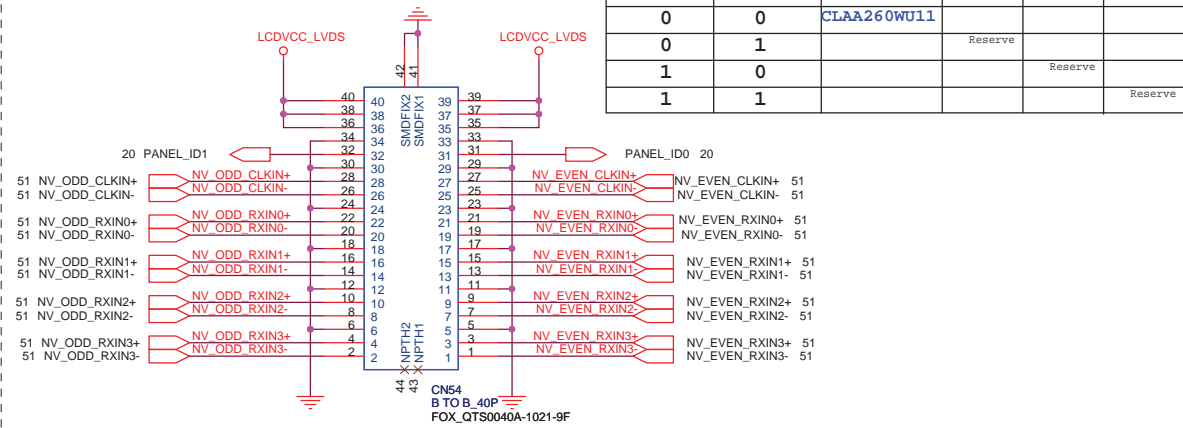
0912

1, Add a AND gate for HIDE MI_SUS_ON;

2, Change the signal net name from HIDE MI_DETECT to HIDE MI_EXIST and HIDE MI_DETECT_CN to HIDE MI_EXIST_CN;

3, Add back up RUN_ON signal to HIDE MI;

LVDS

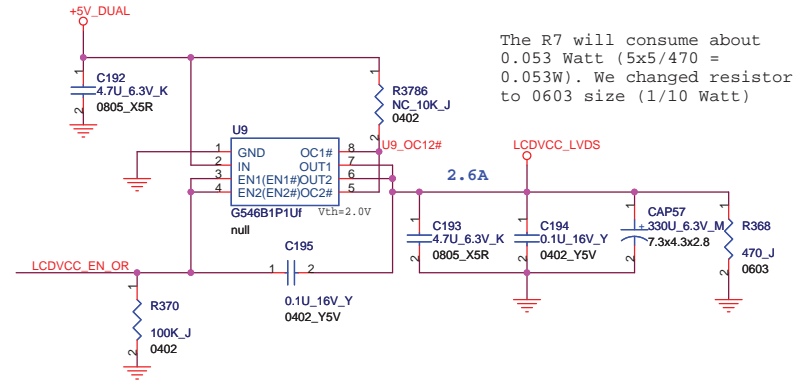


LVDS CONNECTOR

M840_26' Panel ID Table

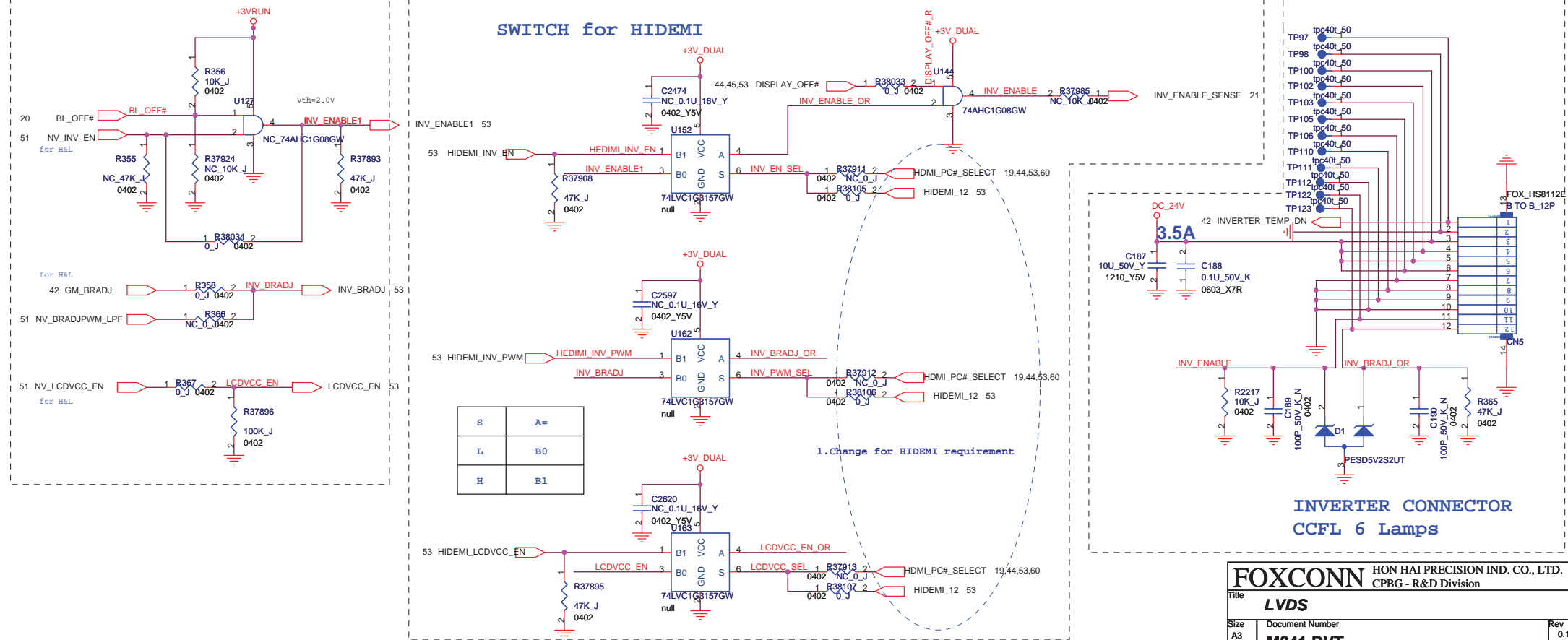
PANEL_ID1	PANEL_ID0	Type 1	Type 2	Type 3	Type 4
0	0	CLAA260WU11			
0	1		Reserve		
1	0			Reserve	
1	1				Reserve

LCD POWER LATCH



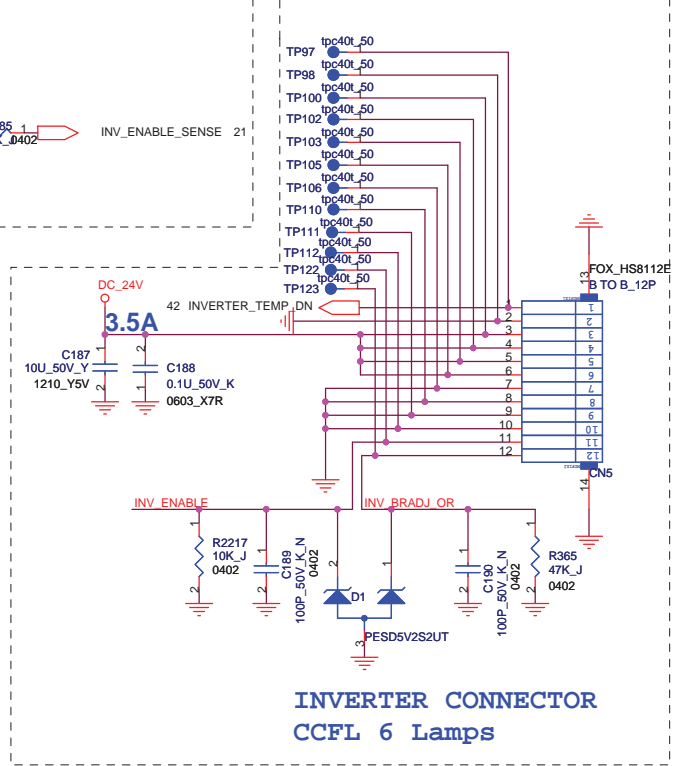
The R7 will consume about 0.053 Watt ($5 \times 5 / 470 = 0.053W$). We changed resistor to 0603 size (1/10 Watt)

SWITCH for HIDEEMI



1. Change for HIDEEMI requirement

INVERTER CONNECTOR CCFL 6 Lamps

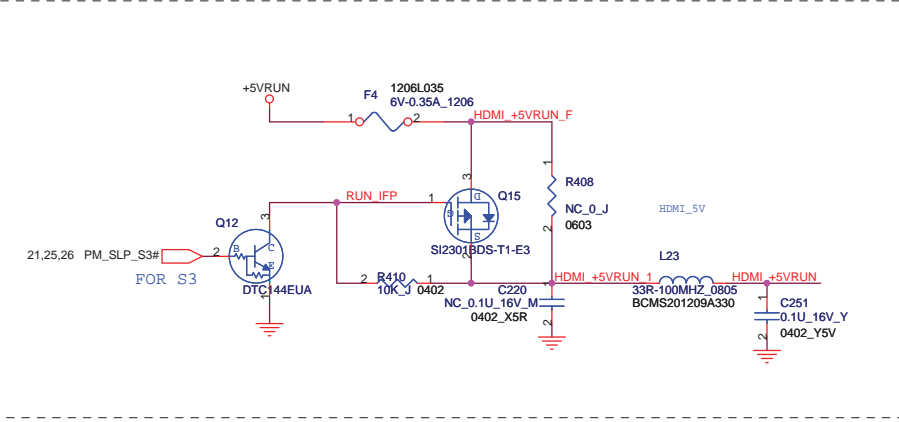
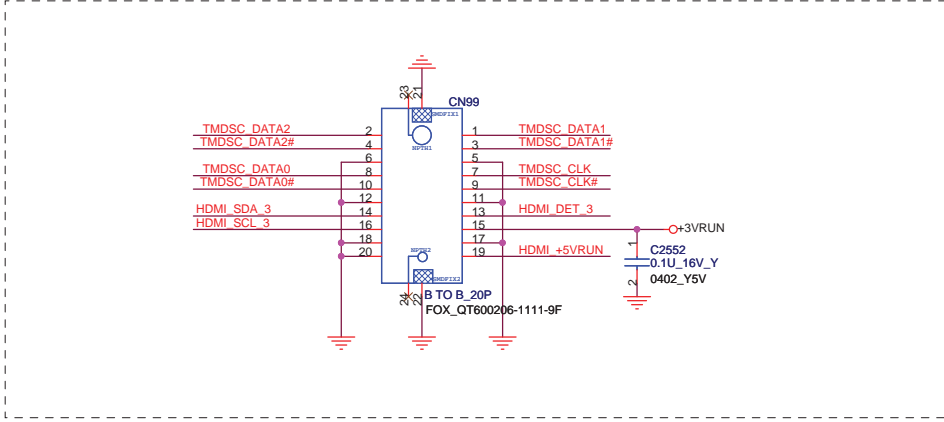
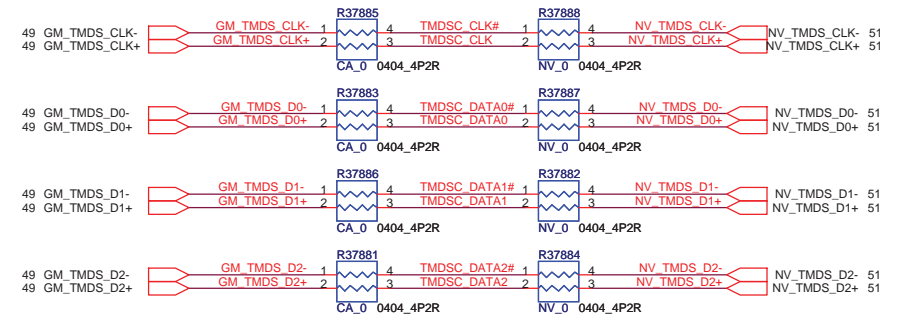
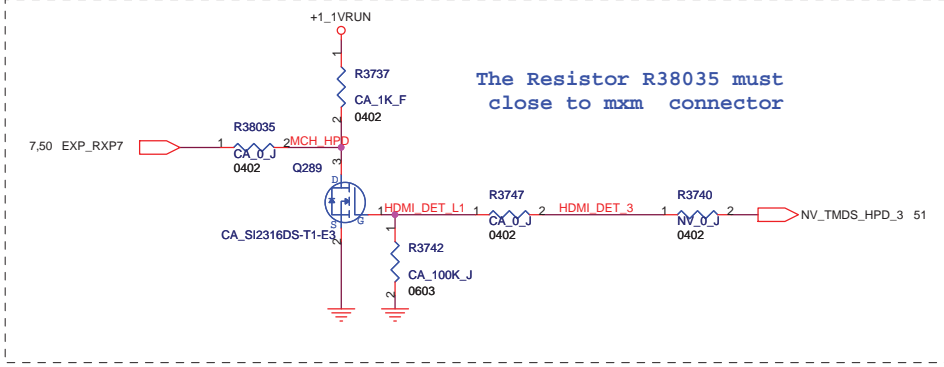
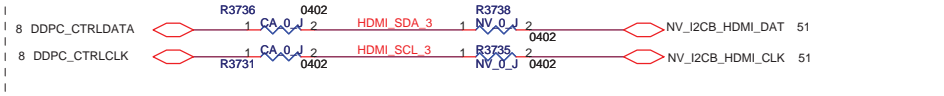


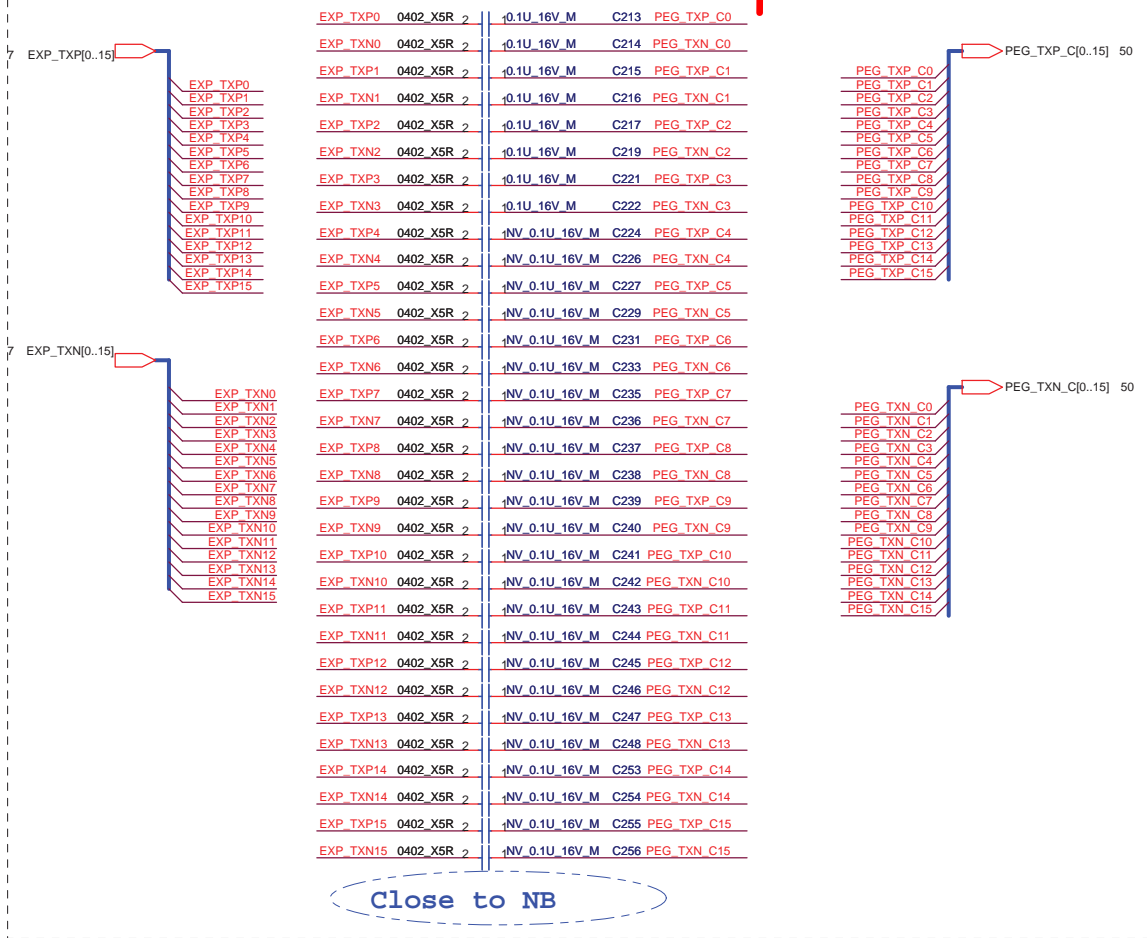
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **LVDS**

Size A3 Document Number: **M841 DVT** Rev 0.1

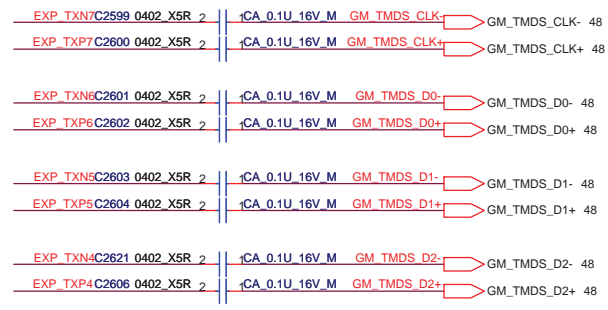
Date: Wednesday, September 17, 2008 Sheet 47 of 77

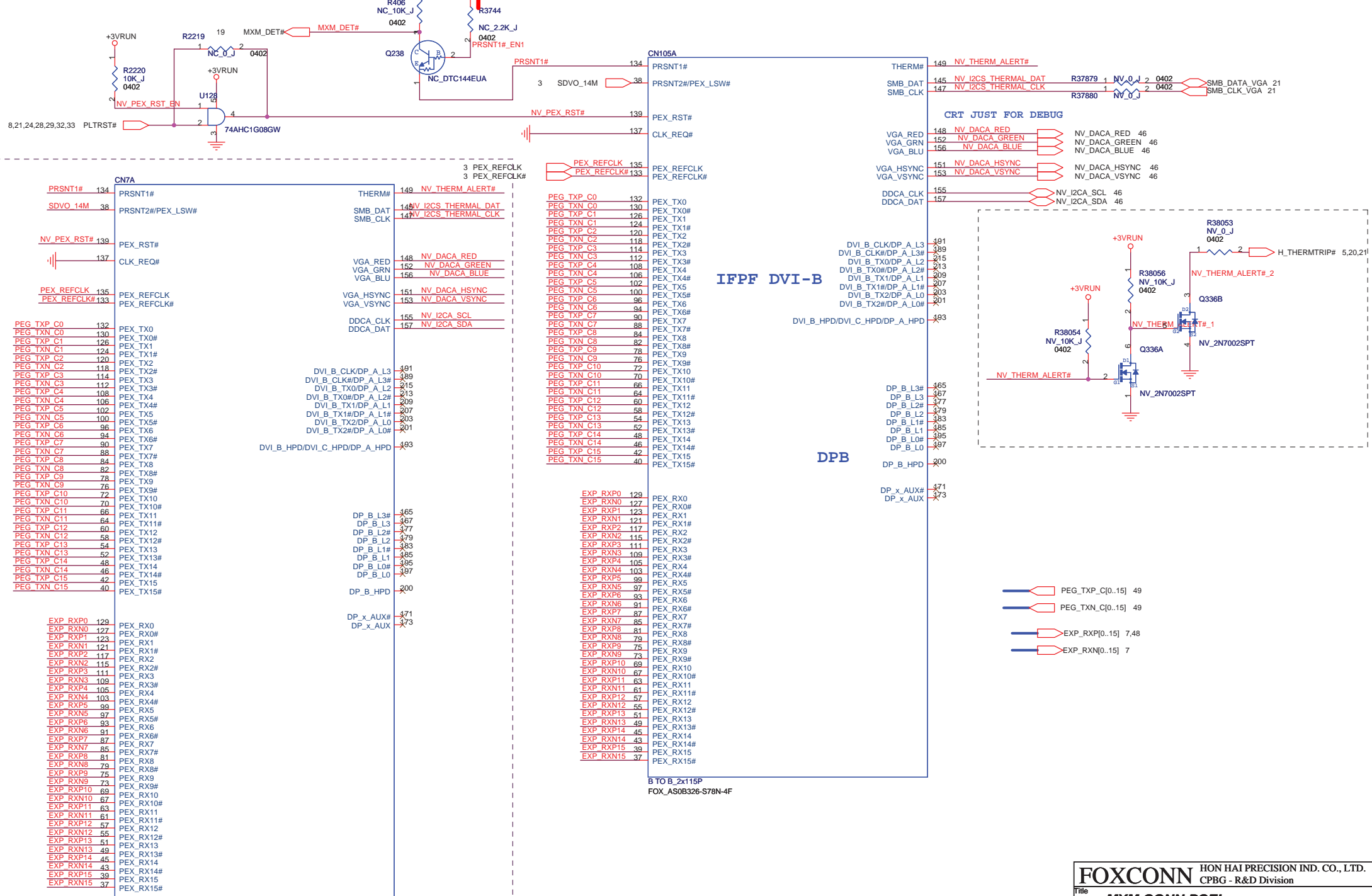




Close to NB

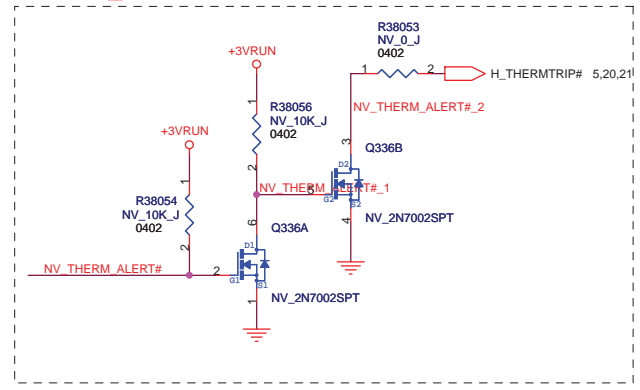
Close to NB and option between NV and CA





CN7A		THERM#	
PRSN1# 134	PRSN1#	149	NV_THERM_ALERT#
SDVO_14M 38	PRSN2#/PEX_LSW#	145	NV_I2CS_THERMAL_DAT
		147	NV_I2CS_THERMAL_CLK
NV_PEX_RST# 139	PEX_RST#	148	NV_DACA_RED
		152	NV_DACA_GREEN
		156	NV_DACA_BLUE
		151	NV_DACA_HSYNC
		153	NV_DACA_VSYNC
PEX_REFCLK 135	PEX_REFCLK	155	NV_I2CA_SCL
PEX_REFCLK# 133	PEX_REFCLK#	157	NV_I2CA_SDA
PEG_TXP_C0 132	PEX_TX0	DVI_B_CLK/DP_A_L3	391
PEG_TXN_C0 130	PEX_TX0#	DVI_B_CLK#/DP_A_L3#	389
PEG_TXP_C1 126	PEX_TX1#	DVI_B_TX0/DP_A_L2	215
PEG_TXN_C1 124	PEX_TX1#	DVI_B_TX0#/DP_A_L2#	213
PEG_TXP_C2 120	PEX_TX2#	DVI_B_TX1/DP_A_L1	209
PEG_TXN_C2 118	PEX_TX2#	DVI_B_TX1#/DP_A_L1#	207
PEG_TXP_C3 114	PEX_TX3#	DVI_B_TX2/DP_A_L0	203
PEG_TXN_C3 112	PEX_TX3#	DVI_B_TX2#/DP_A_L0#	201
PEG_TXP_C4 108	PEX_TX4#	DVI_B_HPDP/DVI_C_HPDP/DP_A_HPDP	393
PEG_TXN_C4 106	PEX_TX4#		
PEG_TXP_C5 102	PEX_TX5#		
PEG_TXN_C5 100	PEX_TX5#		
PEG_TXP_C6 96	PEX_TX6#		
PEG_TXN_C6 94	PEX_TX6#		
PEG_TXP_C7 90	PEX_TX7#		
PEG_TXN_C7 88	PEX_TX7#		
PEG_TXP_C8 84	PEX_TX8#		
PEG_TXN_C8 82	PEX_TX8#		
PEG_TXP_C9 78	PEX_TX9#		
PEG_TXN_C9 76	PEX_TX9#		
PEG_TXP_C10 72	PEX_TX10#		
PEG_TXN_C10 70	PEX_TX10#		
PEG_TXP_C11 66	PEX_TX11#	DP_B_L3#	365
PEG_TXN_C11 64	PEX_TX11#	DP_B_L3	367
PEG_TXP_C12 60	PEX_TX12#	DP_B_L2#	377
PEG_TXN_C12 58	PEX_TX12#	DP_B_L2	379
PEG_TXP_C13 54	PEX_TX13#	DP_B_L1#	383
PEG_TXN_C13 52	PEX_TX13#	DP_B_L1	385
PEG_TXP_C14 48	PEX_TX14#	DP_B_L0#	397
PEG_TXN_C14 46	PEX_TX14#	DP_B_L0	399
PEG_TXP_C15 42	PEX_TX15#	DP_B_HPDP	200
PEG_TXN_C15 40	PEX_TX15#		
EXP_RXP0 129	PEX_RX0	DP_x_AUX#	371
EXP_RXN0 127	PEX_RX0#	DP_x_AUX	373
EXP_RXP1 123	PEX_RX1#		
EXP_RXN1 121	PEX_RX1#		
EXP_RXP2 117	PEX_RX2#		
EXP_RXN2 115	PEX_RX2#		
EXP_RXP3 111	PEX_RX3#		
EXP_RXN3 109	PEX_RX3#		
EXP_RXP4 105	PEX_RX4#		
EXP_RXN4 103	PEX_RX4#		
EXP_RXP5 99	PEX_RX5#		
EXP_RXN5 97	PEX_RX5#		
EXP_RXP6 93	PEX_RX6#		
EXP_RXN6 91	PEX_RX6#		
EXP_RXP7 87	PEX_RX7#		
EXP_RXN7 85	PEX_RX7#		
EXP_RXP8 81	PEX_RX8#		
EXP_RXN8 79	PEX_RX8#		
EXP_RXP9 75	PEX_RX9#		
EXP_RXN9 73	PEX_RX9#		
EXP_RXP10 69	PEX_RX10#		
EXP_RXN10 67	PEX_RX10#		
EXP_RXP11 63	PEX_RX11#		
EXP_RXN11 61	PEX_RX11#		
EXP_RXP12 57	PEX_RX12#		
EXP_RXN12 55	PEX_RX12#		
EXP_RXP13 51	PEX_RX13#		
EXP_RXN13 49	PEX_RX13#		
EXP_RXP14 45	PEX_RX14#		
EXP_RXN14 43	PEX_RX14#		
EXP_RXP15 39	PEX_RX15#		
EXP_RXN15 37	PEX_RX15#		

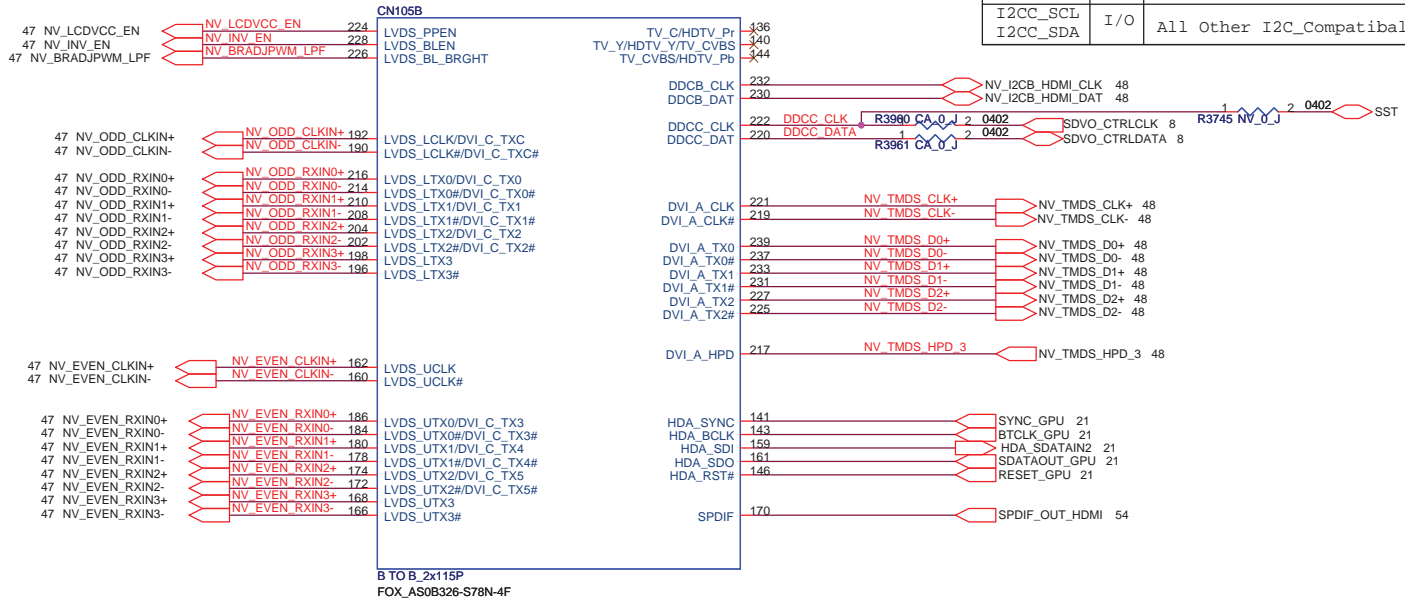
IFPF DVI-B		DPB	
PRSN1# 134	PRSN1#	DP_B_L3#	365
SDVO_14M 38	PRSN2#/PEX_LSW#	DP_B_L3	367
NV_PEX_RST# 139	PEX_RST#	DP_B_L2#	377
		DP_B_L2	379
		DP_B_L1#	383
		DP_B_L1	385
		DP_B_L0#	397
		DP_B_L0	399
		DP_B_HPDP	200
		DP_x_AUX#	371
		DP_x_AUX	373
PEG_TXP_C0 132	PEX_TX0		
PEG_TXN_C0 130	PEX_TX0#		
PEG_TXP_C1 126	PEX_TX1#		
PEG_TXN_C1 124	PEX_TX1#		
PEG_TXP_C2 120	PEX_TX2#		
PEG_TXN_C2 118	PEX_TX2#		
PEG_TXP_C3 114	PEX_TX3#		
PEG_TXN_C3 112	PEX_TX3#		
PEG_TXP_C4 108	PEX_TX4#		
PEG_TXN_C4 106	PEX_TX4#		
PEG_TXP_C5 102	PEX_TX5#		
PEG_TXN_C5 100	PEX_TX5#		
PEG_TXP_C6 96	PEX_TX6#		
PEG_TXN_C6 94	PEX_TX6#		
PEG_TXP_C7 90	PEX_TX7#		
PEG_TXN_C7 88	PEX_TX7#		
PEG_TXP_C8 84	PEX_TX8#		
PEG_TXN_C8 82	PEX_TX8#		
PEG_TXP_C9 78	PEX_TX9#		
PEG_TXN_C9 76	PEX_TX9#		
PEG_TXP_C10 72	PEX_TX10#		
PEG_TXN_C10 70	PEX_TX10#		
PEG_TXP_C11 66	PEX_TX11#		
PEG_TXN_C11 64	PEX_TX11#		
PEG_TXP_C12 60	PEX_TX12#		
PEG_TXN_C12 58	PEX_TX12#		
PEG_TXP_C13 54	PEX_TX13#		
PEG_TXN_C13 52	PEX_TX13#		
PEG_TXP_C14 48	PEX_TX14#		
PEG_TXN_C14 46	PEX_TX14#		
PEG_TXP_C15 42	PEX_TX15#		
PEG_TXN_C15 40	PEX_TX15#		
EXP_RXP0 129	PEX_RX0		
EXP_RXN0 127	PEX_RX0#		
EXP_RXP1 123	PEX_RX1#		
EXP_RXN1 121	PEX_RX1#		
EXP_RXP2 117	PEX_RX2#		
EXP_RXN2 115	PEX_RX2#		
EXP_RXP3 111	PEX_RX3#		
EXP_RXN3 109	PEX_RX3#		
EXP_RXP4 105	PEX_RX4#		
EXP_RXN4 103	PEX_RX4#		
EXP_RXP5 99	PEX_RX5#		
EXP_RXN5 97	PEX_RX5#		
EXP_RXP6 93	PEX_RX6#		
EXP_RXN6 91	PEX_RX6#		
EXP_RXP7 87	PEX_RX7#		
EXP_RXN7 85	PEX_RX7#		
EXP_RXP8 81	PEX_RX8#		
EXP_RXN8 79	PEX_RX8#		
EXP_RXP9 75	PEX_RX9#		
EXP_RXN9 73	PEX_RX9#		
EXP_RXP10 69	PEX_RX10#		
EXP_RXN10 67	PEX_RX10#		
EXP_RXP11 63	PEX_RX11#		
EXP_RXN11 61	PEX_RX11#		
EXP_RXP12 57	PEX_RX12#		
EXP_RXN12 55	PEX_RX12#		
EXP_RXP13 51	PEX_RX13#		
EXP_RXN13 49	PEX_RX13#		
EXP_RXP14 45	PEX_RX14#		
EXP_RXN14 43	PEX_RX14#		
EXP_RXP15 39	PEX_RX15#		
EXP_RXN15 37	PEX_RX15#		



- PEG_TXP_C[0..15] 49
- PEG_TXN_C[0..15] 49
- EXP_RXP[0..15] 7,48
- EXP_RXN[0..15] 7

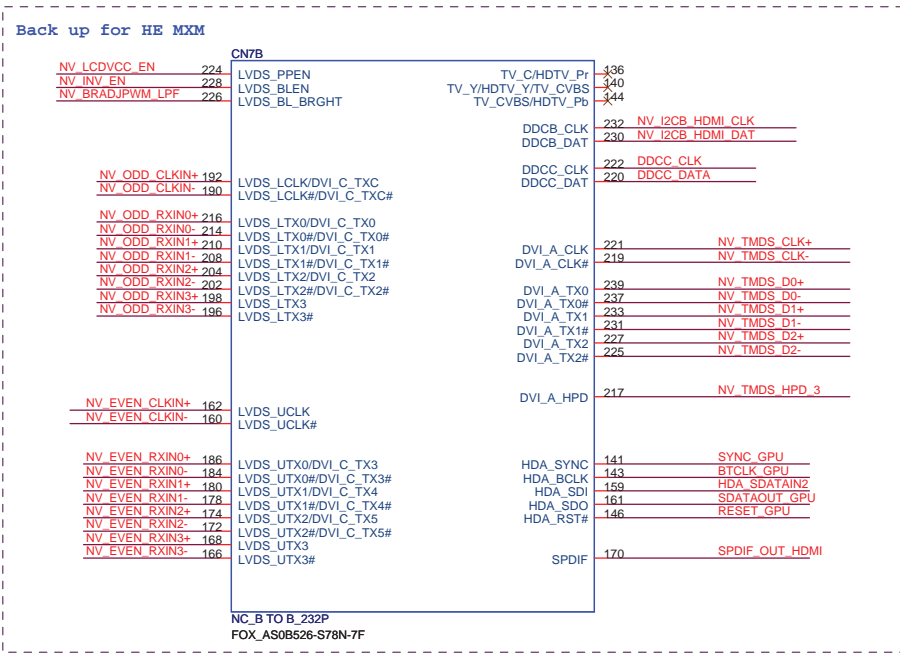
NC_B TO B_232P
FOX_AS0B526-S78N-7F Back up for HE MXM

SIGNAL	I/O	Description	Used for
I2CA_SCL I2CA_SDA	I/O	Notebook VGA I2C_Compatibal Bus Signals	DAC A DDC BUS
I2CB_SCL I2CB_SDA	I/O	Notebook HDMI I2C_Compatibal Bus Signals	HDMI DDC BUS
I2CC_SCL I2CC_SDA	I/O	All Other I2C_Compatibal Bus Signals	SDVO CONTROL BUS/SSST

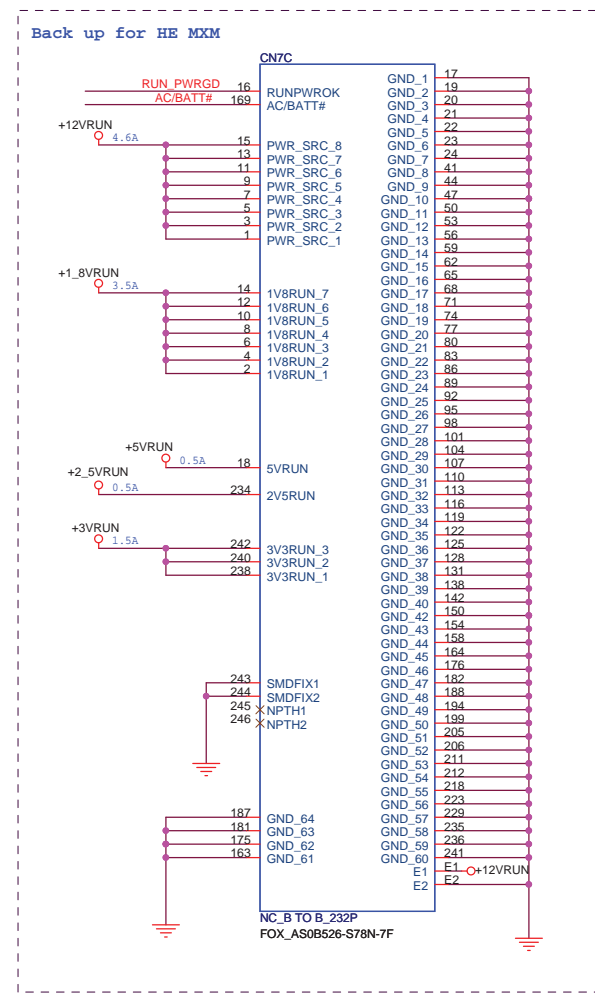
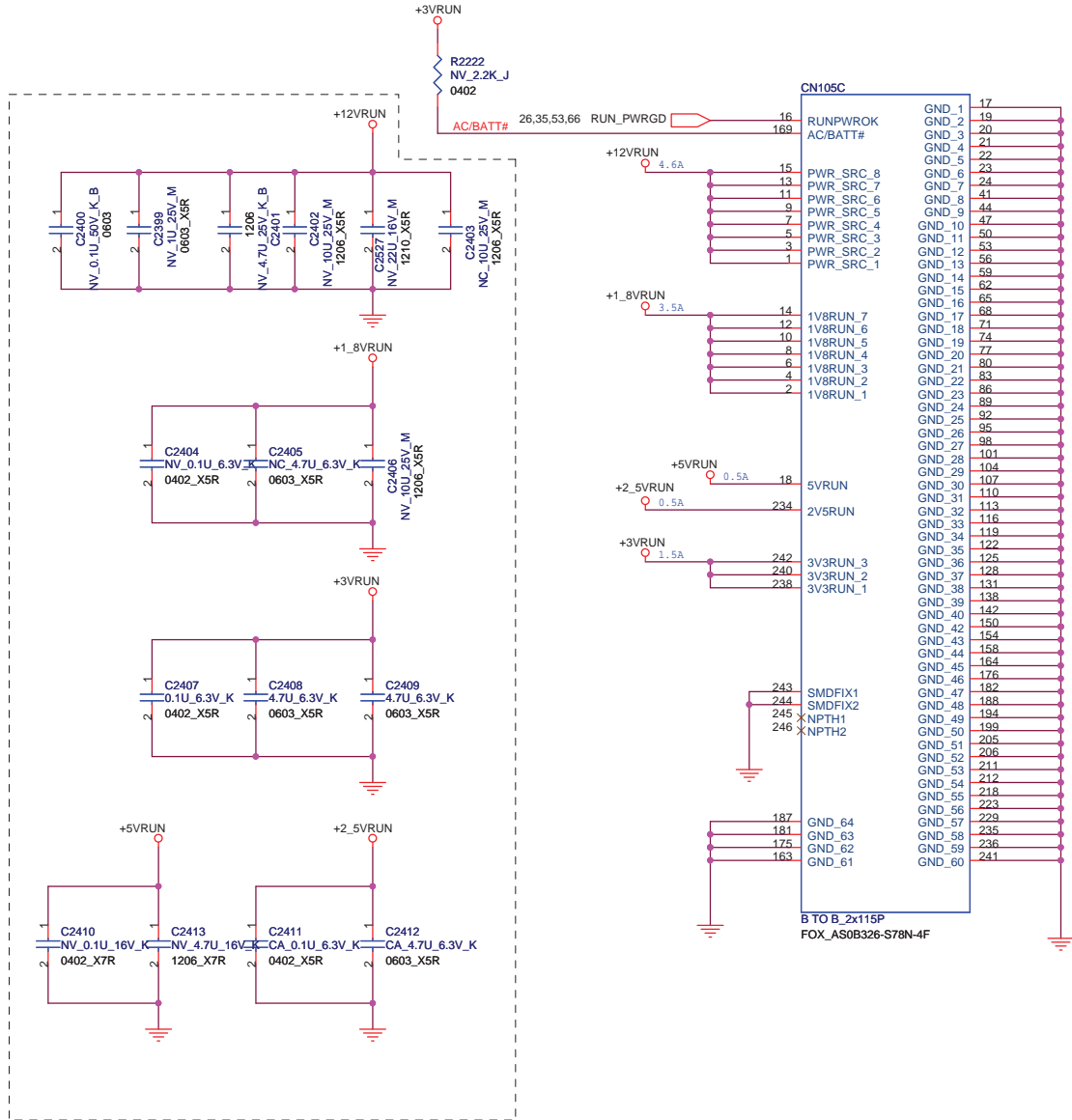


MXM_SST
ADD0:HIGH
ADD1:FLOATING
ADDRESS:0x4D

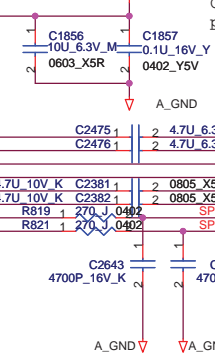
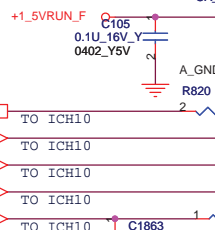
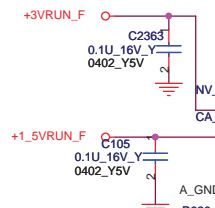
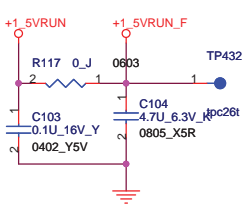
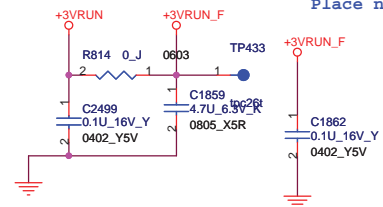
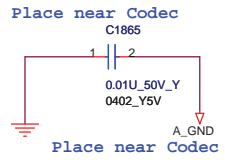
SDVO DDC_AS STRAP=HIGH
High Device Address is 70h.
low Device Address is 72h.



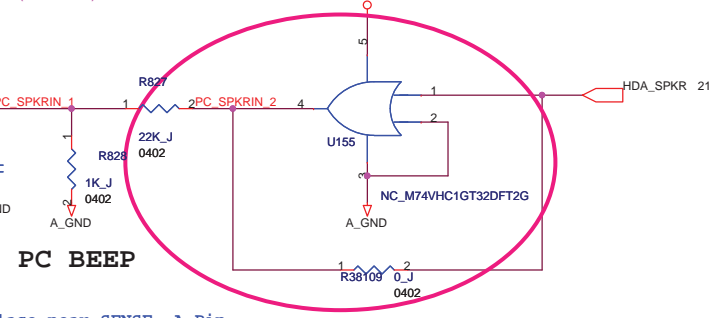
FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title MXM CONN OUT		
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 51	of 77



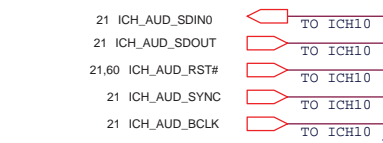
C1856 change from 1U_6.3V to 10U_6.3V
place this 2 capacitors near AVDD2(38)



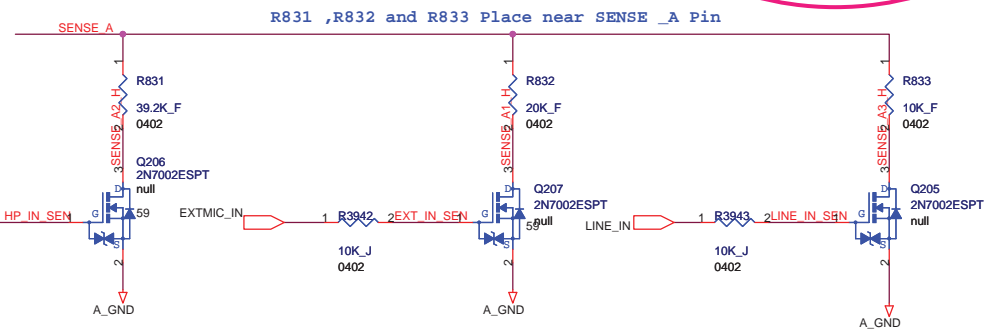
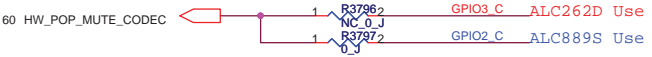
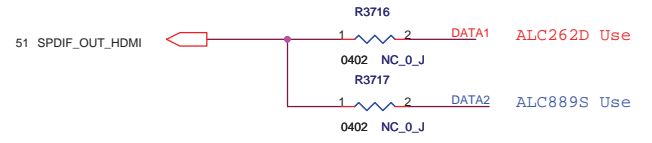
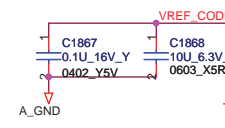
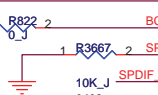
0911 NC U155, change R827 from 33K_J to 22k_J,
add R38109 (0ohm) for cost down



PC BEEP

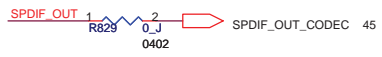


Place C1863 Close CODEC.

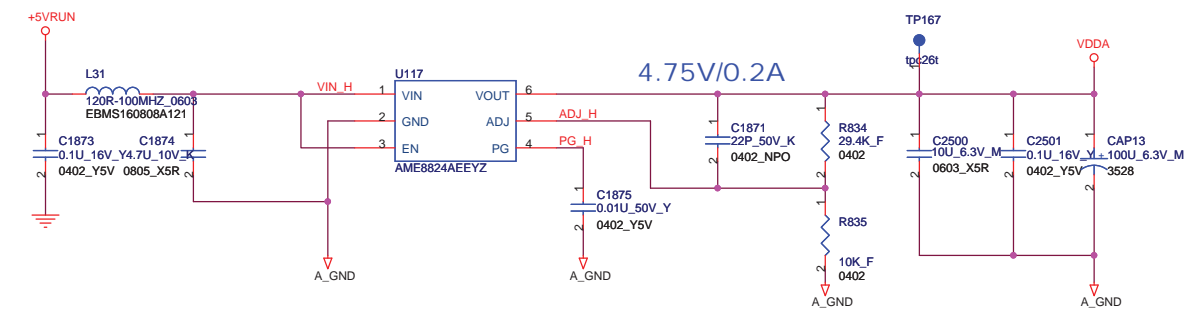


R831 ,R832 and R833 Place near SENSE_A Pin

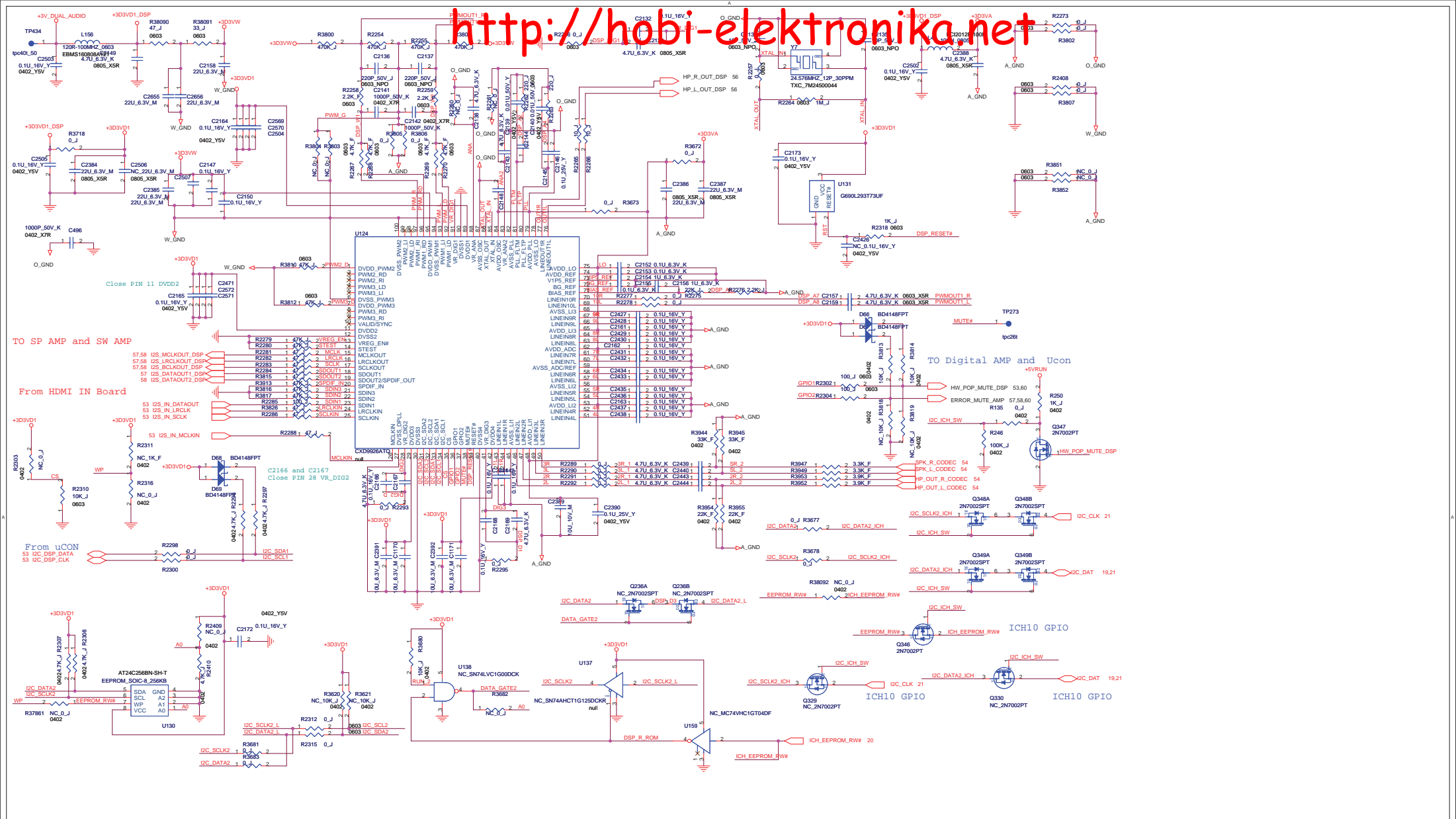
TO I/O CONN



Remove SPDIF OUT CONN to DB.



0131
Place this 2 capacitors near AVDD1(25)



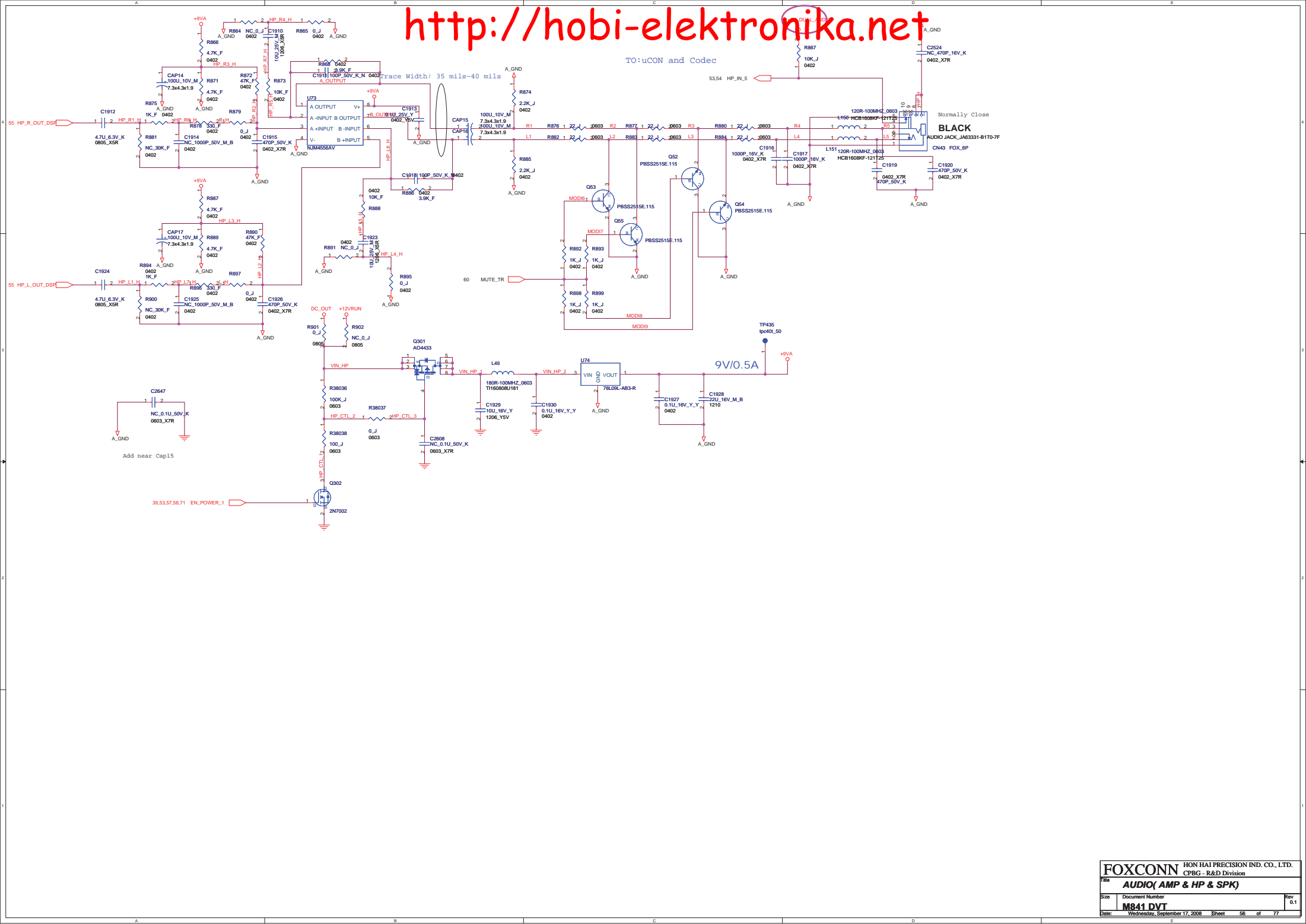
TO SP AMP and SW AMP

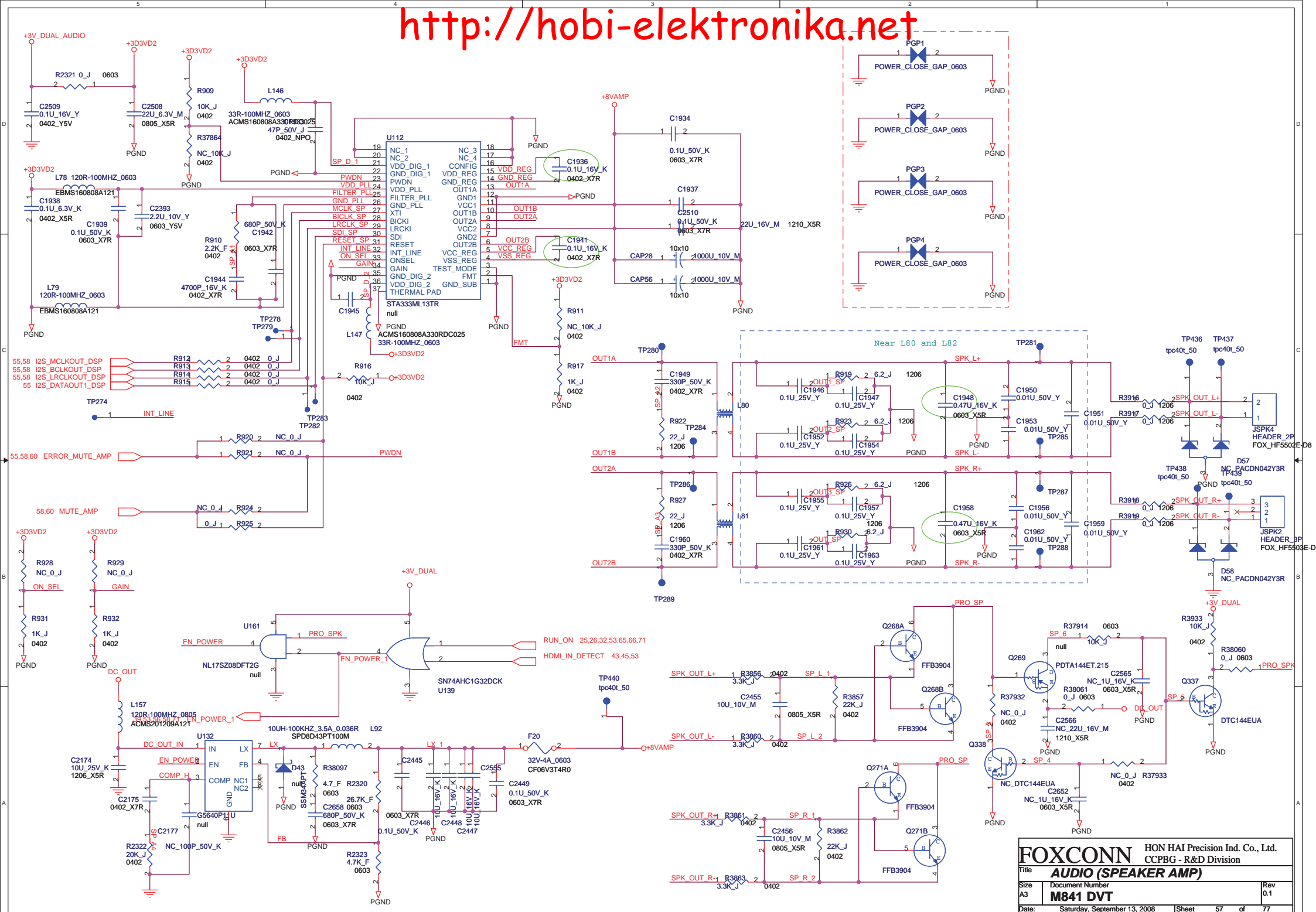
From HDMI IN Board

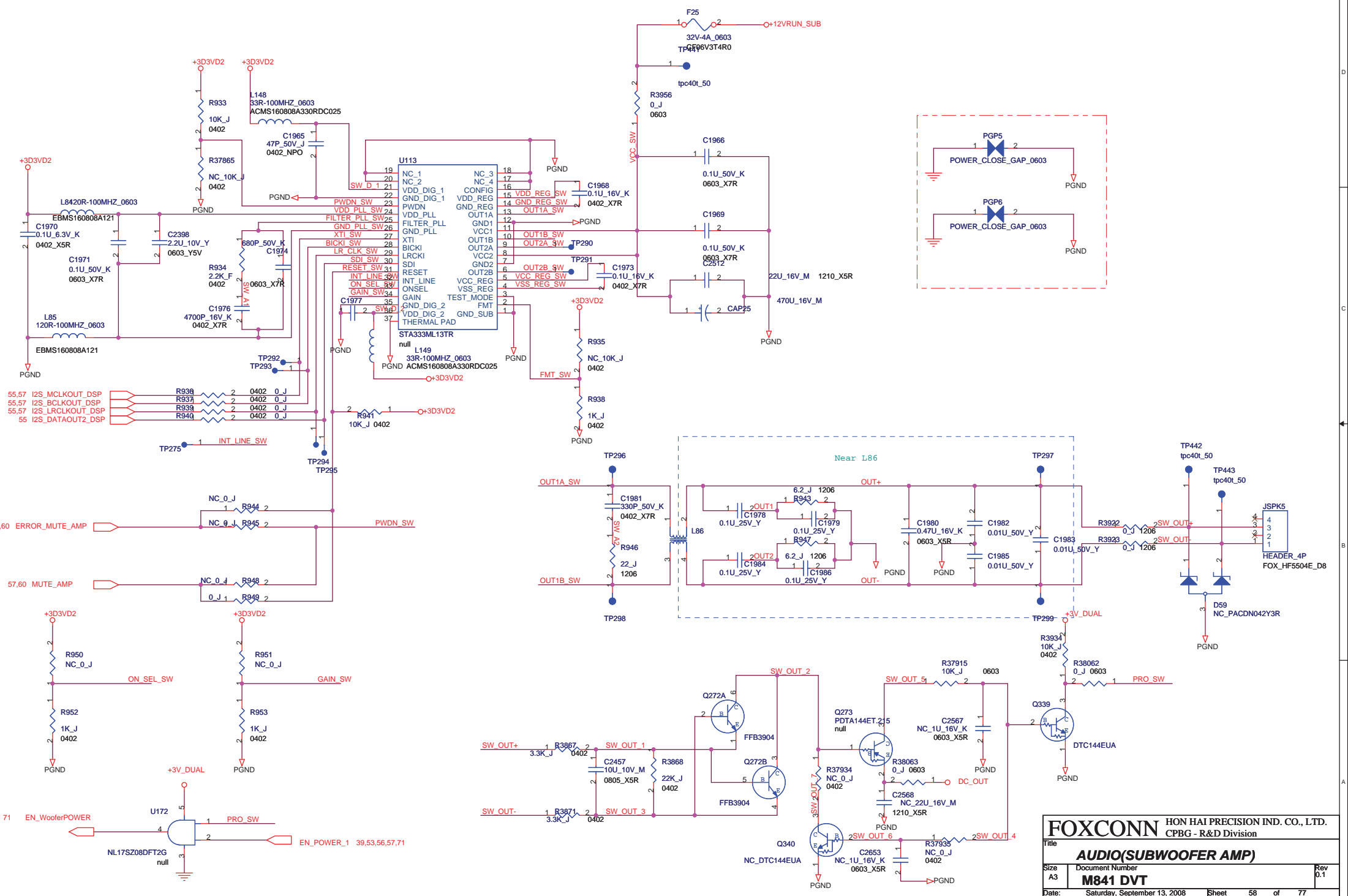
From uCON

TO Digital AMP and Ucon

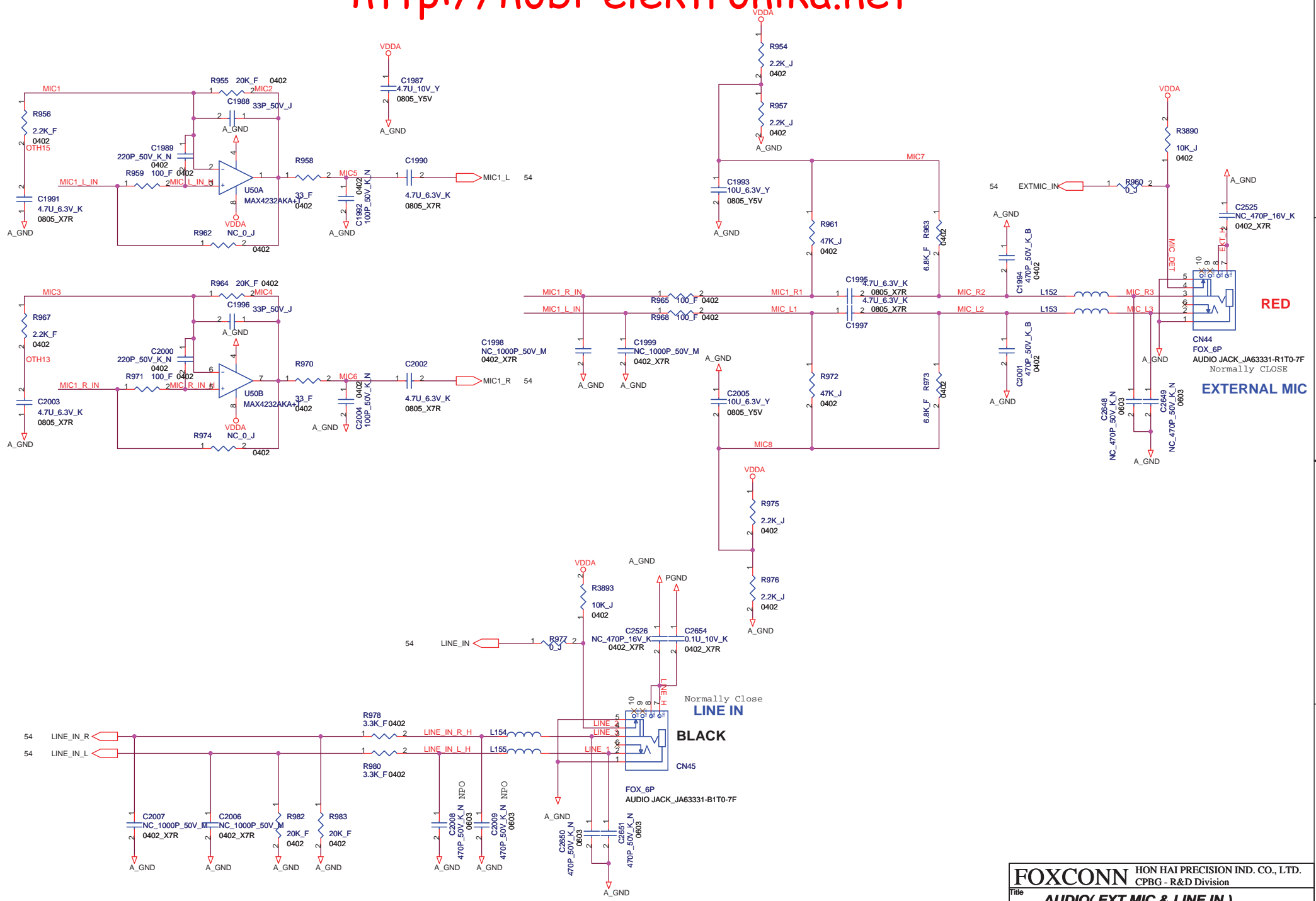
FOXCONN





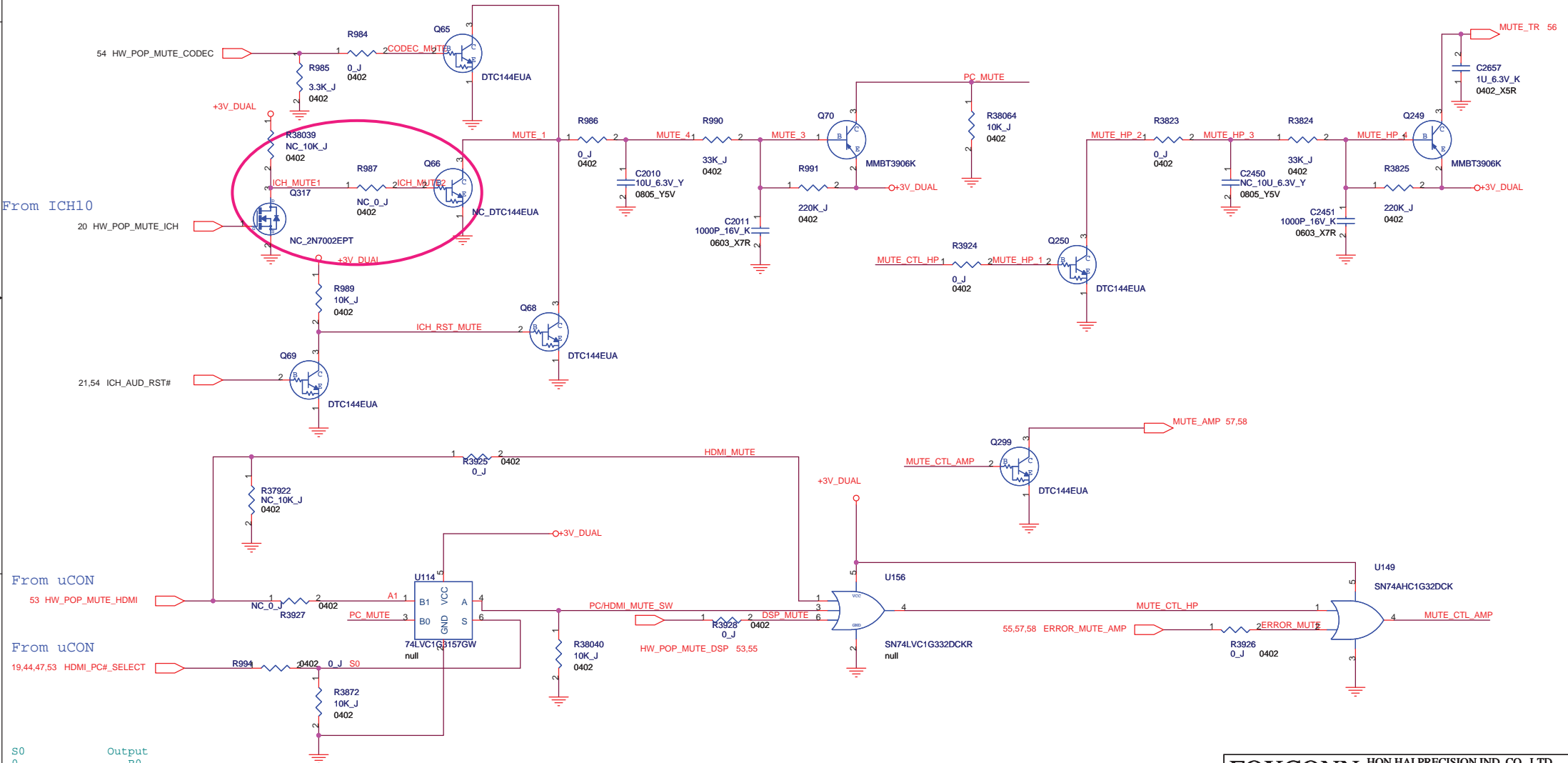


FOXCONN HON HAI PRECISION IND. CO., L.TD. CPBG - R&D Division		
Title AUDIO(SUBWOOFER AMP)		
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 58	of 77



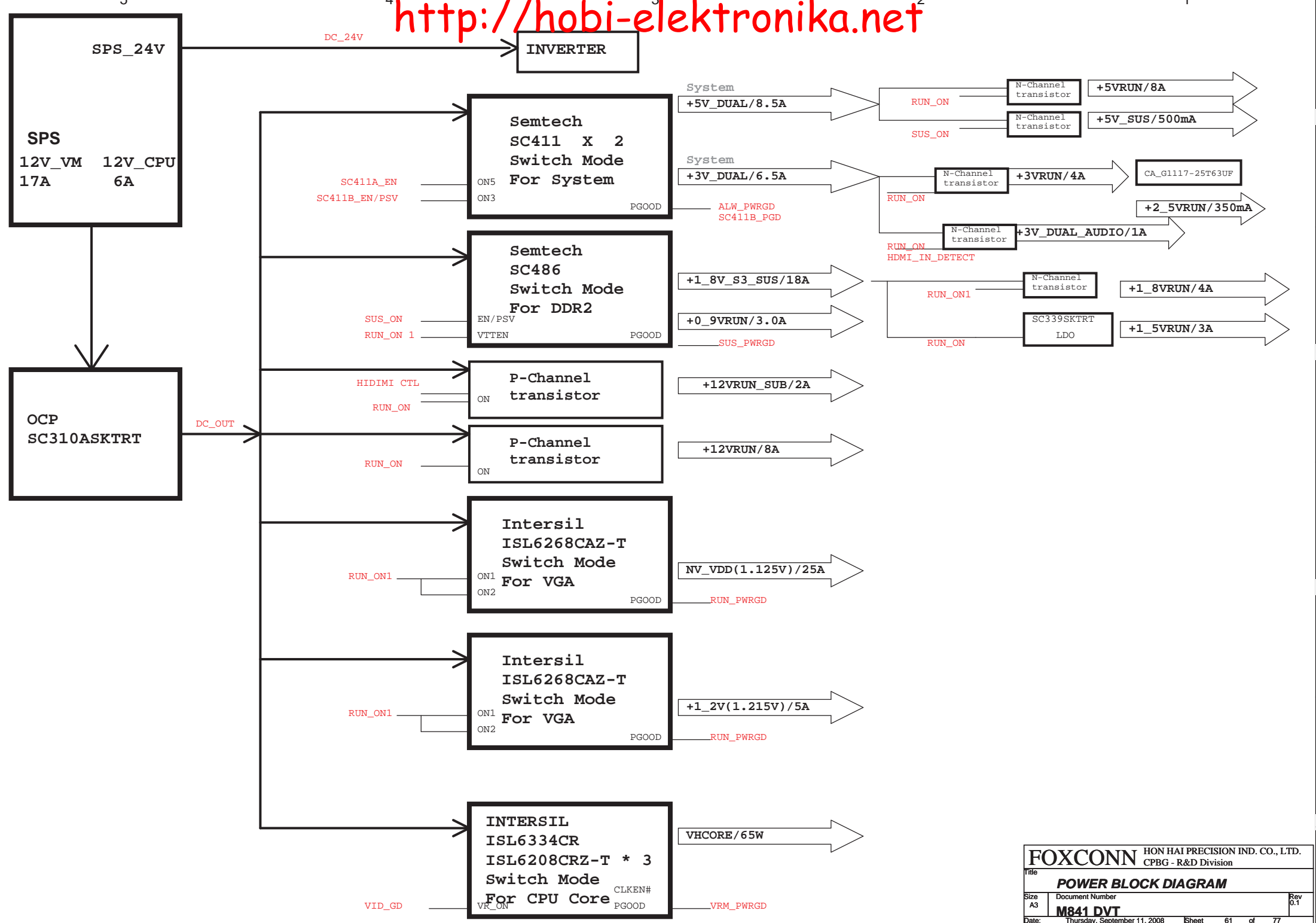
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title AUDIO(EXT MIC & LINE IN)		
Size A3	Document Number M841 DVT	Rev 0.1
Date: Wednesday, September 17, 2008	Sheet 59	of 77

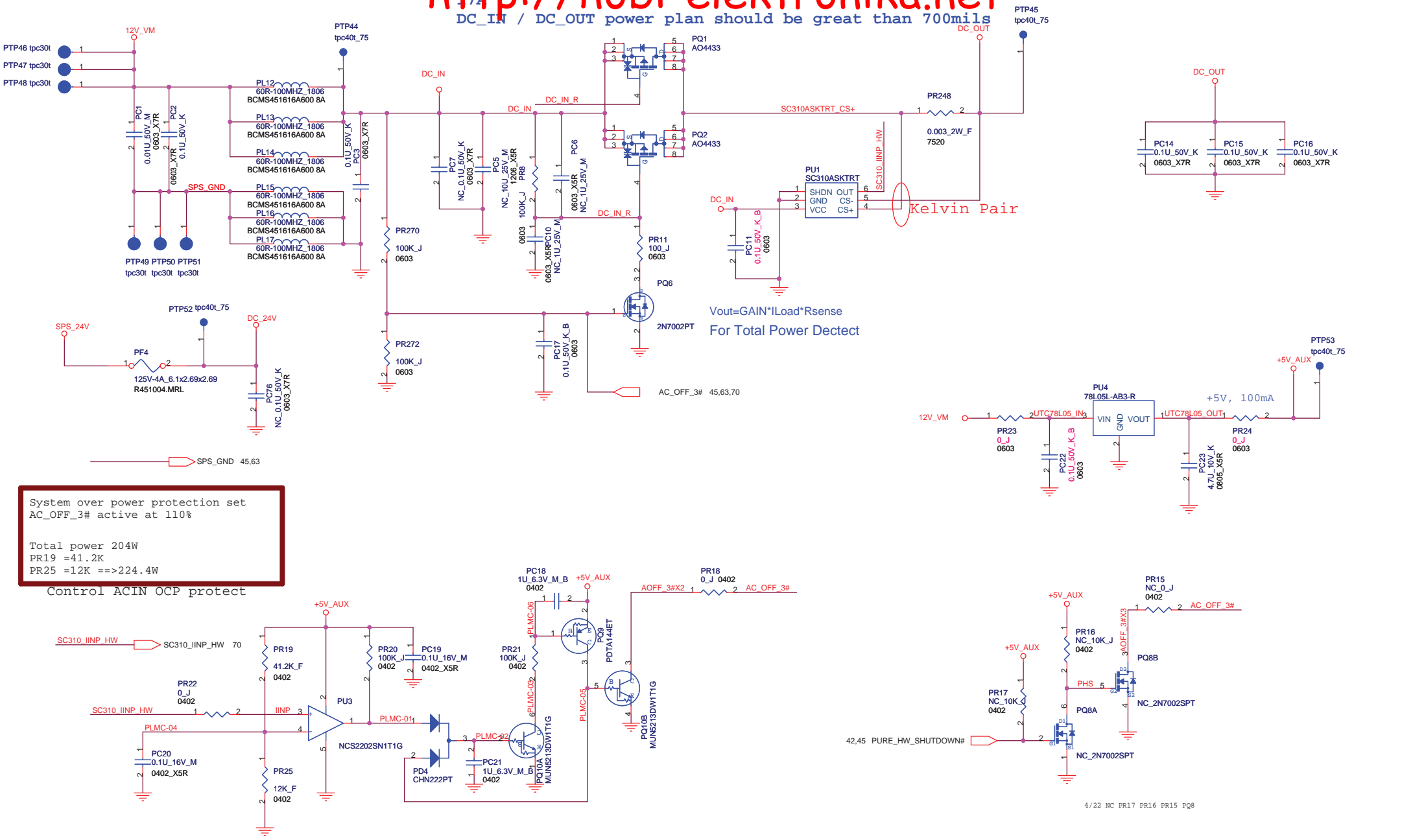
0829 NC Q317,R38039,R987,Q66 for cost down



S0 Output
 0 B0
 1 B1
 When HIDEMI Mode ,HDMI/PC_Select pin is " 1"
 When PC Mode , HDMI/PC_Select pin is "0"

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
AUDIO (MUTE)			
Size		Document Number	
A3		M841 DVT	
Date:		Rev	
Wednesday, September 17, 2008		0.1	
Sheet		of	
60		77	



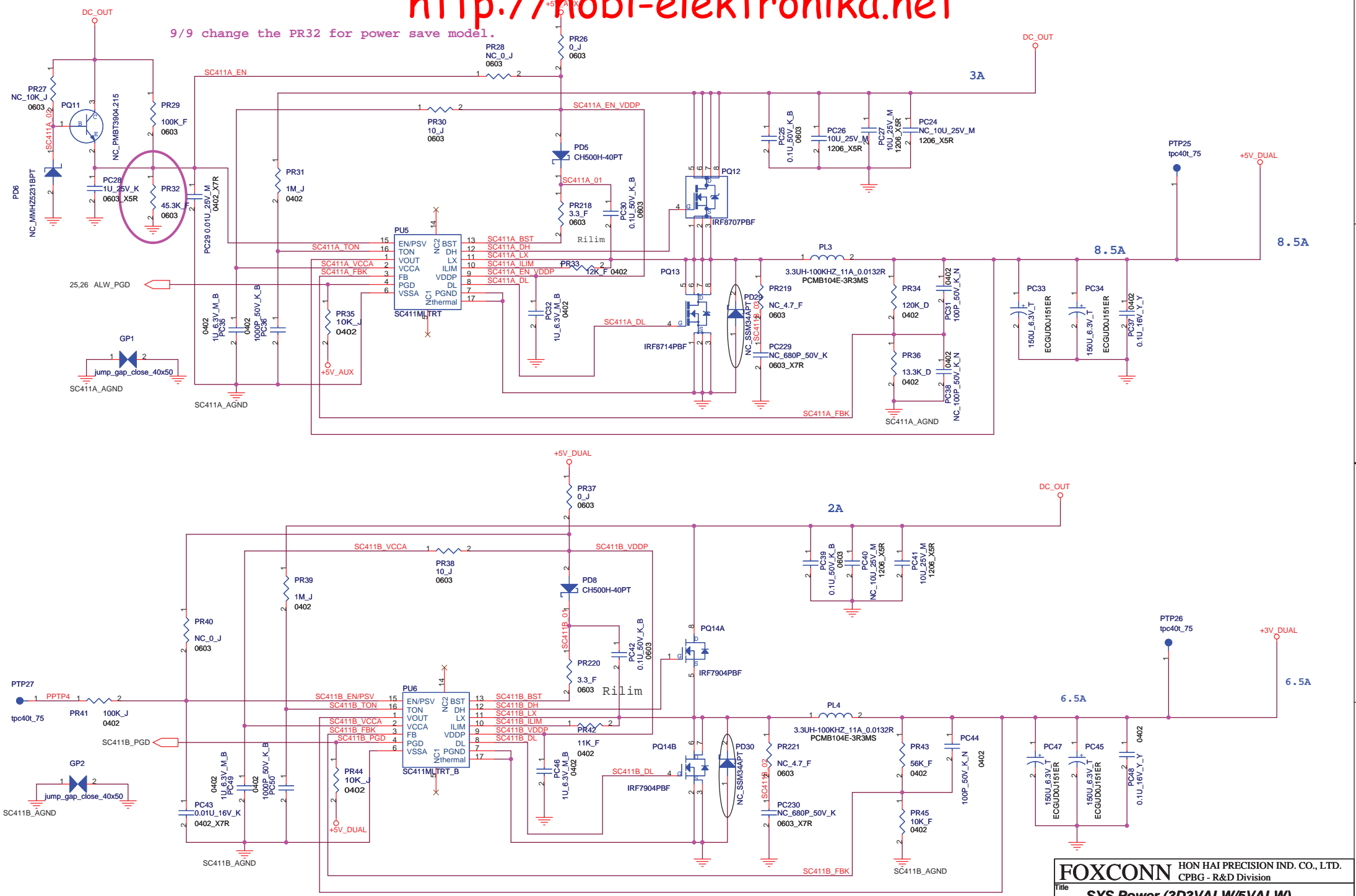


System over power protection set
 AC_OFF_3# active at 110%

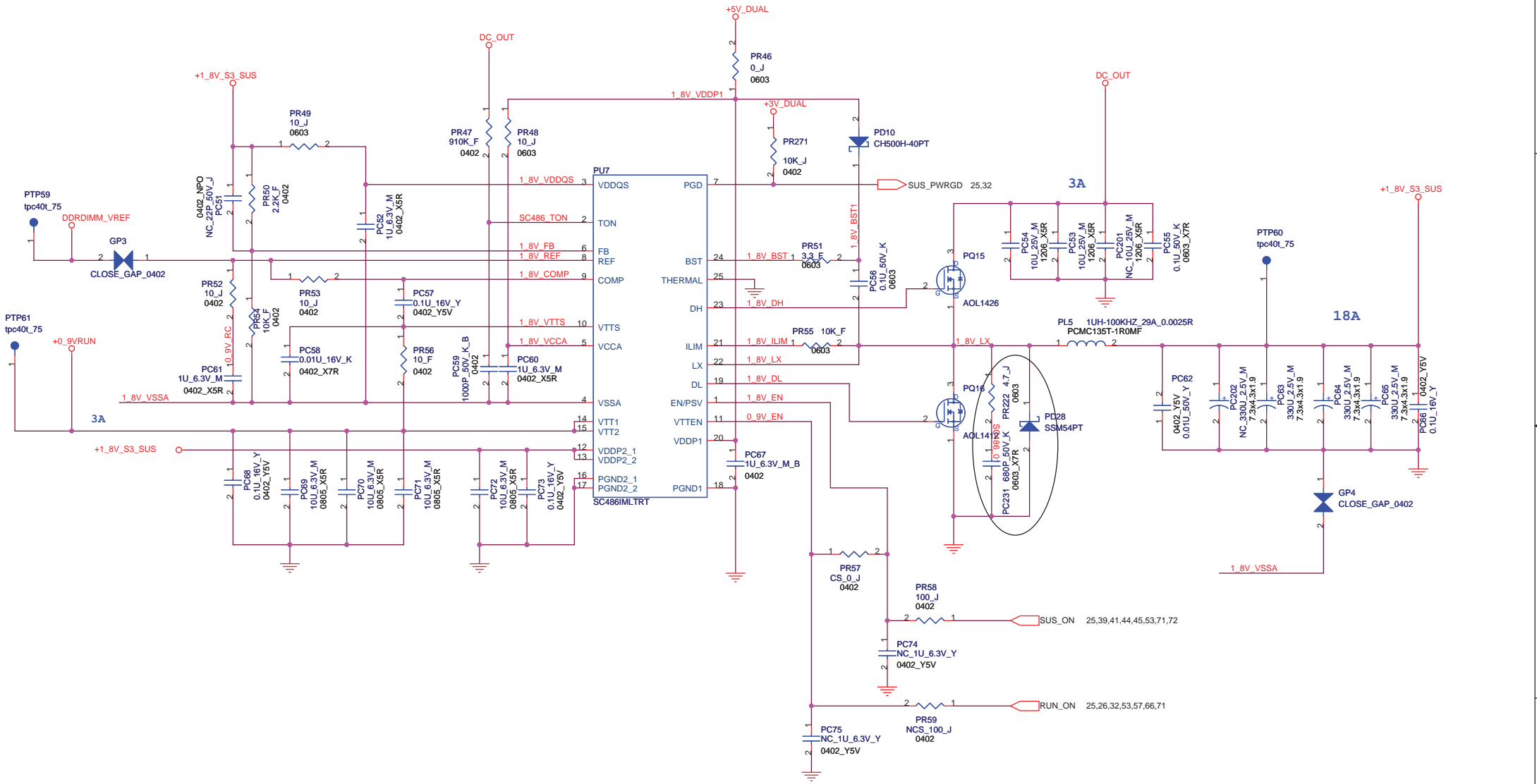
Total power 204W
 PR19 =41.2K
 PR25 =12K ==>224.4W

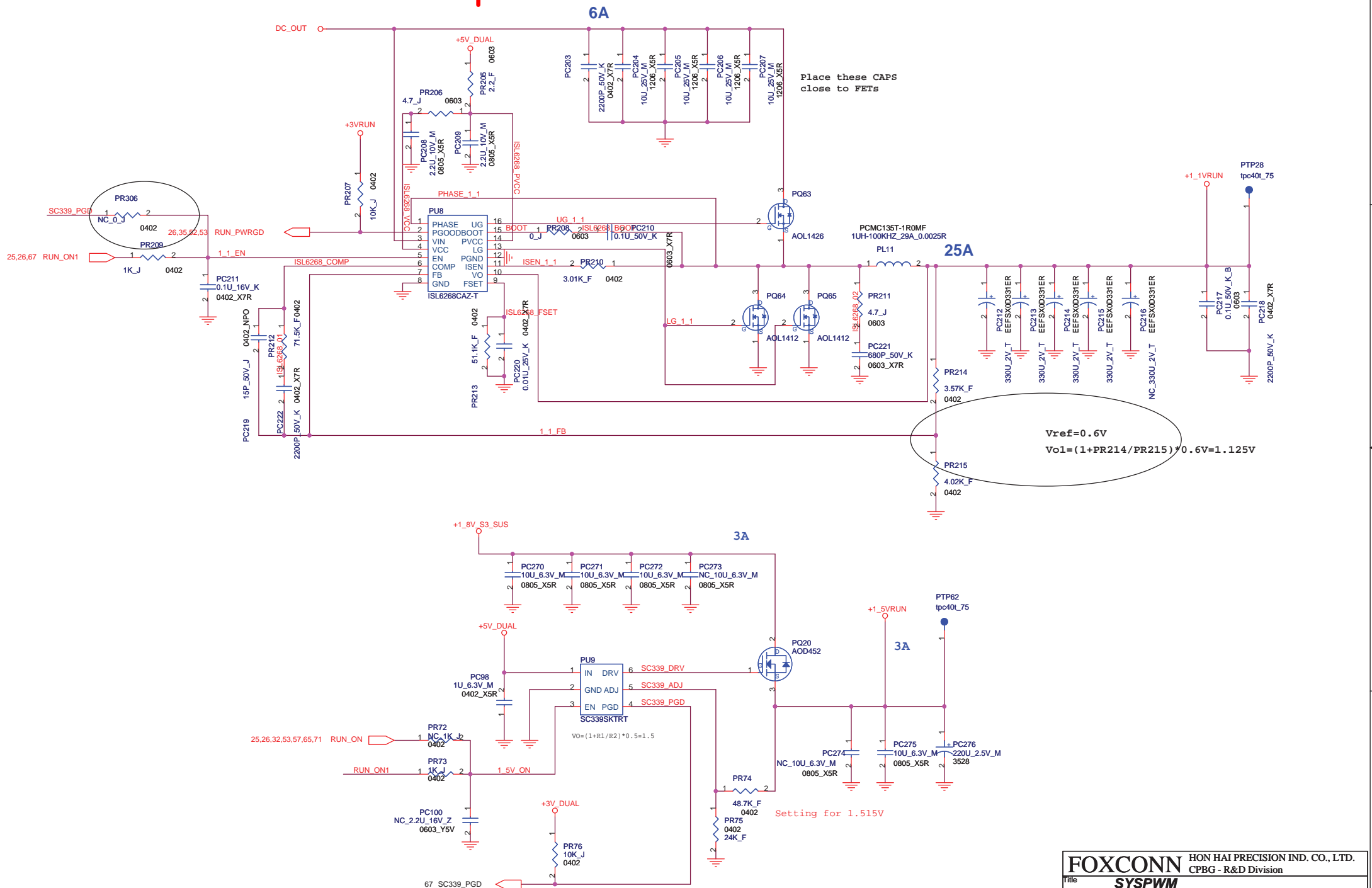
Control ACIN OCP protect

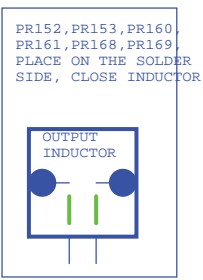
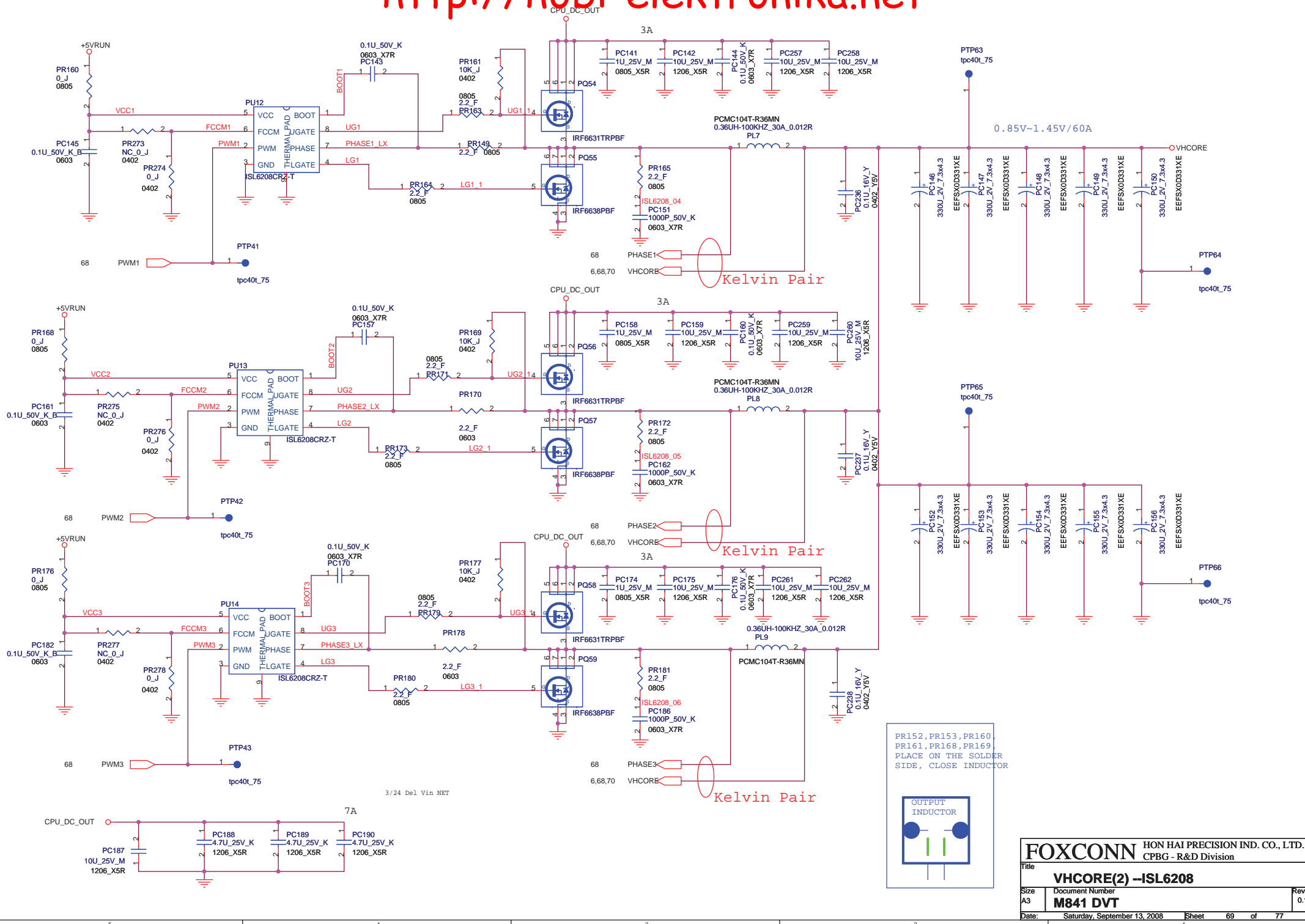
9/9 change the PR32 for power save model.



FOXCONN HON HAI PRECISION IND. CO., L.TD. CPBG - R&D Division		
Title SYS Power (3D3VALW/5VALW)		
Size A3	Document Number M841 DVT	Rev 0.1
Date: Wednesday, September 17, 2008	Sheet 64	of 77





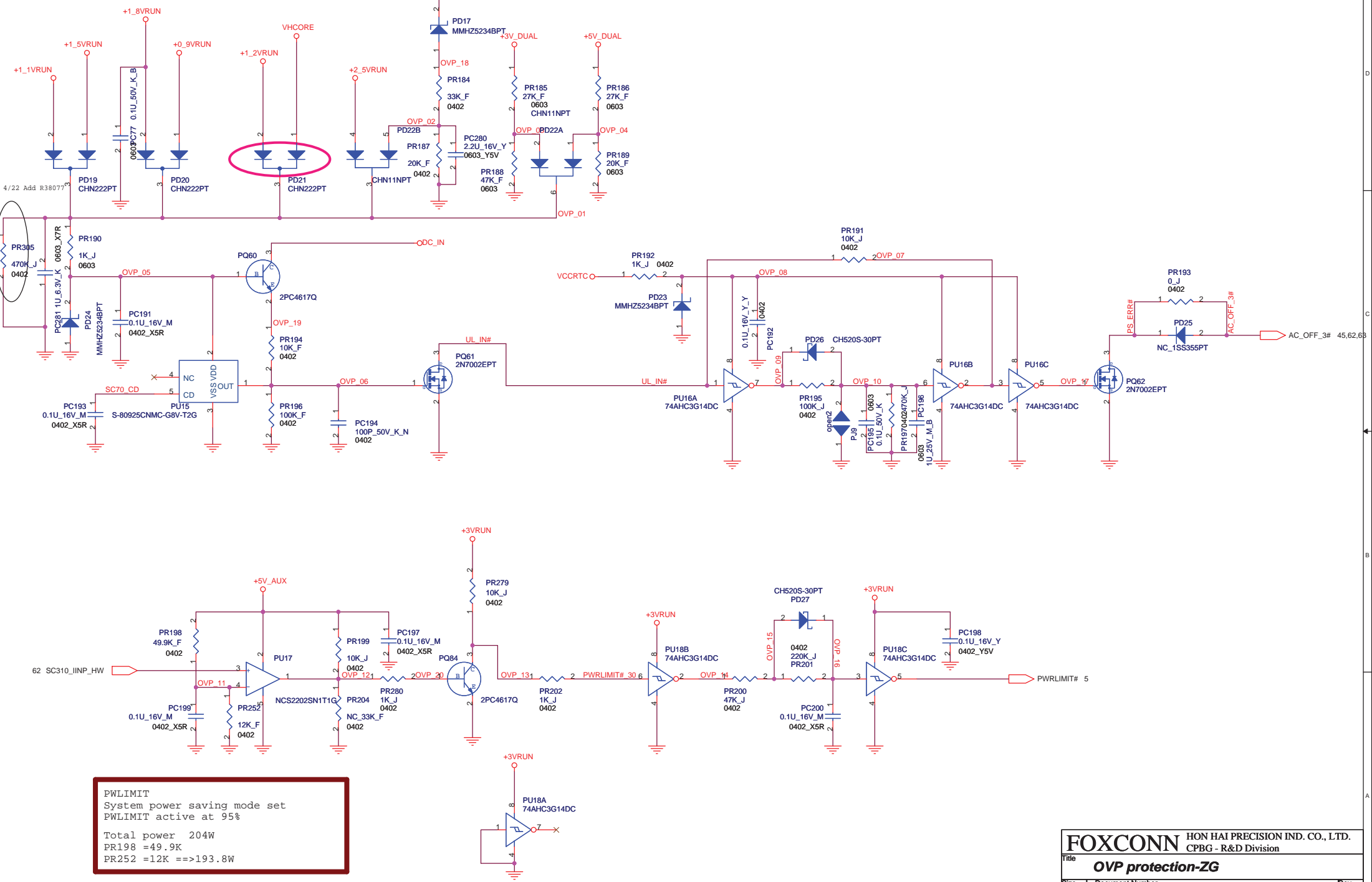


PR152, PR153, PR160
PR161, PR168, PR169
PLACE ON THE SOLDER
SIDE, CLOSE INDUCTOR

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		VHCORE(2) -ISL6208	
Size	Document Number	Rev	
A3	M841 DVT	0.1	
Date:	Saturday, September 13, 2008	Sheet	69 of 77

3/24 Del Vin NET

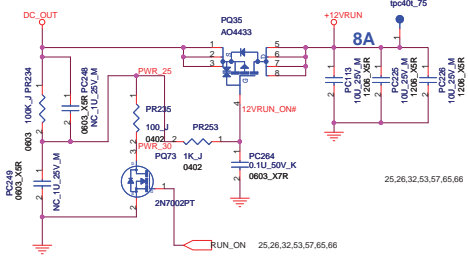
9/12 Change PD18,PD21 from 16-1SS355P-T000 to PD12 (CHN2222PT)



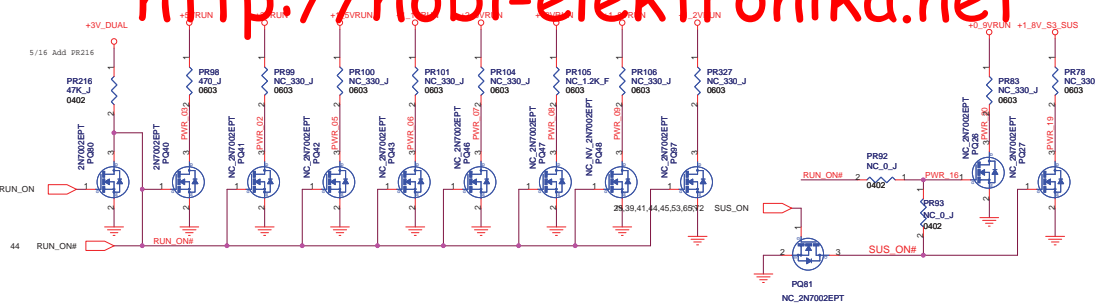
PWLIMIT
 System power saving mode set
 PWLIMIT active at 95%
 Total power 204W
 PR198 =49.9K
 PR252 =12K ==>193.8W

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title OVP protection-ZG			
Size	Document Number		Rev
A3	M841 DVT		0.1
Date:	Wednesday, September 17, 2008	Sheet	70 of 77

Use switch to control the sequence for +12VRUN

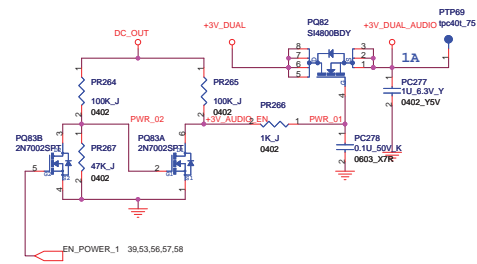
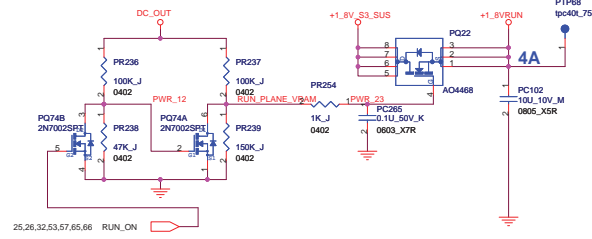
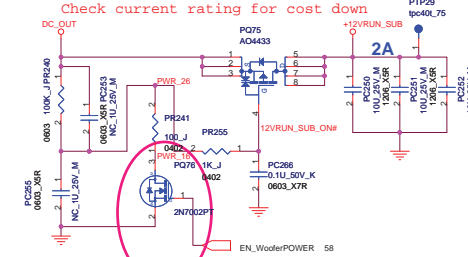


Discharge circuit

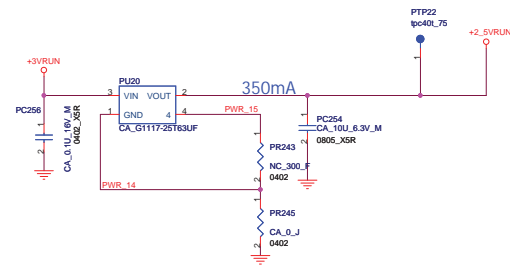
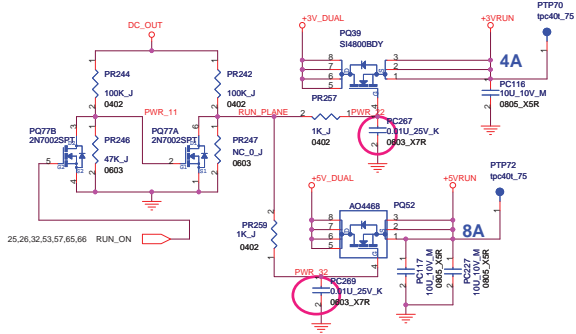
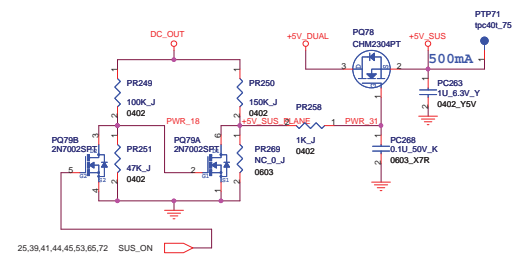


Use switch to control the sequence for +12VRUN SUB

Check current rating for cost down

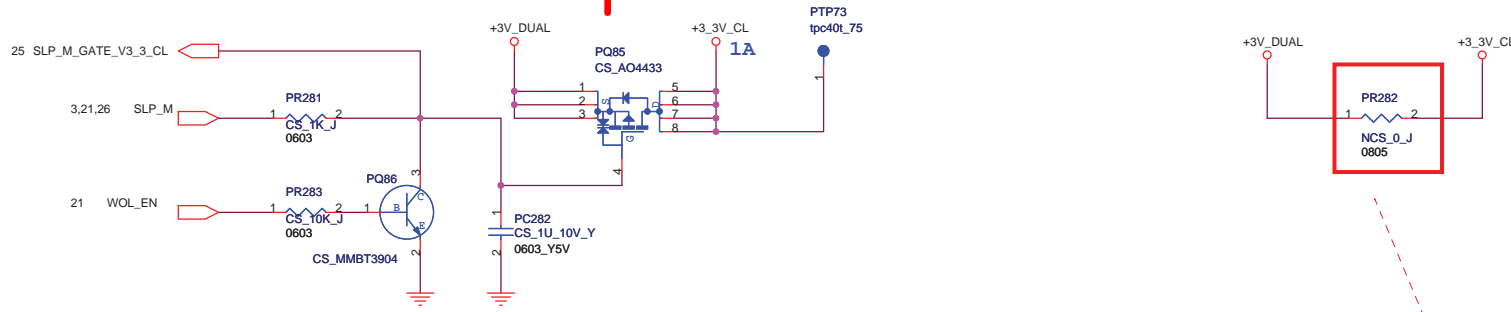


9/9 Change the PQ76 from 17-2N70020-000 to 17-2N7002P-T000 for PUR request

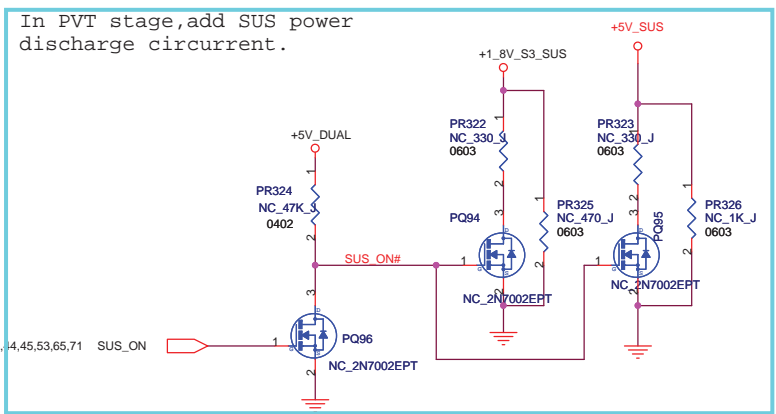
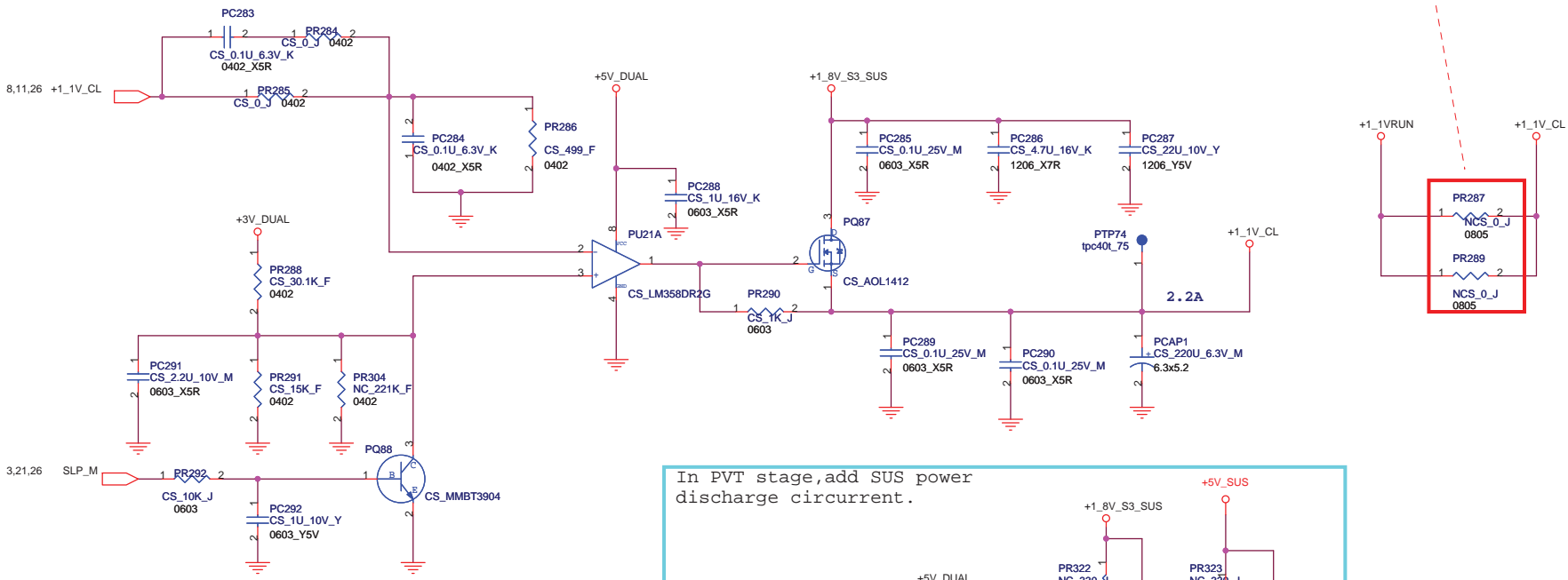


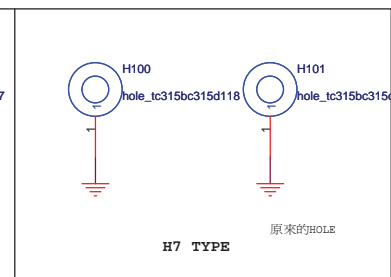
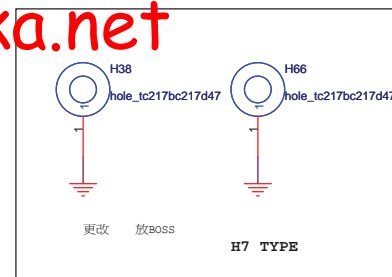
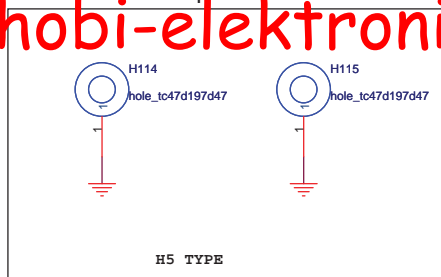
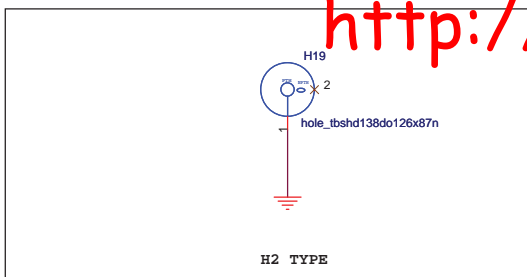
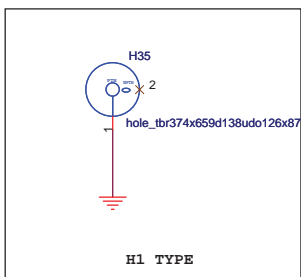
9/23 Change the PC267,PC269 from 1C-2B30104-K000(0.1u) to 1C-2B30103-K000(0.01u) for new TV tuner Lyra

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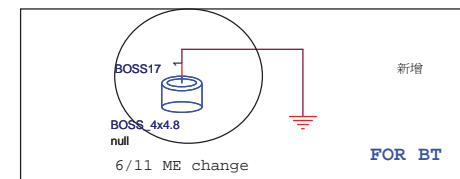
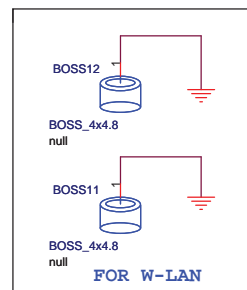
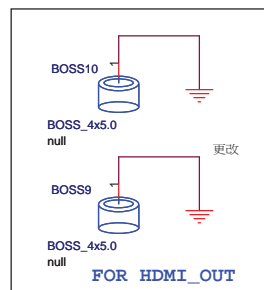
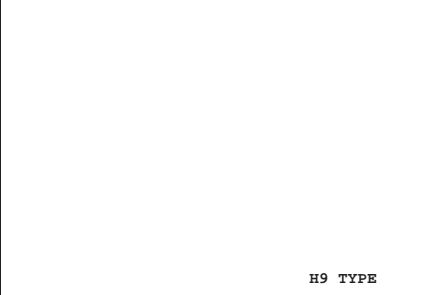
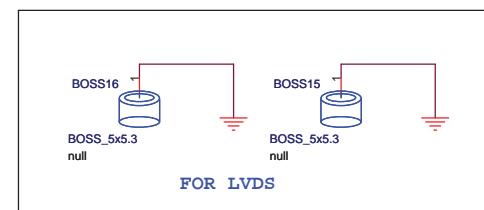
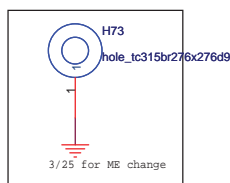
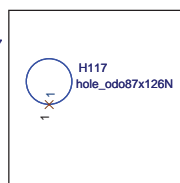
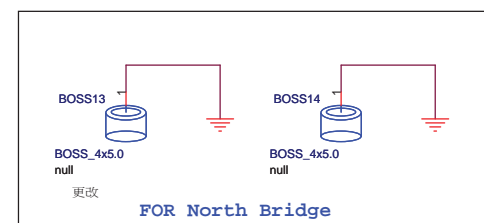
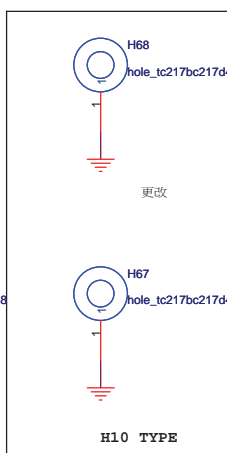
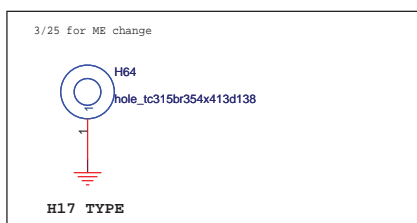
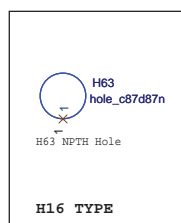
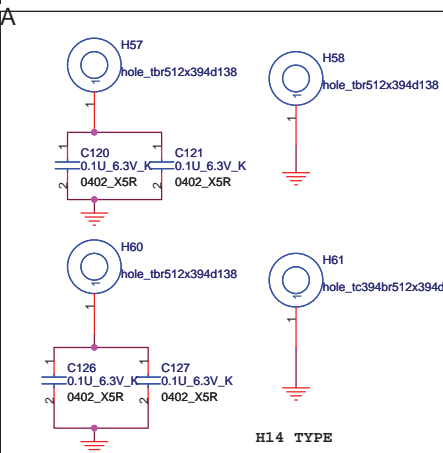
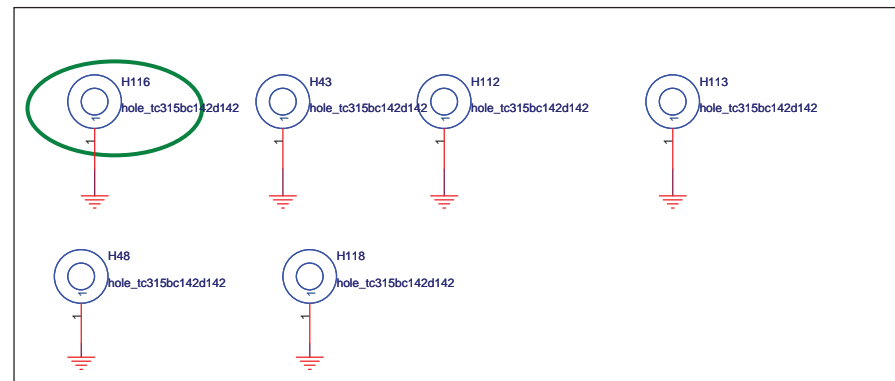
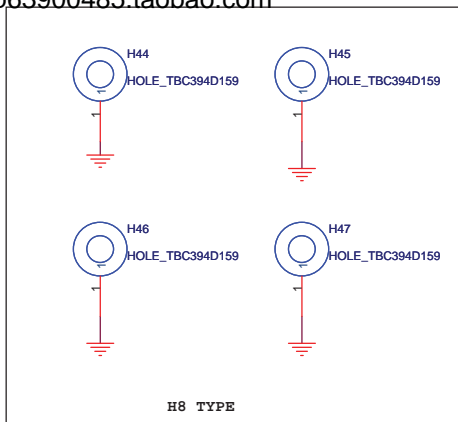
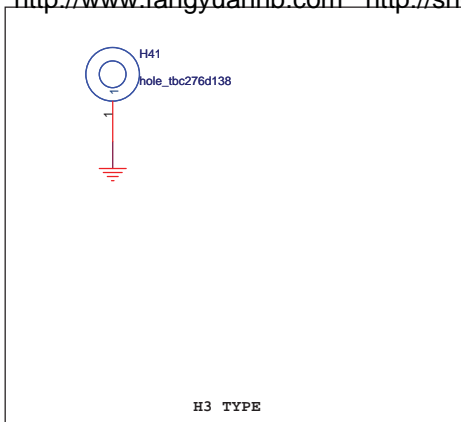


DVT:03/23:Default mount; NC for corwin spring.



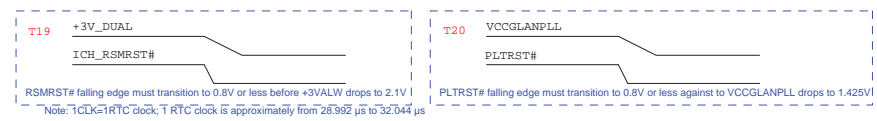
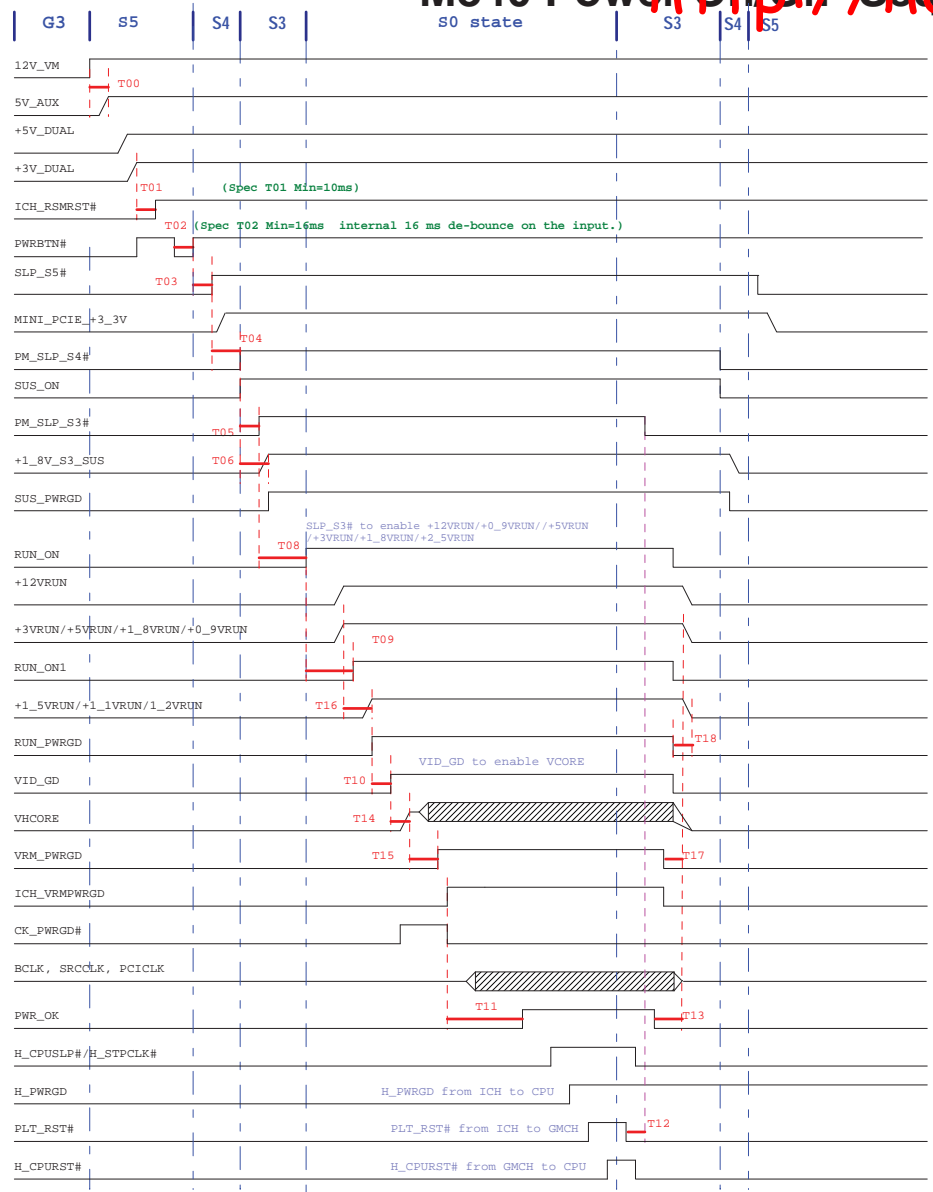


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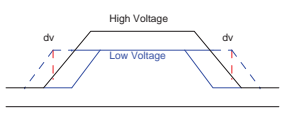
M840 Power On/Off Sequence Specification

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	T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	T12	T13	T14	T15	T16	T17	T18	T19
Min	----	10ms	----	----	?CLK	?CLK	1CLK	----	60ms	10ms	30ms	99ms	1CLK	20ns	----	----	----	----	----	----
Typ	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
Max	----	----	----	----	?CLK	?CLK	----	----	----	----	----	----	2CLK	----	----	----	----	----	----	----

High Voltage	VSREF (+5VRUN)	VSREF_SUS (+5V_DUAL)
Low Voltage	+3VRUN	+3VALW
dv	0.7V	0.7V
Add Diode		



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Title: **Power Sequence Timing**

Size A2 Document Number: **M841 DVT** Rev: 0.1

Date: Friday, September 12, 2008 Sheet: 74 of 77

History (DVT)

2008/09/09

P71: Change the PQ76 from 17-2N70020-0000 to 17-2N7002P-T000 for PUR request

P64: Change the PR32 1R-0000203-F300 to 1R-0004532-F300 for power consumption

P20: For M841 SYS ID
Change R3901 from NC to stuff
Change R3774 from stuff to NC

P43: Add R38100,R38101for Q325 pin1 Q319 pin1 status

P44: Add R38102,LED9,Q350 for debug

P71 : Change the PC267,PC269 from 1C-2B30104-K000(0.1u) to 1C-2B30103-K000(0.01u) for new TV tuner Lyra

2008/09/11

P54: Add R38102,LED9,Q350 for debug

P60 : NC Q317,R38039,R987,Q66 for cost down

P46 : Stuff CRT

Change CN53 pin assignment for HIDEMI,
change pin 12 from GND to SUS_ON;
change Pin 14 from GND to INV_BRADJ;
change Pin 40 from TP to INV_ENABLE1;
change Pin 39 from GND to HIDEMI_DETECT;
Add R38108 1M ohm for HIDEMI_DETECT PD.

P33 : Add F26(NC) for CF test debug

P53 : Add U178,R38110,R38111 back up circuit for HIDEMI2 compatibility with HIDEMI 1 FW

2008/09/12

P30 : Change this circuit(U170,R37966,C2592,C2593,C2594,CN101,R37967) from NC to stuff for EU TV tuner evaluation

P70 : Change PD18,PD21 from 16-1SS355P-T000 to PD12 (CHN222PT)

Page53: Add F27 for safety request

Page44: change CN86,R37898 from NC to stuff for use CRT for debug

Page27: L145 main soure change 1T-INS6824-0300 to 1T-130F50L-0000(height:2.9mm),second source 1T-130F500-0000(height:2.5mm)

Page53: Add R38113(NC),R38114(stuff) , back up for HIDEMI debug

Page53: add 0 ohm R38115,R38116,R38117,R38118 at HIDEMI_SUS_ON, LCDVCC_EN, INV_ENABLE1, INV_BRADJ near HIDEMI connector

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Revision History(1)			
Title			
Size	Document Number	Rev	
A3	M841 DVT	0.1	
Date:	Tuesday, September 23, 2008	Sheet	75 of 77

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Title Revision History(2)		
Size A3	Document Number M841 DVT	Rev 0.1
Date: Thursday, September 11, 2008	Sheet 76	of 77

Title		
Revision History(3)		
Size A3	Document Number M841 DVT	Rev 0.1
Date:	Thursday, September 11, 2008	Sheet 77 of 77