

REVISION LIST

R0.7	2003/10/13	Only chipset circuit but not including DC to DC power circuit
R0.8	2003/10/31	Add Intel 82570 chipset circuit and TPM socket
R0.9	2003/11/04	Add AZALIA CMI9880 chipset circuit and ALS I/F
R0.95	2003/11/10	Key Board changed to OKI HMB989-C Matrix

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT1_IN#_OC	I	+3.3V
BAT2_IN#_OC	I	+3.3V
CHG_EN_OC	I	+3.3V
CHG_LED	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SMCLK_BAT2	IO	+3.3V
SMDATA_BAT2	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.5A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
+1.5VSUS	1.5V	270 mA
+1.8V	1.8V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	390 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 22 mils
IN1/IN3 16 mils

37.5 OHM WIDTH

TOP/BOT 13.5 mils
IN1/IN3 10 mils

42 OHM WIDTH

TOP/BOT 11 mils
IN1/IN3 8.5 mils

55 OHM WIDTH

TOP/BOT 6 mils
IN1/IN3 5 mils

75 OHM WIDTH

TOP/BOT 2.5 mils
IN1/IN3 2 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 8 mils/ 4 mils
IN1/IN3 8 mils/ 3.5 mils

90 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 5 mils
IN1/IN3 5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 4 mils/ 6 mils
IN1/IN3 4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#1
MINIPCI PCI_REQ#3

IDSEL

CB&1394 PCI_AD17
MINIPCI PCI_AD19

PCIE Device

PEG

ATI M24

PCIE Giga NIC

Intel 82570EI

PCB STACK-UP

PCB THICKNESS: 1.2 mm

- L1 TOP
- L2 GND1
- L3 IN1
- L4 IN2
- L5 VCC
- L6 IN3
- L7 GND2
- L8 BOT

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SIGNAL	IN:	VR_VID0 - 5 PM DPRSLPVR STP_CPU# PM_PSI# IMVP_VR_ON
	OUT:	DELAY_VR_PWRGD VR_PWDGD_CK410#
POWER	IN:	AC_BAT_SYS +5VO +3VO
	OUT:	+VCORE

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SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12VO +3VO +5VO

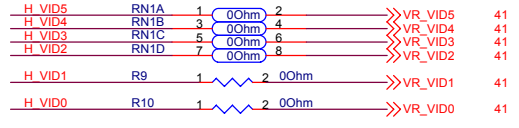
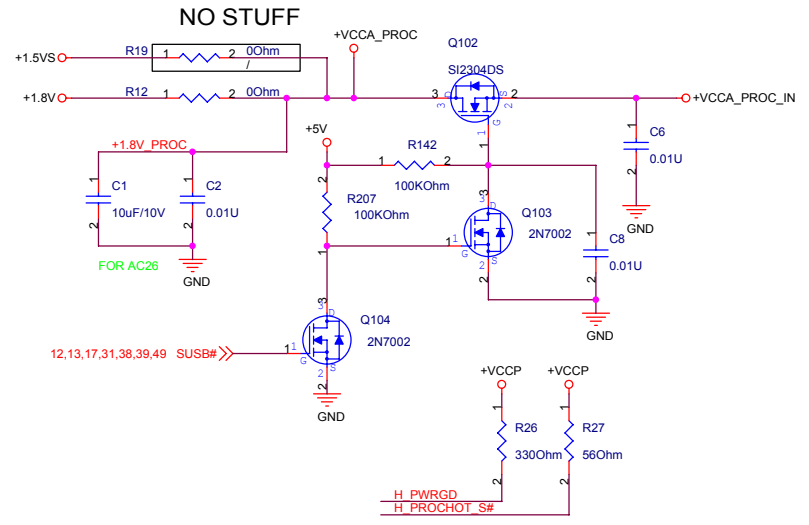
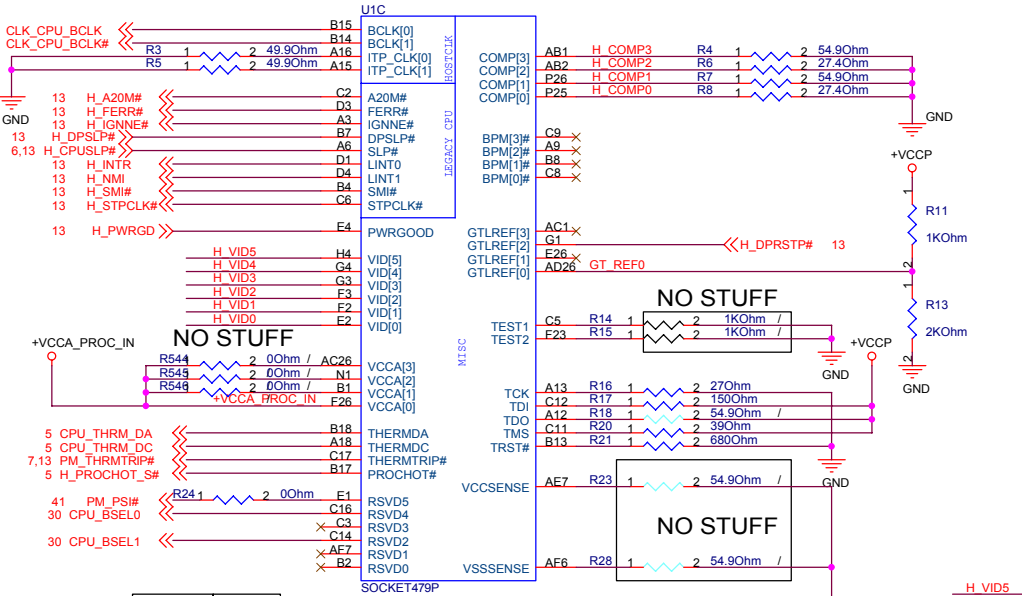
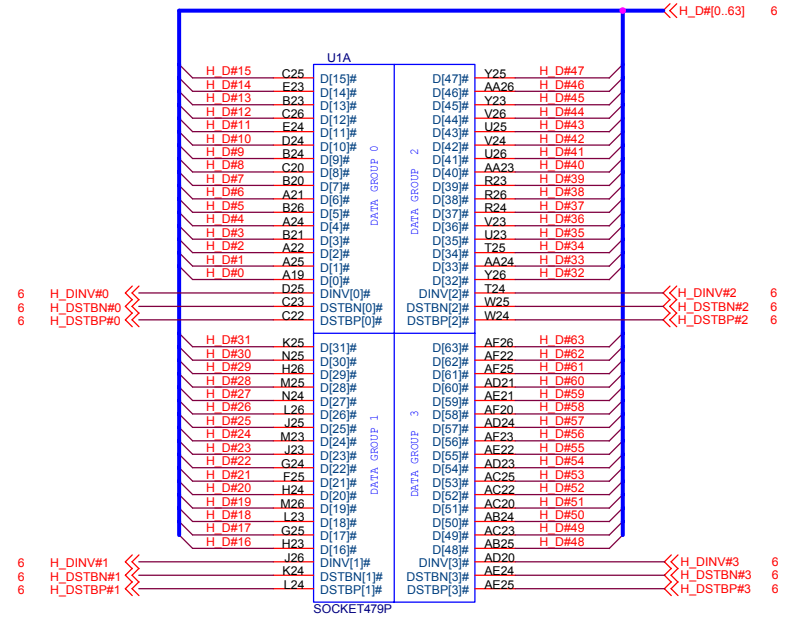
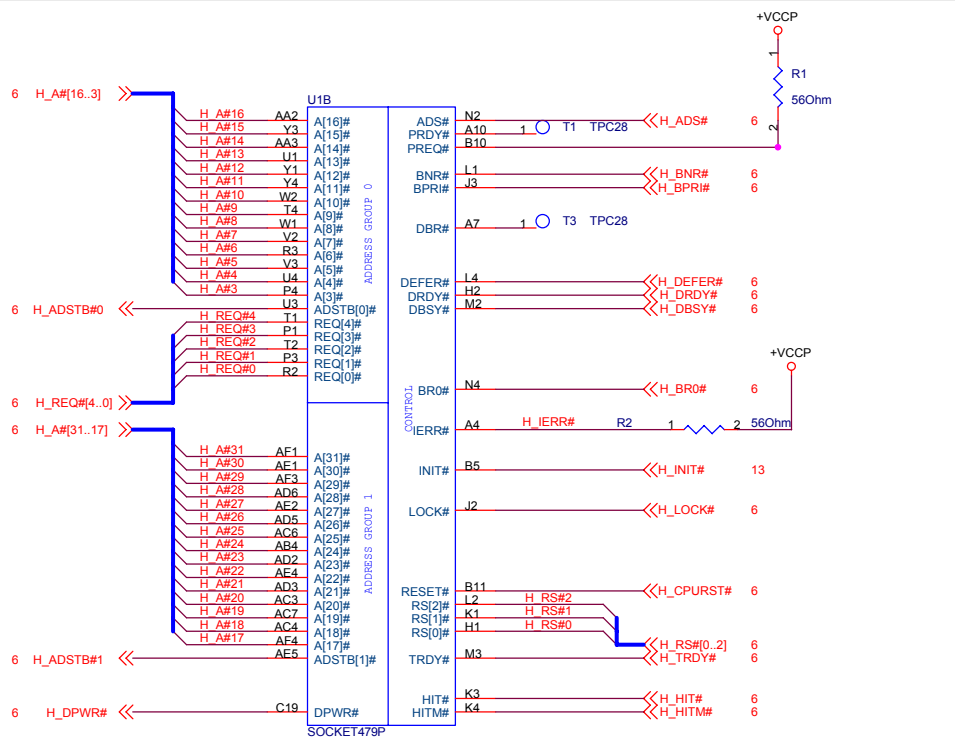
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SIGNAL	IN:	SUSB#_PWR SUSC#_PWR
POWER	IN:	AC_BAT_SYS +3VO
	OUT:	+1.8V +1.5V +2.5V +VCC_GMCH_CORE +5VALWAYS +3VALWAYS

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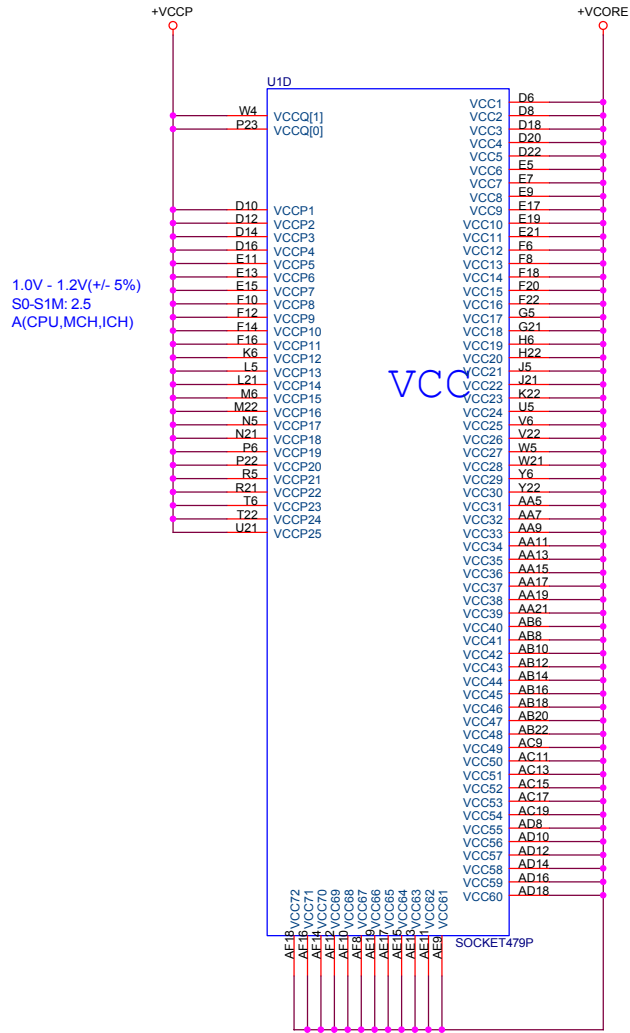
SIGNAL	IN:	SUSB#_PWR
	OUT:	VCC_MCH_VRPWRGD IMVP_VR_ON
POWER	IN:	+3VA +3V +1.8V +VCC_GMCH_CORE
	OUT:	+0.9VS +1.5VA +VCCP

		Title : REVISION LIST	
ASUSTeK COMPUTER INC		Engineer: Frank Lu	
Size	Project Name		Rev
Custom	M7V		0.95
Date: Monday, November 10, 2003	Sheet	2	of 51



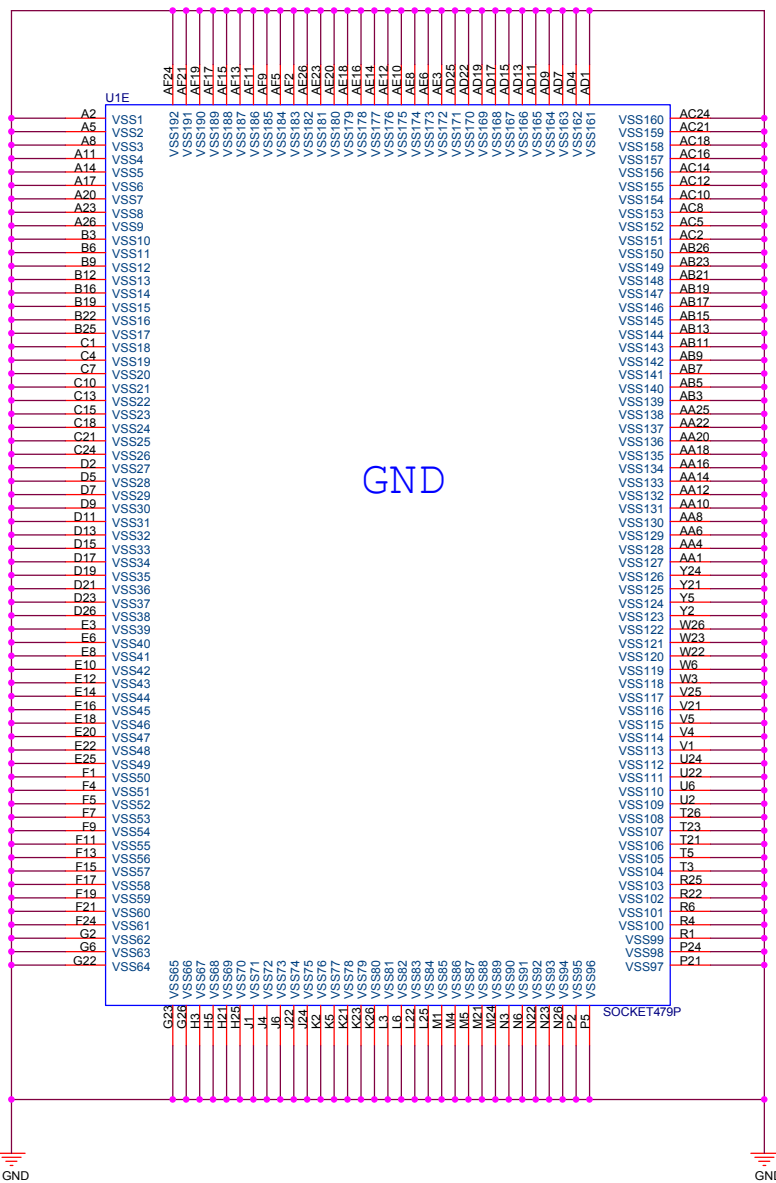
	A-STEP	B-STEP	
	FSB	BSEL1	BSEL0
400	0	0	1
533	0	1	0

ASUS Title : **DOTHAN CPU (1)**
 ASUSTek COMPUTER INC Engineer: **Frank Lu**
 Size Project Name
 Custom **M7V** Rev **0.95**
 Date: Monday, November 10, 2003 Sheet 3 of 51



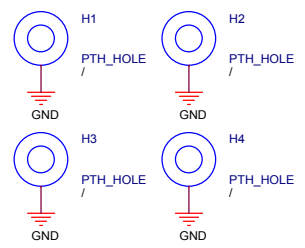
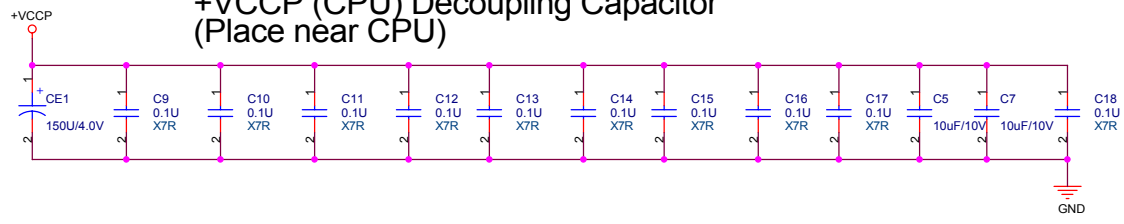
1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

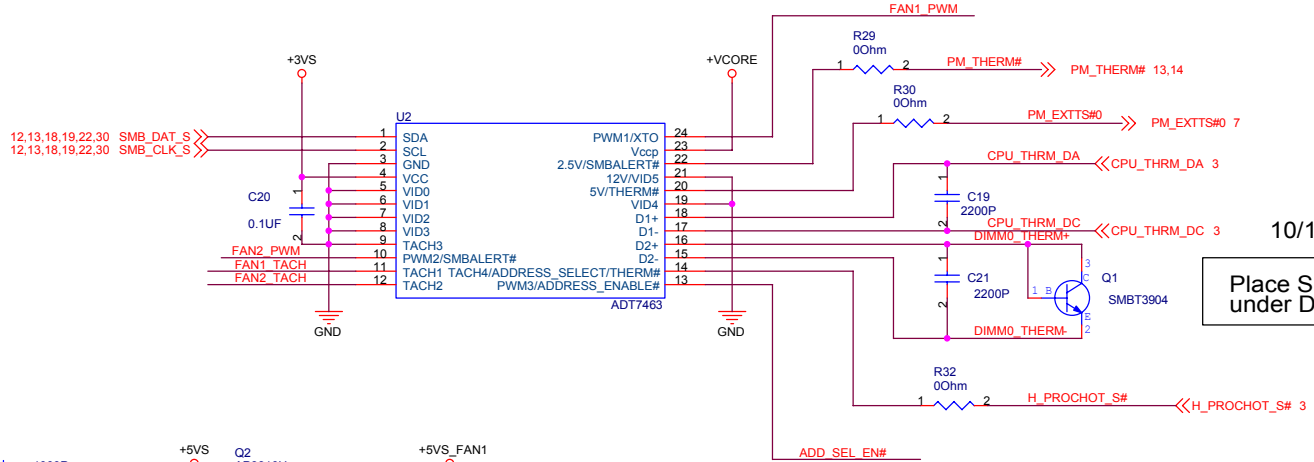
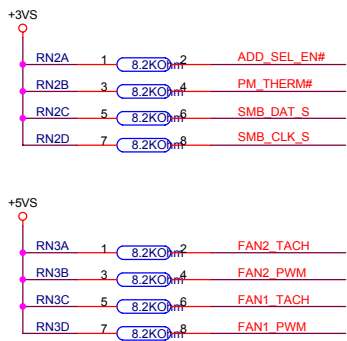
0.745V - 1.356V(+/- 1.5%)
C0: 27 A
C3: 7.59A
C4: 0.9A



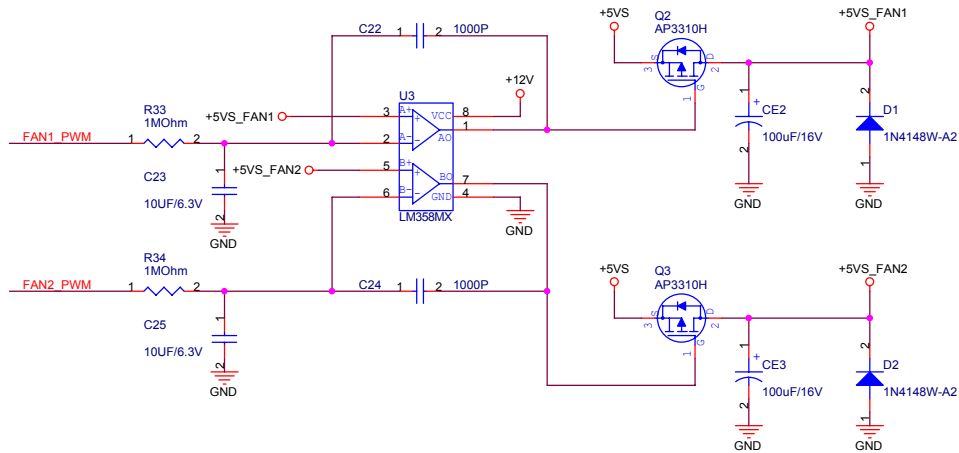
GND

**+VCCP (CPU) Decoupling Capacitor
(Place near CPU)**

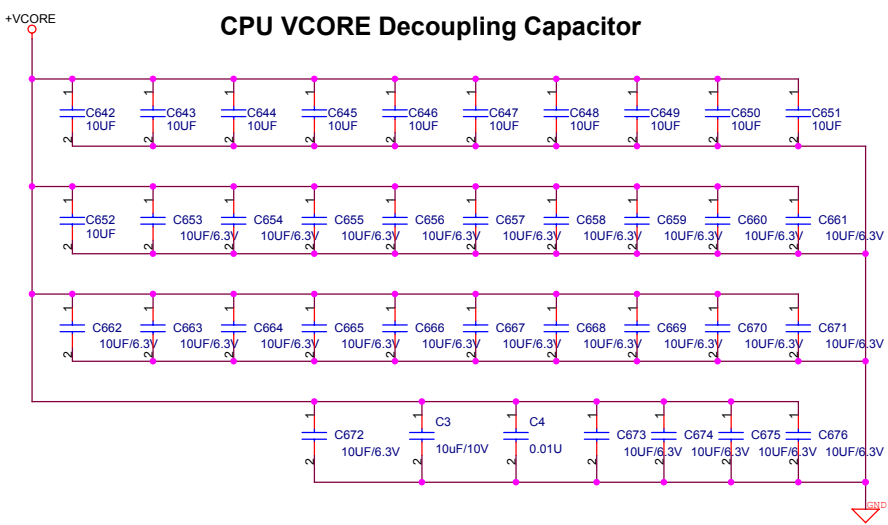
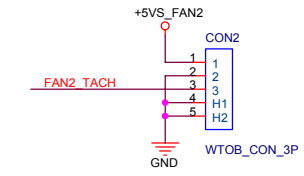
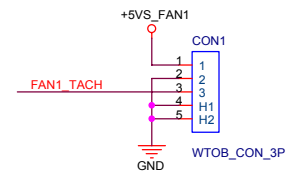




Place SMBT3904 under DIMM0



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

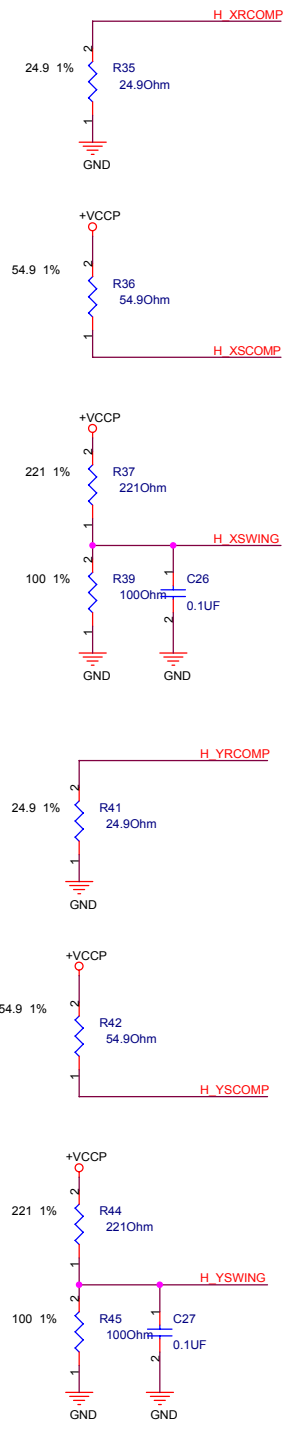


Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+V CORE Bulk Decoupling

Four 200 uF are located in IMVP4



3 H_D#[0..63]

U4D

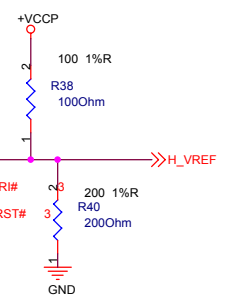
H D#0	F4	HD0#
H D#1	F1	HD1#
H D#2	F4	HD2#
H D#3	H7	HD3#
H D#4	E2	HD4#
H D#5	F1	HD5#
H D#6	E3	HD6#
H D#7	D3	HD7#
H D#8	K7	HD8#
H D#9	F2	HD9#
H D#10	J7	HD10#
H D#11	J8	HD11#
H D#12	H6	HD12#
H D#13	F3	HD13#
H D#14	K8	HD14#
H D#15	K8	HD15#
H D#16	H1	HD16#
H D#17	H2	HD17#
H D#18	K5	HD18#
H D#19	K6	HD19#
H D#20	J4	HD20#
H D#21	G3	HD21#
H D#22	H3	HD22#
H D#23	J1	HD23#
H D#24	L5	HD24#
H D#25	K4	HD25#
H D#26	J5	HD26#
H D#27	P7	HD27#
H D#28	L7	HD28#
H D#29	J3	HD29#
H D#30	P5	HD30#
H D#31	L3	HD31#
H D#32	U7	HD32#
H D#33	V6	HD33#
H D#34	R6	HD34#
H D#35	R5	HD35#
H D#36	P3	HD36#
H D#37	T8	HD37#
H D#38	R7	HD38#
H D#39	R8	HD39#
H D#40	U8	HD40#
H D#41	R4	HD41#
H D#42	T4	HD42#
H D#43	T5	HD43#
H D#44	R1	HD44#
H D#45	T3	HD45#
H D#46	V8	HD46#
H D#47	U6	HD47#
H D#48	W6	HD48#
H D#49	U3	HD49#
H D#50	V5	HD50#
H D#51	W8	HD51#
H D#52	W7	HD52#
H D#53	U2	HD53#
H D#54	L1	HD54#
H D#55	Y5	HD55#
H D#56	Y2	HD56#
H D#57	V4	HD57#
H D#58	Y7	HD58#
H D#59	W1	HD59#
H D#60	Y3	HD60#
H D#61	Y6	HD61#
H D#62	Y6	HD62#
H D#63	W2	HD63#

HOST

HA3#	G9	H A#3
HA4#	C9	H A#4
HA5#	E9	H A#5
HA6#	B7	H A#6
HA7#	A10	H A#7
HA8#	F9	H A#8
HA9#	D8	H A#9
HA10#	B10	H A#10
HA11#	E10	H A#11
HA12#	D9	H A#12
HA13#	E11	H A#13
HA14#	F10	H A#14
HA15#	G11	H A#15
HA16#	G13	H A#16
HA17#	C10	H A#17
HA18#	C11	H A#18
HA19#	D11	H A#19
HA20#	C12	H A#20
HA21#	B13	H A#21
HA22#	A12	H A#22
HA23#	F12	H A#23
HA24#	G12	H A#24
HA25#	E12	H A#25
HA26#	C13	H A#26
HA27#	B11	H A#27
HA28#	D13	H A#28
HA29#	A13	H A#29
HA30#	H A#30	
HA31#	F13	H A#31

H ADS#	F8	H ADS#	<<<	H_ADS#	3
H ADSTB#0	B9	H ADSTB#0	<<<	H_ADSTB#0	3
H ADSTB#1	E13	H ADSTB#1	<<<	H_ADSTB#1	3
HVREF	J11	H_BNR#	<<<	H_BNR#	3
HBNR#	A5	H_BPR#	<<<	H_BPR#	3
HBPR#	E7	H_BREQ#0	<<<	H_BPR#	3
H_BREQ#0	H10	H_CPURST#	<<<	H_BRO#	3
HCPURST#	H10	H_CPURST#	<<<	H_CPURST#	3

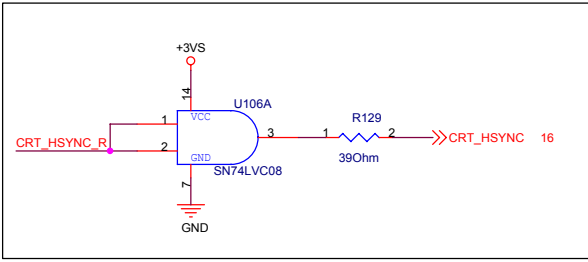
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HCLKINP	AB2	CLK_MCH_BCLK# 30	<<<	H_DIN#0	3
HDBSY#	C6	H_DBSY#	<<<	H_DIN#1	3
HDEFER#	E6	H_DBSY#	<<<	H_DIN#2	3
HDINV#0	H8	H_DIN#0	<<<	H_DIN#3	3
HDINV#1	K3	H_DIN#1	<<<	H_DPWR#	3
HDINV#2	T7	H_DIN#2	<<<	H_DRDY#	3
HDINV#3	U5	H_DIN#3	<<<	H_DSTBN#0	3
HDPWR#	G6	H_DRDY#	<<<	H_DSTBN#1	3
HDRDY#	F7	H_DRDY#	<<<	H_DSTBN#2	3
HDSTBN#0	G4	H_DSTBN#0	<<<	H_DSTBN#3	3
HDSTBN#1	K1	H_DSTBN#1	<<<	H_DSTBP#0	3
HDSTBN#2	R3	H_DSTBN#2	<<<	H_DSTBP#1	3
HDSTBN#3	V3	H_DSTBN#3	<<<	H_DSTBP#2	3
HDSTBP#0	G5	H_DSTBP#0	<<<	H_DSTBP#3	3
HDSTBP#1	D6	H_DSTBP#1	<<<	H_HIT#	3
HDSTBP#2	R2	H_DSTBP#2	<<<	H_HITM#	3
HDSTBP#3	W4	H_DSTBP#3	<<<	H_LOCK#	3
HEDRDY#	F6	TP H_EDRDY#	<<<	H_PCREQ#	3
H_HIT#	D4	H_HIT#	<<<	H_REQ#0	3
H_HITM#	B3	H_HITM#	<<<	H_REQ#1	3
H_LOCK#	A11	TP H_PCREQ#	<<<	H_REQ#2	3
HPCREQ#	A11	TP H_PCREQ#	<<<	H_REQ#3	3
HREQ#0	A7	H_REQ#0	<<<	H_REQ#4	3
HREQ#1	D7	H_REQ#1	<<<	H_RS#0	3
HREQ#2	B8	H_REQ#2	<<<	H_RS#1	3
HREQ#3	C7	H_REQ#3	<<<	H_RS#2	3
HREQ#4	A8	H_REQ#4	<<<	H_RS#2	3
HRS#0	A4	H_RS#0	<<<	H_CPUSLP#	3,13
HRS#1	C5	H_RS#1	<<<	H_TRDY#	3
HRS#2	B4	H_RS#2	<<<		
HCPUSLP#	G8	R43 1 2 00hm	<<<		
HTRDY#	B5	H_TRDY#	<<<		



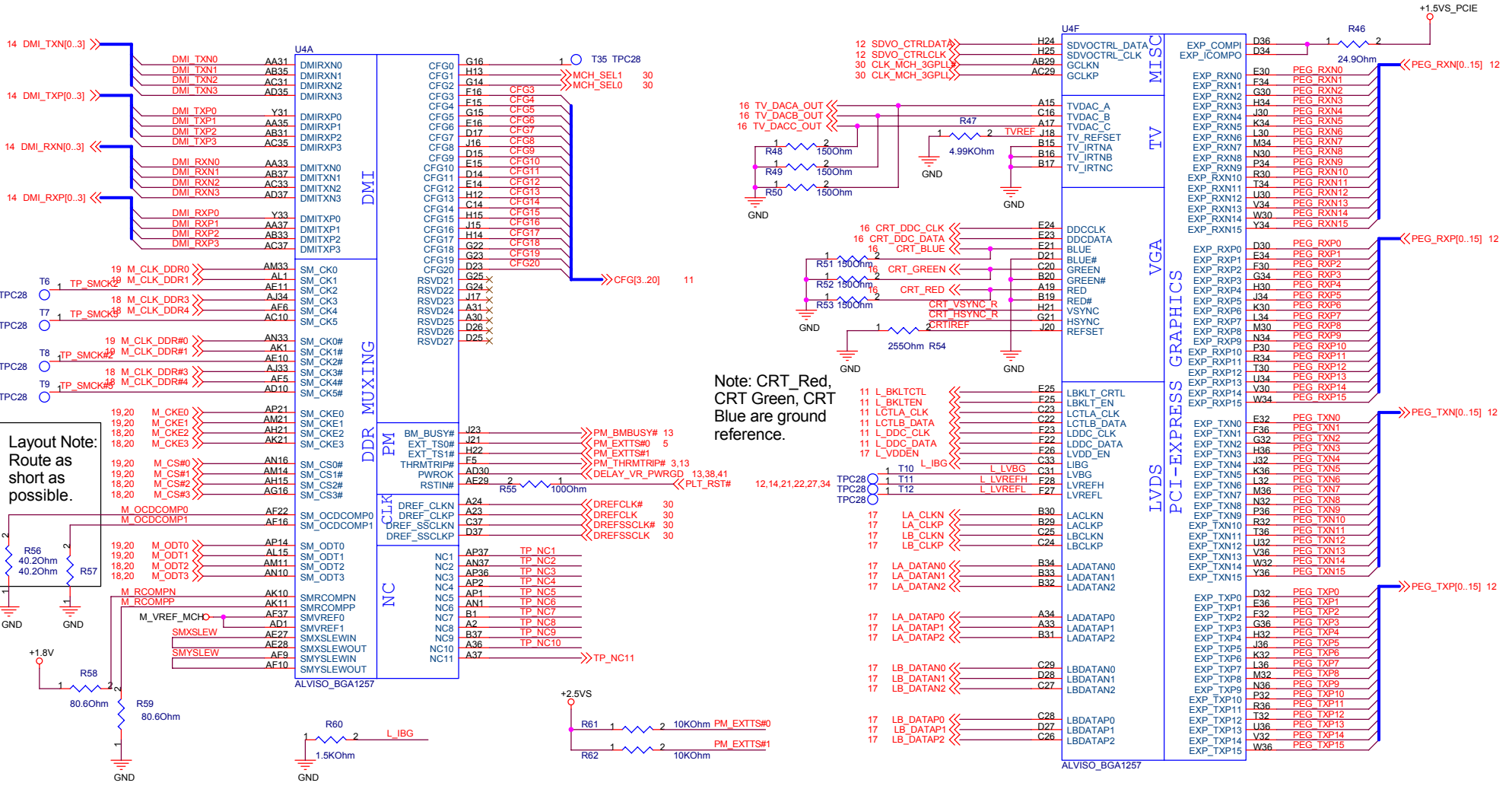
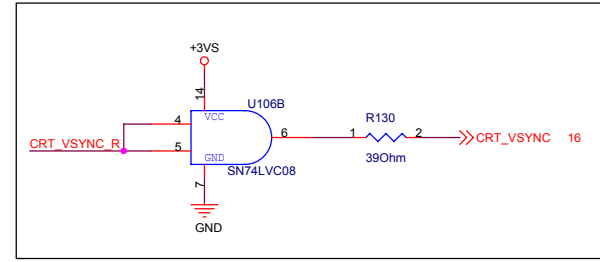
R43 NO STUFF

ALVISO_BGA1257

74LVC08 CLOSE to ALVISO



74LVC08 CLOSE to ALVISO

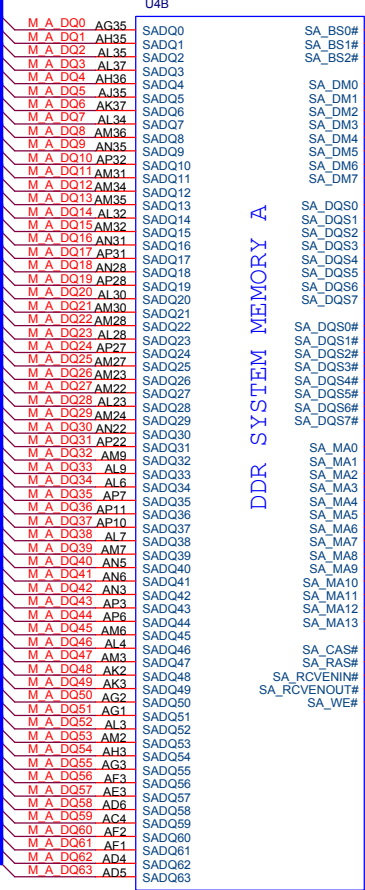


Layout Note:
Route as short as possible.

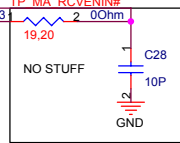
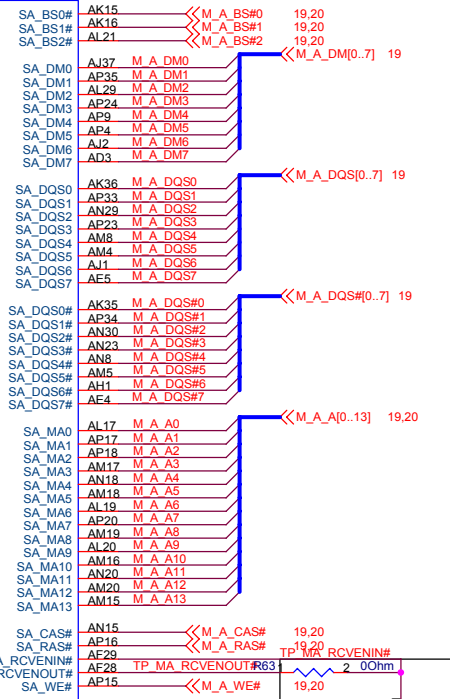
Note: CRT_Red, CRT Green, CRT Blue are ground reference.

ASUS		Title : Alviso GMCH (2)	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size Custom	Project Name M7V	Rev 0.95	
Date: Monday, November 10, 2003		Sheet 7 of 51	

19 M_A_DQ[0..63] >>

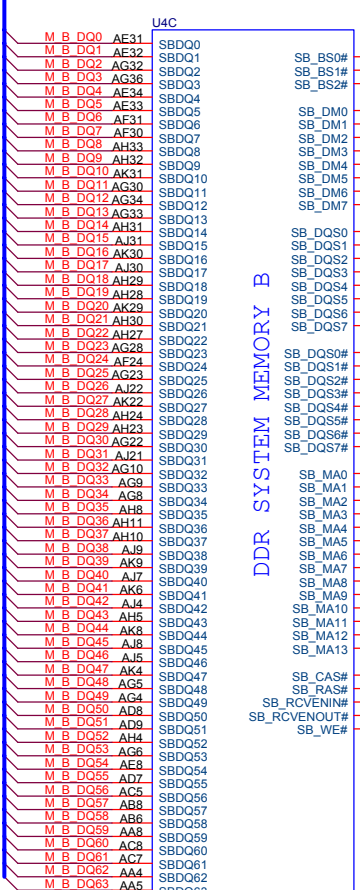


DDR SYSTEM MEMORY A

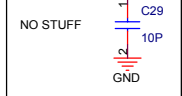
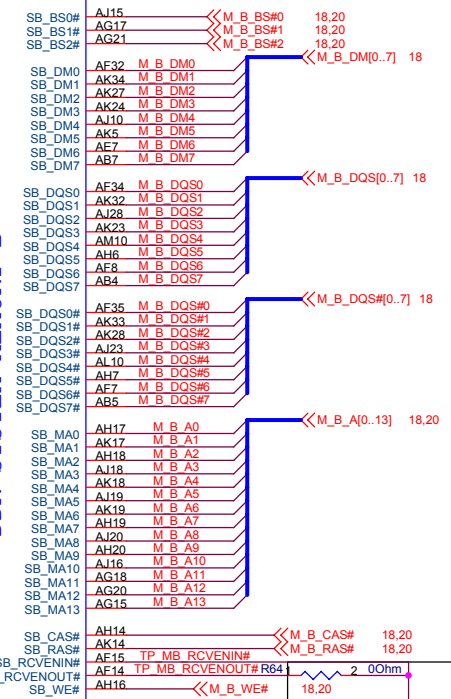


ALVISO_BGA1257

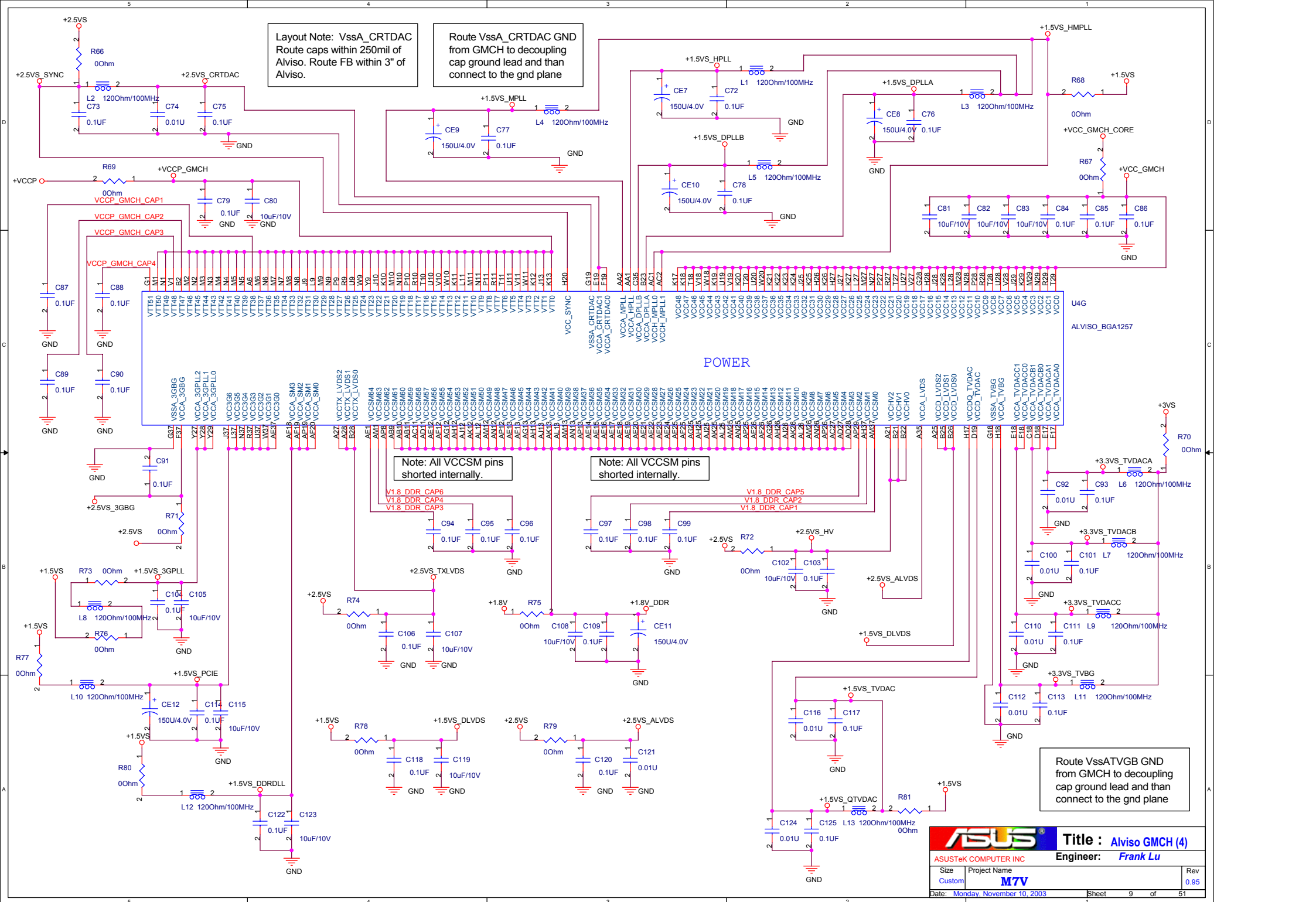
18 M_B_DQ[0..63] >>



DDR SYSTEM MEMORY B



ALVISO_BGA1257



Layout Note: Vssa_CRTDAC
Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

Route Vssa_CRTDAC GND from GMCH to decoupling cap ground lead and then connect to the gnd plane

Note: All VCCSM pins shorted internally.

Note: All VCCSM pins shorted internally.

Route VssaTVGB GND from GMCH to decoupling cap ground lead and then connect to the gnd plane

ASUS		Title : Alviso GMCH (4)	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size Custom	Project Name M7V	Rev 0.95	
Date: Monday, November 10, 2003		Sheet 9 of 51	

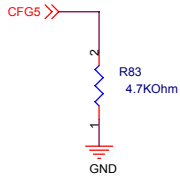


SSA

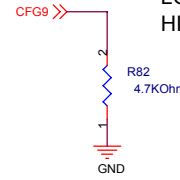
NCTF

ASUS		Title : Alviso GMCH (5)	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size Custom	Project Name M7V	Rev 0.95	
Date: Monday, November 10, 2003		Sheet 10 of 51	

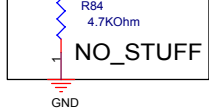
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



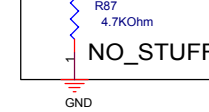
CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



CFG18 : VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



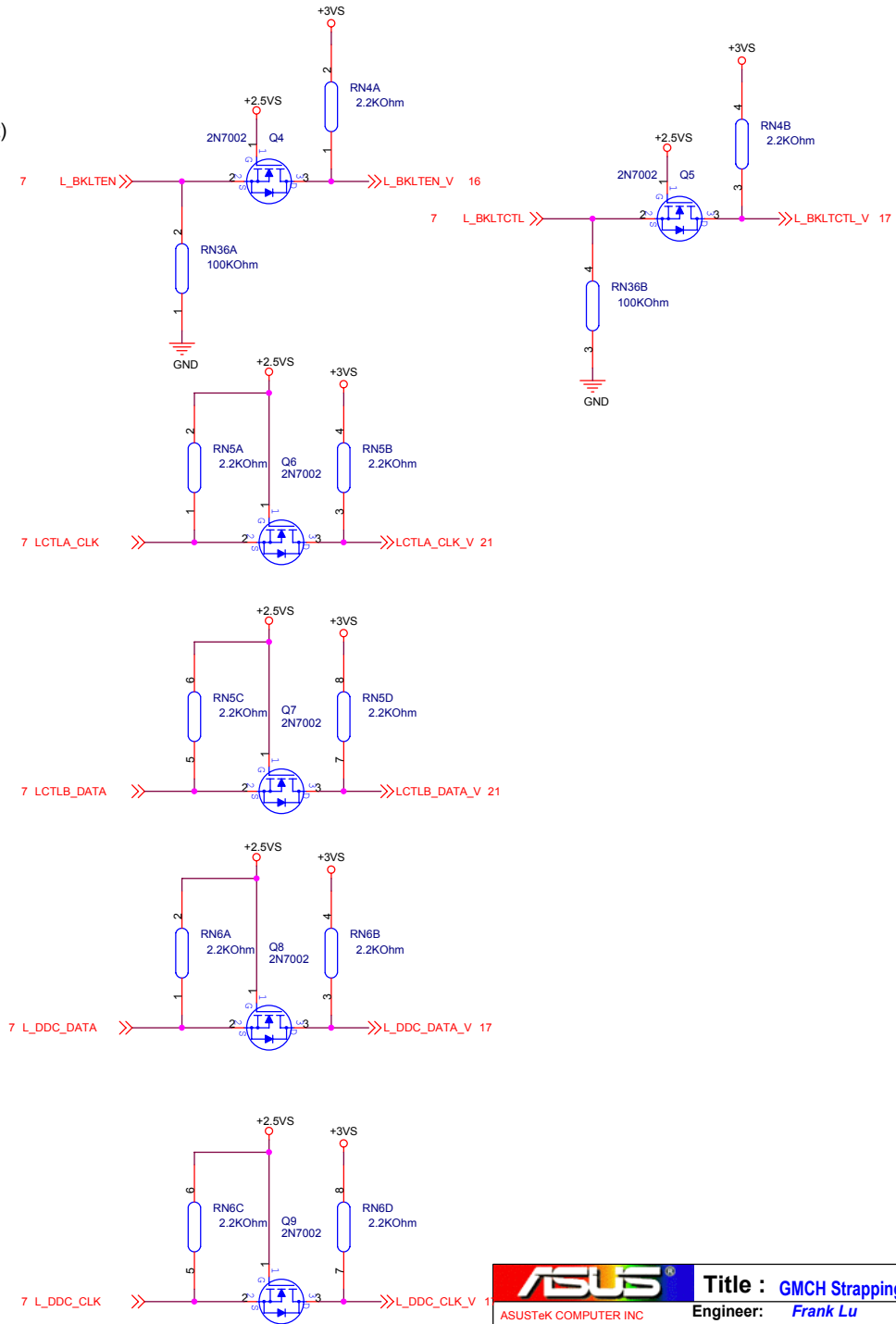
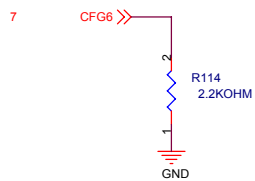
CFG19 : VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V

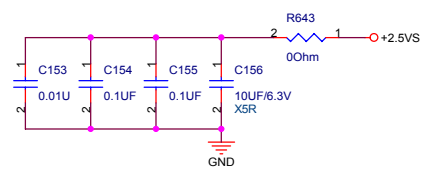
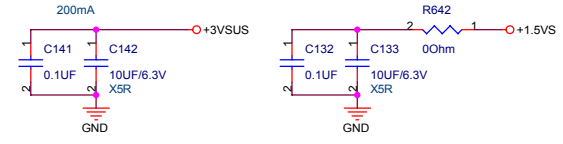
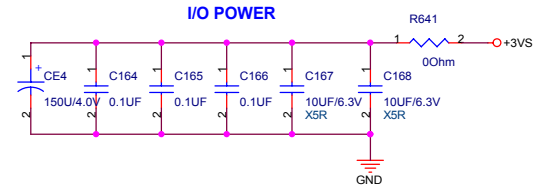
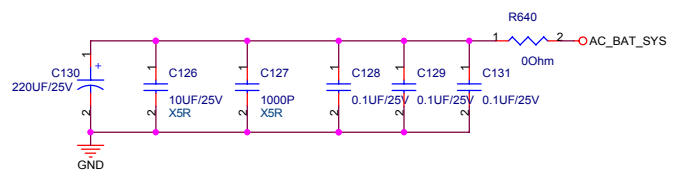
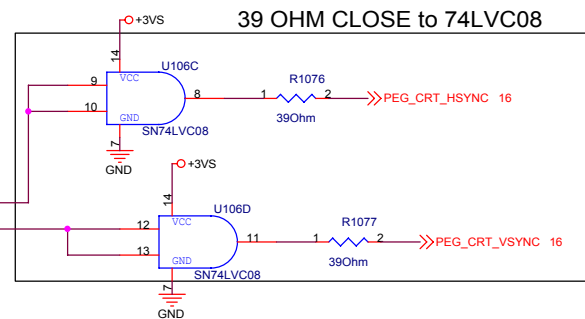
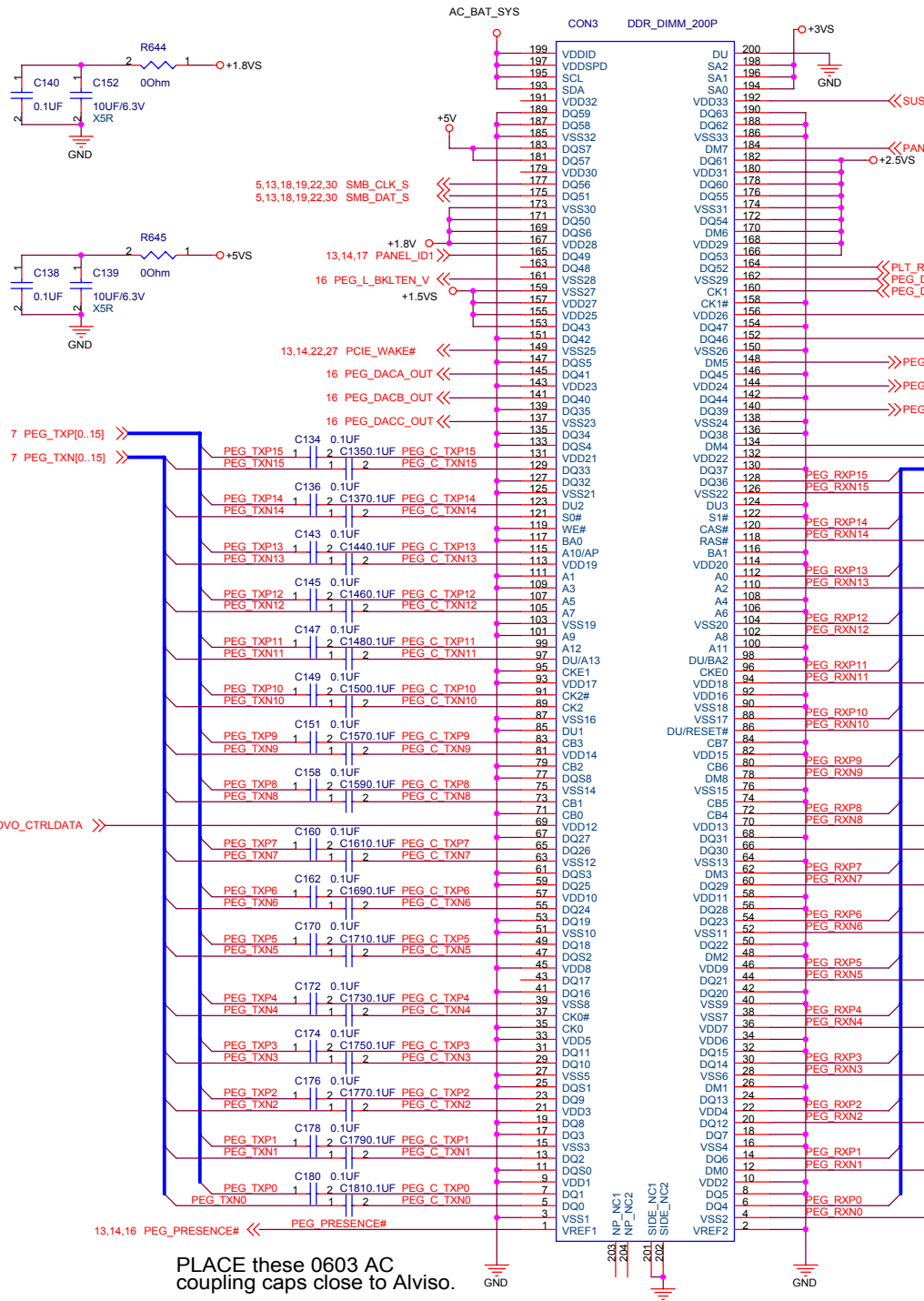


CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.

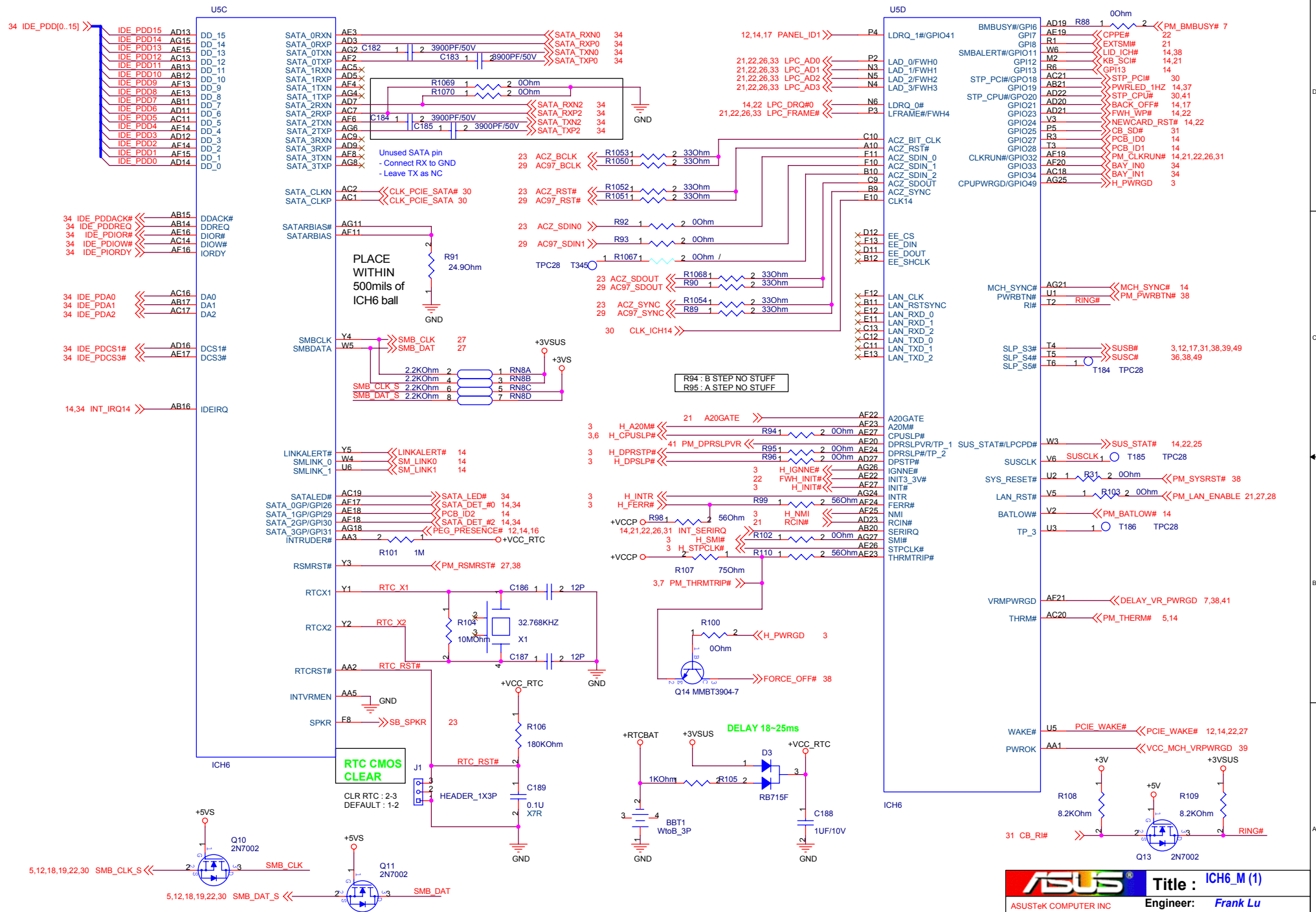
SDVOCRTL_DATA LOW = No SDVO device present (Default)

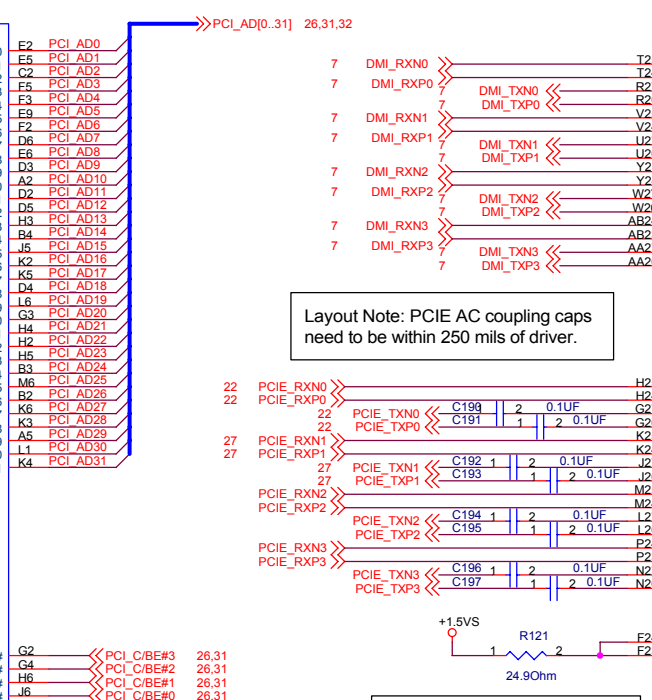
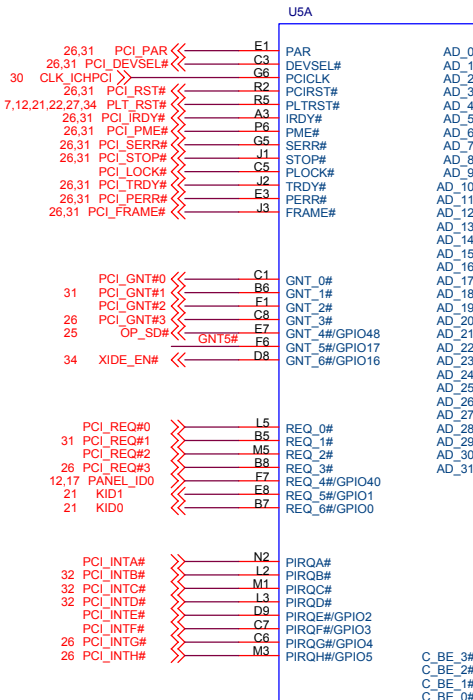
CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)





PLACE these 0603 AC coupling caps close to Alviso.

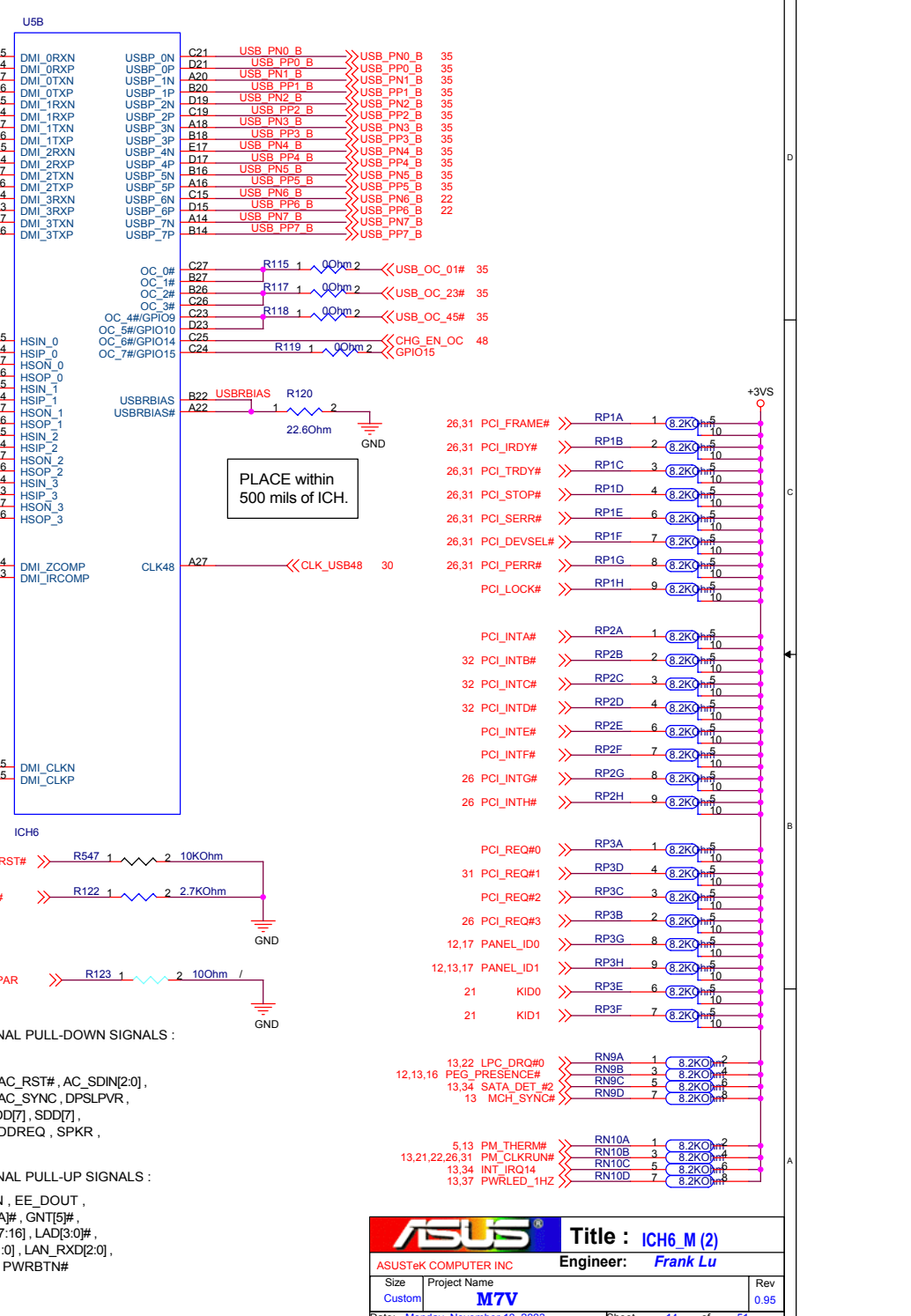
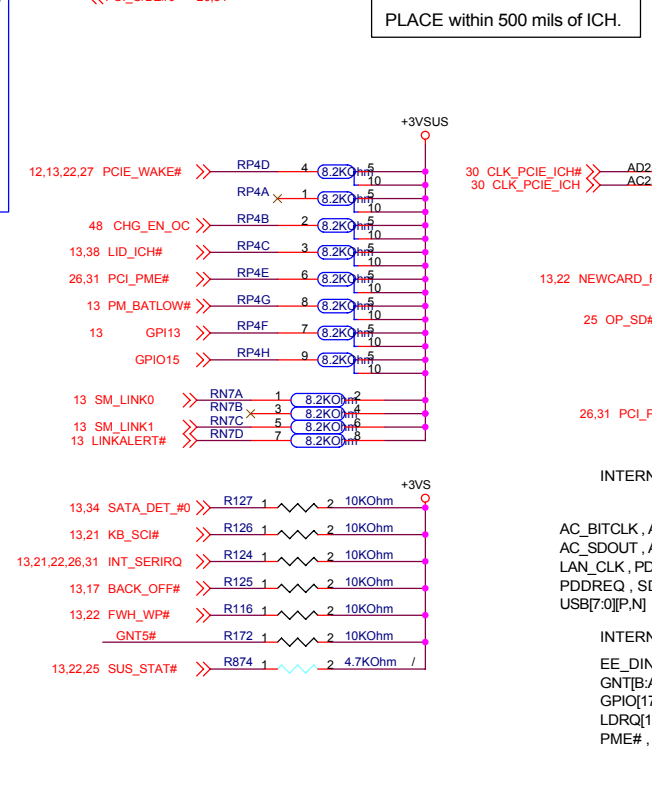
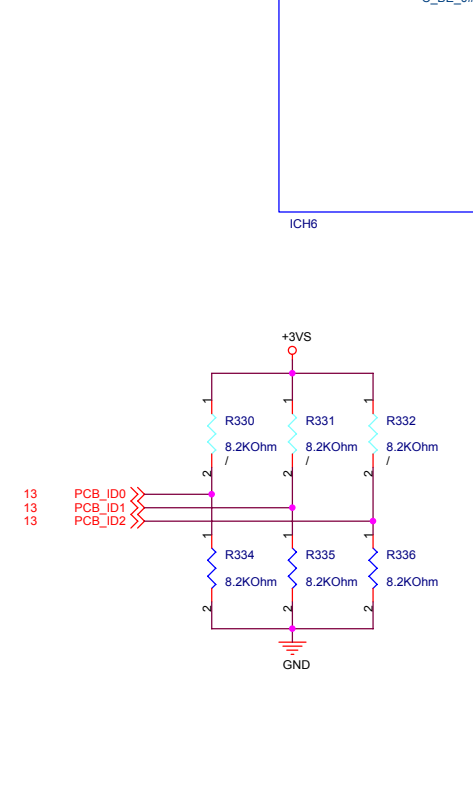




Layout Note: PCIE AC coupling caps need to be within 250 mils of driver.

PLACE within 500 mils of ICH.

PLACE within 500 mils of ICH.



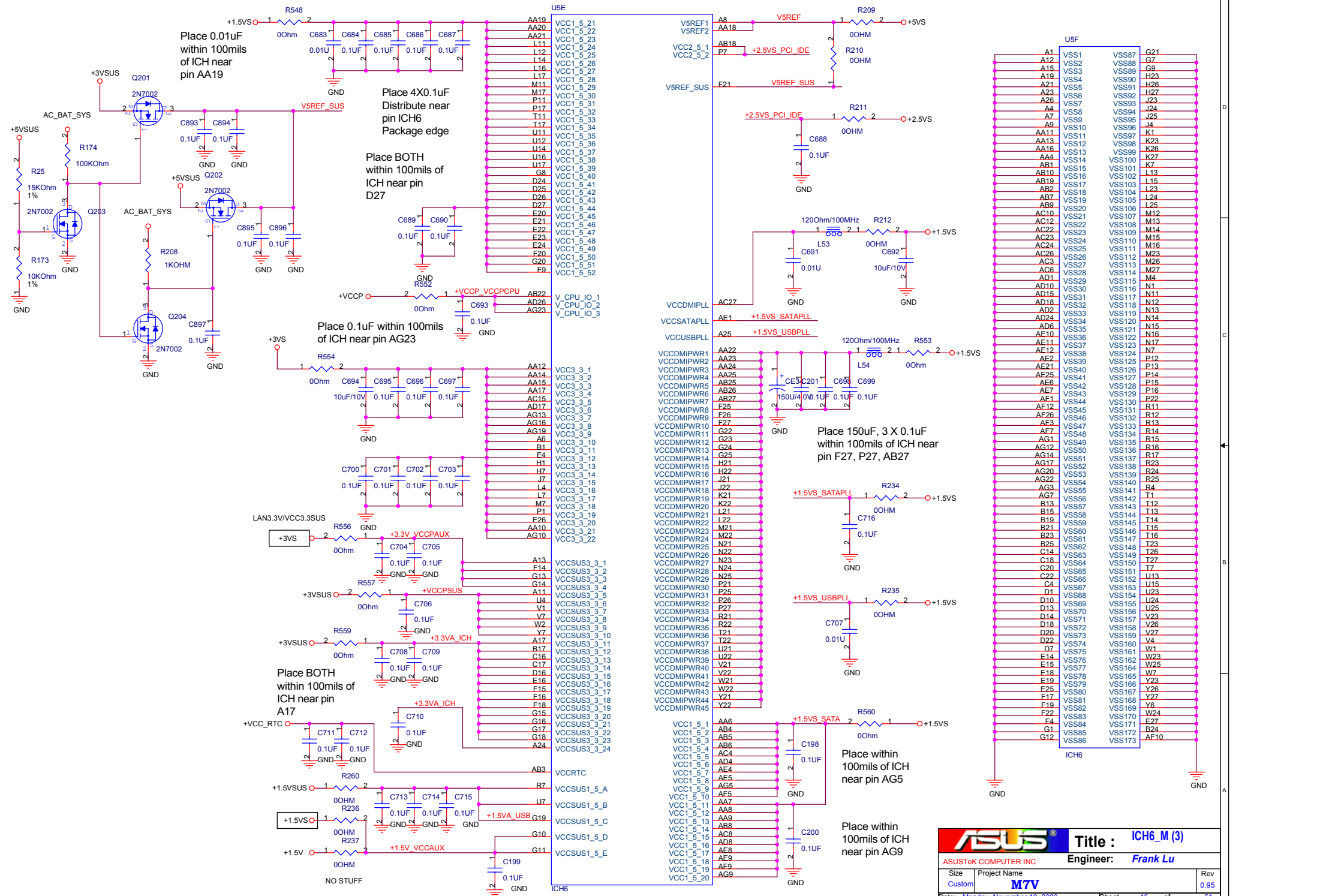
INTERNAL PULL-DOWN SIGNALS :
 AC_BITCLK, AC_RST#, AC_SDIN[2,0], AC_SDOUT, AC_SYNC, DPSL_PVR, LAN_CLK, PDD[7], SDD[7], PDDREQ, SDDREQ, SPKR, USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
 EE_DIN, EE_DOUT, GNT[B:A]#, GNT[5]#, GPIO[17:16], LAD[3:0]#, LDRQ[1:0], LAN_RXD[2:0], PME#, PWRBTN#

ASUS Title : **ICH6_M (2)**
 ASUSTek COMPUTER INC Engineer: **Frank Lu**

Size	Project Name	Rev
Custom	M7V	0.95

Date: Monday, November 10, 2003 Sheet 14 of 51



Place 0.01uF within 100mils of ICH near pin AA19

Place 4X0.1uF Distribute near pin ICH6 Package edge

Place BOTH within 100mils of ICH near pin D27

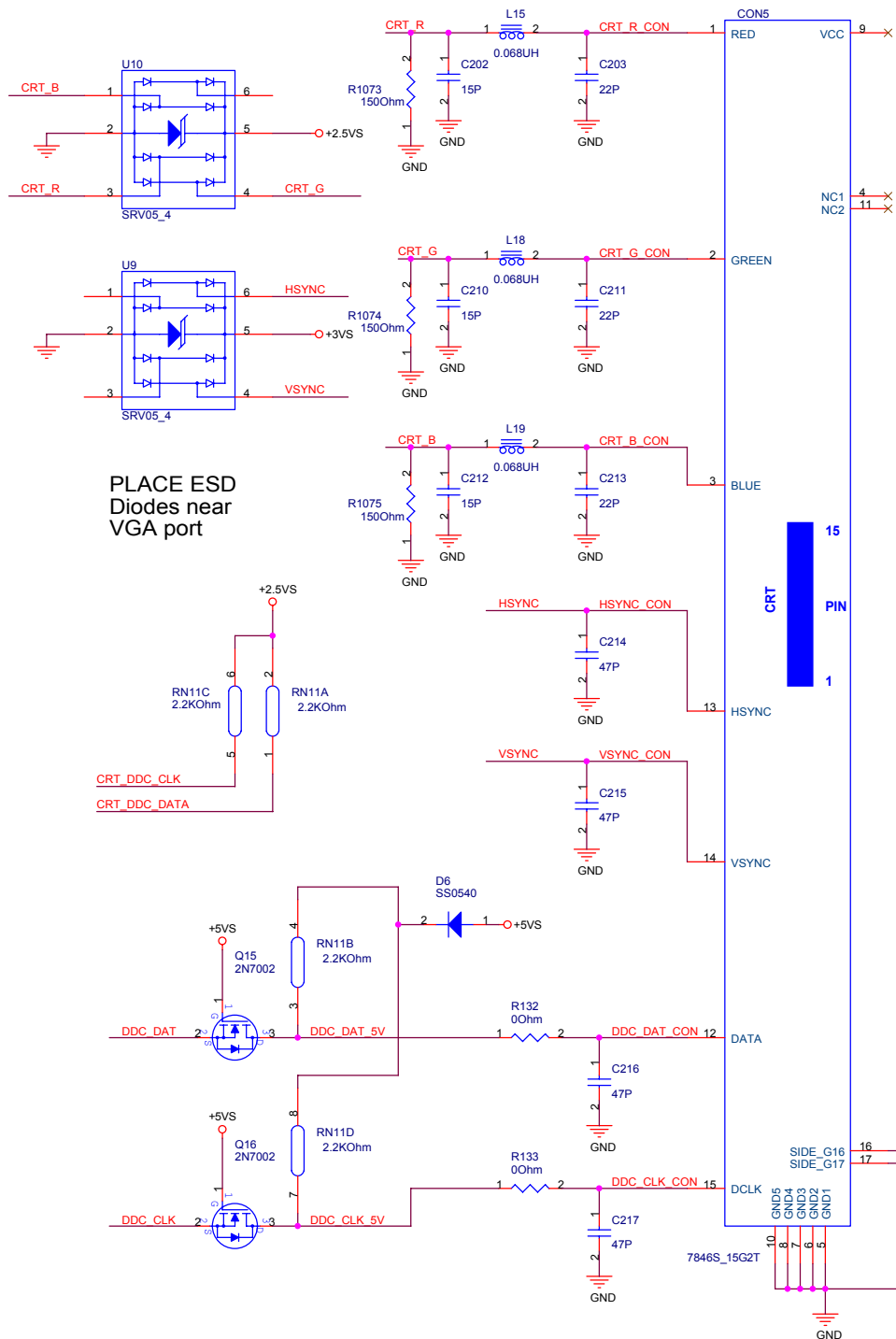
Place 0.1uF within 100mils of ICH near pin AG23

Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27

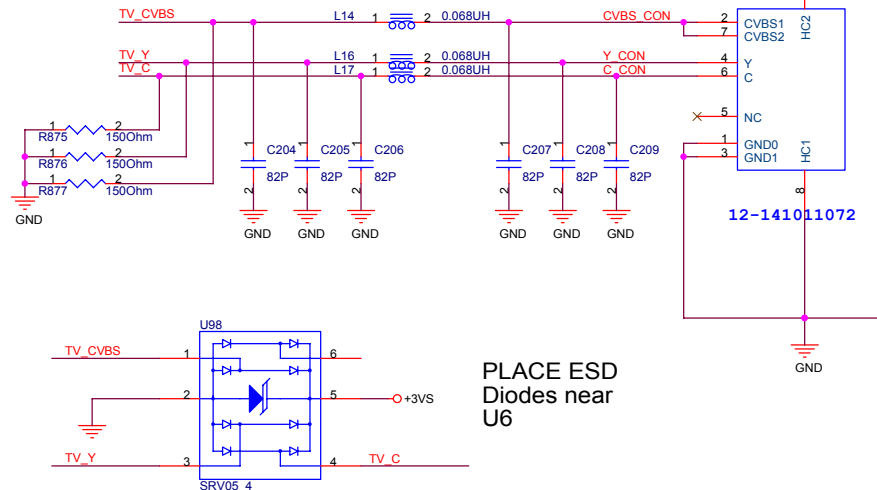
Place within 100mils of ICH near pin AG5

Place within 100mils of ICH near pin AG9

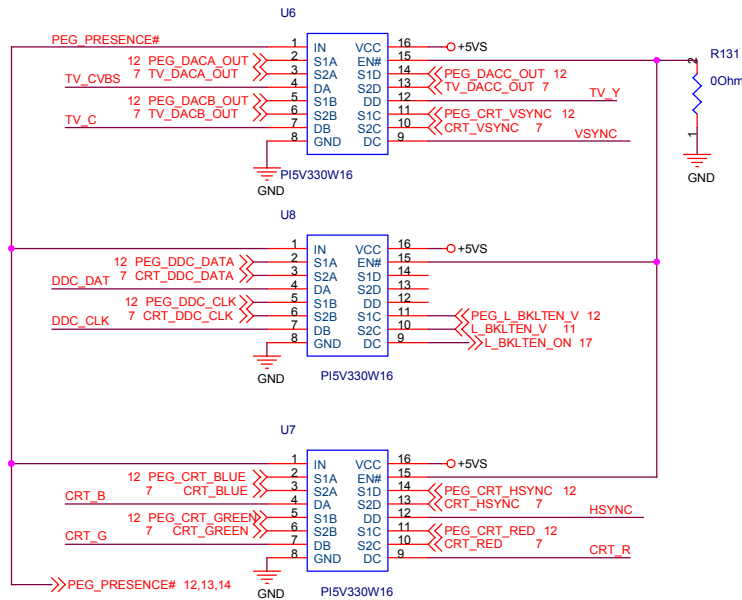
U5F		ICH6	
A1	VSS1	VSS87	G21
A12	VSS2	VSS88	G7
A15	VSS3	VSS89	G9
A19	VSS4	VSS90	H23
A21	VSS5	VSS91	H26
A23	VSS6	VSS92	H27
A26	VSS7	VSS93	J23
A4	VSS8	VSS94	J24
A7	VSS9	VSS95	J25
A9	VSS10	VSS96	K1
AA11	VSS11	VSS97	K23
AA13	VSS12	VSS98	K26
AA16	VSS13	VSS99	K27
AA4	VSS14	VSS100	K7
AB1	VSS15	VSS101	L13
AB10	VSS16	VSS102	L15
AB19	VSS17	VSS103	L23
AB7	VSS18	VSS104	L24
AB9	VSS19	VSS105	L25
AC10	VSS21	VSS107	M12
AC12	VSS22	VSS108	M13
AC22	VSS23	VSS109	M14
AC23	VSS24	VSS110	M15
AC24	VSS25	VSS111	M16
AC26	VSS26	VSS112	M23
AC3	VSS27	VSS113	M26
AC6	VSS28	VSS114	M27
AD1	VSS29	VSS115	M4
AD10	VSS30	VSS116	M4
AD15	VSS31	VSS117	M11
AD18	VSS32	VSS118	M12
AD2	VSS33	VSS119	M13
AD24	VSS34	VSS120	M14
AD6	VSS35	VSS121	M15
AE10	VSS36	VSS122	M16
AE11	VSS37	VSS123	M17
AE12	VSS38	VSS124	N7
AE2	VSS39	VSS125	P12
AE25	VSS40	VSS126	P13
AE6	VSS41	VSS127	P14
AE7	VSS42	VSS128	P16
AF1	VSS43	VSS129	P22
AF12	VSS44	VSS130	R11
AF26	VSS45	VSS131	R12
AF3	VSS46	VSS132	R12
AF7	VSS47	VSS133	R13
AG1	VSS48	VSS134	R14
AG12	VSS49	VSS135	R15
AG14	VSS50	VSS136	R17
AG17	VSS51	VSS137	R23
AG20	VSS52	VSS138	R24
AG22	VSS53	VSS139	R24
AG3	VSS54	VSS140	R25
AG7	VSS55	VSS141	R4
B13	VSS56	VSS142	T1
B15	VSS57	VSS143	T12
B19	VSS58	VSS144	T13
B21	VSS59	VSS145	T14
B23	VSS60	VSS146	T15
B25	VSS61	VSS147	T16
C14	VSS62	VSS148	T26
C18	VSS63	VSS149	T27
C20	VSS64	VSS150	T7
C22	VSS65	VSS151	T7
C4	VSS66	VSS152	U13
D1	VSS67	VSS153	U15
D10	VSS68	VSS154	U23
D13	VSS69	VSS155	U24
D14	VSS70	VSS156	U25
D18	VSS71	VSS157	V23
D19	VSS72	VSS158	V26
D20	VSS73	VSS159	V27
D22	VSS74	VSS160	V4
D7	VSS75	VSS161	W1
E14	VSS76	VSS162	W23
E15	VSS77	VSS163	W25
E18	VSS78	VSS164	W7
E19	VSS79	VSS165	Y23
E25	VSS80	VSS166	Y26
F17	VSS81	VSS167	Y27
F19	VSS82	VSS168	Y6
F22	VSS83	VSS169	W24
F4	VSS84	VSS170	E27
G1	VSS85	VSS171	B24
G12	VSS86	VSS172	AF10



PLACE ESD Diodes near VGA port



PLACE ESD Diodes near U6

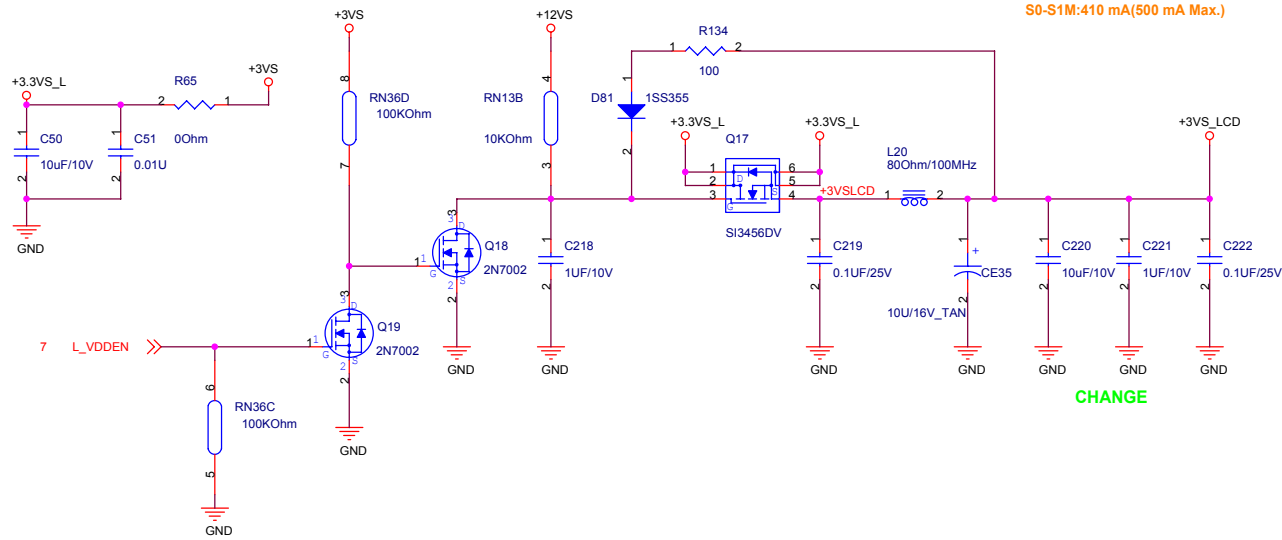


PEG_PRESENCE# : HIGH = GMCH GRAPHIC
LOW = PEG GRAPHIC

LCD Power

SI3865: US\$0.22

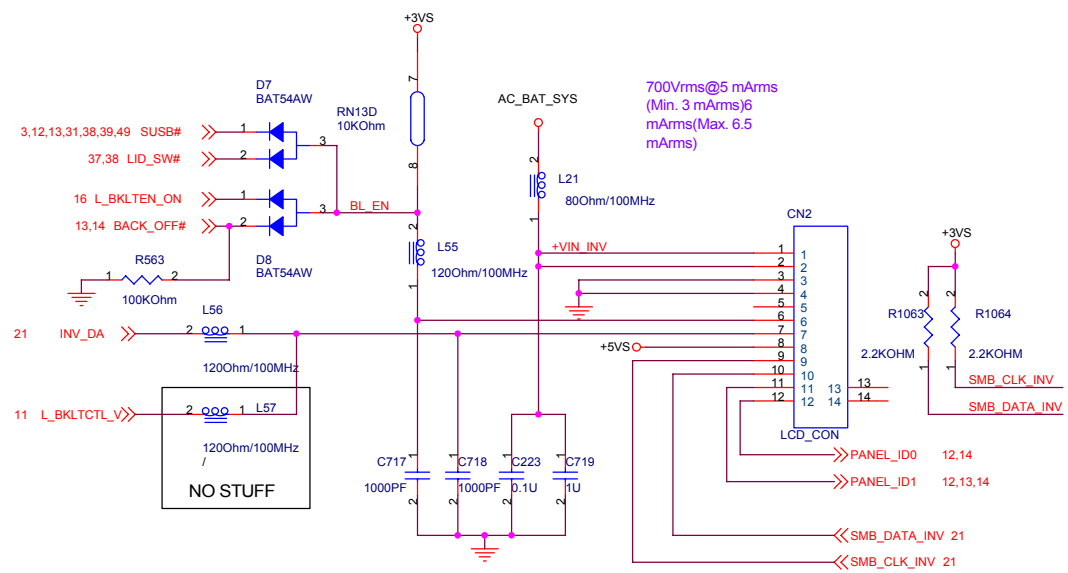
3-3.6V
S0-S1M:410 mA(500 mA Max.)



PANEL ID1 = 1 : WSXGA+ 1680x1050
 PANEL ID1 = 0 : WXGA 1280x800
 PANEL ID0 RESERVE FOR VENDOR

CHANGE

LCD Backlight Control

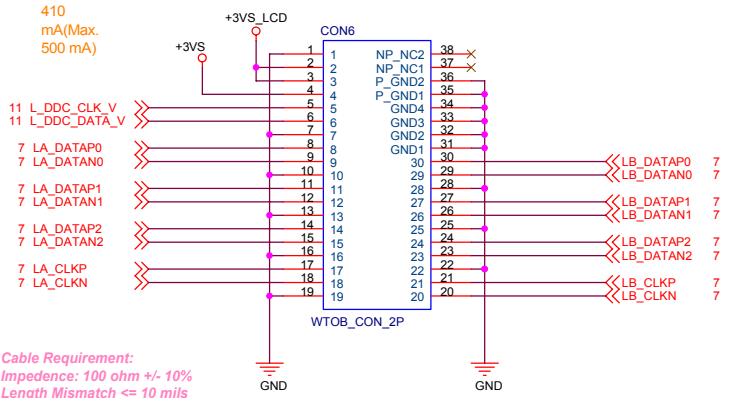


700Vrms@5 mArms
 (Min. 3 mArms)6
 mArms(Max. 6.5
 mArms)

NO STUFF

LCD LVDS Interface

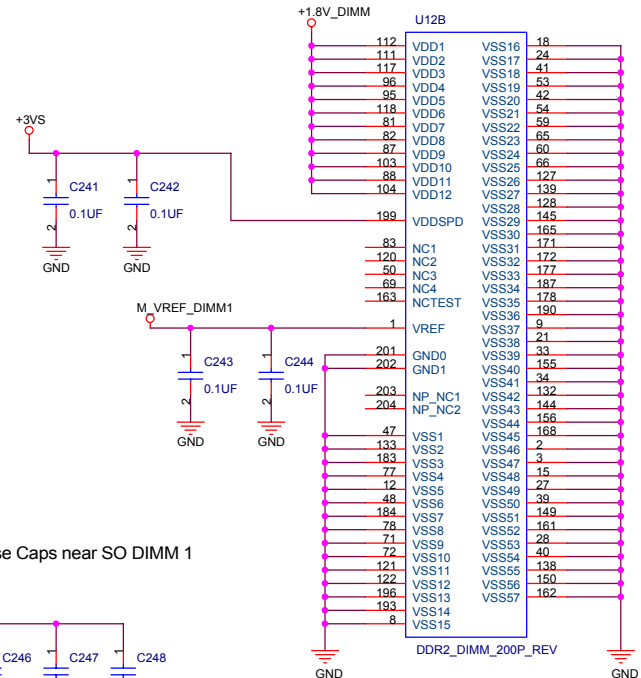
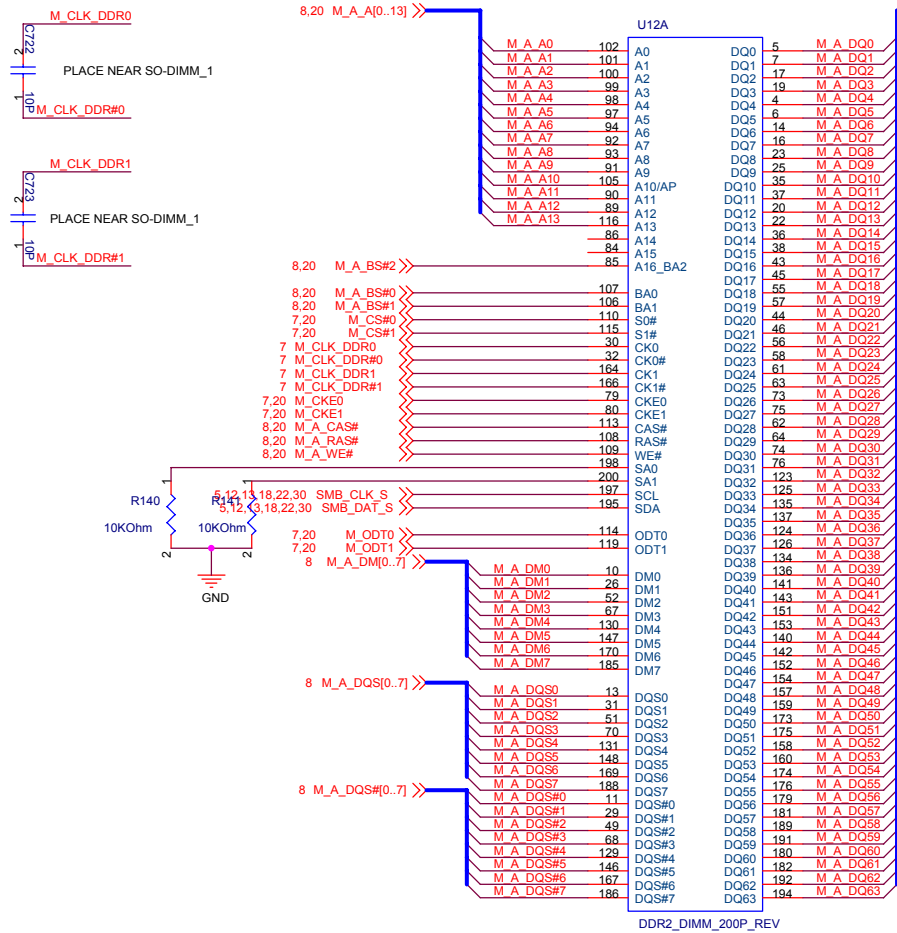
3V-3.6V
 Full
 Active:
 410
 mA(Max.
 500 mA)



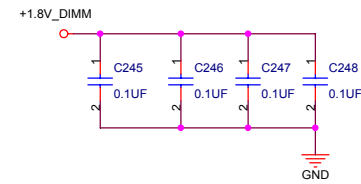
Cable Requirement:
 Impedence: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

ASL (SMB addr : 0x72)
 (Ambient Light Sensor)

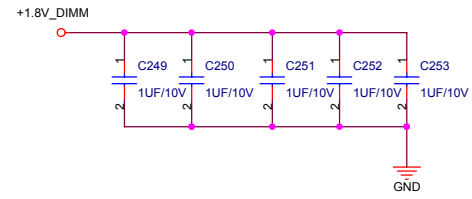
ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size	Project Name	Rev	
Custom	M7V	0.95	
Date: Monday, November 10, 2003	Sheet	17	of 51



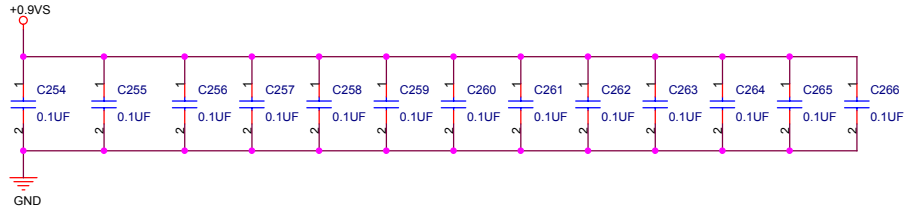
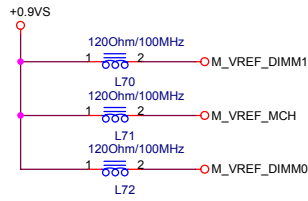
Layout Note: Place these Caps near SO DIMM 1



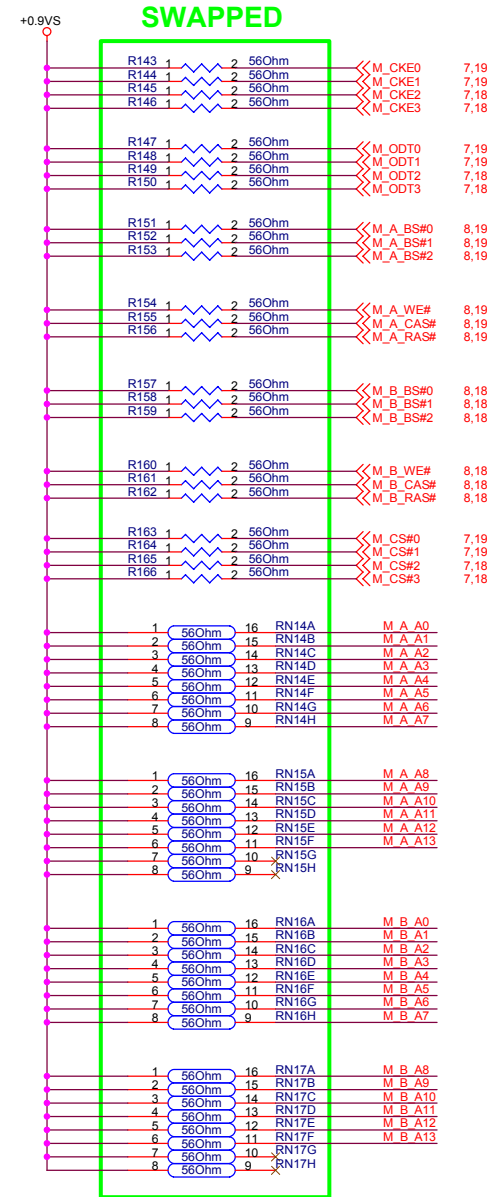
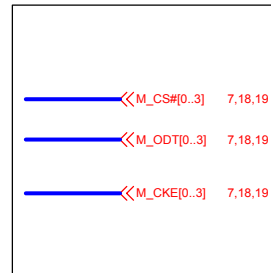
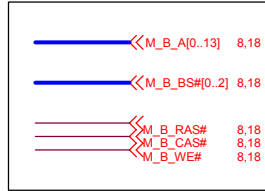
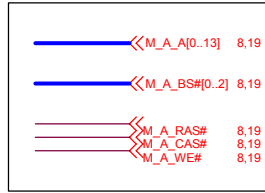
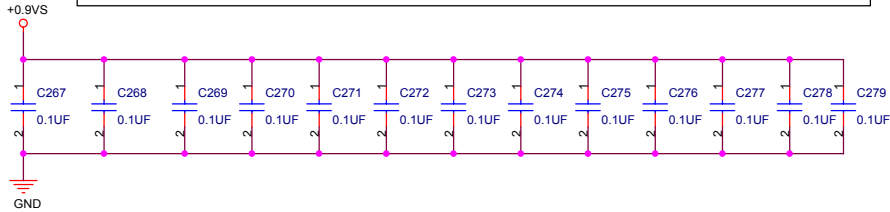
Layout Note: Place these Caps near SO DIMM 1

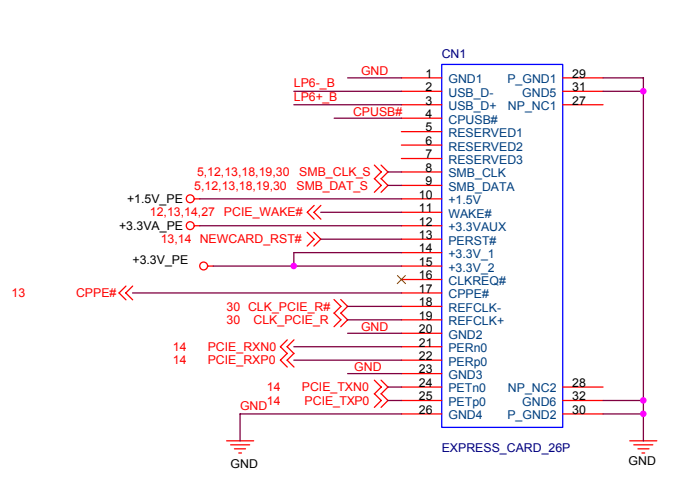


SO-DIMM 1 is placed father from the GMCH than SO-DIMM 0

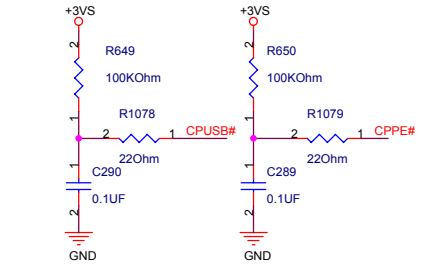
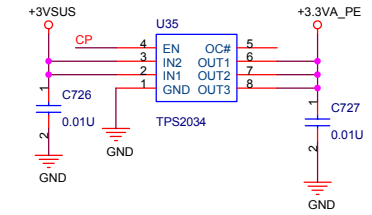
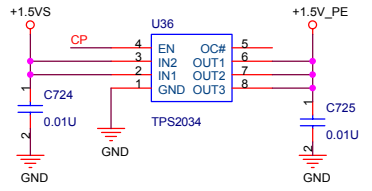
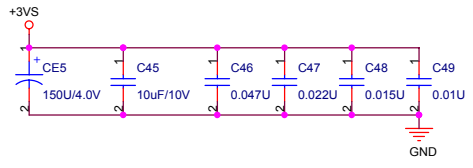
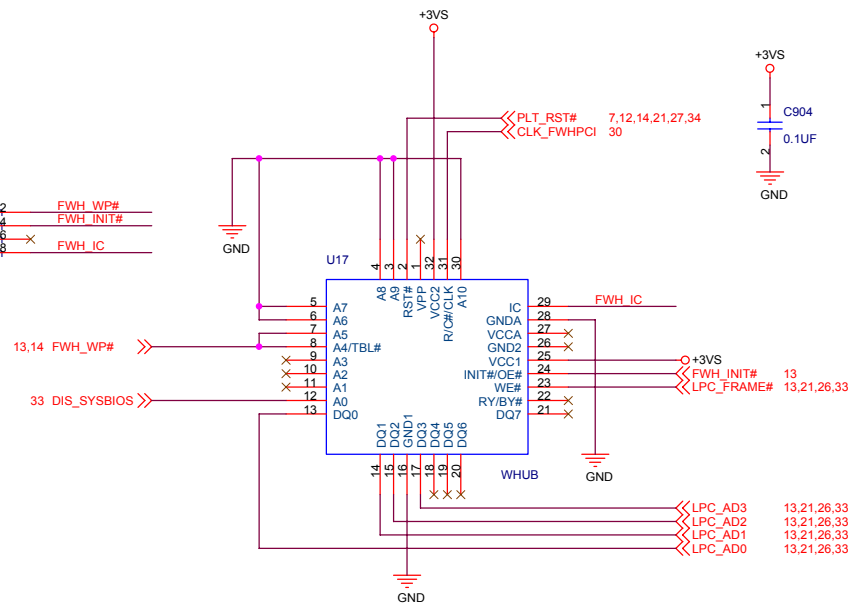
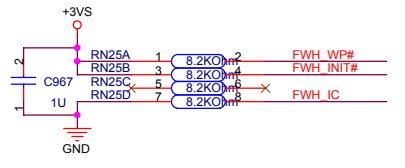


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

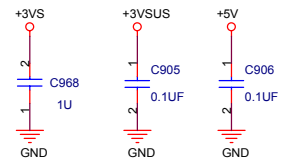
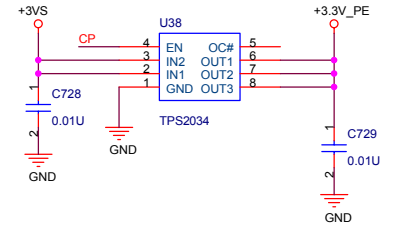
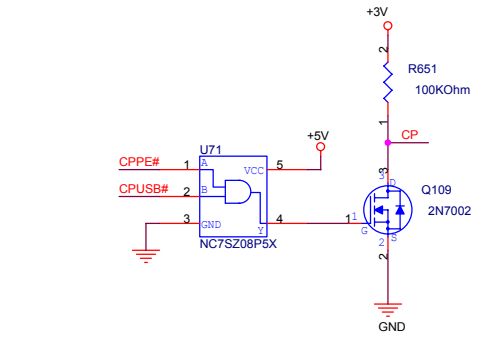
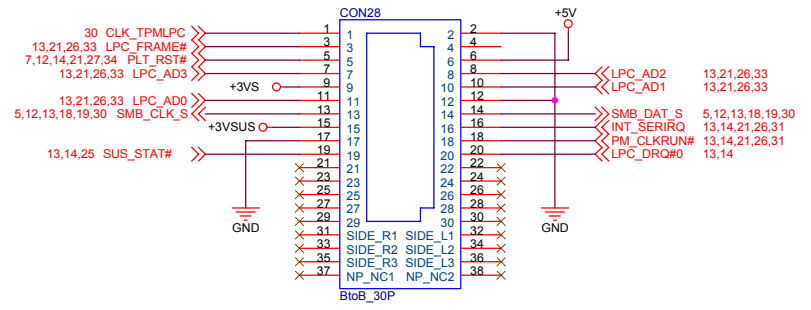




FOLLOW SST FWH SPEC

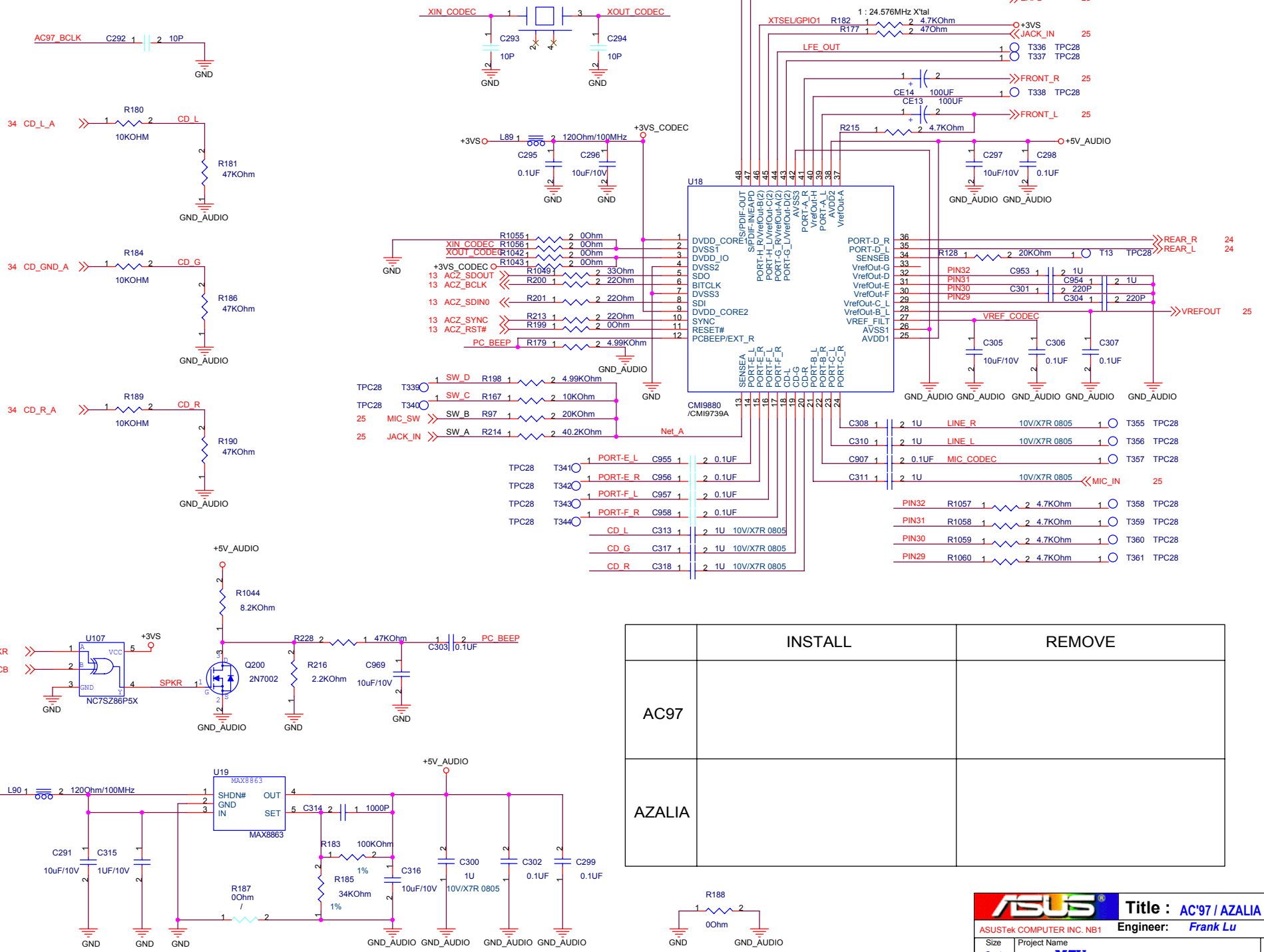


TPM B2B Connector



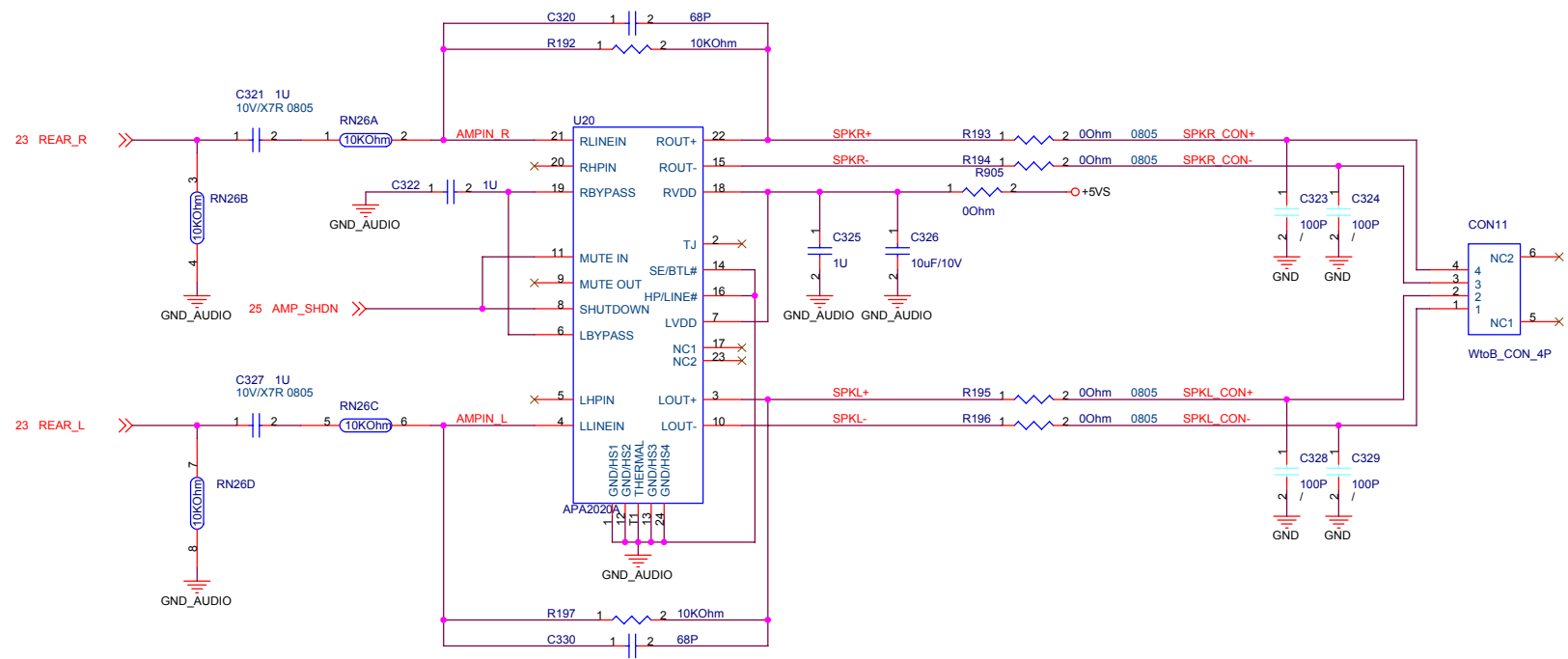
AC97 STUFF

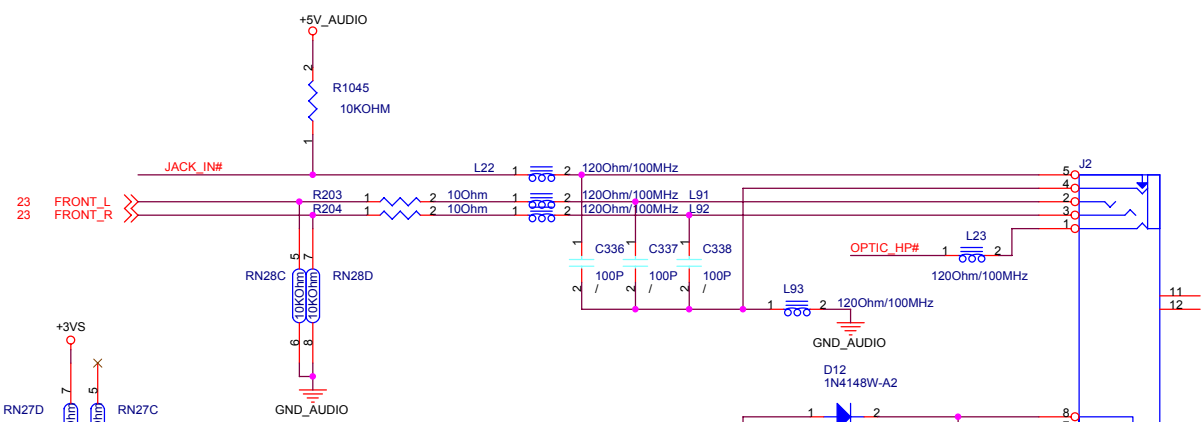
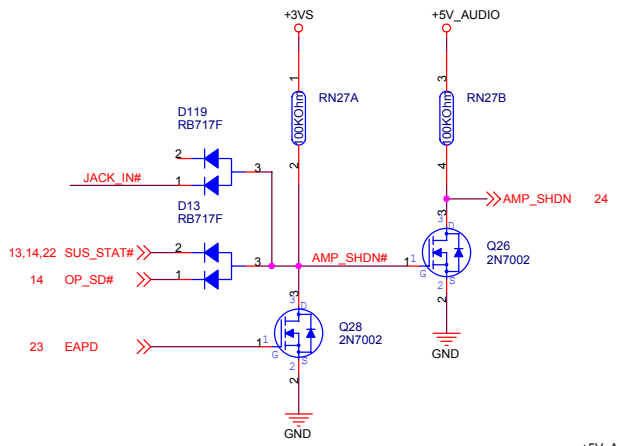
X3 24.576MHZ



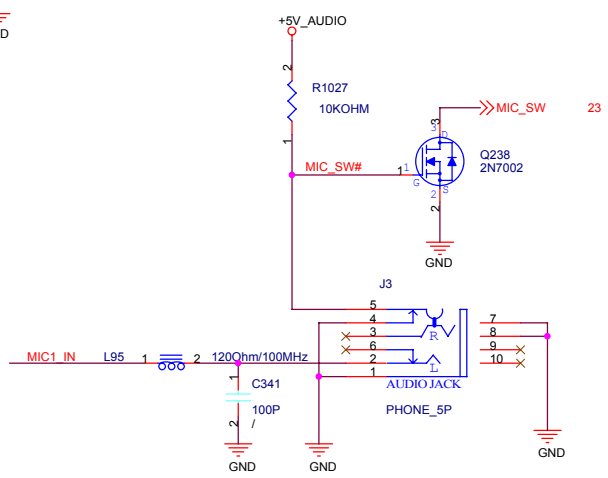
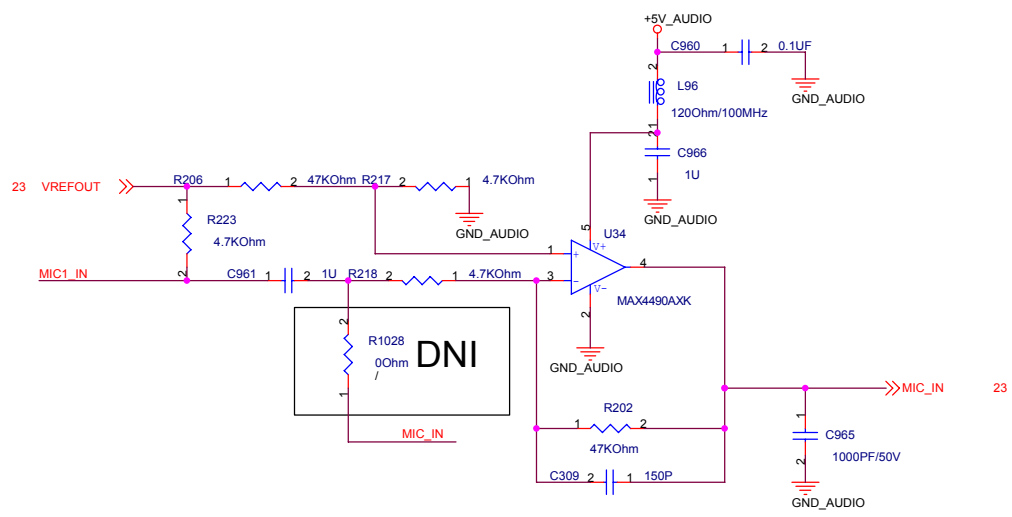
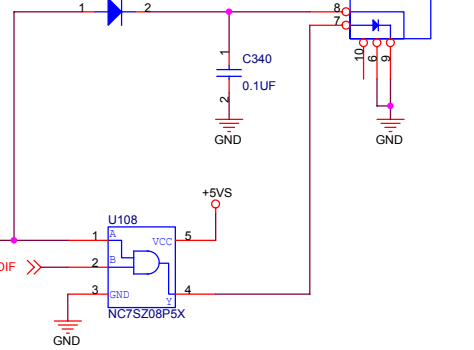
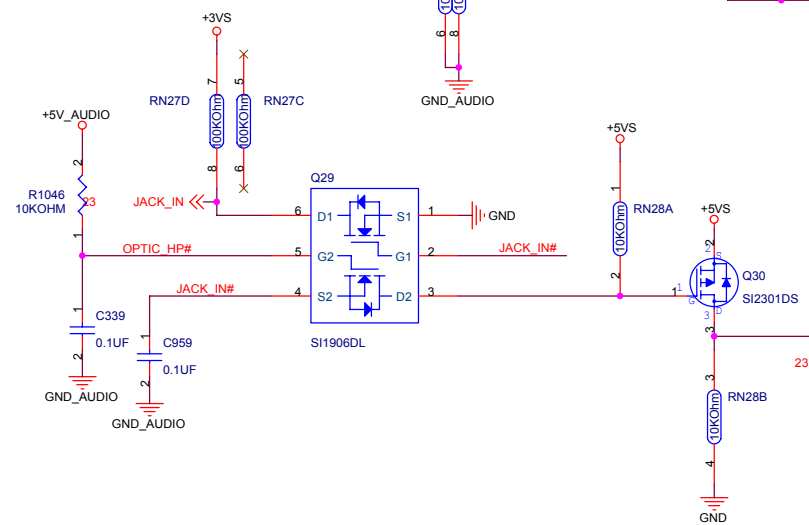
	INSTALL	REMOVE
AC97		
AZALIA		

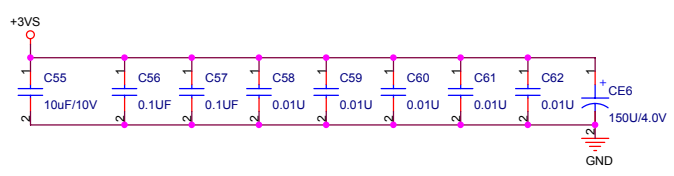
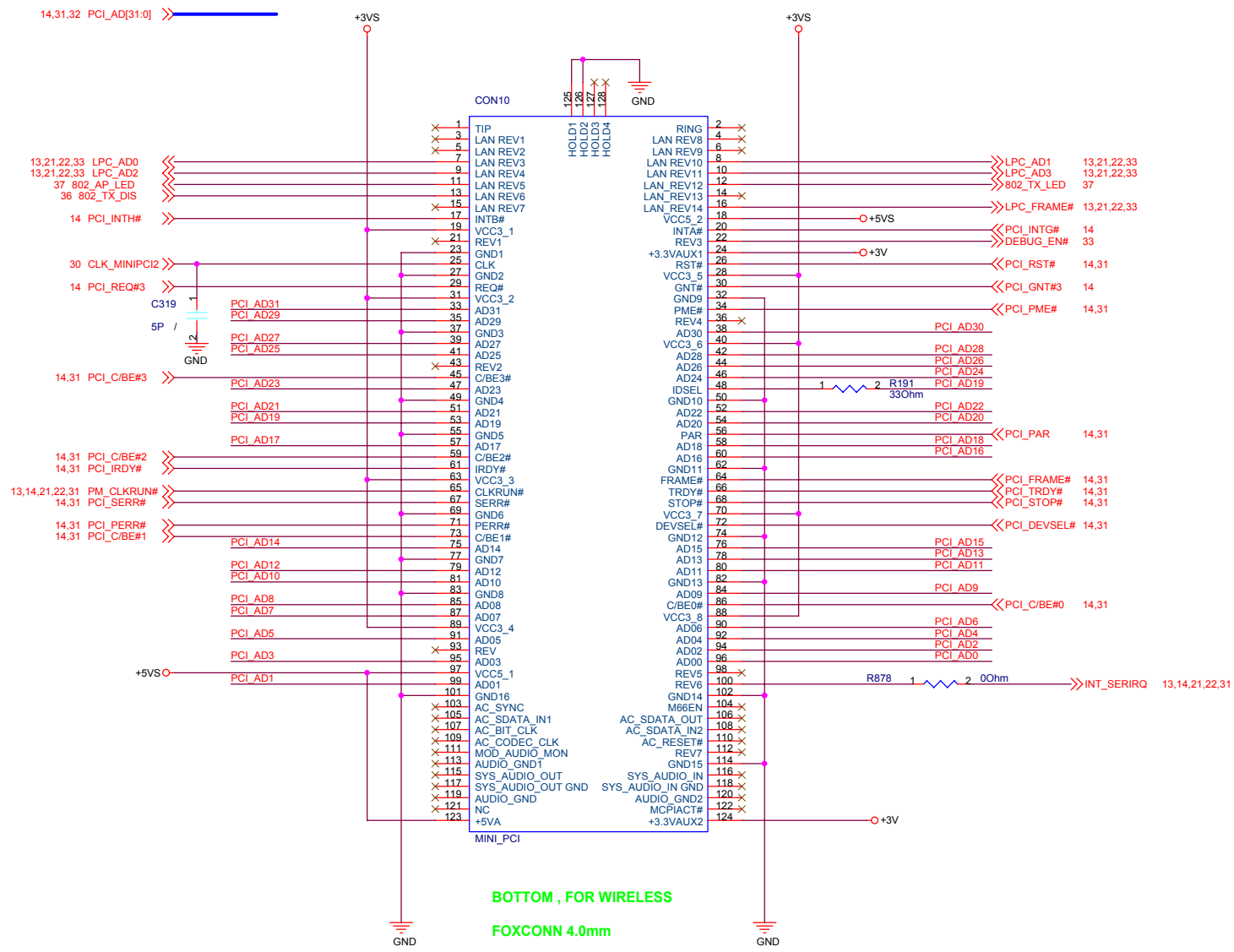
ASUS Title : AC'97 / AZALIA
 ASUSTek COMPUTER INC. NB1 Engineer: Frank Lu
 Size Project Name
 Custom M7V
 Date: Monday, November 10, 2003 Sheet 23 of 51



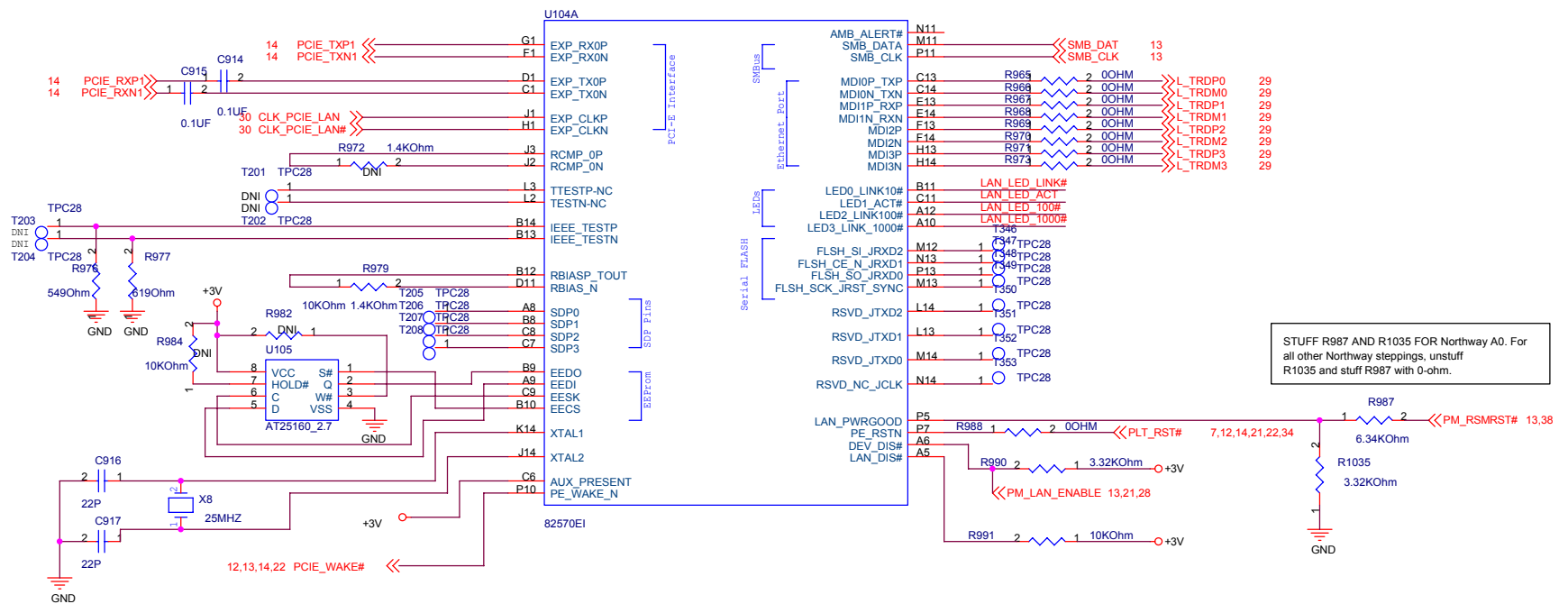


JACK_IN# OPTIC_HP#
 L H SPDIF
 L L LINE OUT
 H H NO CONNECT

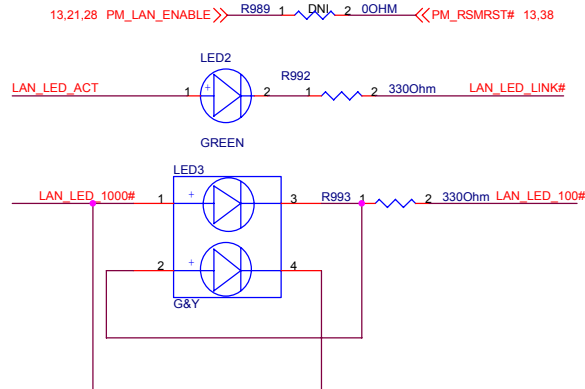
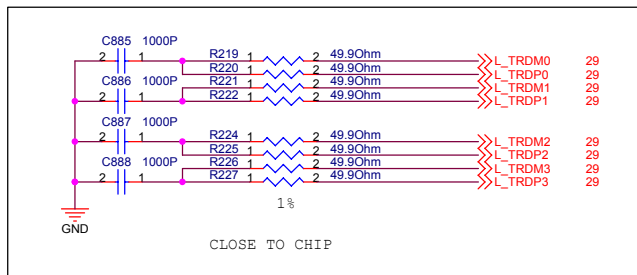


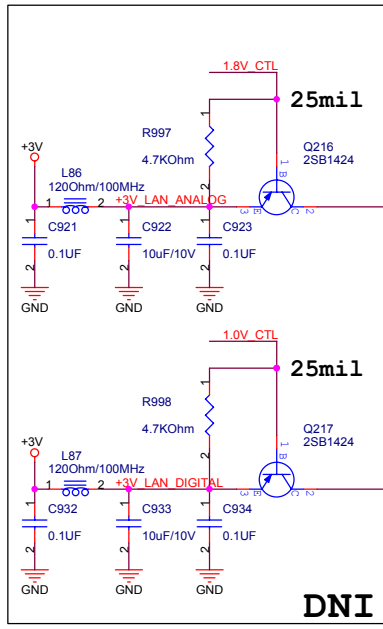


ASUS		Title : MINI_PCI (802.11)	
ASUSTek COMPUTER INC		Engineer: <i>Frank Lu</i>	
Size	Project Name	Rev	
Custom	M7V	0.95	
Date: Monday, November 10, 2003	Sheet 26 of 51		

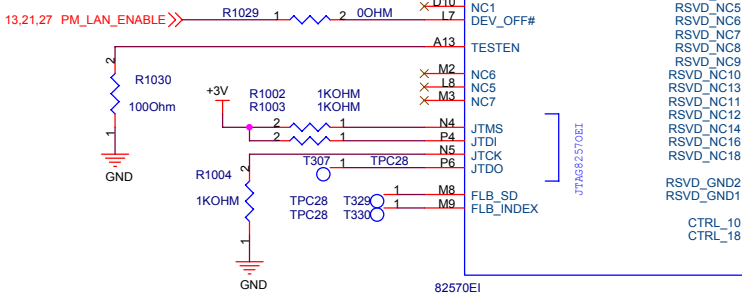
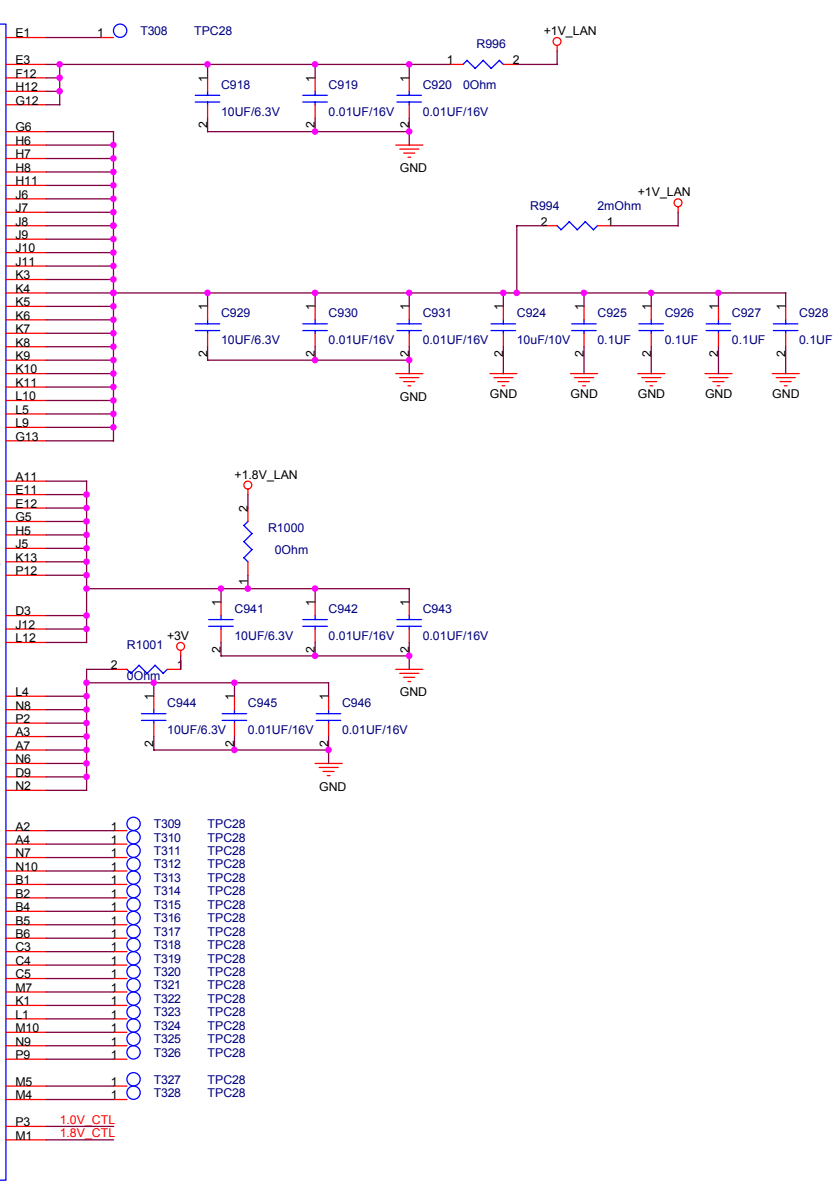
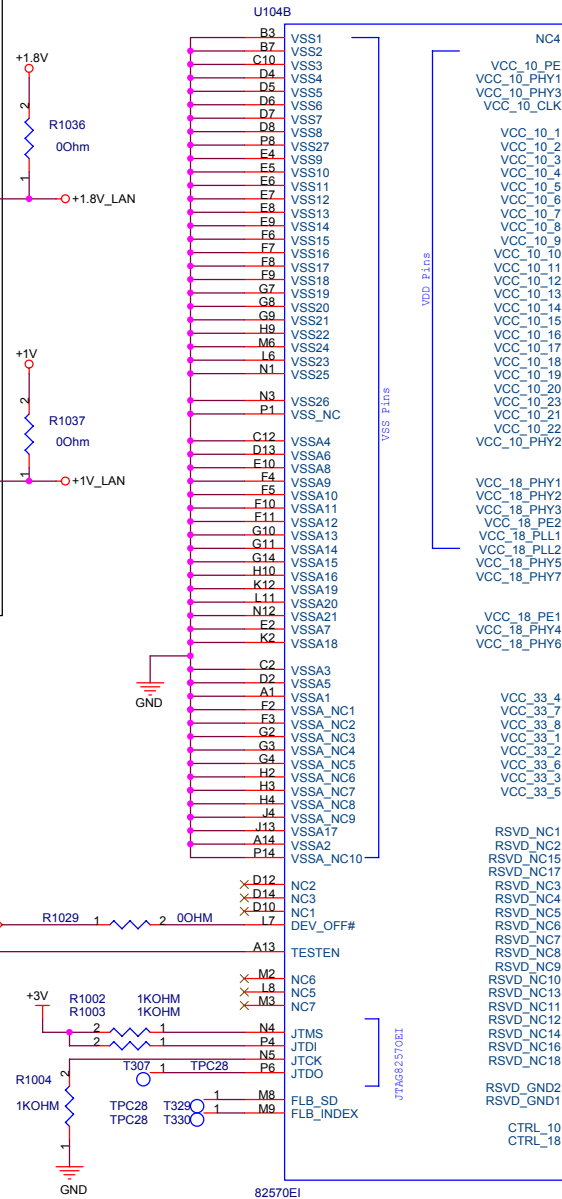


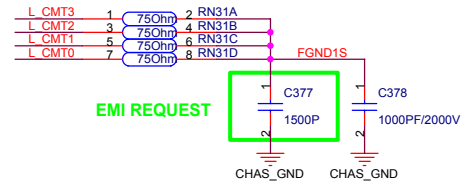
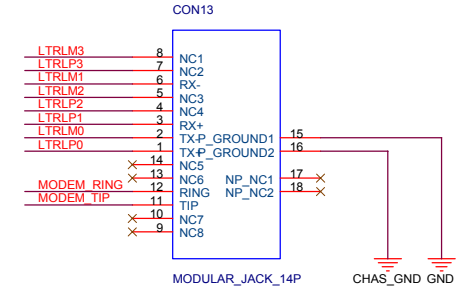
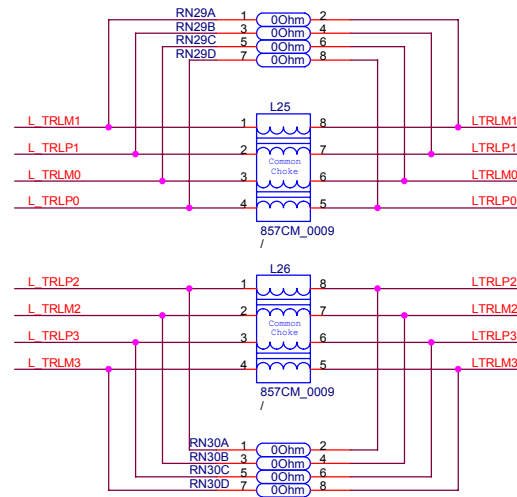
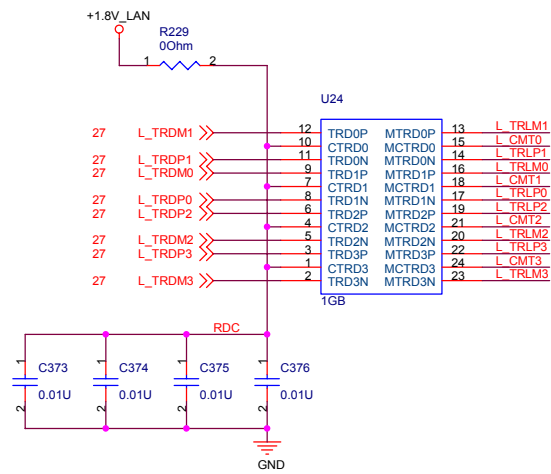
STUFF R987 AND R1035 FOR Northway A0. For all other Northway steppings, unstuff R1035 and stuff R987 with 0-ohm.



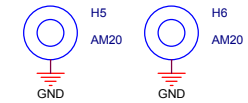
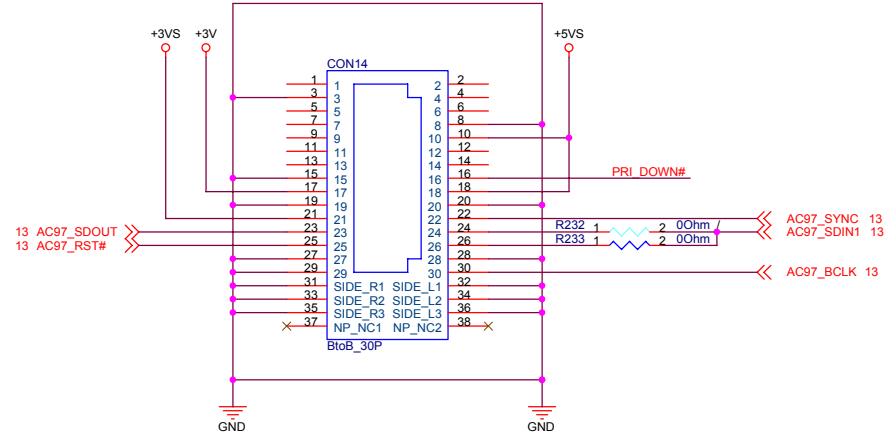
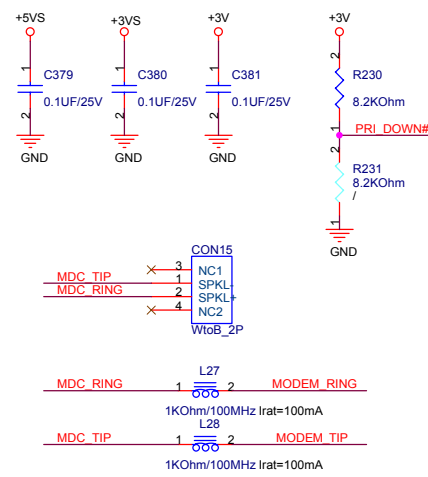


DNI

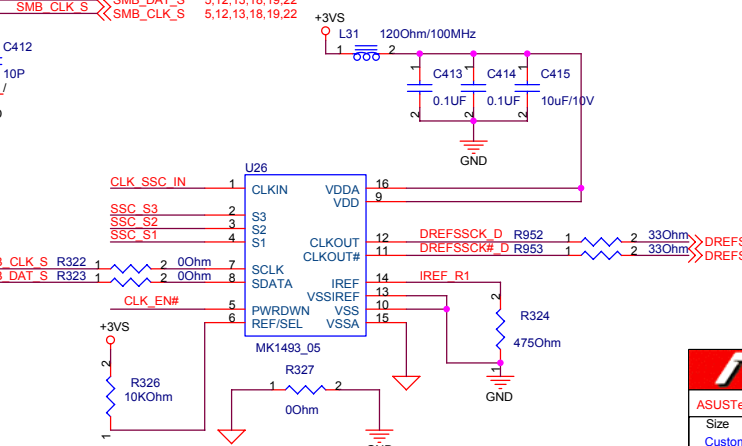
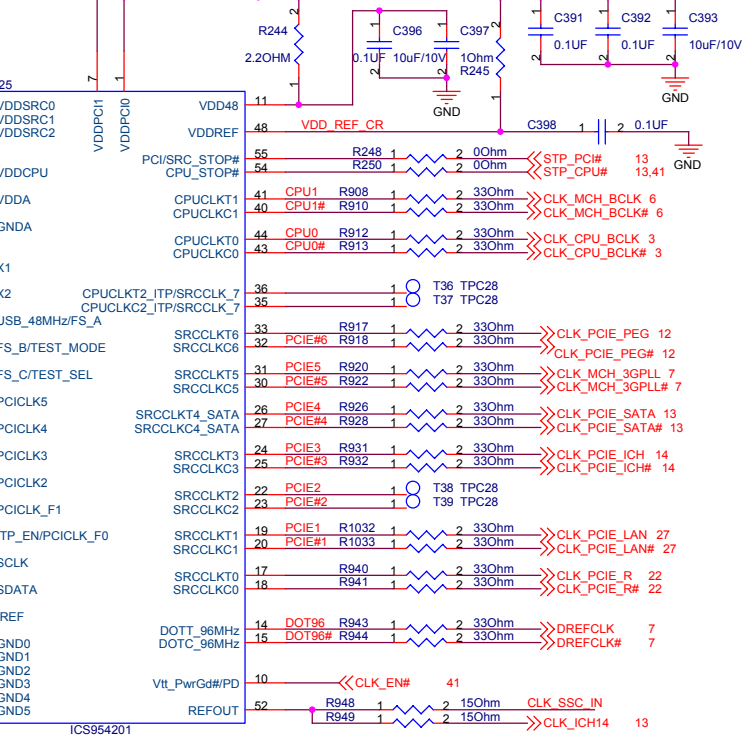
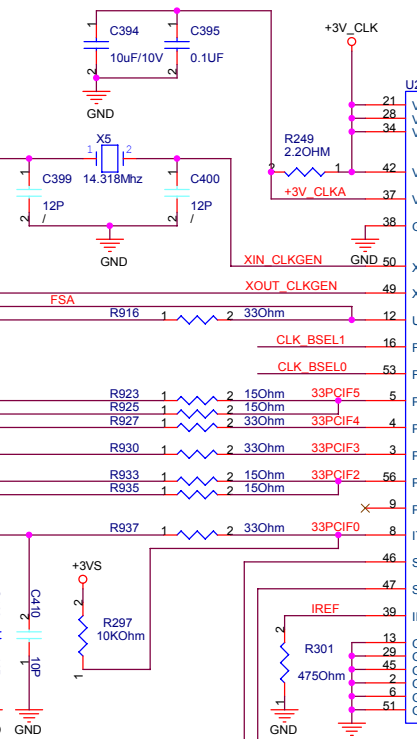
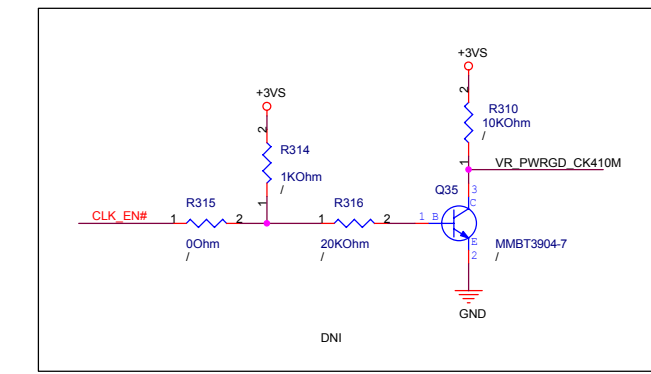
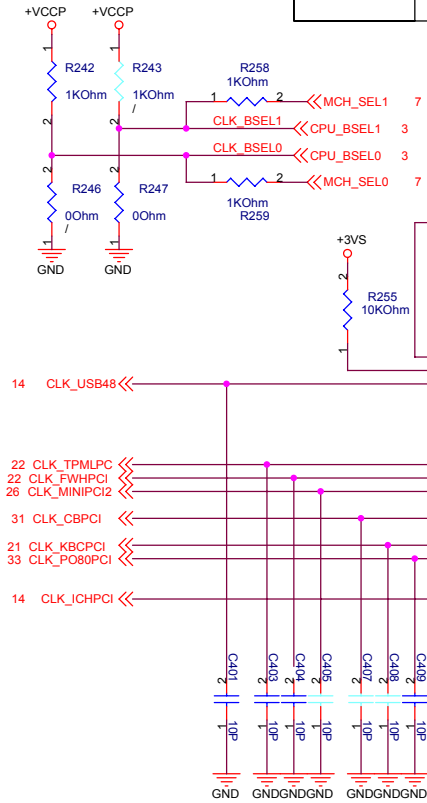




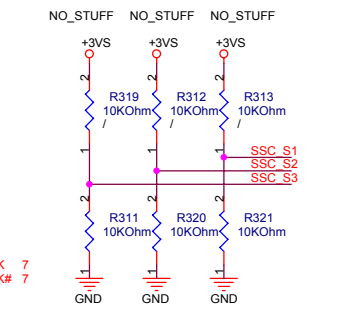
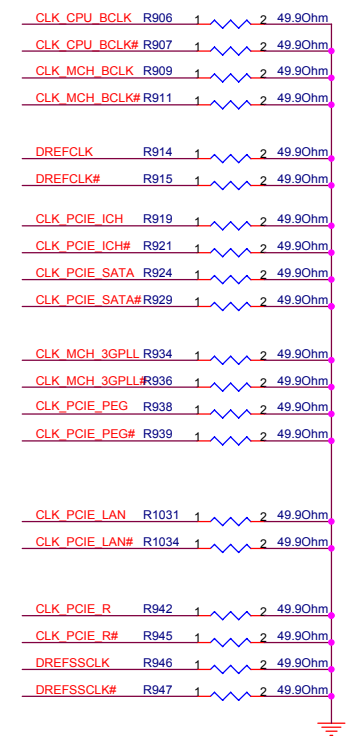
MDC

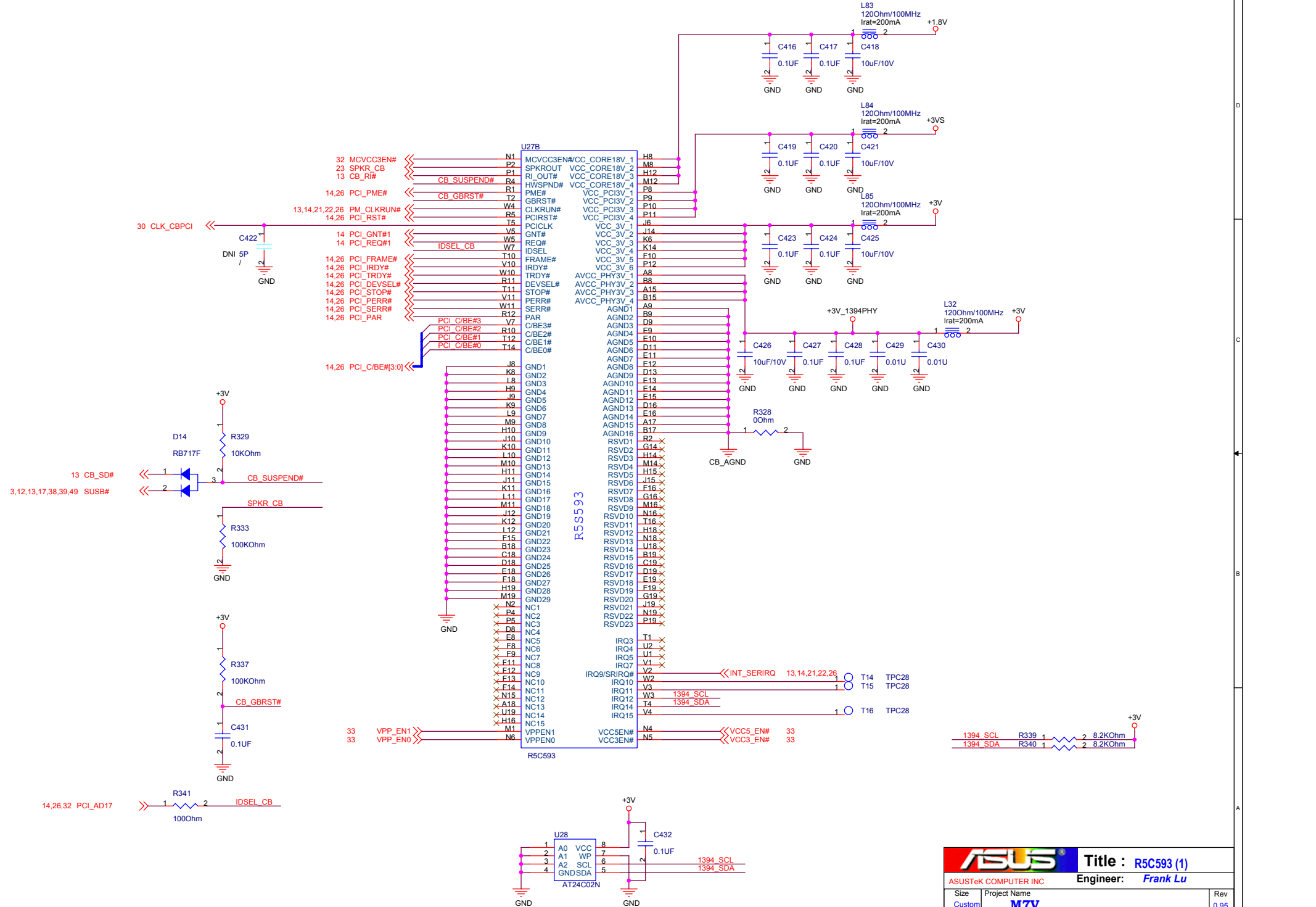


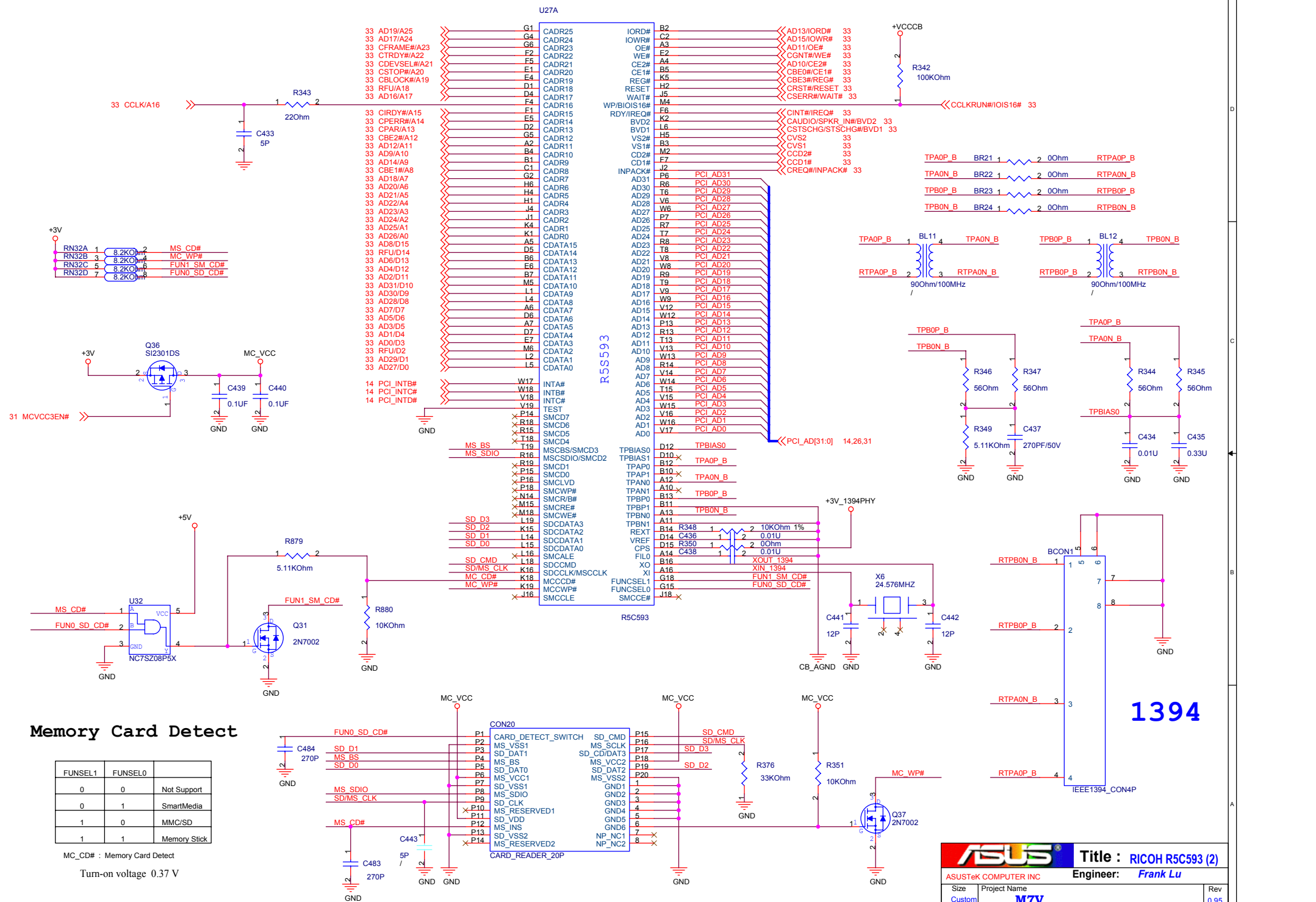
A STEP		B STEP	
BSEL0	BSEL1	BSEL0	HOST CLOCK
0	0	1	100
1	0	0	133



PLACE termination close to source IC





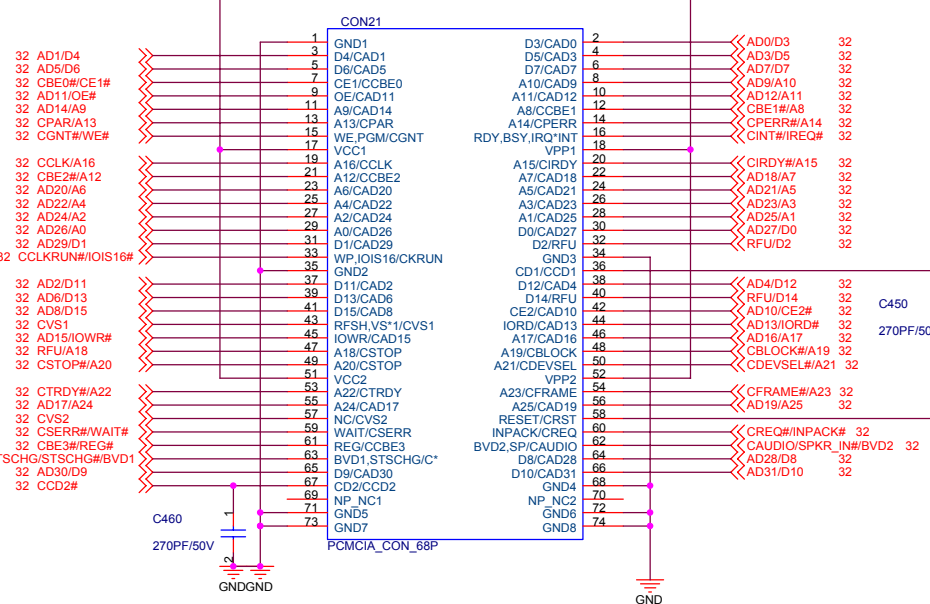
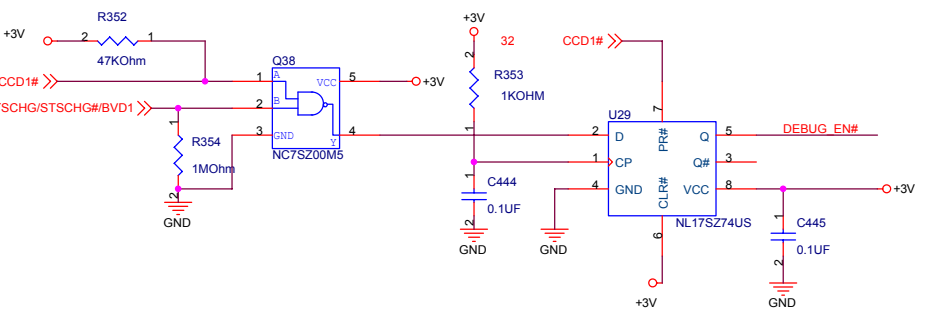
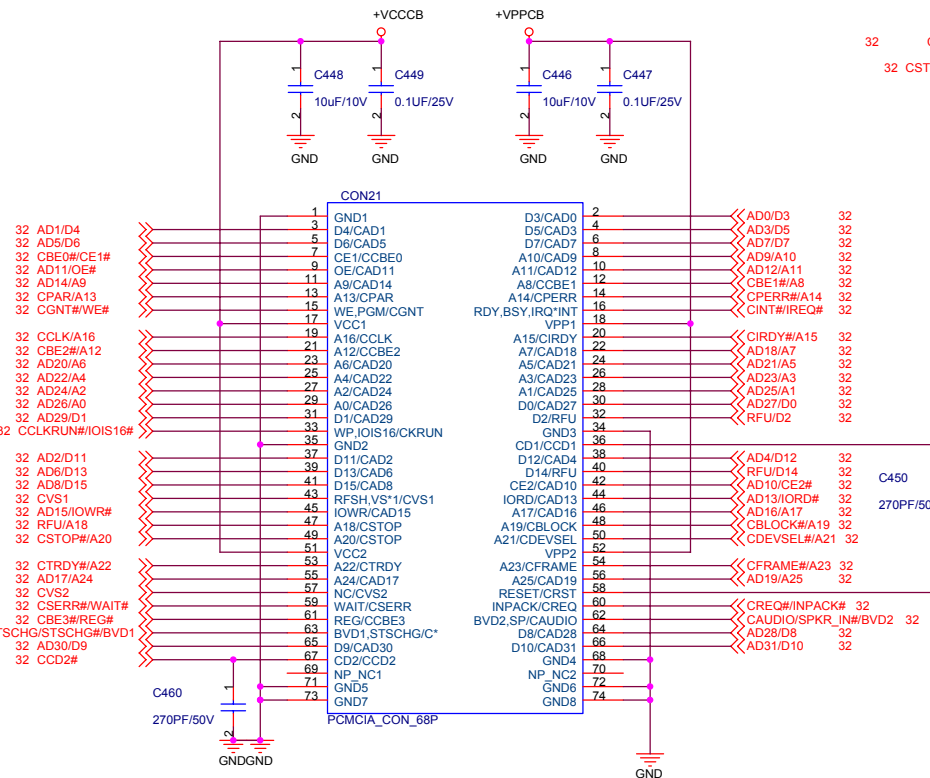
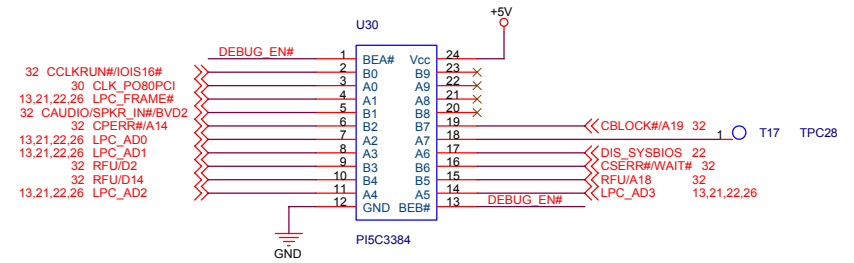
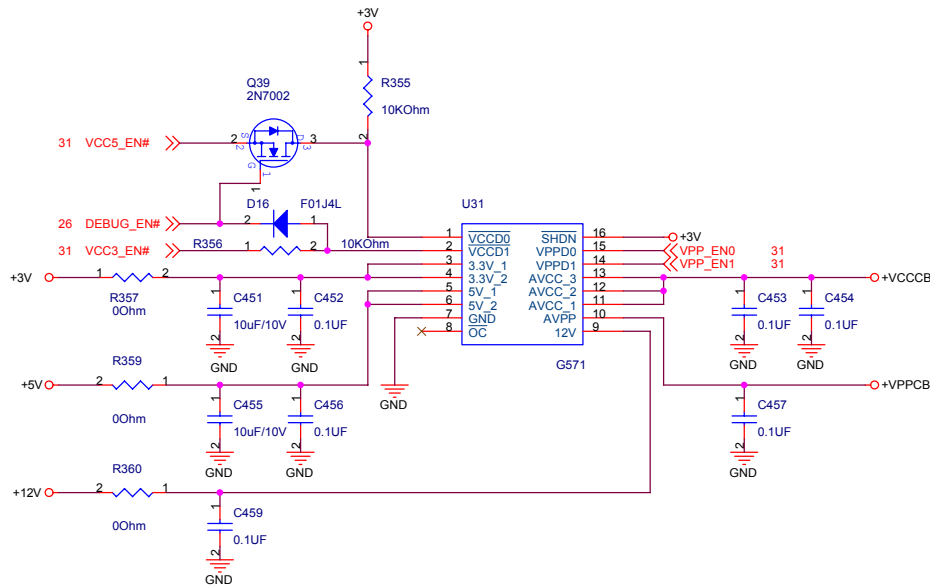


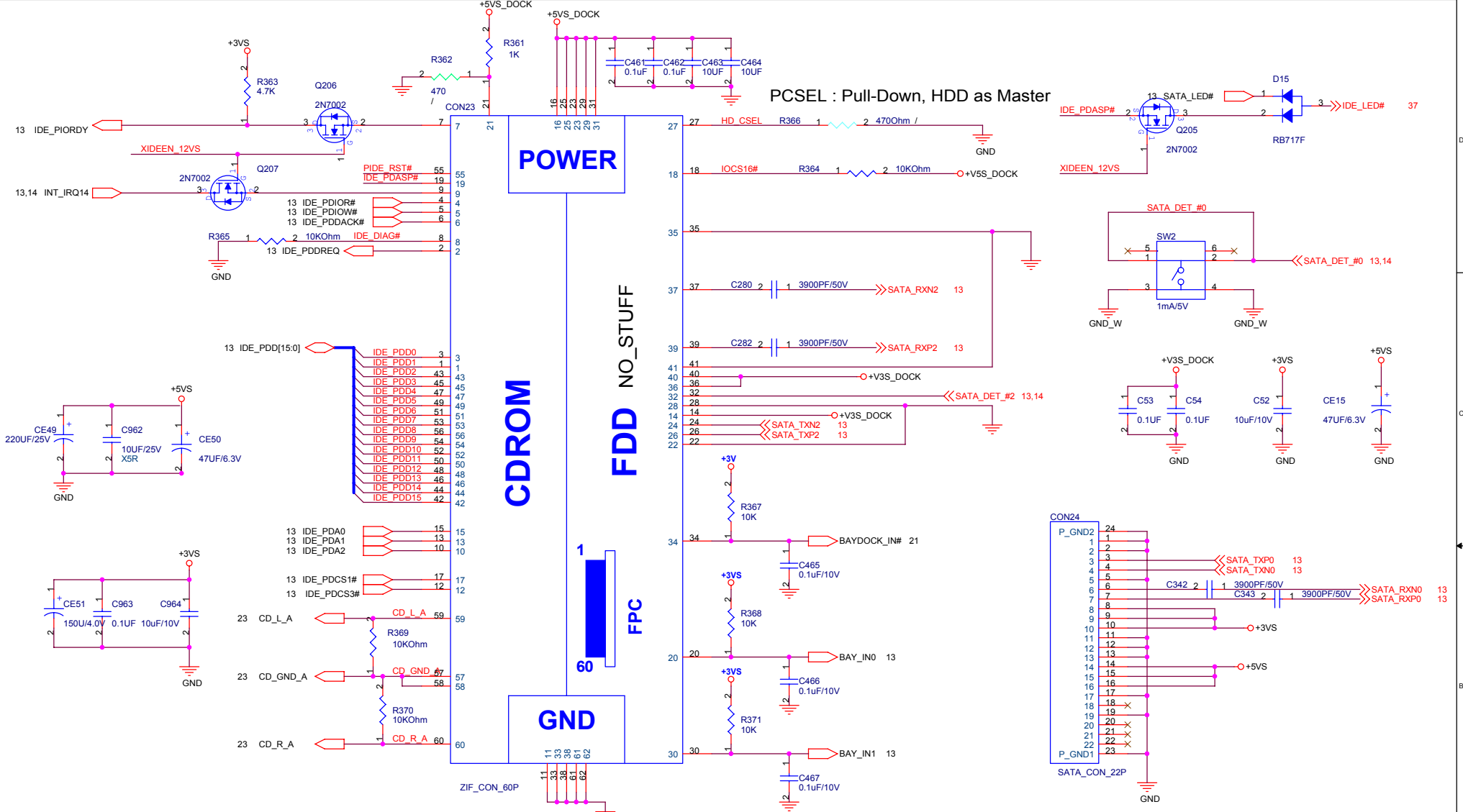
Memory Card Detect

FUNSEL1	FUNSEL0	
0	0	Not Support
0	1	SmartMedia
1	0	MMC/SD
1	1	Memory Stick

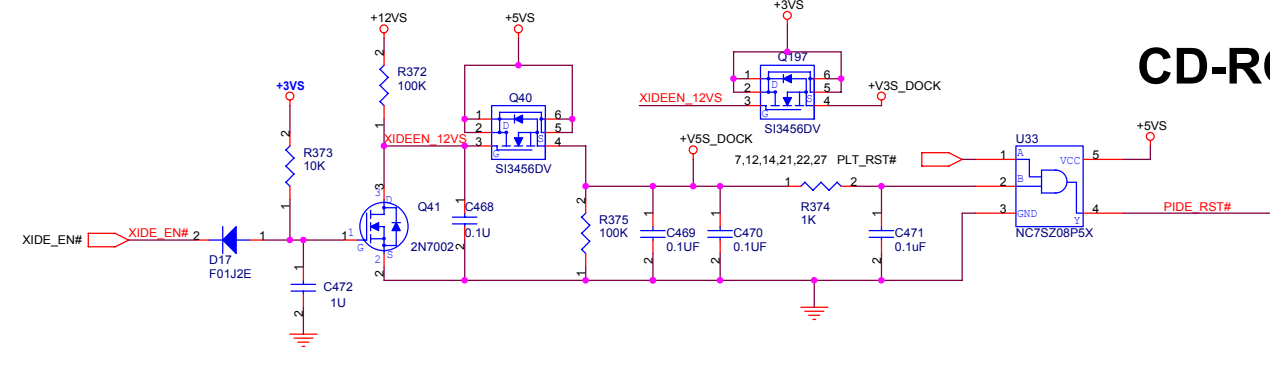
MC_CD# : Memory Card Detect
Turn-on voltage 0.37 V

ASUS Title : RICOH R5C593 (2)
 ASUSTek COMPUTER INC Engineer: Frank Lu
 Size Project Name
 Custom M7V
 Date: Monday, November 10, 2003 Sheet 32 of 51





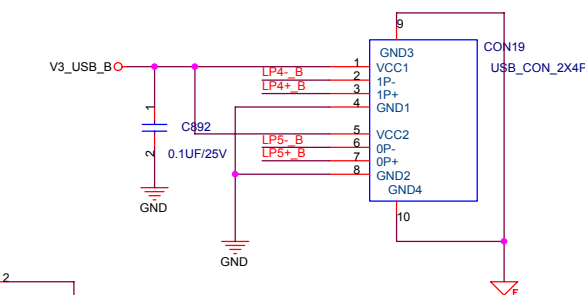
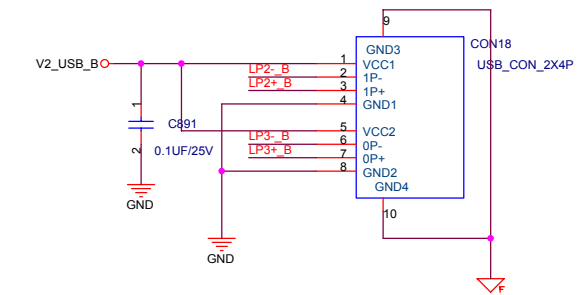
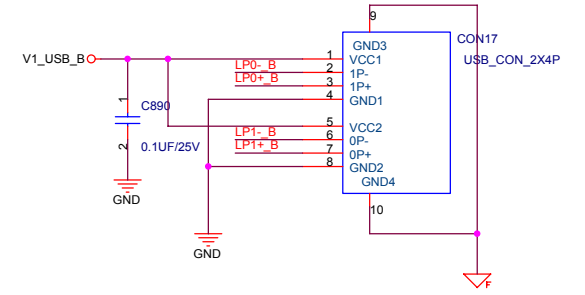
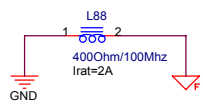
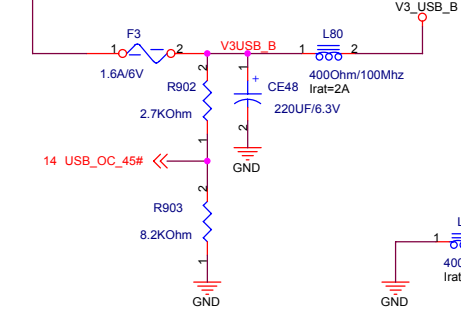
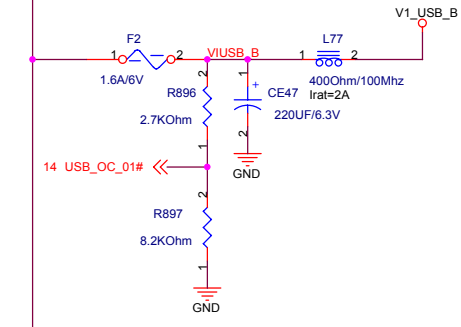
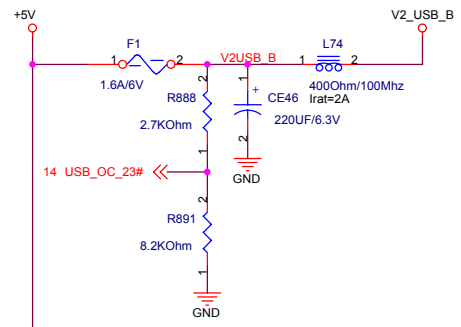
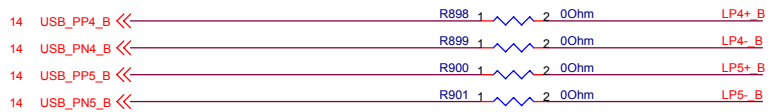
CD-ROM RESET



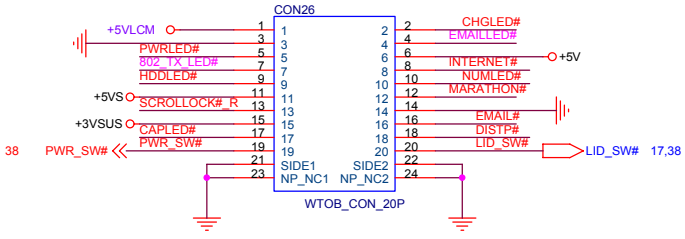
4.75-5.25V
 S0-S1M:1.3A(Typ)1.5A(Max.) Eject
 S0-S1M:0.7A(Typ)0.8A(Max.)
 Read

ASUS		Title : CDROM	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size	Project Name	Rev	
Custom	M7V	0.95	
Date: Monday, November 10, 2003		Sheet	34 of 51

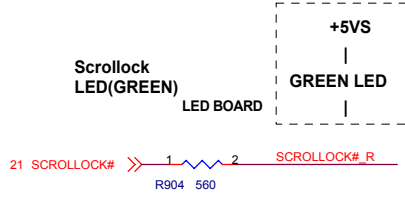
USB



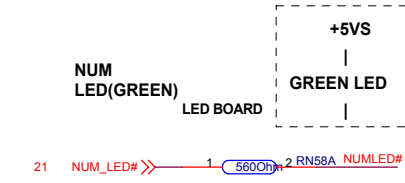
Indicator Connector



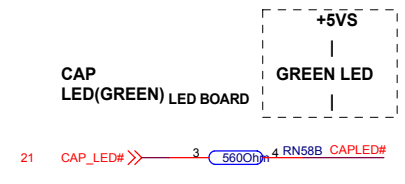
Scrolllock LED(GREEN)



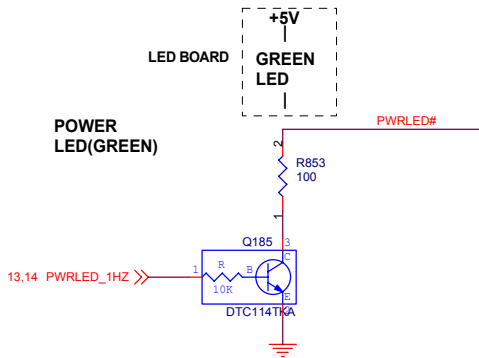
NUM LED(GREEN)



CAP LED(GREEN)

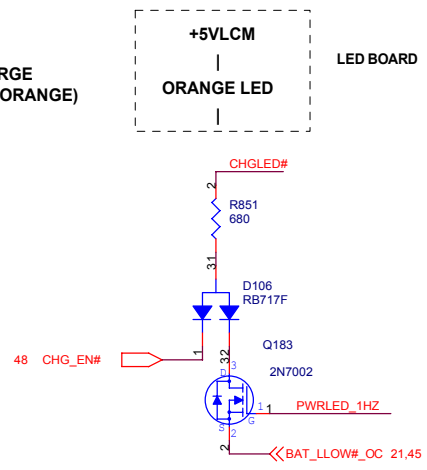


POWER LED(GREEN)

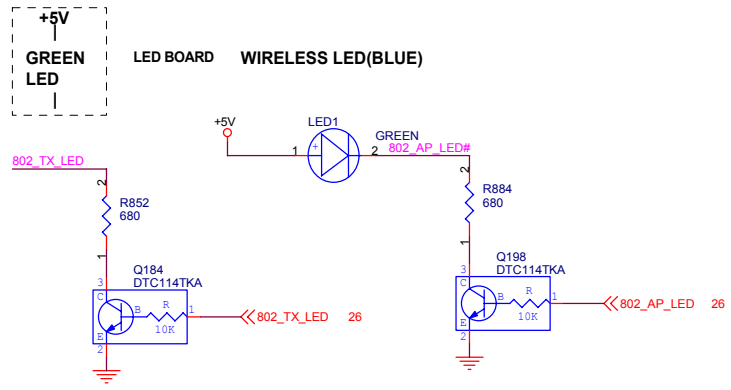


LED

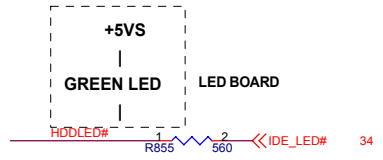
CHARGE LED(ORANGE)



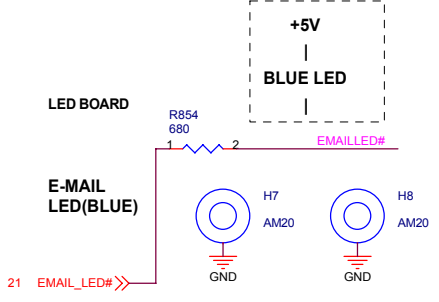
GREEN LED LED BOARD WIRELESS LED(BLUE)



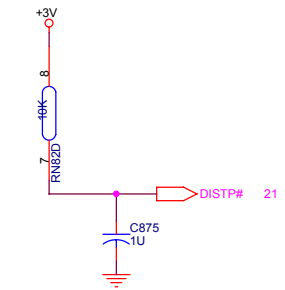
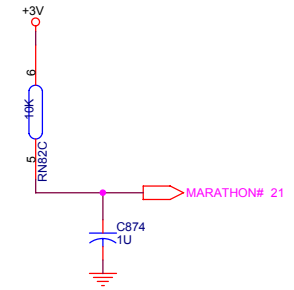
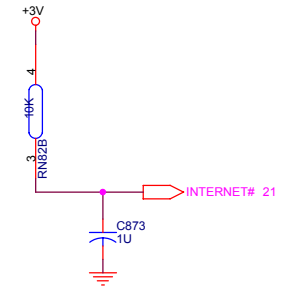
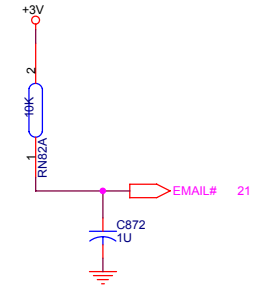
GREEN LED LED BOARD



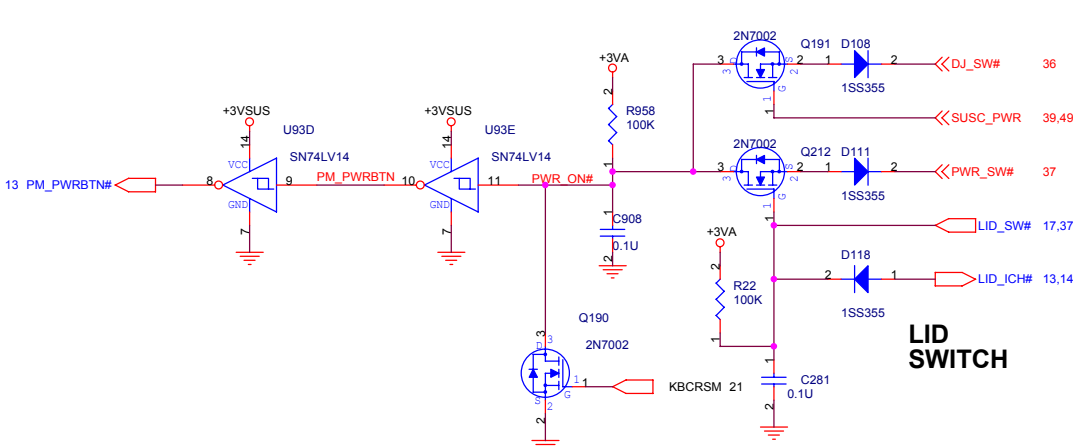
BLUE LED LED BOARD



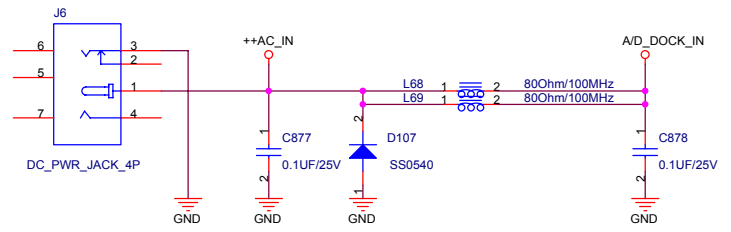
INSTANT KEY



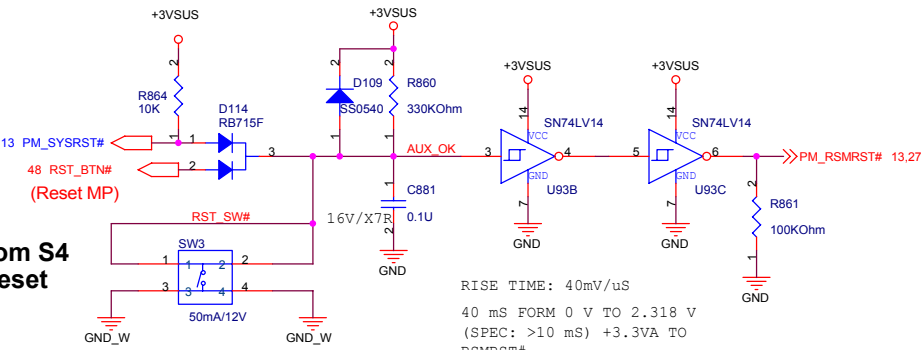
ASUS		Title : LED BOARD	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size	Project Name	Rev	
Custom	M7V	0.95	
Date:	Monday, November 10, 2003	Sheet	37 of 51



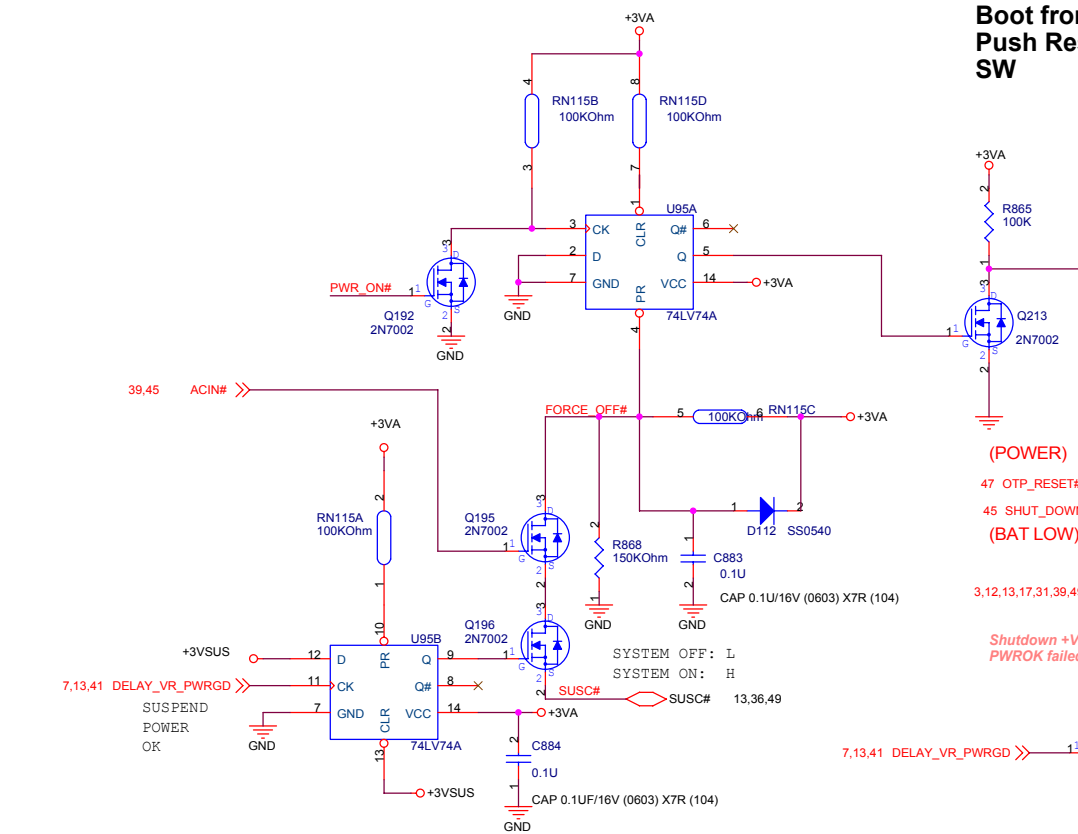
LID SWITCH



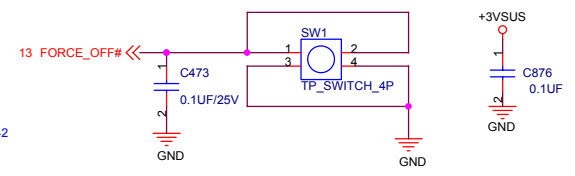
Boot from S4 Push Reset SW



RESET BUTTON

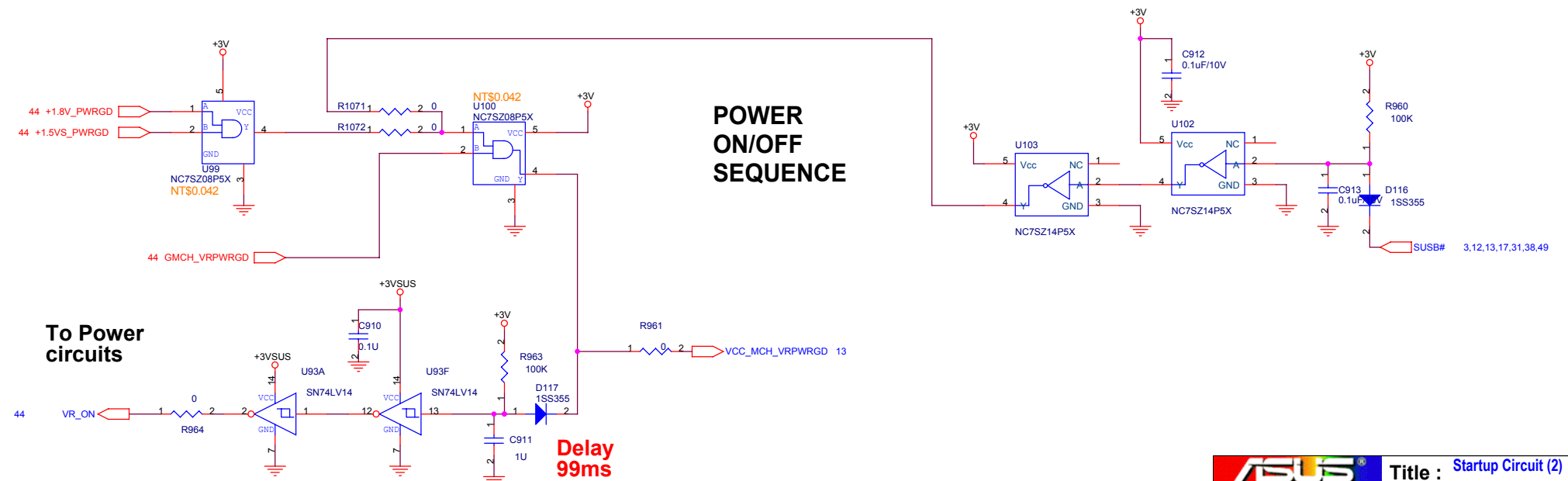
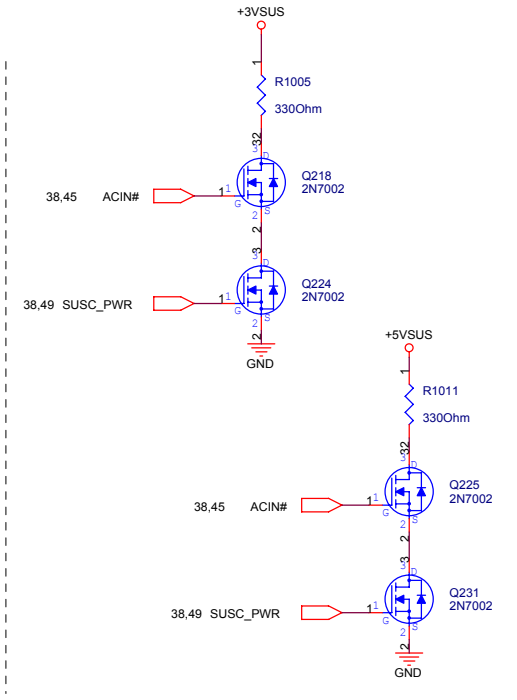
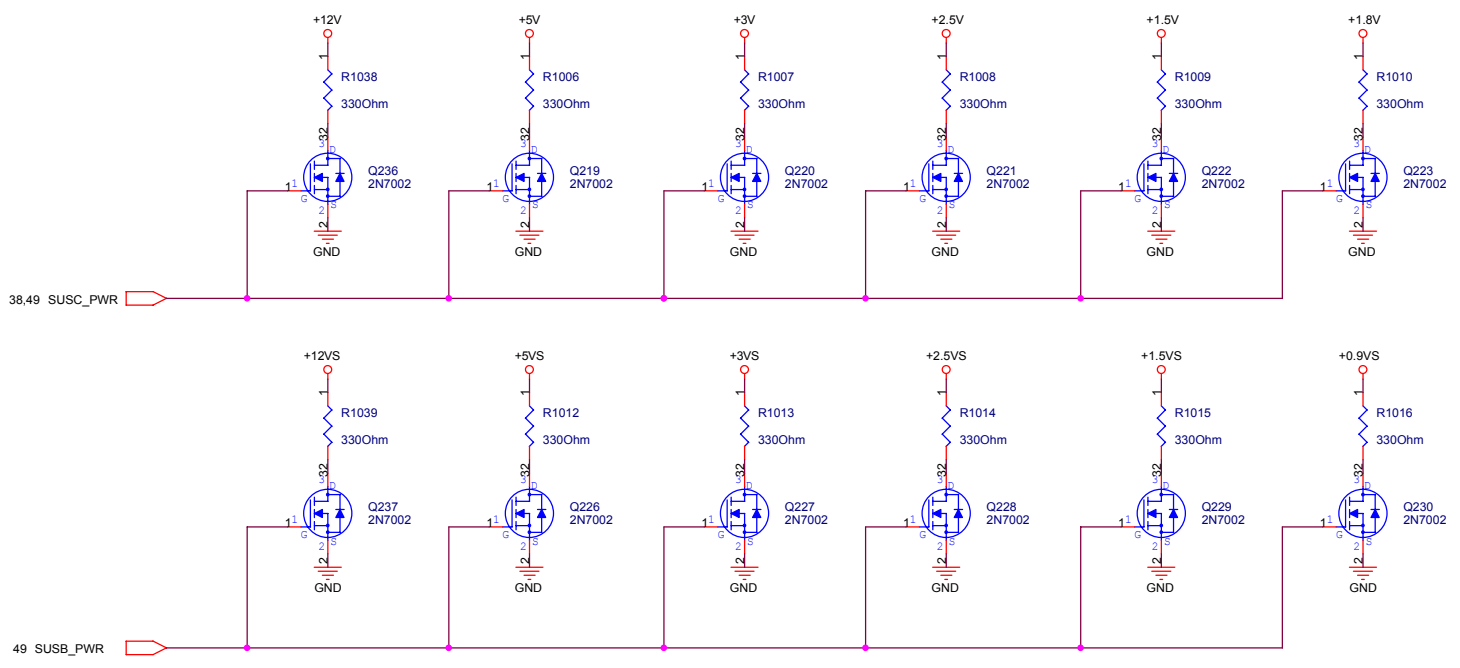


+3.3VSUS ON



System Power Sequence
 +VCCRTC->RTCST#->V5REFSUS->3.3/1.5VSUS->
 RSMRST#->SUSC#->SUBS#->VCCLAN->LANPWROK
 ->V5REF->PWROK->GMCH->VCCP->VCORE
 SUSSTAT#->PCIRST#
 CPU : +VCORE, +VCCP, +1.05VS
 NB : +1.05VS, +1.5VS, +2.5V, +VCCP
 SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS
 M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS

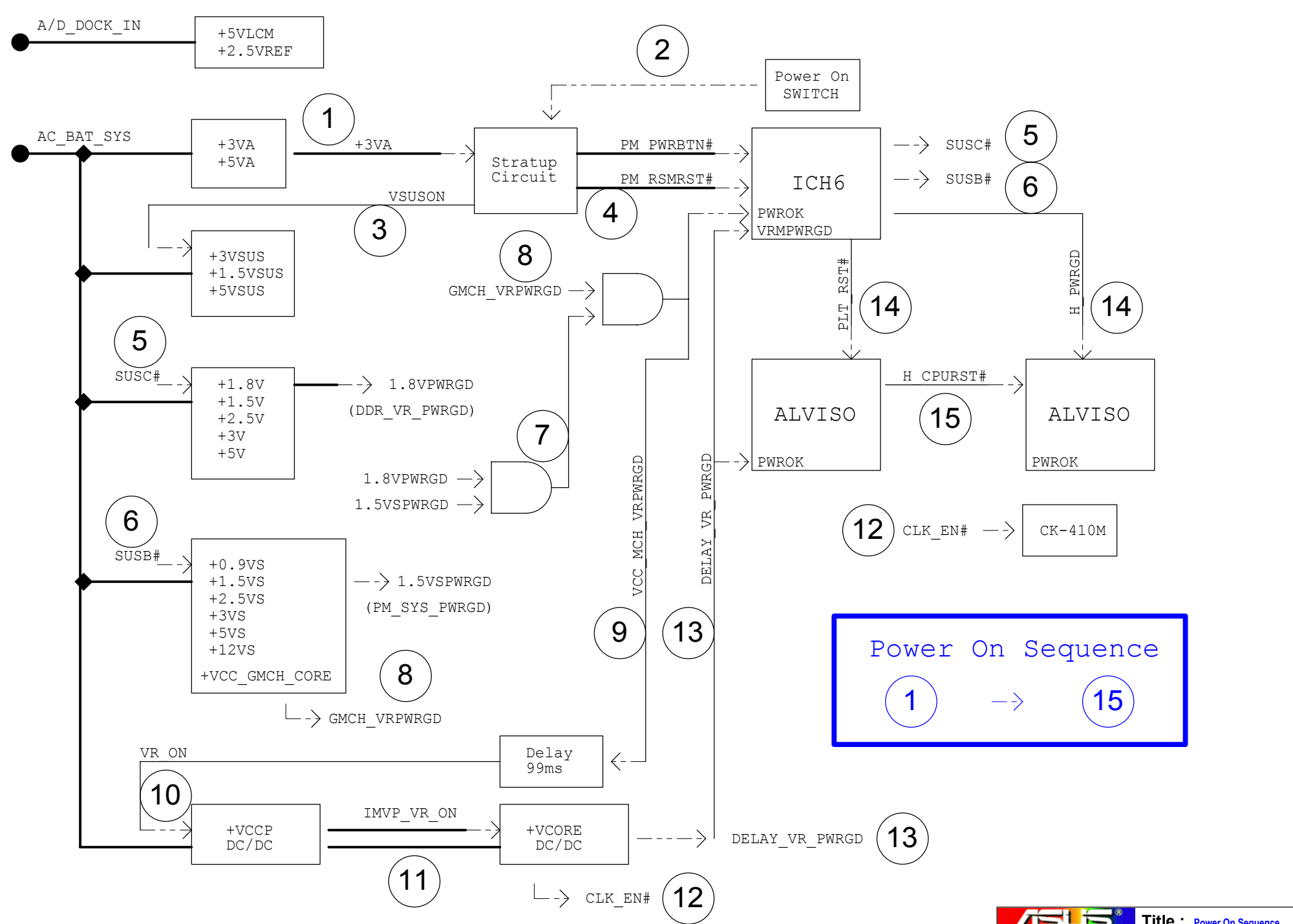
FOR TURN OFF THE VSUS POWER PLANE @ S4/S5 STATUS WHEN BATTERY ONLY



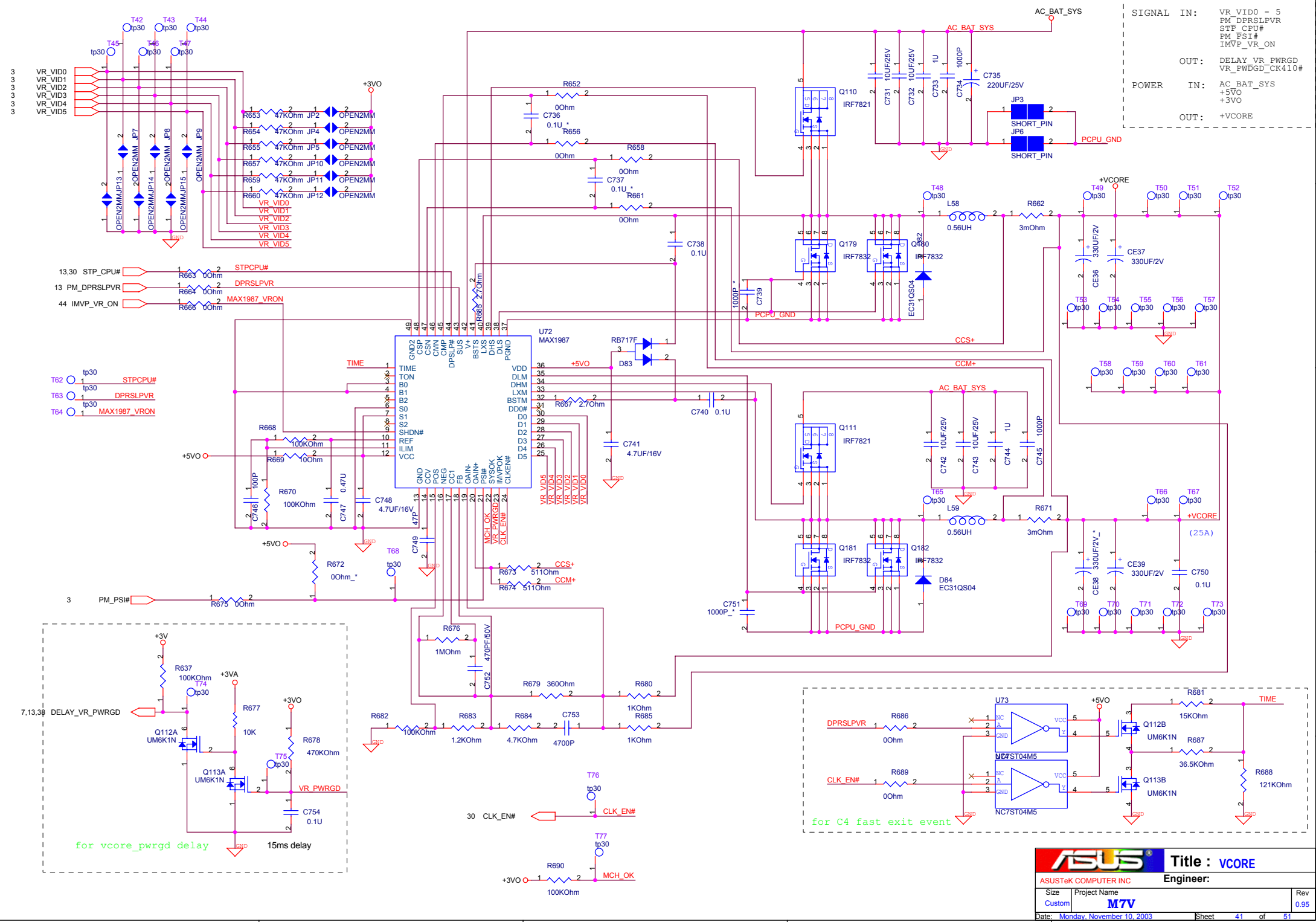
To Power circuits

POWER ON/OFF SEQUENCE

Delay 99ms



Power On Sequence
 1 → 15

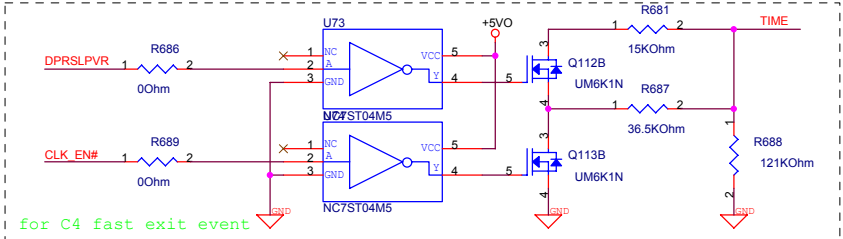


SIGNAL IN: VR_VID0 - 5
 PM_DPRSLPVR
 STP_CPU#
 PM_PSI#
 IMVP_VR_ON

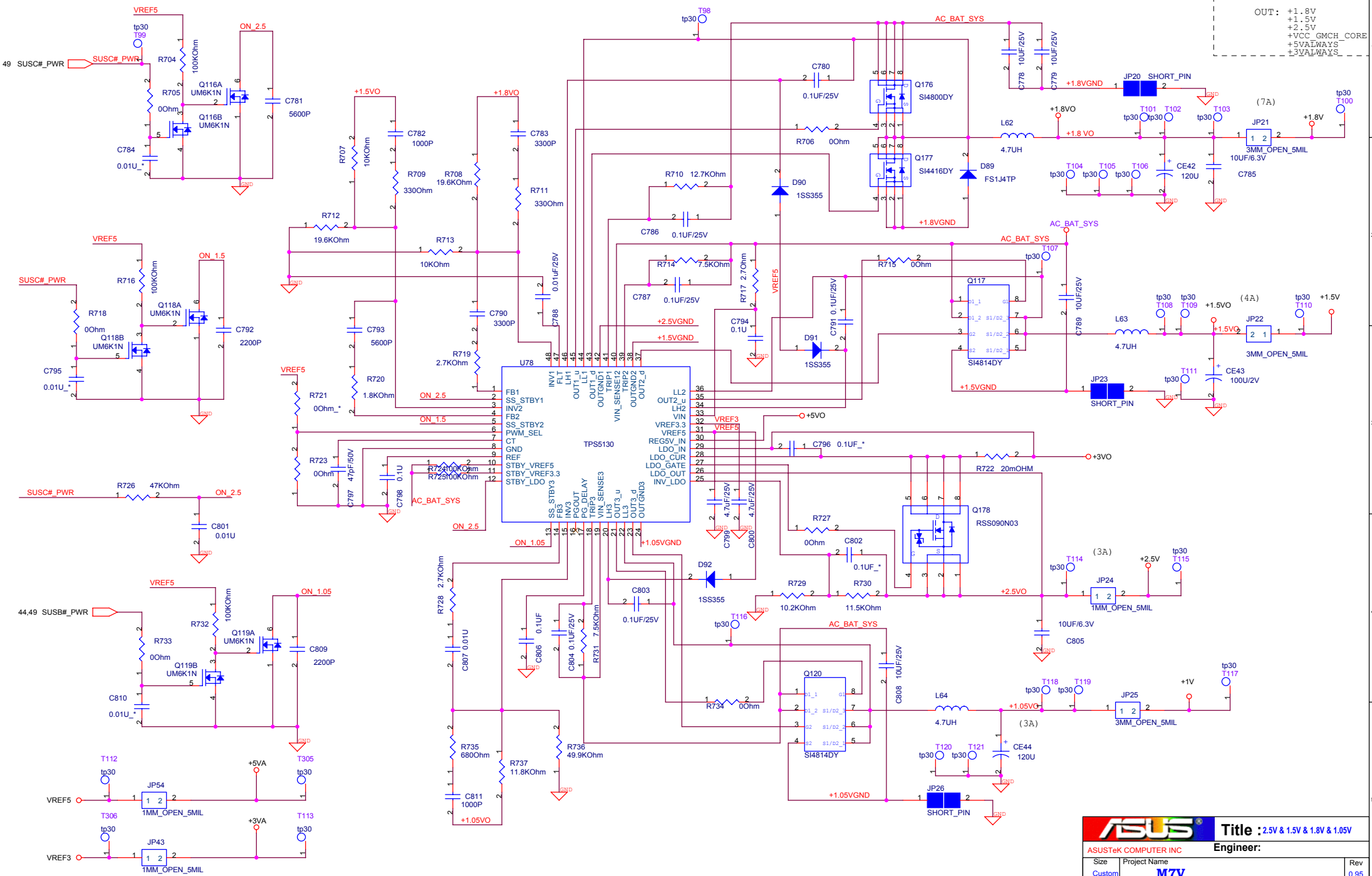
OUT: DELAY_VR_PWRGD
 VR_PWDGD_CK410#

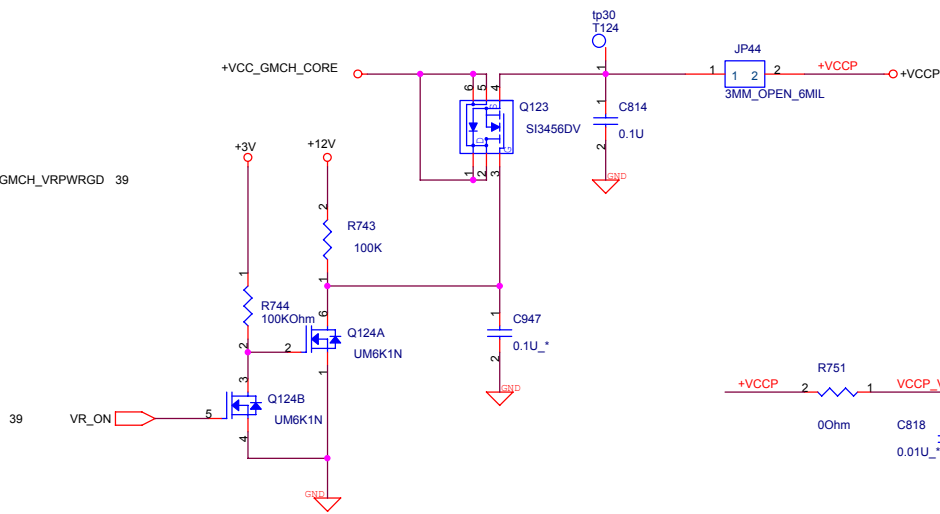
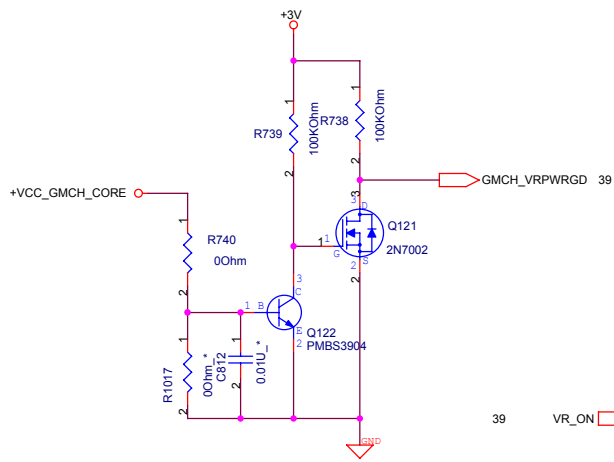
POWER IN: AC_BAT_SYS
 +5V0
 +3V0

OUT: +VCORE



SIGNAL IN: SUSB#_PWR
 SUSC#_PWR
 POWER IN: AC_BAT_SYS
 +3VO
 OUT: +1.8V
 +1.5V
 +2.5V
 +VCC_GMCH_CORE
 +5VALWAYS
 +3VALWAYS

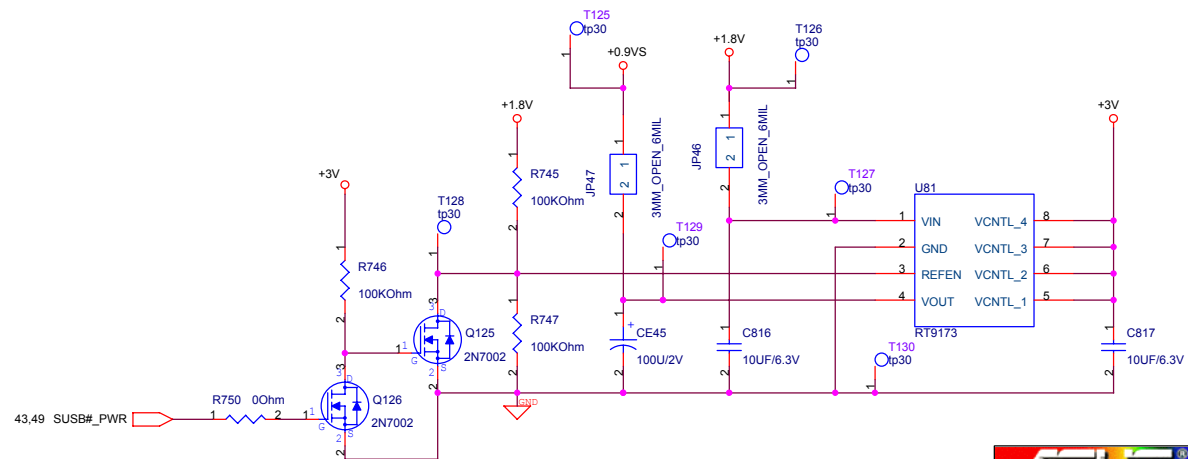
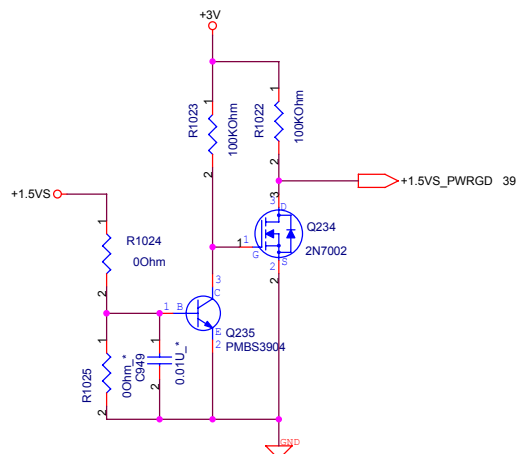
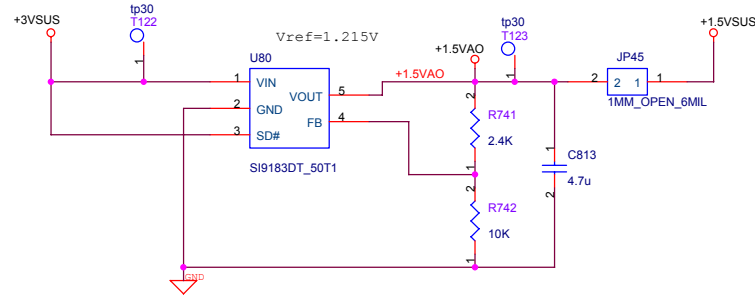
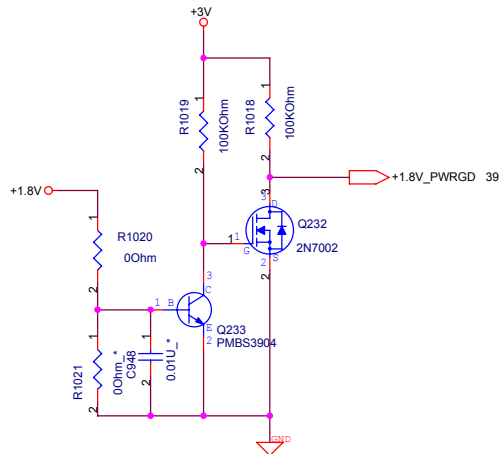


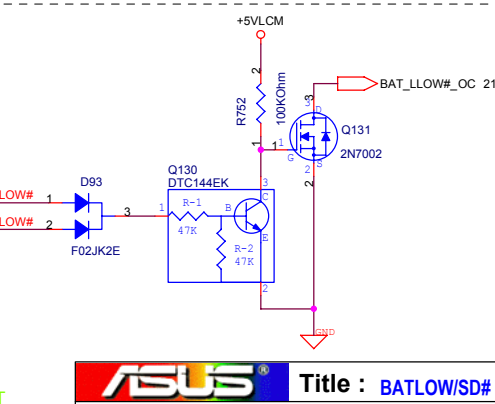
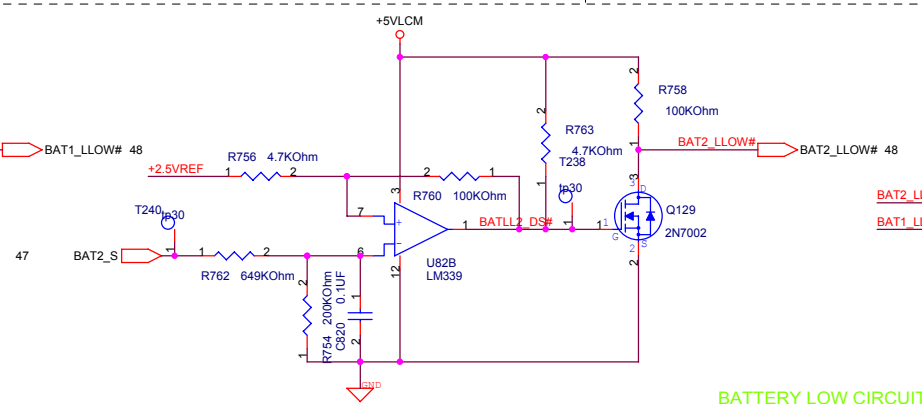
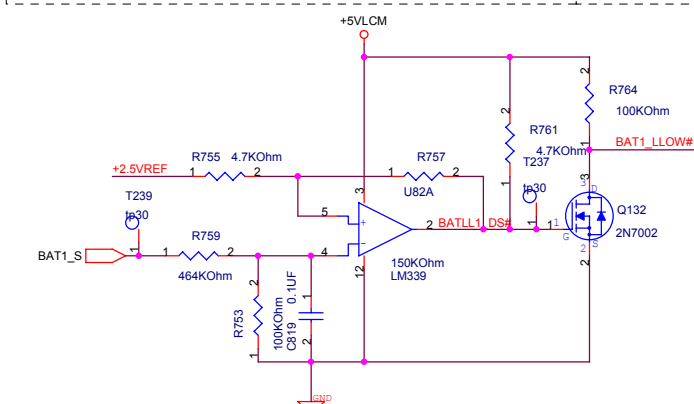
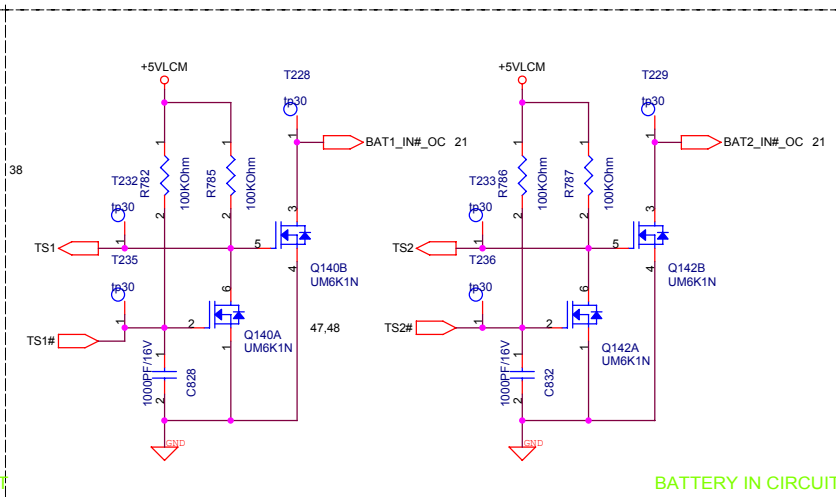
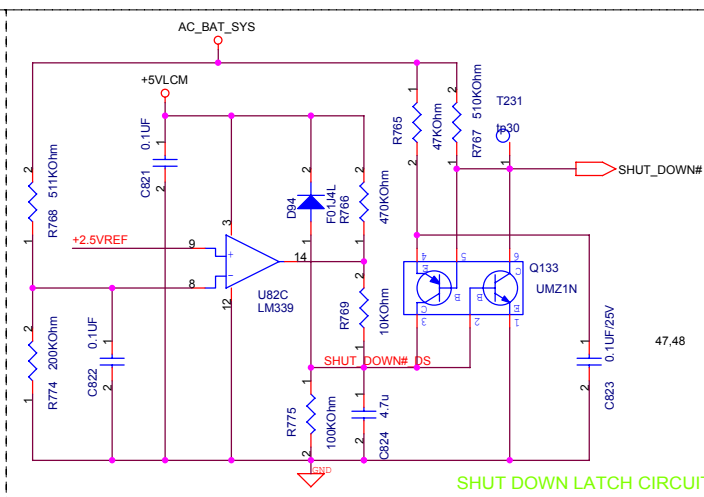
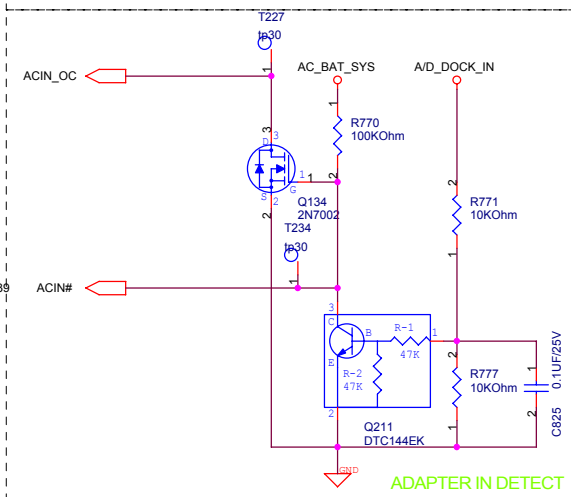
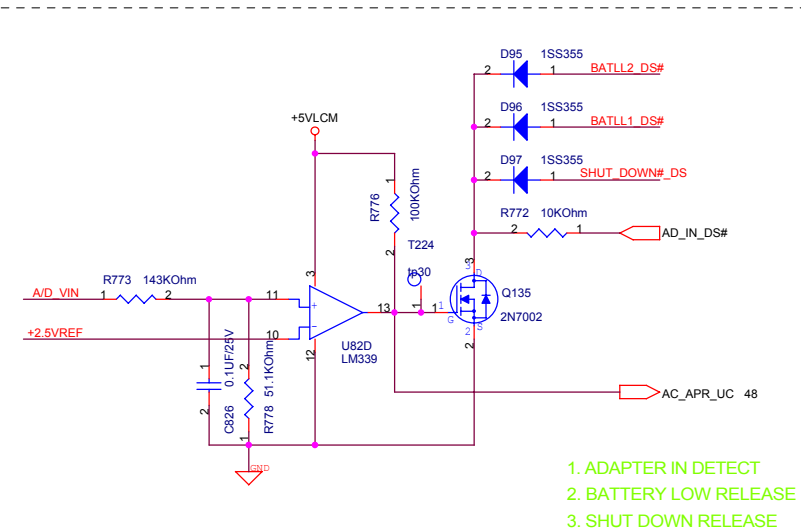
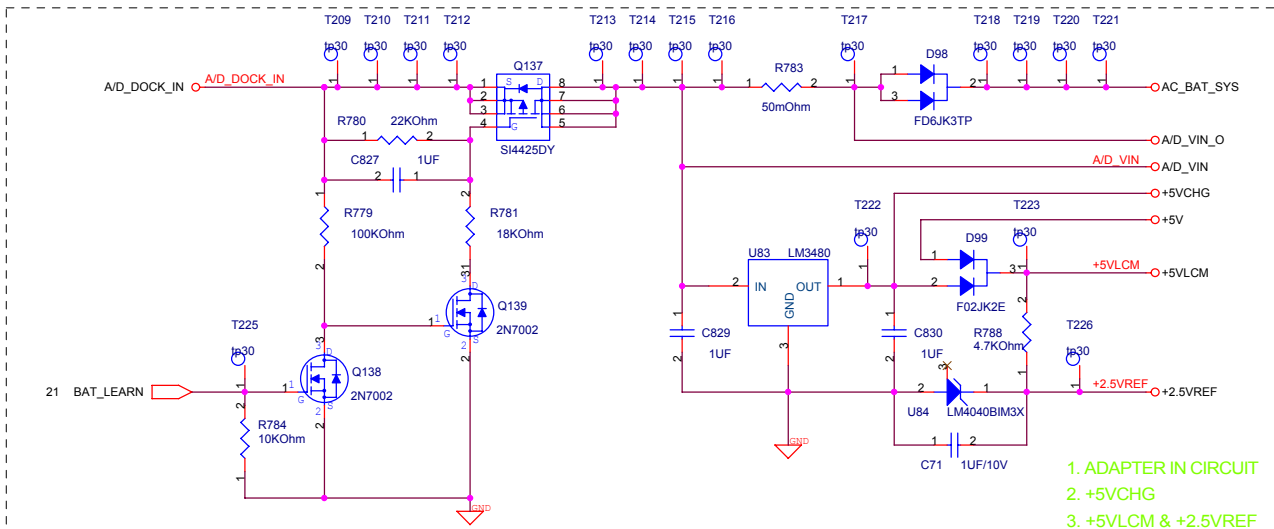


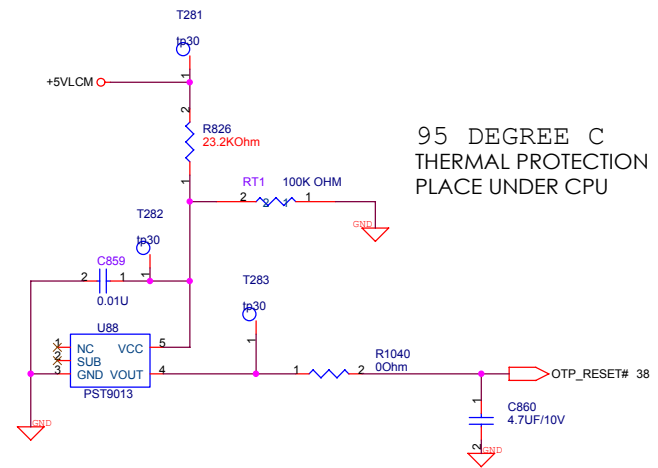
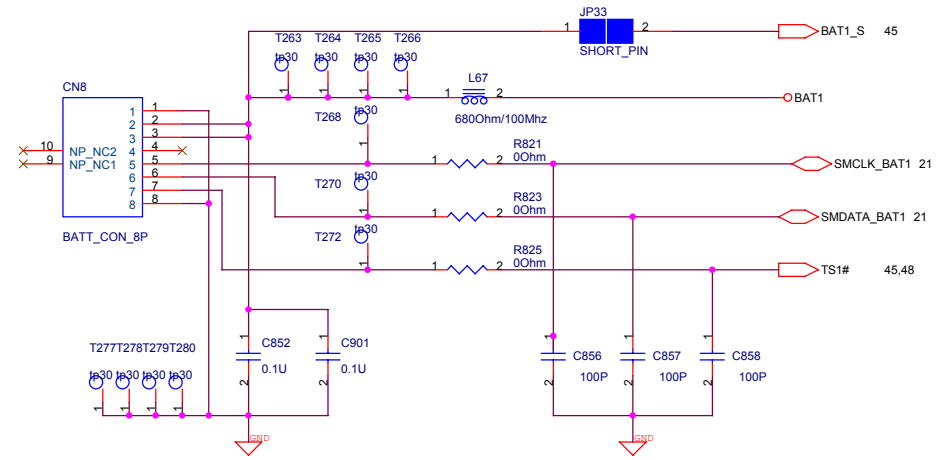
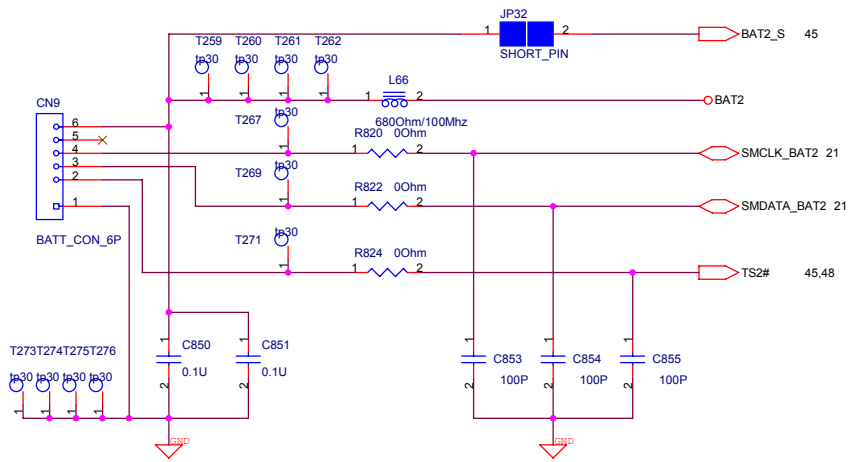
SIGNAL IN: SUSB#_PWR
 OUT: VCC_MCH_VRPWRGD
 IMVP_VR_ON

POWER IN: +3VA
 +3V
 +1.8V
 +VCC_GMCH_CORE

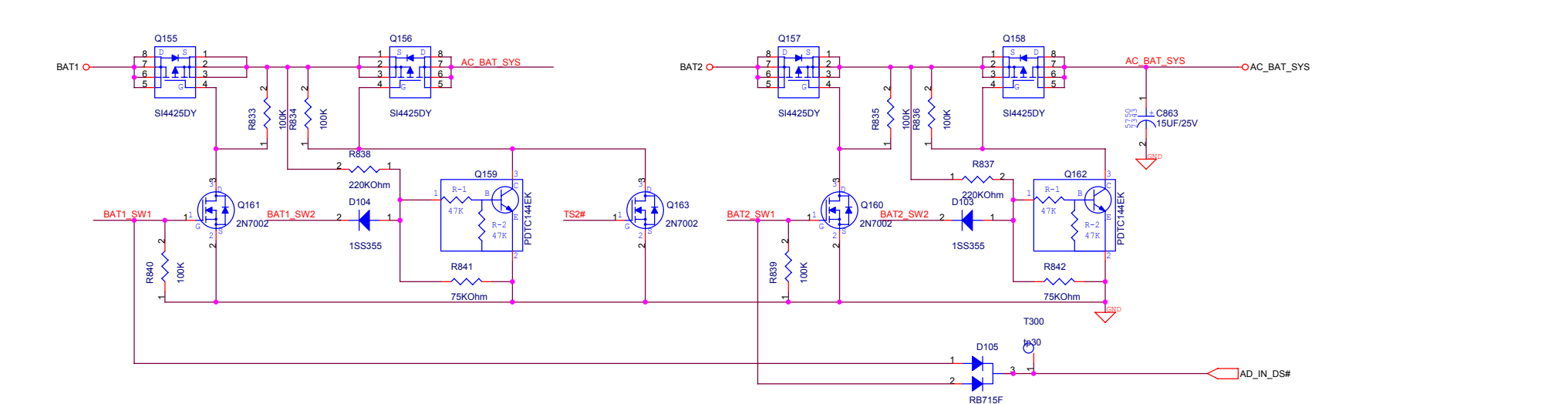
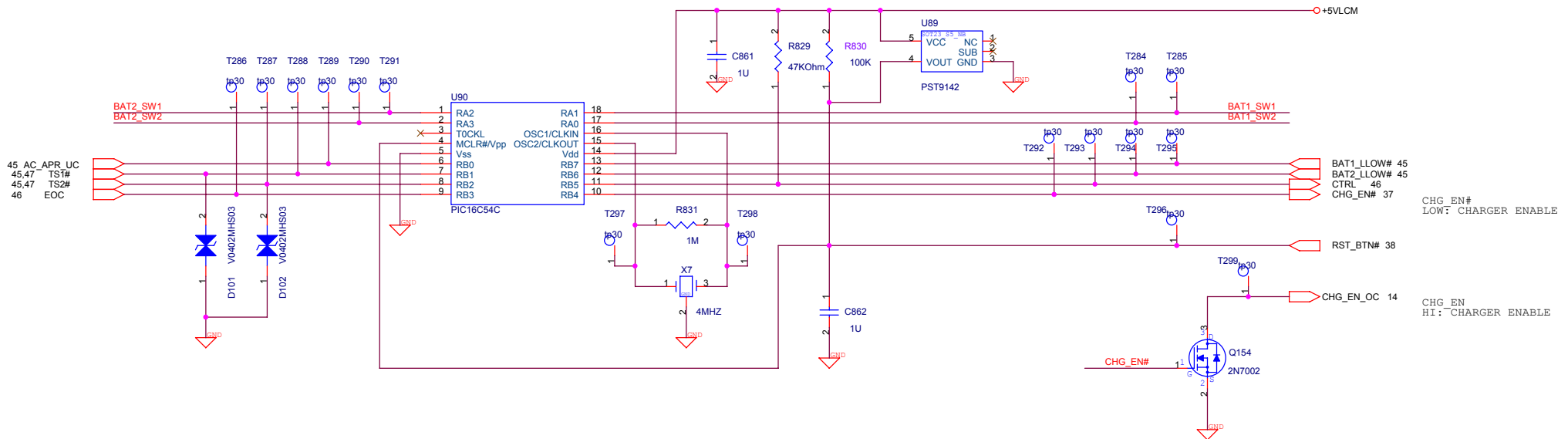
OUT: +0.9VS
 +1.5VA
 +VCCP

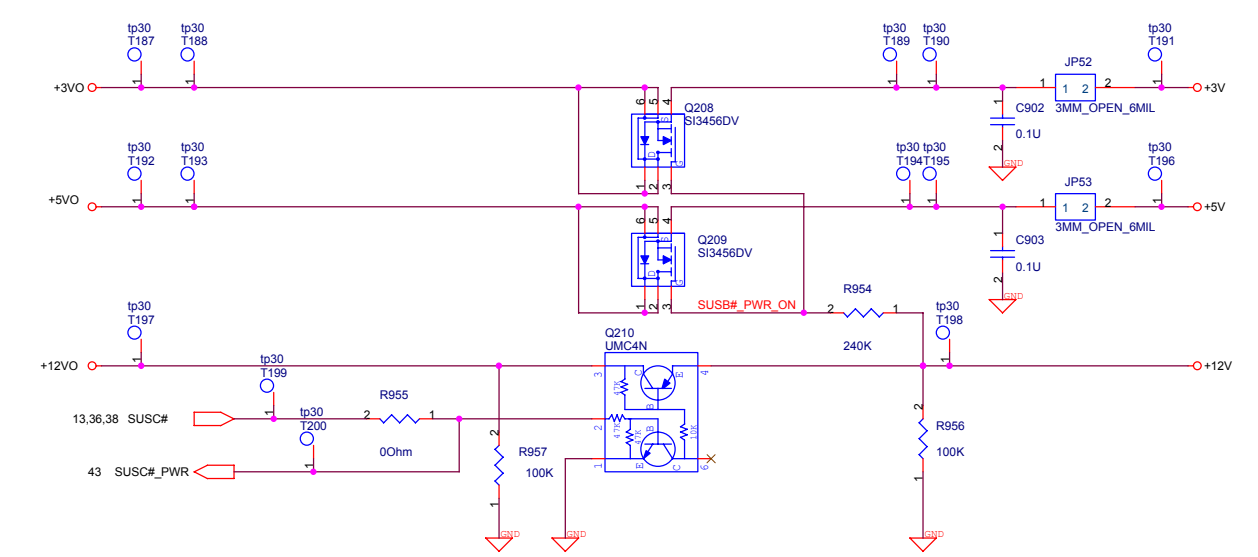
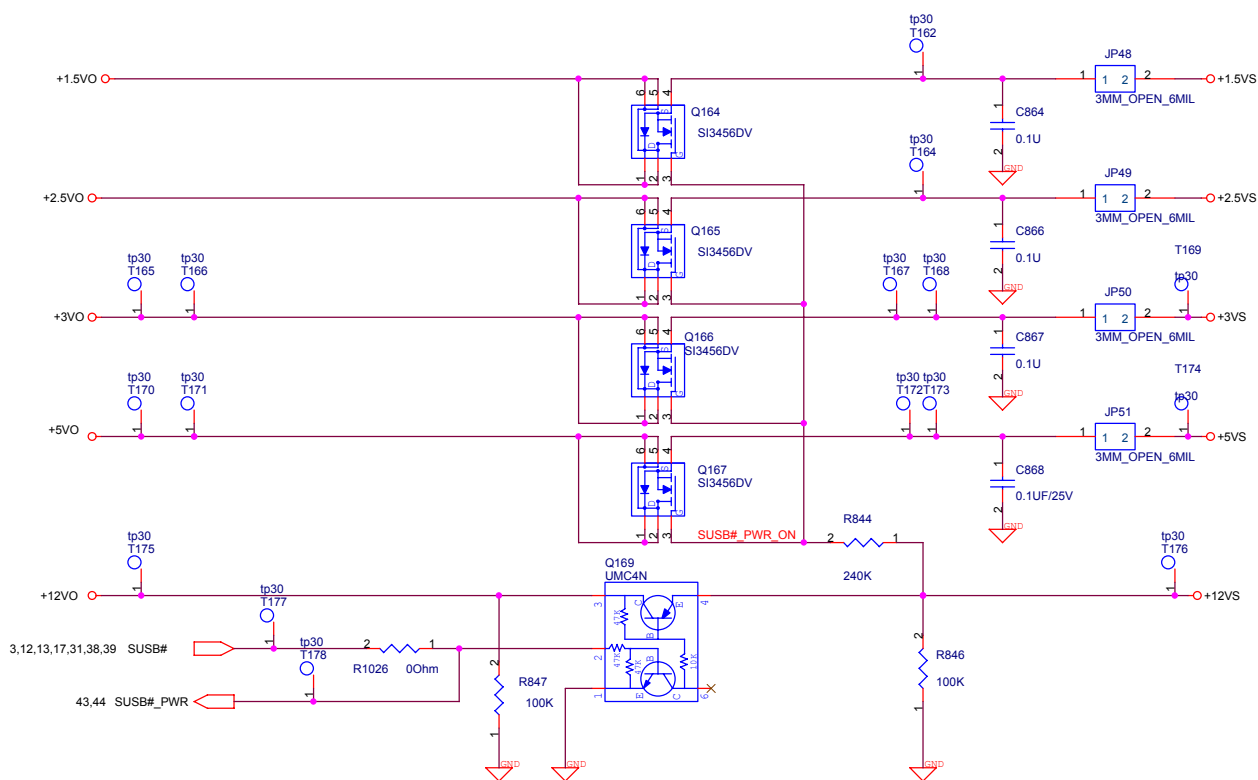
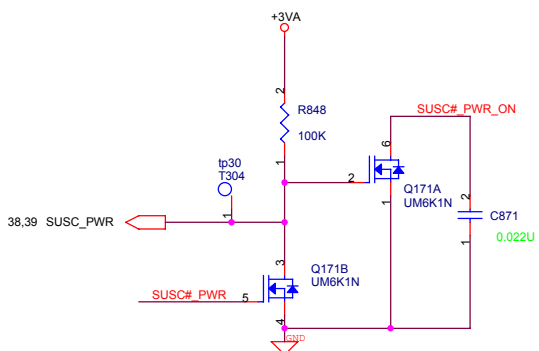
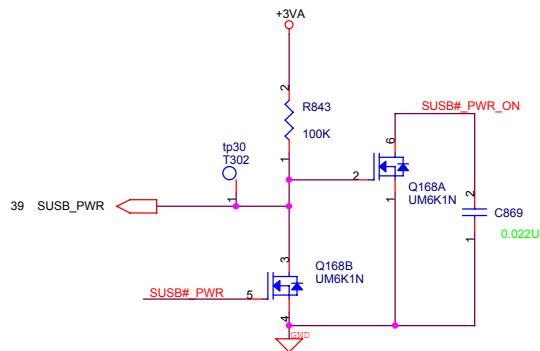
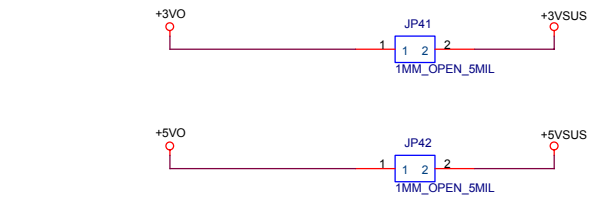






95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU





PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)
Ambient Light Sensor	0111001x (72)

ICH6-M GPIO	M7V	W2	Volt
GPI 0	KID0	KID0	5VREF
GPI 1	KID1	KID1	5VREF
GPI 2			5VREF
GPI 3			5VREF
GPI 4			5VREF
GPI 5			5VREF
GPI 7	CPPE# (NEWCARD)		3V
GPI 8	EXTSMI#	EXTSMI#	3VSUS
GPI 11	LID_ICH#	LID_ICH#	3VSUS
GPI 12	KB_SCI#	KB_SCI#	3V
GPI 13			3VSUS
GPI 14	CHG_EN_OC	CHG_EN_OC	3VSUS
GPI 15			3VSUS
GPO 16	XIDE_EN#		3V
GPO 17			3V
GPO 19	PWRLED_1HZ	PWRLED_1HZ	3V
GPO 21	BACK_OFF#	BACK_OFF#	3V
GPO 23	FWH_WP#	FWH_WP#	3V
GPIO 24	NEWCARD_RST#		3VSUS
GPI 26	SATA_DET#0	SATA_DET#0	3V
GPIO 27	PCB_ID0	PCB_ID0	3VSUS
GPIO 28	PCB_ID1	PCB_ID1	3VSUS
GPI 29	PCB_ID2	PCB_ID2	3V
GPI 30			3V
GPI 31	PEG_PRESENT#		3V
GPIO 33	BAY_IN0		3V
GPIO 34	BAY_IN1		3V
GPI 40	PANEL_ID0	PANEL_ID0	5VREF
GPI 41	PANEL_ID1	PANEL_ID1	3V
GPO 48	OP_SD#	OP_SD#	3V
			3V
GPIO 25	CB_SD#	CB_SD#	3VSUS

KBC GPIO	M7V	W2
P23	CLR_DJ#	MSK_INSTKEY#
P22	BAT_LEARN	BAT_LEARN
P21	BAT_SEL	
P20	KBCRSM	KBCRSM
P42		(WATCHDOG)
P43	SWDJ_EN#	SWDJ_EN#
P44	KB_CPURST	KB_CPURST
P45	KB_GATEA20	KB_GATEA20
P46	KBCSCI	KBCSCI
P47	PM_CLKRUN#	PM_CLKRUN#
P50	BAT_LLOW#_OC	BAT_LLOW#_OC
P51	SWDJ_LED	SWDJ_LED
P52	PM_LAN_ENABLE **	PM_LAN_ENABLE **
P53		
P54	BAYDOCK_IN#	
P55	BAT1_IN#_OC	BAT1_IN_OC#
P56		(FAN_DA1)
P57	INV_DA	ADJ_BL
P67	BAT2_IN#_OC	
P66	PADLOCK#	PADLOCK#
P65	MARATHON#	MARATHON#
P64	ACIN_OC	ACIN_OC
P63		
P62		
P61	INTERNET#	INTERNET#
P60	EMAIL#	EMAIL#
P75		(KB_CLK)
P74		(MS_CLK)
P73	TPAD_CLK	TPAD_CLK
P72		(KB_DAT)
P71		(MS_DAT)
P70	TPAD_DAT	TPAD_DAT
P77	BAT_SMC	BAT_SMC
P76	BAT_SMD	BAT_SMD
P27	SCROLL_LED#	SCROLLLOCK#
P26	NUM_LED#	NUM_LED#
P25	CAP_LED#	CAP_LED#
P24	SET_PLTRSTNS#	SET_PLTRSTNS#
P40	EXT_SMI	KBC_EXTSMI
P41	EMAIL_LED#	EMAIL_LED#