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**BOM Control Table**

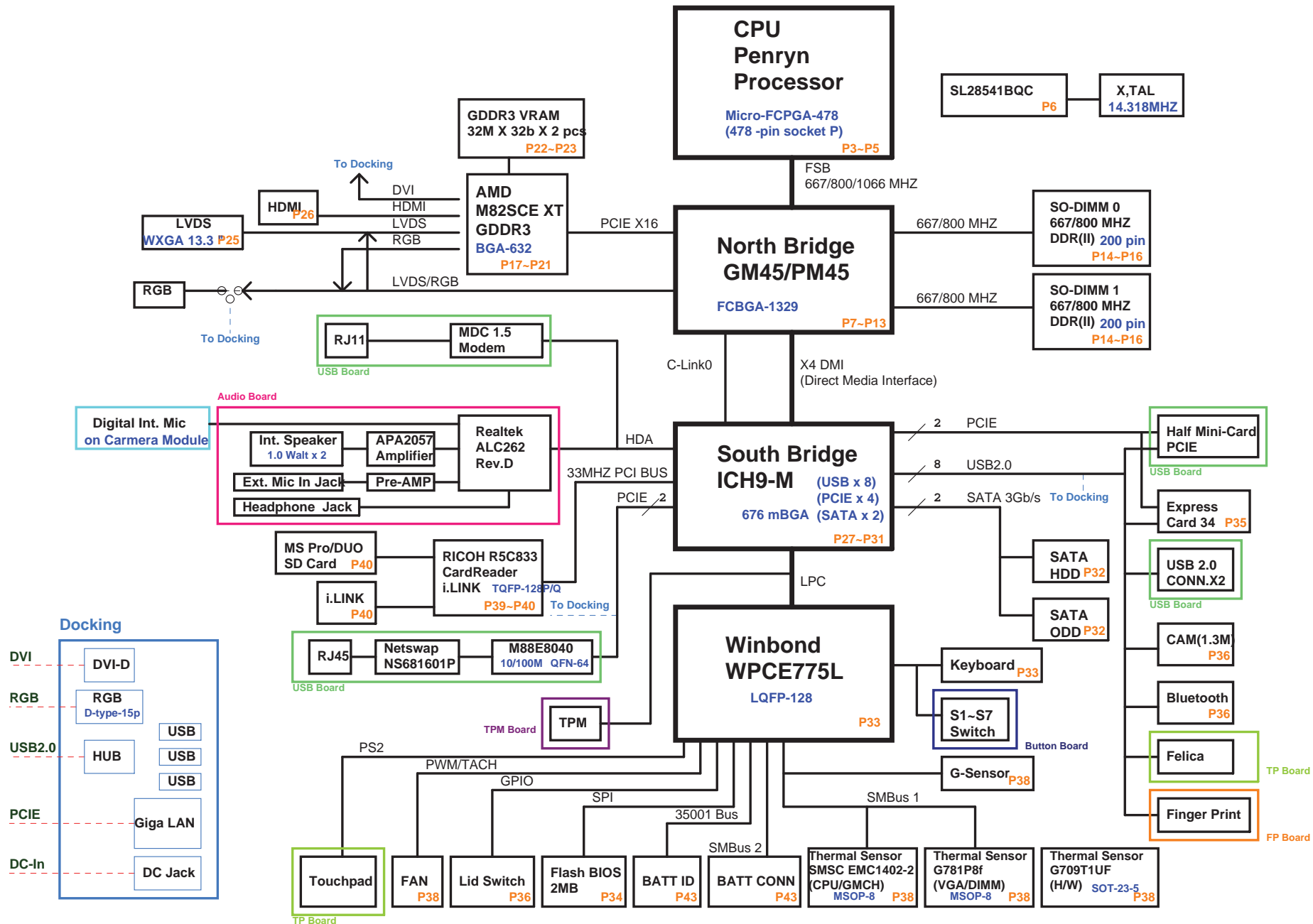
Value Prefix	CA_	AT_	DS_	ND_	LND_	HD_
UMA (W/ Dock)	v		v			
UMA (W/O Dock)	v			v	v	
M82 (W/ Dock)		v	v			
M82 (W/O Dock HDMI)		v		v		
M82 (w/dock W/ HDMI )		v	v			v

**Project Code & Schematics Subject:** M750 Main Board

**PCB P/N:**

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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# M750 (Montevina + M82SCE XT)



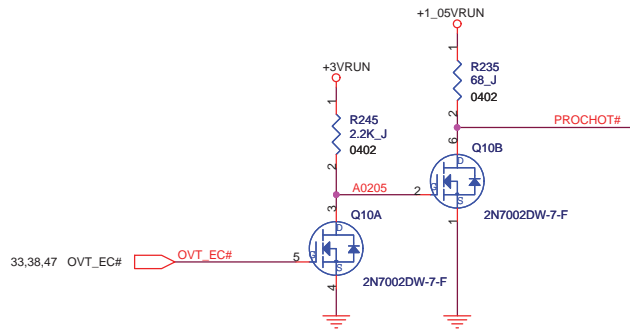
7 H\_AA#[3..35]

7 H\_ADSTB#0  
7 H\_REQ#[4..0]

7 H\_ADSTB#1  
28 H\_A20M#  
28 H\_FERR#  
28 H\_IGNNE#  
28 H\_STPCLK#  
28 H\_INTR#  
28 H\_NMI#  
28 H\_SMI#

TP98 26MIL	1	TP CPU RSVD01	M4	RSVD[01]
TP102 26MIL	1	TP CPU RSVD02	N5	RSVD[02]
TP86 26MIL	1	TP CPU RSVD03	T2	RSVD[03]
TP99 26MIL	1	TP CPU RSVD04	V3	RSVD[04]
TP78 26MIL	1	TP CPU RSVD05	B2	RSVD[05]
TP91 26MIL	1	CPU TEST7	C3	RSVD[06]
TP94 26MIL	1	TP CPU RSVD07	D2	RSVD[07]
TP121 26MIL	1	TP CPU RSVD08	D22	RSVD[08]
TP93 26MIL	1	TP CPU RSVD09	D3	RSVD[09]
TP105 26MIL	1	TP CPU RSVD10	F6	RSVD[10]

CPU SOCKET\_478P  
FOX\_PZ4782A-274M-01



**ADDR GROUP 0**

H A#3	J4	A[3]#
H A#4	L5	A[4]#
H A#5	L4	A[5]#
H A#6	K5	A[6]#
H A#7	M3	A[7]#
H A#8	N2	A[8]#
H A#9	J1	A[9]#
H A#10	N3	A[10]#
H A#11	F5	A[11]#
H A#12	P2	A[12]#
H A#13	L2	A[13]#
H A#14	P4	A[14]#
H A#15	P1	A[15]#
H A#16	R1	A[16]#
H A#17	Y2	A[17]#
H A#18	U5	A[18]#
H A#19	R3	A[19]#
H A#20	W6	A[20]#
H A#21	U4	A[21]#
H A#22	Y5	A[22]#
H A#23	U1	A[23]#
H A#24	R4	A[24]#
H A#25	T5	A[25]#
H A#26	T3	A[26]#
H A#27	W2	A[27]#
H A#28	W5	A[28]#
H A#29	Y4	A[29]#
H A#30	U2	A[30]#
H A#31	V4	A[31]#
H A#32	W3	A[32]#
H A#33	AA4	A[33]#
H A#34	AB2	A[34]#
H A#35	AA3	A[35]#

**ADDR GROUP 1**

H A#17	Y2	A[17]#
H A#18	U5	A[18]#
H A#19	R3	A[19]#
H A#20	W6	A[20]#
H A#21	U4	A[21]#
H A#22	Y5	A[22]#
H A#23	U1	A[23]#
H A#24	R4	A[24]#
H A#25	T5	A[25]#
H A#26	T3	A[26]#
H A#27	W2	A[27]#
H A#28	W5	A[28]#
H A#29	Y4	A[29]#
H A#30	U2	A[30]#
H A#31	V4	A[31]#
H A#32	W3	A[32]#
H A#33	AA4	A[33]#
H A#34	AB2	A[34]#
H A#35	AA3	A[35]#

**CONTROL**

ADSB#	H1	H_ADS# 7
BNR#	E2	H_BNR# 7
BPR#	G5	H_BPR# 7
DEFER#	H5	H_DEFER# 7
DRDY#	F21	H_DRDY# 7
DBSY#	E1	H_DBSY# 7
BR0#	F1	H_BREQ#0 7
IERR#	D20	H_IERR#
INIT#	B3	H_INIT# 28
LOCK#	H4	H_LOCK# 7
RESET#	C1	H_CPURST# 7
RS[0]#	E3	H_RS#0 7
RS[1]#	F4	H_RS#1 7
RS[2]#	G3	H_RS#2 7
TRDY#	G2	H_TRDY# 7
HIT#	G6	H_HIT# 7
HITM#	E4	H_HITM# 7

**THERMAL**

PROCHOT#	D21	PROCHOT#
THERMDA	A24	H_THERMDA 38
THERMDC	B25	H_THERMDC 38
HERMTRIP#	C7	THRMTRIP# CPU R171 1 2

**H CLK**

BCLK[0]	A22	CLK_CPU_BCLK 6
BCLK[1]	A21	CLK_CPU_BCLK# 6

CPU SOCKET\_478P  
FOX\_PZ4782A-274M-01

RESERVED

RESERVED

RESERVED

RESERVED

RESERVED

RESERVED

RESERVED

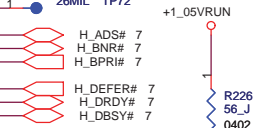
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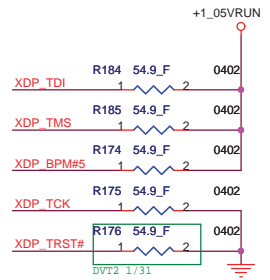
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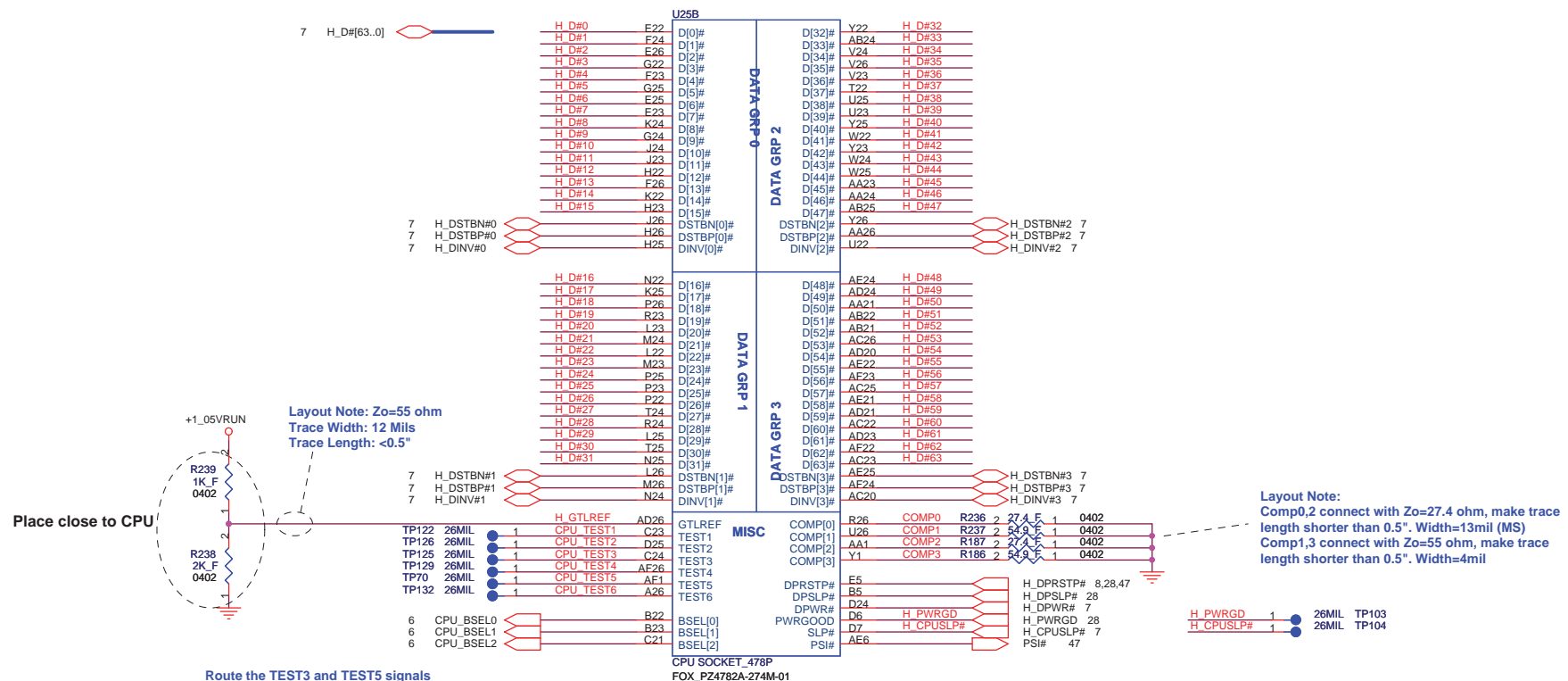


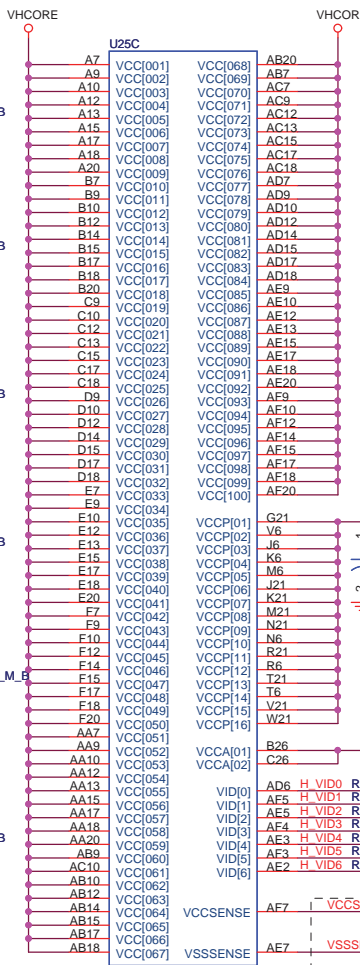
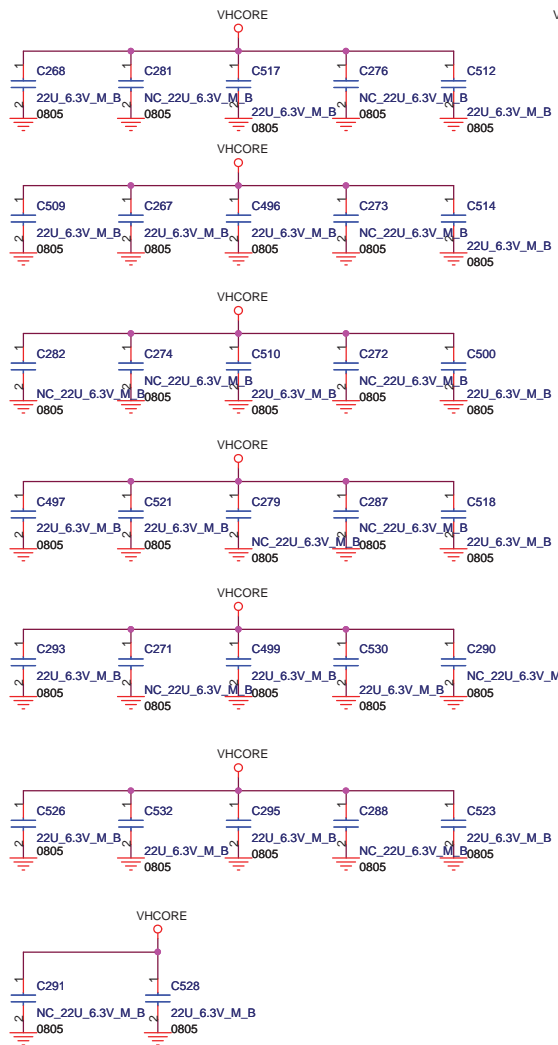
H\_CPURST# 1 26MIL TP85



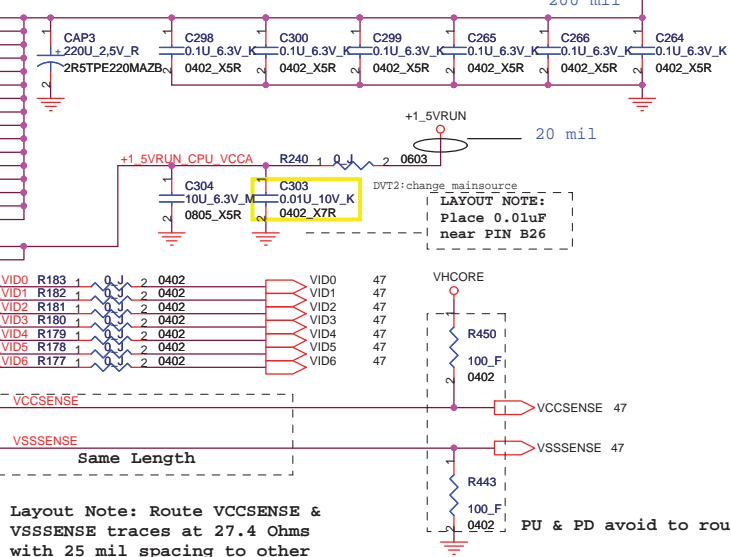
For SI Probe Point

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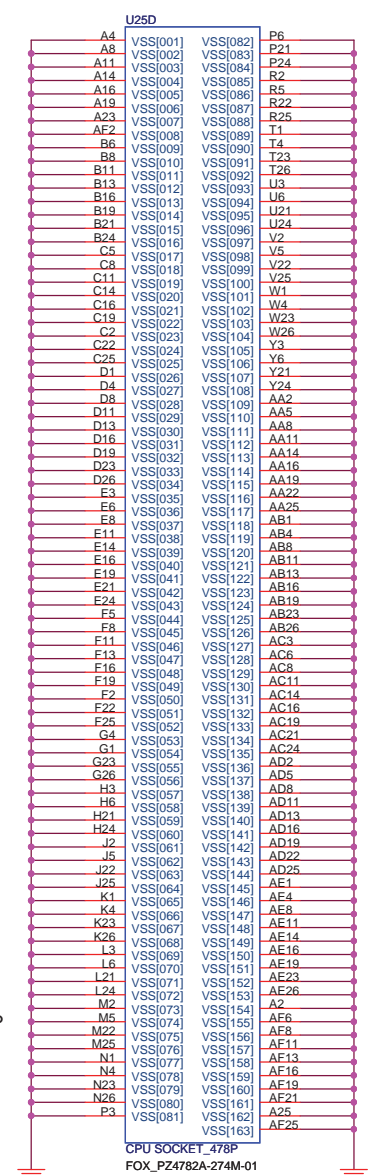


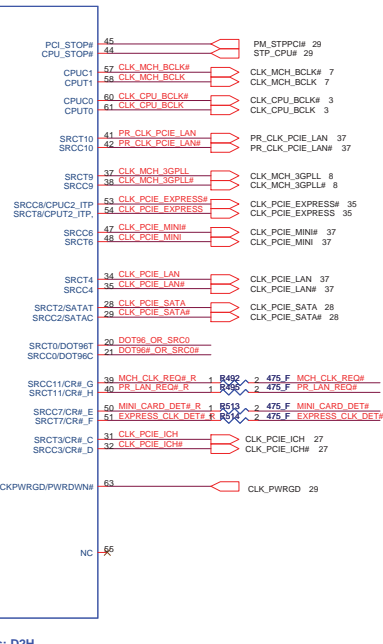
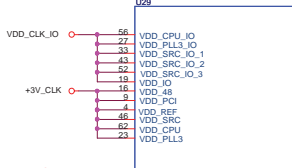
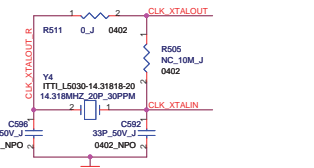
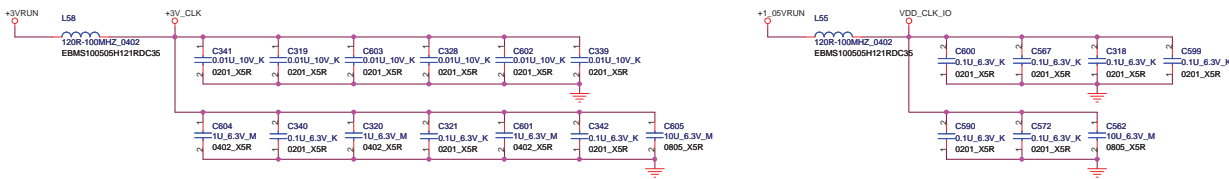
CPU\_VCCA---->0.13A  
 CPU\_VCCP---->2.5A  
 CPU\_VCC---->47A



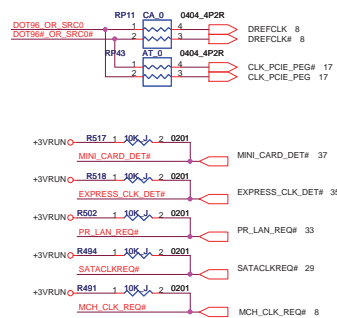
Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.

Outer width=13 mil spacing=7 mil  
 Inner width=13 mil spacing=7 mil  
 Length match < 25 mil



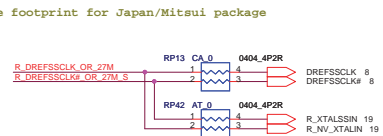
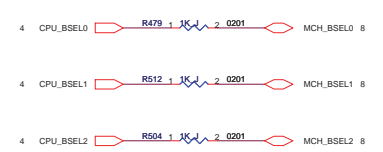


Clock Request	Clock Request Function
CR#A	SRC0, 2
CR#B	SRC1, 4
CR#C	SRC0, 2
CR#D	SRC1, 4
CR#E	SRC6
CR#F	SRC8
CR#G	SRC9
CR#H	SRC10



**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

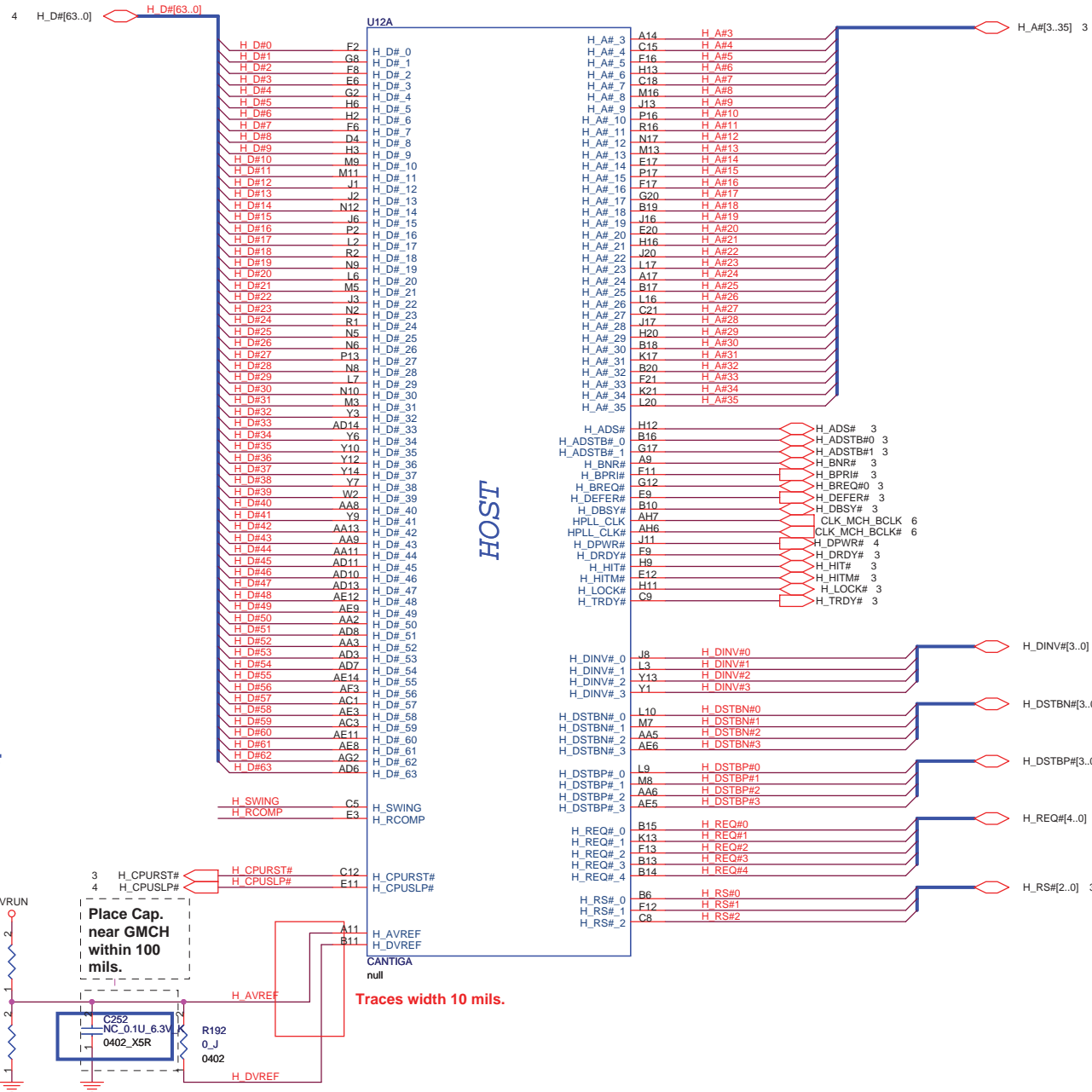


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File: **CLOCK GEN**

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HOST

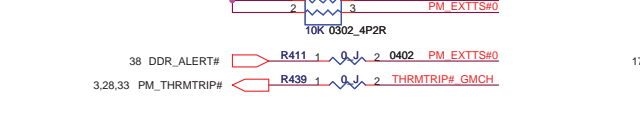
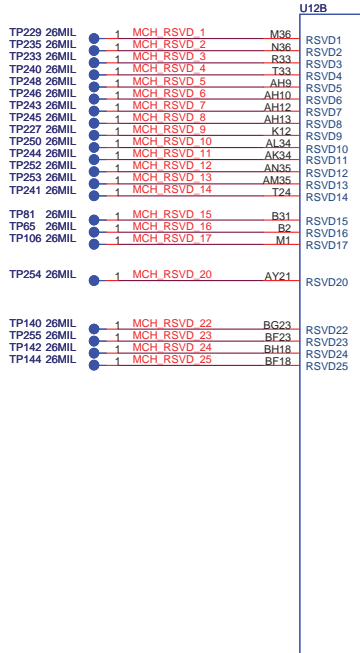
Place Cap.  
near GMCH  
within 100  
mils.

Traces width 10 mils.

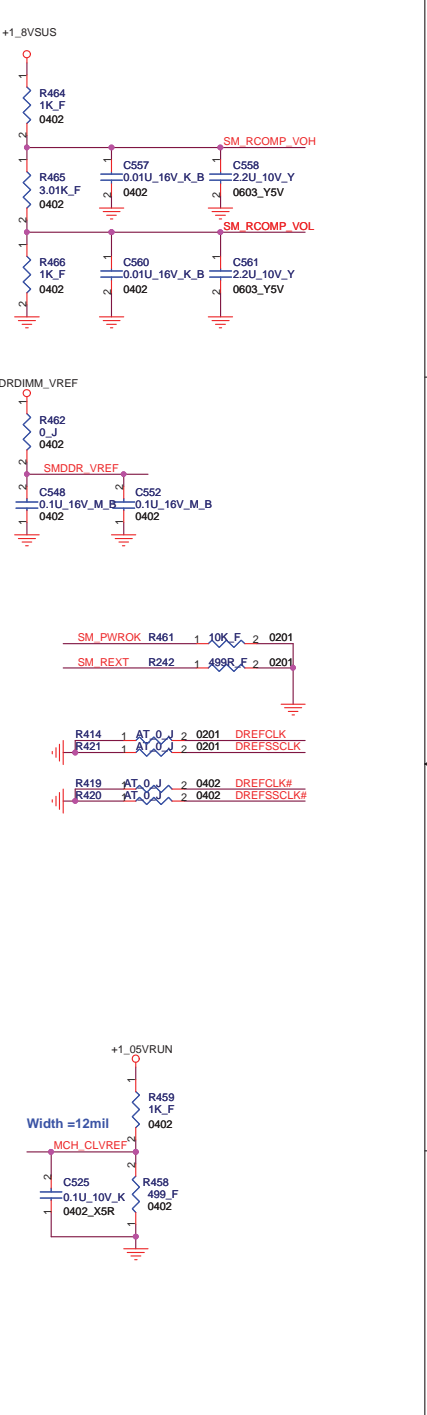
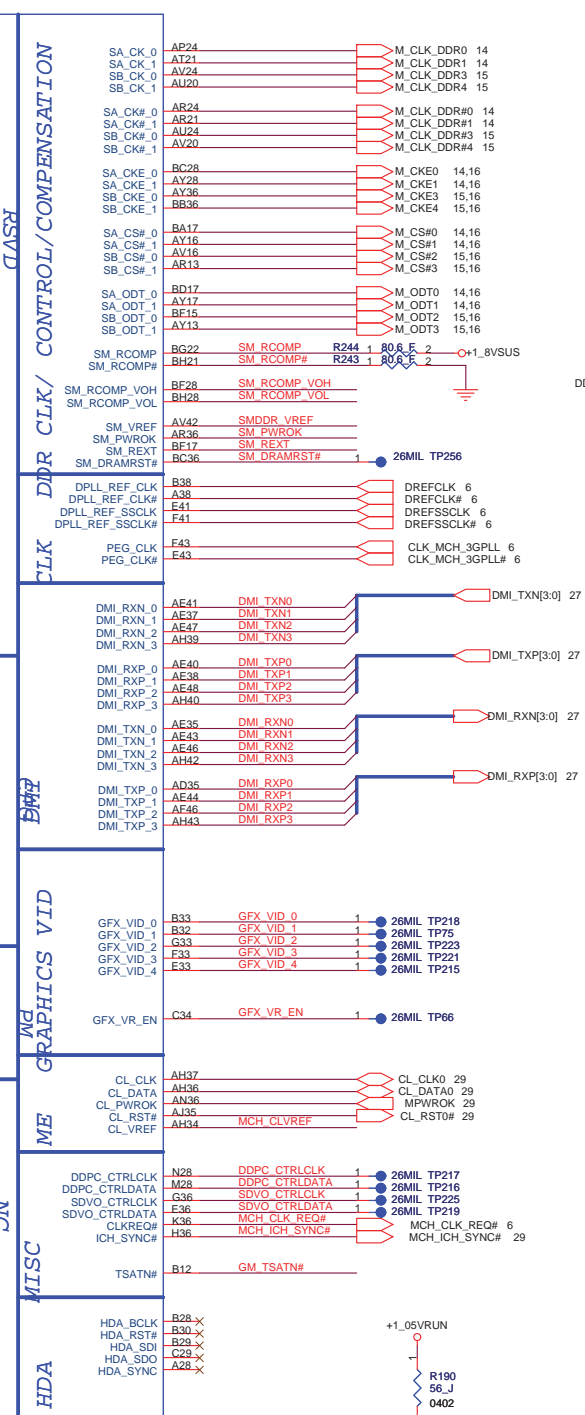
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
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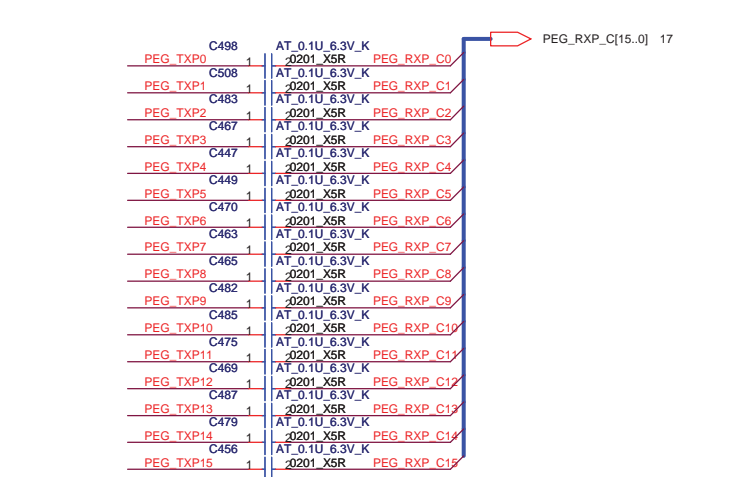
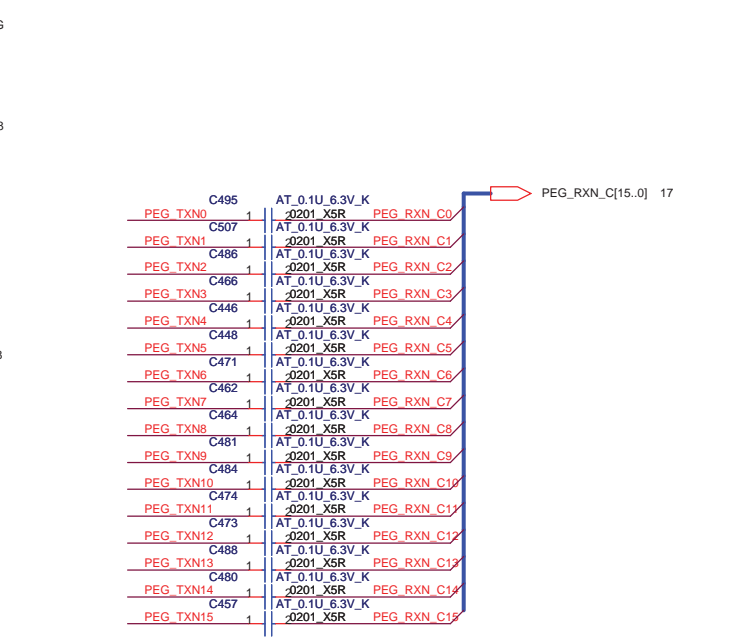
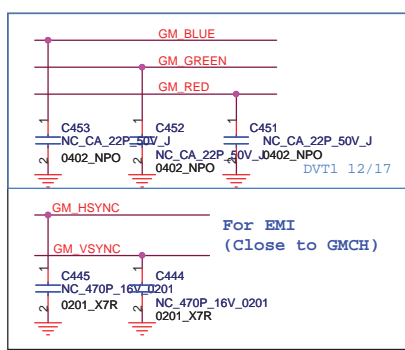
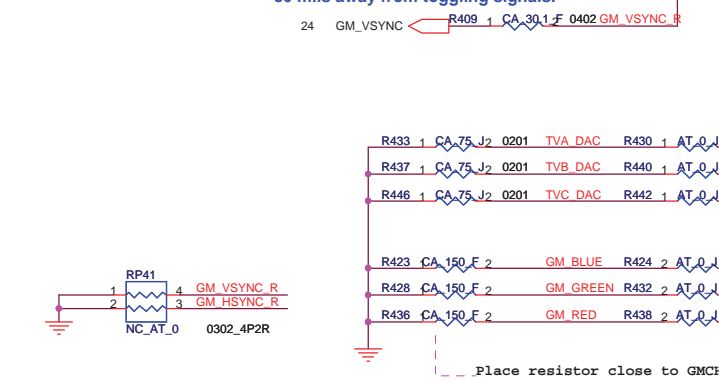
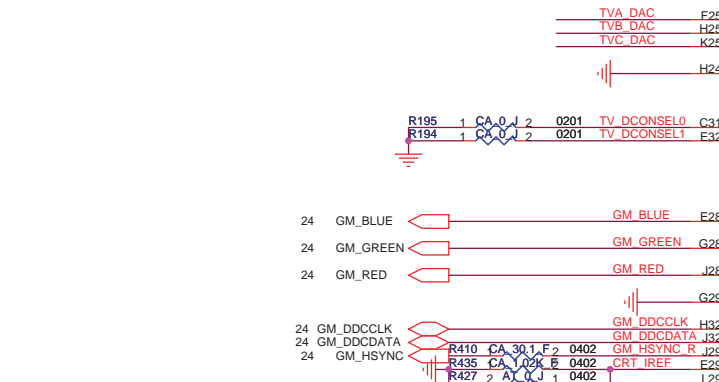
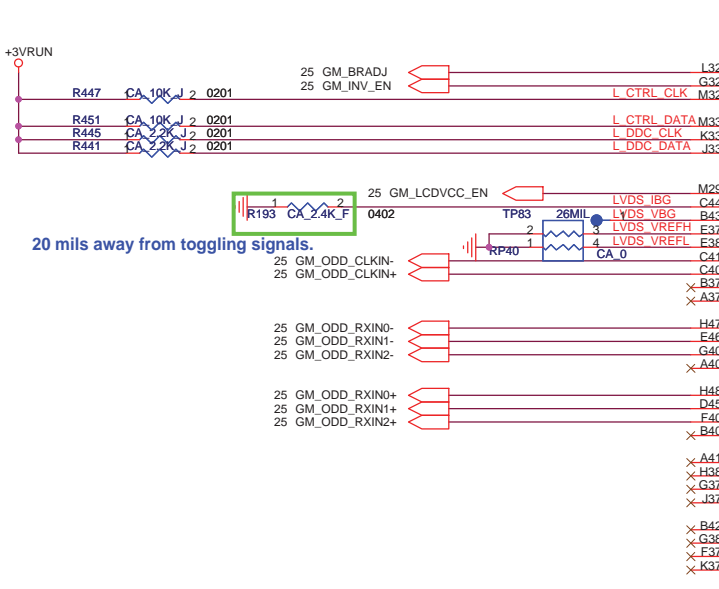
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Lane Reversed High = Normal operation
MCH_CFG_10 PCIe Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously with the PEG port



U12B  
CFG17[3] Internal pull-up  
CFG20[18] Internal pull-down







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14 M\_A\_DQ[63..0]

M_A_DQ0	AJ38	SA_DQ_0
M_A_DQ1	AJ41	SA_DQ_1
M_A_DQ2	AN38	SA_DQ_2
M_A_DQ3	AM38	SA_DQ_3
M_A_DQ4	AJ36	SA_DQ_4
M_A_DQ5	AJ40	SA_DQ_5
M_A_DQ6	AM44	SA_DQ_6
M_A_DQ7	AM42	SA_DQ_7
M_A_DQ8	AN43	SA_DQ_8
M_A_DQ9	AN44	SA_DQ_9
M_A_DQ10	AI40	SA_DQ_10
M_A_DQ11	AT38	SA_DQ_11
M_A_DQ12	AN41	SA_DQ_12
M_A_DQ13	AN39	SA_DQ_13
M_A_DQ14	AI44	SA_DQ_14
M_A_DQ15	AI42	SA_DQ_15
M_A_DQ16	AV39	SA_DQ_16
M_A_DQ17	AY44	SA_DQ_17
M_A_DQ18	BA40	SA_DQ_18
M_A_DQ19	BD43	SA_DQ_19
M_A_DQ20	AV41	SA_DQ_20
M_A_DQ21	AY43	SA_DQ_21
M_A_DQ22	BA43	SA_DQ_22
M_A_DQ23	BC40	SA_DQ_23
M_A_DQ24	AY37	SA_DQ_24
M_A_DQ25	BD38	SA_DQ_25
M_A_DQ26	AV37	SA_DQ_26
M_A_DQ27	AT36	SA_DQ_27
M_A_DQ28	AV38	SA_DQ_28
M_A_DQ29	B338	SA_DQ_29
M_A_DQ30	AV36	SA_DQ_30
M_A_DQ31	AW36	SA_DQ_31
M_A_DQ32	BD13	SA_DQ_32
M_A_DQ33	AU11	SA_DQ_33
M_A_DQ34	BC11	SA_DQ_34
M_A_DQ35	BA12	SA_DQ_35
M_A_DQ36	AU13	SA_DQ_36
M_A_DQ37	AV13	SA_DQ_37
M_A_DQ38	BD12	SA_DQ_38
M_A_DQ39	BC12	SA_DQ_39
M_A_DQ40	BB9	SA_DQ_40
M_A_DQ41	BA9	SA_DQ_41
M_A_DQ42	AU10	SA_DQ_42
M_A_DQ43	AV9	SA_DQ_43
M_A_DQ44	BA11	SA_DQ_44
M_A_DQ45	BD9	SA_DQ_45
M_A_DQ46	AY8	SA_DQ_46
M_A_DQ47	BAG	SA_DQ_47
M_A_DQ48	AV5	SA_DQ_48
M_A_DQ49	AV7	SA_DQ_49
M_A_DQ50	AT9	SA_DQ_50
M_A_DQ51	AN8	SA_DQ_51
M_A_DQ52	AU5	SA_DQ_52
M_A_DQ53	AU6	SA_DQ_53
M_A_DQ54	AT5	SA_DQ_54
M_A_DQ55	AN10	SA_DQ_55
M_A_DQ56	AM11	SA_DQ_56
M_A_DQ57	AM5	SA_DQ_57
M_A_DQ58	AJ9	SA_DQ_58
M_A_DQ59	AJ8	SA_DQ_59
M_A_DQ60	AN12	SA_DQ_60
M_A_DQ61	AM13	SA_DQ_61
M_A_DQ62	AJ11	SA_DQ_62
M_A_DQ63	AJ12	SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	14,16
SA_BS_1	BG18	M_A_BS1	14,16
SA_BS_2	AT25	M_A_BS2	14,16
SA_RAS#	BB20	M_A_RAS#	14,16
SA_CAS#	BD20	M_A_CAS#	14,16
SA_WE#	AY20	M_A_WE#	14,16
SA_DM_0	AM37	M_A_DM0	14
SA_DM_1	AT41	M_A_DM1	14
SA_DM_2	AY41	M_A_DM2	14
SA_DM_3	AU39	M_A_DM3	14
SA_DM_4	BB12	M_A_DM4	14
SA_DM_5	AY6	M_A_DM5	14
SA_DM_6	AT7	M_A_DM6	14
SA_DM_7	AJ5	M_A_DM7	14
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	AT44	M_A_DQS1	14
SA_DQS_2	BA43	M_A_DQS2	14
SA_DQS_3	BC37	M_A_DQS3	14
SA_DQS_4	AW12	M_A_DQS4	14
SA_DQS_5	BC8	M_A_DQS5	14
SA_DQS_6	AU8	M_A_DQS6	14
SA_DQS_7	AM7	M_A_DQS7	14
SA_DQS#_0	AT43	M_A_DQS#0	14
SA_DQS#_1	BA44	M_A_DQS#1	14
SA_DQS#_2	BD37	M_A_DQS#2	14
SA_DQS#_3	AY12	M_A_DQS#3	14
SA_DQS#_4	BD8	M_A_DQS#4	14
SA_DQS#_5	AU9	M_A_DQS#5	14
SA_DQS#_6	AM8	M_A_DQS#6	14
SA_DQS#_7	AM8	M_A_DQS#7	14
SA_MA_0	BA21	M_A_A0	14,16
SA_MA_1	BC24	M_A_A1	14,16
SA_MA_2	BG24	M_A_A2	14,16
SA_MA_3	BH24	M_A_A3	14,16
SA_MA_4	BG25	M_A_A4	14,16
SA_MA_5	BA24	M_A_A5	14,16
SA_MA_6	BD24	M_A_A6	14,16
SA_MA_7	BG27	M_A_A7	14,16
SA_MA_8	BF25	M_A_A8	14,16
SA_MA_9	AW24	M_A_A9	14,16
SA_MA_10	BC21	M_A_A10	14,16
SA_MA_11	BG26	M_A_A11	14,16
SA_MA_12	BH26	M_A_A12	14,16
SA_MA_13	BH17	M_A_A13	14,16
SA_MA_14	AY25	M_A_A14	14,16

CANTIGA  
null

15 M\_B\_DQ[63..0]

M_B_DQ0	AK47	SB_DQ_0
M_B_DQ1	AH46	SB_DQ_1
M_B_DQ2	AP47	SB_DQ_2
M_B_DQ3	AP46	SB_DQ_3
M_B_DQ4	AJ46	SB_DQ_4
M_B_DQ5	AJ48	SB_DQ_5
M_B_DQ6	AM48	SB_DQ_6
M_B_DQ7	AP48	SB_DQ_7
M_B_DQ8	AU47	SB_DQ_8
M_B_DQ9	AI46	SB_DQ_9
M_B_DQ10	BA48	SB_DQ_10
M_B_DQ11	AY48	SB_DQ_11
M_B_DQ12	AT47	SB_DQ_12
M_B_DQ13	AR47	SB_DQ_13
M_B_DQ14	BA47	SB_DQ_14
M_B_DQ15	BC47	SB_DQ_15
M_B_DQ16	BC46	SB_DQ_16
M_B_DQ17	BC44	SB_DQ_17
M_B_DQ18	BG43	SB_DQ_18
M_B_DQ19	BF43	SB_DQ_19
M_B_DQ20	BE45	SB_DQ_20
M_B_DQ21	BC41	SB_DQ_21
M_B_DQ22	BE40	SB_DQ_22
M_B_DQ23	BF41	SB_DQ_23
M_B_DQ24	BG38	SB_DQ_24
M_B_DQ25	BF38	SB_DQ_25
M_B_DQ26	BH35	SB_DQ_26
M_B_DQ27	BC38	SB_DQ_27
M_B_DQ28	BH40	SB_DQ_28
M_B_DQ29	BG39	SB_DQ_29
M_B_DQ30	BG34	SB_DQ_30
M_B_DQ31	BH34	SB_DQ_31
M_B_DQ32	BH14	SB_DQ_32
M_B_DQ33	BG12	SB_DQ_33
M_B_DQ34	BH11	SB_DQ_34
M_B_DQ35	BG8	SB_DQ_35
M_B_DQ36	BH12	SB_DQ_36
M_B_DQ37	BF11	SB_DQ_37
M_B_DQ38	BF8	SB_DQ_38
M_B_DQ39	BG7	SB_DQ_39
M_B_DQ40	BC6	SB_DQ_40
M_B_DQ41	BC6	SB_DQ_41
M_B_DQ42	AY3	SB_DQ_42
M_B_DQ43	AY1	SB_DQ_43
M_B_DQ44	BF6	SB_DQ_44
M_B_DQ45	BF5	SB_DQ_45
M_B_DQ46	BA1	SB_DQ_46
M_B_DQ47	BD3	SB_DQ_47
M_B_DQ48	AV2	SB_DQ_48
M_B_DQ49	AU3	SB_DQ_49
M_B_DQ50	AR3	SB_DQ_50
M_B_DQ51	AN2	SB_DQ_51
M_B_DQ52	AY2	SB_DQ_52
M_B_DQ53	AV1	SB_DQ_53
M_B_DQ54	AP3	SB_DQ_54
M_B_DQ55	AR1	SB_DQ_55
M_B_DQ56	AL1	SB_DQ_56
M_B_DQ57	AL2	SB_DQ_57
M_B_DQ58	AJ1	SB_DQ_58
M_B_DQ59	AH1	SB_DQ_59
M_B_DQ60	AM2	SB_DQ_60
M_B_DQ61	AM3	SB_DQ_61
M_B_DQ62	AH3	SB_DQ_62
M_B_DQ63	AJ3	SB_DQ_63

DDR SYSTEM MEMORY B

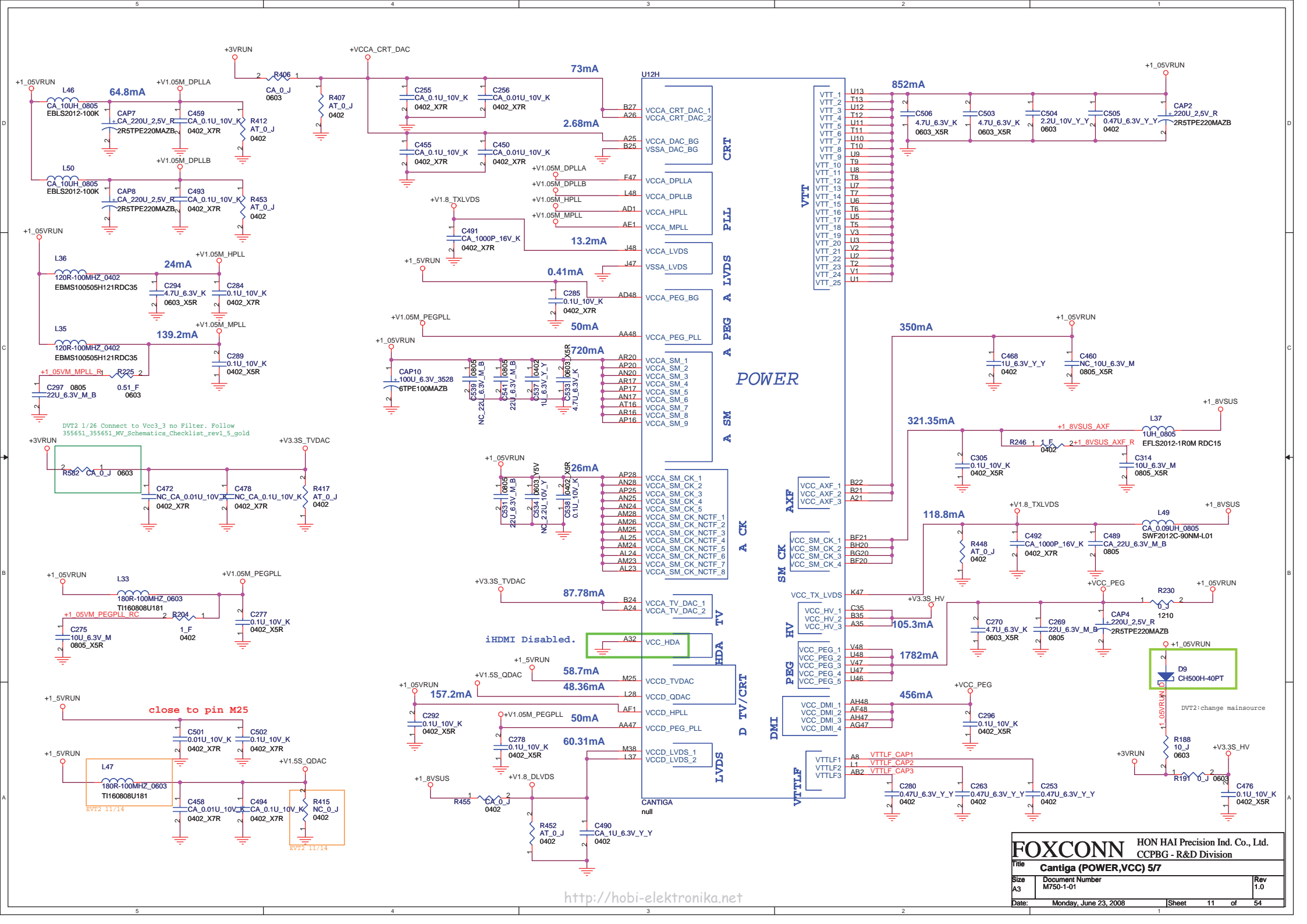
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SB_BS_1	BB17	M_B_BS1	15,16
SB_BS_2	BB33	M_B_BS2	15,16
SB_RAS#	AU17	M_B_RAS#	15,16
SB_CAS#	BG16	M_B_CAS#	15,16
SB_WE#	BF14	M_B_WE#	15,16
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	15
SB_DM_2	BD40	M_B_DM2	15
SB_DM_3	BF35	M_B_DM3	15
SB_DM_4	BG11	M_B_DM4	15
SB_DM_5	BA3	M_B_DM5	15
SB_DM_6	AP1	M_B_DM6	15
SB_DM_7	AK2	M_B_DM7	15
SB_DQS_0	AL47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	15
SB_DQS_2	BG41	M_B_DQS2	15
SB_DQS_3	BG37	M_B_DQS3	15
SB_DQS_4	BH9	M_B_DQS4	15
SB_DQS_5	BB2	M_B_DQS5	15
SB_DQS_6	AU11	M_B_DQS6	15
SB_DQS_7	AN6	M_B_DQS7	15
SB_DQS#_0	AL46	M_B_DQS#0	15
SB_DQS#_1	AV47	M_B_DQS#1	15
SB_DQS#_2	BH41	M_B_DQS#2	15
SB_DQS#_3	BH37	M_B_DQS#3	15
SB_DQS#_4	BC9	M_B_DQS#4	15
SB_DQS#_5	PC2	M_B_DQS#5	15
SB_DQS#_6	AT2	M_B_DQS#6	15
SB_DQS#_7	AN5	M_B_DQS#7	15
SB_MA_0	AV17	M_B_A0	15,16
SB_MA_1	BA25	M_B_A1	15,16
SB_MA_2	BC25	M_B_A2	15,16
SB_MA_3	AU25	M_B_A3	15,16
SB_MA_4	AW25	M_B_A4	15,16
SB_MA_5	BB28	M_B_A5	15,16
SB_MA_6	AU28	M_B_A6	15,16
SB_MA_7	AW28	M_B_A7	15,16
SB_MA_8	AT33	M_B_A8	15,16
SB_MA_9	BD33	M_B_A9	15,16
SB_MA_10	BB16	M_B_A10	15,16
SB_MA_11	AW33	M_B_A11	15,16
SB_MA_12	AY33	M_B_A12	15,16
SB_MA_13	BH15	M_B_A13	15,16
SB_MA_14	AU33	M_B_A14	15,16

CANTIGA  
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**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **Cantiga (DDRII) 47**

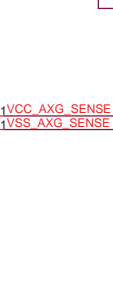
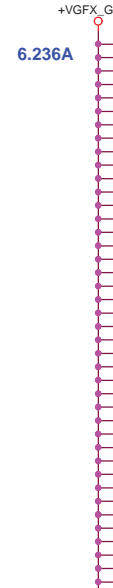
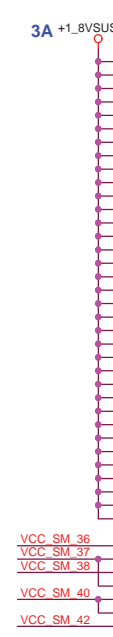
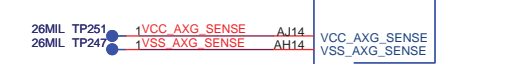
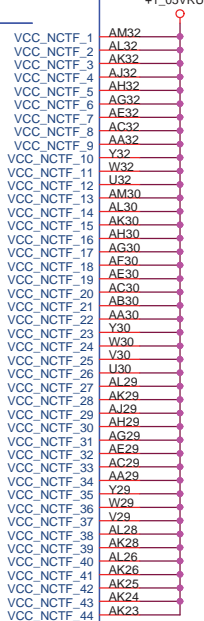
Size: A3	Document Number: M750-1-01	Rev: 1.0
Date: Monday, June 23, 2008	Sheet: 10	of: 54





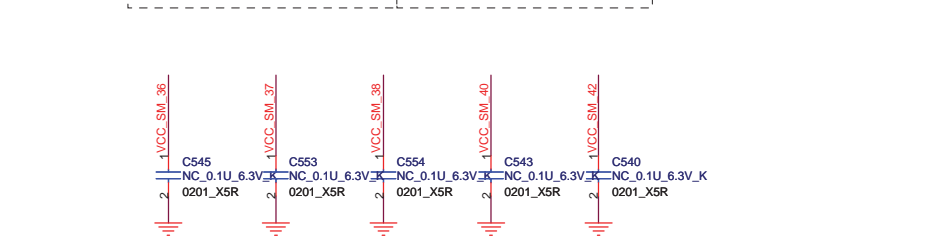
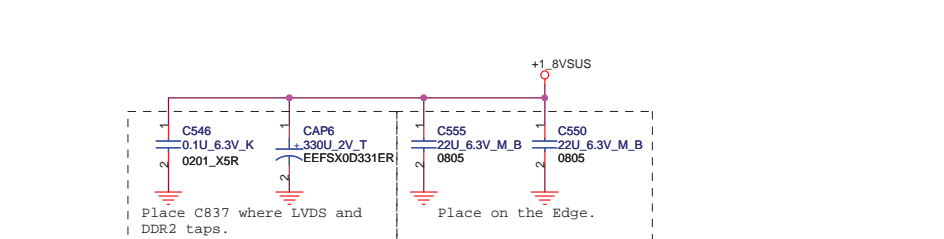
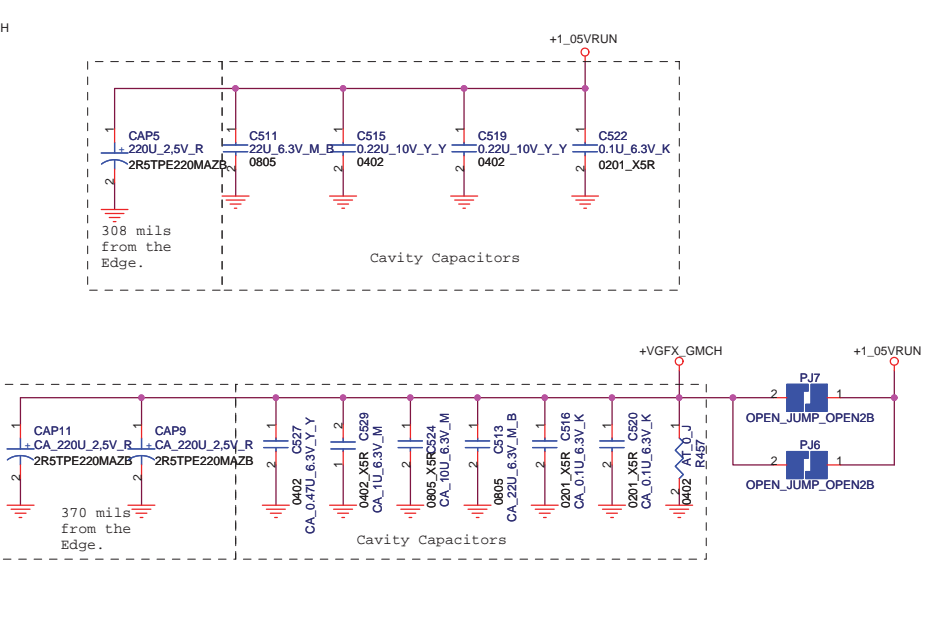
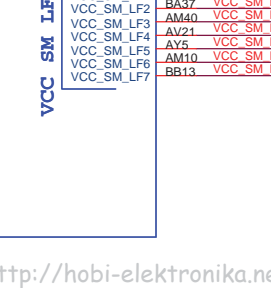
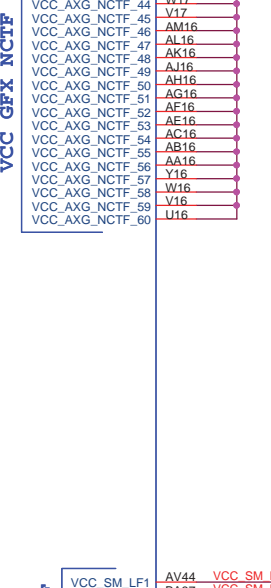
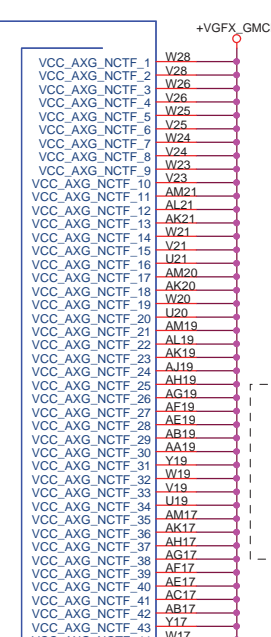
VCC CORE  
POWER

VCC NCTF



VCC SM  
POWER

VCC GFX NCTF  
VCC GFX



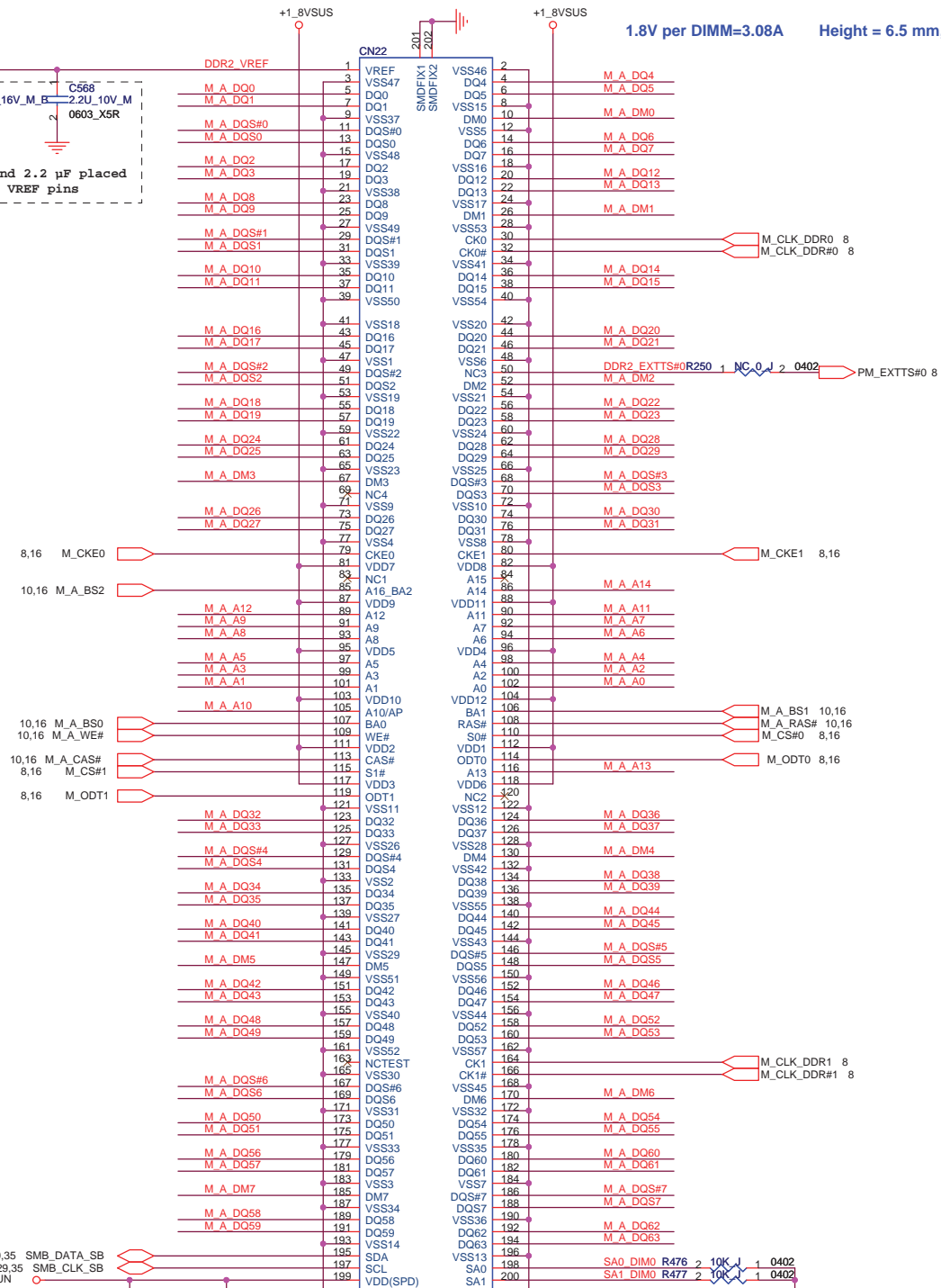
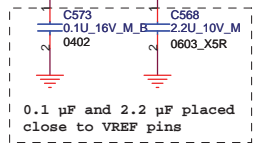
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **Cantiga (VCC CORE) 6/7**

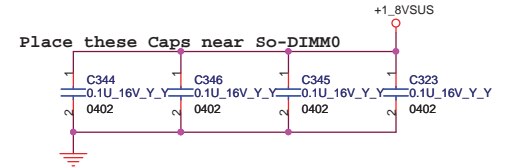
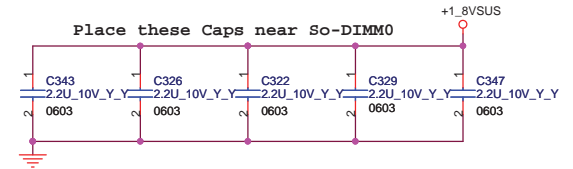
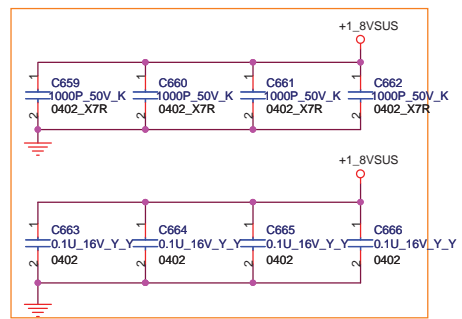
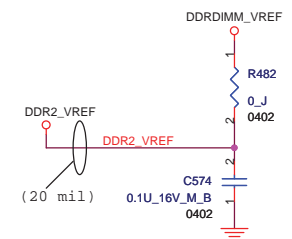
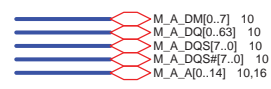
Size: A3	Document Number: M750-1-01	Rev: 1.0
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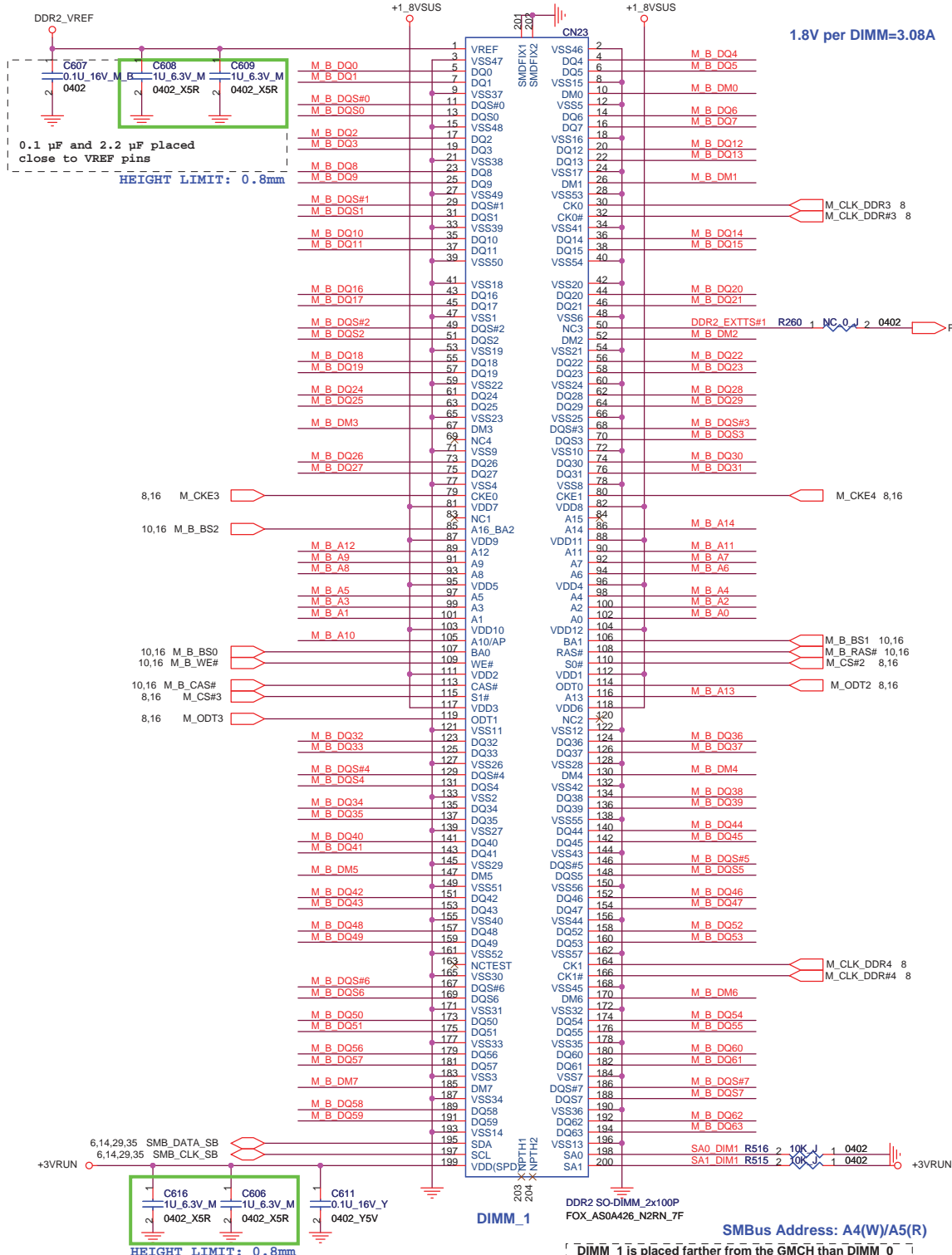


1.8V per DIMM=3.08A Height = 6.5 mm, Standard Type

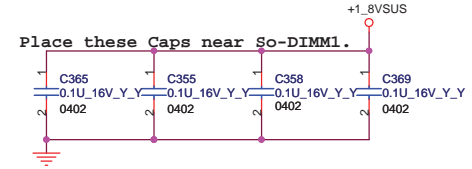
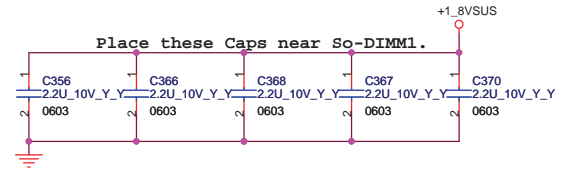
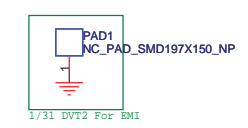
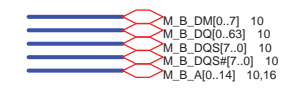


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>DDR(I)SO-DIMM_0</b>		CCPBG - R&D Division	
Size A3	Document Number M750-1-01	Rev 1.0	
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SMBus Address: A0H(W)/A1H(R)  
Place DIMM\_0 near GMCH



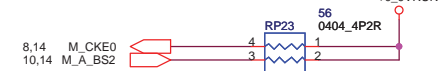
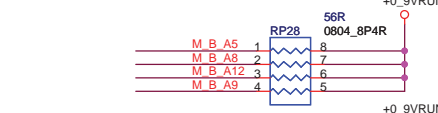
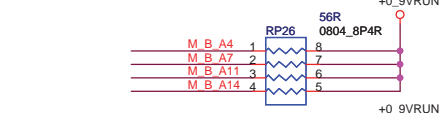
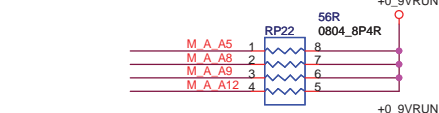
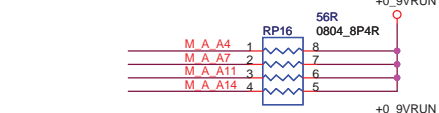
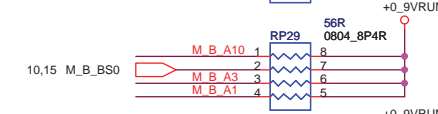
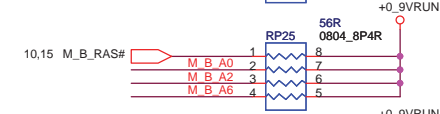
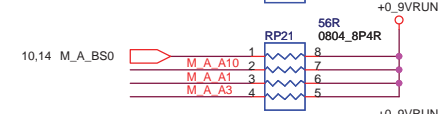
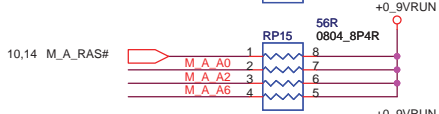
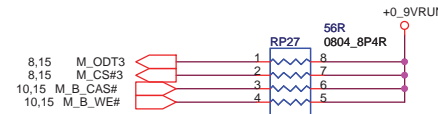
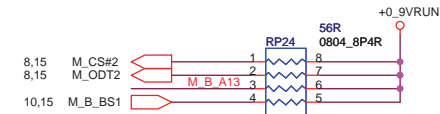
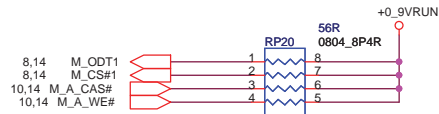
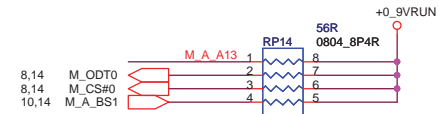
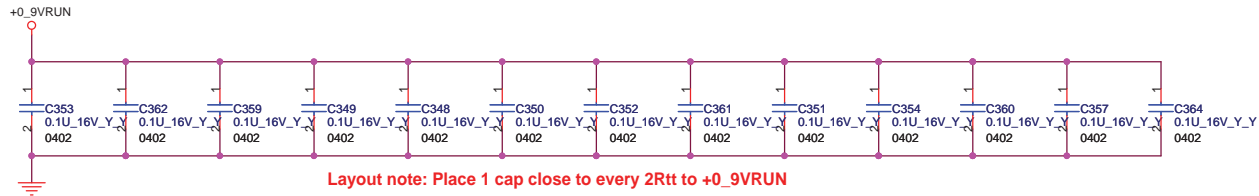
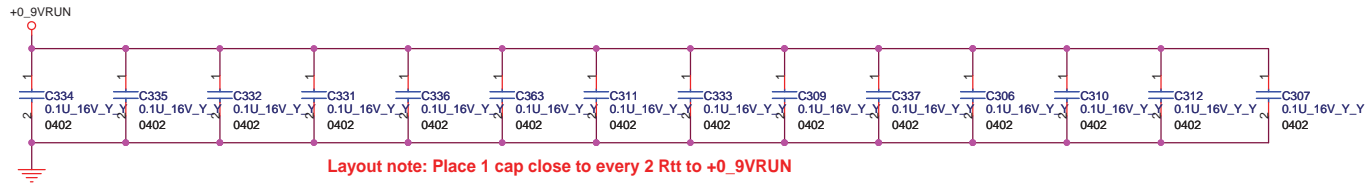
1.8V per DIMM=3.08A Height = 5.2mm, Reversed Type

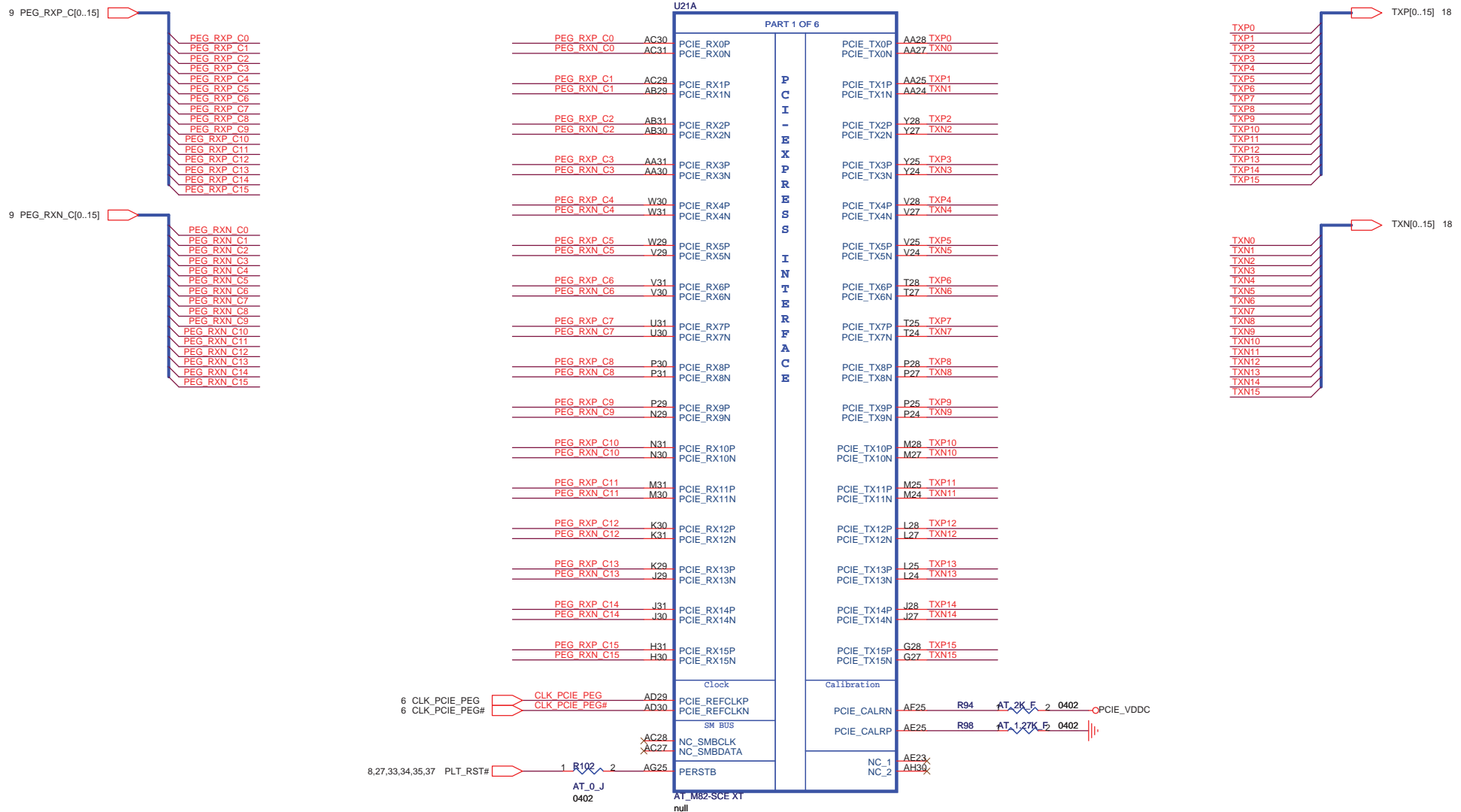


DDR2 SO-DIMM\_2x100P  
FOX\_AS0A426\_N2RN\_7F  
SMBus Address: A4(W)/A5(R)  
DIMM\_1 is placed farther from the GMCH than DIMM\_0

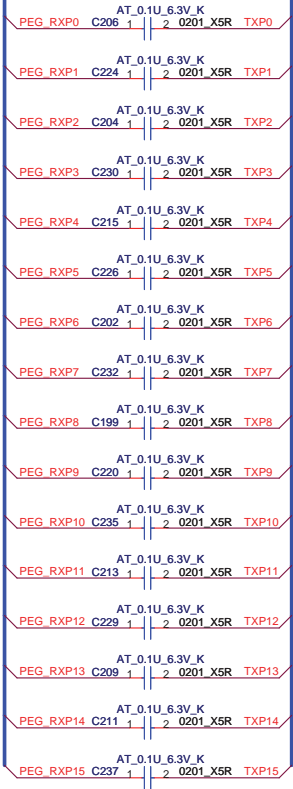
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.	
Title <b>DDR(I)SO-DIMM_1</b>	
Size A3	Document Number M750-1-01
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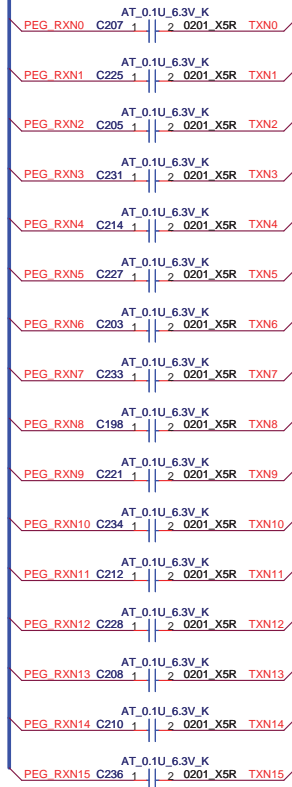




9 PEG\_RXP[0..15] TXP[0..15] 17

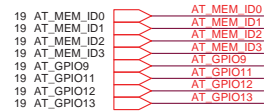
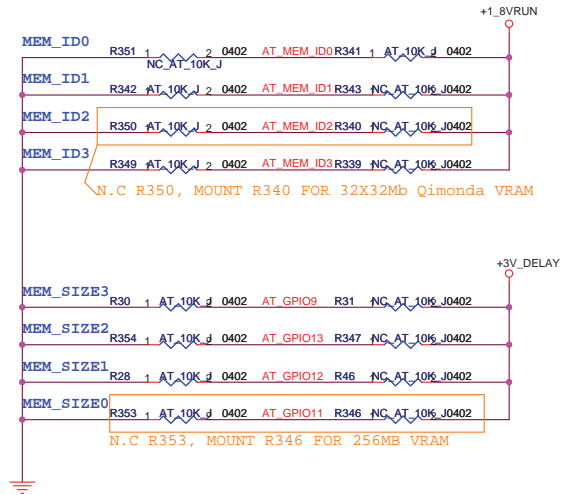


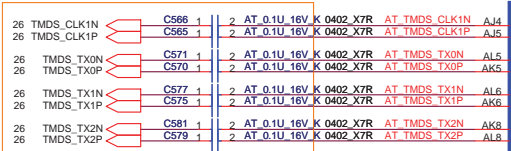
9 PEG\_RXN[0..15] TXN[0..15] 17



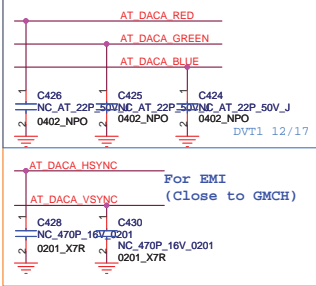
Strap for GDDR3-136ball  
ATL\_DVPDATA[23 : 20 ]  
  
0001 16Mx32 Qimonda  
0010 16Mx32 Hynix  
0011 16Mx32 Samsung  
0101 32Mx32 Qimonda  
0110 32Mx32 Hynix  
0111 32Mx32 Samsung

If no ROM attached, GPIO[9:13:12:11]  
CONFIG(3:0)  
controls the memory aperture size.  
128MB X000  
256MB X001  
64MB X010  
32MB X011  
512MB X100  
1GB X101  
2GB X110  
4GB X111

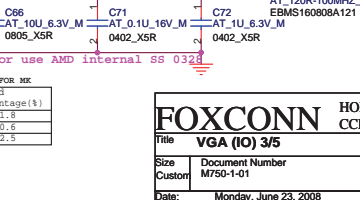
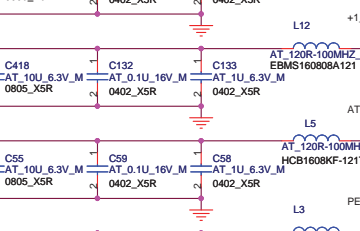
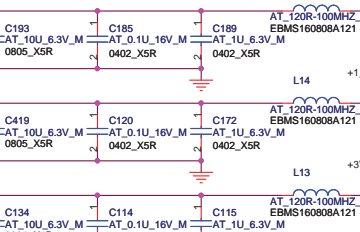
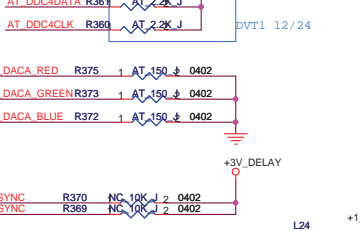
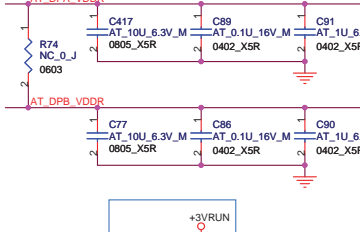
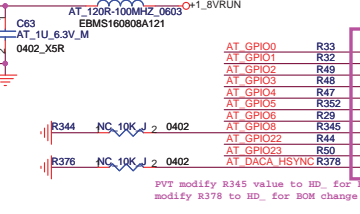
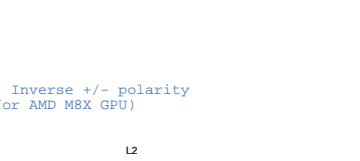
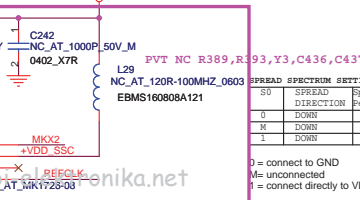
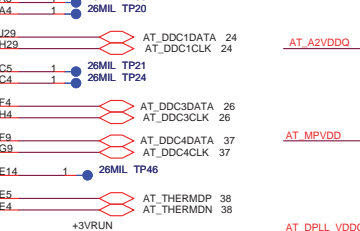
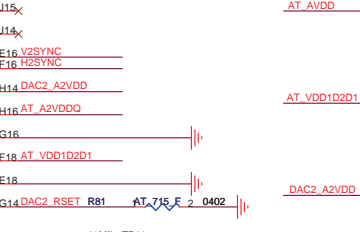
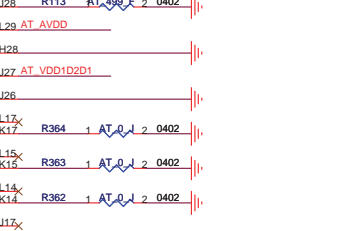
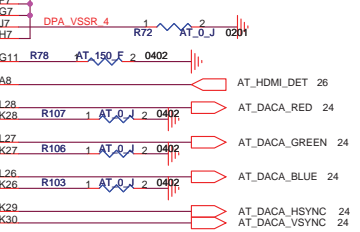
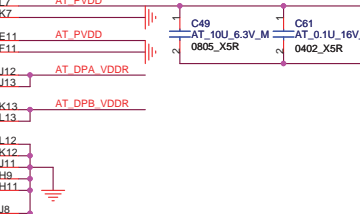
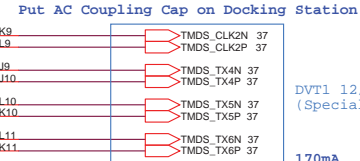
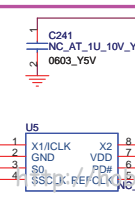
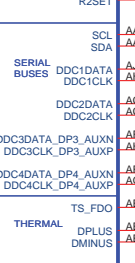
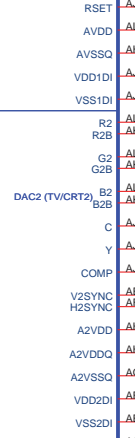
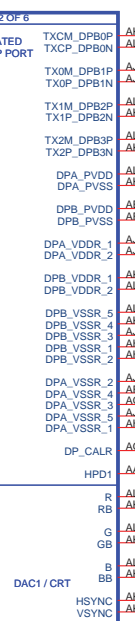
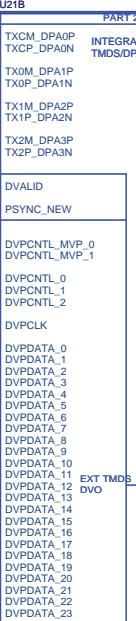
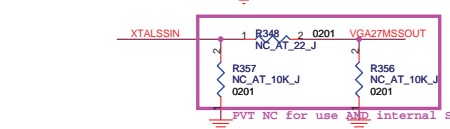
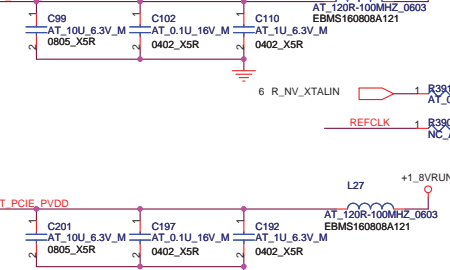
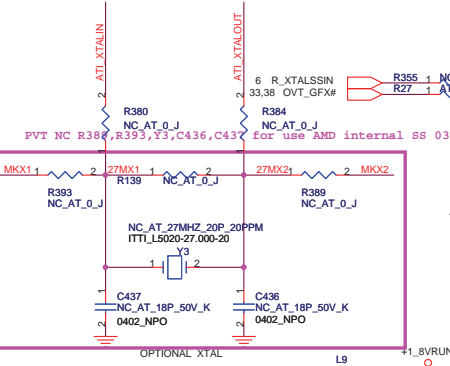
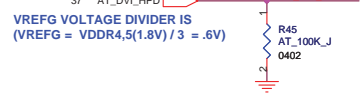




BVT2 11/03 Inverse +/- polarity (Special for AMD M8X GPU)



VGA\_DIS PSYNC\_NEW (M82-S) VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).  
 0: VGA Controller capacity enabled  
 1: The device will not be recognized



SPREAD SPECTRUM SETTING FOR MK

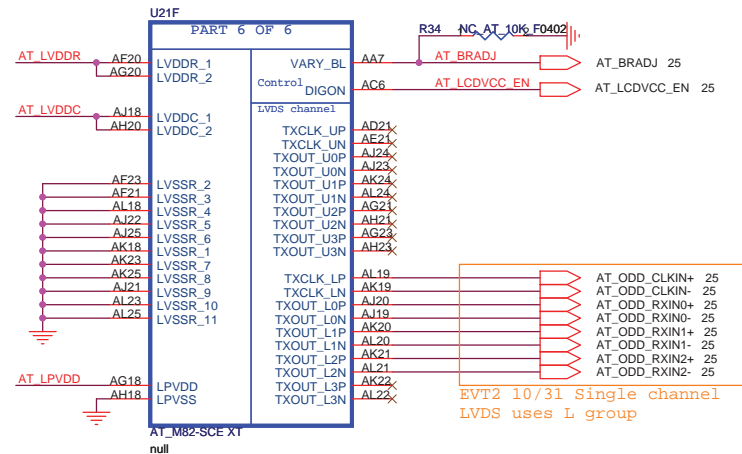
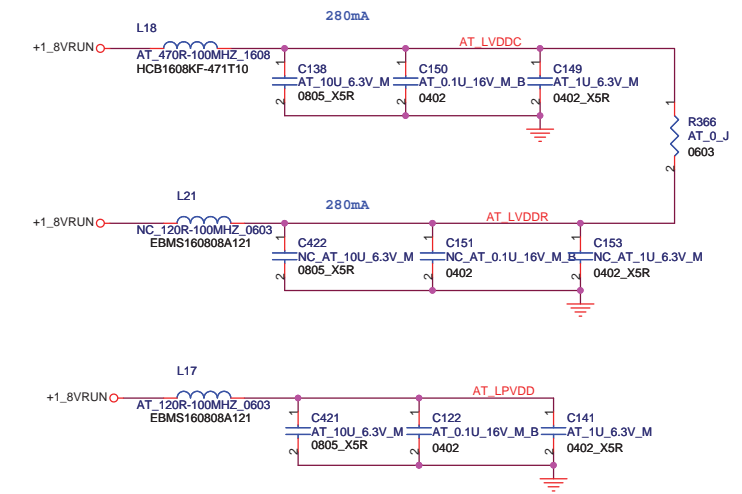
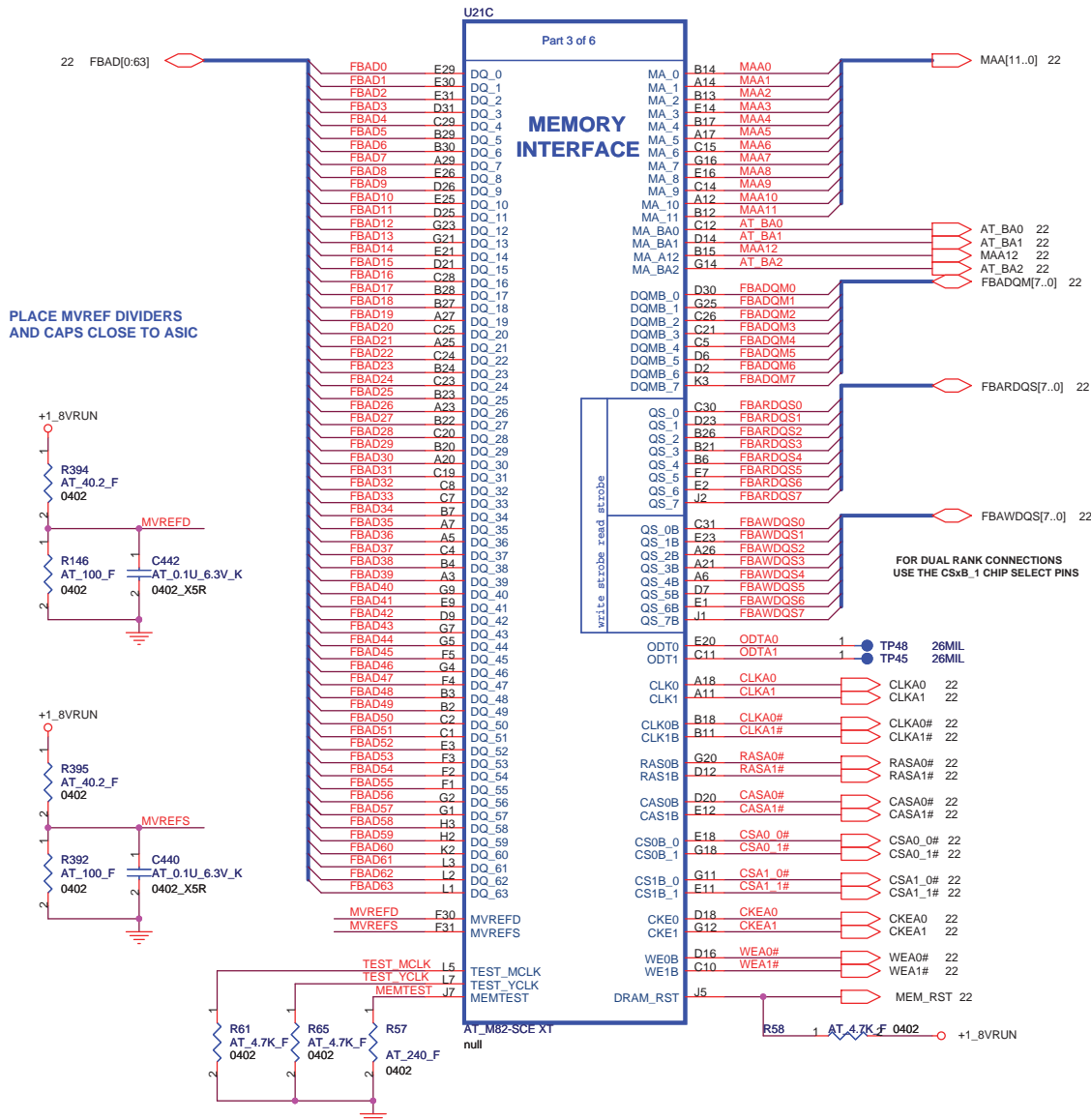
SPREAD DIRECTION	Spread Percentage(%)
0 DOWN	-1.8
1 DOWN	-0.6
2 DOWN	-2.5

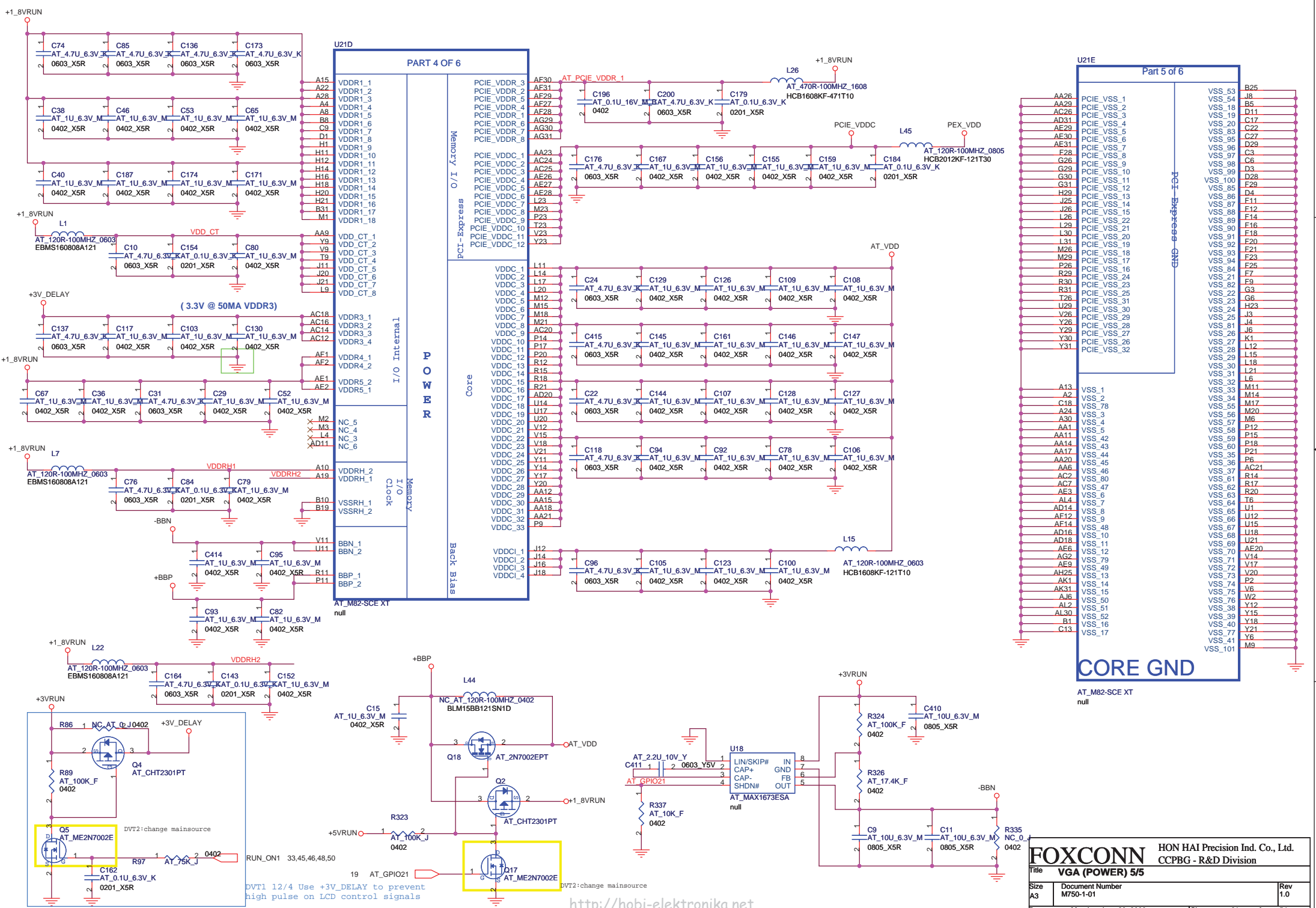
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **VGA (IO) 3/5**

Size: Custom Document Number: M750-1-01 Rev: 1.0

Date: Monday, June 23, 2008 Sheet: 19 of 54



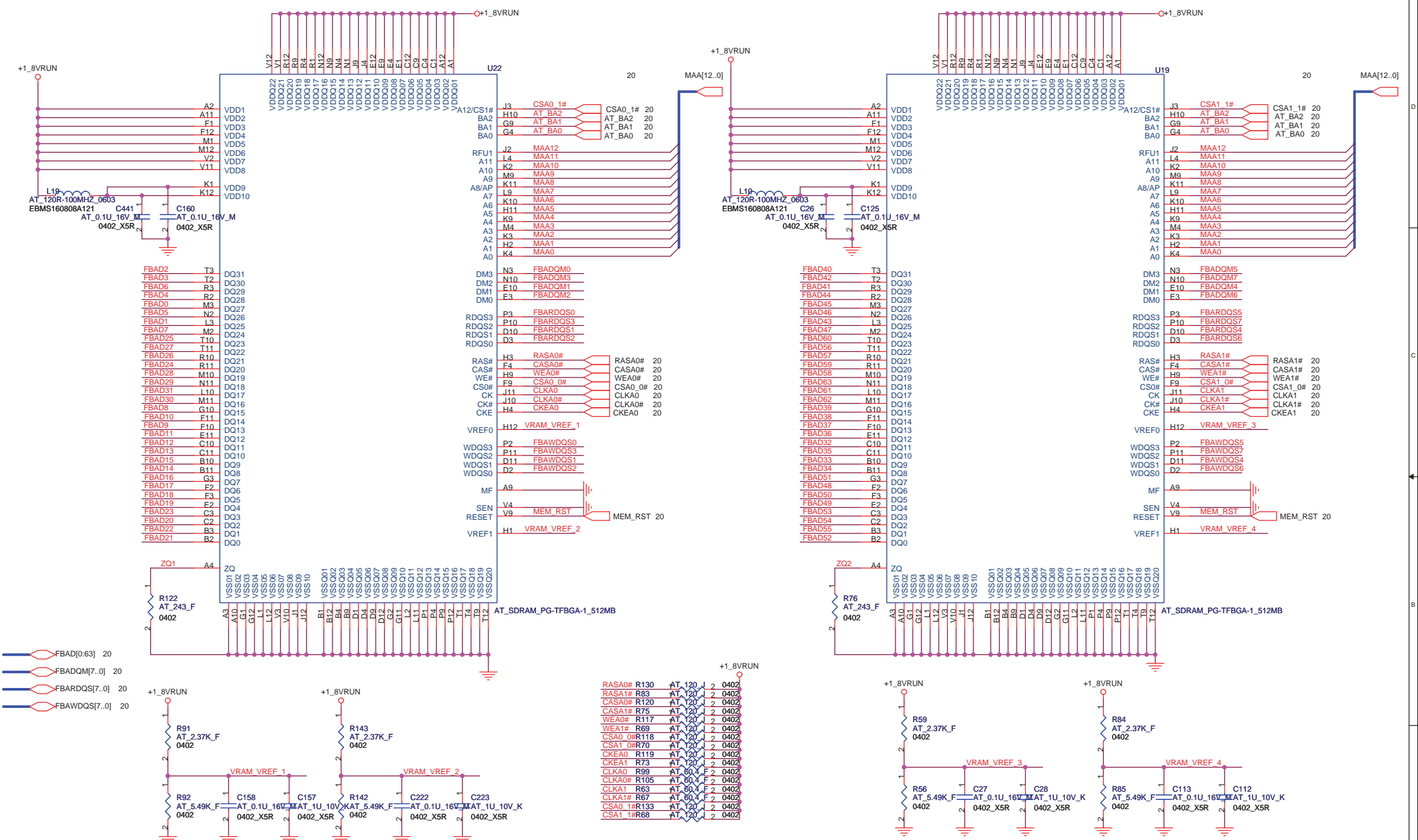


**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

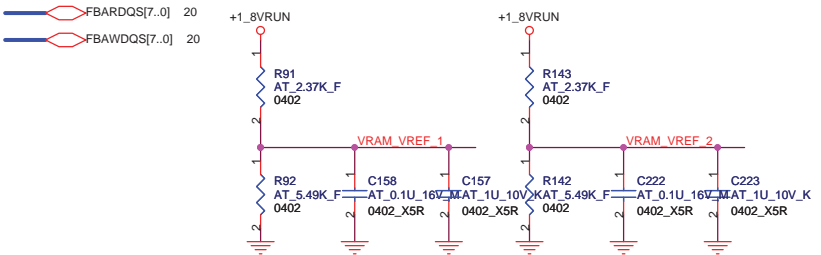
Title: **VGA (POWER) 5/5**

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Date: Monday, June 23, 2008	Sheet 21	of 54



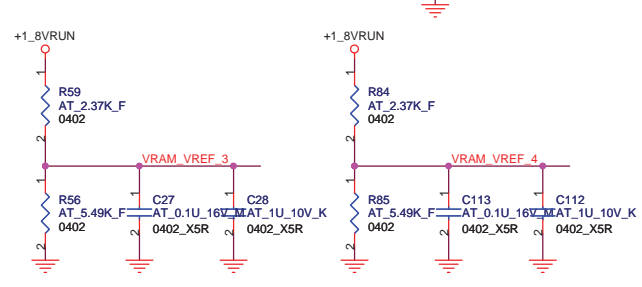


- FBAD[0:63] 20
- FBARDQM[7..0] 20
- FBARDQS[7..0] 20
- FBAWDQS[7..0] 20



VRAM\_VREF is 70%VDDQ for GDDR3

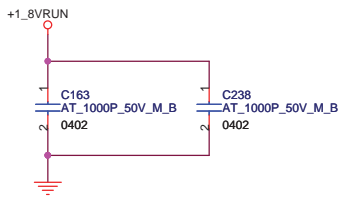
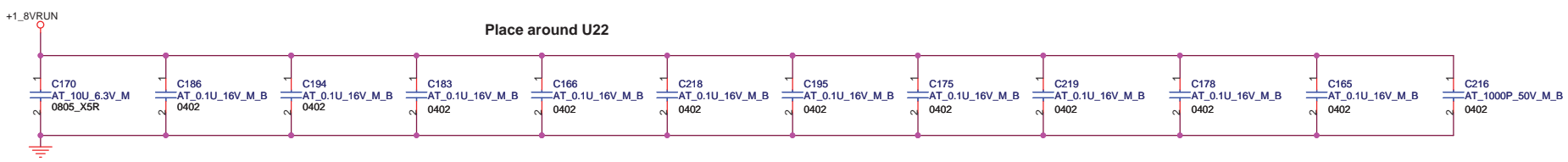
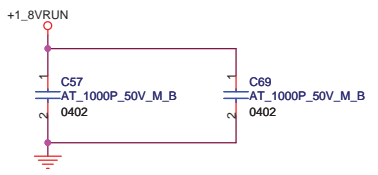
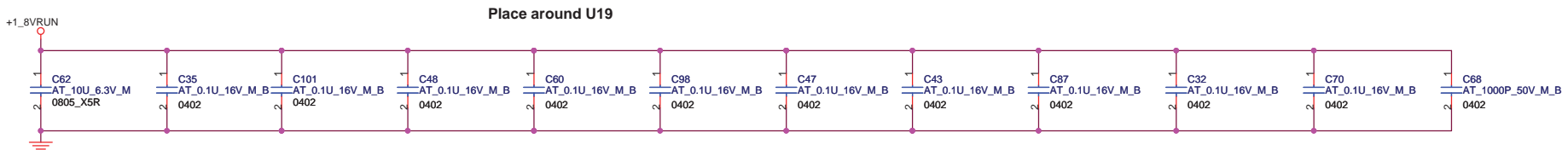
- RASA0# R130 AT\_120 2 0402
- RASA1# R83 AT\_120 2 0402
- CASA0# R120 AT\_120 2 0402
- CASA1# R75 AT\_120 2 0402
- WEA0# R117 AT\_120 2 0402
- WEA1# R63 AT\_120 2 0402
- CSA0\_0#R118 AT\_120 2 0402
- CSA1\_0#R70 AT\_120 2 0402
- CKEA0 R119 AT\_120 2 0402
- CKEA1 R73 AT\_120 2 0402
- CLKA0 R99 AT\_60 4 F 0402
- CLKA0# R105 AT\_60 4 F 0402
- CLKA1# R63 AT\_60 4 F 0402
- CLKA1# R67 AT\_60 4 F 0402
- CSA0\_1#R133 AT\_120 2 0402
- CSA1\_1#R68 AT\_120 2 0402

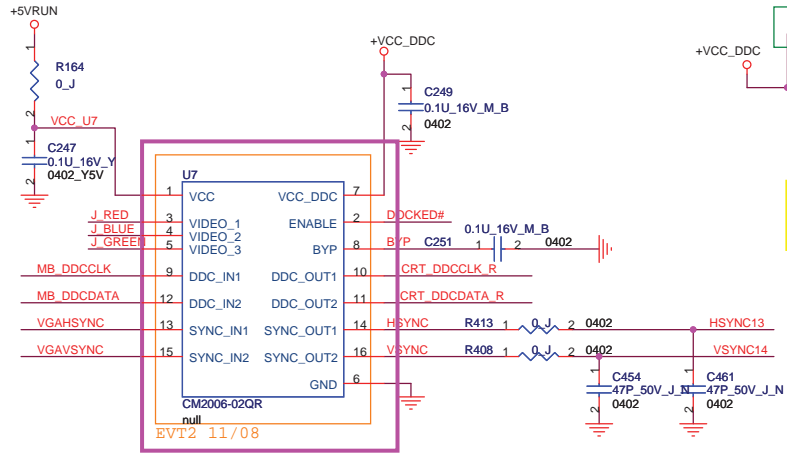
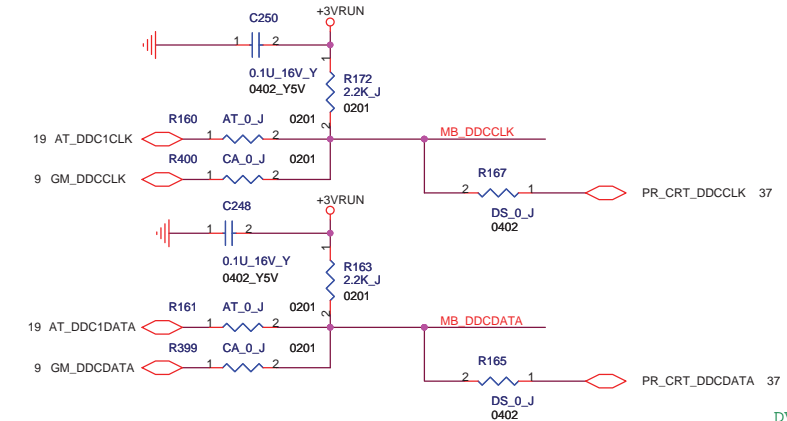
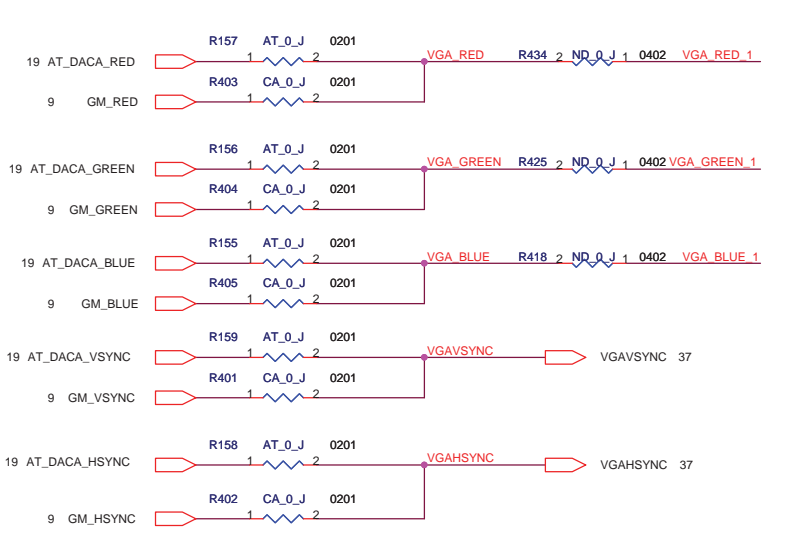


VRAM\_VREF is 70%VDDQ for GDDR3

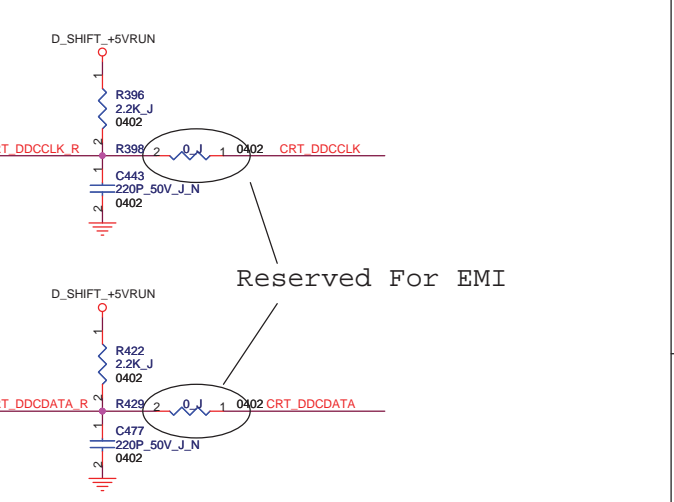
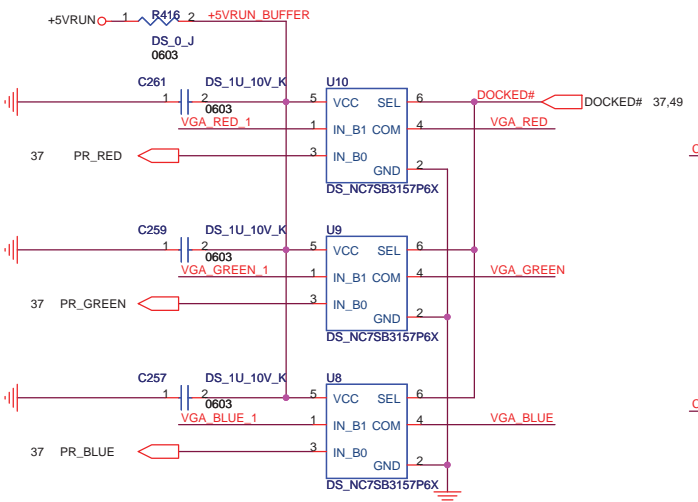
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>VRAM (GDDR3) 1/2</b>			
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 22	of 54	



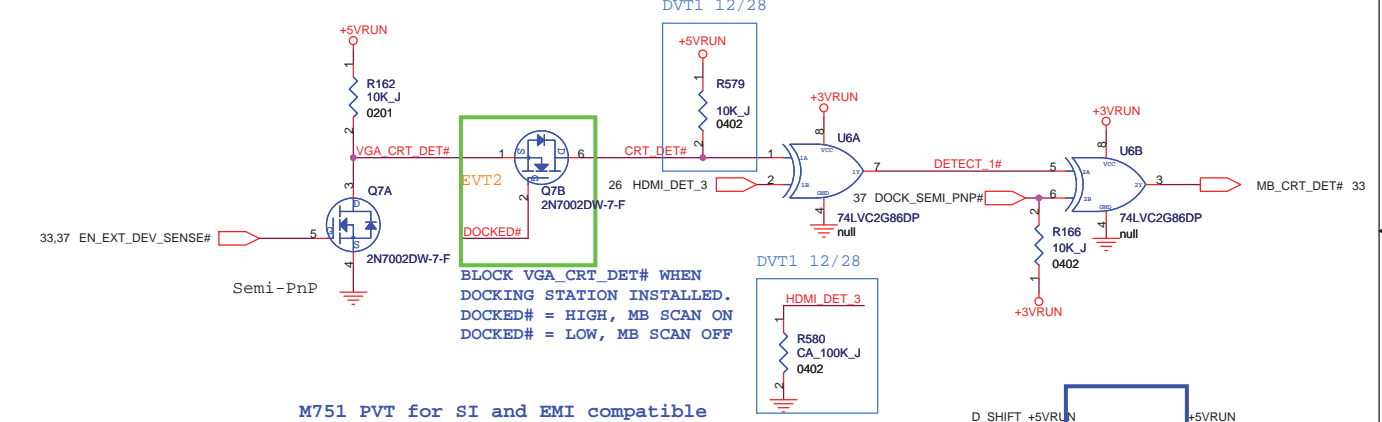




PVT update symbol to CM2006-02QR

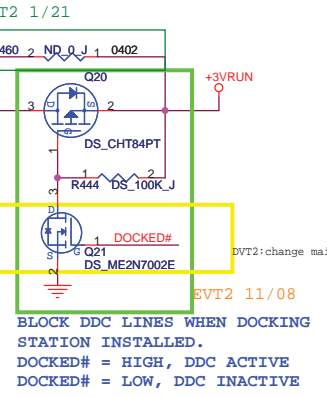


Reserved For EMI

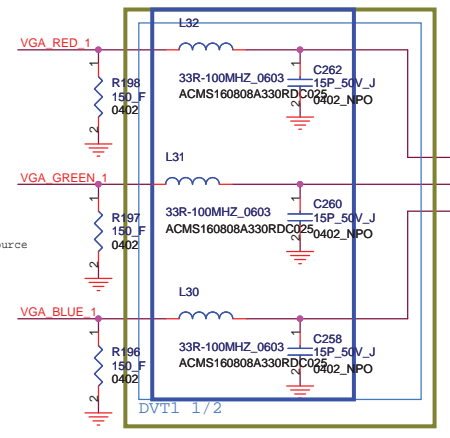


BLOCK VGA\_CRT\_DET# WHEN DOCKING STATION INSTALLED. DOCKED# = HIGH, MB SCAN ON DOCKED# = LOW, MB SCAN OFF

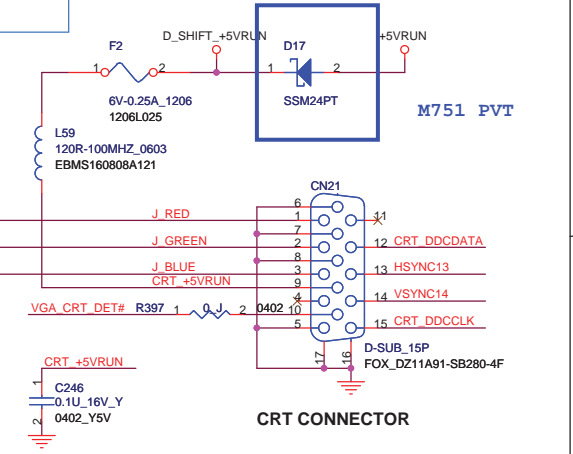
M751 PVT for SI and EMI compatible



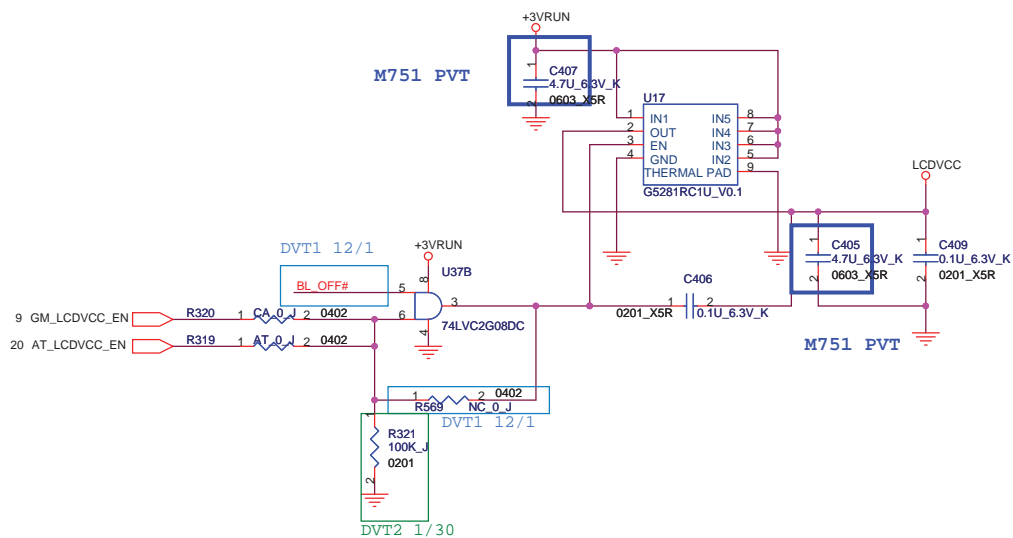
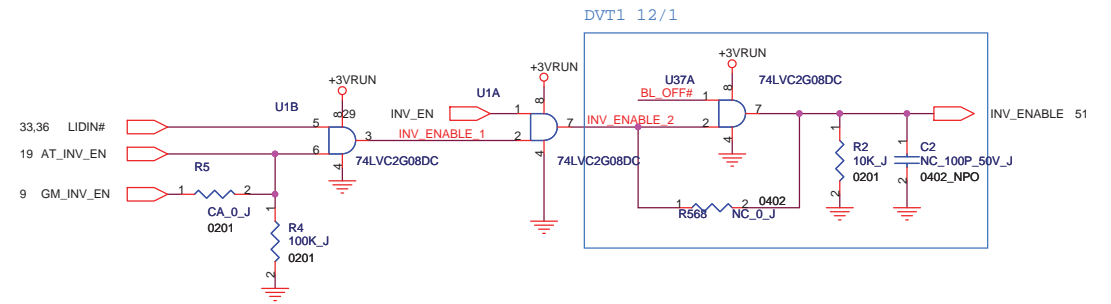
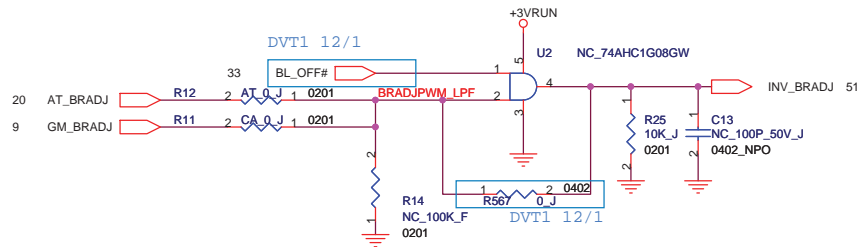
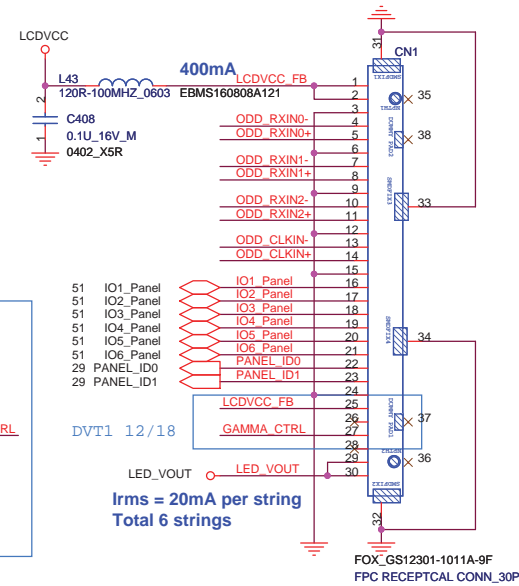
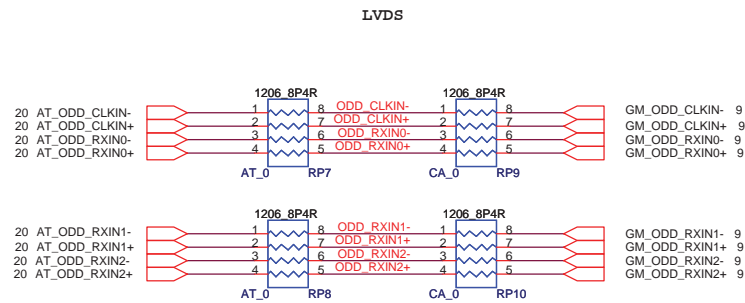
BLOCK DDC LINES WHEN DOCKING STATION INSTALLED. DOCKED# = HIGH, DDC ACTIVE DOCKED# = LOW, DDC INACTIVE



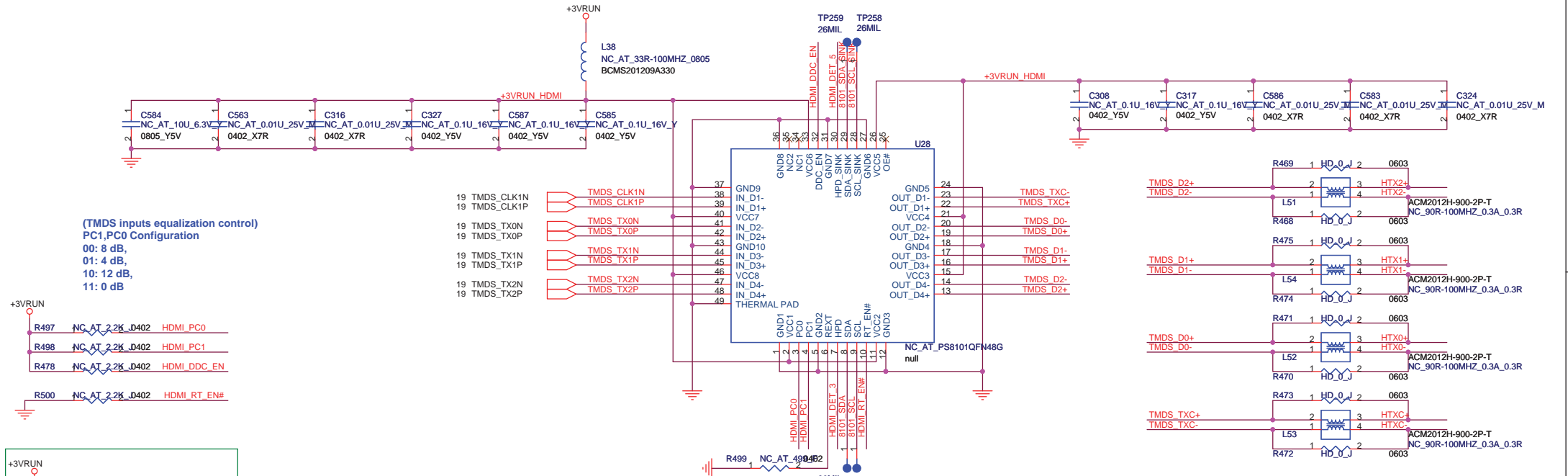
M751 DVT changed for EMI



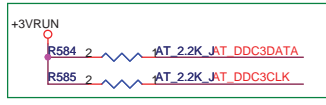
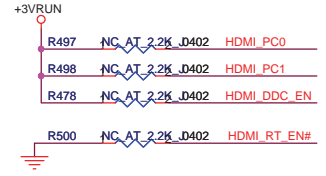
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>CRT</b>		
Size A3	Document Number M750-1-01	Rev 1.0
Date: Thursday, June 26, 2008	Sheet 24	of 54



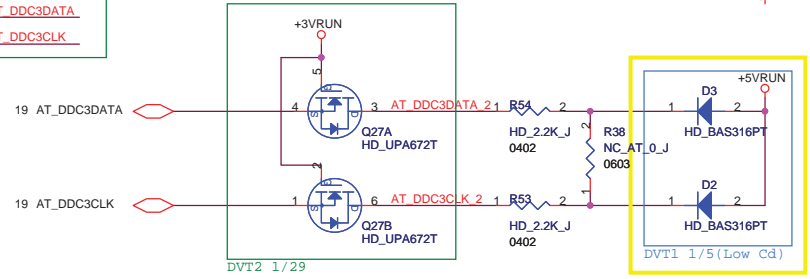
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: <b>LVDS</b>			
Size: A3	Document Number: M750-1-01		Rev: 1.0
Date: Monday, June 23, 2008	Sheet: 25	of 54	



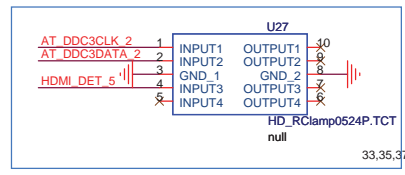
**(TMDS inputs equalization control)  
PC1,PC0 Configuration**  
00: 8 dB,  
01: 4 dB,  
10: 12 dB,  
11: 0 dB



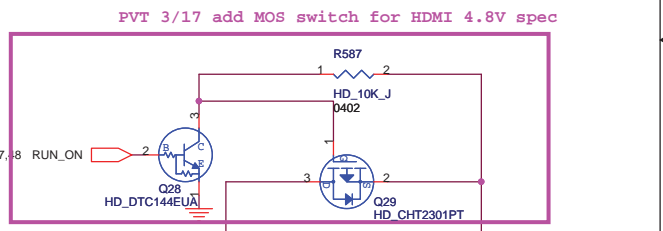
DVT2 1/2/29



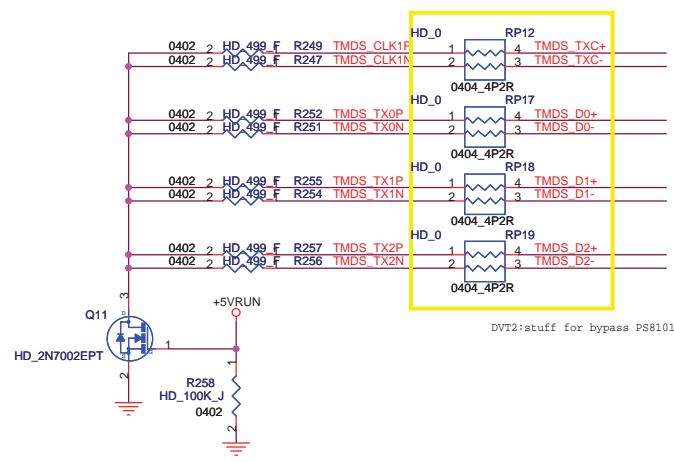
DVT2:change mainsource for common parts



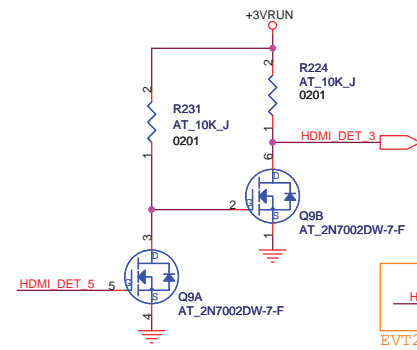
DVT1 12/27



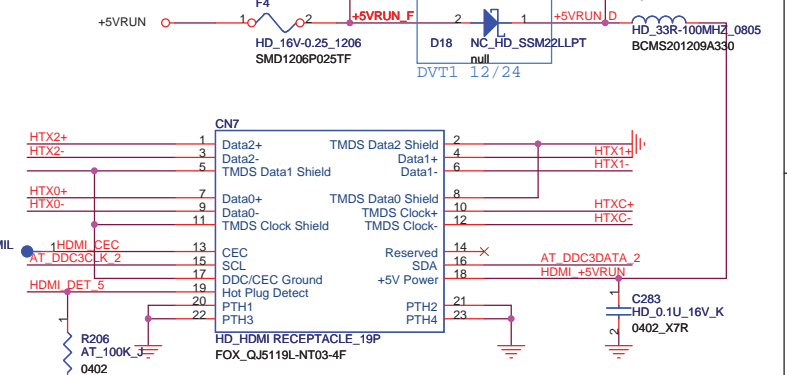
Data line capacitance to GND need less than 10pF, so these parts need close to HDMI connector



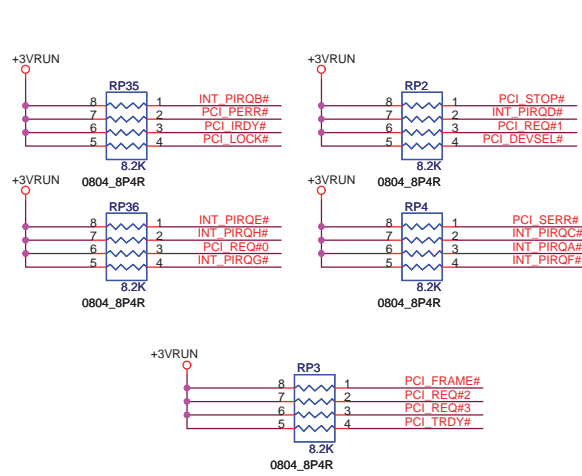
DVT2:stuff for bypass PS8101



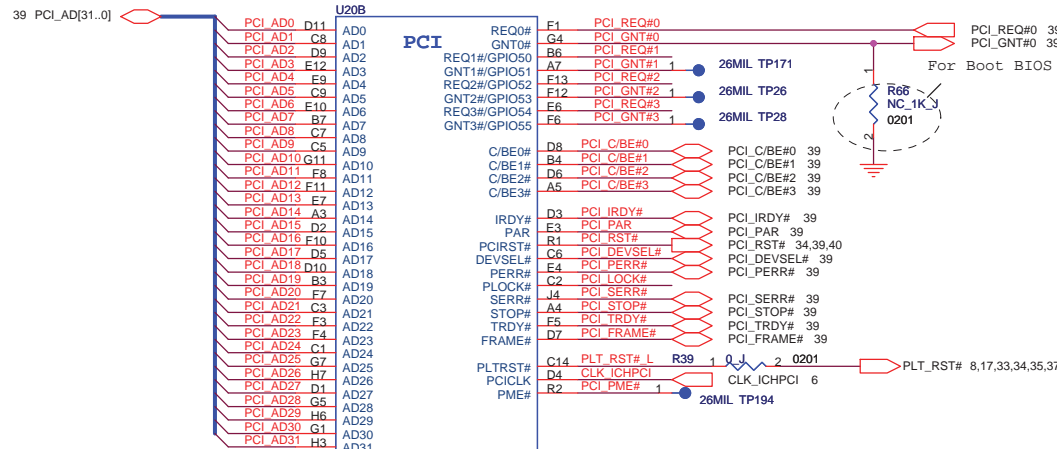
DVT2



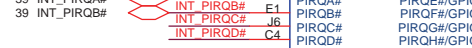
<b>FOXCONN</b>			HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI			Rev
Size	Document Number			1.0
A3	M750-1-01			
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PCI Pullups

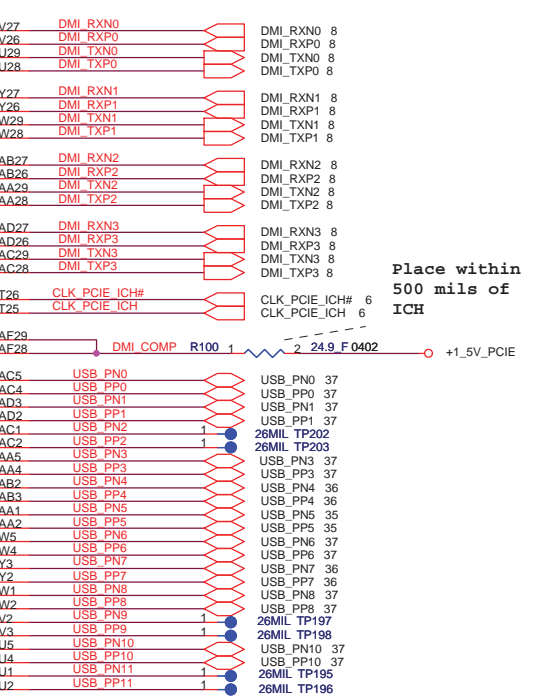
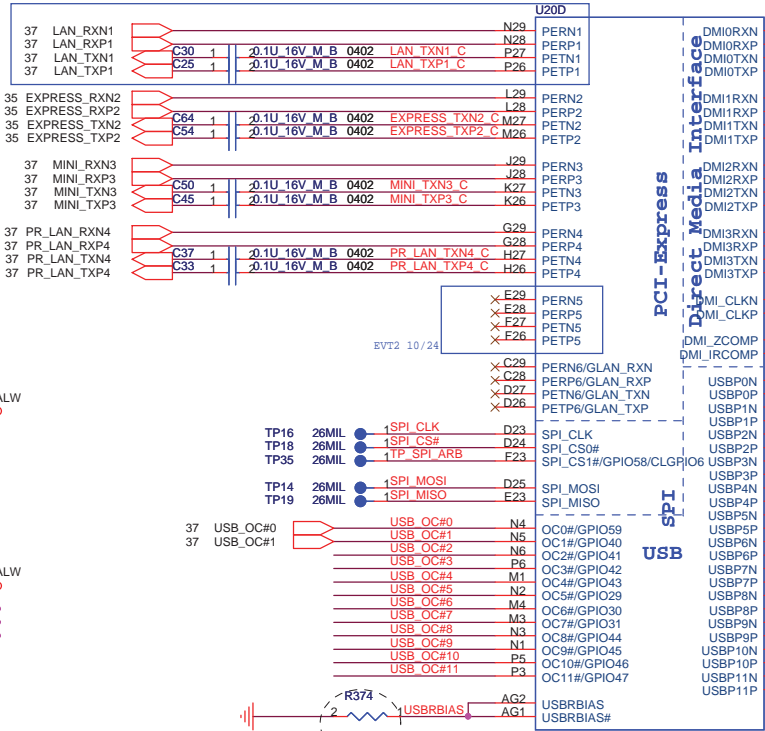


Interrupt I/F



**Strap for Boot-BIOS**

	GNT#	SPI_CS#
I/PC (Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI



USB PORT	Function
PORT-0	SIDE-1
PORT-1	SIDE-2
PORT-2	x
PORT-3	Docking Hub
PORT-4	Bluetooth
PORT-5	ExpressCard
PORT-6	FingerPrint
PORT-7	Camera
PORT-8	Felica
PORT-9	x
PORT-10	Wimax
PORT-11	x

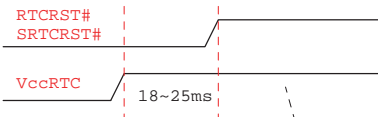
Place within 500 mils of ICH and don't route next to high speed signals

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **ICH9-M (PCI/DMI/USB/PCIE) 1/5**

Size A3 Document Number M750-1-01 Rev 1.0

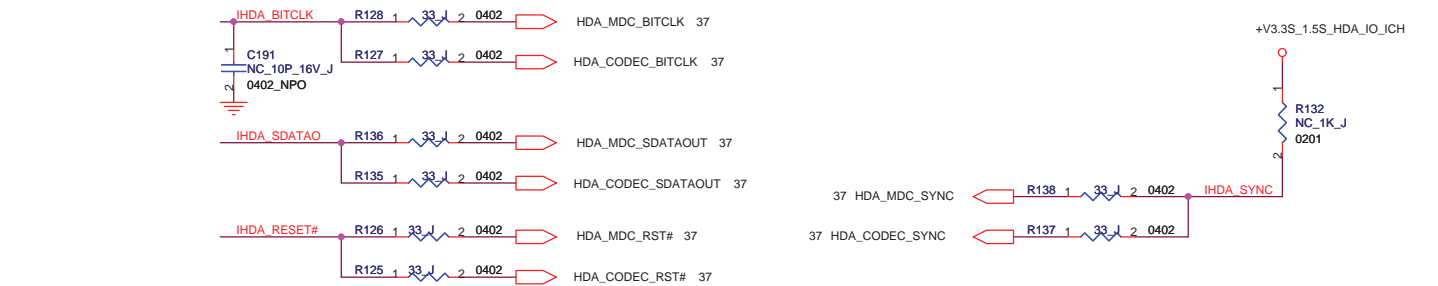
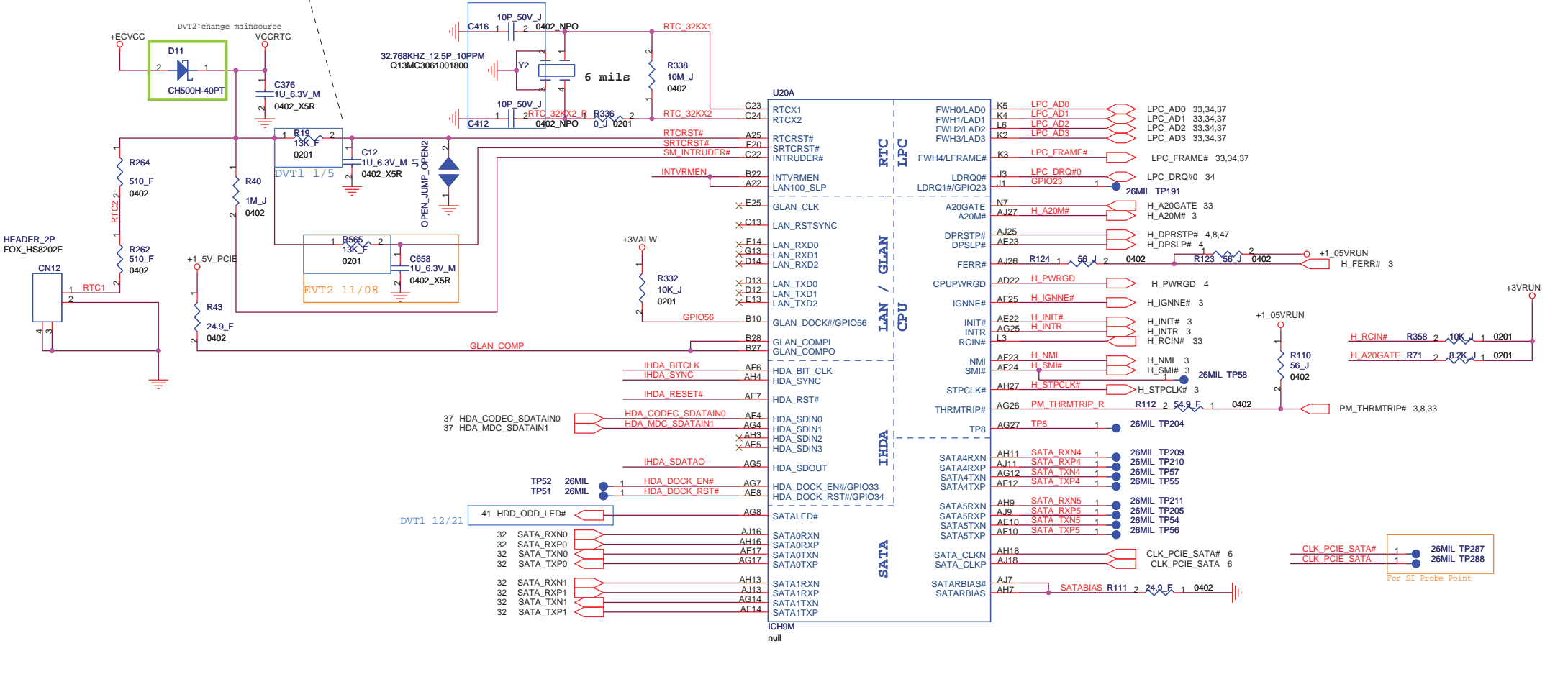
Date: Monday, June 23, 2008 Sheet 27 of 54



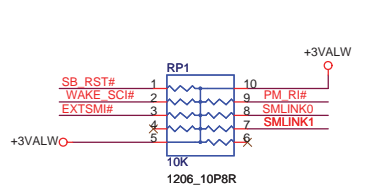
Internal VRM enabled for VccSus1_05, VccSus1_5, VccC1_5, VccLAN1_05 and VccC1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)



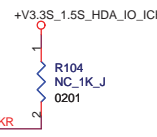
The traces inside this block should be wider.  
DVT1 12/23



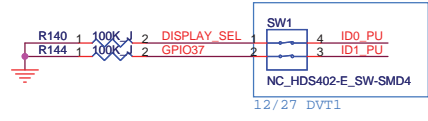
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title <b>ICH9-M (LPC,IDE,SATA) 2/5</b>	
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Stuff for No-reboot  
Low=Default  
High=No-reboot



SYSTEM ID0-3

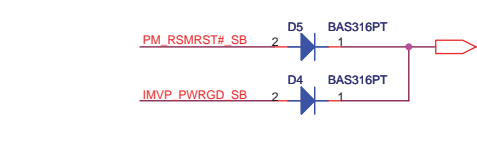
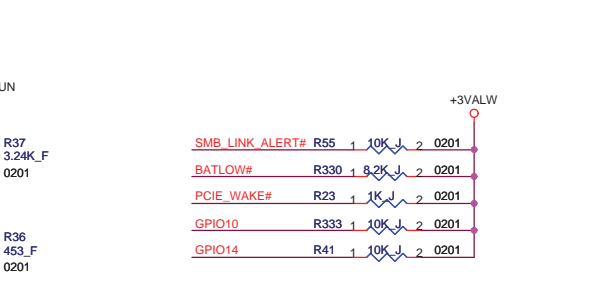
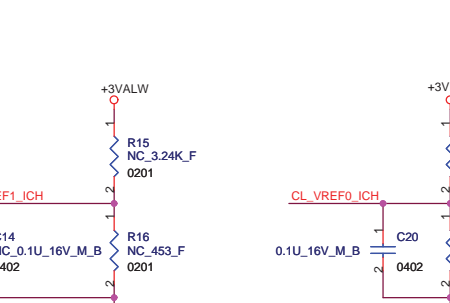
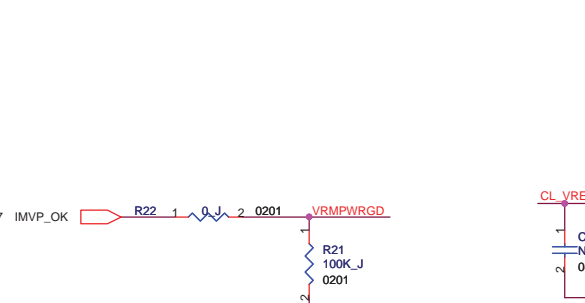
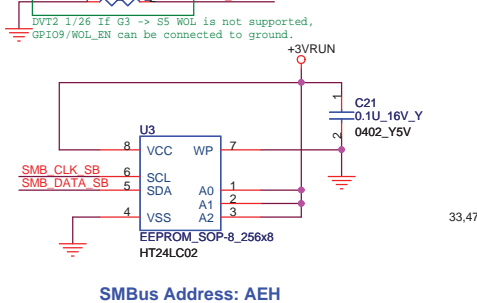
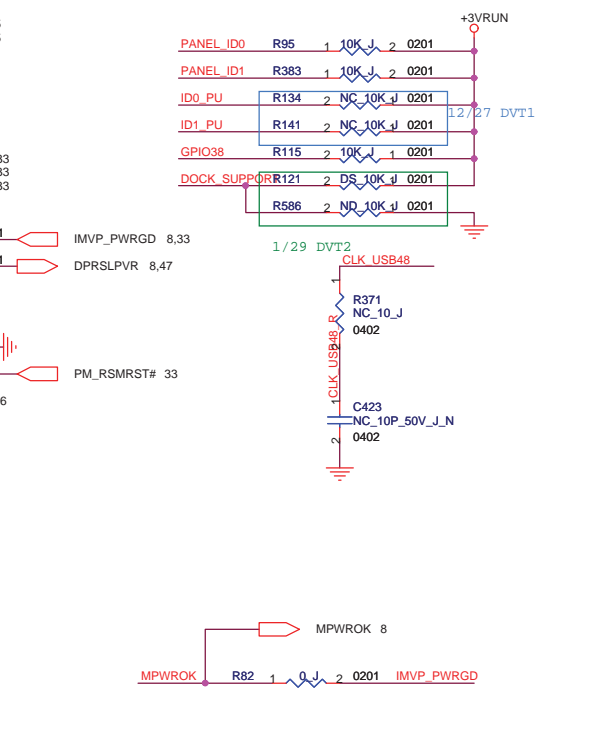
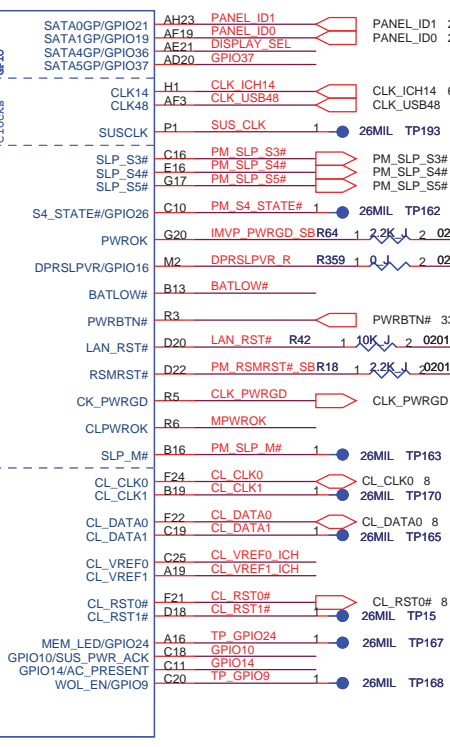
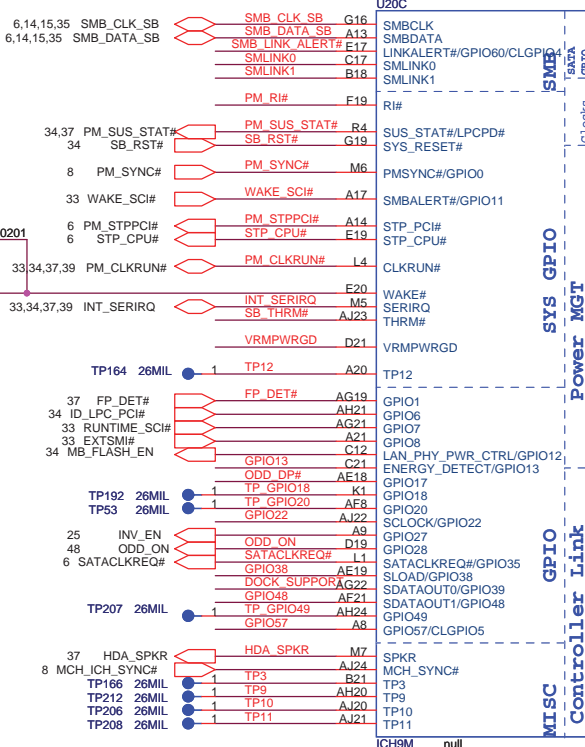
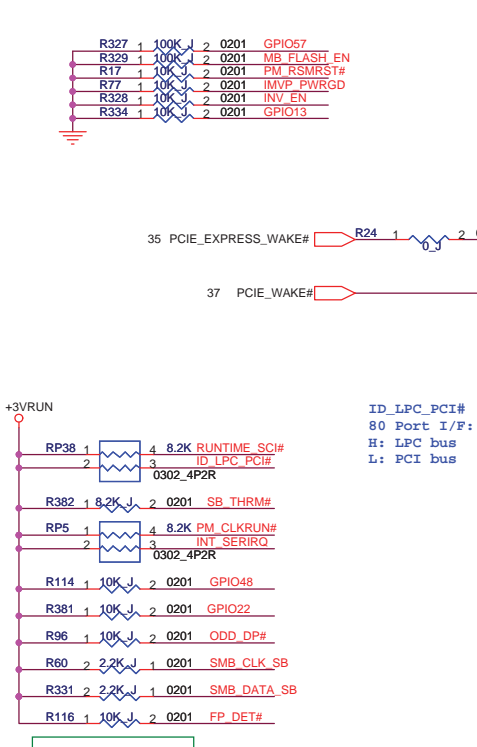
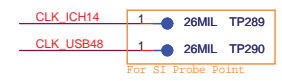


SW1: DISPLAY OUTOUT SELECTION  
(FOR DEBUG ONLY)

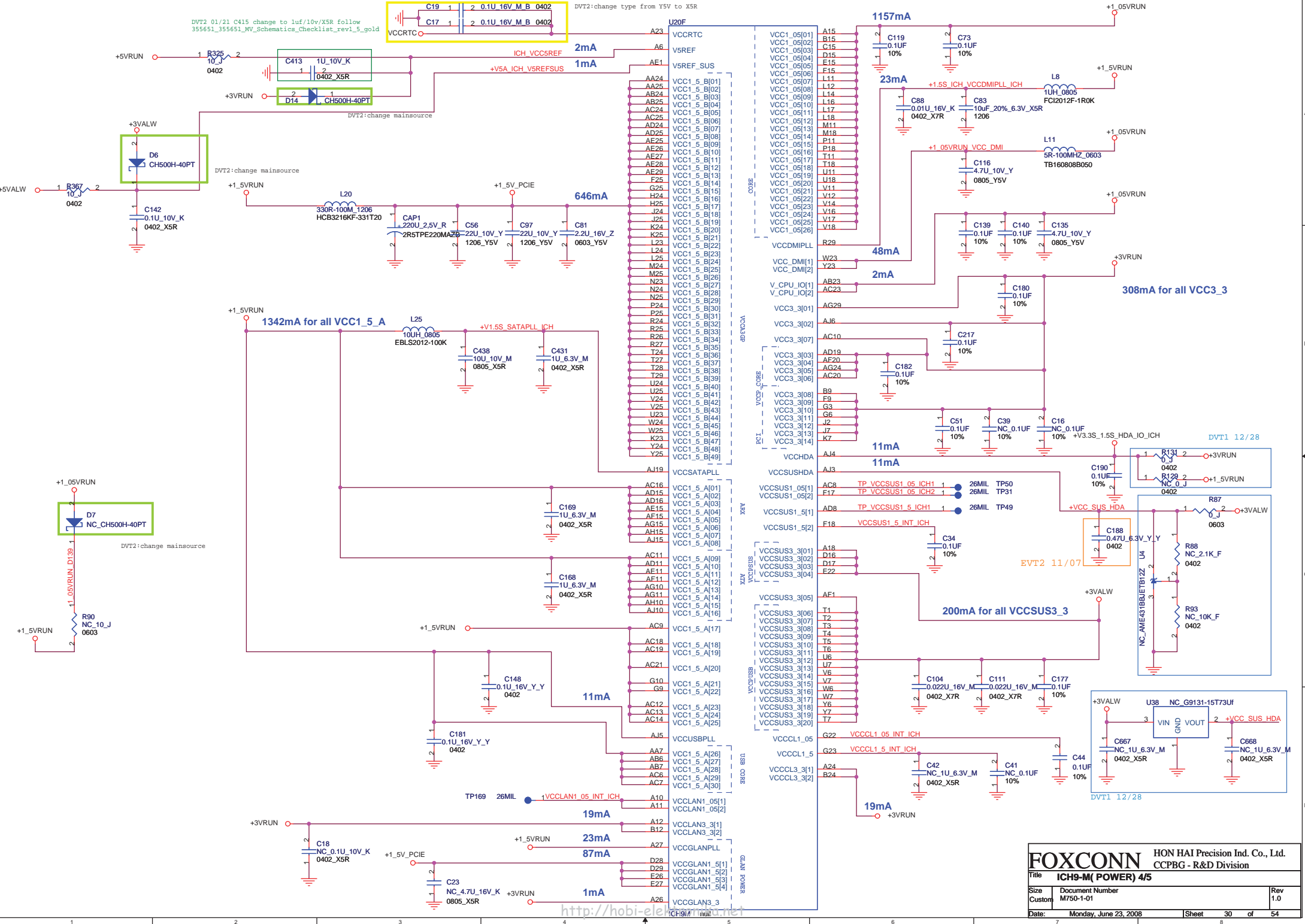
DISPLAY_SEL	
0	CRT
1	LVDS

Dock Support Selection

	Dock Support
0	Not Support
1	Support







**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **ICH9-M (POWER) 4/5**

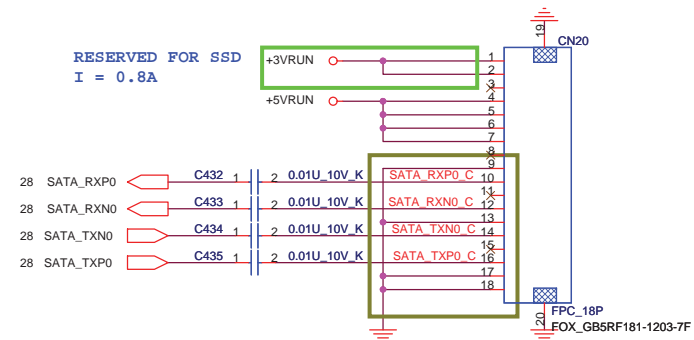
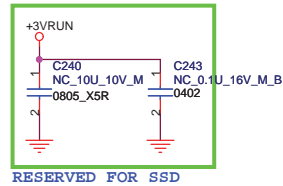
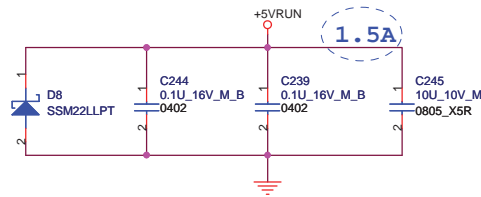
Size	Document Number	Rev
Custom	M750-1-01	1.0

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U20E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB29	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD5	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AF13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF26	VSS[047]	VSS[153]	R13
AF27	VSS[048]	VSS[154]	R14
AF5	VSS[049]	VSS[155]	R15
AF7	VSS[050]	VSS[156]	R16
AF9	VSS[051]	VSS[157]	R17
AG13	VSS[052]	VSS[158]	R19
AG18	VSS[053]	VSS[159]	R28
AG20	VSS[054]	VSS[160]	T12
AG23	VSS[055]	VSS[161]	T13
AG3	VSS[056]	VSS[162]	T14
AG6	VSS[057]	VSS[163]	T15
AG9	VSS[058]	VSS[164]	T16
AH12	VSS[059]	VSS[165]	T17
AH14	VSS[060]	VSS[166]	T23
AH17	VSS[061]	VSS[167]	B26
AH19	VSS[062]	VSS[168]	U12
AH2	VSS[063]	VSS[169]	U13
AH22	VSS[064]	VSS[170]	U14
AH25	VSS[065]	VSS[171]	U15
AH28	VSS[066]	VSS[172]	U16
AH5	VSS[067]	VSS[173]	U17
AH8	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AJ12	VSS[070]	VSS[176]	U27
AJ14	VSS[071]	VSS[177]	U3
AJ17	VSS[072]	VSS[178]	V1
AJ8	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B14	VSS[075]	VSS[181]	V23
B17	VSS[076]	VSS[182]	V28
B2	VSS[077]	VSS[183]	V29
B20	VSS[078]	VSS[184]	V4
B23	VSS[079]	VSS[185]	V5
B5	VSS[080]	VSS[186]	W26
B8	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	W3
C27	VSS[083]	VSS[189]	Y1
E11	VSS[084]	VSS[190]	Y28
E14	VSS[085]	VSS[191]	Y29
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	AG28
E24	VSS[089]	VSS[195]	AH6
E5	VSS[090]	VSS[196]	AF2
E8	VSS[091]	VSS[197]	B25
F16	VSS[092]	VSS[198]	
F28	VSS[093]		
F29	VSS[094]	VSS_NCTF[01]	A1
G12	VSS[095]	VSS_NCTF[02]	A2
G14	VSS[096]	VSS_NCTF[03]	A28
G18	VSS[097]	VSS_NCTF[04]	A29
G21	VSS[098]	VSS_NCTF[05]	AH4
G24	VSS[099]	VSS_NCTF[06]	AH29
G26	VSS[100]	VSS_NCTF[07]	AJ1
G27	VSS[101]	VSS_NCTF[08]	AJ2
G8	VSS[102]	VSS_NCTF[09]	AJ28
H2	VSS[103]	VSS_NCTF[10]	AJ29
H23	VSS[104]	VSS_NCTF[11]	B1
H28	VSS[105]	VSS_NCTF[12]	B29
H29	VSS[106]		

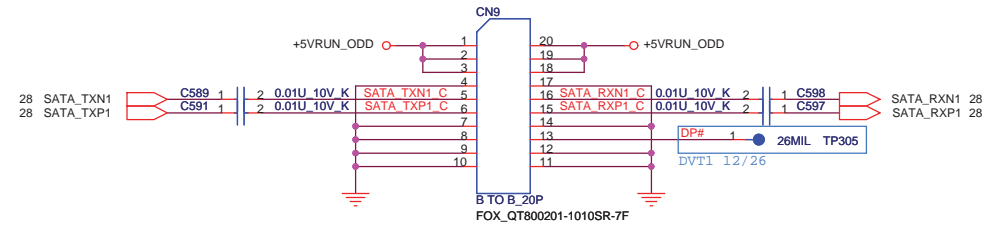
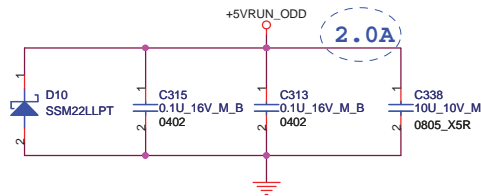
<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ICH9-M (GND) 5/5		
Size	Document Number	Rev	
A3	M750-1-01	1.0	
Date:	Monday, June 23, 2008	Sheet	31 of 54



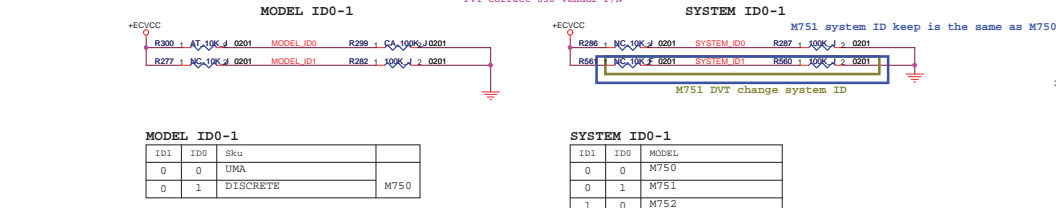
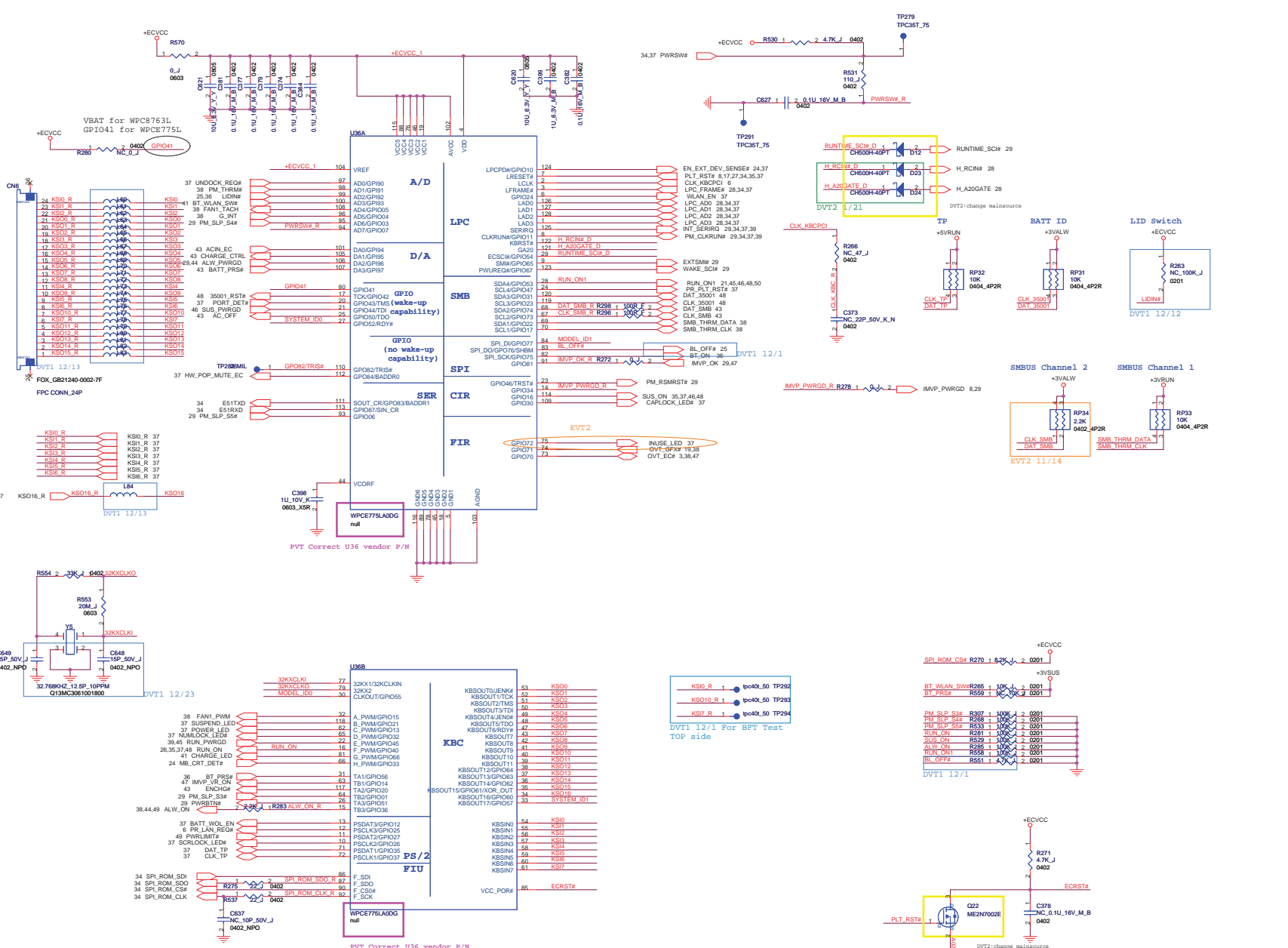
M751 DVT to increase the impedance for sata SI fail

## SATA HDD CONN



## SATA ODD CONN

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		SATA HDD/ODD	
Size	Document Number	Rev	
A3	M750-1-01	1.0	
Date:	Monday, June 23, 2008	Sheet	32 of 54

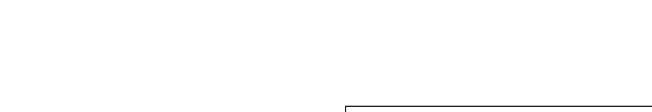


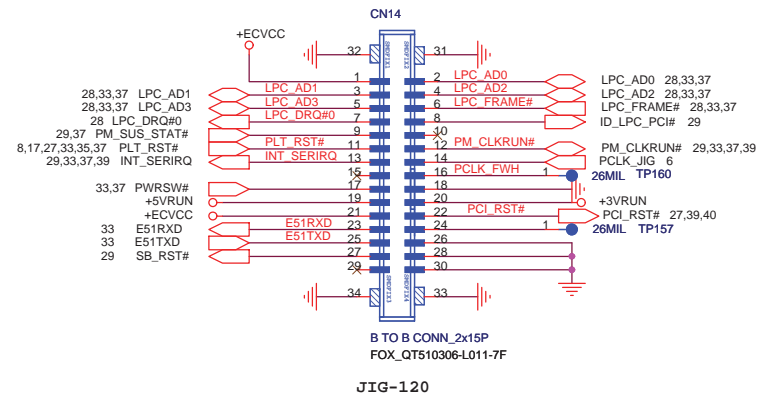
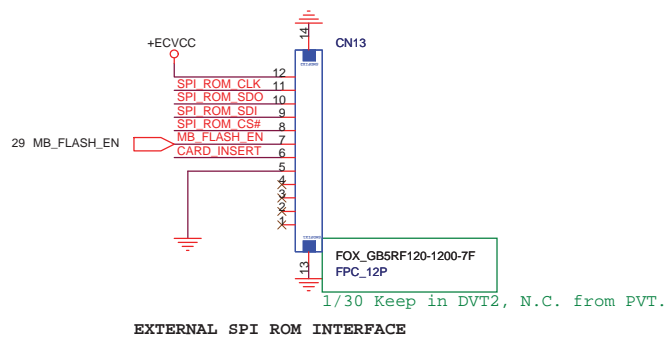
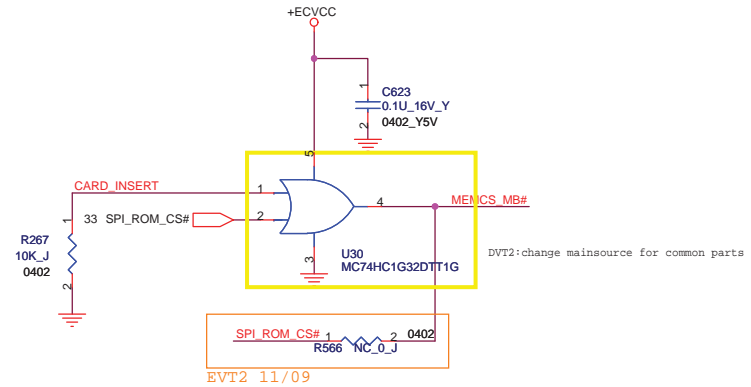
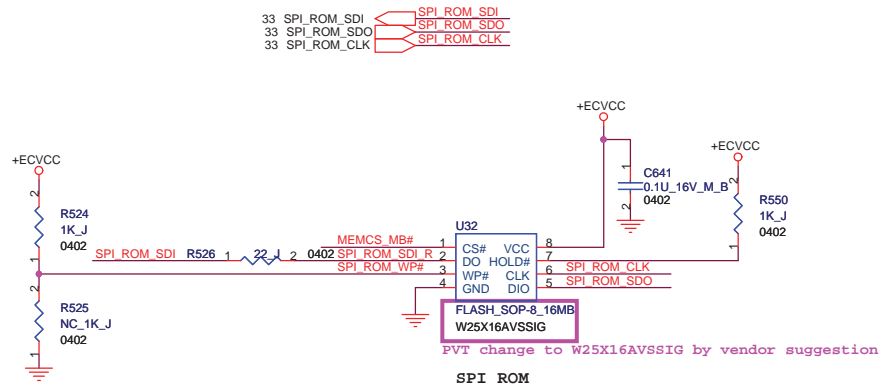
**MODEL ID0-1**

ID1	ID0	Sku	MODEL
0	0	UMA	
0	1	DISCRETE	M750

**SYSTEM ID0-1**

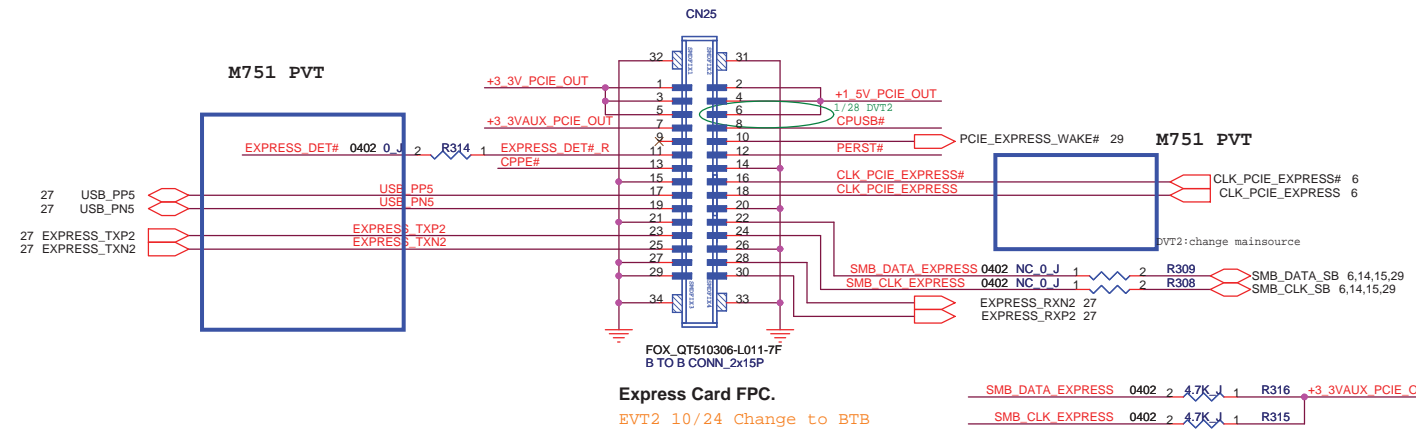
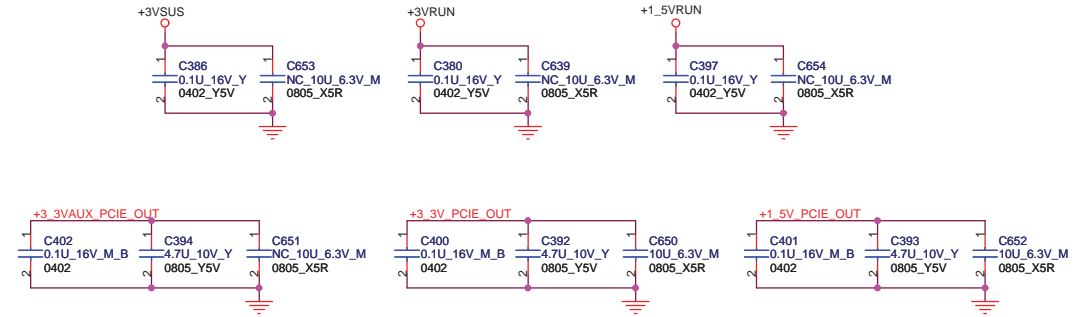
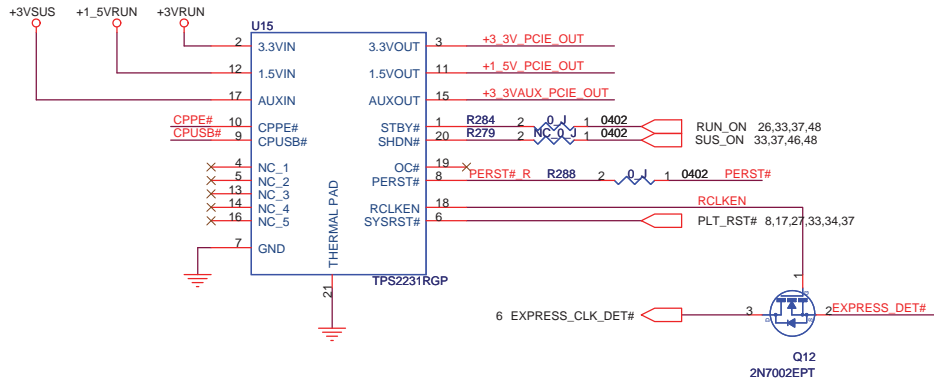
ID1	ID0	MODEL
0	0	M750
0	1	M751
1	0	M752





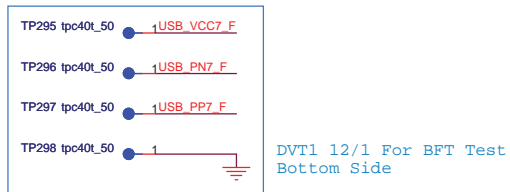
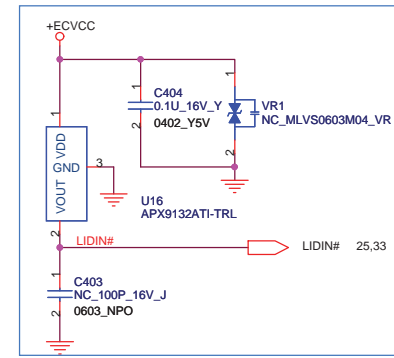
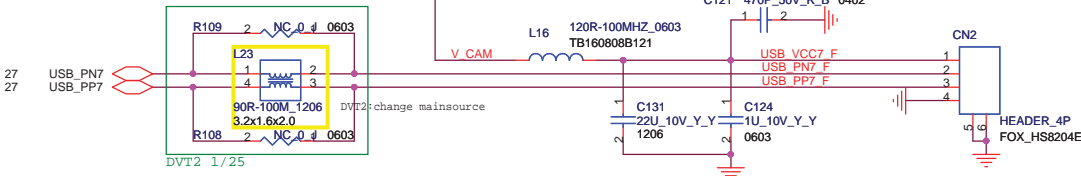
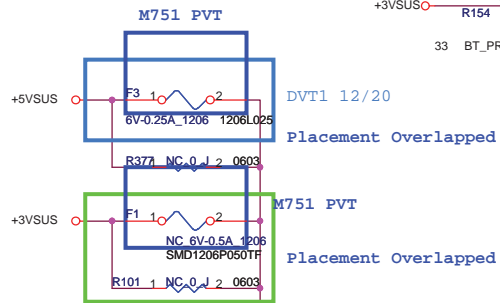
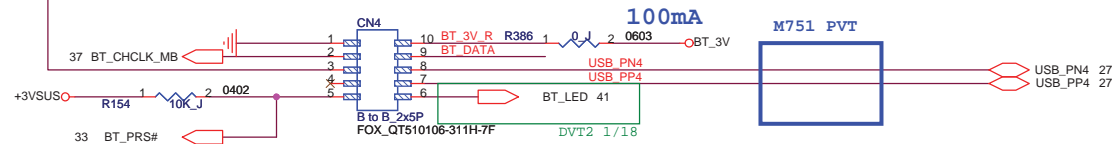
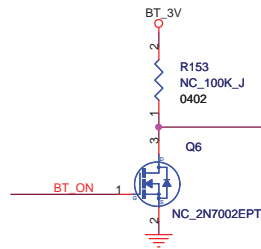
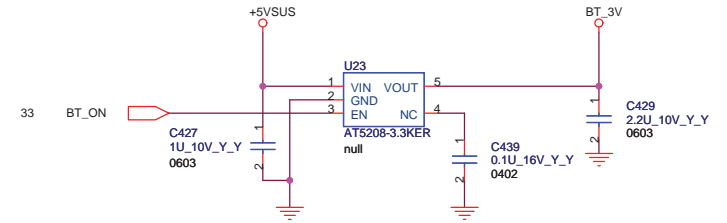
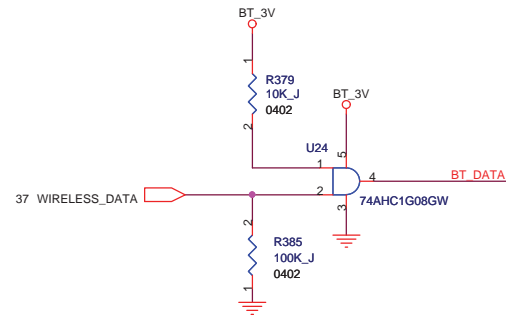
+1\_5V=>0.65A  
 +3\_3VAux=>0.275A  
 +3\_3V=>1.3A

Express Card Power Switch

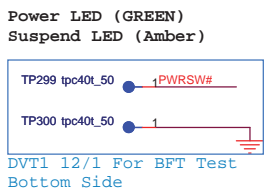
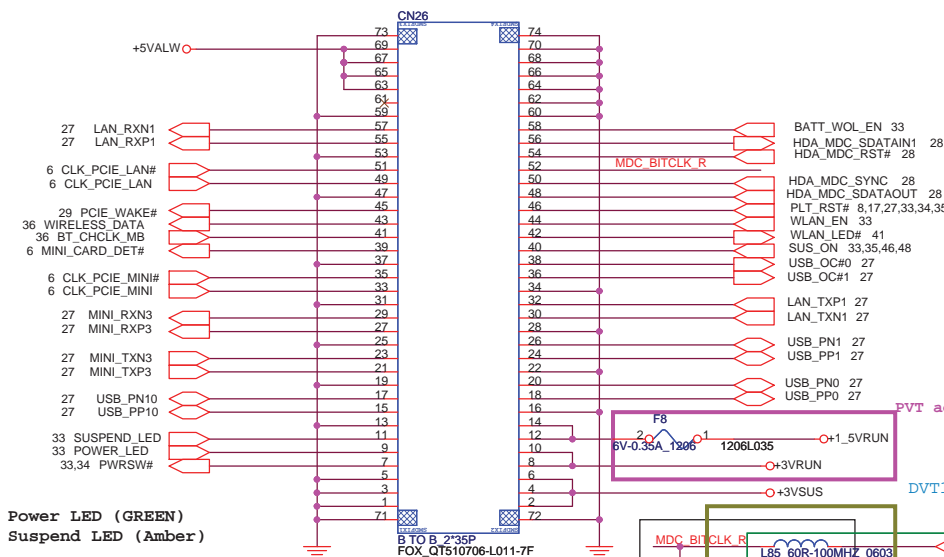


Express Card FPC.  
 EVT2 10/24 Change to BTB

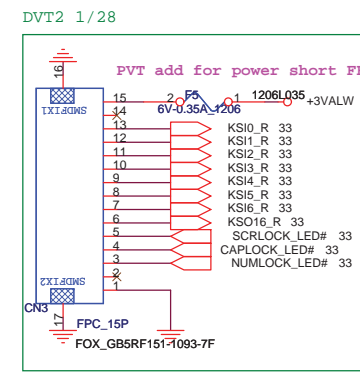
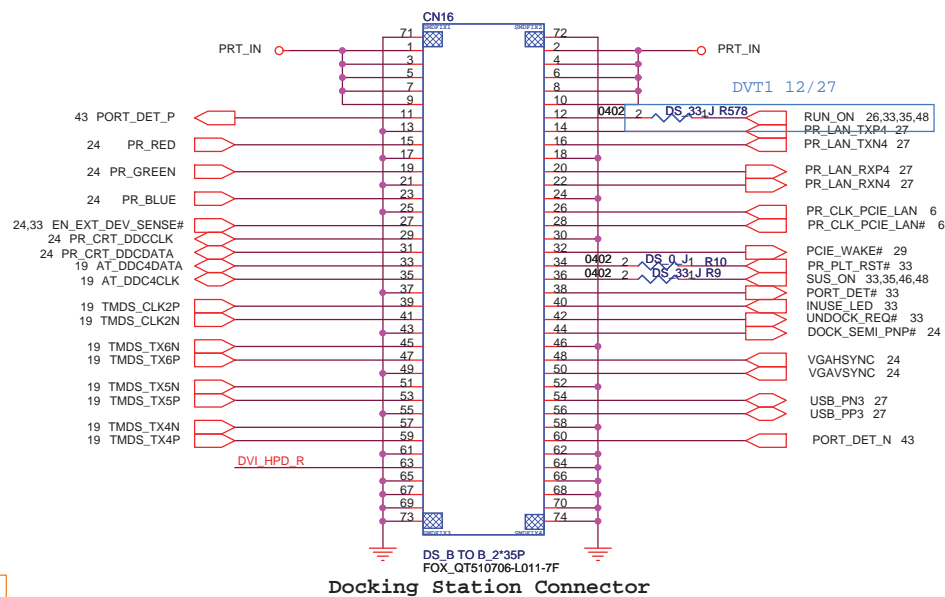
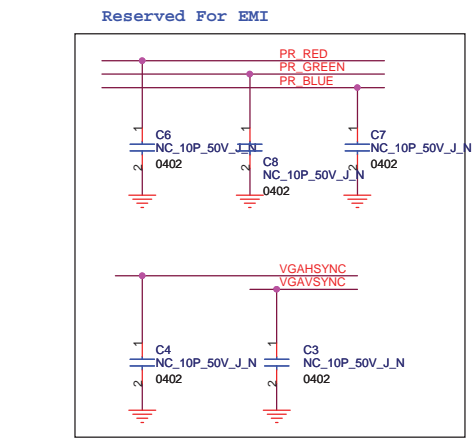
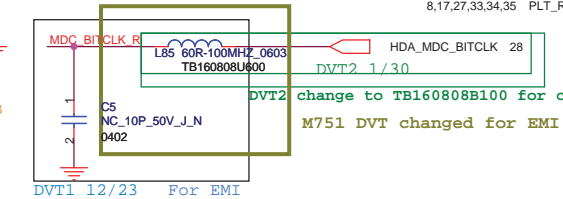
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>EXPRESS CARD</b>		CCPBG - R&D Division	
Size A3	Document Number M750-1-01	Rev 0.1	
Date: Monday, June 23, 2008	Sheet 35	of 54	



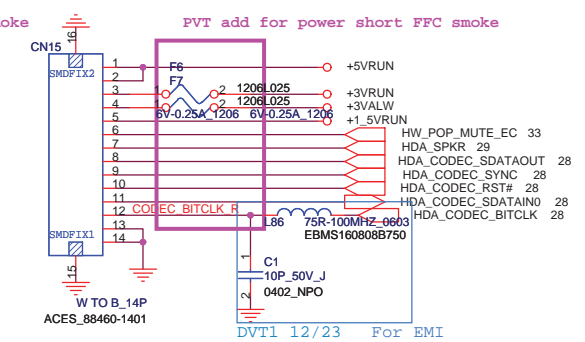




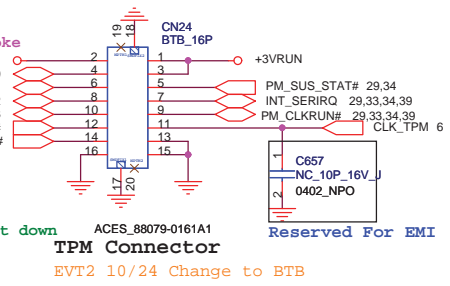
**USB board connector**  
EVT2 10/24 Change to BTB



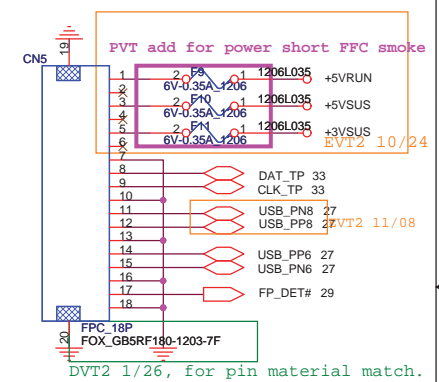
**Button Board FUNCTION TBD**



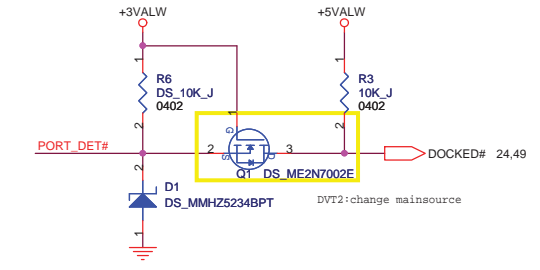
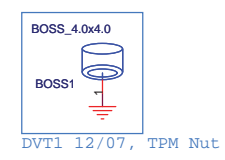
**Audio Board Connector**



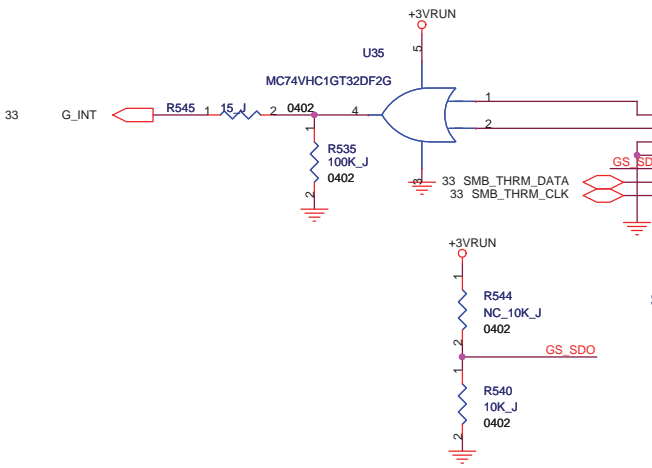
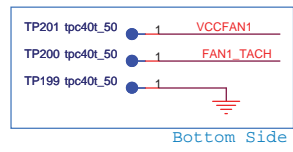
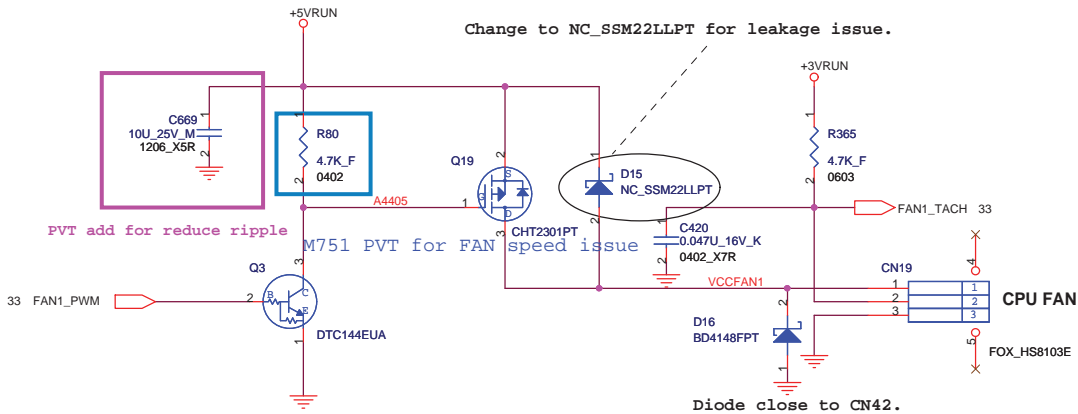
**TPM Connector**  
EVT2 10/24 Change to BTB



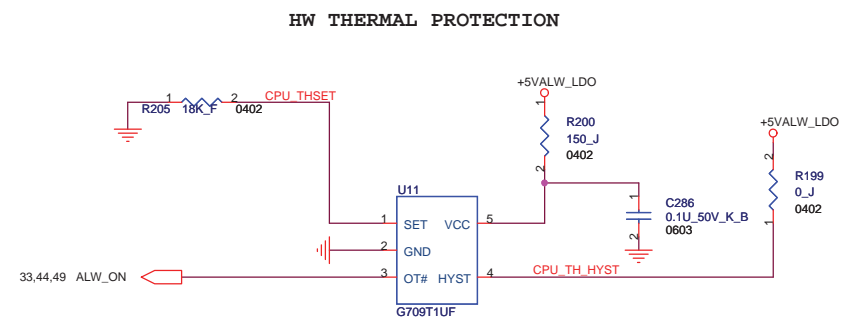
**Touch Pad Board Connector**



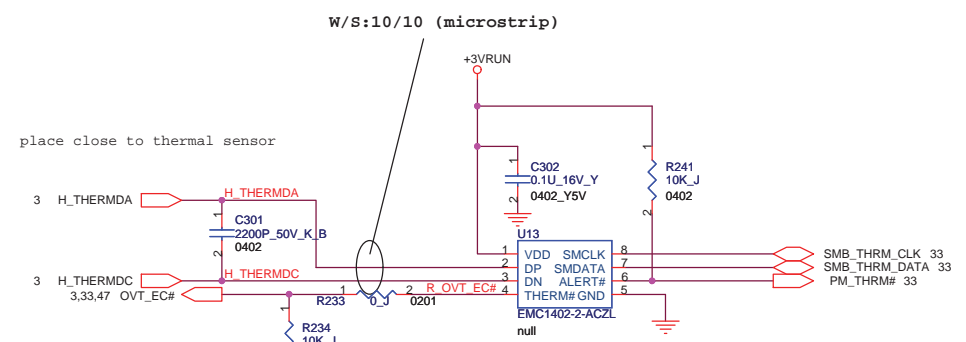
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
<b>Title DB connector &amp; Docking</b>		
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 37	of 54



**G-Sensor**  
SMBus Address: 38H

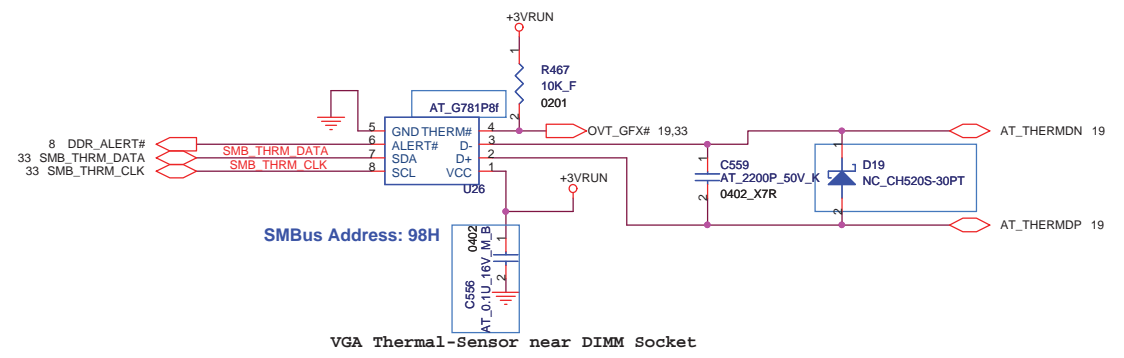


**HW thermal shut down temperature setting 95 degree . Put Near CPU .**



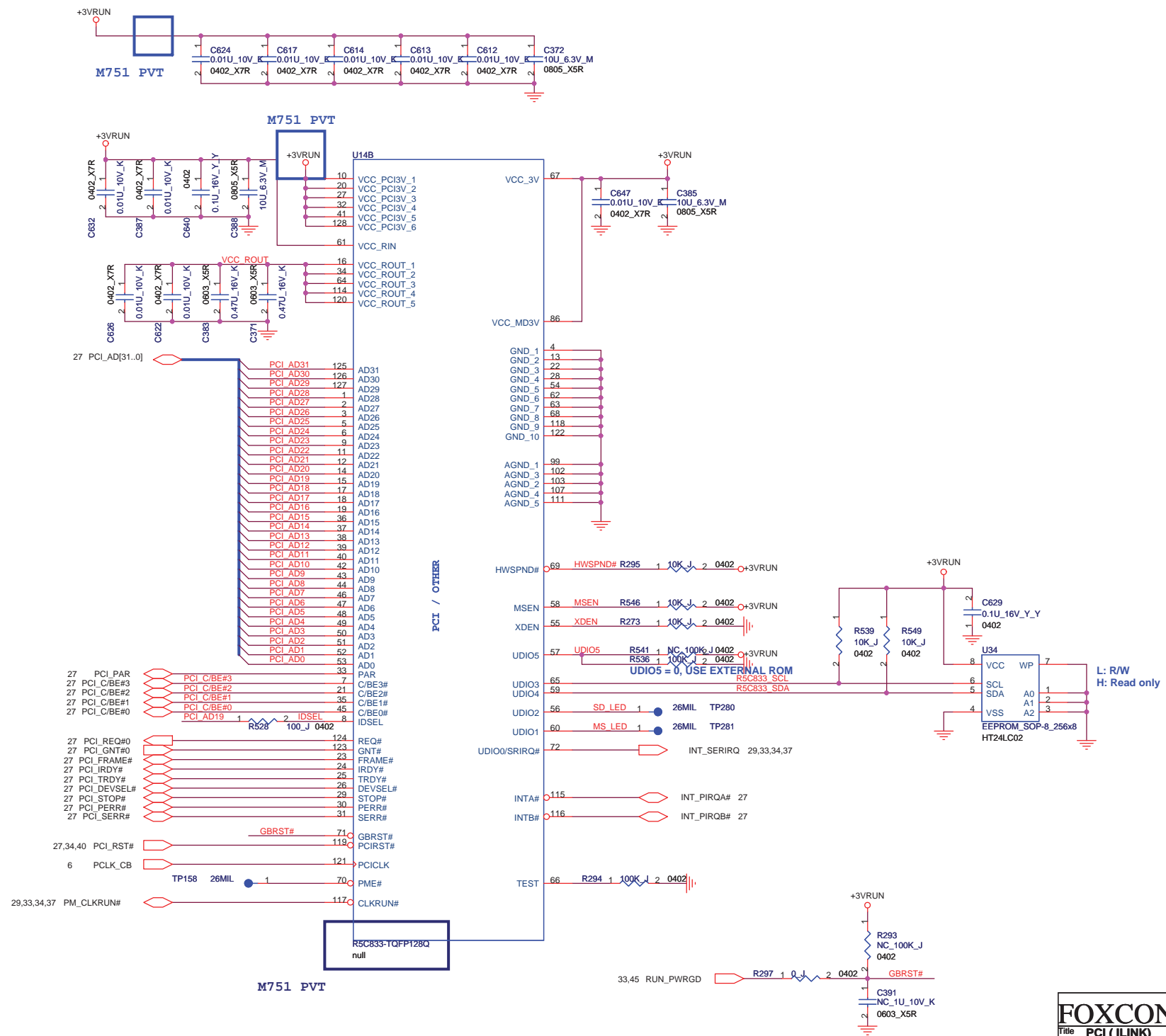
**SMBus Address: 9AH**

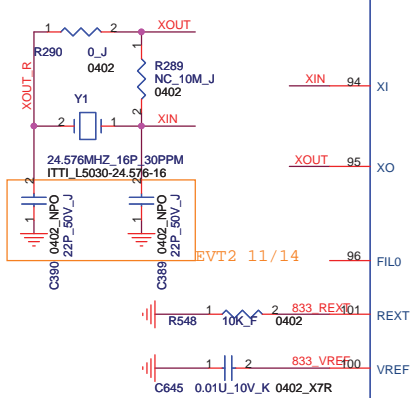
**CPU Thermal-Sensor**  
Place Thermal-Sensor near GMCH.



**SMBus Address: 98H**

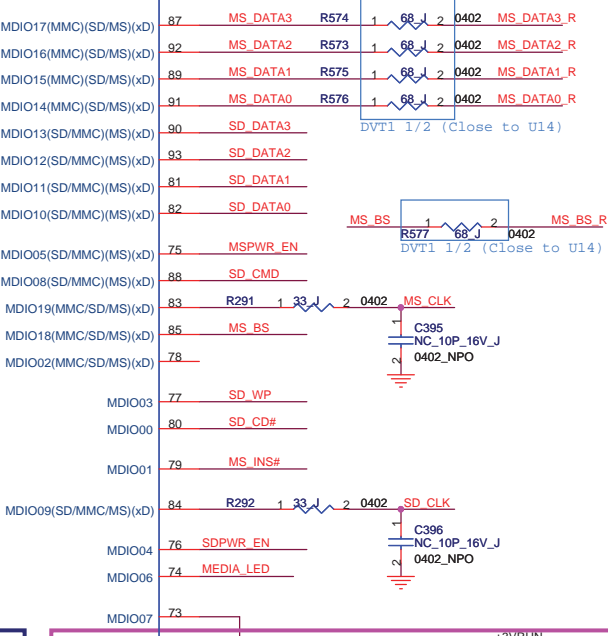
**VGA Thermal-Sensor near DIMM Socket**





Add net name

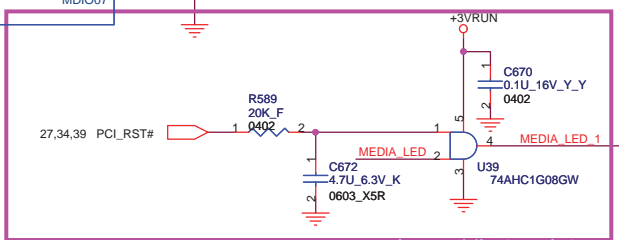
IEEE1394/SD



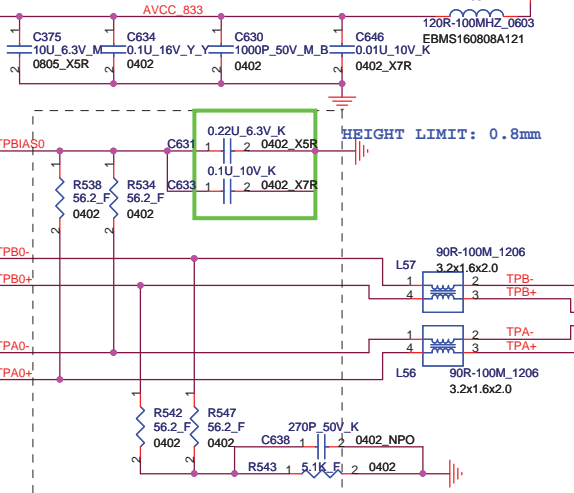
AS CLOSE AS POSSIBLE TO R5C833



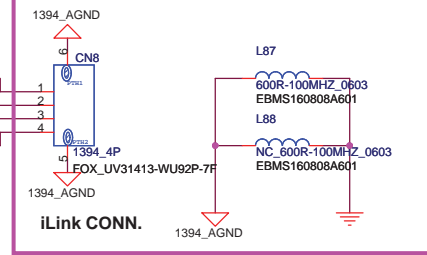
M751 PVT



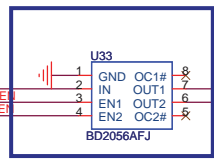
PVT add for MEDIA\_LED have high pulses cause the MEDIA\_LED light when power on Q328



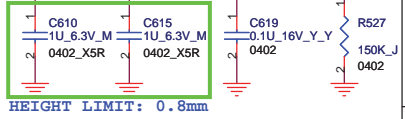
HEIGHT LIMIT: 0.8mm



M751 PVT

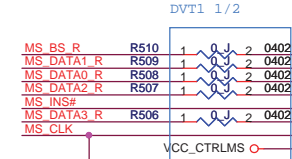


MS/SD POWER

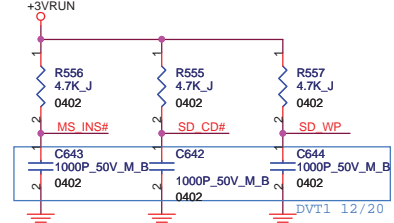


HEIGHT LIMIT: 0.8mm

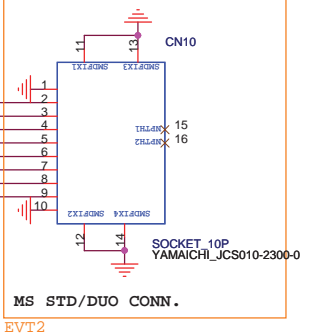
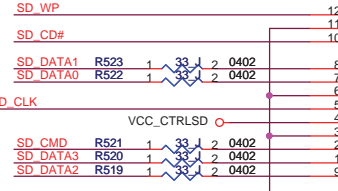
PVT add for EMI



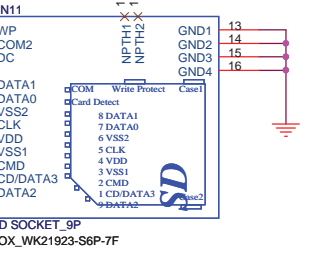
DVT1 1/2



+3VRUN



MS STD/DUO CONN.

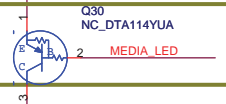


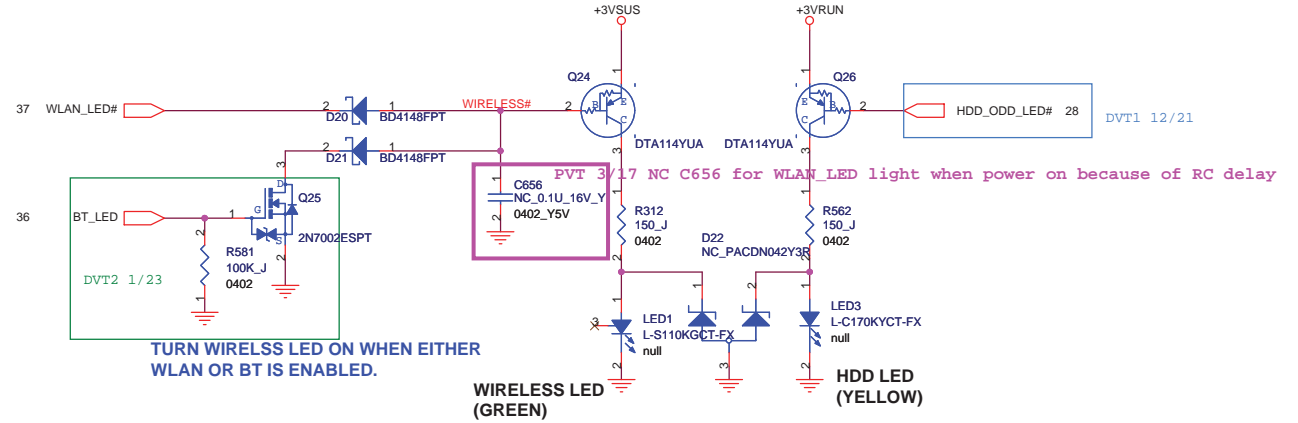
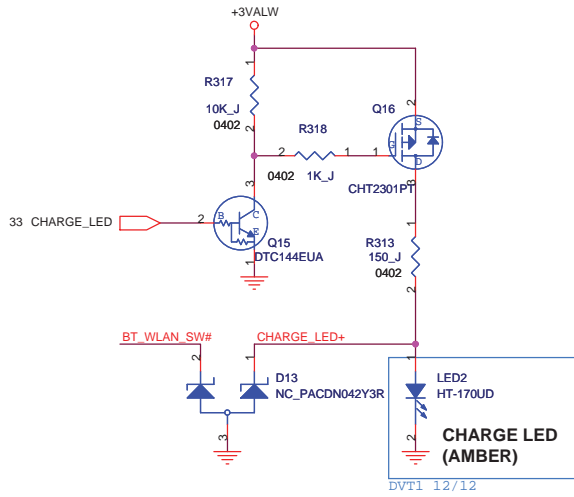
SD CONN.

DVT add Q30 for cost down need change EEPROM

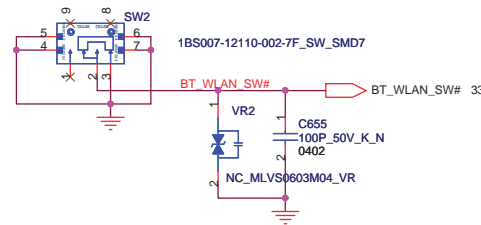


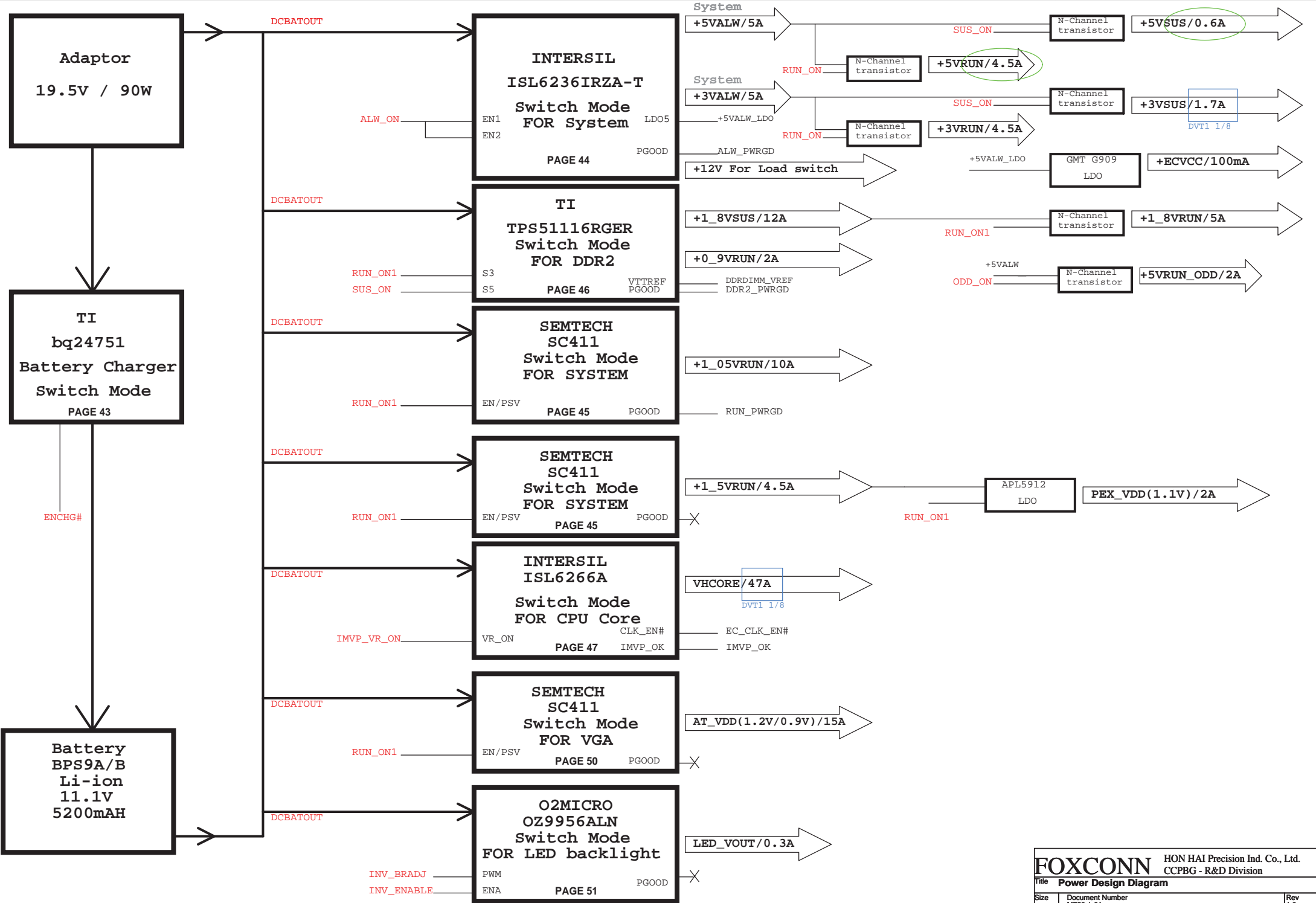
MS/SD LED (YELLOW)

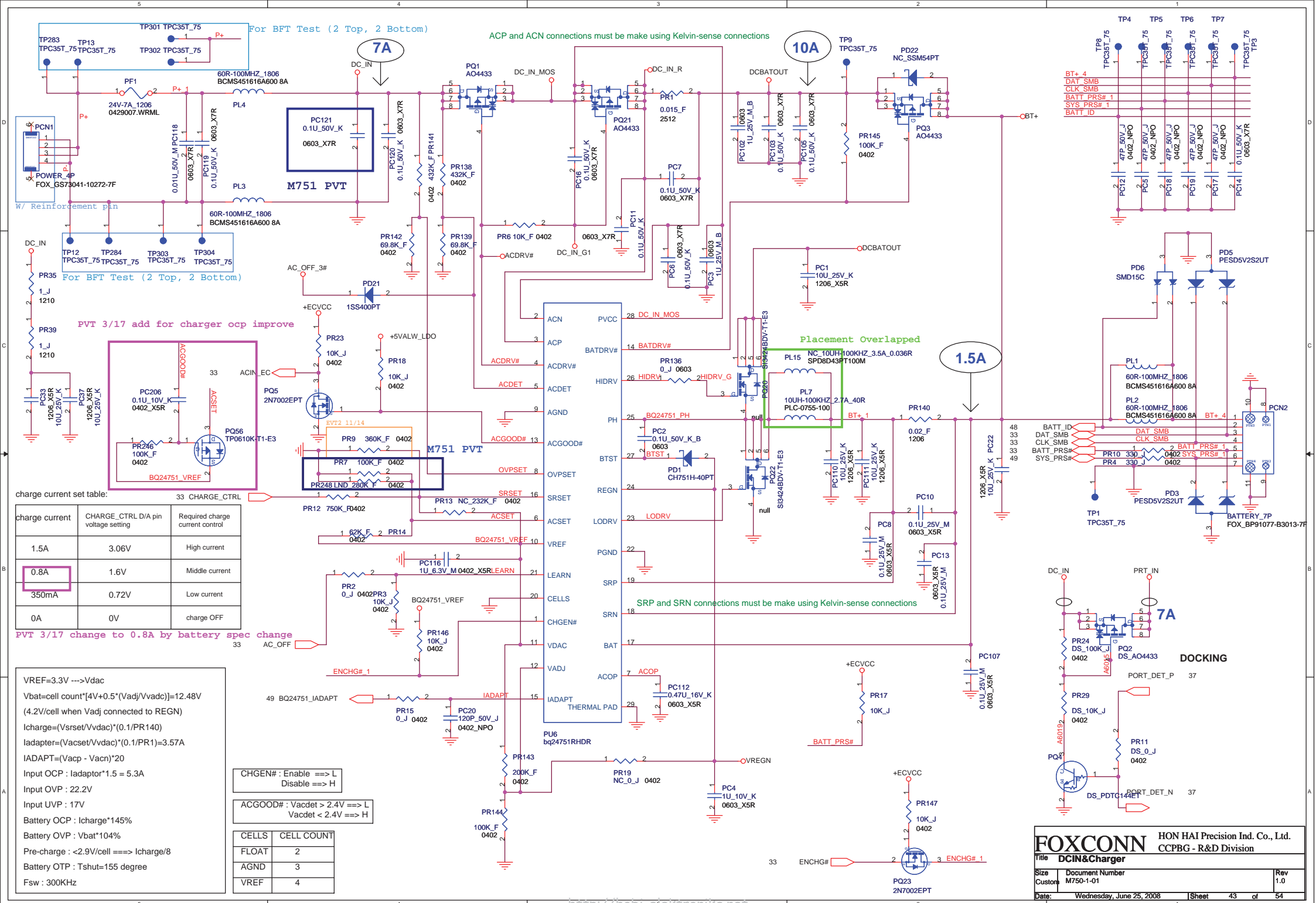




### WLAN/BT ON/OFF SWITCH







For BFT Test (2 Top, 2 Bottom)

TP12 TPC35T\_75  
TP284 TPC35T\_75  
TP303 TPC35T\_75  
TP304 TPC35T\_75

PVT 3/17 add for charger ocp improve

charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V ---> Vdac  
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vadc})] = 12.48V$   
 (4.2V/cell when Vadj connected to REGN)  
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR140)$   
 $I_{adaptor} = (V_{acset} / V_{vdac}) * (0.1 / PR1) = 3.57A$   
 $IADAPT = (V_{acp} - V_{vacn}) * 20$   
 Input OCP :  $I_{adaptor} * 1.5 = 5.3A$   
 Input OVP : 22.2V  
 Input UVP : 17V  
 Battery OCP :  $I_{charge} * 145\%$   
 Battery OVP :  $V_{bat} * 104\%$   
 Pre-charge :  $< 2.9V / \text{cell} \implies I_{charge} / 8$   
 Battery OTP :  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$

CHGEN# : Enable ==> L  
 Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L  
 Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

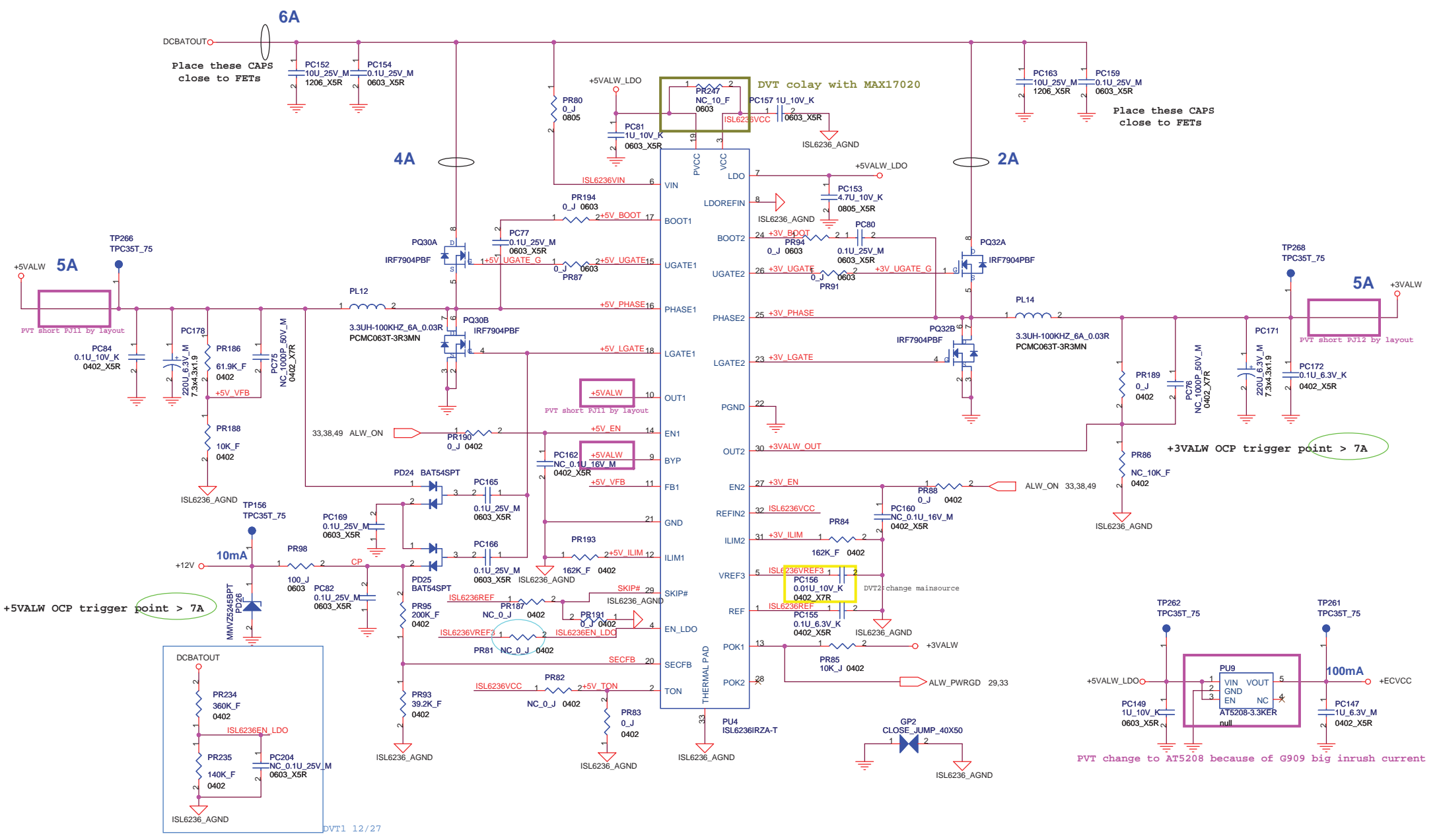
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title **DCin&Charger**

Size	Document Number	Rev
Custom	M750-1-01	1.0

Date: Wednesday, June 25, 2008 Sheet 43 of 54





TON	Operating Freqence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / (VIN * f * LIR * ILOAD(MAX))$$

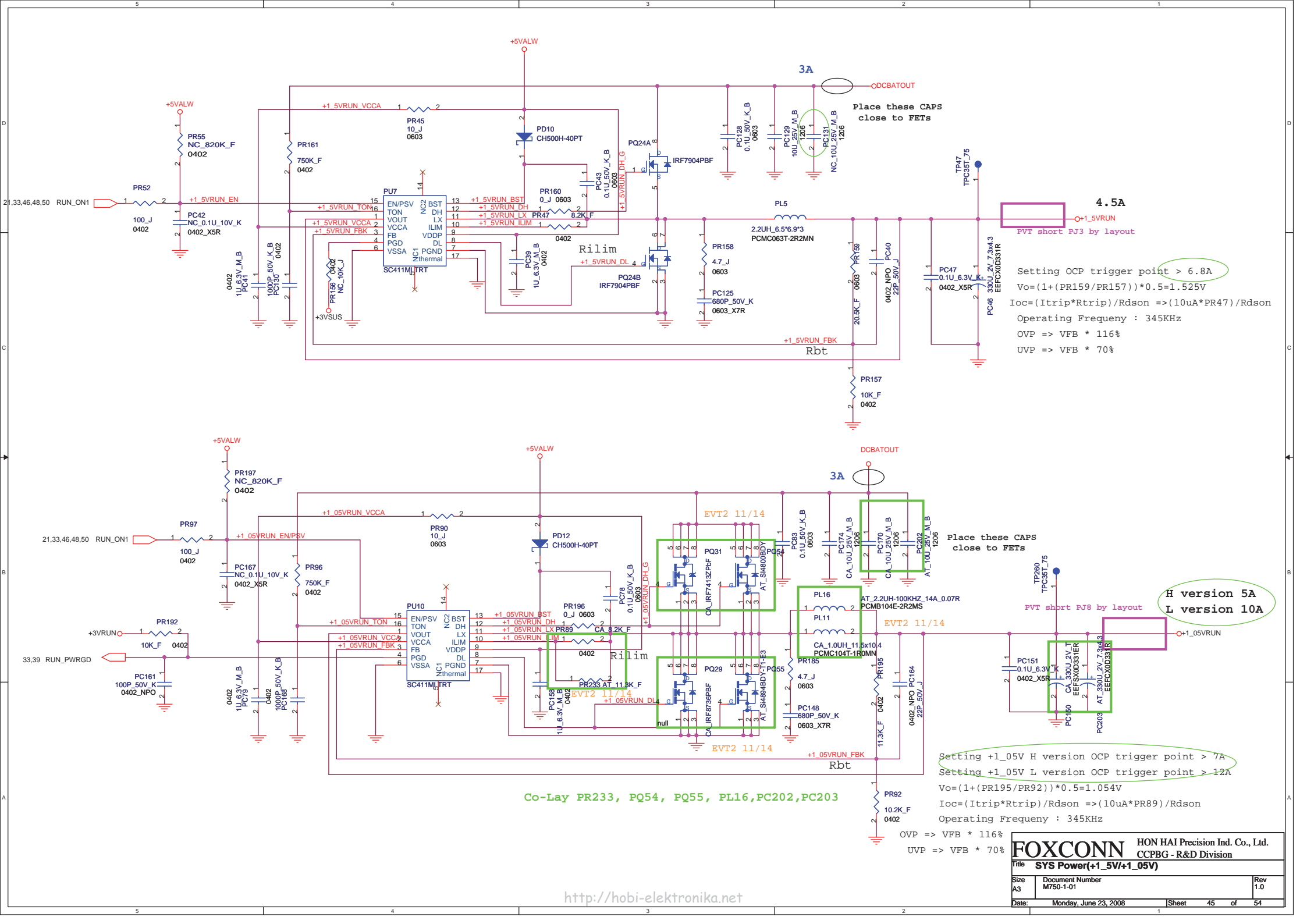
$$R_{ocp} = (I_{ocp} - I_{ripple}/2) * (10 * R_{ds}(on)) / 5u$$

$$+5VALW = ((PR186/PR188) + 1) * VFBI$$

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title **SYS Power (+3.3V/+5V)**

Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 44	of 54



Place these CAPS close to FETs

4.5A  
PVT short PJ3 by layout

Setting OCP trigger point > 6.8A

$V_o = (1 + (PR159/PR157)) * 0.5 = 1.525V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR47) / R_{dson}$   
 Operating Frequency : 345KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%

H version 5A  
L version 10A

Place these CAPS close to FETs

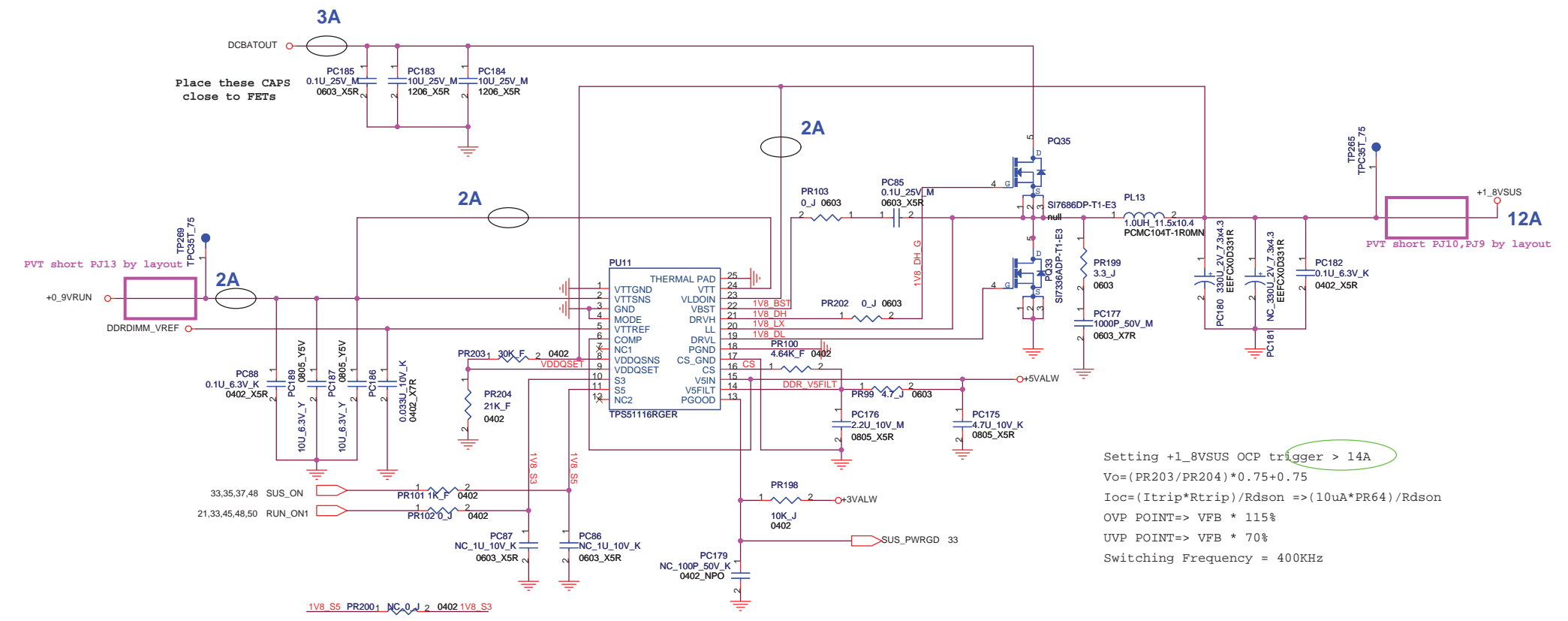
PVT short PJ8 by layout

Setting +1.05V H version OCP trigger point > 7A  
Setting +1.05V L version OCP trigger point > 12A

$V_o = (1 + (PR195/PR92)) * 0.5 = 1.054V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR89) / R_{dson}$   
 Operating Frequency : 345KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%

Co-Lay PR233, PQ54, PQ55, PL16, PC202, PC203

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>SYS Power(+1.5V/+1.05V)</b>		CCPBG - R&D Division	
Size A3	Document Number M750-1-01	Rev 1.0	
Date:	Monday, June 23, 2008	Sheet	45 of 54



DCBATOUT

Place these CAPS close to FETs

VVT short PJ13 by layout

TP289  
TPC35T\_75

DDRDIMM\_VREF

VVT short PJ10, PJ9 by layout

TP285  
TPC35T\_75

+1\_8VSUS

Setting +1\_8VSUS OCP trigger > 14A

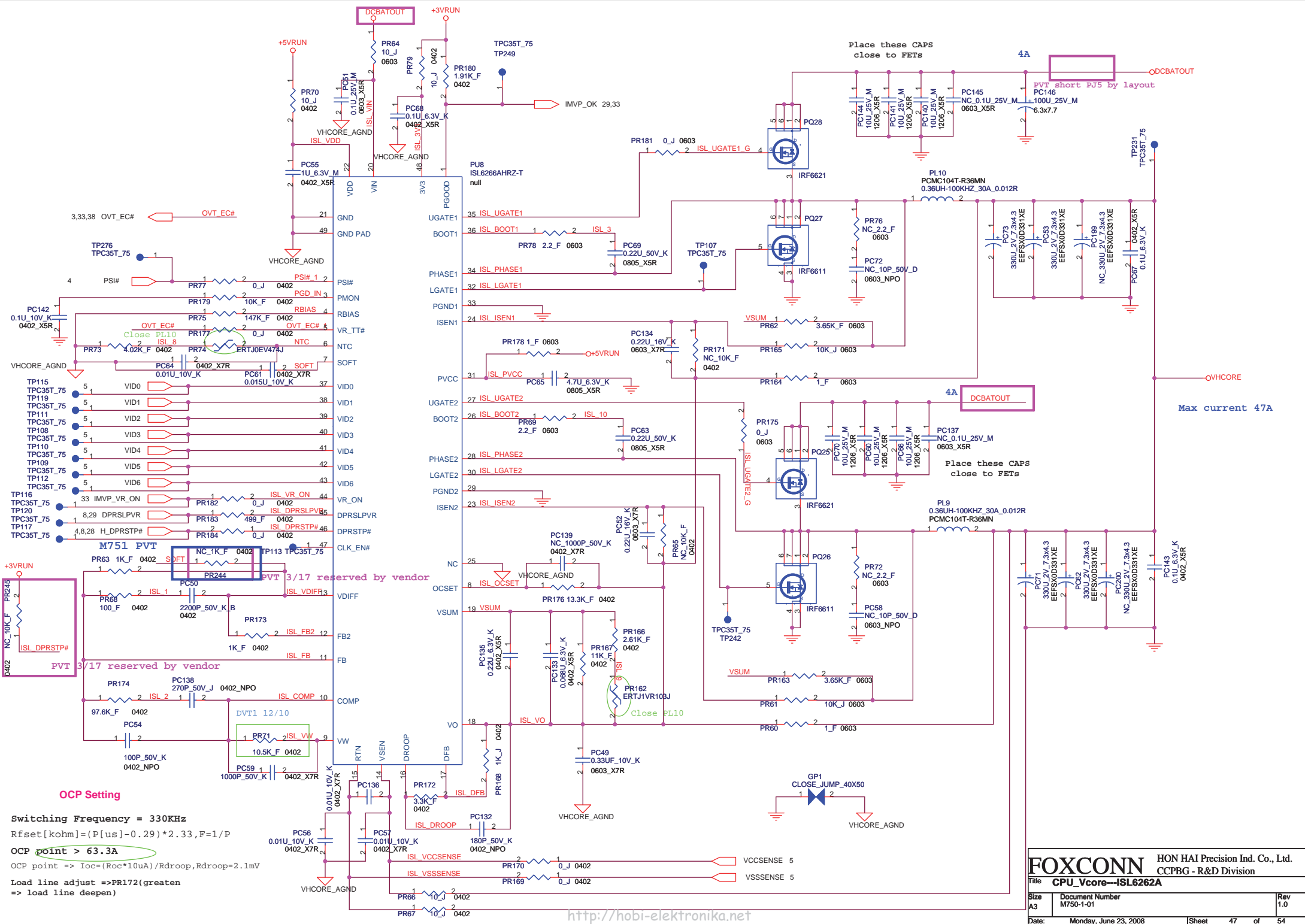
$$V_o = (PR203/PR204) * 0.75 + 0.75$$

$$I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR64) / R_{dson}$$

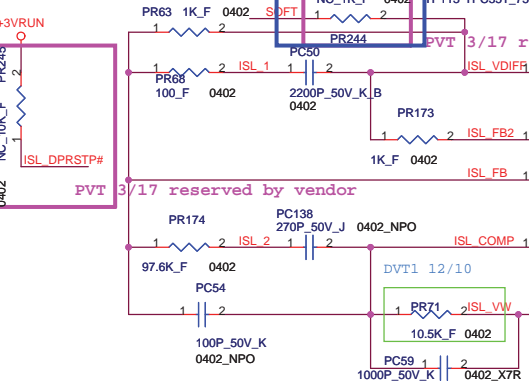
OVP POINT => VFB \* 115%

UVP POINT => VFB \* 70%

Switching Frequency = 400KHz



- TP276 TPC35T\_75
- TP115 TPC35T\_75
- TP119 TPC35T\_75
- TP111 TPC35T\_75
- TP108 TPC35T\_75
- TP110 TPC35T\_75
- TP109 TPC35T\_75
- TP112 TPC35T\_75
- TP116 TPC35T\_75
- TP120 TPC35T\_75
- TP117 TPC35T\_75
- TP118 TPC35T\_75
- TP113 TPC35T\_75
- TP114 TPC35T\_75
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- TP138 TPC35T\_75
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- TP140 TPC35T\_75
- TP141 TPC35T\_75
- TP142 TPC35T\_75
- TP143 TPC35T\_75
- TP144 TPC35T\_75
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- TP146 TPC35T\_75
- TP147 TPC35T\_75
- TP148 TPC35T\_75
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- TP152 TPC35T\_75
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- TP164 TPC35T\_75
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- TP249 TPC35T\_75
- TP250 TPC35T\_75



**OCP Setting**

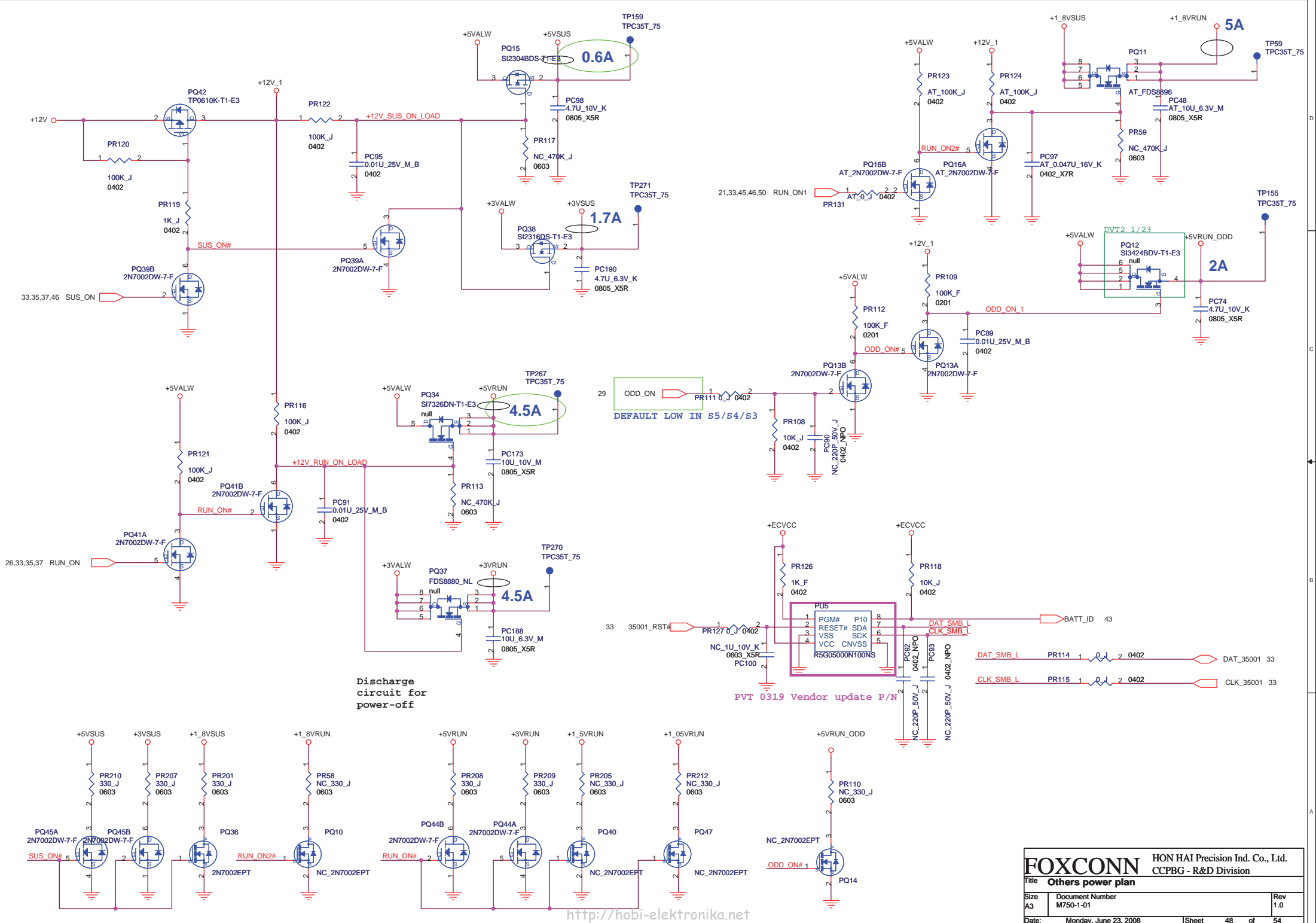
Switching Frequency = 330KHz

$$R_{set}[kohm] = (P_{us} - 0.29) * 2.33, F = 1/P$$

OCP point > 63.3A

OCP point =>  $I_{oc} = (R_{oc} * 10\mu A) / R_{droop}, R_{droop} = 2.1mV$

Load line adjust => PR172(greaten => load line deepen)

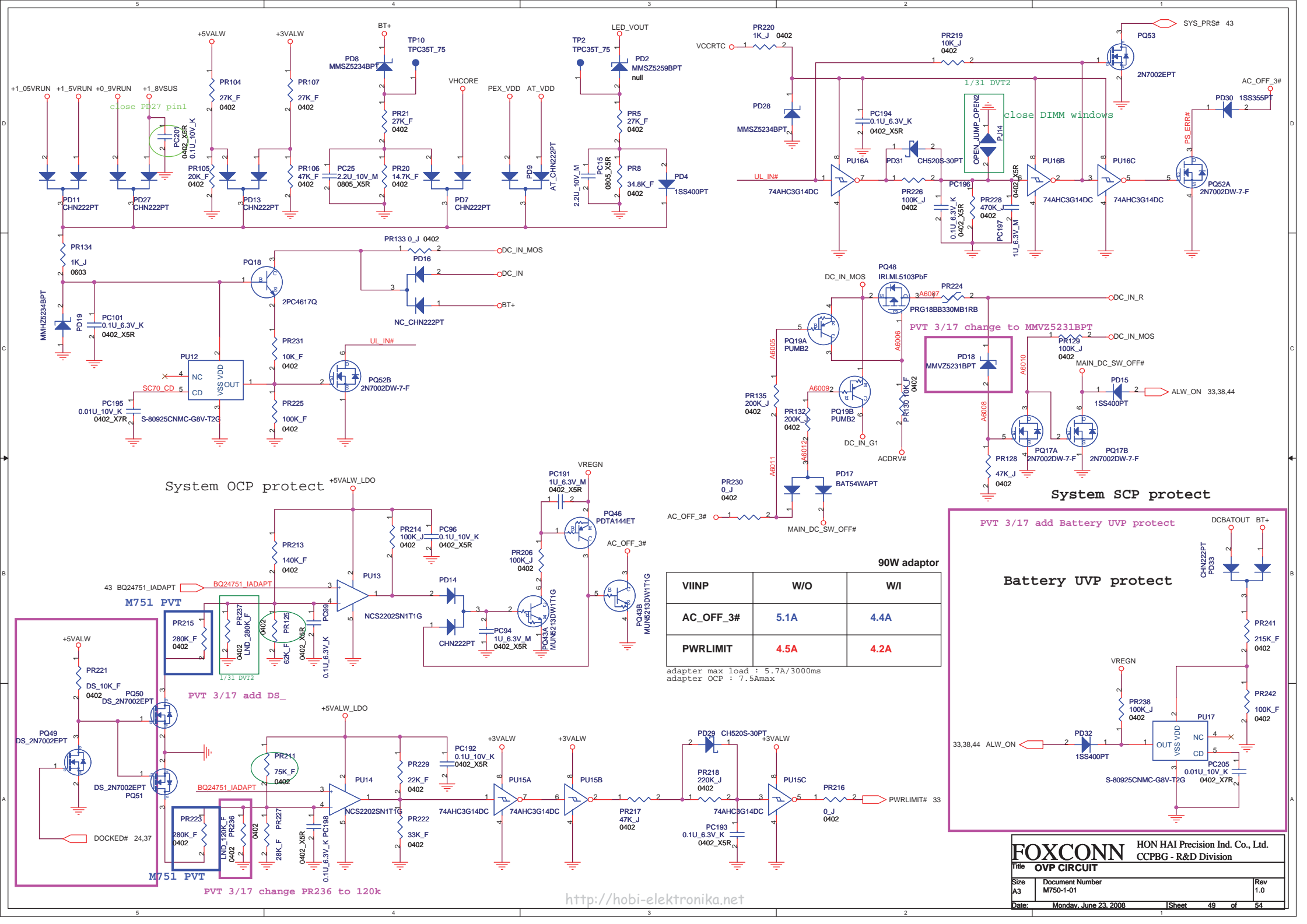


Discharge  
circuit for  
power-off

29 ODD\_ON  
DEFAULT LOW IN S5/S4/S3

PVT 0319 Vendor update P/N

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Title Others power plan</b>			
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 48	of 54	



System OCP protect

System SCP protect

Battery UVP protect

90W adaptor

VIINP	W/O	W/I
AC_OFF_3#	5.1A	4.4A
PWRLIMIT	4.5A	4.2A

adapter max load : 5.7A/3000ms  
 adapter OCP : 7.5Amax

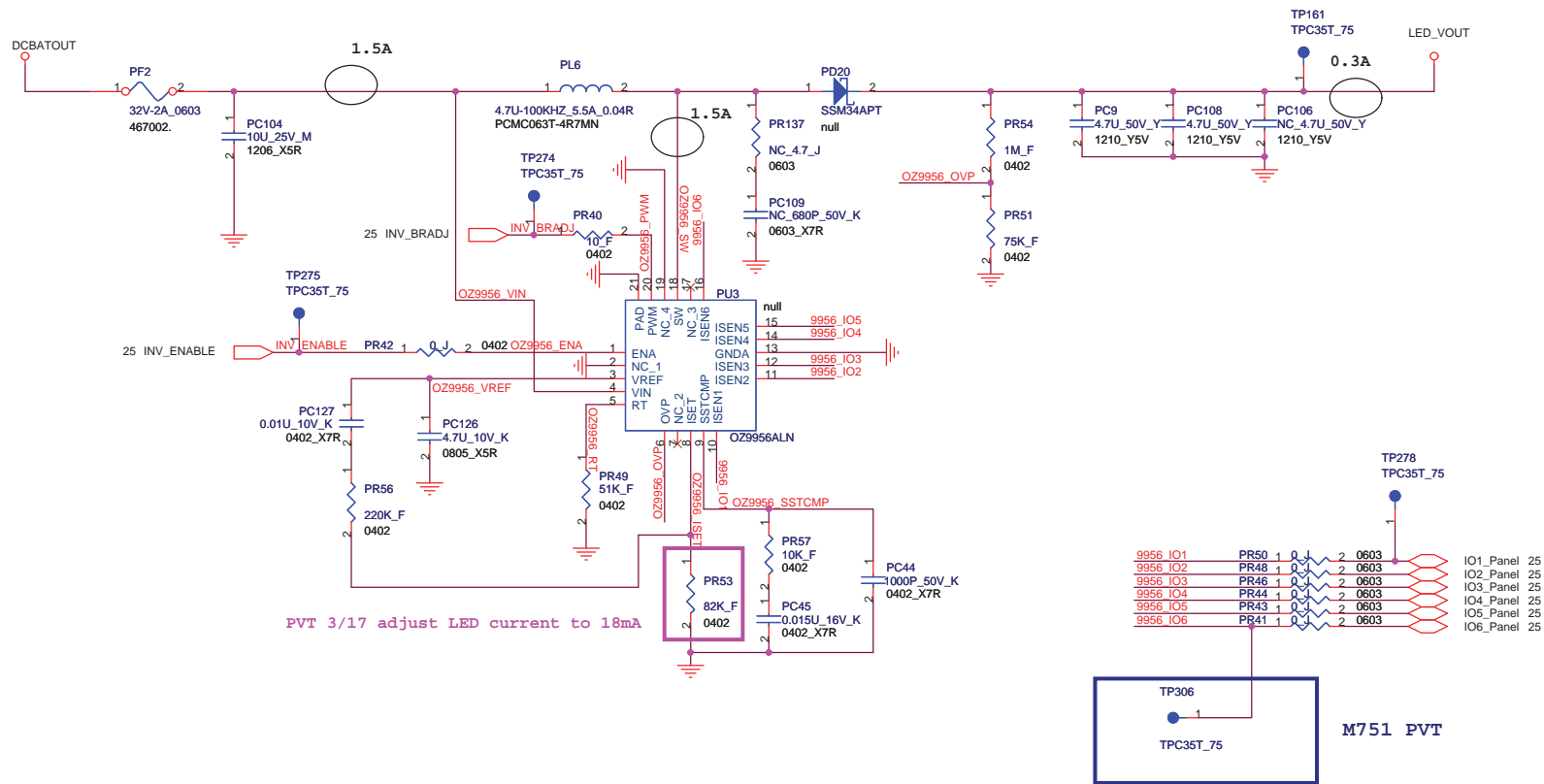
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

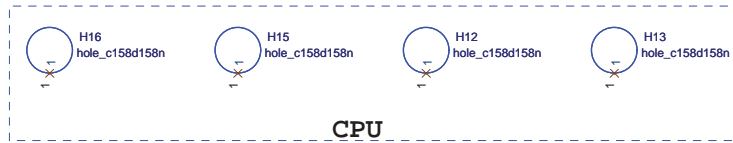
Title: **OVP CIRCUIT**

Size: A3	Document Number: M750-1-01	Rev: 1.0
Date: Monday, June 23, 2008	Sheet: 49	of 54

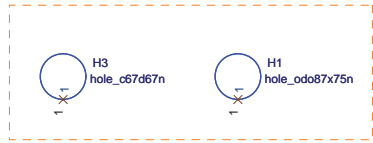




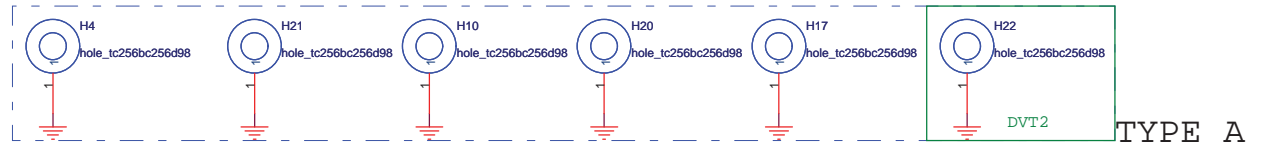
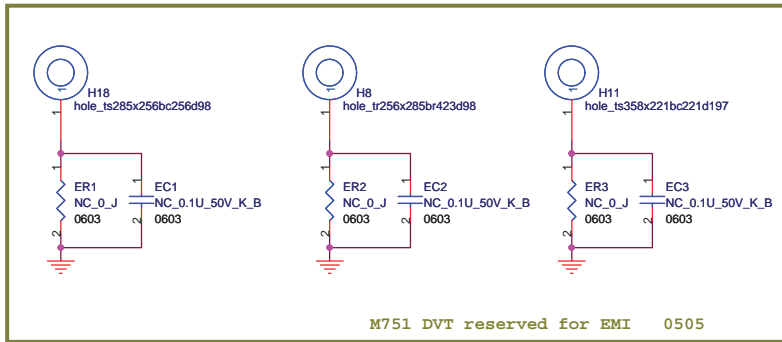




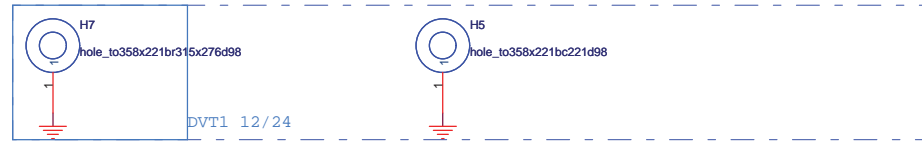
CPU



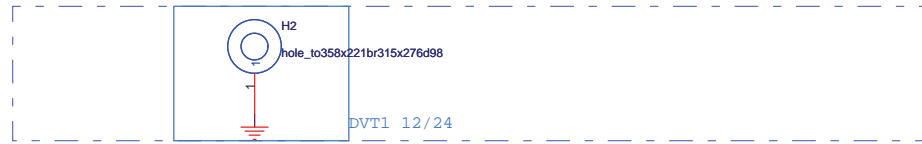
EVT2 11/10 Guide Pin Hole



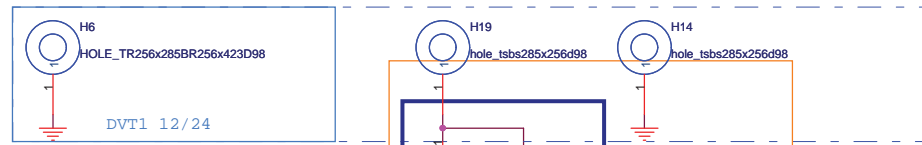
TYPE A



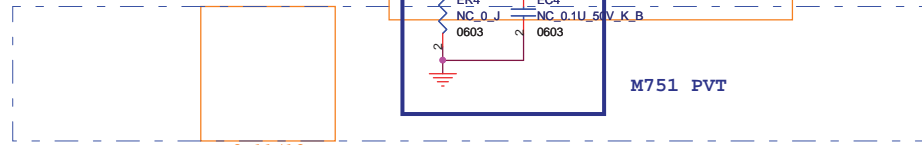
TYPE C



TYPE G



TYPE J



TYPE O

EVT2 11/12

Mainboard

M751 PVT

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		HOLE	
Size	Document Number	Rev	
A3	M750-1-01	1.0	
Date:	Wednesday, June 25, 2008	Sheet	52 of 54

10/12 Change color of MS/SD/HDD LED.  
Mount R419, R414, R420, R421.  
10/13 SYSTEM\_ID, MODEL\_ID definition update.  
10/20 CPU 22uP CAP N.C. parts location change.  
N.C. R101 For EVT2 (Use +5V type camera module)  
10/24 Move PCI Express pair of LAN from port5 to port1.  
10/29 Change FR9 to 422K.  
Add PL15 and PL7 co-lay.  
Modify charge current setting table.  
Mount PR83.  
PL11 change to 1uH.  
Add TP276 test point.  
Add PC201 0.1uF and close to PD27 pin1.  
Change PL6 to 4.7uH and add TP274,TP275 test points.  
10/30 Refer to PUR suggestoin to change component source.  
Add NC\_PR232  
Change PR30 to 10K and PR31 to 1K.  
Mount PC30  
Add TP278 test point.  
10/31 Refer to PUR suggestoin to change component source.  
Swap LVDS group of ATI M82.  
11/02 Change "\*" to net "EN\_EXT\_DEV\_SENSE" for low active.  
Modify MB Semi-PNP circuit.  
11/03 Inverse HDMI pairs polarity(DVI pairs inversed on docking side).  
11/04 Change USB board connector.  
Combine MS/SD LED to one(MEDIA\_LED).  
11/05 N.C. R377, Mount F3.  
Change INUSE\_LED to GPIO72.  
Change MS slot to YAMAICHI JCS010-2300-0.  
11/06 Change part of CN16/CN26.(Height Change)  
Change netname of "SD\_WP#" to "SD\_WP".  
Change PR143 to 200Kohm.  
Update charge current setting table.  
Reserve BATT\_WOL\_EN for LAN wake up enable/disable in battery mode.  
11/07 C453, C452, C451,C426, C425, C424 change size to 0402.  
Mount PR158, PC125 and PR185, PC148 and PR199, PC177 and PR16, PC21.  
N.C. PR36.  
Change C188 from 0.1uF to 0.47uF.  
11/08 Swap USB\_PP8/PN8 for ease of routing.  
Change button board connector to WBF31326-F04TR.  
Change MS/SD LED to side view, yellow color.  
Change U7 from CM2009 to CM2006.  
Update VCC\_DDC power isolation circuit.  
Add R565,C658 for SRTCST#.  
11/09 Change PC31 from 22p to 100p.  
Reserve R566 for removal of Ext. SPI Conn on DVT.  
Reverse Button Brd CN pin assignment.  
Add EMI Cap C659-C666 on +1\_8VSUS.  
11/10 Delete guide pin hole H9, H22.  
N.C. F3, mount P1.(Use +3VSUS for camera power on EVT2).  
11/11 Change pin assignment of Express CN.

10/12 Change PTH hole size. (H11)  
Add TP283,TP284.  
Change net name "ISL\_VSSSENSE\_" to "ISL\_VSSSENSE".  
11/13 Change PR285-290 for SI probe point.  
Change type of H14,H19.  
Change PR22=51K, PR232=200K.  
11/14 Tune crystal accuracy, change C390/C389/C416/C412 to 22PF,C648/C649 to 18PF.  
Change PR6=360K.(Charge Current Control)  
Co-Lay PR233, PQ54, PQ55, PL16.  
Change RP34 to 2.2K for SI.  
N.C. R415, mount L47 on H model.  
11/19 N.C. R559 (Double pull up on BT\_PRS#)  
11/23 Change camera power to +5VSUS.  
DVT1 12/01 Swap DVI bus polarity.  
Route RUN\_ON to docking station CN.  
Add logic gate(U37) to prevent panel flash when boot up.  
Add R567, bypass brightness control signal.  
Use +3V\_DELAY(Q4) to prevent M82 high pulse on LCD control signals.  
12/07 Change DC-IN CN(PCN1, With Reinforcement Pin).  
Add TPM Nut (BOSS1).  
Change Button Board CN (CN3) to 15 pin.  
Add R570 for power consumption measurement.  
12/12 Change U6 from Quad to Dual XOR gate.  
Change EMI Caps C424-C426, C451-453 to 10pF.  
Change color of LED2(Charge LED) to Amber.  
Change U16 from MR-sensor to Hall-sensor. (N.C. R263)  
12/13 Change damping resistors of keyboard matrix to 120ohm Ferrite bead.(For EMI)  
12/17 Change C451,C452,C453,C424,C425,C451 to 22pF. (For EMI)  
Add one more +3VSUS (CN26) for WLAN module to cover 1500mA(peak)/1100mA(normal) requirement.  
12/18 Add one more LCDVCC pin (CN1) for panel to improve voltage drop.  
Add optional resistors(R571,R572) for gamma control.  
Reduce LED\_VOOUT from 6 pins to 2 pins.  
12/20 Reserve net "BL\_OFF" to "BL\_OFF#".  
Add R573-577 to improve MS signal overshoot/undershoot.  
Mount C642-644.  
Change F3 to 0.25A.  
12/21 Change Net "HDD\_LED#" to "HDD\_ODD\_LED#"  
12/23 Change C412/C416 from 22pF to 10pF.  
Change C648,C649 from 18pF to 15pF.  
Mount U26(VGA Thermal Sensor) on H model only.  
Add 75 ohm bead, 10pF capacitor on HDA\_MDC\_BITCLK/HDA\_CODECD\_BITCLK for EMI.  
12/24 Update H2/H6/H7/H8 footprint.  
Delete R563, R564 (CR1\_GND).  
Change D17, D18 to SSM22 to reduce voltage drop.  
Change pull up voltage of R360/R361 to +3VRUN. (Only Strap/GPIO pin connected to +3V\_DELAY)  
N.C. C403 (Not necessary for ESD)  
12/26 Delete ODD\_DP# connection to ICH9M.

12/27 Add PC204 for noise filtering.  
Add R578 for protection.  
Change U27 from RClamp0514 to RClamp0524.  
N.C. SW1, R134,R141  
Change PR38 to 2K, PR37 to 5.1K.  
12/28 N.C. U4 shunt regulator to reduce S4 consumption.  
Mount R131, N.C. R129.  
Reserve LDO (U38) for 1.5V type VCCSUSDA.  
Add R579,R580 to avoid floating on input pin.  
1/2 N.C. C451-453, C424-426.  
N.C. PC204.  
Add prefix AT\_ on R322, R51.  
Change damping resistor value of MS card.  
(R573-577 from 33 to 68 ohm)  
(R506-510 from 33 to 0 ohm)  
Change L30-32 to 27mH inductor.  
Change C258,260,262 to 2.2pF.  
Change revision of clock generator(U29) to Rev.B  
1/5 Change D2/D3 to low capacitance type.  
Fine tune delay timing. Change R19/R565 to 13K.  
1/8 Update power design spec.  
VCore: 47A, +3VSUS: 1.7A.  
DVT2  
1/15 Update power budget of VCCCHA,VCCSUSDA,VCCDMI,VCC1\_5\_A  
Add GND pin on C130.2.  
1/19 Add BT\_LED on CM4.6  
Update WIRELESS LED circuit. Page41.  
1/21 Add screw hole H22.  
Add D23, D24 for leakage issue when EC initialization.  
Add R460 for Non-Dock Sku.  
1/23 PD12 change to S134248DV-T1-E3.  
PR125 change to 62Kohm  
PR215 change to 205Kohm  
PR211 change to 75Kohm  
PR223 change to 154Kohm  
Add PR237 ND\_280Kohm , PR236 ND\_154Kohm for Non-Dock sku.  
Add pull down resistor (R581) on BT\_LED.  
1/25 Mount L23, N.C. R108, R109 for EMI.  
Change L86 from 75R to 10R for SI.  
For Docking sku, add prefix DS\_ on value of C257,C259,C261,CN16 D1,PQ2,PQ4,PR11,PR24,PR29,Q1,Q20,Q21,R6,R9,R10,R165,R167,R416 R444,R578,U8,U9,U10.  
1/26 Change R176 from 54.9 to 649 Ohm.  
Del L48, Add R582, R583 (N.C.)  
Change C413 from 0.1uf to 1uF.  
Change CN5 from Gold plated to TIN plated.  
1/28 Mount R555, R556, R557.  
Add +1.5V\_PCIE\_OUT on CN25.6 to reduce voltage drop.  
Change CN3 from WBF31526-F04TR to GBSRF151-1093-7F.  
(Vendor naming rule change, same part.  
layout footprint pin reversed)  
1/29 Add R584, R585, Q27 to solve DDC capacitance issue.  
Add R586 for identification of Dock support.  
1/30 Change L86 back to 75R, change L85 from 75R to 10R.  
Mount CN13 for software debug on DVT2.  
N.C. R572.  
Move R321 to U37B.6  
1/31 Move PJ14 to PR226.2  
Change R176 back to 54.9 ohm.  
Add prefix LND on PR236,PR237 for Non-Dock skue for LOW model.  
Add PAD1 for EMI Grounding.

0218 change U30 from NC7832M5X(14-NC7832M-5X00) to MC74HC1G32D7T1G(14-MC74HC1-G300)  
change D2,D3 from BAS316(16-BAS3160-0000) to BAS316PT(16-BAS316P-T000) for common parts  
change D6,D7,D9,D11,D12,D14,D23,D24 from 16-SCS500V-4000 to CHS500H-40PT16-CHS00H4-0P00) for common parts  
change Q1,Q5,Q17,Q21,Q22 from 17-2N7002P-T000 to ME2N7002E(17-ME2N700-2E00) for common parts  
change Q23 from 17-MMBT390-4001 to PMBT3904.215(17-PMBT390-4200) for common parts  
change C303,PC156 from 0.01U,6.3V,K(1C-2B20103-K100) to 0.01U,10V,K(1C-2B20103-K200) for common parts  
change L23,L28,L40,L41,L42 from 90R-100MHZ\_0R35(1L-FDLW315-N900) to 90R-100M\_1206(1L-FWCM321-6F00) for common parts  
change C19,C17 from Y5V to X5R tolerance  
change PR32 to 11K, PR33 to 19.6k to set the battery mode voltage to 0.95V by AMD for battery mode dual display

0318 PVT  
NC C656 for WLAN\_LED light when power on because of RC delay  
update battery identify (CPU5) P/N to R500500N10N0NS by vendor  
update U7 symbol to CM2006-02OR  
remove R345 value to HD\_ for BOM change of disable Hdaudio in 128MB SKU  
modify PU11,PU12,PU3,PU8,PU10,PU9,PU13,PU5 and short by layout  
correct U36 vendor P/N to WPCB775LA0DG  
change U32 to W25X16VSSIG by vendor suggestion  
add PQ56,PC206,PR246 for charger ocp improve by M760 battery OCP issue  
modify P43 charge current table ,middle current change from 1A to 0.8A  
add PR244 and PR245(dummy directly) for intersil ISL6266A found C4 hang at the other company  
change PD18 to MMVZ5231BPT for SCP circuit  
add UVP circuit (PU17,PR238,PD32,PC205,PR242,PR241,PD33)  
change PR236 to 120Kohm for power limit point improved  
change PQ50,PQ51,PQ49,PR221 value title to DS.  
change PR53 to 82Kohm for LED backlight current modify  
add R587,Q28,Q29 for improve HDMI voltage drop

0326 Short RJ1,RJ2,PJ4 by layout  
add C669 for reduce fan power source ripple  
add L87,L88 for EMI  
add U39,C670 for MS/SD abnormal behavior

0327 change PU9 to AT5208 because of G909 big inrush current

0328 NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS  
add R589,C672 for MS/SD led abnormal when power on

NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS  
add R589,C672 for MS/SD led abnormal when power on  
reserve R588 for reduce G-sensor power ripple

0402 add FS-P11 for power short

0403 change PR241 from 232K to 215K for UVP circuit improve

0408 NC R348,R356,R357 for using AMD internal SS  
change R378 value to HD\_ for HDMI disable

M751 DVT  
0505  
Reserve EC1,EC2,EC3, ER1,ER2,ER3 for Hynix 1GB EMI  
change HDD sata CN20 pin define to increase the impedance for SATA SI  
0506  
reserve PR247 for colay with MAX17020  
Update U29 footprint for Japan/Mitsui package  
change L85 to 60ohm for EMI  
NC C5 for EMI  
0508  
add Q30 for MS/SD LED cost down  
M751 PVT

0618  
Page 24:Change L30,L31,L32 to 33ohm and change C258,C260,C262 to 15PF for SI issue  
Page 25:chang C405 C407 to 1C-2B30475-K100 for PUR request  
Page 33:NC R561,Mount R560 ,keep system ID the same as M750  
Page 36:NC F1 ,mount F3,for 5v Camera moudle  
Page 38:Change R80 to 4.7k from 10k , for FAN speed issue  
Page 40 :NC Q30 ,Mount U39 Q13 C672 C670 R589 for mor Request  
Page 47:NC PR244 ,Vendor suggestion and it is related with DC4  
Page 43,49:1.PR14 change to 62Kohm , co-lay PR248 LMD 86.6Kohm with PR7.  
2.PR215 205Kohm change to 280Kohm  
3.PR223 154Kohm change to 280Kohm  
Page 24: change D17 to 16-SSM24AP-T000' for leakage issue  
Page 7:Change C254,C252 rating to 6.3v for cost down  
Page 35:del R301,R302,R303,R304,R305,R306,L40,L41,L42 for cost down  
Page36:del R147 H150 L28 for cost down  
Page 39:del R261 for cost down,change U14 version  
Page 33:Change CN6 to 1N-0024000-F170 for pur request  
Page 52:add ER4 EC4 for EMI Issue

0625  
Page 43:.PC121 change from 0.1uF/25V to 0.1uF/50V(1C-2B30104-K000)  
Page 52 : change ER4 EC4 to 0603 for EMI request  
Page 40:modify the U33 P/N to 15-BD2056A-FJ00 for CE update component library  
Page 35:resume CN6 main source 1N-0024000-M170, for 2nd source layout issue  
Page 24:change D17 to 16-SSM24PT-0000 For design change  
Page 51:add one test point in PR41 pin1.