Compal Confidential

VIWZ1/VIWZ2 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13P

2012-11-10

LA-9061P

REV:2.A

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Compal confidential
File Name : VIWZ1/VIWZ2

U4 HM76@ PCH-HM76 SA00005FH70

U4 HM70@ PCH-HM70 SA00005MQ80

ZZZ LA9061 DA_PCB DA80000TU2A

VIWZ1
LS9061P PWR/B
LS9062P USB/B

VIWZ2
LS9061P PWR/B
LS9062P USB/B
LS9063P ODD/B
LS9064P LED/B

Page23-32
nVIDIA N13P-GSR
nVIDIA N13P-GLR
VRAM 128*16 DDR3*8

PCI-E x16

Intel
Ivy Bridge
Socket-rPGA988B
37.5mm*37.5mm
Page5-11

DDR3 SO-DIMM *2
BANK 0, 1, 2, 3
Page12-13
Up to 8GB

Dual Channel
DDR3 1066MHz(1.5V)
DDR3 1333MHz(1.5V)
DDR3 1600MHz(1.5V)

100MHz 2.7GT/s
FDI *8
DMI *4

HDMI Connector Page35

CRT Connector Page34

LVDS Connector Page33

LVDS
eDP

Intel
Panther Point
HM70 / HM76
FCBGA 989
25mm*25mm
Page14-22

AZALIA

Audio Codec
Realtek
ALC259-VC2
Page41

2 channel speaker Page41

Int. Digital MIC array (Combine with webcam) Page41

Combo Jack*1 Page43

USB3.0 *1(Left) include USB2.0*1 Page45

USB 3.0
USB2.0

USB2.0 *14

Camera Conn. Page33

BlueTooth Conn. Page40

PCI-E x1 *6

SATA *6

SPIROM BIOS Page14

LPC BUS

EC
ENE KB9012
Page42

Realtek
RTL8111F(GLAN)
RTL8105E-VD(10/100)
Page37

RJ-45 Connector Page38

Card Reader Page44
Reltek
RTS5178 for SDR50
SDXC/MMC

USB2.0 *2(Right)
Page 43

Touch Pad Page43

Int. KBD Page43

Thermal Sensor
EMC1403 Page39

Mini PCIE Half size Slot *1
WLAN Page36

PCI-E(WLAN)

Mini PCIE Full size Slot *1
SSD Page36

SATA HDD Page40

SATA ODD Page40

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	Z-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	Z-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	Z-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	Z-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Reserved	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Reserved	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Reserved	PVT
7	NC	2.500 V	3.300 V	3.300 V	Reserved	MP

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
USB Charger	1010 111X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
USB3.0		1	Touch Screen
	UHCI1	2	Blue Tooth
		3	Camera
EHCI1	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Port (Right Side USB-BD)
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GS&GL	N13P@
OPTIMUS part	OPT@
integrate Graphic part	UMA@
GPU:N13P-GS&GSR	GS@
GPU:N13P-GL&GLR	GL@
GPU:N13P-GS Strap	GS1@
GPU:N13P-GL Strap	GL1@
GPU:N13P-GSR Strap	GSR@
GPU:N13P-GLR Strap	GLR@
OPTIMUS no support GCLK	OPTNOGCLK@
OPTIMUS support GCLK	OPTGCLK@
Support Green CLK	GCLK@
not Support Green CLK	NOGCLK@
Support Green CLK 244	GCLK244@
Support Green CLK 304	GCLK304@
Cardreader	CR@
Support HP Woofer	woofer@
Gastube	Gastube@
EC RESET function	RESET@
HDMI	HDMI@
BlueTooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8105@
GIGA LAN	GIGA@
Deep Sleep S3	DS3@
Not Support Deep Sleep S3	NODS3@
ISCT	AOAC@
ISCT not support	NOAOAC@
Camera	CMOS@
For Z490 (14")	14@
For Z590 (15")	15@
Unpop	@
USB Charger	CHG@
not USBCharger	NOCHG@
Keyboard Back Light	KBL@
Touch Screen	TS@
HM76 by PCH	HM76@
HM70 by PCH	HM70@
Cardreader RTS5178	RTS5178@
Cardreader RTS5170	RTS5170@
for 14" Touch Screen	TS_14@
for 15" Touch Screen	TS_15@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	TP
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	X
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	V +3VS
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	X

GPU BOM Structure Table

BOM Structure	N13P-GS	N13P-GL	N13P-GSR	N13P-GLR
OPT@	V	V	V	V
OPTNOGCLK@	V	V	V	V
N13P@	V	V	V	V
GS@	V		V	
GL@		V		V
GS1@	V			
GL1@		V		
GSR@			V	
GLR@				V

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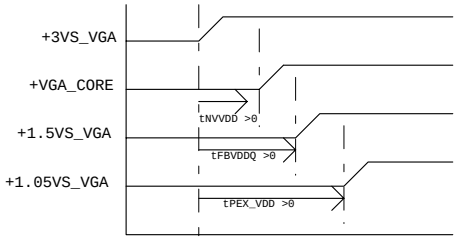
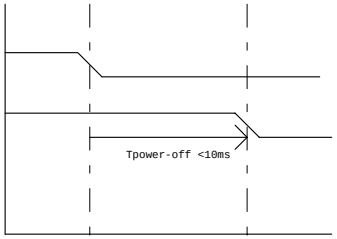
Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

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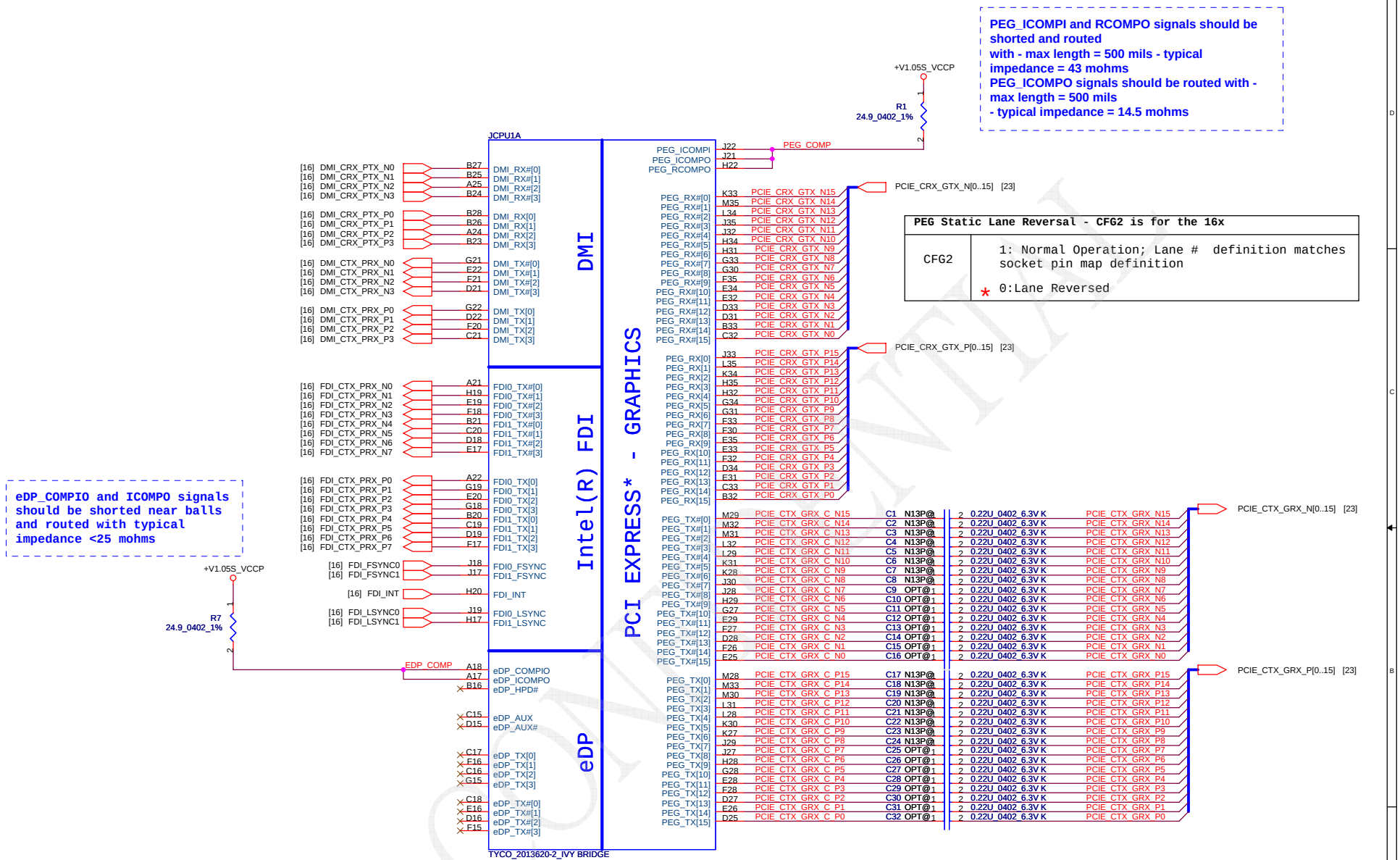

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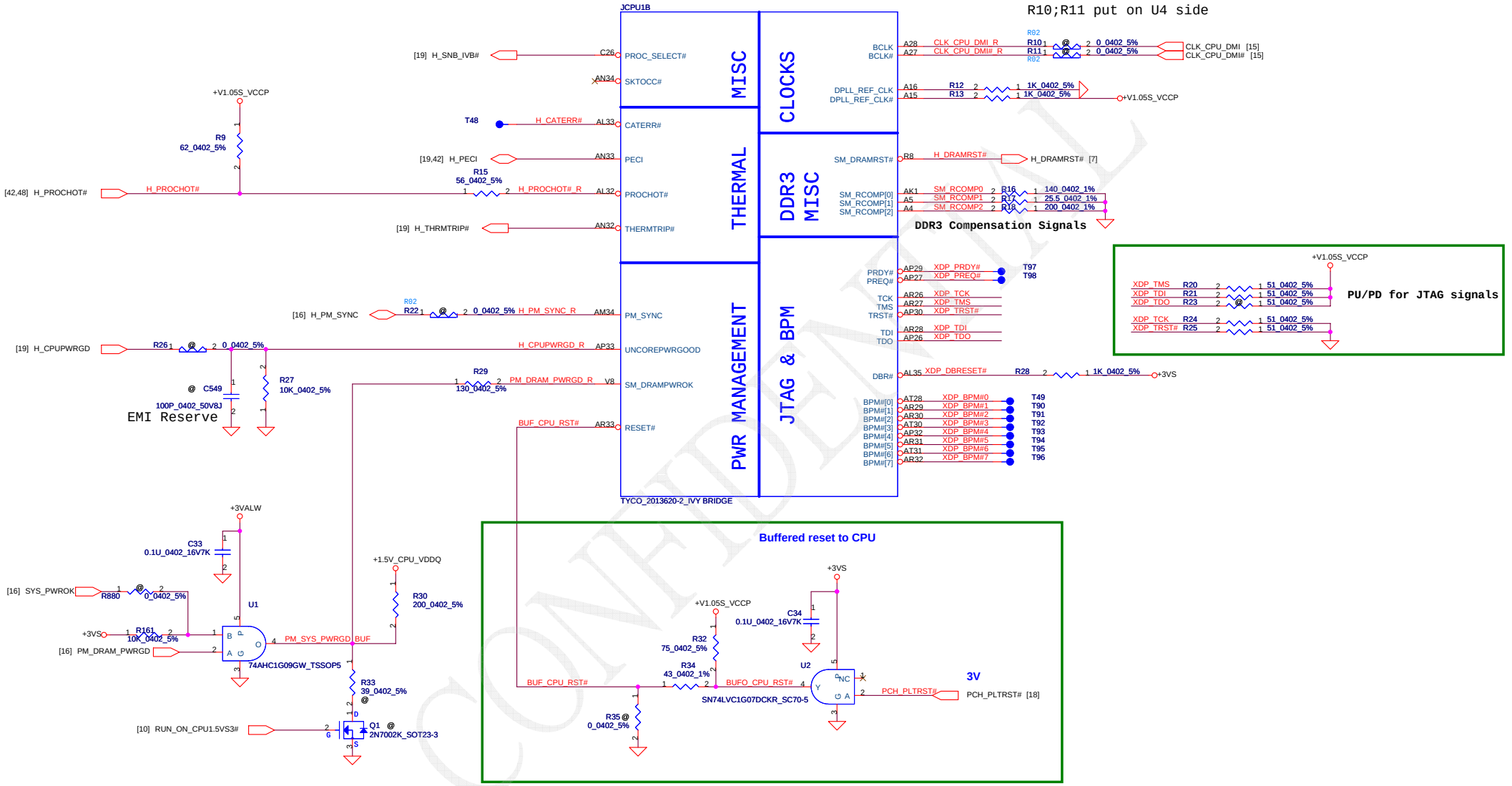

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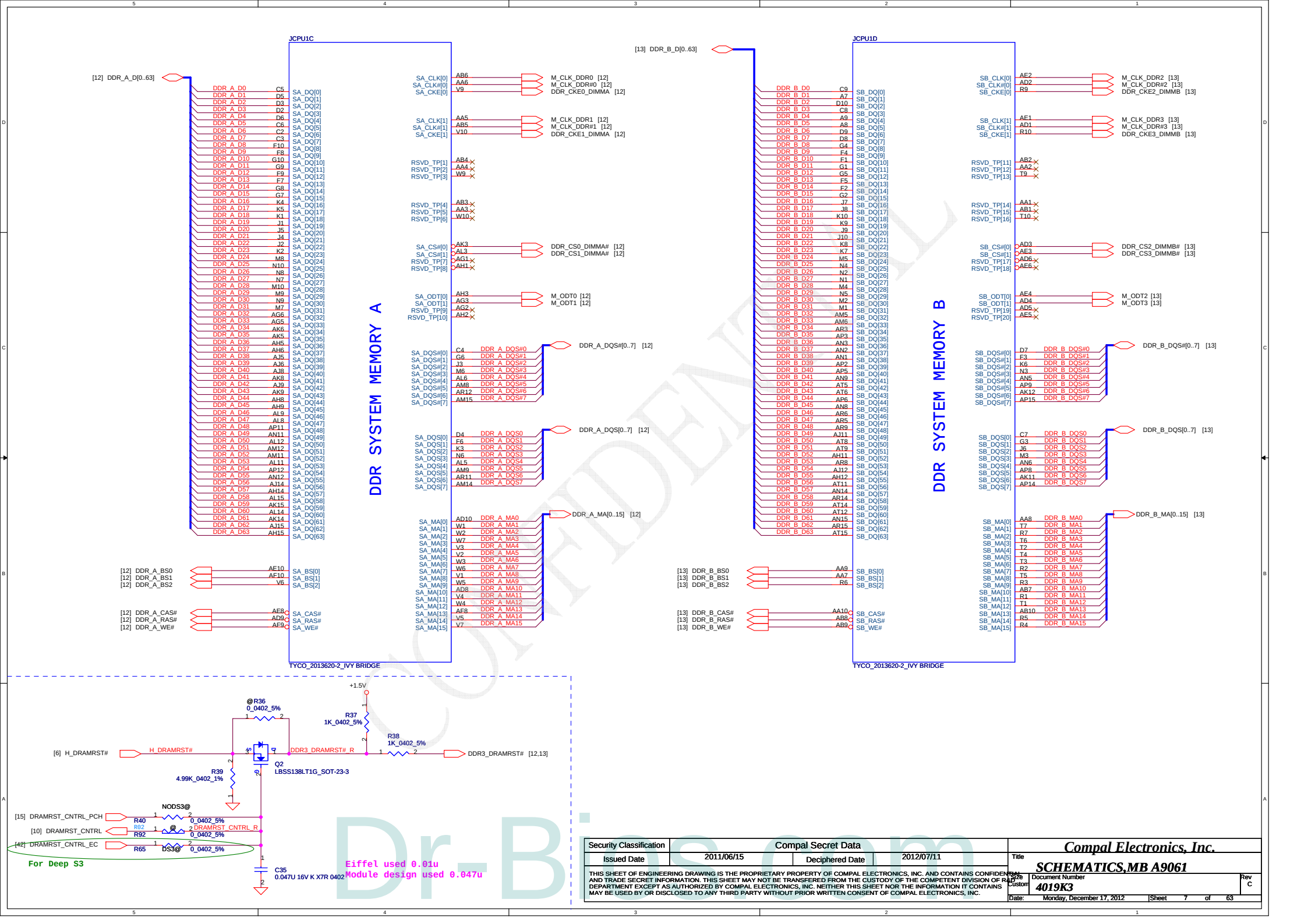

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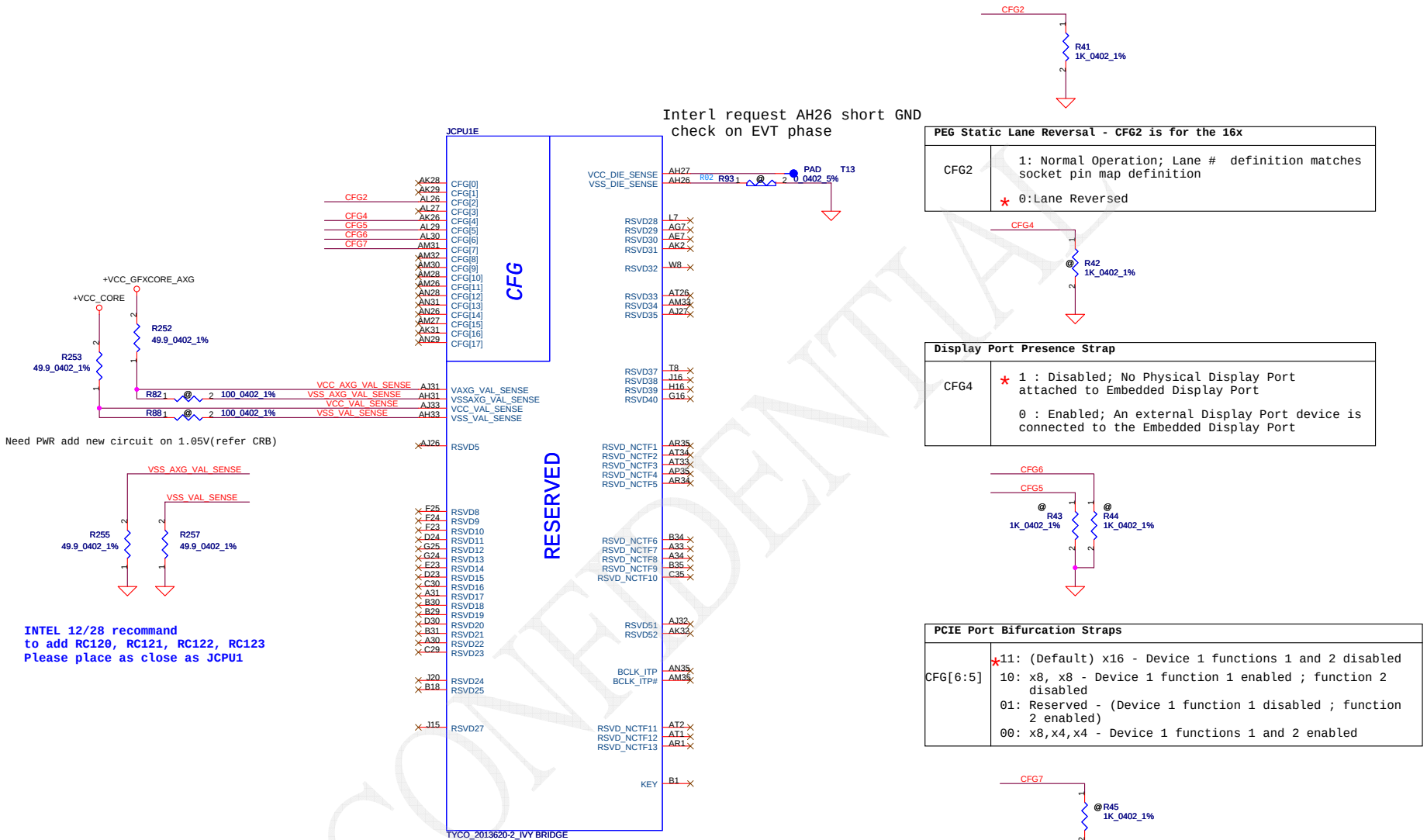
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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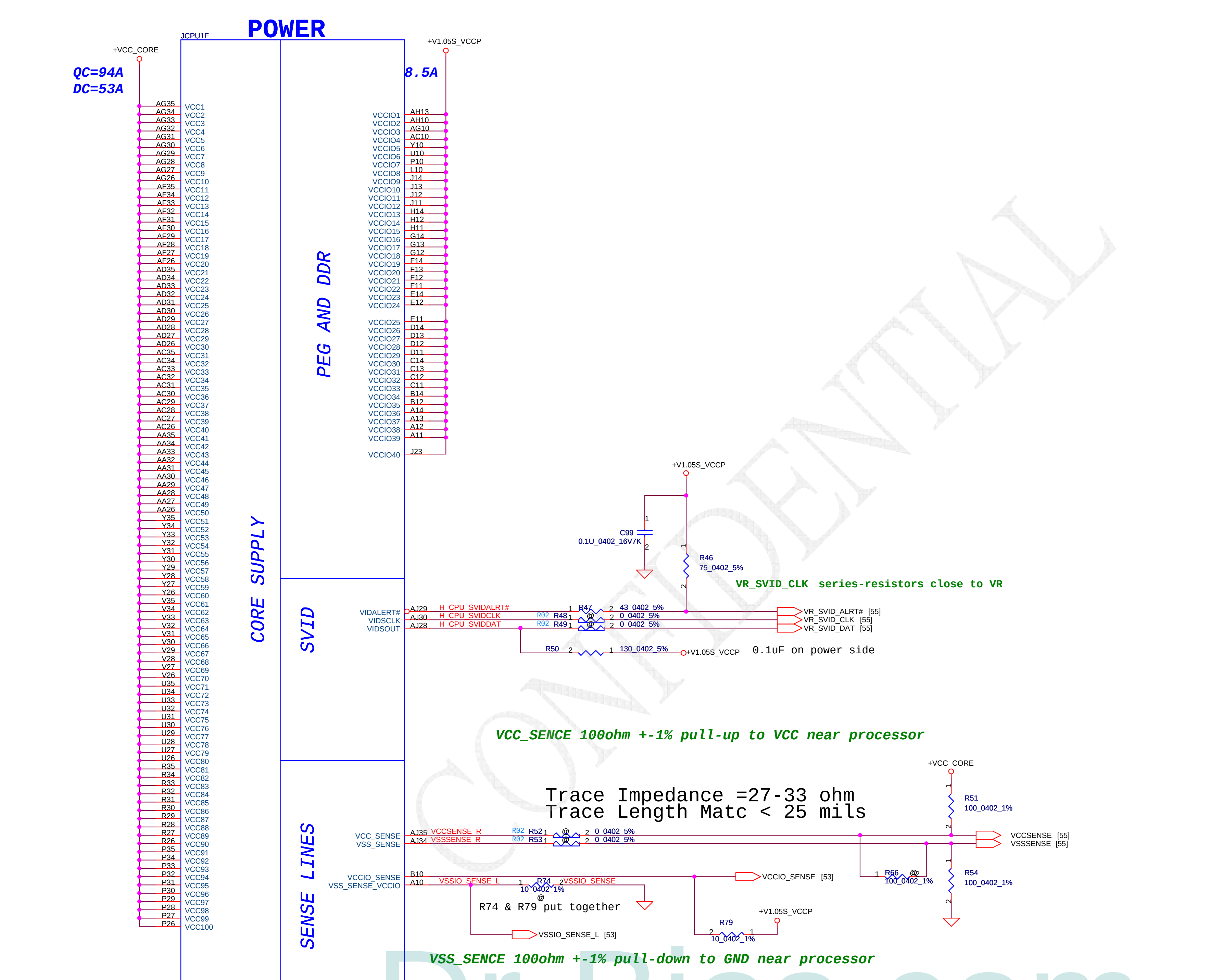

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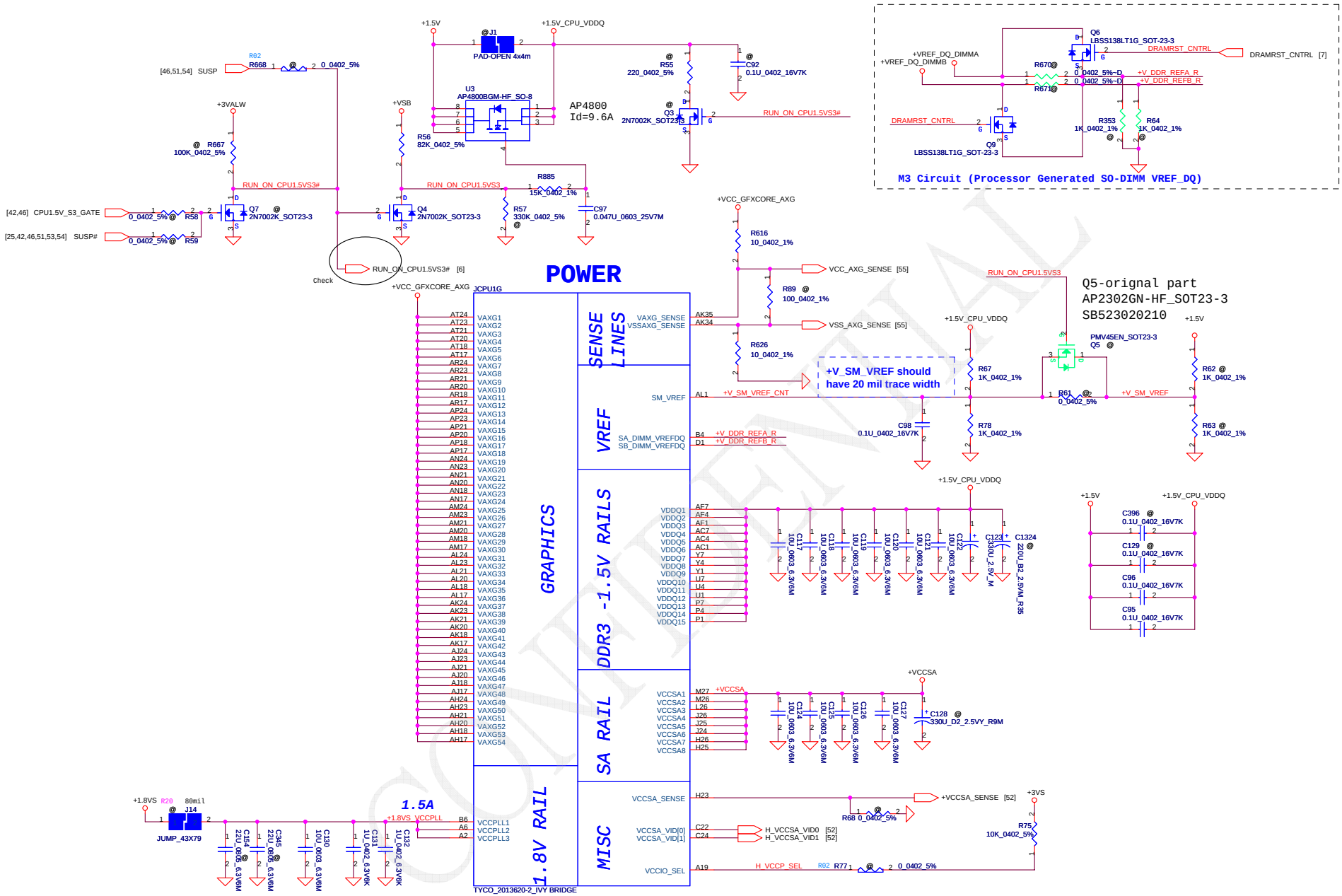

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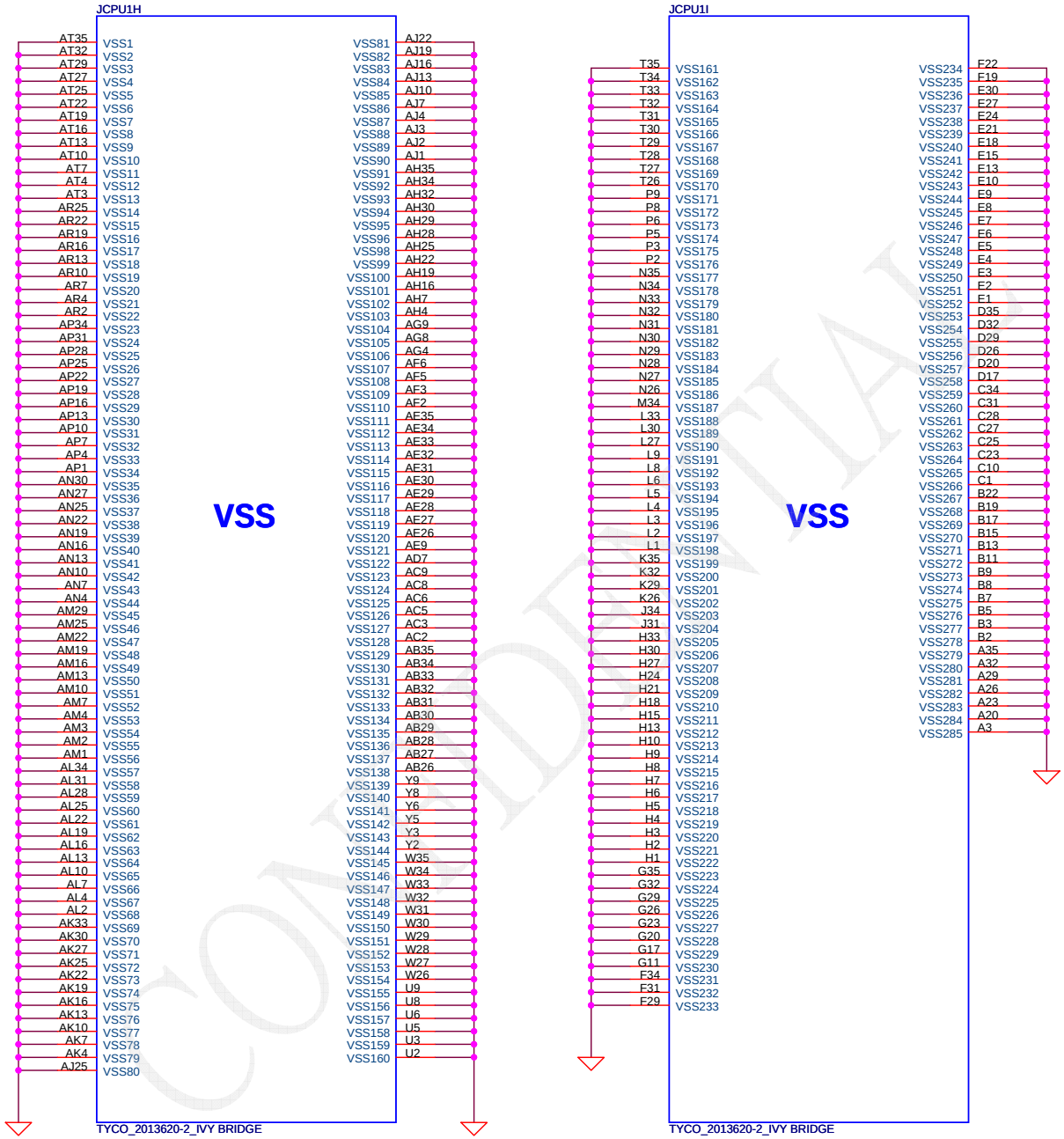

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DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4806-0103

ME@

[7] DDR_A_D[0..63]
[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_MA[0..15]

DDR3_DRAMRST# [13,7]

SMB_DATA_S3 [13,15,36,43]
SMB_CLK_S3 [13,15,36,43]

+0.75VS

0.65A@.75V

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

EVT Check

7/28 Update connect GND directly

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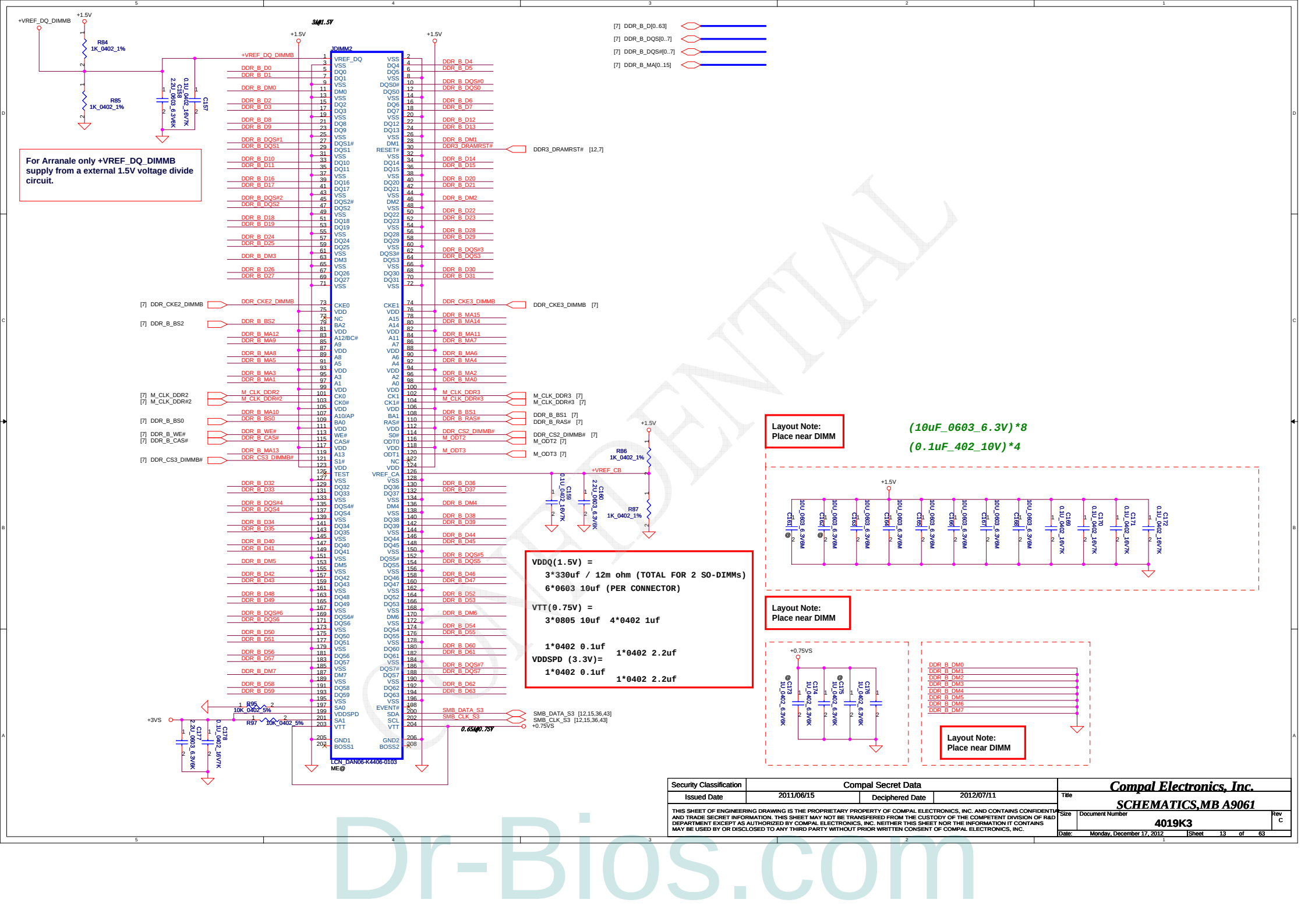

W=20mils
+RTCVCC
R99
1K_0402_5%
C179
1U_0402_6.3V6K
W=20mils
+RTCBATT
CLRP1
SHORT PADS

PCH_RTCX1
R98
10M_0402_5%
NOGCLK@
PCH_RTCX2
Y1
32.768KHZ_12.5PF_CM31532768DZFT
C180
18P_0402_50V8J
NOGCLK@
NOGCLK@
C181
18P_0402_50V8J
NOGCLK@
R02
Remove R176
close to Y1

R182
0_0402_5%
GCLK@
GCLK_32K
GCLK_32K [44]

CMOS
CLRP2
SHORT PADS
CLRP3
SHORT PADS
C183
1U_0402_6.3V6K
R103
20K_0402_5%
R100
20K_0402_5%
C182
1U_0402_6.3V6K

U4A
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
RTC

LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
LDRQ1# / GPIO23
SERIRQ
LPC_AD0 [36,42]
LPC_AD1 [36,42]
LPC_AD2 [36,42]
LPC_AD3 [36,42]
LPC_FRAME# [36,42]
SERIRQ [42]
EC and Mini card debug port

R101
1M_0402_5%
SM_INTRUDER#
R102
330K_0402_5%
PCH_INTVRMEN

INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

R105
1K_0402_5%
HDA_SPKR
HIGH= Enable (No Reboot)
* LOW= Disable (Default)

R106
1K_0402_5%
HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

R108
1K_0402_5%
HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
* 1.8V when sampled low
Needs to be pulled High for Chief River platfrom

HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
IHDA

[41] HDA_SPKR
[41] HDA_SDIN0
[42] ME_FLASH
R109
0_0402_5%
R107
1K_0402_1%
PCH_GPIO33
10K_0402_5%
R264
+3V_PCH

JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG
R110
51_0402_5%

SATA 6G
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA

SATA_ITX_C_DRX_N0
SATA_ITX_C_DRX_P0
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0 [36]
SATA_DTX_C_IRX_P0 [36]
SATA_ITX_C_DRX_N0 [36]
SATA_ITX_C_DRX_P0 [36]
SSD
C184
C185
CAP on Conn, side

SATA_ITX_C_DRX_N1
SATA_ITX_C_DRX_P1
SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
R311
R312
R5593
R5594
SATA_DTX_C_IRX_N1 [40]
SATA_DTX_C_IRX_P1 [40]
SATA_ITX_C_DRX_N1 [40]
SATA_ITX_C_DRX_P1 [40]
HDD
C198
C199
CAP on Conn, side

SATA_DTX_C_IRX_N2
SATA_DTX_C_IRX_P2
SATA_ITX_C_DRX_N2
SATA_ITX_C_DRX_P2
SATA_DTX_C_IRX_N2 [40]
SATA_DTX_C_IRX_P2 [40]
SATA_ITX_C_DRX_N2 [40]
SATA_ITX_C_DRX_P2 [40]
ODD

HM70 Disable SATA Port 1,3

SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_ITX_C_DRX_N1
SATA_ITX_C_DRX_P1
R318
R315
C229
C237
HDD

SATAICOMPO
SATAICOMPI
R111
37.4_0402_1%
+1.05VS_VCC_SATA
SATA_COMP
SATA3RCOMPO
SATA3COMPI
R113
49.9_0402_1%
+1.05VS_SATA3
SATA3_COMP
SATA3RBIAS
RBIAS_SATA3
R115
750_0402_1%

SATALED#
PCH_GPIO21
BBS_BIT0_R
R117
R119
R187
10K_0402_5%
+3VS

PANTHER-POINT_FCBGA989

[41] HDA_BITCLK_AUDIO
[41] HDA_SYNC_AUDIO
[41] HDA_RST_AUDIO#
[41] HDA_SDOUT_AUDIO
R112
R114
R116
R118
33_0402_5%
HDA_BIT_CLK
HDA_SYNC_R
HDA_RST#
HDA_SDOUT

+5VS
Q10
LBSS138LT1G_SOT-23-3
HDA_SYNC
R878
1M_0402_5%
R175
0_0402_5%

SPI_CLK_PCH_R
SPI_SB_CS0#
SPI_SB_CS1#
SPI_SI
SPI_SO_R
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
SPI

check with vender
Del Q10 check with codec
VDDIO using 3VALW

+3V_PCH
R121
R122
R123
200_0402_5%
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAG_TDI
R125
R126
R128
100_0402_1%
DPDG1.1

SPI_CLK_PCH_R
R124
33_0402_5%
C190
22P_0402_50V8J
R124;c190 close to U4.T3 pin

+3VS
R266
R221
R127
R129
3.3K_0402_5%
SPI_WP#1
SPI_HOLD#1
SPI_WP#
SPI_HOLD#

8MB SPI ROM FOR ME
& Non-share ROM.

R02
R291
0_0402_5%
R188
33_0402_5%
SPI_SB_CS1#
SPI_SO_R
SPI_WP#1
SPI_SO1
U6
CS#
SO
WP#
GND
VCC
HOLD#
SCLK
SI
SPI_HOLD#1
SPI_CLK1
SPI_SI1
R199
0_0402_5%
R196
33_0402_5%
SPI_CLK_PCH_R
SPI_SI
16M W25Q16BVSSIG SOIC 8P

U6 Rersver 4M+2M Solution

R130
0_0402_5%
R131
33_0402_5%
SPI_SB_CS0#
SPI_SO_R
SPI_WP#
SPI_SO_L
U5
W25Q32BVSSIG_SO8
C191
0.1U_0402_16V7K
R132
0_0402_5%
R133
33_0402_5%
SPI_HOLD#
SPI_CLK_PCH
SPI_SI_R

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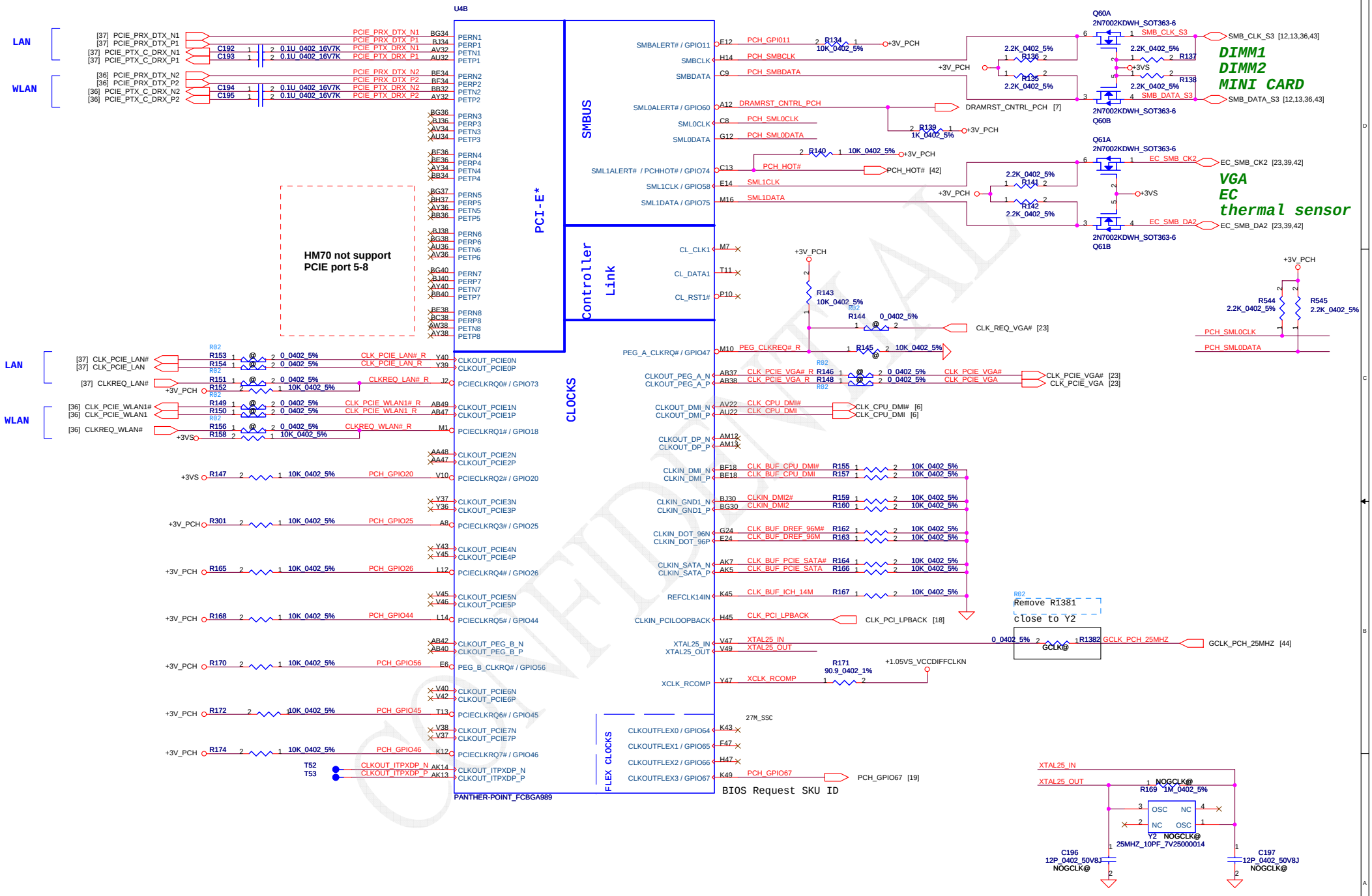

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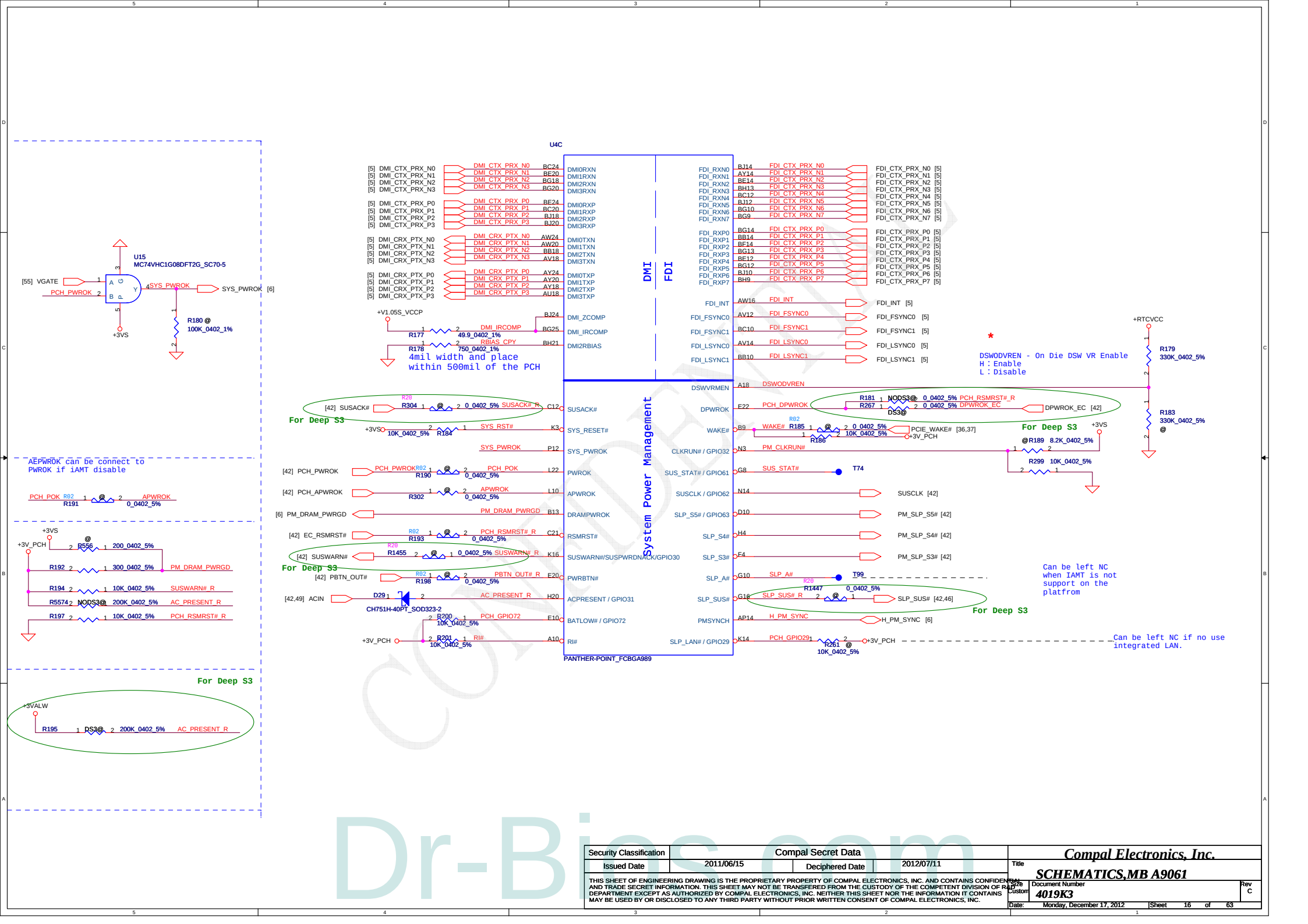

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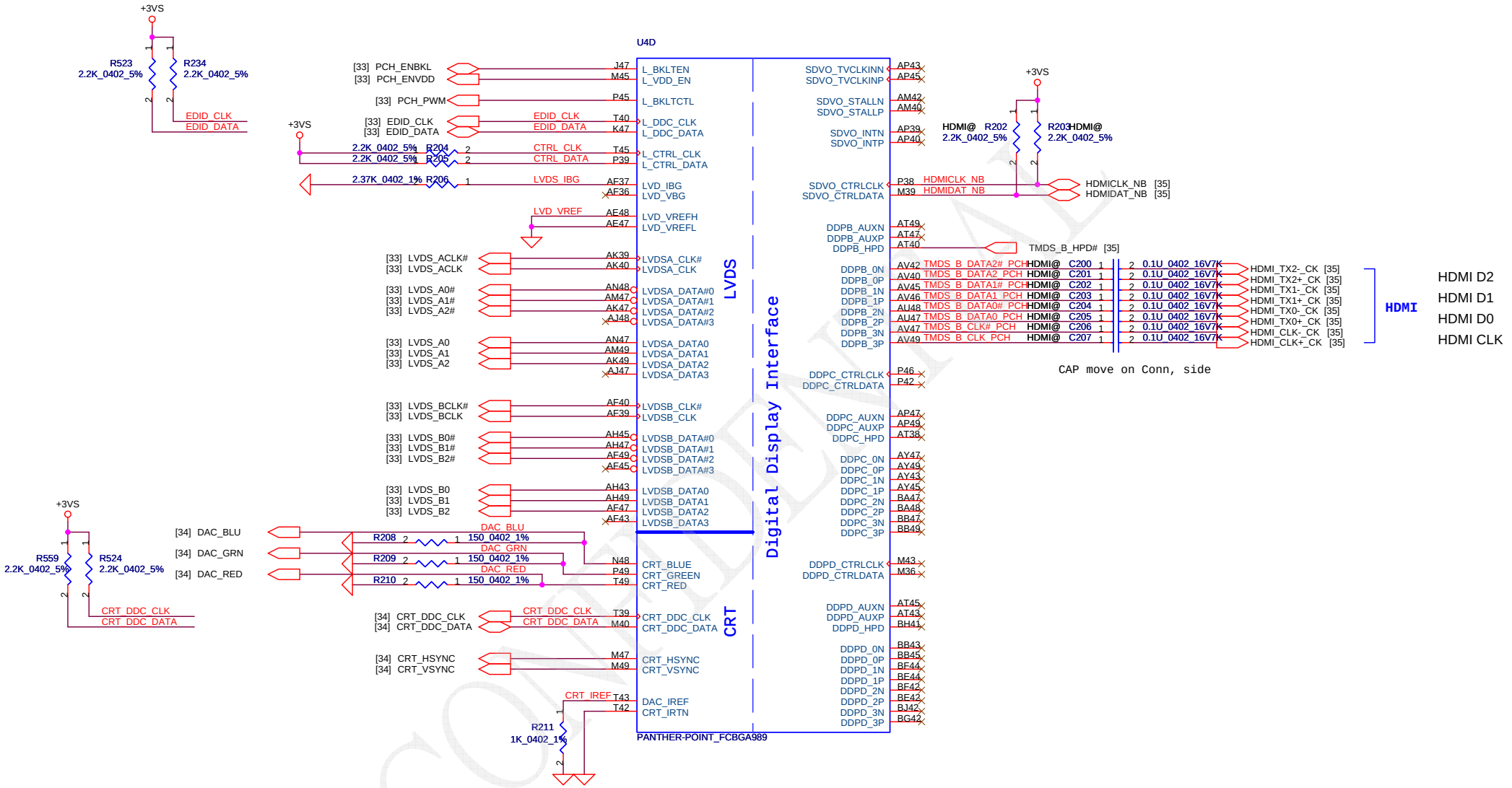

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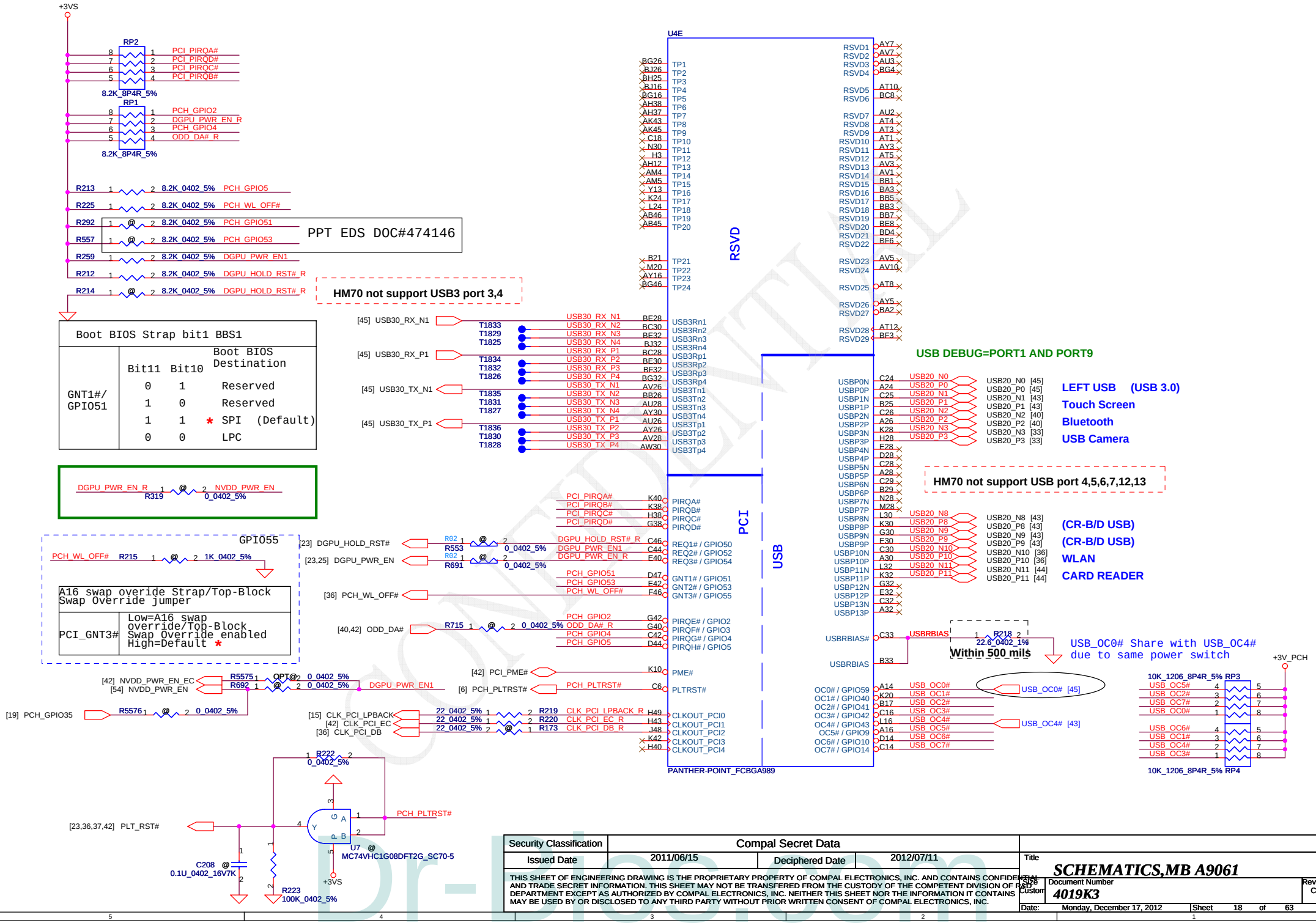

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PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

PCH_GPIO70	Function
0	14/15"
1	17"

+3V_PCH — Weak internal pull-high — R235 10K_0402_5% — EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 @ 1K_0402_5% PCH_GPIO28

* Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27

PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
For DS3

+3VALW — DS3@ R5530 10K_0402_5% — R245 @ 10K_0402_5% PCH_GPIO27

[46,54] DGPU_PWROK
PU on power side
[36] BT_DISABLE

[42] EC_WAKE# — EC_WAKE# R262 @ 0_0402_5% PCH_GPIO27

[36,40] PCH_BT_ON# — R241 10K_0402_5% PCH_GPIO28 — R242 10K_0402_5% PCH_BT_ON#

[18] PCH_GPIO35 — R243 10K_0402_5% PCH_GPIO35

[36] INTEL_BT_OFF# — INTEL_BT_OFF# V8

R244 @ 10K_0402_5% PCH_GPIO37 — R881 10K_0402_5%
R250 @ 10K_0402_5% INTEL_BT_OFF# — R547 10K_0402_5%

BIOS Request SKU ID

R711 UMA@ 10K_0402_5% — R246 10K_0402_5% UMA@
PCH_GPIO38
PCH_GPIO67 — PCH_GPIO67 [15]
OPT@ R709 10K_0402_5% — R295 10K_0402_5% OPT@

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
1	1	UMA

U4F

GPIO:
BMBUSY# / GPIO0 — T7 — PCH_GPIO0
TACH1 / GPIO1 — A42 — PCH_GPIO1
TACH2 / GPIO6 — H36 — PCH_GPIO6
TACH3 / GPIO7 — E38 — EC_SCI# [42]
GPIO8 — C10 — EC_SMI# [42]
LAN_PHY_PWR_CTRL / GPIO12 — C4 — PCH_GPIO12
GPIO15 — G2 — EC_LID_OUT# [42]
SATA4GP / GPIO16 — U2 — mSATA_DET# [36]
TACH0 / GPIO17 — D40 — DGPU_PWROK_R
SCLOCK / GPIO22 — T5 — BT_DISABLE
GPIO24 — E8 — ODD_EN [40]
GPIO27 — E16 — PCH_GPIO27
GPIO28 — P8 — PCH_GPIO28
STP_PCI# / GPIO34 — K1 — PCH_BT_ON#
GPIO35 — K4 — PCH_GPIO35
SATA2GP / GPIO36 — V8 — INTEL_BT_OFF# [36]
SATA3GP / GPIO37 — M5 — PCH_GPIO37
SLOAD / GPIO38 — N2 — PCH_GPIO38
SDATAOUT0 / GPIO39 — M3 — PCH_GPIO39
SDATAOUT1 / GPIO48 — V13 — PCH_GPIO48
SATA5GP / GPIO49 / TEMP_ALERT# — V3 — PCH_GPIO49
GPIO57 — D6 — PCH_GPIO57

CPU/MISC:
TACH4 / GPIO68 — C40 — PCH_GPIO68 — R224 10K_0402_5% +3VS
TACH5 / GPIO69 — B41 — PCH_GPIO69
TACH6 / GPIO70 — C41 — PCH_GPIO70
TACH7 / GPIO71 — A40 — PCH_GPIO71 — R704 10K_0402_5% +3VS
A20GATE — P4 — R236 10K_0402_5% +3VS — GATEA20 [42]
PECI — AU16 — PCH_PECI_R — R237 @ 0_0402_5% — H_PECI [42,6]
RCIN# — P5 — KBRST# — KBRST# [42]
PROCPWRGD — AY11 — H_CPUPWRGD [6]
THRMTRIP# — AY10 — PCH_THRMTRIP#_R — R239 390_0402_5% — H_THRMTRIP# [6]
INIT3_3V# — T14
DF_TVS — AY1 — PCH_THRMTRIP#_R [23]
TS_VSS1 — AH8
TS_VSS2 — AK11
TS_VSS3 — AH10
TS_VSS4 — AK10
NC_1 — P37 — NV_CLE — R217 1K_0402_5% — R216 2.2K_0402_5% +1.8VS — H_SNB_IVB# [6]

KBRST# — R226 10K_0402_5% +3VS

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

Weak internal PU,Do not pull low

CLOSE TO THE BRANCHING POINT

NCTF:
VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49
VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

PANTHER-POINT_FCBGA989

HM70@ R702 10K_0402_5% — PCH_GPIO69 — R707 HM76@ 10K_0402_5%
17@ R703 10K_0402_5% — PCH_GPIO70 — R705 200K_0402_5%

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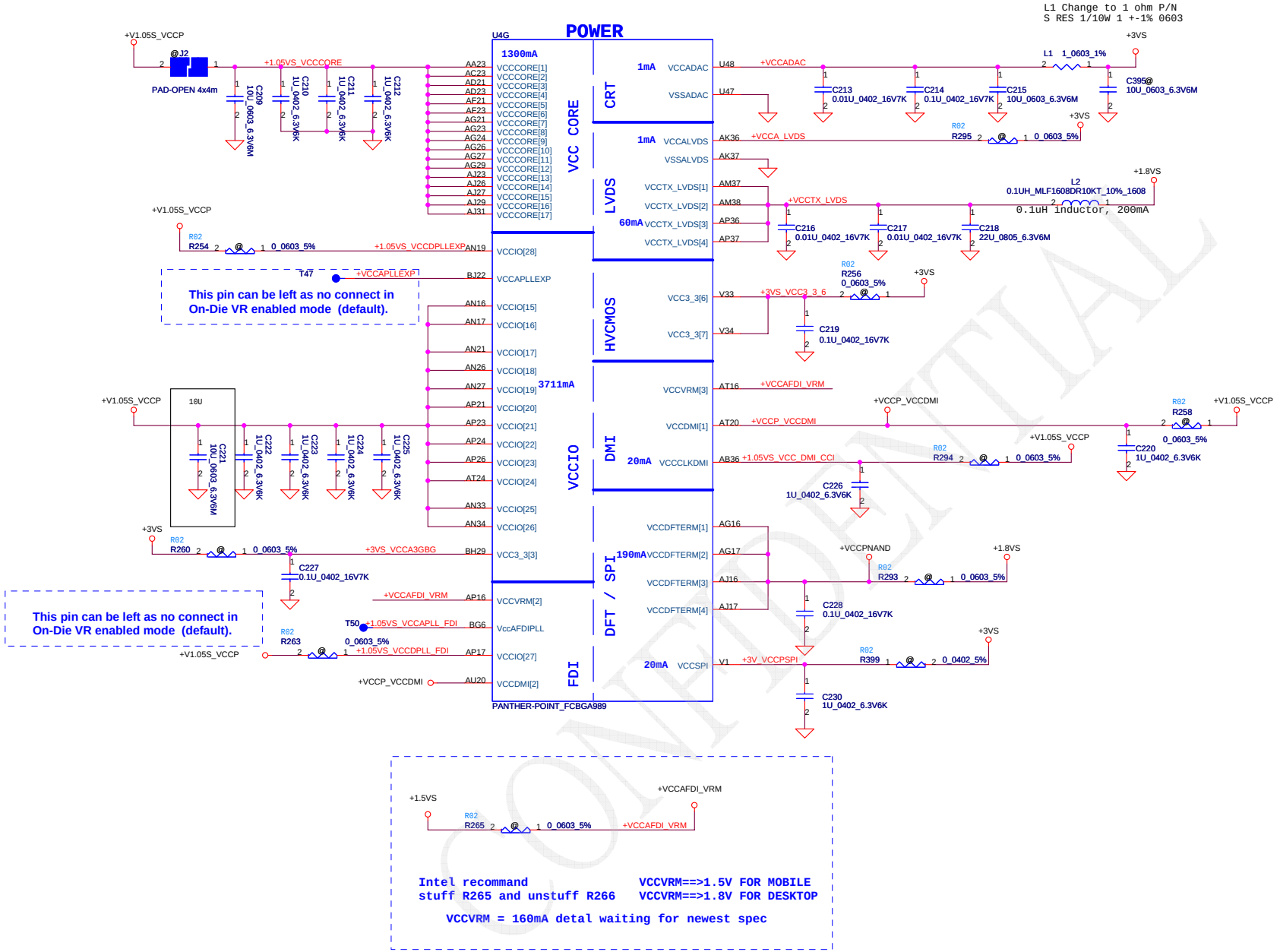

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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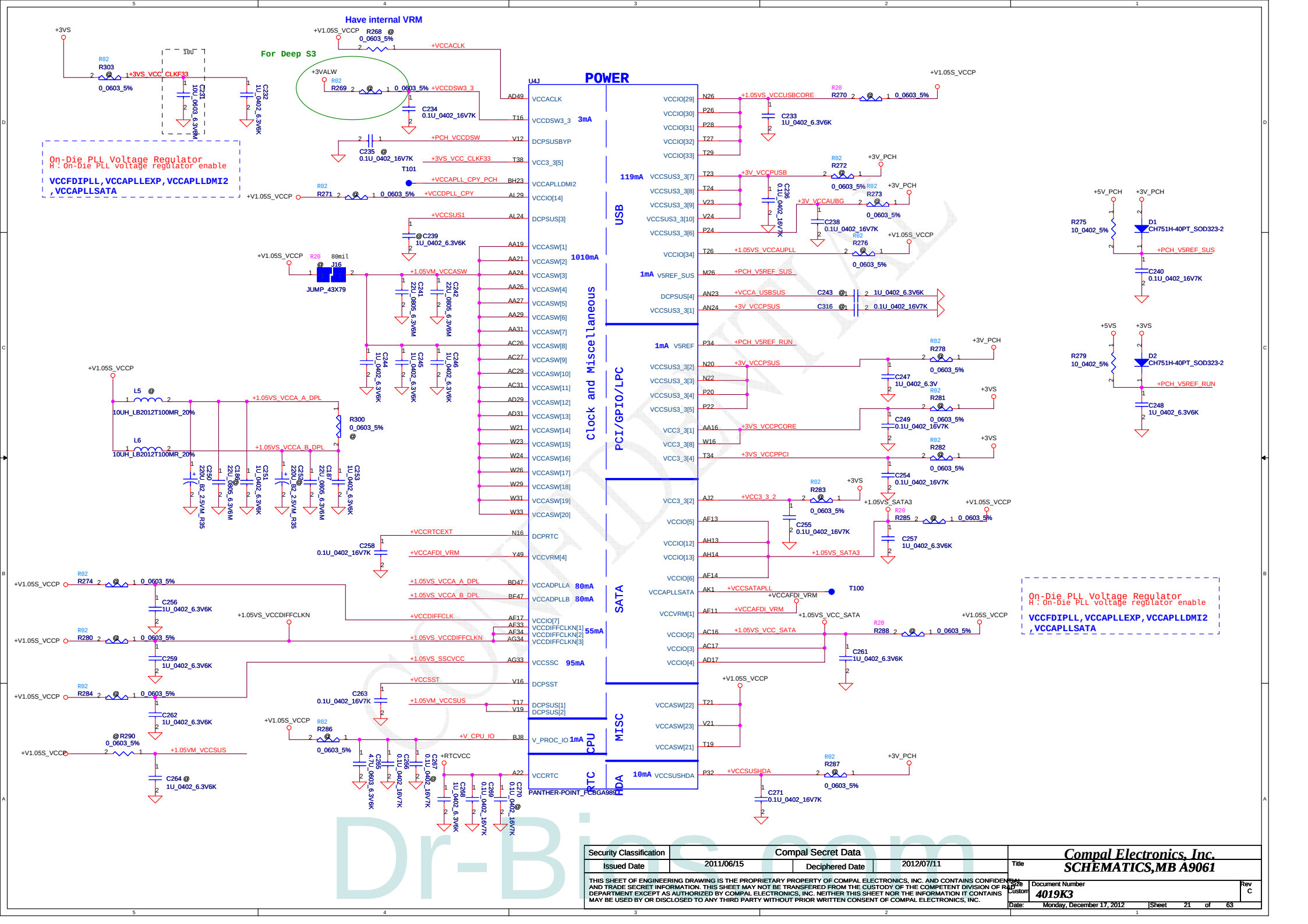

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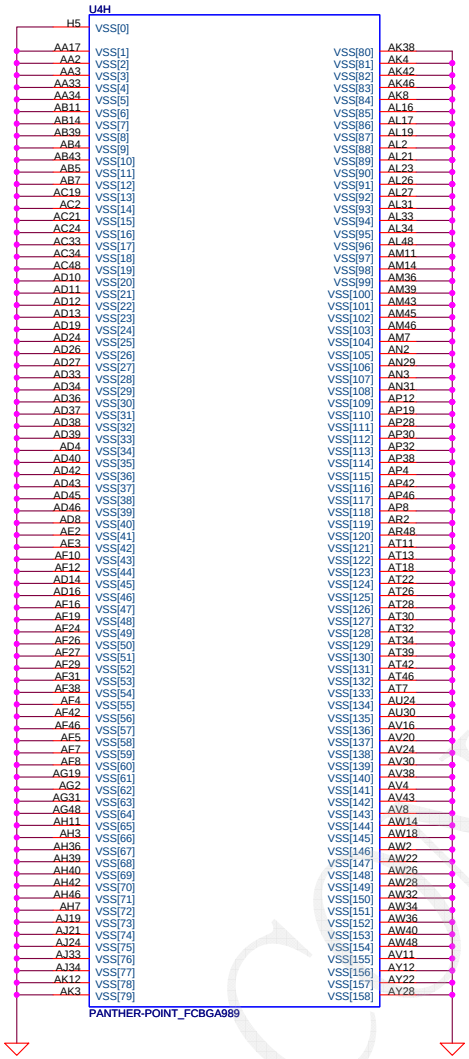

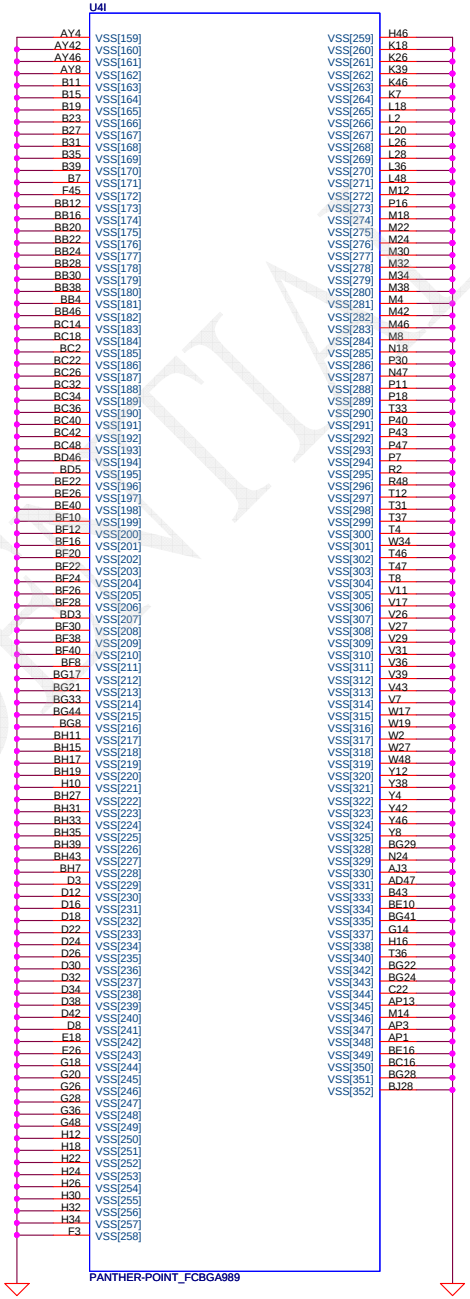

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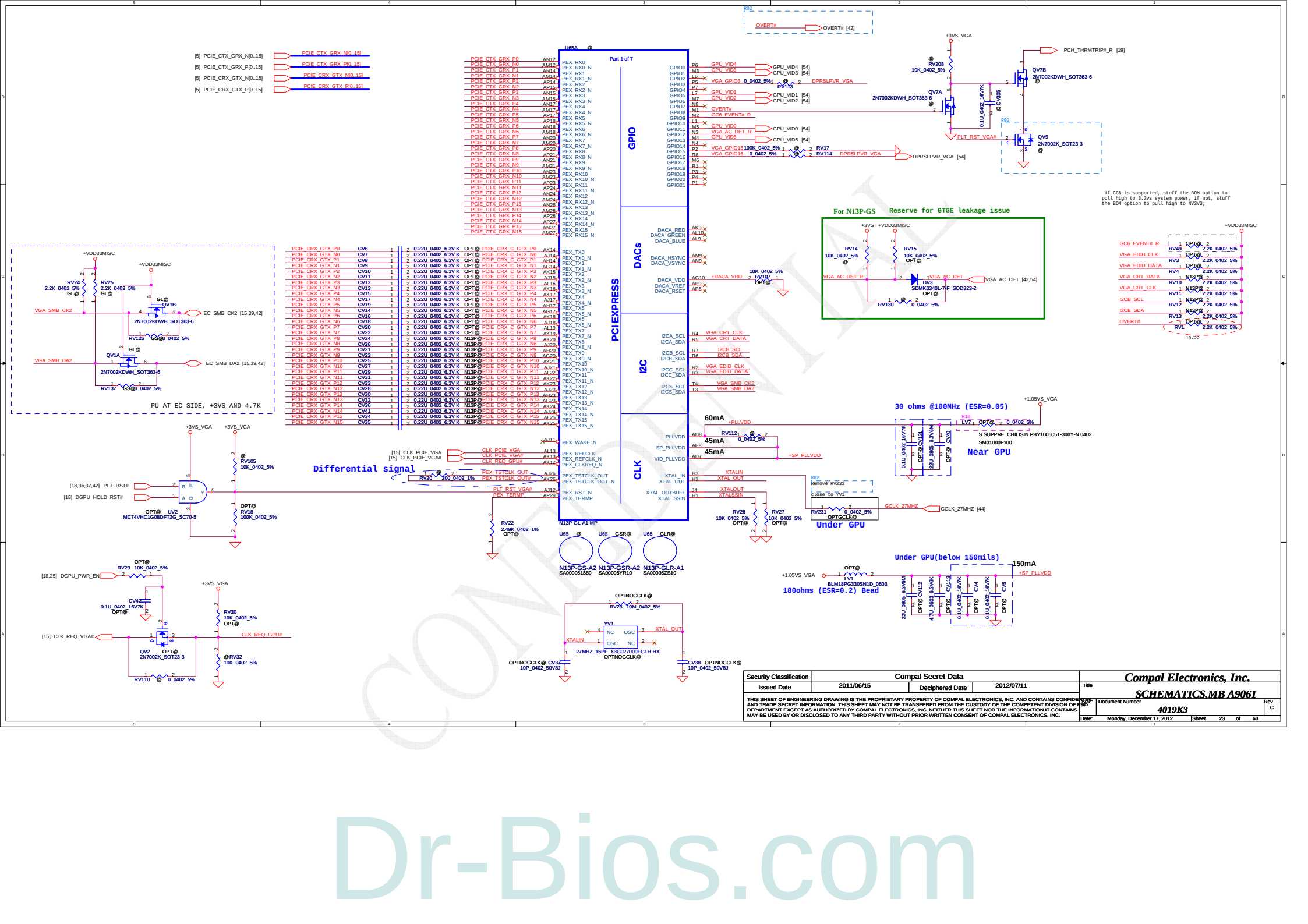
PCIE_CTX_GRX_N[0..15]
PCIE_CTX_GRX_P[0..15]
PCIE_CRX_GTX_N[0..15]
PCIE_CRX_GTX_P[0..15]
U65A
Part 1 of 7
PCI EXPRESS
GPIO
DACs
I2C
CLK
PEX_RX0
PEX_RX0_N
PEX_RX1
PEX_RX1_N
PEX_RX2
PEX_RX2_N
PEX_RX3
PEX_RX3_N
PEX_RX4
PEX_RX4_N
PEX_RX5
PEX_RX5_N
PEX_RX6
PEX_RX6_N
PEX_RX7
PEX_RX7_N
PEX_RX8
PEX_RX8_N
PEX_RX9
PEX_RX9_N
PEX_RX10
PEX_RX10_N
PEX_RX11
PEX_RX11_N
PEX_RX12
PEX_RX12_N
PEX_RX13
PEX_RX13_N
PEX_RX14
PEX_RX14_N
PEX_RX15
PEX_RX15_N
PEX_TX0
PEX_TX0_N
PEX_TX1
PEX_TX1_N
PEX_TX2
PEX_TX2_N
PEX_TX3
PEX_TX3_N
PEX_TX4
PEX_TX4_N
PEX_TX5
PEX_TX5_N
PEX_TX6
PEX_TX6_N
PEX_TX7
PEX_TX7_N
PEX_TX8
PEX_TX8_N
PEX_TX9
PEX_TX9_N
PEX_TX10
PEX_TX10_N
PEX_TX11
PEX_TX11_N
PEX_TX12
PEX_TX12_N
PEX_TX13
PEX_TX13_N
PEX_TX14
PEX_TX14_N
PEX_TX15
PEX_TX15_N
PEX_WAKE_N
PEX_REFCLK
PEX_REFCLK_N
PEX_CLKREQ_N
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
PEX_RST_N
PEX_TERMP
N13P-GL-A1 MP
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPU_VID4
GPU_VID3
VGA_GPIO3
GPU_VID1
GPU_VID2
OVERT#
GC6_EVENT#_R
GPU_VID0
VGA_AC_DET_R
GPU_VID5
VGA_GPIO15
VGA_GPIO16
DPRSLPVR_VGA
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA
VGA_CRT_CLK
VGA_CRT_DATA
VGA_EDID_CLK
VGA_EDID_DATA
VGA_SMB_CK2
VGA_SMB_DA2
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTALIN
XTAL_OUT
XTALOUT
XTALSSIN
XTAL_OUTBUFF
XTAL_SSIN
PCIE_CRX_GTX_P0 CV6
PCIE_CRX_GTX_N0 CV7
PCIE_CRX_GTX_P1 CV8
PCIE_CRX_GTX_N1 CV9
PCIE_CRX_GTX_P2 CV10
PCIE_CRX_GTX_N2 CV11
PCIE_CRX_GTX_P3 CV12
PCIE_CRX_GTX_N3 CV13
PCIE_CRX_GTX_P4 CV15
PCIE_CRX_GTX_N4 CV17
PCIE_CRX_GTX_P5 CV19
PCIE_CRX_GTX_N5 CV14
PCIE_CRX_GTX_P6 CV16
PCIE_CRX_GTX_N6 CV18
PCIE_CRX_GTX_P7 CV20
PCIE_CRX_GTX_N7 CV22
PCIE_CRX_GTX_P8 CV24
PCIE_CRX_GTX_N8 CV26
PCIE_CRX_GTX_P9 CV21
PCIE_CRX_GTX_N9 CV23
PCIE_CRX_GTX_P10 CV25
PCIE_CRX_GTX_N10 CV27
PCIE_CRX_GTX_P11 CV29
PCIE_CRX_GTX_N11 CV31
PCIE_CRX_GTX_P12 CV33
PCIE_CRX_GTX_N12 CV28
PCIE_CRX_GTX_P13 CV30
PCIE_CRX_GTX_N13 CV32
PCIE_CRX_GTX_P14 CV36
PCIE_CRX_GTX_N14 CV41
PCIE_CRX_GTX_P15 CV34
PCIE_CRX_GTX_N15 CV35
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_P0
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_N0
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_P1
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_N1
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_P2
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_N2
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_P3
0.22U 0402 6.3V K OPT@ PCIE_CRX_C_GTX_N3
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P4
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N4
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P5
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N5
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P6
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N6
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P7
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N7
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P8
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N8
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P9
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N9
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P10
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N10
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P11
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N11
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P12
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N12
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P13
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N13
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P14
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N14
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_P15
0.22U 0402 6.3V K N13P@ PCIE_CRX_C_GTX_N15
PU AT EC SIDE, +3VS AND 4.7K
Differential signal
For N13P-GS
Reserve for GTGE leakage issue
if GC6 is supported, stuff the BOM option to pull high to 3.3vs system power, if not, stuff the BOM option to pull high to NV3V3;
60mA
45mA
45mA
30 ohms @100MHz (ESR=0.05)
Near GPU
Under GPU
Under GPU(below 150mils)
150mA
180ohms (ESR=0.2) Bead
N13P-GS-A2 SA00005188O
N13P-GSR-A2 SA00005YR10
N13P-GLR-A1 SA00005ZS10
Security Classification
Compal Secret Data
Issued Date
2011/06/15
Deciphered Date
2012/07/11
Compal Electronics, Inc.
SCHEMATICS,MB A9061
4019K3
Rev C
Monday, December 17, 2012
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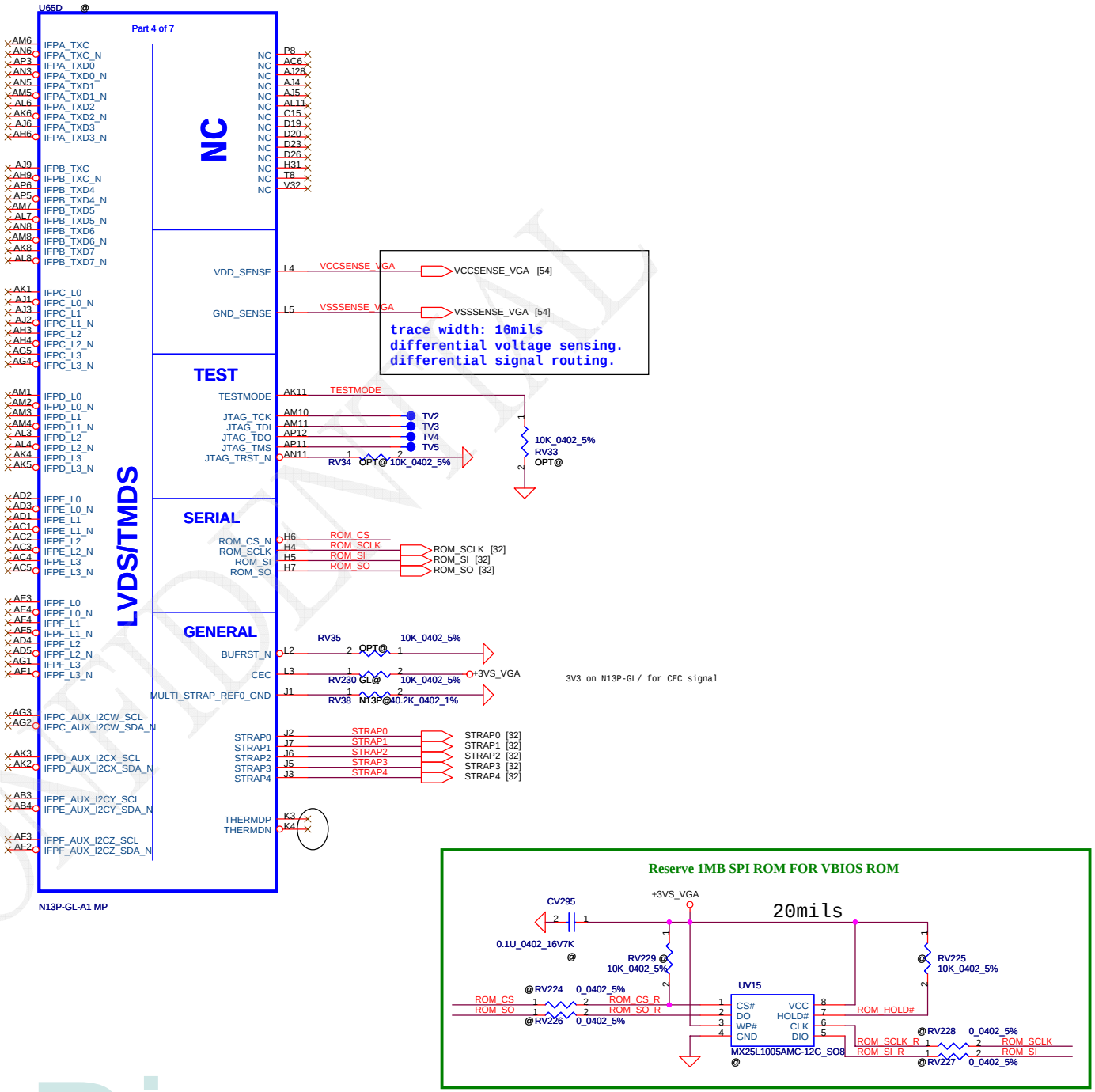

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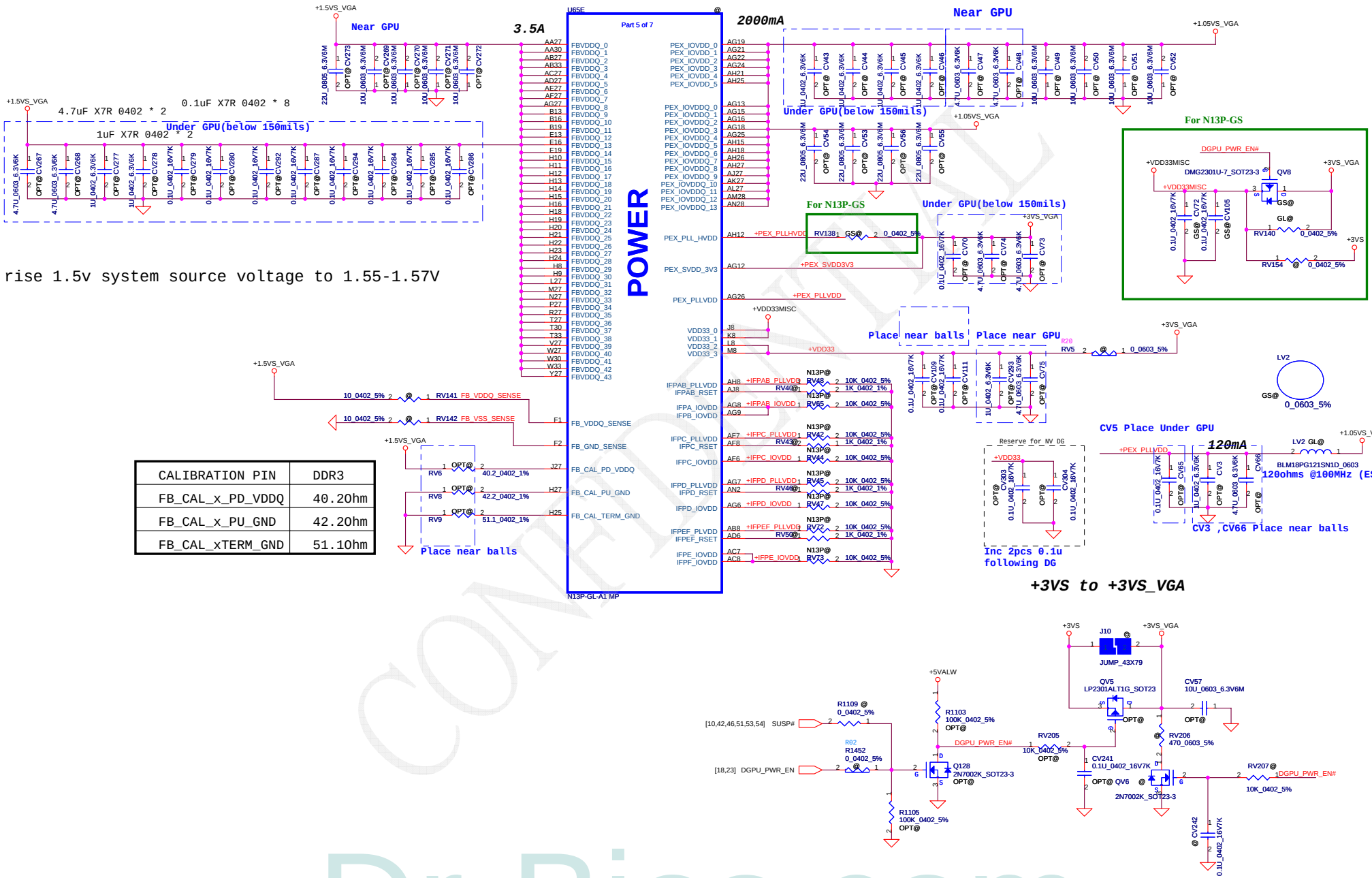

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

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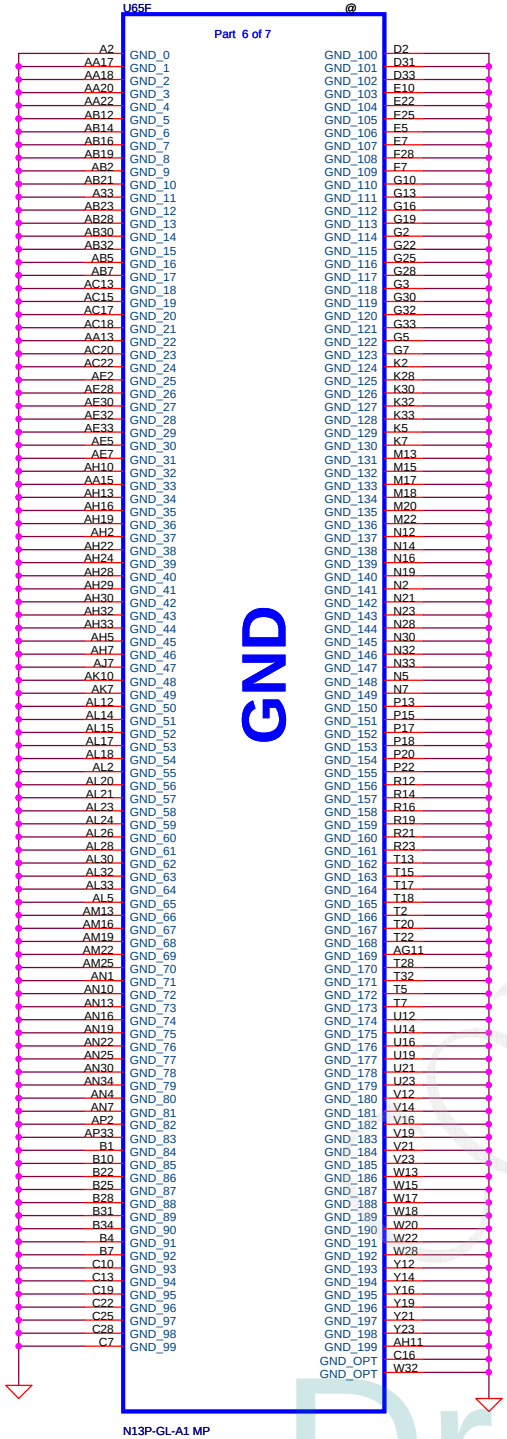

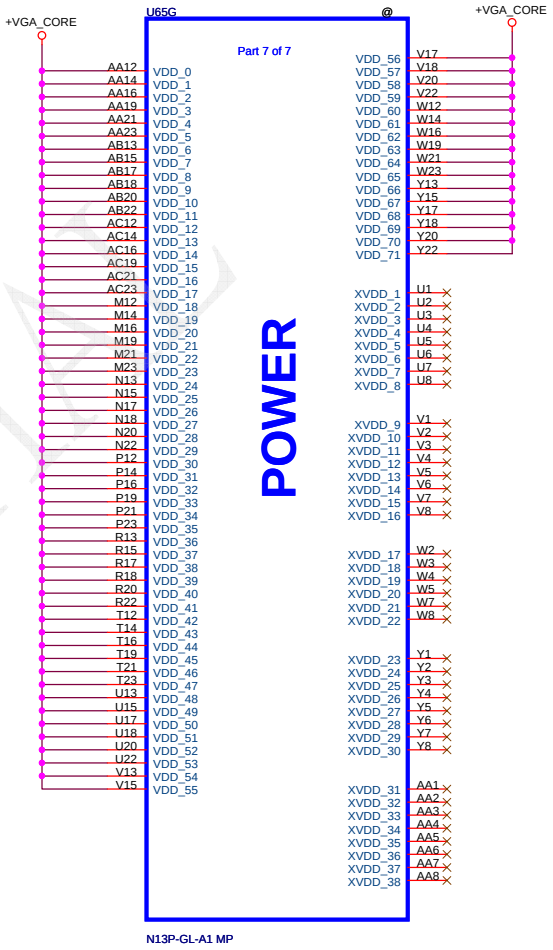

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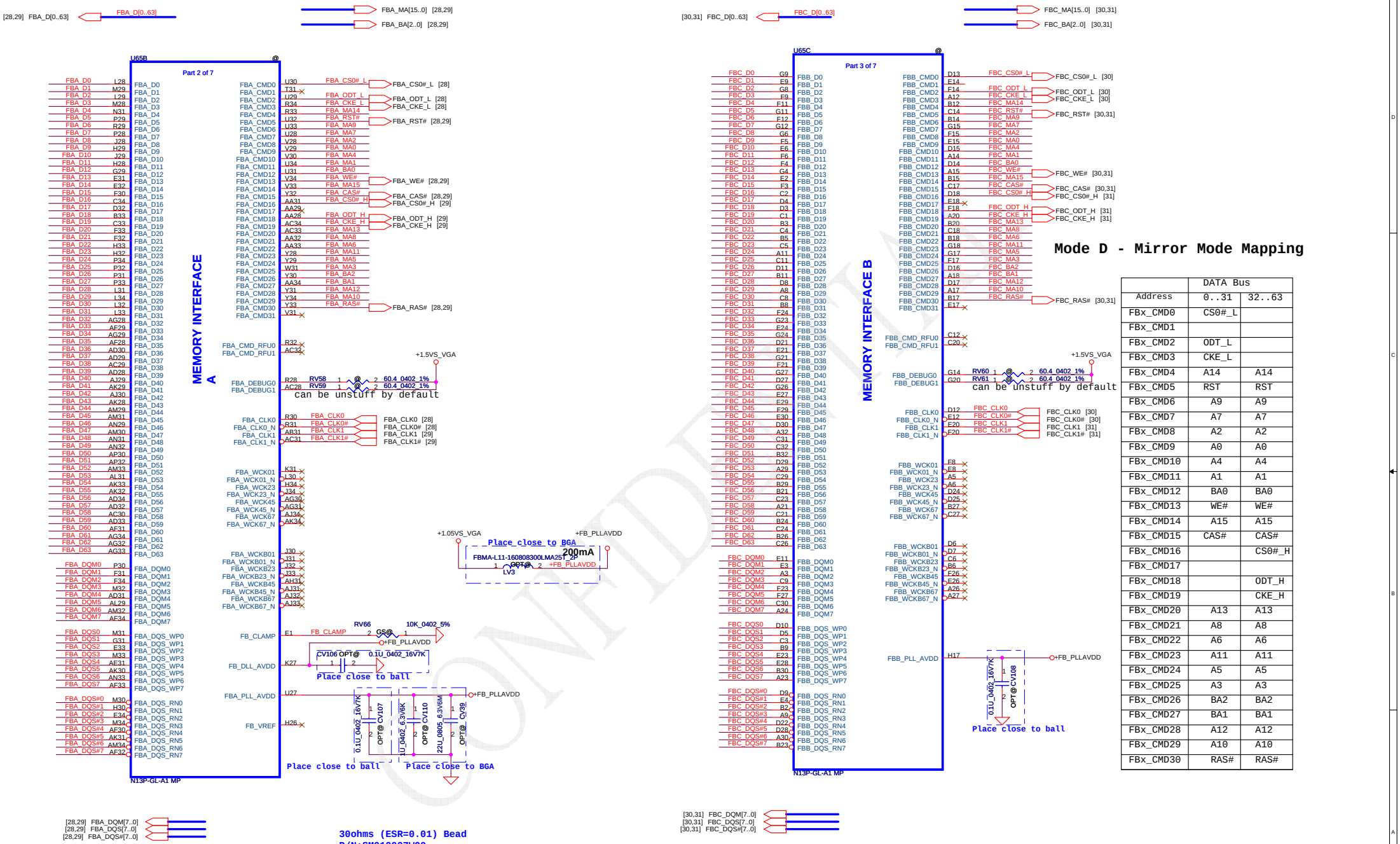

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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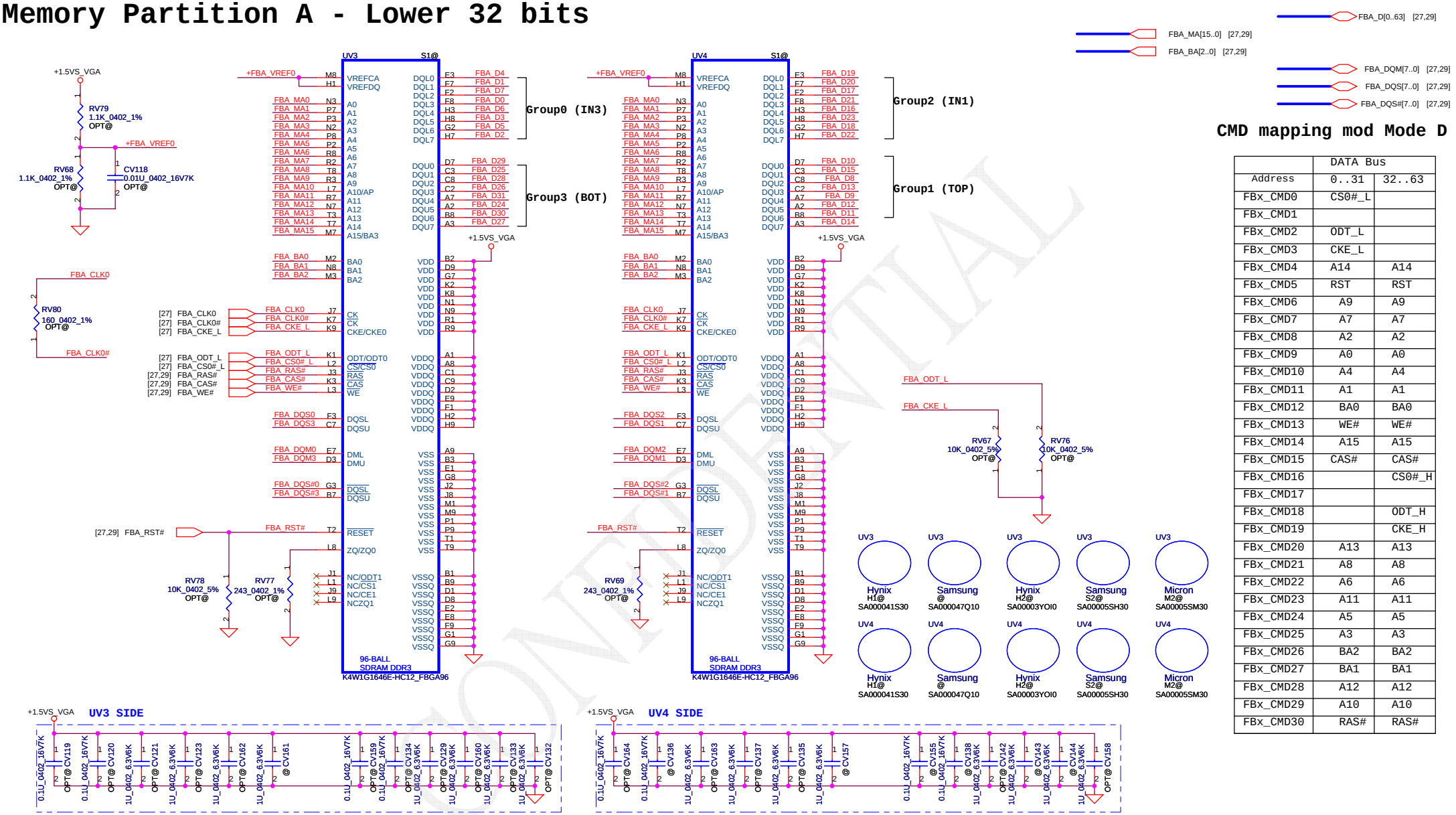
Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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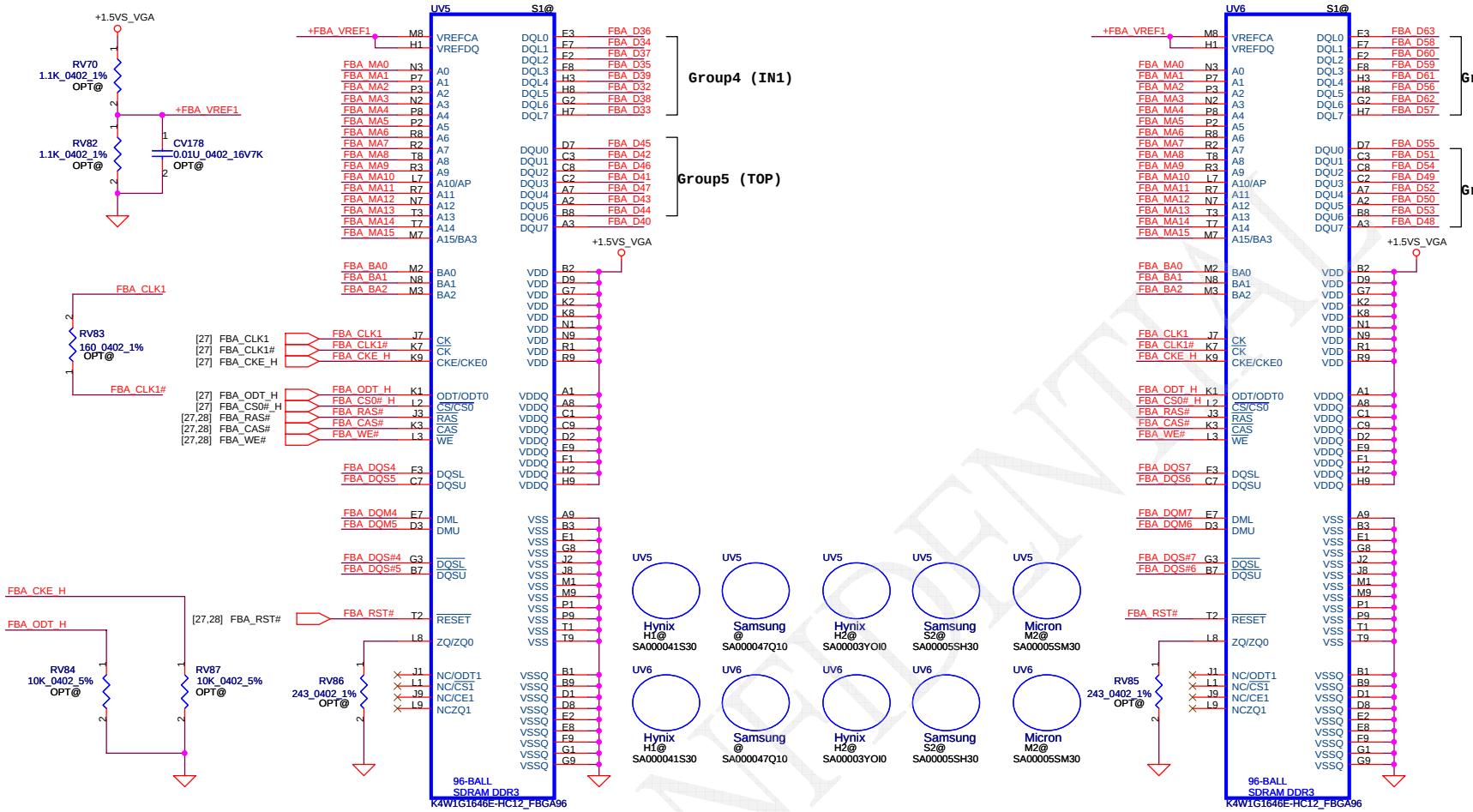
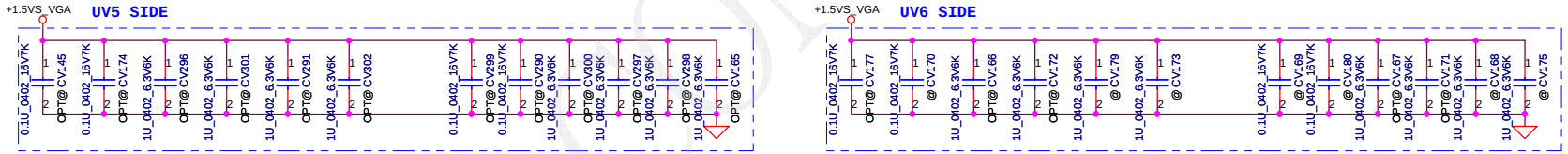
Memory Partition A - Upper 32 bits





FBA_D[0..63] [27,28]
FBA_MA[15..0] [27,28]
FBA_BA[2..0] [27,28]
FBA_DQM[7..0] [27,28]
FBA_DQS[7..0] [27,28]
FBA_DQS#[7..0] [27,28]

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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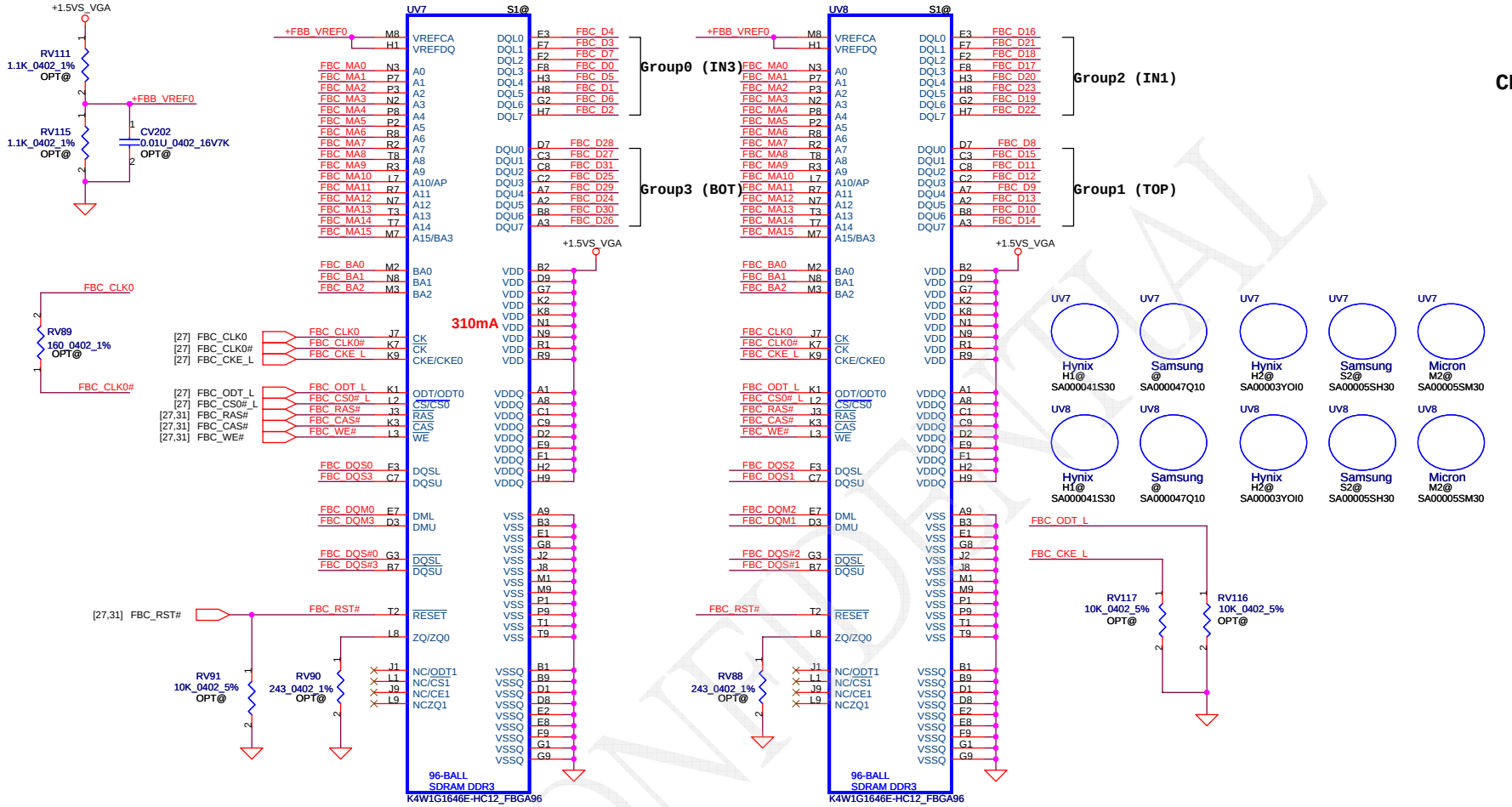
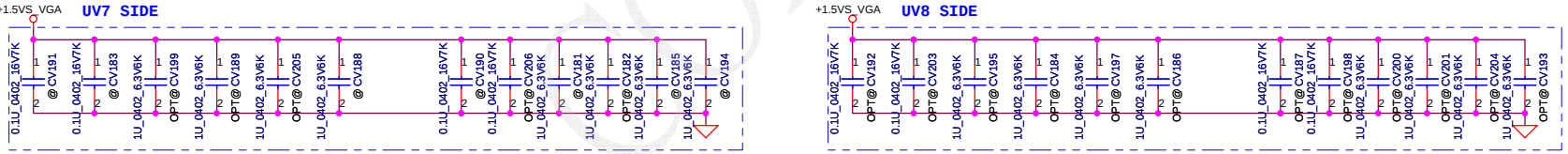
Memory Partition C - Lower 32 bits



FBC_D[0..63] [27,31]
FBC_MA[15..0] [27,31]
FBC_BA[2..0] [27,31]
FBC_DQM[7..0] [27,31]
FBC_DQS[7..0] [27,31]
FBC_DQS#[7..0] [27,31]

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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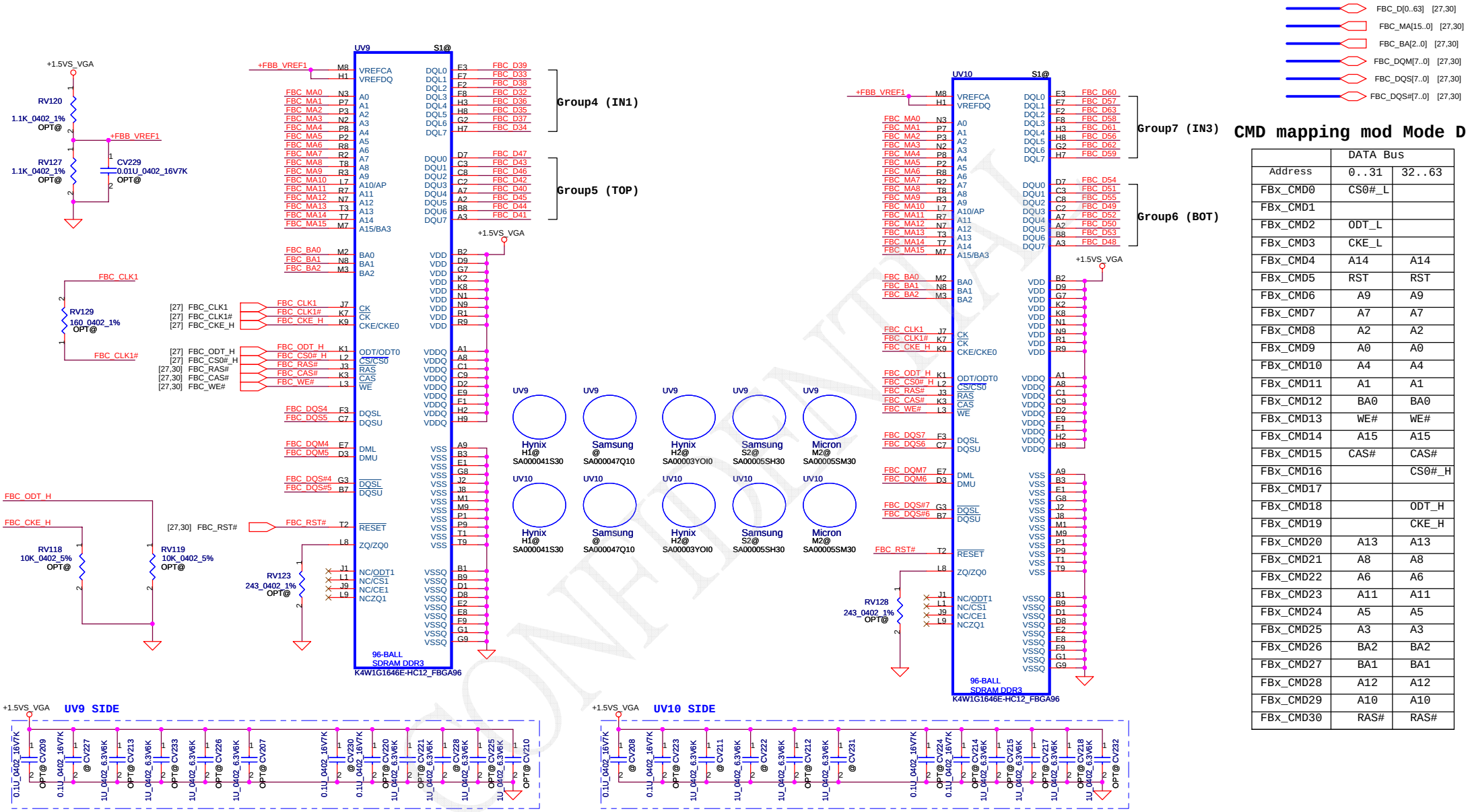
Memory Partition C - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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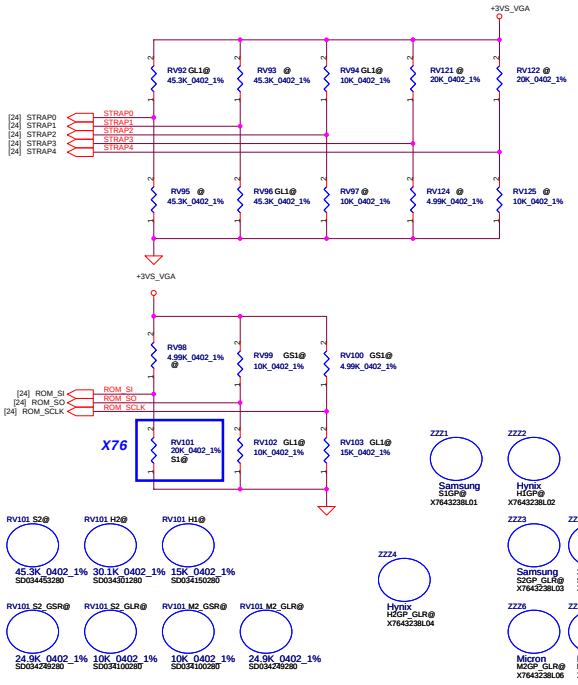

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Vendor	VRAM Sturcture
Samsung 2G	S2@
Hynix 2G	H2@
Samsung 1G	S1@
Hynix 1G	H1@

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

For N13P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 30.1K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PU 5K	R PD 15K	R PD 5K	R PD 45K	R PD 15K	R PU 10K	R PU 5K

X76

strap0 RV92 GS1@ 45.3K_0402_1% SD034453280
strap1 RV96 GS1@ 4.99K_0402_1% SD034499180
strap2 RV97 GS1@ 15K_0402_1% SD034150280
strap3 RV124 GS1@ 4.99K_0402_1% SD034499180
strap4 RV125 GS1@ 45.3K_0402_1% SD034453280

For N13P-GSR strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 5K	R PU 10K	R PD 5K	R PD 45K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 5K	R PU 10K	R PD 5K	R PD 45K	R PD 30.1K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 5K	R PU 10K	R PD 5K	R PD 45K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PU 5K	R PU 10K	R PD 5K	R PD 45K	R PD 15K	R PU 10K	R PU 5K

X76

strap0 RV92_GSR@ 45.3K_0402_1% SD034453280
strap1 RV96_GSR@ 4.99K_0402_1% SD034499180
strap2 RV94_GSR@ 10K_0402_1% SD034100280
strap3 RV124 GSR@ 4.99K_0402_1% SD034499180
strap4 RV125 GSR@ 45.3K_0402_1% SD034453280
ROM_SO RV99_GSR@ 10K_0402_1% SD034100280
ROM_SCLK RV100 GSR@ 4.99K_0402_1% SD034499180

For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 30.1K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

X76

For N13P-GLR strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 30.1K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

X76

strap0 RV92_GLR@ 45.3K_0402_1% SD034453280
strap1 RV96_GLR@ 45.3K_0402_1% SD034453280
strap2 RV97_GLR@ 20K_0402_1% SD034200280
strap3
strap4
ROM_SO RV102 GLR@ 10K_0402_1% SD034100280
ROM_SCLK RV103 GLR@ 15K_0402_1% SD034150280

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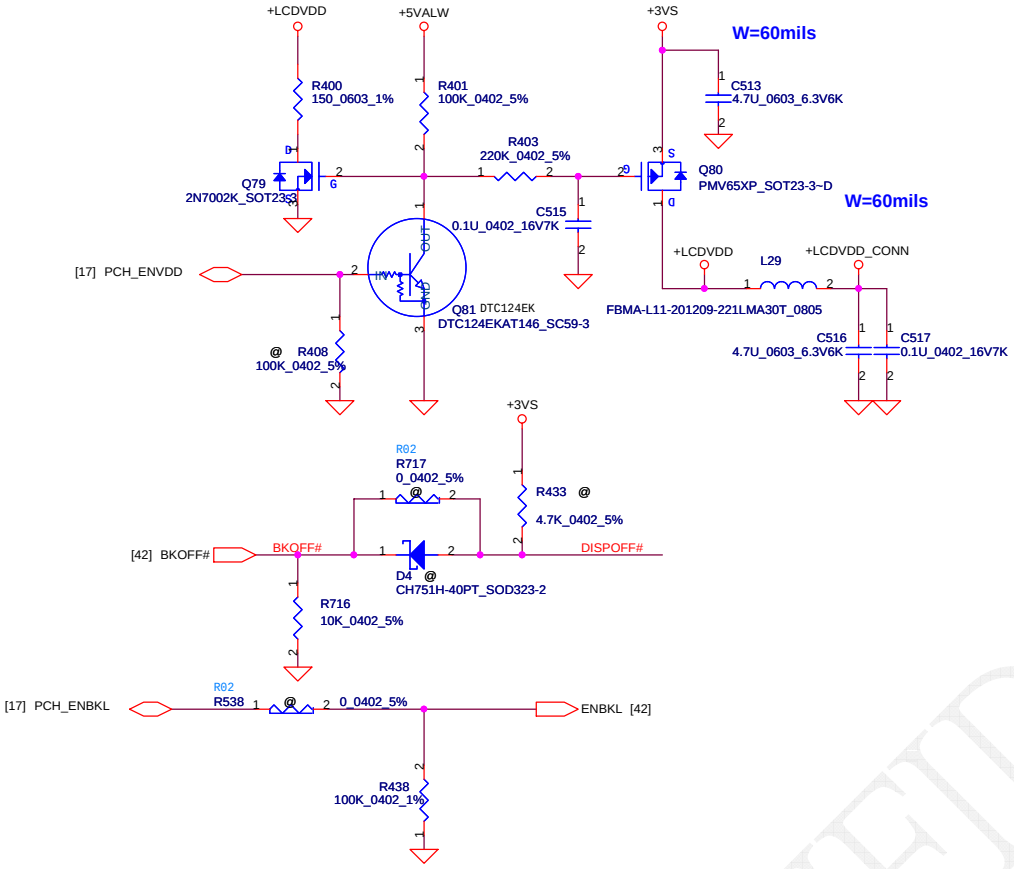
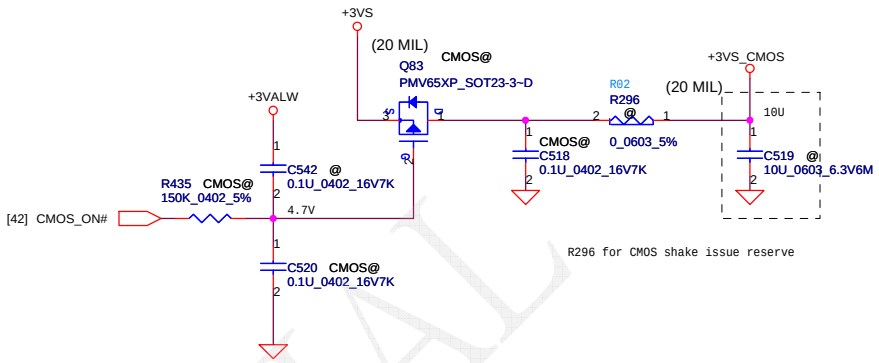
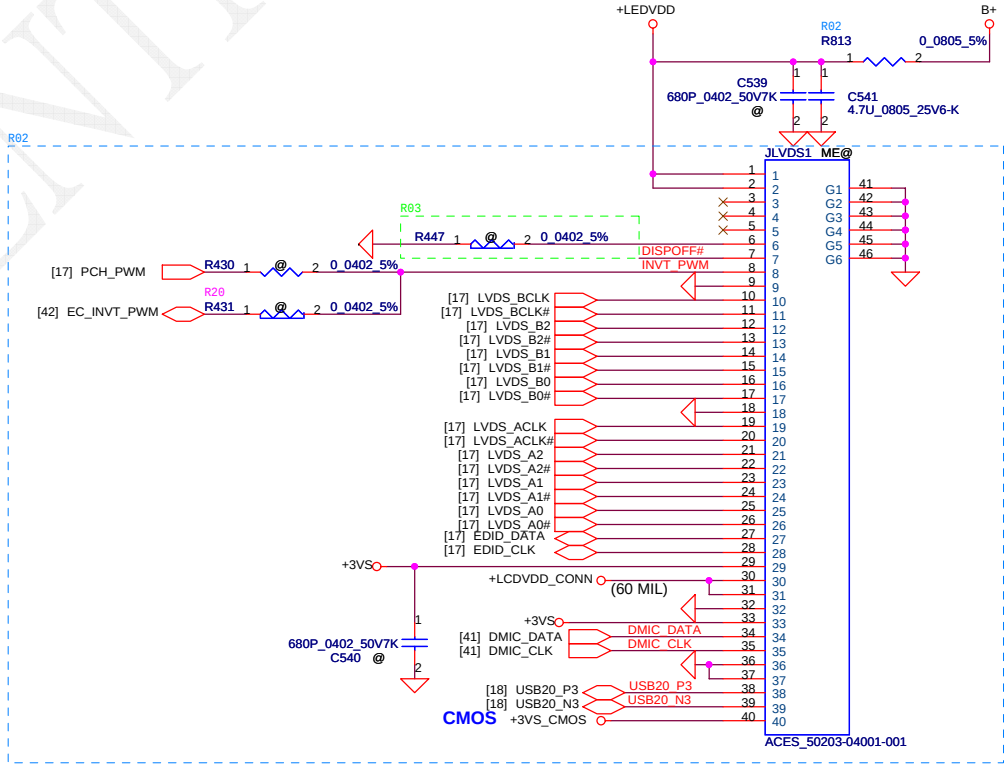
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



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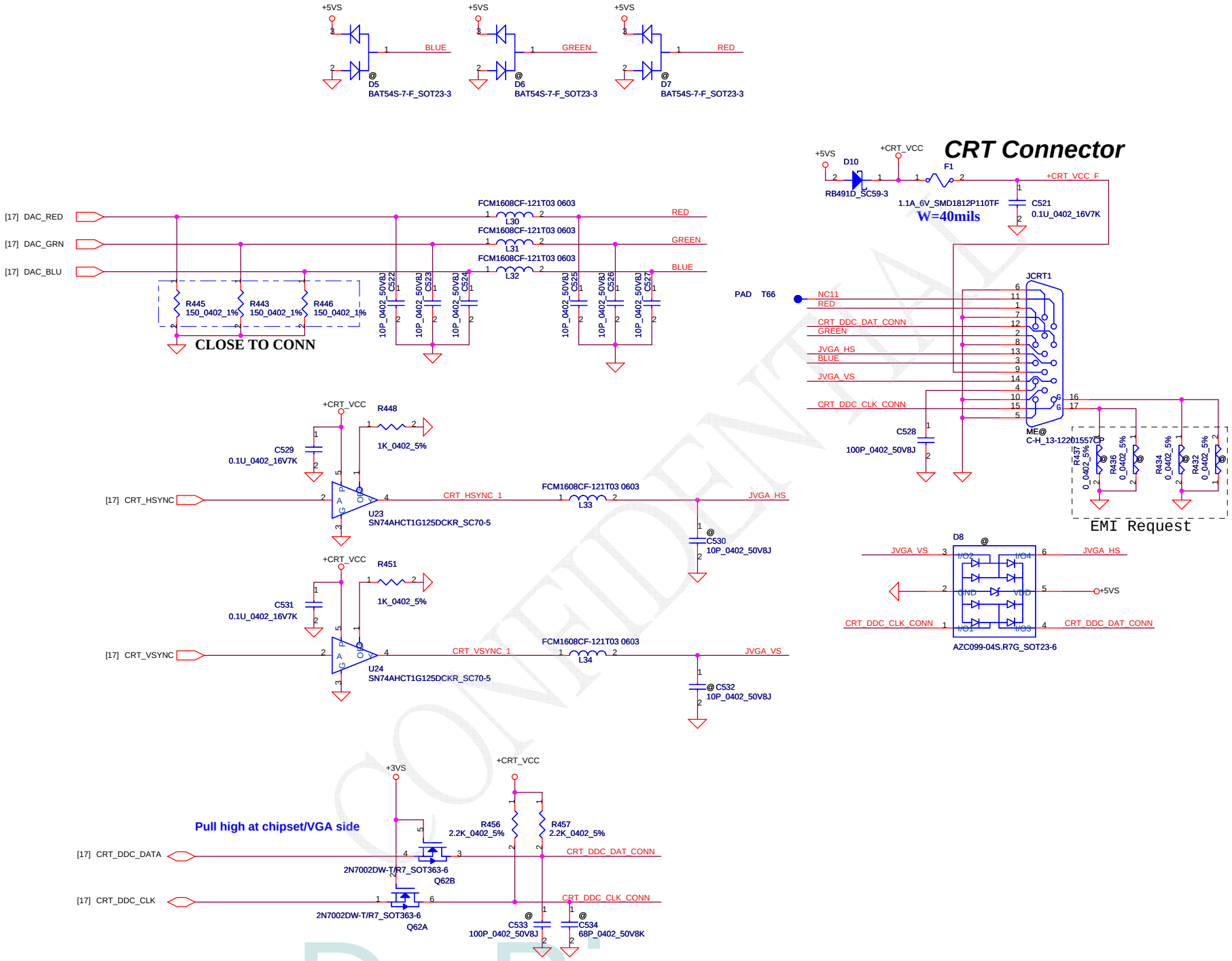

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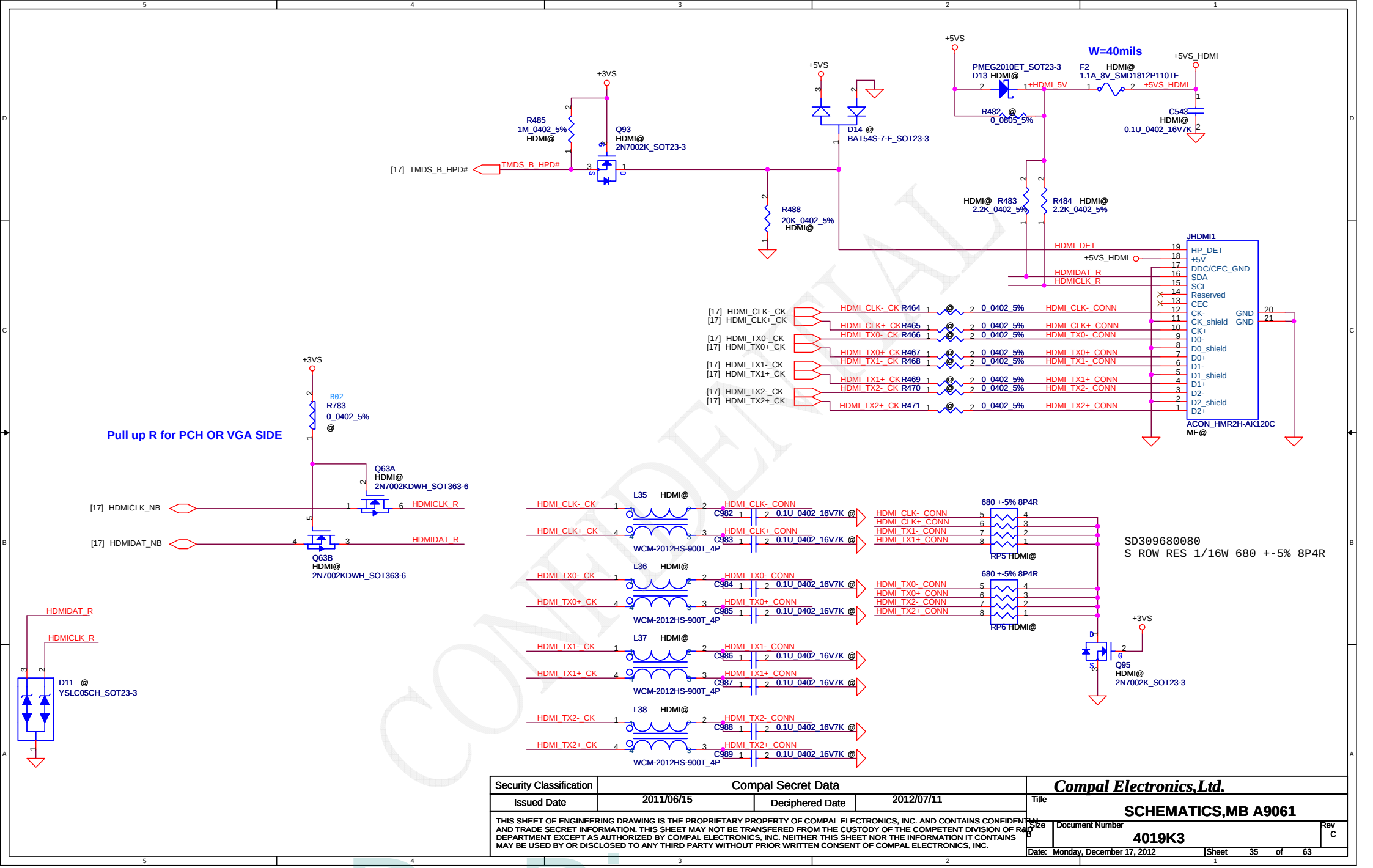

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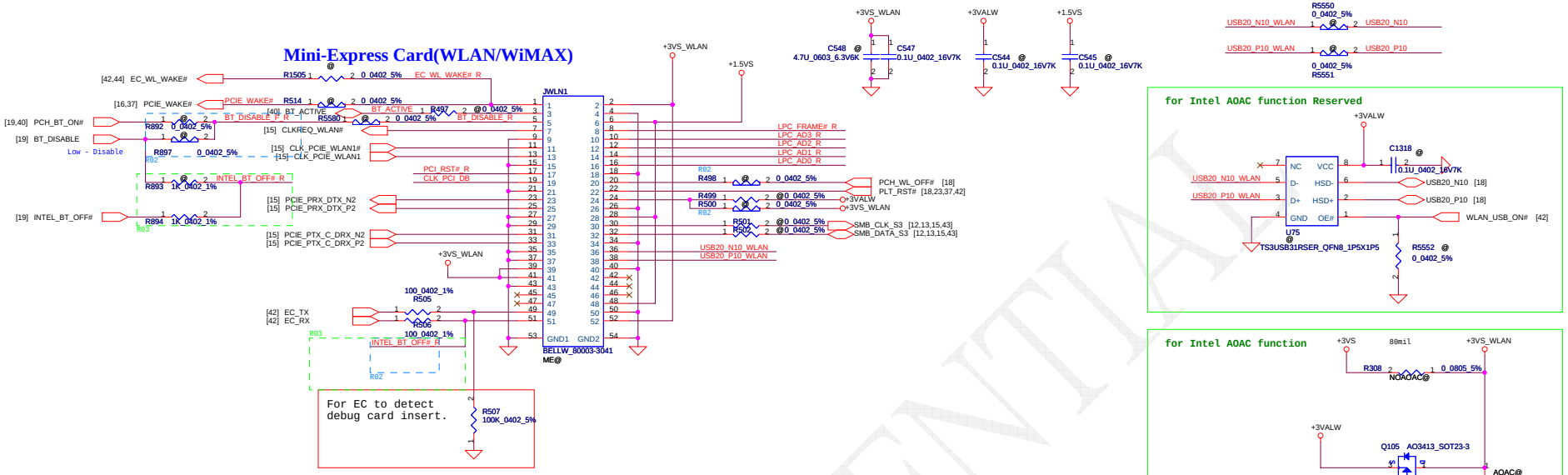
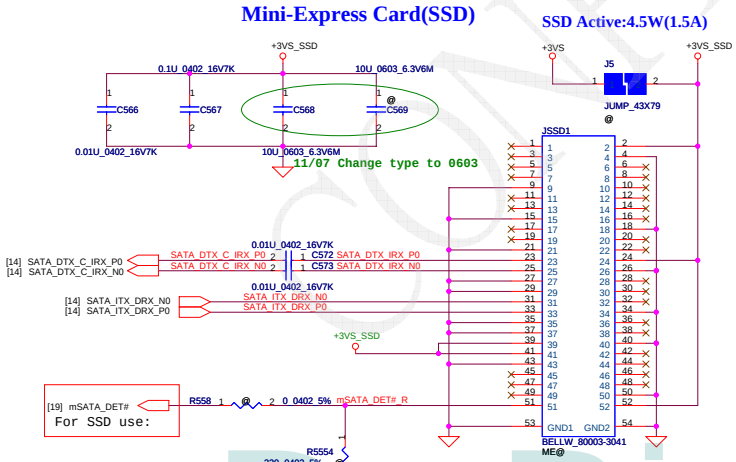
Mini-Express Card for WLAN/WiMAX(Half)





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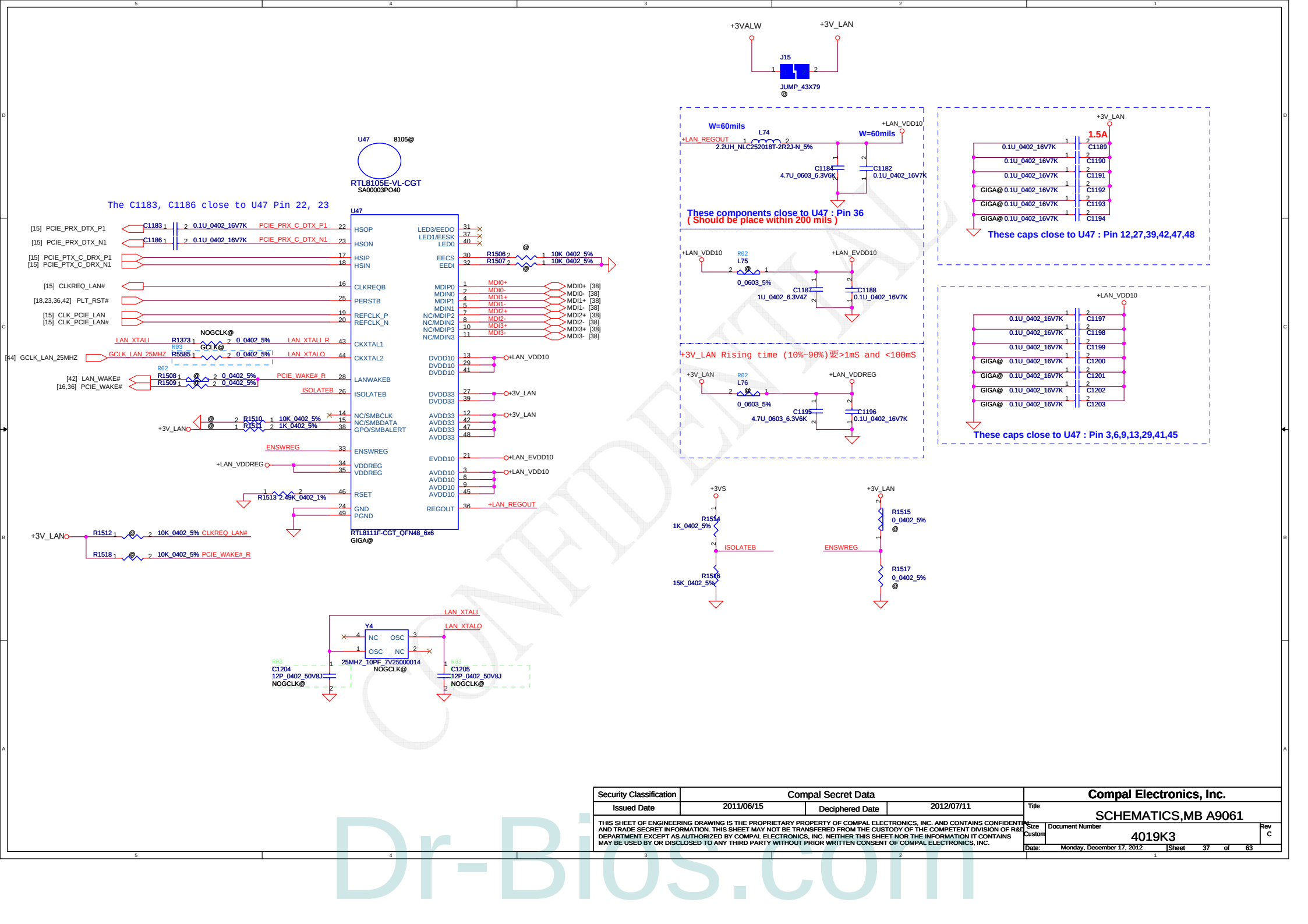

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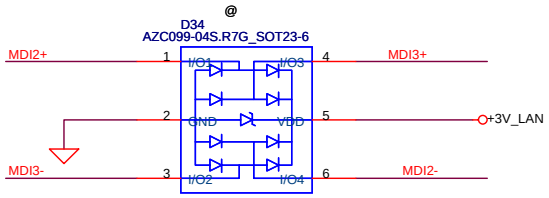
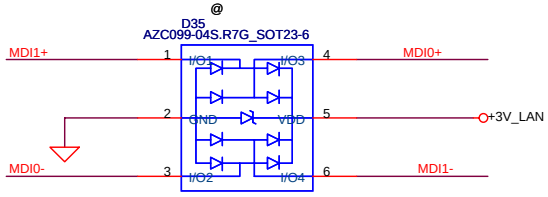


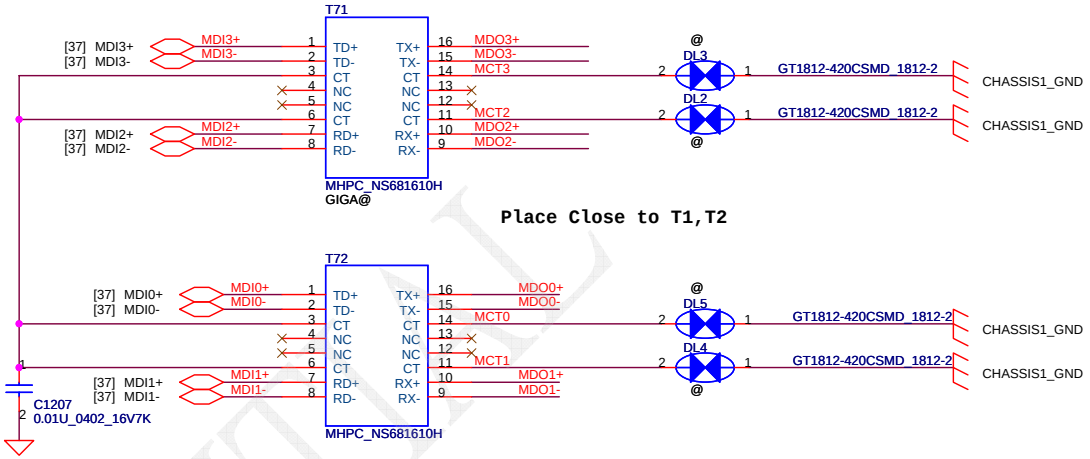
Place Close to T71



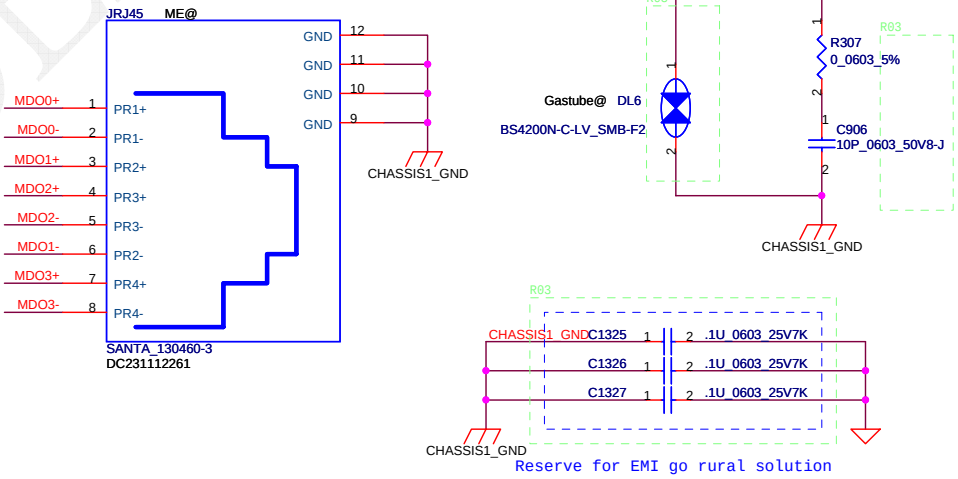
Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

Reserve gas tube for EMI go rural solution



Place Close to T1,T2



Reserve for EMI go rural solution

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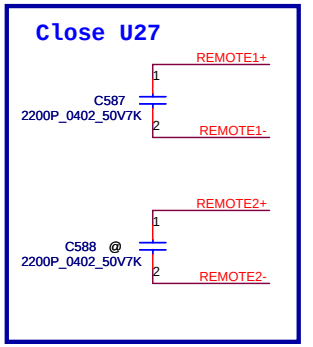
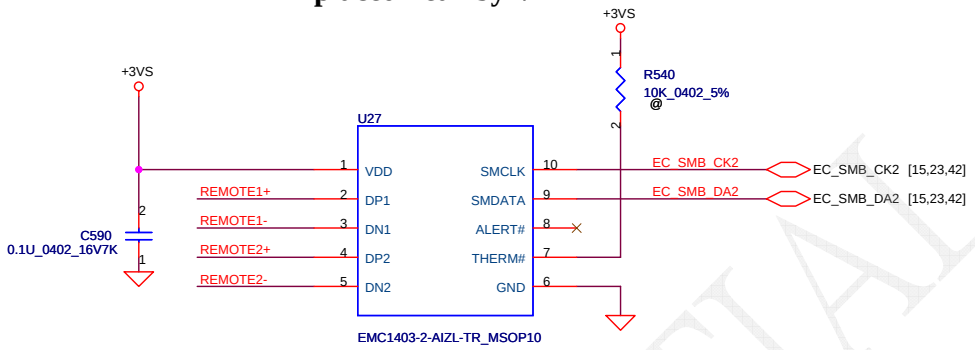
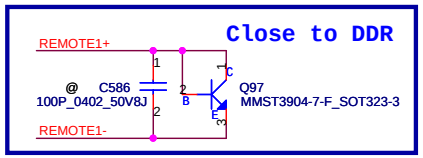
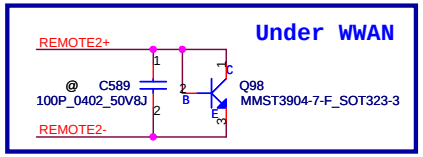
SMSC thermal sensor placed near by VRAM



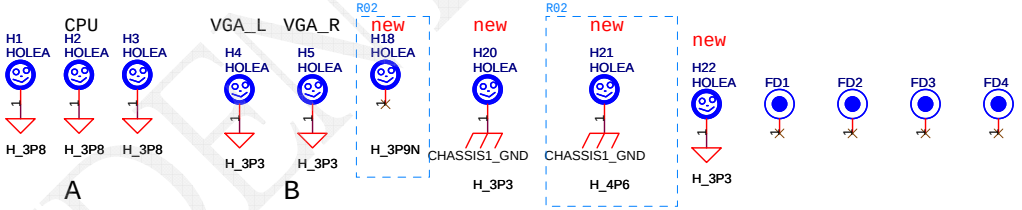


Address 1001_101xb

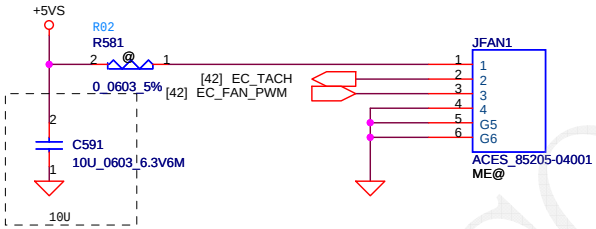


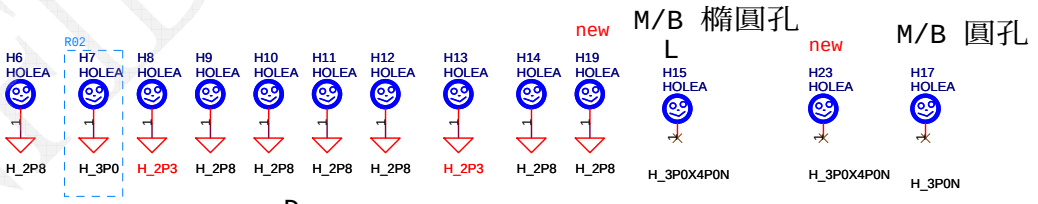


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn





2P8 * 7 pcd

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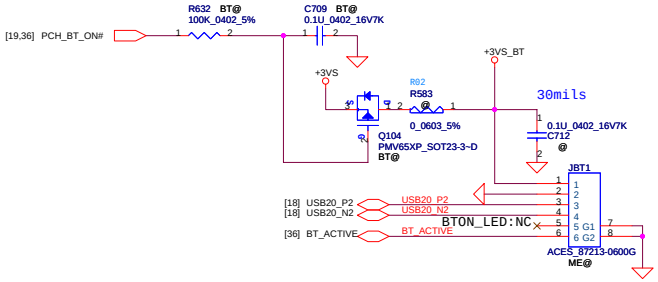
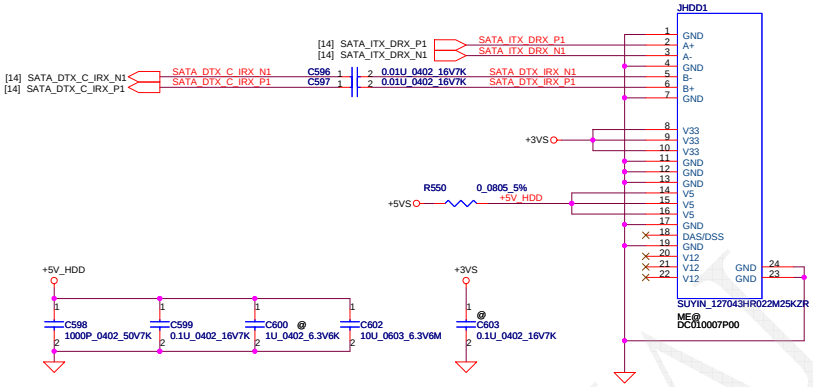
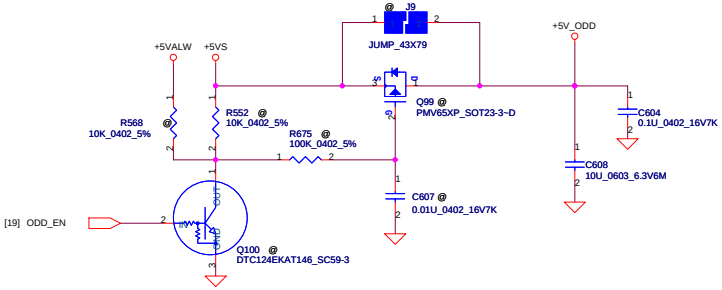
BT MODULE CONN



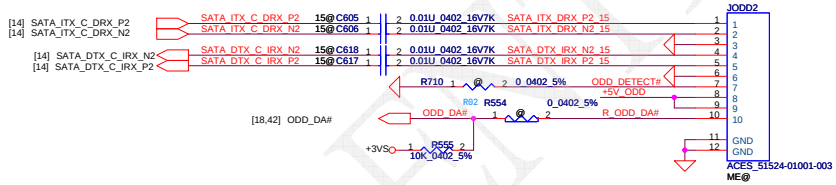
SATA HDD Conn.

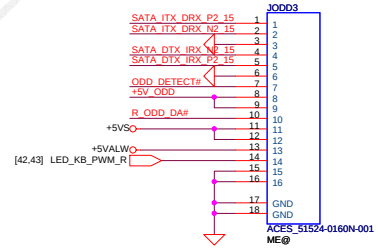


ODD Power Control

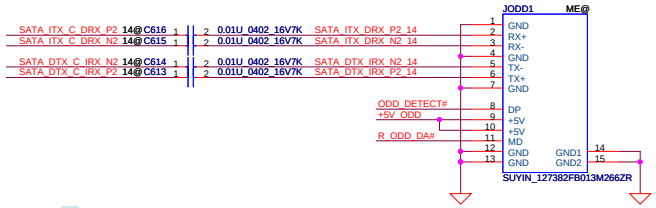


FOR 15" SATA ODD FFC Conn.





Co-lay FOR 14" SATA ODD Conn.



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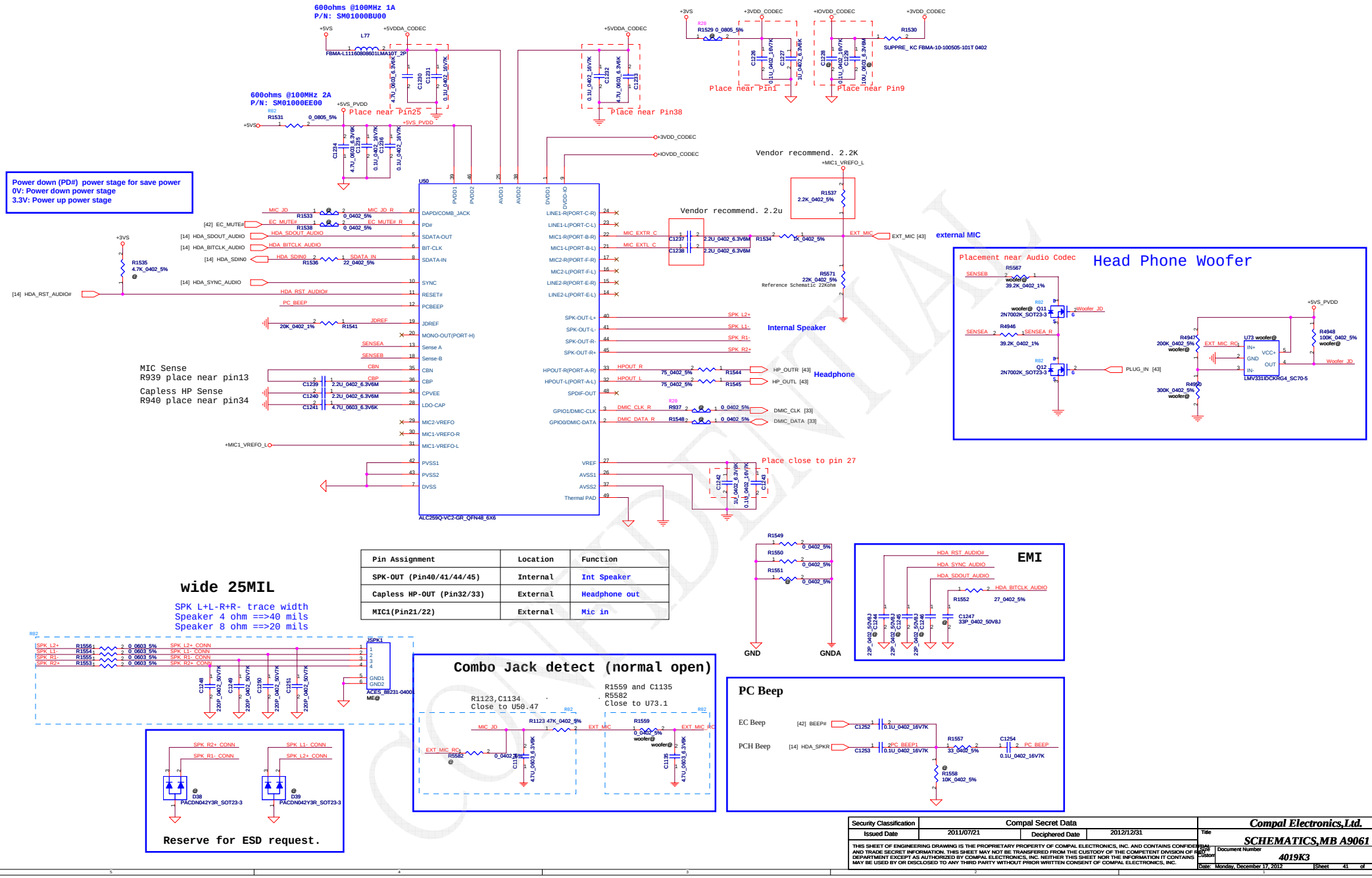

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

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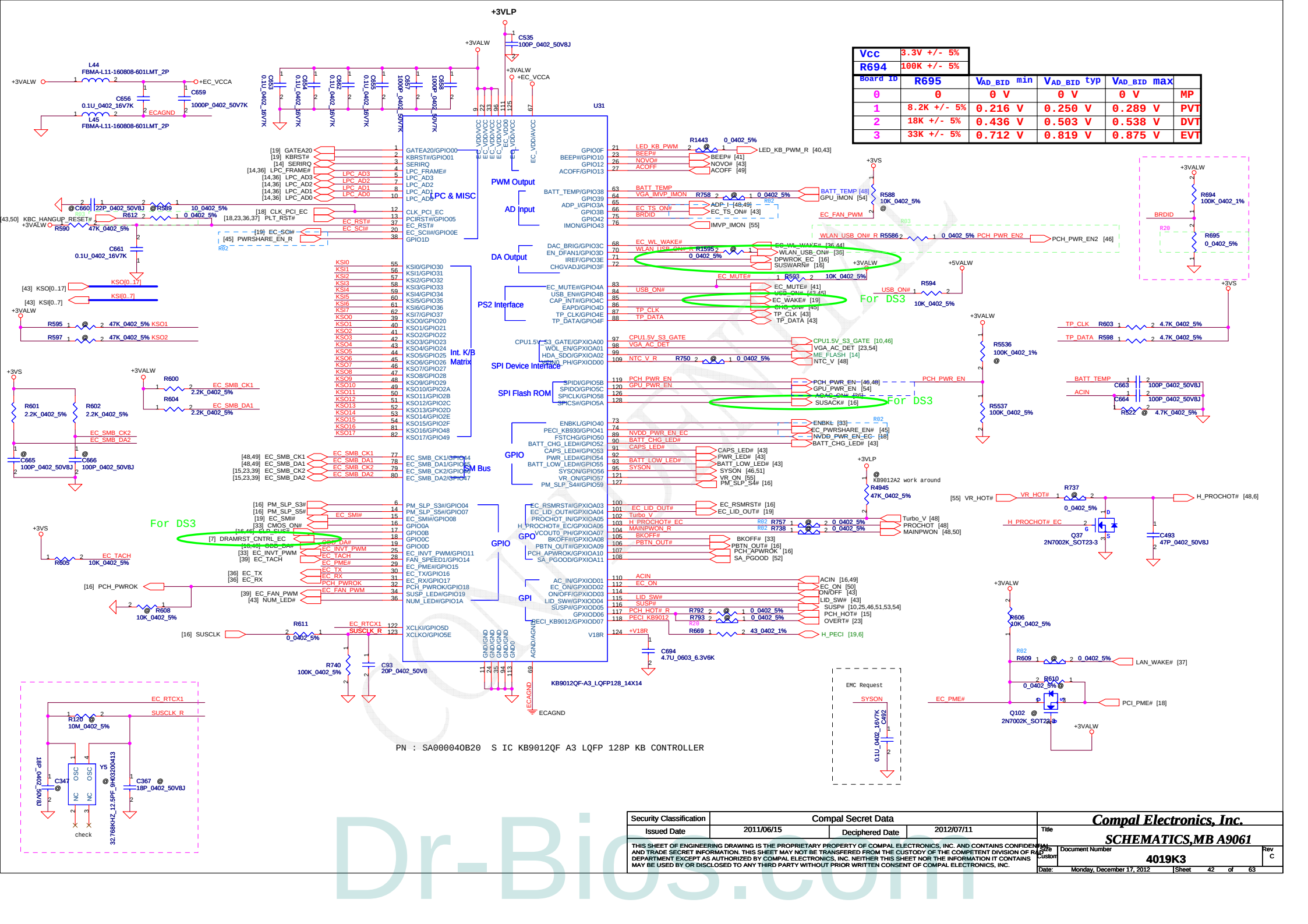
+3VLP
U31
KB9012QF-A3_LQFP128_14X14
PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
For DS3
EMC Request
Vcc 3.3V +/- 5%
R694 100K +/- 5%
Board ID | R695 | VAD_BID min | VAD_BID typ | VAD_BID max
0 | 0 | 0 V | 0 V | 0 V | MP
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | PVT
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | DVT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | EVT
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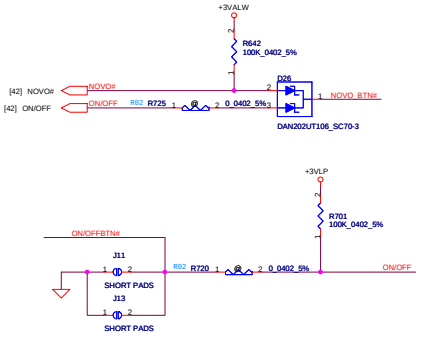
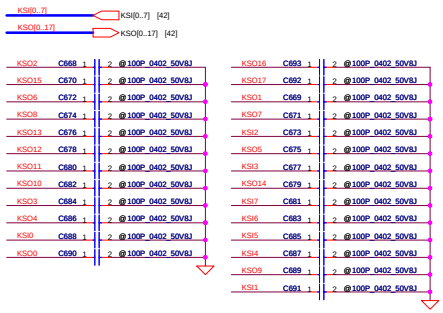
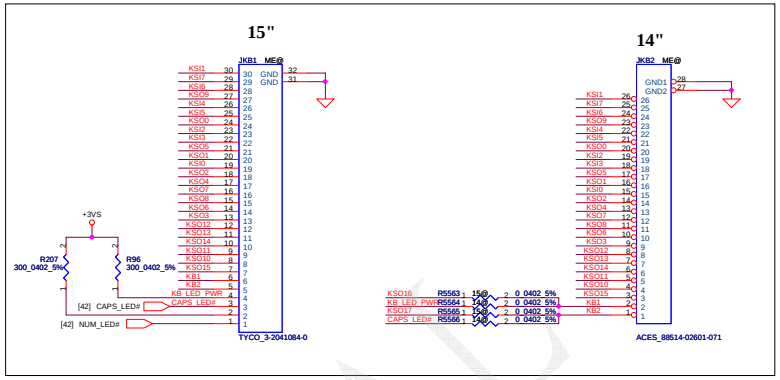
ON/OFF switch

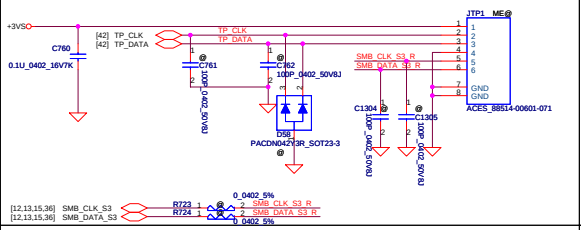


K/B Connector

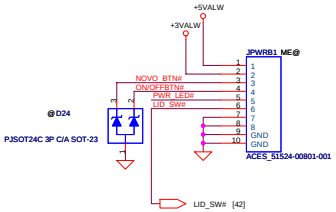




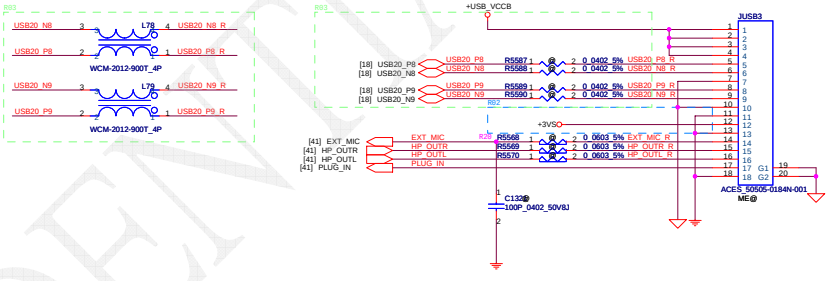
TP/B Connector



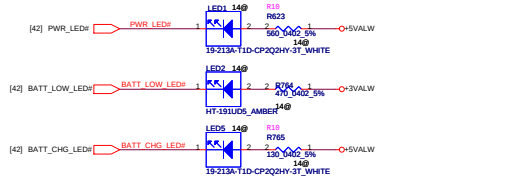
PWR/B Connector



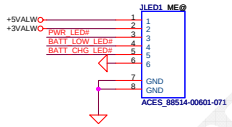
USB I/O Connector



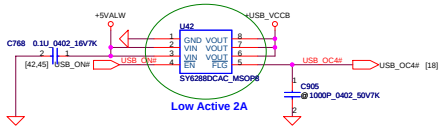
LED (For 14")



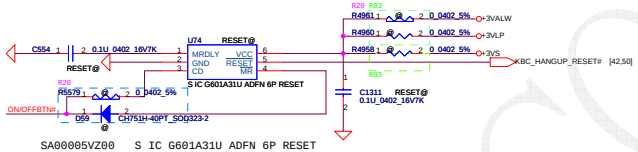
LED (For 15")



Right Side USB2.0 Port X 2 (USB/B)

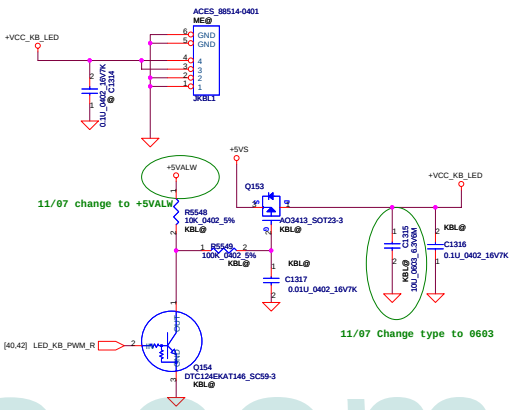


EC RESEST function

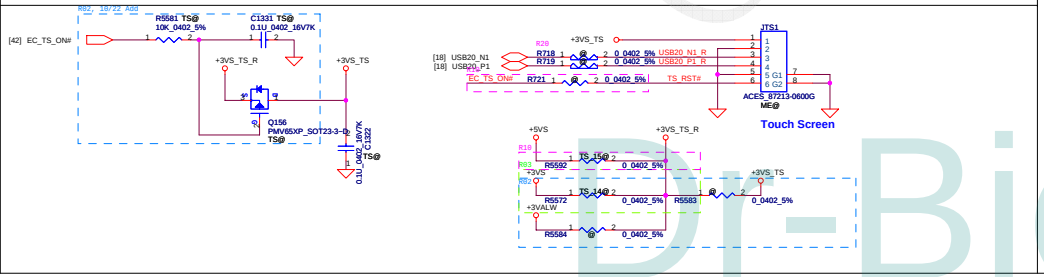


SA00005VZ00 S IC G601A31U ADFN 6P RESET

KB Lighting CONN.4pin



Touch Screen



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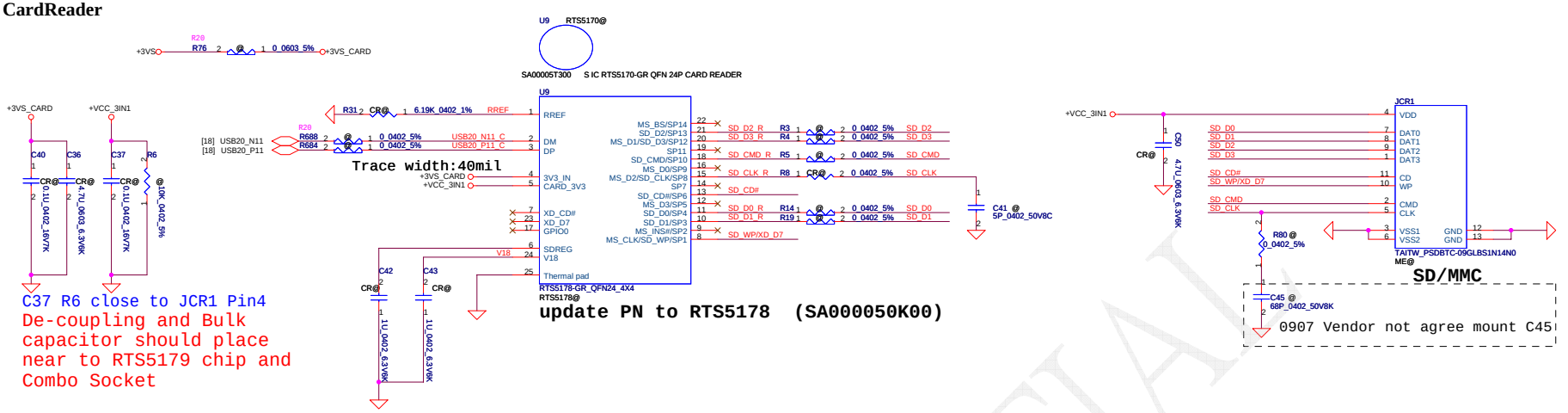
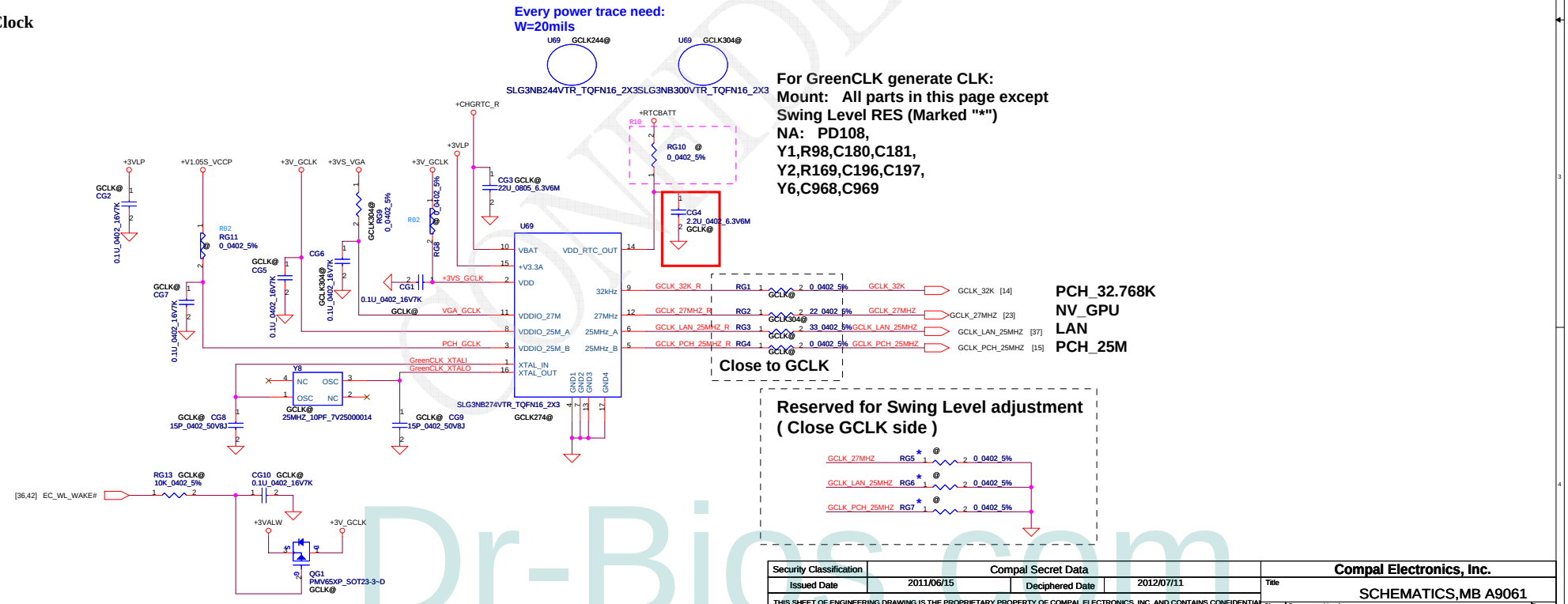
RTS5178 CardReader



Green Clock



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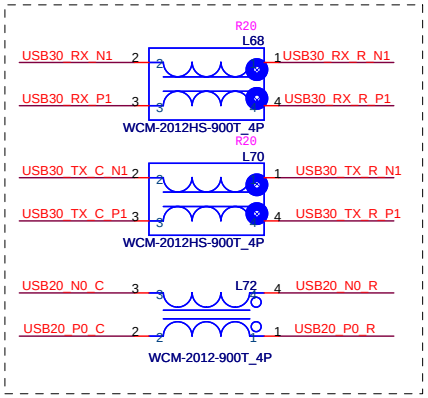
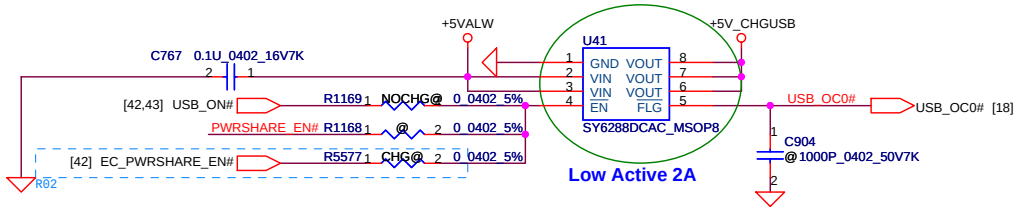
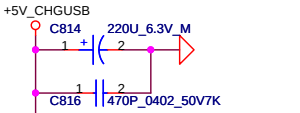
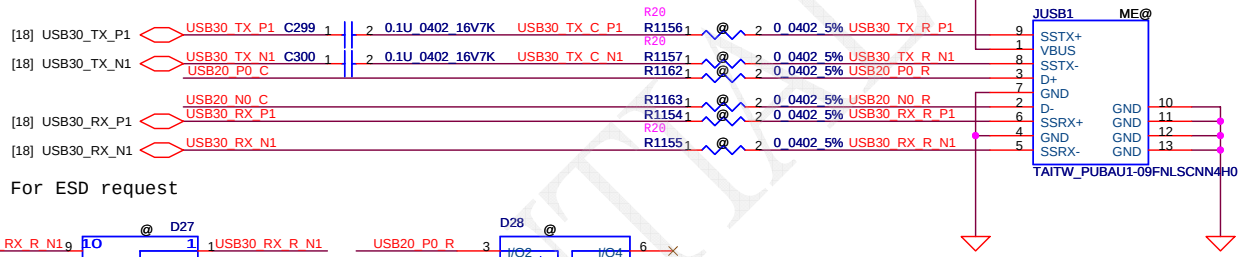
LEFT SIDE USB3.0 PORT X1

For EMI request
USB2.0 choke --> SM070000K00
USB3.0 Choke --> SM070001S00



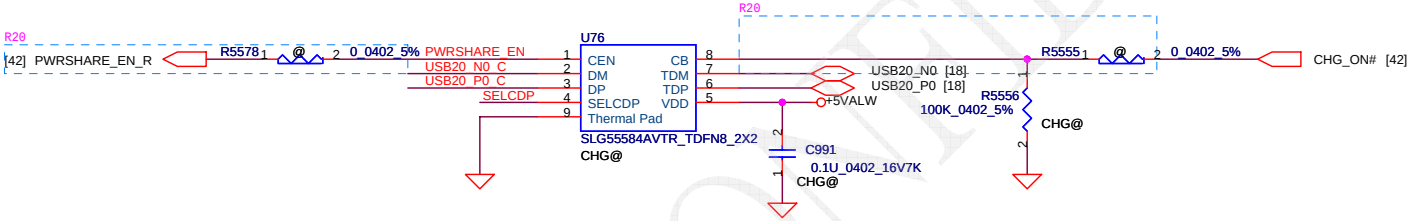


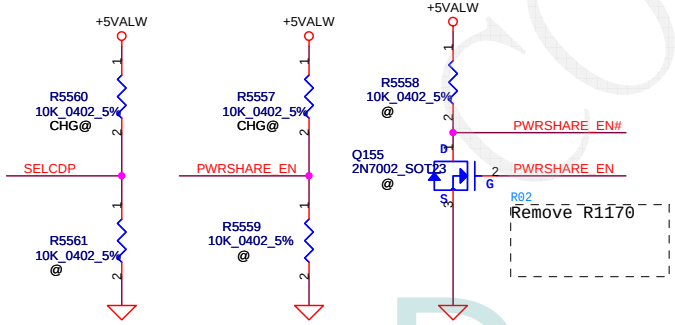


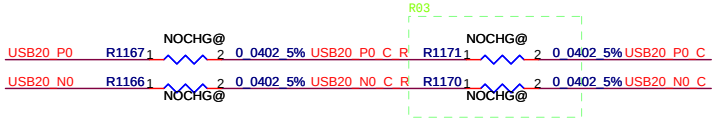


For ESD request

Left Side Charger USB3.0 Port







CB	SELCDP	Function
0	X	DCP autodetect with mouse /keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

USB2.0/3.0 choke and ESD diode at sub-B.

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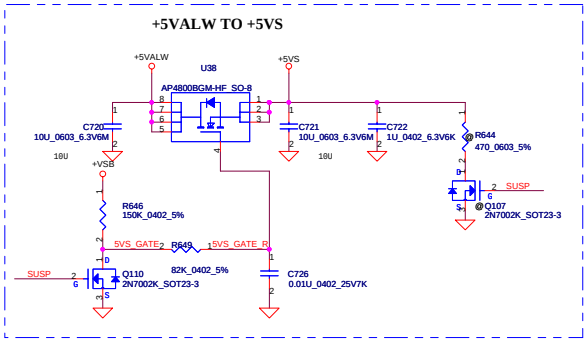

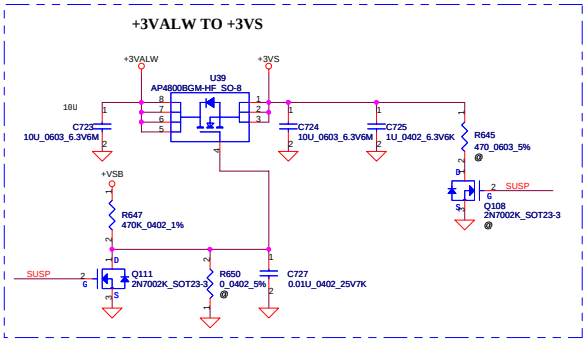

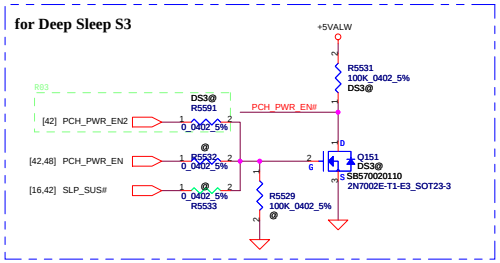

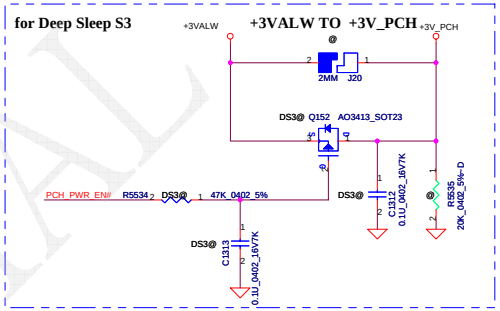

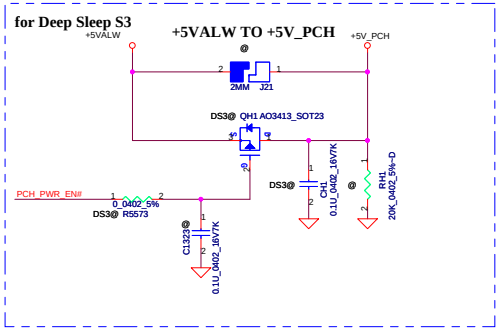

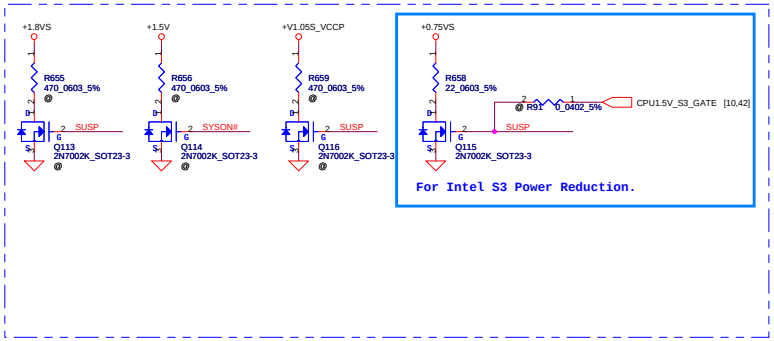

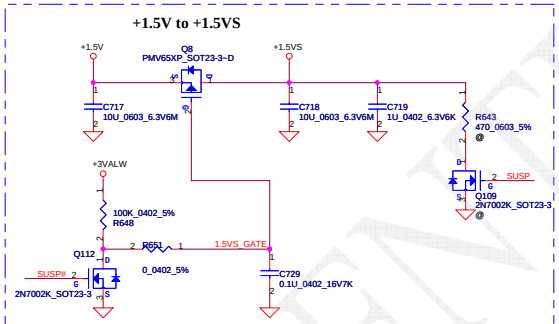

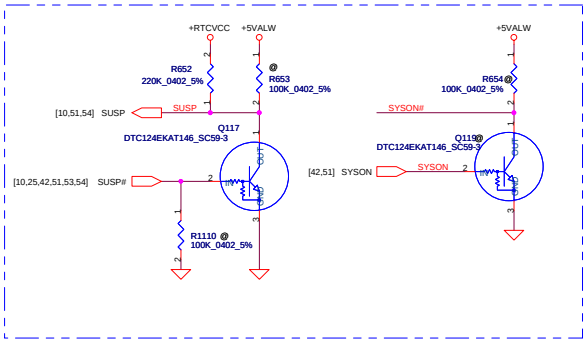

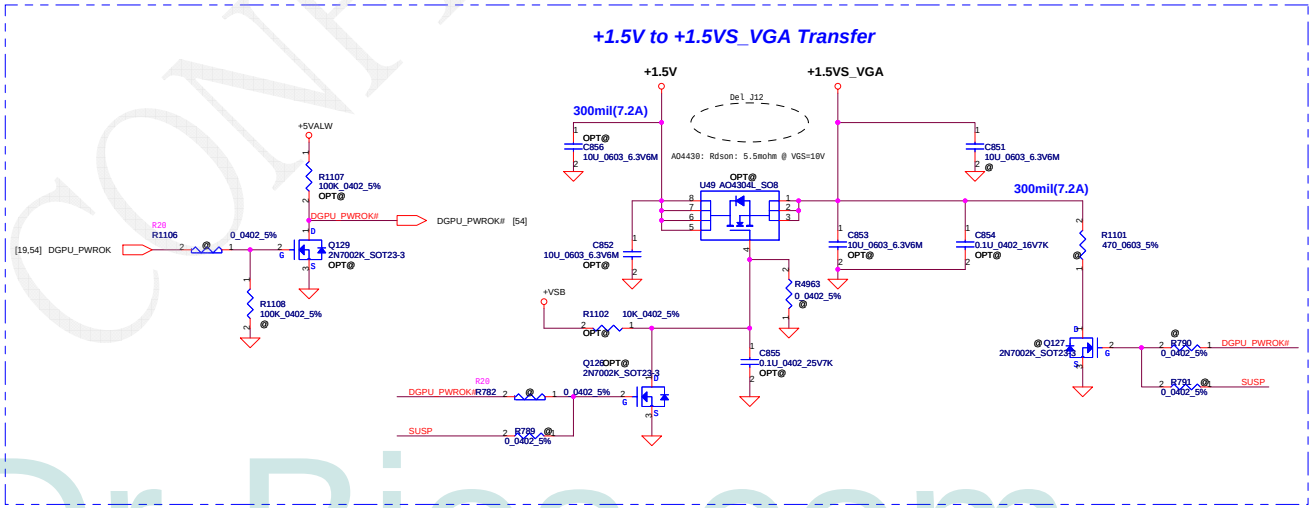

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			Size Custom / Document Number 4019K3 / Rev C
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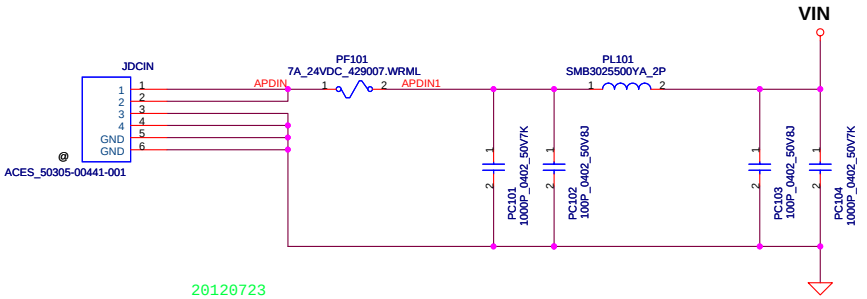
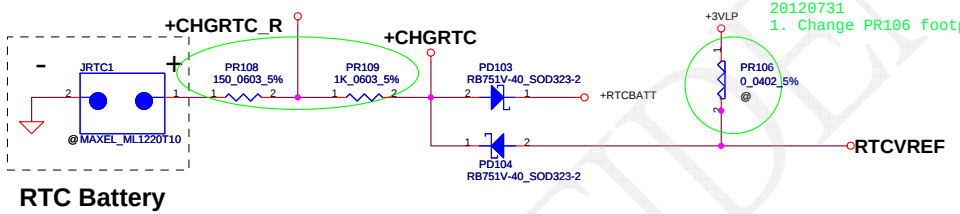


20120723
For all sku
1. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080
   Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080



20120731
1. Change PR106 footprint to R0402_0ohm-NEW

20120731
1. Add PR110 SD013000080 0_0603_5%
   Add PR111 SD013150080 150_0603_5%

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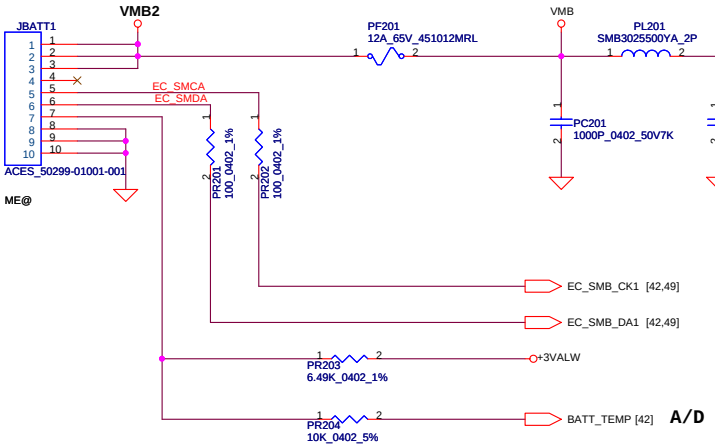


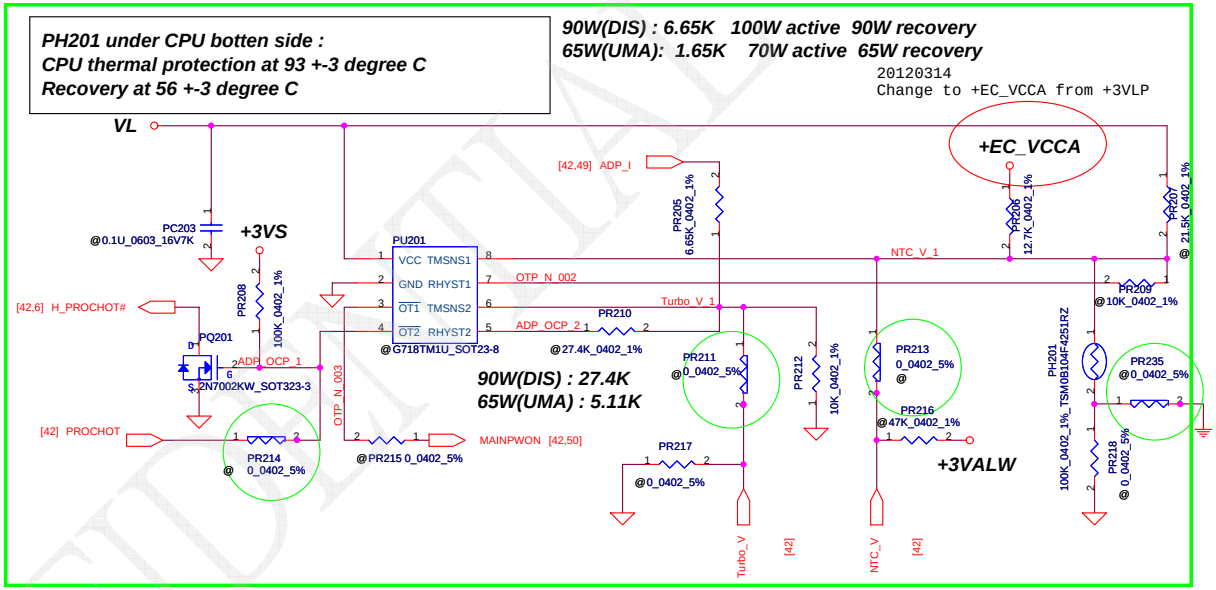
ADP_I need to write Charge Options Register (0x12H)=> bit6=1

0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output

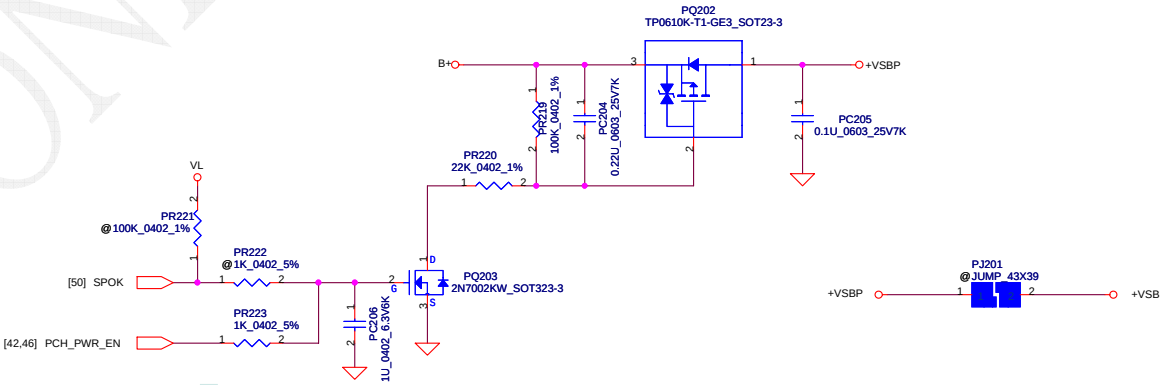
PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA): 1.65K 70W active 65W recovery

20120314
Change to +EC_VCCA from +3VLP



20120731
1. Change PR214,PR211,PR213 and PR235 footprint to R0402_0ohm-NEW



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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Need EC write ChargeOption() bit[8]=1
Setting (ACP to PHASE Rising Threshold)=1350mV(min)

SH00000AA00

SA000051W00

20120615
Change PR313 to 60.4K_0603_1% SD014604280
from 64.9K_0603_1% SD014649280

20120723
Change PR313 to 59K_0603_1% SD014590280
from 60.4K_0603_1% SD014604280

For disable pre-charge circuit.

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Compal Electronics, Inc.			
Title: CHARGER			
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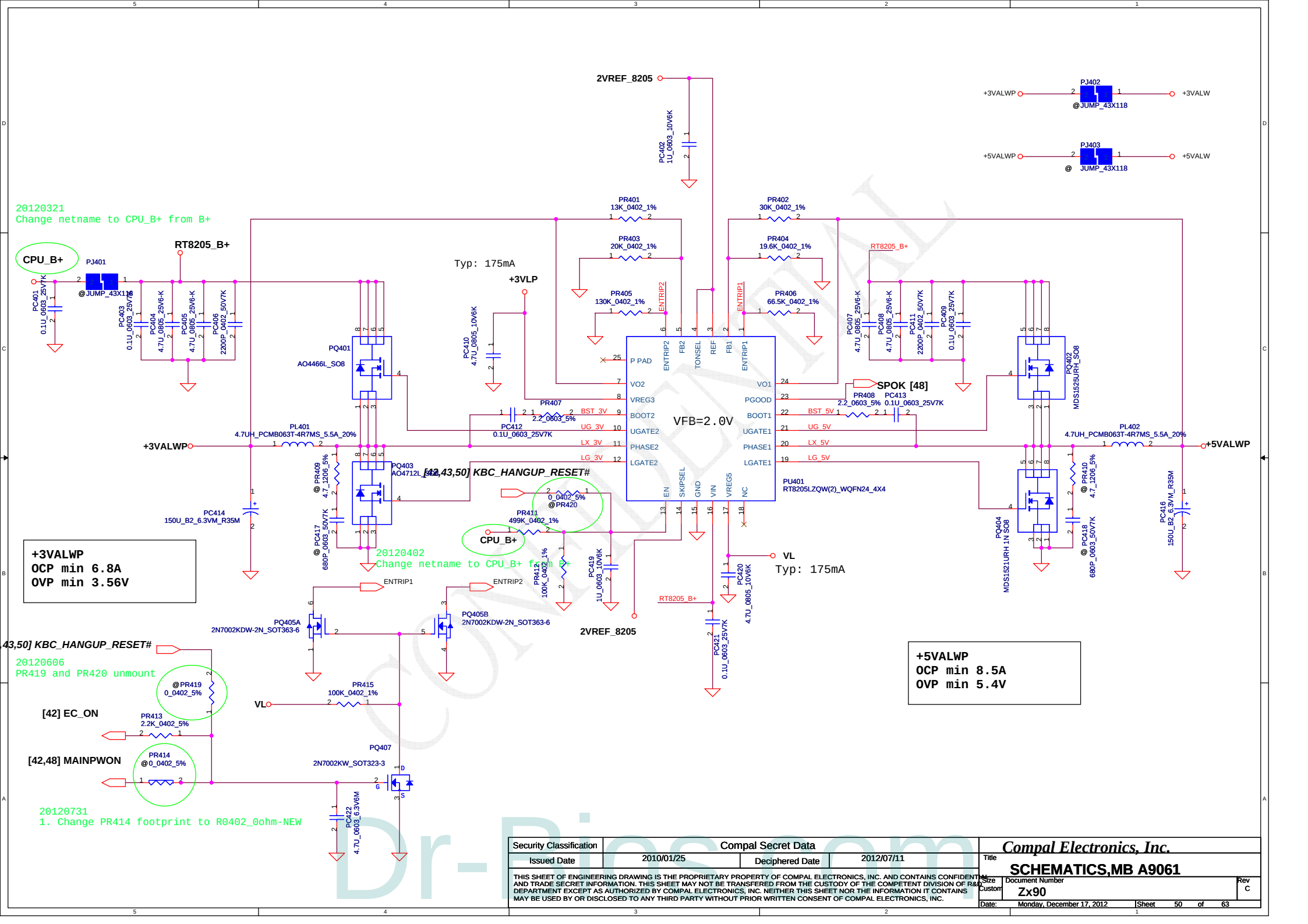
2VREF_8205
PC402 1U_0603_10V6K
+3VALWP
PJ402
@JUMP_43X118
+3VALW
+5VALWP
PJ403
@JUMP_43X118
+5VALW
20120321
Change netname to CPU_B+ from B+
CPU_B+
PJ401
@JUMP_43X118
RT8205_B+
PC401 0.1U_0603_25V7K
PC403 0.1U_0603_25V7K
PC404 4.7U_0805_25V6-K
PC405 4.7U_0805_25V6-K
PC406 220P_0402_50V7K
Typ: 175mA
+3VLP
PC410 4.7U_0805_10V6K
PR401 13K_0402_1%
PR402 30K_0402_1%
PR403 20K_0402_1%
PR404 19.6K_0402_1%
PR405 130K_0402_1%
PR406 66.5K_0402_1%
ENTRIP2
ENTRIP1
PQ401
AO4466L_SO8
PR407
2.2_0603_5%
PC412 0.1U_0603_25V7K
BST_3V
UG_3V
LX_3V
LG_3V
P PAD
VO2
VREG3
BOOT2
UGATE2
PHASE2
LGATE2
FB2
TONSEL
REF
FB1
VO1
PGOOD
BOOT1
UGATE1
PHASE1
LGATE1
EN
SKIPSEL
GND
VIN
VREG5
NC
VFB=2.0V
PU401
RT8205LZQW(2)_WQFN24_4X4
SPOK [48]
PR408 2.2_0603_5%
PC413 0.1U_0603_25V7K
BST_5V
UG_5V
LX_5V
LG_5V
PC407 4.7U_0805_25V6-K
PC408 4.7U_0805_25V6-K
PC411 220P_0402_50V7K
PC409 0.1U_0603_25V7K
PQ402
MDS1525URH_SO8
PL401
4.7UH_PCMB063T-4R7MS_5.5A_20%
PL402
4.7UH_PCMB063T-4R7MS_5.5A_20%
+3VALWP
+5VALWP
PQ403
AO4712L_SO8
@ PR409 4.7_1206_5%
@ PC417 680P_0603_50V7K
PC414 150U_B2_6.3VM_R35M
[42,43,50] KBC_HANGUP_RESET#
0_0402_5%
@PR420
PR411 499K_0402_1%
CPU_B+
PQ404
MDS1521URH 1N SO8
@ PR410 4.7_1206_5%
@ PC418 680P_0603_50V7K
PC416 150U_B2_6.3VM_R35M
+3VALWP
OCP min 6.8A
OVP min 3.56V
20120402
Change netname to CPU_B+ from B+
PR412 100K_0402_1%
PC419 1U_0603_10V6K
VL
Typ: 175mA
PC420 4.7U_0805_10V6K
RT8205_B+
PC421 0.1U_0603_25V7K
2VREF_8205
ENTRIP1
ENTRIP2
PQ405A
2N7002KDW-2N_SOT363-6
PQ405B
2N7002KDW-2N_SOT363-6
+5VALWP
OCP min 8.5A
OVP min 5.4V
[43,50] KBC_HANGUP_RESET#
20120606
PR419 and PR420 unmount
@PR419 0_0402_5%
[42] EC_ON
PR413 2.2K_0402_5%
[42,48] MAINPWON
PR414 @0_0402_5%
PR415 100K_0402_1%
VL
PQ407
2N7002KW_SOT323-3
PC422 4.7U_0603_6.3V6M
20120731
1. Change PR414 footprint to R0402_0ohm-NEW
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Security Classification
Compal Secret Data
Issued Date
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2012/07/11
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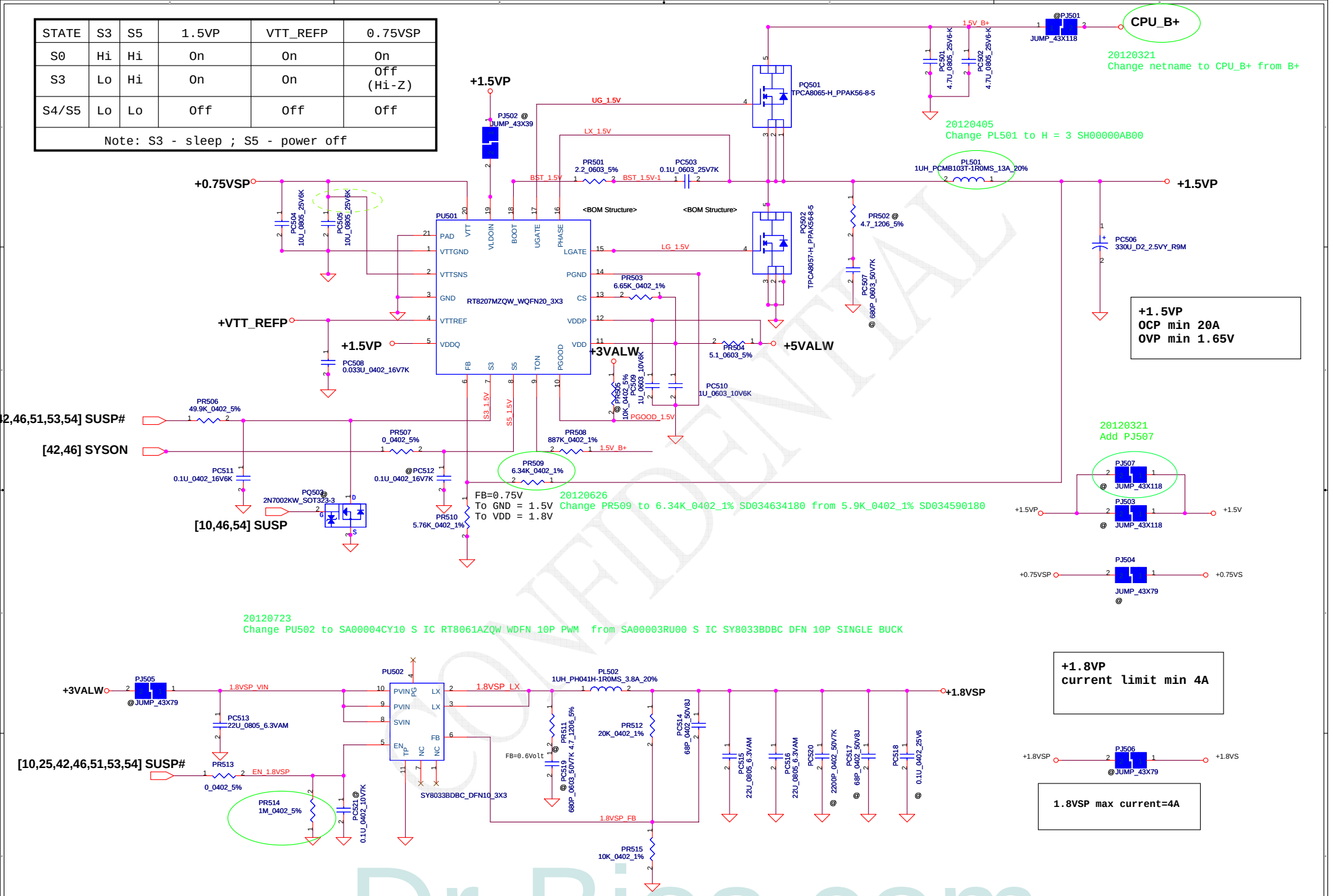
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



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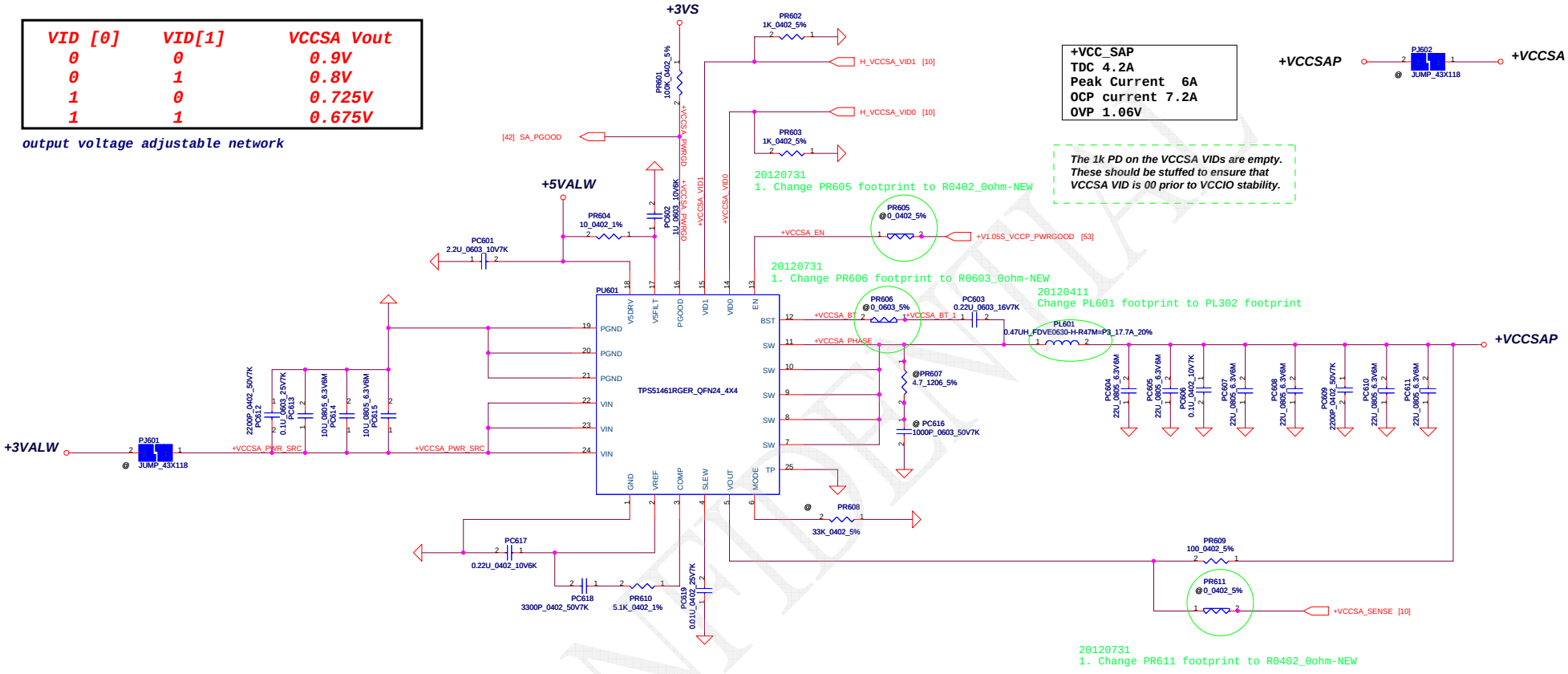

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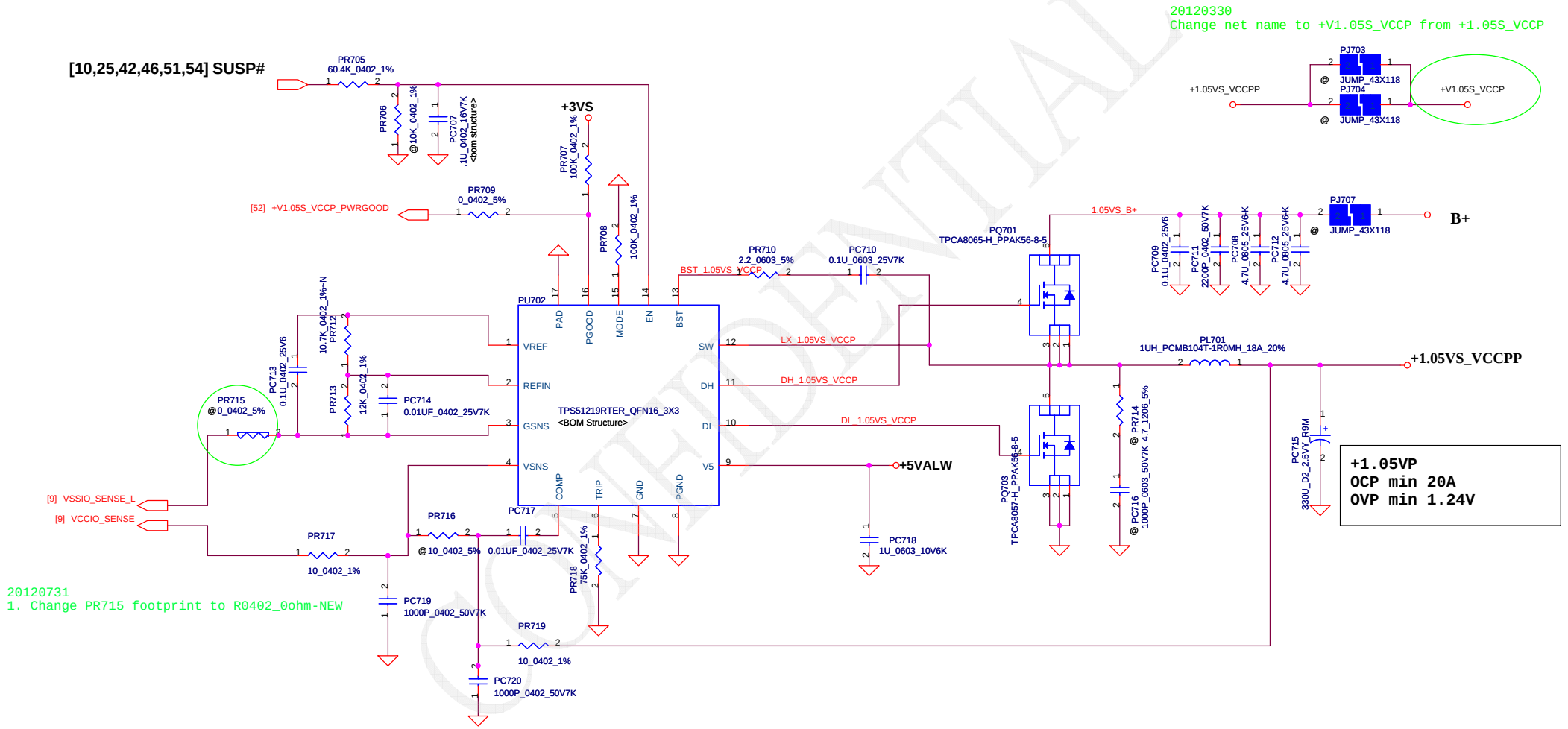

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Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Size: Custom	Document Number: Zx90		Rev: C
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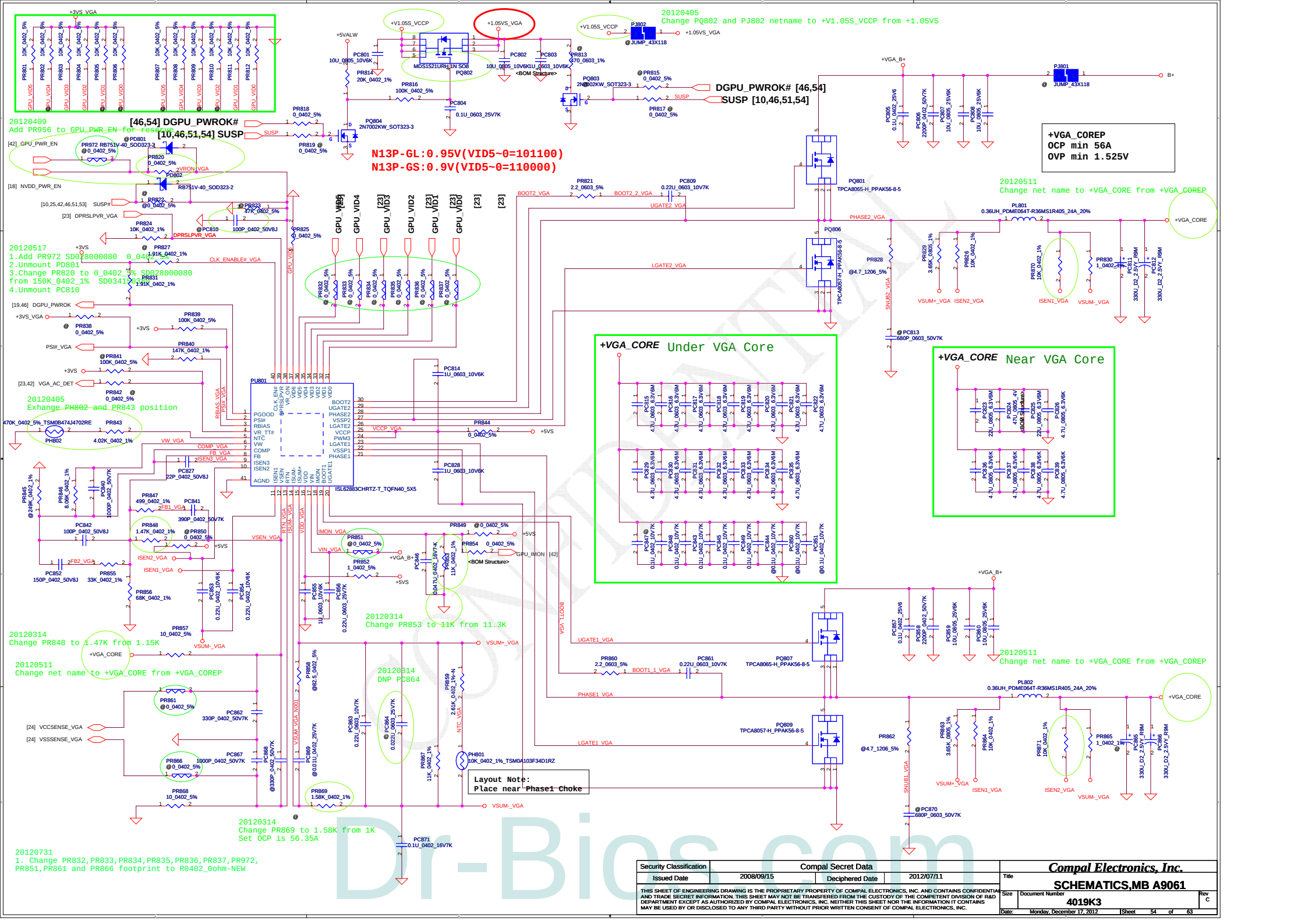
20120405
Change PQ802 and PJ802 netname to +V1.05S_VCCP from +1.05VS
20120409
Add PR956 to GPU_PWR_EN for reserve
[46,54] DGPU_PWROK#
[10,46,51,54] SUSP
N13P-GL:0.95V(VID5~0=101100)
N13P-GS:0.9V(VID5~0=110000)
+VGA_COREP
OCP min 56A
OVP min 1.525V
20120511
Change net name to +VGA_CORE from +VGA_COREP
20120517
1.Add PR972 SD028000080 0_0402_5%
2.Unmount PD801
3.Change PR820 to 0_0402_5% SD028000080
from 150K_0402_1% SD034150080
4.Unmount PC810
20120405
Exhange PH802 and PR843 position
+VGA_CORE Under VGA Core
+VGA_CORE Near VGA Core
20120314
Change PR848 to 1.47K from 1.15K
20120314
Change PR853 to 11K from 11.3K
20120314
DNP PC864
20120314
Change PR869 to 1.58K from 1K
Set OCP is 56.35A
Layout Note:
Place near Phase1 Choke
20120731
1. Change PR832,PR833,PR834,PR835,PR836,PR837,PR972,
PR851,PR861 and PR866 footprint to R0402_0ohm-NEW
ISL62883CHRTZ-T_TQFN40_5X5
TPCA8065-H_PPAK56-8-5
TPCA8057-H_PPAK56-8-5
MDS1521URH_TN SO8
2N7002KW_SOT323-3
RB751V-40_SOD323-2
JUMP_43X118
0.36UH_PDME064T-R36MS1R405_24A_20%
Security Classification
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Issued Date
2008/09/15
Deciphered Date
2012/07/11
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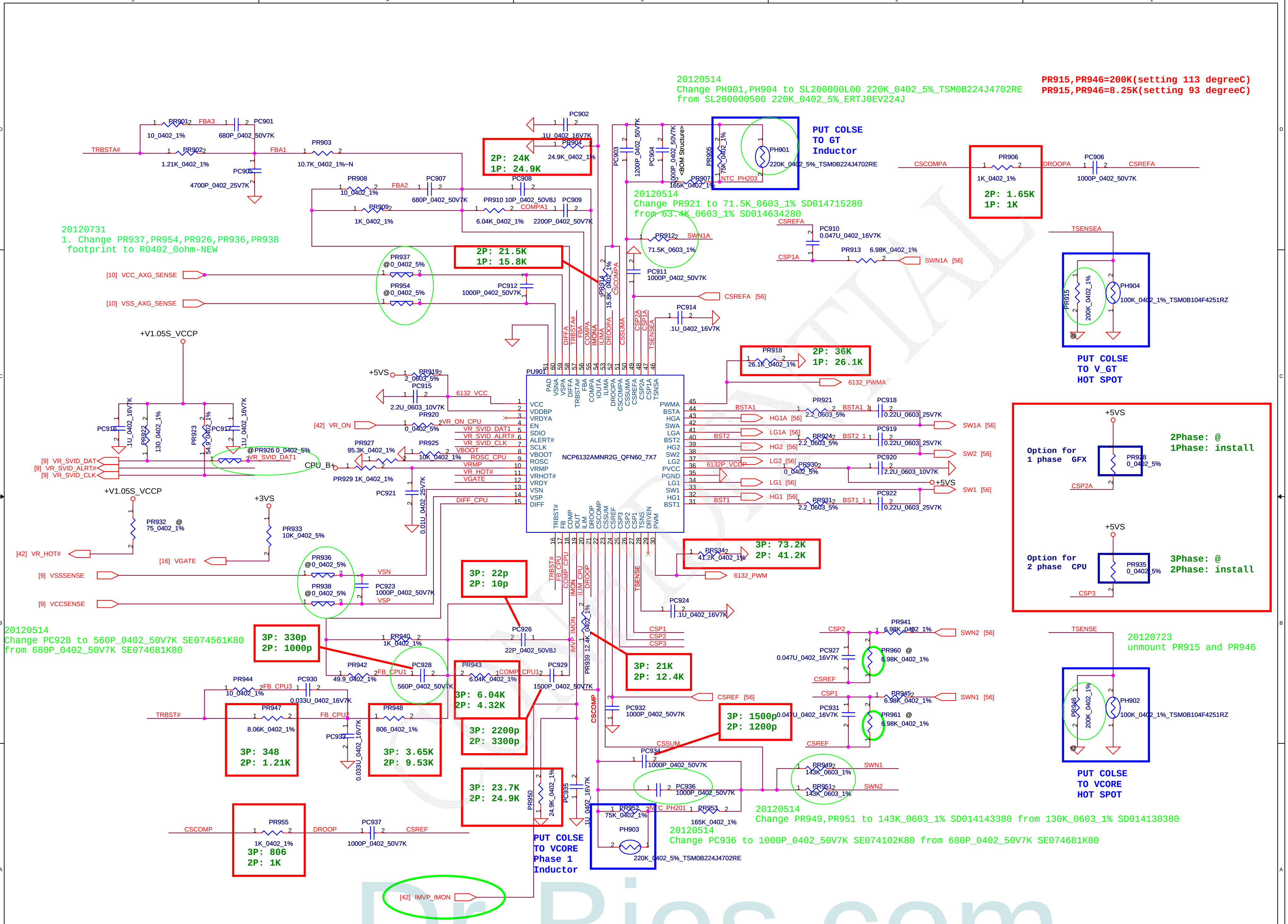
20120514
Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE
from SL200000500 220K_0402_5%_ERTJ0EV224J
PR915,PR946=200K(setting 113 degreeC)
PR915,PR946=8.25K(setting 93 degreeC)
PUT COLSE
TO GT
Inductor
20120514
Change PR921 to 71.5K_0603_1% SD014715280
from 63.4K_0603_1% SD014634280
20120731
1. Change PR937,PR954,PR926,PR936,PR938
footprint to R0402_0ohm-NEW
2P: 24K
1P: 24.9K
2P: 1.65K
1P: 1K
2P: 21.5K
1P: 15.8K
2P: 36K
1P: 26.1K
PUT COLSE
TO V_GT
HOT SPOT
NCP6132AMNR2G_QFN60_7X7
Option for
1 phase GFX
2Phase: @
1Phase: install
Option for
2 phase CPU
3Phase: @
2Phase: install
3P: 73.2K
2P: 41.2K
3P: 22p
2P: 10p
20120514
Change PC928 to 560P_0402_50V7K SE074561K80
from 680P_0402_50V7K SE074681K80
3P: 330p
2P: 1000p
3P: 21K
2P: 12.4K
20120723
unmount PR915 and PR946
3P: 6.04K
2P: 4.32K
3P: 2200p
2P: 3300p
3P: 1500p
2P: 1200p
3P: 348
2P: 1.21K
3P: 3.65K
2P: 9.53K
3P: 23.7K
2P: 24.9K
PUT COLSE
TO VCORE
HOT SPOT
3P: 806
2P: 1K
PUT COLSE
TO VCORE
Phase 1
Inductor
20120514
Change PR949,PR951 to 143K_0603_1% SD014143380 from 130K_0603_1% SD014130380
20120514
Change PC936 to 1000P_0402_50V7K SE074102K80 from 680P_0402_50V7K SE074681K80

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Issued Date	2009/12/01	Deciphered Date	2012/07/11

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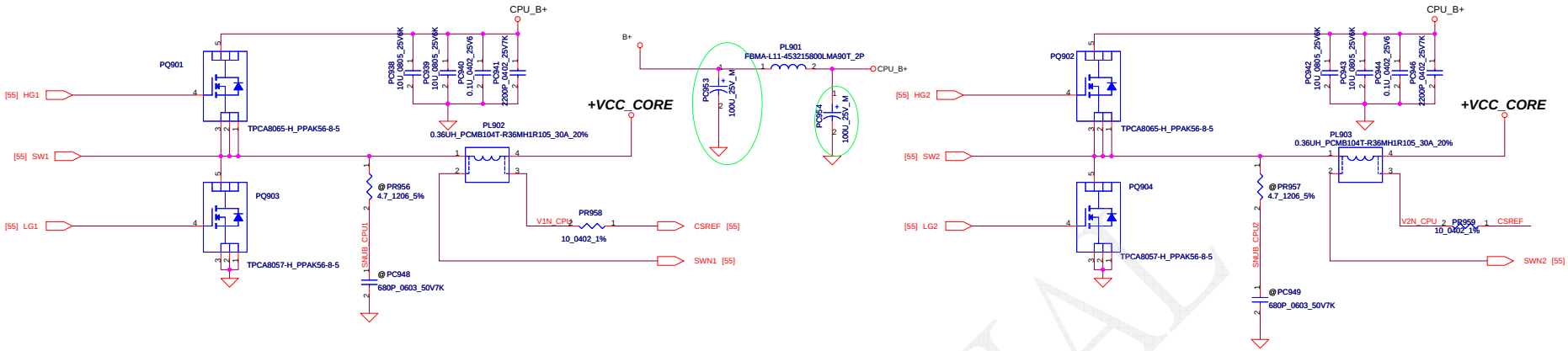
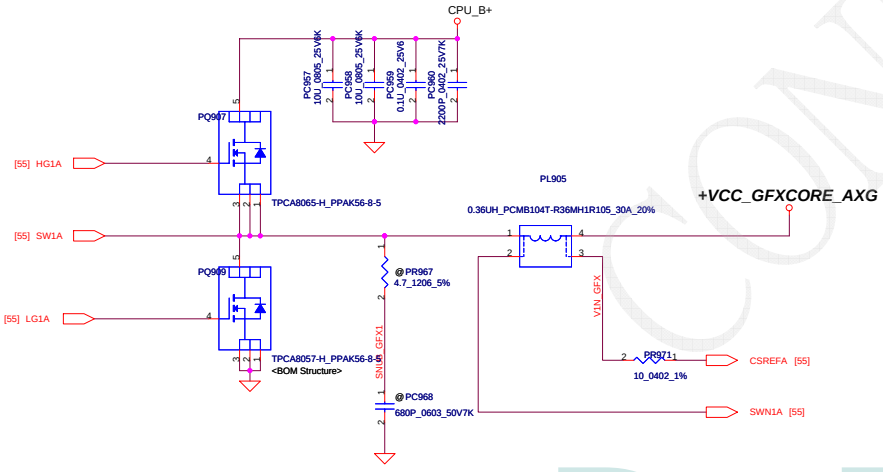
Date: Monday, December 17, 2012 |



DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
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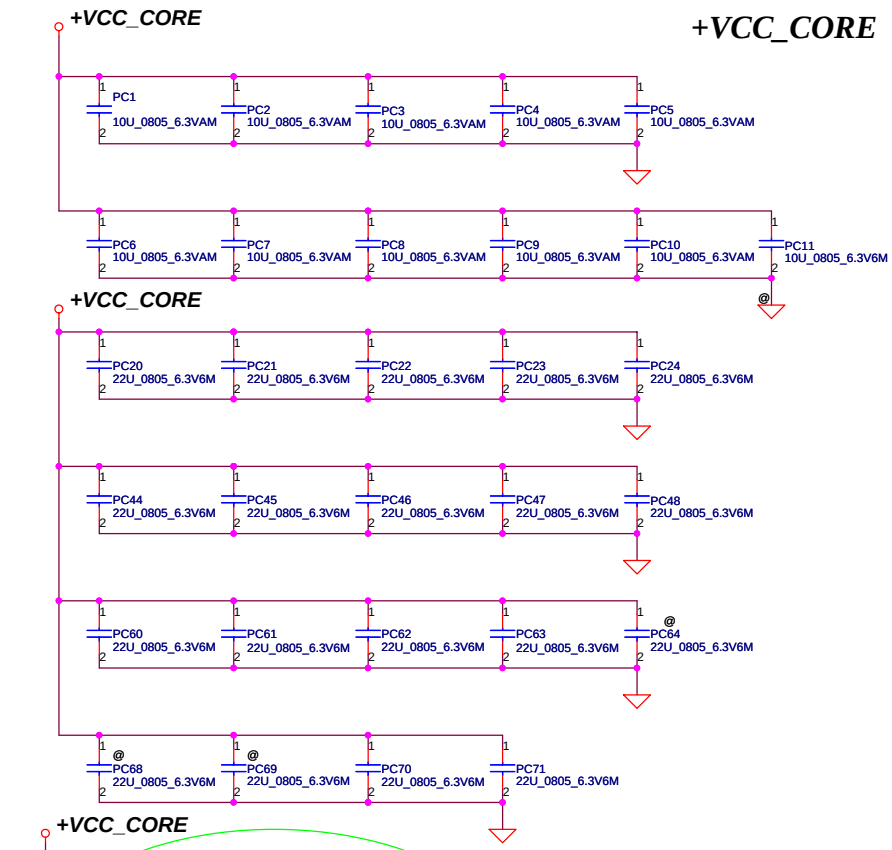
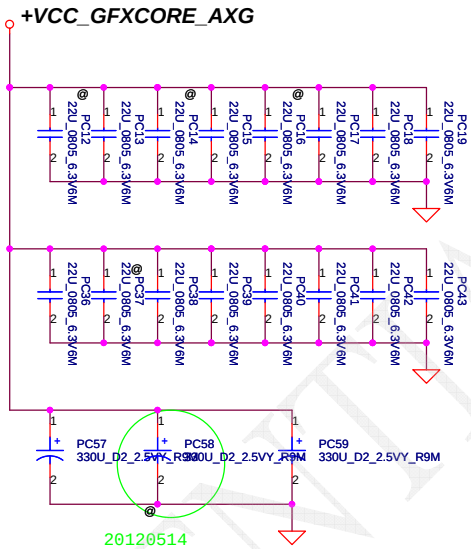


20120514
Unpop PC75
Change PC72,PC73,PC74,PC76 to SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680

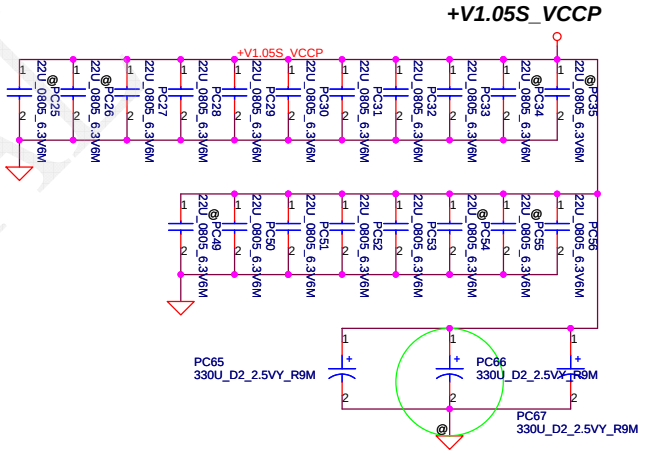
20120318
Change PC72,PC73,PC74,PC75 to 2 pin footprint



20120514
Unpop PC58

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



20120514
Unpop PC66

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For EC net name	P48	PR206 change pull high voltage to +EC_VCCA from +3VLP	20120316	EVT
2	Intersil advise	P54	1.Change PR848 to 1.47K SD000009480 from 1.15K 2.Unmount PC864	20120316	EVT
3	VGA IMON setting	P54	Change PR853 to 11K SD034110280 from 11.3K	20120316	EVT
4	set OCP is 56A	P54	Change PR869 to 1.58K (SD00000SJ80) from 1K	20120316	EVT
5	For 1.5V current	P51	Add PJ507 for 1.5V	20120321	EVT
6	For B+ layout	P55 P50 P51 P50	1.Change PC954 pull high to CPU_B+ from B+ 2.Change 3/5VALWP B+ input netname to CPU_B+ 3.Change 1.5VALWP B+ input netname to CPU_B+ 4.Change PR411 netname to CPU_B+ from B+	20120321	EVT
7	For HW net name	P53 P54	1.Change +1.05S_VCCP netname to +V1.05S_VCCP 2.Change PQ802.5 netname to +V1.05S_VCCP from +1.05VS	20120330	EVT
8	For HW power sequence	P54	1.Add control PU801 pin GPU_PWR_EN and reserve PR956 0_0402_5% 2.Change PR820 to SD034150380 150K_0402_1% from 100K 3.Change PC810 to SE071101J80 100P_0402_50V8J from 0.1u	20120330	EVT
9	For Intersil advise	P54	Change PR853 pull down netname to gnd	20120409	EVT
10	For IMON design	P55	Change PU901 to NCP6132A from ISL95836	20120412	EVT
11	For layout design	P54	1.Del PJ803 PJ804 2.Change net name to VGACORE from VGACOREP	20120511	DVT
12	For 1.05V, GFX_CORE,CPU_CORE design fine tune	P57	Unpop PC58, PC66,PC75 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
13	For CPU_CORE design fine tune and ON advise	P57	Change PC72,PC73,PC74,PC76 to S POLY C 330U 2V M D2 ESR9M SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
14	For CPU_CORE design fine tune and ON advise	P55	1.Change PC928 to 560P_0402_50V7K SE074561K80 from 680P_0402_50V7K SE074681K80 2.Change PR949,PR951 to 140K from 130K 3.Change PR912 to 71.5K_0603_1% SD014715280 from 63.4K_0603_1% SD014634280 4.Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
15	For material EOL	P55	Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
16	For HW VGA power sequence	P54	Add PR972 SD028000080 0_0402_5% Unmount PD801 Change PR820 to 0_0402_5% SD028000080 from 150K_0402_1% SD034150380 Unmount PC810	20120516	DVT

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Item	Reason for change	PG#	Modify List	Date	Phase
17	For HW reset function	P50	1.Add PR420 SD028000080 0_0402_5% for reserve 2 reserve.PR419 and PR420	20120606	PVT
18	For ACDET function	P49	1.Change PR313 to 60.4K_0603_1% SD014604280 from 64.9K_0603_1% SD014649280	20120615	PVT
19	For HW Grenn clock UMA sku trial tun	P47	1. unmount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120625	PVT
20	For ACDET function	P49	1.Change PR313 to 59K_0603_1% SD014590280 from 60.4K_0603_1% SD014604280	20120705	PVT
21	For VR_HOT	P55	1.unmount PR915 and PR946	20120705	PVT
22	For HW Grenn clock	P47	1. mount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120723	SVT
23	For material issue	P51	1.Change PU502 to SA00004CY10 S IC RT8061AZQW WDFN 10P PWM from SA00003RU00 S IC SY8033BDBC DFN 10P SINGLE BUCK	20120723	SVT

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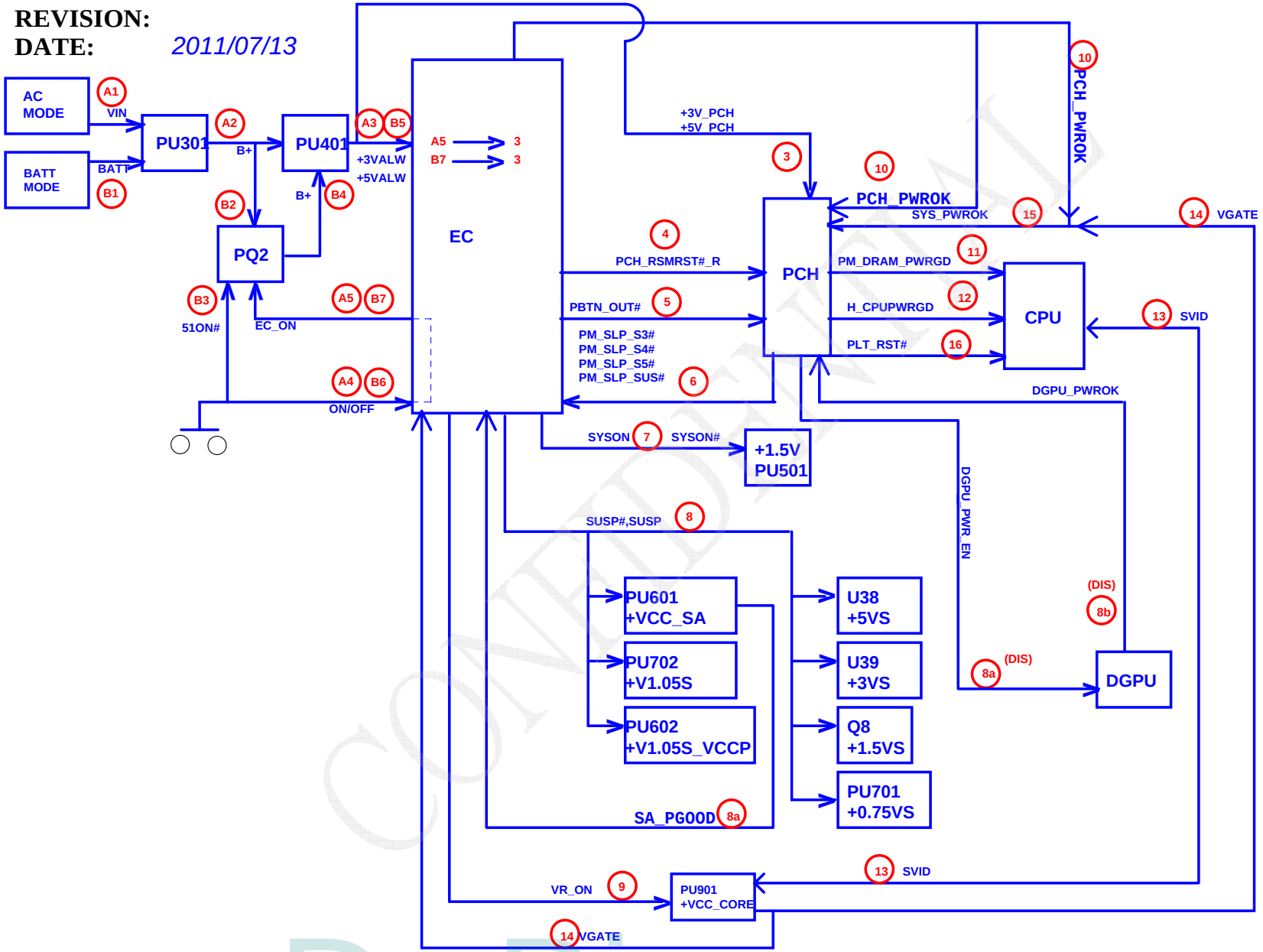
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial			5/7	DVT
2	For Green CLK and Crystal co-lay better layout	P14 P15 P23	Delete R176,R1381 and RV232	5/7	DVT
3	For Change Audio Woofer MOSFET from Dual to single channel	P15	Changer Part from SB00000EO10 to SB00000EN00	5/7	DVT
4	For OVERT# Glitch issue at Power on status	P23	Add QV9	5/7	DVT
5	For BT&WLAN Combo Card	P36	to modify R897 value from 0 ohm to 1K ohm add BT_DISABLE_F_R on JWLN1.51 add R5580	5/8	DVT
6	For Factory request and cost down LVDS PIN Define	P33	To Modify LVDS PIN Define	5/8	DVT
7	For USB Charger mode control request	P45 P42	To Add PWRSHARE_EN_R on U31.38 To Add EC_PWRSHARE_EN# on U31.74 add R5577 and R5578, delete CHG_ON#	5/8	DVT
8	To change Reset IC G601	P42	to change R4959 value from 200K ohm to 0 ohm add R5579 0 ohm	5/8	DVT
9	Reserved Touch Screen Power Control	P42 P43	add R5581,C1331,R5572,R5583,R5584 and Q156 add EC_TS_ON on U31.66 add +3VS_TS,+3VS_TS_R	5/8	DVT
10	To change Speaker PIN define for ME routing request	P41	SPK_L2+ R1556 net in JSPK1.1 SPK_L1- R1554 net in JSPK1.2 SPK_R1- R1555 net in JSPK1.3 SPK_R2+ R1553 net in JSPK1.4	5/8	DVT
11	for Realtek Vendor recommand	P41	R1123,C1134 close to U50.47 R5582,R1559 and C1135 Close to U73.1 EXT_MIC_R	5/8	DVT
12	for ME request	P39	To Modify H21,H7,H18 PCB Footprint as below H21 from H_3P3 to H_4P6 H7 from H_2P8 to H_3P0 H18 from H_3P3 to H_3P9N	5/8	DVT
13	for LAN Clock be better	P37	change C990 value from 5PF to 0 ohm.	5/9	DVT
14	for Audio Vendor recommand	P43	change JUSB3.11 from GND to +3VS change JUSB3.12 from +3VS to AGND	5/10	DVT
15	for Crystal finetune Capacitor	P43	C180,C181 from 18PF to 12PF	5/16	DVT
16	for DVT Board ID request	P42	R695 from 33K to 18K	5/17	DVT
17	for PVT request	P37	Change Reference from C990 to R5585	5/23	PVT
18	for Surge request	P38	C1325,C1326,C1327 change package from 0402 to 0603	5/23	PVT
19	for Reset IC function	P42, P50,P43	add R612,PR420,R4960,R4961 Delete R4959	5/24	PVT

Item	Reason for change	PG#	Modify List	Date	Phase
20	for USB2.0 Port 0 TLC fine tune	P45	add R1170,R1171	5/29	PVT
21	for INTEL Combo card BT off	P36 P19	add R893,R894 1Kohm ,change R897 to 0 ohm change net name from PCH_GPIO36 to INTEL_BT_OFF# add INTEL_BT_OFF#_R JWLN1.51 chnage NET from BT_DISABLE_F_R to INTEL_BT_OFF#_R	6/5	PVT
22	for LVDS prevent short EC DISPOFF#	P33	R447 change value from no stuff to stuff 0ohm	6/12	PVT
23	for VSB and PCH Power rail control issue	P42 P46	add R5586 and R5591	6/21	PVT
24	add common choke for USB port 8, port 9	P43	add L78,L79,R5587,R5588,R5589,R5590	6/21	PVT
25	no need reserved C1330	P38	remove C1330	6/21	PVT
26	for PVT Board ID request	P42	R695 from 18K to 8.2K	6/21	PVT
27	for Surge modify	P38	DL6 change Part from SCV00001C00 to SCV00001D00	6/21	PVT
28	for Crystal finetune Capacitor	P14 P37	C180,C181 change value from 12P to 18P C1204,C1205 change value from 27P to 12P	6/25	PVT
29	for SMT Request	P23	LV7 change value from KC_FBMA-10-100505-300T_2P to 0ohm_0402	07/11	SVT
30	for Vendor recommand	P23	add RG10 0ohm	07/19	SVT
31	for Touch Screen request	P43	add R5592,R721 0 ohm,	07/25	SVT
32	for Green CLK request	P44	add QG1,RG13,CG10	8/1	SVT
33	for LED Brightness	P44	modify R623,R765 value from 300 ohm to 560 ohm	8/1	SVT
34	for reduce component count	P10 P	Modify footprint to jumper R69 to J14 R277 to J16	8/1	SVT
35	for SVT Board ID request	P42	R695 from 8.2K to 0 ohm	8/1	SVT

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Item	Reason for change	PG#	Modify List	Date	Phase
36	for EMI Request	P45	not stuff R1154,R1155,R1156,R1157 Stuff L68,L70	8/1	SVT
37	for Remove ODD Zero Power Function	P40	Q99,Q100 R552,R675,C607 not stuff on MB		