

Compal Confidential

STORM M/B Schematic

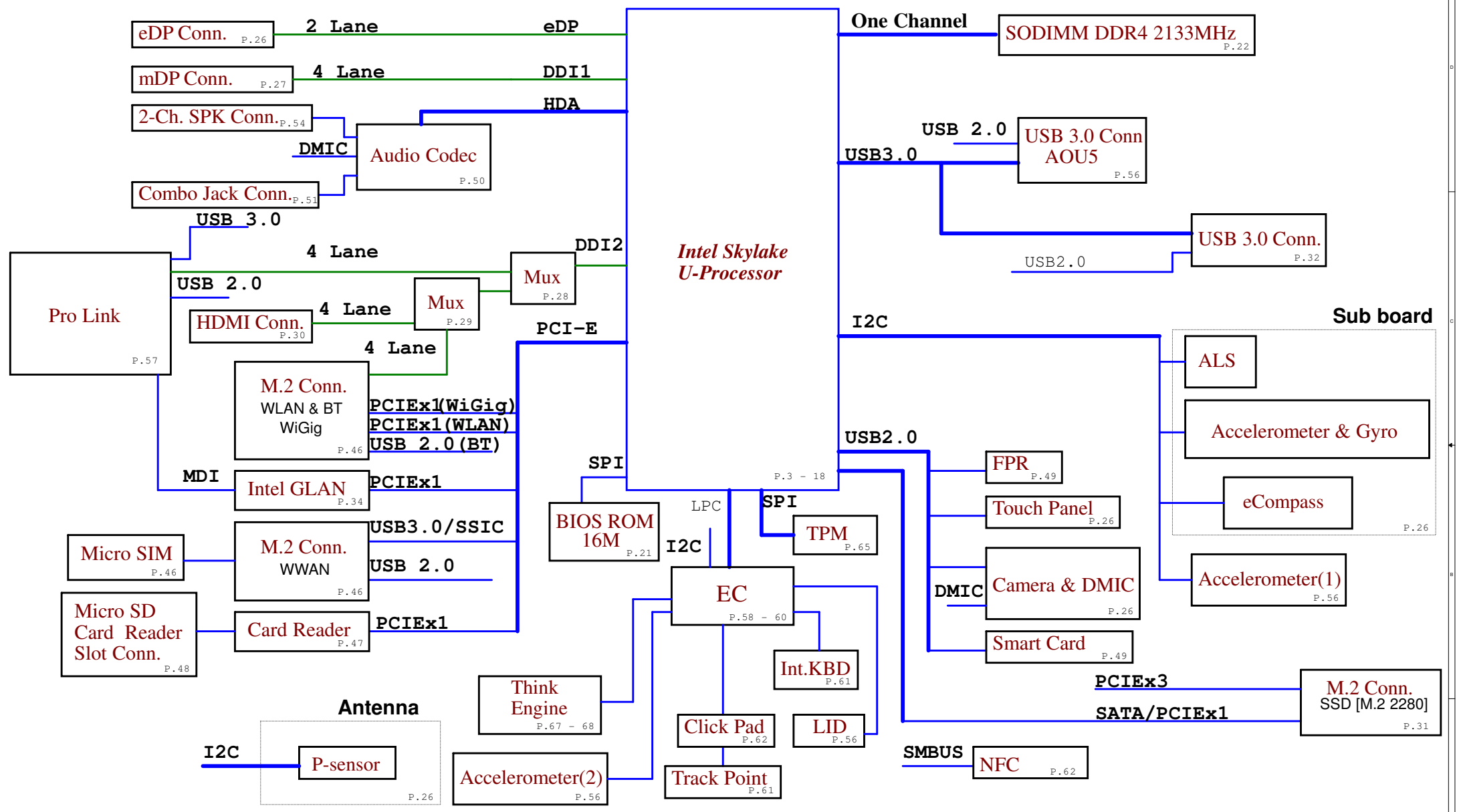
LA-C581P

Rev: 1.0_D

2015.08.13

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	COVER PAGE	
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STORM Block-Diagram



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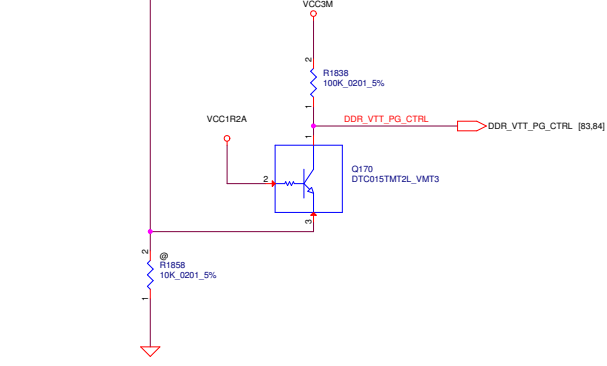
TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AY33	DDR0_DQ[41]	DDR1_DQ[9]
	AW33	DDR0_DQ[42]	DDR1_DQ[10]
	BB35	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]



TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]



TABLE

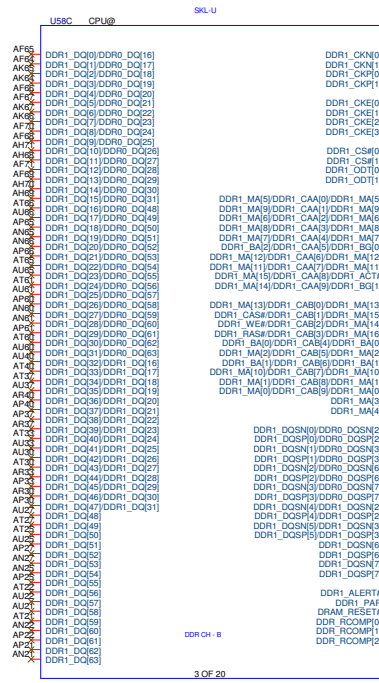
Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AP30	DDR1_DQ[46]	DDR1_DQ[30]
			DDR1_DQ[47]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
AT22	DDR1_DQ[56]	DDR1_DQ[56]	
AU22	DDR1_DQ[57]	DDR1_DQ[57]	
AU21	DDR1_DQ[58]	DDR1_DQ[58]	
AT21	DDR1_DQ[59]	DDR1_DQ[59]	
AN22	DDR1_DQ[60]	DDR1_DQ[60]	
AP22	DDR1_DQ[61]	DDR1_DQ[61]	
AP21	DDR1_DQ[62]	DDR1_DQ[62]	
AN21	DDR1_DQ[63]	DDR1_DQ[63]	

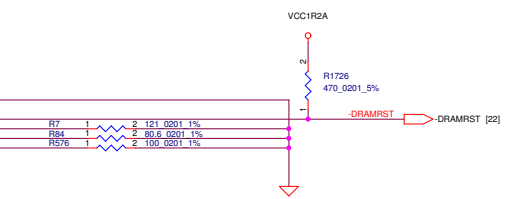


TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG70	DDR1_DQSN[1]	DDR0_DQSN[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

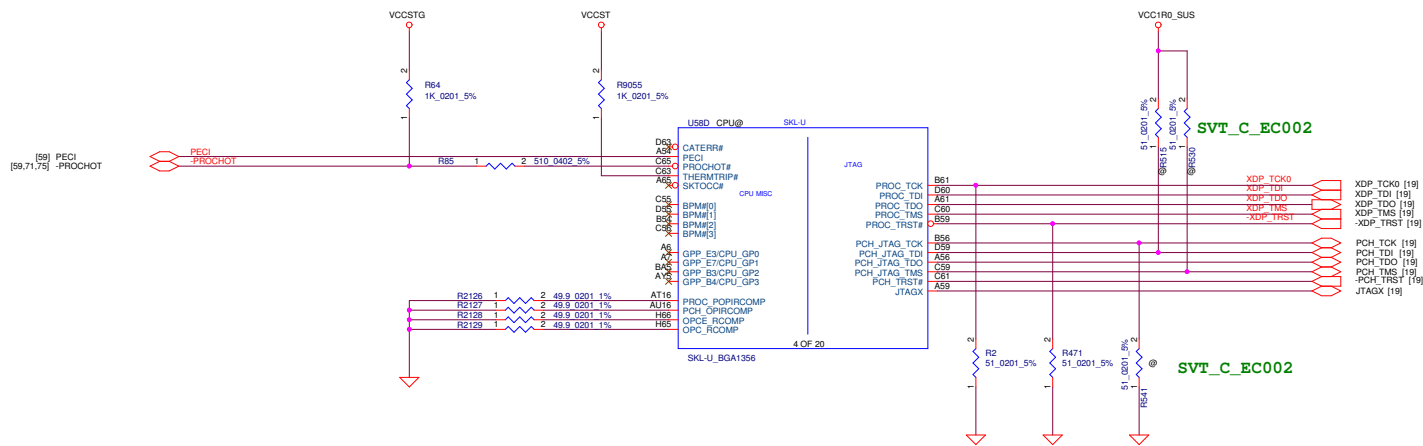
Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_BA[0]	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[1]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_BA[0]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[11]	DDR1_CAB[8]	DDR1_MA[11]
BA46	DDR1_MA[3]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[4]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]



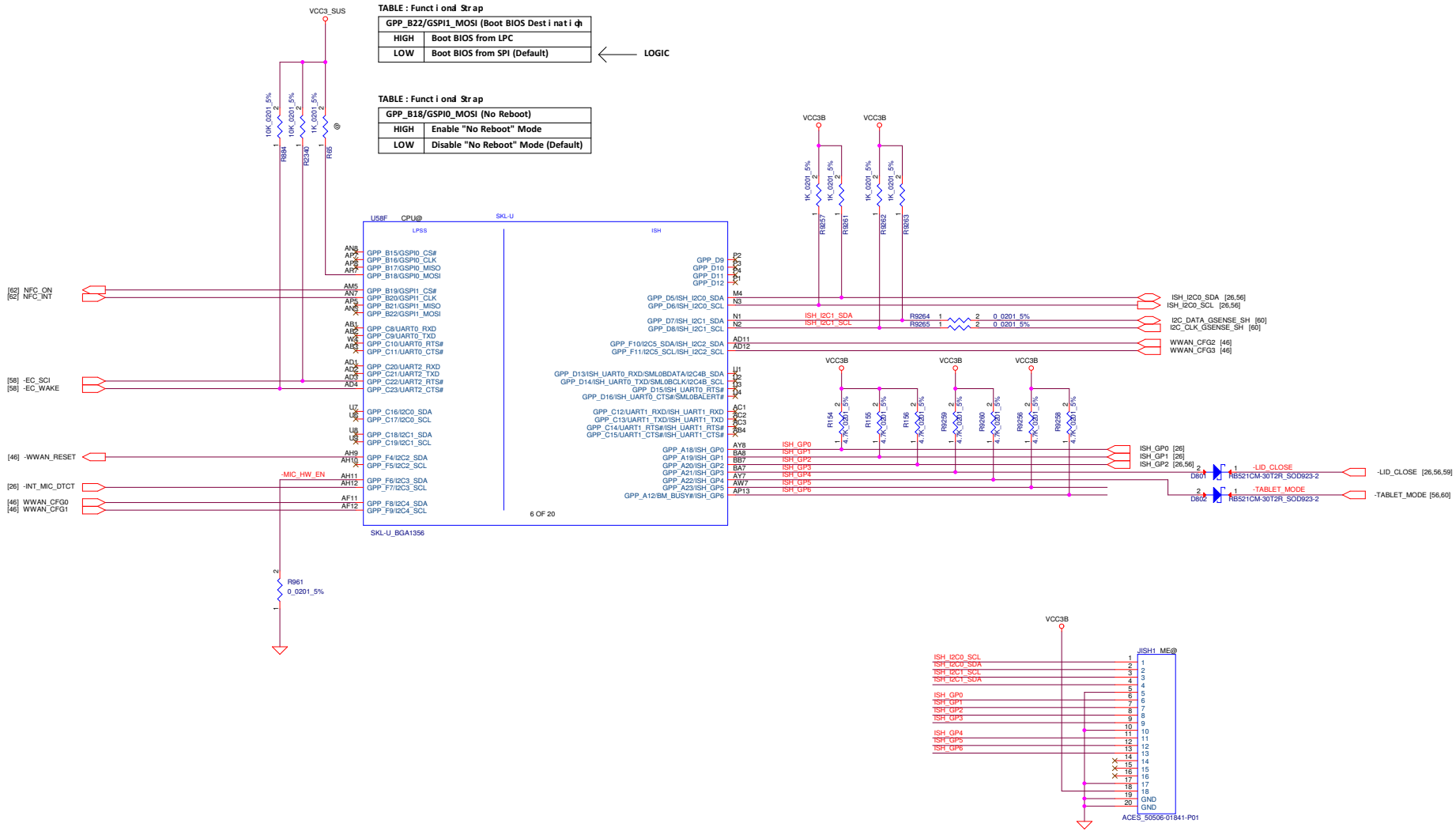
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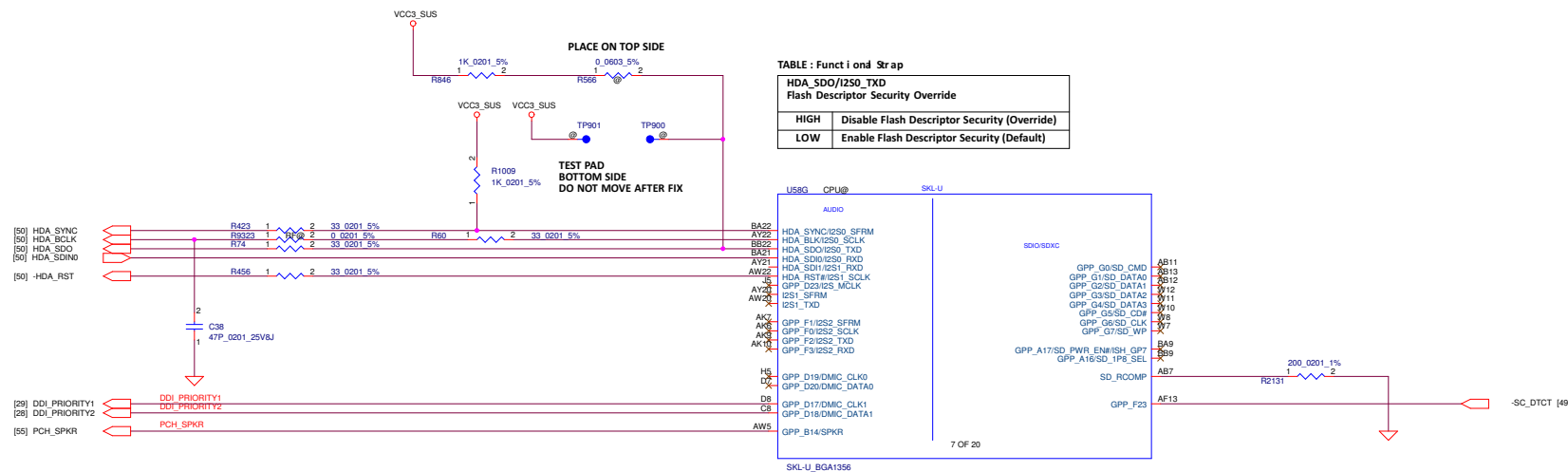


TABLE : Function and Strap

HDA_SDO/I2SD_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

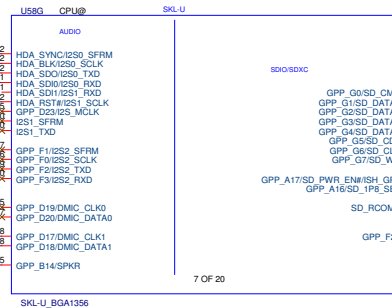


TABLE : Function and Strap

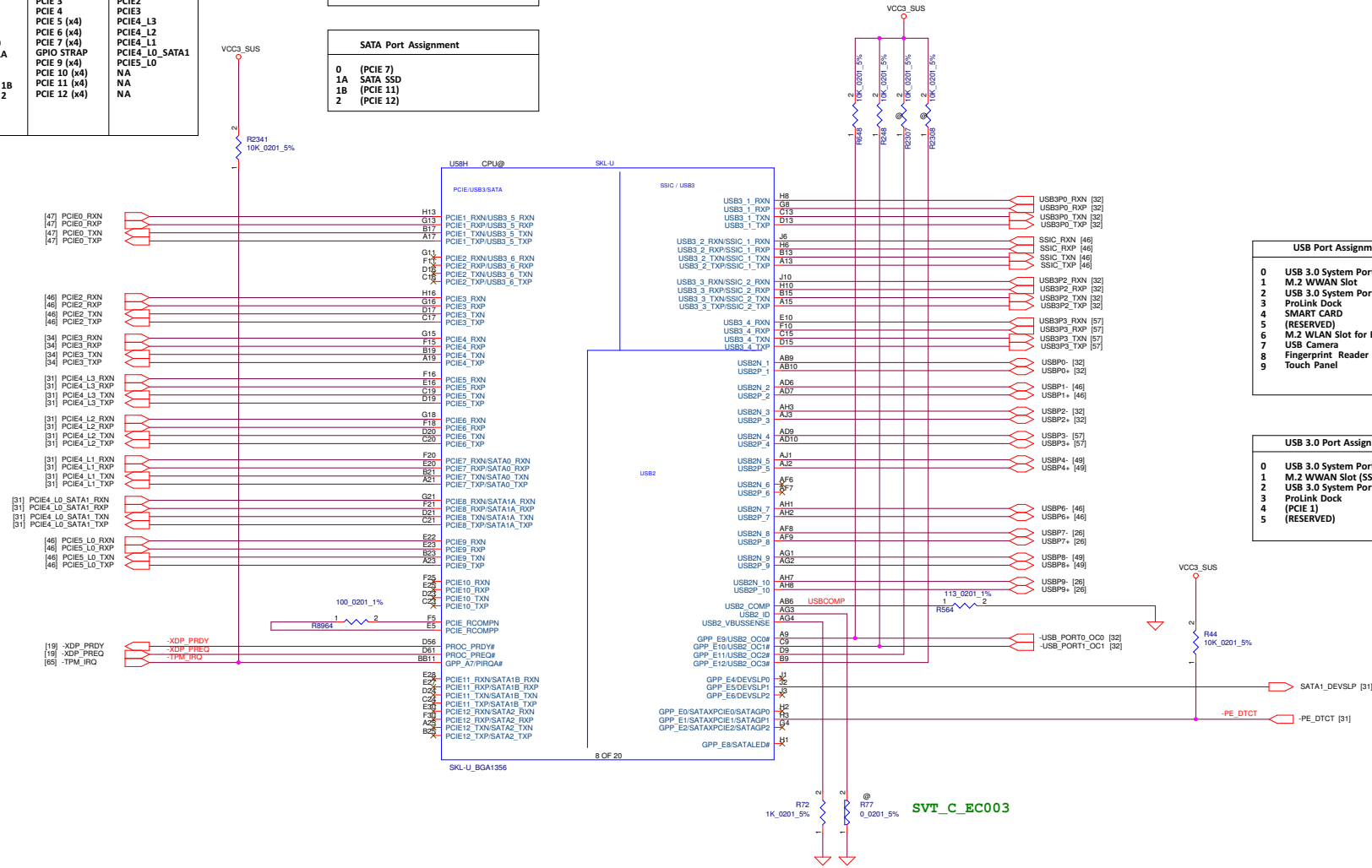
GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

← LOGIC

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	SSIC	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE 2	USB3 6	USB3P5
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE2
Port 8	PCIE 4 (GbE)	PCIE 4	PCIE3
Port 9	PCIE 5 (GbE)	PCIE 5 (x4)	PCIE4_L3
Port 10	PCIE 6	PCIE 6 (x4)	PCIE4_L2
Port 11	PCIE 7/SATA 0	PCIE 7 (x4)	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_LO_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE5_L0
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	NA
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	NA
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	NA

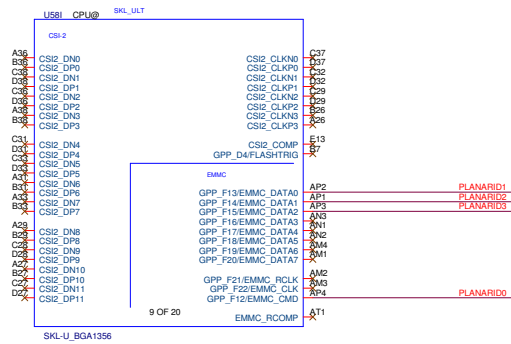
PCIe Port Assignment	
0	Media Card Controller (USB3 6)
1	M.2 WLAN Slot 0 for WLAN
2	SSIC
3	GbE PHY
4 (x4)	PCIe SSD
5_L0	M.2 WLAN Slot 1 for WiFi

SATA Port Assignment	
0	(PCIe 7)
1A	SATA SSD
1B	(PCIe 11)
2	(PCIe 12)



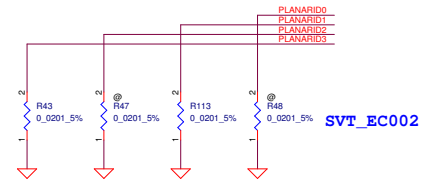
USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	M.2 WWAN Slot
2	USB 3.0 System Port
3	ProLink Dock
4	SMART CARD
5	(RESERVED)
6	M.2 WLAN slot for BT
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	M.2 WWAN Slot (SSIC)
2	USB 3.0 System Port
3	ProLink Dock
4	(PCIe 1)
5	(RESERVED)



TABLE

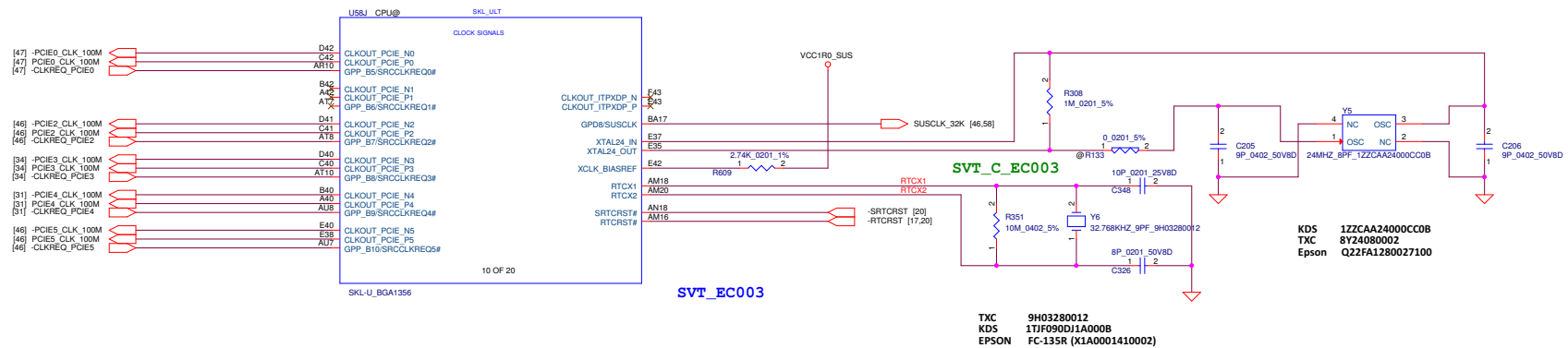
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM



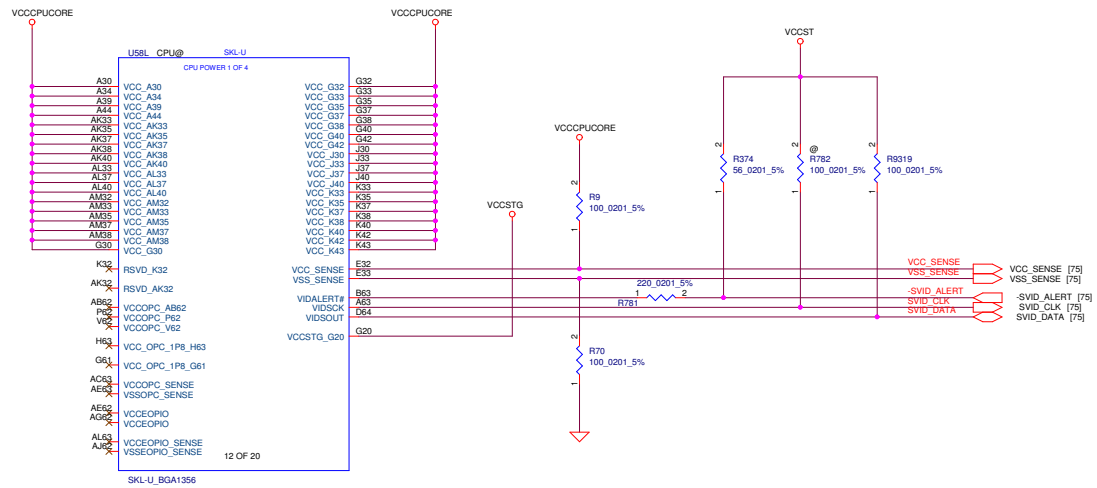
TABLE

LEVEL	PLANARID[3..0]
PDV	0001B
FVT	0010B
SIT	0011B
SIT-R	0100B
SVT	0101B

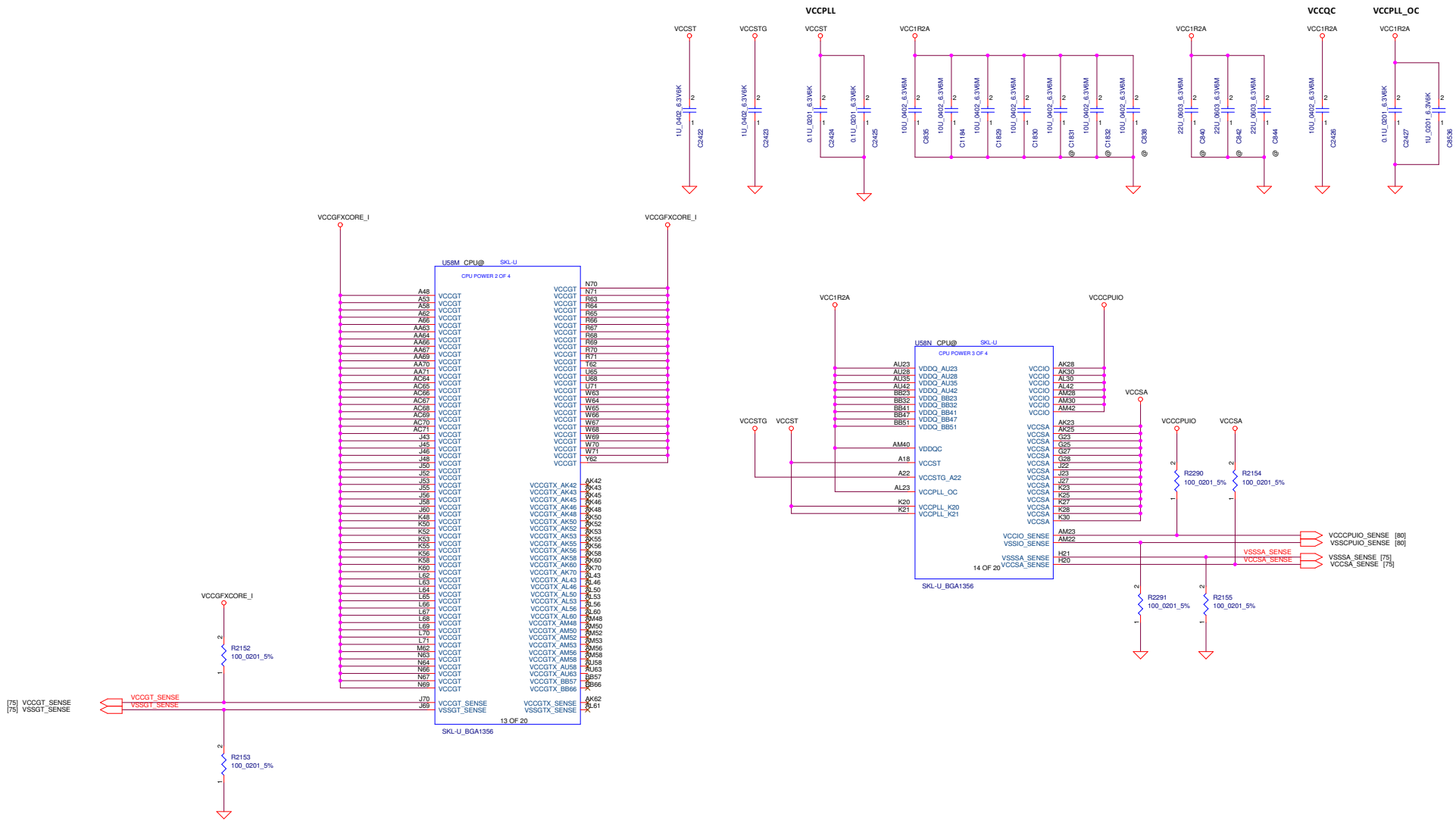
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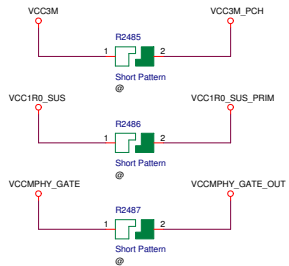


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Compal Electronics, Inc.
CPU : CPU POWER (2/2)

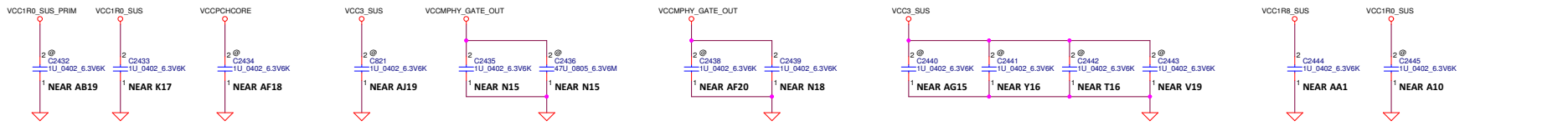
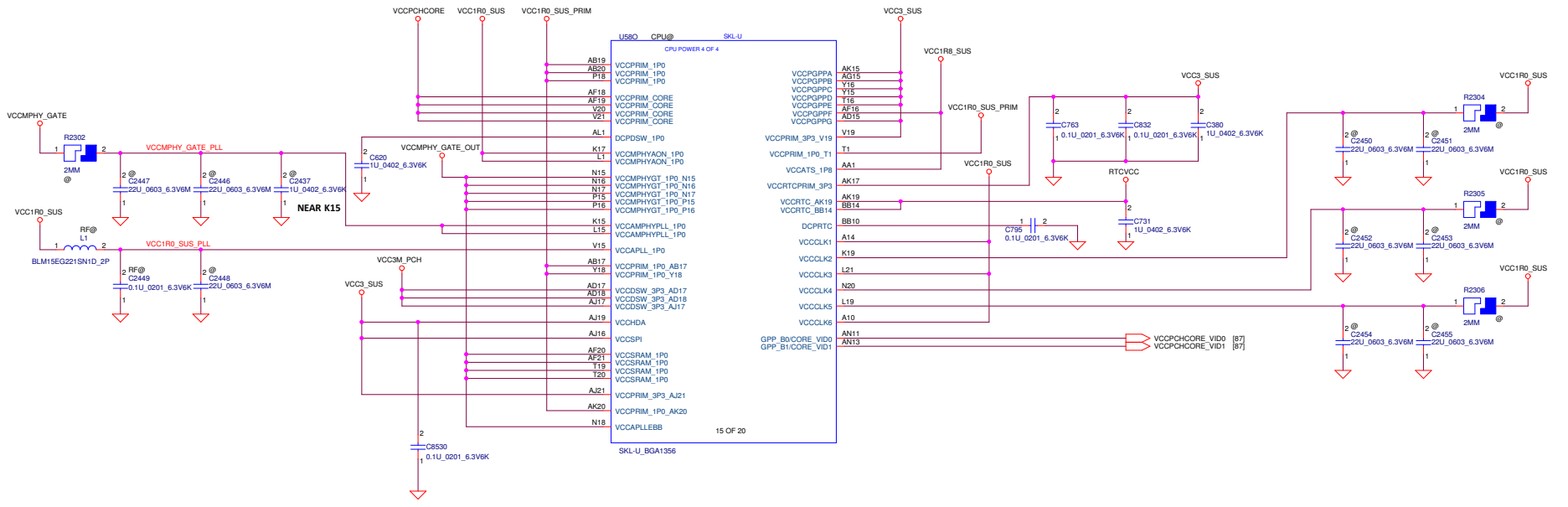
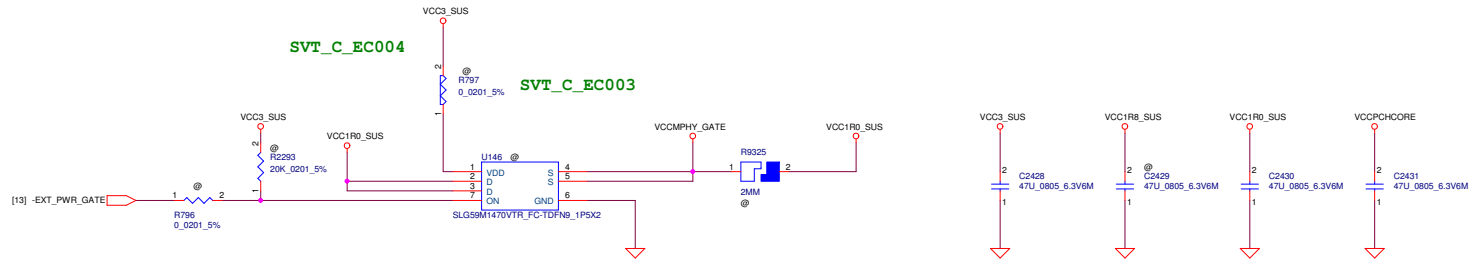
SVT_C_EC005

Short Pattern: R2485, R2486, R2487

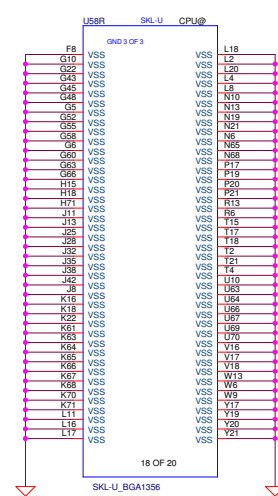
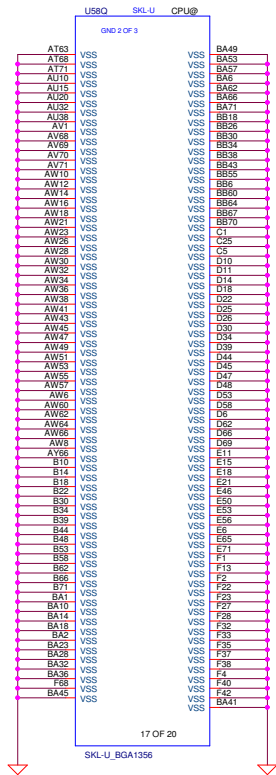
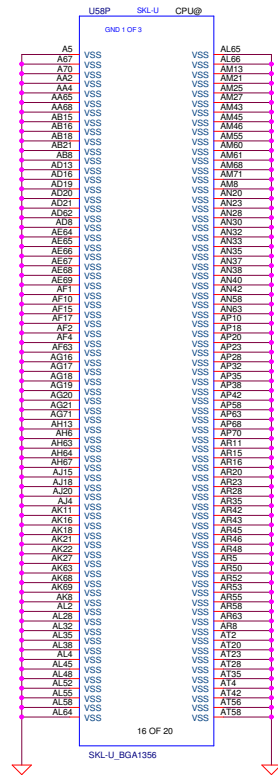


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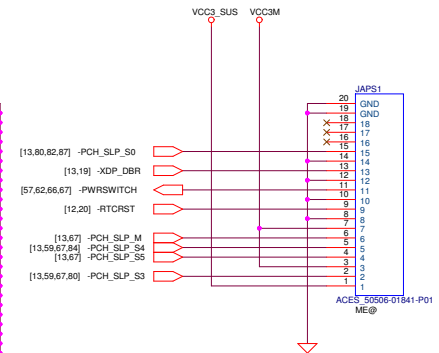
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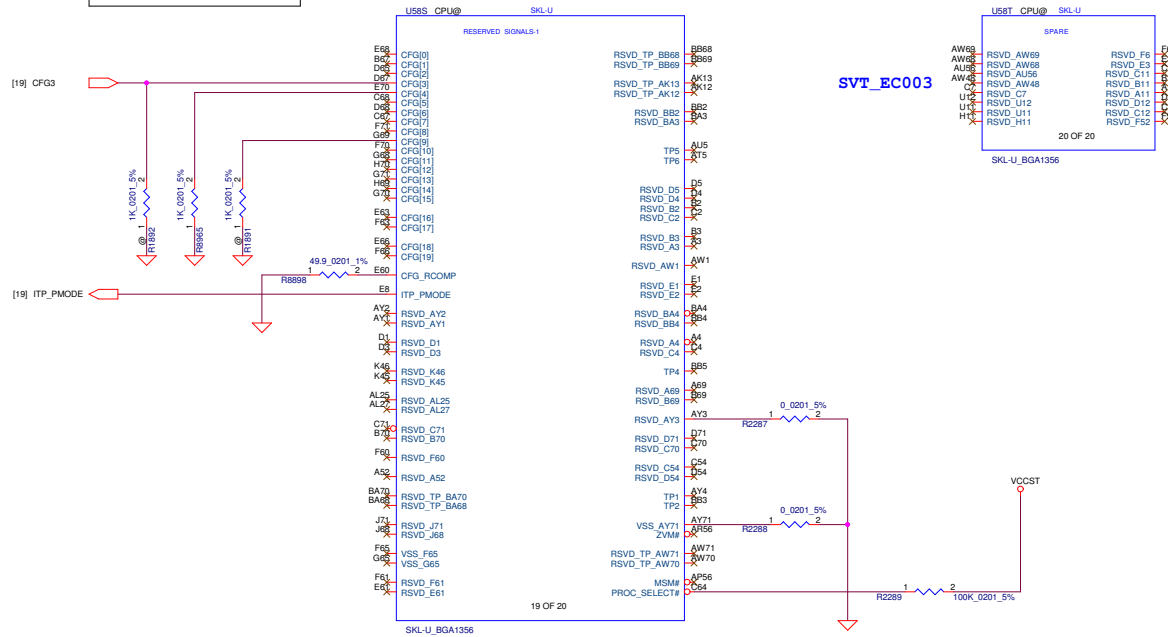
APS/PETS Interface



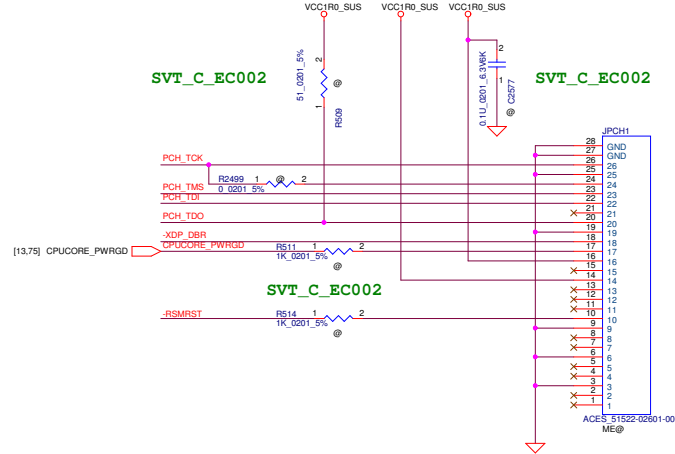
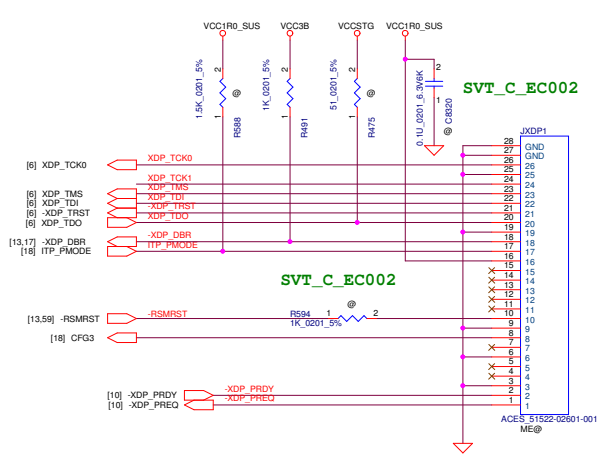
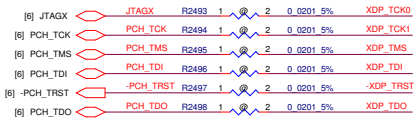
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TABLE

<p>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted</p> <p>1 : No Stall</p> <p>0 : Stall</p>
<p>CFG3 : MSR Privacy Bit Feature</p> <p>1 : MSR (C80h) bit[0] set, t1g</p> <p>0 : MSR (C80h) bit[0] overridden</p>
<p>CFG4 : eDP Enable</p> <p>1 : Disabled</p> <p>0 : Enabled</p>
<p>CFG9 : SVID Bus Communication</p> <p>1 : Enabled</p> <p>0 : Disabled</p>



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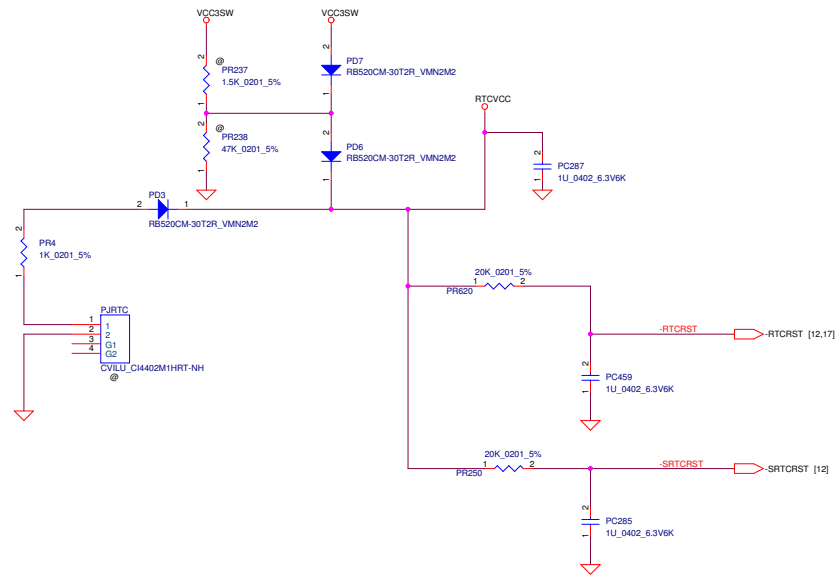


TABLE

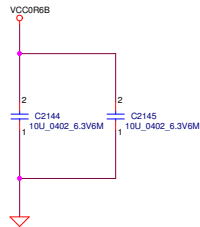
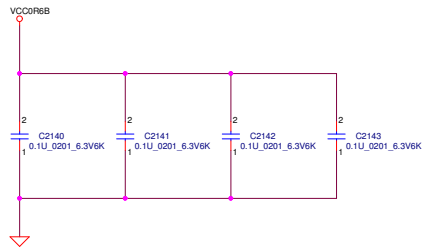
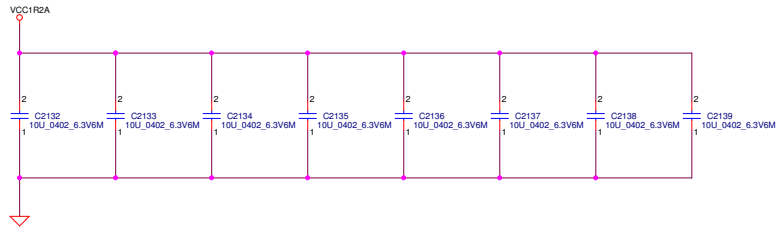
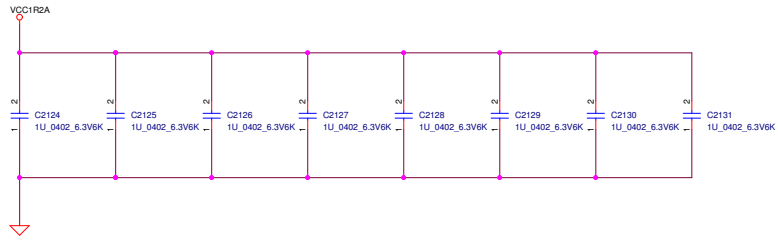
	Individual Port	Merged Port	DCI 2.0 w/o Connector
R2	ASM	ASM	ASM
R471	ASM	NO_ASM	NO_ASM
R541	ASM	NO_ASM	NO_ASM
R515	ASM	NO_ASM	NO_ASM
R530	ASM	NO_ASM	NO_ASM
R475	ASM	ASM	ASM
J8	ASM	ASM	NO_ASM
C8320	ASM	ASM	NO_ASM
R491	ASM	ASM	ASM
R588	ASM	ASM	NO_ASM
R594	ASM	ASM	NO_ASM
R2499	NO_ASM	NO_ASM	NO_ASM
R509	ASM	NO_ASM	NO_ASM
J9	ASM	ASM	NO_ASM
C2577	ASM	ASM	NO_ASM
R511	ASM	ASM	NO_ASM
R514	ASM	ASM	NO_ASM
R2493	NO_ASM	ASM	ASM
R2494	NO_ASM	ASM	NO_ASM
R2495	NO_ASM	ASM	ASM
R2496	NO_ASM	ASM	ASM
R2497	NO_ASM	ASM	ASM
R2498	NO_ASM	ASM	ASM

↑
LOGIC

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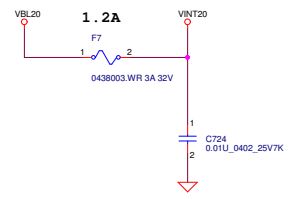
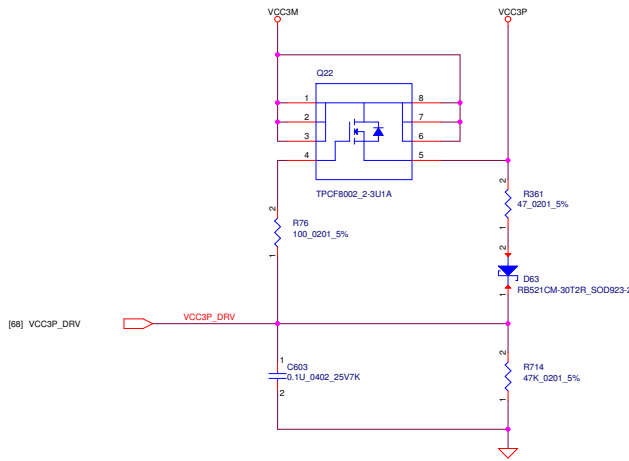
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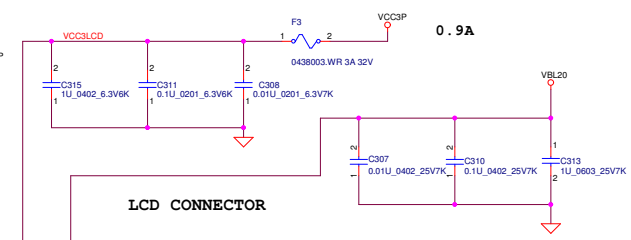
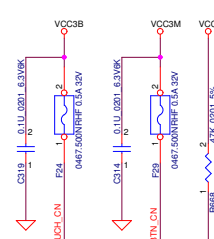
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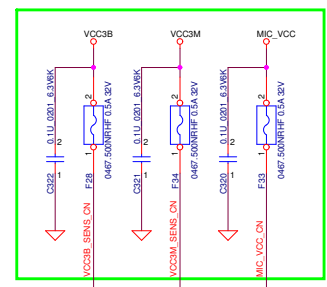
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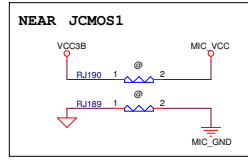
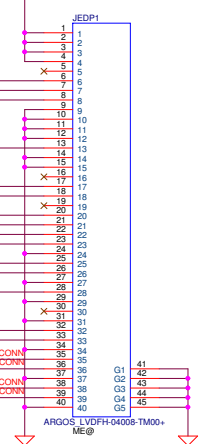
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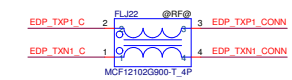
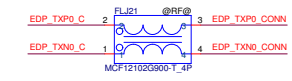
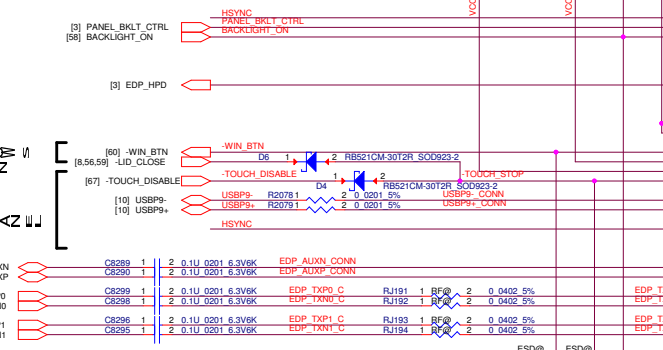
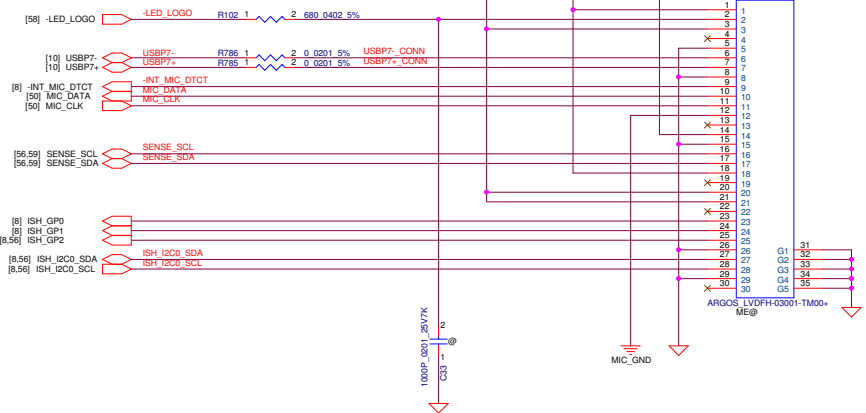
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LCD CONNECTOR



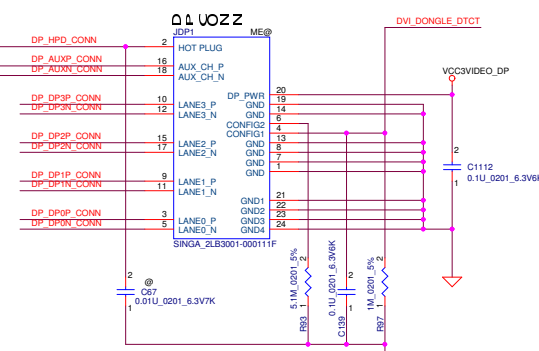
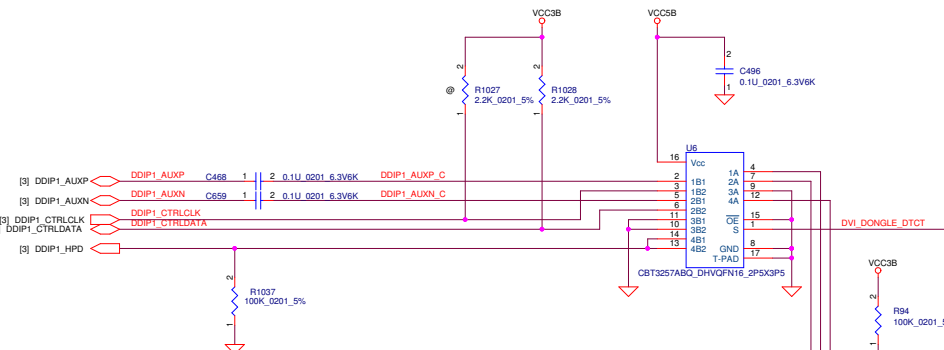
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 UM UEA BO<C<D
 A-VLZ VO R
 WLZ VO R BO<C<D



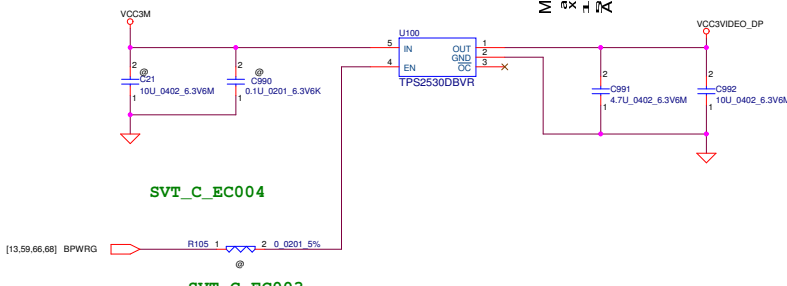
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Q & W V H I E D L Z W R D L U O Z Z

[3] DDIP1_3N	C339	1	2	0.1U_0201_6.3V6K	DP_DP3N_CONN
[3] DDIP1_3P	C339	1	2	0.1U_0201_6.3V6K	DP_DP3P_CONN
[3] DDIP1_2N	C312	1	2	0.1U_0201_6.3V6K	DP_DP2N_CONN
[3] DDIP1_2P	C312	1	2	0.1U_0201_6.3V6K	DP_DP2P_CONN
[3] DDIP1_1N	C277	1	2	0.1U_0201_6.3V6K	DP_DP1N_CONN
[3] DDIP1_1P	C276	1	2	0.1U_0201_6.3V6K	DP_DP1P_CONN
[3] DDIP1_0N	C218	1	2	0.1U_0201_6.3V6K	DP_DP0N_CONN
[3] DDIP1_0P	C226	1	2	0.1U_0201_6.3V6K	DP_DP0P_CONN



Z W R D L U O Z Z



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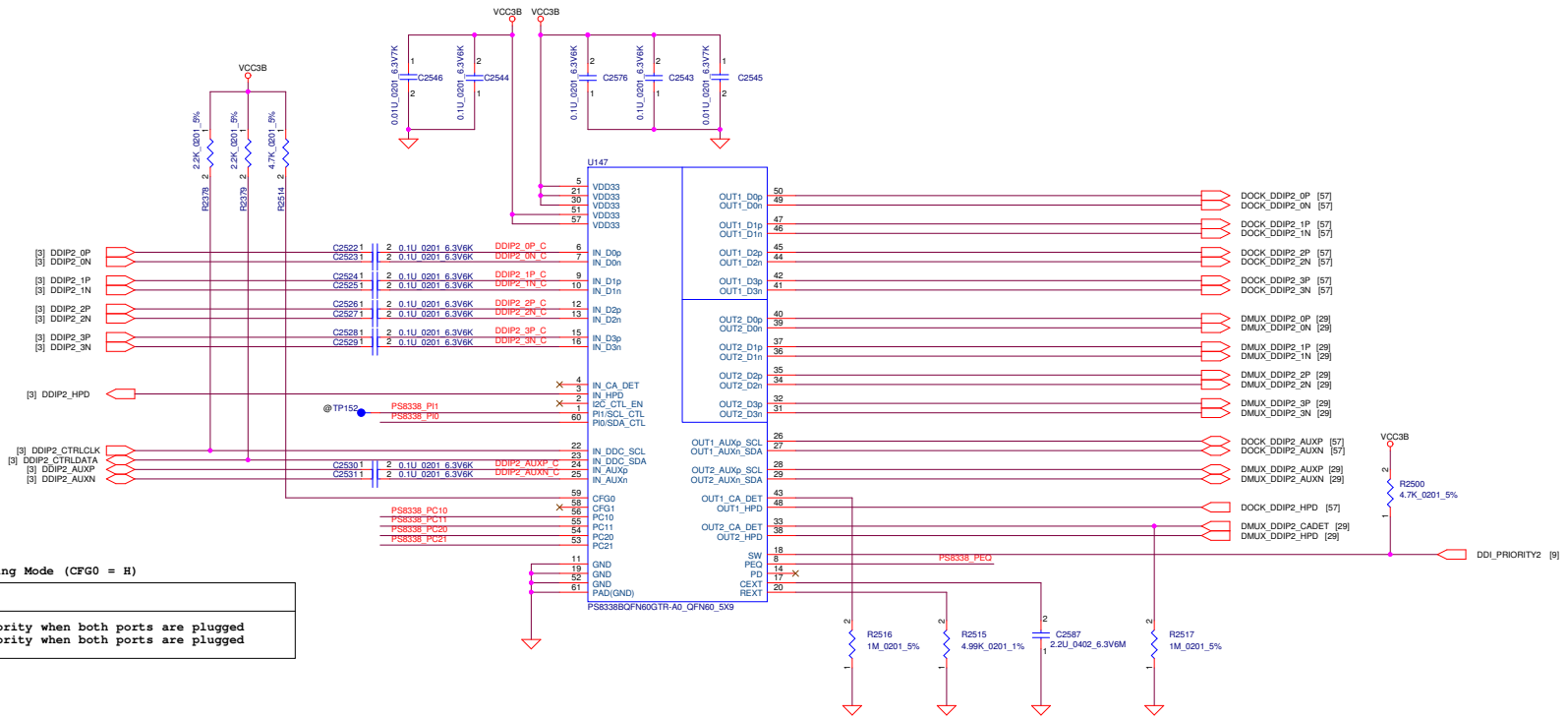


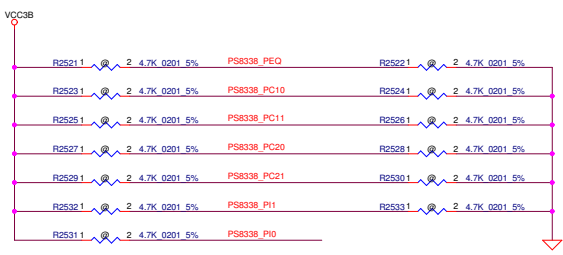
TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY2)
L Port 1 has higher priority when both ports are plugged
H Port 2 has higher priority when both ports are plugged

PEQ (INT PD)	R2521	R2522
HEQ 14.5dB	ASM	NO_ASM
LLEQ 8.5dB	ASM	ASM
LEQ 11.5dB	NO_ASM	NO_ASM

	PC10 (INT PD)		PC20 (INT PD)	
	R2523	R2524	R2527	R2528
AUX interception DIS Output 800mV & 0dB	ASM	NO_ASM	ASM	NO_ASM
AUX interception DIS Output 400mV & 0dB	ASM	ASM	ASM	ASM
AUX interception EN	NO_ASM	NO_ASM	NO_ASM	NO_ASM

	PC11 (INT PD)		PC21 (INT PD)	
	R2525	R2526	R2529	R2530
Swing +20%	ASM	NO_ASM	ASM	NO_ASM
Swing -16.7%	ASM	ASM	ASM	ASM
Swing default	NO_ASM	NO_ASM	NO_ASM	NO_ASM

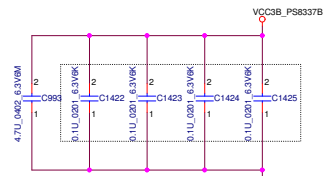
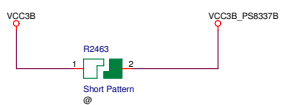


P11 (INT PD)	R2532	R2533
Auto test EN & Offset cancellation EN	ASM	NO_ASM
Auto test DIS & Offset cancellation DIS	ASM	ASM
Auto test DIS & Offset cancellation EN	NO_ASM	NO_ASM

P10 (INT PD)	R2531
Auto EQ DIS	ASM
Auto EQ EN	NO_ASM

Priority 1	H	L
Priority 2	H	L
H	HDMI	WiGig
L	Prolink	Prolink

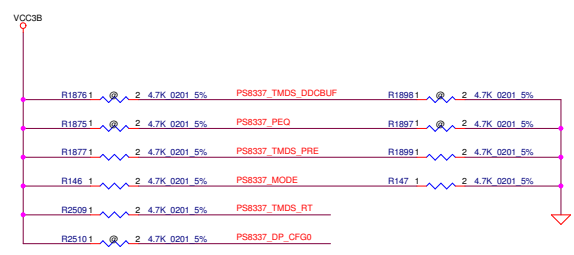
SVT_C_EC005
Short Pattern: R2463



Δ P U Q # 3 L U Δ V C C 0 3 B U Δ V C C 0 3 B P S 8 3 3 7 B

TABLE : Automatic Switching Mode (MODE = H, M)

SW (DDI_PRIORITY1)
L DP Port has higher priority when both ports are plugged
H TMSD Port has higher priority when both ports are plugged



TMSD DDCBUF (INT PD)	R1876	R1898
DDC Active Buffer	ASM	NO_ASM
DDC Pass Through w/ PU	ASM	ASM
DDC Pass Through w/o PU	NO_ASM	NO_ASM

← LOGIC

PEQ (INT PD)	R1875	R1897
HEQ 15dB	ASM	NO_ASM
LLEQ 5dB	ASM	ASM
LEQ 12dB	NO_ASM	NO_ASM

← LOGIC

TMSD PRE (INT PD)	R1877	R1899
1.5dB	ASM	NO_ASM
3.0dB	ASM	ASM
0dB	NO_ASM	NO_ASM

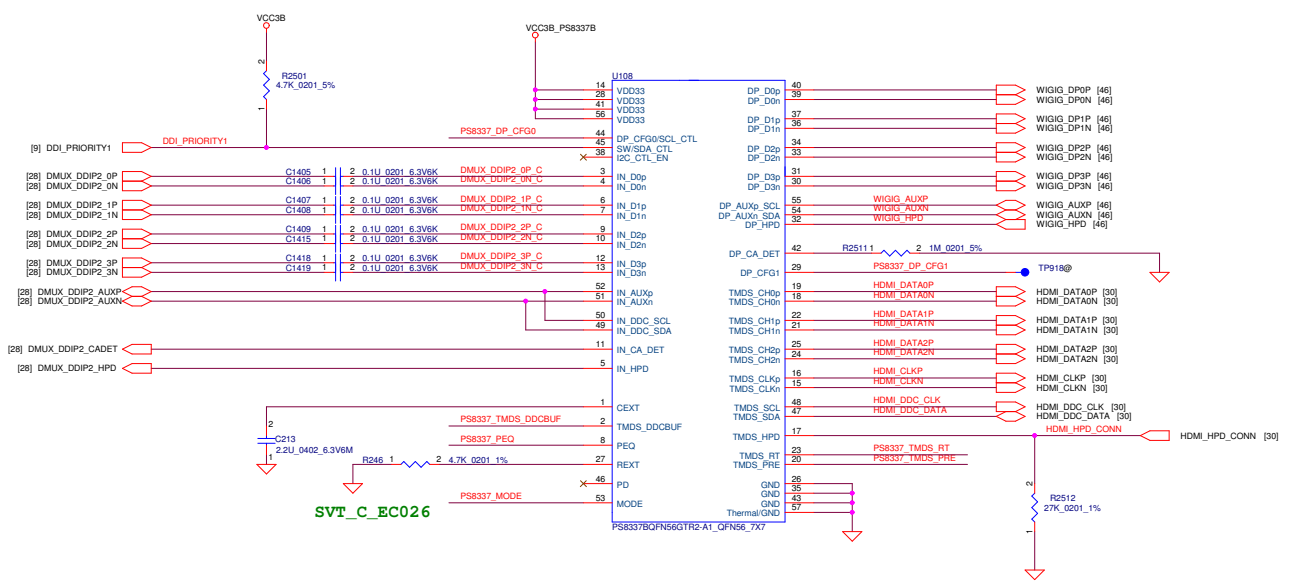
← LOGIC

MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

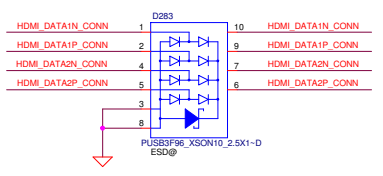
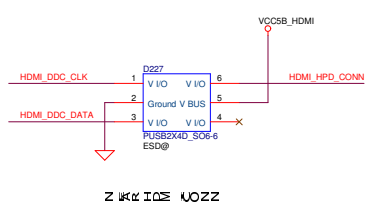
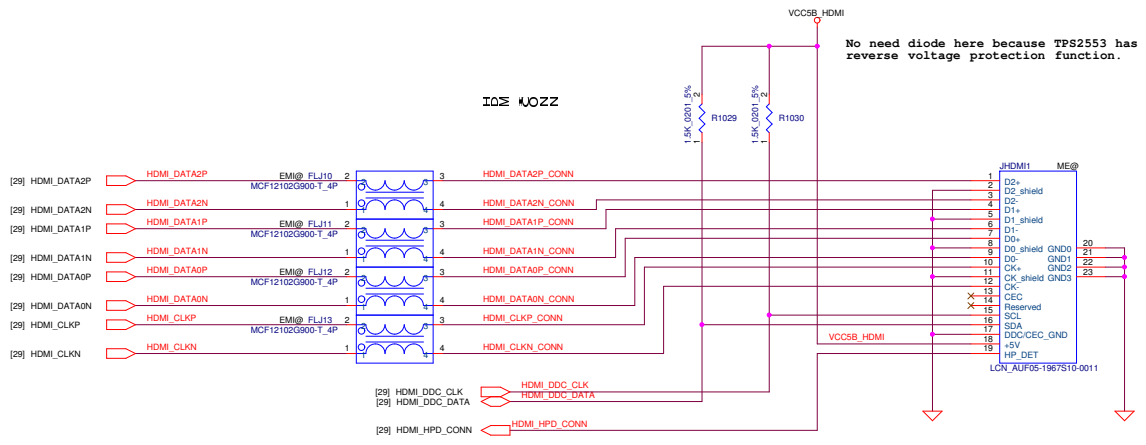
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TMSD RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM

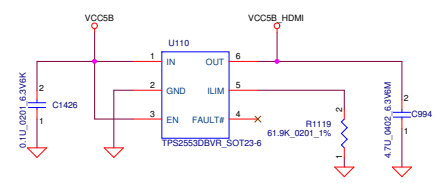
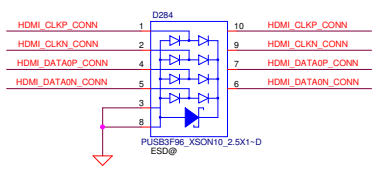
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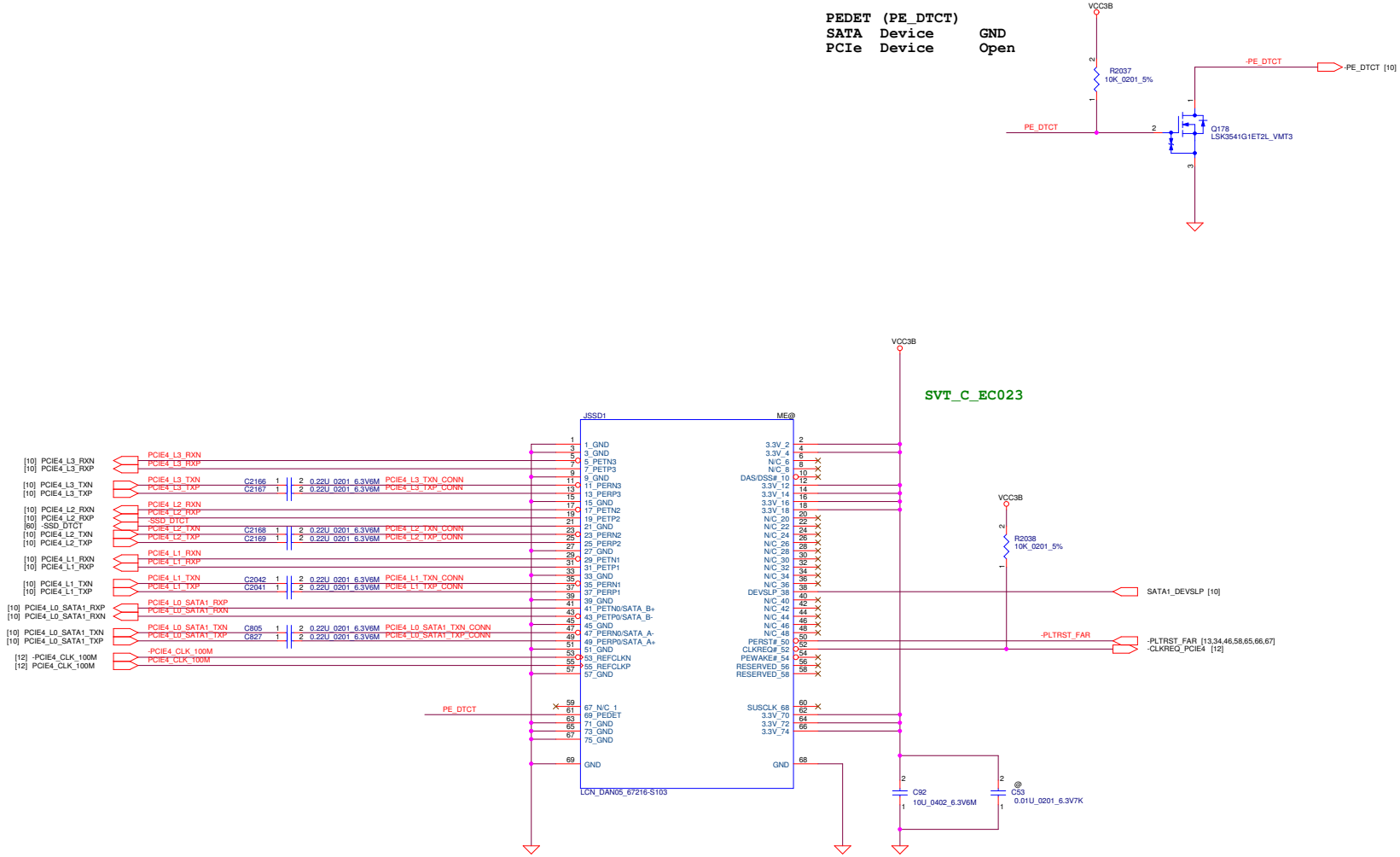
SVT_C_EC026



Current Limit Target : 400mA
Requirement : 300mA
HDMI Spec : 50mA - 500mA



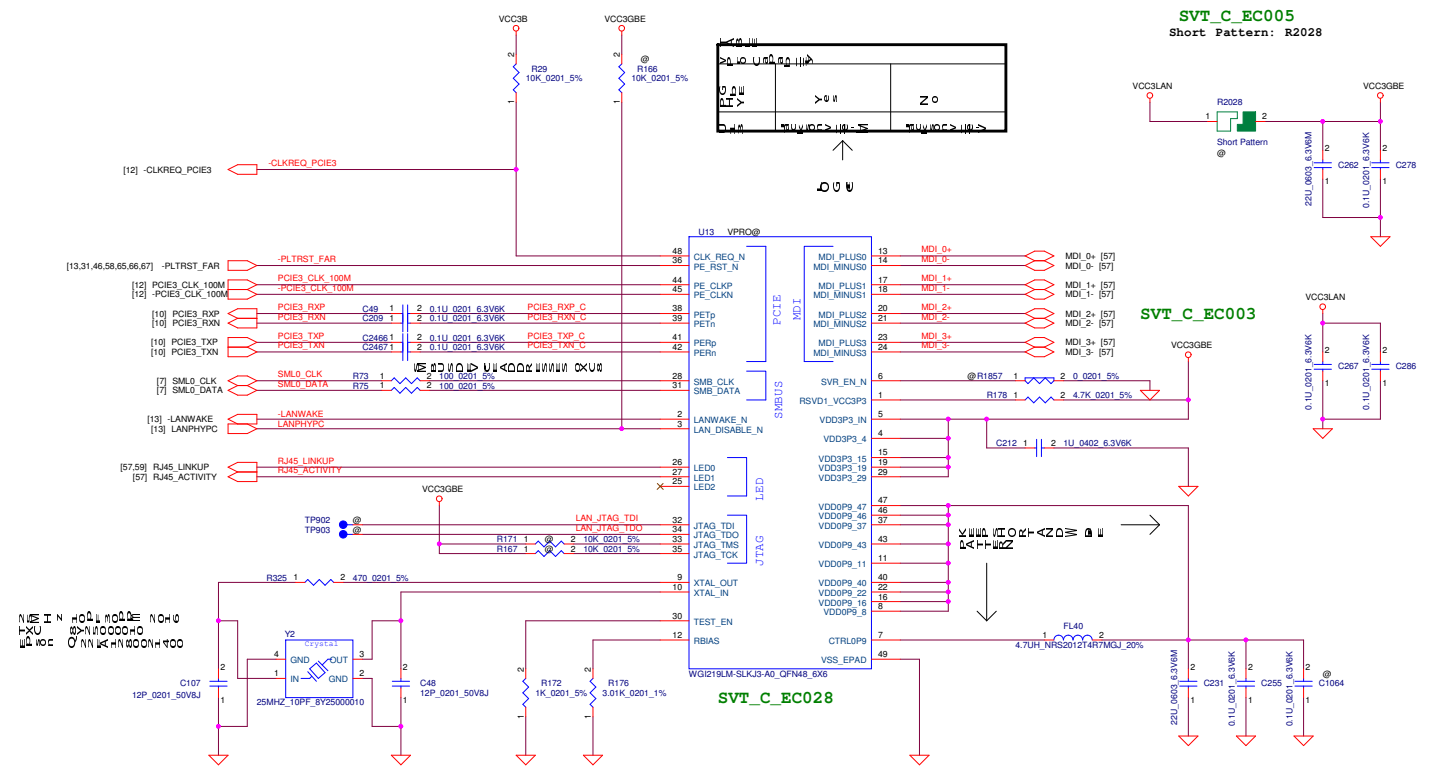
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	HDMI CONNECTOR	
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SVT_C_EC005
Short Pattern: R2028

SVT_C_EC003

SVT_C_EC028

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				Document Number	0.5
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				Document Number	0.5
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				Document Number	0.5
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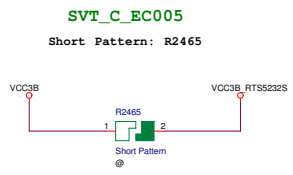
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				Document Number	0.5
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				Document Number	0.5
				Customer	LA-C581P
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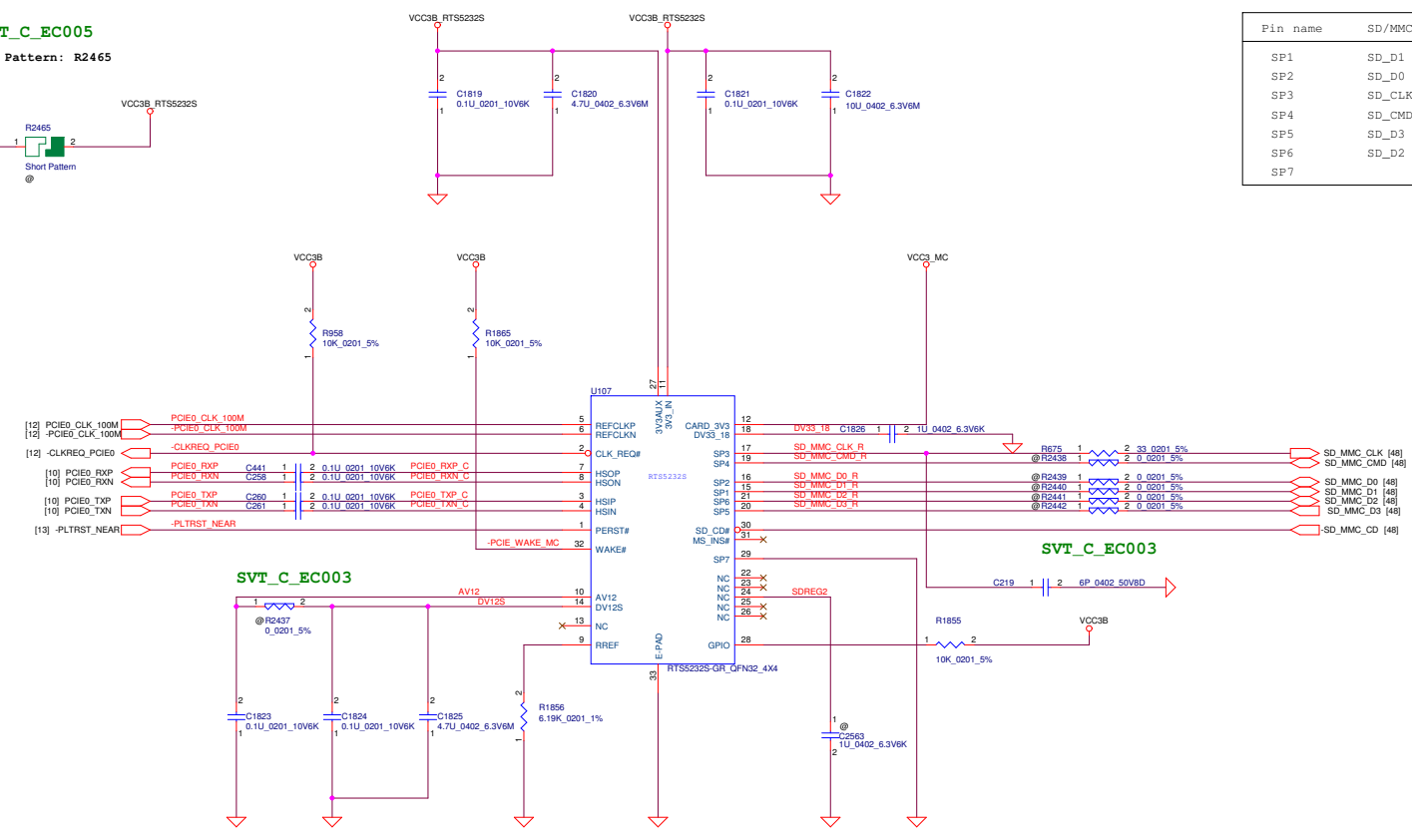
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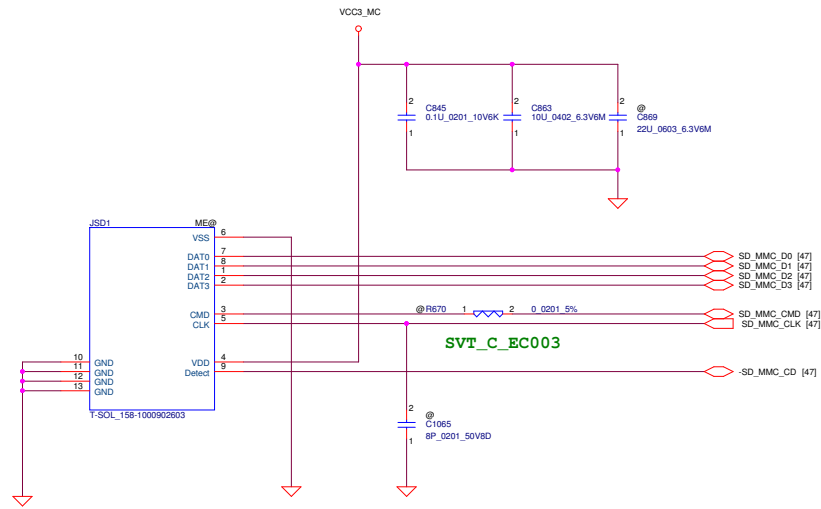
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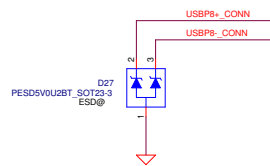
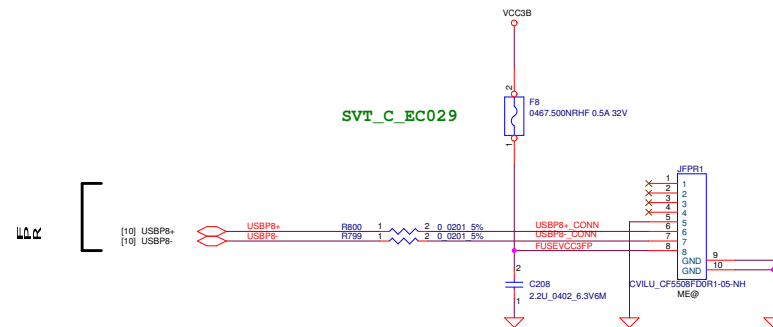
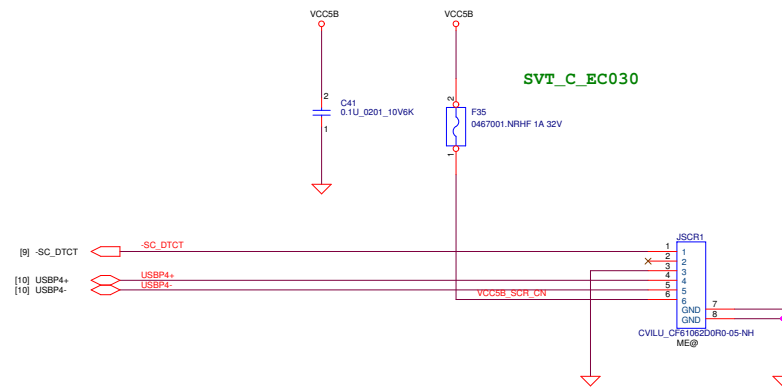
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Pin name	SD/MMC	MEMORSTICK
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SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7		

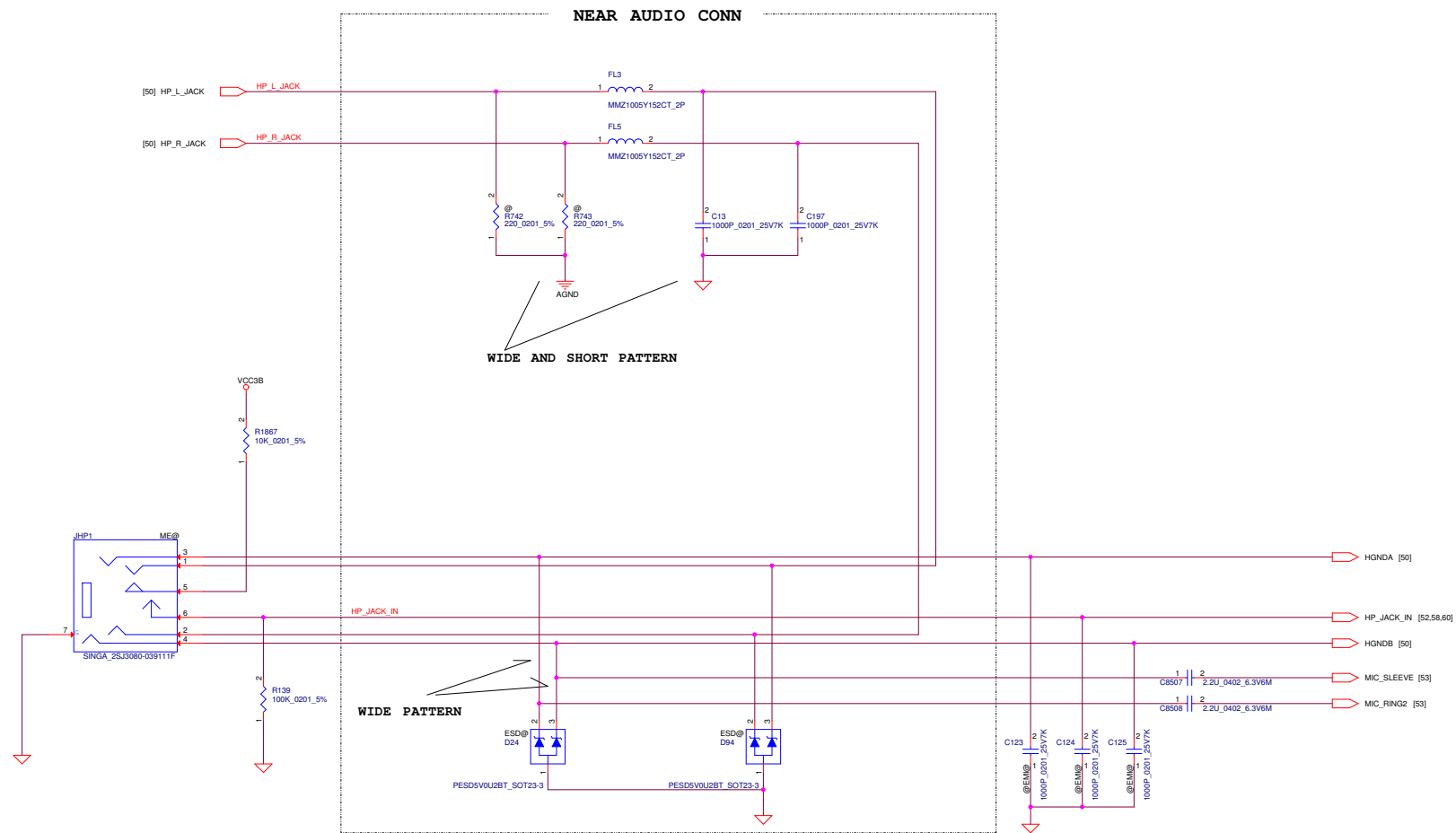




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Date: Thursday, August 13, 2015			Sheet 49 of 102	Customer Number: LA-C581P



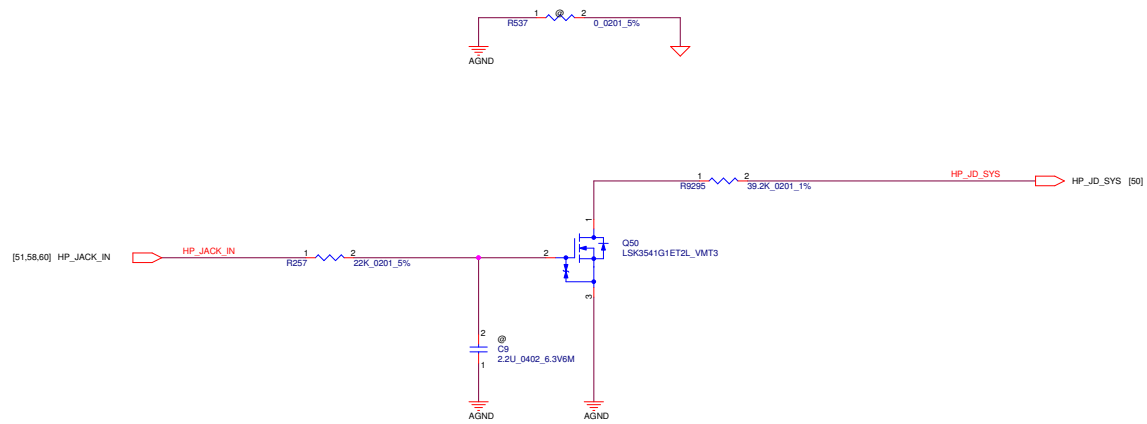
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Date: Thursday, August 13, 2015			Sheet	51 of 102

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AUDIO CONNECTOR

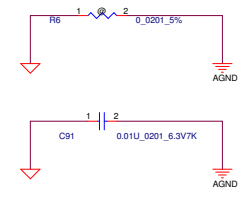
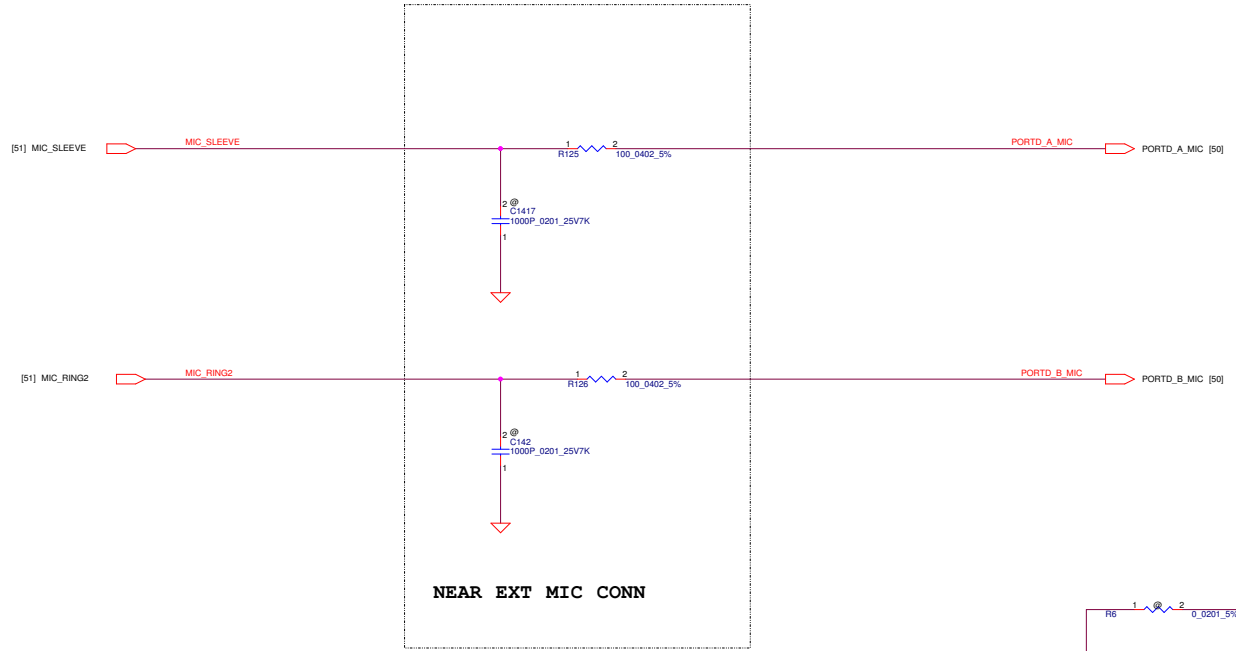
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Sheet 51 of 102

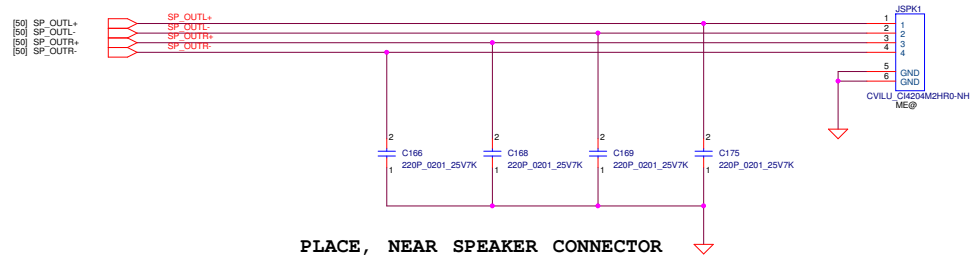


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				Rev
Date: Thursday, August 13, 2015				Sheet 52 of 102

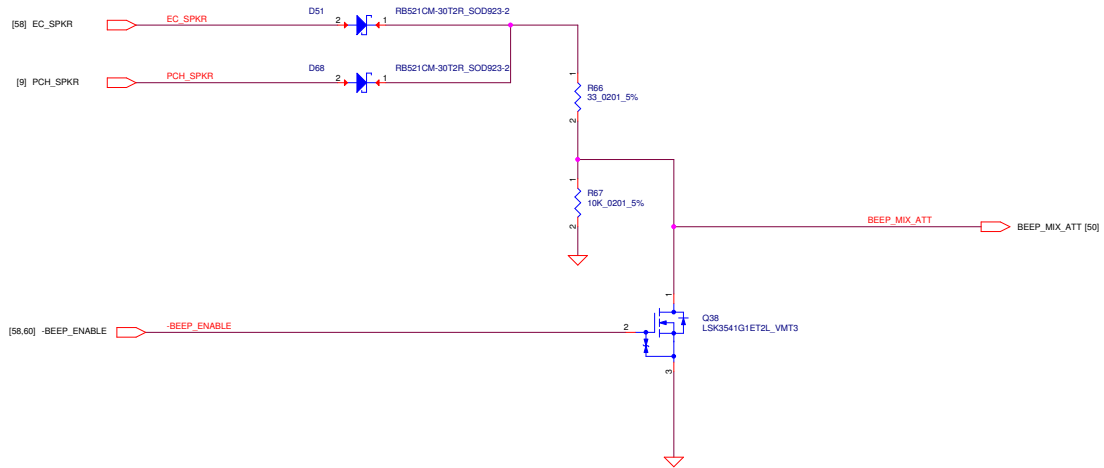
AUDIO JACK SENSE
 Custom Number: **LA-C581P**
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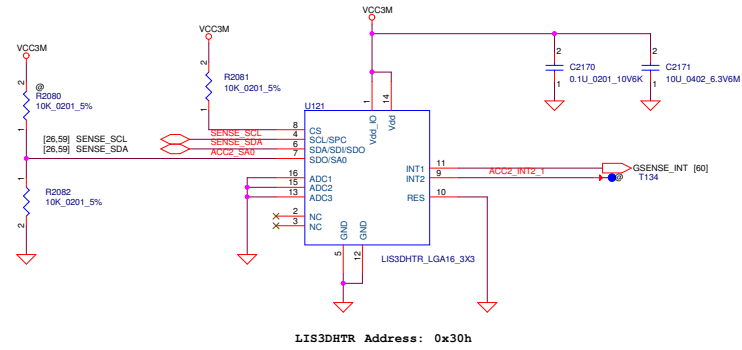
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Size Document Number Custom LA-C581P			Date: Thursday, August 13, 2015 Sheet 54 of 102	



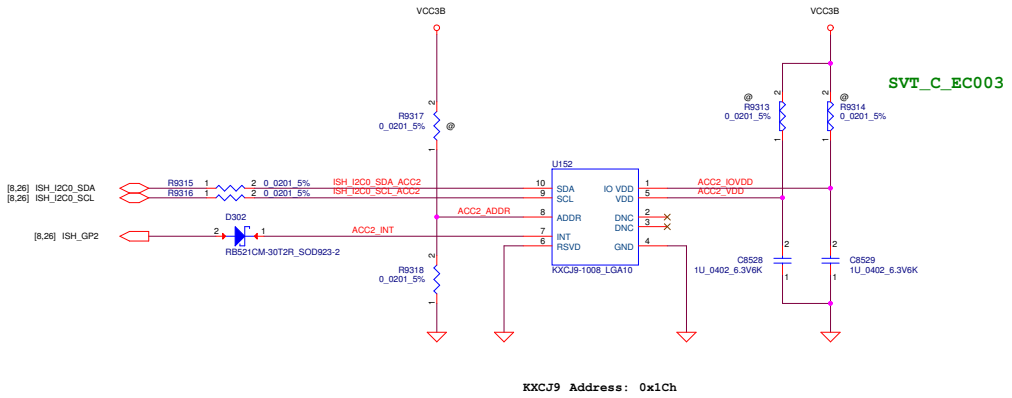
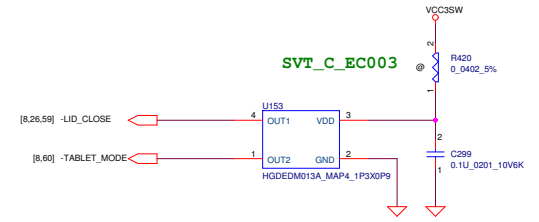
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CS	Mode Selection
H	I2C Mode
L	SPI Mode

ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

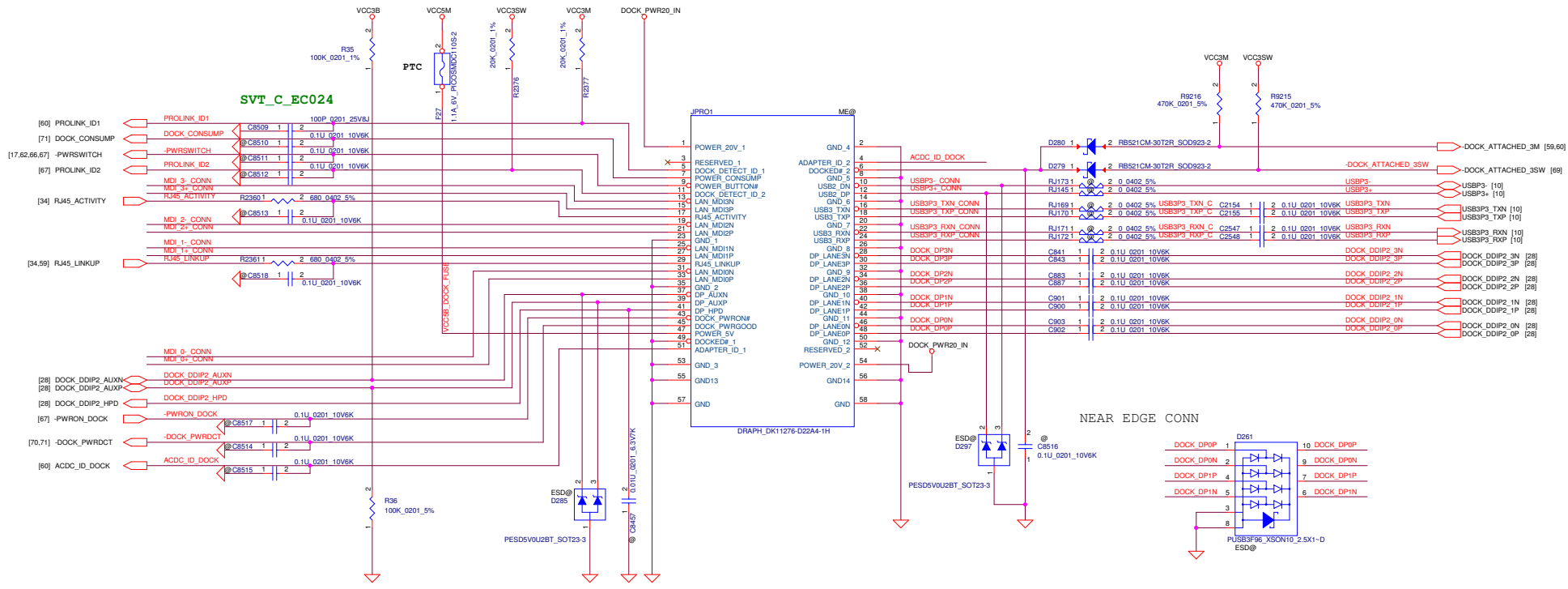


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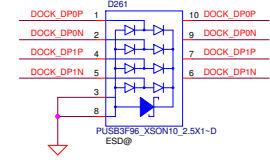


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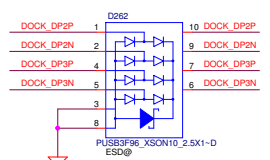
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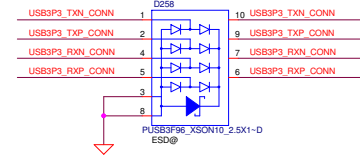
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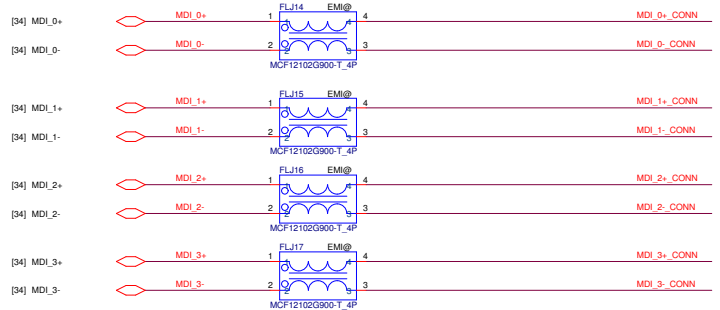
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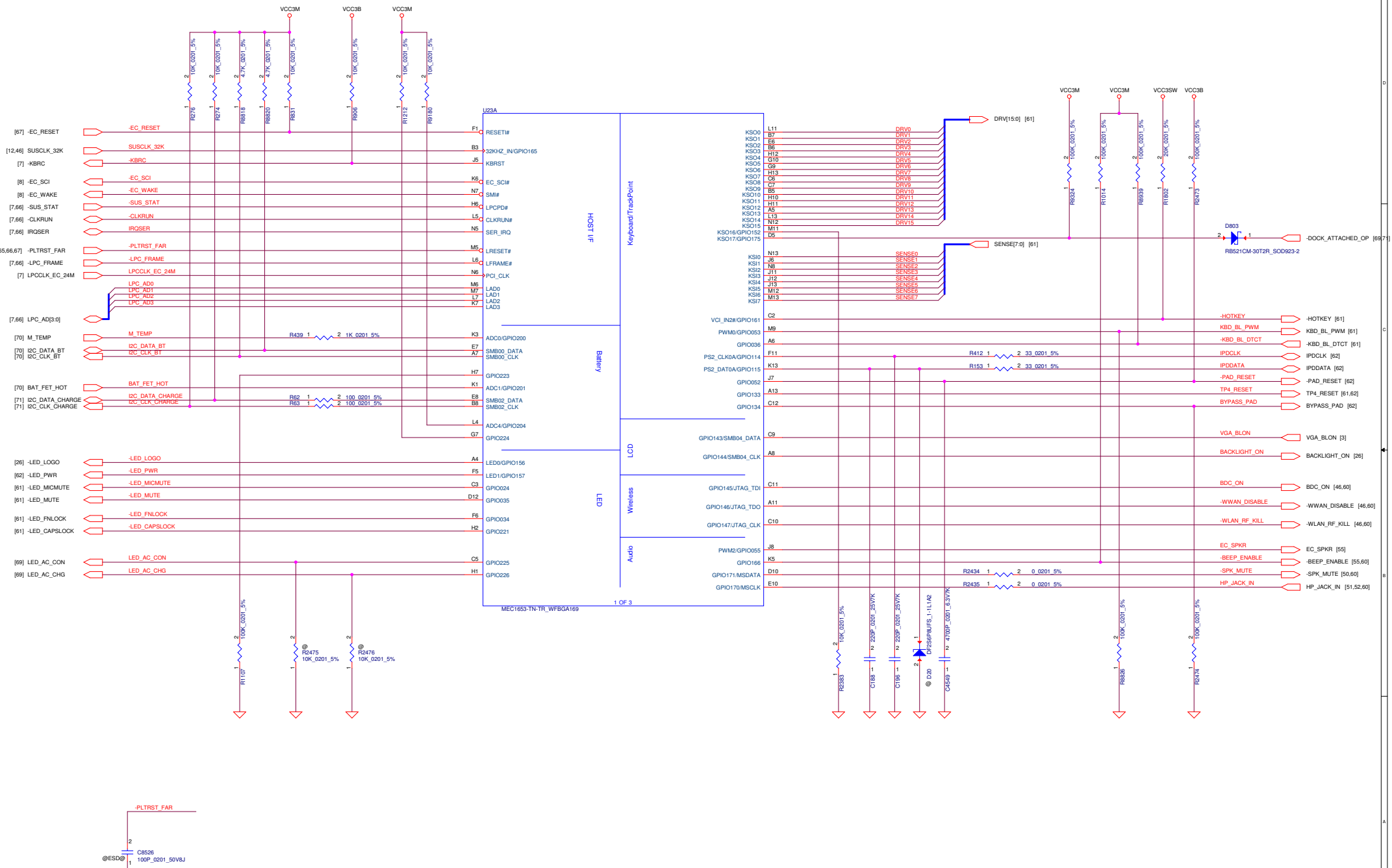
NEAR EDGE CONN



D287 / D244
NEAR EDGE CONN



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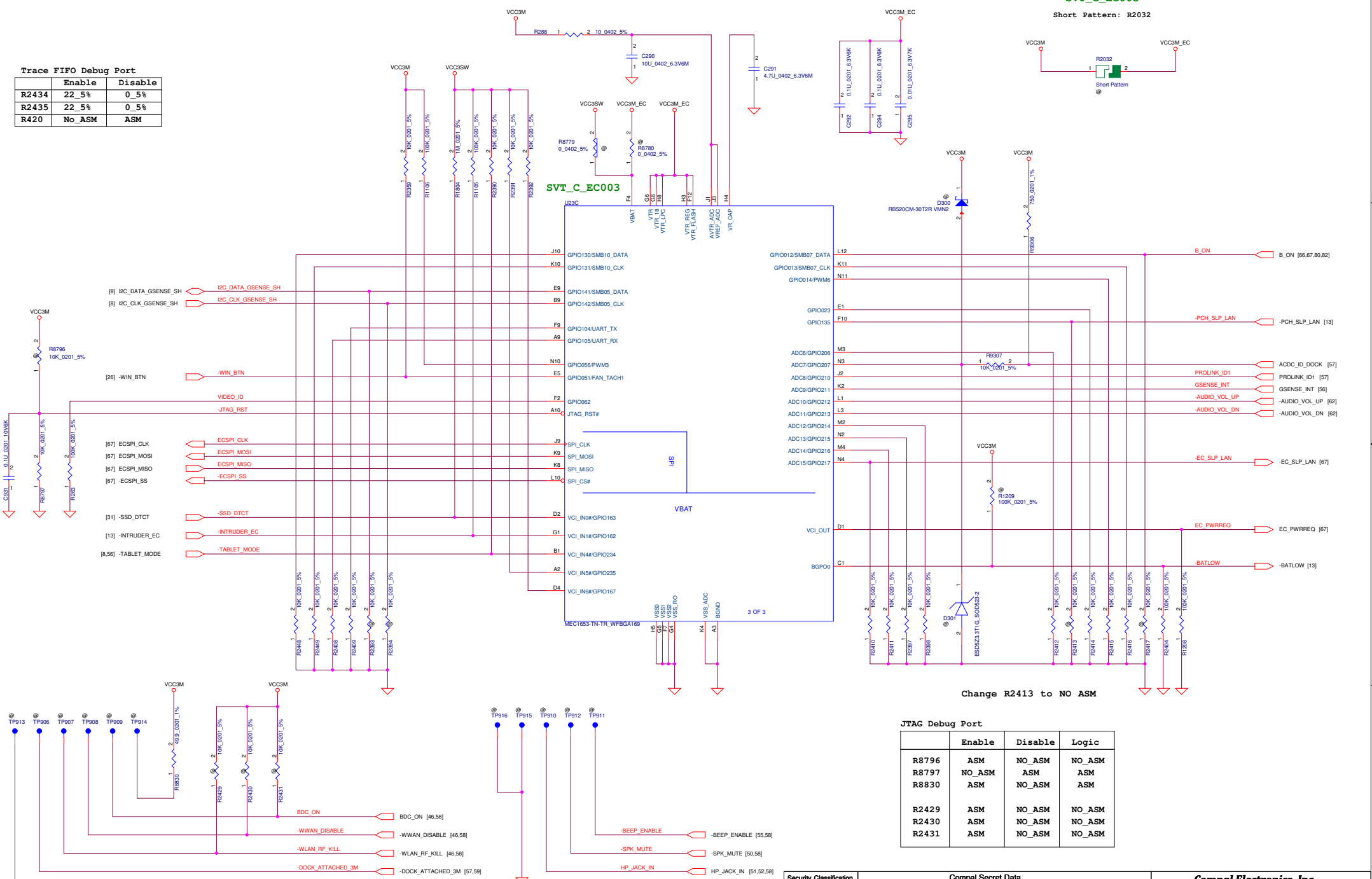


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SVT_C_EC005
Short Pattern: R2032

Trace FIFO Debug Port

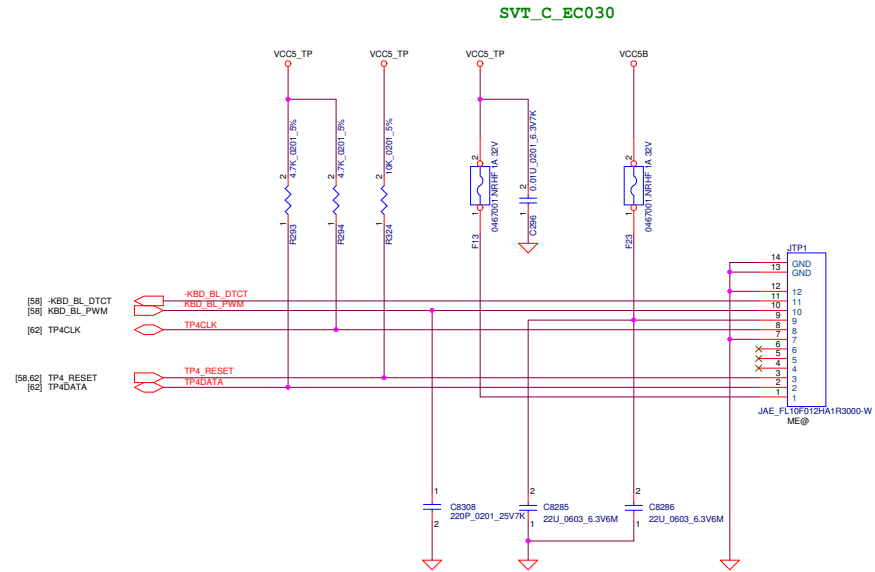
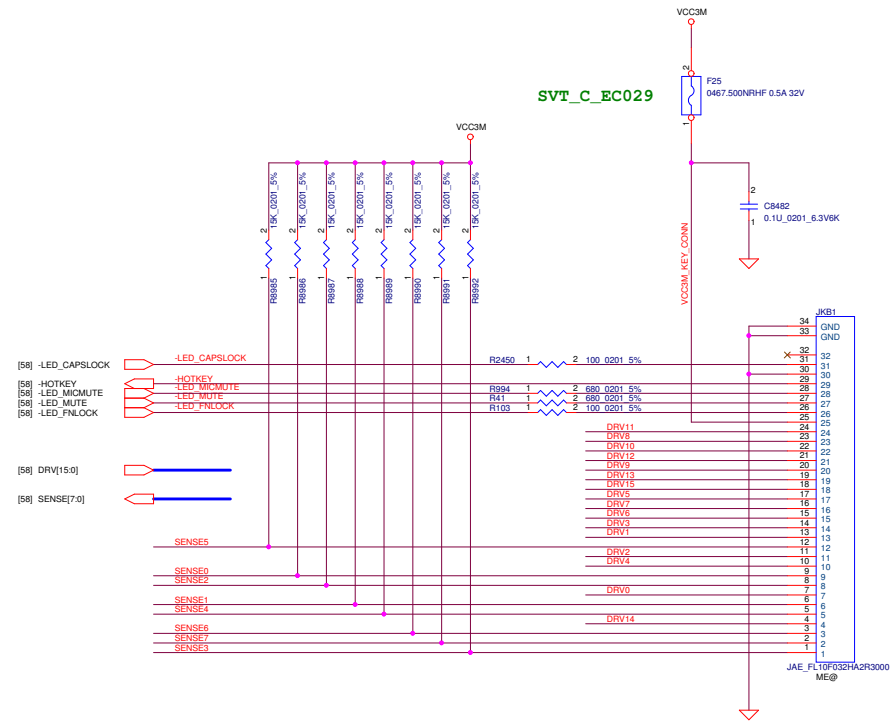
	Enable	Disable
R2434	22.5%	0.5%
R2435	22.5%	0.5%
R420	No_ASM	ASM



Change R2413 to NO ASM

JTAG Debug Port

	Enable	Disable	Logic
R8796	ASM	NO_ASM	NO_ASM
R8797	NO_ASM	ASM	ASM
R8830	ASM	NO_ASM	ASM
R2429	ASM	NO_ASM	NO_ASM
R2430	ASM	NO_ASM	NO_ASM
R2431	ASM	NO_ASM	NO_ASM



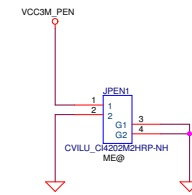
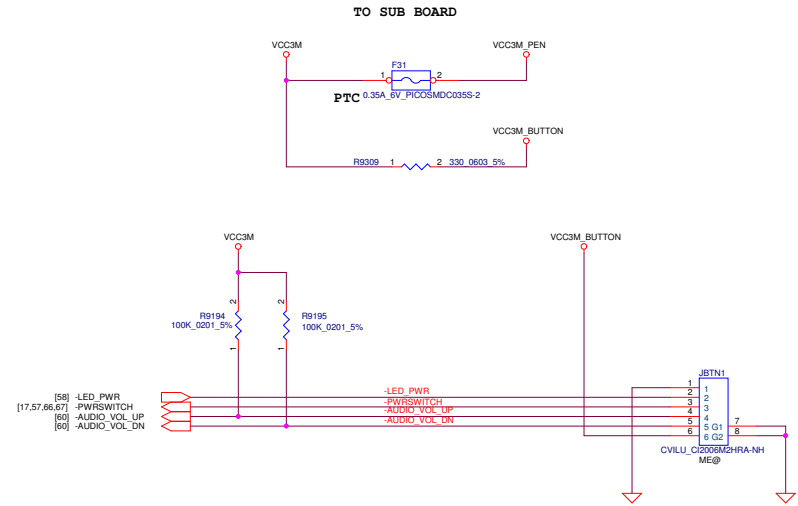
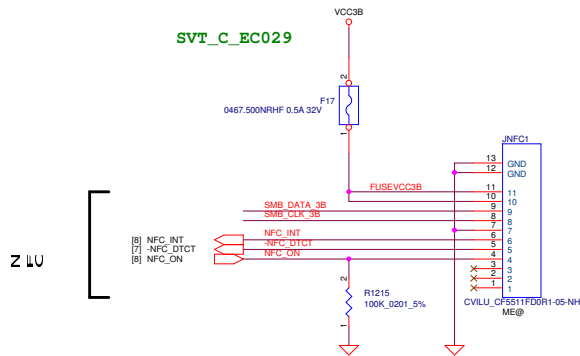
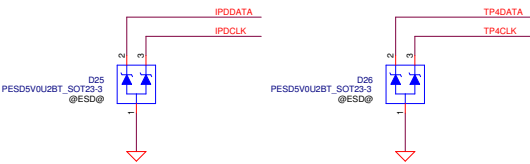
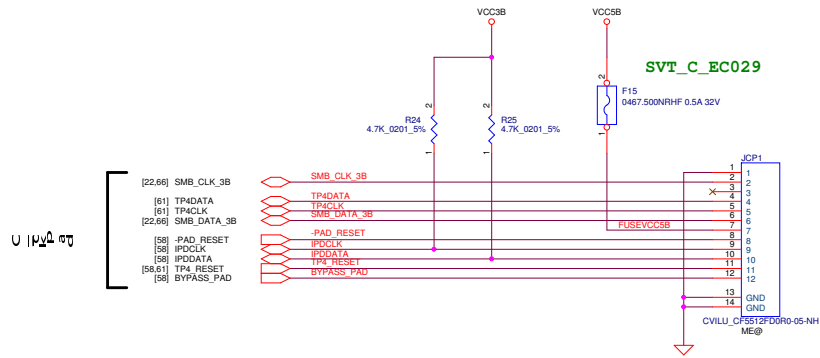
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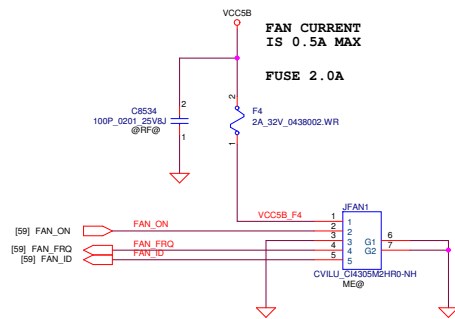
LA-C581P

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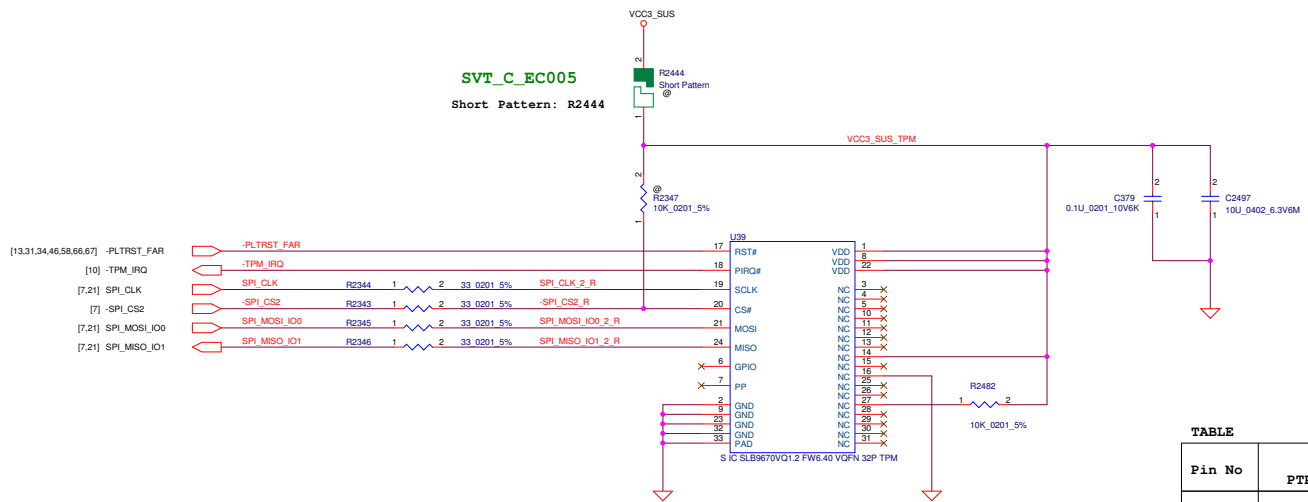
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-Change FW version of Infineon TPM to 6.40
 -Change Nuvoton parts number to NPCT650LB0YX

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.40	Nuvoton NPCT650LB0YX
1	VDD	VDD	VSB
2	GND	GND	NC
3	GPIO	NC	GPX/GPIO2
4	GPIO	NC	PP
5	NC	NC	TEST
6	VNC/GPIO	GPIO	GPIO3
7	GPIO/VDD	PP	NC
8	VDD	VDD	VDD
9	GND	GND	GND
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	Reserved
13	VNC/GPIO	NC	GPIO4
14	VDD	NC	VDD
15	NC	NC	DNC
16	GND	NC	GND
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SCLK
20	SPI_CS#	CS#	SCS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VDD
23	GND	GND	GND
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	(SERIRQ)
28	NC	NC	DNC
29	VNC/ GPIO	NC	GPIO0
30	VNC/ GPIO	NC	GPIO1
31	VNC	NC	NC
32	GND	GND	GND

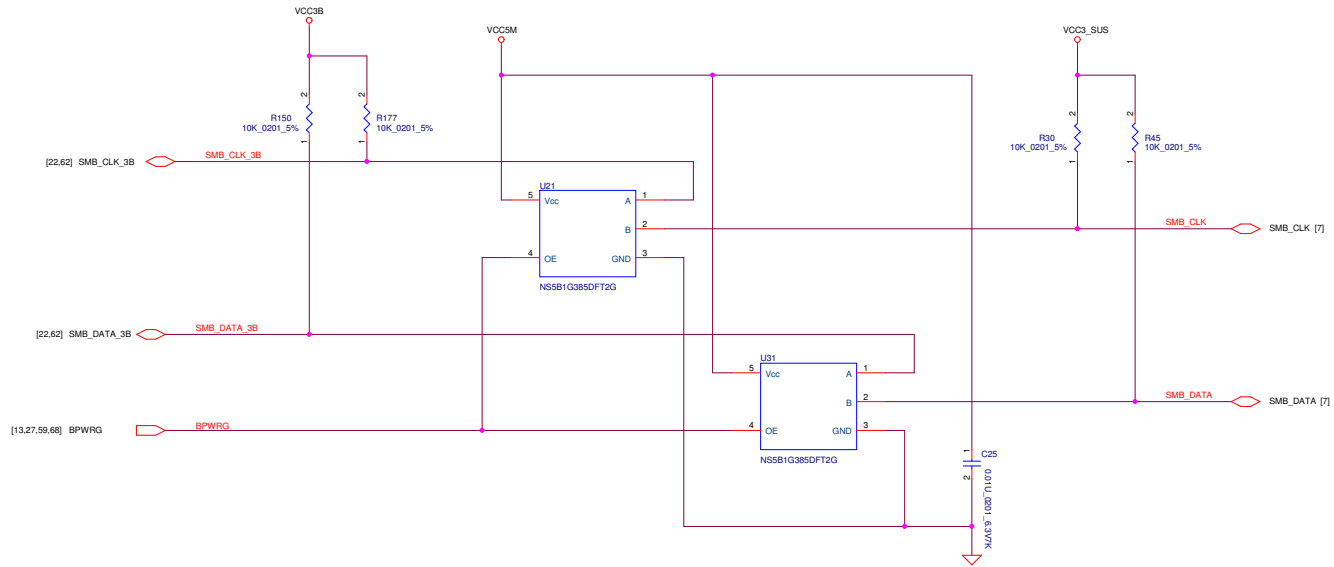
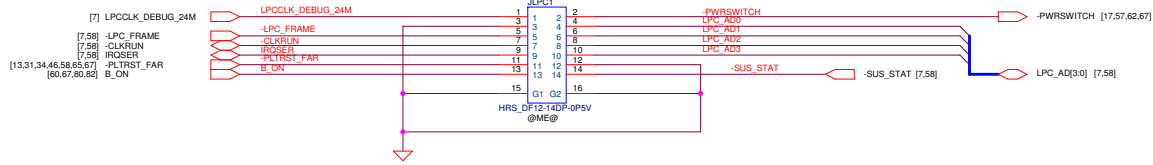
TABLE

REF DES	ENABLE	DISABLE
JLPC1	ASM	NO_ASM
R220	ASM	NO_ASM

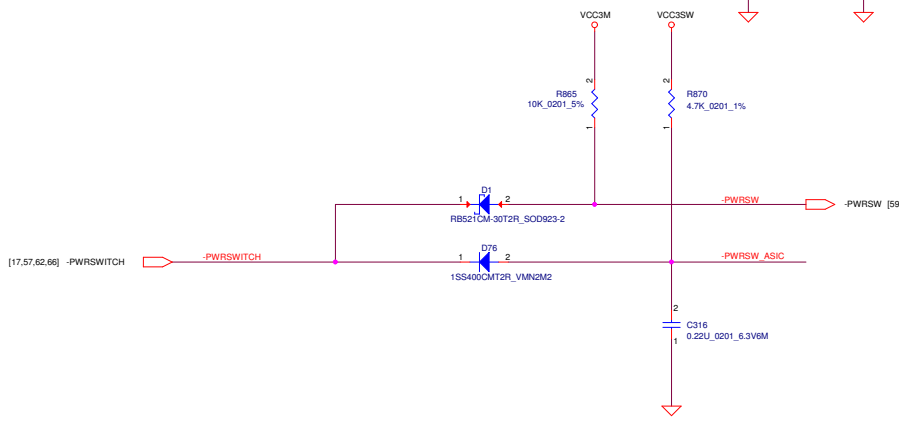
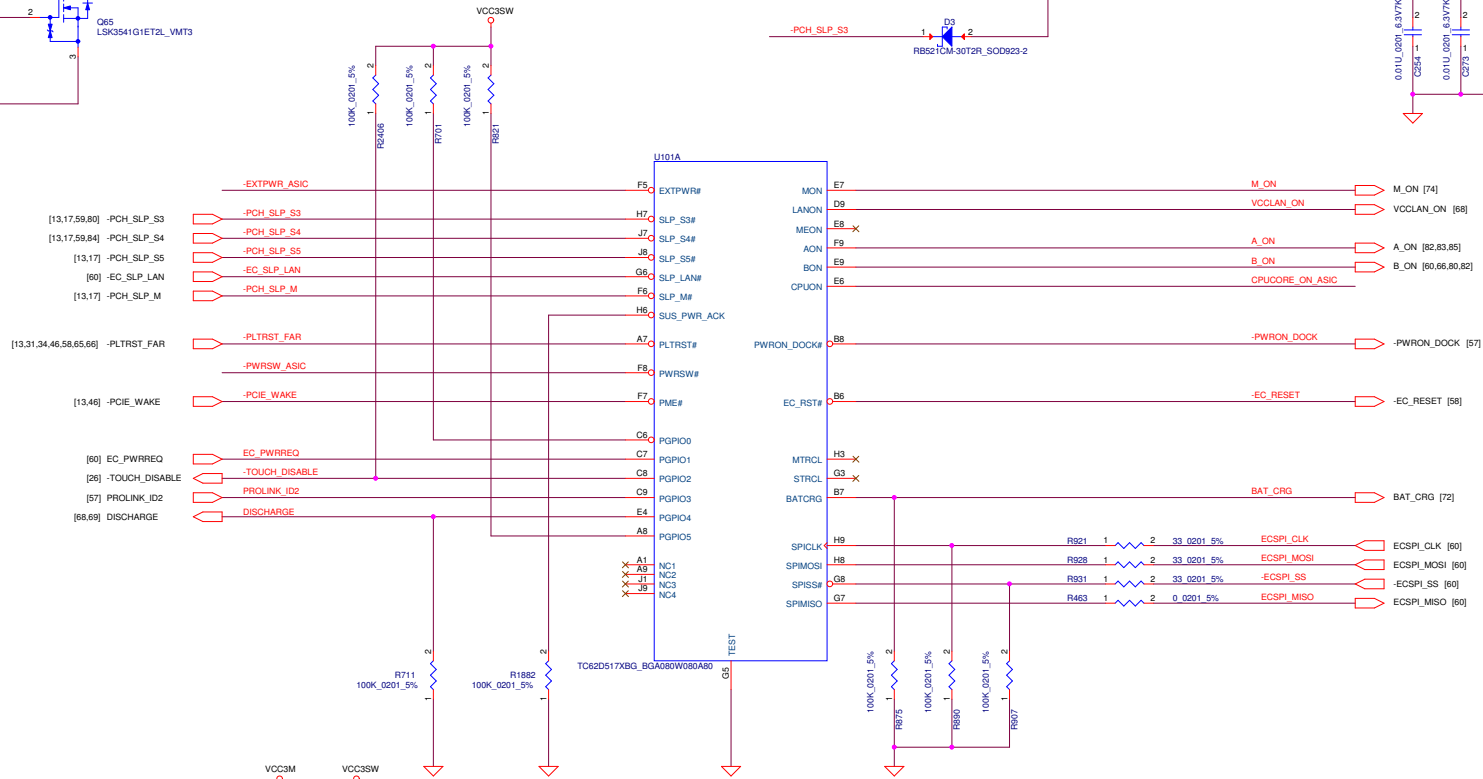
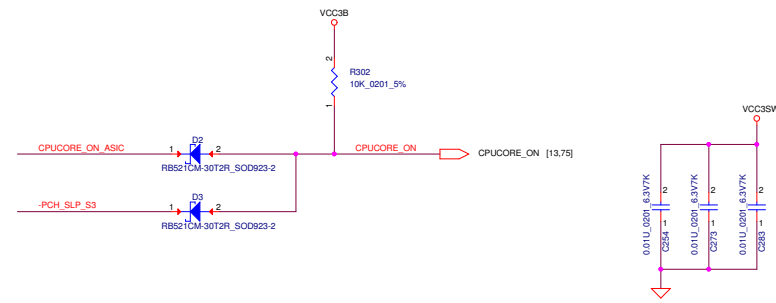
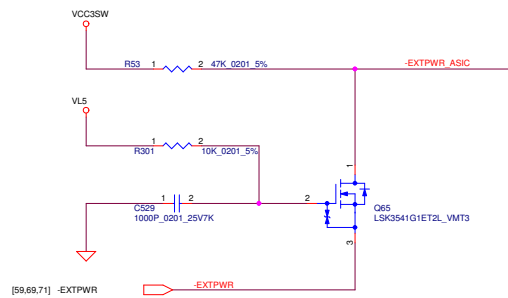
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LOGIC

SVT_EC004

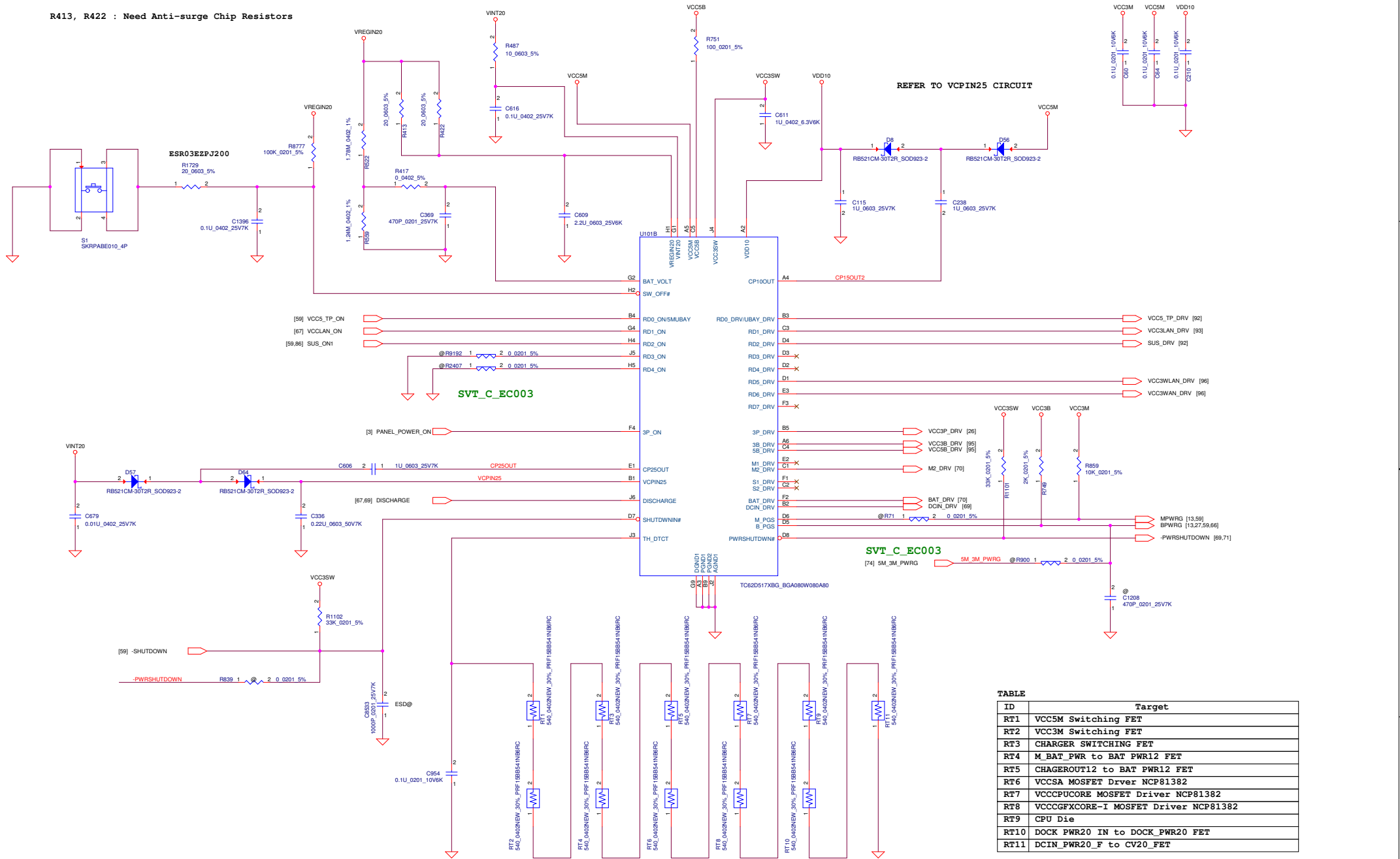


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Custm	LA-C581P	0.5		Thursday, August 13, 2015	
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R413, R422 : Need Anti-surge Chip Resistors

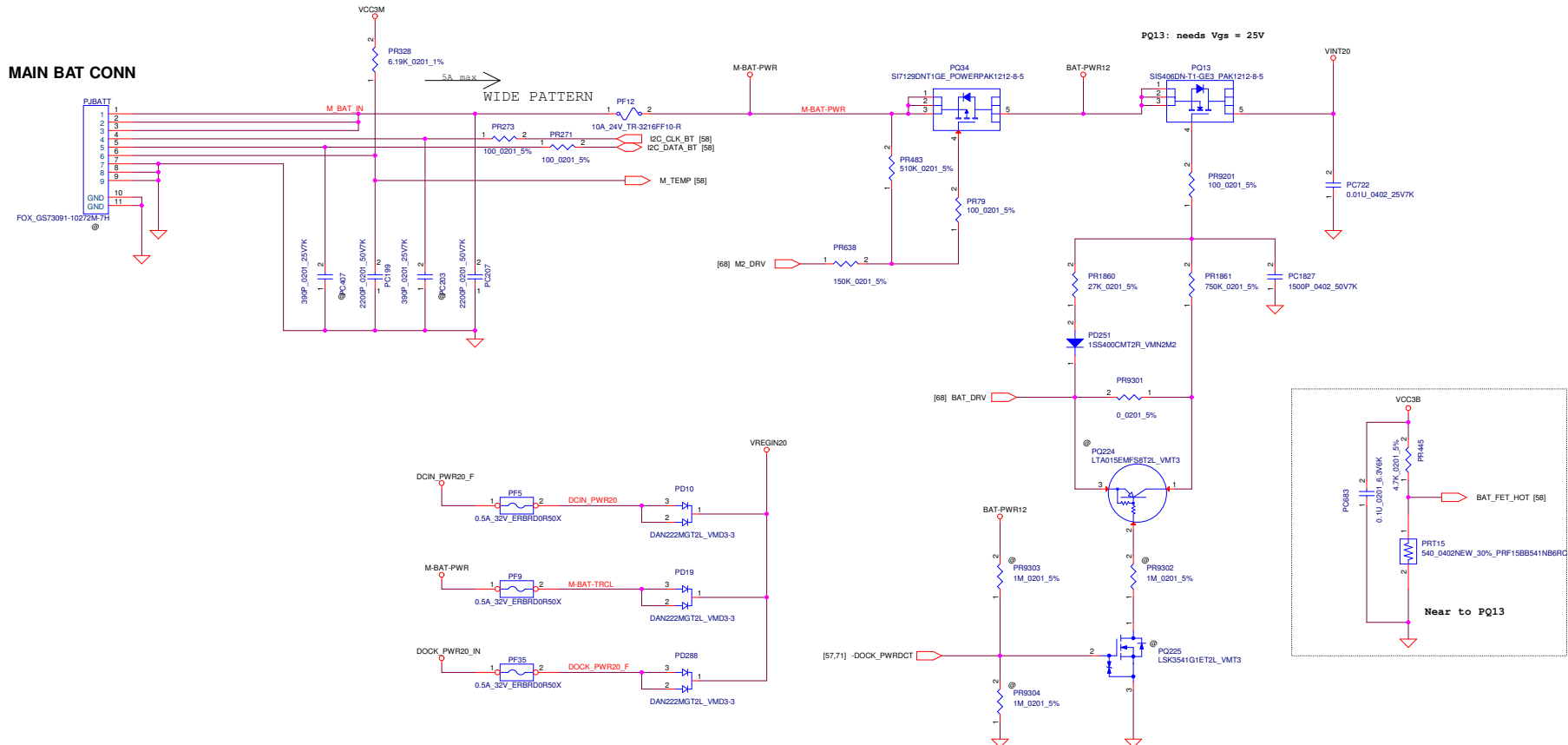


REFER TO VCPIN25 CIRCUIT

ID	Target
RT1	VCC5M Switching FET
RT2	VCC3M Switching FET
RT3	CHARGER SWITCHING FET
RT4	M_BAT_PWR to BAT_PWR12 FET
RT5	CHAGEROUT12 to BAT_PWR12 FET
RT6	VCCSA MOSFET Driver NCP81382
RT7	VCCPCUCORE MOSFET Driver NCP81382
RT8	VCCCGFXCORE-I MOSFET Driver NCP81382
RT9	CPU Die
RT10	DOCK_PWR20 IN to DOCK_PWR20 FET
RT11	DCIN_PWR20_F to CV20_FET

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MAIN BAT CONN



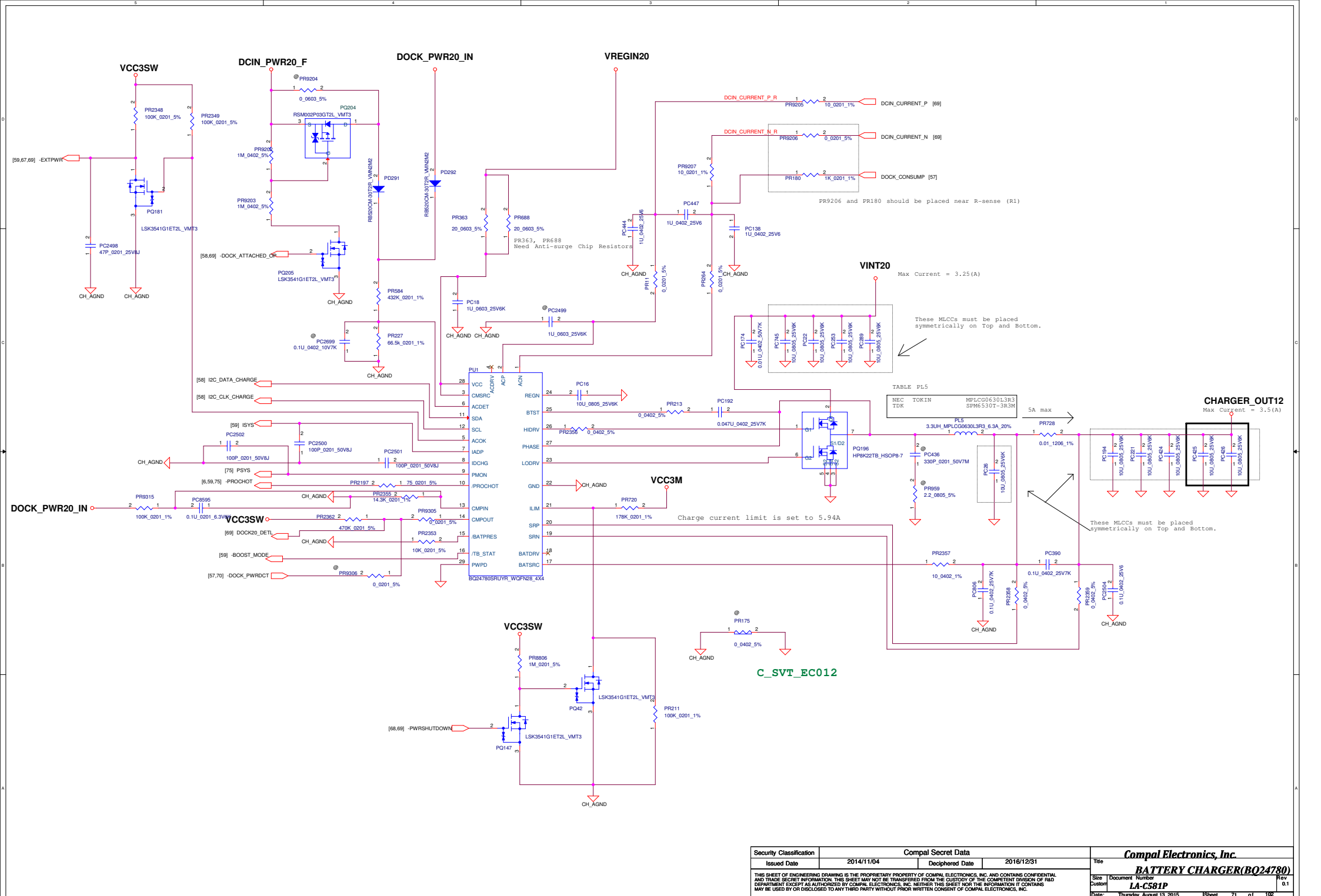
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BATTERY INPUT

LA-C581P

Thursday, August 13, 2015



PR9206 and PR180 should be placed near R-sense (R1)

Max Current = 3.25(A)
These MLCCs must be placed symmetrically on Top and Bottom.

TABLE PL5
NEC TOKIN
MPLCG0630L3R3
SPM6530T-3R3M
5A max

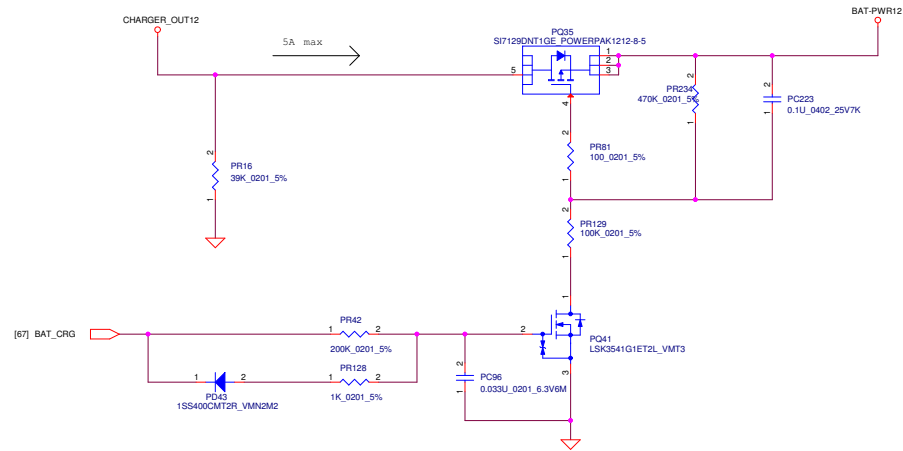
CHARGER_OUT12
Max Current = 3.5(A)

These MLCCs must be placed symmetrically on Top and Bottom.

Charge current limit is set to 5,94A

C_SVT_EC012

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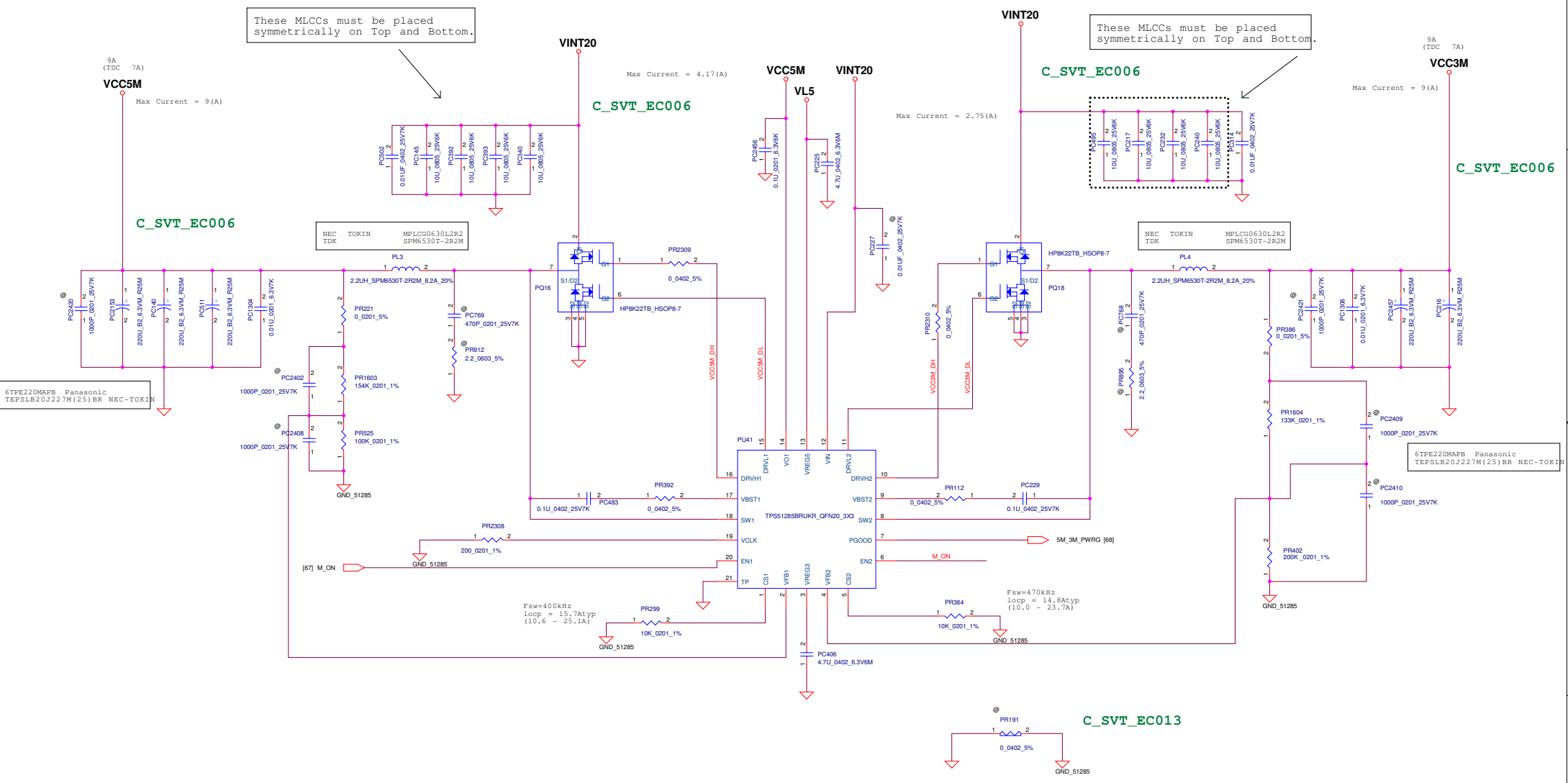
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These MLCCs must be placed symmetrically on Top and Bottom.

These MLCCs must be placed symmetrically on Top and Bottom.



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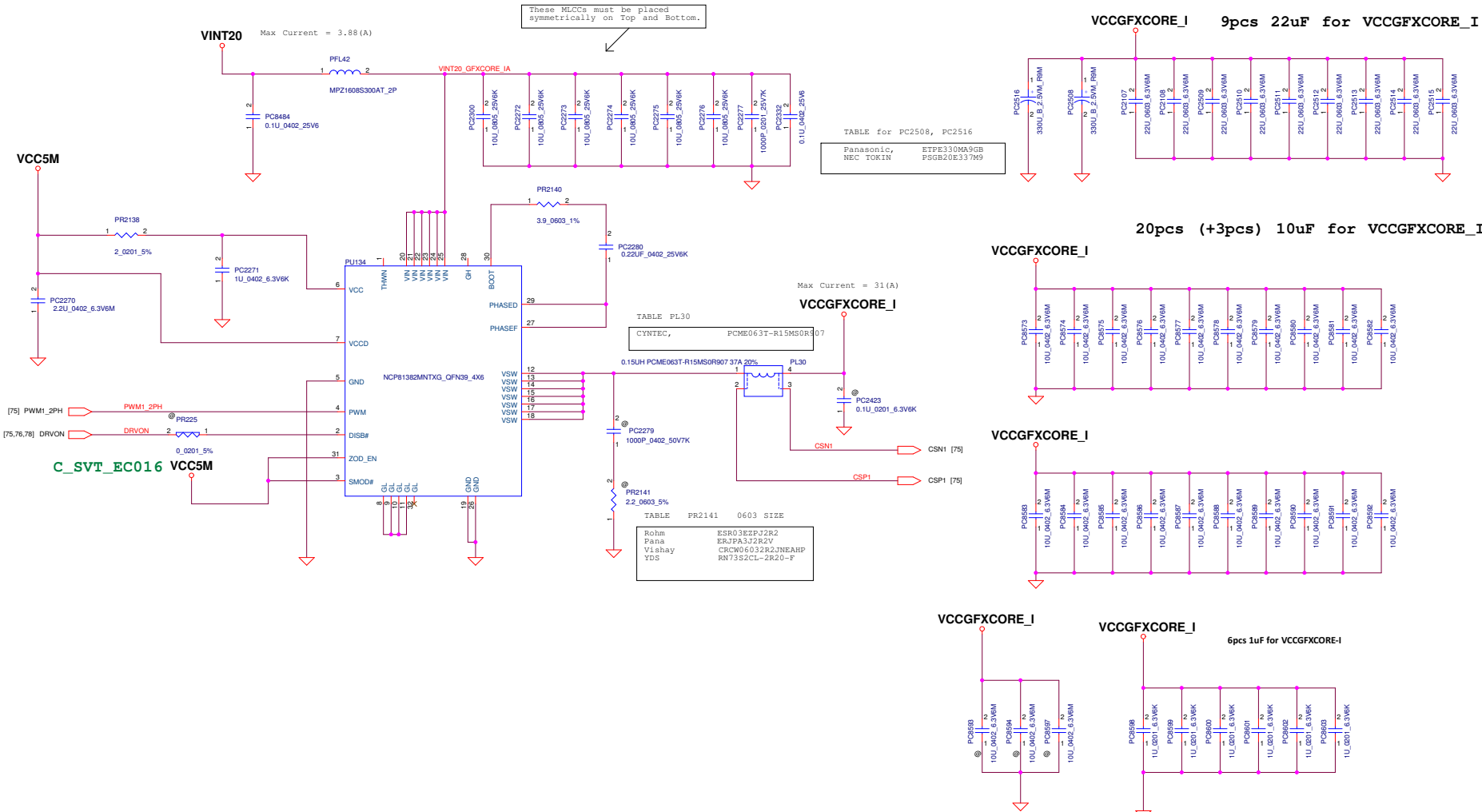


TABLE for PC2508, PC2516

Panasonic,	ETPE330MA9GB
NEC TOKIN	PSGB20E337M9

TABLE PL30

CYNTEC,	PCME063T-R15MS0R907
---------	---------------------

TABLE PR2141 0603 SIZE

Rohm	ESR03ETP72R2
Pana	ERJPA3J2R2V
Vishay	CRC06032R2JNEAHP
YDS	RN75S2CL-2R20-F

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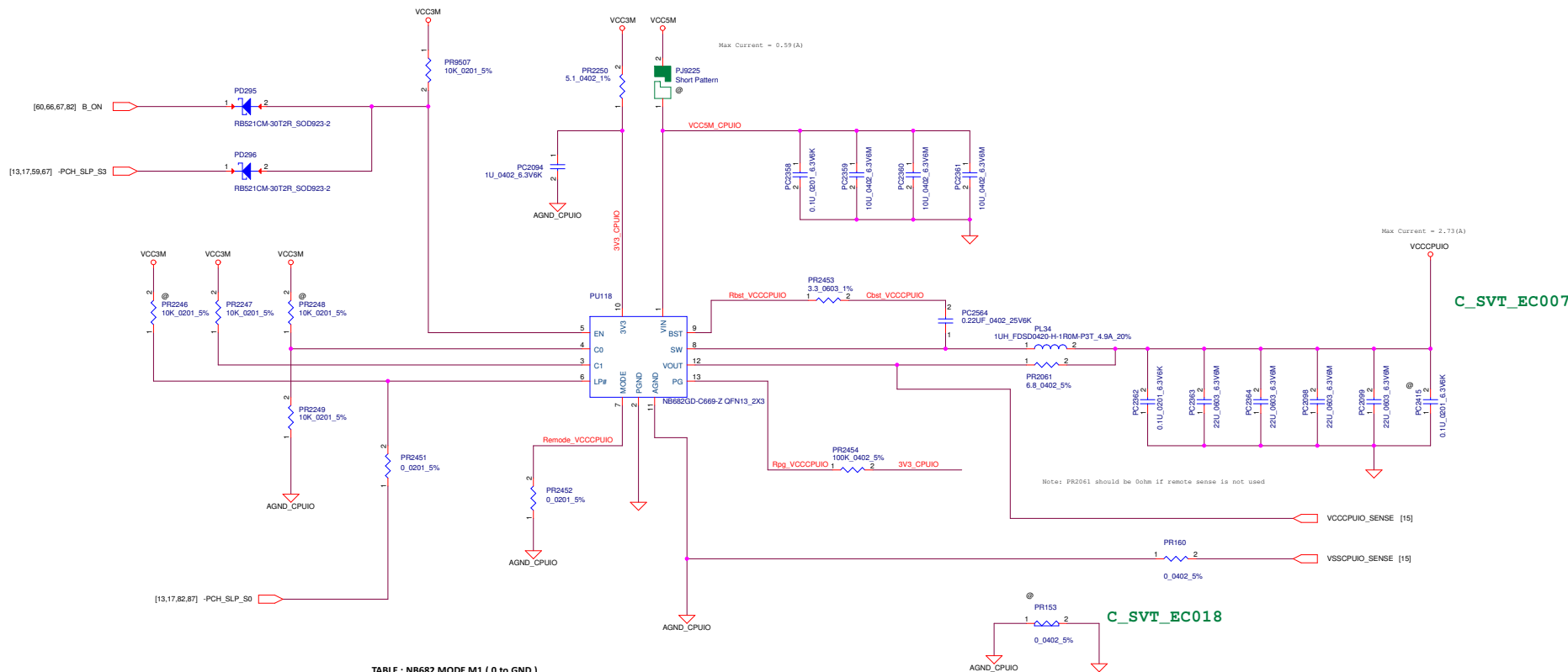
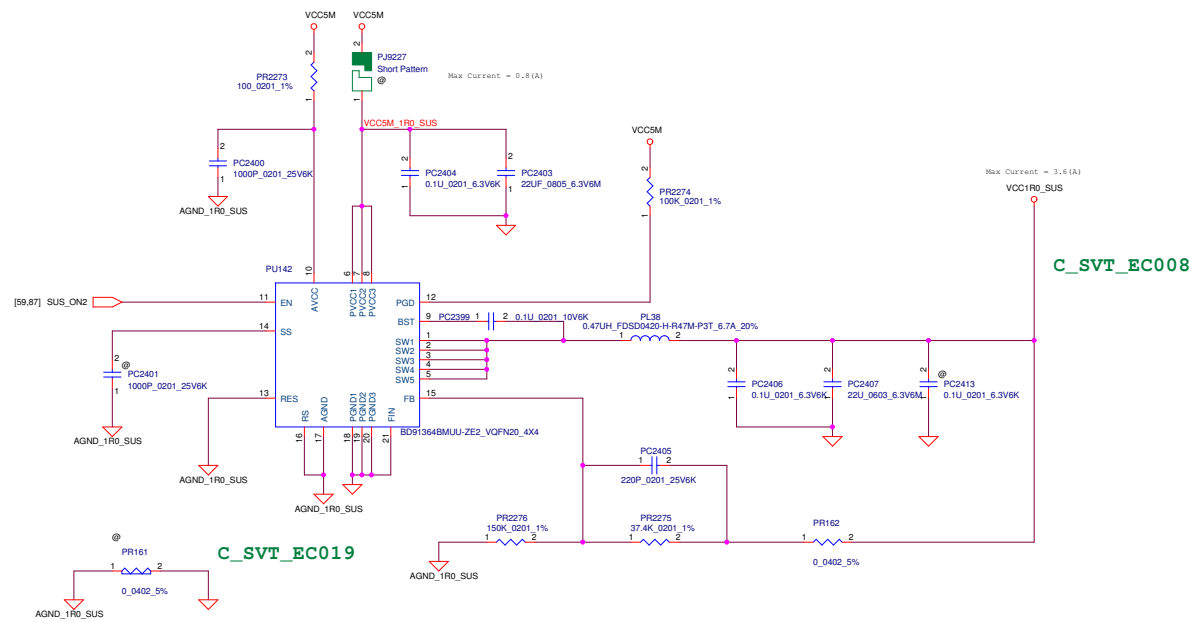


TABLE : NB682 MODE M1 (0 to GND)

LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

← SLP_S0#

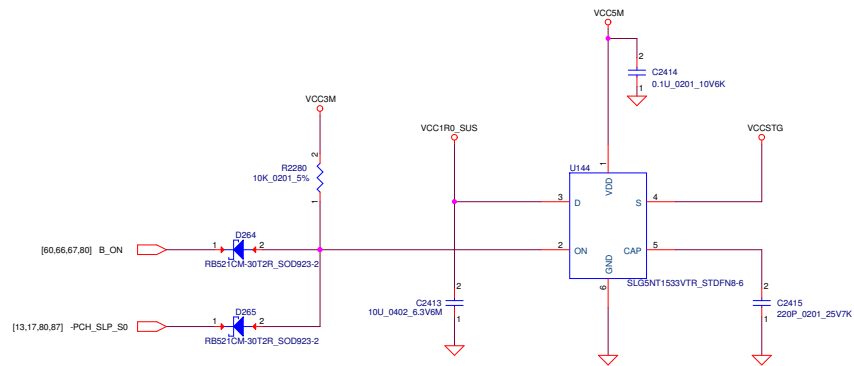
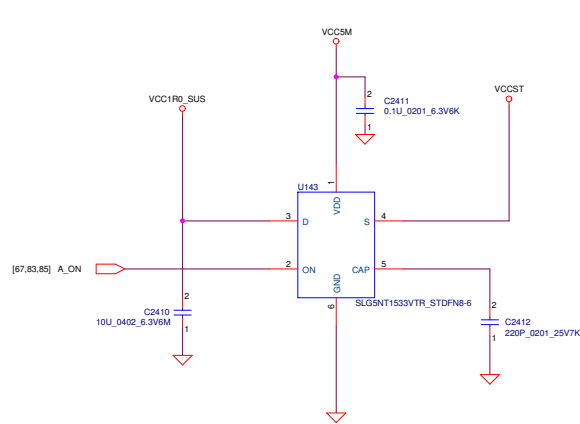
← LOGIC



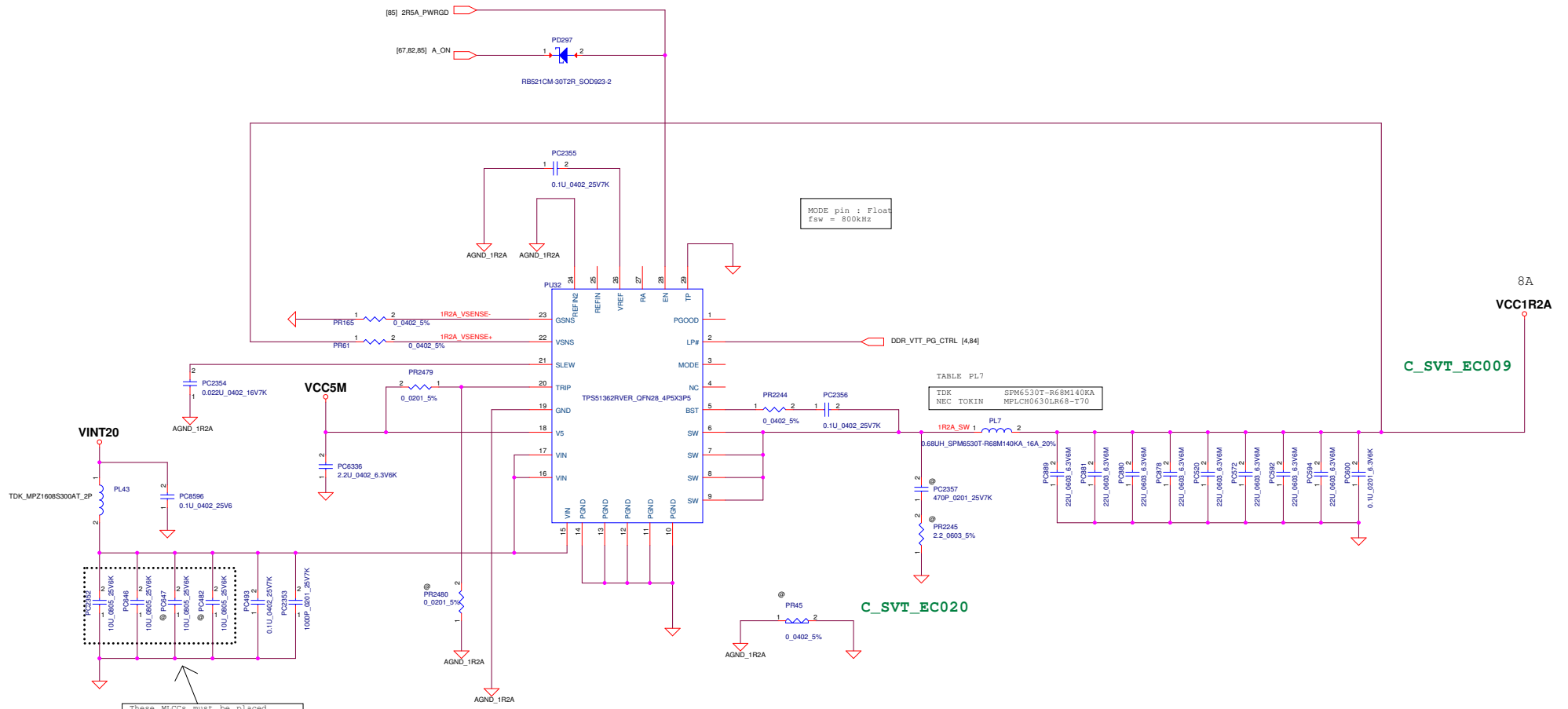
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C_SVT_EC019

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These MLCCs must be placed symmetrically on Top and Bottom.

MODE pin : Float
fsw = 800kHz

TABLE:TPS51362

REFIN	REFIN2	VOUT
GND	GND	1.05V
Float	GND	1.20V
GND	Float	1.50V
Float	Float	1.35V

← LOGIC

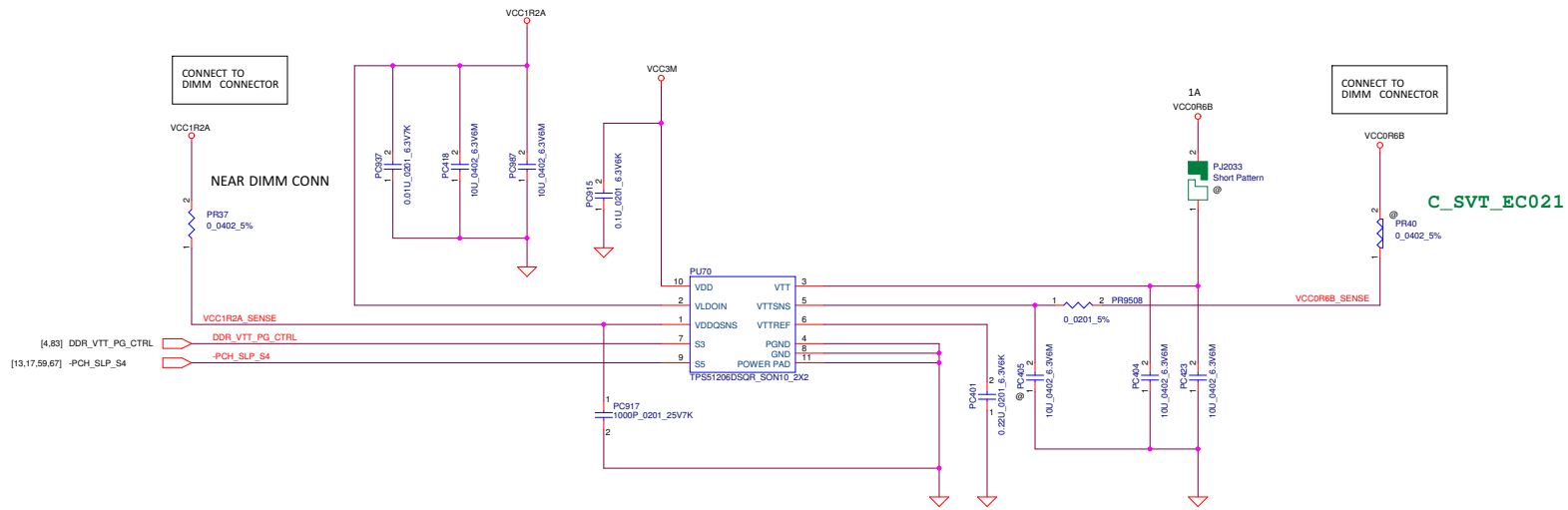
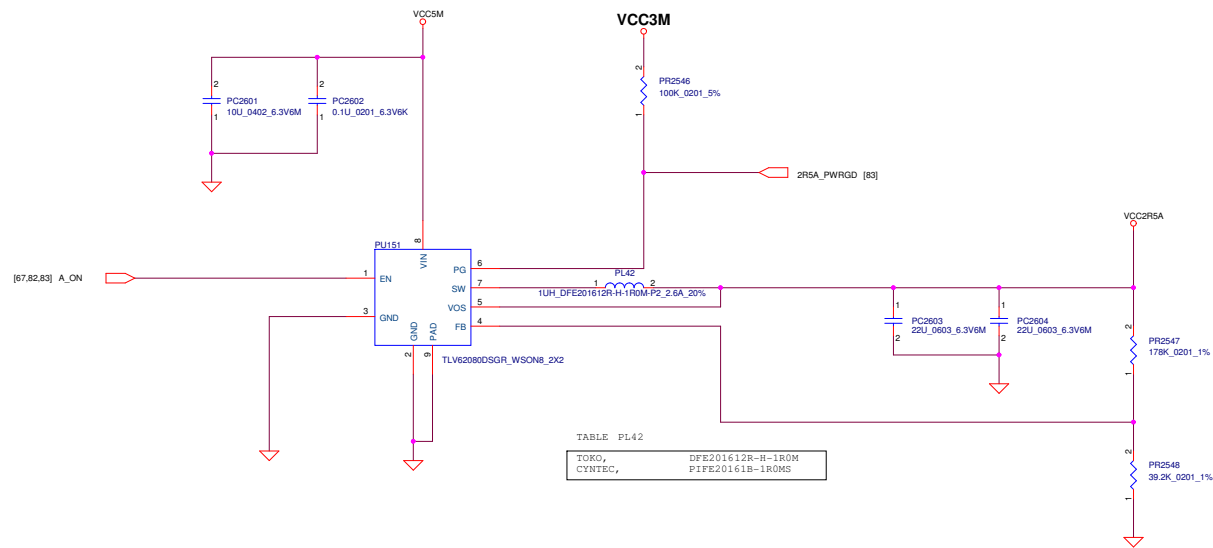
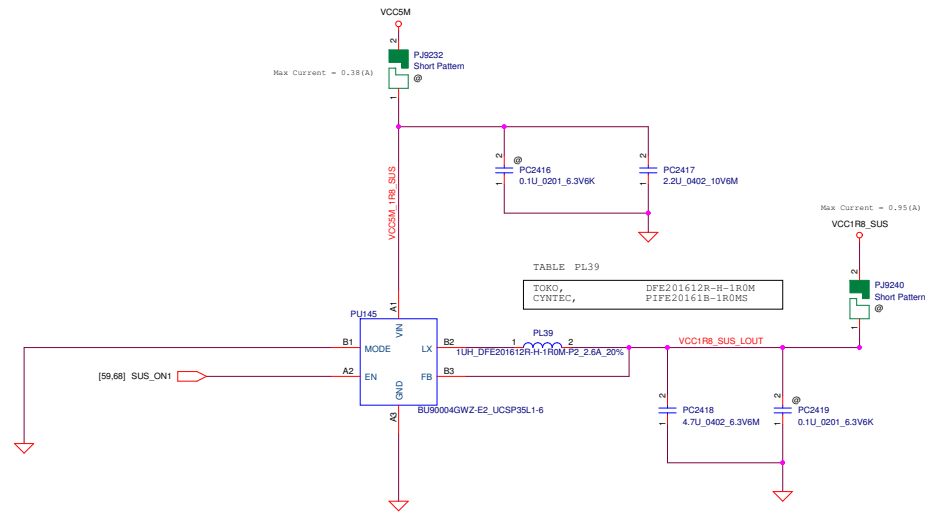


TABLE : TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)



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DC/DC VCC1R8 SUS
 Size: 11.0 x 17.0
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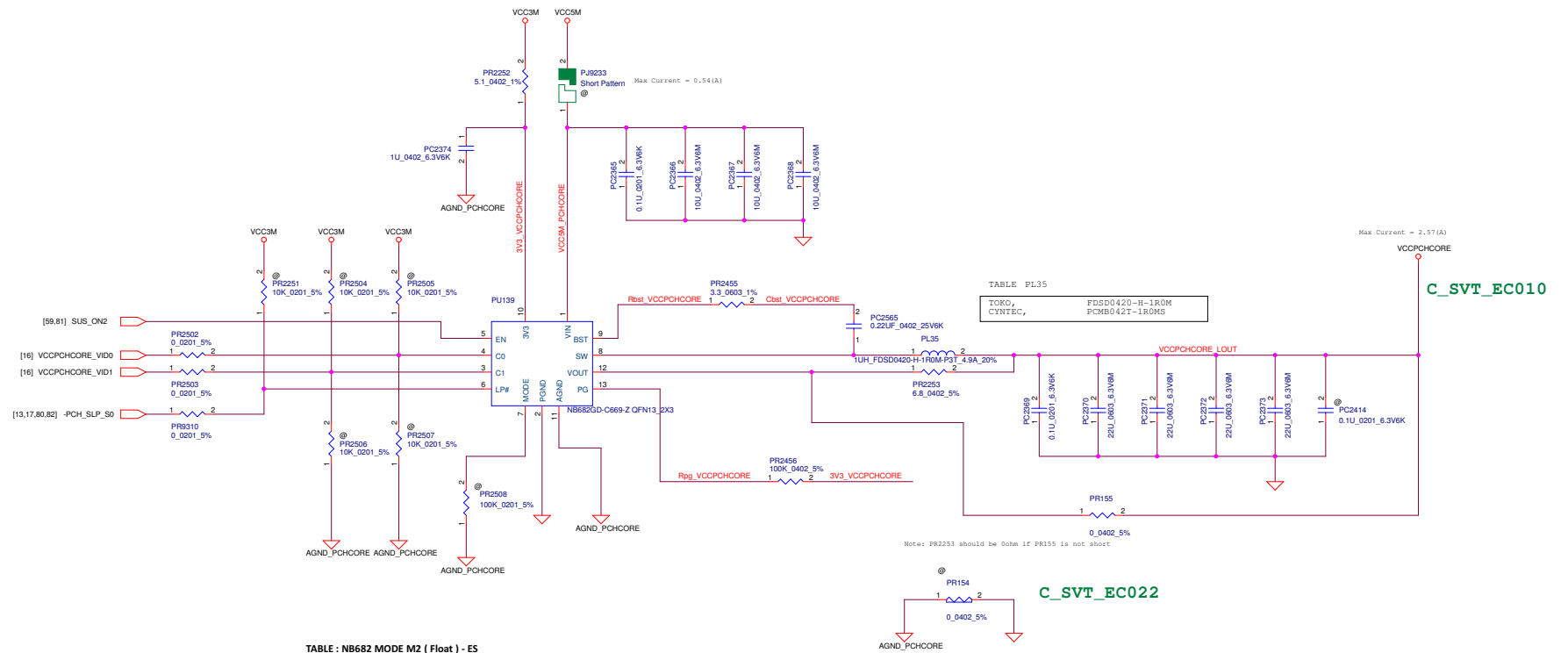


TABLE : NB682 MODE M2 (Float) - ES

LP#	C1	C0	VOUT
0	X	X	0.700V
1	0	0	0.850V
1	0	1	0.900V
1	1	0	0.950V
1	1	1	1.000V

← SLP_S0#

← DEFAULT

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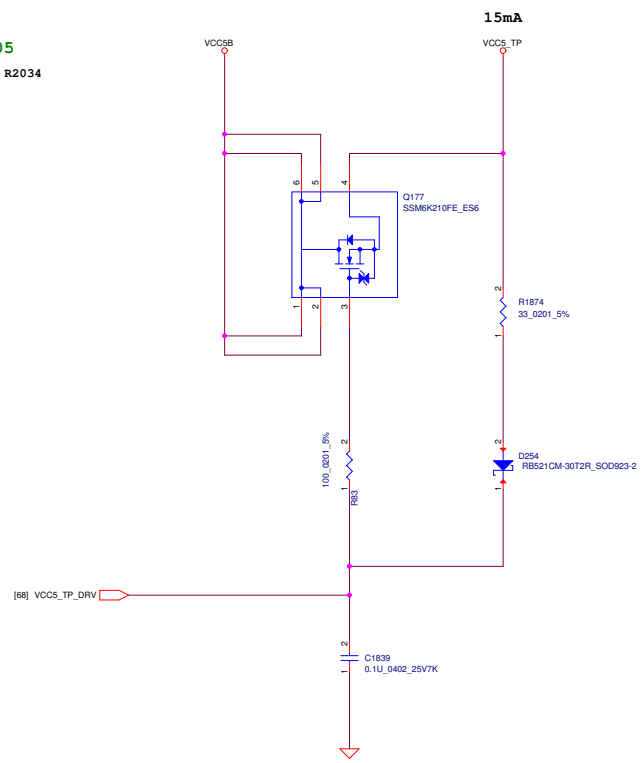
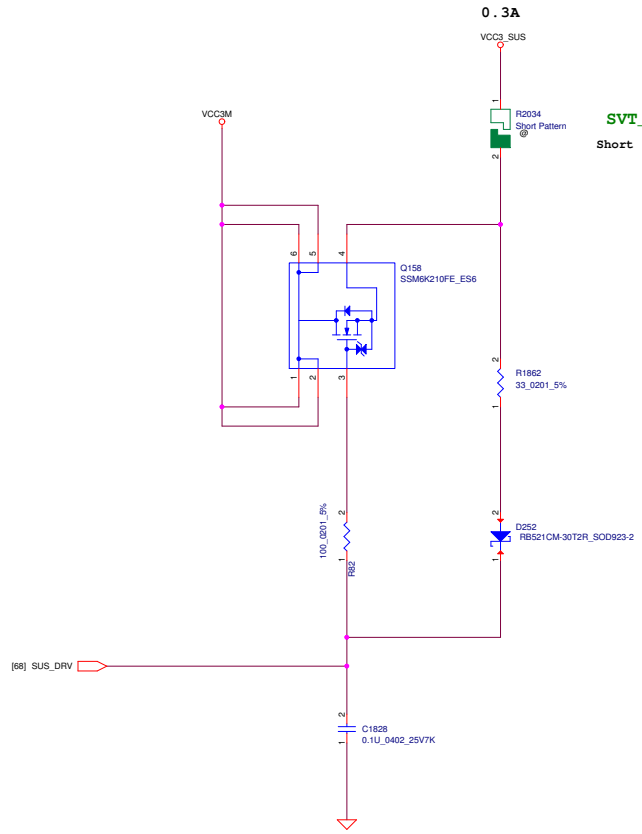
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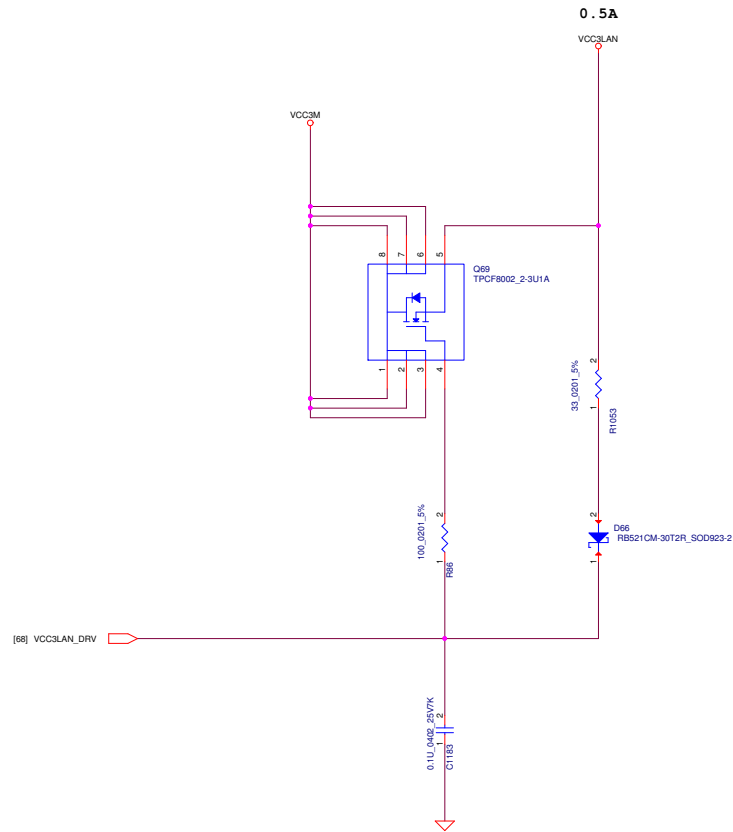
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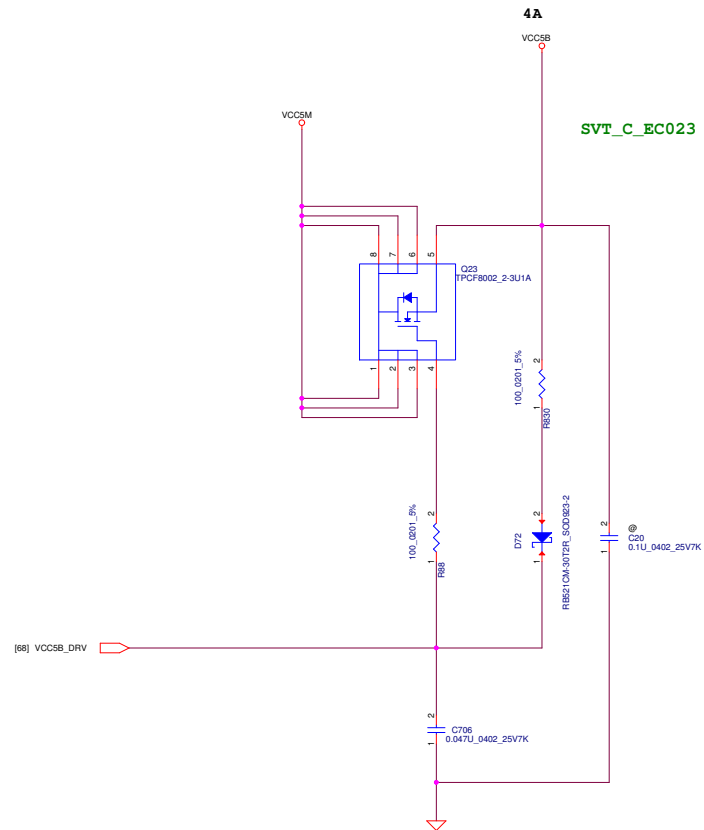
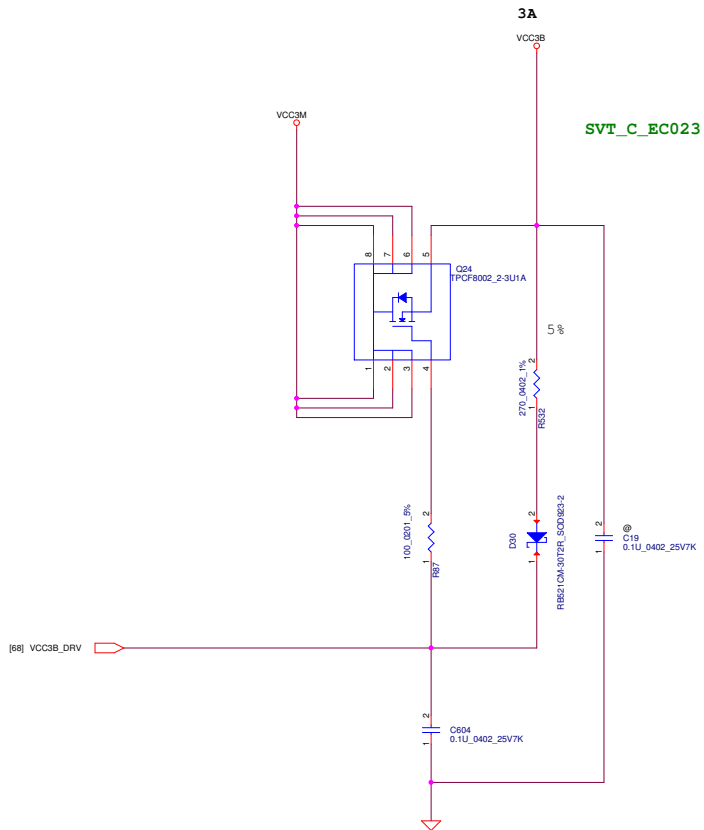
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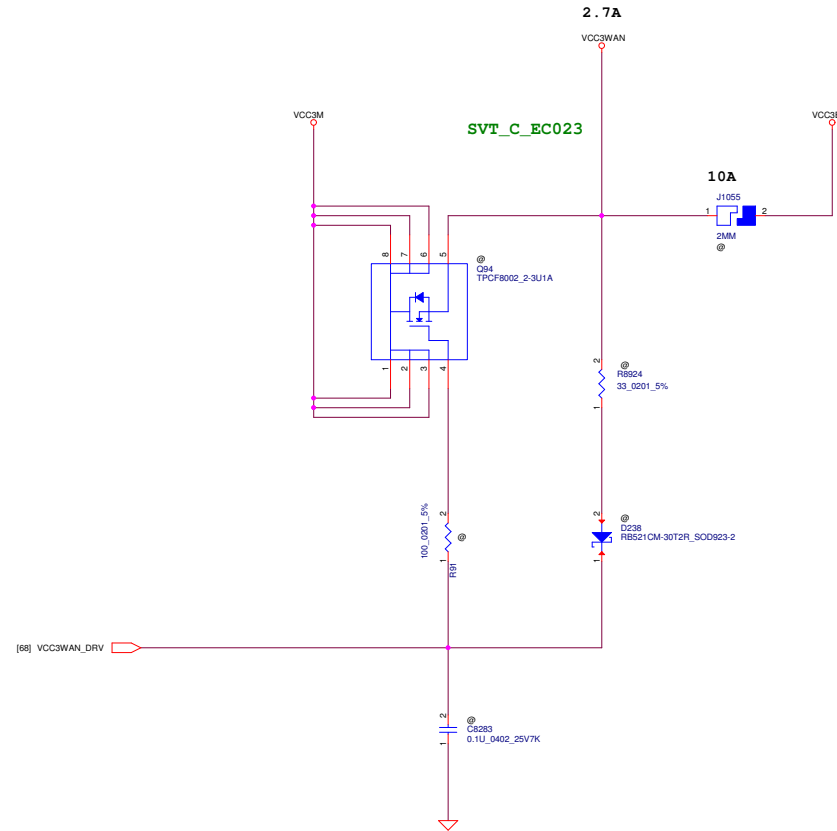
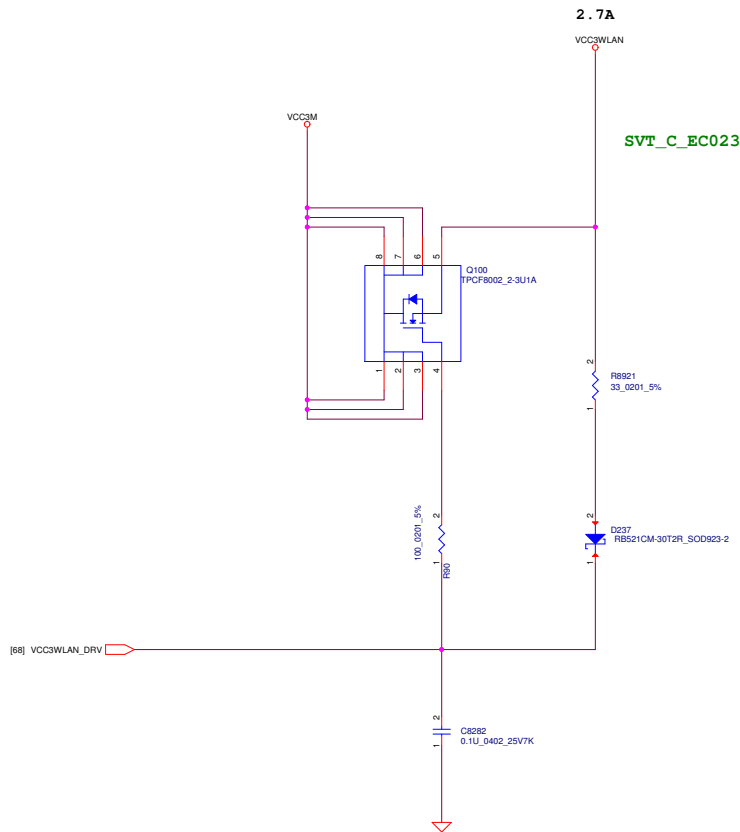
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TABLE

	YES	NO
AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R91	ASM	NO-ASM
R8924	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

↑
LOGIC

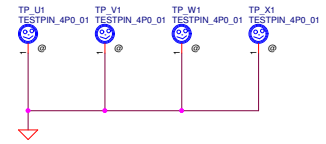
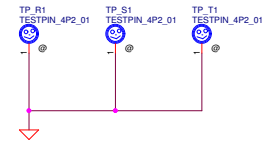
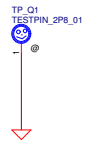
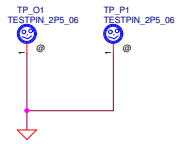
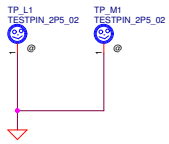
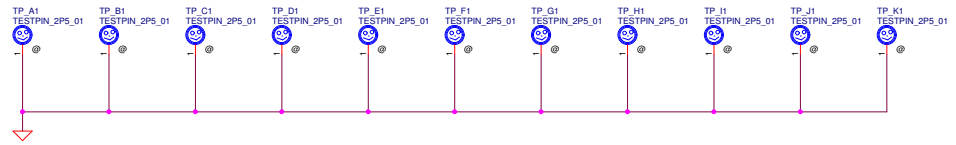
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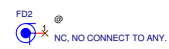
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PTH FOR SCREW HOLE

Value	Hole Dia	Pad Dia		QTY
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6	6	11
TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



NPTH



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Board Area

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