KL1 BLOCK DIAGRAM

01

PCB STACK UP
8L

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU (Penryn)
478P (uPGA)/35W
PAGE 4,5

CPU THERMAL SENSOR
PAGE 5

CPU CORE(MAX17021)
PAGE 41

FSB 667/800/1066

14.318MHz

CLOCK GEN
ICS9LPRS365BGLFT
PAGE 3

CLK_CPU_BCLK,CLK_CPU_BCLK#
CLK_MCH_BCLK,CLK_MCH_BCLK#
DREFCLK,DREFCLK#
DREFSSCLK,DREFSSCLK#

VCCP +1.05V AND GMCH +1.5V(RT8204)
PAGE 28

PCI-Express 1X

Level-Shifter(PS8101)
PAGE 22

GDDR3 X 2 (256MB)
PAGE 18

GDDR3 X 2 (256MB)
PAGE 19

FBA
FBC

NORTH BRIDGE
Cantiga
PAGE 6~10

27MHz

NVIDIA
N10M-GS1(64bit)
N10P-GE1(128bit)
PAGE 13~19

HDMI CONN
PAGE 22

CRT CONN
PAGE 20

VGACORE(OZ8119)
PAGE 42

LCD CONN
PAGE 21

Single link

PCI-Express 16X

DDR III (TPS51116REGR)
1.5VSUS/SMDDR_VTERM
/SMDDR_VREF
PAGE 39

DDRIII-SODIMM1
PAGE 11

DDRIII-SODIMM2
PAGE 12

DDRIII 800/1066 MHz
DDRIII 800/1066 MHz

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

USB2.0

SOUTH BRIDGE
ICH-9M
PAGE 23,24,25,26

SATA - HDD
PAGE 35

SATA - CD-ROM
PAGE 35

USB+eSATA
PAGE 32

SATA0 150MB
SATA1 150MB
SATA5 150MB

0,1,8
USB2.0 Ports X3
PAGE 32

9
USB+eSATA Port X1
PAGE 32

4
BlueTooth
PAGE 36

2
CCD Module
PAGE 37

6,10,11
Mini PCI-E Card X 2 Express Card
PAGE 33,36

PCI-E

Azalia

X2
Mini PCI-E Card
(WLAN/ WWAN)
PAGE 33

X1
LAN
BCM5784M
(10/100/1G LAN)
PAGE 29,30

X1
Express Card
(NEW CARD)
PAGE 36

X1
Card Reader
JMB380
PAGE 27

24.576MHz

25MHz

RJ45 CONN
PAGE 30

1394 CONN
PAGE 27

6-IN-1 Card Reader CONN
PAGE 28

AUDIO CODEC
ALC269Q-GR
PAGE 31

Digital MIC
(Internal MIC)
PAGE 31

Audio Jack
(External MIC)
PAGE 31

Head-Phone Jack + SPDIF
PAGE 31

SYSTEM POWER(ISL6237)
PAGE 40

SYSTEM CHARGER(ISL6251A)
PAGE 28

32.768KHz

LPC

EC
IT8512E
PAGE 34

Touch Pad
PAGE 36

Keyboard
PAGE 37

CIR
PAGE 34

FAN
PAGE 37

SPI BIOS
PAGE 34

PROJECT : KL1
Quanta Computer Inc.

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Custom	BLOCK DIAGRAM	A1A

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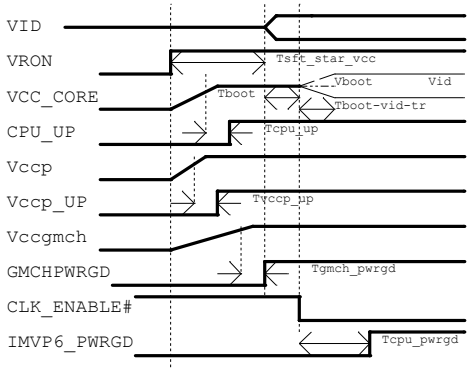
Board Stack up Description

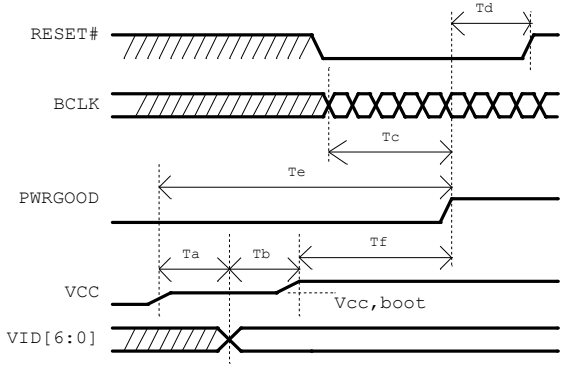
PCB Layers

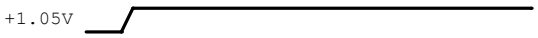
Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Penryn Power-up Timing Specifications



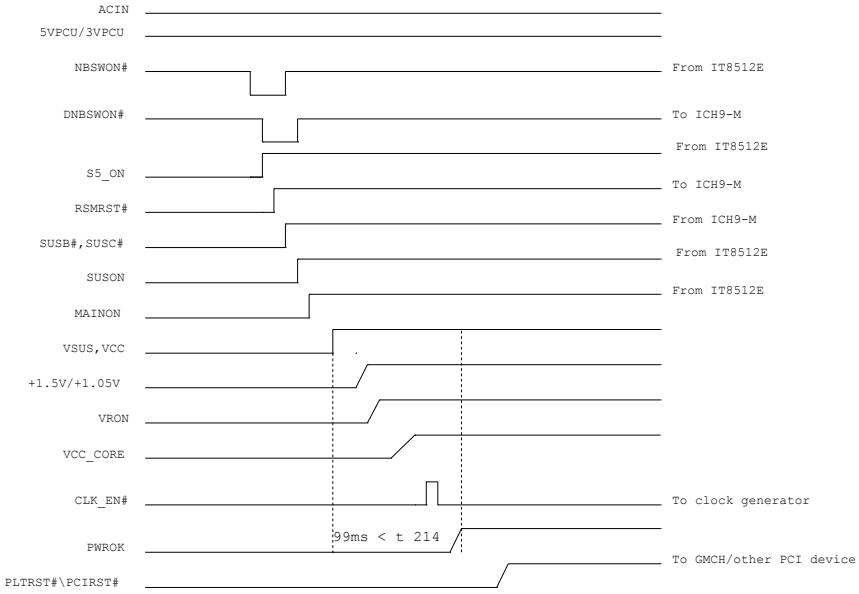


Ta=VCC and VCCP asseration to VID[6:0] vaild
Tb=VID[6:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	V				VRON
+1.5V	V				MAINON
+1.05V	V				MAINON
5V_S5/3V_S5	V	V	V	V	S5_ON
5VSUS/3VSUS/1.5VSUS	V	V			SUSON
SMDDR_VTERM/+3V/+5V/+15V/+1.8V	V				MAINON
+VGACORE/+VGA1.1V	V				MAINON
LANVCC	V	V			LAN_ON
3VPCU	V	V	V	V	VL
5VPCU	V	V	V	V	VL

ACIN POWER ON TIMING



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM INFORMATION	A1A

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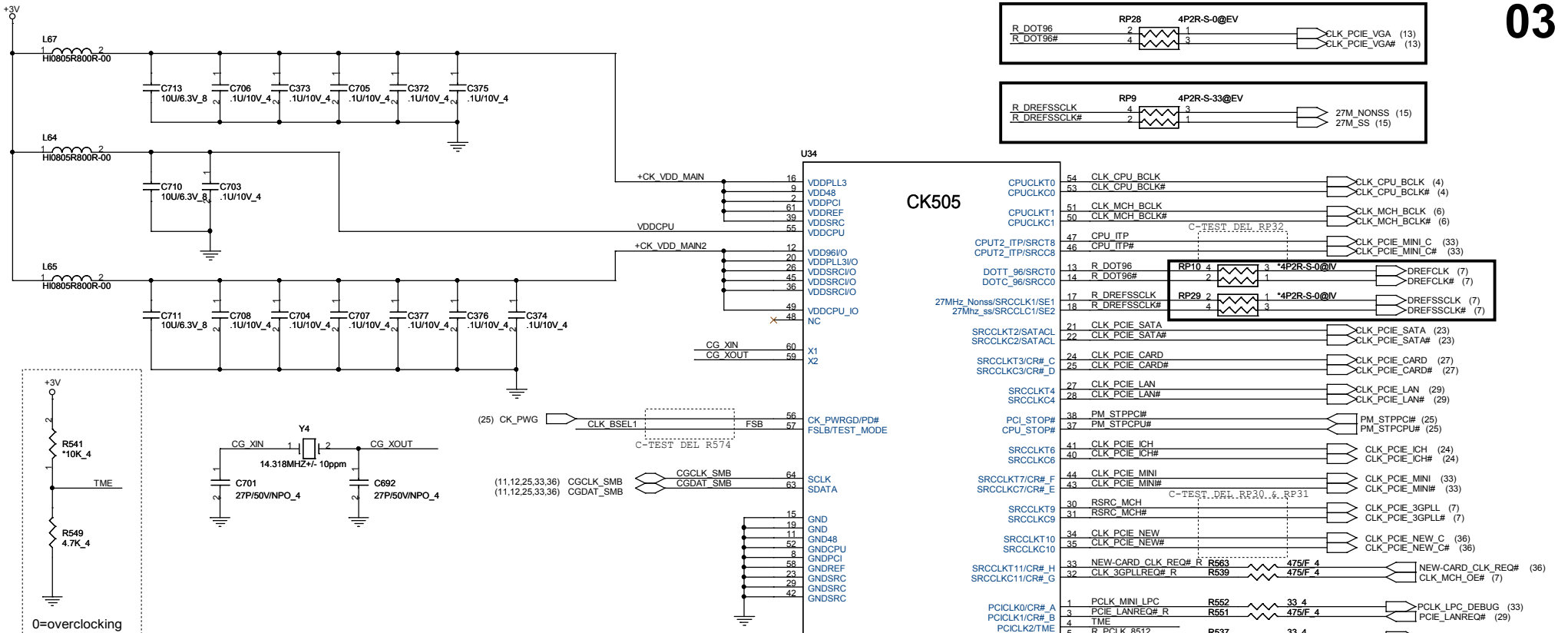
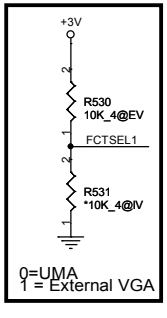
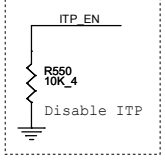






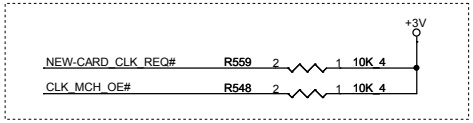
GCLK_SEL = FCTSEL1

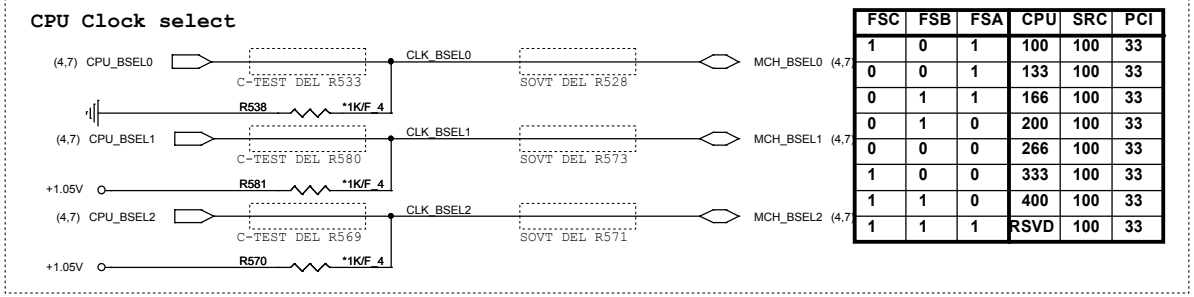
FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CK505 TSSOP64

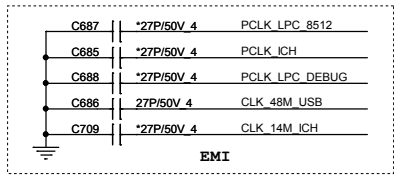
Realtek RTM875T-606-VD-GRT AL000875K00

ICS ICS9LPRS365BGLFT ALPRS365K13





FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	A1A
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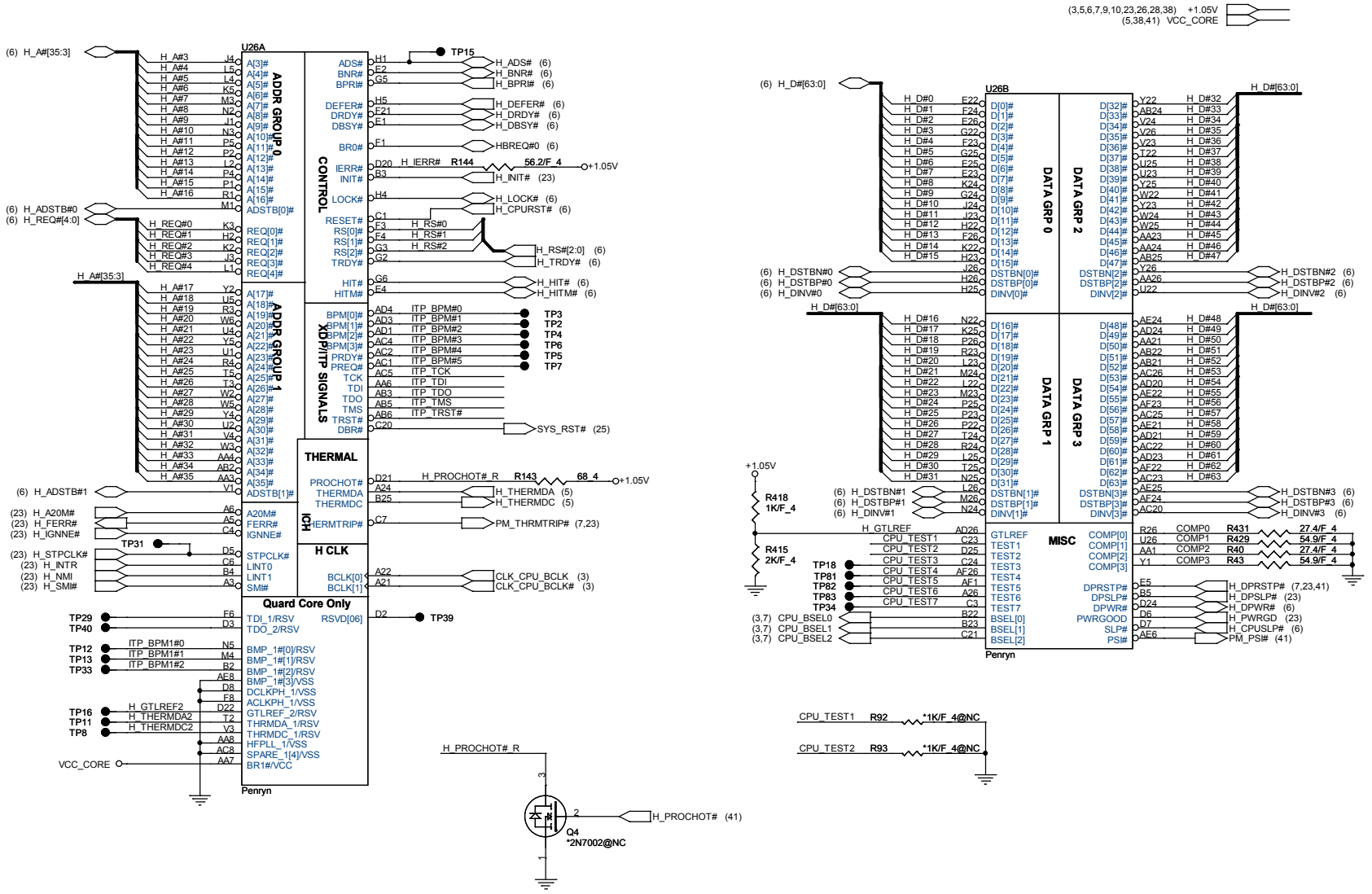
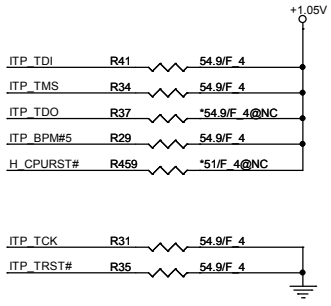
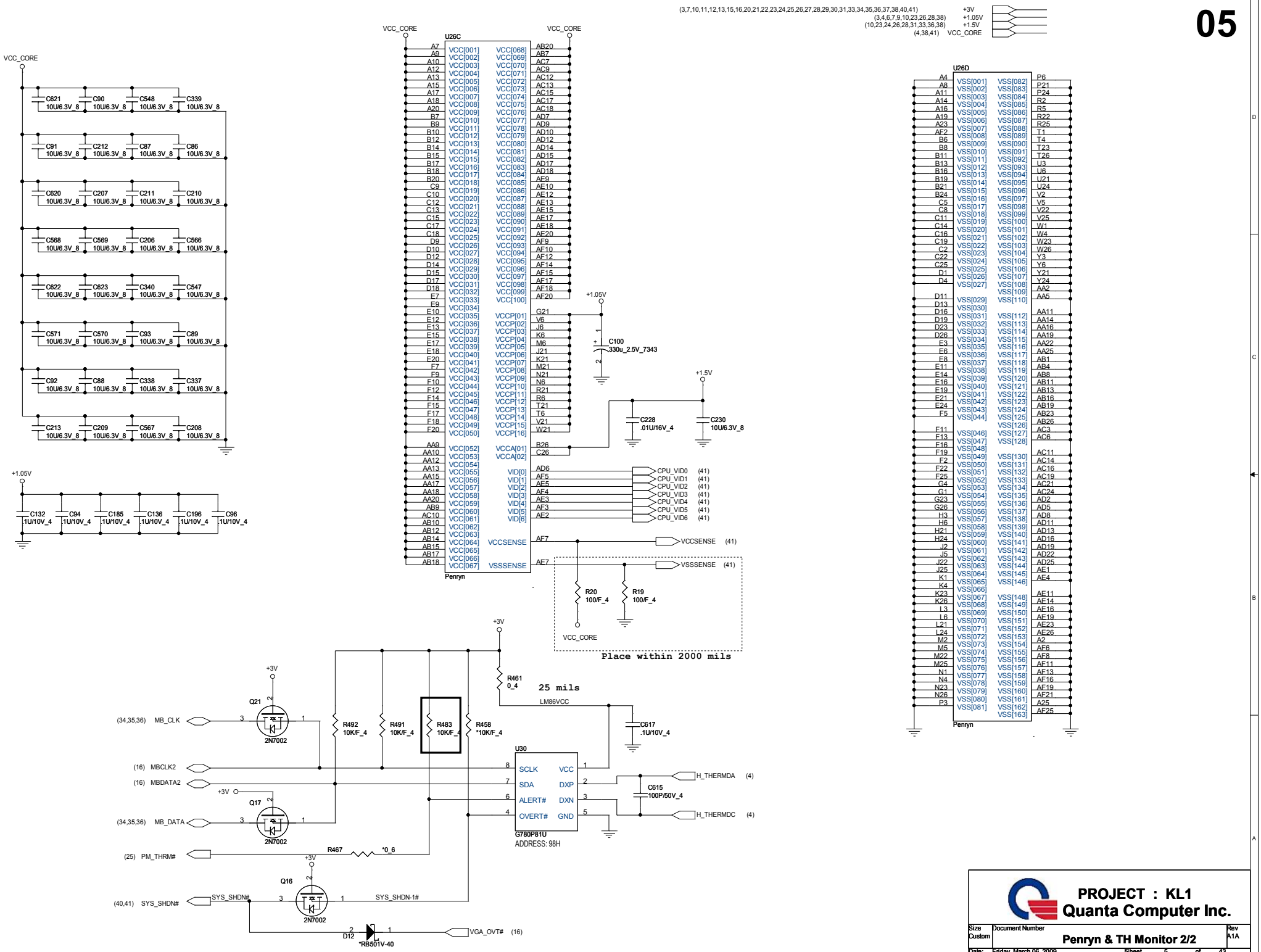


Populate ITP700Flex for bringup



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn 1/2	A1A
Date: Friday, March 06, 2009	Sheet 4 of 43	



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn & TH Monitor 2/2	A1A
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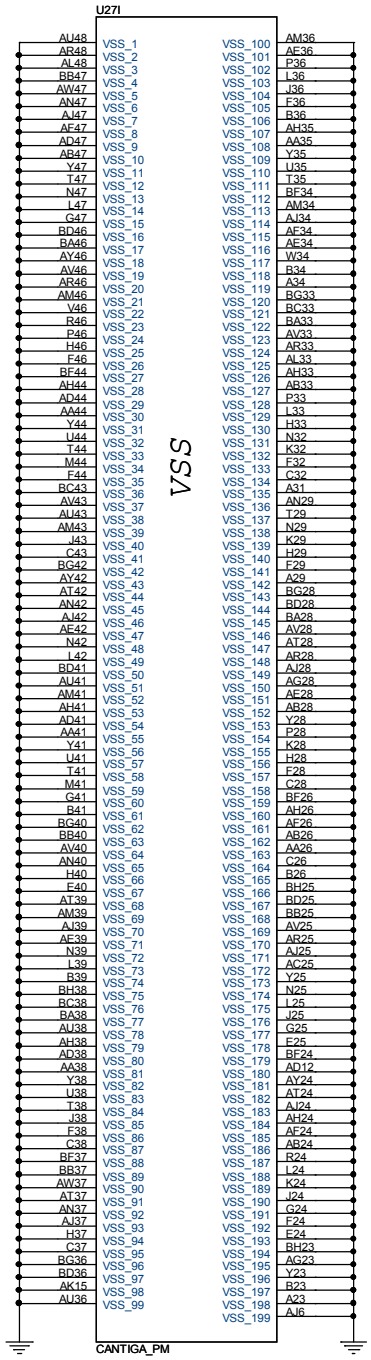

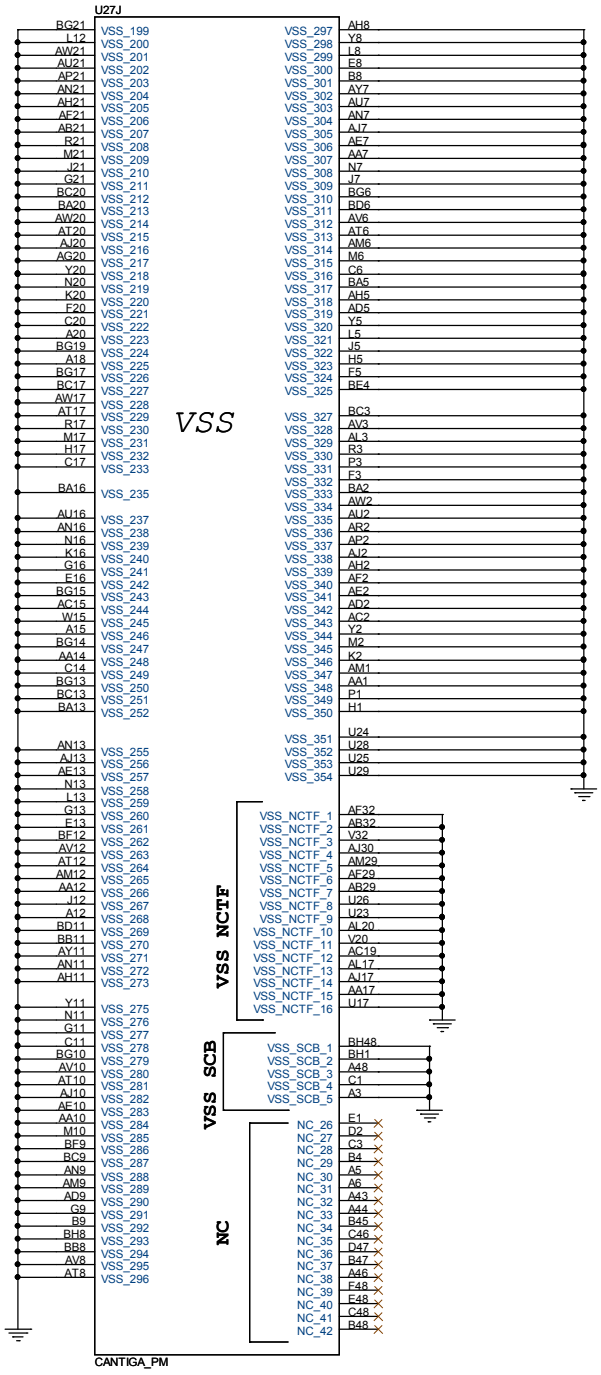

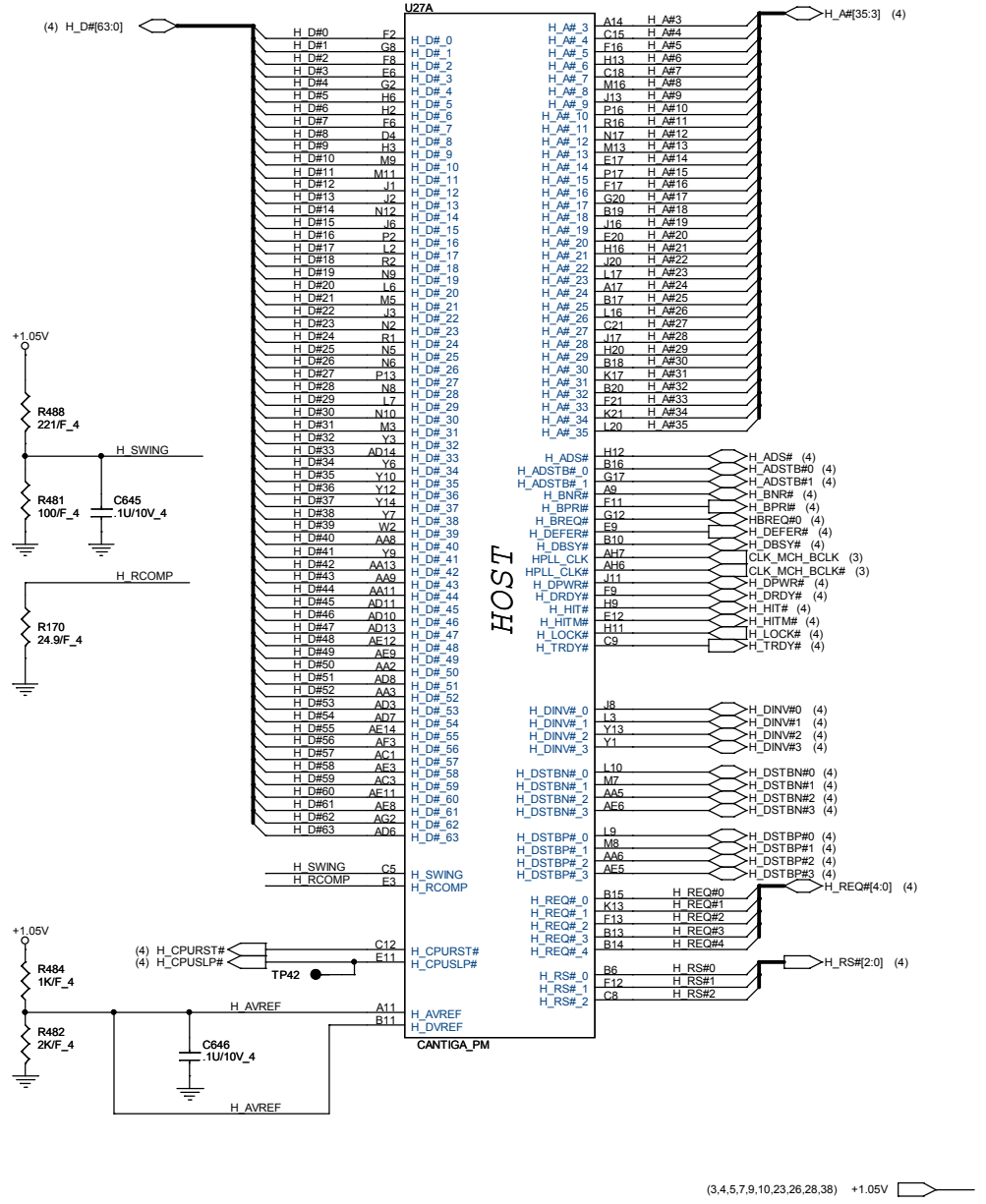

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Host & VSS 1/5	A1A
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MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reversed

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

U27B

RSVD
RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK / CONTROL/COMPENSATION
SA_CK_0 SA_CK_1 SA_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#
M_A_CLK0 M_A_CLK1 M_B_CLK0 M_B_CLK1 M_A_CLK0# M_A_CLK1# M_B_CLK0# M_B_CLK1# M_A_CKE0 M_A_CKE1 M_B_CKE0 M_B_CKE1 M_A_CS#0 M_A_CS#1 M_B_CS#0 M_B_CS#1 M_A_ODT0 M_A_ODT1 M_B_ODT0 M_B_ODT1
SM_RCOMP R411 80.6/F_4
SM_RCOMP# R410 80.6/F_4
SM_RCOMP_VOH
SM_RCOMP_VOL
SMVREF_MCH
SM_PWROK
SM_REXT R44 499/F_4
DDR3_DRAMRST# (11,12)
1.5VSUS
R52 15K/F_4
DDR3_PWG (39)
R57 18.7K/F_4

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#
DREFCLK (3) DREFCLK# (3) DREFSSCLK (3) DREFSSCLK# (3)
PEG_CLK PEG_CLK#
CLK_PCIE_3GPLL (3) CLK_PCIE_3GPLL# (3)

JTAG
ME_JTAG_TCK ME_JTAG_TDI ME_JTAG_TDO ME_JTAG_TMS
TP17 TP14 TP10 TP9

DMI
DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3
DMI_TXN[3:0] (24) DMI_TXP[3:0] (24)
DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3
DMI_RXN[3:0] (24) DMI_RXP[3:0] (24)

CFG
(3,4) MCH_BSEL0 (3,4) MCH_BSEL1 (3,4) MCH_BSEL2
MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_19 MCH_CFG_20
+3V

GRAPHICS VID
GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN
GFXVR_VID_0 GFXVR_VID_1 GFXVR_VID_2 GFXVR_VID_3 GFXVR_VID_4 GFXVR_EN
TP86 TP43 TP27 TP35 TP41 TP85

PM
(25) PM_SYNC# (4,23,41) H_DPRSTP# (11,12) PM_EXTTS#0 PM_EXTTS#1 (25,41) DELAY_VR_PWRGOOD (13,24) PLT_RST-R# (4,23) PM_THRMTRIP# (25,41) DPRSLPVR
R56 100/F_4 RST_IN# MCH
R117 *0_4 PM_THRMTRIP# R
PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF
CL_CLK0 (25) CL_DATA0 (25) ECPWROK (25,34) CL_RST#0 (25)
0.35 V MCH_CLVREF
C193 1U/10V_4
R73 1K/F_4
R74 499/F_4
+1.05V

MISC
DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC#
TSATN#
SDVO_CLK (22) SDVO_DATA (22) CLK_MCH_OE# (3) MCH_ICH_SYNC# (25)
MCH_TSATN R478 56.2/F_4
TP22 TP21

HDA
HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC
ACZ_BITCLK_MCH (23) ACZ_RST#_MCH (23) ACZ_SDIN3 (23) ACZ_SDOUT_MCH (23) ACZ_SYNC_MCH (23)
ACZ_SDIN3 MCH R475 *0_4@0V

NC
BG48 BF48 BD48 BC48 BH47 BG47 BE47 BH46 BF46 BG45 BH44 BH43 BH5 BG4 BH3 BH5 BG4 BF3 BH2 BG2 BE2 BG1 BF1 BD1 BC1 F1 A47
NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26
R124 10K/F_4 PM_EXTTS#0
R116 10K/F_4 PM_EXTTS#1

CANTIGA_PM

(3,5,10,11,12,13,15,16,20,21,22,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(9,10,11,12,38,39) 1.5VSUS
(3,4,5,6,9,10,23,26,28,38) +1.05V
(3,4,5,6,9,10,23,26,28,38) +1.05V_PEG

UMA & Discrete setting
LVDS Discrete / UMA
R120 NC 10K
R131 NC 10K
R120 *10K/F_4@0V
R131 *10K/F_4@0V
+3VO

(21) INT_DPST_PWM
(21) INT_LVDS_BLON
(21) INT_EDIDCLK
(21) INT_EDIDDATA
(21) INT_DISP_ON

LVDS Discrete / UMA
R474 NC 2.37K
UMA & Discrete setting
R474 *2.37K/F_4@0V
TP88

U27C

LVDS
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK LVDSA_DATA#_0 LVDSA_DATA#_1 LVDSA_DATA#_2 LVDSA_DATA#_3 LVDSA_DATA_0 LVDSA_DATA_1 LVDSA_DATA_2 LVDSA_DATA_3 LVDSB_DATA#_0 LVDSB_DATA#_1 LVDSB_DATA#_2 LVDSB_DATA#_3 LVDSB_DATA_0 LVDSB_DATA_1 LVDSB_DATA_2 LVDSB_DATA_3

(21) LA_CLK# (21) LA_CLK
(21) LA_DATAN0 (21) LA_DATAN1 (21) LA_DATAN2
(21) LA_DATAP0 (21) LA_DATAP1 (21) LA_DATAP2
TP45 TP84 TP48 TP47 TP49 TP36 TP38 TP28 TP87 TP46 TP44 TP26

TV
TVA_DAC TVB_DAC TVC_DAC TV_RTN TV_DCONSEL_0 TV_DCONSEL_1
R171 0@EV_75@0V TV_COMP1
R156 0@EV_75@0V TV_Y/G1
R142 0@EV_75@0V TV_C/R1
R173 *0@0V TV_DCONSEL0
R161 *0@0V TV_DCONSEL1

VGA
CRT_BLUE CRT_GREEN CRT_RED CRT_IRTN CRT_DDC_CLK CRT_DDC_DAT CRT_HSYNC CRT_TVO_IREF CRT_VSYNC
(20) INT_CRT_BLU
(20) INT_CRT_GRN
(20) INT_CRT_RED
(20) INT_CRT_DDCCLK
(20) INT_CRT_DDCDAT
(20) INT_HSYNC
(20) INT_VSYNC
R159 0@EV_150@0V
R158 0@EV_150@0V
R149 0@EV_150@0V
R147 *33@0V HSYNC_INT
R160 0@EV_1.02K@0V CRTIREF
R133 *33@0V VSYNC_INT

PCI-EXPRESS GRAPHICS
PEG_TX#[15:0] PEG_TX[15:0] PEG_RX#[15:0] PEG_RX[15:0]
PEG_TX#[15:0] (13) PEG_TX[15:0] (13) PEG_RX#[15:0] (13) PEG_RX[15:0] (13)
PEG_COMPI PEG_COMPO
T37 PEG_COMP R113 49.9/F_4
+1.05V_PEG
PEG_RX#_0 PEG_RX#_1 PEG_RX#_2 PEG_RX#_3 PEG_RX#_4 PEG_RX#_5 PEG_RX#_6 PEG_RX#_7 PEG_RX#_8 PEG_RX#_9 PEG_RX#_10 PEG_RX#_11 PEG_RX#_12 PEG_RX#_13 PEG_RX#_14 PEG_RX#_15
PEG_RX_0 PEG_RX_1 PEG_RX_2 PEG_RX_3 PEG_RX_4 PEG_RX_5 PEG_RX_6 PEG_RX_7 PEG_RX_8 PEG_RX_9 PEG_RX_10 PEG_RX_11 PEG_RX_12 PEG_RX_13 PEG_RX_14 PEG_RX_15
R150 HDMI_HPD# *0_4@0V
PEG_TX#_0 PEG_TX#_1 PEG_TX#_2 PEG_TX#_3 PEG_TX#_4 PEG_TX#_5 PEG_TX#_6 PEG_TX#_7 PEG_TX#_8 PEG_TX#_9 PEG_TX#_10 PEG_TX#_11 PEG_TX#_12 PEG_TX#_13 PEG_TX#_14 PEG_TX#_15
PEG_TX_0 PEG_TX_1 PEG_TX_2 PEG_TX_3 PEG_TX_4 PEG_TX_5 PEG_TX_6 PEG_TX_7 PEG_TX_8 PEG_TX_9 PEG_TX_10 PEG_TX_11 PEG_TX_12 PEG_TX_13 PEG_TX_14 PEG_TX_15
C_PEG_TX#0 C626 1U/10V_4@EV PEG_TX#0
C_PEG_TX#1 C612 1U/10V_4@EV PEG_TX#1
C_PEG_TX#2 C609 1U/10V_4@EV PEG_TX#2
C_PEG_TX#3 C605 1U/10V_4@EV PEG_TX#3
C_PEG_TX#4 C601 1U/10V_4@EV PEG_TX#4
C_PEG_TX#5 C598 1U/10V_4@EV PEG_TX#5
C_PEG_TX#6 C593 1U/10V_4@EV PEG_TX#6
C_PEG_TX#7 C590 1U/10V_4@EV PEG_TX#7
C_PEG_TX#8 C585 1U/10V_4@EV PEG_TX#8
C_PEG_TX#9 C583 1U/10V_4@EV PEG_TX#9
C_PEG_TX#10 C578 1U/10V_4@EV PEG_TX#10
C_PEG_TX#11 C572 1U/10V_4@EV PEG_TX#11
C_PEG_TX#12 C562 1U/10V_4@EV PEG_TX#12
C_PEG_TX#13 C560 1U/10V_4@EV PEG_TX#13
C_PEG_TX#14 C552 1U/10V_4@EV PEG_TX#14
C_PEG_TX#15 C550 1U/10V_4@EV PEG_TX#15
C_PEG_TX0 C627 1U/10V_4@EV PEG_TX0
C_PEG_TX1 C616 1U/10V_4@EV PEG_TX1
C_PEG_TX2 C611 1U/10V_4@EV PEG_TX2
C_PEG_TX3 C607 1U/10V_4@EV PEG_TX3
C_PEG_TX4 C603 1U/10V_4@EV PEG_TX4
C_PEG_TX5 C600 1U/10V_4@EV PEG_TX5
C_PEG_TX6 C597 1U/10V_4@EV PEG_TX6
C_PEG_TX7 C592 1U/10V_4@EV PEG_TX7
C_PEG_TX8 C589 1U/10V_4@EV PEG_TX8
C_PEG_TX9 C586 1U/10V_4@EV PEG_TX9
C_PEG_TX10 C581 1U/10V_4@EV PEG_TX10
C_PEG_TX11 C575 1U/10V_4@EV PEG_TX11
C_PEG_TX12 C564 1U/10V_4@EV PEG_TX12
C_PEG_TX13 C561 1U/10V_4@EV PEG_TX13
C_PEG_TX14 C556 1U/10V_4@EV PEG_TX14
C_PEG_TX15 C549 1U/10V_4@EV PEG_TX15

CANTIGA_PM

UMA & Discrete setting
CRT/TV Discrete / UMA

R171	0	75
R156	0	75
R142	0	75
R173	NC	0
R161	NC	0
R159	0	150
R158	0	150
R149	0	150
R147	NC	33
R160	0	1.02K
R133	NC	33

DREFCLK R476 0_4@EV
DREFCLK# R477 0_4@EV
DREFSSCLK R175 0_4@EV
DREFSSCLK# R157 0_4@EV

UMA & Discrete setting
Discrete DREFCLK/ DREFCLK# 0Ω
Discrete DREFSSCLK/ DREFSSCLK# 0Ω
UMA DREFCLK/ DREFCLK# NC
UMA DREFSSCLK/ DREFSSCLK# NC

For UMA HDMI Function

PEG_TX#0 PEG_TX0 RP4 *4P2R-S-0@0V IN_D2# (22) IN_D2 (22)
PEG_TX#1 PEG_TX1 RP3 *4P2R-S-0@0V IN_D1# (22) IN_D1 (22)
PEG_TX#2 PEG_TX2 RP2 *4P2R-S-0@0V IN_D0# (22) IN_D0 (22)
PEG_TX#3 PEG_TX3 RP1 *4P2R-S-0@0V IN_CLK# (22) IN_CLK (22)

C626,C612,C609,C605
C627,C616,C611,C607
Need to install for GM45

(22) HDMI_HPD_CON
+3VO R194 *20K/F_4@0V HDMI_HPD#
Level: 0.9V
Q6 *ME2N7002E@0V
R190 *7.5K/F_4@0V
R192 *100K/F_4@0V

HPD# Inverting Level Shifting Circuit

1.5VSUS
R408 1K/F_4
SM_RCOMP_VOH
C538 .01U/16V_4
C532 2.2U/6.3V_6
R407 3.01K/F_4
SM_RCOMP_VOL
C537 .01U/16V_4
C531 2.2U/6.3V_6
R406 1K/F_4

1.5VSUS
R38 *1K/F_4
SMVREF_MCH
SOVT DEL R39
SMDDR_VREF (11,12,39)
C124 1U/10V_4
C112 470P/50V_4
R45 *1K/F_4

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DMI/DISP 2/5	A1A

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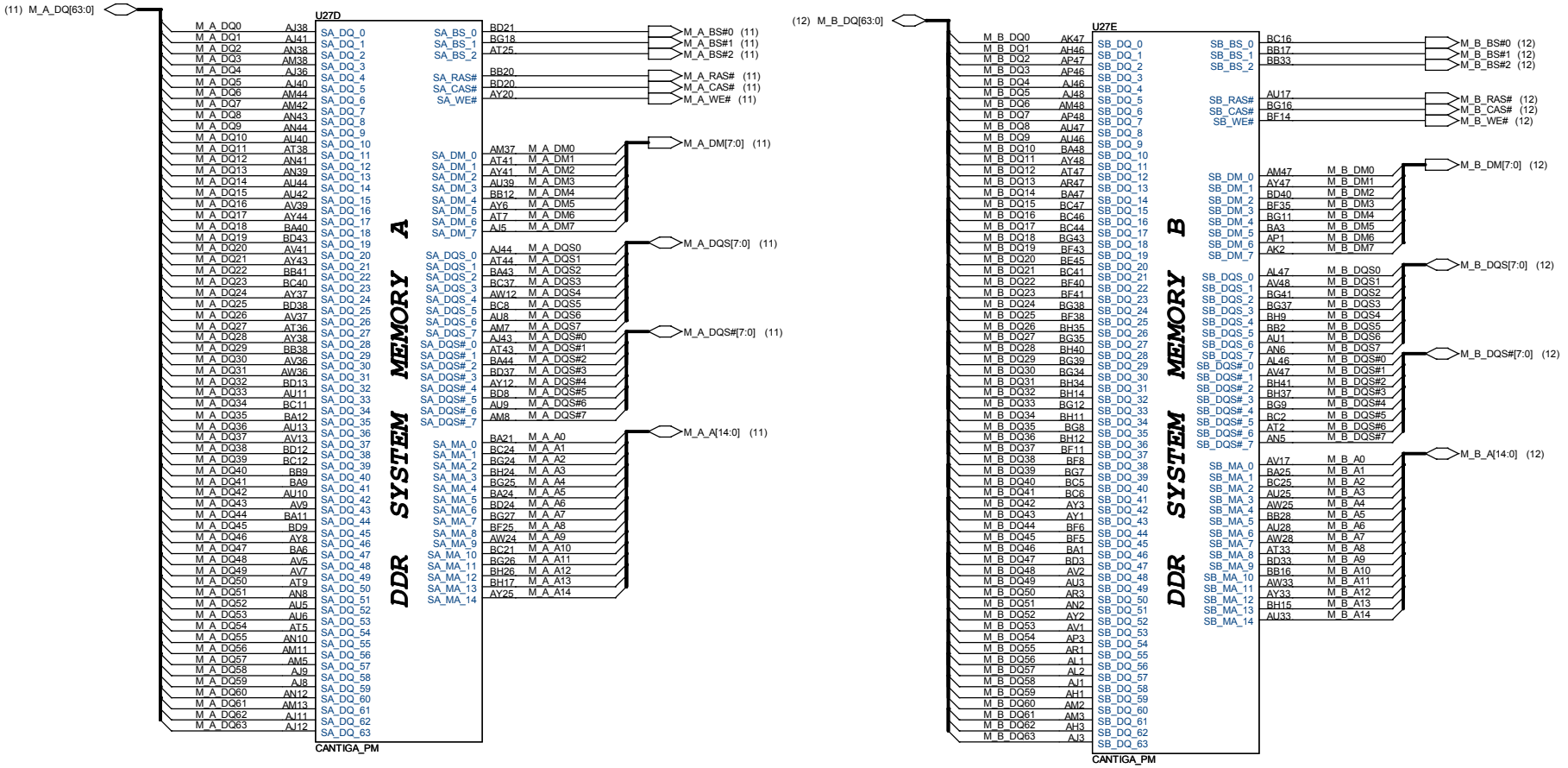


PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DDR3 3/5	A1A
Date: Friday, March 06, 2009	Sheet 8 of 43	

DDR3

1.5VSUS

U27G

VCC SM POWER

VCC_SM_1 AP33
VCC_SM_2 AN33
VCC_SM_3 BH32
VCC_SM_4 BG32
VCC_SM_5 BF32
VCC_SM_6 BD32
VCC_SM_7 BC32
VCC_SM_8 BB32
VCC_SM_9 BA32
VCC_SM_10 AY32
VCC_SM_11 AW32
VCC_SM_12 AV32
VCC_SM_13 AU32
VCC_SM_14 AT32
VCC_SM_15 AR32
VCC_SM_16 AP32
VCC_SM_17 AN32
VCC_SM_18 BH31
VCC_SM_19 BG31
VCC_SM_20 BF31
VCC_SM_21 BG30
VCC_SM_22 BH29
VCC_SM_23 BG29
VCC_SM_24 BF29
VCC_SM_25 BD29
VCC_SM_26 BC29
VCC_SM_27 BB29
VCC_SM_28 BA29
VCC_SM_29 AY29
VCC_SM_30 AW29
VCC_SM_31 AV29
VCC_SM_32 AU29
VCC_SM_33 AT29
VCC_SM_34 AR29
VCC_SM_35 AP29

C126 *.1U/10V_4
C109 *.1U/10V_4
C102 *.1U/10V_4
C101 *.1U/10V_4
C118 *.1U/10V_4
C127 *.1U/10V_4
C151 *.1U/10V_4

VCC_SM_36/NC BA36
VCC_SM_37/NC BB24
VCC_SM_38/NC BD16
VCC_SM_39/NC BB21
VCC_SM_40/NC AW16
VCC_SM_41/NC AW13
VCC_SM_42/NC AT13

+1.05V

VCC GFX POWER

VCC_AXG_1 Y26
VCC_AXG_2 AE25
VCC_AXG_3 AB25
VCC_AXG_4 AA25
VCC_AXG_5 AE24
VCC_AXG_6 AC24
VCC_AXG_7 AA24
VCC_AXG_8 Y24
VCC_AXG_9 AE23
VCC_AXG_10 AC23
VCC_AXG_11 AB23
VCC_AXG_12 AA23
VCC_AXG_13 AJ21
VCC_AXG_14 AG21
VCC_AXG_15 AE21
VCC_AXG_16 AC21
VCC_AXG_17 AA21
VCC_AXG_18 Y21
VCC_AXG_19 AH20
VCC_AXG_20 AF20
VCC_AXG_21 AE20
VCC_AXG_22 AC20
VCC_AXG_23 AB20
VCC_AXG_24 AA20
VCC_AXG_25 T17
VCC_AXG_26 T16
VCC_AXG_27 AM15
VCC_AXG_28 AL15
VCC_AXG_29 AE15
VCC_AXG_30 AJ15
VCC_AXG_31 AH15
VCC_AXG_32 AG15
VCC_AXG_33 AF15
VCC_AXG_34 AB15
VCC_AXG_35 AA15
VCC_AXG_36 Y15
VCC_AXG_37 V15
VCC_AXG_38 U15
VCC_AXG_39 AN14
VCC_AXG_40 AM14
VCC_AXG_41 U14
VCC_AXG_42 T14

+1.05V

R83 10_4
R82 10_4

VCC_AXG_SENSE AJ14
VSS_AXG_SENSE AH14

VCC_AXG_SENSE
VSS_AXG_SENSE

VCC GFX NCTF

VCC_AXG_NCTF_1 W28
VCC_AXG_NCTF_2 V28
VCC_AXG_NCTF_3 V26
VCC_AXG_NCTF_4 W25
VCC_AXG_NCTF_5 V25
VCC_AXG_NCTF_6 W24
VCC_AXG_NCTF_7 V24
VCC_AXG_NCTF_8 W23
VCC_AXG_NCTF_9 V23
VCC_AXG_NCTF_10 AM21
VCC_AXG_NCTF_11 AL21
VCC_AXG_NCTF_12 AK21
VCC_AXG_NCTF_13 W21
VCC_AXG_NCTF_14 V21
VCC_AXG_NCTF_15 U21
VCC_AXG_NCTF_16 AM20
VCC_AXG_NCTF_17 AK20
VCC_AXG_NCTF_18 W20
VCC_AXG_NCTF_19 U20
VCC_AXG_NCTF_20 AM19
VCC_AXG_NCTF_21 AL19
VCC_AXG_NCTF_22 AK19
VCC_AXG_NCTF_23 AJ19
VCC_AXG_NCTF_24 AH19
VCC_AXG_NCTF_25 AG19
VCC_AXG_NCTF_26 AF19
VCC_AXG_NCTF_27 AE19
VCC_AXG_NCTF_28 AB19
VCC_AXG_NCTF_29 AA19
VCC_AXG_NCTF_30 Y19
VCC_AXG_NCTF_31 W19
VCC_AXG_NCTF_32 V19
VCC_AXG_NCTF_33 U19
VCC_AXG_NCTF_34 AM17
VCC_AXG_NCTF_35 AK17
VCC_AXG_NCTF_36 AH17
VCC_AXG_NCTF_37 AG17
VCC_AXG_NCTF_38 AF17
VCC_AXG_NCTF_39 AE17
VCC_AXG_NCTF_40 AC17
VCC_AXG_NCTF_41 AB17
VCC_AXG_NCTF_42 Y17
VCC_AXG_NCTF_43 W17
VCC_AXG_NCTF_44 V17
VCC_AXG_NCTF_45 AM16
VCC_AXG_NCTF_46 AL16
VCC_AXG_NCTF_47 AK16
VCC_AXG_NCTF_48 AJ16
VCC_AXG_NCTF_49 AH16
VCC_AXG_NCTF_50 AG16
VCC_AXG_NCTF_51 AF16
VCC_AXG_NCTF_52 AE16
VCC_AXG_NCTF_53 AC16
VCC_AXG_NCTF_54 AB16
VCC_AXG_NCTF_55 AA16
VCC_AXG_NCTF_56 Y16
VCC_AXG_NCTF_57 W16
VCC_AXG_NCTF_58 V16
VCC_AXG_NCTF_59 U16
VCC_AXG_NCTF_60

CANTIGA_PM

+1.05V

Ivcc_axg=6326.84mA

C629 *390U/2.5V_6X5.8ESR10@IV
C242 .47U/6.3V_4@MV
C241 1U/6.3V_4@MV
C279 10U/6.3V_8@MV
C227 *10U/6.3V_8@IV
C226 *10U/6.3V_8@IV
C268 .1U/10V_4@MV
C224 *.1U/10V_4@IV

B-TEST B-TEST

+1.05V

Ivcc=1930.4+508.12=2438.52mA

C546 *330u_2.5V_7343@NC
C162 10U/6.3V_8
C248 10U/6.3V_8
C243 .33U/6.3V_4
C267 .33U/6.3V_4
C249 .1U/10V_4

4140mA

1.5VSUS

C81 .1U/10V_4
C105 10U/6.3V_8
C106 10U/6.3V_8
C534 10U/6.3V_8
C528 10U/6.3V_8

U27F

VCC CORE POWER

AG34 VCC_1
AC34 VCC_2
AB34 VCC_3
AA34 VCC_4
Y34 VCC_5
V34 VCC_6
U34 VCC_7
AM33 VCC_8
AK33 VCC_9
AJ33 VCC_10
AG33 VCC_11
AF33 VCC_12
AE33 VCC_13
AC33 VCC_14
AA33 VCC_15
Y33 VCC_16
W33 VCC_17
V33 VCC_18
U33 VCC_19
AH28 VCC_20
AF28 VCC_21
AC28 VCC_22
AA28 VCC_23
AJ26 VCC_24
AG26 VCC_25
AE26 VCC_26
AC26 VCC_27
AH25 VCC_28
AG25 VCC_29
AF25 VCC_30
AG24 VCC_31
AJ23 VCC_32
AH23 VCC_33
AF23 VCC_34
T32 VCC_35

CANTIGA_PM

+1.05V

VCC NCTF

VCC_NCTF_1 AM32
VCC_NCTF_2 AL32
VCC_NCTF_3 AK32
VCC_NCTF_4 AJ32
VCC_NCTF_5 AH32
VCC_NCTF_6 AG32
VCC_NCTF_7 AE32
VCC_NCTF_8 AC32
VCC_NCTF_9 AA32
VCC_NCTF_10 Y32
VCC_NCTF_11 W32
VCC_NCTF_12 U32
VCC_NCTF_13 AM30
VCC_NCTF_14 AL30
VCC_NCTF_15 AK30
VCC_NCTF_16 AH30
VCC_NCTF_17 AG30
VCC_NCTF_18 AF30
VCC_NCTF_19 AE30
VCC_NCTF_20 AC30
VCC_NCTF_21 AB30
VCC_NCTF_22 AA30
VCC_NCTF_23 Y30
VCC_NCTF_24 W30
VCC_NCTF_25 V30
VCC_NCTF_26 U30
VCC_NCTF_27 AL29
VCC_NCTF_28 AK29
VCC_NCTF_29 AJ29
VCC_NCTF_30 AH29
VCC_NCTF_31 AG29
VCC_NCTF_32 AE29
VCC_NCTF_33 AC29
VCC_NCTF_34 AA29
VCC_NCTF_35 Y29
VCC_NCTF_36 W29
VCC_NCTF_37 V29
VCC_NCTF_38 AL28
VCC_NCTF_39 AK28
VCC_NCTF_40 AL26
VCC_NCTF_41 AK26
VCC_NCTF_42 AK25
VCC_NCTF_43 AK24
VCC_NCTF_44 AK23

VCC SM LF

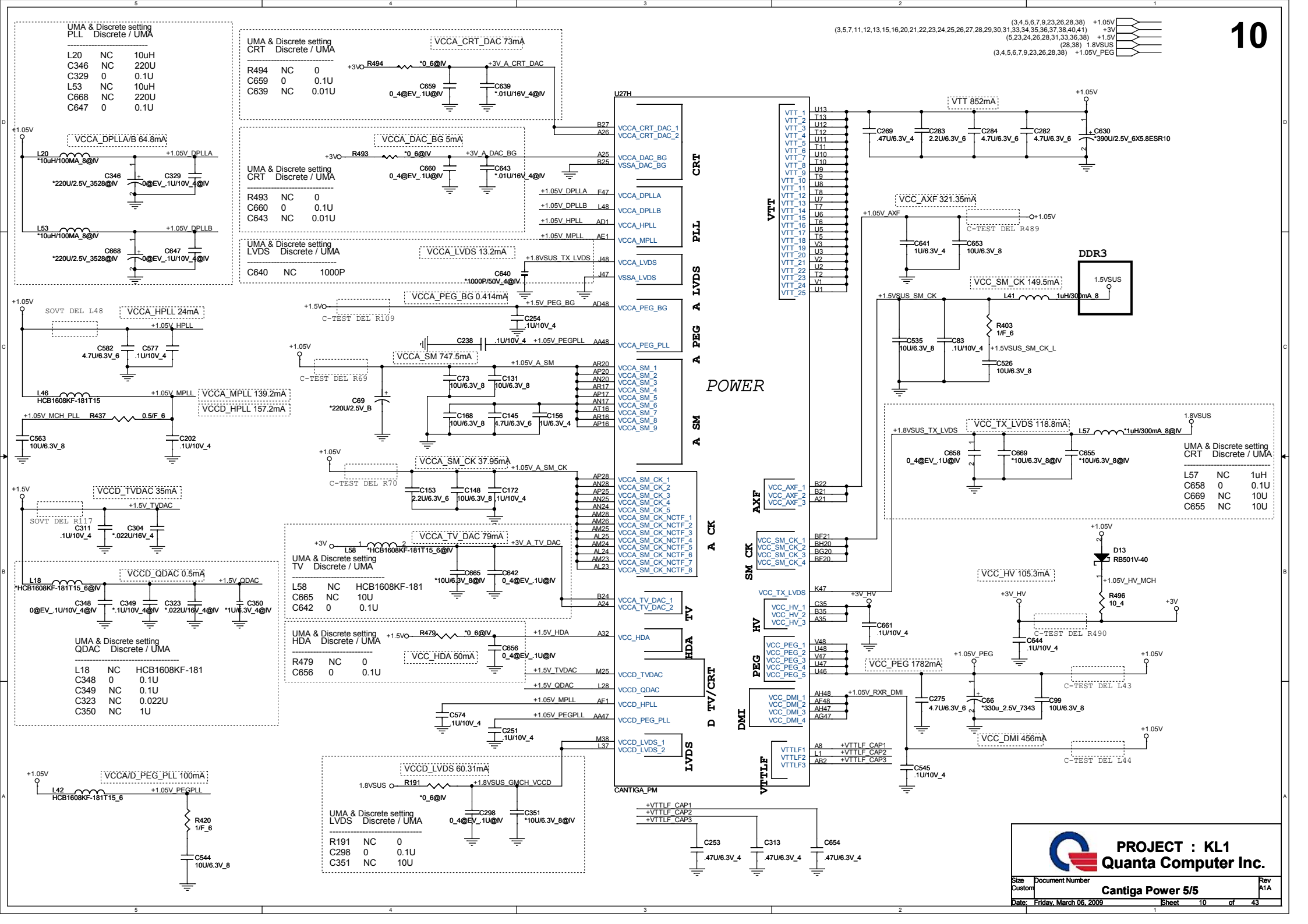
VCC_SM_LF1 AV44 +VCCSM_LF1
VCC_SM_LF2 BA37 +VCCSM_LF2
VCC_SM_LF3 AM40 +VCCSM_LF3
VCC_SM_LF4 AV21 +VCCSM_LF4
VCC_SM_LF5 AY5 +VCCSM_LF5
VCC_SM_LF6 AM10 +VCCSM_LF6
VCC_SM_LF7 BB13 +VCCSM_LF7

C110 .1U/10V_4
C175 .1U/10V_4
C120 .33U/6.3V_4
C117 .33U/6.3V_4
C173 .47U/6.3V_4
C111 1U/6.3V_4
C149 1U/6.3V_4

(7,10,11,12,38,39) 1.5VSUS
(3,4,5,6,7,10,23,26,28,38) +1.05V

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Vcc 4/5	A1A
Date: Friday, March 06, 2009	Sheet 9 of 43	


UMA & Discrete setting
PLL Discrete / UMA
L20 NC 10uH
C346 NC 220U
C329 0 0.1U
L53 NC 10uH
C668 NC 220U
C647 0 0.1U
UMA & Discrete setting
CRT Discrete / UMA
R494 NC 0
C659 0 0.1U
C639 NC 0.01U
UMA & Discrete setting
CRT Discrete / UMA
R493 NC 0
C660 0 0.1U
C643 NC 0.01U
UMA & Discrete setting
LVDS Discrete / UMA
C640 NC 1000P
UMA & Discrete setting
HDA Discrete / UMA
R479 NC 0
C656 0 0.1U
UMA & Discrete setting
TV Discrete / UMA
L58 NC HCB1608KF-181
C665 NC 10U
C642 0 0.1U
UMA & Discrete setting
QDAC Discrete / UMA
L18 NC HCB1608KF-181
C348 0 0.1U
C349 NC 0.1U
C323 NC 0.022U
C350 NC 1U
UMA & Discrete setting
LVDS Discrete / UMA
R191 NC 0
C298 0 0.1U
C351 NC 10U
UMA & Discrete setting
CRT Discrete / UMA
L57 NC 1uH
C658 0 0.1U
C669 NC 10U
C655 NC 10U
VCCA_CRT_DAC 73mA
VCCA_DAC_BG 5mA
VCCA_DPLLA/B 64.8mA
VCCA_LVDS 13.2mA
VCCA_PEG_BG 0.414mA
VCCA_HPLL 24mA
VCCA_SM 747.5mA
VCCA_MPLL 139.2mA
VCCD_HPLL 157.2mA
VCCA_SM_CK 37.95mA
VCCD_TVDAC 35mA
VCCA_TV_DAC 79mA
VCCD_QDAC 0.5mA
VCC_HDA 50mA
VCCD_LVDS 60.31mA
VCCA/D_PEG_PLL 100mA
VTT 852mA
VCC_AXF 321.35mA
VCC_SM_CK 149.5mA
VCC_TX_LVDS 118.8mA
VCC_HV 105.3mA
VCC_PEG 1782mA
VCC_DMI 456mA
DDR3
POWER
CANTIGA_PM
U27H
CRT
PLL
LVDS
PEG
SM
SM_CK
AXF
HV
TV
HDA
TV/CRT
DMI
VTTLF
VTT
(3,4,5,6,7,9,23,26,28,38) +1.05V
(3,5,7,11,12,13,15,16,20,21,22,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(5,23,24,26,28,31,33,36,38) +1.5V
(28,38) 1.8VSUS
(3,4,5,6,7,9,23,26,28,38) +1.05V_PEG
PROJECT : KL1
Quanta Computer Inc.
Size Custom
Document Number
Cantiga Power 5/5
Rev A1A
Date: Friday, March 06, 2009
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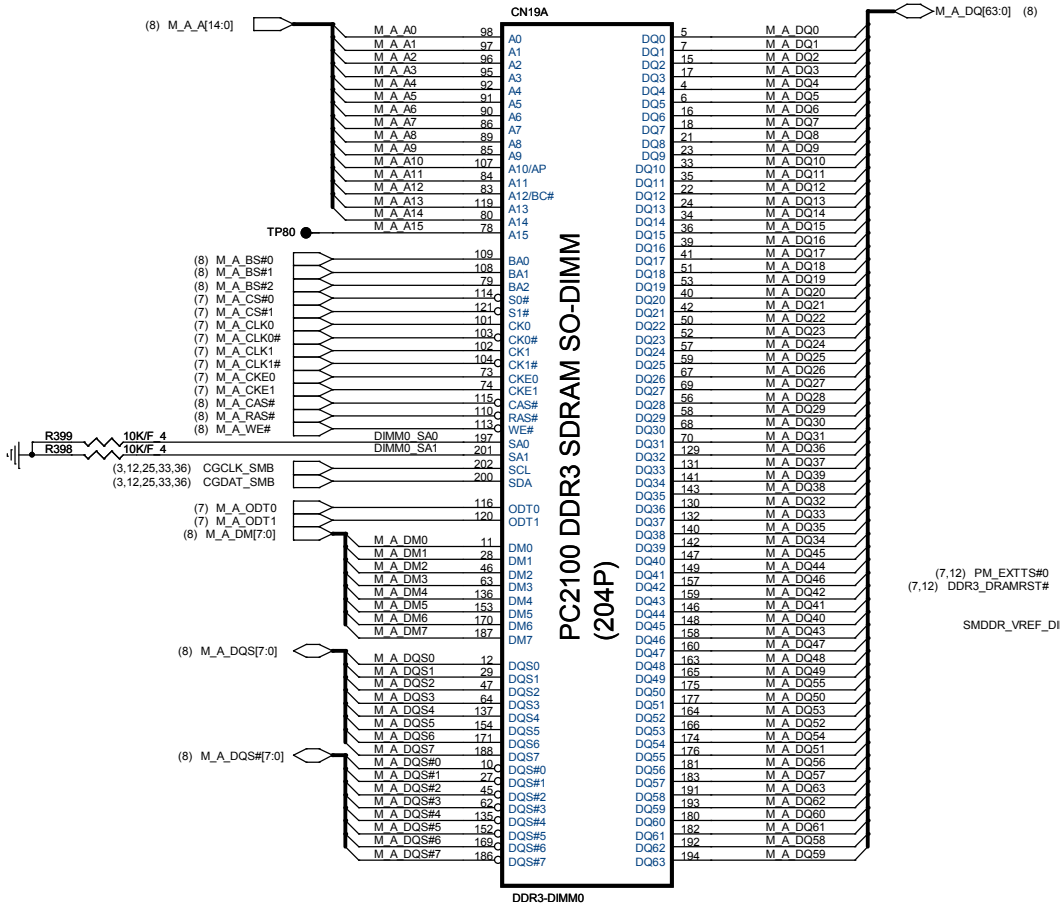
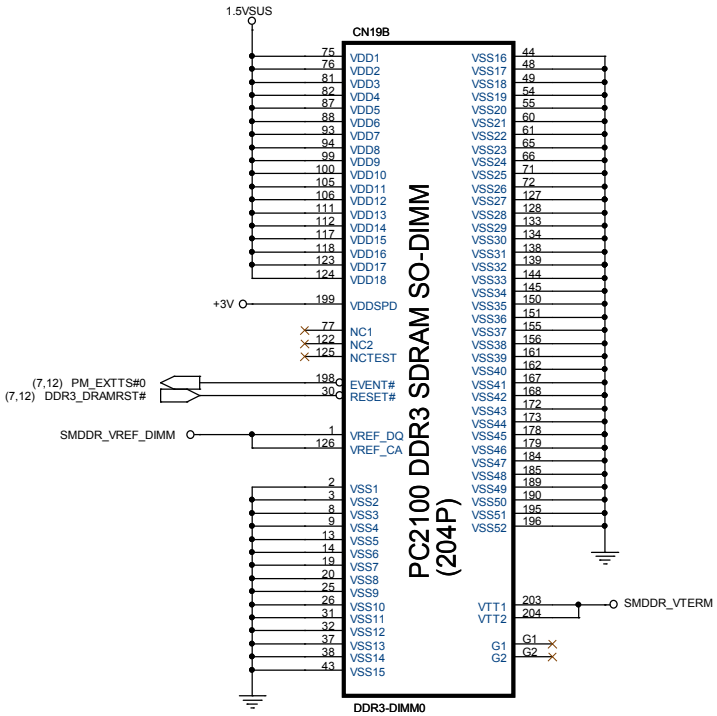
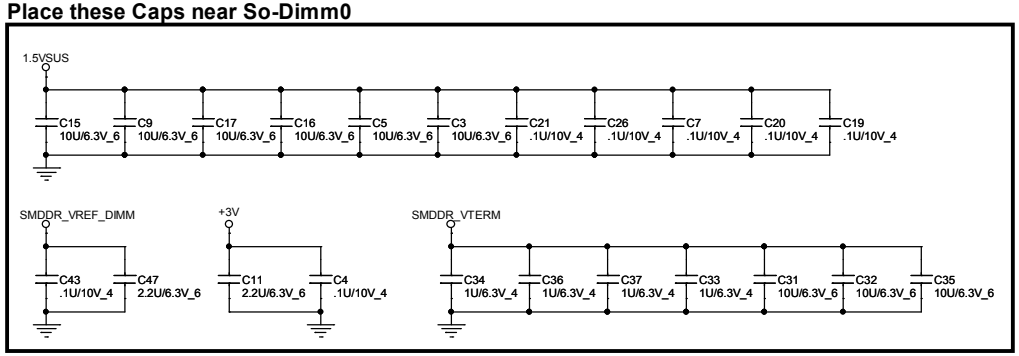
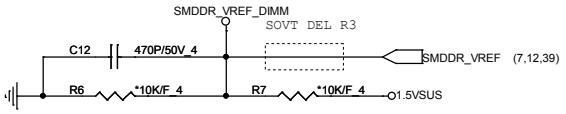




Place these Caps near So-Dimm0





PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0(H=5.2)	A1A

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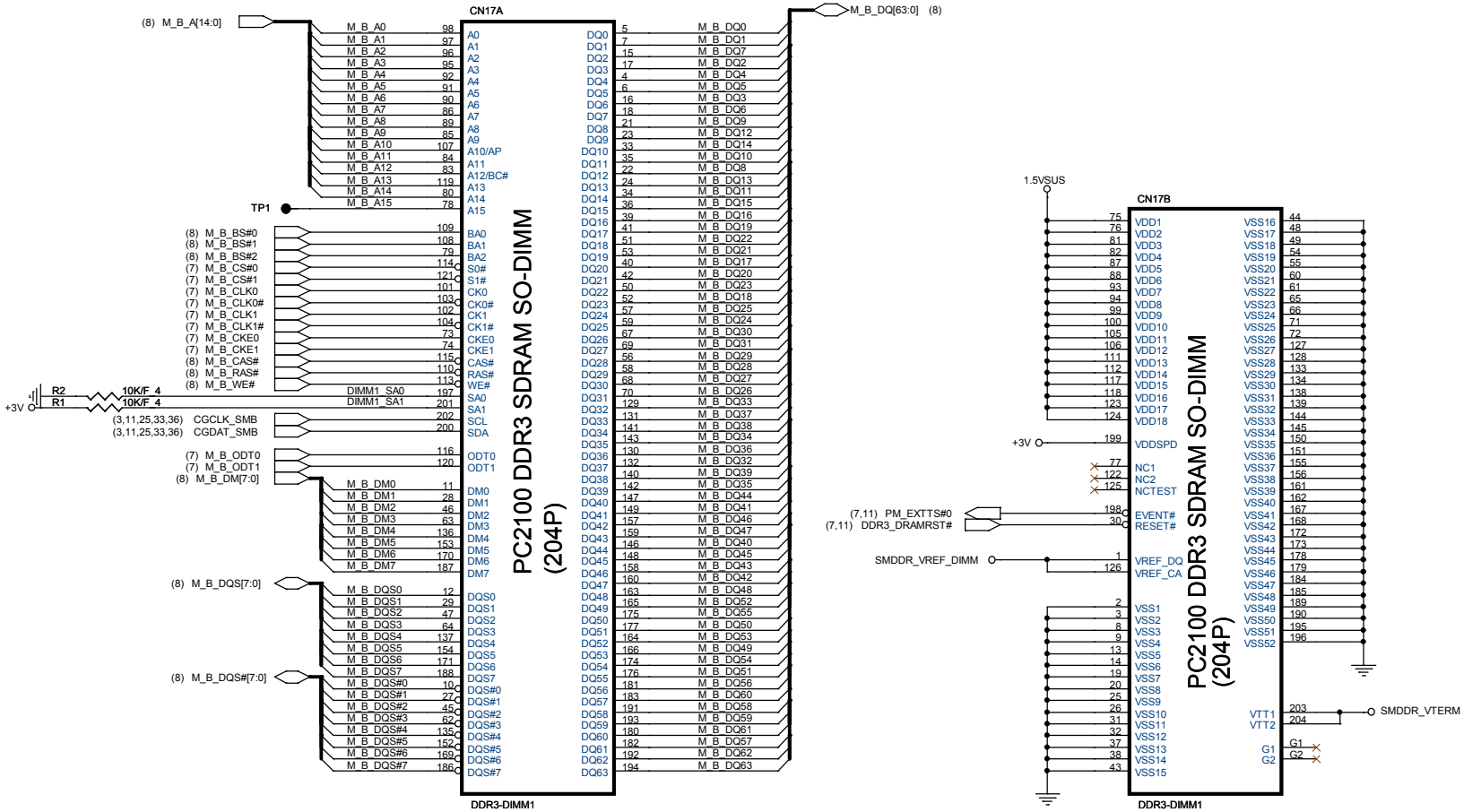
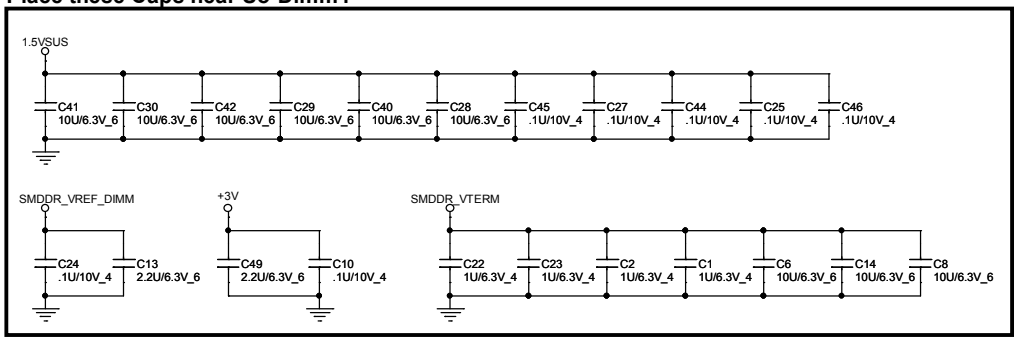


Place these Caps near So-Dimm1



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=9.2)	A1A

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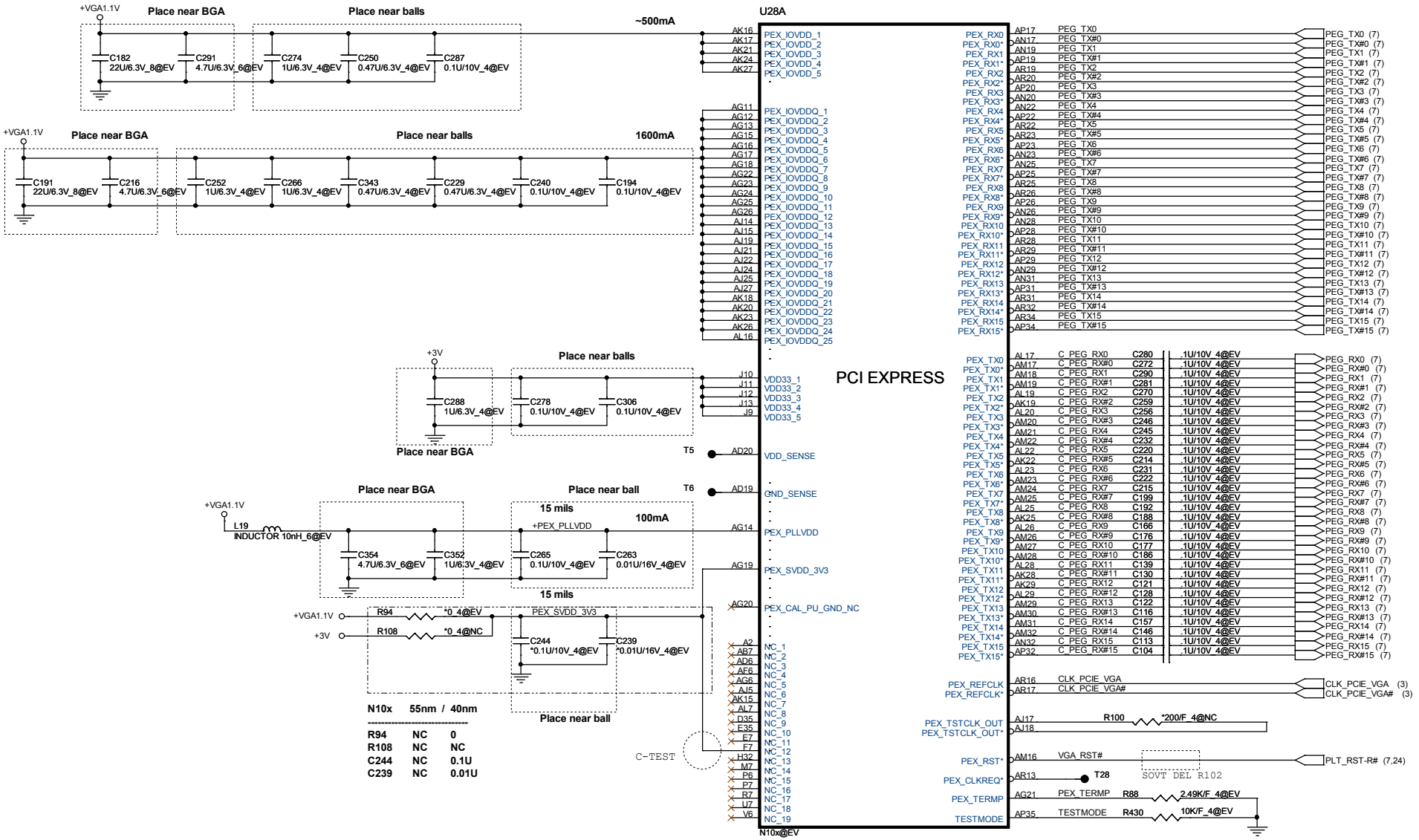
+VGA1.1V (14,15,38)
+3V (3,5,7,10,11,12,15,16,20,21,22,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41)



N10x	55nm / 40nm
R94	NC 0
R108	NC NC
C244	NC 0.1U
C239	NC 0.01U

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X (PCIE I/F) 1/5	A1A
Date: Friday, March 06, 2009	Sheet 13 of 43	

U28B

MEMORY I/F A

U28C

MEMORY I/F B

(18) FBA_CMD[29..0]
(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]

(19) FBC_CMD[29..0]
(19) VMC_DQ[63..0]
(19) VMC_DM[7..0]
(19) VMC_WDQS[7..0]
(19) VMC_RDQS[7..0]

+1.8V (15,18,19,28,37,38)
+VGA1.1V (13,15,38)

FBA_CMD7 FBA_CMD15 FBA_CMD18

R50 *10K_4@EV
R55 10K_4@EV
R54 10K_4@EV

N10x	55nm / 40nm	
R50	NC	10K
R55	10K	10K
R54	10K	10K

FBC_CMD7 FBC_CMD15 FBC_CMD18

R63 *10K_4@EV
R80 10K_4@EV
R77 10K_4@EV

N10x	55nm / 40nm	
R63	NC	10K
R80	10K	10K
R77	10K	10K

Using internal Vref, ext divider no stuff

+1.8V
R188 *549/F_4@NC
R181 *931/F_4@NC
R164 *1.33K/F_4@NC
C330 *0.01U/16V_4@NC
Q5 *2N7002E@NC
FB_VREF J27 +FB_VREF1
GDDR3_VREF_SW (16,18,19)

15 mils

For Debug only

FBA_DEBUG T30 R66 60.4/F_4@EV +1.8V

FB_DLLAVDD0 AG27 +FB_PLLAVDD
FB_PLLAVDD0 AF27
C247 0.01U/16V_4@EV
C225 0.1U/10V_4@EV
C147 1U/6.3V_4@EV
C165 4.7U/6.3V_6@EV
L11 HCB1608KF-181T15_6@EV +VGA1.1V

Place near balls
Place near BGA

N10x-55nm for GDDR3

FB_CAL_PD_VDDQ K27 R65 48.7/F_4@EV +1.8V
FB_CAL_PU_GND L27 R76 33.2/F_4@EV
FB_CAL_TERM_GND M27 R75 40.2/F_4@EV
FBC_DEBUG G19 R90 60.4/F_4@EV +1.8V

FB_DLLAVDD1_NC J19 +FB_PLLAVDD
FB_PLLAVDD1_NC J18
C237 .1U/10V_4@EV
C181 .1U/10V_4@EV

N10x	55nm / 40nm	
C237	0.1U	NC
C181	0.1U	NC

+1.8V
C160 4.7U/6.3V_6@EV
C178 1U/6.3V_4@EV
C171 1U/6.3V_4@EV
C309 1U/6.3V_4@EV
C159 1U/6.3V_4@EV
C261 0.1U/10V_4@EV
C297 0.1U/10V_4@EV
C271 0.1U/10V_4@EV
C164 0.1U/10V_4@EV
C195 0.1U/10V_4@EV
C174 0.1U/10V_4@EV

Place near BGA
Place near balls

	N10M-55nm N10P-55nm	N10M-40nm N10P-40nm
Signal Name	GDDR3	GDDR3
FBCAL_PD_VDDQ	48.7 ohm	
FBCAL_PU_GND	33.2 ohm	
FBCAL_TERM_GND	40.2 ohm	

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X (MEMORY I/F) 2/5	A1A

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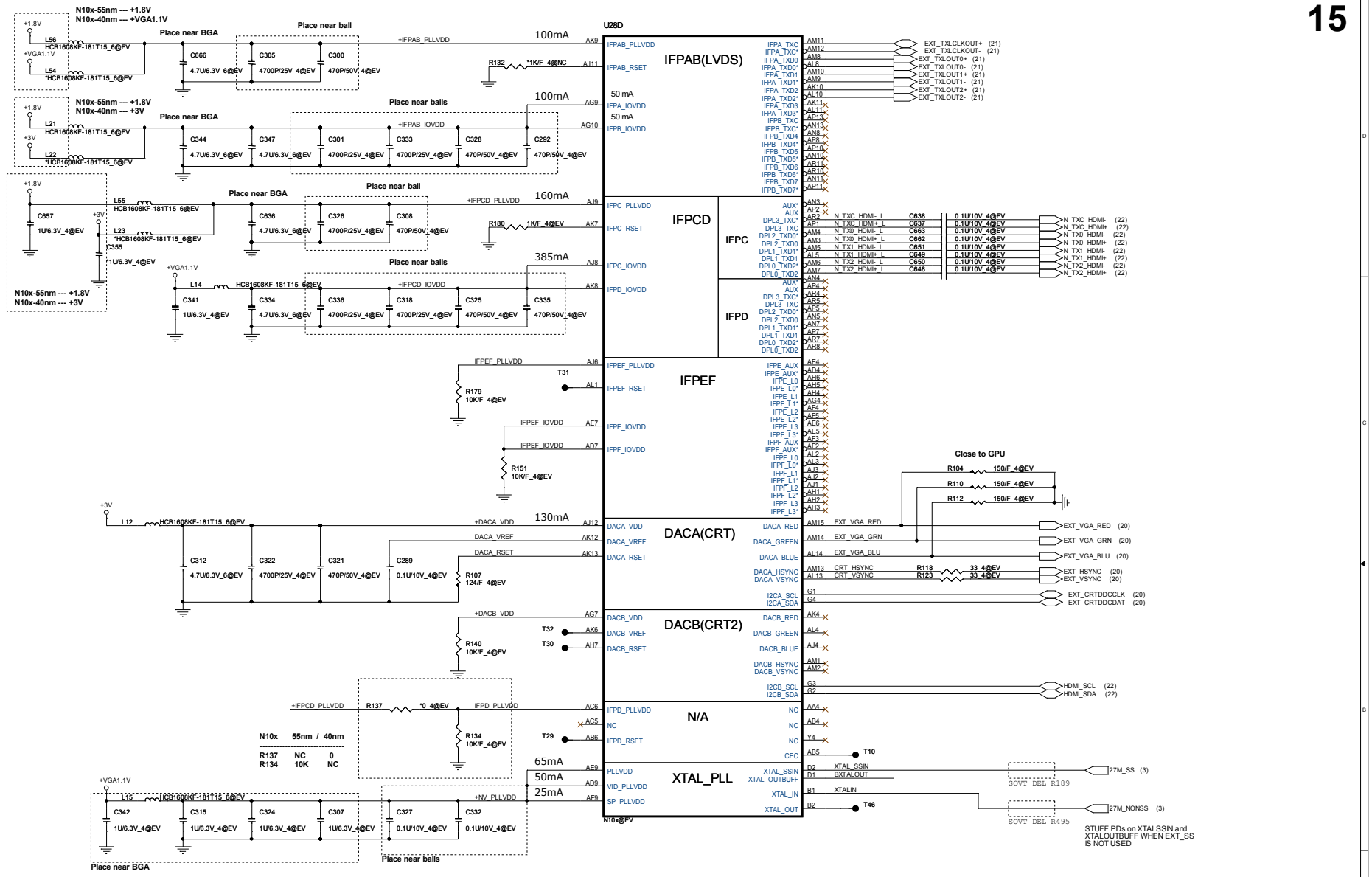
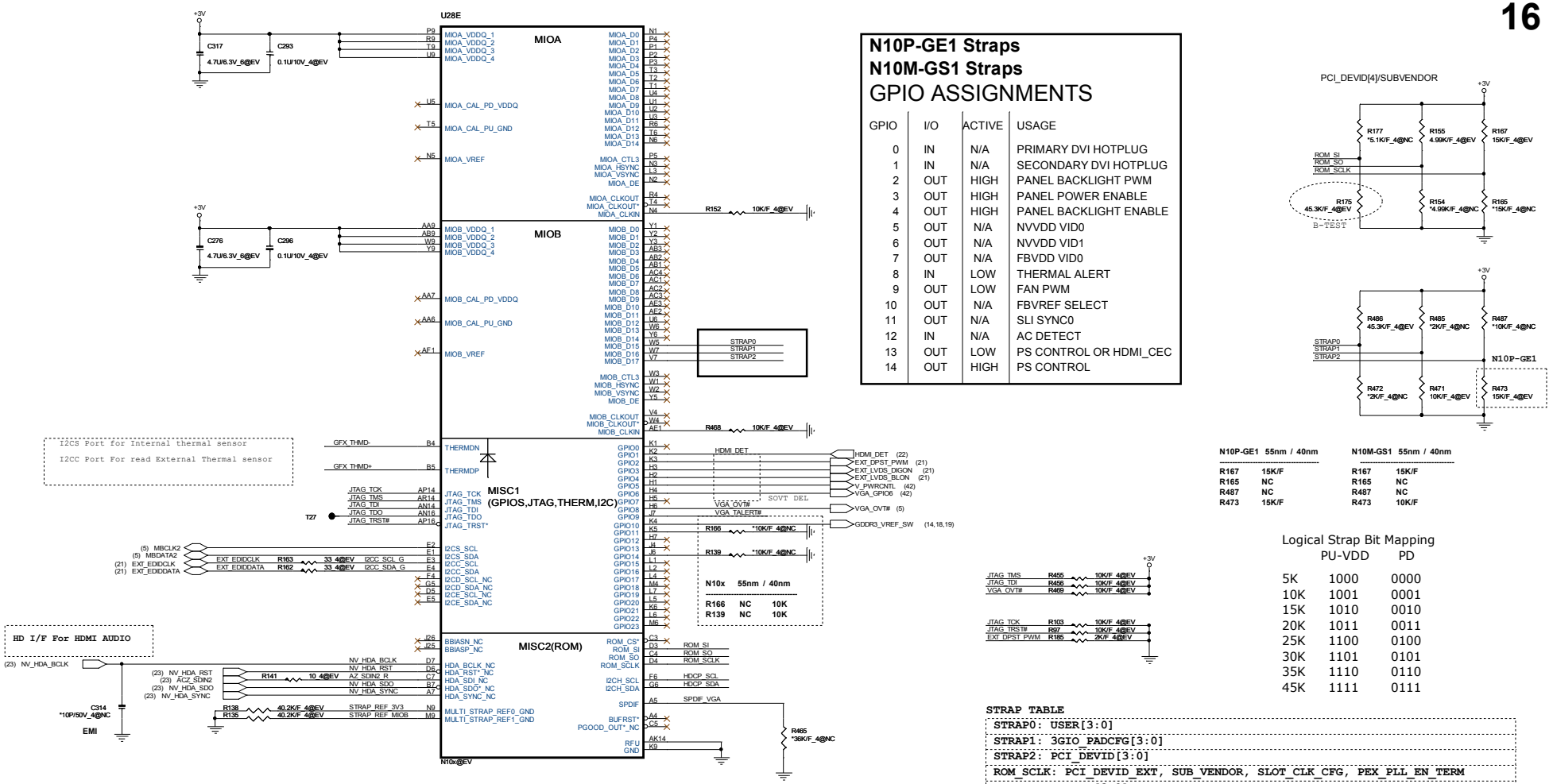


PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X (DISPLAY) 3/5	A1A
Date: Friday, March 06, 2009	Sheet 15 of 43	



N10P-GE1 Straps
N10M-GS1 Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

N10P-GE1 55nm / 40nm		N10M-GS1 55nm / 40nm	
R167	15K/F	R167	15K/F
R165	NC	R165	NC
R487	NC	R487	NC
R473	15K/F	R473	10K/F

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP TABLE

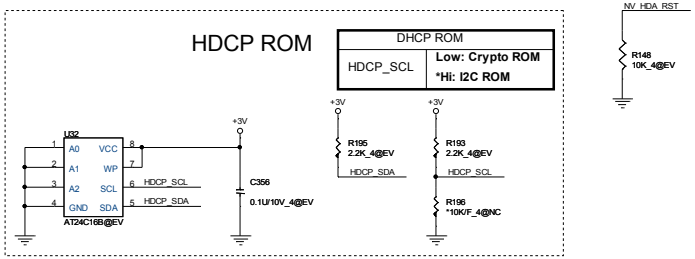
STRAP0: USER[3:0]
STRAP1: 3GIO_PADCFG[3:0]
STRAP2: PCI_DEVID[3:0]
ROM_SCLK: PCI_DEVID_EXT, SUB_VENDOR, SLOT_CLK_CFG, PEX_PLL_EN_TERM
ROM_SI: RAMCFG[3:0]
ROM_SO: XCLK_417, FB_0_BAR_SIZE, SMB_ALT_ADDR, VGA_DEVICE

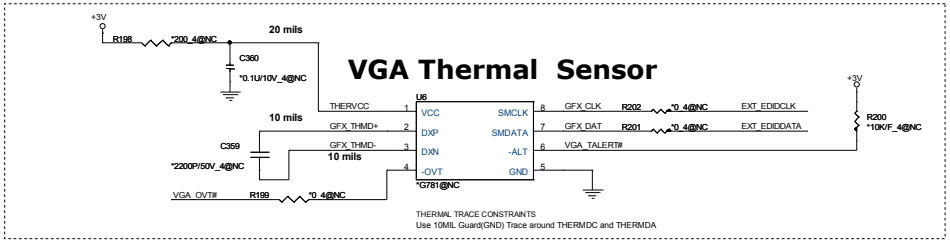
KL1 STRAP FUNCTION MAPPING

USER[3:0]: 1111
3GIO_PADCFG[3:0]: 0001 NoteBook
PCI_DEVID[3:0]: 0001
SUB_VENDOR: 0 No Vedio BIOS ROM
SLOT_CLK_CLG: 1 GPU AND MCH USE COMMON REF CLOCK
PEX_PLL_EN_TERM: 0 DISABLE PEX_PLL TERMINATION
RAMCFG[3:0]: 0000 AND 0001
XCLK_417: 1 USING 27MHZ
FB_0_BAR_SIZE:
SMB_ALT_ADDR:
VGA_DEVICE:

ROM_SI	RAMCFG LSIT:	
PD R175:45K/F	0111	SAMSUNG K4J10324QD-HC12 32M32b * 4PCS
PD R175:30K/F	0101	QIMONDA HYB18H1G321AF-11 32M32b * 2PCS

B-TEST





+3V (3,5,7,10,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41)

PROJECT : KL1
Quanta Computer Inc.

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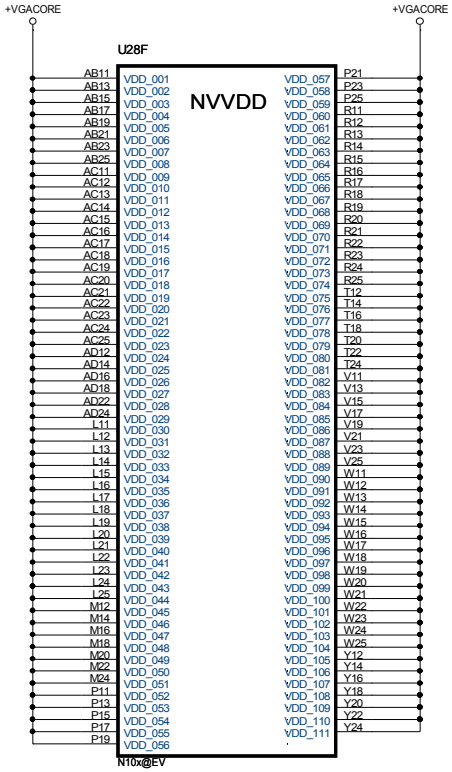
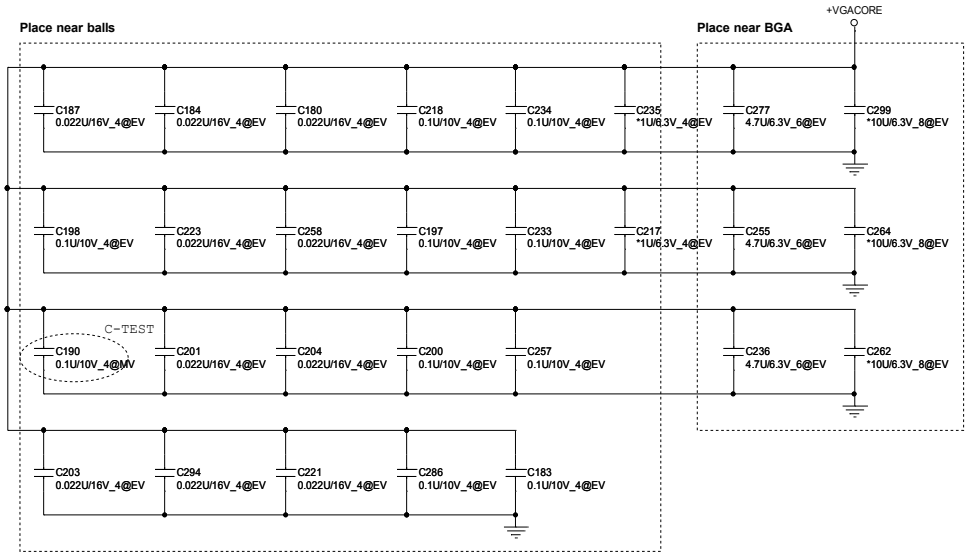
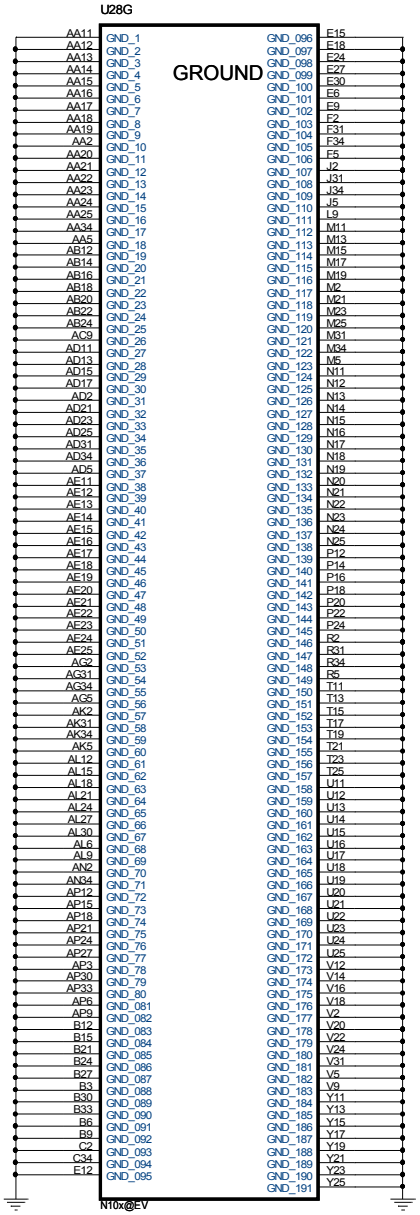
NVVDD Decoupling

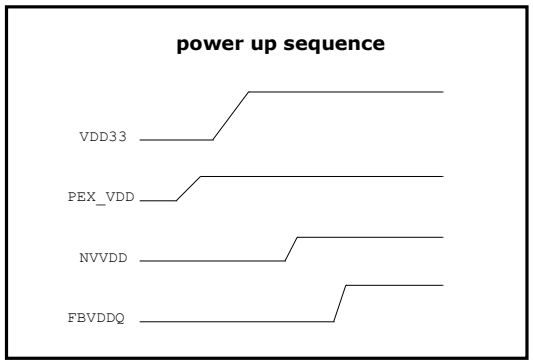




N10x	55nm	40nm
C187	0.022U	0.01U
C198	0.1U	0.01U
C190	0.1U	0.01U
C235	NC	1U
C217	NC	1U
C277	4.7U	1U
C255	4.7U	4.7U
C236	4.7U	NC
C299	NC	10U
C264	NC	10U
C262	NC	10U



N10P-GE1: +VGACORE +0.90V (Normal)



+VGACORE (37,38,42)

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X (POWER & GND) 5/5	A1A
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(14) FBA_CMD[29..0]
(14) VMA_DQ[63..0]
(14) VMA_DM[7..0]
(14) VMA_WDQS[7..0]
(14) VMA_RDQS[7..0]

N10x	55nm		40nm	
DQ	0..31	32..63	0..31	32..63
CMD0	A4		A4	
CMD1	RAS*	RAS*	RAS*	RAS*
CMD2	A5		A5	
CMD3	BA1	BA1	BA1	BA1
CMD4		A2		A2
CMD5		A4		A4
CMD6		A3		A3
CMD7	CS1*	CS1*		CKE
CMD8	CS0*	CS0*		CS0*
CMD9	A11	A11	A11	A11
CMD10	CAS*	CAS*	CAS*	CAS*
CMD11	WE*	WE*	WE*	WE*
CMD12	BA0	BA0	BA0	BA0
CMD13		A5		A5
CMD14	A12	A12	A12	A12
CMD15	RST/ODT	RST/ODT	RST/ODT	RST/ODT
CMD16	A7	A7	A7	A7
CMD17	A10	A10	A10	A10
CMD18	CKE	CKE	CKE	
CMD19	A0	A0	A0	A0
CMD20	A9	A9	A9	A9
CMD21	A6	A6	A6	A6
CMD22	A2		A2	
CMD23	A8	A8	A8	A8
CMD24	A3		A3	
CMD25	A1	A1	A1	A1
CMD26	A13	A13	A13	A13
CMD27	BA2	BA2	BA2	BA2
CMD28				ODT/CS1*
CMD29			CS0*	
CMD30			ODT/CS1*	

Group 3: D24~D31
Group 0: D0~D7
Group 2: D16~D23
Group 1: D8~D15

U2

VMA_DQ31 T3 … VMA_DQ8 G3, VMA_DQ9 F2, VMA_DQ10 F3, VMA_DQ11 E2, VMA_DQ14 C3, VMA_DQ13 C2, VMA_DQ15 B3, VMA_DQ12 B2

FBA_CMD27 H10, FBA_CMD3 G9, FBA_CMD12 G4, FBA_CMD9 L4, FBA_CMD17 K2, FBA_CMD20 M9, FBA_CMD23 K11, FBA_CMD16 L9, FBA_CMD21 K10, FBA_CMD2 H11, FBA_CMD0 K9, FBA_CMD24 M4, FBA_CMD22 K3, FBA_CMD25 H2, FBA_CMD19 K4, FBA_CS0* F9, FBA_CMD11 H9, FBA_CMD1 H3, FBA_CMD10 F4, FBA_CMD18 H4

(14) VMA_CLK0# J10, (14) VMA_CLK0 J11

VMA_RDQS3 P3, VMA_RDQS0 P10, VMA_RDQS2 D10, VMA_RDQS1 D3, VMA_WDQS3 P2, VMA_WDQS0 P11, VMA_WDQS2 D11, VMA_WDQS1 D2, VMA_DM3 N3, VMA_DM0 N10, VMA_DM2 E10, VMA_DM1 E3, FBA_CMD15 V9

R23 243/F_4@EV FBA_ZQ1 A4

FBA_VREF0 H1, FBA_VREF1 H12

DQ31 | DQ23 … DQ0 | DQ8 (VDDQ A1, A12, C1, C4, C9, C12, E1, E4, E9, E12, J4, J9, N1, N4, N9, N12, R1, R4, R9, R12, V1, V12; VDD A2, A11, F1, F12, M1, M12, V2, V11; VSSQ B1, B4, B9, B12, D1, D4, D9, D12, G2, G11, L2, L11, P1, P4, P9, P12, T1, T4, T9, T12, A3, A10, G1, G12, L1, L12, V3, V10)

BA2 | RAS, BA1 | BA0, BA0 | BA1
A11 | A7, A10 | A8, A9 | A3, A8/AP | A10, A7 | A11, A6 | A2, A5 | A1, A4 | A0, A3 | A9, A2 | A6, A1 | A5, A0 | A4
CS | CAS, WE | CKE, RAS | BA2, CAS | CS, CKE | WE

VSSQ#B4, VSSQ#B9, VSSQ#B12, VSSQ#D1, VSSQ#D4, VSSQ#D9, VSSQ#D12, VSSQ#G2, VSSQ#G11, VSSQ#L2, VSSQ#L11, VSSQ#P1, VSSQ#P4, VSSQ#P9, VSSQ#P12, VSSQ#T1, VSSQ#T4, VSSQ#T9, VSSQ#T12, VSS, VSS#A10, VSS#G1, VSS#G12, VSS#L1, VSS#L12, VSS#V3, VSS#V10

CK, CK → VDDA, VDDA#K12 (K1, K12)

RDQS3 | RDQS2, RDQS2 | RDQS3, RDQS1 | RDQS0, RDQS0 | RDQS1

WDQS3 | WDQS2, WDQS2 | WDQS3 VSSA#J12, WDQS1 | WDQS0 VSSA, WDQS0 | WDQS1

DM3 | DM2 → RFU2 J3 FBA_CMD14
DM2 | DM3
DM1 | DM0 → RFU1 J2 T3
DM0 | DM1
RFU0 V4

RESET
ZQ
VREF
VREF#H12
MF A9
GND | VDD

VRAM@EV

C520 0.1U/10V_4@EV

QIMONDA: HYB18H1G321AF-11
SAMSUNG: K4J10324QD-HC12

FBA_CMD18 R409 0_4@EV
FBA_CMD7 R412 *0_4@EV
→ FBA_CKE

FBA_CMD8 R414 0_4@EV
FBA_CMD29 R416 *0_4@EV
→ FBA_CS0*

N10x	55nm / 40nm
R409	0 NC
R412	NC 0
R414	0 NC
R416	NC 0

Group 7: D56~D63
Group 5: D40~D47
Group 6: D48~D55
Group 4: D32~D39

U24

VMA_DQ59 T3 … VMA_DQ33 B2

FBA_CMD1 H10, FBA_CMD12 G9, FBA_CMD3 G4, FBA_CMD16 L4, FBA_CMD23 K2, FBA_CMD6 M9, FBA_CMD17 K11, FBA_CMD9 L9, FBA_CMD4 K10, FBA_CMD25 H11, FBA_CMD19 K9, FBA_CMD20 M4, FBA_CMD21 K3, FBA_CMD13 H2, FBA_CMD5 K4, FBA_CMD10 F9, FBA_CKE H9, FBA_CMD27 H3, FBA_CMD8 F4, FBA_CMD11 H4

(14) VMA_CLK1# J10, (14) VMA_CLK1 J11

VMA_RDQS7 P3, VMA_RDQS5 P10, VMA_RDQS6 D10, VMA_RDQS4 D3, VMA_WDQS7 P2, VMA_WDQS5 P11, VMA_WDQS6 D11, VMA_WDQS4 D2, VMA_DM7 N3, VMA_DM5 N10, VMA_DM6 E10, VMA_DM4 E3, FBA_CMD15 V9

R404 243/F_4@EV FBA_ZQ2 A4

FBA_VREF0 H1, FBA_VREF1 H12

DQ31 | DQ23 … DQ0 | DQ8 (VDDQ A1, A12, C1, C4, C9, C12, E1, E4, E9, E12, J4, J9, N1, N4, N9, N12, R1, R4, R9, R12, V1, V12; VDD A2, A11, F1, F12, M1, M12, V2, V11; VSSQ B1, B4, B9, B12, D1, D4, D9, D12, G2, G11, L2, L11, P1, P4, P9, P12, T1, T4, T9, T12, A3, A10, G1, G12, L1, L12, V3, V10)

BA2 | RAS, BA1 | BA0, BA0 | BA1
A11 | A7, A10 | A8, A9 | A3, A8/AP | A10, A7 | A11, A6 | A2, A5 | A1, A4 | A0, A3 | A9, A2 | A6, A1 | A5, A0 | A4
CS | CAS, WE | CKE, RAS | BA2, CAS | CS, CKE | WE

VSSQ#B4, VSSQ#B9, VSSQ#B12, VSSQ#D1, VSSQ#D4, VSSQ#D9, VSSQ#D12, VSSQ#G2, VSSQ#G11, VSSQ#L2, VSSQ#L11, VSSQ#P1, VSSQ#P4, VSSQ#P9, VSSQ#P12, VSSQ#T1, VSSQ#T4, VSSQ#T9, VSSQ#T12, VSS, VSS#A10, VSS#G1, VSS#G12, VSS#L1, VSS#L12, VSS#V3, VSS#V10

CK, CK → VDDA, VDDA#K12 (K1, K12)

RDQS3 | RDQS2, RDQS2 | RDQS3, RDQS1 | RDQS0, RDQS0 | RDQS1

WDQS3 | WDQS2, WDQS2 | WDQS3 VSSA#J12, WDQS1 | WDQS0 VSSA, WDQS0 | WDQS1

DM3 | DM2 → RFU2 J3 FBA_CMD14
DM2 | DM3
DM1 | DM0 → RFU1 J2 T24
DM0 | DM1
RFU0 V4

RESET
ZQ
VREF
VREF#H12
MF A9
GND | VDD

VRAM@EV

C302 0.1U/10V_4@EV

QIMONDA: HYB18H1G321AF-11
SAMSUNG: K4J10324QD-HC12

(14,16,19) GDDR3_VREF_SW

FBA_VREF0 R425 931/F_4@EV → Q14 2N7002E@EV → R428 10K/F_4@EV
FBA_VREF1 R9 931/F_4@EV → Q1 2N7002E@EV → R428 10K/F_4@EV

Place near U2 VDDQ

C541 10U/6.3V_6@EV
C529 10U/6.3V_6@EV
C539 10U/6.3V_6@EV
C79 1U/6.3V_4@EV
C521 1U/6.3V_4@EV
C519 0.1U/10V_4@EV
C542 0.1U/10V_4@EV
C179 0.1U/10V_4@EV
C50 0.1U/10V_4@EV
C55 0.1U/10V_4@EV
C518 0.1U/10V_4@EV
C125 0.1U/10V_4@EV
C540 0.01U/16V_4@EV
C533 0.01U/16V_4@EV

Place near U24 VDDQ

C78 10U/6.3V_6@EV
C65 10U/6.3V_6@EV
C71 10U/6.3V_6@EV
C76 1U/6.3V_4@EV
C85 1U/6.3V_4@EV
C331 0.1U/10V_4@EV
C295 0.1U/10V_4@EV
C56 0.1U/10V_4@EV
C48 0.1U/10V_4@EV
C114 0.1U/10V_4@EV
C54 0.1U/10V_4@EV
C53 0.1U/10V_4@EV
C68 0.01U/16V_4@EV
C98 0.01U/16V_4@EV

Place near VRAM side

R421 475/F_4@EV VMA_CLK0# / VMA_CLK0
R12 475/F_4@EV VMA_CLK1# / VMA_CLK1

16 ~ 20 mils
R10 1.33K/F_4@EV FBA_VREF0 R11 549/F_4@EV +1.8V
C52 0.01U/16V_4@EV

16 ~ 20 mils
R424 1.33K/F_4@EV FBA_VREF1 R427 549/F_4@EV +1.8V
C543 0.01U/16V_4@EV

+1.8V (14,15,19,28,37,38)

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X GDDR3 SDRAM-1 (BGA136)	A1A
Date: Friday, March 06, 2009	Sheet 18 of 43	

(14) FBC_CMD[29..0]
(14) VMC_DQ[63..0]
(14) VMC_DM[7..0]
(14) VMC_WDQS[7..0]
(14) VMC_RDQS[7..0]

Group 2: D16~D23
Group 3: D24~D31
Group 0: D0~D7
Group 1: D8~D15
Group 6: D48~D55
Group 5: D40~D47
Group 4: D32~D39
Group 7: D56~D63

N10x	55nm		40nm	
DQ	0..31	32..63	0..31	32..63
CMD0	A4		A4	
CMD1	RAS*	RAS*	RAS*	RAS*
CMD2	A5		A5	
CMD3	BA1	BA1	BA1	BA1
CMD4		A2		A2
CMD5		A4		A4
CMD6		A3		A3
CMD7	CS1*	CS1*		CKE
CMD8	CS0*	CS0*		CS0*
CMD9	A11	A11	A11	A11
CMD10	CAS*	CAS*	CAS*	CAS*
CMD11	WE*	WE*	WE*	WE*
CMD12	BA0	BA0	BA0	BA0
CMD13		A5		A5
CMD14	A12	A12	A12	A12
CMD15	RST/ODT	RST/ODT	RST/ODT	RST/ODT
CMD16	A7	A7	A7	A7
CMD17	A10	A10	A10	A10
CMD18	CKE	CKE	CKE	
CMD19	A0	A0	A0	A0
CMD20	A9	A9	A9	A9
CMD21	A6	A6	A6	A6
CMD22	A2		A2	
CMD23	A8	A8	A8	A8
CMD24	A3		A3	
CMD25	A1	A1	A1	A1
CMD26	A13	A13	A13	A13
CMD27	BA2	BA2	BA2	BA2
CMD28				ODT/CS1*
CMD29			CS0*	
CMD30			ODT/CS1*	

U5 — VRAM@EV

QIMONDA: HYB18H1G321AF-11
SAMSUNG: K4J10324QD-HC12

U29 — VRAM@EV

QIMONDA: HYB18H1G321AF-11
SAMSUNG: K4J10324QD-HC12

(14,16,18) GDDR3_VREF_SW
FBC_VREF0 R58 931/F_4@EV
Q3 2N7002E@EV
R49 10K/F_4@EV
FBC_VREF1 R432 931/F_4@EV
Q15 2N7002E@EV

Place near U5 VDDQ
C75 10U/6.3V_6@EV
C137 10U/6.3V_6@EV
C138 10U/6.3V_6@EV
C51 1U/6.3V_4@EV
C319 1U/6.3V_4@EV
C353 0.1U/10V_4@EV
C310 0.1U/10V_4@EV
C140 0.1U/10V_4@EV
C594 0.1U/10V_4@EV
C142 0.1U/10V_4@EV
C170 0.1U/10V_4@EV
C189 0.1U/10V_4@EV
C133 0.01U/16V_4@EV
C143 0.01U/16V_4@EV

Place near U29 VDDQ
C551 10U/6.3V_6@EV
C150 10U/6.3V_6@EV
C107 10U/6.3V_6@EV
C345 1U/6.3V_4@EV
C530 1U/6.3V_4@EV
C608 0.1U/10V_4@EV
C555 0.1U/10V_4@EV
C553 0.1U/10V_4@EV
C536 0.1U/10V_4@EV
C610 0.1U/10V_4@EV
C606 0.1U/10V_4@EV
C628 0.1U/10V_4@EV
C602 0.01U/16V_4@EV
C554 0.01U/16V_4@EV

C285 0.1U/10V_4@EV
C316 0.1U/10V_4@EV

(14) VMC_CLK0#
(14) VMC_CLK0
(14) VMC_CLK1#
(14) VMC_CLK1

FBC_CMD18 R71 0_4@EV
FBC_CMD7 R64 *0_4@EV
FBC_CKE
FBC_CMD8 R85 0_4@EV
FBC_CMD29 R89 *0_4@EV
FBC_CS0*

N10x	55nm / 40nm
R71	0
R64	NC
R85	0
R89	NC

R169 243/F_4@EV FBC_ZQ1
R464 243/F_4@EV FBC_ZQ2

T7
T26
FBC_CMD14

Place near VRAM side
R448 475/F_4@EV VMC_CLK0#
VMC_CLK0
R86 475/F_4@EV VMC_CLK1#
VMC_CLK1

16 ~ 20 mils
R105 1.33K/F_4@EV FBC_VREF0 R101 549/F_4@EV +1.8V
C273 0.01U/16V_4@EV

16 ~ 20 mils
R441 1.33K/F_4@EV FBC_VREF1 R438 549/F_4@EV +1.8V
C587 0.01U/16V_4@EV

+1.8V (14,15,18,28,37,38)

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X GDDR3 SDRAM-2 (BGA136)	A1A
Date: Friday, March 06, 2009	Sheet 19 of 43	

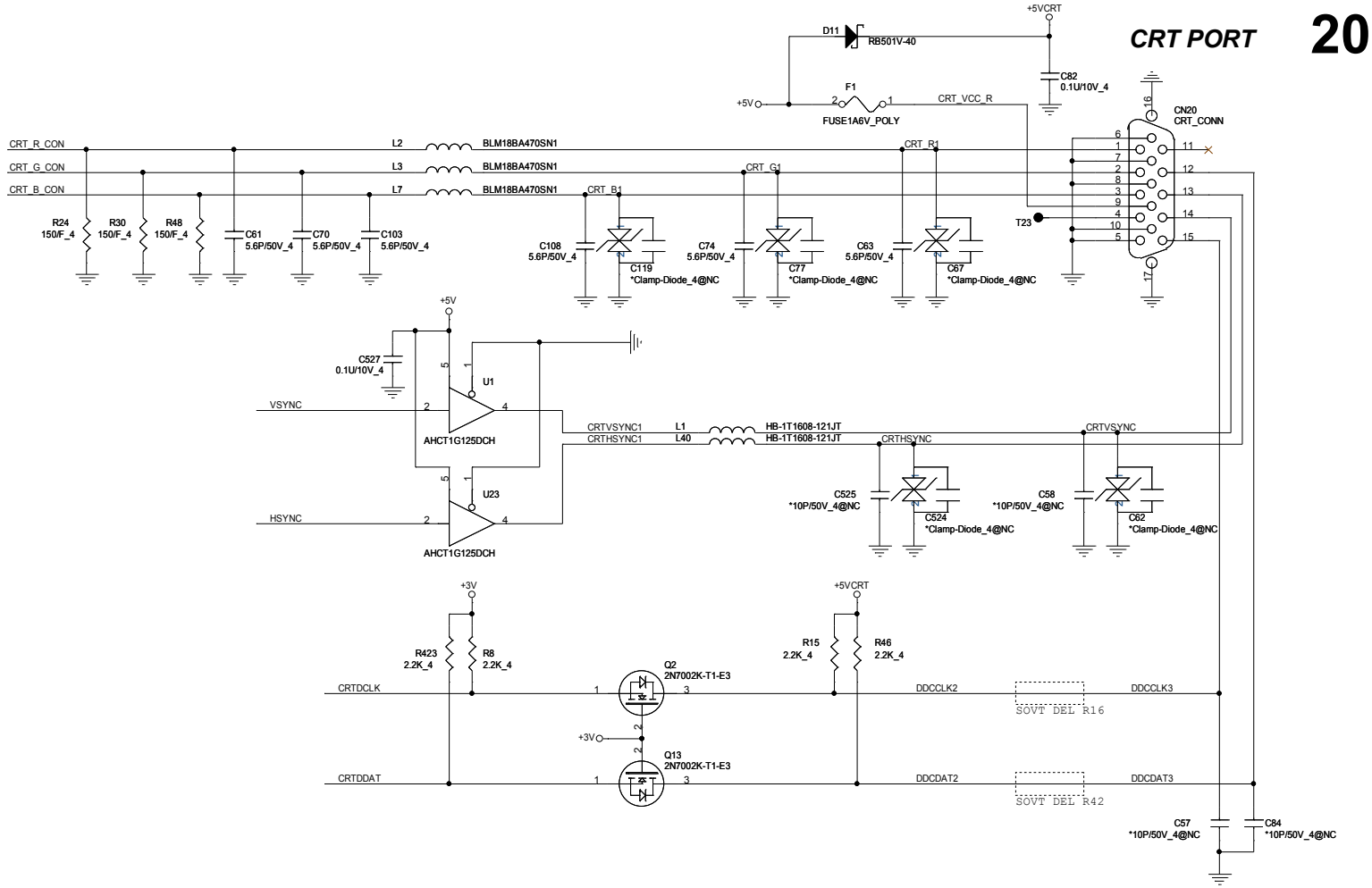
CRT PORT 20

CRT SWITCH

(15)	EXT_VGA_RED	R27	0_4@EV	CRT_R_CON
(15)	EXT_VGA_GRN	R33	0_4@EV	CRT_G_CON
(15)	EXT_VGA_BLU	R51	0_4@EV	CRT_B_CON
(15)	EXT_HSYNC	R400	0_4@EV	HSYNC
(15)	EXT_VSYNC	R18	0_4@EV	VSYNC
(15)	EXT_CRTDDCCLK	R5	0_4@EV	CRTDCLK
(15)	EXT_CRTDDCDAT	R422	0_4@EV	CRTDDAT
(7)	INT_CRT_RED	R28	*0_4@IV	
(7)	INT_CRT_GRN	R36	*0_4@IV	
(7)	INT_CRT_BLU	R53	*0_4@IV	
(7)	INT_HSYNC	R401	*0_4@IV	
(7)	INT_VSYNC	R17	*0_4@IV	
(7)	INT_CRT_DDCCLK	R4	*0_4@IV	
(7)	INT_CRT_DDCDAT	R417	*0_4@IV	

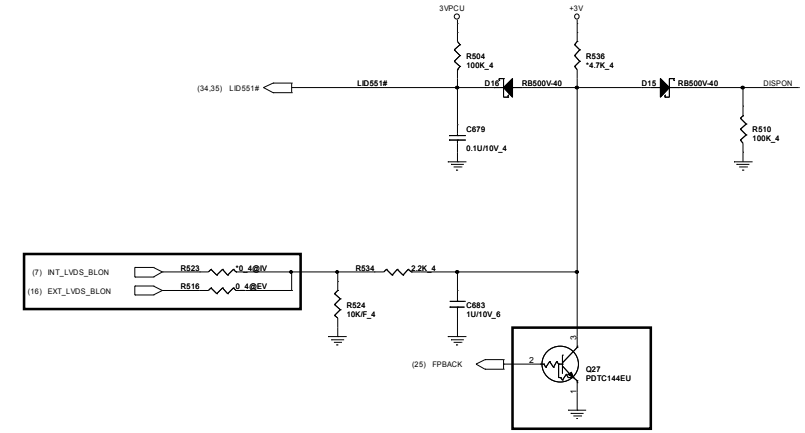
UMA & Discrete setting

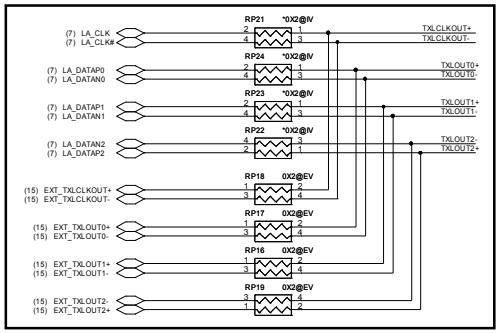
LVDS	Discrete	/ UMA
R27	0	NC
R33	0	NC
R51	0	NC
R400	0	NC
R18	0	NC
R5	0	NC
R422	0	NC
R28	NC	0
R36	NC	0
R53	NC	0
R401	NC	0
R17	NC	0
R4	NC	0
R417	NC	0

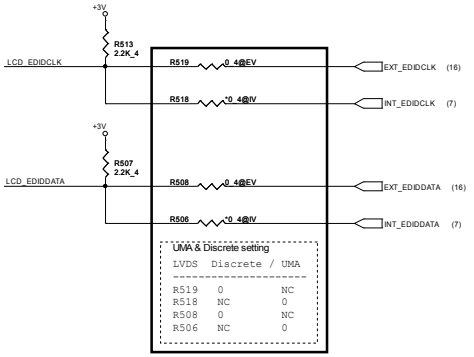


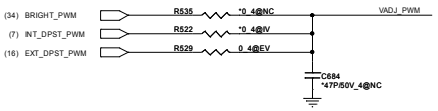
PROJECT : KL1
Quanta Computer Inc.

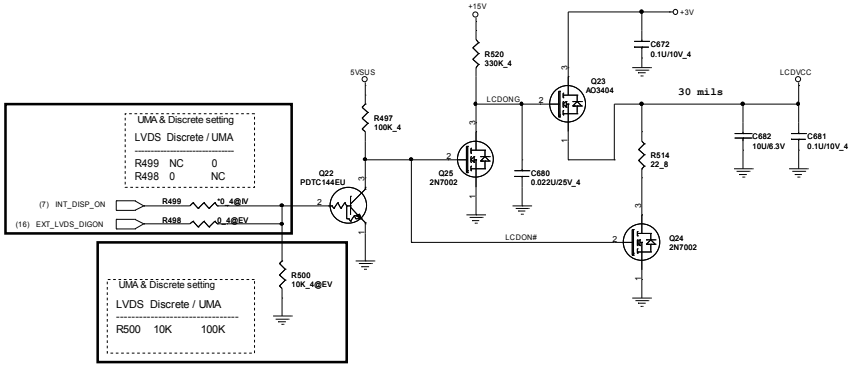
Size	Document Number	Rev
Custom	CRT CONN	A1A
Date: Friday, March 06, 2009	Sheet 20 of 43	







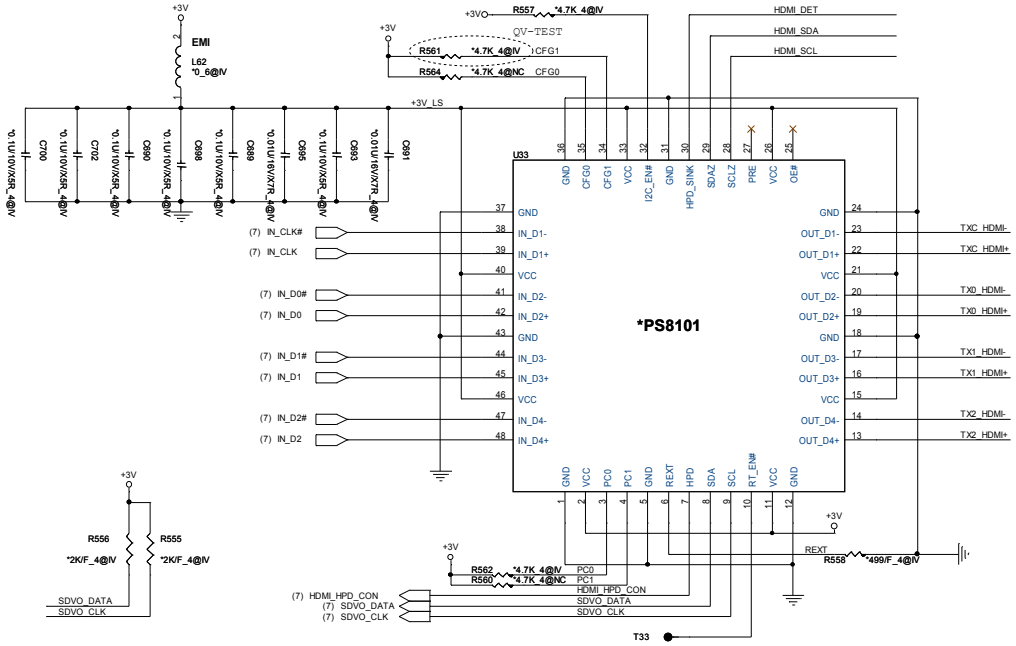




PROJECT : KL1
Quanta Computer Inc.

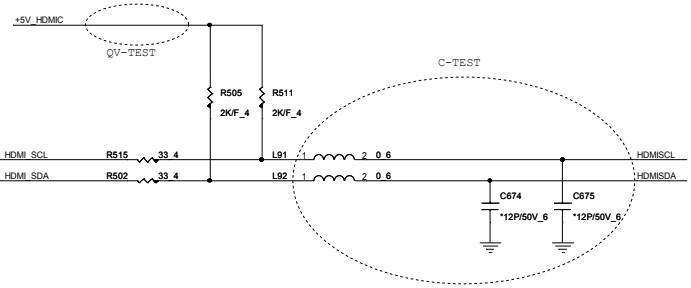
Size	Document Number	Rev
Custom	LCD & LID CONN	A1A
Date: Friday, March 06, 2009	Sheet 21 of 43	

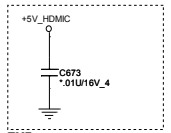
(3,5,7,10,11,12,13,15,16,20,21,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(20,26,28,31,34,35,36,37,38) +5V

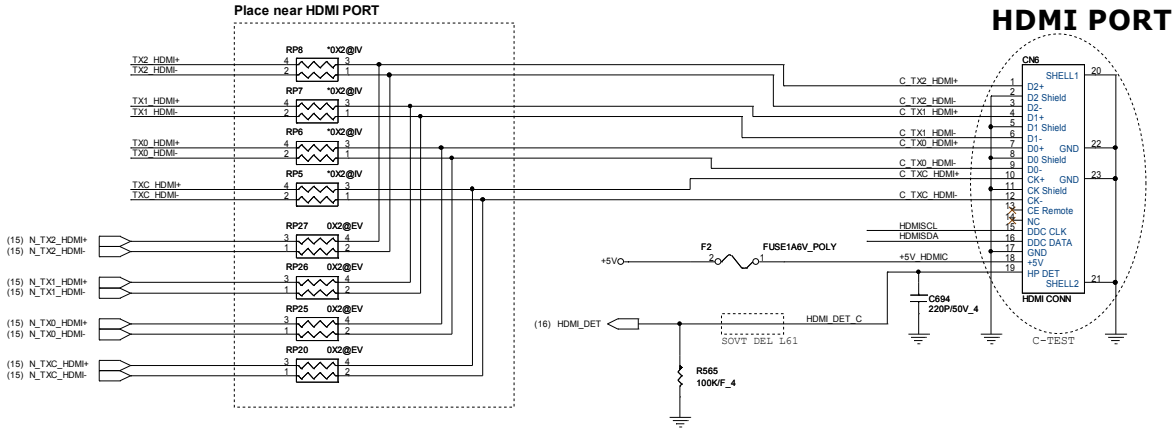


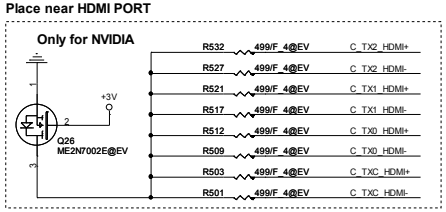
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB



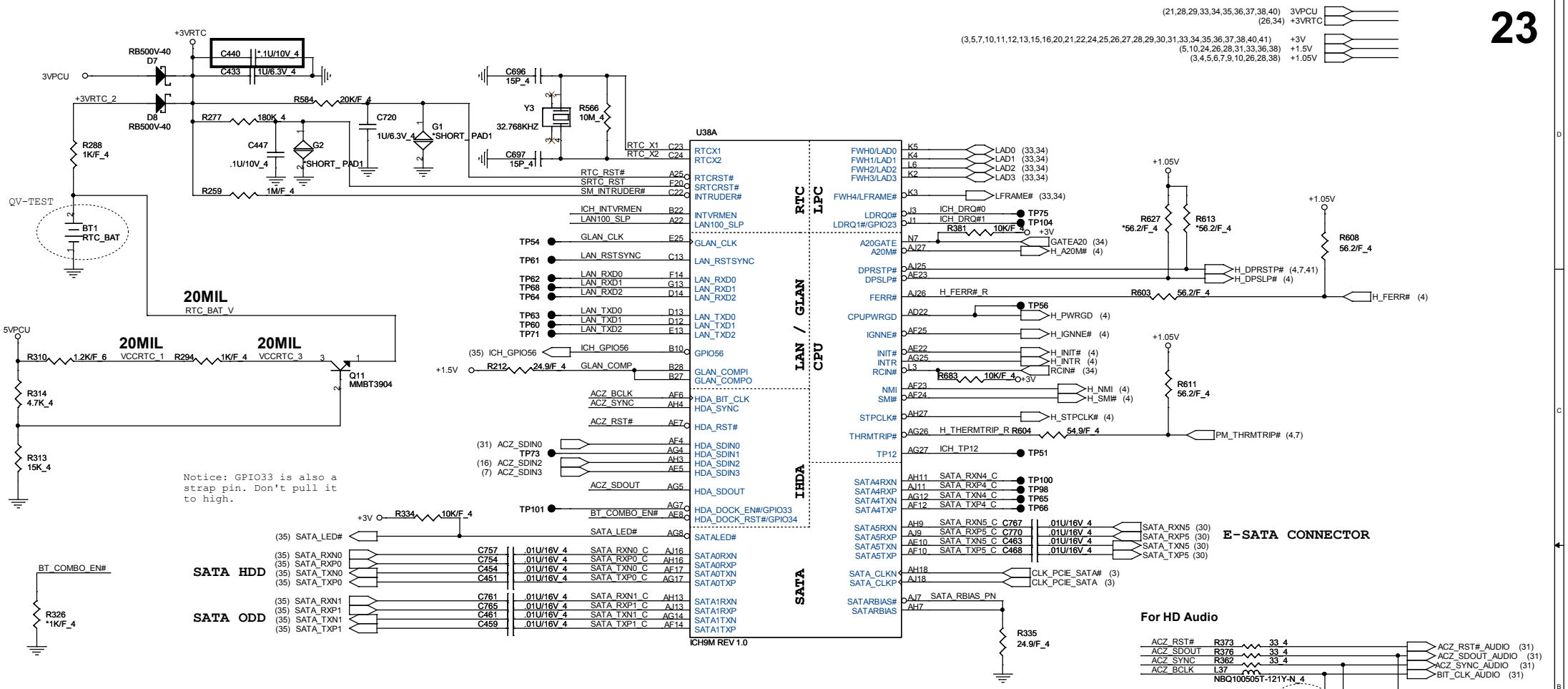






PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
C	PS8101 & HDMI CONN	A1A
Date: Friday, March 06, 2009	Sheet 22 of 43	



(21,28,29,33,34,35,36,37,38,40) 3VPCU
(26,34) +3VRTC
(3,5,7,10,11,12,13,15,16,20,21,22,24,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(5,10,24,26,28,31,33,36,38) +1.5V
(3,4,5,6,7,9,10,26,28,38) +1.05V

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

For HD Audio

For UMA

For Discrete

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M Host 1/4	A1A
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(5,10,23,26,28,31,33,36,38) +1.5V
(3,5,7,10,11,12,13,15,16,20,21,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(25,33,34,36,38,39,41,42) 3VSUS

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E(WWAN)

MINI CARD PCI-E(WLAN)

MINI CARD PCI-E(CARD)

PCIE-LAN

U38D

PCI-Express / Direct Media Interface

SPI

USB

ICH9M REV 1.0

USB Connector
USB Connector
CCD Module

BLUETOOTH

EXPRESS CARD

USB Connector
USB+E-SATA Connector
WWAN Min-Card
WLAN Min-Card

512K byte SPI ROM
For HDCP only

U38B

PCI

Interrupt I/F

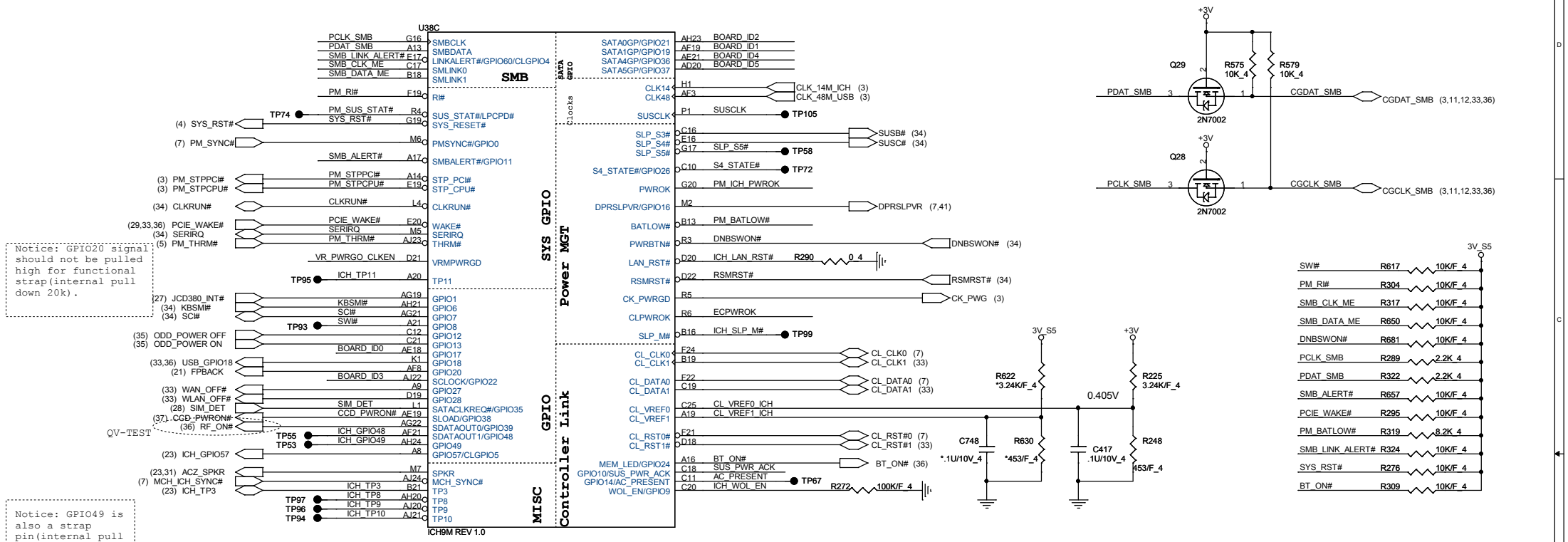
ICH9M REV 1.0

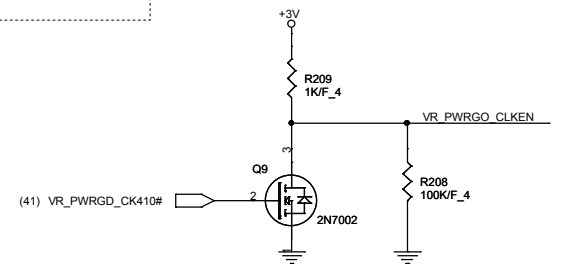
U18 *TC7SH08FU

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M PCIE 2/4	A1A
Date: Friday, March 06, 2009	Sheet 24 of 43	

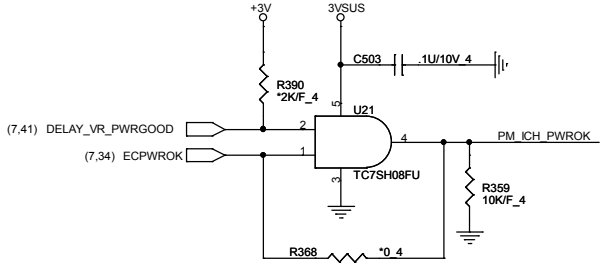
(3,5,7,10,11,12,13,15,16,20,21,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(23,24,26,38) 3V_S5
(33,34,36,38,39,41,42) 3VSUS

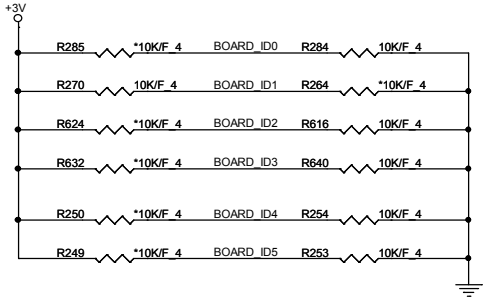


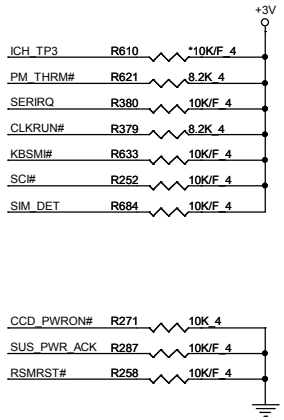


Board ID For Function	ID3 GPIO22	ID2 GPIO21	ID1 GPIO19	ID0 GPIO17
Default	0	0	1	0
GL40	0	1	1	0
GM47	1	0	1	0

Board ID For Model	ID5 GPIO37	ID4 GPIO36
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1
KL1	0	0

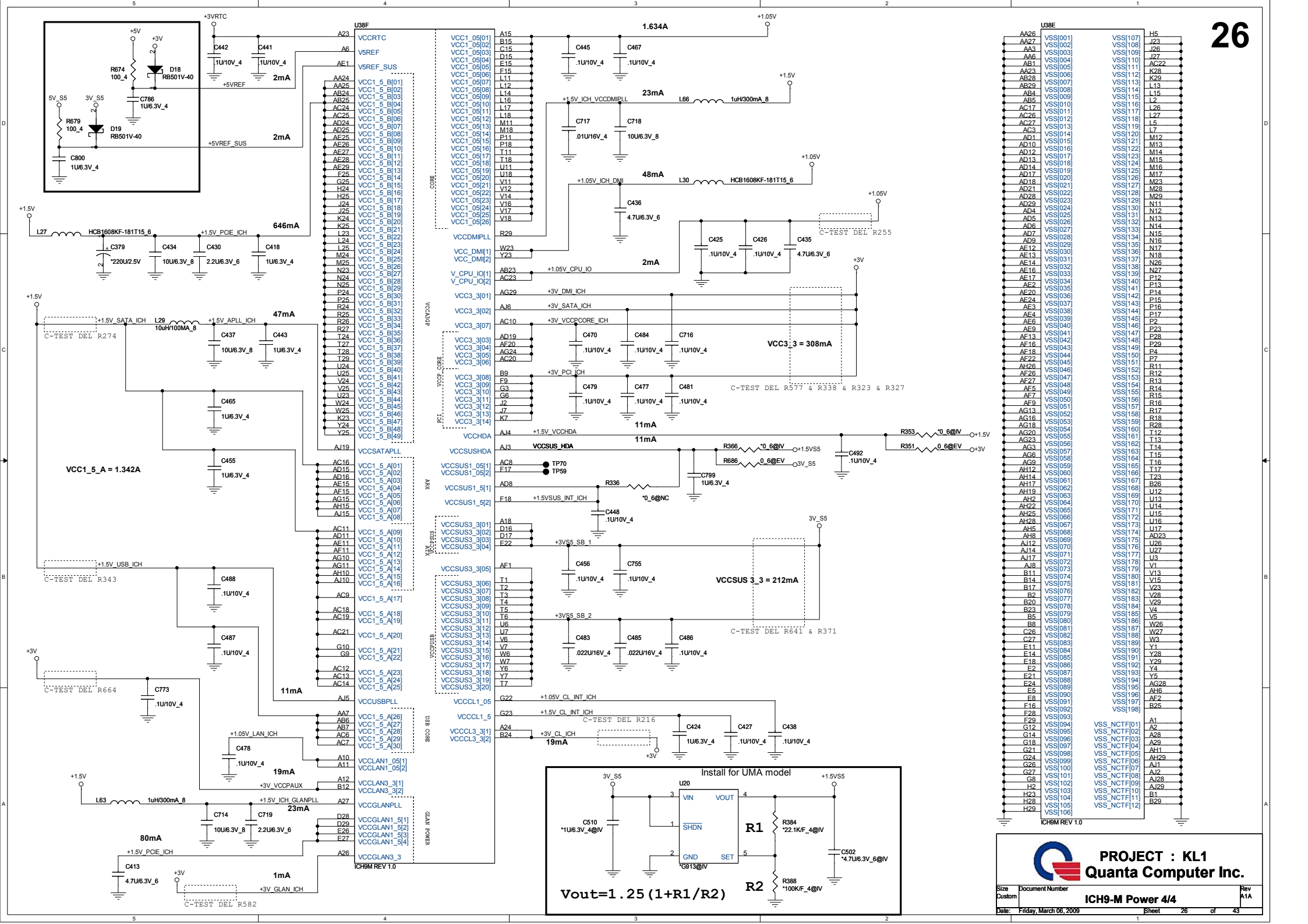


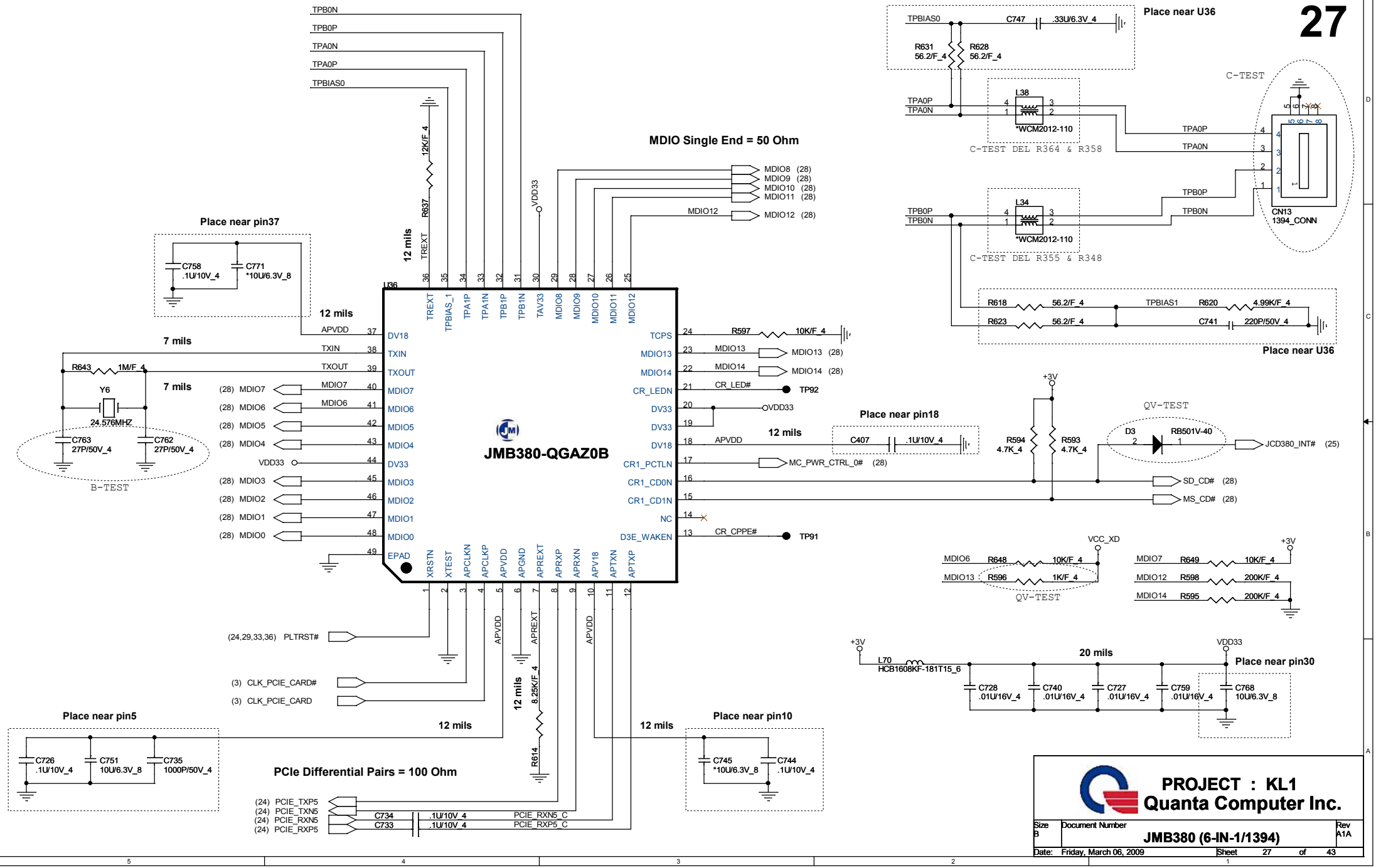




PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	A1A
Date: Friday, March 06, 2009	Sheet 25 of 43	


U38F
U38E
VCC1_5_A = 1.342A
VCCSUS 3_3 = 212mA
VCC3_3 = 308mA
1.634A
23mA
48mA
2mA
11mA
19mA
80mA
1mA
646mA
47mA
Install for UMA model
Vout=1.25(1+R1/R2)
ICH9M REV 1.0
PROJECT : KL1
Quanta Computer Inc.
ICH9-M Power 4/4
Friday, March 06, 2009


JMB380-QGAZ0B
U36
MDIO Single End = 50 Ohm
PCIe Differential Pairs = 100 Ohm
Place near pin37
Place near pin18
Place near pin5
Place near pin10
Place near U36
Place near pin30
B-TEST
C-TEST
QV-TEST
C-TEST DEL R364 & R358
C-TEST DEL R355 & R348
*WCM2012-110
CN13
1394_CONN
12 mils
7 mils
20 mils
TPB0N
TPB0P
TPA0N
TPA0P
TPBIAS0
TPBIAS1
VDD33
+3V
VCC_XD
APVDD
APREXT
PLTRST#
CLK_PCIE_CARD#
CLK_PCIE_CARD
PCIE_RXN5_C
PCIE_RXP5_C
MC_PWR_CTRL_0#
SD_CD#
MS_CD#
JCD380_INT#
CR_LED#
CR_CPPE#
PROJECT : KL1
Quanta Computer Inc.
JMB380 (6-IN-1/1394)
Size B
Document Number
Rev A1A
Date: Friday, March 06, 2009
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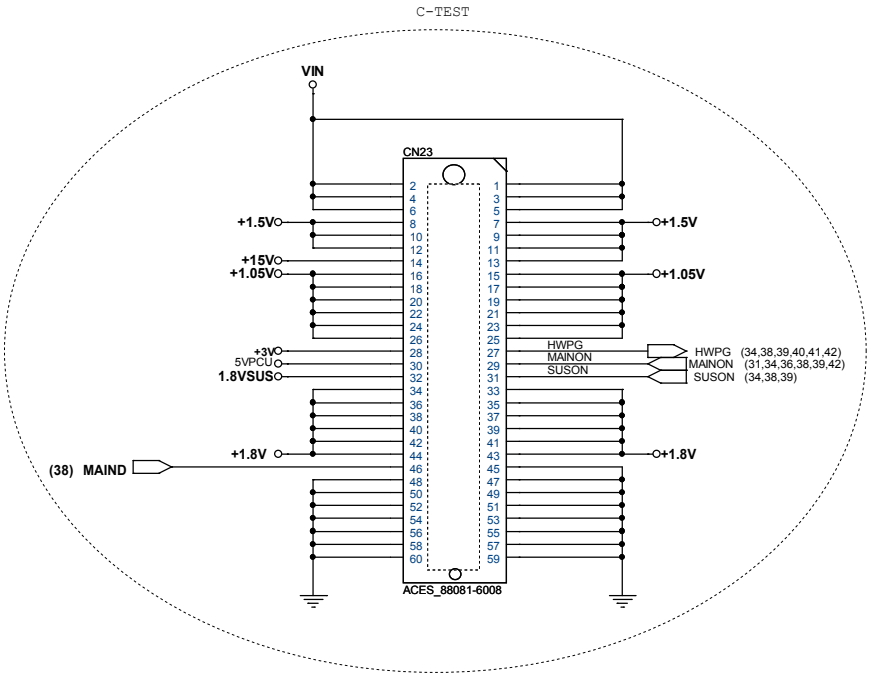
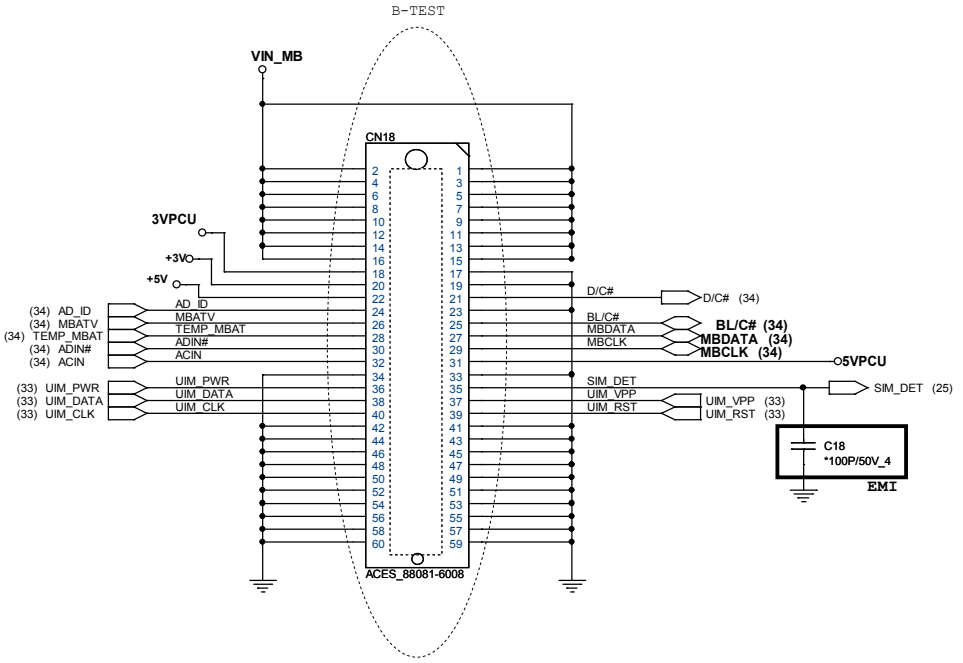
Power Board B to B 60PIN CONN

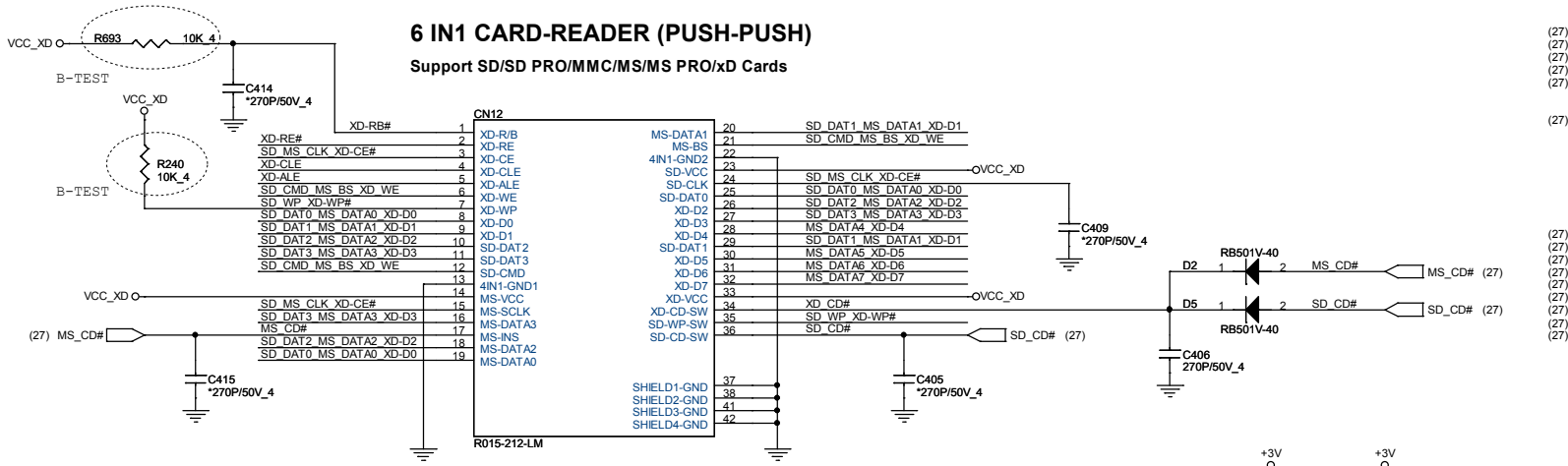


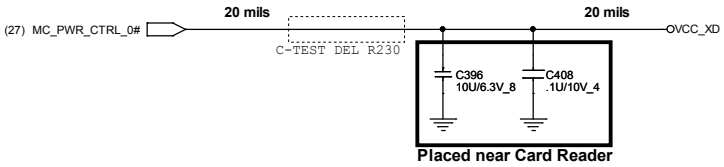
Charger+SIM CARD B to B 60PIN CONN

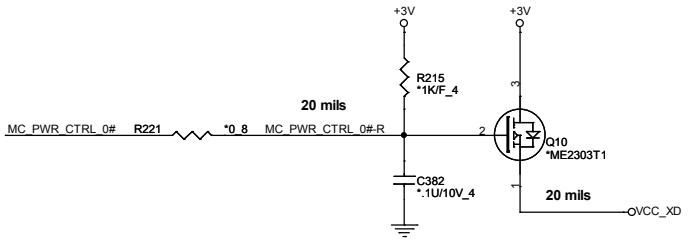


6 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

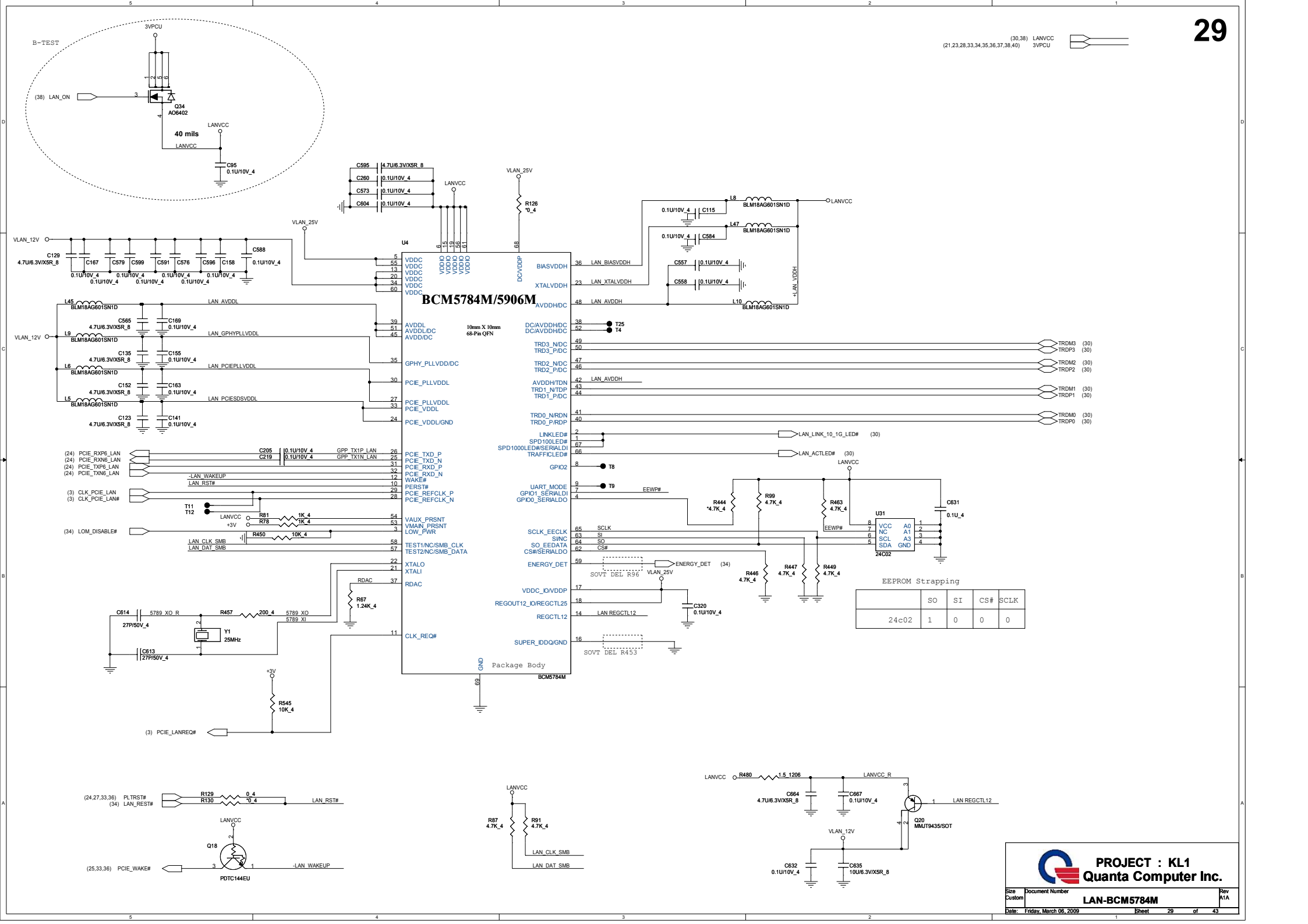






PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	B to B CONN & CR SOCKET	A1A
Date: Friday, March 06, 2009	Sheet 28 of 43	



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN-BCM5784M	A1A

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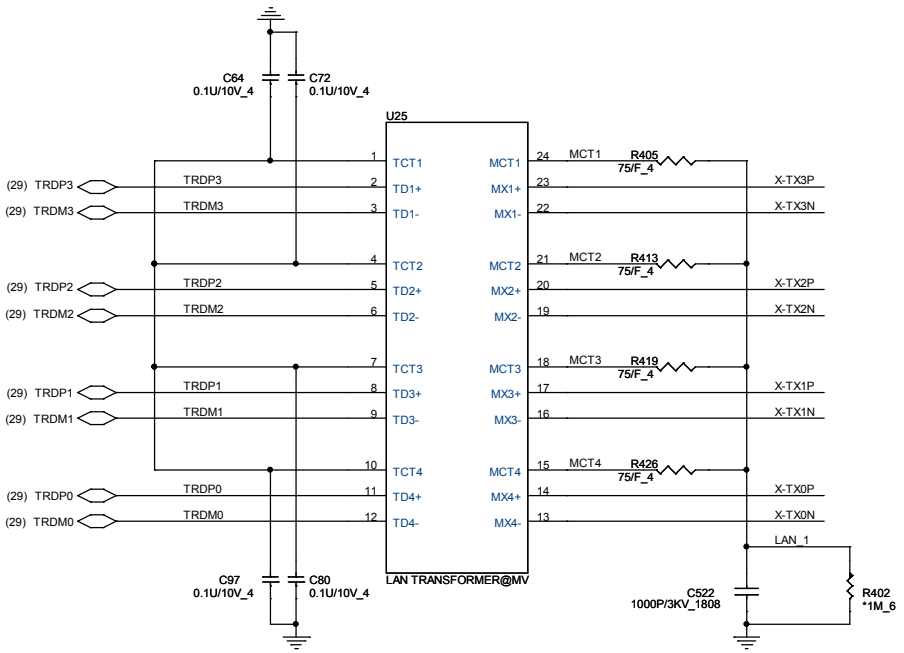
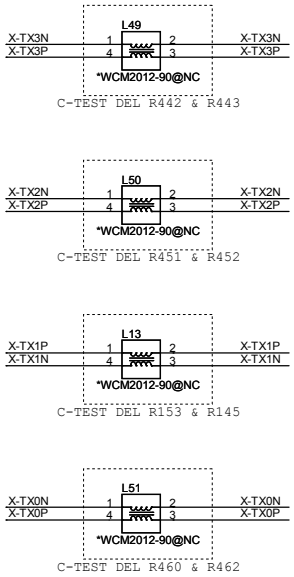
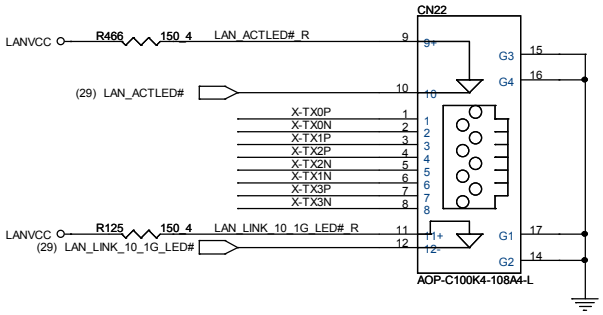
(29,38) LANVCC

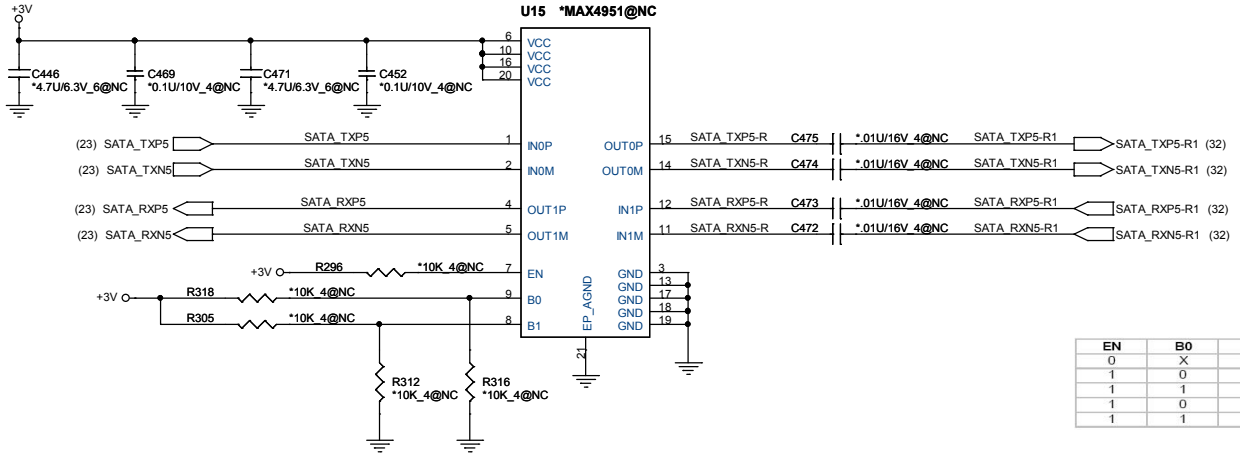




RJ45 CONN



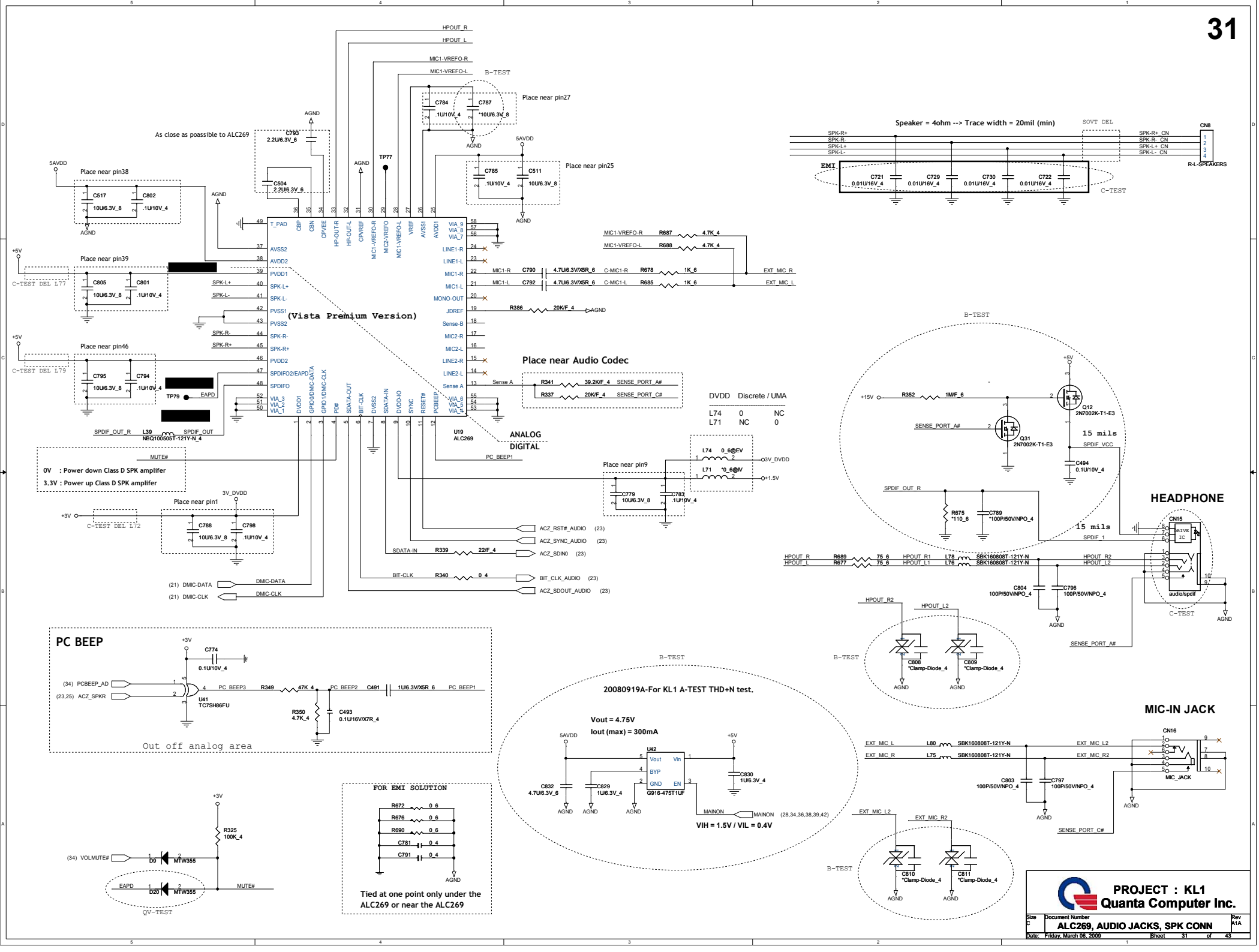
E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

PROJECT : KL1
Quanta Computer Inc.

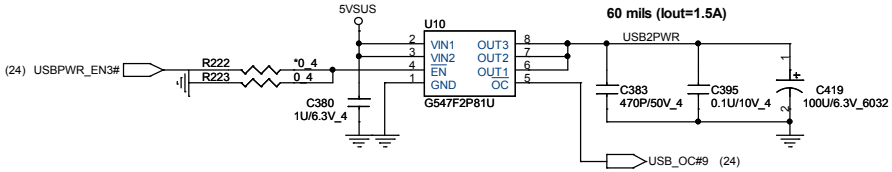
Size	Document Number	Rev
Custom	RJ45, E-SATA RE-DRIVER	A1A
Date: Friday, March 06, 2009	Sheet 30 of 43	

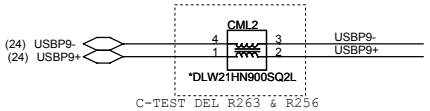


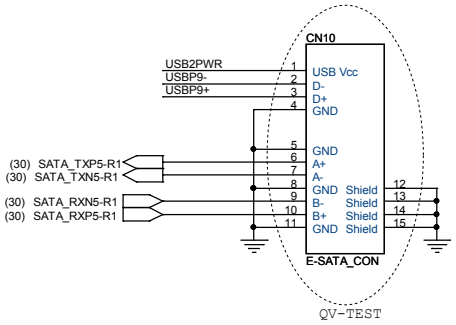
PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
C	ALC269, AUDIO JACKS, SPK CONN	1A
Date: Friday, March 06, 2009	Sheet 31 of 43	

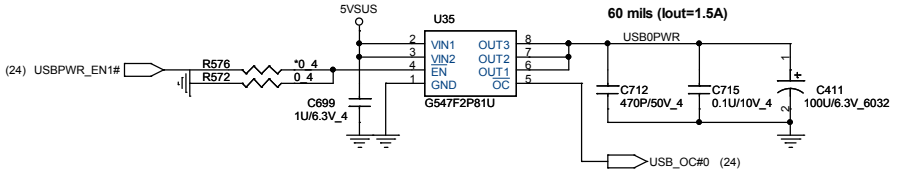
USB + eSATA CONNECTOR

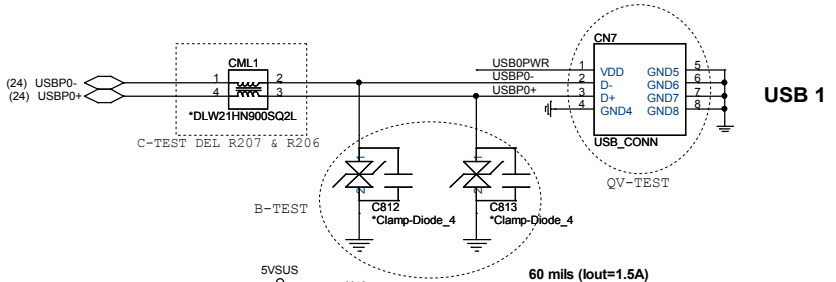


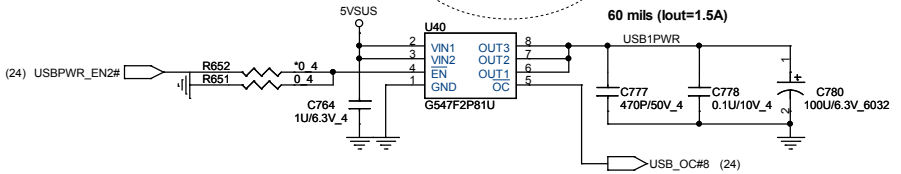


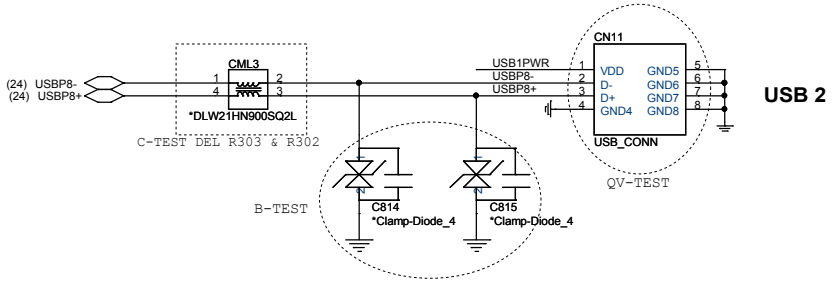


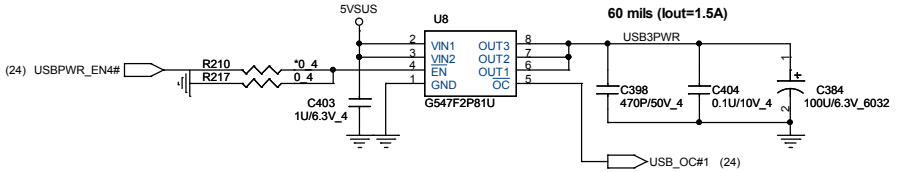
USBX3

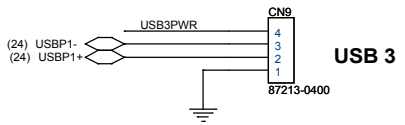








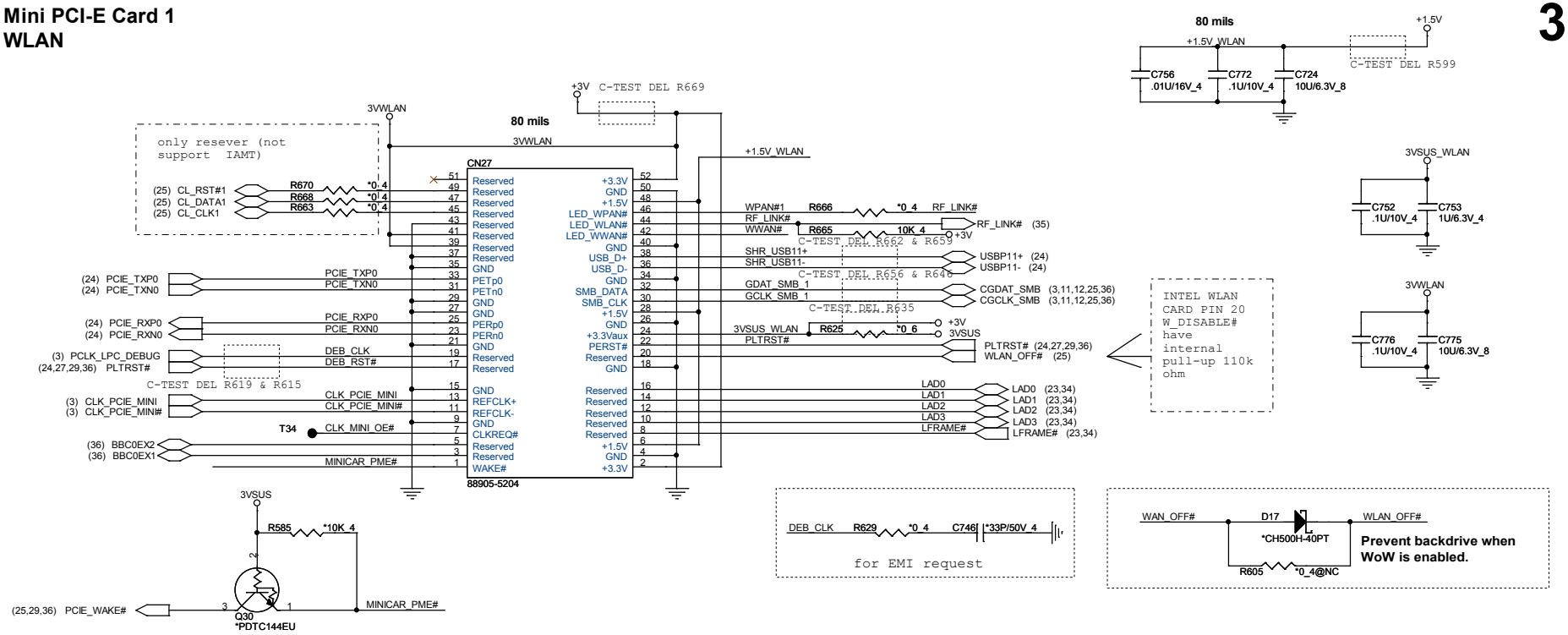




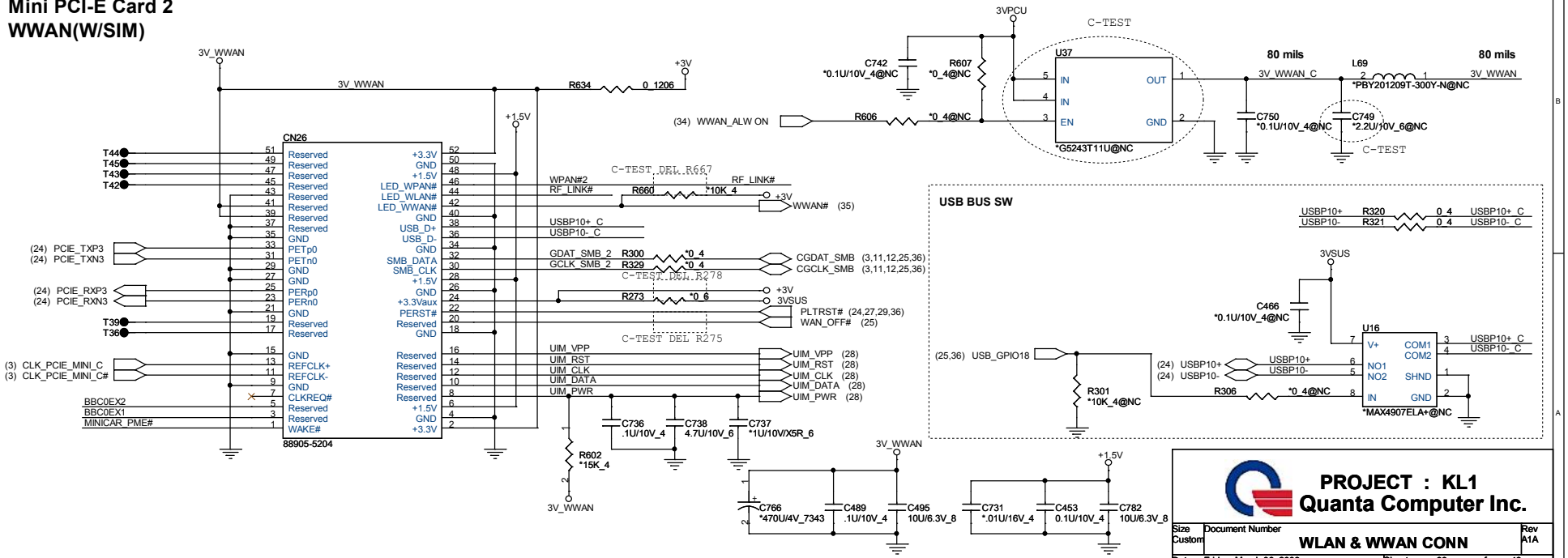
PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USBX3, USB+E-SATA CONN	A1A
Date: Friday, March 06, 2009	Sheet 32 of 43	

Mini PCI-E Card 1
WLAN

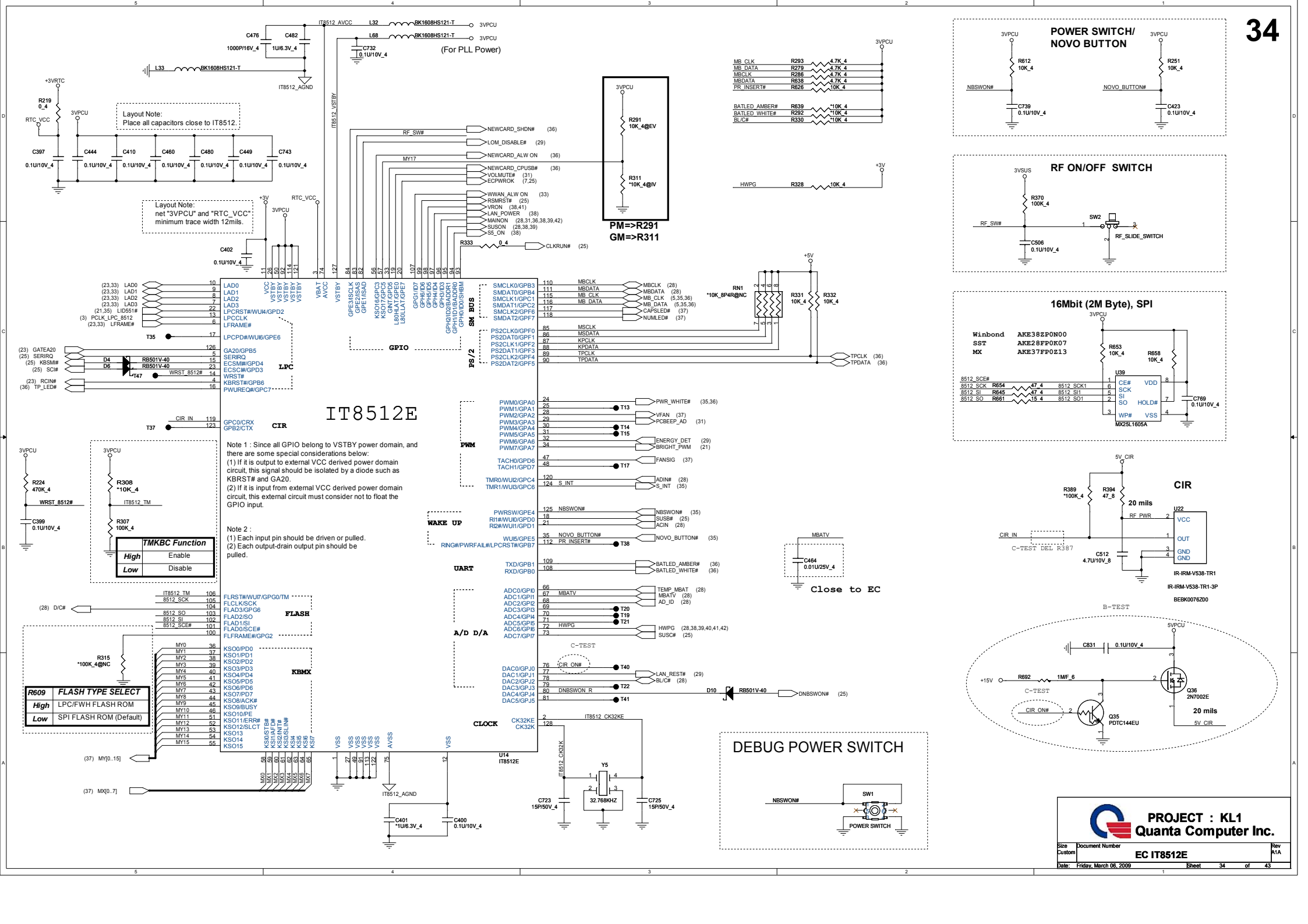


Mini PCI-E Card 2
WWAN(W/SIM)

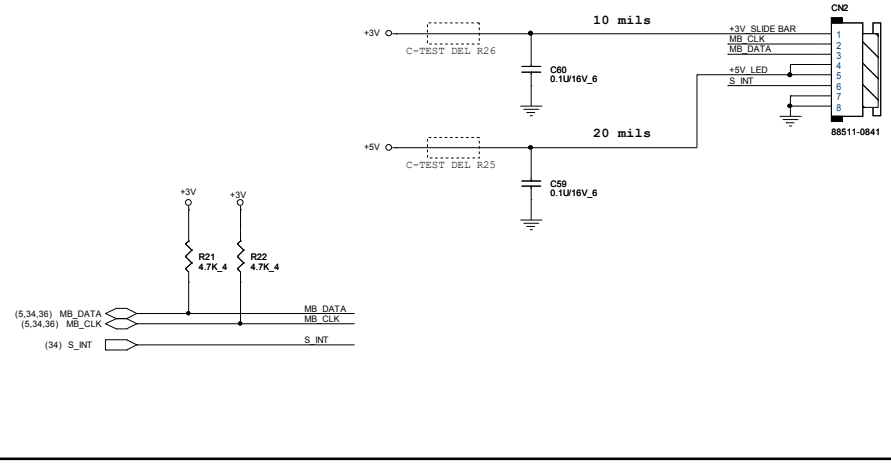


PROJECT : KL1
Quanta Computer Inc.

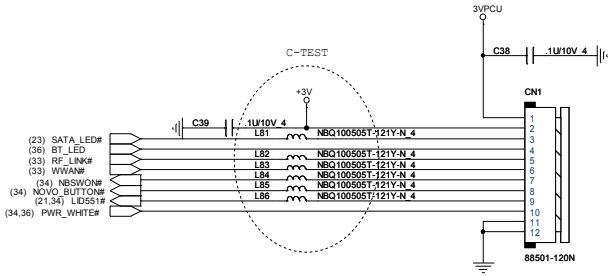
Size	Document Number	Rev
Custom	WLAN & WWAN CONN	A1A
Date: Friday, March 06, 2009	Sheet 33 of 43	


IT8512E
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
PM=>R291
GM=>R311
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R609 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
Close to EC
DEBUG POWER SWITCH
POWER SWITCH/ NOVO BUTTON
RF ON/OFF SWITCH
16Mbit (2M Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
CIR
IR-IRM-V538-TR1
IR-IRM-V538-TR1-3P
BEBK0076Z00
B-TEST
PROJECT : KL1
Quanta Computer Inc.
EC IT8512E
Date: Friday, March 06, 2009
Sheet 34 of 43

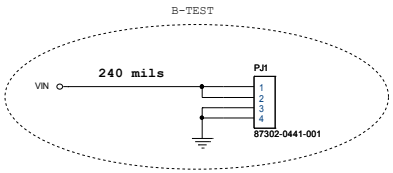
SLIDE BAR CONN



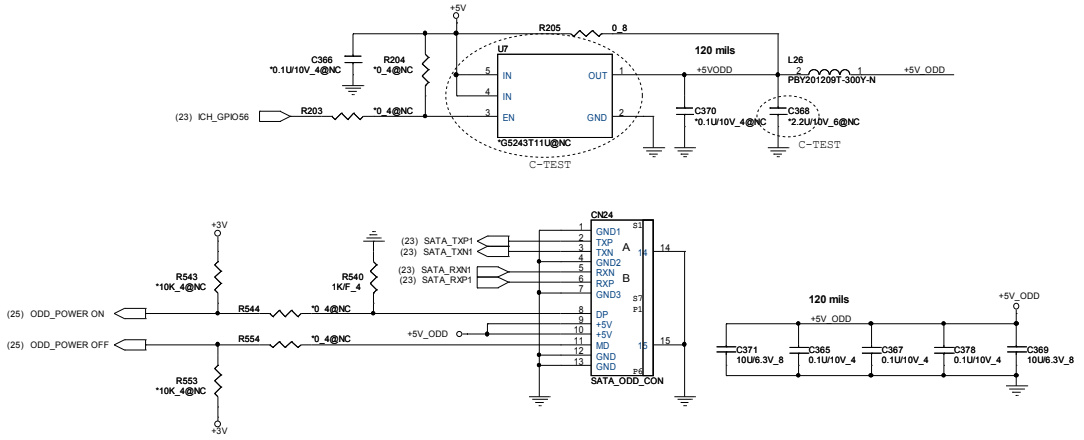
POWER BUTTON/B CONN



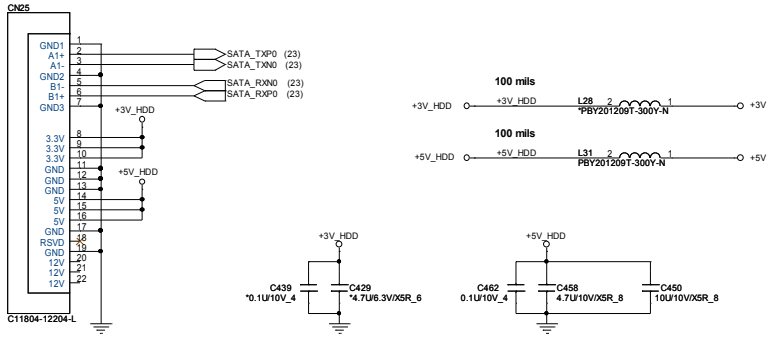
VIN CABLE CONN



SATA CD-ROM



SATA-HDD CONNECTOR



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
C	SATA ODD&HDD, SB, PB/B CONN	MA

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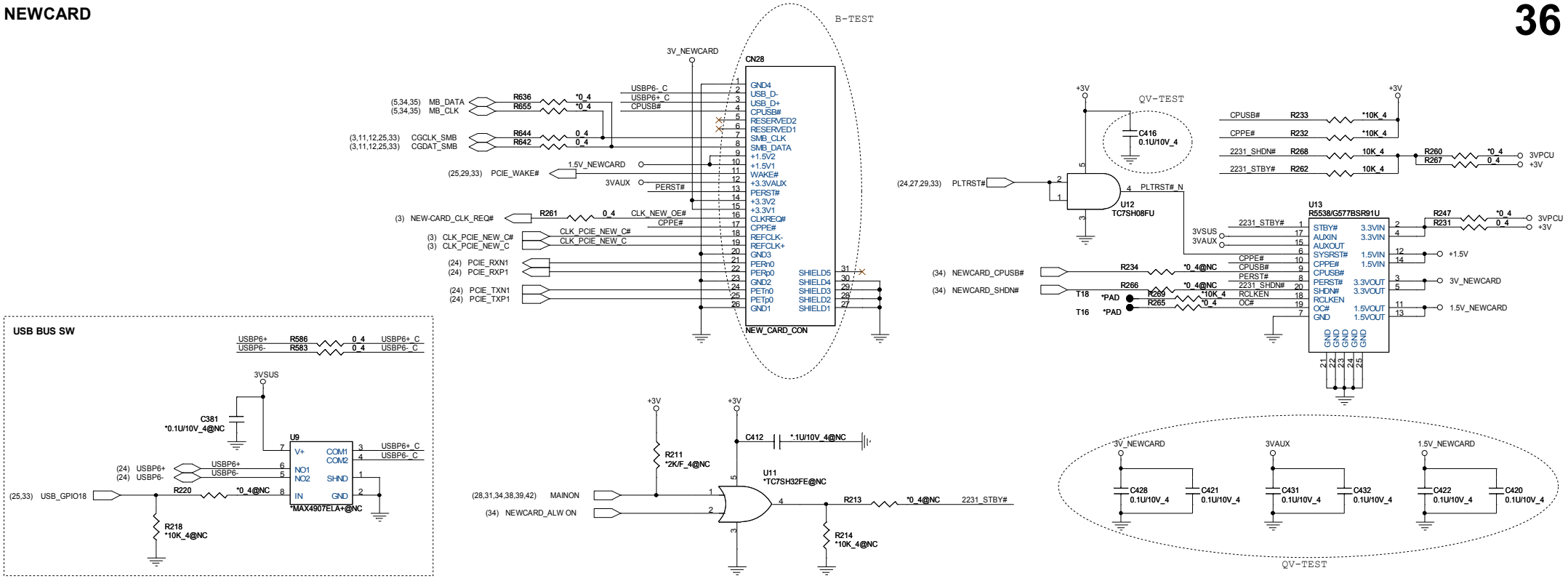
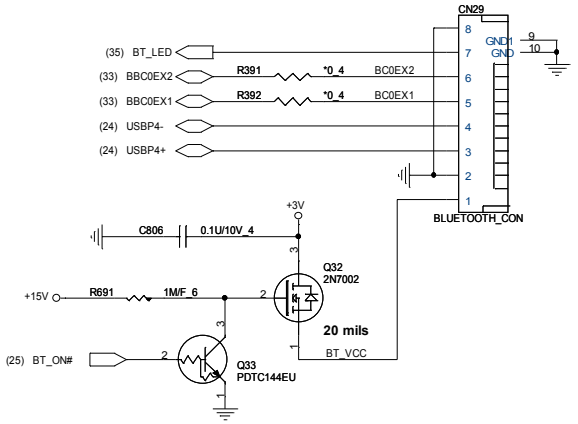
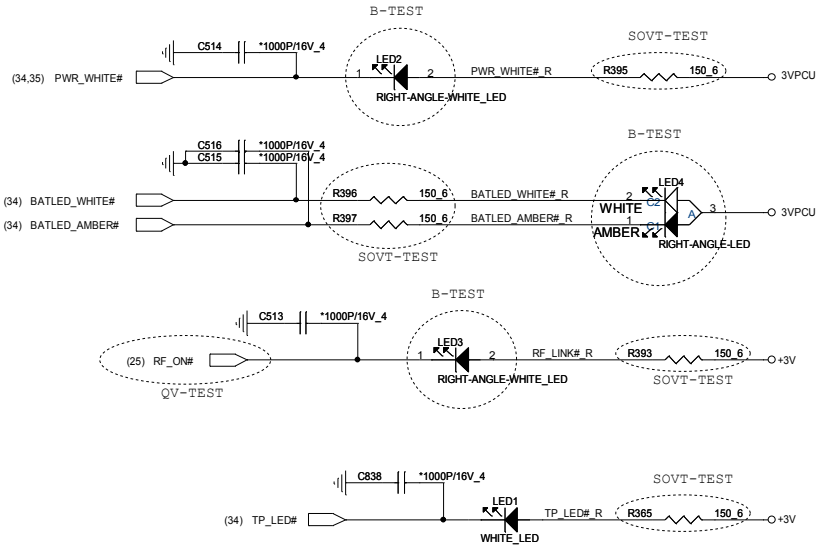
NEWCARD



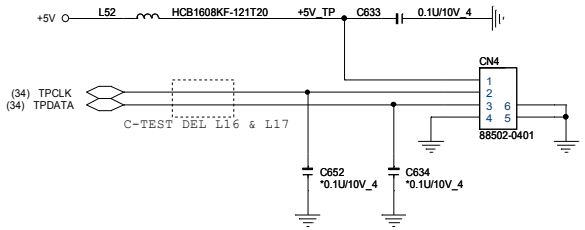
BLUETOOTH



LED



TOUCH PAD



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	T/P, NEW CARD, B/T, LED	A1A

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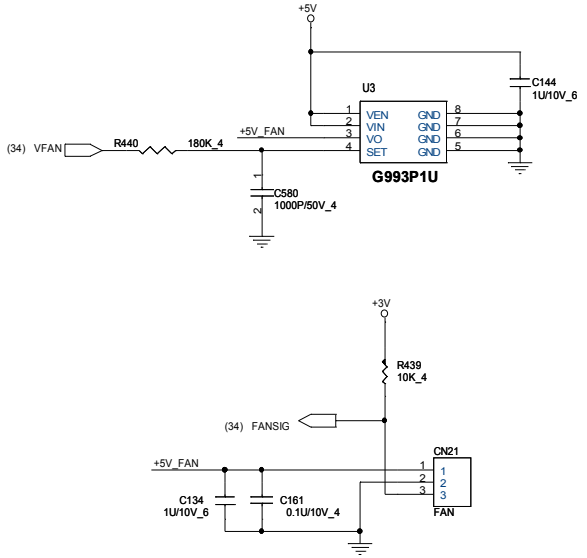
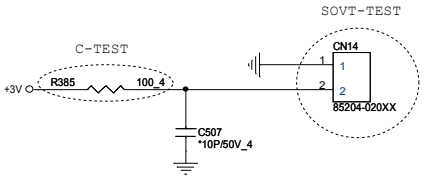
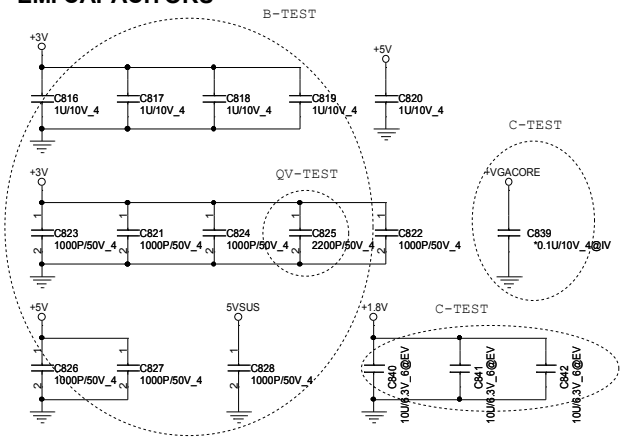
FAN CONTROL

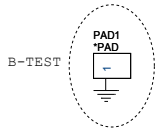


Logo LED CONN



EMI CAPACITORS





WLAN & WWAN CABLE HOLE (NON-PTH)

HOLE9 *H-O157X374D157X374N

(NON-PTH)

HOLE11 *H-C87D87N

M/B SCREW HOLE

HOLE2 *h-c276d110p2
HOLE13 *h-c276d110p2
HOLE4 *h-c217d110p2
HOLE10 *H-C276I150D110P2
C-TEST
B-TEST
HOLE12 *h-c276d110p2
HOLE14 *h-c276d110p2
HOLE15 *h-c276d110p2
HOLE1 *h-c276d110p2
HOLE8 *h-c276d110p2

CPU HOLE (NON-PTH)

HOLE3 *h-c142d142n
HOLE6 *h-c142d142n
HOLE7 *h-c142d142n
HOLE5 *h-c142d142n

QV-TEST

VGA NUT (NON-PTH)

HOLE18 h-c197d142p2
HOLE17 h-c197d142p2

C-TEST

WLAN NUT

HOLE22 H-C150I110D80P2
HOLE20 H-C150I110D80P2

WWAN NUT

HOLE21 H-C150I110D80P2
HOLE23 H-C150I110D80P2

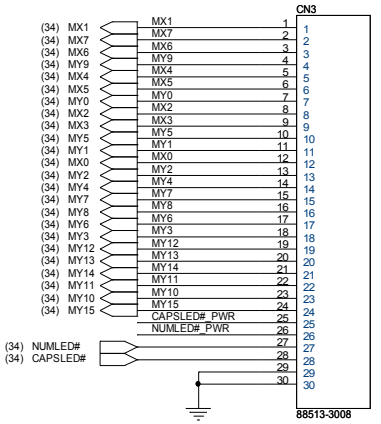
CHARGER+SIM/B NUT

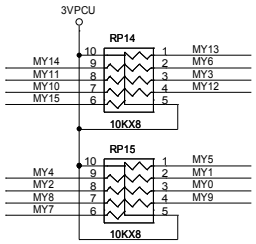
HOLE16 H-C228D87P2

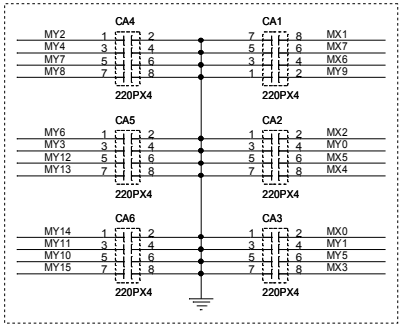
POWER/B NUT

HOLE19 H-C228D87P2

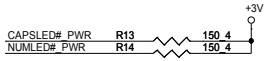
KEYBOARD



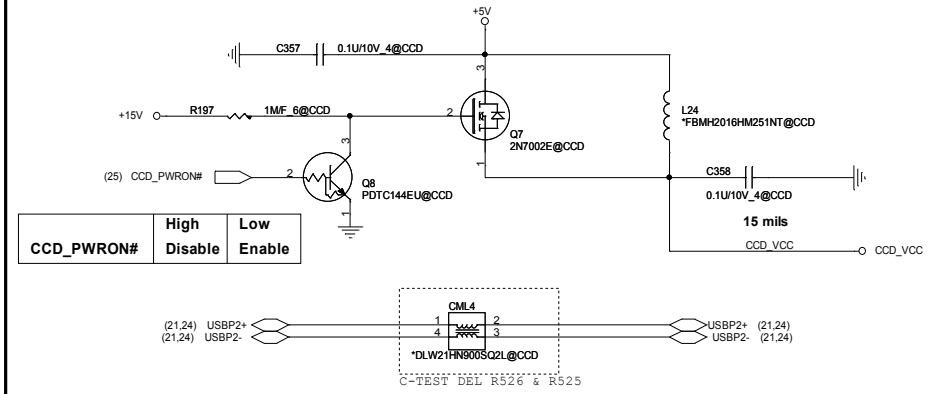




For EMI request



CCD MODULE



CCD_PWRON#	High	Low
	Disable	Enable

C-TEST DEL R526 & R525

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN & K/B CONN, CCD, HOLES, EMI	A1A
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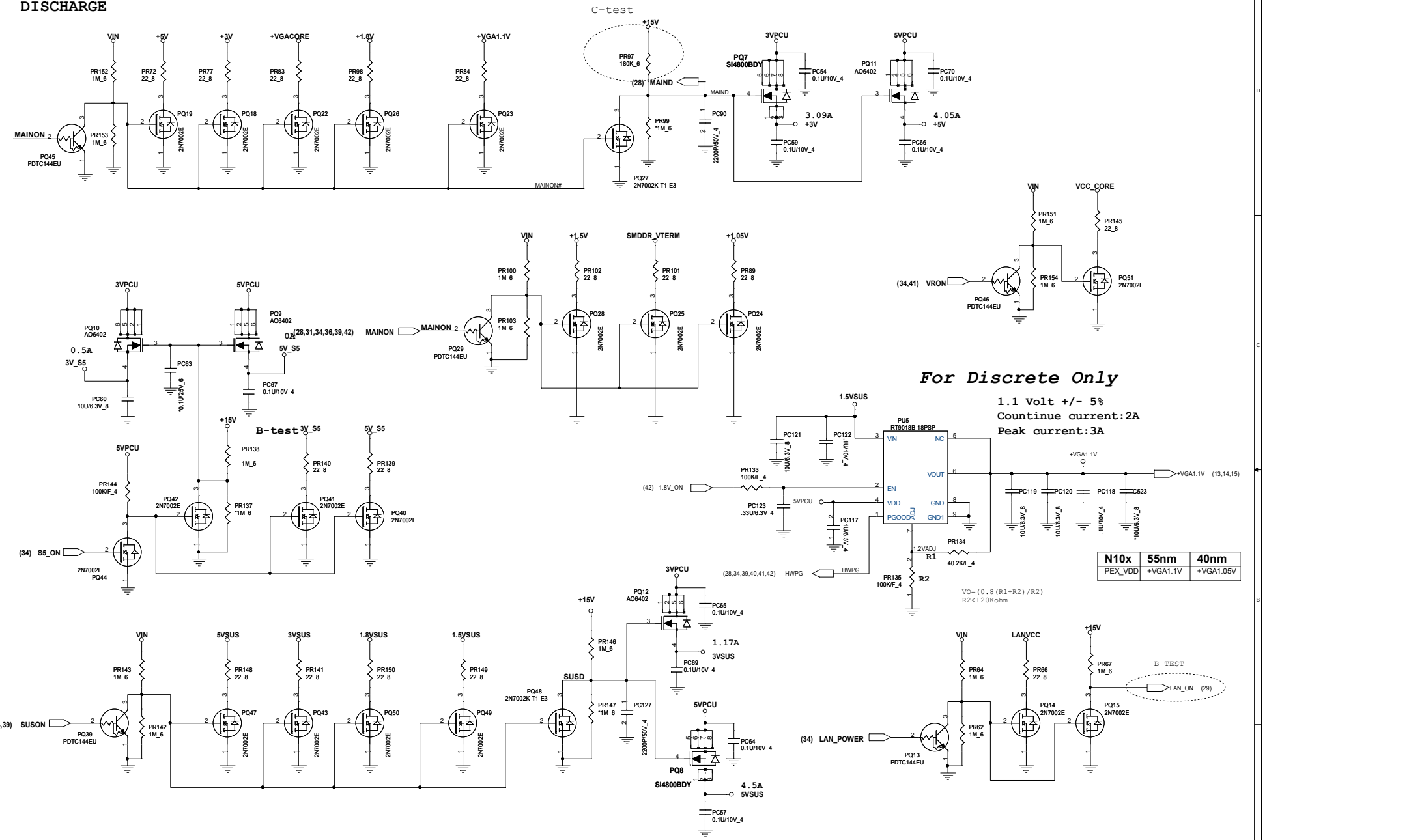
DISCHARGE



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	A1A

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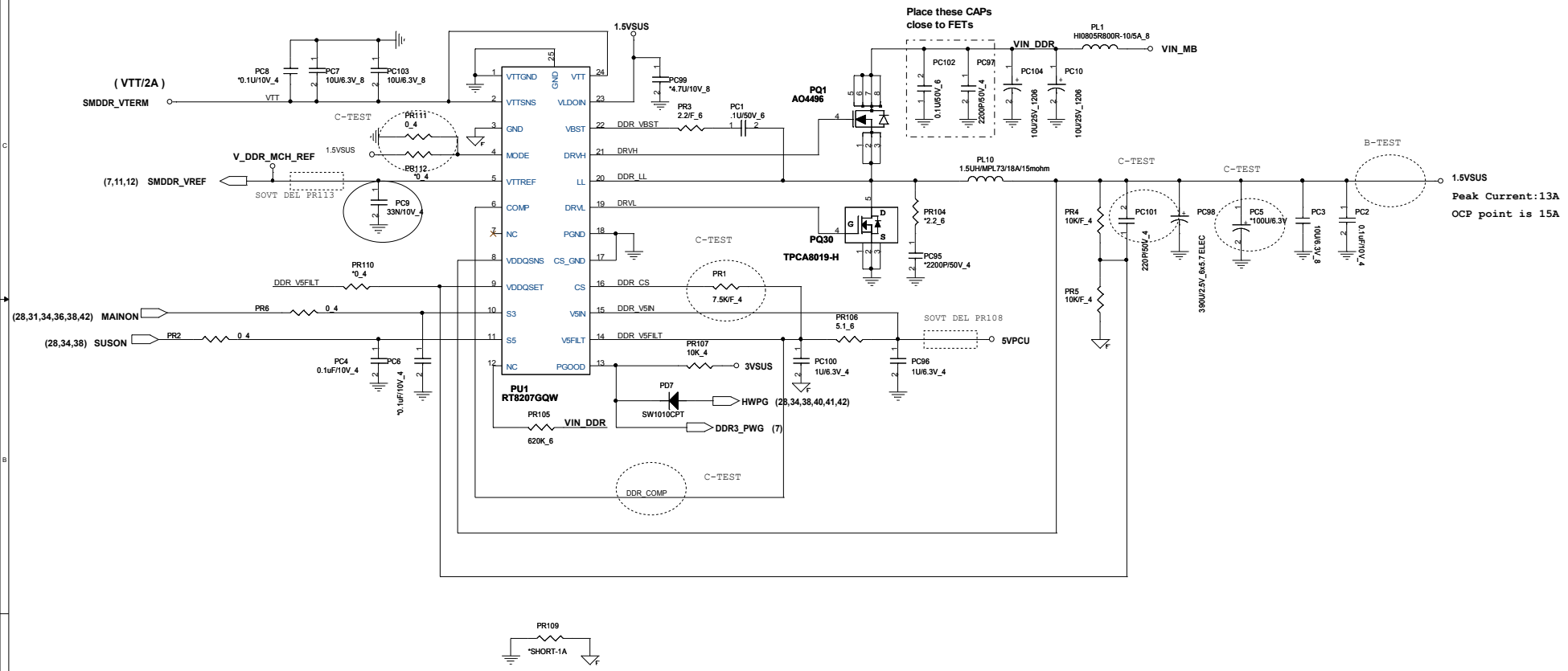

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (TPS51116PEGR)	A1A

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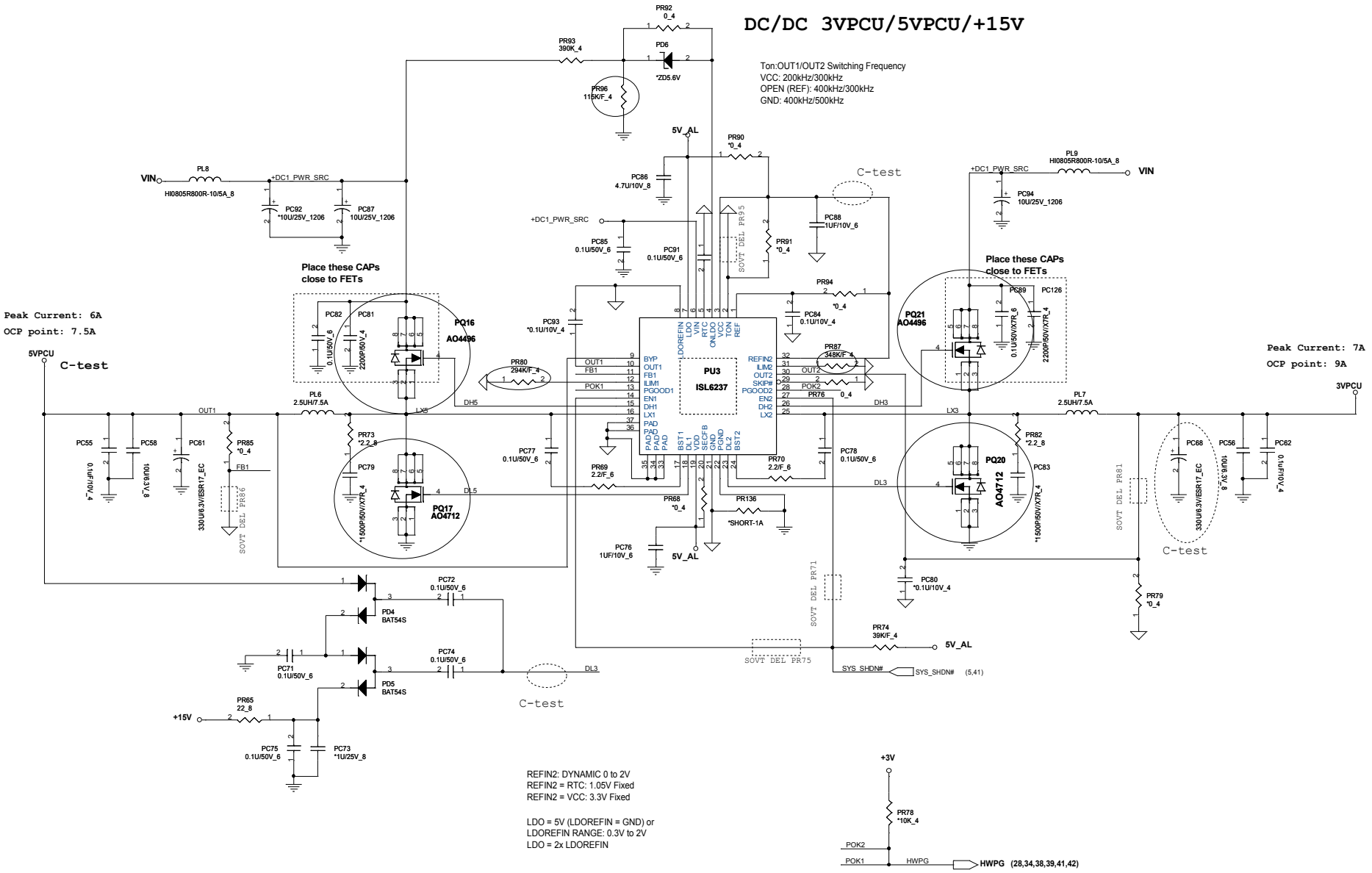
DC/DC 3VPCU/5VPCU/+15V



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+5V (ISL6237)	A1A

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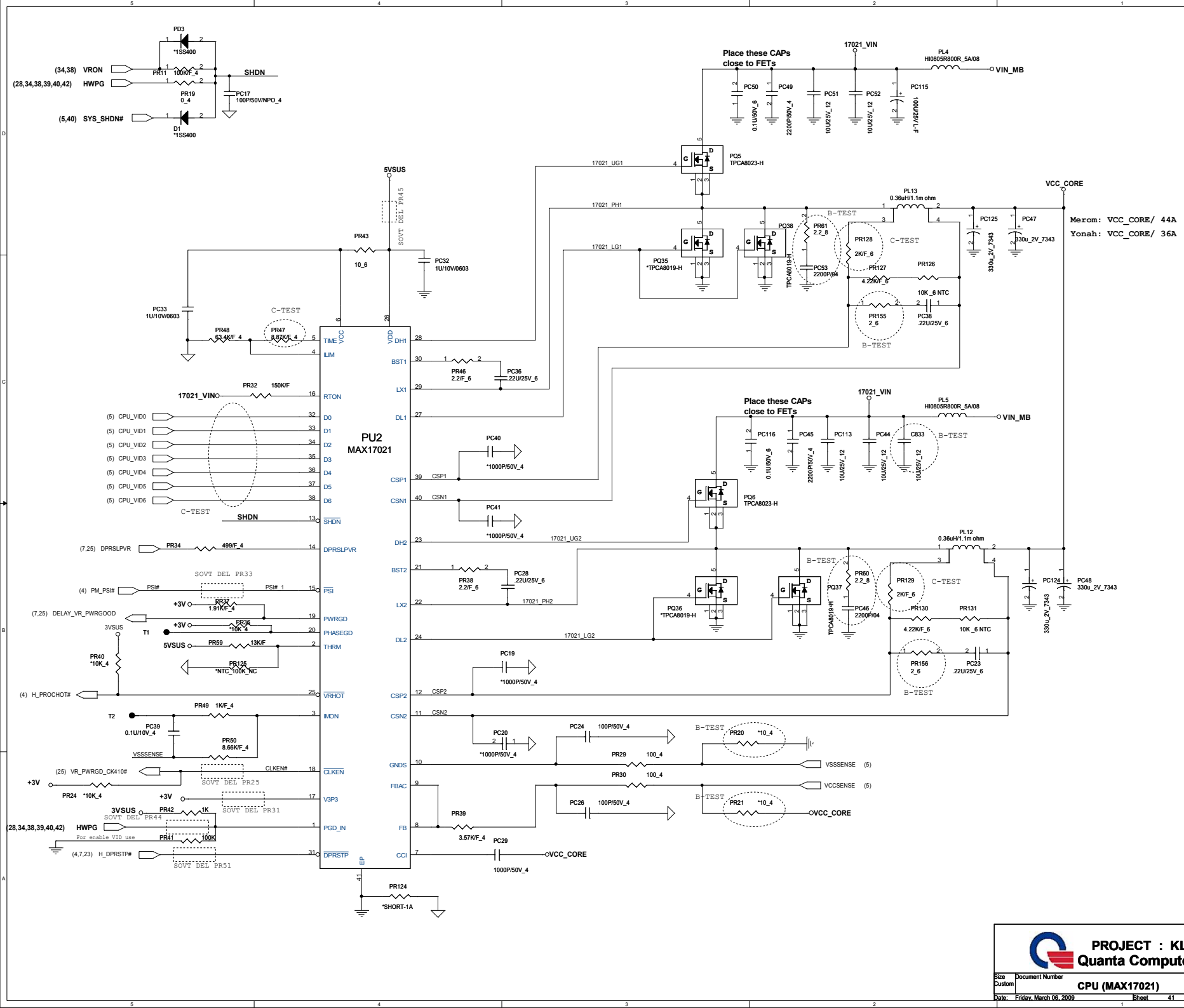
PU2
MAX17021
17021_VIN
5VSUS
VCC_CORE
Place these CAPs close to FETs
Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
PD3 *1SS400
D1 *1SS400
(34,38) VRON
(28,34,38,39,40,42) HWPG
(5,40) SYS_SHDN#
SHDN
PR11 100K/F_4
PR19 0_4
PC17 100P/50V/NPO_4
PR43 10_6
PC32 1U/10V/0603
SOVT DEL PR45
PC33 1U/10V/0603
C-TEST
PR48 63.4K/F_4
PR47 8.87K/F_4
PR32 150K/F
PR46 2.2/F_6
PC36 .22U/25V_6
PC40 *1000P/50V_4
PC41 *1000P/50V_4
PC19 *1000P/50V_4
PC20 *1000P/50V_4
PC24 100P/50V_4
PC26 100P/50V_4
PR39 3.57K/F_4
PC29 1000P/50V_4
PR124 *SHORT-1A
PR20 *10_4
PR21 *10_4
PR29 100_4
PR30 100_4
VSSSENSE (5)
VCCSENSE (5)
PQ5 TPCA8023-H
PQ35 *TPCA8019-H
PQ38 TPCA8019-H
PQ6 TPCA8023-H
PQ36 *TPCA8019-H
PQ37 TPCA8019-H
PR61 2.2_8
PR128 2K/F_6
PR127 4.22K/F_6
PR126 10K_6 NTC
PR155 2_6
PC53 2200P/04
PC38 .22U/25V_6
PL13 0.36uH/1.1m ohm
PC125 330u_2V_7343
PC47 330u_2V_7343
PC50 0.1U/50V_6
PC49 2200P/50V_4
PC51 10U/25V_12
PC52 10U/25V_12
PC115 100U/25V_L-F
PL4 HI0805R800R_5A/08
VIN_MB
PC116 0.1U/50V_6
PC45 2200P/50V_4
PC113 10U/25V_12
PC44 10U/25V_12
C833 10U/25V_12
PL5 HI0805R800R_5A/08
PR60 2.2_8
PR129 2K/F_6
PR46 4.22K/F_6
PR130 4.22K/F_6
PR131 10K_6 NTC
PR156 2_6
PC46 2200P/04
PC23 .22U/25V_6
PL12 0.36uH/1.1m ohm
PC124 330u_2V_7343
PC48 330u_2V_7343
B-TEST
C-TEST
17021_UG1
17021_PH1
17021_LG1
17021_UG2
17021_PH2
17021_LG2
TIME
ILIM
RTON
D0
D1
D2
D3
D4
D5
D6
SHDN
DPRSLPVR
PSI
PWRGD
PHASEGD
THRM
VRHOT
IMON
CLKEN
V3P3
PGD_IN
DPRSTP
VCC
VDD
DH1
BST1
LX1
DL1
CSP1
CSN1
DH2
BST2
LX2
DL2
CSP2
CSN2
GNDS
FBAC
FB
CCI
EP
(5) CPU_VID0
(5) CPU_VID1
(5) CPU_VID2
(5) CPU_VID3
(5) CPU_VID4
(5) CPU_VID5
(5) CPU_VID6
(7,25) DPRSLPVR
(4) PM_PSI#
(7,25) DELAY_VR_PWRGOOD
(4) H_PROCHOT#
(25) VR_PWRGD_CK410#
(4,7,23) H_DPRSTP#
PR34 499/F_4
PR37 1.91K/F_4
PR36 *10K_4
PR59 13K/F
PR125 *NTC_100K_NC
PR40 *10K_4
PR49 1K/F_4
PC39 0.1U/10V_4
PR50 8.66K/F_4
PR24 *10K_4
PR42 1K
PR41 100K
For enable VID use
SOVT DEL PR33
SOVT DEL PR25
SOVT DEL PR31
SOVT DEL PR44
SOVT DEL PR51
T1
T2
3VSUS
+3V
PROJECT : KL1
Quanta Computer Inc.
CPU (MAX17021)
Size Custom
Document Number
Rev A1A
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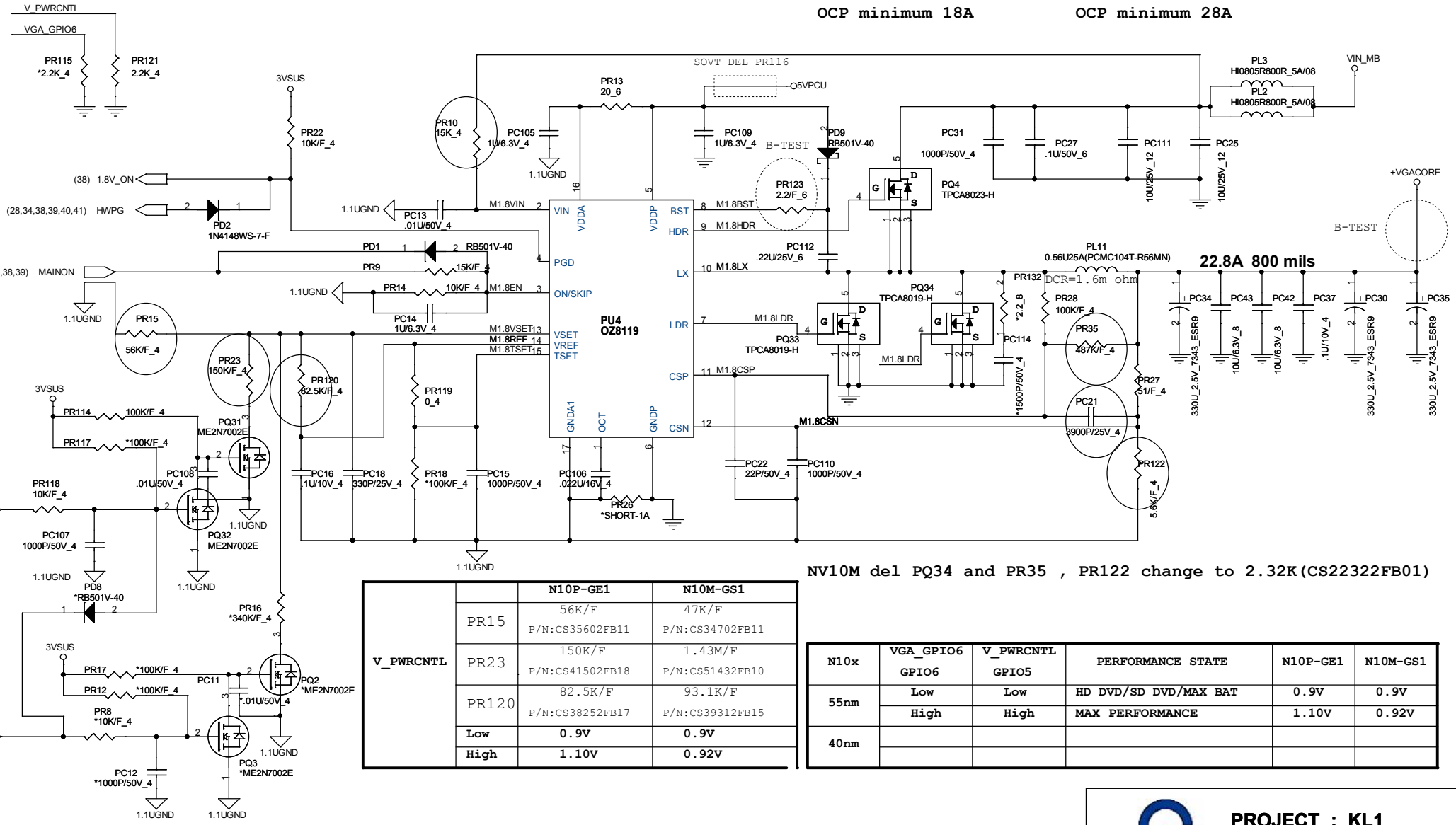
VGA Core & VCC1.1

NV10M +0.92Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 18A

NV10P +1.1Volt +/- 5%
Countinue current:20A
Peak current:23A
OCP minimum 28A



V_PWRCNTL		N10P-GE1	N10M-GS1
	PR15	56K/F P/N:CS35602FB11	47K/F P/N:CS34702FB11
	PR23	150K/F P/N:CS41502FB18	1.43M/F P/N:CS51432FB10
	PR120	82.5K/F P/N:CS38252FB17	93.1K/F P/N:CS39312FB15
	Low	0.9V	0.9V
	High	1.10V	0.92V

NV10M del PQ34 and PR35 , PR122 change to 2.32K(CS22322FB01)

N10x	VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	PERFORMANCE STATE	N10P-GE1	N10M-GS1
55nm	Low	Low	HD DVD/SD DVD/MAX BAT	0.9V	0.9V
	High	High	MAX PERFORMANCE	1.10V	0.92V
40nm					

PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
B	VGA Core (OZ8119)	A1A
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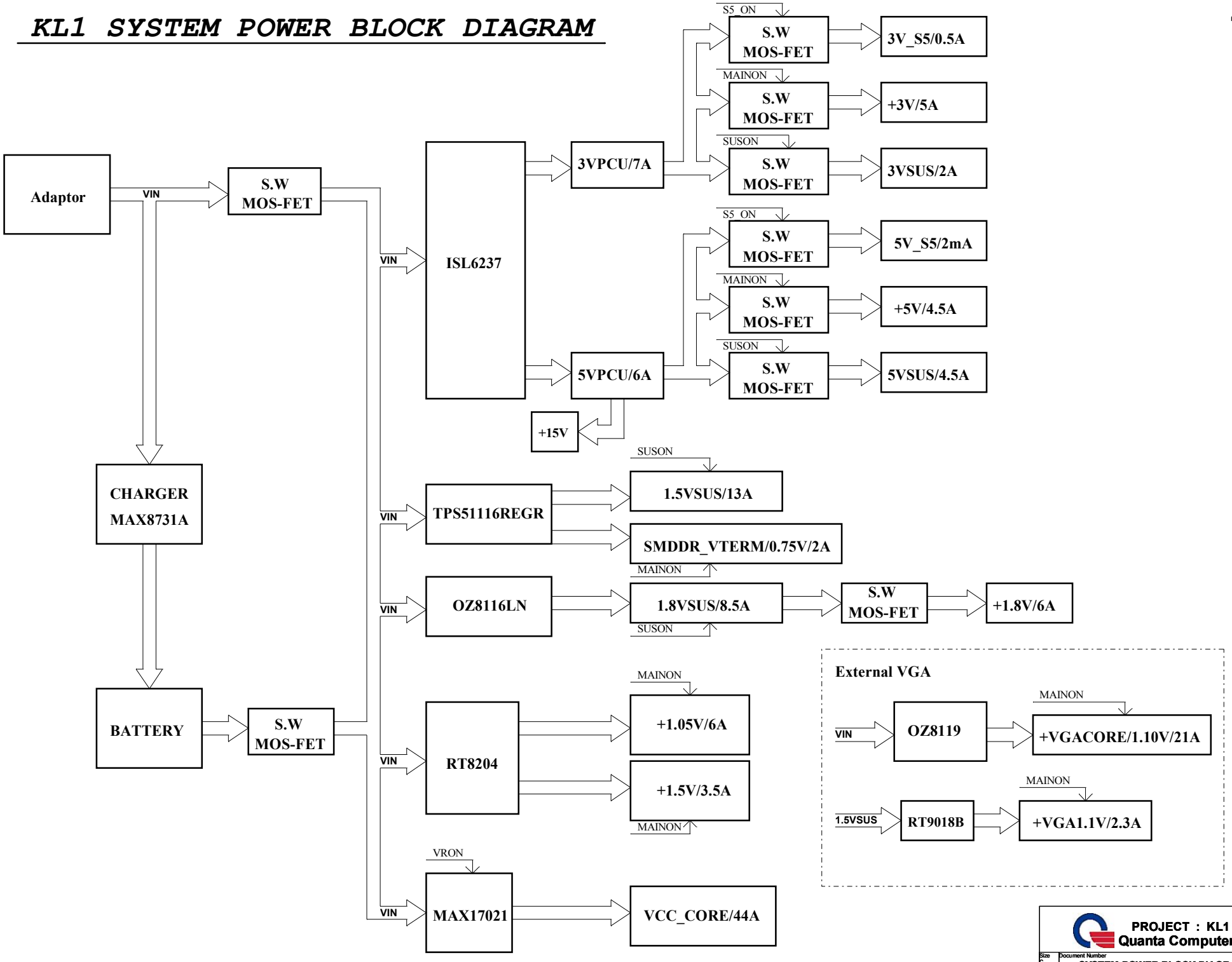
KL1 SYSTEM POWER BLOCK DIAGRAM



PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
C	SYSTEM POWER BLOCK DIAGRAM	MA

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