Compal Confidential

NAWE5 Schematics Document

AMD Danube

Champlain Processor with RS880M/SB820/Park VGA

2010-04-29

LA5753 REV: 1.A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/04/30	Title: Cover Page

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Model Name : AMD Danube + Park

ZZZ1 LA5753P
DAZ@
DA80000IK10
DAZ0E500100

POWER BD: (ZZZ2 LS-5751P @ DA40000PW10)
POWER BTN
NOVO BTN
POWER MANAGE BTN

CAP SENSOR BD: (ZZZ3 4 layer LS5756P @ DA40000T310)
VOLUME UP
VOLUME DOWN
MUTE
AUDIO ENHANCE
BUTTON & LED

CARD READER BD: (ZZZ4 LS5753P @ DA40000Q210)
RTS5159
HP JACK
MIC JACK

Danube

VRAM 512MB 64M16 x 4 page 18
DDR3
ATI Park - S3 uFCBGA-631 Page 13,14,15,16,17
PCI-Express x 16
Gen2

AMD S1G4 Processor uPGA-638 Package Champlain page 4,5,6,7
Hyper Transport Link 16 x 16
Memory BUS(DDR3) Dual Channel 1.5V DDRIII 800~1333MHz
204pin DDRIII-SO-DIMM X2 BANK 0, 1, 2, 3 page 8,9

ATI RS880M uFCBGA-528 page 10,11,12,13

Thermal Sensor ADM1032 page 6
Clock Generator ICS9LPRS488 page 19

LVDS page 27
CRT page 25
HDMI Conn. page 26

A link Express2 Gen1

ATI SB820M uFCBGA-605 page 20,21,22,23,24

page 37 USB PORT (LEFT) — USB port 0
page 37 USB conn (Right) — USB port 12
page 27 CMOS Camera — USB port 5
page 37 Bluetooth Conn <Option> — USB port 6
page 28 Mini card (WL)X1 — USB port 11
page 28 3G/GPS WWAN <Option> — USB port 10
page 28 New Card — USB port 7

3.3V 48MHz
USB

S-ATA Gen2

3.3V 24.576MHz/48Mhz
HD Audio

New Card WLAN page 28 — GPP3
3G/WWAN MINI Card page 28 — GPP2
MINI Card WLAN page 28 — GPP1
LAN(GbE) Atheros AR8151/8152 page 29 — GPP0
SIM Card page28
USB (WWAN)
RJ45 page 30

SATA HDD Conn. page 32 — port 0
CDROM Conn. page 32 — port 1
ESATA & USB Combine CON — USB port 4 page28

LPC BUS

ENE KB926 page 34
Touch Pad page 35
Int.KBD page 35
BIOS page 34

Audio Codec Realtec ALC259 page33
Analog MIC_Int page33
2Channel Speaker page33

USB port 2
Card Reader / Audio Jack SB CONN page38
RTS5159-GR
MS/MS
pro/SD/SD
pro/mmc/XD
HP X 1+
MIC_Ext X1

LED page 36
LID SW / IO BD page 32
Power On/Off CKT. page 32
DC/DC Interface CKT. page 38
Fan Control page 31
Power Circuit page 39,40,41,42,43,44,45,46,47,48,49

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.75VS	+0.75VS LDO power rail for DDR3 VTT	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
EMC1402-1 (CPU)	100_1100b	4CH
EMC1412-A (GPU)	111_1100b	7CH
TMP411C (GPU)	100_1110b	4EH
EMC1403-2 (DDR,WWAN)	100_1101b	4DH

SB820 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94

SB820 SM Bus 1 address

Device	Address

BOM Config

EXT CLK Mode:EXT@
INT CLK mode:INT@
UMA only SKU: UMA@
DIS ONLY (Park S3): DIS@
LAN GIGA: 8151@
CMOS@
BT@
3G@
S@
H@
LAN 100: 8152@
ESATA@
HDMI@+HDMI_UMA@
HDMI@+HDMI_DIS@
Express Card: EXP@
KB_LED: E7@

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Title: Notes List			
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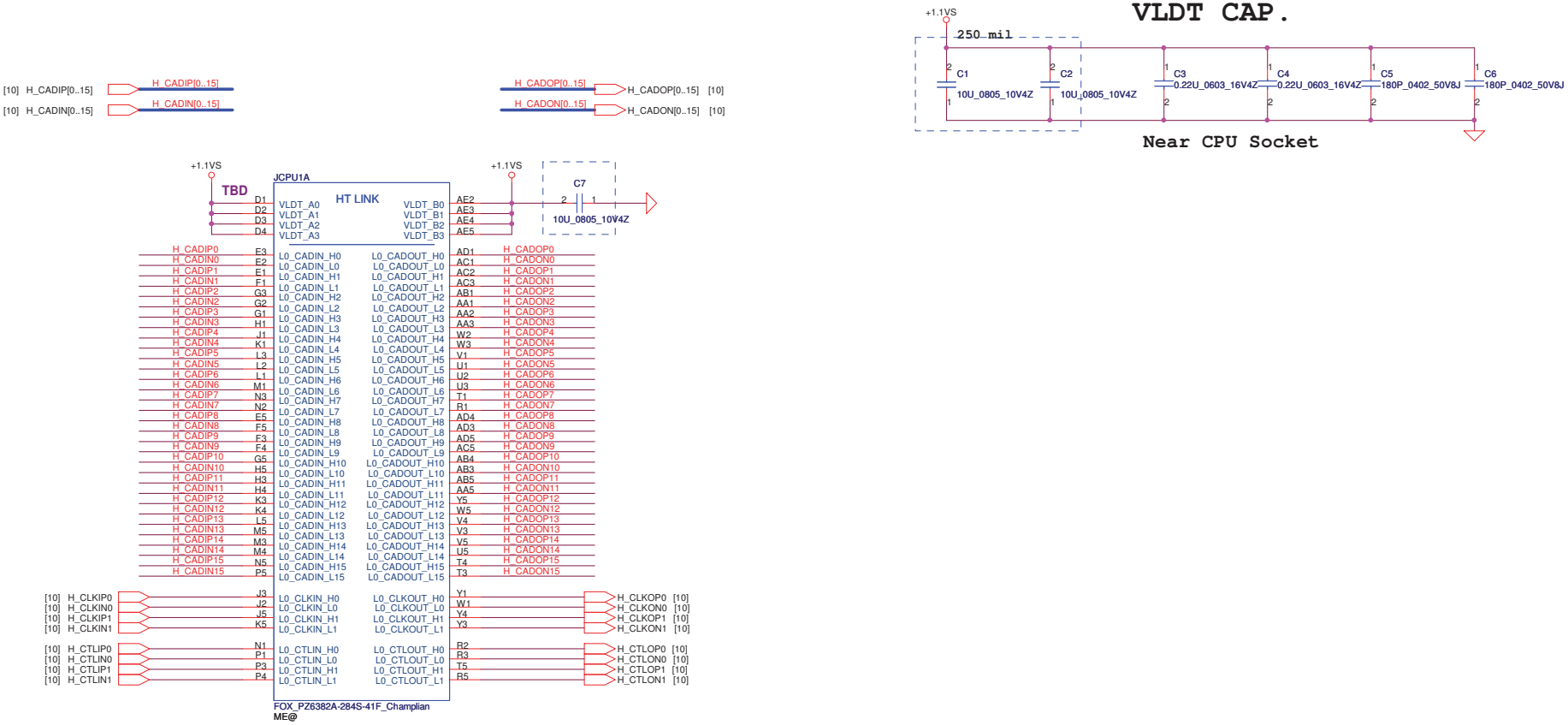

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/04/30	Title AMD CPU S1G4 HT I/F
Size Custom	Document Number NAWE5 LA-5753P		Rev 1.A
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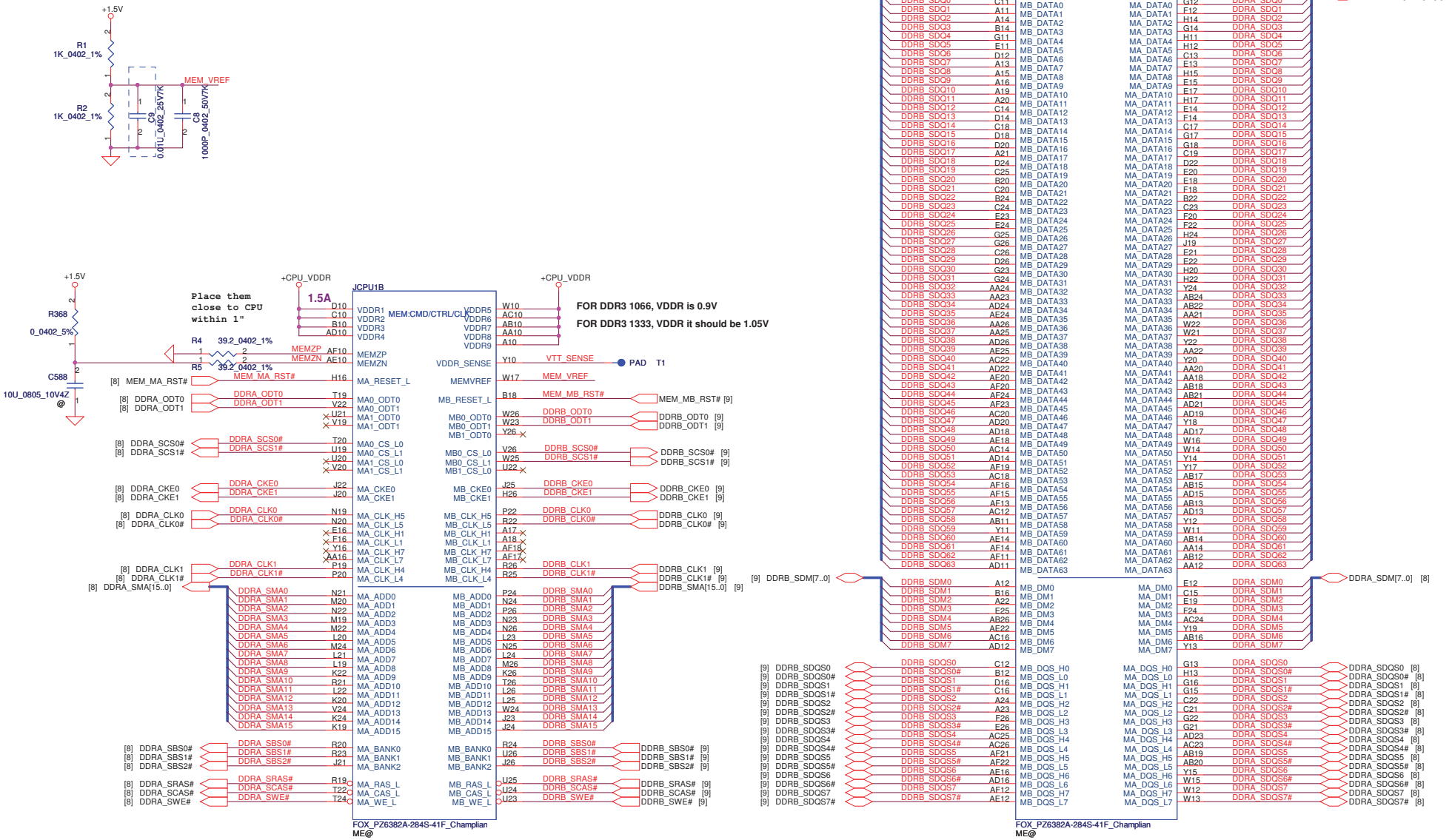
Processor DDR3 Memory Interface



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Title: AMD CPU S1G4 DDRII I/F

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Champlain: C1E
C1E: LDT_REQ# no connect
CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
no support in S1g4

VDDA=0.25A

JCPU1D

FOX_PZ6382A-284S-41F_Champlian
ME@

PROCHOT:
Input: For HTC Function
Output: Over Temperature Condition

For SCAN connect use

R1A

TI
TMP411ADGKR MSOP 8P
SA00002DE10
Address: 100 1100

EMC1402-1
(SA00001Z700)
Address 100_1100b
S IC EMC1402-1-ACZL-TR MSOP 8P SENSOR

EMC1402-1-ACZL-TR-MSOP-8P

CPU internal thermal sensor

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

2.09V for Gate

ACES_87212-12G0
ME@

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Title: AMD CPU S1G4 CTRL

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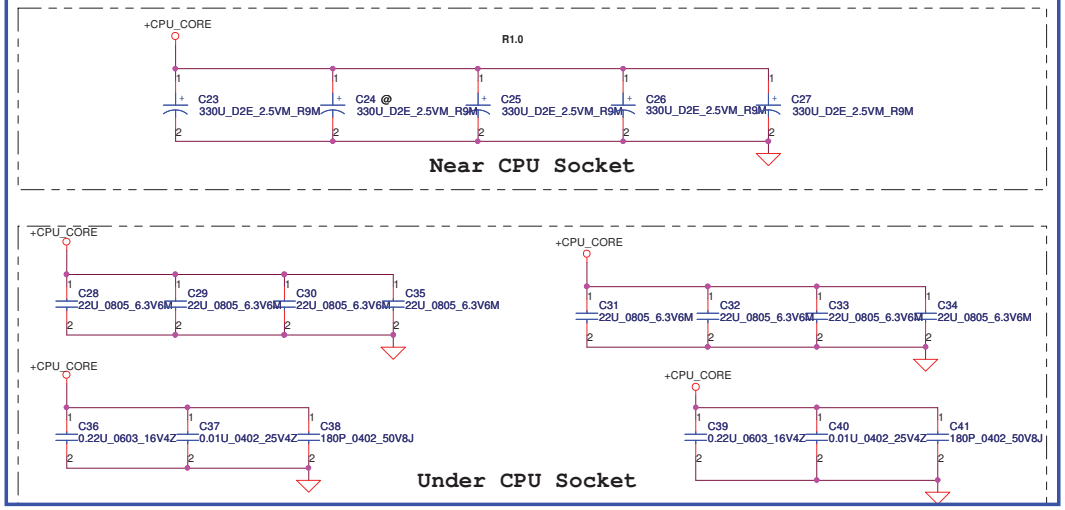
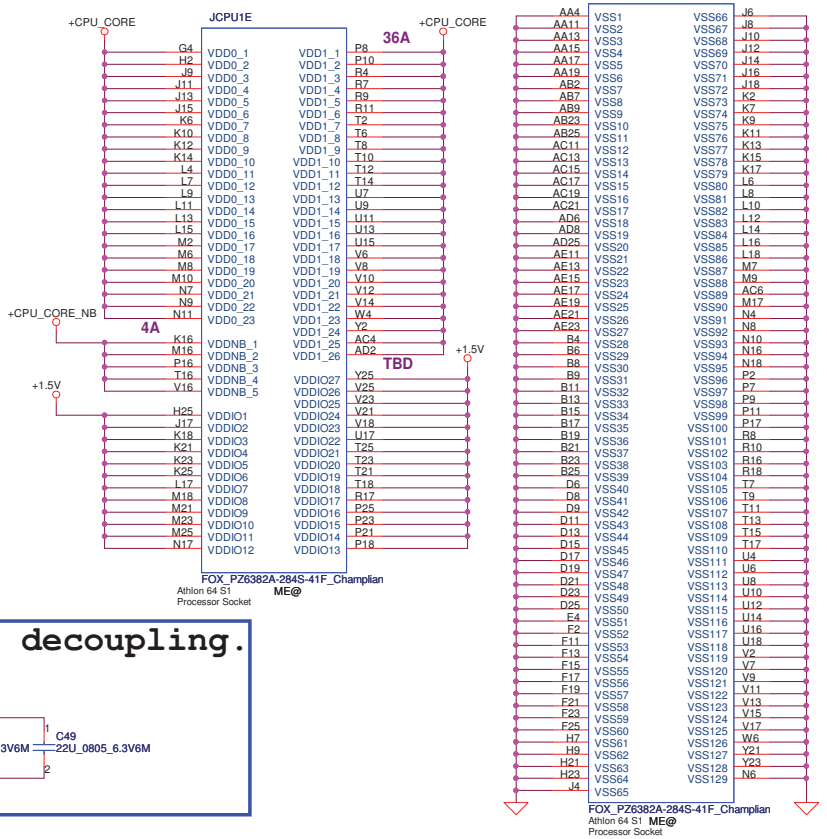
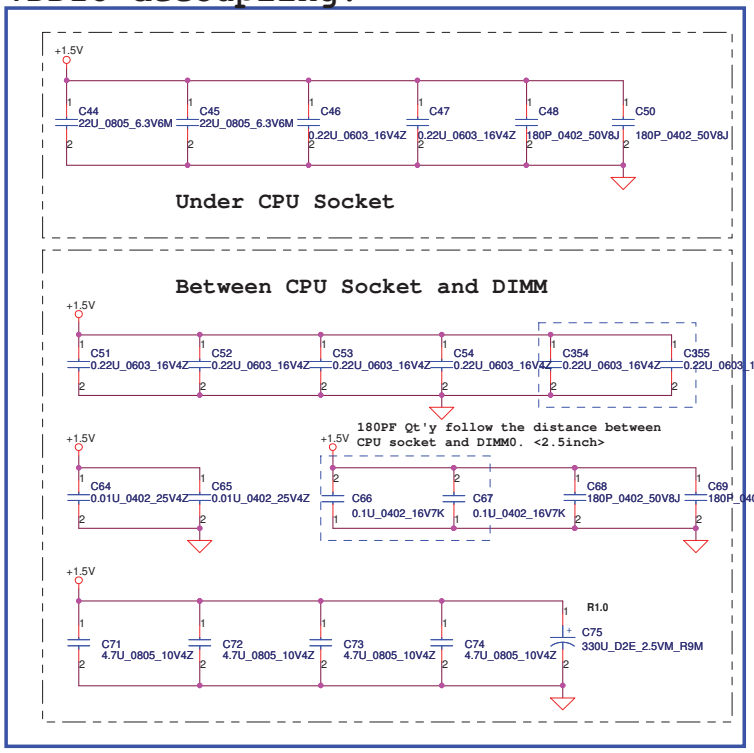
VDD(+CPU_CORE) decoupling.

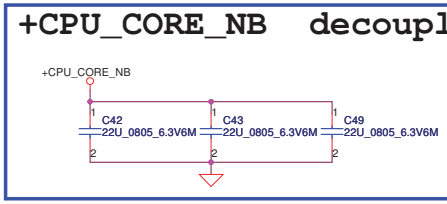




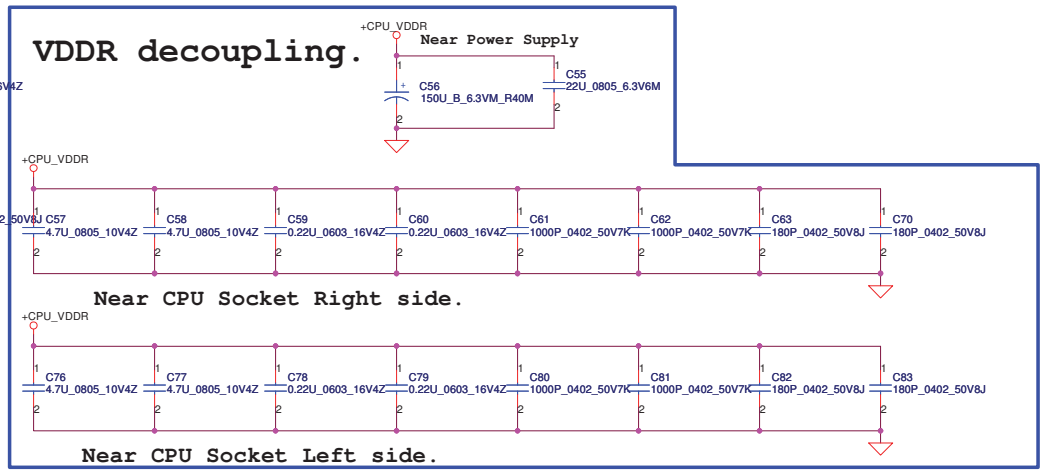
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VDDR decoupling.



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Compal Electronics, Inc.	
Title	AMD CPU S1G4 PWR & GND
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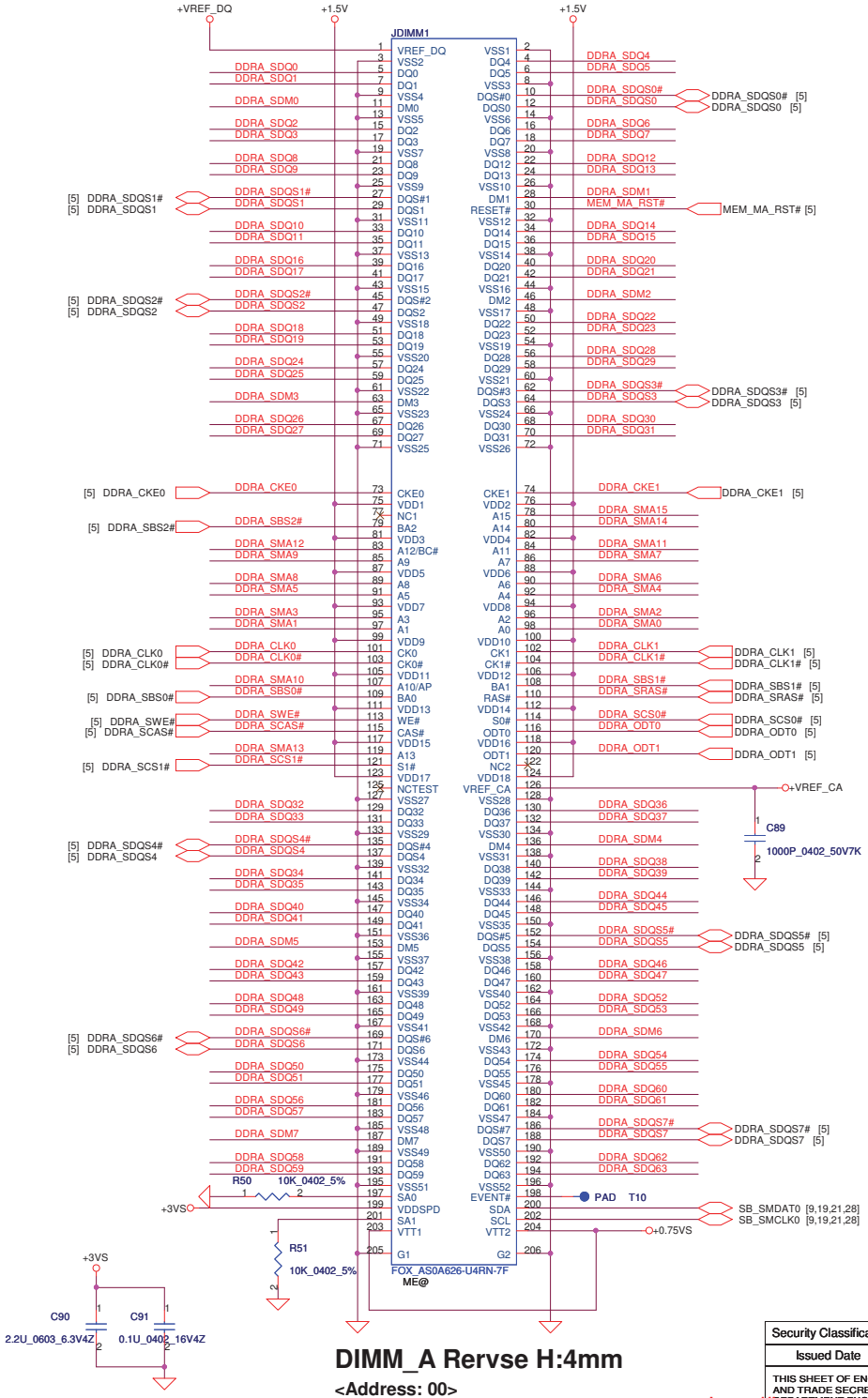

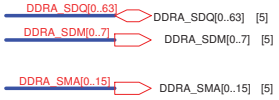

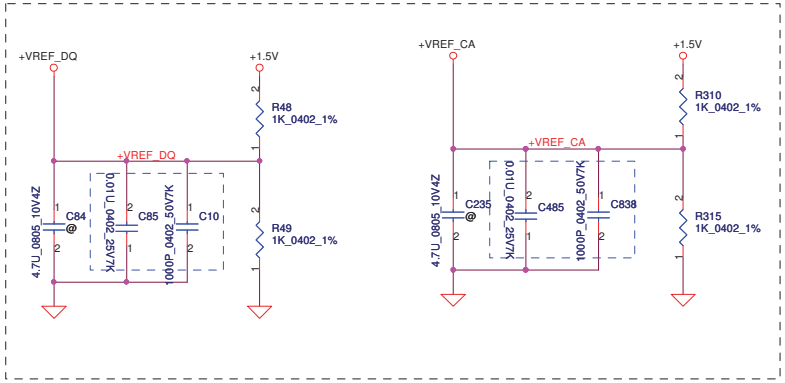

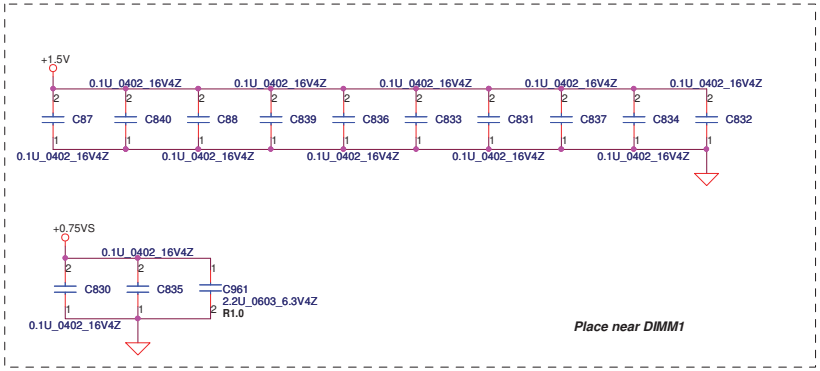

DIMM_A Rervse H:4mm

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Compal Electronics, Inc.

Title: DDRII SO-DIMM 1

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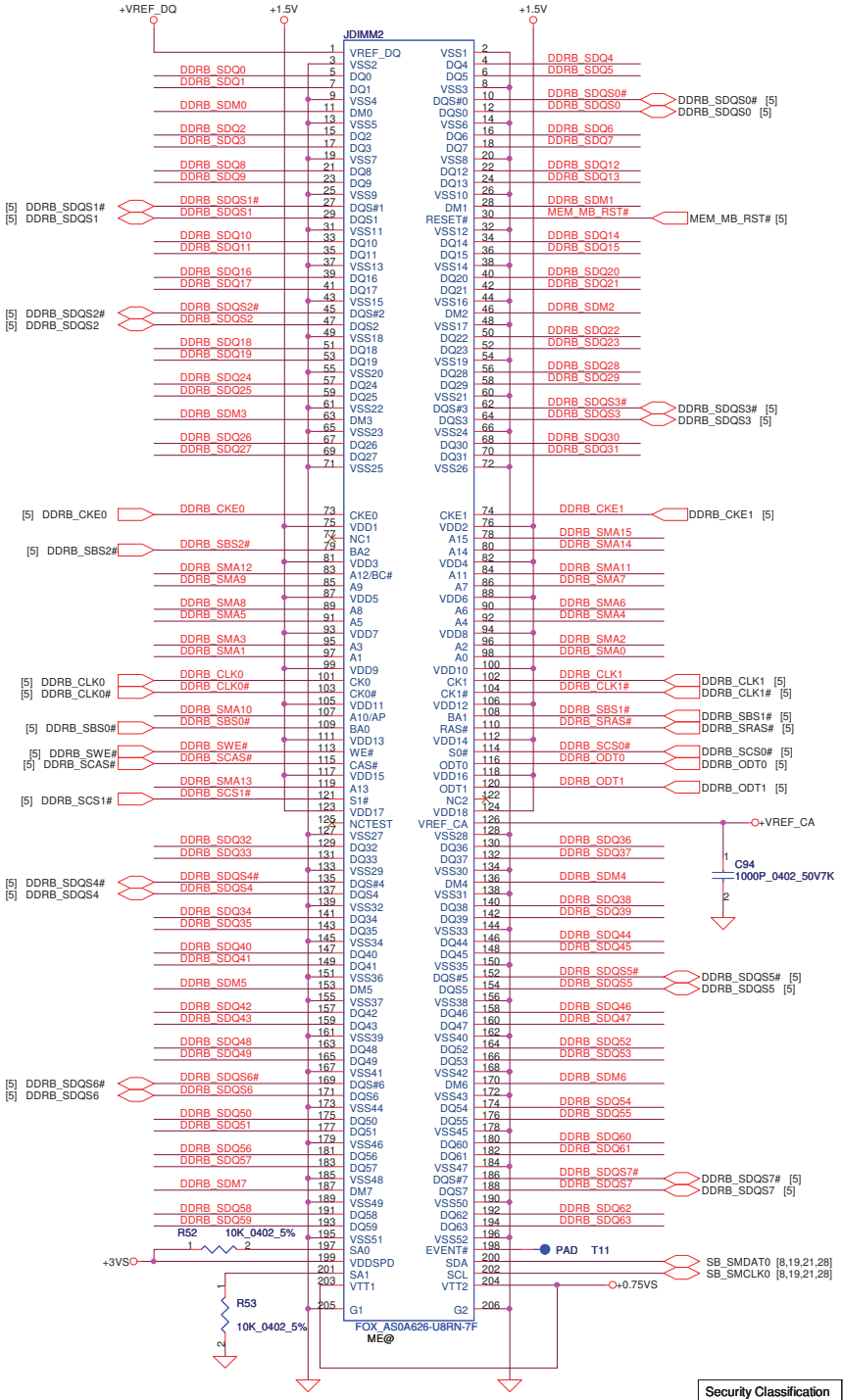

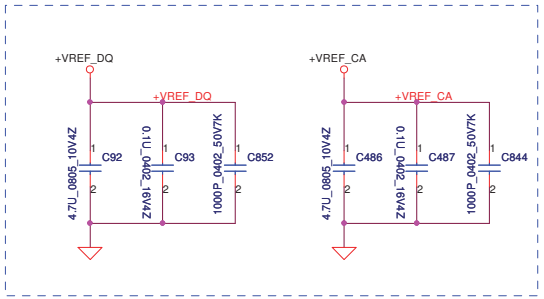

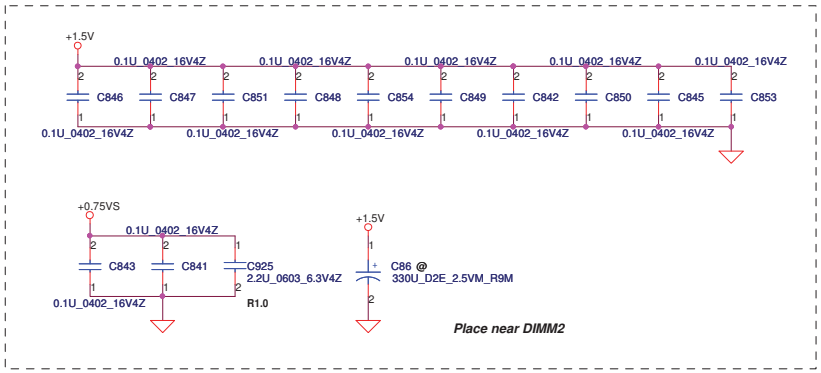

DIMM_B Reverse H:8mm

<Address: 01>

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Compal Electronics, Inc.			
Title: DDRII SO-DIMM 2			
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[13] PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]
[13] PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] [13]
PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] [13]

UMA HDMI

R1.0

PCIE_MTX_GRX_P0		C488 1	2 0.1U_0402_16V7K	UMA_HDMI_P0 [26]
PCIE_MTX_GRX_N0	C489 1	2 0.1U_0402_16V7K	HDMI_UMA@	UMA_HDMI_N0 [26]
PCIE_MTX_GRX_P1		HDMI_UMA@ C491 1	2 0.1U_0402_16V7K	UMA_HDMI_P1 [26]
PCIE_MTX_GRX_N1	C490 1	2 0.1U_0402_16V7K	HDMI_UMA@	UMA_HDMI_N1 [26]
PCIE_MTX_GRX_P2		HDMI_UMA@ C497 1	2 0.1U_0402_16V7K	UMA_HDMI_P2 [26]
PCIE_MTX_GRX_N2	C500 1	2 0.1U_0402_16V7K	HDMI_UMA@	UMA_HDMI_N2 [26]
PCIE_MTX_GRX_P3		HDMI_UMA@ C499 1	2 0.1U_0402_16V7K	UMA_HDMI_P3 [26]
PCIE_MTX_GRX_N3	C498 1	2 0.1U_0402_16V7K	HDMI_UMA@	UMA_HDMI_N3 [26]
		HDMI_UMA@		

Cap close NB

U3B — PART 2 OF 6 — PCIE I/F GFX

PCIE_GTX_C_MRX_P0	D4	GFX_RX0P	GFX_TX0P	A5	PCIE_MTX_GRX_P0 C95 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P0
PCIE_GTX_C_MRX_N0	C4	GFX_RX0N	GFX_TX0N	B5	PCIE_MTX_GRX_N0 C96 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N0
PCIE_GTX_C_MRX_P1	A3	GFX_RX1P	GFX_TX1P	A4	PCIE_MTX_GRX_P1 C97 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P1
PCIE_GTX_C_MRX_N1	B3	GFX_RX1N	GFX_TX1N	B4	PCIE_MTX_GRX_N1 C98 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N1
PCIE_GTX_C_MRX_P2	C2	GFX_RX2P	GFX_TX2P	C3	PCIE_MTX_GRX_P2 C99 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P2
PCIE_GTX_C_MRX_N2	C1	GFX_RX2N	GFX_TX2N	B2	PCIE_MTX_GRX_N2 C100 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N2
PCIE_GTX_C_MRX_P3	E5	GFX_RX3P	GFX_TX3P	D1	PCIE_MTX_GRX_P3 C101 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P3
PCIE_GTX_C_MRX_N3	F5	GFX_RX3N	GFX_TX3N	D2	PCIE_MTX_GRX_N3 C102 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N3
PCIE_GTX_C_MRX_P4	G5	GFX_RX4P	GFX_TX4P	E2	PCIE_MTX_GRX_P4 C103 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P4
PCIE_GTX_C_MRX_N4	G6	GFX_RX4N	GFX_TX4N	E1	PCIE_MTX_GRX_N4 C104 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N4
PCIE_GTX_C_MRX_P5	H5	GFX_RX5P	GFX_TX5P	F4	PCIE_MTX_GRX_P5 C105 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P5
PCIE_GTX_C_MRX_N5	H6	GFX_RX5N	GFX_TX5N	F3	PCIE_MTX_GRX_N5 C106 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N5
PCIE_GTX_C_MRX_P6	J6	GFX_RX6P	GFX_TX6P	F1	PCIE_MTX_GRX_P6 C107 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P6
PCIE_GTX_C_MRX_N6	J5	GFX_RX6N	GFX_TX6N	F2	PCIE_MTX_GRX_N6 C108 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N6
PCIE_GTX_C_MRX_P7	J7	GFX_RX7P	GFX_TX7P	H4	PCIE_MTX_GRX_P7 C109 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P7
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PCIE_GTX_C_MRX_P8	L5	GFX_RX8P	GFX_TX8P	H1	PCIE_MTX_GRX_P8 C111 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P8
PCIE_GTX_C_MRX_N8	L6	GFX_RX8N	GFX_TX8N	H2	PCIE_MTX_GRX_N8 C112 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N8
PCIE_GTX_C_MRX_P9	M8	GFX_RX9P	GFX_TX9P	J2	PCIE_MTX_GRX_P9 C113 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P9
PCIE_GTX_C_MRX_N9	L8	GFX_RX9N	GFX_TX9N	J1	PCIE_MTX_GRX_N9 C114 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N9
PCIE_GTX_C_MRX_P10	P7	GFX_RX10P	GFX_TX10P	K4	PCIE_MTX_GRX_P10 C115 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P10
PCIE_GTX_C_MRX_N10	M7	GFX_RX10N	GFX_TX10N	K3	PCIE_MTX_GRX_N10 C116 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N10
PCIE_GTX_C_MRX_P11	P5	GFX_RX11P	GFX_TX11P	K1	PCIE_MTX_GRX_P11 C117 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P11
PCIE_GTX_C_MRX_N11	M5	GFX_RX11N	GFX_TX11N	K2	PCIE_MTX_GRX_N11 C118 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N11
PCIE_GTX_C_MRX_P12	R8	GFX_RX12P	GFX_TX12P	M4	PCIE_MTX_GRX_P12 C119 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P12
PCIE_GTX_C_MRX_N12	P8	GFX_RX12N	GFX_TX12N	M3	PCIE_MTX_GRX_N12 C120 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N12
PCIE_GTX_C_MRX_P13	R6	GFX_RX13P	GFX_TX13P	M1	PCIE_MTX_GRX_P13 C121 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P13
PCIE_GTX_C_MRX_N13	R5	GFX_RX13N	GFX_TX13N	M2	PCIE_MTX_GRX_N13 C122 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N13
PCIE_GTX_C_MRX_P14	P4	GFX_RX14P	GFX_TX14P	N2	PCIE_MTX_GRX_P14 C123 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P14
PCIE_GTX_C_MRX_N14	P3	GFX_RX14N	GFX_TX14N	N1	PCIE_MTX_GRX_N14 C124 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N14
PCIE_GTX_C_MRX_P15	T4	GFX_RX15P	GFX_TX15P	P1	PCIE_MTX_GRX_P15 C125 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P15
PCIE_GTX_C_MRX_N15	T3	GFX_RX15N	GFX_TX15N	P2	PCIE_MTX_GRX_N15 C126 1 2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N15

PCIE I/F GPP

	AE3	GPP_RX0P	GPP_TX0P	AC1	
	AD4	GPP_RX0N	GPP_TX0N	AC2	
[28] PCIE_PTX_C_IRX_P1	AE2	GPP_RX1P	GPP_TX1P	AB4	PCIE_ITX_PRX_P1 C201 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P1 [28] WLAN
[28] PCIE_PTX_C_IRX_N1	AD3	GPP_RX1N	GPP_TX1N	AB3	PCIE_ITX_PRX_N1 C200 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N1 [28]
[29] PCIE_PTX_C_IRX_P2	AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_ITX_PRX_P2 C482 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P2 [29] GLAN
[29] PCIE_PTX_C_IRX_N2	AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_ITX_PRX_N2 C481 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N2 [29]
[28] PCIE_PTX_C_IRX_P3	V5	GPP_RX3P	GPP_TX3P	Y1	PCIE_ITX_PRX_P3 C484 1 2 3G@ 0.1U_0402_16V7K PCIE_ITX_C_PRX_P3 [28] WWAN
[28] PCIE_PTX_C_IRX_N3	W6	GPP_RX3N	GPP_TX3N	Y2	PCIE_ITX_PRX_N3 C483 1 2 3G@ 0.1U_0402_16V7K PCIE_ITX_C_PRX_N3 [28] WWAN
	U5	GPP_RX4P	GPP_TX4P	Y4	
	U6	GPP_RX4N	GPP_TX4N	Y3	
	U8	GPP_RX5P	GPP_TX5P	V1	
	U7	GPP_RX5N	GPP_TX5N	V2	

PCIE I/F SB

[20] SB_RX0P	AA8	SB_RX0P	SB_TX0P	AD7	SB_TX0P_C C133 1 2 0.1U_0402_16V7K SB_TX0P [20]
[20] SB_RX0N	Y8	SB_RX0N	SB_TX0N	AE7	SB_TX0N_C C134 1 2 0.1U_0402_16V7K SB_TX0N [20]
[20] SB_RX1P	AA7	SB_RX1P	SB_TX1P	AE6	SB_TX1P_C C135 1 2 0.1U_0402_16V7K SB_TX1P [20]
[20] SB_RX1N	Y7	SB_RX1N	SB_TX1N	AD6	SB_TX1N_C C136 1 2 0.1U_0402_16V7K SB_TX1N [20]
[20] SB_RX2P	AA5	SB_RX2P	SB_TX2P	AB6	SB_TX2P_C C137 1 2 0.1U_0402_16V7K SB_TX2P [20]
[20] SB_RX2N	AA6	SB_RX2N	SB_TX2N	AC6	SB_TX2N_C C138 1 2 0.1U_0402_16V7K SB_TX2N [20]
[20] SB_RX3P	W5	SB_RX3P	SB_TX3P	AD5	SB_TX3P_C C139 1 2 0.1U_0402_16V7K SB_TX3P [20]
[20] SB_RX3N	Y5	SB_RX3N	SB_TX3N	AE5	SB_TX3N_C C140 1 2 0.1U_0402_16V7K SB_TX3N [20]

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AC8 — R59 1 2 1.27K_0402_1%
AB8 — R58 1 2 2K_0402_1% — +1.1VS

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RS880 A11(SA000032710)

[4] H_CADOP[0..15] → H_CADOP[0..15]
[4] H_CADON[0..15] → H_CADON[0..15]
H_CADIP[0..15] → H_CADIP[0..15] [4]
H_CADIN[0..15] → H_CADIN[0..15] [4]

U3A — PART 1 OF 6 — HYPER TRANSPORT CPU I/F

H_CADOP0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	H_CADIP0
H_CADON0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	H_CADIN0
H_CADOP1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	H_CADIP1
H_CADON1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	H_CADIN1
H_CADOP2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	H_CADIP2
H_CADON2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	H_CADIN2
H_CADOP3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	H_CADIP3
H_CADON3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	H_CADIN3
H_CADOP4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	H_CADIP4
H_CADON4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	H_CADIN4
H_CADOP5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	H_CADIP5
H_CADON5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	H_CADIN5
H_CADOP6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	H_CADIP6
H_CADON6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	H_CADIN6
H_CADOP7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	H_CADIP7
H_CADON7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	H_CADIN7
H_CADOP8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	H_CADIP8
H_CADON8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	H_CADIN8
H_CADOP9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	H_CADIP9
H_CADON9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	H_CADIN9
H_CADOP10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	H_CADIP10
H_CADON10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	H_CADIN10
H_CADOP11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	H_CADIP11
H_CADON11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	H_CADIN11
H_CADOP12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	H_CADIP12
H_CADON12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	H_CADIN12
H_CADOP13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	H_CADIP13
H_CADON13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	H_CADIN13
H_CADOP14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	H_CADIP14
H_CADON14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	H_CADIN14
H_CADOP15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	H_CADIP15
H_CADON15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	H_CADIN15

[4] H_CLKOP0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	H_CLKIP0 [4]
[4] H_CLKON0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	H_CLKIN0 [4]
[4] H_CLKOP1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	H_CLKIP1 [4]
[4] H_CLKON1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	H_CLKIN1 [4]
[4] H_CTLOP0	H_CTLOP0 M22	HT_RXCTL0P	HT_TXCTL0P	M24	H_CTLIP0 H_CTLIP0 [4]
[4] H_CTLON0	H_CTLON0 M23	HT_RXCTL0N	HT_TXCTL0N	M25	H_CTLIN0 H_CTLIN0 [4]
[4] H_CTLOP1	H_CTLOP1 R21	HT_RXCTL1P	HT_TXCTL1P	P19	H_CTLIP1 H_CTLIP1 [4]
[4] H_CTLON1	H_CTLON1 R20	HT_RXCTL1N	HT_TXCTL1N	R18	H_CTLIN1 H_CTLIN1 [4]
	R60 1 2	HT_RXCALP C23	HT_TXCALP	B24	HT_TXCALP 1 R61 2
	301_0402_1%	HT_RXCALN A24	HT_TXCALN	B25	HT_TXCALN 301_0402_1%
	Place within 1" layout 1:2	HT_RXCALP	HT_TXCALP		Place within 1" layout 1:2
		HT_RXCALN	HT_TXCALN		

RS880M_FCBGA528

RS880 A11(SA000032710)

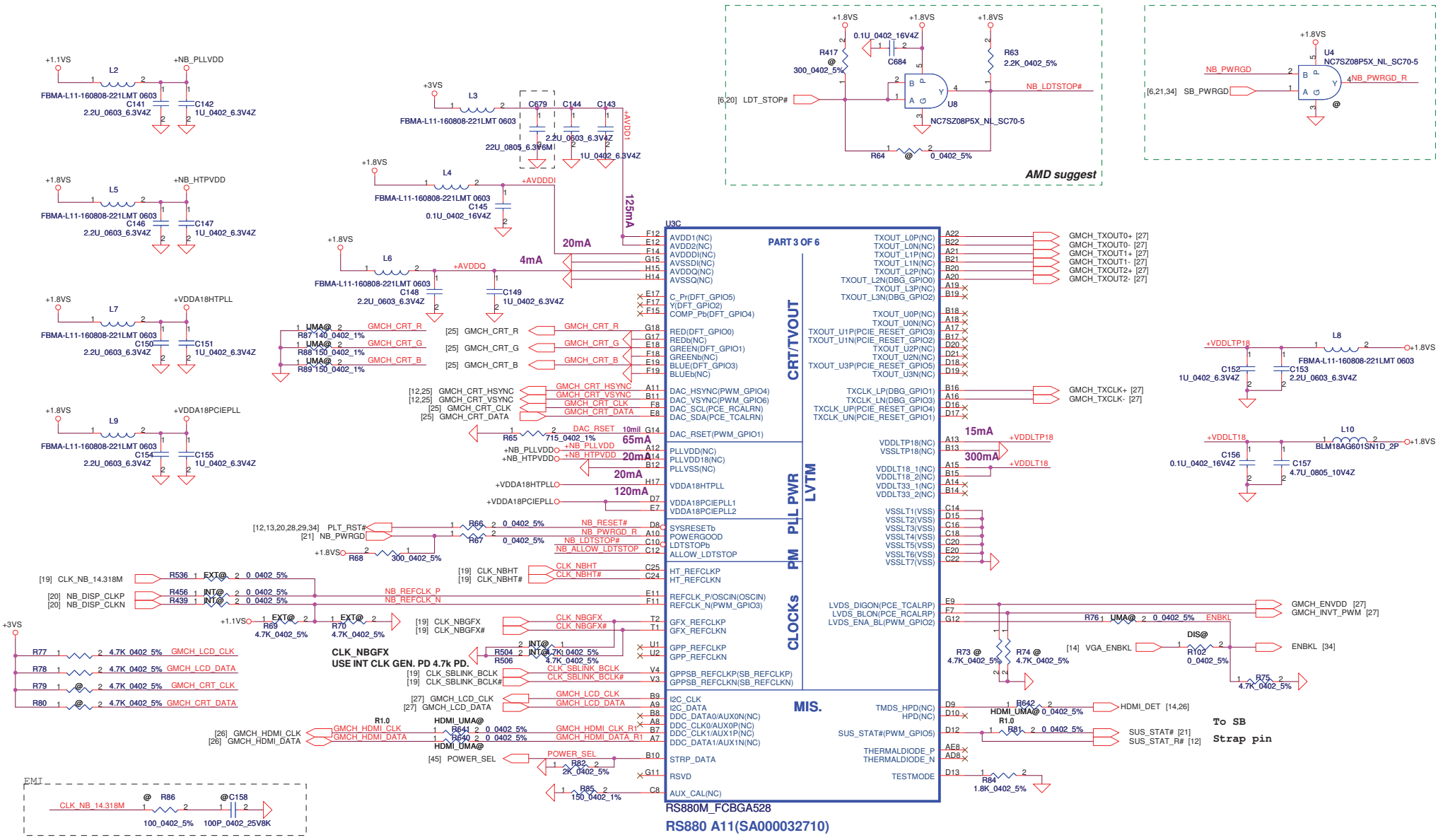
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: RS880-HT/PCIE

Size: B2B Custom | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 10 of 48



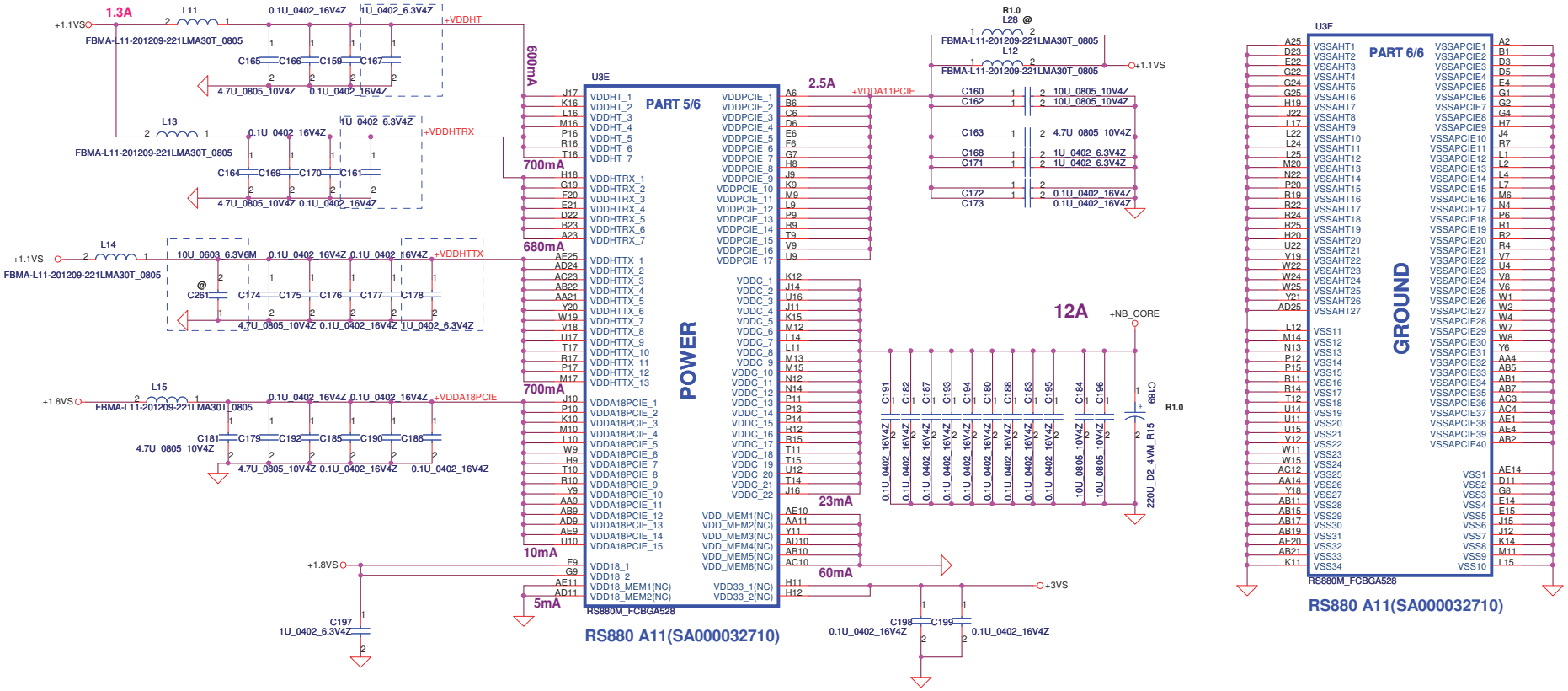
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: RS880 VEDIO/CLK GEN

Size	Document Number	Rev
B/28 Custom	NAWE5 LA-5753P	1.A

Date: Tuesday, May 18, 2010 | Sheet 11 of 48



Side port and Strap setting

Debug Mode

[11,25] GMCH_CRT_VSYNC — R92 3K_0402_5% — +3VS; R93 @ 3K_0402_5%

Load EEPROM Strap

[11] SUS_STAT_R# — D1 @ CH751H-40PT_SOD323-2 — PLT_RST# [11,13,20,28,29,34]; R264 @ 3K_0402_5%

Enable Side Port Memory

[11,25] GMCH_CRT_HSYNC — R94 3K_0402_5% — +3VS; R95 @ 3K_0402_5%

DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

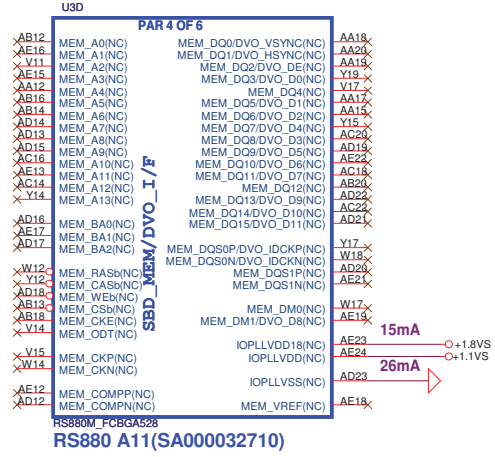
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

Enable Side Port Memory

```
RS880: HSYNC#
0:   Enable        Register Readback of strap:
1 :  Disable       NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: RS880 PWR/GND

Size: B/28 Custom | Document Number: NAWE5 LA-5753P | Rev: 1.A

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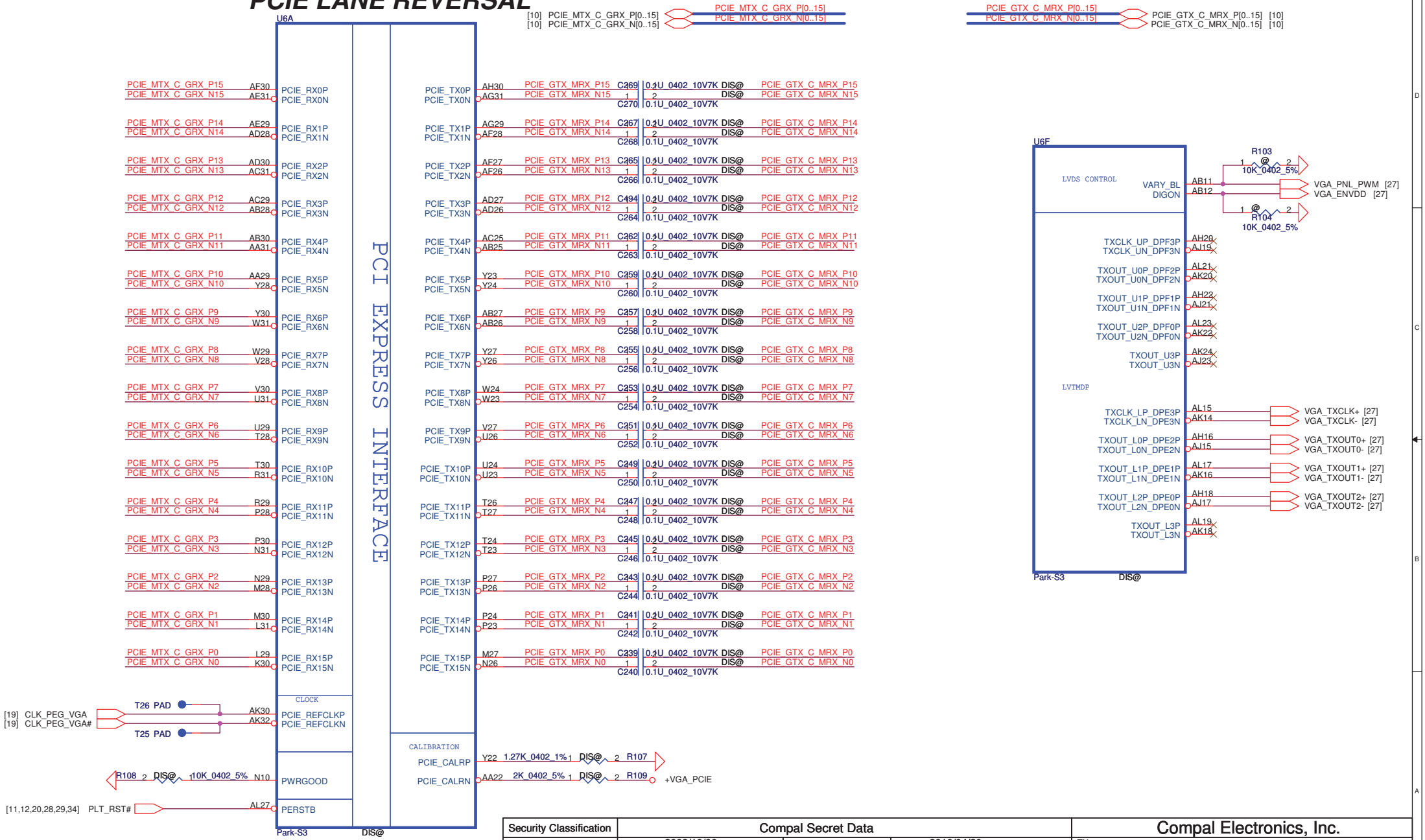
PCIE LANE REVERSAL



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: PARK-S3 PCIE/LVDS

Size	Document Number	Rev
Custom	NAWE5 LA-5753P	1.A

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TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
	GPIO8		0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

STRAPS

GPU_GPIO0 R111 10K_0402_5%
GPU_GPIO1 R112 10K_0402_5%
GPU_GPIO2 R113 10K_0402_5%
GPU_GPIO8 R114 10K_0402_5%
GPU_GPIO9 R115 10K_0402_5%
GPU_GPIO11 R117 10K_0402_5%
GPU_GPIO12 R118 10K_0402_5%
GPU_GPIO13 R119 10K_0402_5%
R120;R121 NC on PAWE7&PAWE8 DIS
VGA_CRT_HSYNC R120 10K_0402_5%
VGA_CRT_VSYNC R121 10K_0402_5%
VGA_CRT_VSYNC2 R122 10K_0402_5%
VGA_CRT_HSYNC2 R123 10K_0402_5%

VGA Thermal Sensor ADM1032 Closed to GPU

TMP411C (GPU)
100_1110b

EMC1412-A (SA00003YA00)
Address 1111_100xb
S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

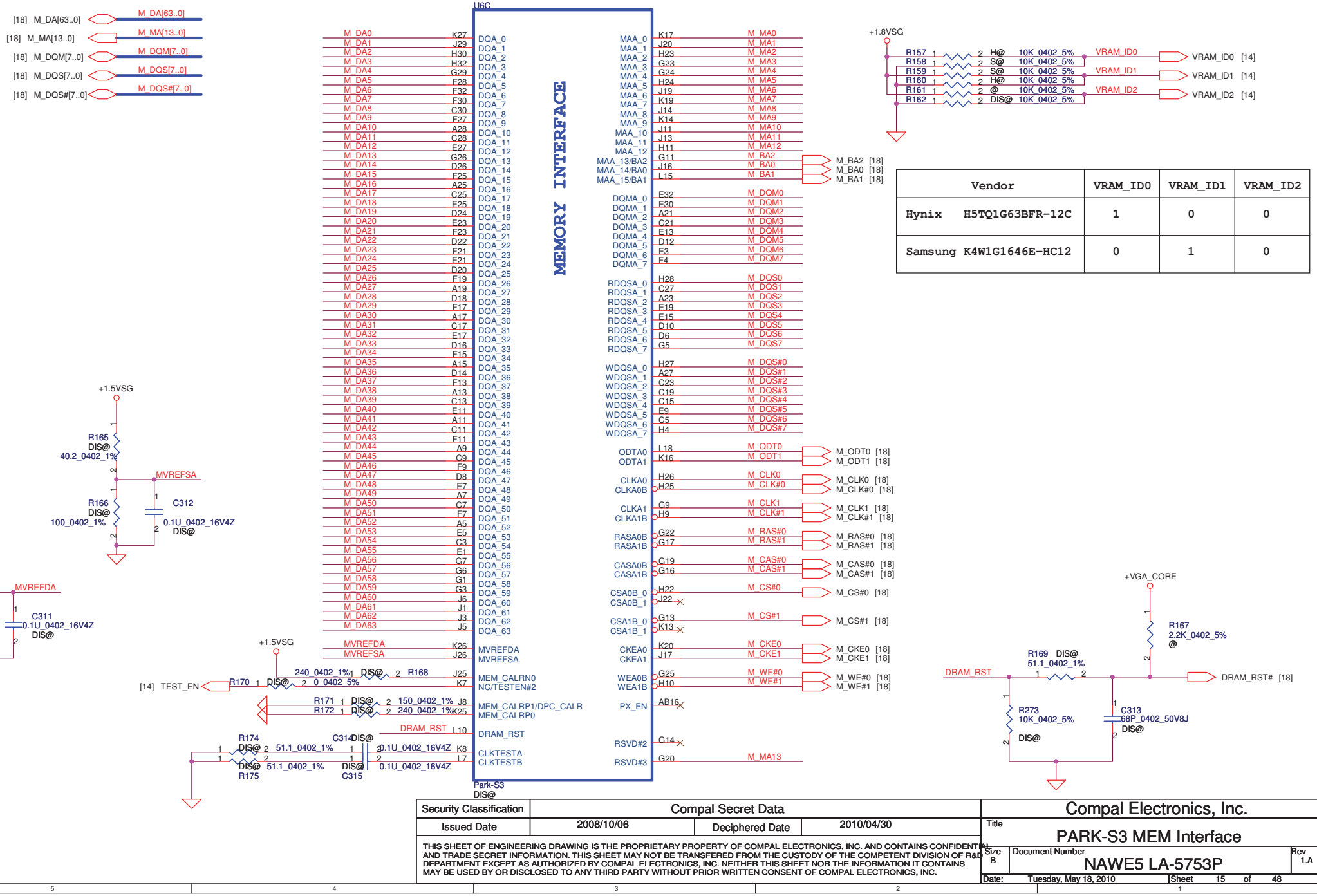
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: PARK-S3 Main Generic/MSIC

Size	Document Number	Rev
C	NAWE5 LA-5753P	1.A

Date: Tuesday, May 18, 2010 Sheet 14 of 48

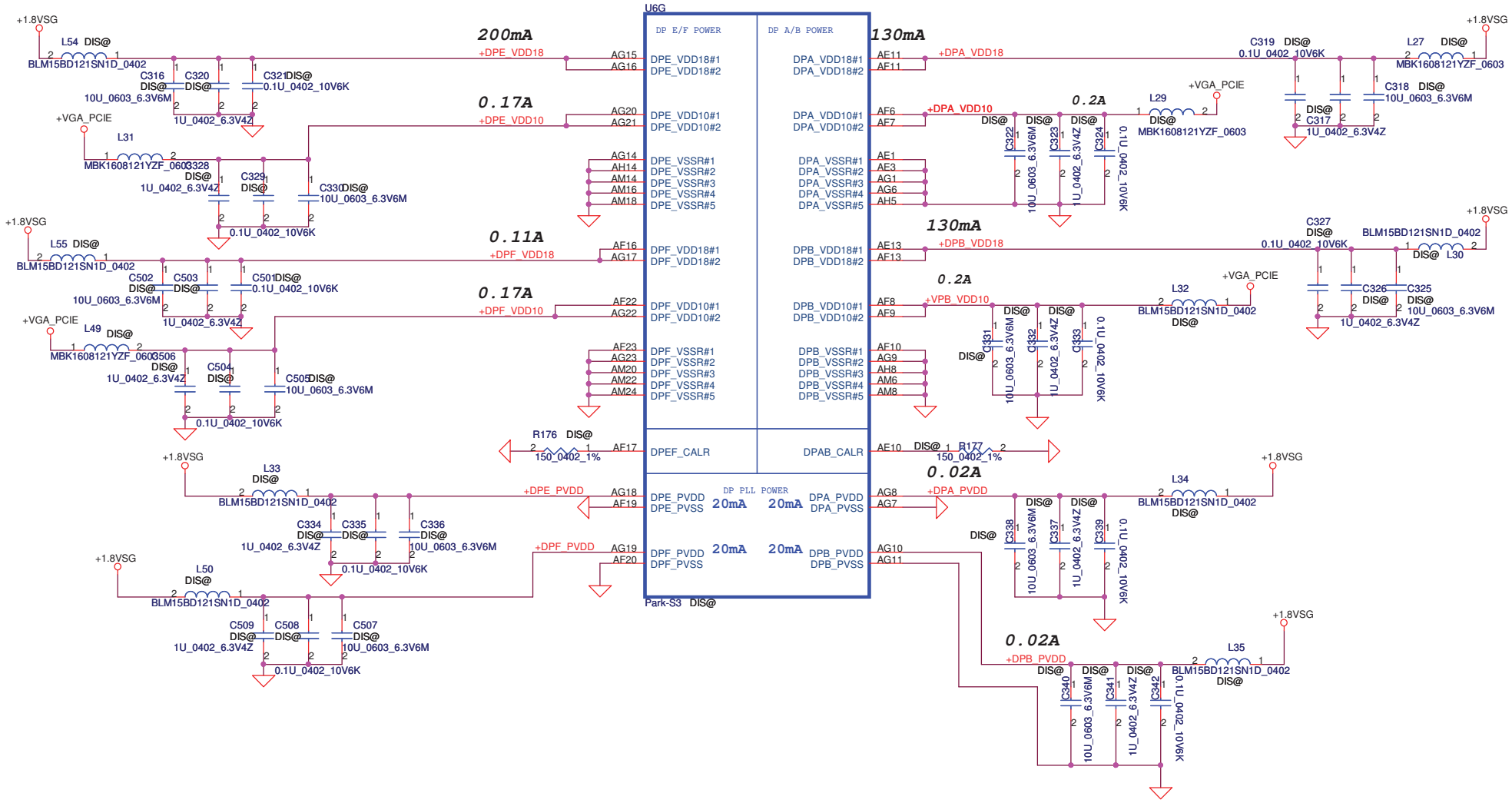


Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix H5TQ1G63BFR-12C	1	0	0
Samsung K4W1G1646E-HC12	0	1	0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2010/04/30

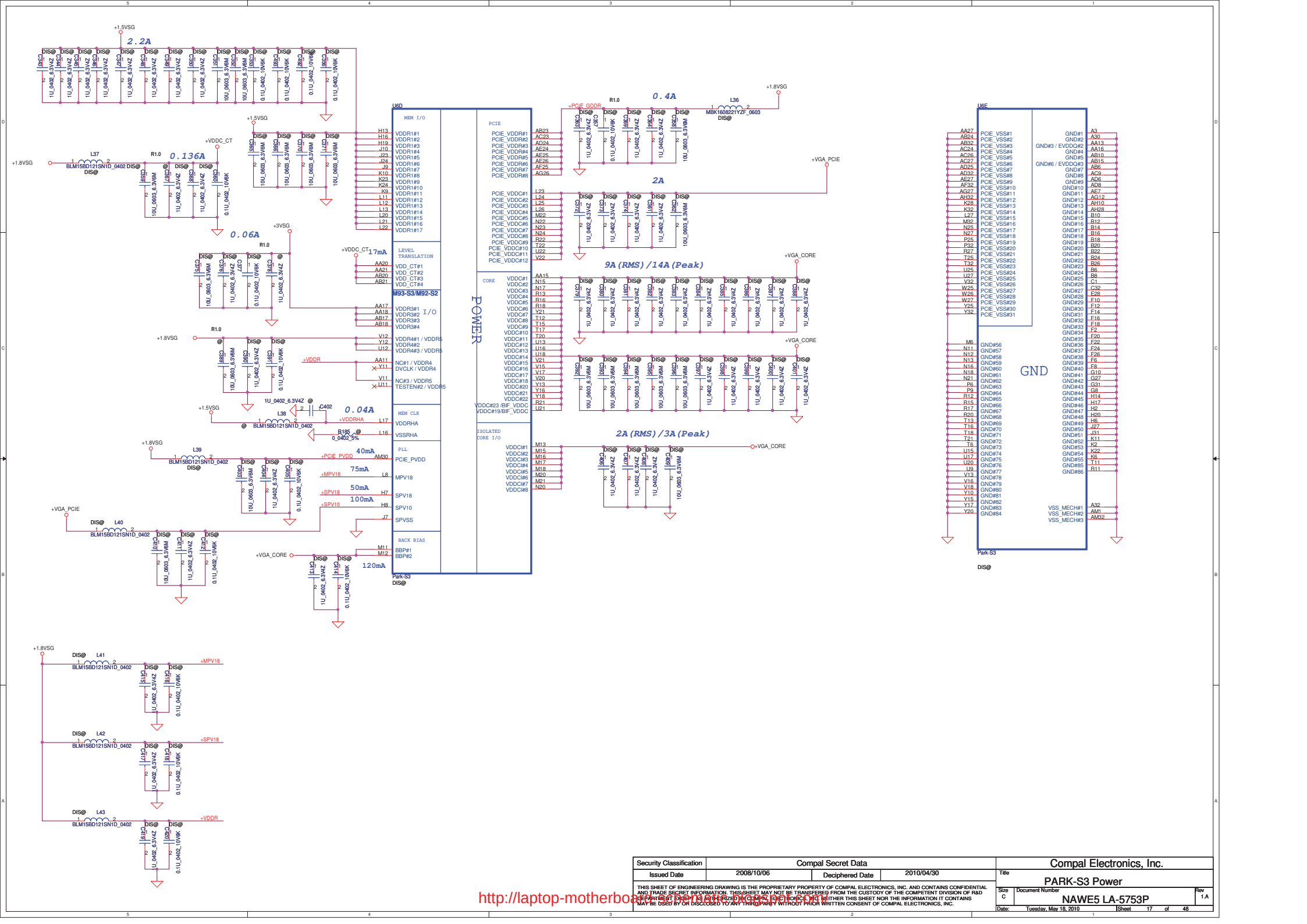
Title	PARK-S3 MEM Interface		
Size B	Document Number NAWE5 LA-5753P		Rev 1.A
Date: Tuesday, May 18, 2010	Sheet 15 of 48		

DPE_VDD10 DPF_VDD10	Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.			
Title: PARK-S3 DPX Power			
Size: B	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 16 of 48		



Compal Electronics, Inc.			
Title	PARK-S3 Power		
Size C	Document Number NAWE5 LA-5753P		Rev 1.A
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[15] M_DA[63..0] → M_DA[63..0]
[15] M_MA[13..0] → M_MA[13..0]
[15] M_DQM[7..0] → M_DQM[7..0]
[15] M_DQS[7..0] → M_DQS[7..0]
[15] M_DQS#[7..0] → M_DQS#[7..0]

X76-H Hynix X76H@ X7622338L02
X76-S Samsung X76S@ X7622338L01

U9 SAMSUNG VRAM S@
U10 SAMSUNG VRAM S@
U11 SAMSUNG VRAM S@
U12 SAMSUNG VRAM S@

U9 VREFCA VREFD_Q1 VREFDQ
U10 VREFCA VREFD_Q2 VREFDQ
U11 VREFCA VREFD_Q3 VREFDQ
U12 VREFCA VREFD_Q4 VREFDQ

M_MA0 M_MA1 M_MA2 M_MA3 M_MA4 M_MA5 M_MA6 M_MA7 M_MA8 M_MA9 M_MA10 M_MA11 M_MA12 M_MA13
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15/BA3

DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7

U9: M_DA16 M_DA23 M_DA19 M_DA21 M_DA17 M_DA18 M_DA22 M_DA20 M_DA0 M_DA4 M_DA1 M_DA6 M_DA3 M_DA7 M_DA2 M_DA5
U10: M_DA25 M_DA27 M_DA24 M_DA31 M_DA26 M_DA30 M_DA28 M_DA29 M_DA14 M_DA10 M_DA15 M_DA11 M_DA12 M_DA8 M_DA13 M_DA9
U11: M_DA38 M_DA34 M_DA33 M_DA37 M_DA35 M_DA39 M_DA32 M_DA36 M_DA44 M_DA42 M_DA47 M_DA40 M_DA45 M_DA43 M_DA46 M_DA41
U12: M_DA54 M_DA52 M_DA53 M_DA49 M_DA51 M_DA50 M_DA55 M_DA48 M_DA57 M_DA58 M_DA60 M_DA61 M_DA63 M_DA62 M_DA56 M_DA59

[15] M_BA0 [15] M_BA1 [15] M_BA2 → M_BA0 M_BA1 M_BA2 → BA0 BA1 BA2

U9: [15] M_CLK0 [15] M_CLK#0 [15] M_CKE0 → M_CLK0 M_CLK#0 M_CKE0 → CK CK CKE/CKE0
U10: M_CLK0 M_CLK#0 M_CKE0 → CK CK CKE/CKE0
U11: [15] M_CLK1 [15] M_CLK#1 [15] M_CKE1 → M_CLK1 M_CLK#1 M_CKE1 → CK CK CKE/CKE0
U12: M_CLK1 M_CLK#1 M_CKE1 → CK CK CKE/CKE0

U9: [15] M_ODT0 [15] M_CS#0 [15] M_RAS#0 [15] M_CAS#0 [15] M_WE#0 → M_ODT0 M_CS#0 M_RAS#0 M_CAS#0 M_WE#0 → ODT/ODT0 CS RAS CAS WE
U10: M_ODT0 M_CS#0 M_RAS#0 M_CAS#0 M_WE#0 → ODT/ODT0 CS RAS CAS WE
U11: [15] M_ODT1 [15] M_CS#1 [15] M_RAS#1 [15] M_CAS#1 [15] M_WE#1 → M_ODT1 M_CS#1 M_RAS#1 M_CAS#1 M_WE#1 → ODT/ODT0 CS RAS CAS WE
U12: M_ODT1 M_CS#1 M_RAS#1 M_CAS#1 M_WE#1 → ODT/ODT0 CS RAS CAS WE

U9: M_DQS2 M_DQS0 → DQSL DQSU
U10: M_DQS3 M_DQS1 → DQSL DQSU
U11: M_DQS4 M_DQS5 → DQSL DQSU
U12: M_DQS6 M_DQS7 → DQSL DQSU

U9: M_DQM2 M_DQM0 → DML DMU
U10: M_DQM3 M_DQM1 → DML DMU
U11: M_DQM4 M_DQM5 → DML DMU
U12: M_DQM6 M_DQM7 → DML DMU

U9: M_DQS#2 M_DQS#0 → DQSL DQSU
U10: M_DQS#3 M_DQS#1 → DQSL DQSU
U11: M_DQS#4 M_DQS#5 → DQSL DQSU
U12: M_DQS#6 M_DQS#7 → DQSL DQSU

[15] DRAM_RST# → RESET

ZQ/ZQ0

NC/ODT1 NC/CS1 NC/CE1 NCZQ1

VDD VDDQ VSS VSSQ

100-BALL SDRAM_DDR3
64MX16 H5TQ1G63BFR-12C FBGA
H@

+1.5VSG

R189 240_0402_1% DIS@
R190 240_0402_1% DIS@
R191 240_0402_1% DIS@
R192 240_0402_1% DIS@

R193 4.99K_0402_1% DIS@ — VREFD_Q1 — R201 4.99K_0402_1% DIS@ — C421 DIS@ 0.1U_0402_10V6K
R194 4.99K_0402_1% DIS@ — VREFC_A1 — R202 4.99K_0402_1% DIS@ — C422 DIS@ 0.1U_0402_10V6K
R195 4.99K_0402_1% DIS@ — VREFC_A2 — R203 4.99K_0402_1% DIS@ — C423 DIS@ 0.1U_0402_10V6K
R196 4.99K_0402_1% DIS@ — VREFD_Q2 — R204 4.99K_0402_1% DIS@ — C424 DIS@ 0.1U_0402_10V6K
R197 4.99K_0402_1% DIS@ — VREFC_A3 — R205 4.99K_0402_1% DIS@ — C425 DIS@ 0.1U_0402_10V6K
R198 4.99K_0402_1% DIS@ — VREFD_Q3 — R206 4.99K_0402_1% DIS@ — C426 DIS@ 0.1U_0402_10V6K
R199 4.99K_0402_1% DIS@ — VREFC_A4 — R207 4.99K_0402_1% DIS@ — C427 DIS@ 0.1U_0402_10V6K
R200 4.99K_0402_1% DIS@ — VREFD_Q4 — R208 4.99K_0402_1% DIS@ — C428 DIS@ 0.1U_0402_10V6K

M_CLK0 — R209 DIS@ 56_0402_1%
M_CLK#0 — R211 DIS@ 56_0402_1%
C455 0.01U_0402_16V7K DIS@

M_CLK1 — R210 DIS@ 56_0402_1%
M_CLK#1 — R212 DIS@ 56_0402_1%
C456 0.01U_0402_16V7K DIS@

+1.5VSG — 10U_0603_6.3V6M DIS@ — C446 C429 C447 C448 C449 C430 — 10U_0603_6.3V6M DIS@

+1.5VSG — 1U_0402_6.3V4Z DIS@ — C431 C432 C433 C434 C435 C436 C437 C438 C450 C439

+1.5VSG — 1U_0402_6.3V4Z DIS@ — C440 C441 C451 C442 C443 C444 C452 C453 C454 C445

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: PARK-S3 DDR3 VRAM

Size	Document Number	Rev
C	NAWE5 LA-5753P	1.A

Date: Tuesday, May 18, 2010 Sheet 18 of 48

Check Timing +1.1VS <50us +3VS for EXT CLKGEN satable

+1.1VS → EXT@ L44 FBMA-L11-201209-221LMA30T_0805 → +VDDCLK_IO
C457 22U_0805_6.3V6M EXT@
C458 0.1U_0402_16V4Z EXT@
C459 0.1U_0402_16V4Z EXT@
C460 0.1U_0402_16V4Z EXT@
C461 0.1U_0402_16V4Z EXT@
C462 0.1U_0402_16V4Z EXT@

+3VS → L45 EXT@ FBMA-L11-201209-221LMA30T_0805 → +3VS_CLK
C464 22U_0805_6.3V6M EXT@
C465 0.1U_0402_16V4Z EXT@
C466 0.1U_0402_16V4Z EXT@
C467 0.1U_0402_16V4Z EXT@
C468 0.1U_0402_16V4Z EXT@
C469 0.1U_0402_16V4Z EXT@
C470 0.1U_0402_16V4Z EXT@
C471 0.1U_0402_16V4Z EXT@
C474 1U_0402_6.3V4Z EXT@
1U CLOSE PIN 69

EXT@ L46 FBMA-L11-201209-221LMA30T_0805 → +3VS_CLKVDDA 100mA
C475 22U_0805_6.3V6M EXT@
C476 0.1U_0402_16V4Z EXT@
C477 0.1U_0402_16V4Z EXT@

U13
ICS 9LPRS488
SLG8SP626VTR_QFN72_10x10 EXT@

49	VDDA	SMBCLK	1
48	GNDA	SMBDAT	2
62	VDDREF	SB_SRC_SLOW#	41
66	GNDREF		
12	VDDSRC_IO	CPUKG0T_LPRS	56
18	VDDSRC_IO	CPUKG0C_LPRS	55
28	VDDATIG_IO		
37	VDDSB_SRC_IO	HTT0T_LPRS / 66 M	60
53	VDDCPU_IO	HTT0C_LPRS / 66 M	59
3	VDDDOT	SB_SRC0T_LPRS	40
17	VDDSRC	SB_SRC0C_LPRS	39
29	VDDATIG		
38	VDDSB_SRC	SB_SRC1T_LPRS	35
44	VDDSATA	SB_SRC1C_LPRS	34
54	VDDCPU		
61	VDDHTT	ATIG0T_LPRS	33
69	VDD48	ATIG0C_LPRS	32
24	CLKREQ0 #	ATIG1T_LPRS	31
51	CLKREQ1#	ATIG1C_LPRS	30
50	CLKREQ2#	ATIG2T_LPRS	26
43	CLKREQ3#	ATIG2C_LPRS	25
42	CLKREQ4#		
63	REF2/SEL_27	SRC0T_LPRS	23
64	REF1/SEL_SATA	SRC0C_LPRS	22
65	REF0/SEL_HTT66	SRC1T_LPRS	21
71	48MHz_0	SRC1C_LPRS	20
70	48MHz_1	SRC2T_LPRS	16
67	X1	SRC2C_LPRS	15
68	X2	SRC3T_LPRS	14
		SRC3C_LPRS	13
6	GNDDOT	SRC4T_LPRS	10
11	GNDSRC	SRC4C_LPRS	9
19	GNDSRC	SRC5T_LPRS	8
27	GNDATIG	SRC5C_LPRS	7
36	GNDSB_SRC	SRC6T/SATAT_LPRS	46
47	GNDSATA	SRC6C/SATAC_LPRS	45
52	GNDCPU	SRC7T_LPRS/27MHz_SS	5
58	GNDHTT	SRC7C_LPRS/27MHz_NS	4
72	GND48	PD#	57
73	GNDPAD		

SB_SMCLK0 [8,9,21,28]
SB_SMDAT0 [8,9,21,28]
SRC_SLOW

CPU: CPU_HT_CLKP [20], CPU_HT_CLKN [20] (R214, R215); CLK_CPU_BCLK [6], CLK_CPU_BCLK# [6]
NB HT: CLK_NBHT [11], CLK_NBHT# [11]; NB_HT_CLKP [20], NB_HT_CLKN [20] (R217, R218)
NB GFX: CLK_NBGFX [11], CLK_NBGFX# [11]
VGA: ATIG1 / ATIG1# (R225, R226); CLK_PEG_VGA [13], CLK_PEG_VGA# [13]; VGA_CLKP [20], VGA_CLKN [20] (R227, R228)
GLAN: GPP_CLK1P [20], GPP_CLK1N [20]; CLK_PCIE_LAN [29], CLK_PCIE_LAN# [29] (R229, R230)
MiniCard_WLAN: GPP_CLK3P [20], GPP_CLK3N [20]; CLK_PCIE_WLAN [28], CLK_PCIE_WLAN# [28] (R232, R233)
MiniCard_WWAN: GPP_CLK5P [20], GPP_CLK5N [20]; CLK_PCIE_WWAN [28], CLK_PCIE_WWAN# [28] (R235, R236)
New Card: GPP_CLK7P [20], GPP_CLK7N [20]; CLK_PCIE_EXP [28], CLK_PCIE_EXP# [28] (R238, R239)
NB A LINK: CLK_SBLINK_BCLK [11], CLK_SBLINK_BCLK# [11]
SB RCLK: CLK_SBSRC_BCLK [20], CLK_SBSRC_BCLK# [20]

CLK_SRC7C_SS, CLK_SRC7C (R276, R277) → 27M_CLK (R548) → 27M_NSSC [14]
PD# → +3VS_CLK (R243 8.2K_0402_5%)
VGA_DBCLK [34] (R271 0_0402_5%)

CLK SB / CLK SB#:
CLK_SBLINK_BCLK (R244), CLK_SBLINK_BCLK# (R246), CLK_SBSRC_BCLK# (R248), CLK_SBSRC_BCLK (R249)

LAN [21,29] LAN_CLKREQ#
Mini Card_WLAN [21,28] WLAN_CLKREQ#
WWAN [20,28] WWAN_CLKREQ#
NEW CARD [20,28] EXP_CLKREQ#
R219 R220 R221 R222 8.2K_0402_5% @ EXT@ R1.0 EXP@

L47 BLM18AG601SN1D_2P EXT@

27M_SEL → R234 90.9_0402_1%
SEL_SATA
[11] CLK_NB_14.318M → R237 158_0402_1% → CLK_14.318M
[21] CLK_48M_USB → R240 33_0402_5% → CLK_48M
CLK_XTAL_IN
CLK_XTAL_OUT

+3VS_CLK → R213 8.2K_0402_5% EXT@ → SRC_SLOW → R216 8.2K_0402_5% @
+3VS_CLK → R223 8.2K_0402_5% @, R224 8.2K_0402_5% EXT@ → SEL_SATA, 27M_SEL → R231 8.2K_0402_5% EXT@

CLK_XTAL_OUT
CLK_XTAL_IN
Y2 EXT@ 14.318MHZ_16PF_7A14300083
C478 EXT@ 33P_0402_50V8J
C479 EXT@ 33P_0402_50V8J

Change Y2 to TXC-SJ100009R00 <20ppm / 20pF>
Routing the trace at at least 10mil

	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1	NON SPREAD 100M_SATA SRC6 output
	* 0	SPREAD 100M_SATA SRC6 output

* default

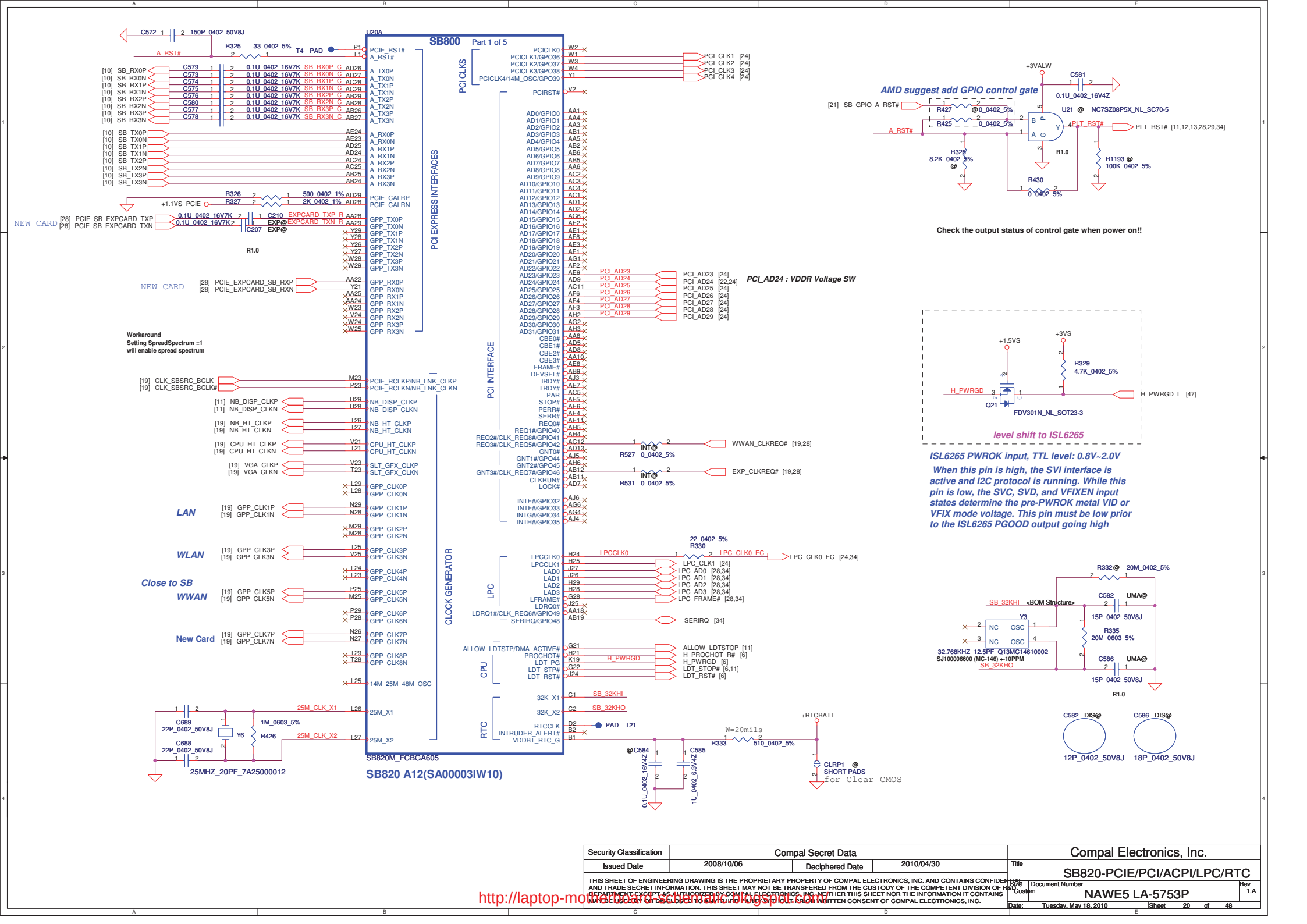
1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: Clock generator

Size: B	Custom	Document Number: NAWE5 LA-5753P	Rev: 1.A
Date: Tuesday, May 18, 2010		Sheet 19 of 48	



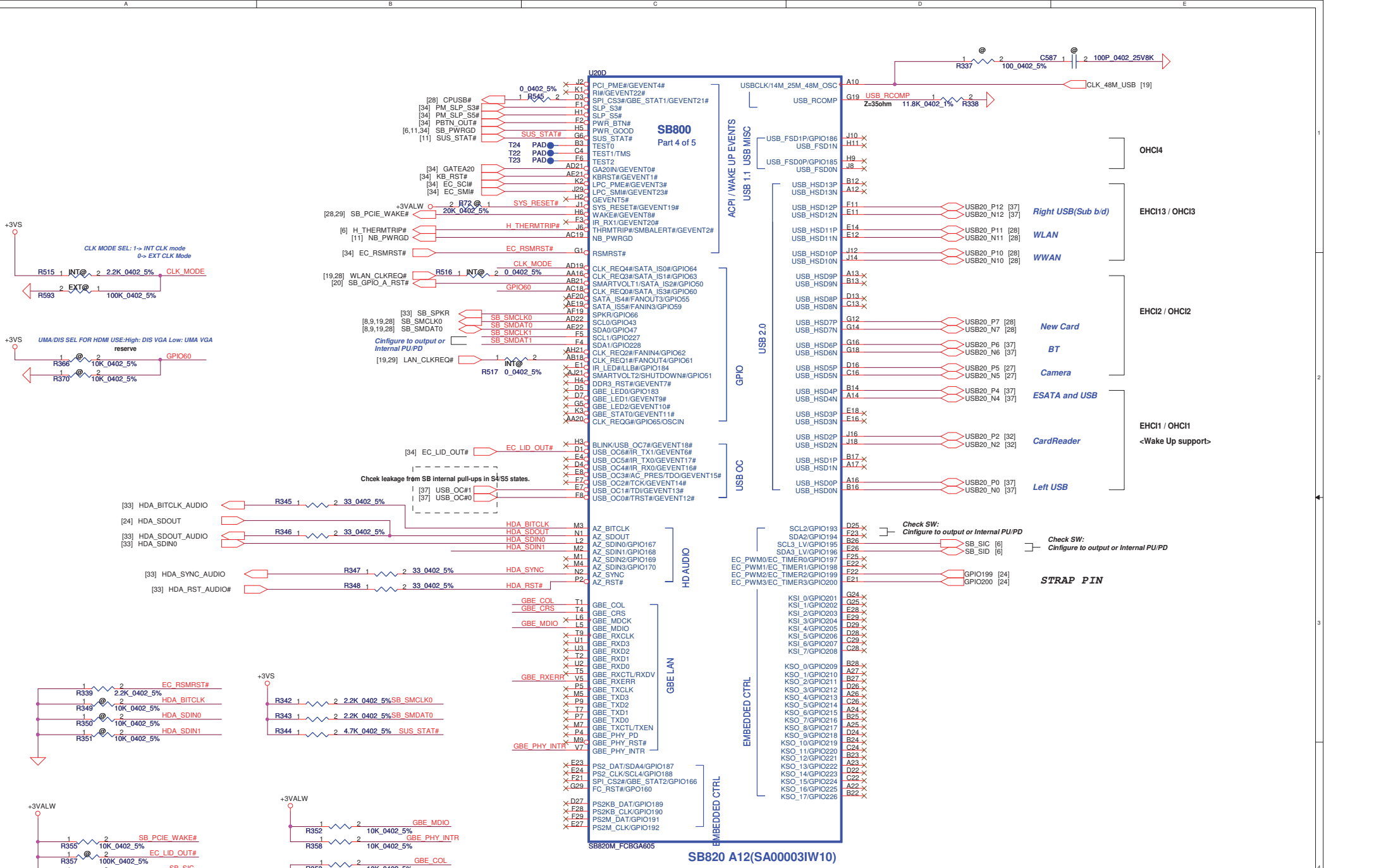
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: SB820-PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	NAWE5 LA-5753P	1.A

Date: Tuesday, May 18, 2010 Sheet 20 of 48



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: SB820 USB/HD audio

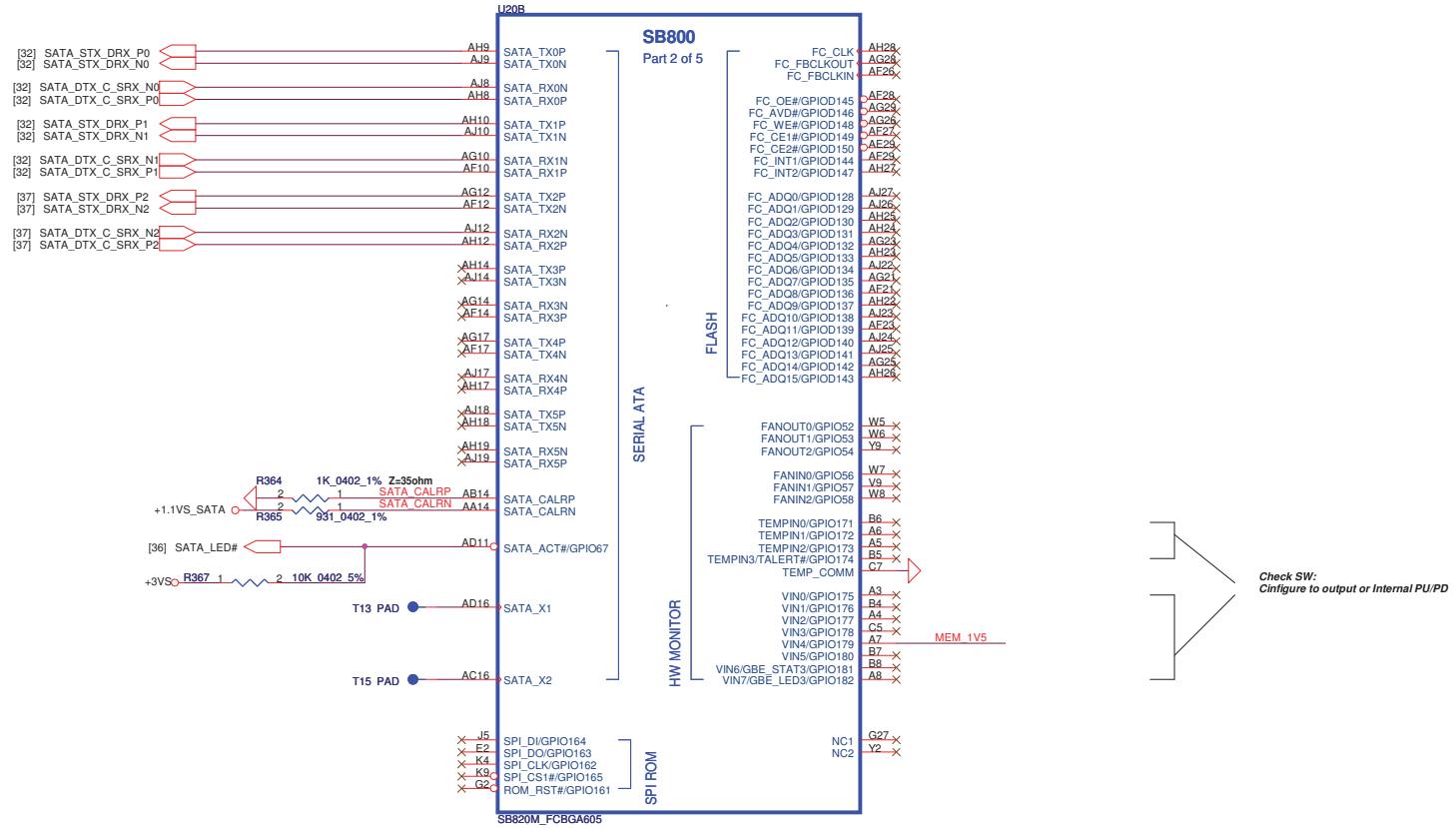
Size: B(28) Custom | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 21 of 48

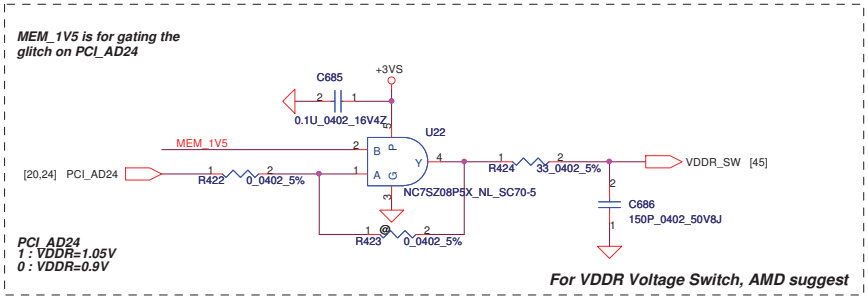
HDD

ODD

e-SATA



SB820 A12(SA00003IW10)



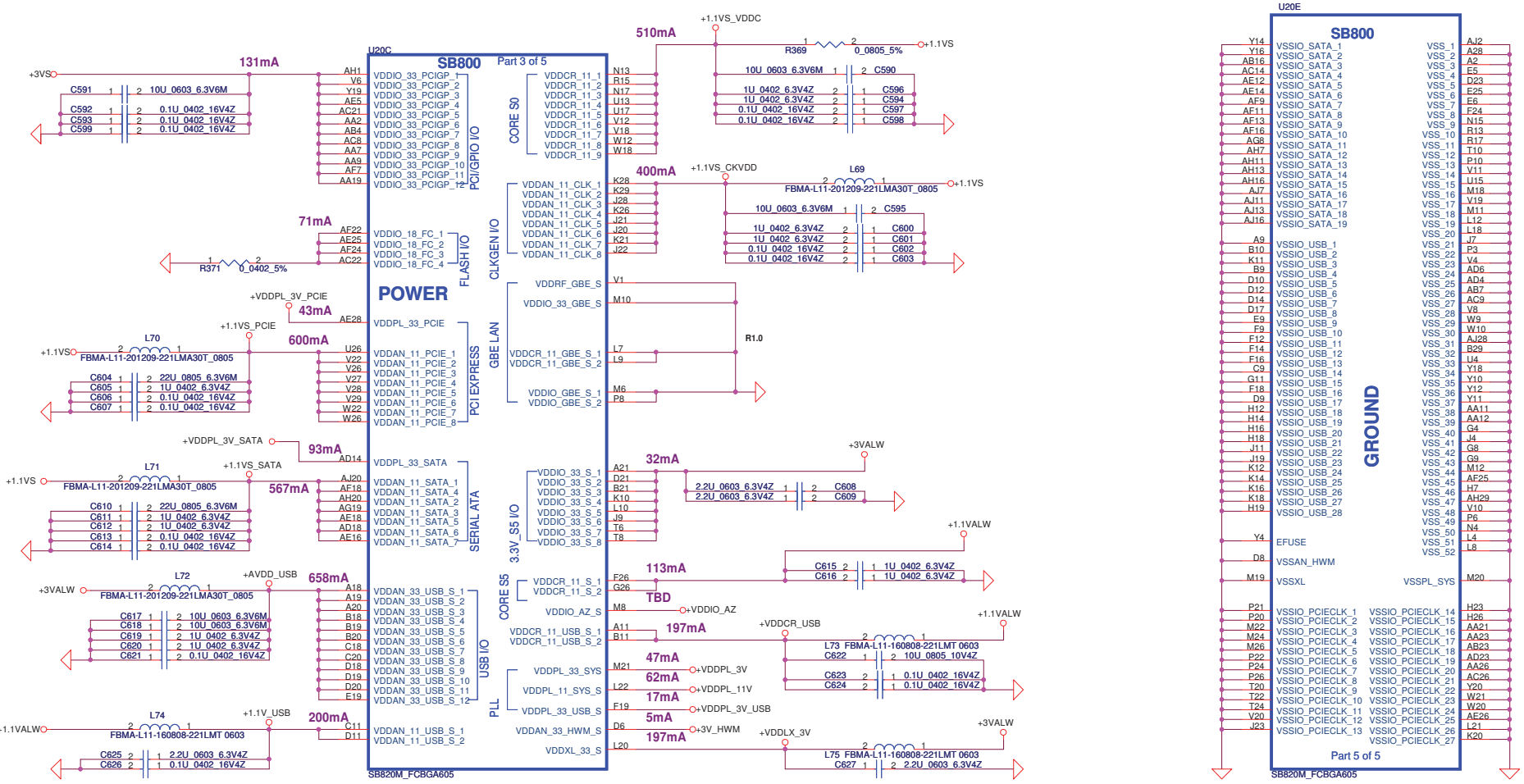
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: SB820 SATA/IDE/SPI

Size: B/28 Custom | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 22 of 48



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: SB820 power/GND

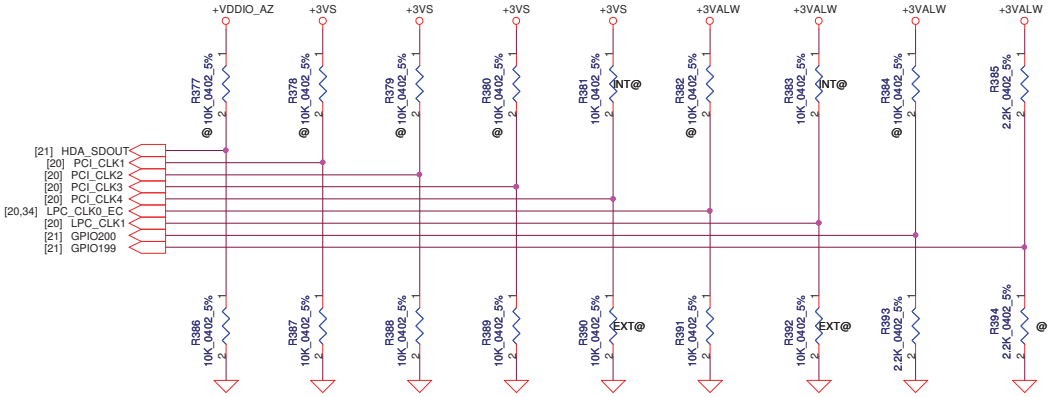
Size: B/28 Custom | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 23 of 48

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	CPU/HT CLK SEL Disable	EC DISABLE	CLOCKGEN DISABLE	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	



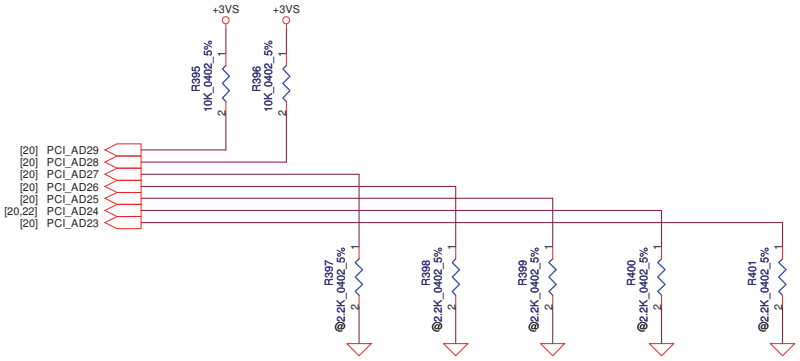
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

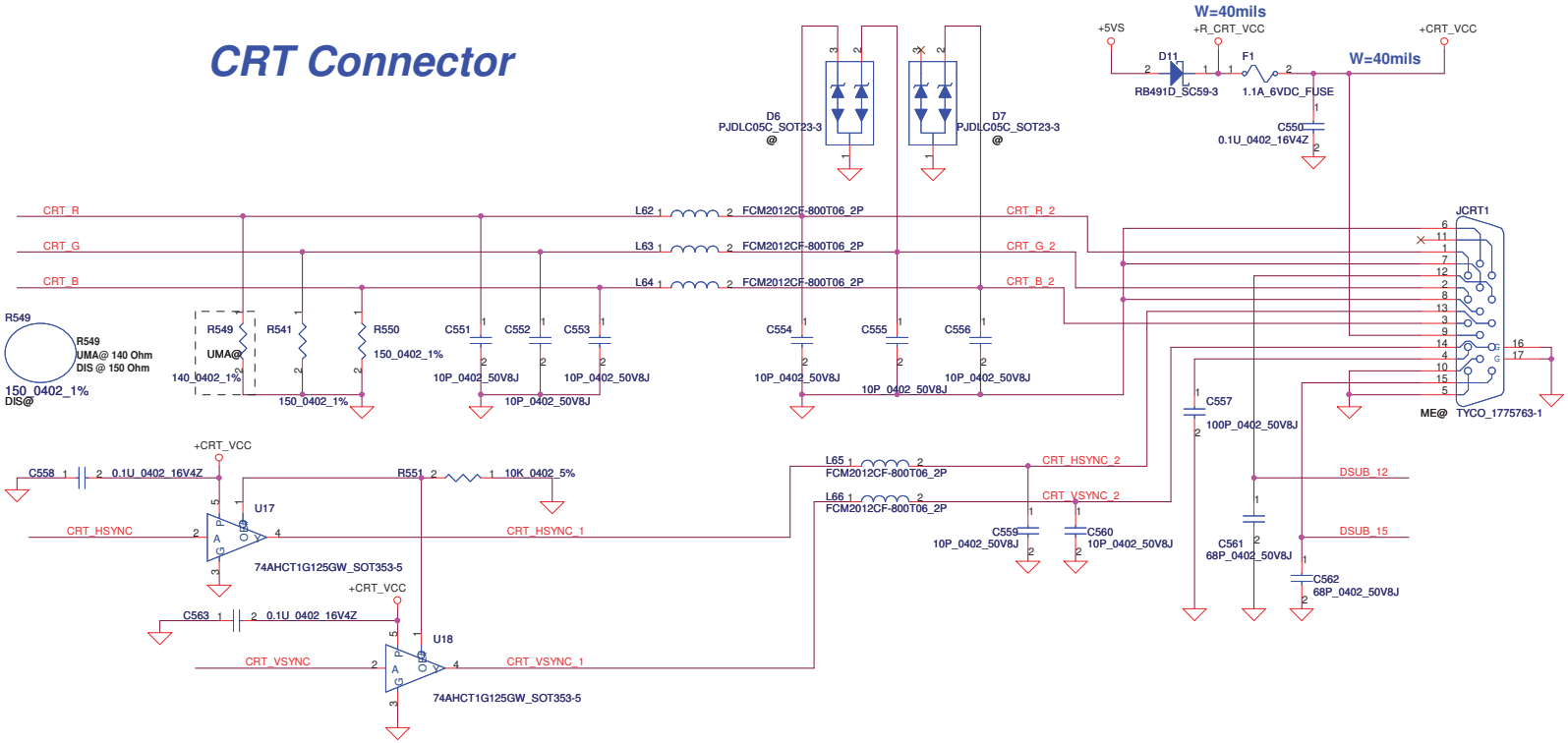
Check AD29,AD28 strap function

check default



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/04/30	Title SB820 STRAPS
Size B/28 Custom	Document Number NAWE5 LA-5753P		Rev 1.A
Date: Tuesday, May 18, 2010	Sheet 24 of 48		

CRT Connector



For UMA Only

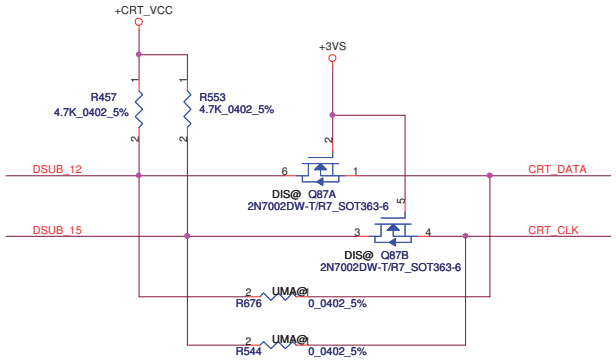
[11] GMCH_CRT_R	GMCH_CRT_R	R677	UMA@	0_0402_5%	CRT_R
[11] GMCH_CRT_G	GMCH_CRT_G	R542	UMA@	0_0402_5%	CRT_G
[11] GMCH_CRT_B	GMCH_CRT_B	R679	UMA@	0_0402_5%	CRT_B
[11,12] GMCH_CRT_HSYNC	GMCH_CRT_HSYNC	R547	UMA@	0_0402_5%	CRT_HSYNC
[11,12] GMCH_CRT_VSYNC	GMCH_CRT_VSYNC	R543	UMA@	0_0402_5%	CRT_VSYNC
[11] GMCH_CRT_DATA	GMCH_CRT_DATA	R546	UMA@	0_0402_5%	CRT_DATA
[11] GMCH_CRT_CLK	GMCH_CRT_CLK	R678	UMA@	0_0402_5%	CRT_CLK

For VGA Only

[14] VGA_CRT_R	VGA_CRT_R	R539	DIS@	0_0402_5%	CRT_R
[14] VGA_CRT_G	VGA_CRT_G	R552	DIS@	0_0402_5%	CRT_G
[14] VGA_CRT_B	VGA_CRT_B	R554	DIS@	0_0402_5%	CRT_B
[14] VGA_CRT_HSYNC	VGA_CRT_HSYNC	R535	DIS@	0_0402_5%	CRT_HSYNC
[14] VGA_CRT_VSYNC	VGA_CRT_VSYNC	R557	DIS@	0_0402_5%	CRT_VSYNC
[14] VGA_CRT_DATA	VGA_CRT_DATA	R538	DIS@	0_0402_5%	CRT_DATA
[14] VGA_CRT_CLK	VGA_CRT_CLK	R556	DIS@	0_0402_5%	CRT_CLK

NOTE:
IF RS880M ONLY(NO MXM SUPPORT),
DAC_SDAT AND DAC_SCL DON'T
NEED LEVEL SHIFT, PU TO +5V DIRECTLY.
DAC_SDAT AND DAC_SCL ARE 5V TOLERANCE.

Close to Conn side



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.	
Title	CRT Connector
Size	B
Document Number	NAWE5 LA-5753P
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Date:	Tuesday, May 18, 2010
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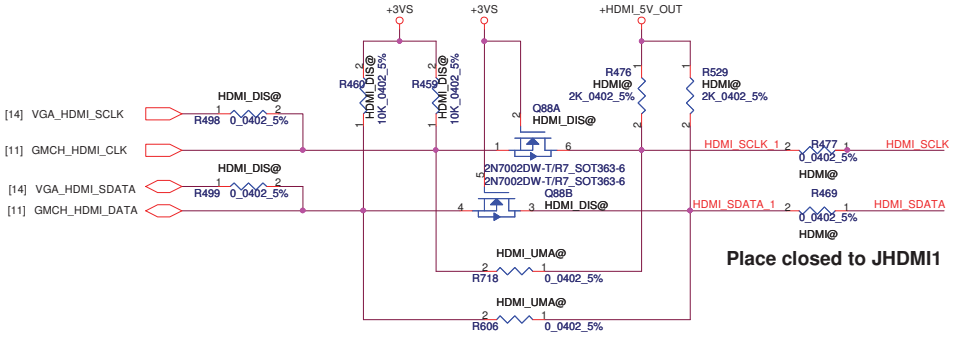
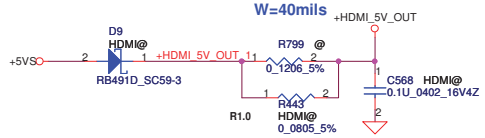
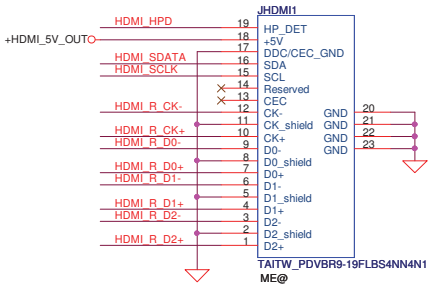


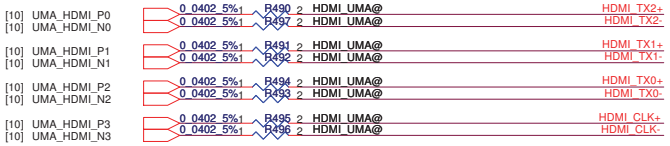
Place closed to JHDMI1

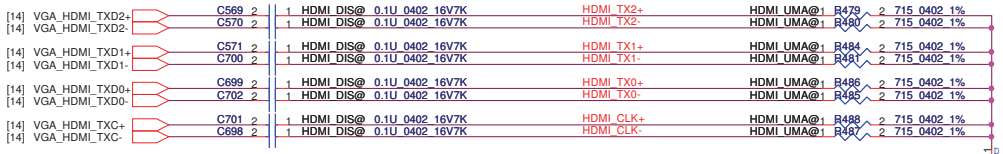
W=40mils



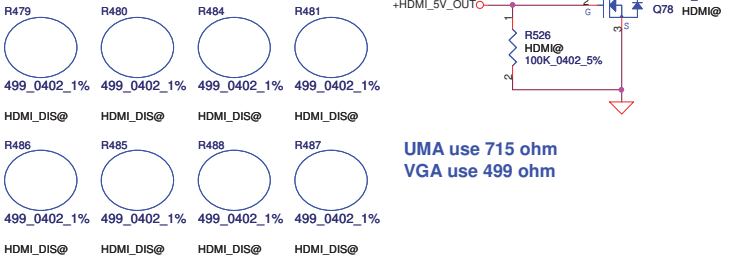


R1.0

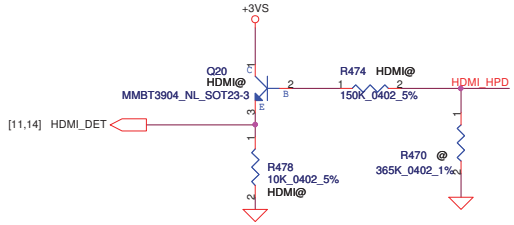


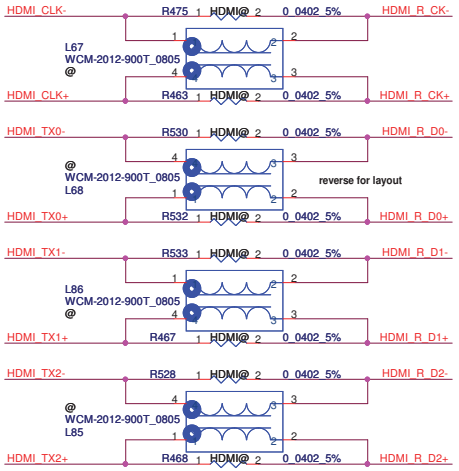


Place closed to JHDMI1



UMA use 715 ohm
VGA use 499 ohm





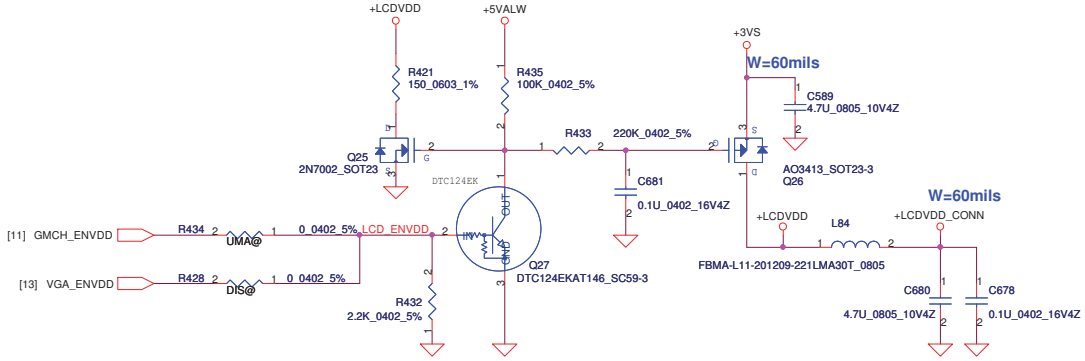
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

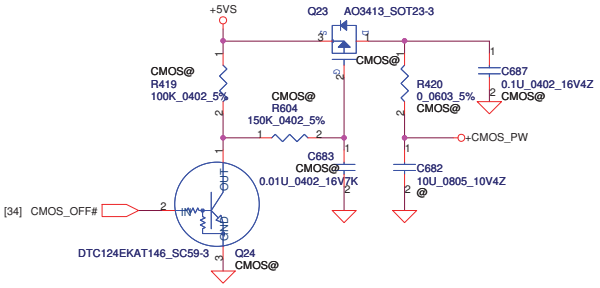
Title: HDMI Connector

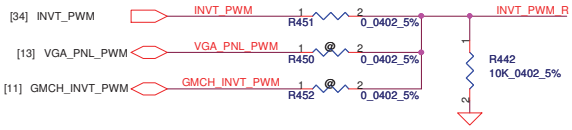
Size: B2B Custom	Document Number: NAWE5 LA-5753P	Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 26 of 48	

LCD POWER CIRCUIT

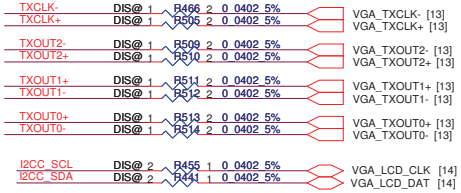


CMOS Camera

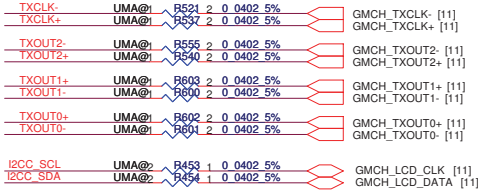


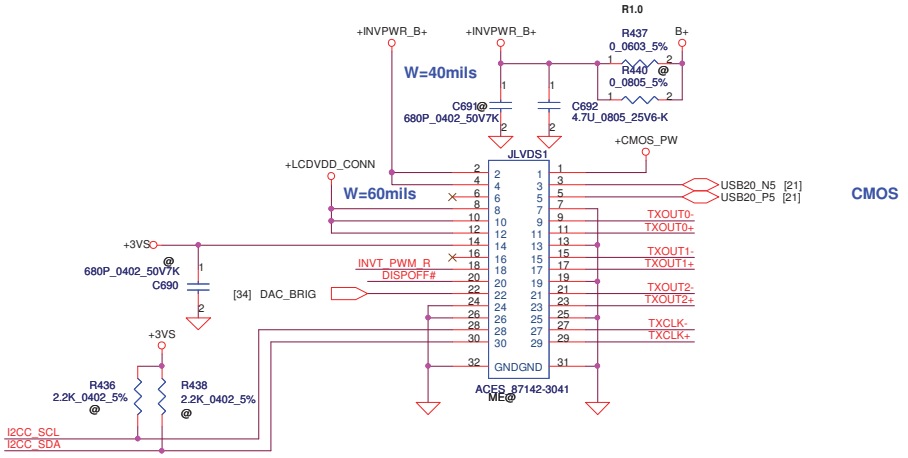


VGA ONLY

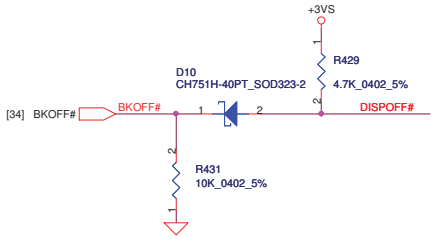


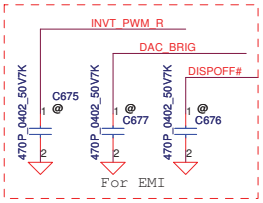
UMA ONLY





CMOS

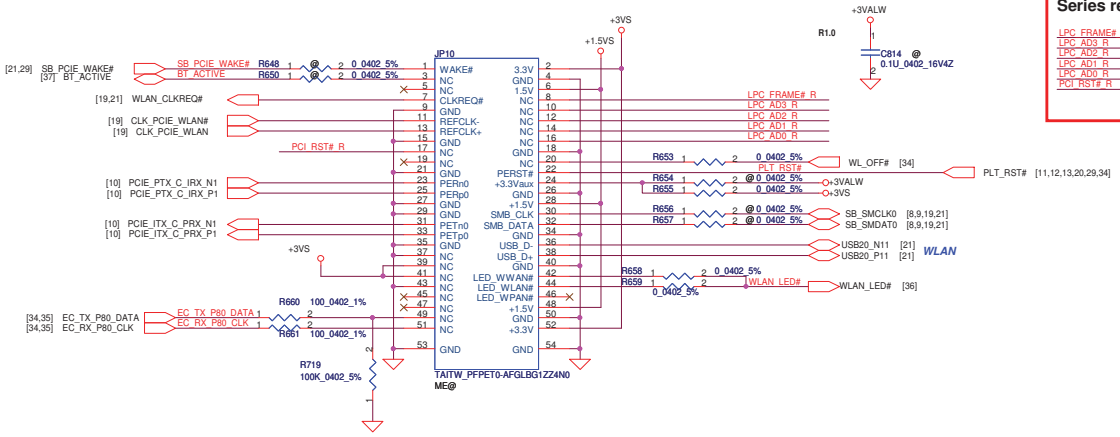




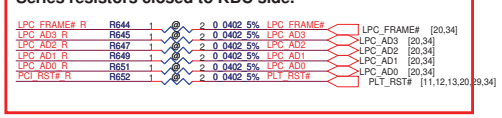
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2010/04/30

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: Custom	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 27 of 48		

Mini-Express Card for WLAN/WiMAX(Half)

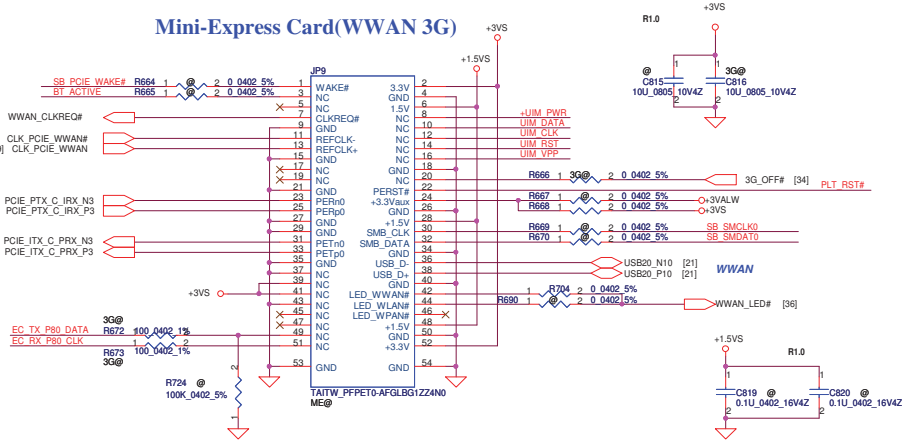


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

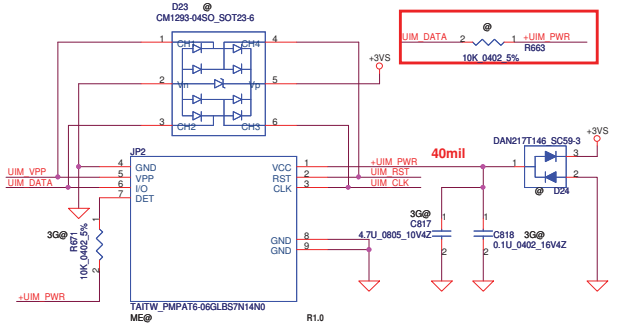


Mini-Express Card for WWAN(Full)

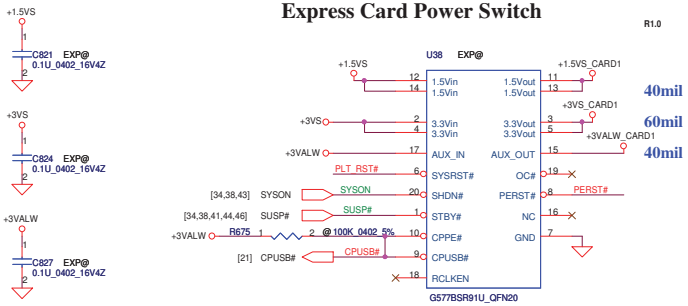
Mini-Express Card(WWAN 3G)

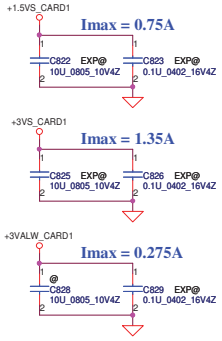


Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

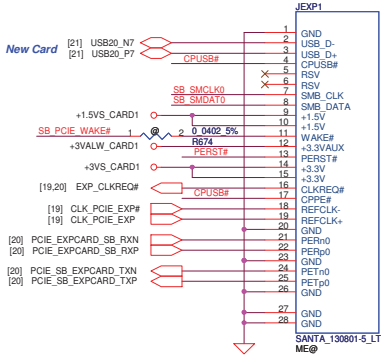


Express Card Power Switch



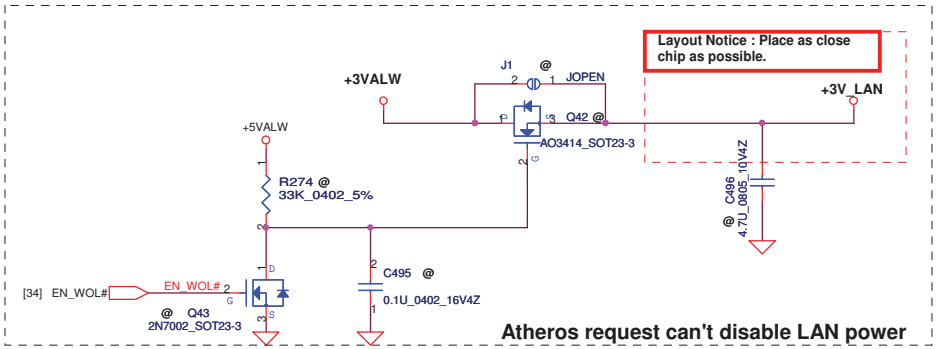


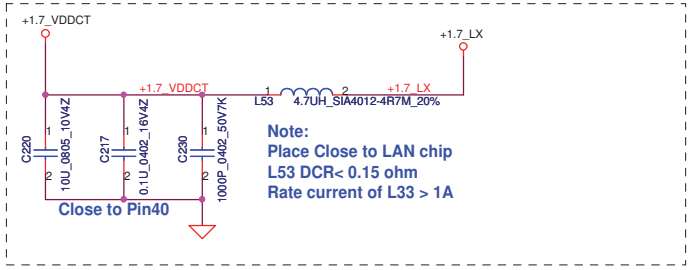
New Card 34mm Socket (Left/TOP)



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2010/04/30

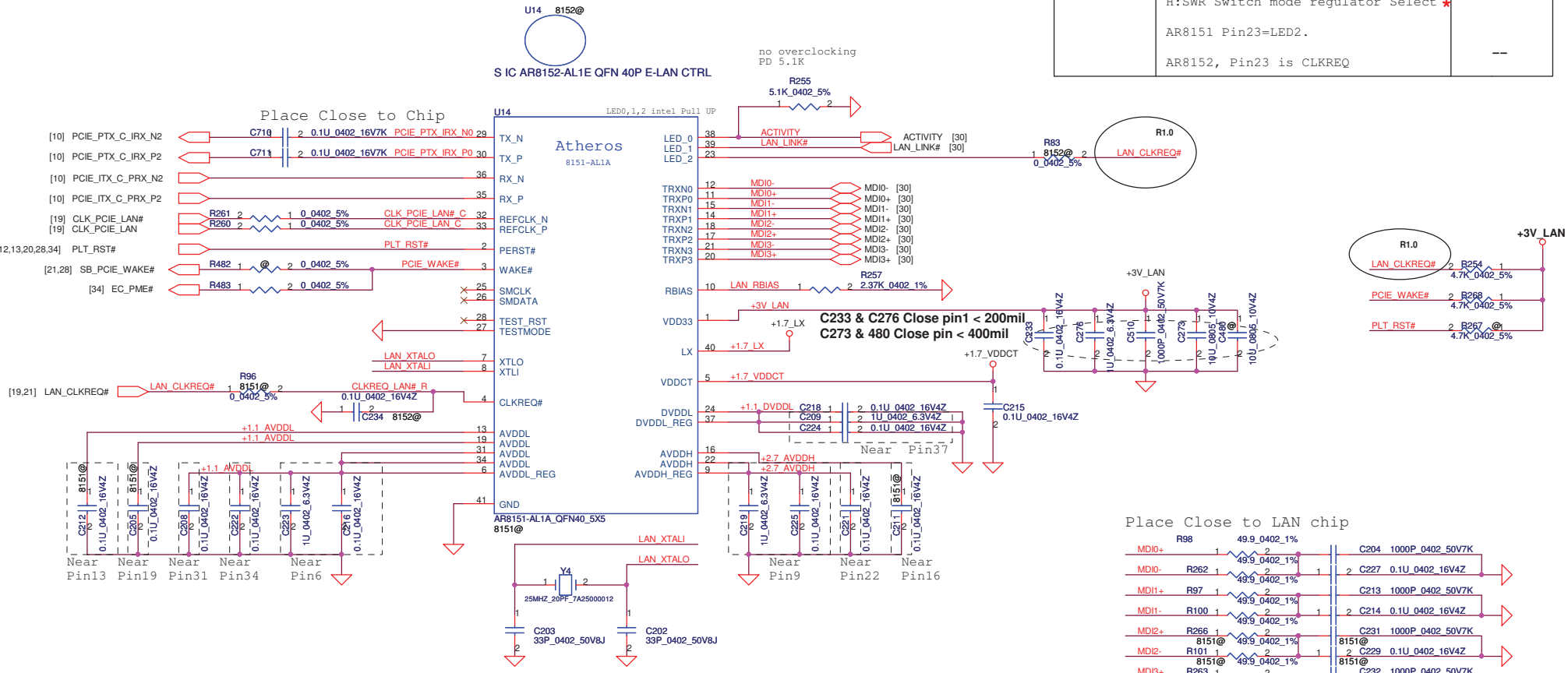
Compal Electronics, Inc.			
Title: Mini-Card/Nwe Card/SIM			
Size	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 28 of 48		





Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable ★	H
	H:SWR Switch mode regulator Select ★ AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



For AR8152, pin23 is the LDO output. Mount C234 and no mount R96.close to this pin4

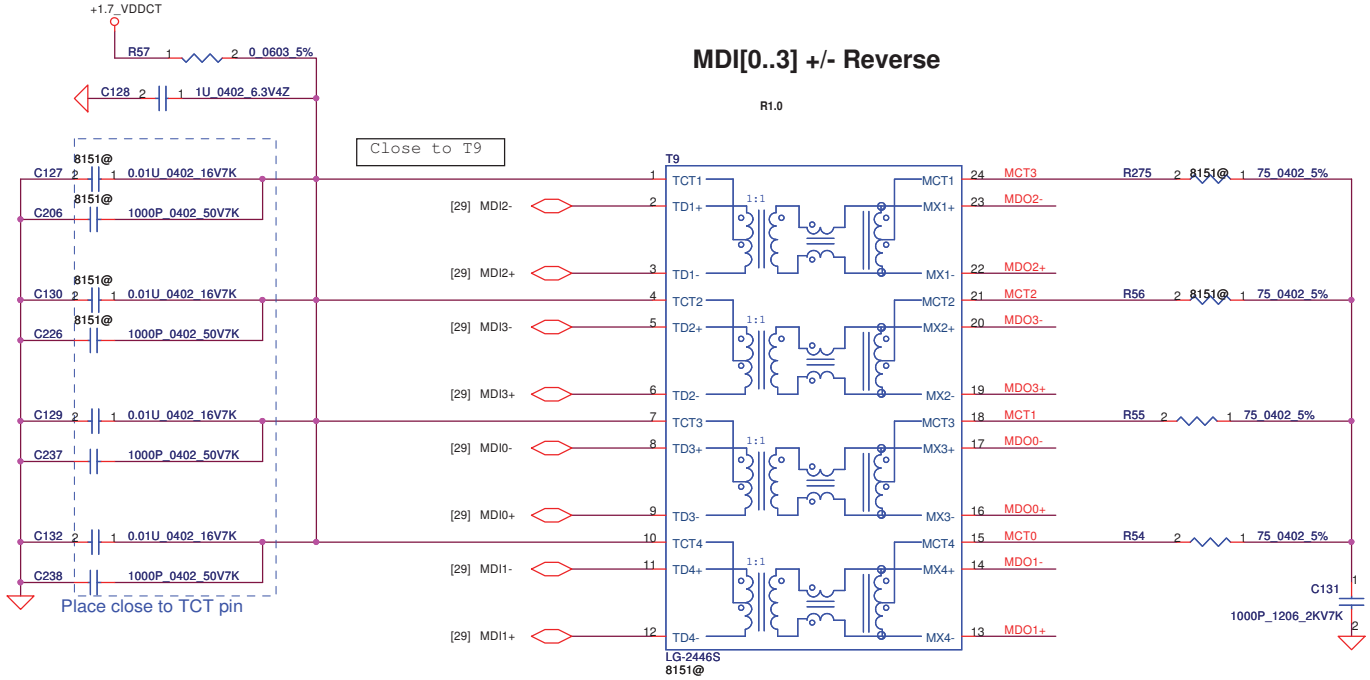
For AR8151, pin4 is the CLKREQn pin, mount R96 and no mount C234.close to this pin4

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2010/04/30

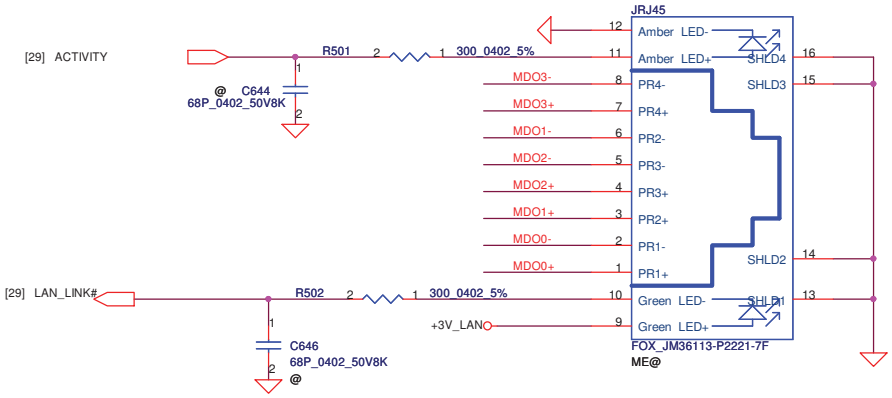
Compal Electronics, Inc.			
Title	LAN-AR8151/8152		
Size: Custom	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 29 of 48		

MDI[0..3] +/- Reverse

R1.0



RJ45 Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/03/20	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: LAN_Transformer

Size	Document Number	Rev
Custom	NAWE5 LA-5753P	1.A

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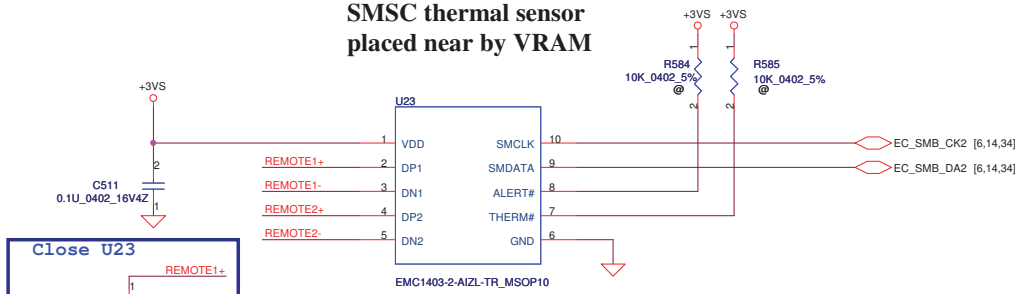
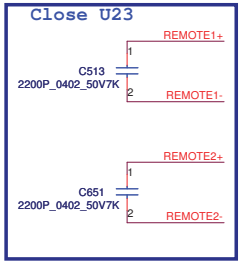
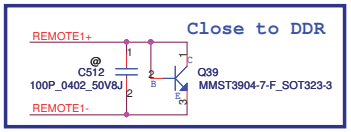
SMSC thermal sensor placed near by VRAM

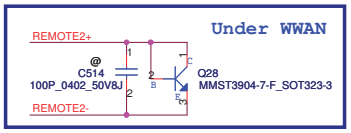


Address 1001_101xb

P/N SA000029210

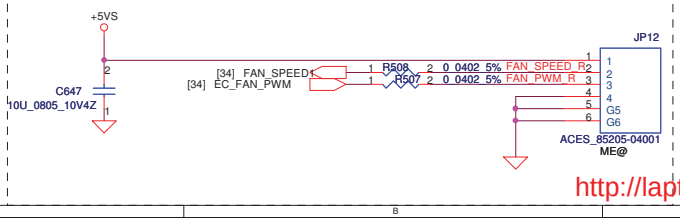






REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

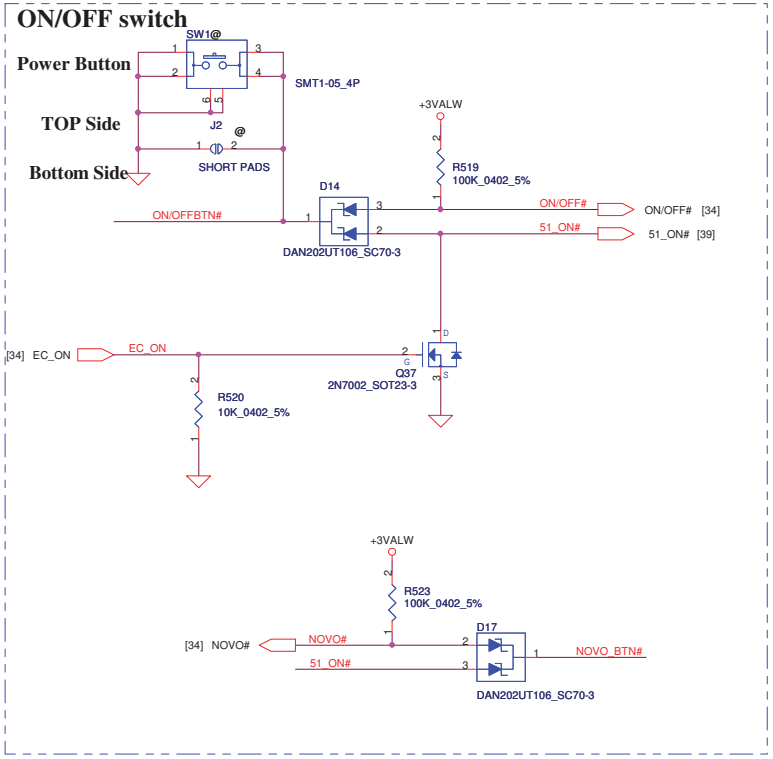
Compal Electronics, Inc.

Title: EMC1403_sensor/FAN

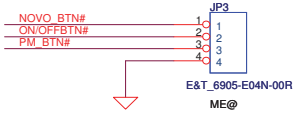
Size: B | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 31 of 48

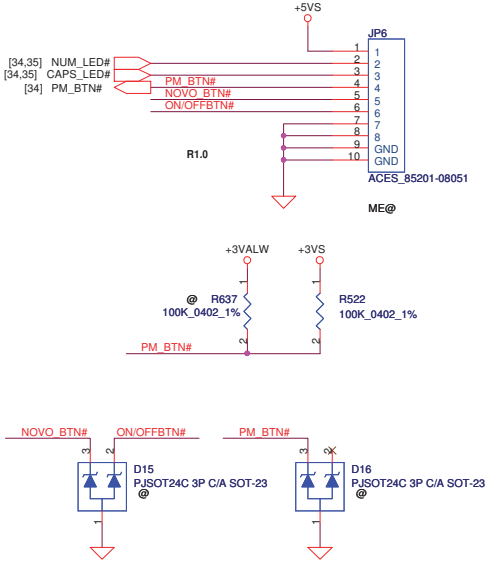
ON/OFF switch



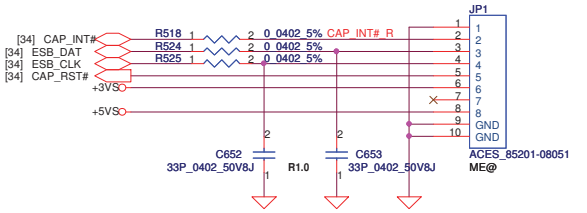
Power Bottom Board Conn. 4pin



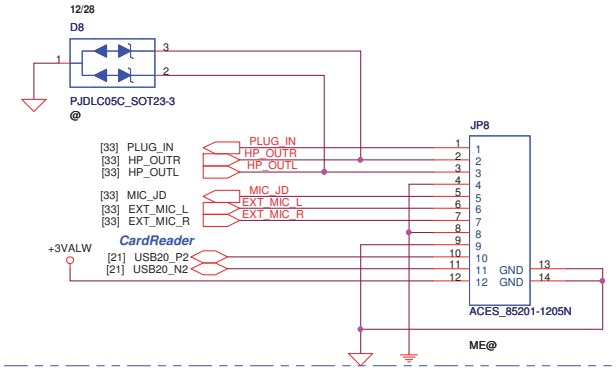
Power Bottom Board Conn. 8pin



Cap Sensor Board Conn. 8pin



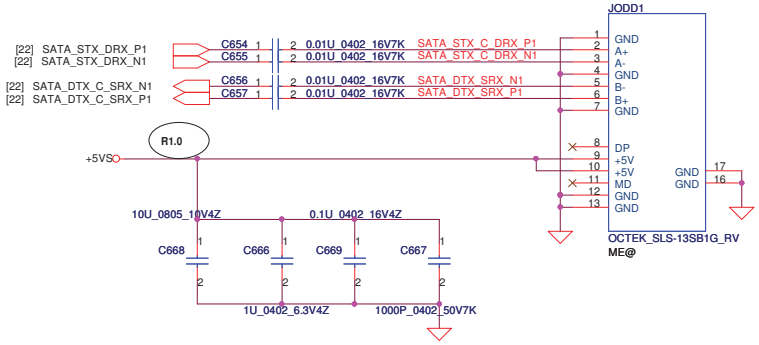
Card Reader/Audio Jack SB CONN

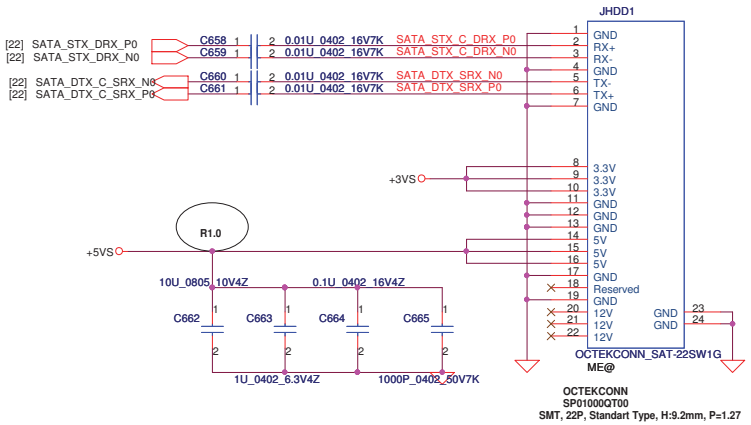


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

SATA HDD Conn.

SATA ODD Conn.



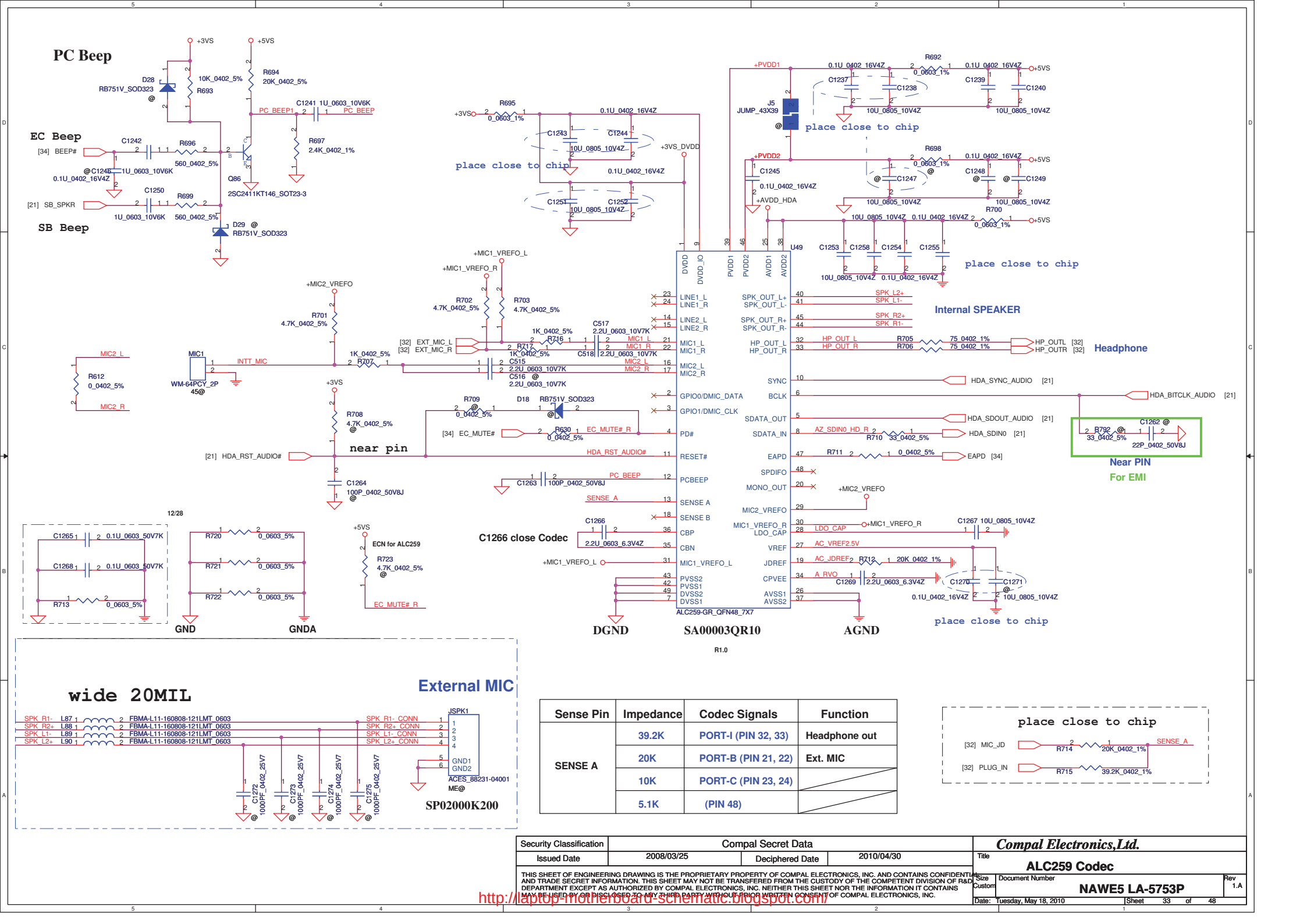


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2010/04/30

Compal Electronics, Inc.

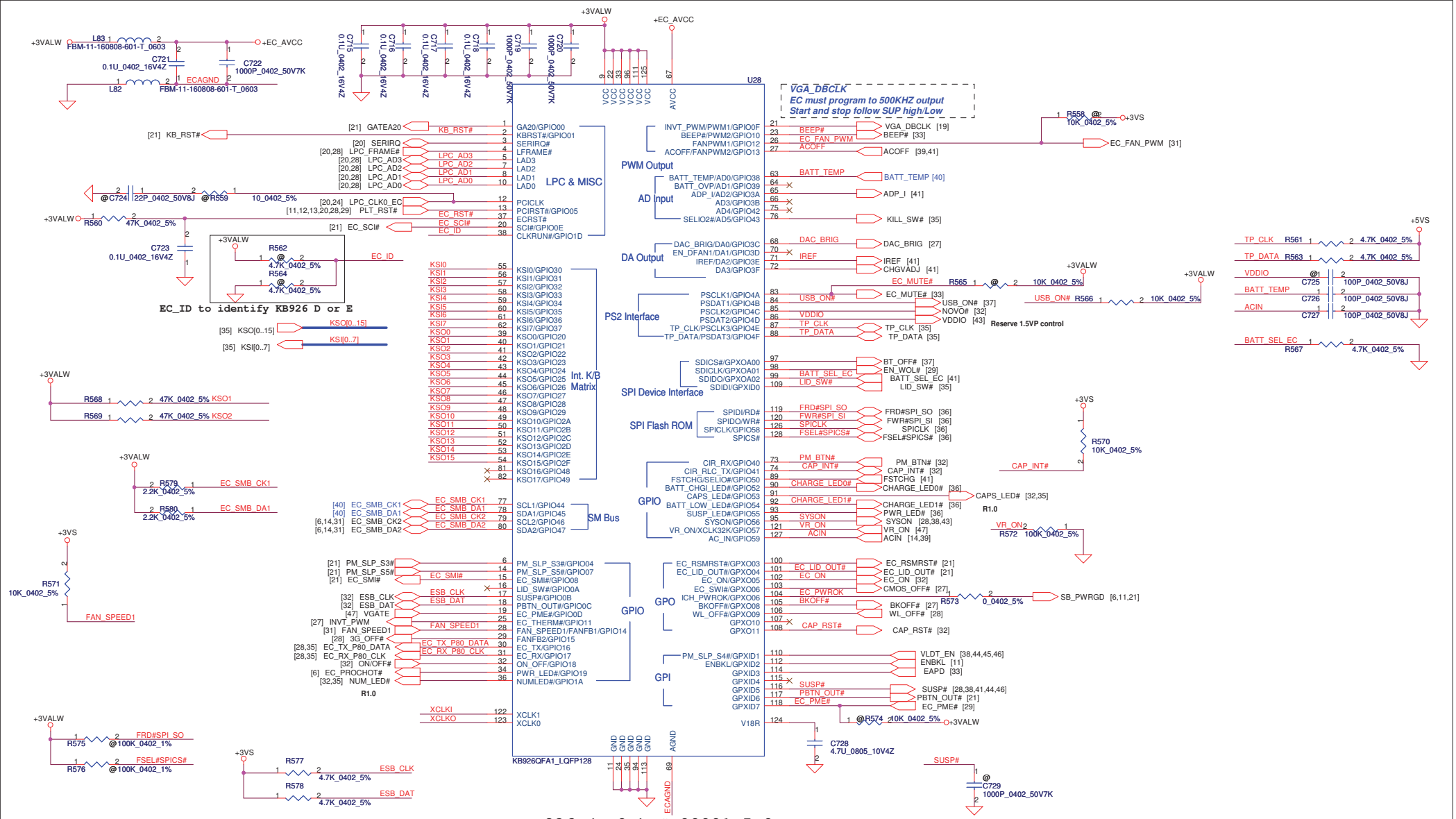
Title: *HDD/ODD Connector*

Size: B/28 Custom	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 32 of 48		



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

Security Classification	Compal Secret Data		Compal Electronics,Ltd.
Issued Date	2008/03/25	Deciphered Date	2010/04/30
Title	ALC259 Codec		
Size: Custom	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 33 of 48		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2010/04/30

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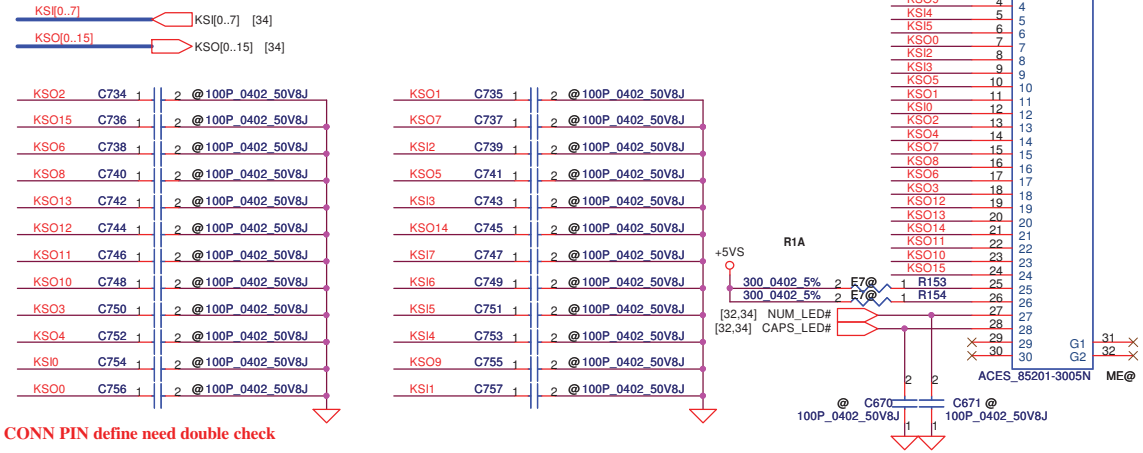
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: Custom | Document Number: **NAWE5 LA-5753P** | Rev: 1.A

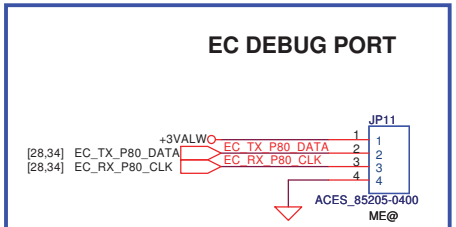
Date: Tuesday, May 18, 2010 | Sheet 34 of 48

INT_KBD Conn.

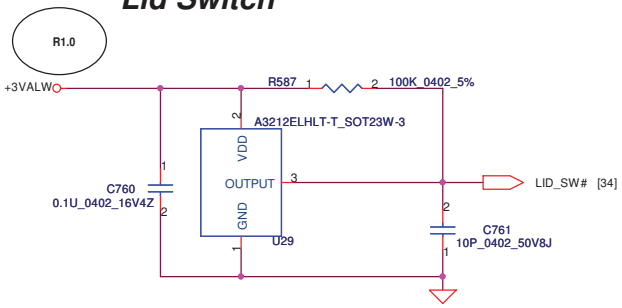


CONN PIN define need double check

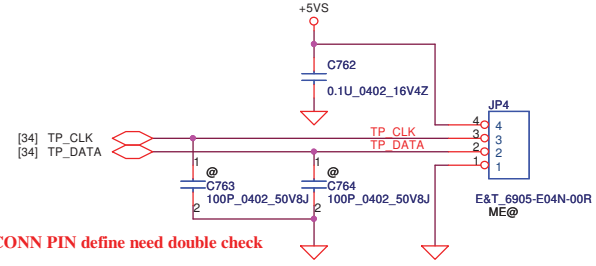
EC DEBUG PORT



Lid Switch

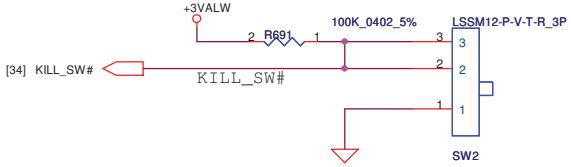


To TP/B Conn.



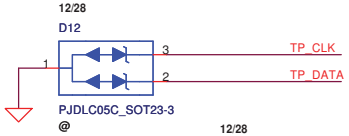
CONN PIN define need double check

Kill Switch



Kill

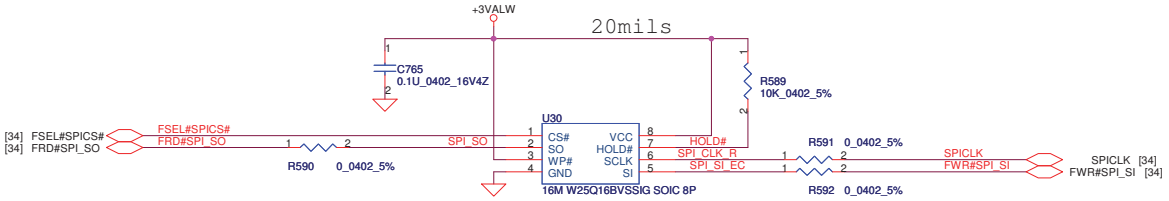
STATUS	
1,2(LOW)	OFF
2,3(HI)	ON

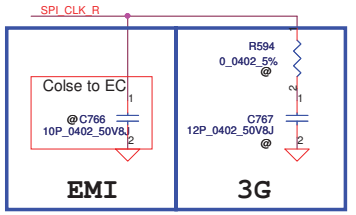


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2010/04/30

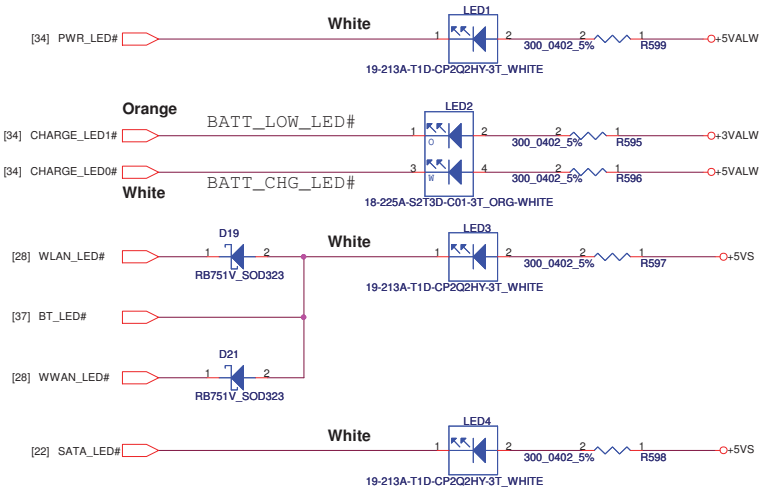
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010		Sheet 35 of 48	

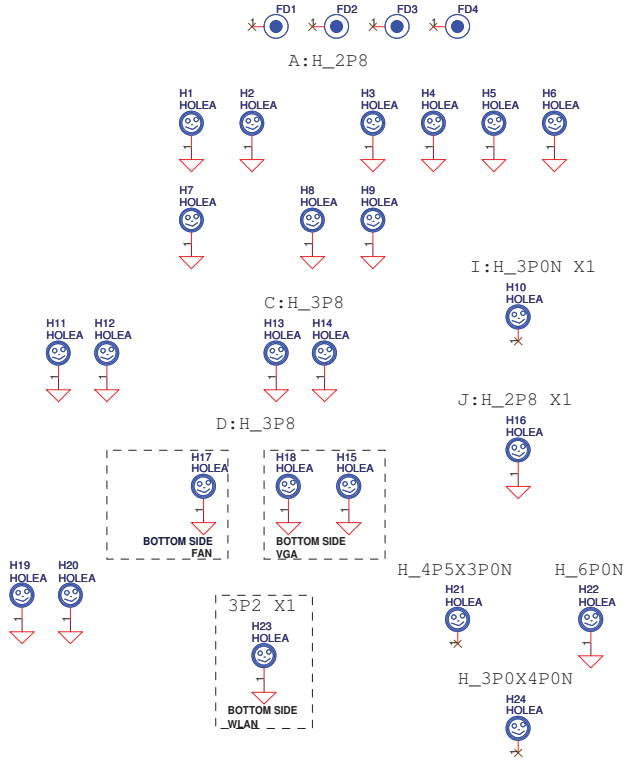
SA00002TO00 pakage 200mil
S IC FL 16MBIT MX25L1605AM2C-12G SO8 ROM

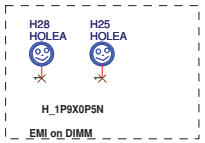




LED







Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2010/04/30

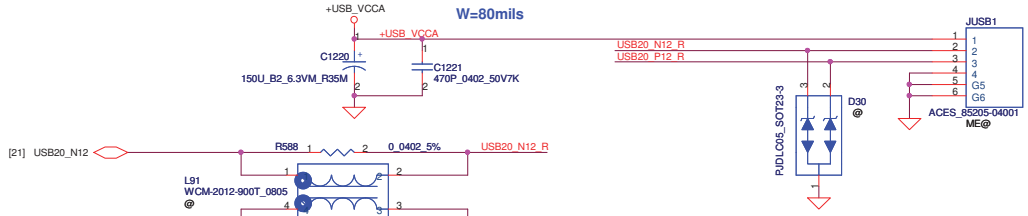
Compal Electronics, Inc.

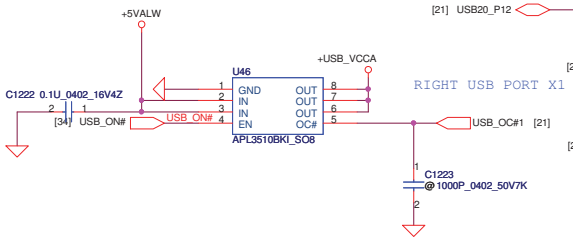
Title: LED/EC SPI ROM

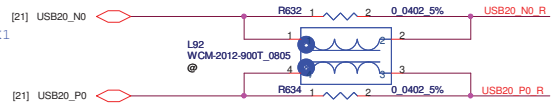
Size: B | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 36 of 48

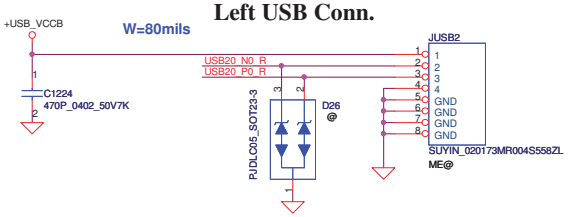
Right USB Conn.





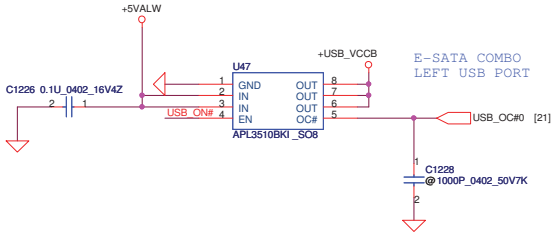


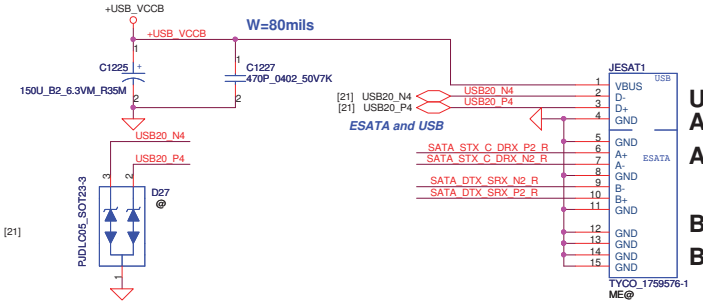
Left USB Conn.

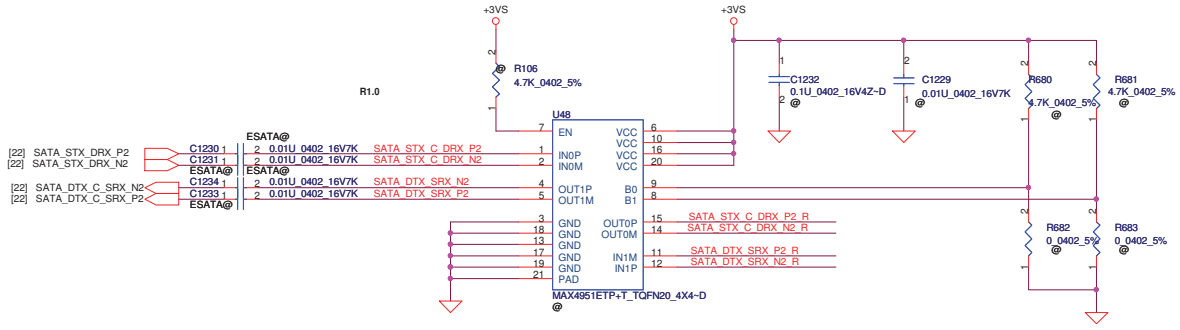


USB power switch need update symbol
to SA000039E00(Low enable)

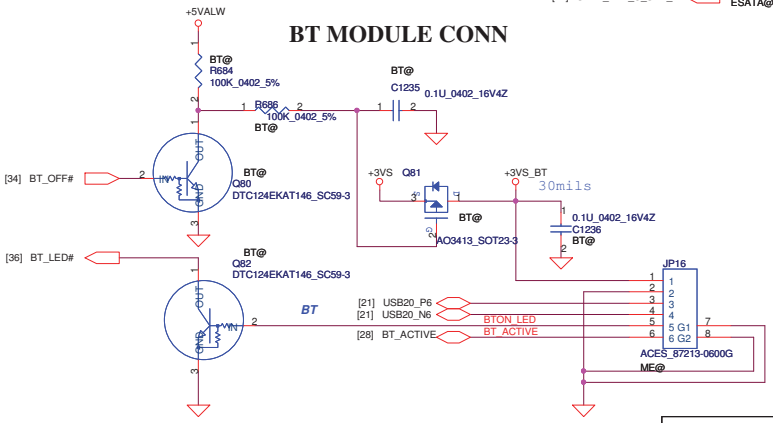
ESATA and USB Conn.







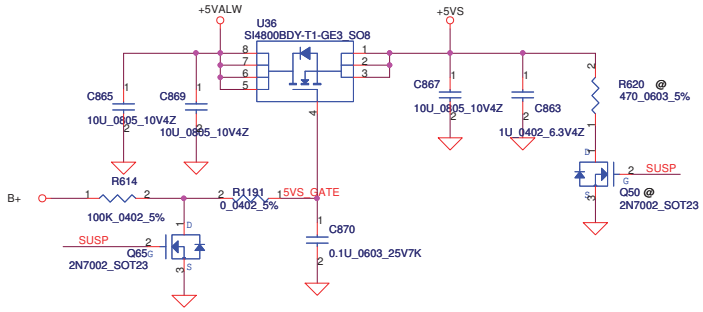
BT MODULE CONN



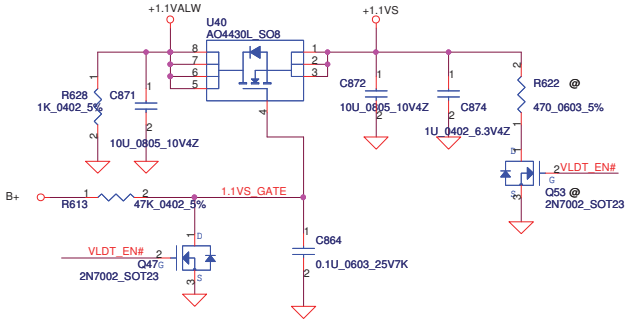
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2010/04/30

Compal Electronics, Inc.	
Title	USB ports/BT/E-SATA
Size: Custom	Document Number: NAWE5 LA-5753P
Rev	1.A
Date: Tuesday, May 18, 2010	Sheet 37 of 48

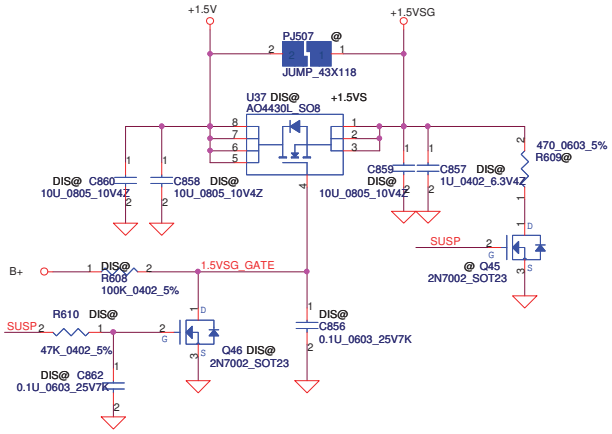
+5VALW TO +5VS



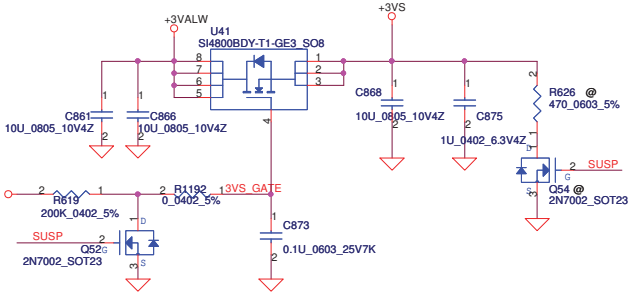
+1.1VALW TO +1.1VS (NB HT)

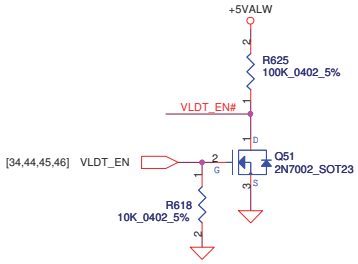


+1.5V to +1.5VSG

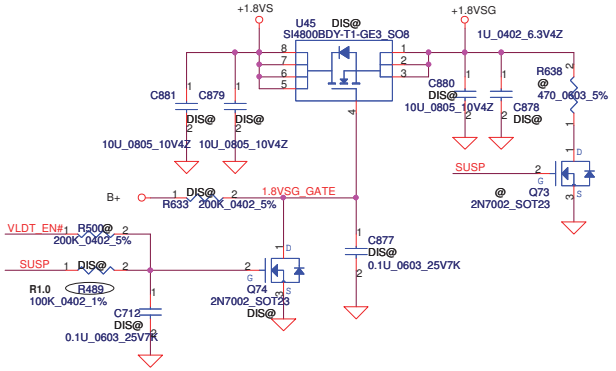


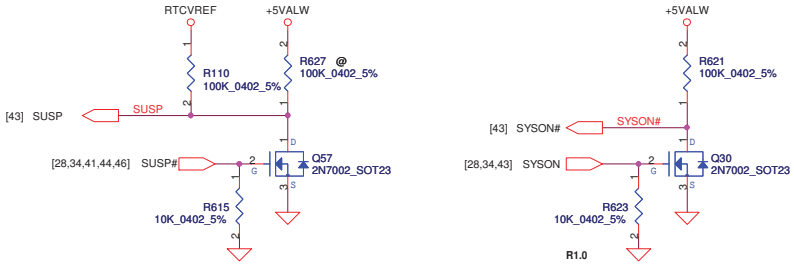
+3VALW TO +3VS



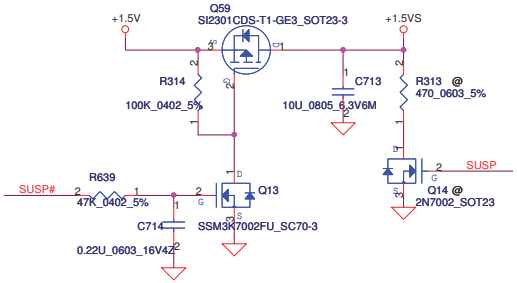


+1.8VS to +1.8VSG

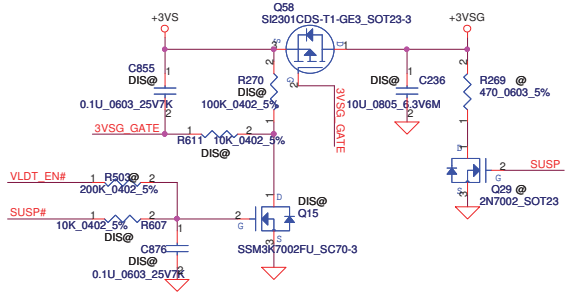


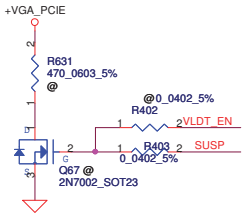


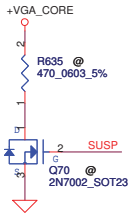
+1.5VS

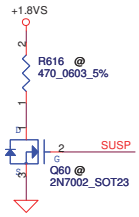


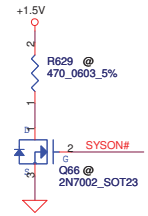
+3VSG

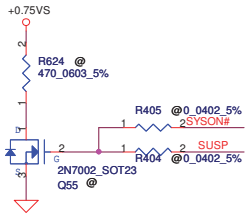


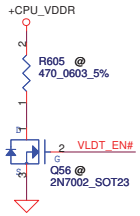


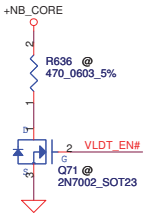


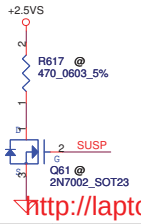












Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: NAWE5 LA-5753P | Rev: 1.A

Date: Tuesday, May 18, 2010 | Sheet 38 of 48

DC030006J00

VIN

PF101 7A_24VDC_429007.WRML

PL101 SMB3025500YA_2P

APDIN APDIN1

@4602-Q04C-09R 4P P2.5 JDCIN

PC101 @ 0.1U_0603_25V7K
PC102 1000P_0402_50V7K
PC103 100P_0402_50V8J
PC104 @ 0.1U_0603_25V7K
PC105 100P_0402_50V8J
PC106 1000P_0402_50V7K

ACIN

Precharge detector	Min.	typ.	Max
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Vin Detector	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

PR101 1K_1206_5%
PR102 1K_1206_5%
PR103 1K_1206_5%
PD101 LL4148_LL34-2
PQ101 TP0610K-T1-E3_SOT23-3
PR104 100K_0402_1%
PR105 100K_0402_1%
PR106 100K_0402_1%
PQ102 DDTC115EUA-7-F_SOT323-3
[34,41] ACOFF
PQ103 DDTC115EUA-7-F_SOT323-3
B+

PR107 1M_0402_1%
VINDE-2
VS
PC107 0.01U_0402_25V7K
PR108 84.5K_0402_1%
PR111 22K_0402_1%
VINDE-1
VINDE-3
PC108 0.068U_0603_16V7K
PR112 20K_0402_1%
PC109 0.1U_0402_16V7K
PU101A LM393DG_SO8
PR109 10K_0805_5%
PR110 10K_0402_1%
ACIN [14,34]
PACIN
PACIN [41]
PD102 LLZ4V3B_LL34-2
PR114 10K_0402_5%
PR115 10K_0402_5%
RTCVREF
3.3V

VL
PR113 2.2M_0402_5%
PR117 100K_0402_1%
PR116 499K_0402_1%
[6,40,42] MAINPWON
[41] ACON
PD103 BAS40CW_SOT323-3
PU101B LM393DG_SO8
PC113 0.1U_0603_25V7K
PC111 1000P_0402_50V7K
PR118 205K_0402_1%
PR119 499K_0402_1%
PC112 0.01U_0402_25V7K
PRG++
PR124 10K_0402_5%
RTCVREF
PQ105 2N7002KW_SOT323-3
PR125 47K_0402_5%
PACIN [41]
PQ106 DDTC115EUA-7-F_SOT323-3
+5VALW

VIN
PD104 LL4148_LL34-2
51ON-1
PR121 68_1206_5%
PR122 68_1206_5%
BATT+
PD105 LL4148_LL34-2
PQ104 TP0610K-T1-E3_SOT23-3
PR123 200_0603_5%
CHGRTCP
51ON-2
VS
PR126 100K_0402_1%
PC114 0.22U_0603_25V7K
PR127 22K_0402_1%
[32] 51_ON#
51ON-3
PC115 0.1U_0603_25V7K

JRTC
@MAXEL_ML1220T10
PR129 560_0603_5%
+RTCBATT
PD106 RB751V-40_SOD323-2
+CHGRTC
RTC Battery

RTCVREF
+CHGRTC
PR130 560_0603_5%
3.3V
PU102 G920AT24U_SOT89-3
OUT
IN
GND
2CHGRTON
PR128 200_0603_5%
PC116 10U_0603_6.3V6M
PC117 1U_0805_25V6K

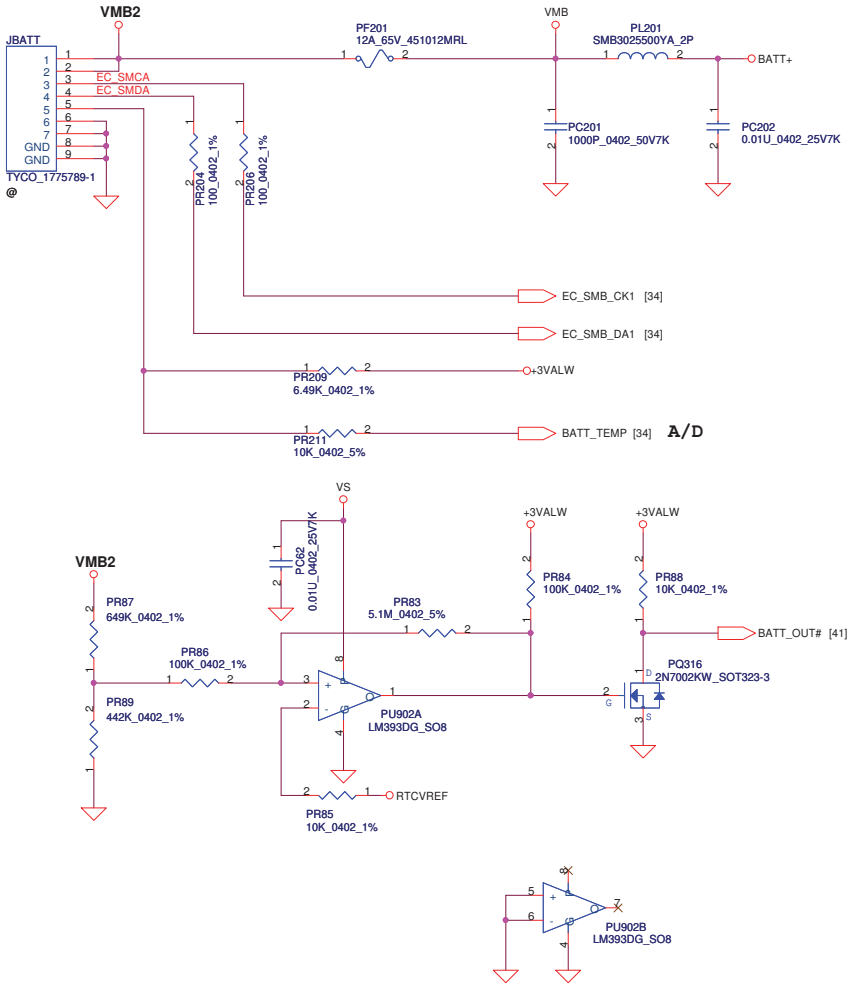
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

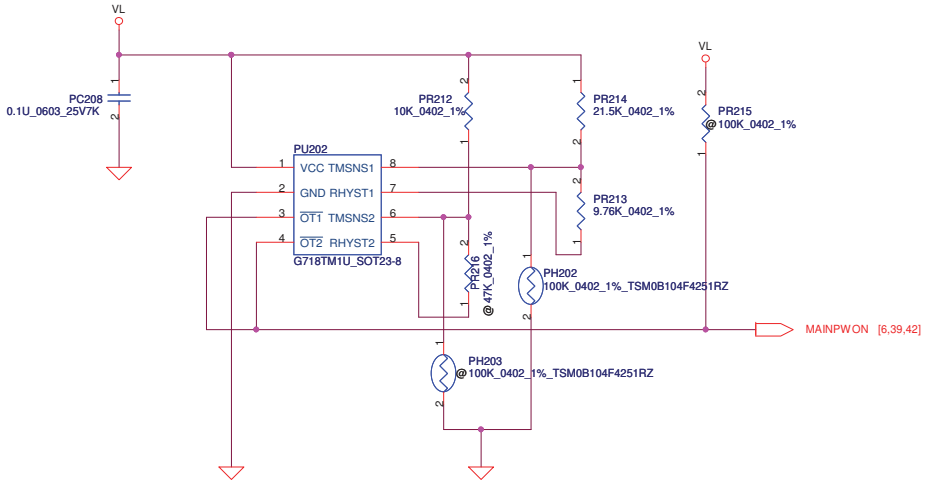
Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, May 18, 2010 Sheet 39 of 48



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



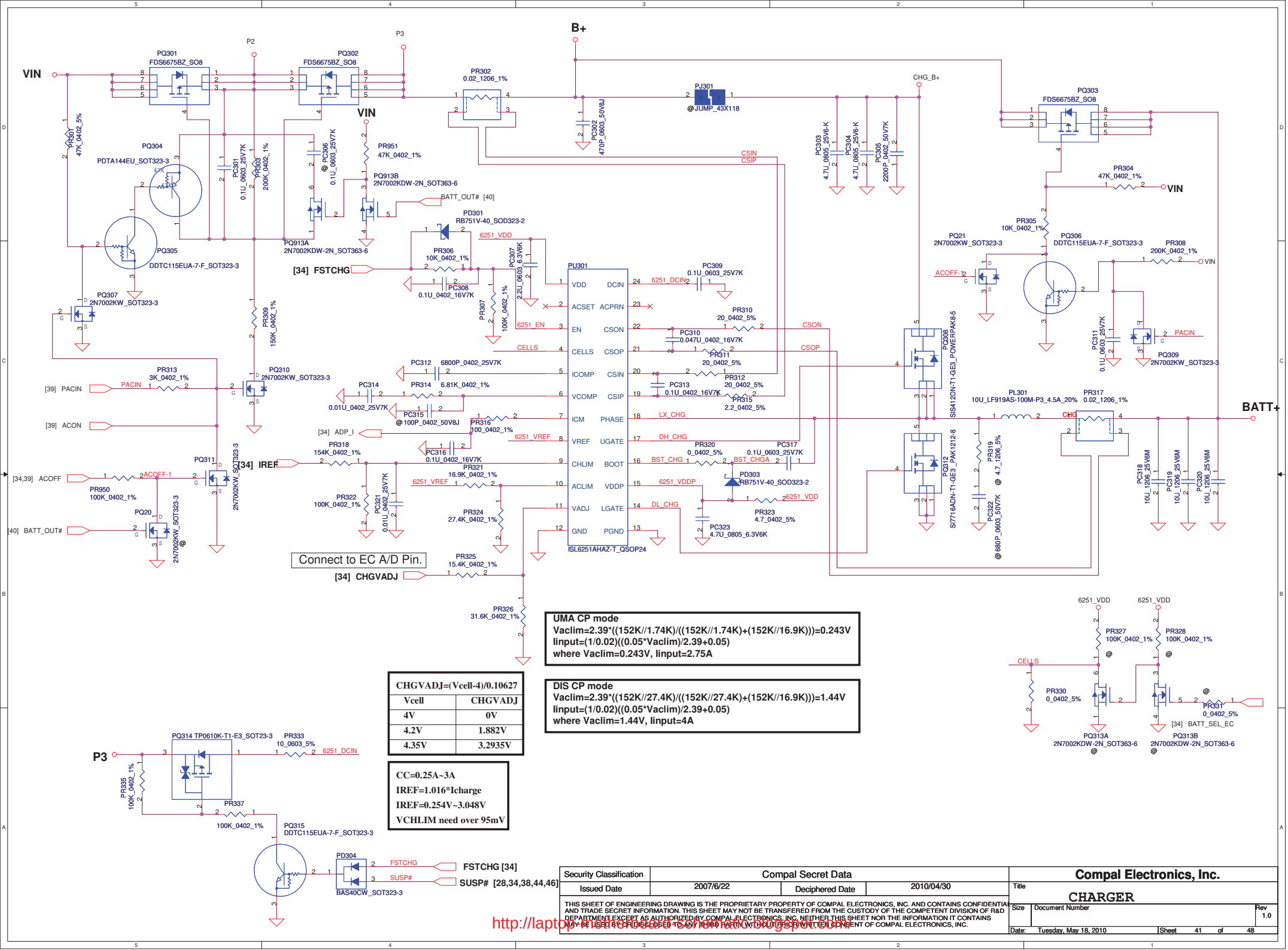
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		1.0

Date: Tuesday, May 18, 2010 | Sheet 40 of 48



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

UMA CP mode
Vaclim=2.39*((152K//1.74K)/((152K//1.74K)+(152K//16.9K)))=0.243V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.243V, Iinput=2.75A

DIS CP mode
Vaclim=2.39*((152K//27.4K)/((152K//27.4K)+(152K//16.9K)))=1.44V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=1.44V, Iinput=4A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

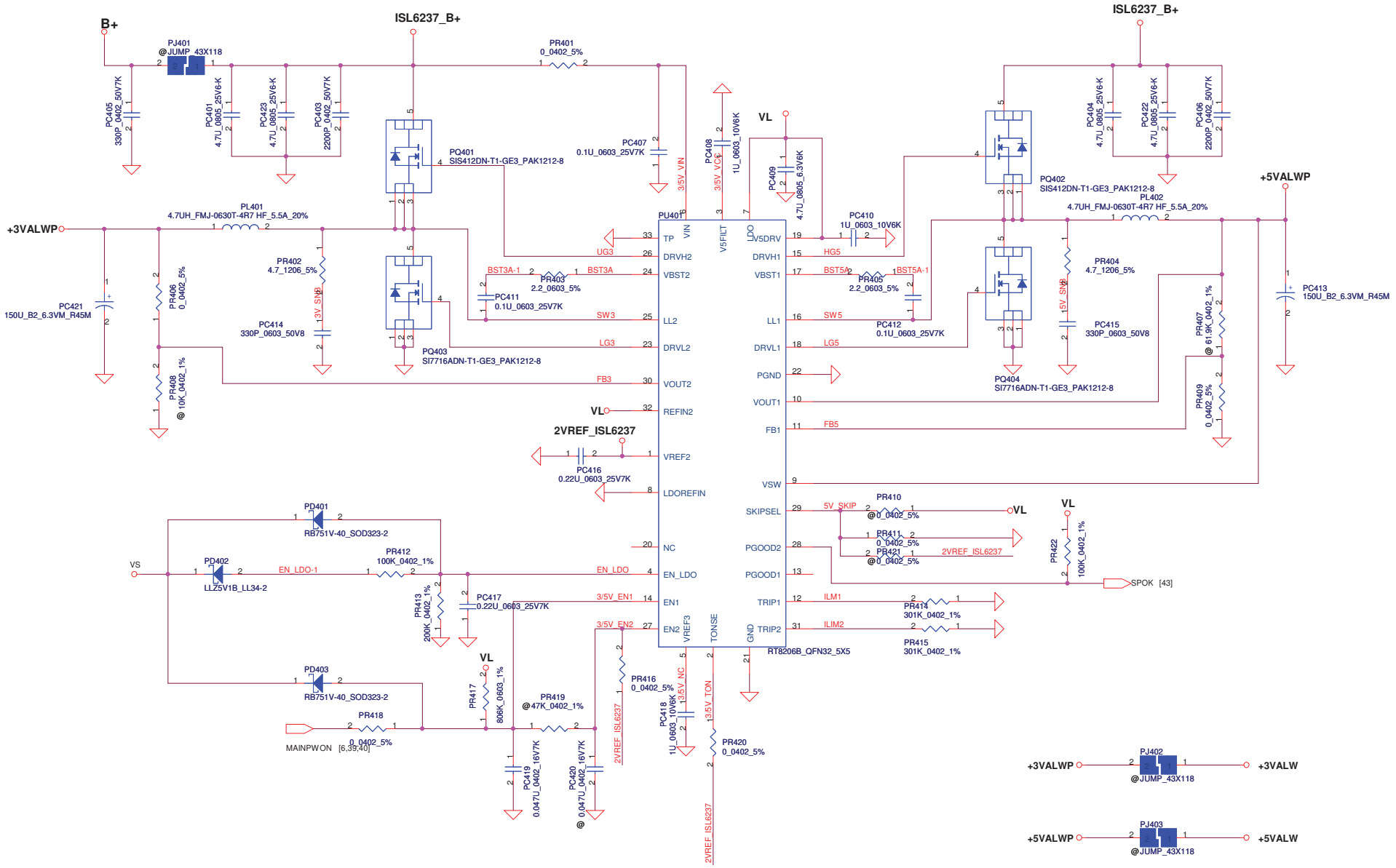
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: | Rev: 1.0

Date: Tuesday, May 18, 2010 | Sheet 41 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/04/30

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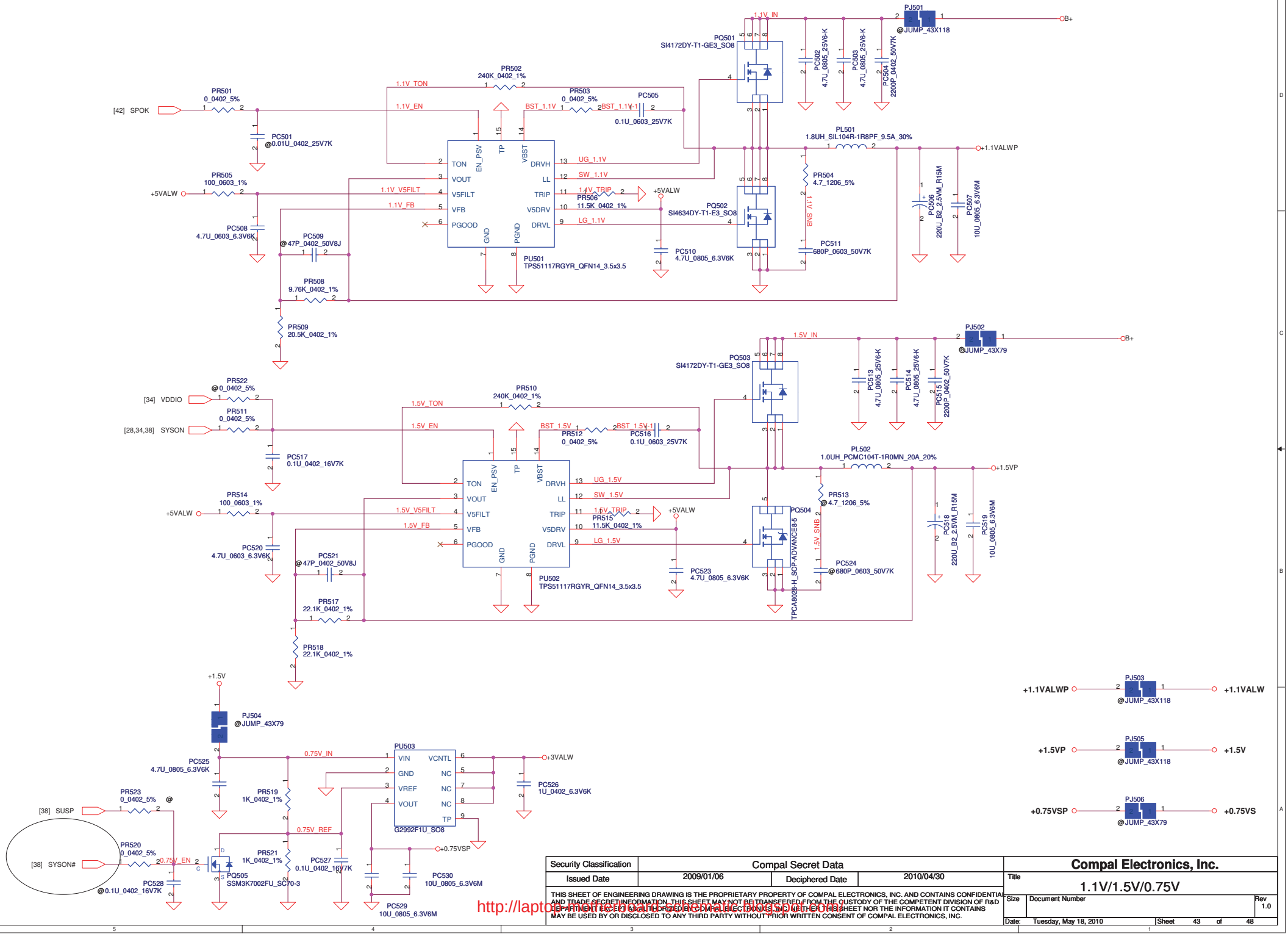
Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, May 18, 2010 | Sheet 42 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/04/30

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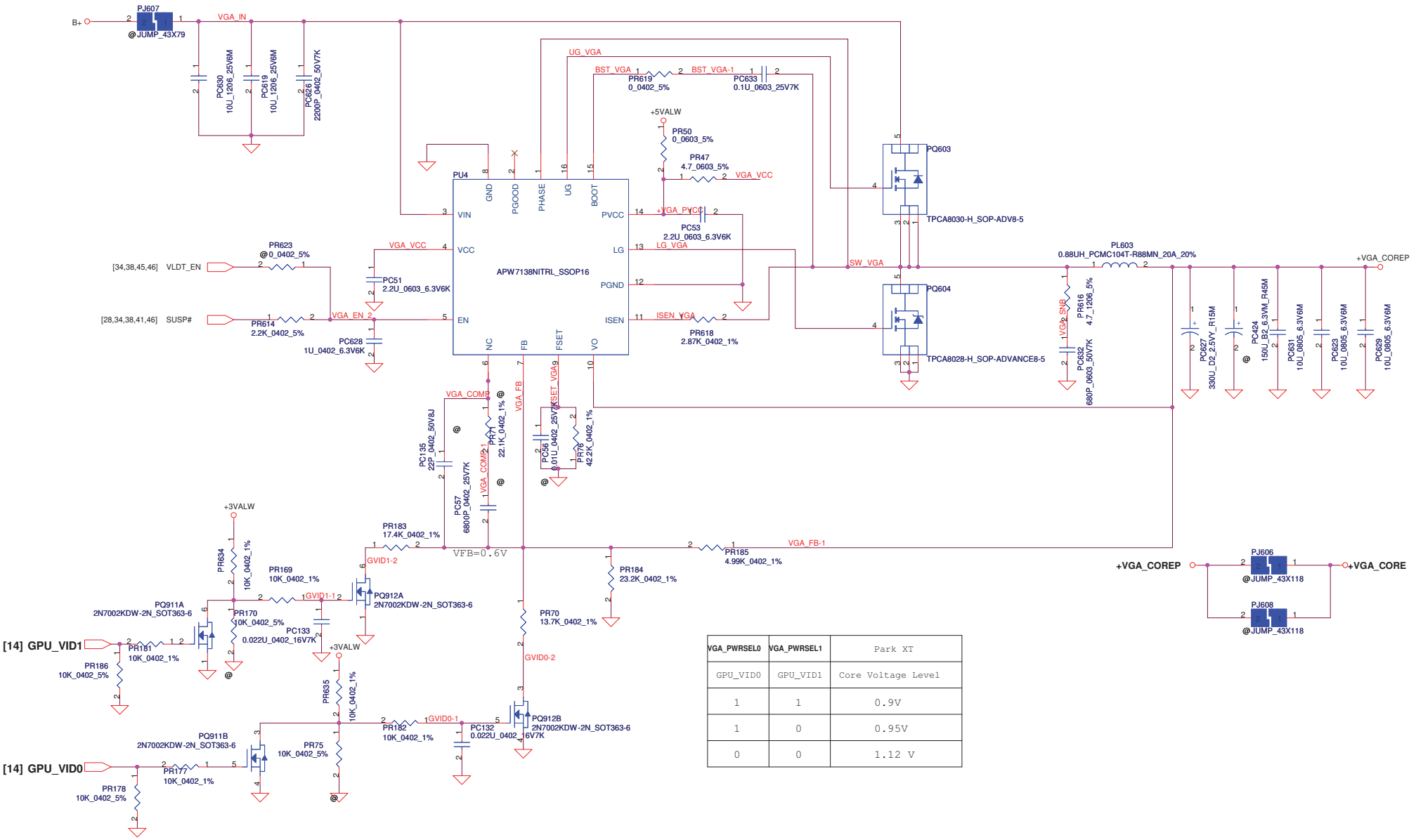
Compal Electronics, Inc.

Title: 1.1V/1.5V/0.75V

Size | Document Number | Rev 1.0

Date: Tuesday, May 18, 2010 | Sheet 43 of 48



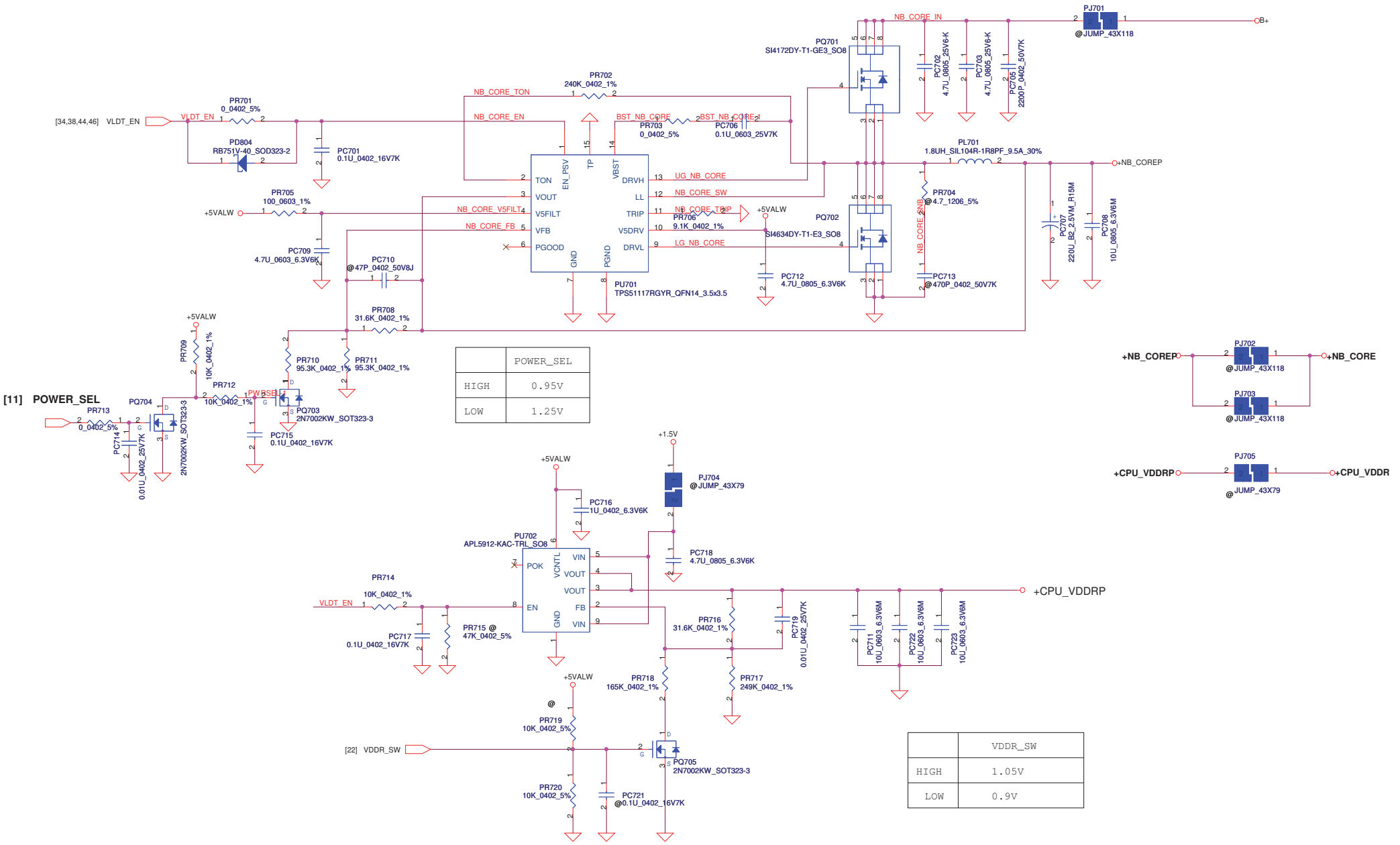
VGA_PWRSEL0	VGA_PWRSEL1	Park XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V

Compal Electronics, Inc.

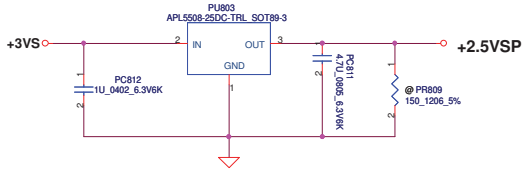
Title: 1.5V/VGA_CORE

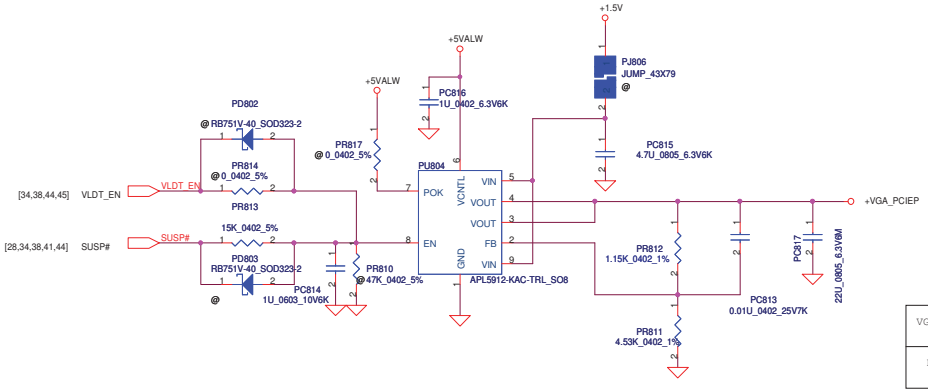
Size	Document Number	Rev
		1.0

Date: Tuesday, May 18, 2010 | Sheet 44 of 48

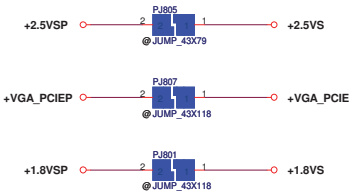


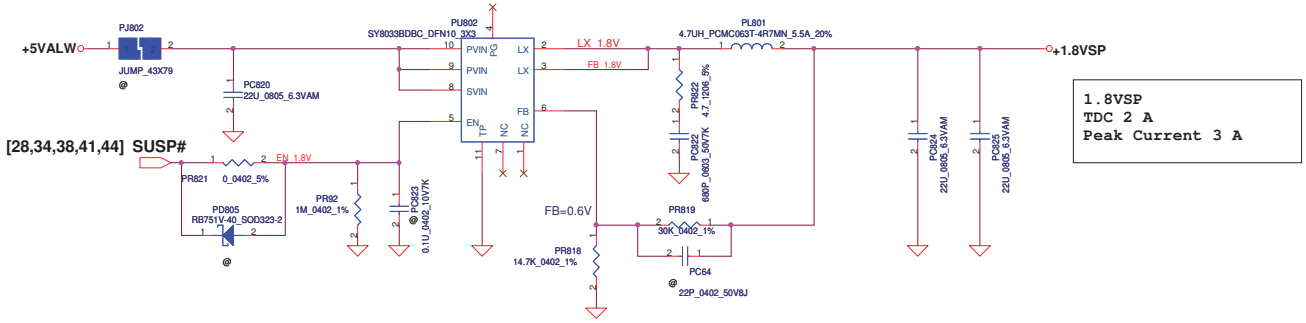
Compal Electronics, Inc.			
Title	+NB_CORE		
Size: Custom	Document Number		Rev: 1.0
Date: Tuesday, May 18, 2010	Sheet 45 of 48		





VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K





1.8VSP
TDC 2 A
Peak Current 3 A

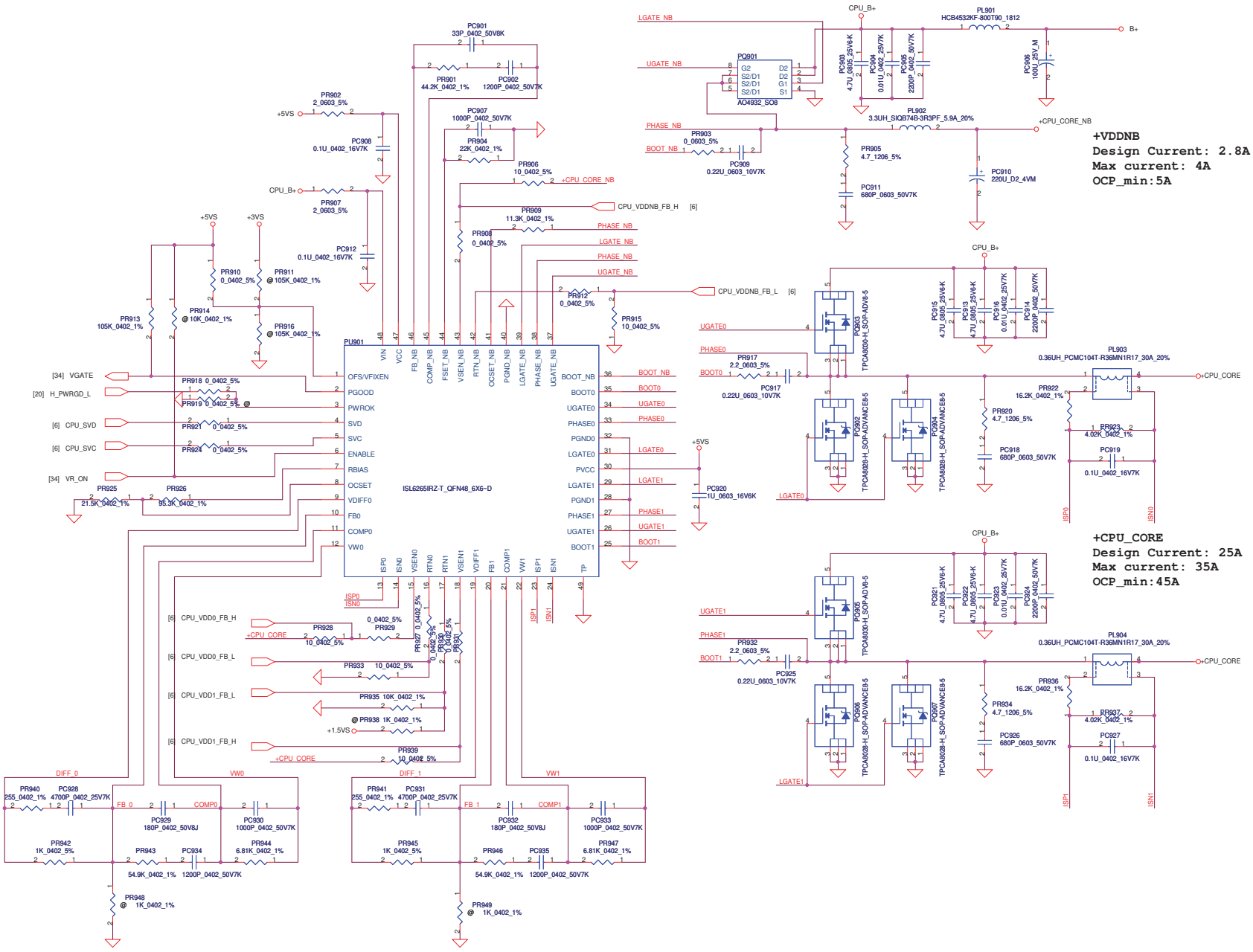
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/04/30

Compal Electronics, Inc.

Title: 2.5VS/PCIE/1.8VS

Size	Document Number	Rev
		1.0

Date: Tuesday, May 18, 2010 Sheet 46 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/04/30

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Compal Electronics, Inc.			
Title: CPU_CORE			
Size	Document Number		Rev 1.0
Date: Tuesday, May 18, 2010	Sheet 47 of 48		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Del NC parts	cpu internal sensor & debug port parts NC	0.2	6	Del U2,R41,R42,C22,Q2,Q3	2010-02-24	PVT_NAWE5
2	Add Park HDMI strap pin	DIS park HDMI abnomal	0.2	14	Add R120,121 (10k.0402)	2010-02-24	PVT_NAWE5
3	EMC1412-A address resister	Reserve thermal sensor address	0.2	14	Add R637 (4.7k.0402)	2010-02-24	PVT_NAWE5
4	change to Interanl clk GEN	modify Interanl clk PU resister	0.2	19	change R219,R220,R221,R222 Pin 2 from +3VS_CLK to +3VS	2010-02-24	PVT_NAWE5
5	change to Interanl clk GEN	using internal CLK GEN	0.2	19	Del EXT@ parts to INT@ parts	2010-02-24	PVT_NAWE5
6	change new card PCIE	new card pcie port from NB to SB	0.2	20	PCIE_SB_EXPCARD_TXP;PCIE_SB_EXPCARD_TXN PCIE_EXPCARD_SB_RXP;PCIE_EXPCARD_SB_RXN	2010-02-24	PVT_NAWE5
7	Reserve UMA/DIS HDMI strap pin	BIOS demand	0.2	21	add R366;R370 (10k,0402)	2010-02-24	PVT_NAWE5
8	new card function	ADD CPUSB# signal	0.2	21	add R545 (0R.0402)	2010-02-24	PVT_NAWE5
9	Change Cap footprint size	Change footprint for ME interfere	0.2	23	change C590,,C617,C618 from 10uF.0805 to 0603	2010-02-24	PVT_NAWE5
10	Change Cap footprint size	Change footprint for ME interfere	0.2	23	C591,C595,22uF Change to 10uF0603	2010-02-24	PVT_NAWE5
11	change R431 location	modify BKOFF# PD resister	0.2	27	R431 (10k.0402)	2010-02-24	PVT_NAWE5
12	Add LCD_ENVDD PD Resister	to prevent LCD flicker issue	0.2	27	add R432 (2.2k.0402)	2010-02-24	PVT_NAWE5
13	disable VARY_ BL Function	back light controll change to EC	0.2	27	add 451 (0ohm.0402) del R450;R452(0ohm.0402)	2010-02-24	PVT_NAWE5
14	Mimi card leakage issue	fix Intel WLAN card leagage issue	0.2	28	Add R719 (100k.0402) add R660;R661(100ohm.0402)	2010-02-24	PVT_NAWE5
15	reserve resister for Intel WLAN	for Intel WLAN LED use	0.2	28	add R658 (0ohm.0402)	2010-02-24	PVT_NAWE5
16	change CLKREQ_LAN# PU resister	flash Lan MAC sometime has fail	0.2	29	Add R254 (4.7k.0402) del R219 (8.2k.0402)	2010-02-24	PVT_NAWE5
17	Del LAN NC parts	disable EN_WOL# Function	0.2	29	del Q43,R274,C495,Q42,C496	2010-02-24	PVT_NAWE5
18	LAN Cystal accurate	modify cystal 25MHz of CAP	0.2	29	change C203,C202 from(27pF to 33pF.0402)	2010-02-24	PVT_NAWE5
19	codec common design	codec Internal MIC cap del	0.2	33	Add R612 (0ohm.0402) Del (C516 2.2uF.0603)	2010-02-24	PVT_NAWE5
20	KBC Cystal accurate	modify cystal 32.768KHz of CAP	0.2	34	change C730,C733 from(15pF to 27pF.0402)	2010-02-24	PVT_NAWE5
21	change ROM footprint	ROM pakage from 150mil to 200mil	0.2	36	change U30 pakage size	2010-02-24	PVT_NAWE5
22	BT_LED controll	BT_LED no need diode	0.2	36	Del D20	2010-02-24	PVT_NAWE5
23	leakage issue	fix +3VS leakage	0.2	38	Del R627 (100k,0402) add R110 (100k,0402)	2010-02-24	PVT_NAWE5
24	Disable discharge circuit	NC discharge circuit parts	0.2	38	del R620,Q50,R626,Q54,R622,Q53,R313,Q14,R638,Q73, R269,Q29,R631,Q67,R635,Q70,R616,Q60,R617,Q61, R636,Q71,R605,Q56,R404,R624,Q55,R629,Q66	2010-02-24	PVT_NAWE5
25	Del L28 220 ohm bead	NC part	1.0	12	del L28	2010-02-24	MP_NAWE5
26	Del test Resister	Del test 0 ohm Resister	1.0	23,28, 32,35	R447;R4448;R586;R662;R646;R440,R372,R373,R374,R375	2010-04-28	MP_NAWE5
27	Reserve JP6 for LED of Num/Cap	For NAWE7 power b/d co-lay	1.0	38	Add JP6 Location,ADD R637 100k ohm	2010-04-28	MP_NAWE5
28	ADD R430 0ohm , Del U21	reserve RST_buffer	1.0	20	ADD R430 , Del U21	2010-04-28	MP_NAWE5
29	For VGA timing	for VGA timing delay +1.8VS	1.0	38	Change R489 from 84.5K to 100K	2010-04-28	MP_NAWE5
30	Add C652 & C653 33pF	EMI demand	1.0	32	Add C652 & C653 33pF	2010-04-28	MP_NAWE5
31	Change C189 from 330uF to 220uF	change +NB_CORE CAP	1.0	12	Change C189 from 330uF to 220uF	2010-04-28	MP_NAWE5

Compal Electronics, Inc.			
Title: PIR (HW)			
Size: Custom	Document Number: NAWE5 LA-5753P		Rev: 1.A
Date: Tuesday, May 18, 2010	Sheet 48 of 48		