

# KIWA5/A6

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM/PM+ICH9-M core logic

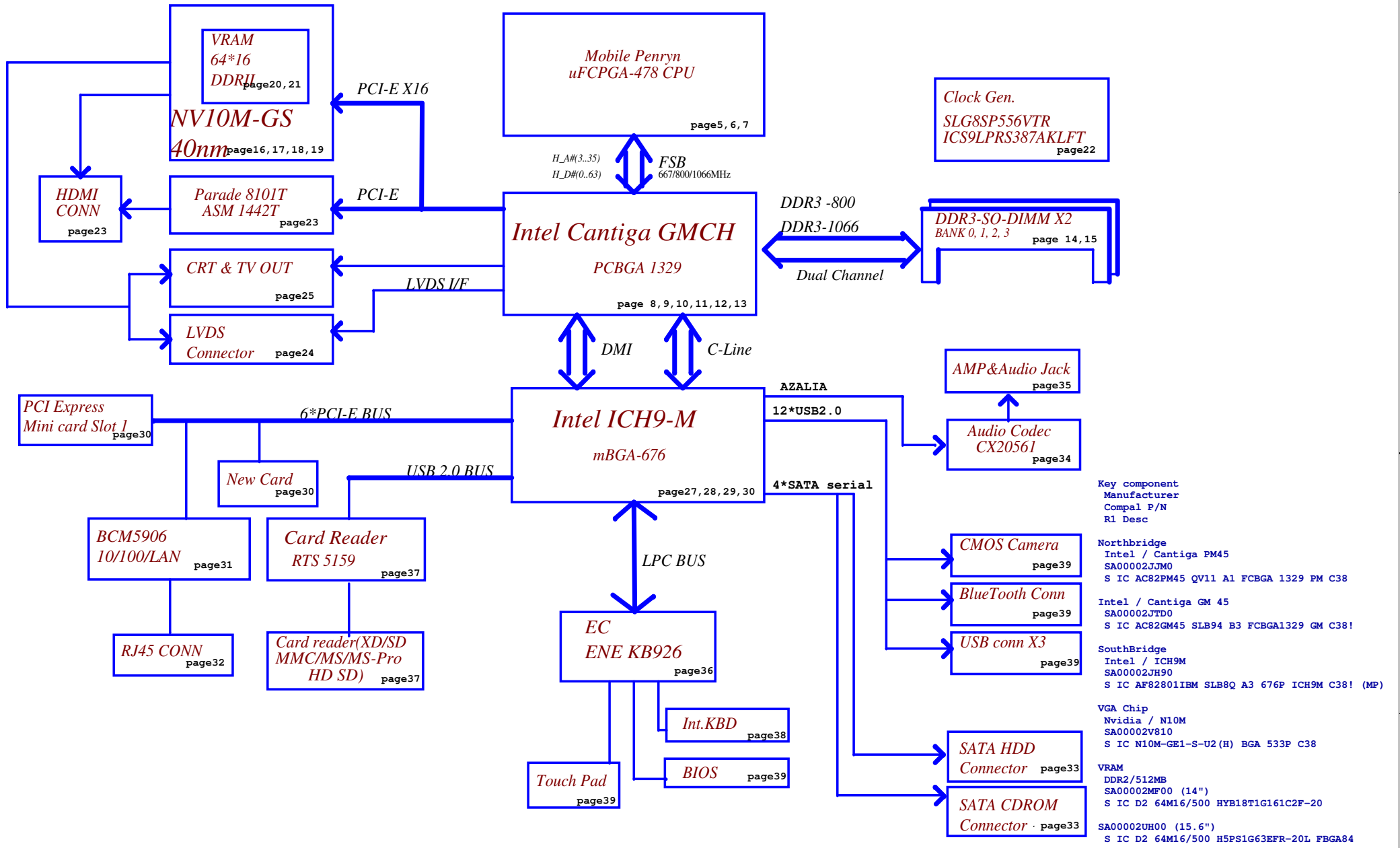
REV: 1.0

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				B	<b>KIWAX LA-5081P</b>
				Date: Tuesday, April 28, 2009	Sheet 1 of 51



**POWER Board**

**CAP SENSE LEDs Board**



- Key component  
 Manufacturer  
 Compal P/N  
 RI Desc
- Northbridge  
 Intel / Cantiga PM45  
 SA00002JJM0  
 S IC AC82PM45 QV11 A1 FCBGA 1329 PM C38
  - Intel / Cantiga GM 45  
 SA00002JTD0  
 S IC AC82GM45 SLB94 B3 FCBGA1329 GM C38!
  - SouthBridge  
 Intel / ICH9M  
 SA00002JH90  
 S IC AF82801IBM SLB8Q A3 676P ICH9M C38! (MP)
  - VGA Chip  
 Nvidia / N10M  
 SA00002V810  
 S IC N10M-GE1-S-U2(H) BGA 533P C38
  - VRAM  
 DDR2/512MB  
 SA00002MF00 (14")  
 S IC D2 64M16/500 HYB18T1G161C2F-20  
 SA00002UH00 (15.6")  
 S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

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Size	Document Number	Rev	Date: Tuesday, April 28, 2009   Sheet 2 of 51			
Custor	KIWAX_LA-5081P	1.0				

# DDR3 Voltage Rails

power plane State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS <b>+0.75VS</b> +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
EC_SMB_CK2 EC_SMB_DA2	KB926	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
ICH_SMBCLK ICH_SMBDAT	ICH9	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
LVDS_SCL LVDS_SDA	Cantiga	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
HDMICLK_NB HDMIDAT_NB	Cantiga	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
VGA_DDCLK VGA_DDCDATA	N10M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
VGA_LVDS_SCL VGA_LVDS_DAT	N10M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
VGA_HDMI_SCL VGA_HDMI_DAT (55nm)	N10M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
HDCP_SMB_CK1 HDCP_SMB_DA1	N10M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
IFPC_AUX IFPC_AUX_N (40nm)	N10M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗

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				Date: Tuesday, April 28, 2009	Rev 1.0
				Sheet 3 of 51	

# VGA and DDR2 Voltage Rails (N10M)

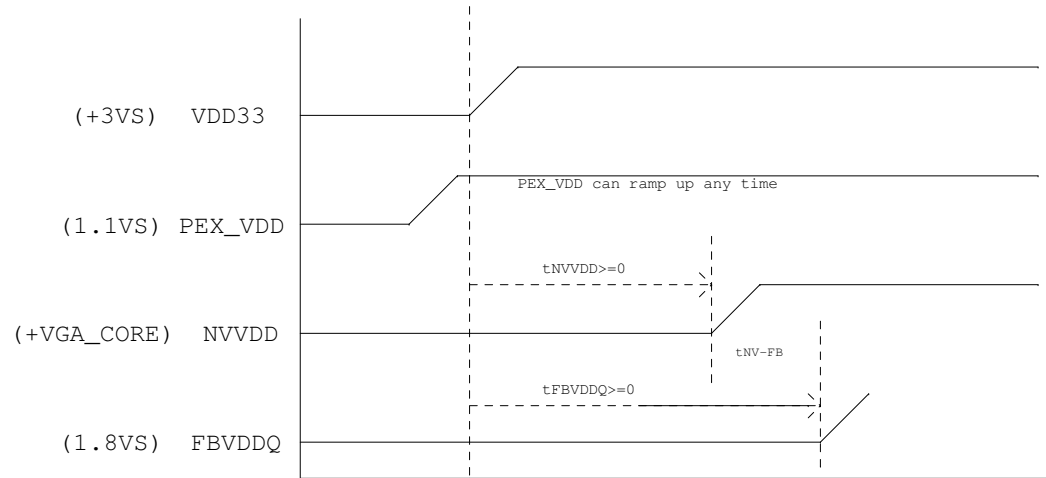
power plane	+3VS
	+VGA_CORE
State	+1.1VS
	+1.8VS
S0	○
S1	○
S3	✗
S5 S4/AC	✗
S5 S4/ Battery only	✗
S5 S4/AC & Battery don't exist	✗

# EDP at Tj = 97C\*

Power Supply Rail (V)		NB10M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
<b>TOTAL</b>	<b>1.1</b>	<b>3.425A</b>		<b>2.435A</b>	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
<b>TOTAL</b>	<b>1.8</b>	<b>2.76A</b>	<b>2.17A</b>	<b>2.575A</b>	<b>2.085A</b>
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
<b>TOTAL</b>	<b>3.3</b>	<b>0.445A</b>		<b>0.445A</b>	

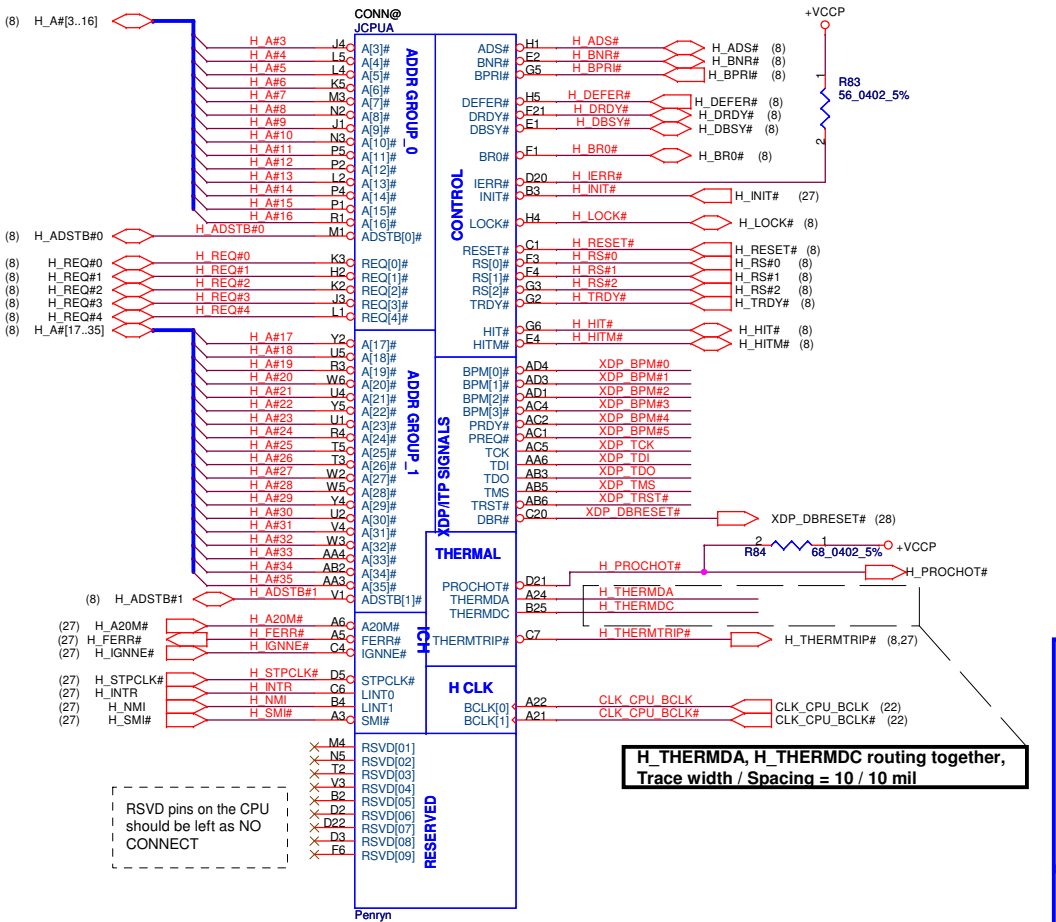
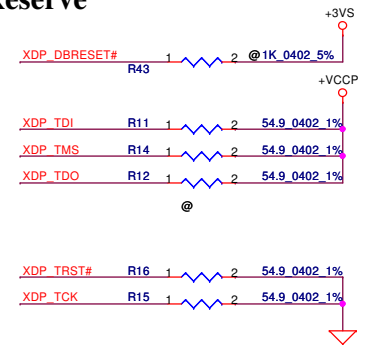
## POWER SEQUENCE

The ramp time for any rail must be more than 40us

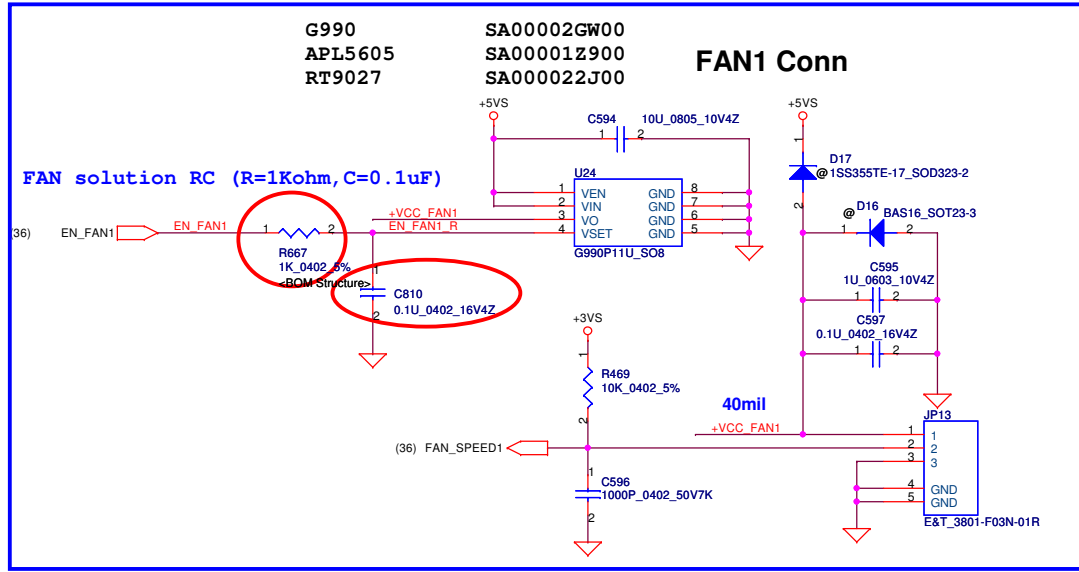
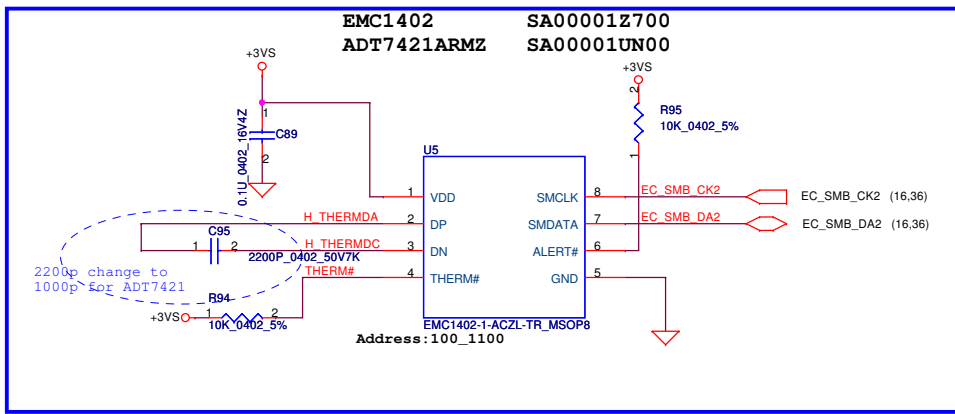


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				B	KIWA5/6 LA-5081P	1.0
				Date:	Tuesday, April 28, 2009	Sheet 4 of 51

# XDP Reserve

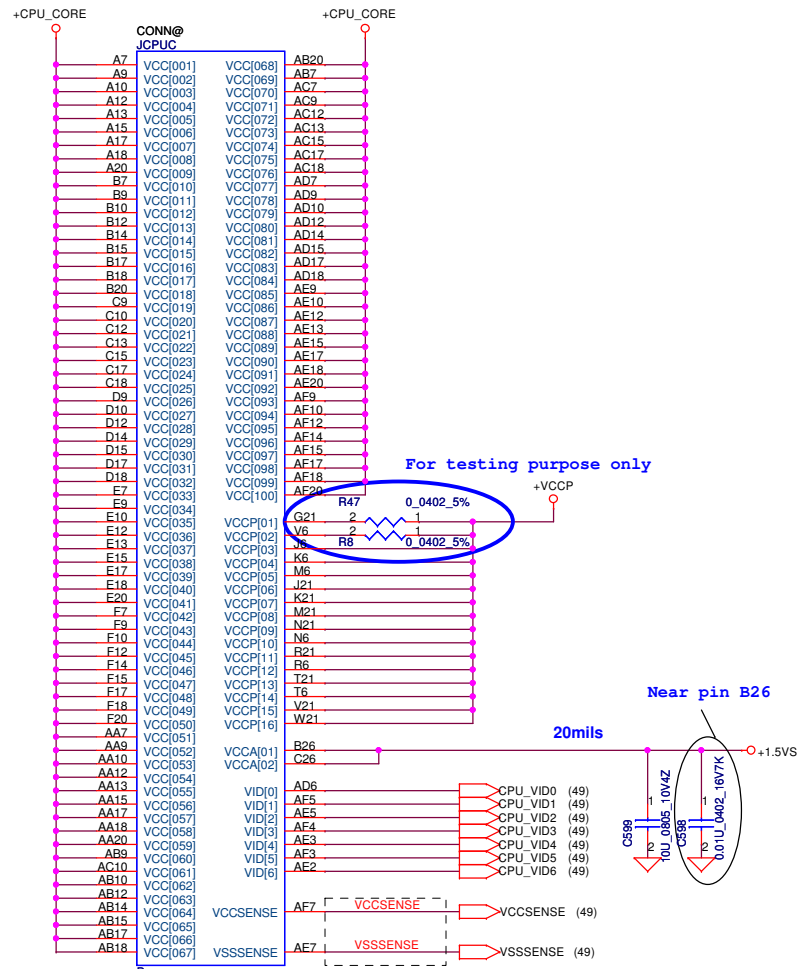
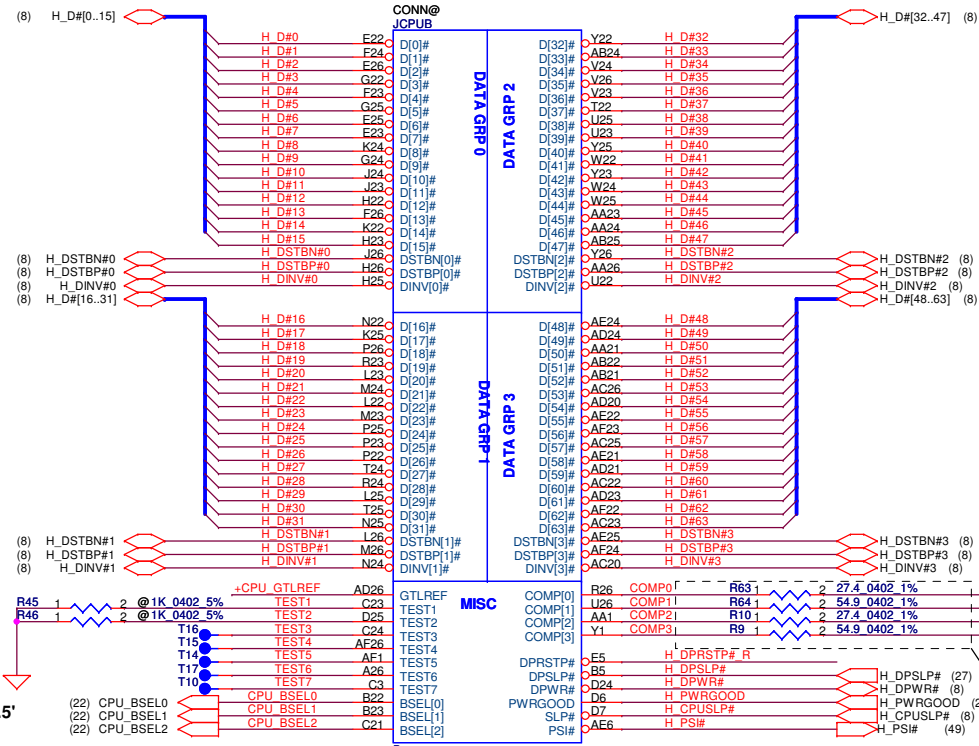


**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**



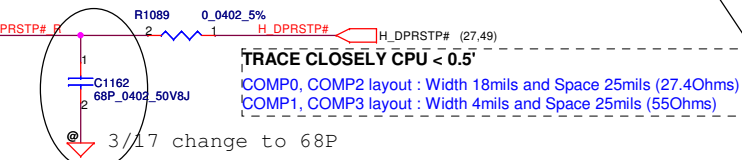
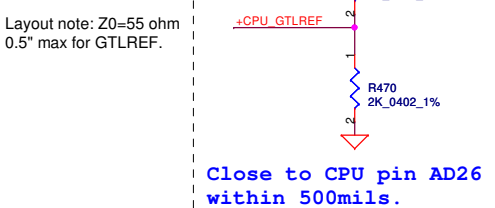
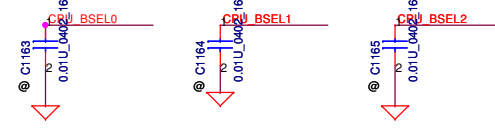
RSVD pins on the CPU should be left as NO CONNECT

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Size B	Document Number	Date		Rev	
	KIWAX_LA-5081P	Tuesday, April 28, 2009		1.0	
				Sheet 5 of 51	



Trace Close CPU < 0.5'

Width=4 mil ,  
Spacing: 15mil  
(55Ohms)

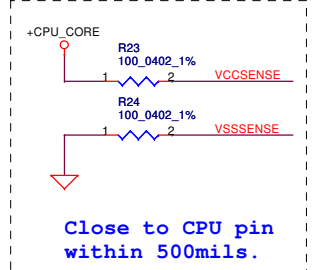


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

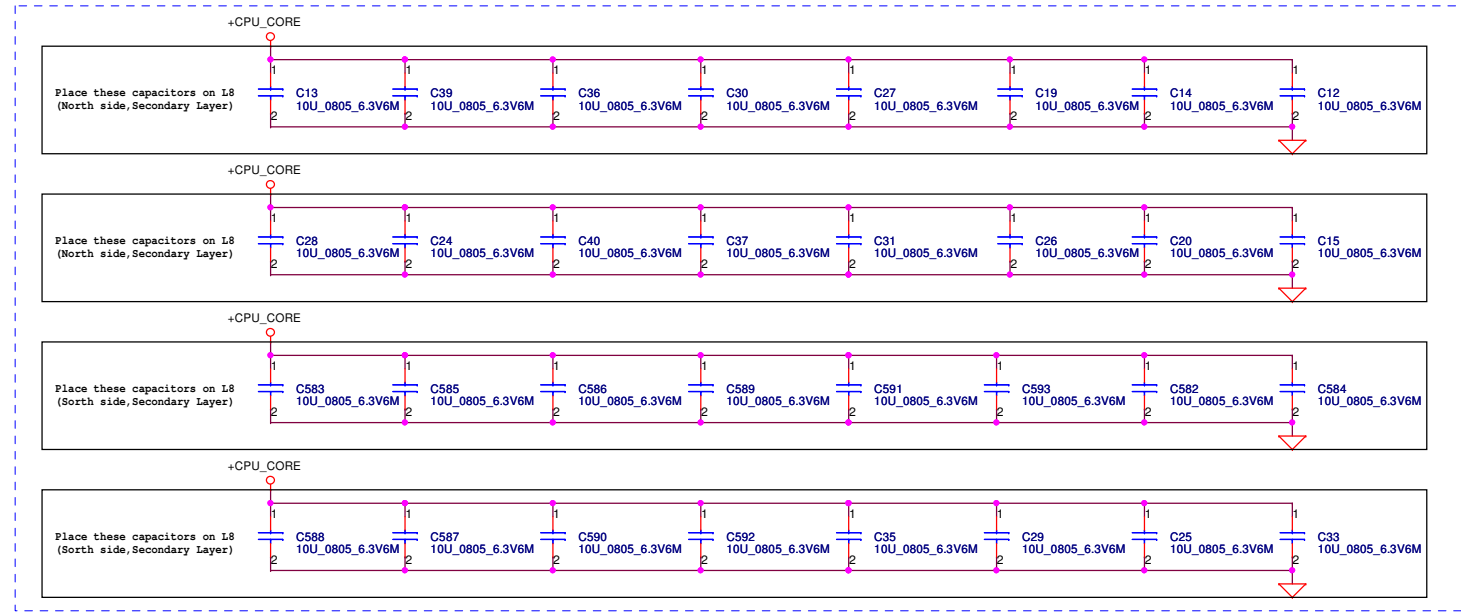
Length match within 25 mils.  
The trace width/space/other is 16/7/25.

Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.

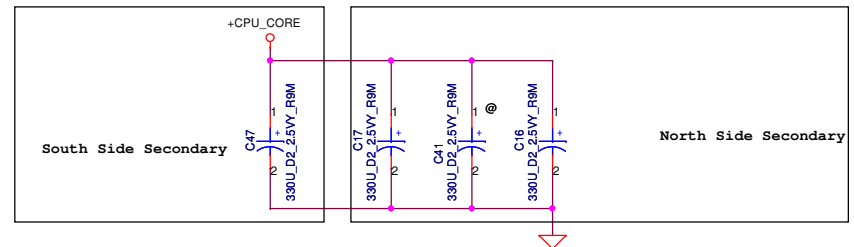


CONN@  
JCPU@

A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
BB	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	AF6
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N23	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
	VSS[082]	AF25

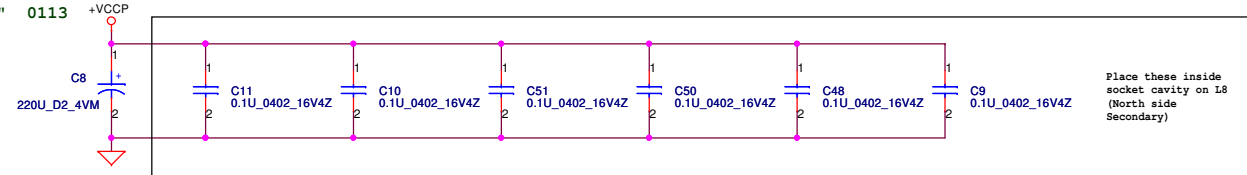


Mid Frequency Decoupling



ESR <= 1.5m ohm  
Capacitor > 1980uF

Delete "REMOVE?" 0113



Place these inside  
socket cavity on L8  
(North side  
Secondary)

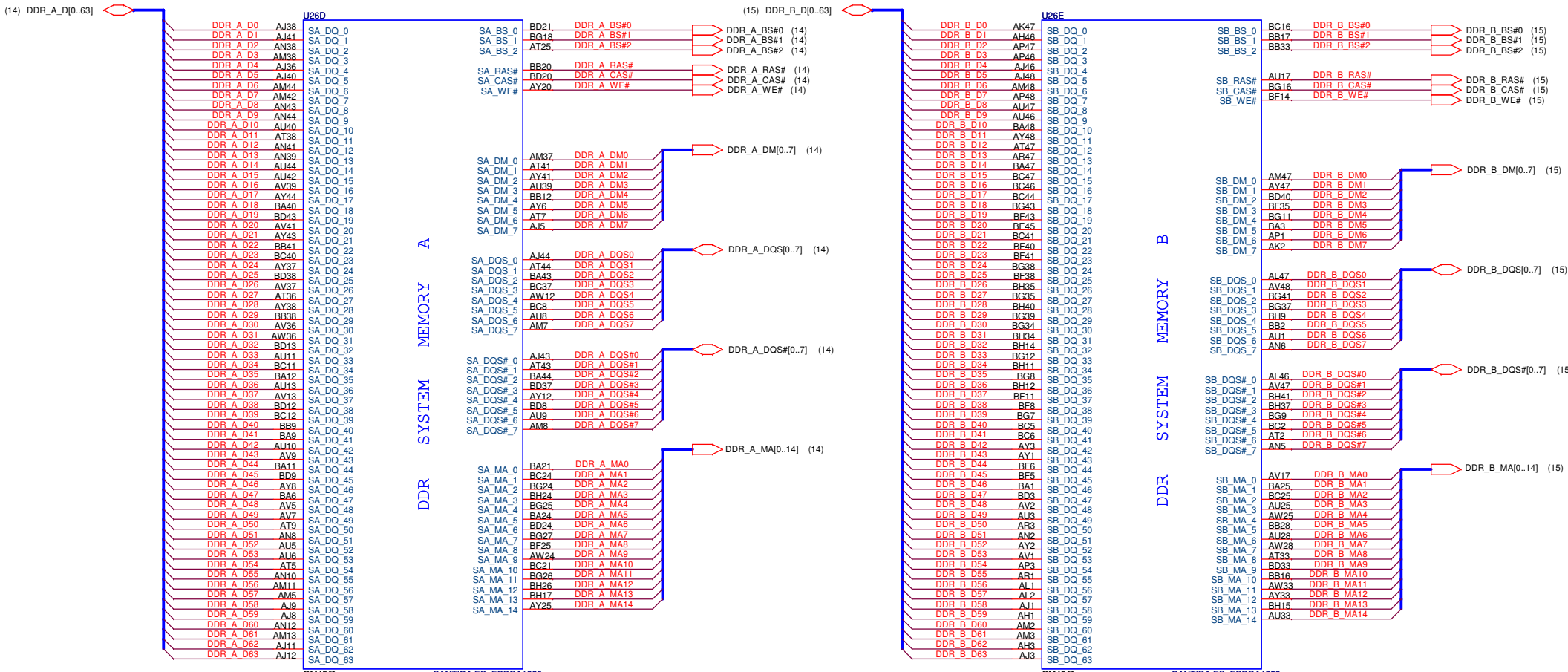
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				Date:	Tuesday, April 28, 2009
				Sheet	7 of 51

Penryn (3/3)  
Rev 1.0









GM45@

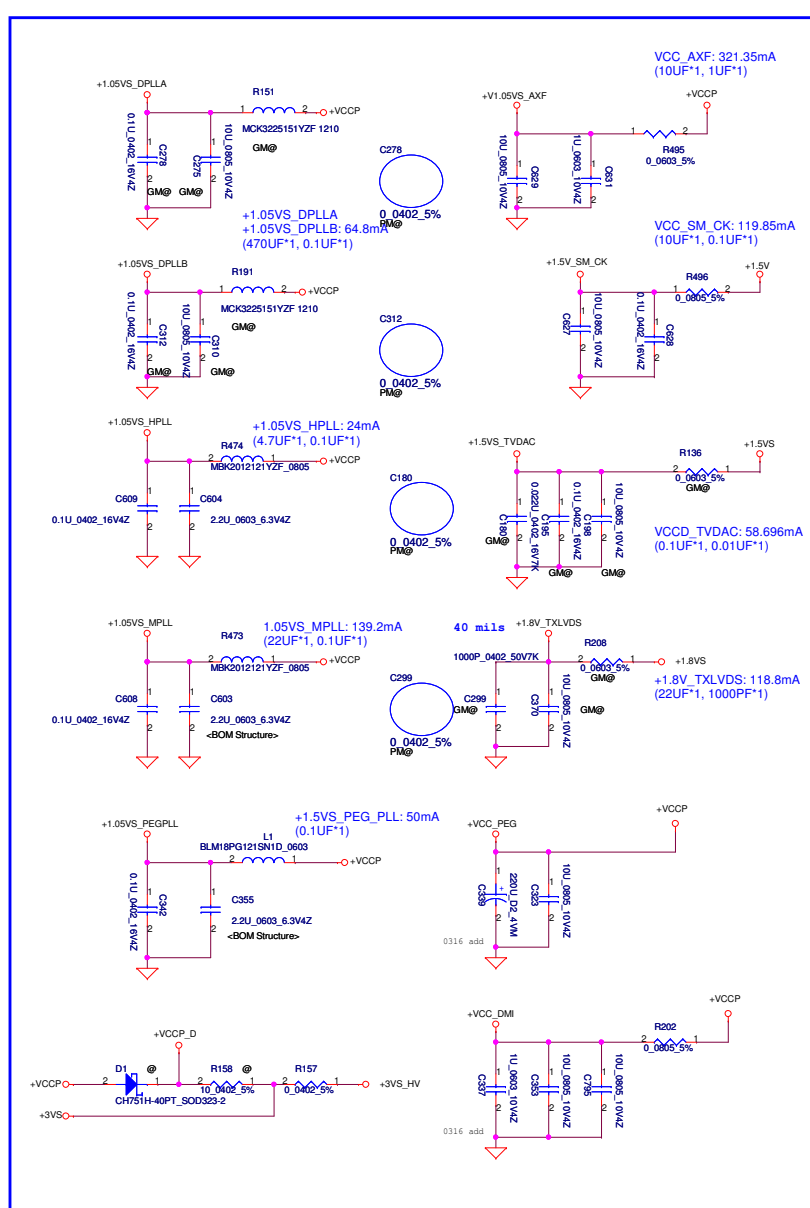
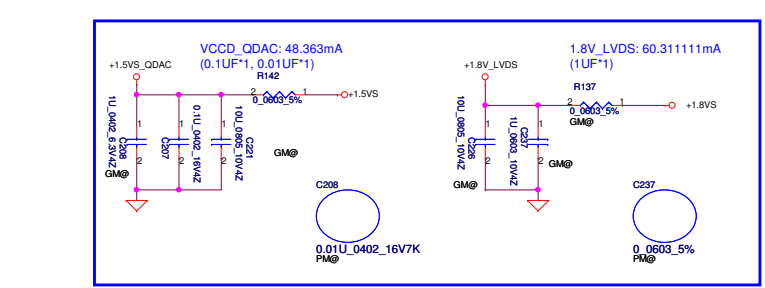
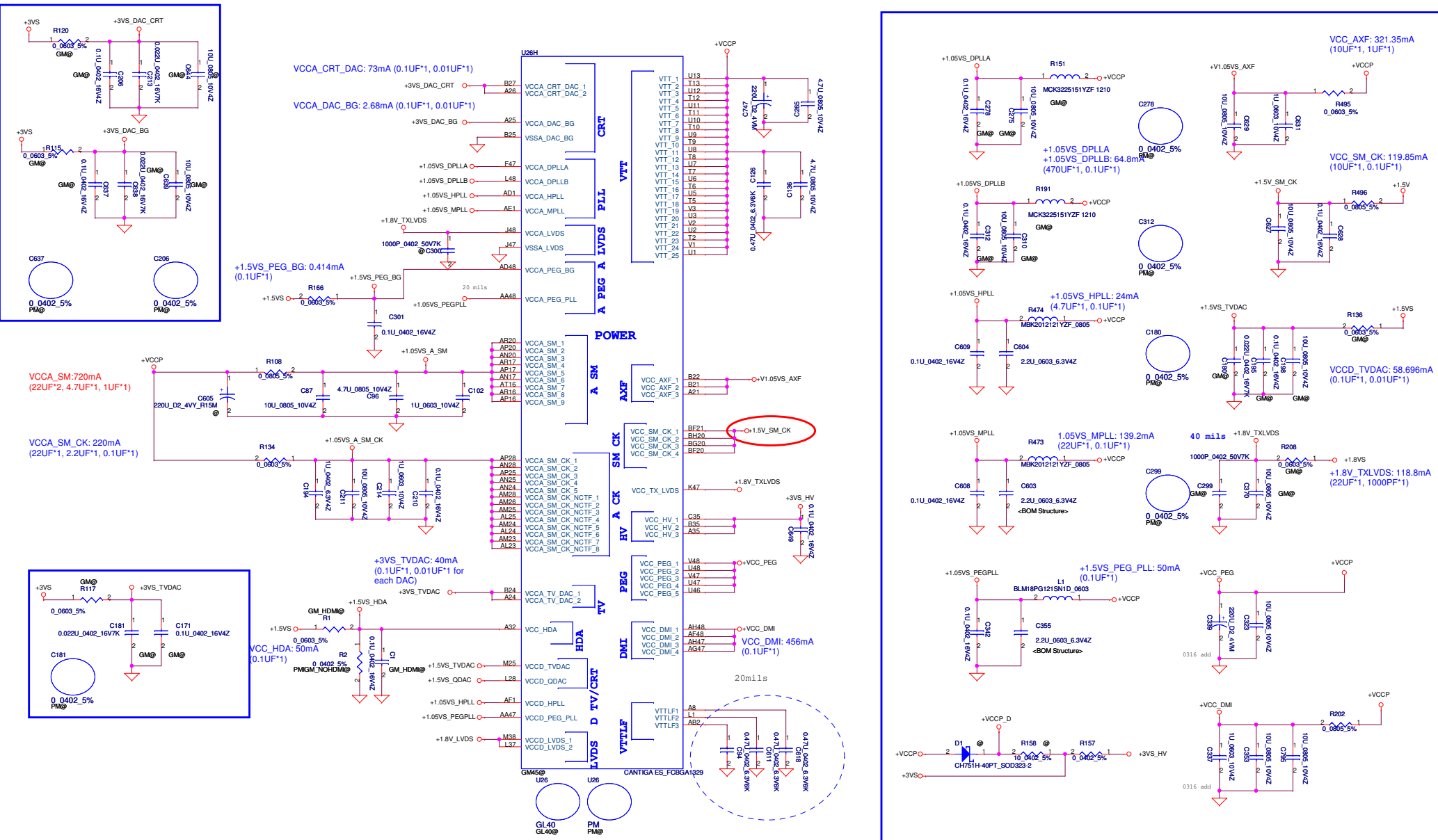
CANTIGA ES\_FCBGA1329

GM45@

CANTIGA ES\_FCBGA1329

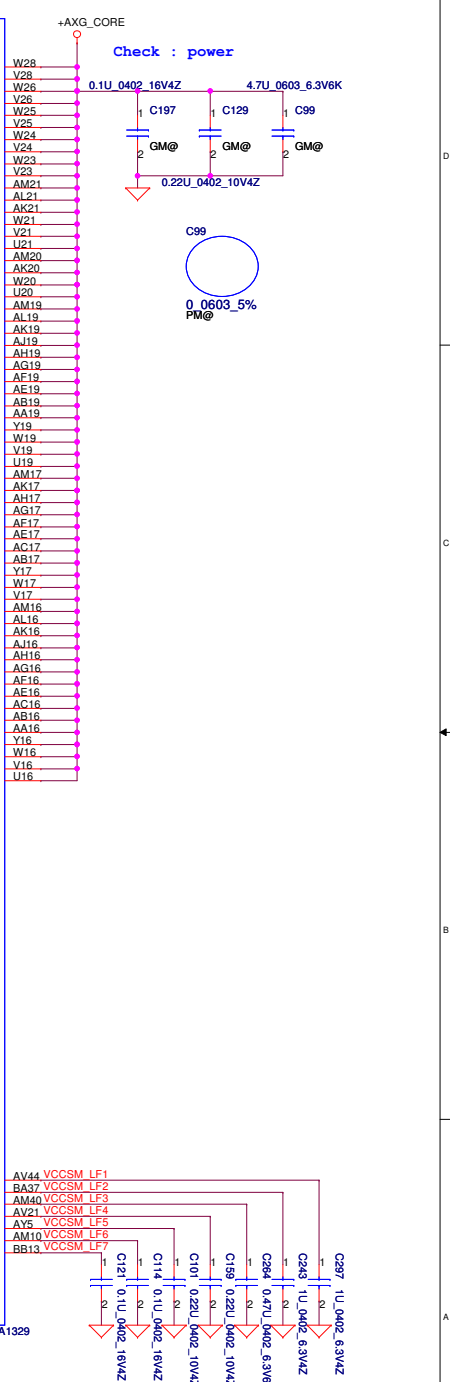
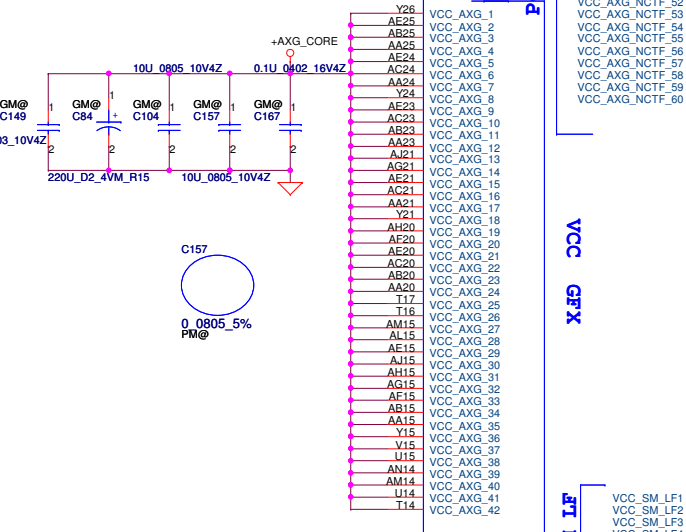
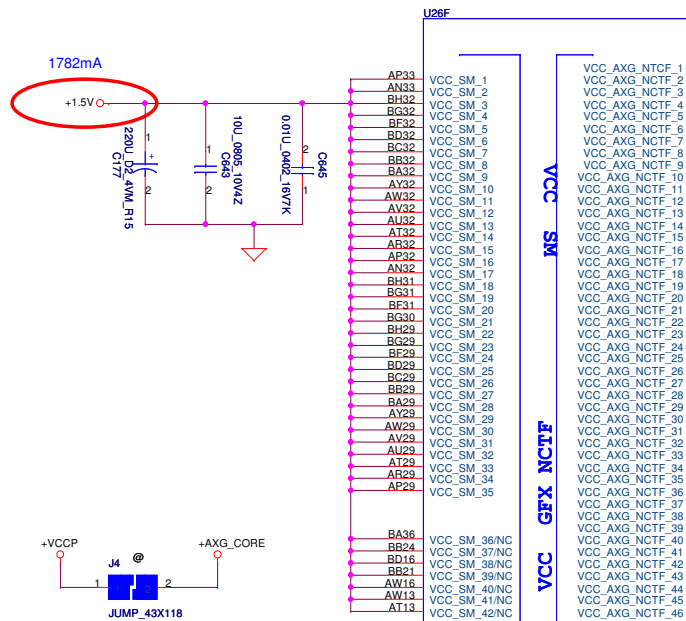
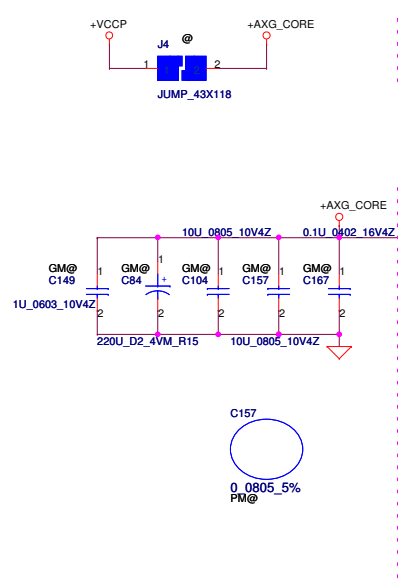
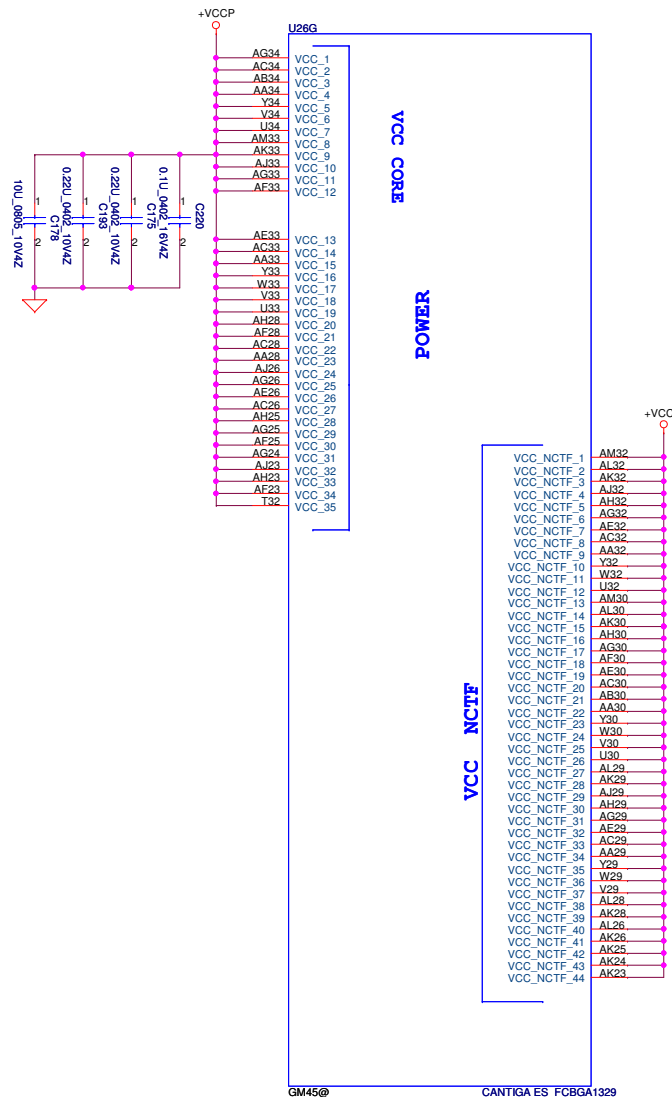
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Size	Document Number	Date		Rev	1.0
B	KIWAX_LA-5081P	Tuesday, April 28, 2009		Sheet	9 of 51



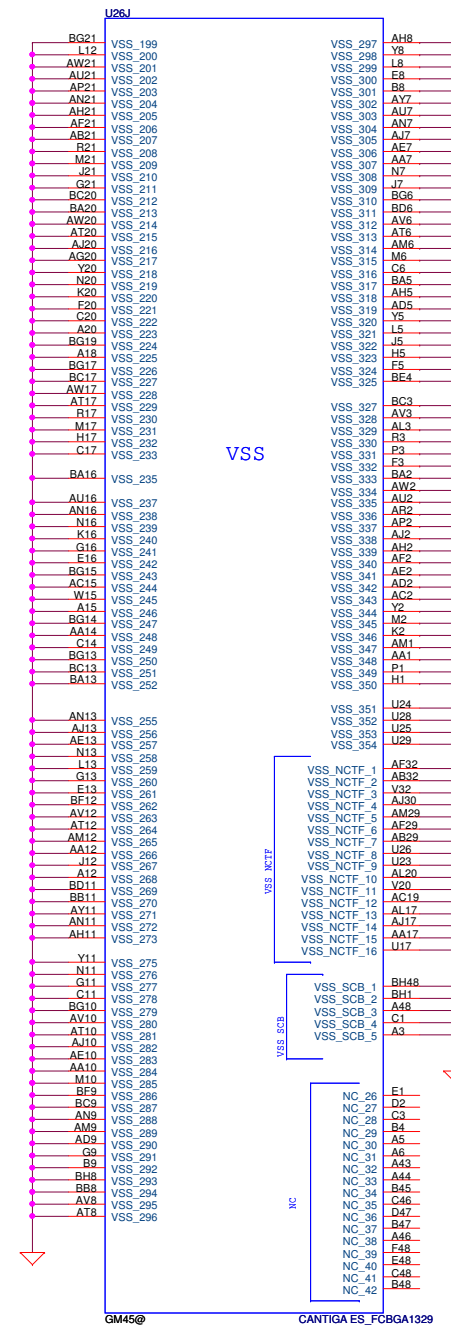
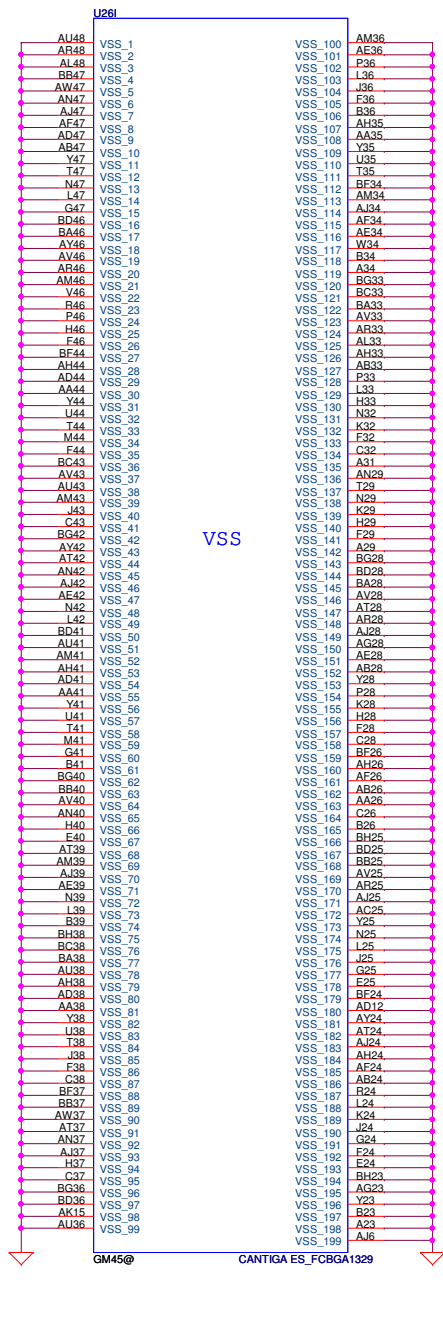


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Size	Document Number	Rev		1.0
Customer	KIWAX_LA-508IP	Date		Tuesday, April 28, 2009
Date			Tuesday, April 28, 2009	Sheet 11 of 51

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**Crestline GMCH (4/6)-VCC**



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Size	Document Number	K1WAX_LA-5081P		Rev	1.0
Date	Tuesday, April 28, 2009	Sheet	12	of 51	

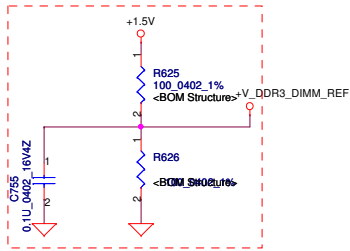


Security Classification	Compal Secret Data	
Issued Date	2009/04/23	Deciphered Date
		2010/05
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Title			
Compal Electronics, Inc.			
Cantiga GMCH (6/6)-GND			
Size	Document Number	Rev	
Custom	KIWAX_LA-5081P	1.0	
Date:	Tuesday, April 28, 2009	Sheet	13 of 51

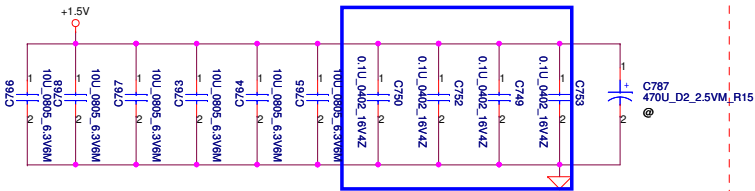


- (9) DDR\_A\_DQS#[0..7]
- (9) DDR\_A\_D[0..63]
- (9) DDR\_A\_DM[0..7]
- (9) DDR\_A\_DQS[0..7]
- (9) DDR\_A\_MA[0..14]

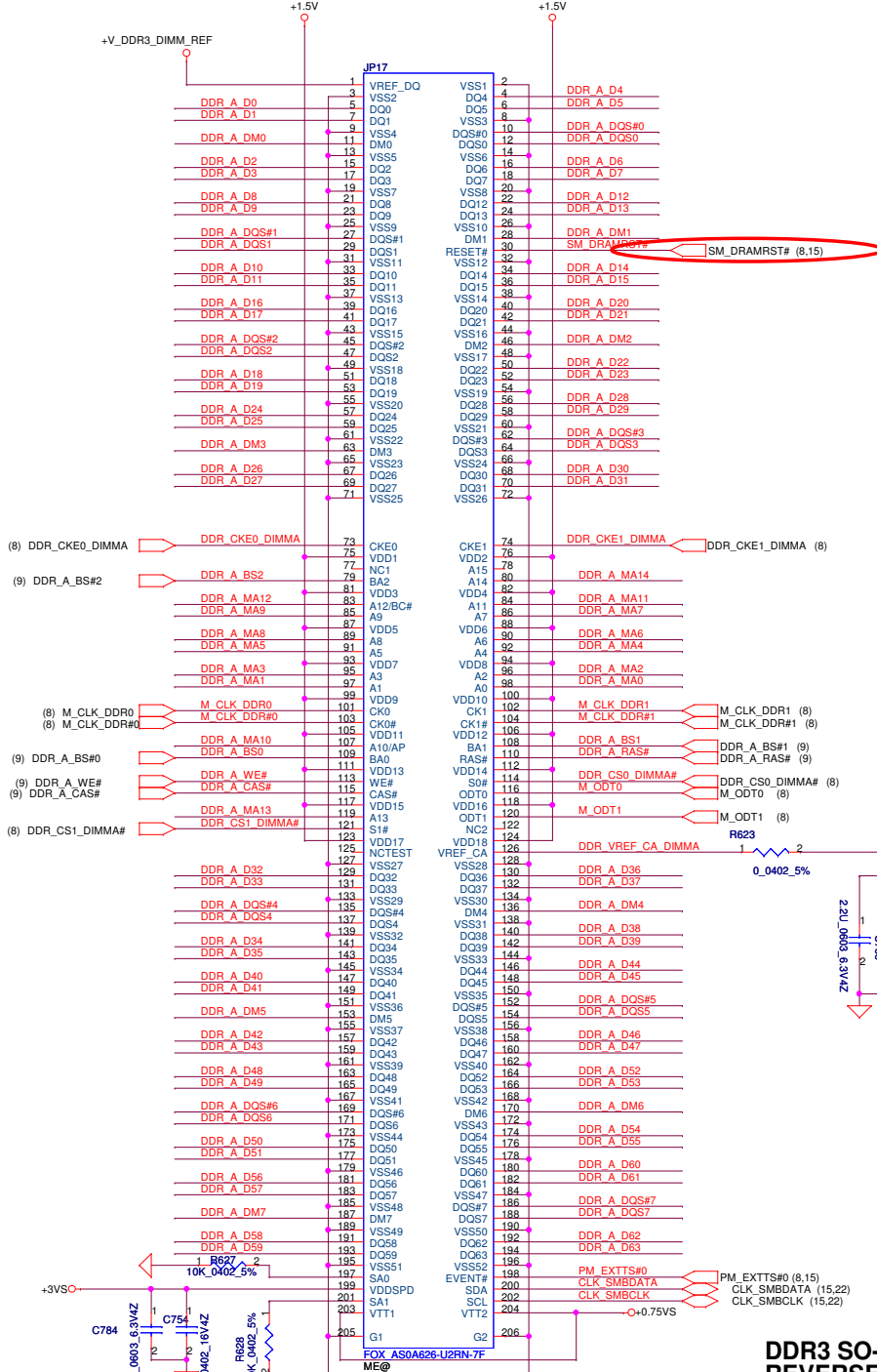
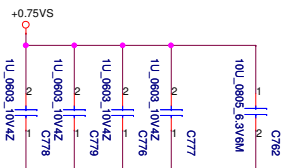


**Layout Note:**  
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



**Layout Note:**  
Place near JP4.203 & JP4.204



**DDR3 SO-DIMM A  
REVERSE**

Security Classification	Compal Secret Data	
Issued Date	2009/04/23	Deciphered Date
		2010/05

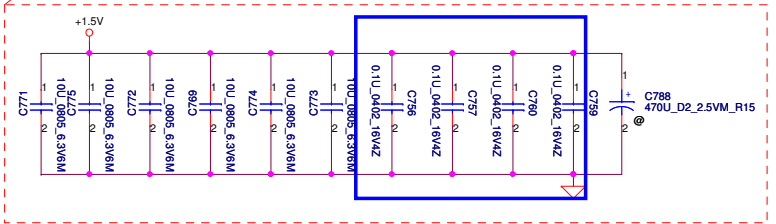
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Title		
<b>Compal Electronics, Inc.</b>		
<b>DDR3II-SODIMM SLOT1</b>		
Size	Document Number	Rev
Custort	<b>KIWAX_LA-5081P</b>	<b>1.0</b>
Date:	Tuesday, April 28, 2009	Sheet 14 of 51

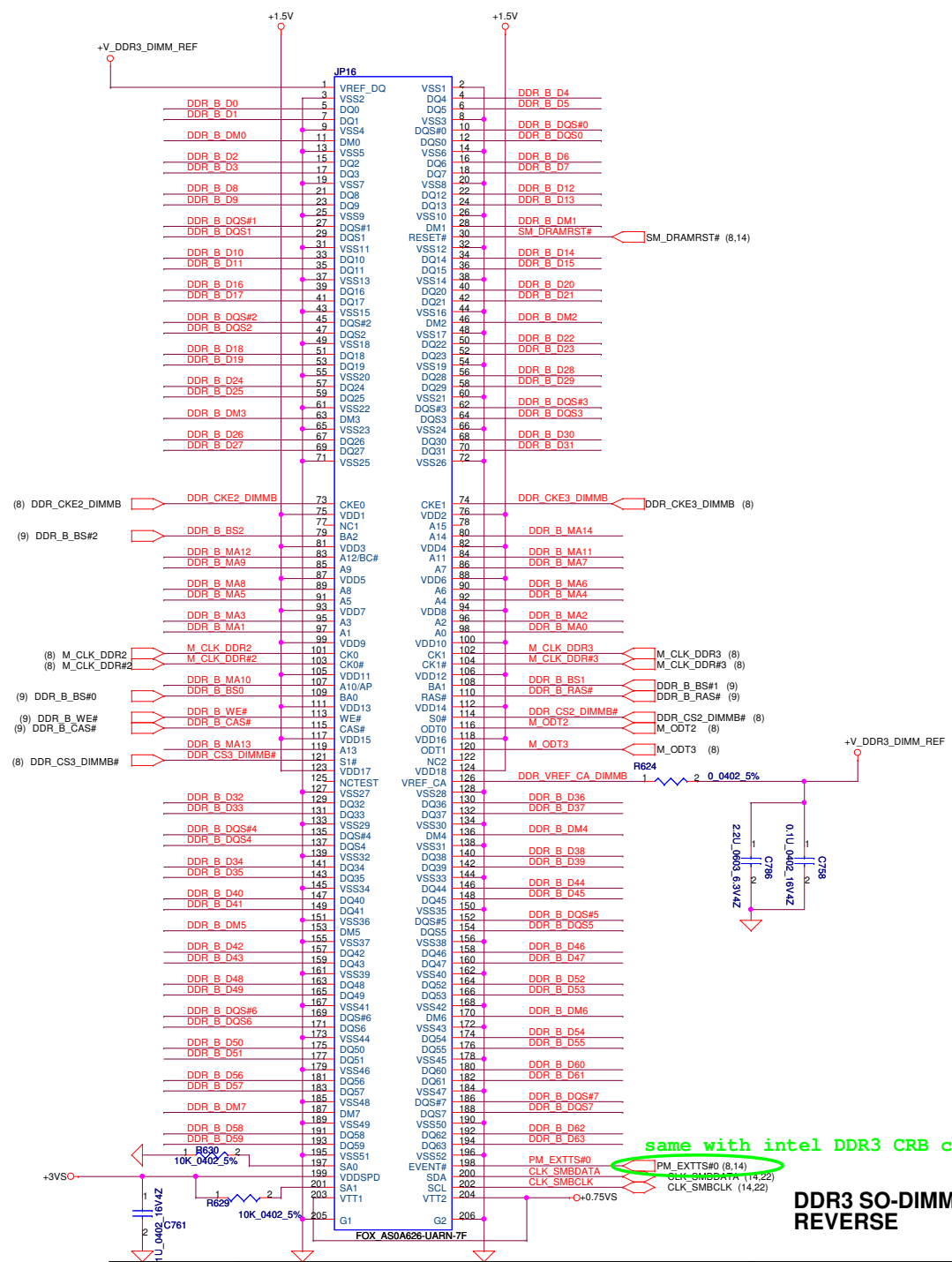
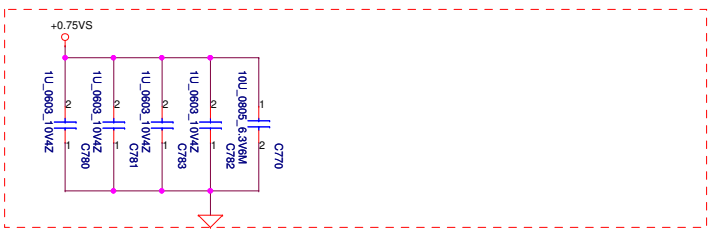
- (9) DDR\_B\_DQS#[0..7]
- (9) DDR\_B\_D[0..63]
- (9) DDR\_B\_DM[0..7]
- (9) DDR\_B\_DQS[0..7]
- (9) DDR\_B\_MA[0..14]

**Layout Note:**  
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



**Layout Note:**  
Place near JP5.203 & JP5.204

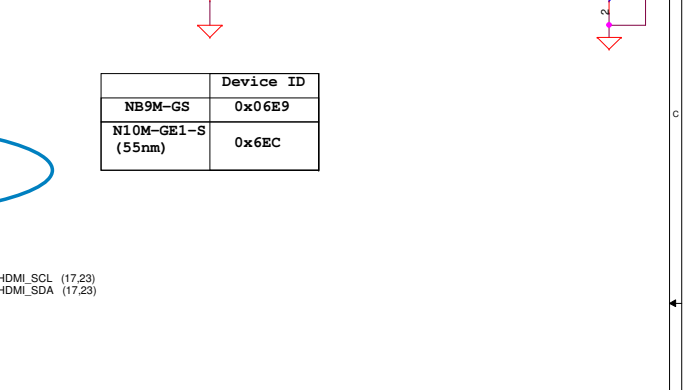
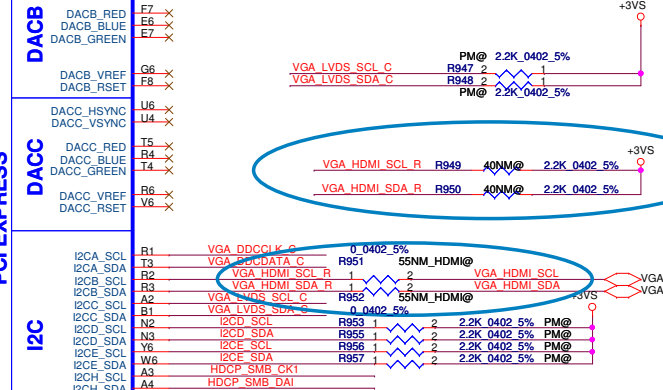
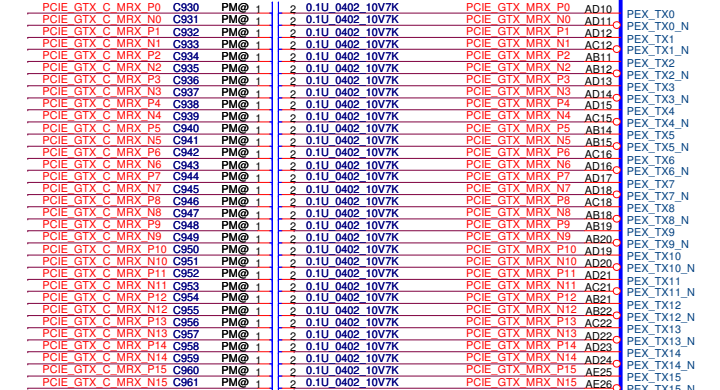
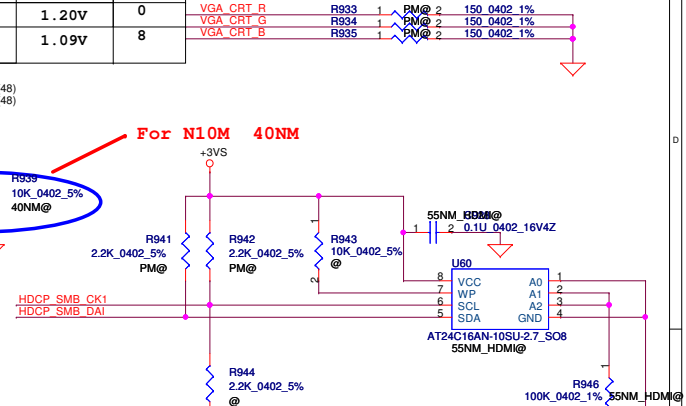
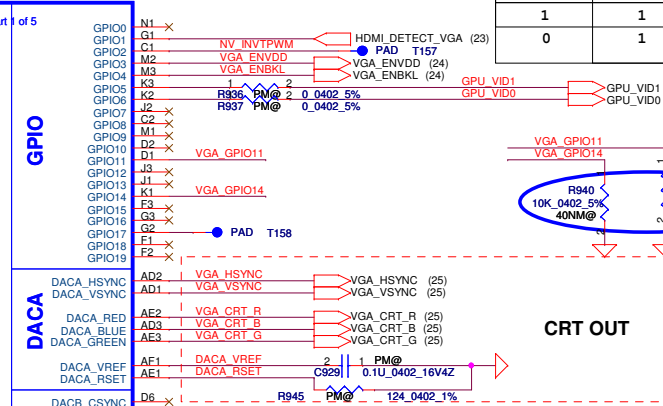
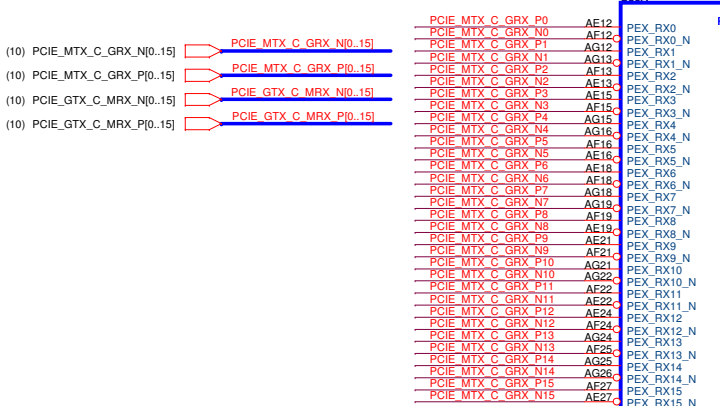
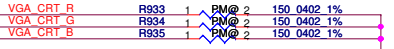


**DDR3 SO-DIMM B REVERSE**

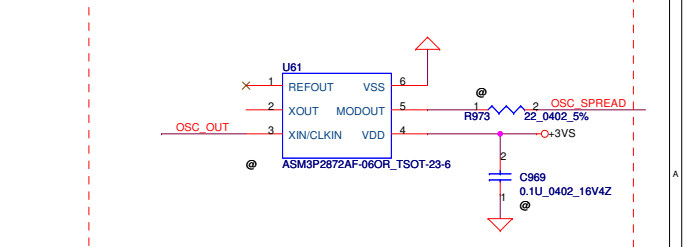
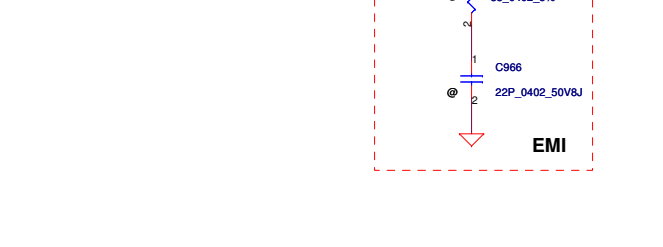
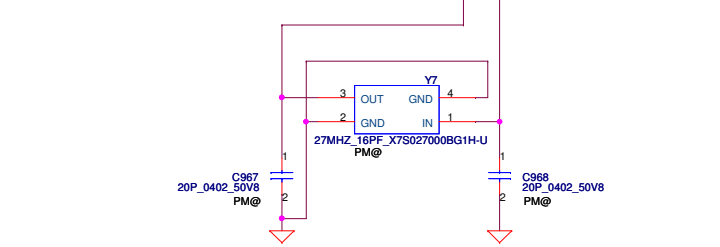
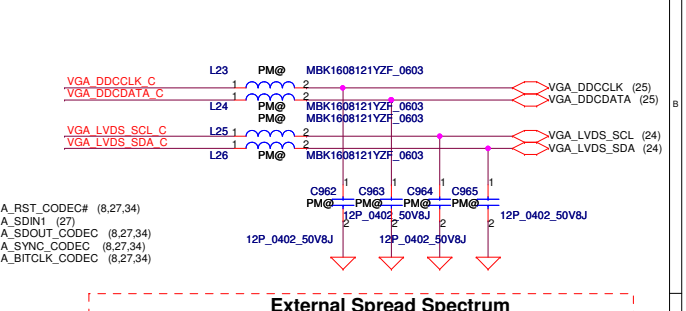
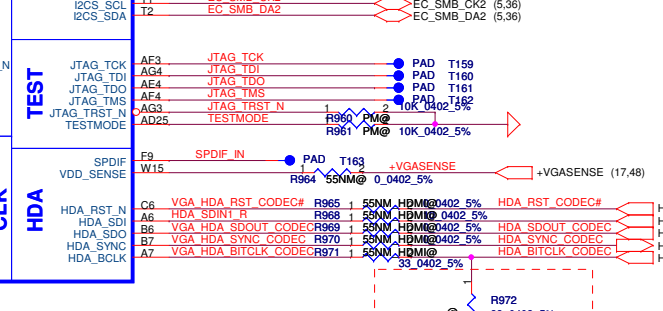
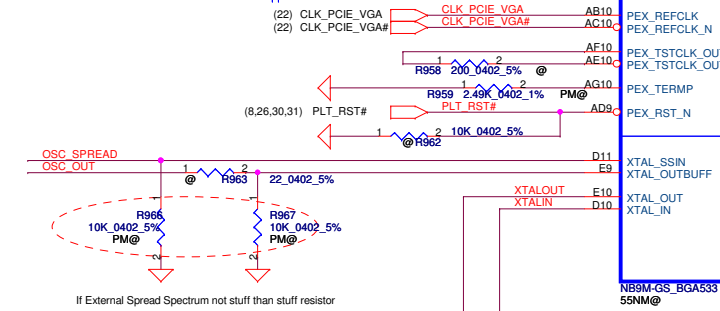
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Issued Date	2009/04/23	Deciphered Date	2010/05	Compal Electronics, Inc.	
				DDR3-SODIMM SLOT2	
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					KIWX LA-5081P
				Date:	Tuesday, April 28, 2009
				Sheet	15 of 51



GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10, 12
1	1	1.20V	0
0	1	1.09V	8



	Device ID
NB9M-GS	0x06E9
N10M-GE1-S (55nm)	0x6EC



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Issued Date	2009/04/23	Deciphered Date	2010/05
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**Compal Electronics, Inc.**

**N10M\_PCIE, LVDS, GPIO, CLK**

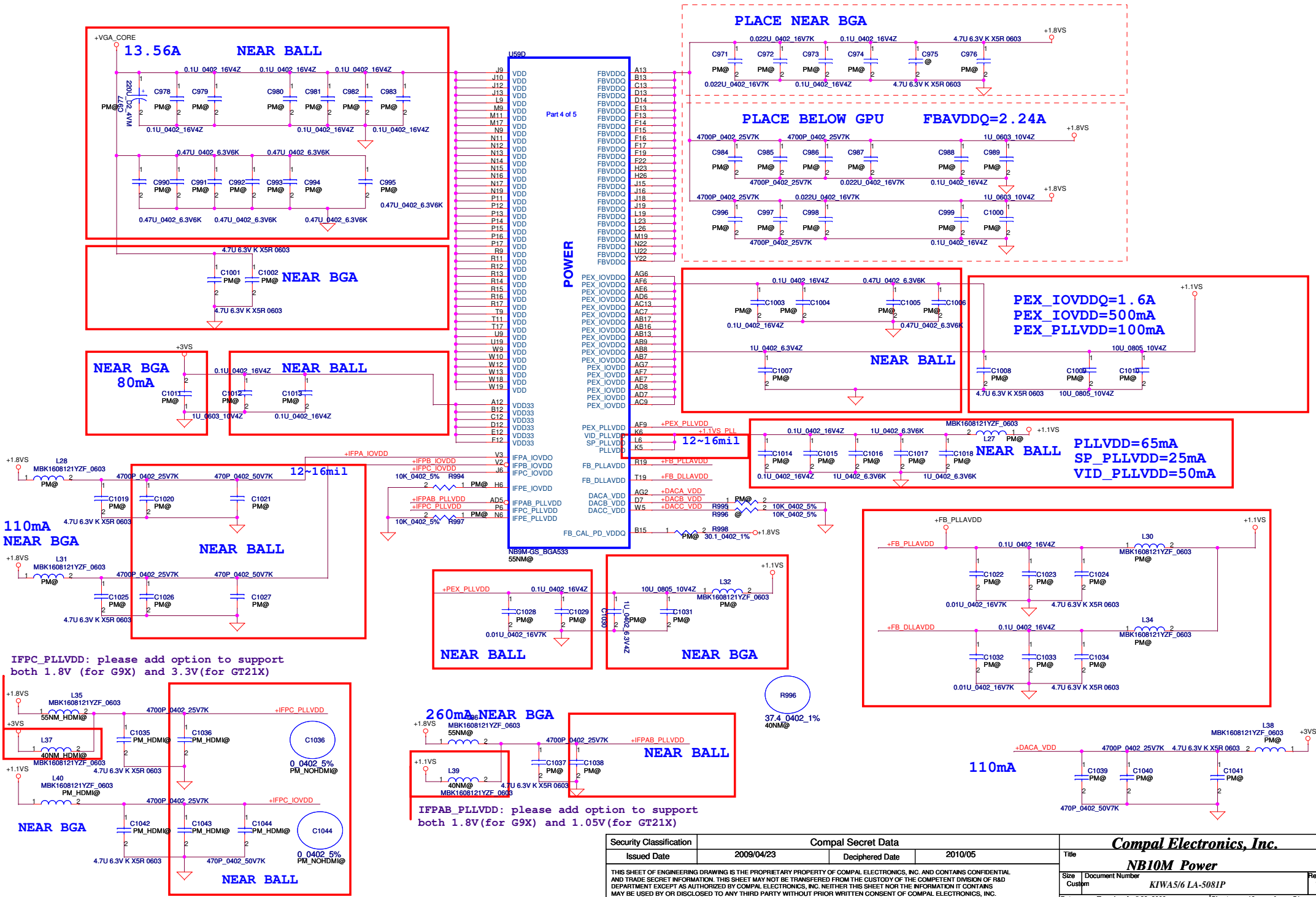
Title: N10M\_PCIE, LVDS, GPIO, CLK

Size B, Document Number: KIWA5/6 LA-5081P, Rev 1.0

Date: Tuesday, April 28, 2009, Sheet 16 of 51

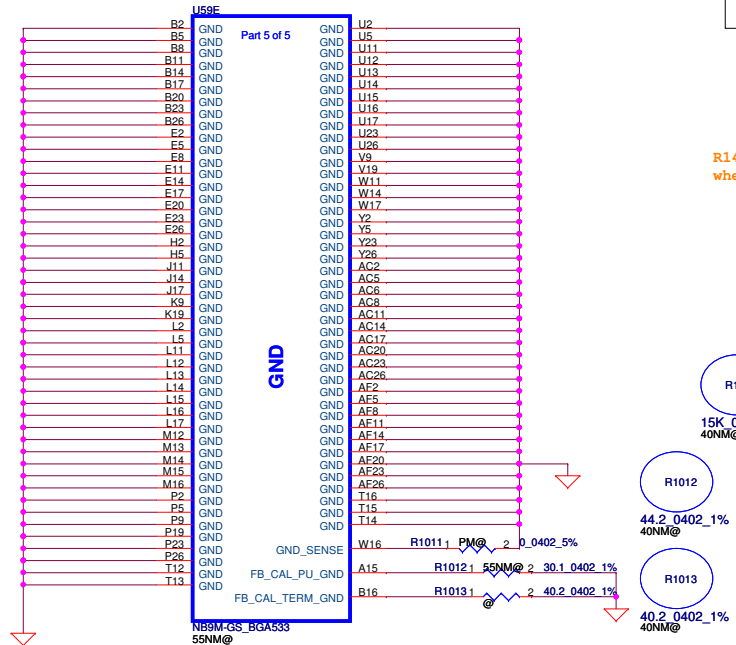


FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS



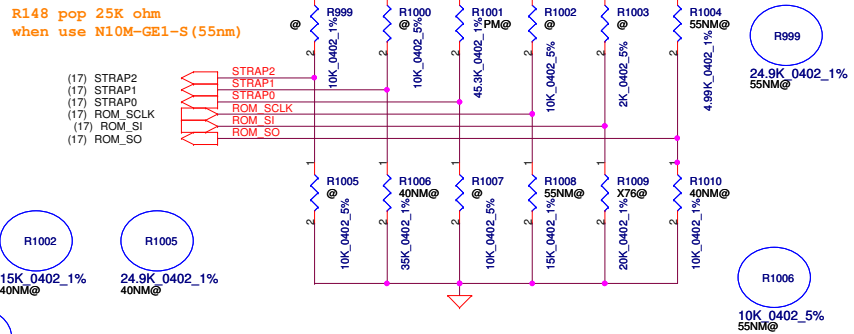
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/04/23	Deciphered Date	2010/05	Title	<b>NB10M Power</b>
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			KIWA5/6 LA-5081P		1.0
Date:	Tuesday, April 28, 2009	Sheet	18	of	51

A total of 8 signals are required for GB1 strapping this includes  
 2 reference signals  
 6 physical strapping pins  
 4 logical strapping bits  
 A total of 24 logical strapping bits are available



Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001\_V06 (2008/4/01)

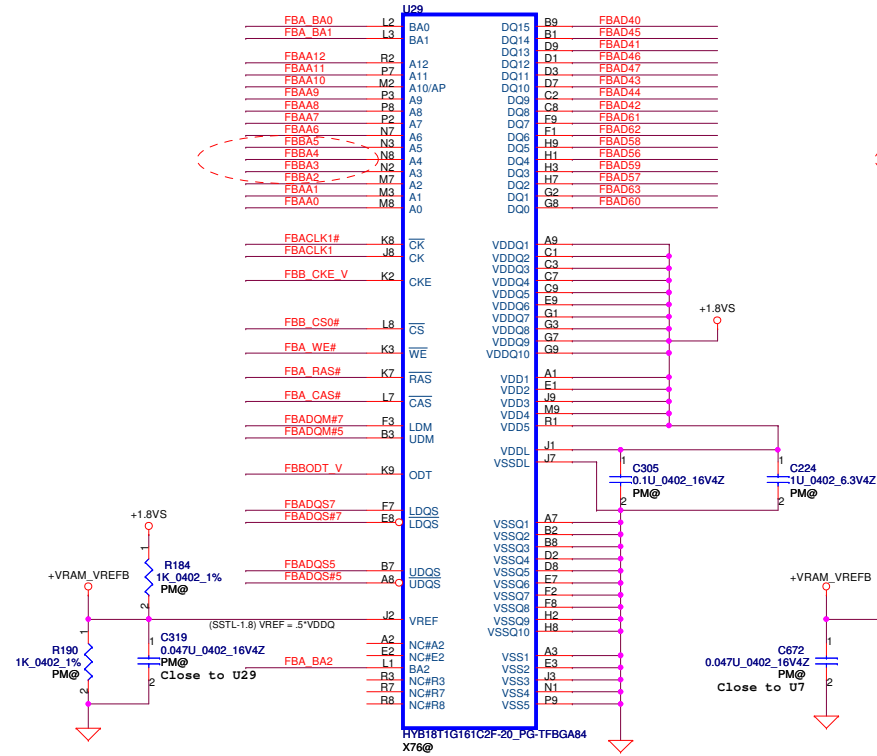


GB1 Family GPU Strap Options X76

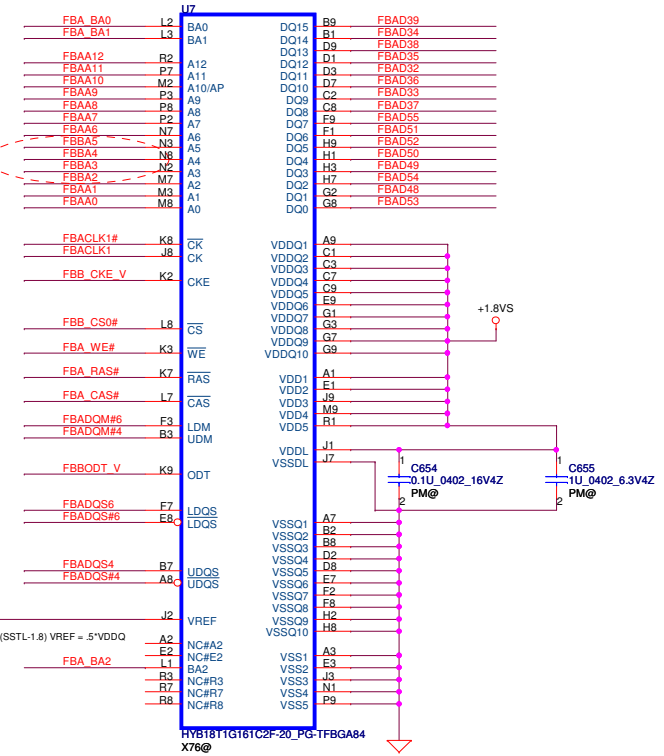
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung 64Mx16	PU 5K	PD 15K	PD 20K	PU 25K	PD 10K	PU 45K
	Hynix 64Mx16	PU 5K	PD 15K	PD 5K	PU 25K	PD 10K	PU 45K
	Qimonda 64Mx16	PU 5K	PD 15K	PD 15K	PU 25K	PD 10K	PU 45K
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
	Samsung 64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 35K	PU 45K
	Hynix 64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 35K	PU 45K
Qimonda 64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 35K	PU 45K	

4/23 update strap1 10K to 35K according to N10M latest PUN

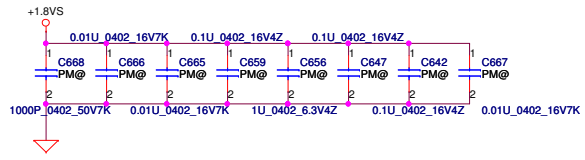
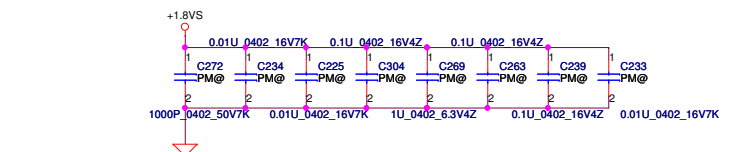
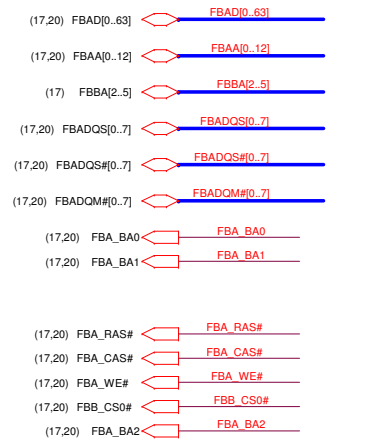




DDR2 BGA MEMORY



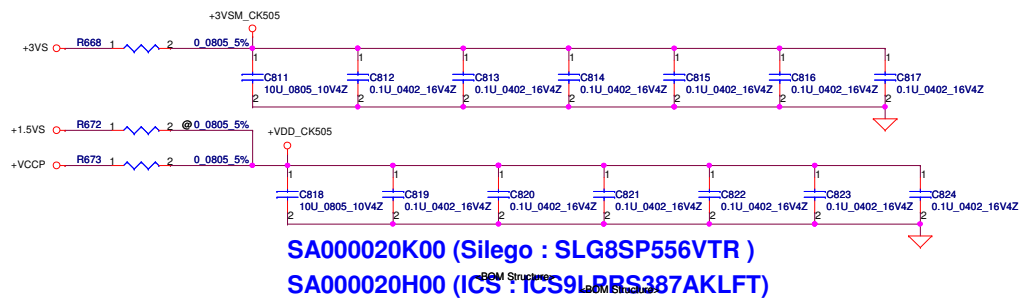
DDR2 BGA MEMORY



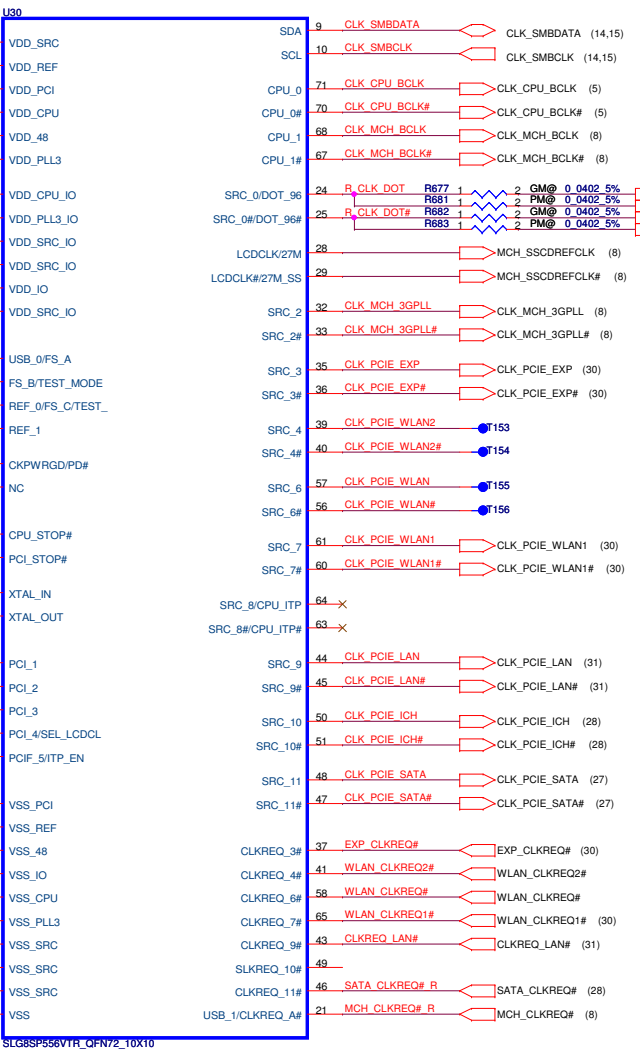
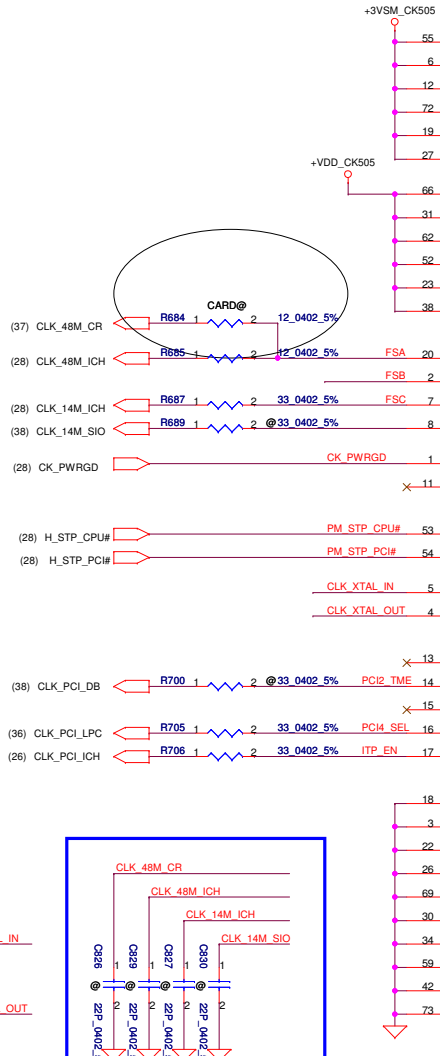
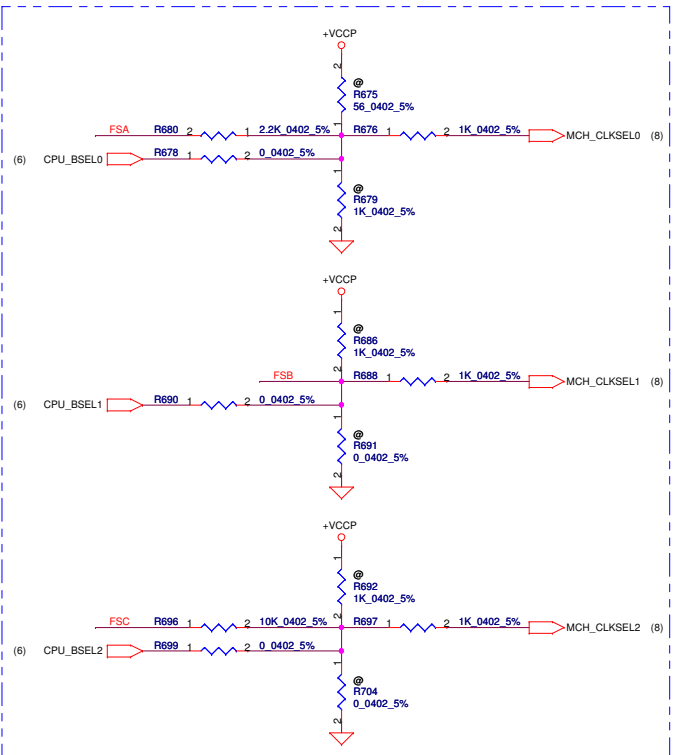
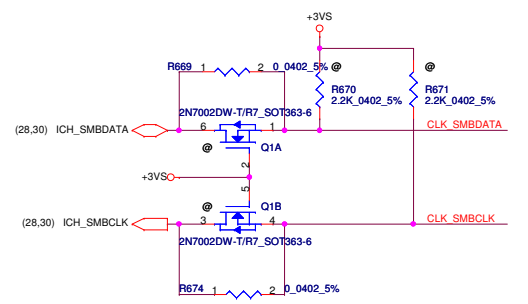
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Issued Date	2009/04/23	Deciphered Date	2010/05	<b>Compal Electronics, Inc.</b> <b>VRAM DDRB</b>	
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Custom	Document Number	KIWA5/6 LA-5081P		1.0	
Date:	Tuesday, April 28, 2009	Sheet	21	of 51	



FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
<b>Reserved</b>								



**SA000020K00 (Silego : SLG8SP556VTR)**  
**SA000020H00 (ICS : ICS9LRS387AKLFT)**

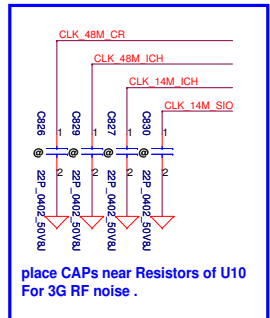
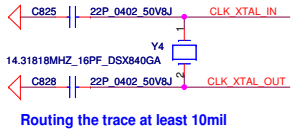
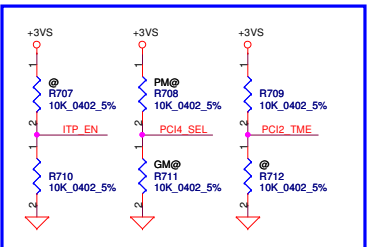


**SRC PORT LIST**

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN
SRC6	PCIE_WLAN1
SRC8	PCIE_WLAN
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

**REQ PORT LIST**

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	PCIE_LAN
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL



For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
 For PCI4\_SEL, 0 = Pin24/25 : DOT96 / DOT96#  
 Pin28/29 : LCDCLK / LCDCLK#  
 1 = Pin24/25 : SRC\_0 / SRC\_0#  
 Pin28/29 : 27M/27M\_SS

Routing the trace at least 10mil

place CAPs near Resistors of U10  
 For 3G RF noise .

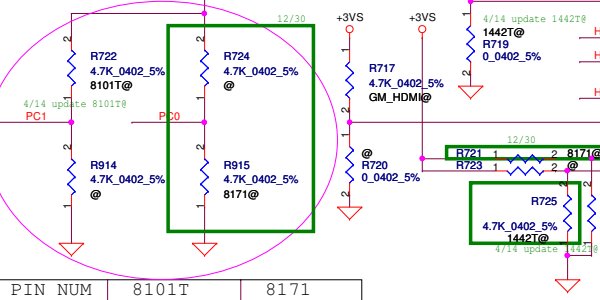
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Compal Electronics, Inc.		
<b>Clock Generator CK505</b>		
Title	Document Number	Rev
	KIWA5/6 LA-5081P	1.0
Date: Tuesday, April 28, 2009	Sheet	22 of 51



10/30 update PS8171 co-lay circuit  
4/14 update 1442T co-lay circuit

For 8171

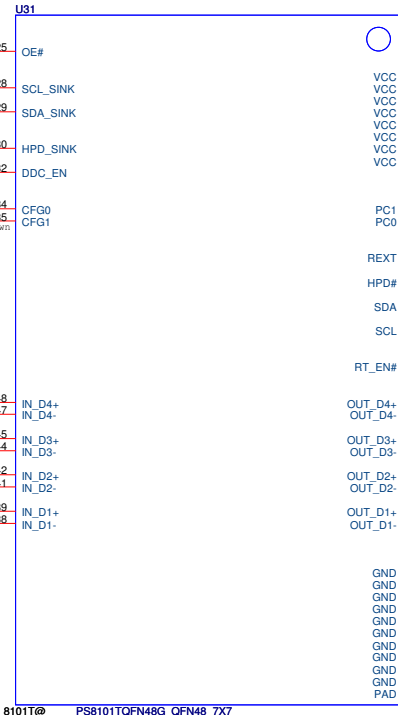


PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	P10
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	APD
PIN12	GND	ASQ1
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

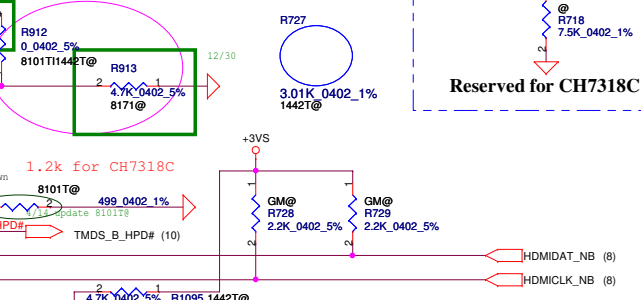
- (10) TMDS\_B\_CLK
- (10) TMDS\_B\_CLK#
- (10) TMDS\_B\_DATA0
- (10) TMDS\_B\_DATA0#
- (10) TMDS\_B\_DATA1
- (10) TMDS\_B\_DATA1#
- (10) TMDS\_B\_DATA2
- (10) TMDS\_B\_DATA2#

For 8171 net name:  
EMI0, EMI1  
ASQ0, ASQ1  
APD

P/N:SA00002D700 (8101T)  
P/N:SA00001U920 (CH7318C)

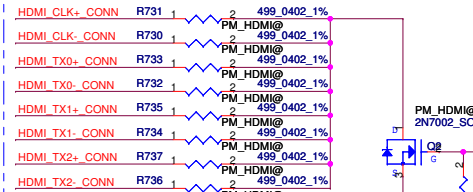


For 8171

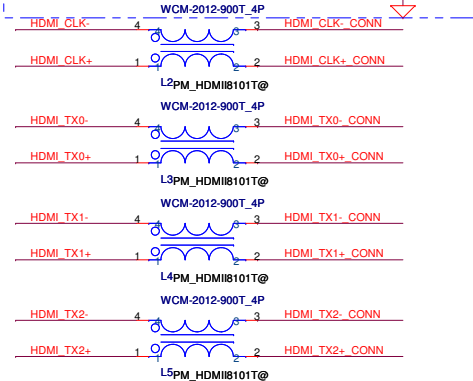


place those component near JP? for NV request 0515

TMDS pull down (500ohm) resistors for ATI M92-S2 XT



NEAR CONNECTOR



HDMI CLK+	R751	1442T@	2	0.0402_5%	HDMI CLK+ CONN
HDMI CLK-	R752	1442T@	2	0.0402_5%	HDMI CLK- CONN
HDMI TX0+	R753	1442T@	2	0.0402_5%	HDMI TX0+ CONN
HDMI TX0-	R754	1442T@	2	0.0402_5%	HDMI TX0- CONN
HDMI TX1+	R755	1442T@	2	0.0402_5%	HDMI TX1+ CONN
HDMI TX1-	R756	1442T@	2	0.0402_5%	HDMI TX1- CONN
HDMI TX2+	R757	1442T@	2	0.0402_5%	HDMI TX2+ CONN
HDMI TX2-	R758	1442T@	2	0.0402_5%	HDMI TX2- CONN

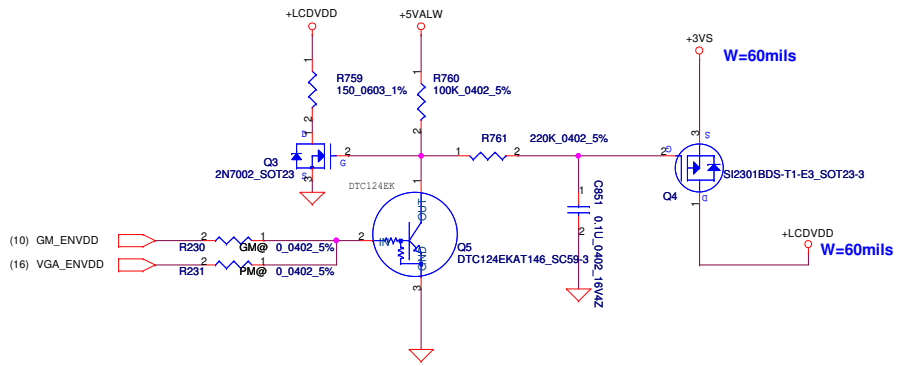
KIWB3/B4\_LA4551P

Security Classification	Compal Secret Data	
Issued Date	2009/04/23	Deciphered Date
		2010/05

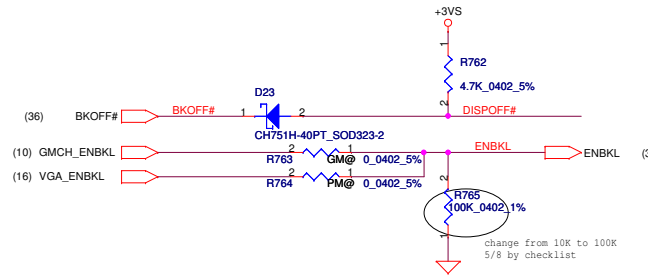
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Compal Electronics, Inc.	
Title	
Level Shifter_PS8101T	
Size	Document Number
Custom	KIWAX_LA-5081P
Date	Tuesday, April 28, 2009
Sheet	23 of 51
Rev	1.0

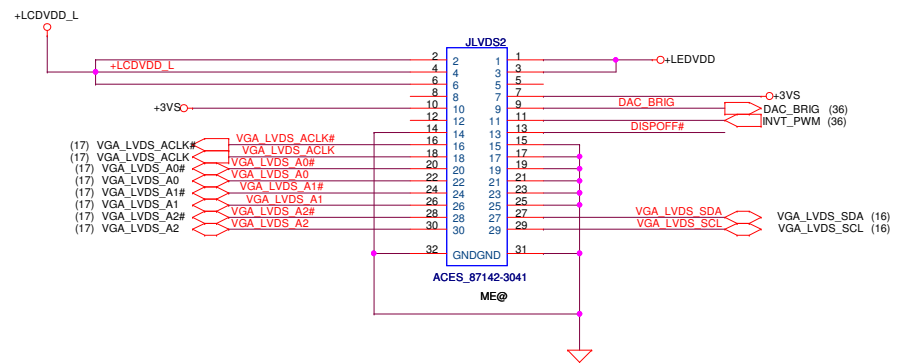
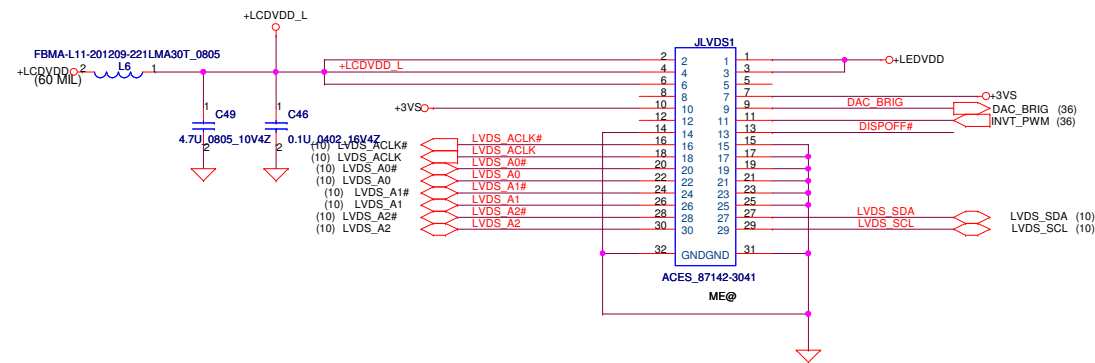
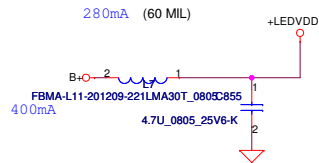
# LCD POWER CIRCUIT



LCD/PANEL BD. Conn.  
FOR UMA



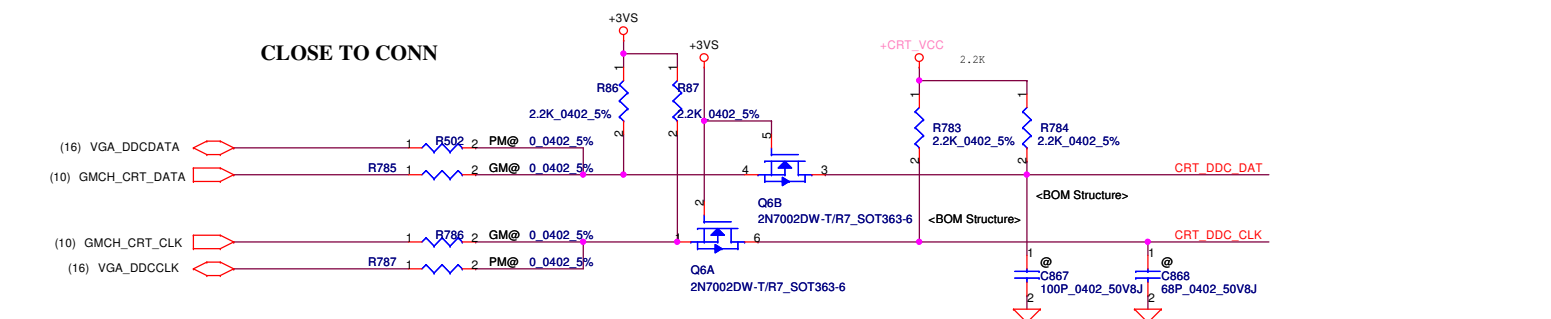
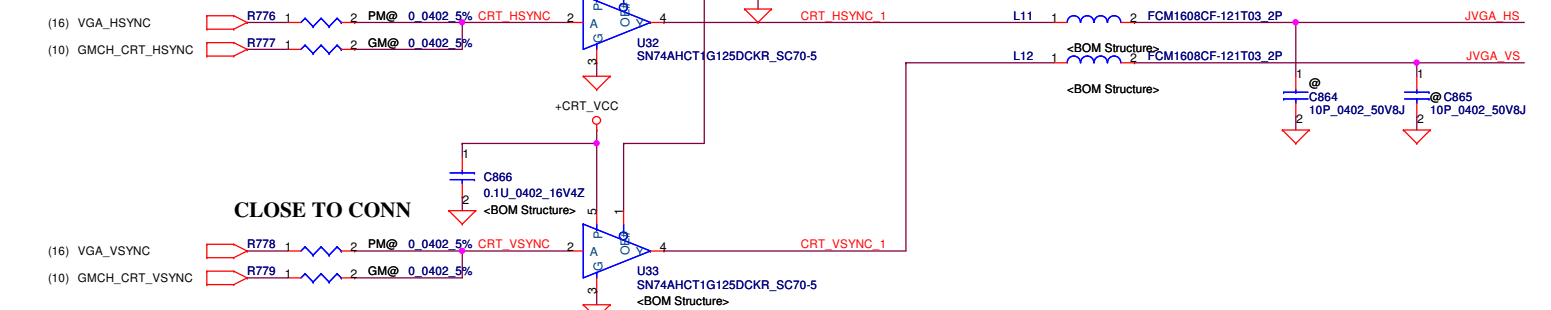
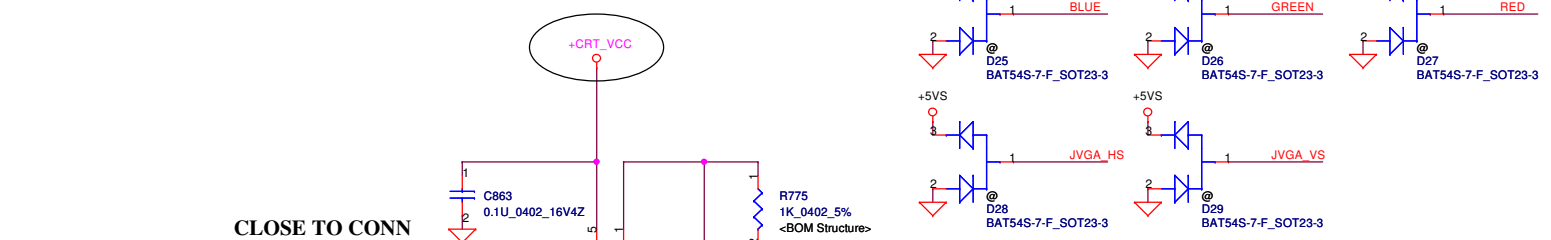
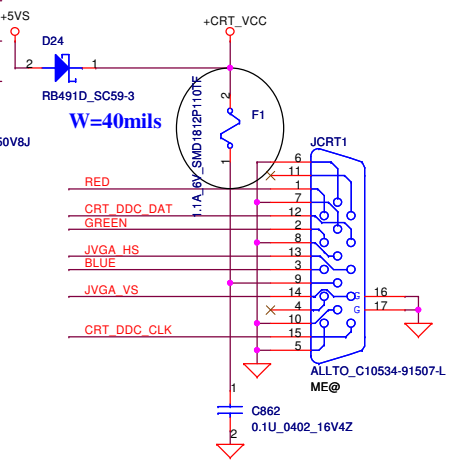
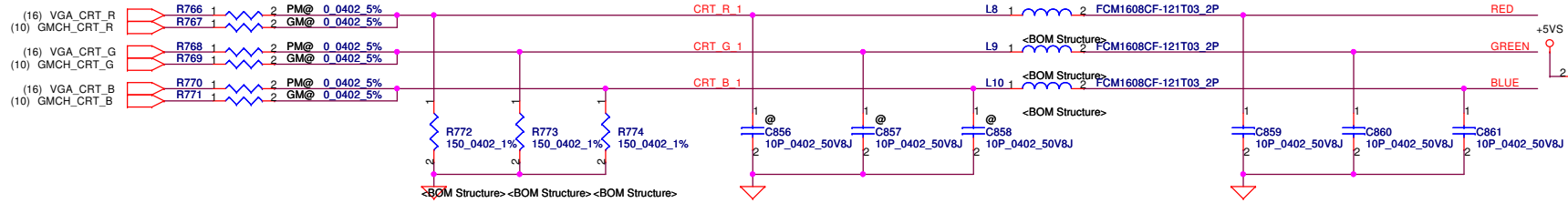
LCD/PANEL BD. Conn.  
FOR DIS



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				KIWA5/6 LA-5081P		
				Date:	Tuesday, April 28, 2009	Sheet 24 of 51

# CRT Connector

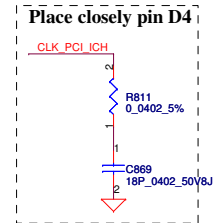
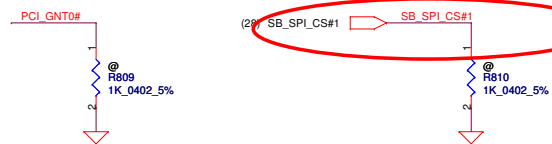
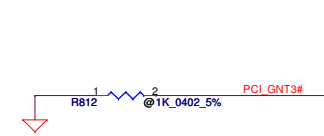
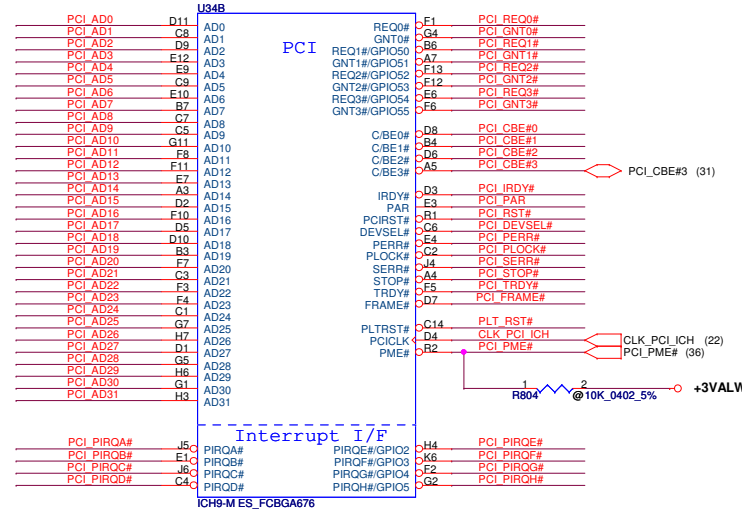
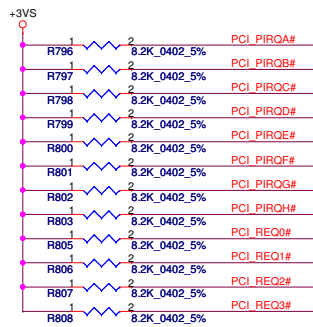
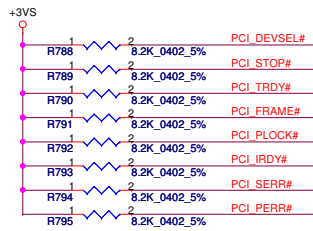
## CLOSE TO CONN



## PIN ASSIGMENT

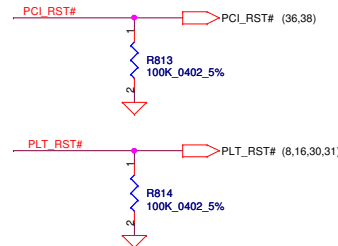
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

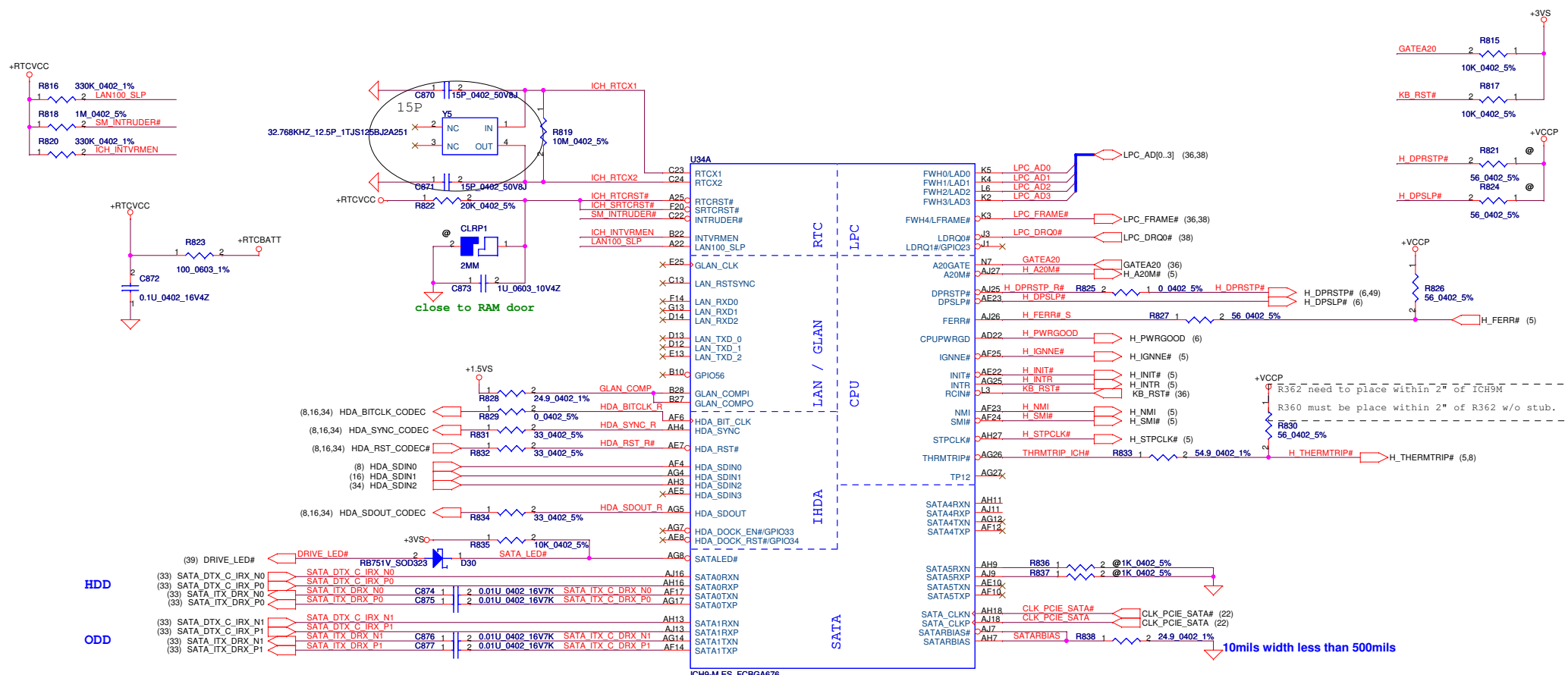
Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05	Compal Electronics, Inc.	
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Size	Document Number	Date		Rev	1.0
Custom	KIWA5/6 LA-5081P	Tuesday, April 28, 2009		Sheet	25 of 51



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*





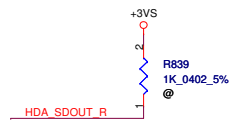
HDD  
ODD

close to RAM door

+VCCP  
R362 need to place within 2" of ICH9M  
R360 must place within 2" of R362 w/o stub.

10mils width less than 500mils

Need check

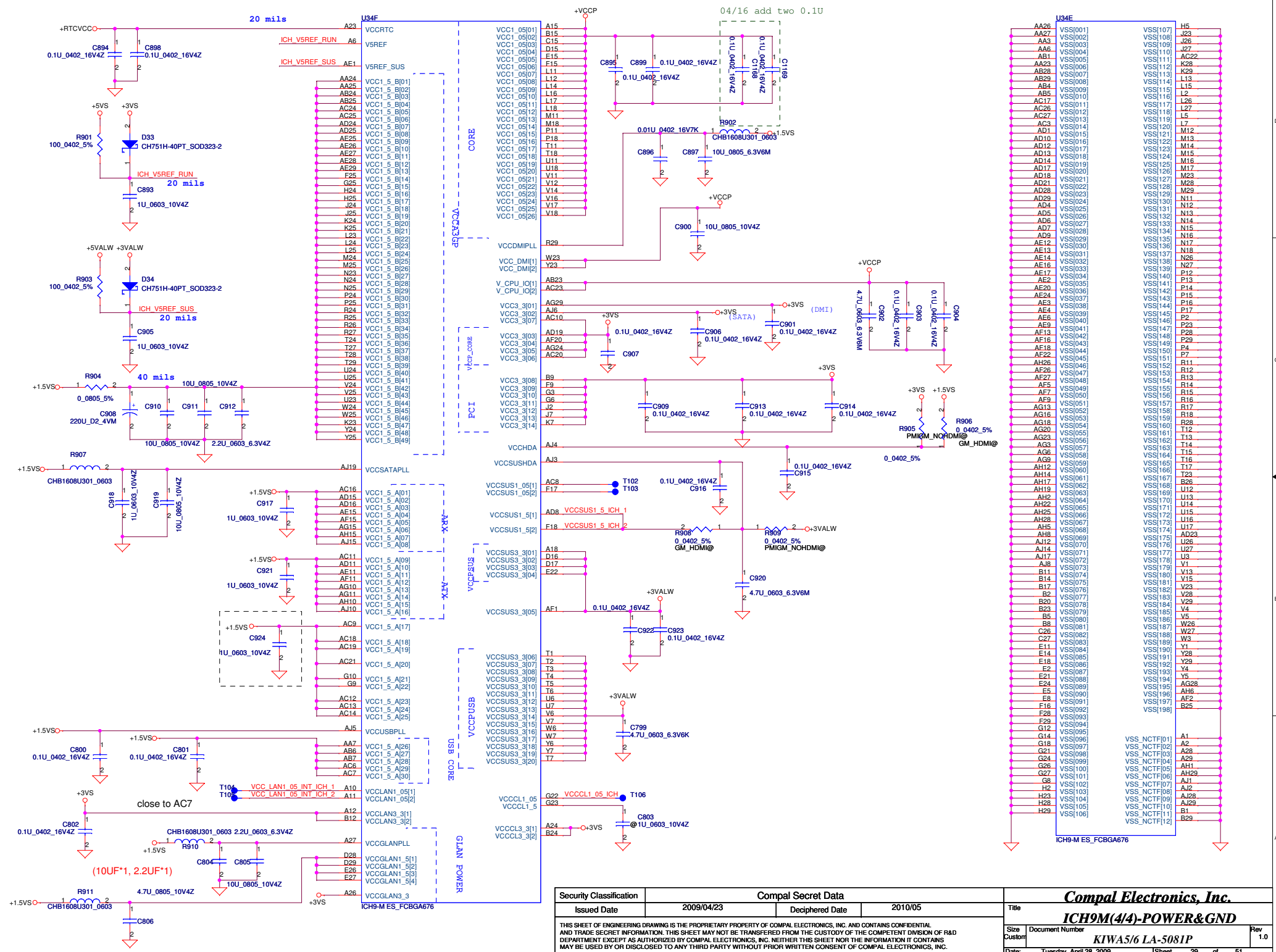


XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	





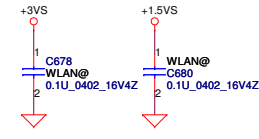
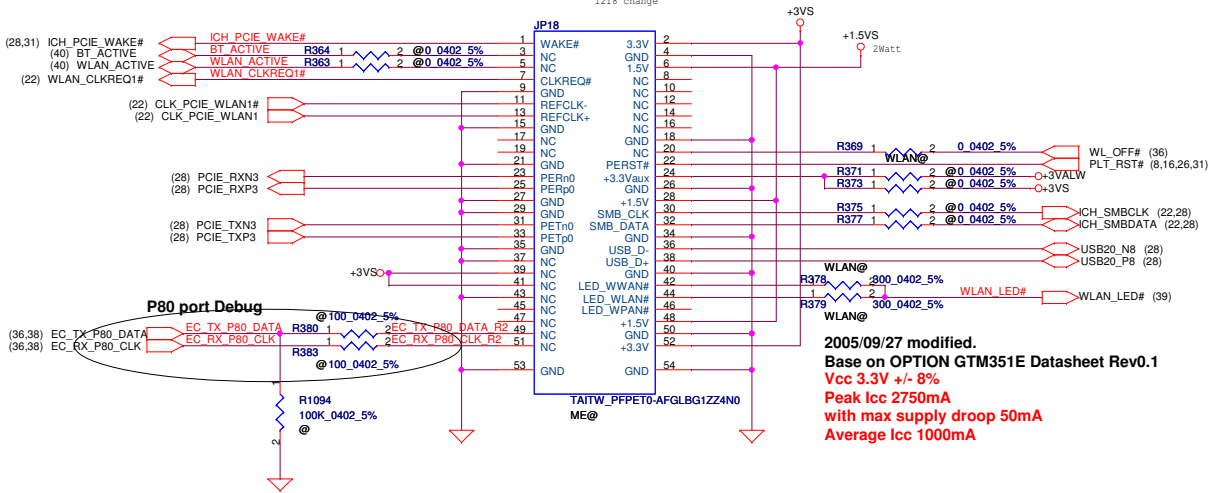


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Issued Date	2009/04/23	Deciphered Date	2010/05
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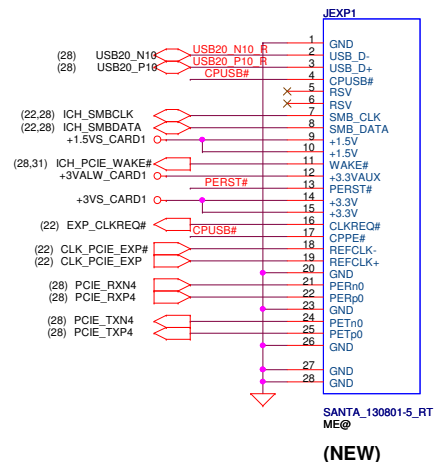
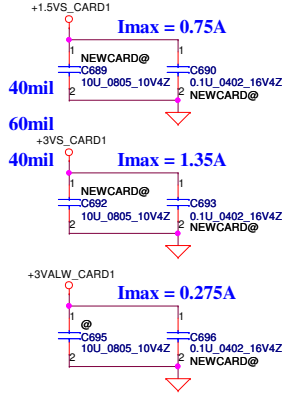
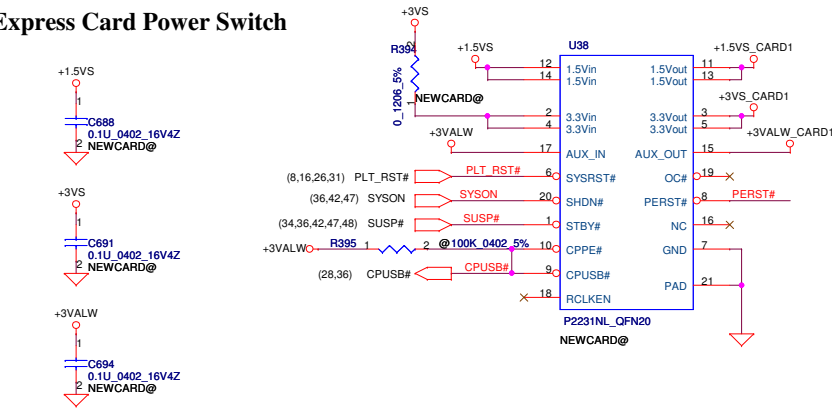
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Size	Document Number	Date	Rev
Custom		Tuesday, April 28, 2009	1.0
		Sheet	29 of 51



# Mini-Express Card(Slot 2-WIRELESS) 5.2mm high

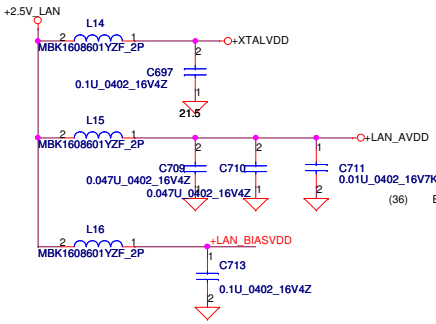


## Express Card Power Switch

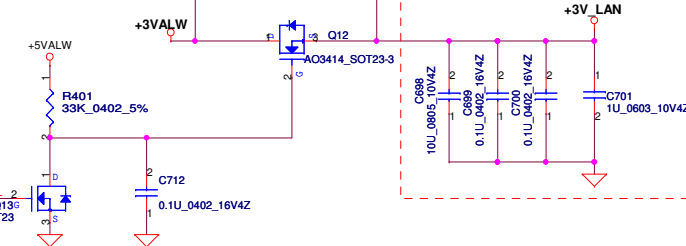


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Size	Document Number	Date		Rev	Date	
	KIWAX_LA-5081P	Tuesday, April 28, 2009		1.0	Sheet 30 of 51	

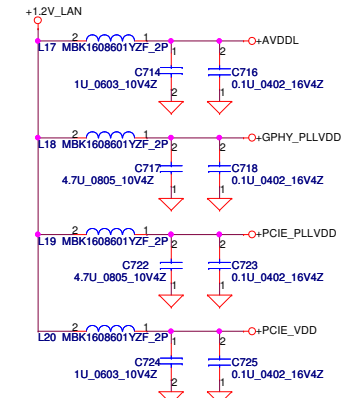
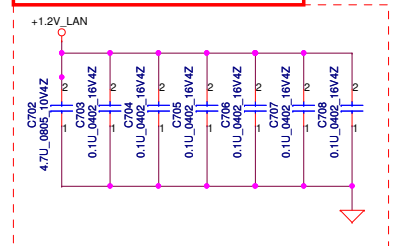
Layout Notice : Filter place as close chip as possible.



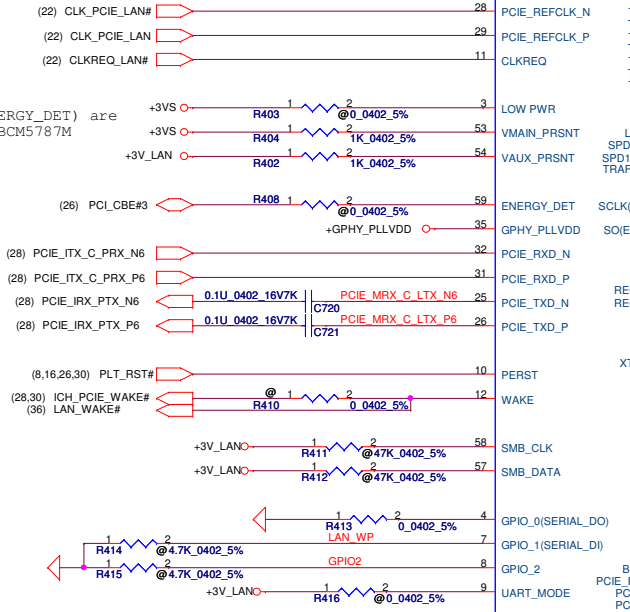
Layout Notice : Place as close chip as possible.



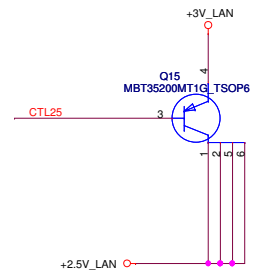
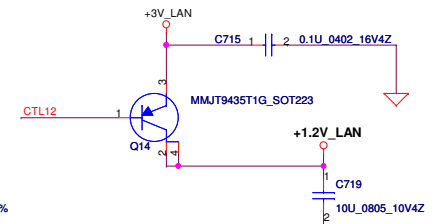
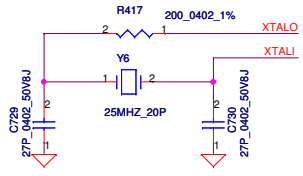
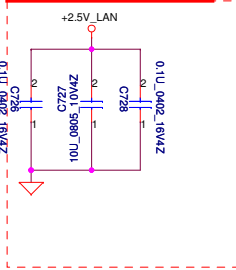
Layout Notice : 1.2V filter. Place as close chip as possible.



(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M

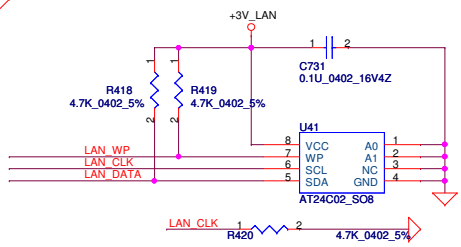


Layout Notice : Place as close chip as possible.



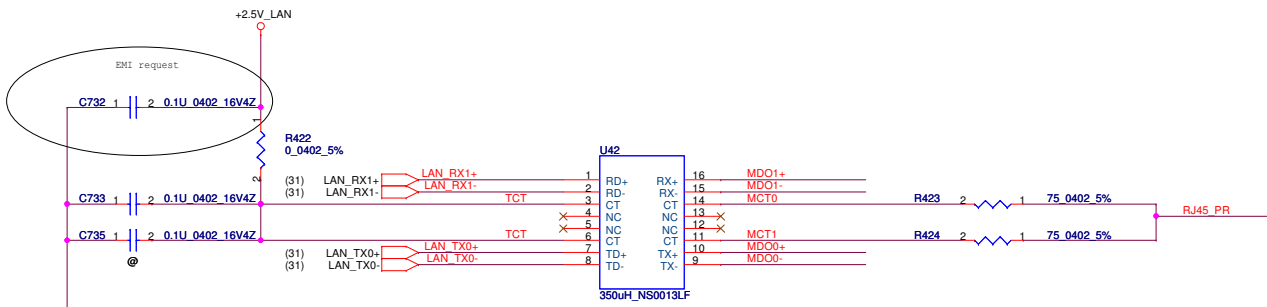
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

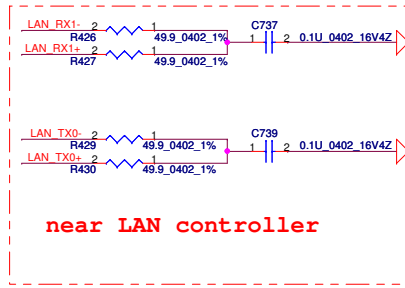


Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05
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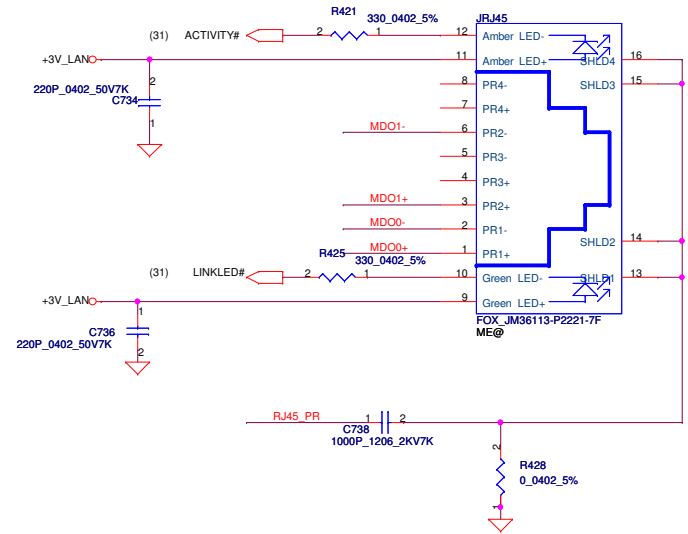
Title			
Compal Electronics, Inc.			
BCM5906			
Size	Document Number	Rev	
Custom	KIWA5/6 LA-5081P	1.0	
Date:	Tuesday, April 28, 2009	Sheet	31 of 51



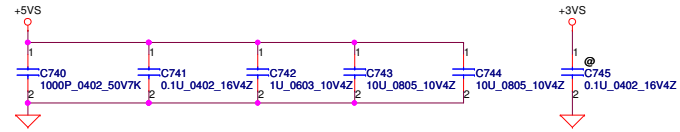
Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



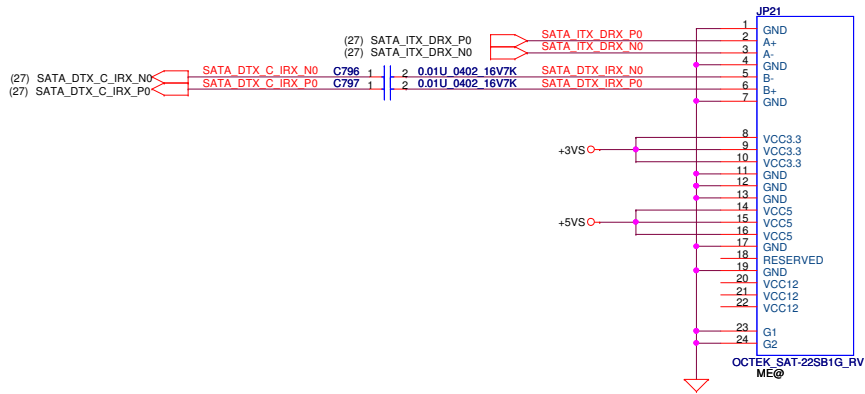
## RJ45 CONN



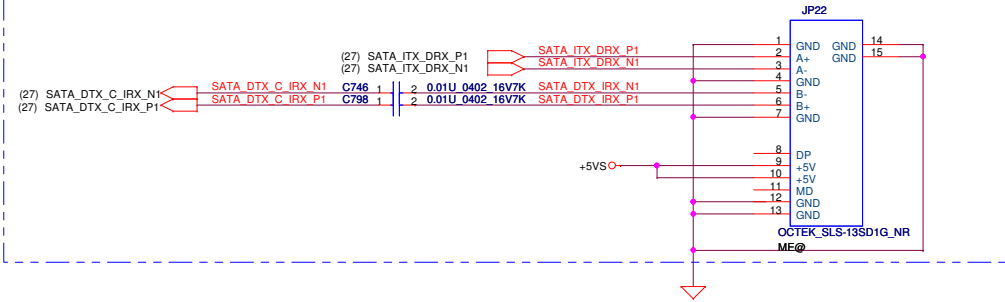
Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05	LAN CONTROLLER	
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Date: Tuesday, April 28, 2009				Rev 1.0	Page 32 of 51



### SATA HDD Conn.



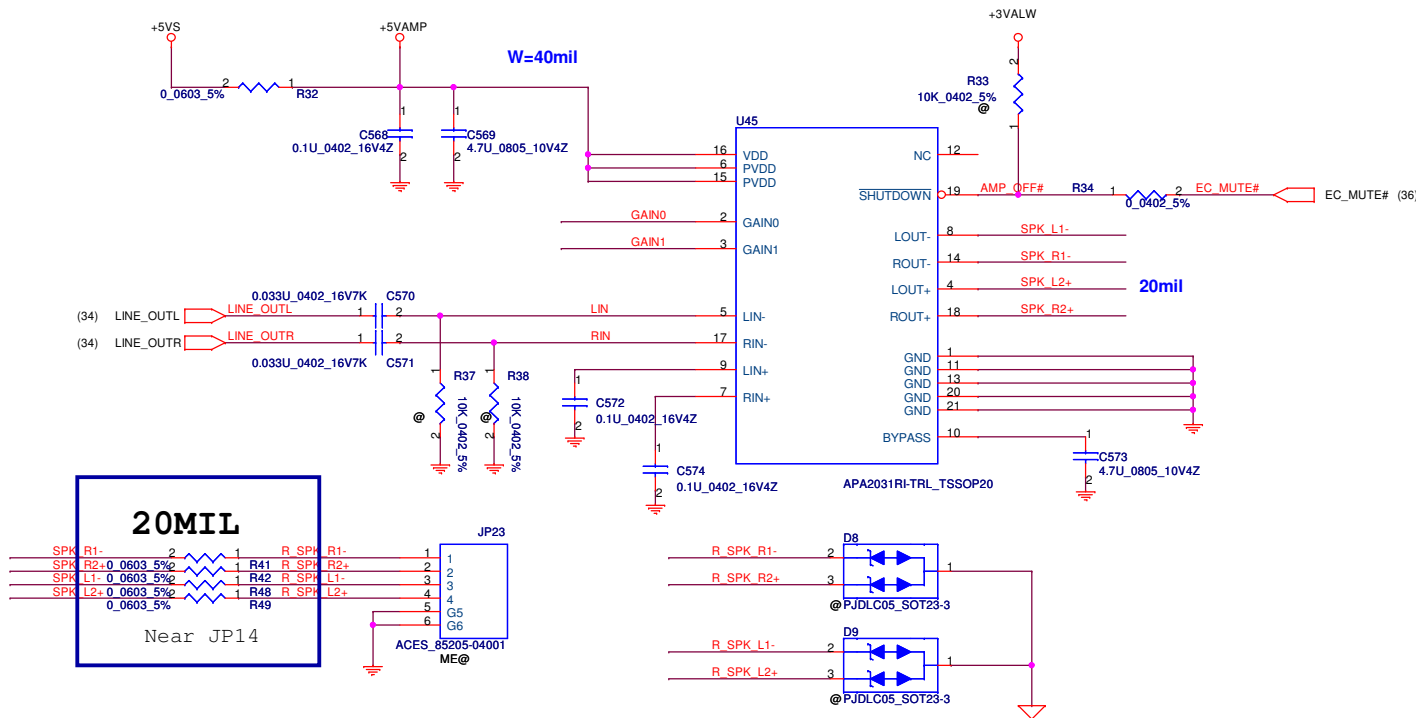
### SATA ODD Conn.



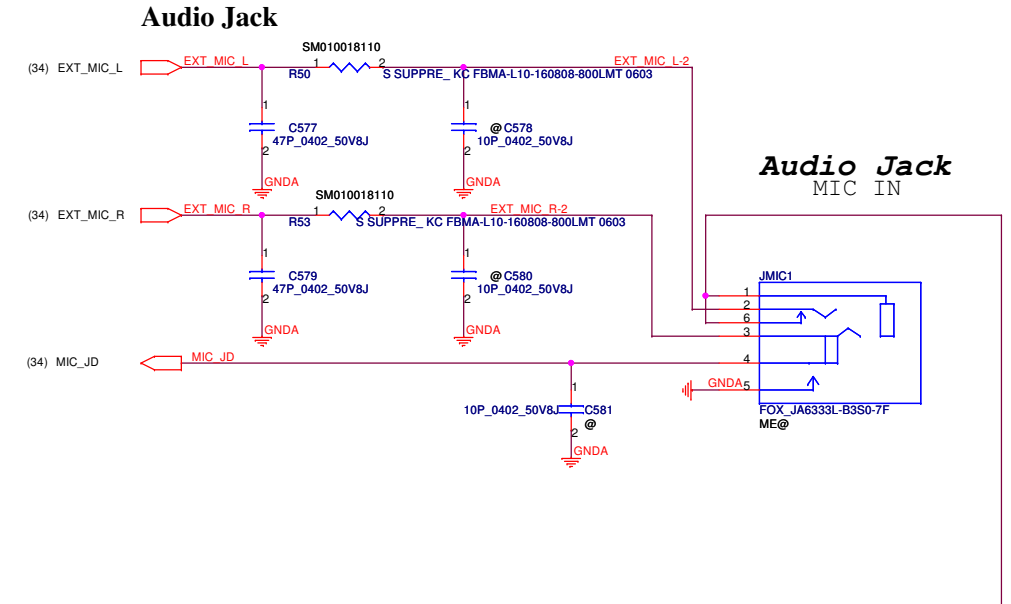
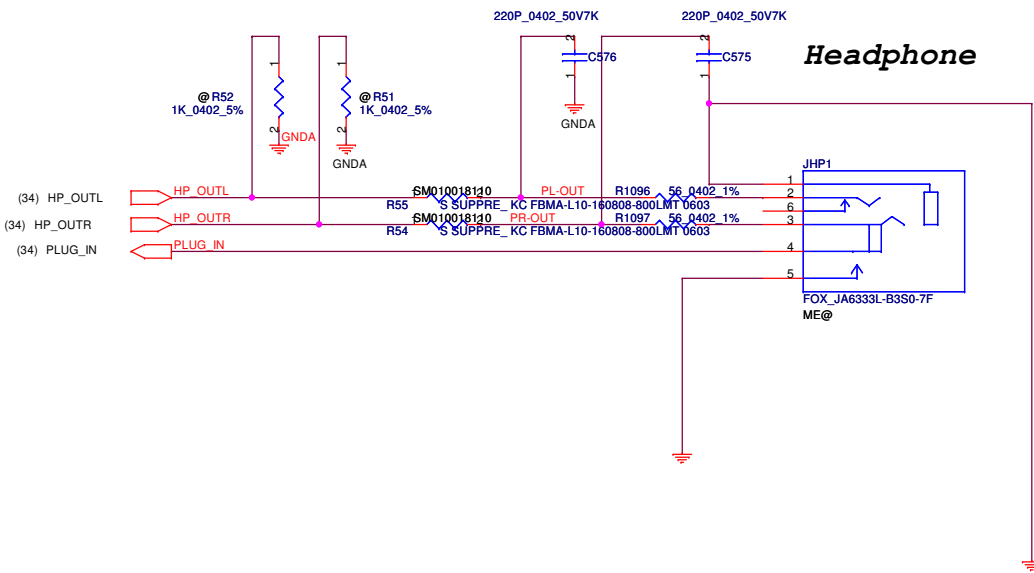
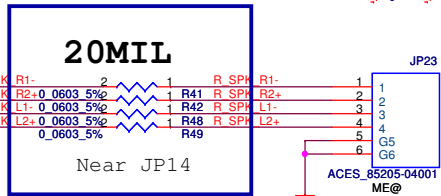
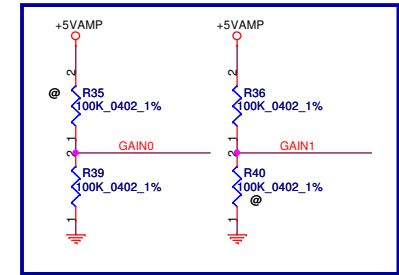
Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05	<b>Compal Electronics, Inc.</b> <b>HDD &amp; ODD Connector</b>	
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				<b>KIWA5/6 LA-5081P</b>	
				Date: Tuesday, April 28, 2009	Rev 1.0
				Sheet 33	of 51



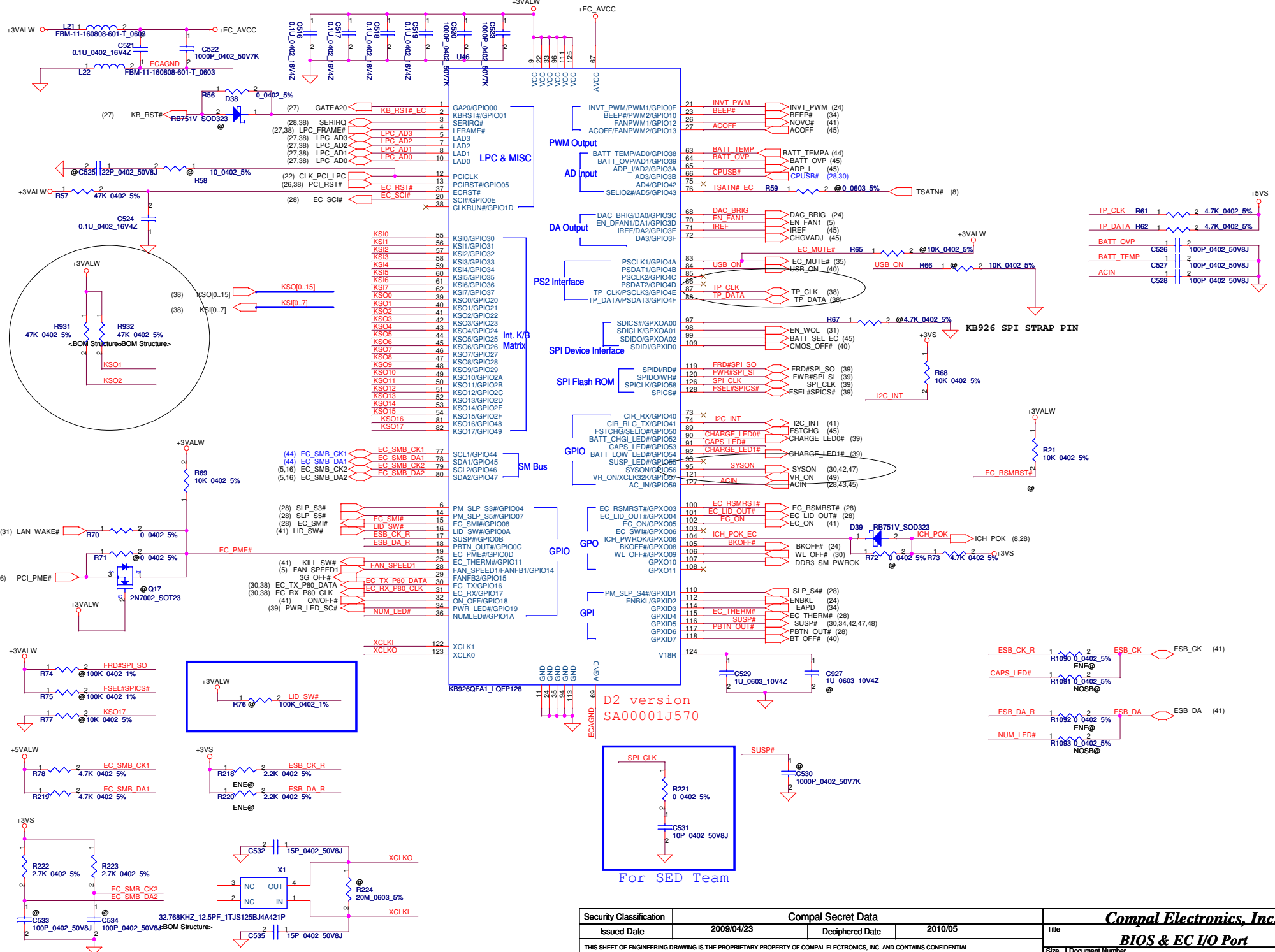
# Speaker Connector



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

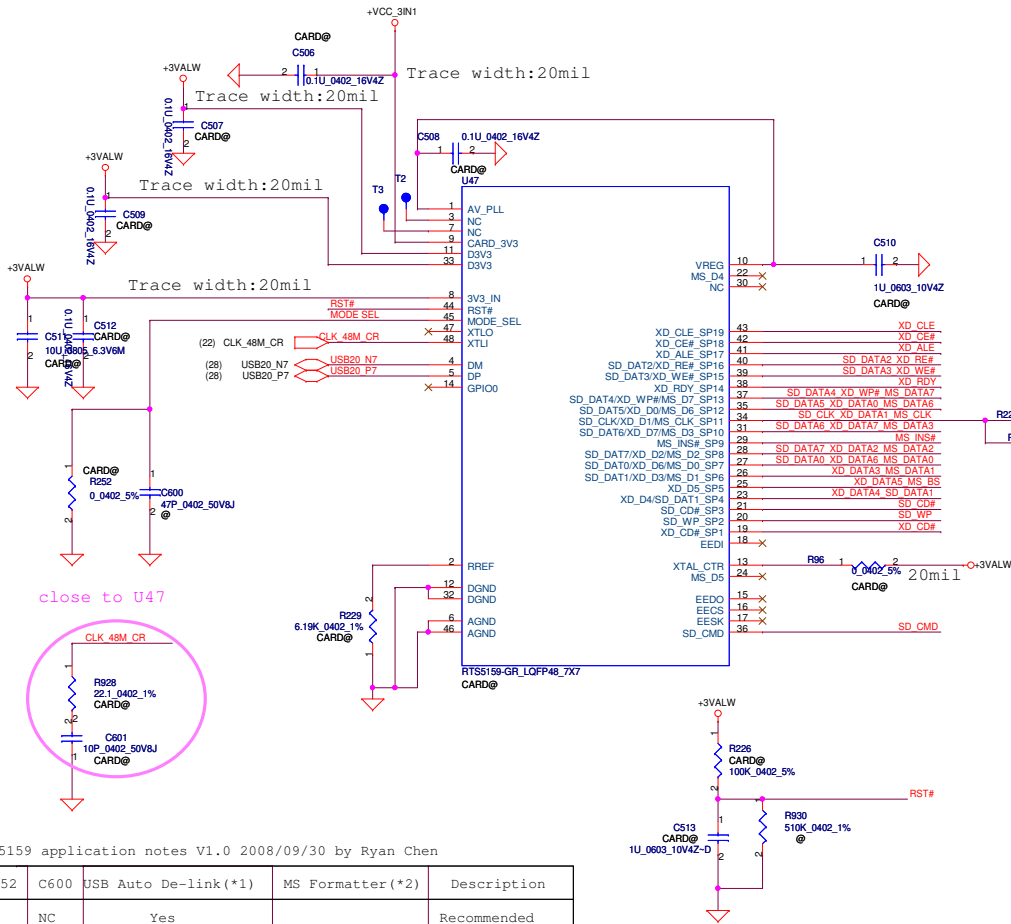


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Issued Date	2009/04/23	Deciphered Date	2010/05	Title	AMP Audio speaker CONN
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				Customer	KIWA5/6 LA-5081P
				Date	Tuesday, April 28, 2009
				Sheet	35 of 51
				Rev	1.0

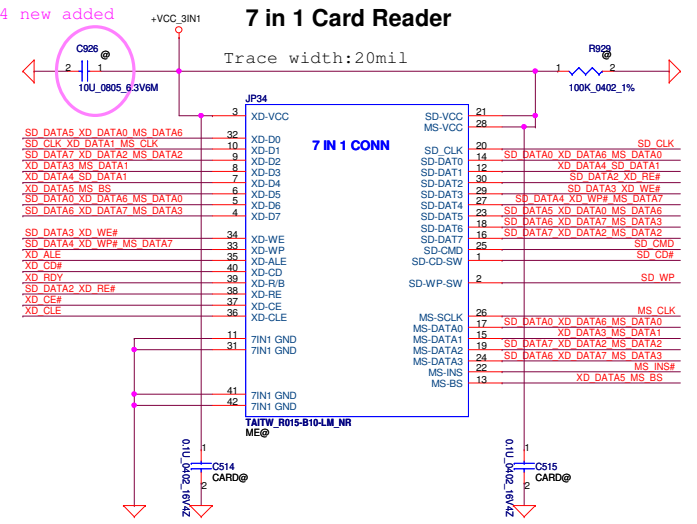




# Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



11/04 new added



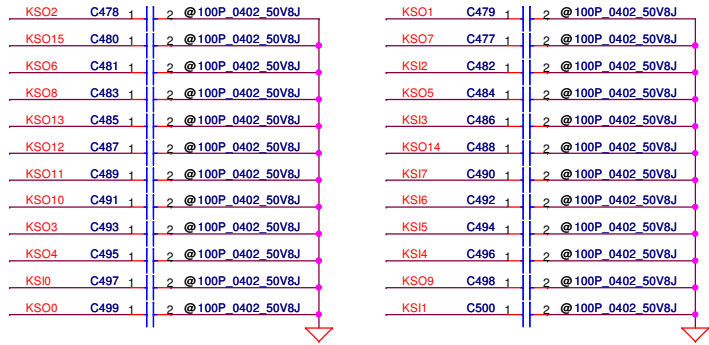
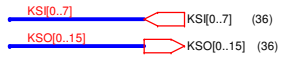
RTS5159 application notes V1.0 2008/09/30 by Ryan Chen

R252	C600	USB Auto De-link(*1)	MS Formatter(*2)	Description
0	NC	Yes		Recommended
NC	47pF	Yes	Yes	
NC	NC			Compatible with RTS5158E
NC	680pF	Yes		LED ON (*3)
10K	180pF			LED ON (*3)
10K	680pF		Yes	

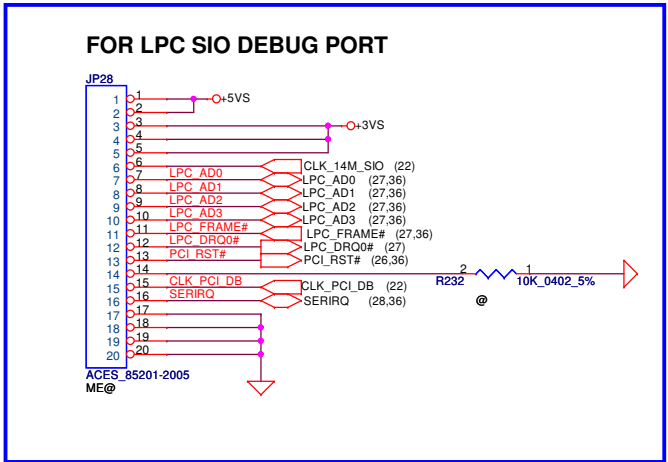
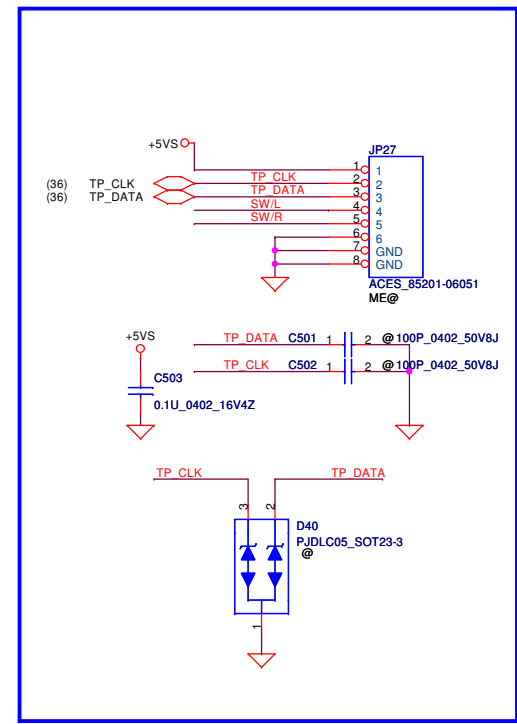
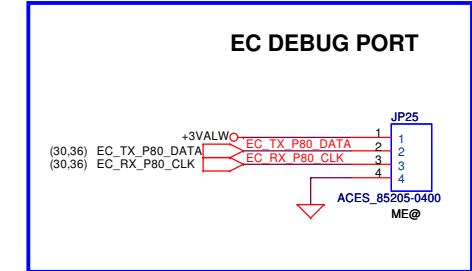
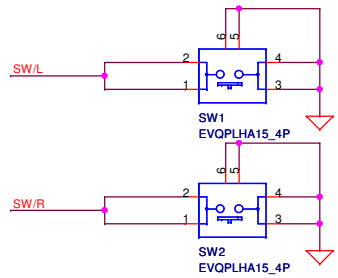
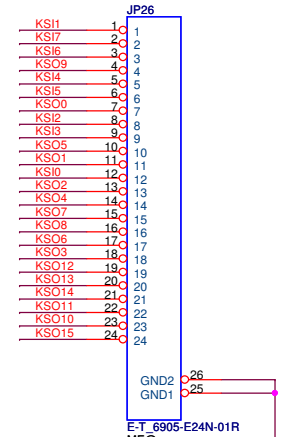
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2009/04/23	Deciphered Date	2010/05	USB_CR board			
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Size	Document Number	KTIWAX_LA-5081P		Rev	1.0		
Date	Tuesday, April 28, 2009	Sheet	37	of	51		

Source:SP01000IE00  
 2nd source:SP01000IF00  
 30 pin

**INT\_KBD Conn.**

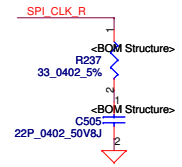
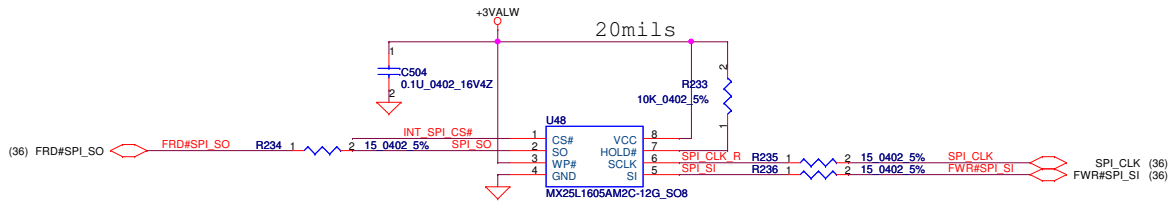


CONN PIN define need double check

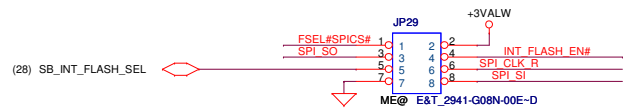
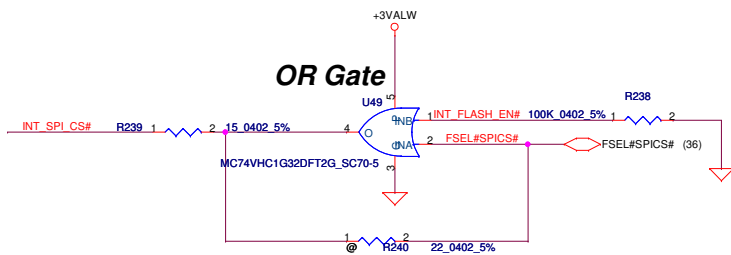


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Size	Document Number	Date		Rev	1.0
B	KIWA5/6 LA-5081P	Tuesday, April 28, 2009		Sheet	38 of 51

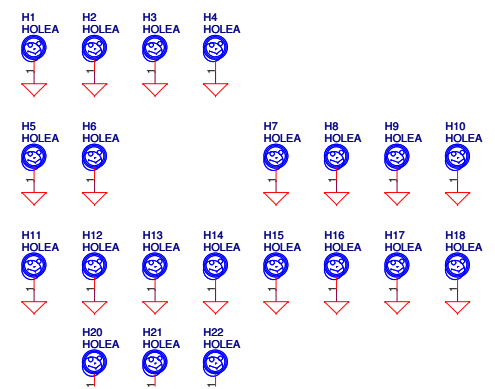
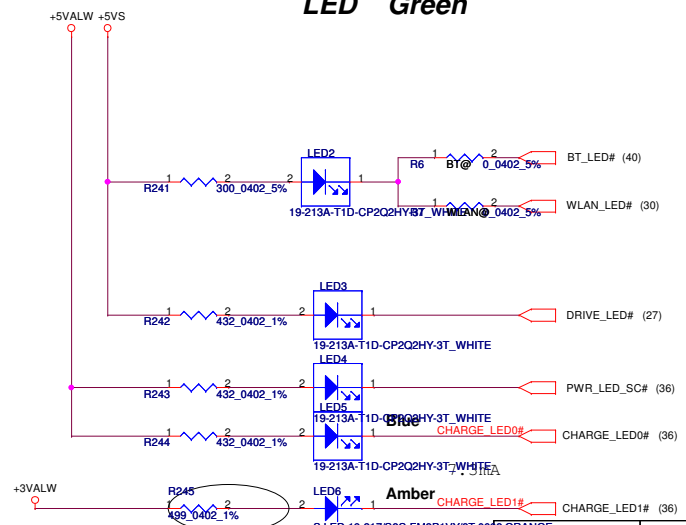
FOR EC 16M SPI ROM



INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H



LED Green



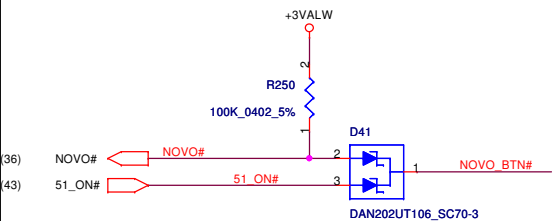
Security Classification				Compal Secret Data		Title	
Issued Date		2009/04/23		Deciphered Date		2010/05	
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Date: Tuesday, April 28, 2009						Sheet 39 of 51	

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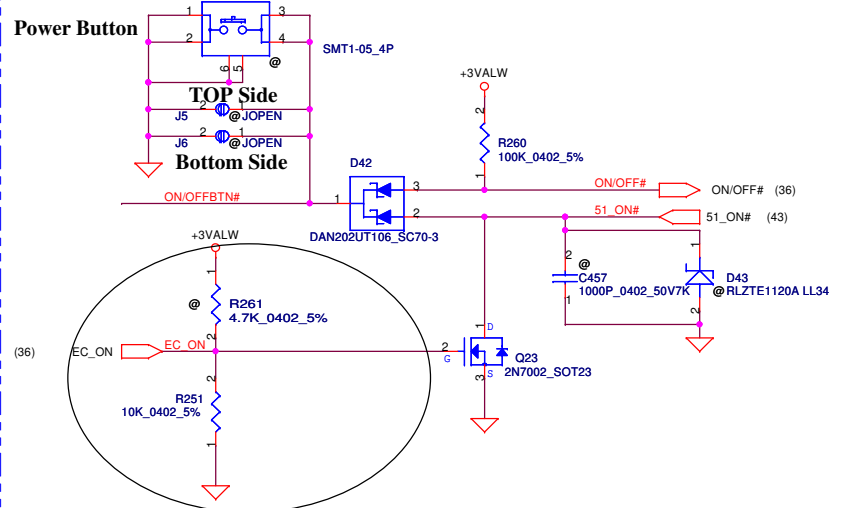
LED/EC SPI ROM

Size B	Document Number	Rev 1.0
KIWA5/6 LA-5081P		

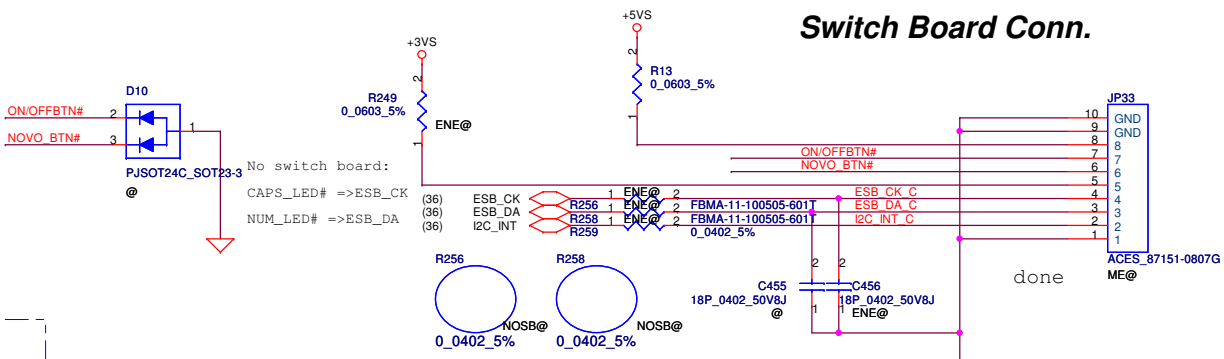
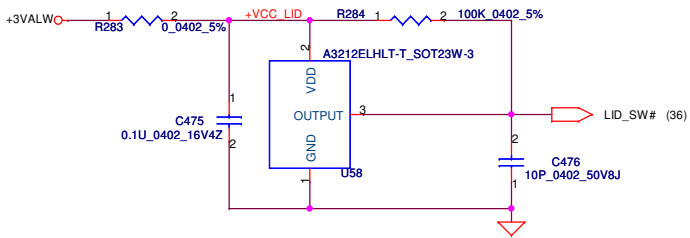




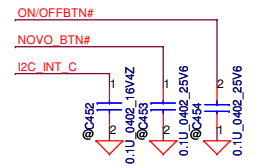
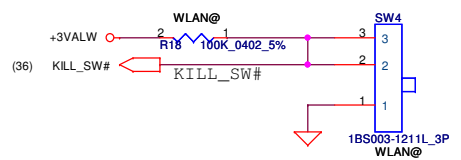
### ON/OFF switch



### Lid Switch

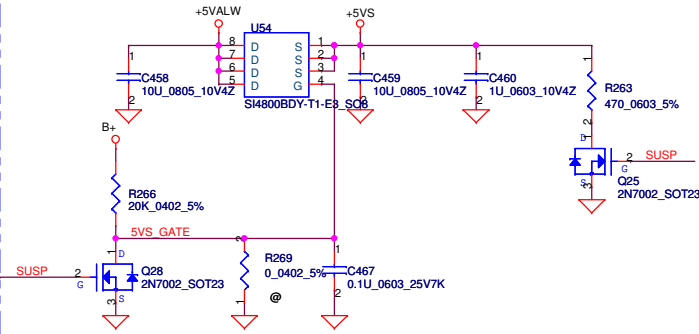


02/26 remove Smbus for CY  
Kill Switch

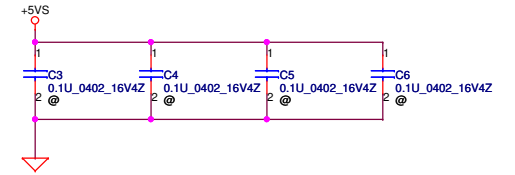
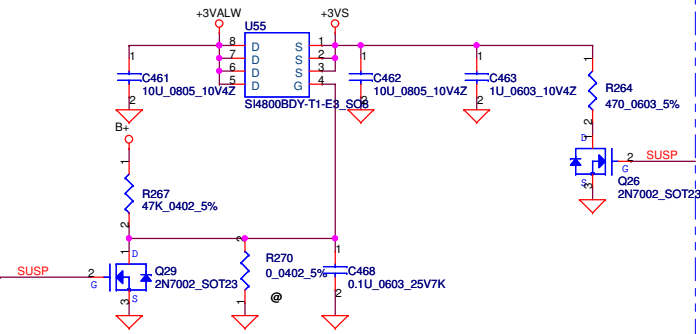


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Size Custom	Document Number	KIWA5/6 LA-5081P		Rev 1.0
Date: Tuesday, April 28, 2009	Sheet	41	of	51

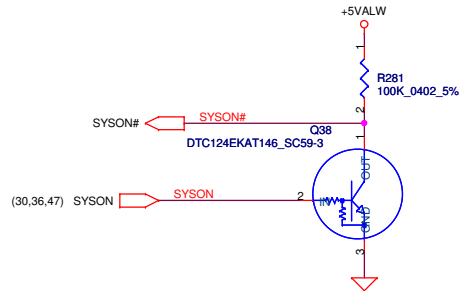
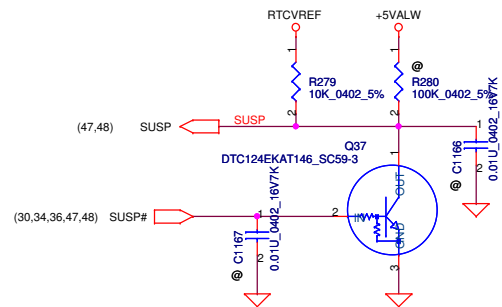
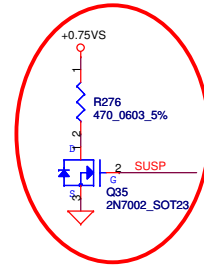
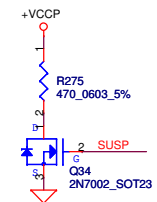
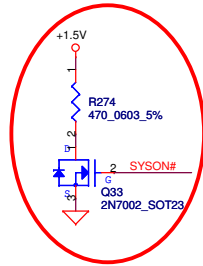
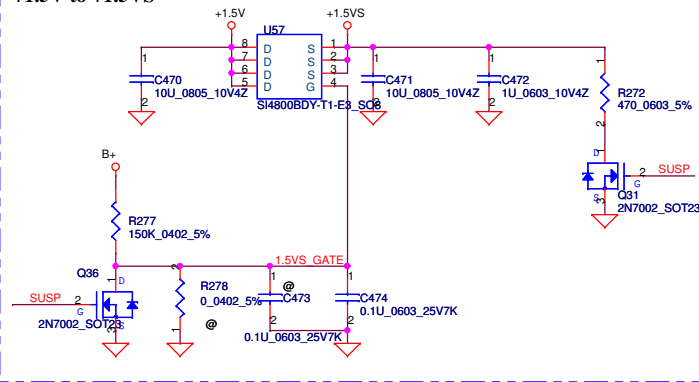
**+5VALW TO +5VS**



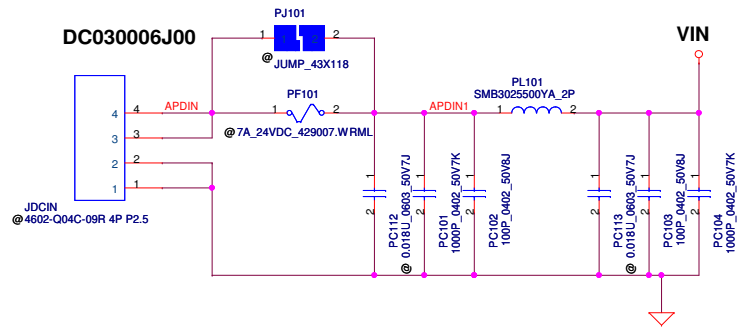
**+3VALW TO +3VS**



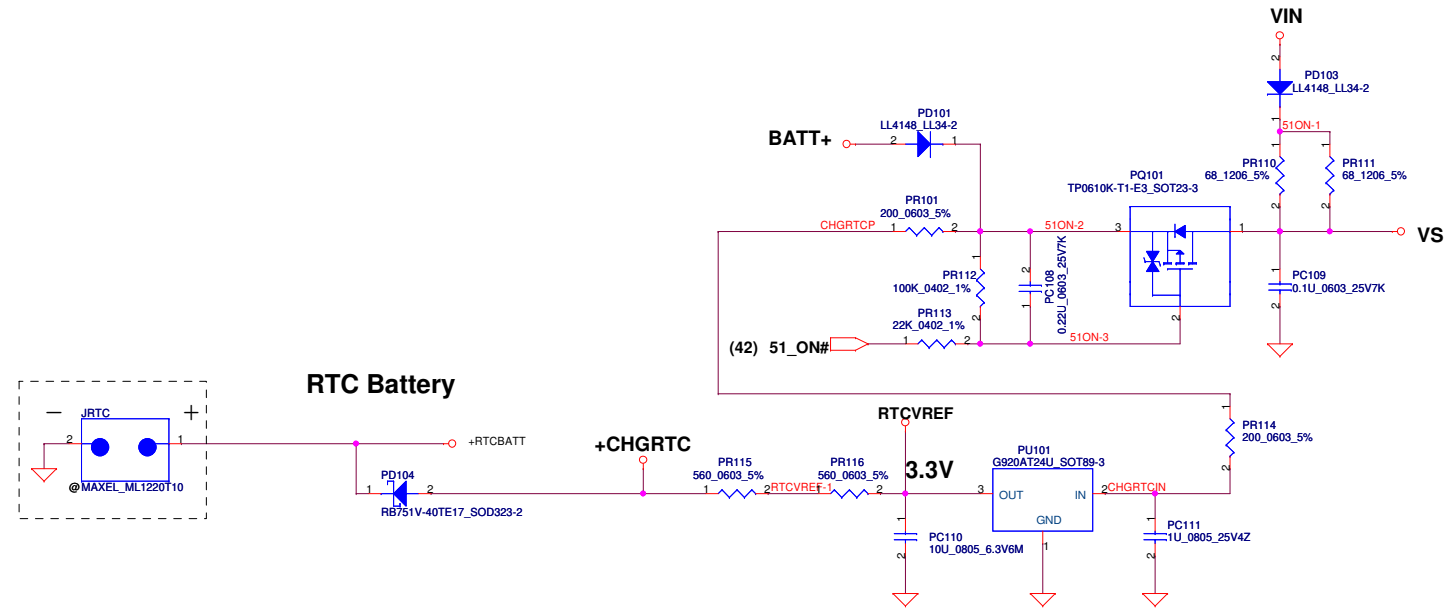
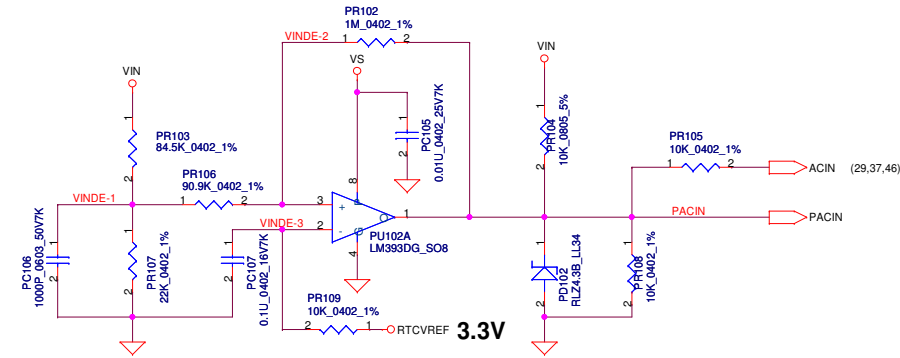
**+1.5V to +1.5VS**



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Size	Document Number	Rev		1.0	
Custom	KIWA5/6 LA-5081P	Date:		Tuesday, April 28, 2009	
				Sheet	42 of 51

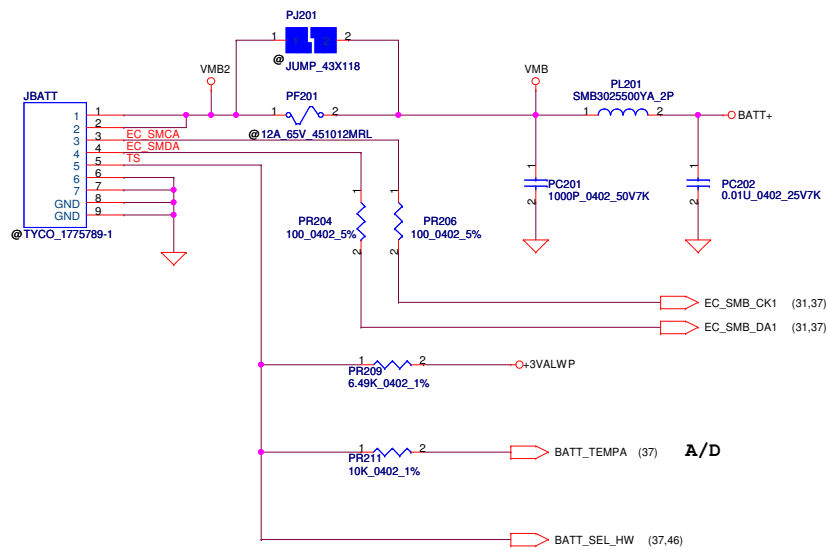


Vin Detector		
High	17.944	17.470
Low	16.242	15.808



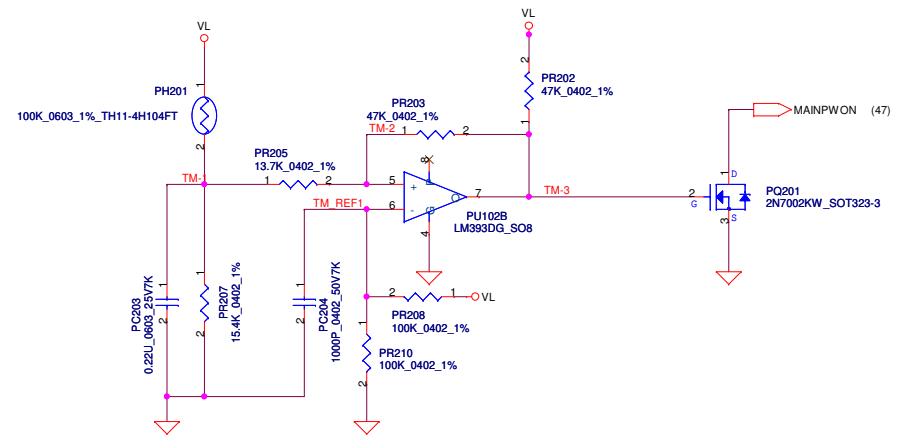
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title				
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Size	Document Number				Rev			
Custom					0.1			
Date:	Tuesday, April 28, 2009	Sheet	44	of	53			



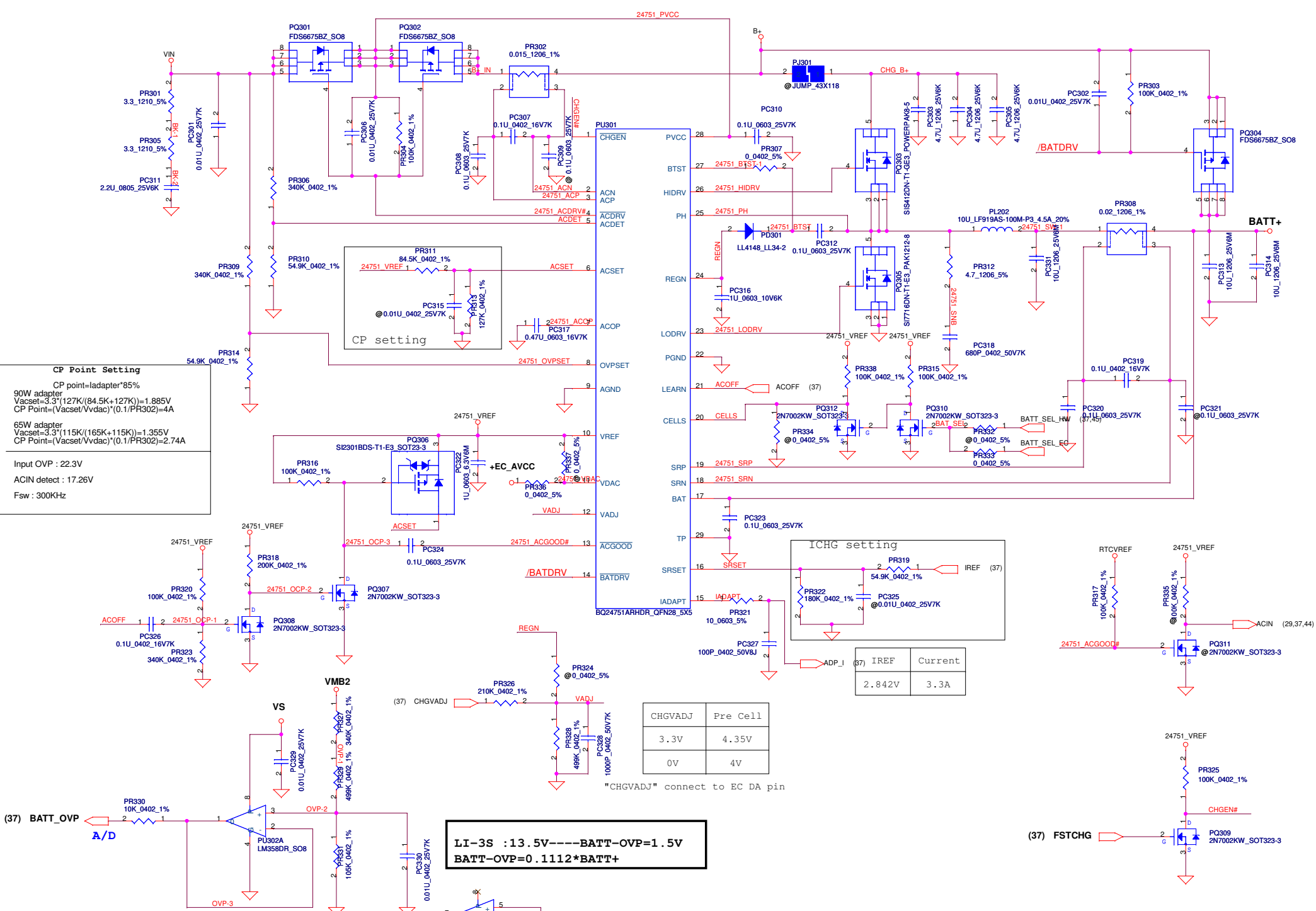


**PH1 under CPU bottom side :**

CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



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Size	Document Number			Rev	
				0.1	
Date:	Tuesday, April 26, 2009	Sheet	45	of	53



**CP Point Setting**

CP point=ladapler\*85%

90W adapter  
 $V_{acset}=3.3 \times (127K / (84.5K + 127K)) = 1.885V$   
 $CP\ Point = (V_{acset} / V_{vdac}) \times (0.1 / PR302) = 4A$

65W adapter  
 $V_{acset}=3.3 \times (115K / (165K + 115K)) = 1.355V$   
 $CP\ Point = (V_{acset} / V_{vdac}) \times (0.1 / PR302) = 2.74A$

Input OVP : 22.3V  
 ACIN detect : 17.26V  
 Fsw : 300KHz

**CP setting**

PR311 84.5K\_0402\_1%  
 PC315 @0.01U\_0402\_25V7K  
 PR313 127K\_0402\_1%

**ICHG setting**

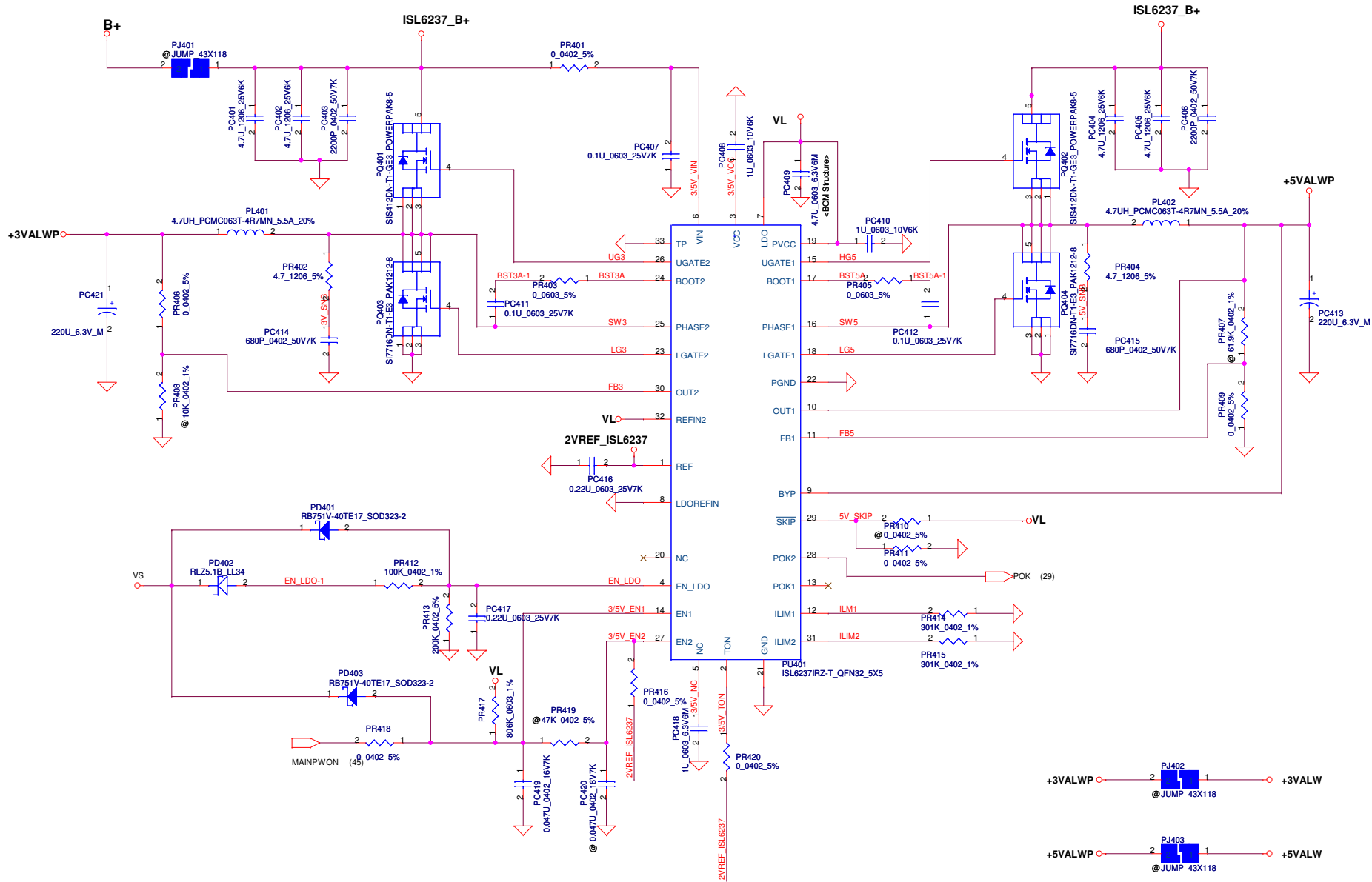
PR319 54.9K\_0402\_1%  
 PC325 @0.01U\_0402\_25V7K  
 PR322 180K\_0402\_1%

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

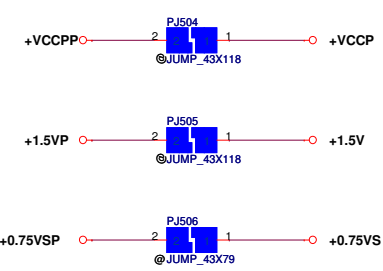
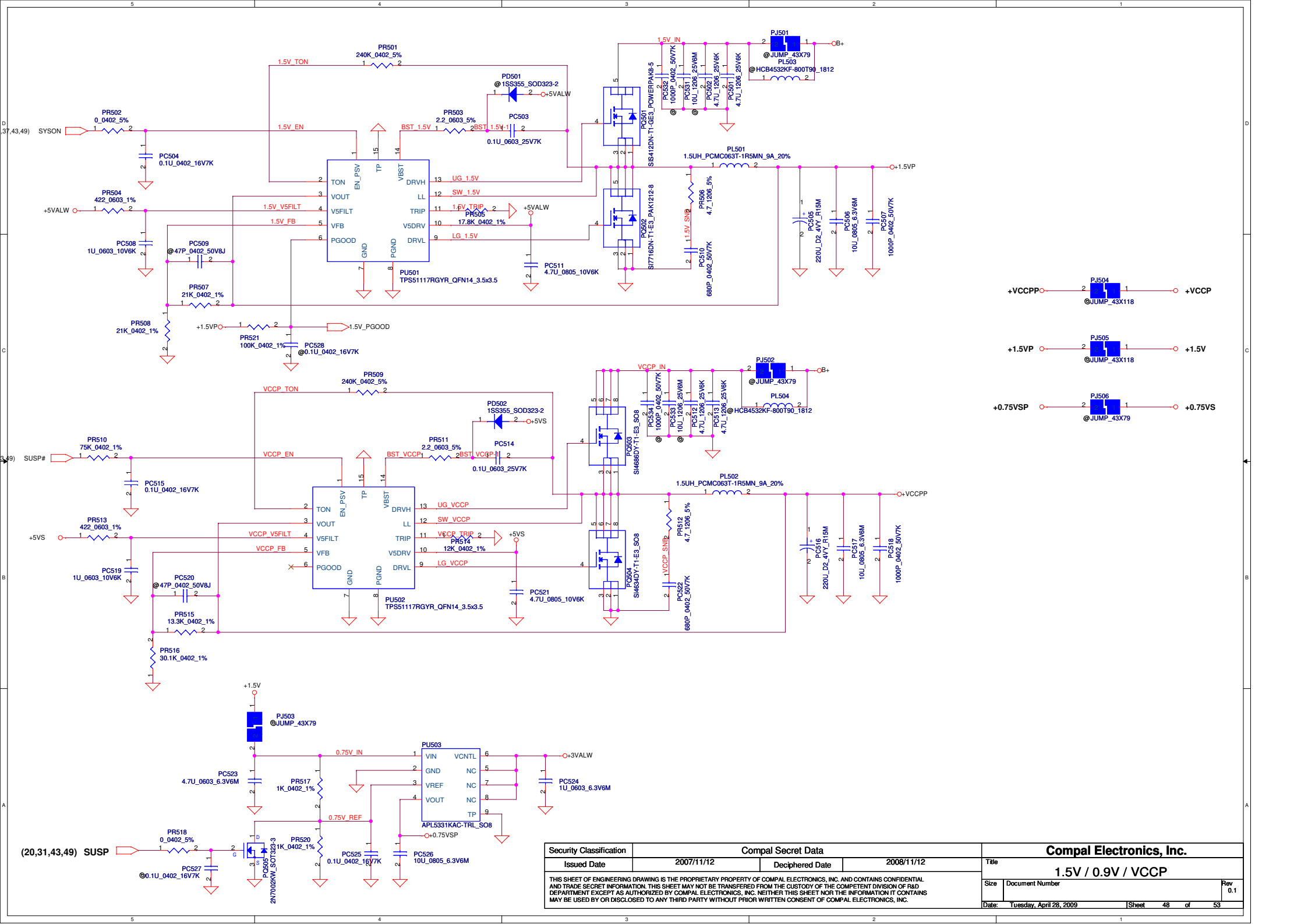
"CHGVADJ" connect to EC DA pin

**LI-3S : 13.5V----BATT-OVP=1.5V**  
**BATT-OVP=0.1112\*BATT+**

ADP_I (37)	IREF	Current
		2.842V
		3.3A

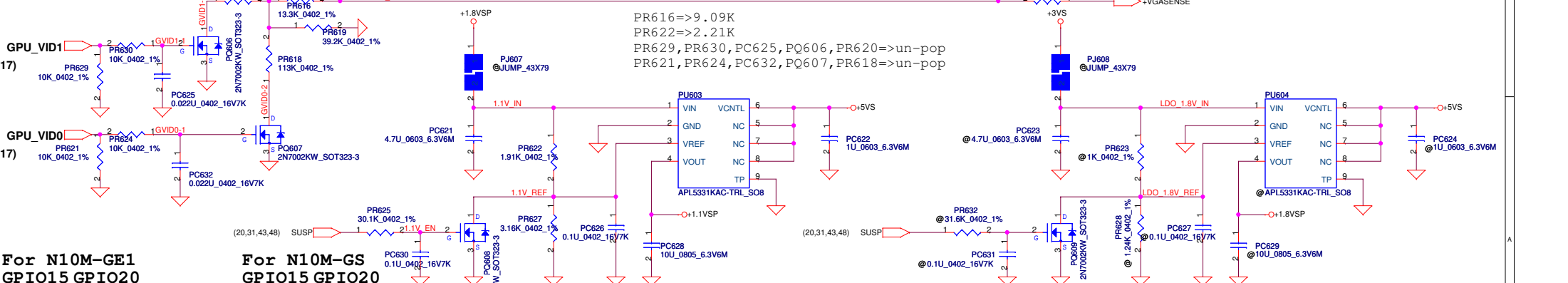
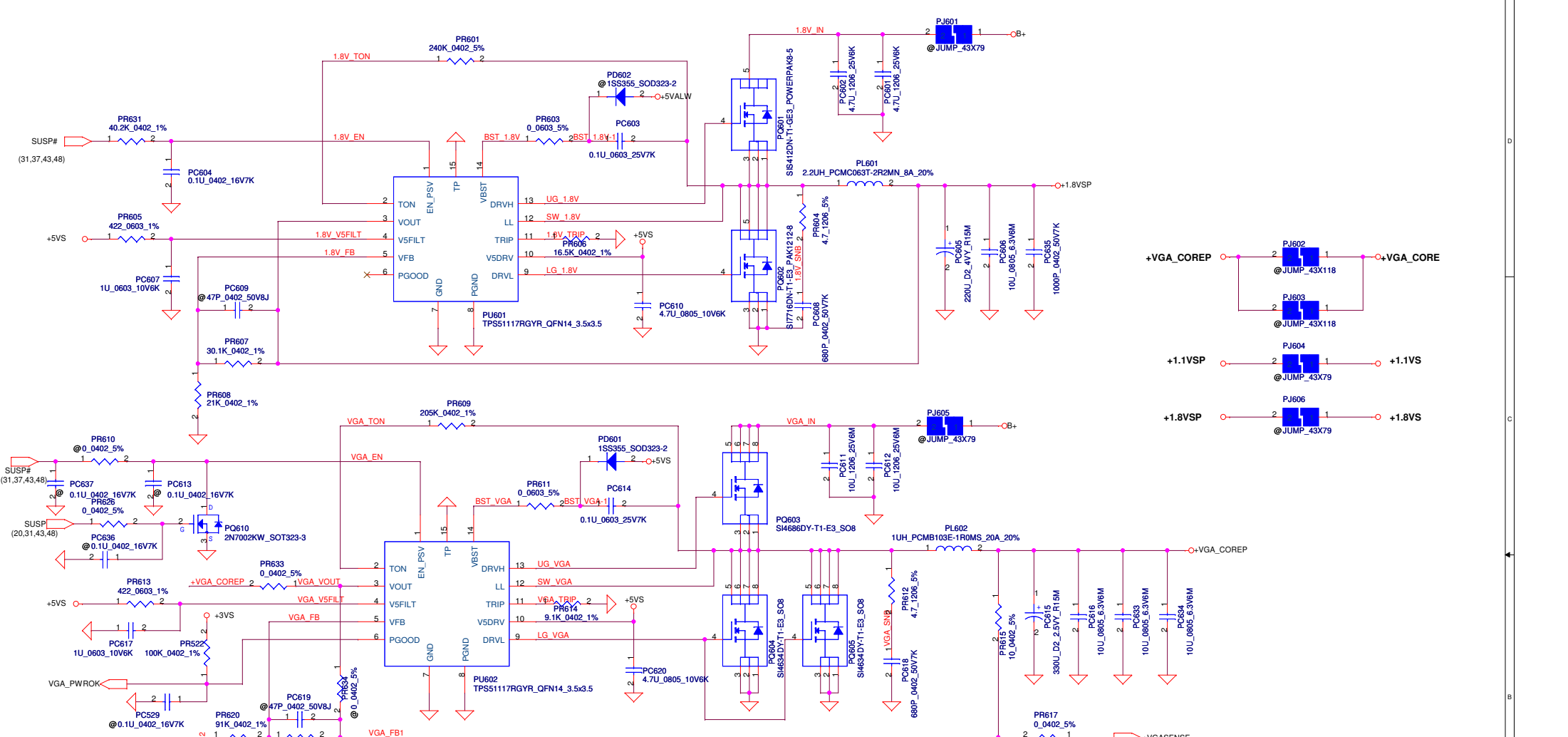


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Date: Tuesday, April 28, 2009				Rev 0.1
Sheet 47 of 53				



(20,31,43,49) SUSP

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Date:	Tuesday, April 28, 2009	Sheet	48	of	53



For N10M-GE1  
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS  
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
0	1	0.9V
1	1	1.0V

PR616=>9.09K  
PR622=>2.21K  
PR629, PR630, PC625, PQ606, PR620=>un-pop  
PR621, PR624, PC632, PQ607, PR618=>un-pop

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Date: Tuesday, April 28, 2009			Sheet 49 of 53

**Compal Electronics, Inc.**  
VGA\_CORE/1.8V/1.1VS



Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)	2009.01.14	
3							
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21							

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Size	Document Number	Date		Rev	
Custom	LA-5081P	Tuesday, April 28, 2009		0.1	
				Sheet	51 of 53



NO DATE PAGE

MODIFICATION LIST

PURPOSE

1 12/10 39 Remove D11, and add R6, R7  
 12/10 36 change PWR\_LED\_SC# from U46.38 to U46.34

2 1/15 39 modify H18 hold size, and change the H5、H6 and H18 hold type.  
 42 add 4 CAPs C3, C4, C5 and C6 for EMI.  
 35 change C572 and C574 footprint from 0603 to 0402.  
 34 add R25 for BEEP# test

3 3/16 06 add R1089, C1162 and H\_DPRSTP#\_R  
 add C1163, C1164, and C1165 for EMC request.  
 08 change H\_DPRSTP# to H\_DPRSTP#\_R  
 19 P19 add Bom structure 40nm@ GPU and 55nm@ GPU  
 R999 change to 24.9K  
 23 add R1095 pull high  
 35 swap HP\_OUTL and HP\_OUTR  
 36 add R1090, R1091, R1092, R1093  
 CAPS\_LED#, NUJM\_LED#, ESB\_CK\_R, and ESB\_DA\_R  
 41 add R256, R258 Bom configuration  
 Remove CY SMBus  
 42 add C1166, C1167 for EMC request.

4 4/20 27 R829 changed to 0ohm.  
 08 R80 changed to 33ohm  
 34 R1044 changed to 33ohm  
 R1056 changed to 33ohm  
 C1089 changed to 10P

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				Size B	Document Number	Rev	1.0
				Date:	Tuesday, April 28, 2009	Sheet	51 of 51