LWG2-D Block Diagram (Discrete)

Project code: 91.4Q801.001
PCB P/N : 55.4Q801.XXX
REVISION : 06210-2
(Hannstar, ACCL)

CLK GEN.
IDT CV125PA 3

Mobile CPU
Yonah 478
1.83G/2G/2.16G 4, 5

G792 19

HOST BUS 400/533/667MHz

DDR2 533 MHz 11,12
DDR2 533 MHz 11,12
533/667MHz
533/667MHz

Calistoga
Ver.:A3 :71.945PM.A0U / QK58
KI.94501.006 / SL8Z4
6,7,8,9,10

PCI Express x16
M56 Ver.: B24
M52 Ver.: A12
M54 Ver.: A12

ATI M54P / M52P 42,43,44,45
VRAM x4 128/256M 47,48

TVO 14
LVDS
14"WSXGA+ LCD 13
RGB CRT
CRT 14

DMI I/F 100MHz

ICH7M
Ver. : B0, 71.ICH7M.A0U / QK65
KI.80101.017 / SL8YB
15,16,17,18

AZALIA
Codec ALC883 28
29 MIC In
INT.MIC
29 INT.SPKR
Line Out 29
OP AMP G1432 29
OP AMP MAX4411 29
RJ11
MODEM MDC Card 21

PCI BUS
TI PCI 7412
CARDBUS 1394 CardReader 24,25
PCMCIA I/F
PWR SW TSP2220A 27
PCMCIA SLOT Support TypeII 27
1394 CONN 26
MS/MMC/SD 3 in 1 26
Mini-PCI 802.11A/B/G 30

PCIEx1
Giga LAN BCM5789/5787M 22
TXFM 23
RJ45 23
Mini Card*1 802.11A/B/G 26

BCM5787MKFBG-A1
BCM5789KFBG-C1
BCM4401EKFBG-B0

SPI I/F
BIOS SST25LF080A 34
LPC BUS

USB
SATA
PATA

USB 3 PORT 21
Finger Print 20
HDD 20
CDROM 20
MINI USB 21
Blue-tooth

KBC Renesas RE144B 30
LPC DEBUG CONN. 32
Touch Pad 31
INT. KB 31

PCB STACKUP

TOP	
GND	
S	
S	
VCC	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 38

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 40

1D8V_S3	DDR_VREF_S0

APL5332KAC 40

3D3V_S0	2D5V_S0

APL5912-U 40

1D8V_S3	1D5V_S0

MAXIM CHARGER MAX8725 39

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 35, 36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 44A

ATI M54 DC/DC FAN5234 49

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

APL5331KAC 43

1D8V_S0	1D2V_S0

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Wednesday, June 21, 2006 | Sheet 1 of 52

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

History

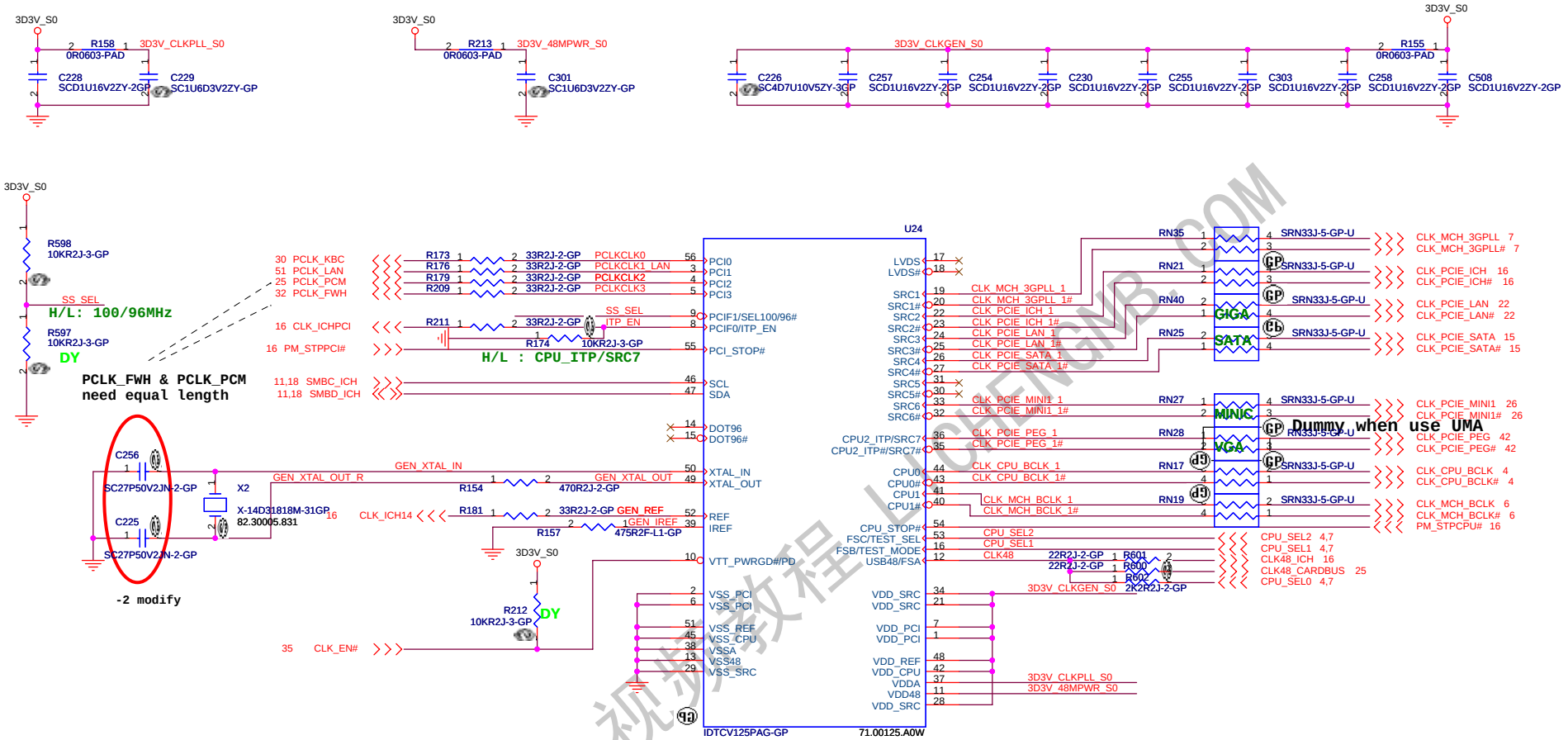
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 2 of 52



SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

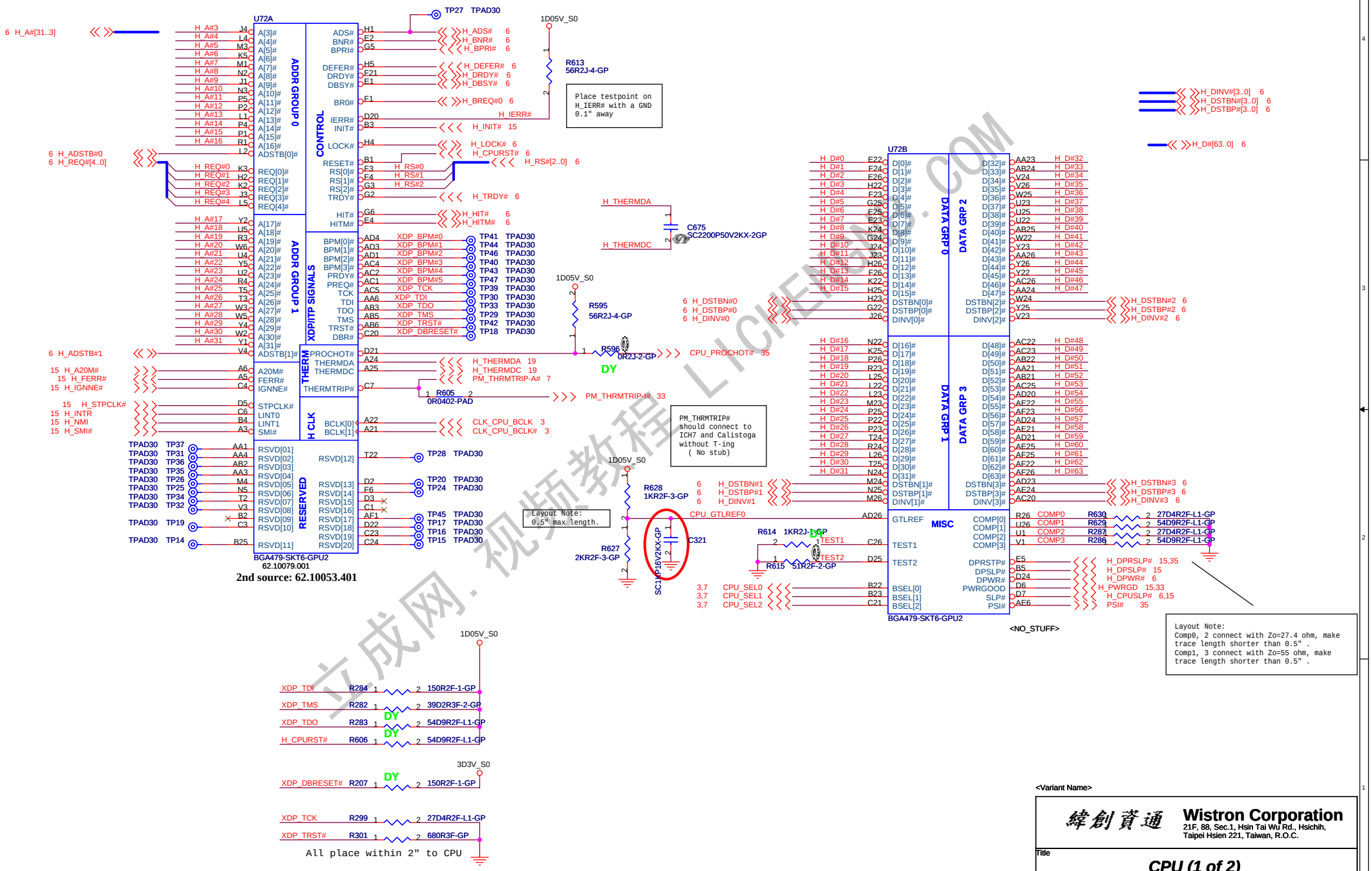
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator IDT CVT125PAG

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 3 of 52



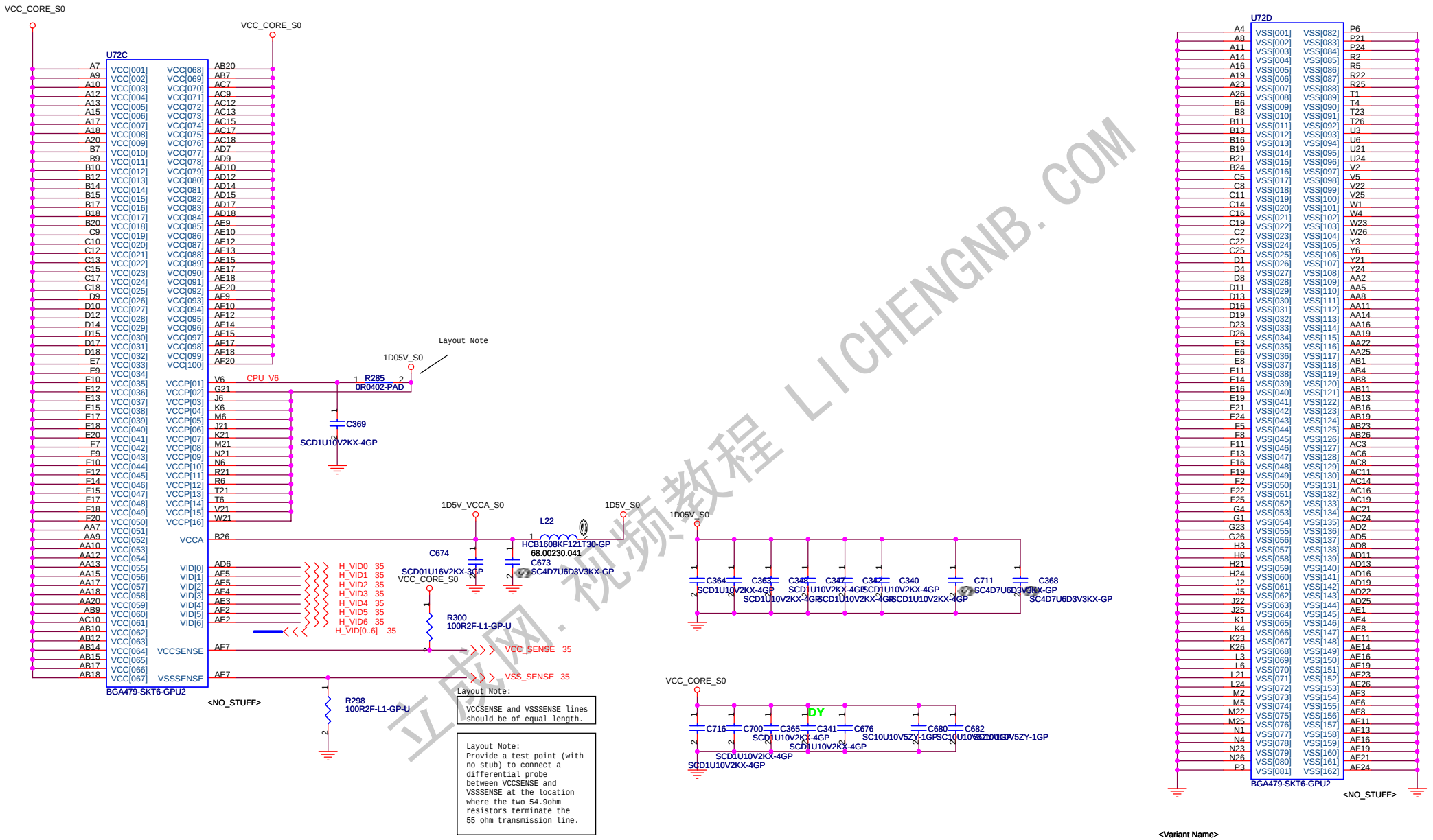
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (1 of 2)

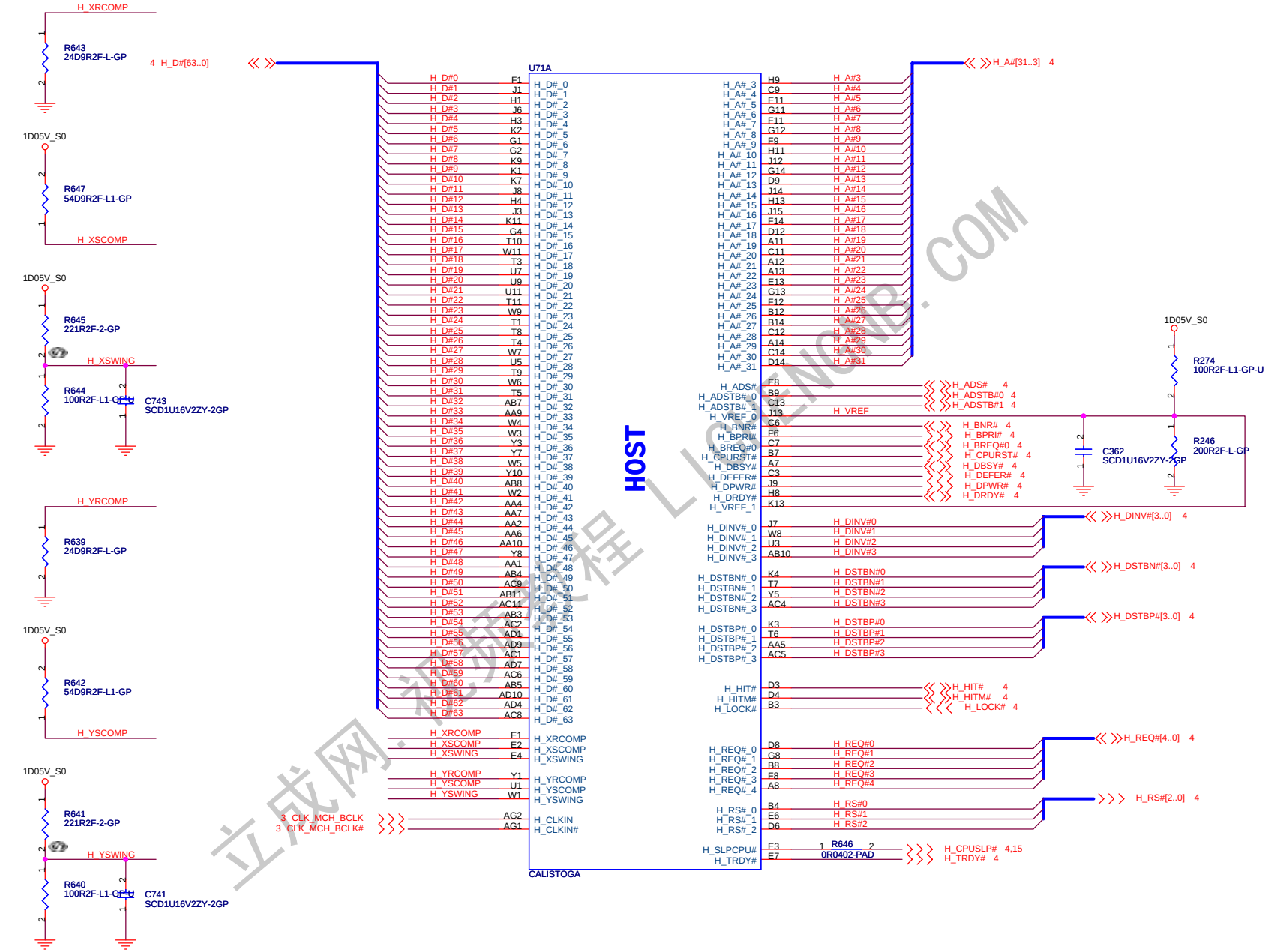
Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 4 of 52



<Variant Name>

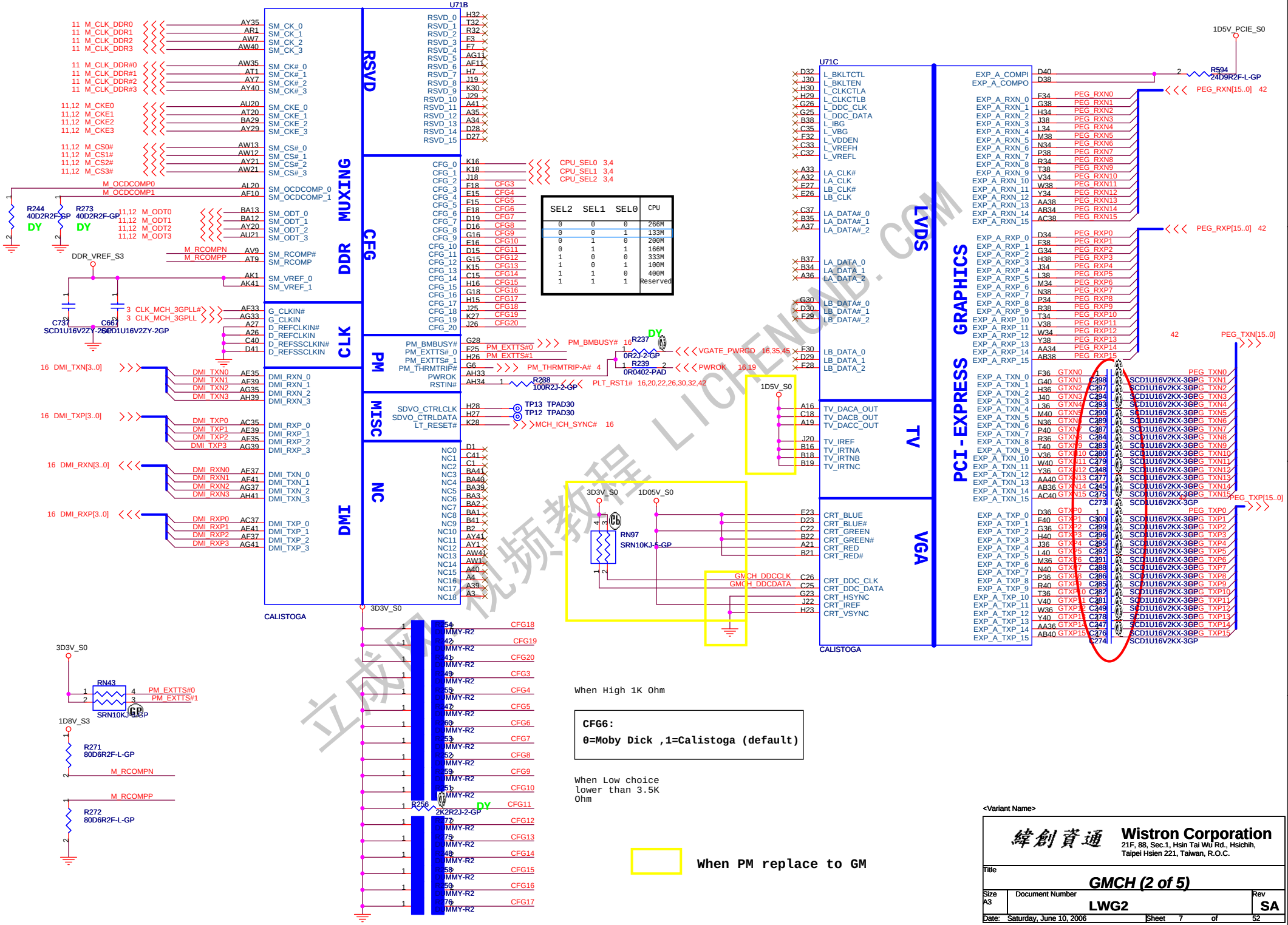
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (2 of 2)
Size A3	Document Number LWG2
Rev	SA
Date: Saturday, June 10, 2006	Sheet 5 of 52

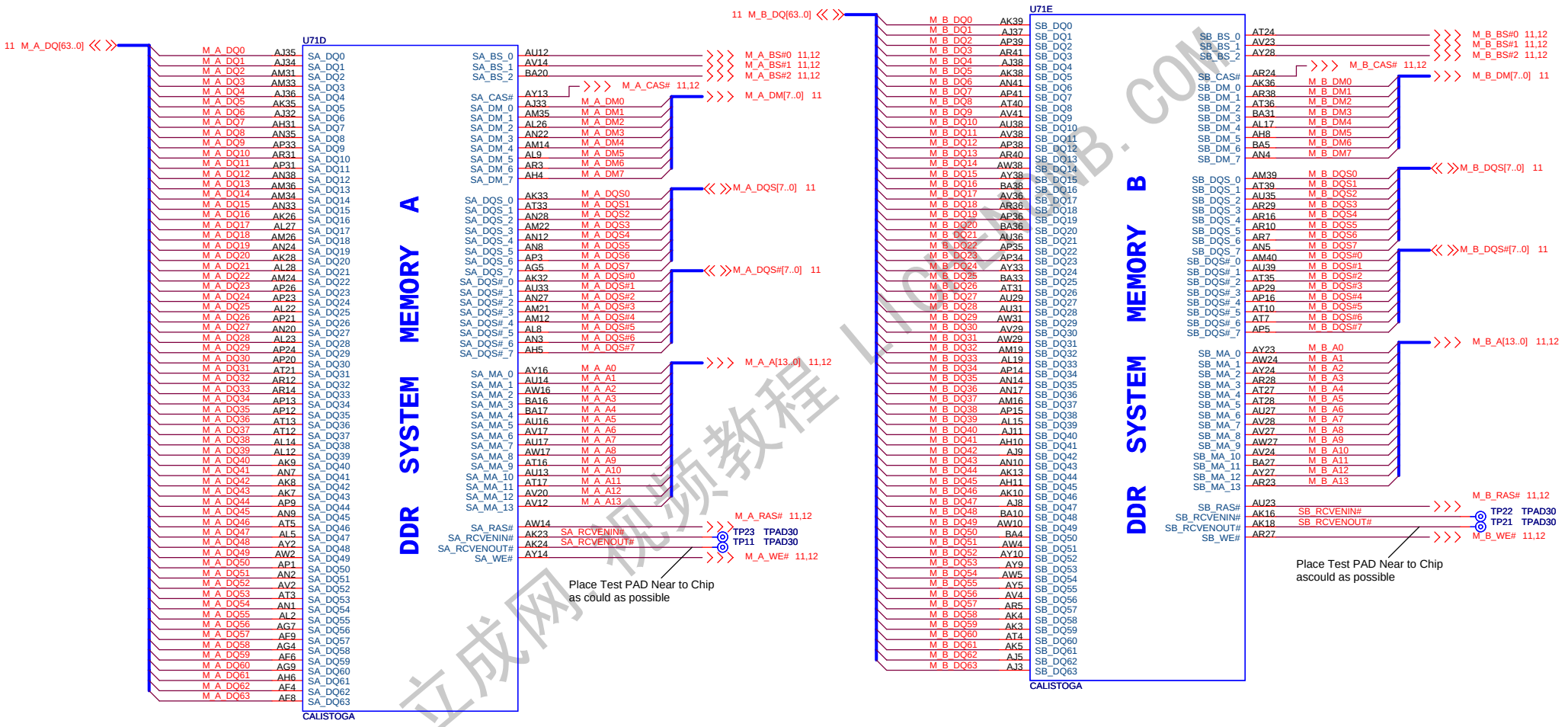


Place them near to the chip (< 0.5")

<variant_name><Variant Name></variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GMCH (1 of 5)		
Size: A3	Document Number: LWG2	Rev: SA
Date: Saturday, June 10, 2006	Sheet 6 of 52	





<Variant Name>

緯創資通 Wistron Corporation
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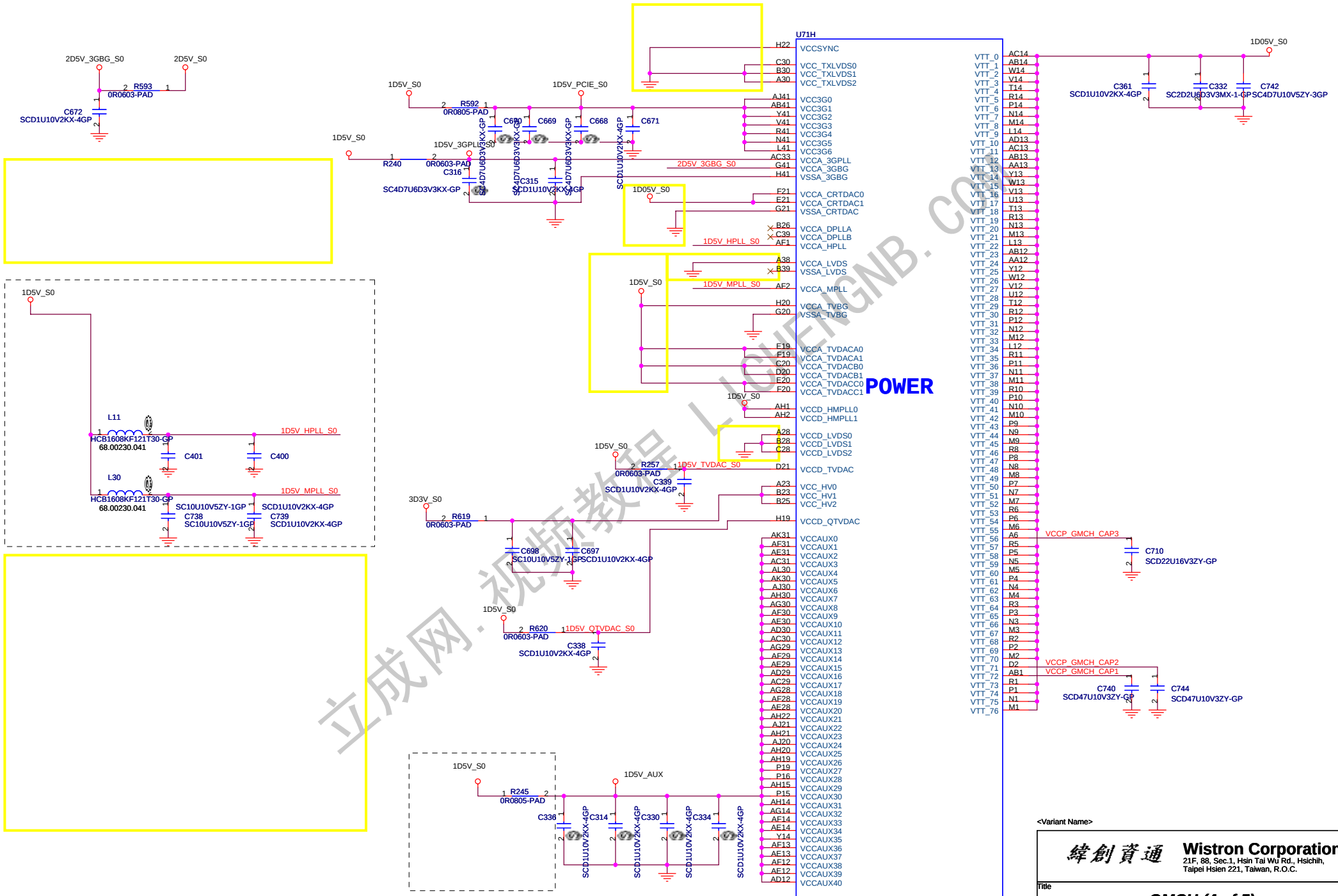
Title: GMCH (3 of 5)

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 8 of 52



<Variant Name>

緯創資通 Wistron Corporation
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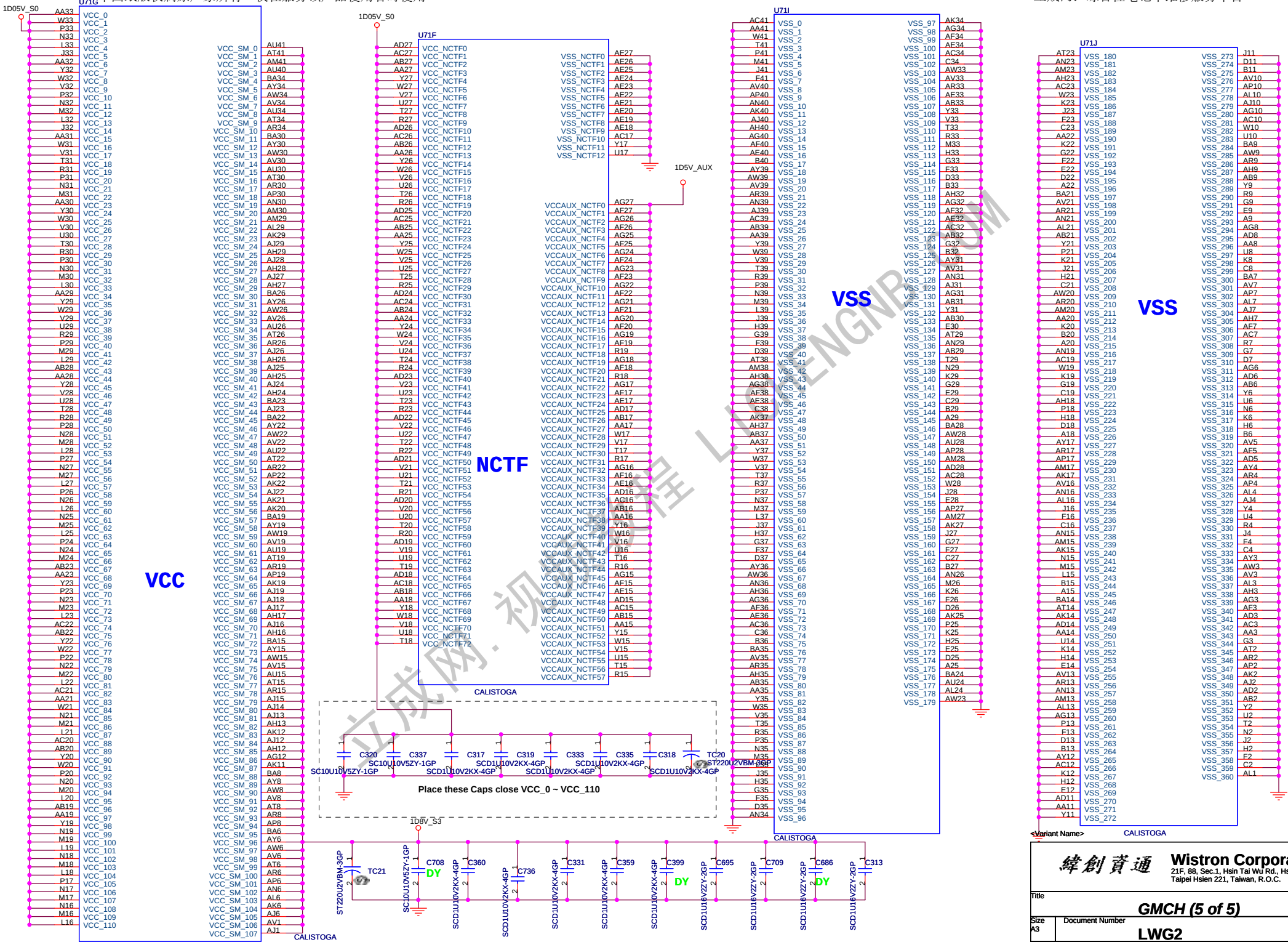
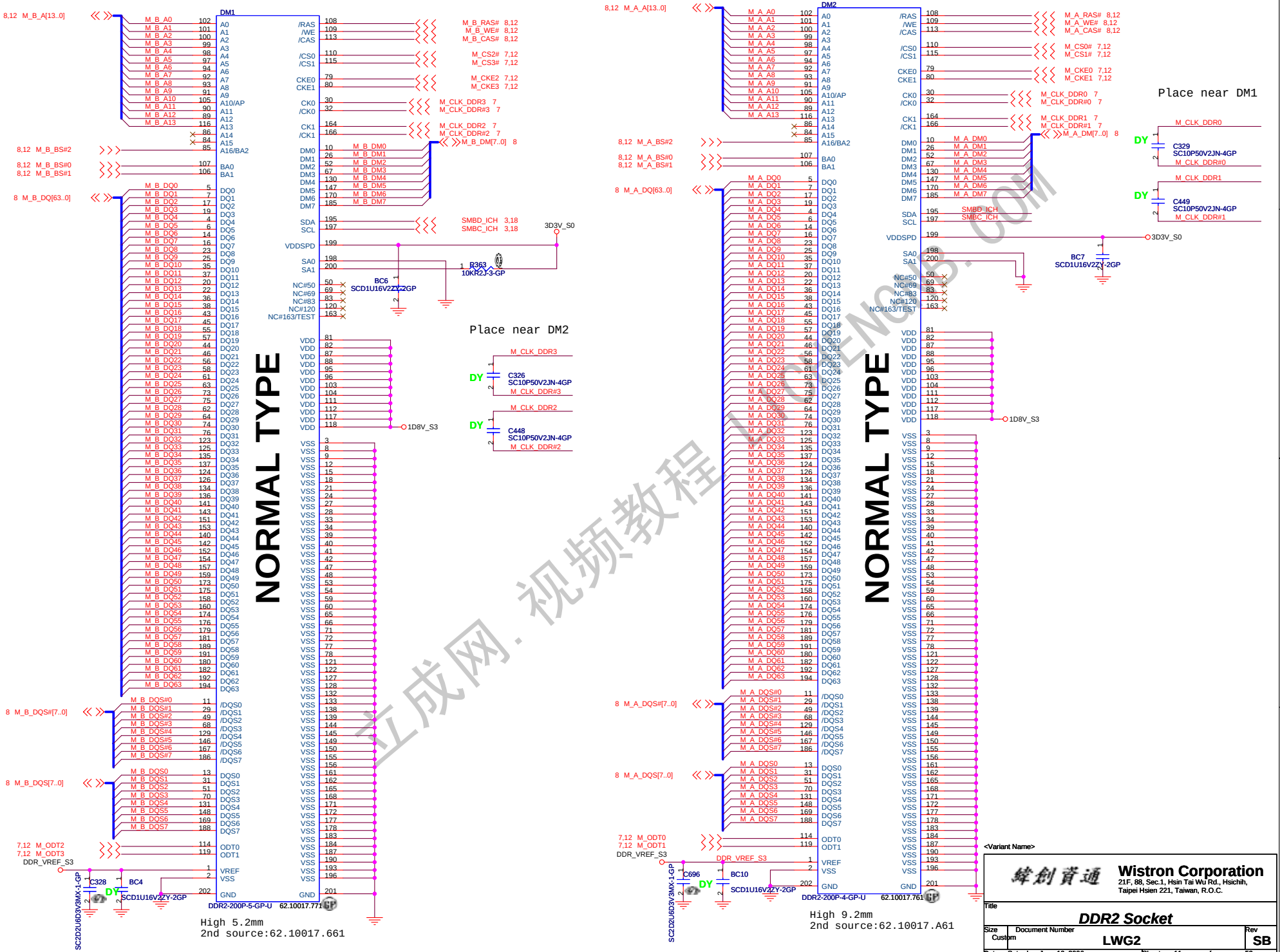
Title: GMCH (4 of 5)

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 9 of 52



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GMCH (5 of 5)	
Size A3	Document Number LWG2	Rev SA
Date: Saturday, June 10, 2006	Sheet 10 of 52	



<Variant Name>

蜂创資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Socket

Size: Custom | Document Number: LWG2 | Rev: SB

Date: Saturday, June 10, 2006 | Sheet 11 of 52

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN55 SRN56J-5-GP
M_CKE2 7,11
M_B_BS#2 8,11
M_B_A12
M_B_A9
M_A_A[13..0] 8,11
M_B_A[13..0] 8,11

R314 56R2J-4-GP
R312 56R2J-4-GP M_A_A9
R315 56R2J-4-GP M_B_A8
R313 56R2J-4-GP
M_ODT1 7,11
M_ODT3 7,11

RN62 SRN56J-5-GP
M_B_A5
M_B_A3
M_B_A1
M_B_A10

RN60 SRN56J-5-GP
M_B_A13
M_ODT2 7,11
M_CS2# 7,11
M_B_RAS# 8,11

RN59 SRN56J-5-GP
M_B_BS#1 8,11
M_B_A0
M_B_A2
M_B_A4

RN54 SRN56J-5-GP
M_B_A6
M_B_A7
M_B_A11
M_CKE3 7,11

RN61 SRN56J-5-GP
M_B_BS#0 8,11
M_B_WE# 8,11
M_CS3# 7,11
M_B_CAS# 8,11

RN63 SRN56J-5-GP
M_A_A13
M_ODT0 7,11
M_CS0# 7,11
M_A_RAS# 8,11

RN65 SRN56J-5-GP
M_A_BS#1 8,11
M_A_A0
M_A_A2
M_A_A4

RN66 SRN56J-5-GP
M_A_BS#0 8,11
M_A_WE# 8,11
M_A_CAS# 8,11
M_CS1# 7,11

RN56 SRN56J-5-GP
M_CKE0 7,11
M_A_BS#2 8,11
M_A_A12
M_A_A8

RN64 SRN56J-5-GP
M_A_A6
M_A_A7
M_A_A11
M_CKE1 7,11

RN67 SRN56J-5-GP
M_A_A5
M_A_A3
M_A_A1
M_A_A10

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C435 C419 C413 C387 C386 C411 C384 C412 C438 C385 C391
C418 C396 C415 C434 C436 C398 C397 C409 C408 C407 C437
SCD1U16V2ZY-2GP
DY

1D8V_S3

Place these Caps near DM1

C734 C735 C394 C395 C417
C389 C414 C388 C410
SC2D2U6D3V3MX-1-GP
SCD1U16V2ZY-2GP
DY

1D8V_S3

Place these Caps near DM2

C733 C392 C390 C759 C761
C382 C383 C416 C393
SC2D2U6D3V3MX-1-GP
SCD1U16V2ZY-2GP
DY

<Variant Name>

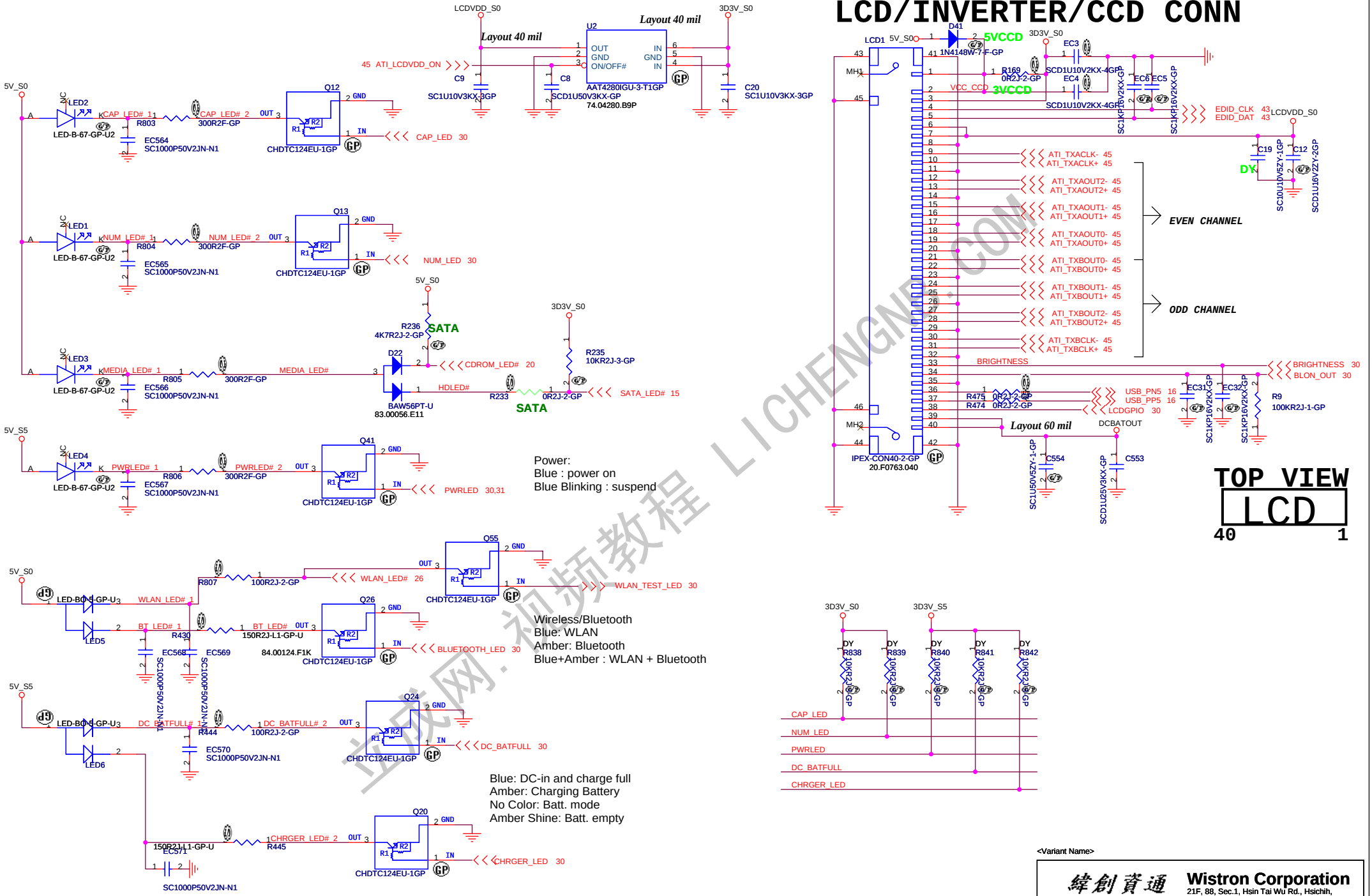
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Termination Resistor

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 12 of 52

LCD/INVERTER/CCD CONN



Front panel

LED left side Right side

Power Battery Wireless Num Caps HDD

<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LAUNCH / LEDs**

Size	Document Number	Rev
Custom	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 13 of 52

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 47 ohm@100MHz

SB change

43 ATI_RED
43 ATI_GREEN
43 ATI_BLUE

L17 BLM18BB470SN1-GP → CRT_R
L18 BLM18BB470SN1-GP → CRT_G
L19 BLM18BB470SN1-GP → CRT_B

R456 150R2F-1-GP
R457 150R2F-1-GP
R458 150R2F-1-GP
C541 SC3P50V2CN-1-GP
C543 SC3P50V2CN-1-GP
C545 SC3P50V2CN-1-GP

C542 SC6D8P50V2DN-GP
C544 SC6D8P50V2DN-GP
C546 SC6D8P50V2DN-GP

-1 for CRT SIV Fail

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V_S0
D2 CH751H-40PT
RN3 SRN10KJ-5-GP
C2 SCD01U16V2KX-3GP
5V_CRT_S0

CRT1 VIDEO-15-42-GP-U 20.20378.015

DAT_DDC1_5
JVGA_HS
JVGA_VS
CLK_DDC1_5

C4 SC100P50V2JN-3GP
C6 SC18P50V2JN-1-GP
C7 SC100P50V2JN-3GP
C5 SC18P50V2JN-1-GP

-1 for CRT SIV Fail

Hsync & Vsync level shift

5V_S0
C539 SCD1U16V2ZY-2GP
U59A TSAHCT125PW-GP
U59B TSAHCT125PW-GP

43 ATI_HSY → R451 47R2J-2-GP → HSYNC_4 → JVGA_HS
43 ATI_VSY → R449 47R2J-2-GP → VSYNC_4 → JVGA_VS

For System CRT

DDC_CLK & DATA level shift

3D3V_S0
RN4 SRN2K2J-1-GP

43 ATI_DDCDAT → DAT_DDC1_5
43 ATI_DDCCLK → CLK_DDC1_5

Q3 2N7002-7F-GP
Q4 2N7002-7F-GP

TV OUT CONN

43 ATI_TV_CRMA → CRMA_1
43 ATI_TV_LUMA → LUMA_1
43 ATI_TV_COMP → COMP_1

L26 IND-1D2UH-5-GP
L24 IND-1D2UH-5-GP
L25 IND-1D2UH-5-GP

R621 150R2F-1-GP
R617 150R2F-1-GP
R616 150R2F-1-GP

C705 SC33P50V3JN-GP
C704 SC150P-GP
C706 SC270P50V2JN-2GP
C690 SC33P50V3JN-GP
C689 SC150P-GP
C693 SC270P50V2JN-2GP
C691 SC33P50V3JN-GP
C688 SC150P-GP
C692 SC270P50V2JN-2GP

TVOUT1 MINDIN7-11-U2-GP 22.10021.D81

Reverse type

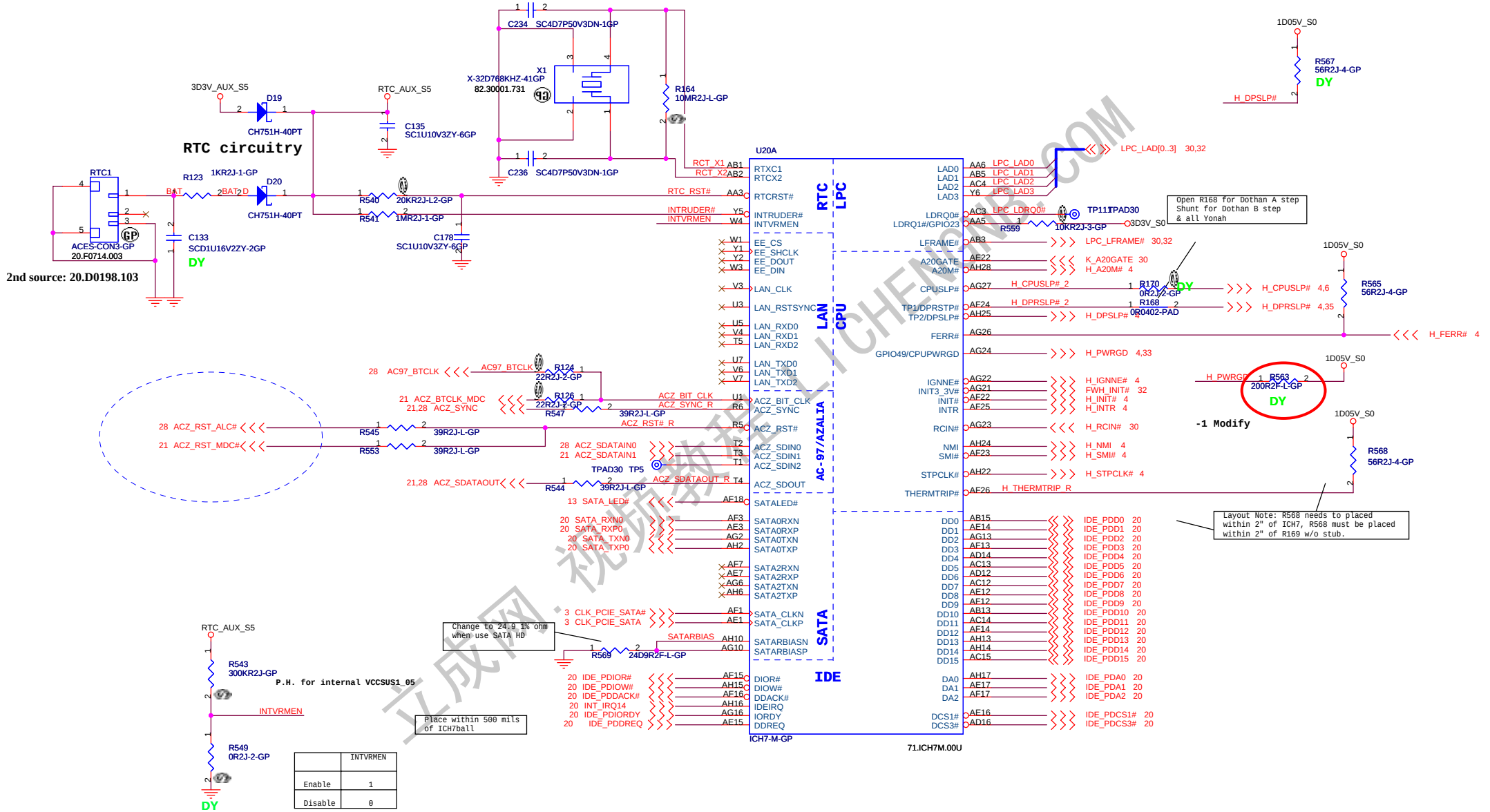
5V_S0
LUMA_1 → D23 BAV99PT-GP-U
CRMA_1 → D25 BAV99PT-GP-U
COMP_1 → D24 BAV99PT-GP-U

5V_S0
CRT_R → D32 BAV99PT-GP-U
CRT_G → D33 BAV99PT-GP-U
CRT_B → D34 BAV99PT-GP-U

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Saturday, June 10, 2006 | Sheet 14 of 52

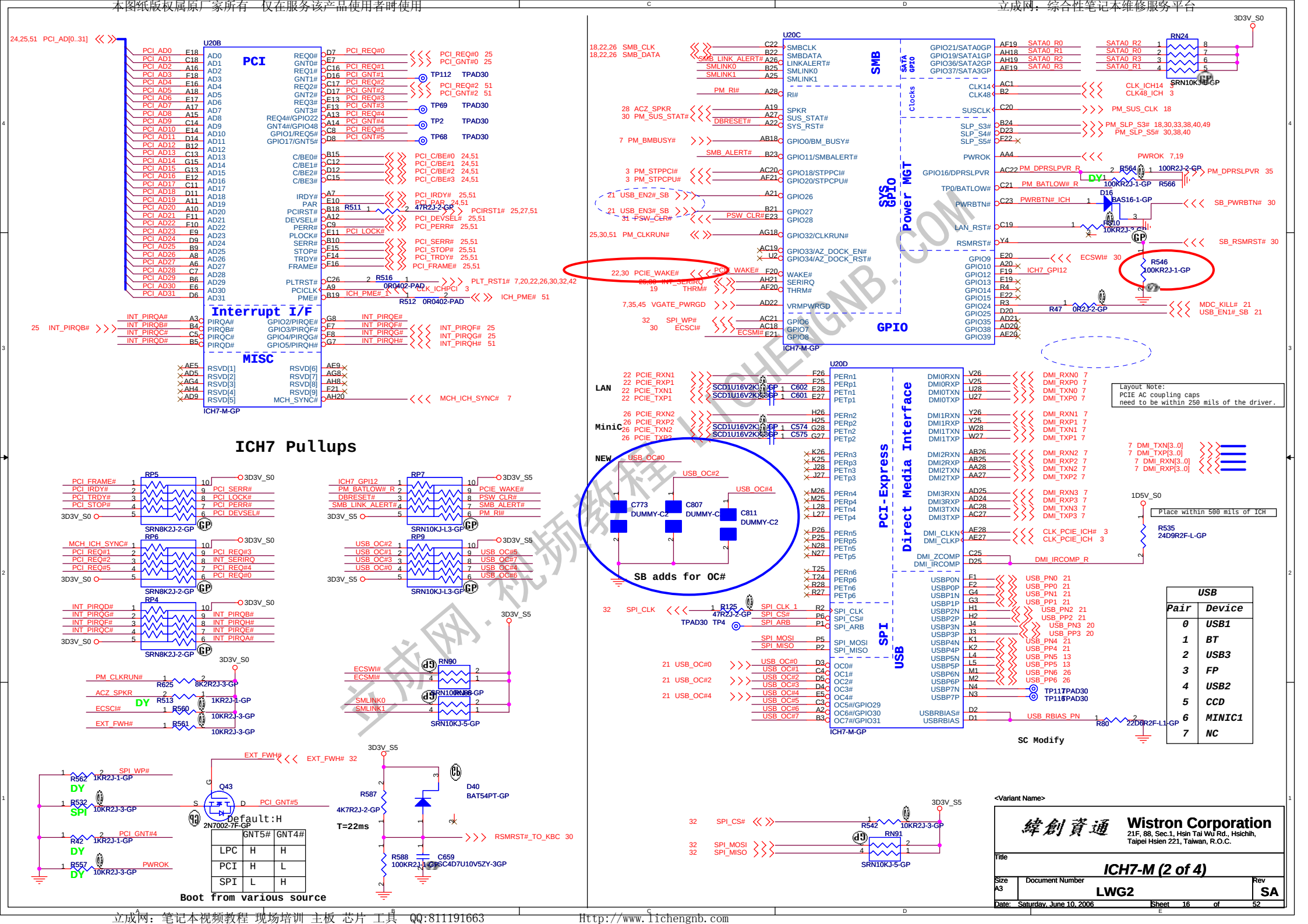


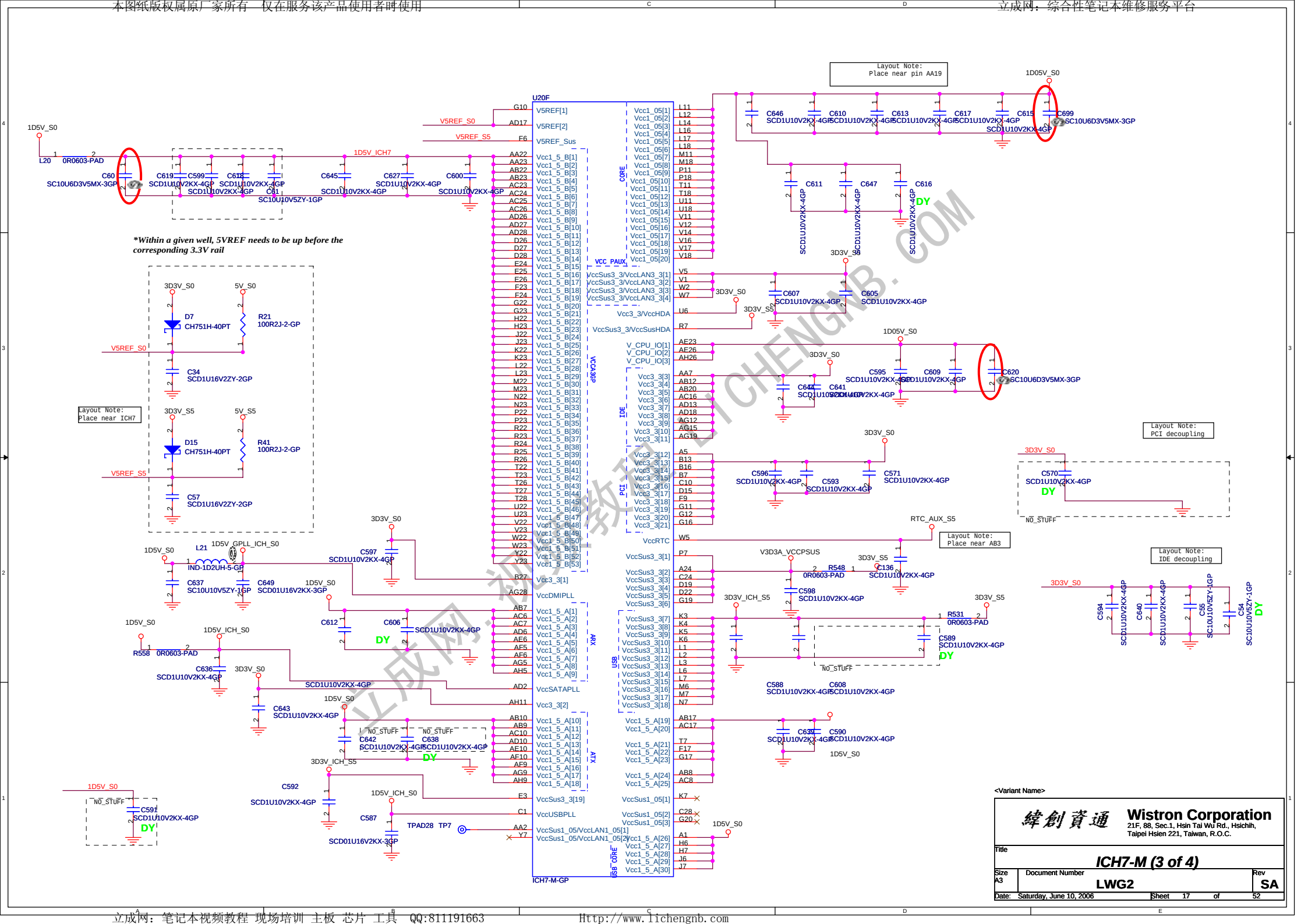
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M (1 of 4)

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Wednesday, June 21, 2006 | Sheet 15 of 52





U20E

A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB11
J5	VSS[49]	VSS[146]	AB14
J24	VSS[50]	VSS[147]	AB16
J25	VSS[51]	VSS[148]	AB19
J26	VSS[52]	VSS[149]	AB21
K24	VSS[53]	VSS[150]	AB24
K27	VSS[54]	VSS[151]	AB27
K28	VSS[55]	VSS[152]	AB28
L13	VSS[56]	VSS[153]	AC2
L15	VSS[57]	VSS[154]	AC5
L24	VSS[58]	VSS[155]	AC9
L25	VSS[59]	VSS[156]	AC11
L26	VSS[60]	VSS[157]	AD1
M3	VSS[61]	VSS[158]	AD3
M4	VSS[62]	VSS[159]	AD4
M5	VSS[63]	VSS[160]	AD7
M12	VSS[64]	VSS[161]	AD8
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD15
M15	VSS[67]	VSS[164]	AD19
M16	VSS[68]	VSS[165]	AD23
M17	VSS[69]	VSS[166]	AE2
M24	VSS[70]	VSS[167]	AE4
M27	VSS[71]	VSS[168]	AE8
M28	VSS[72]	VSS[169]	AE11
N1	VSS[73]	VSS[170]	AE13
N2	VSS[74]	VSS[171]	AE18
N5	VSS[75]	VSS[172]	AE21
N6	VSS[76]	VSS[173]	AE24
N11	VSS[77]	VSS[174]	AE25
N12	VSS[78]	VSS[175]	AF2
N13	VSS[79]	VSS[176]	AF4
N14	VSS[80]	VSS[177]	AF8
N15	VSS[81]	VSS[178]	AF11
N16	VSS[82]	VSS[179]	AF27
N17	VSS[83]	VSS[180]	AF28
N18	VSS[84]	VSS[181]	AG1
N24	VSS[85]	VSS[182]	AG3
N25	VSS[86]	VSS[183]	AG7
N26	VSS[87]	VSS[184]	AG11
P3	VSS[88]	VSS[185]	AG14
P4	VSS[89]	VSS[186]	AG17
P12	VSS[90]	VSS[187]	AG20
P13	VSS[91]	VSS[188]	AG25
P14	VSS[92]	VSS[189]	AH1
P15	VSS[93]	VSS[190]	AH3
P16	VSS[94]	VSS[191]	AH7
P17	VSS[95]	VSS[192]	AH12
P24	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27

ICH7-M-GP

32K suspend clock output

3D3V_S5

U11

16,30,33,38,40,49 PM_SLP_S3#
16 PM_SUS_CLK

OE, A, GND, VCC, Y

NC7SZ126P5X-GP

73.7S126.AAH

32KHZ

R44 100R2J-2-GP

G792_32K 19

R43 240KR3-GP

63.24434.15L

SMBUS

5V_S0

3D3V_S0

3D3V_S5

RN10 SRN4K7J-8-GP

RN9 SRN4K7J-8-GP

Q37 2N7002-7F-GP

16,22,26 SMB_CLK

16,22,26 SMB_DATA

SMBC_ICH 3,11

SMBD_ICH 3,11

SB Mirror

Q36 2N7002-7F-GP

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

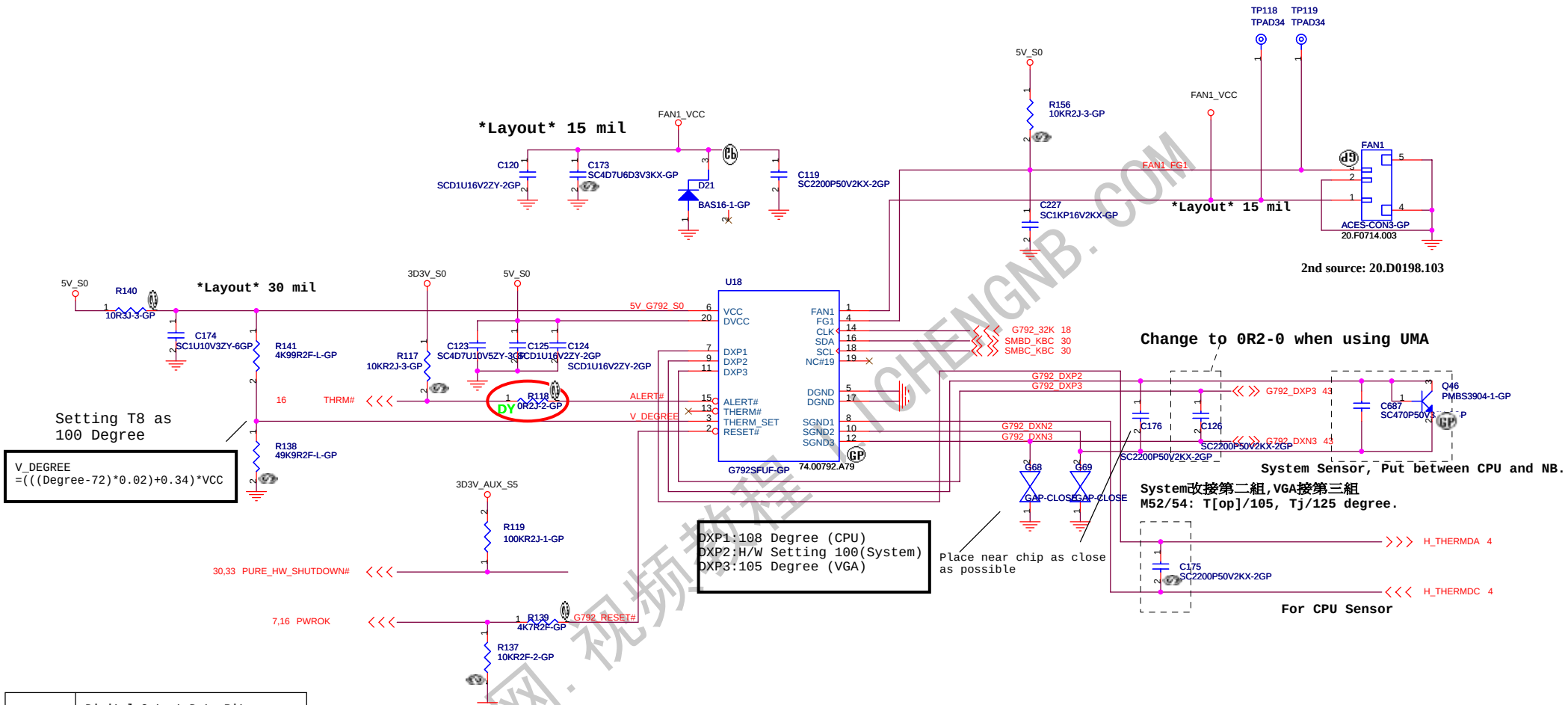
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (4 of 4)**

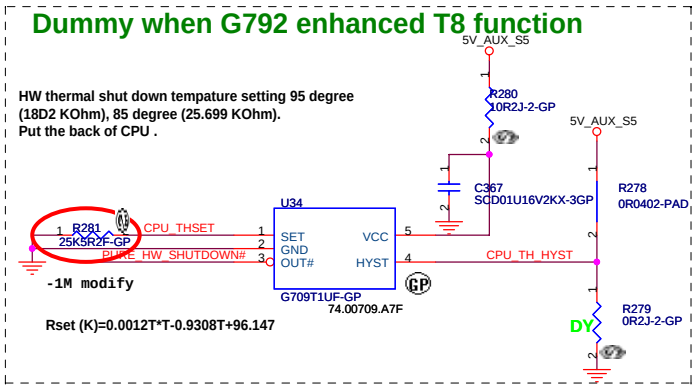
Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 18 of 52



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Dummy when G792 enhanced T8 function



Thermal Get Setting

		T6	T7
Sencor 0	CPU DTS	98	100
Sencor 1	G792-1 CPU	98	100
Sencor 2	G792-2 System	78	83
Sencor 3	G792-3 VGA	110	115

<Variant Name>

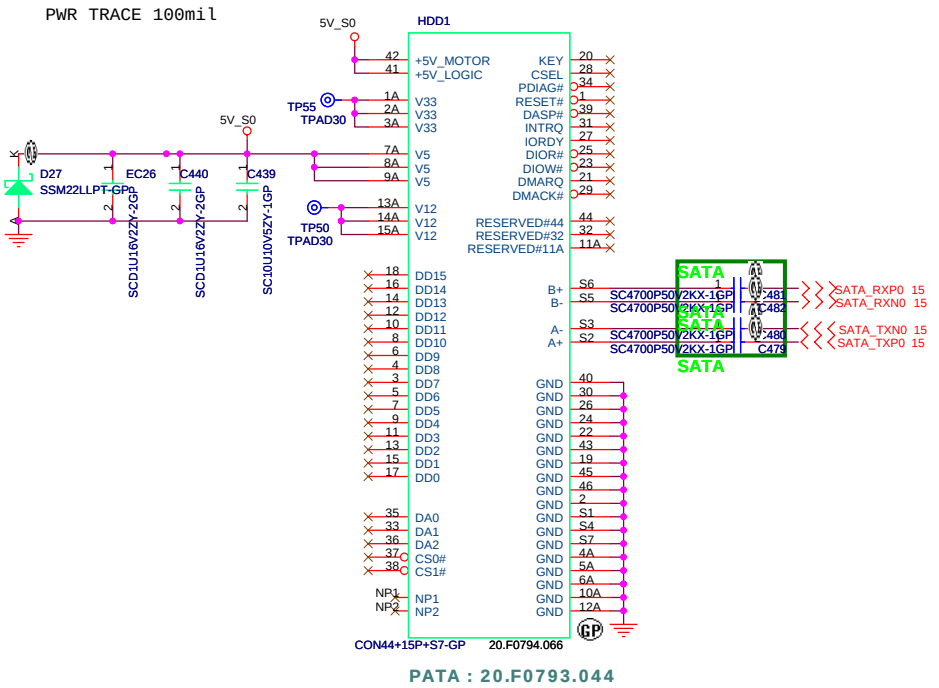
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

Size: Custom | Document Number: LWG2 | Rev: SA

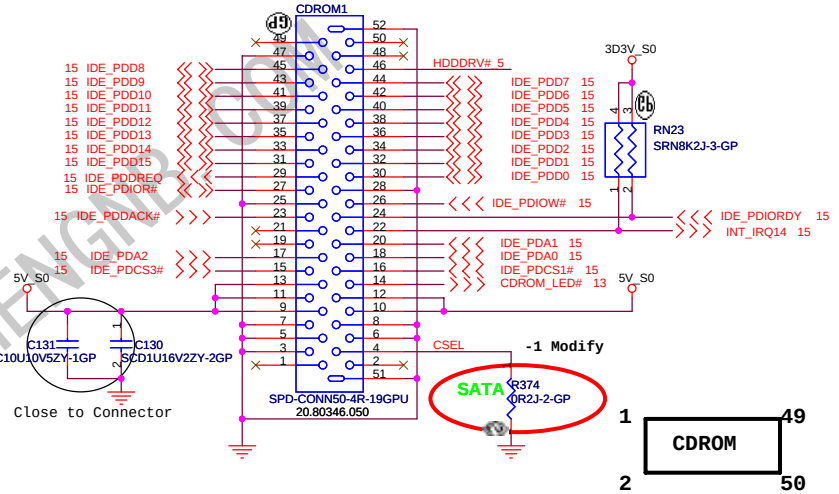
Date: Saturday, June 10, 2006 | Sheet 19 of 52

SATA Connector

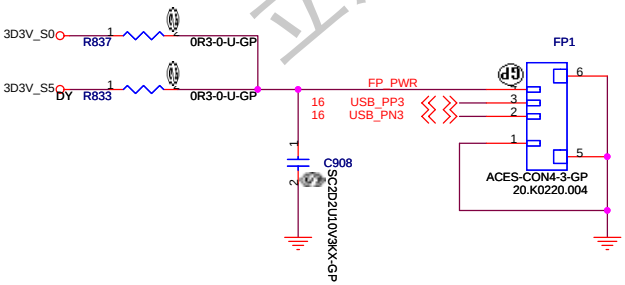


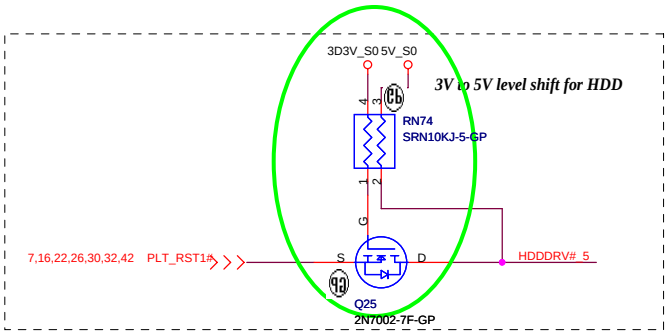
PATA : 20.F0793.044

CDROM Connector



Finger Print





EC: N060446

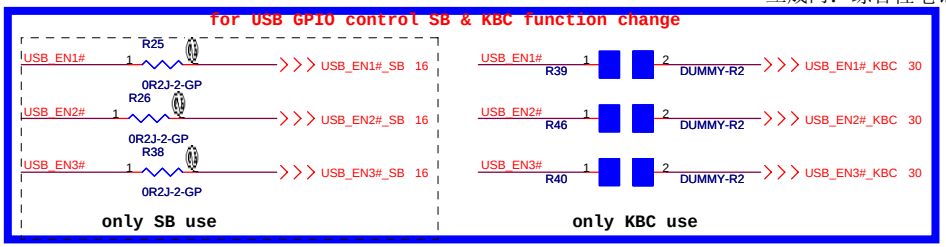
<Variant Name>

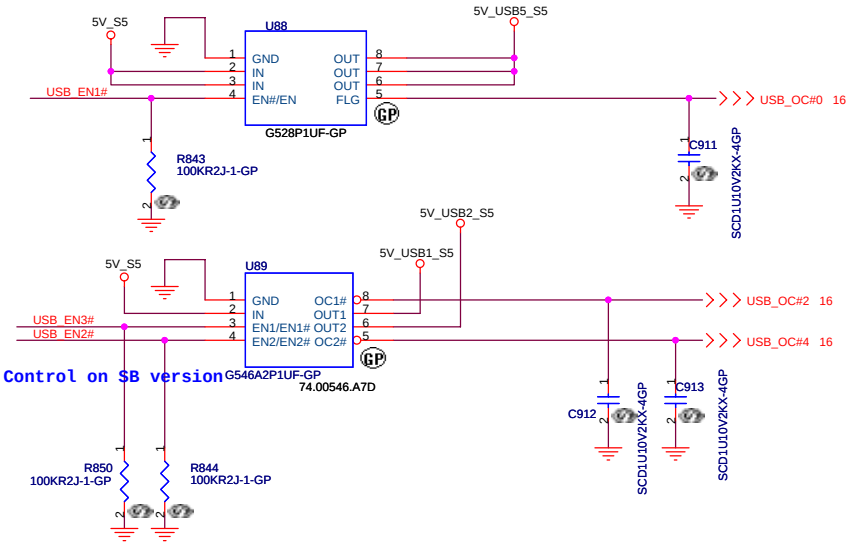
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

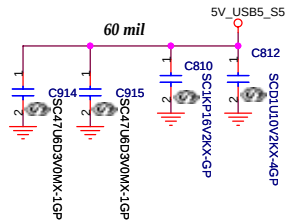
Title: SATA HDD / ODD /FINGER PRINT

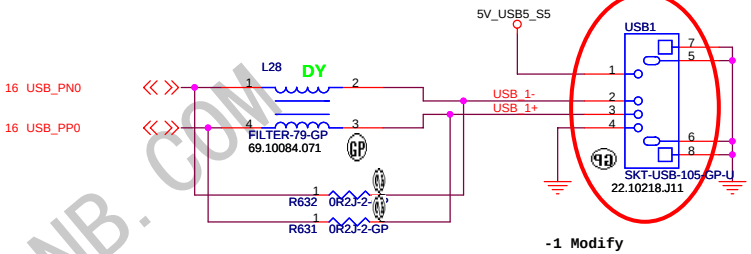
Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 20 of 52

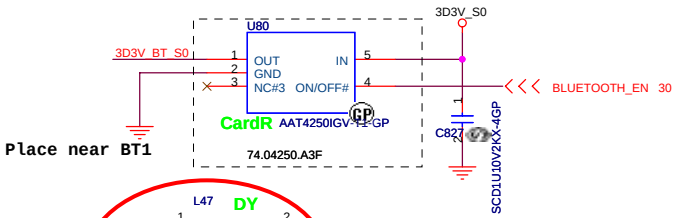


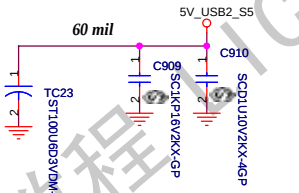


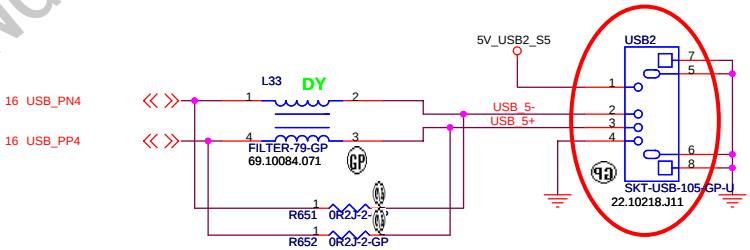


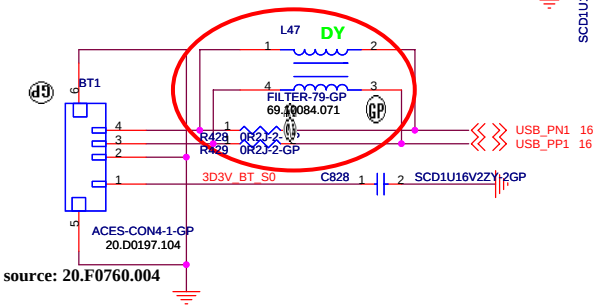


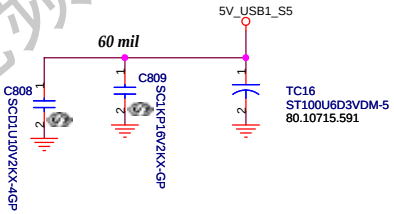
BLUETOOTH MODULE CONNECTOR

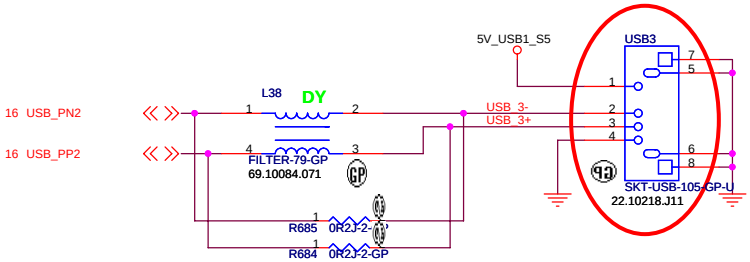






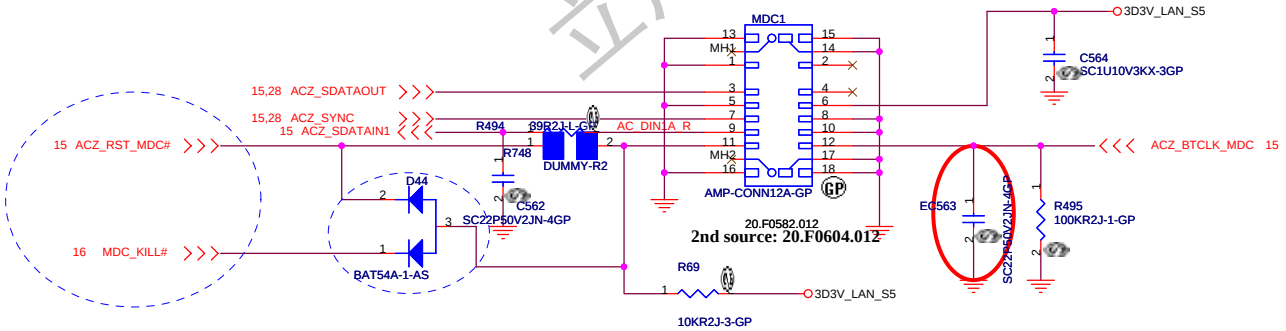






MDC 1.5 CONN

USB PORT



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC I/F

Size	Document Number	Rev
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Date: Saturday, June 10, 2006 Sheet 21 of 52

BCM5789
BCM5787M

CLOSE TO GPHY PINS

Place PLLVDD/AVDDL CKT as close to chip as possible

"GIGA" -- stuff when 5789 or 5787M.
"5789" -- stuff when 5789.
"5787" -- stuff when 5787.

-2 modify

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM5787M / BCM5789

Size: A3 | Document Number: LWG2 | Rev: SA

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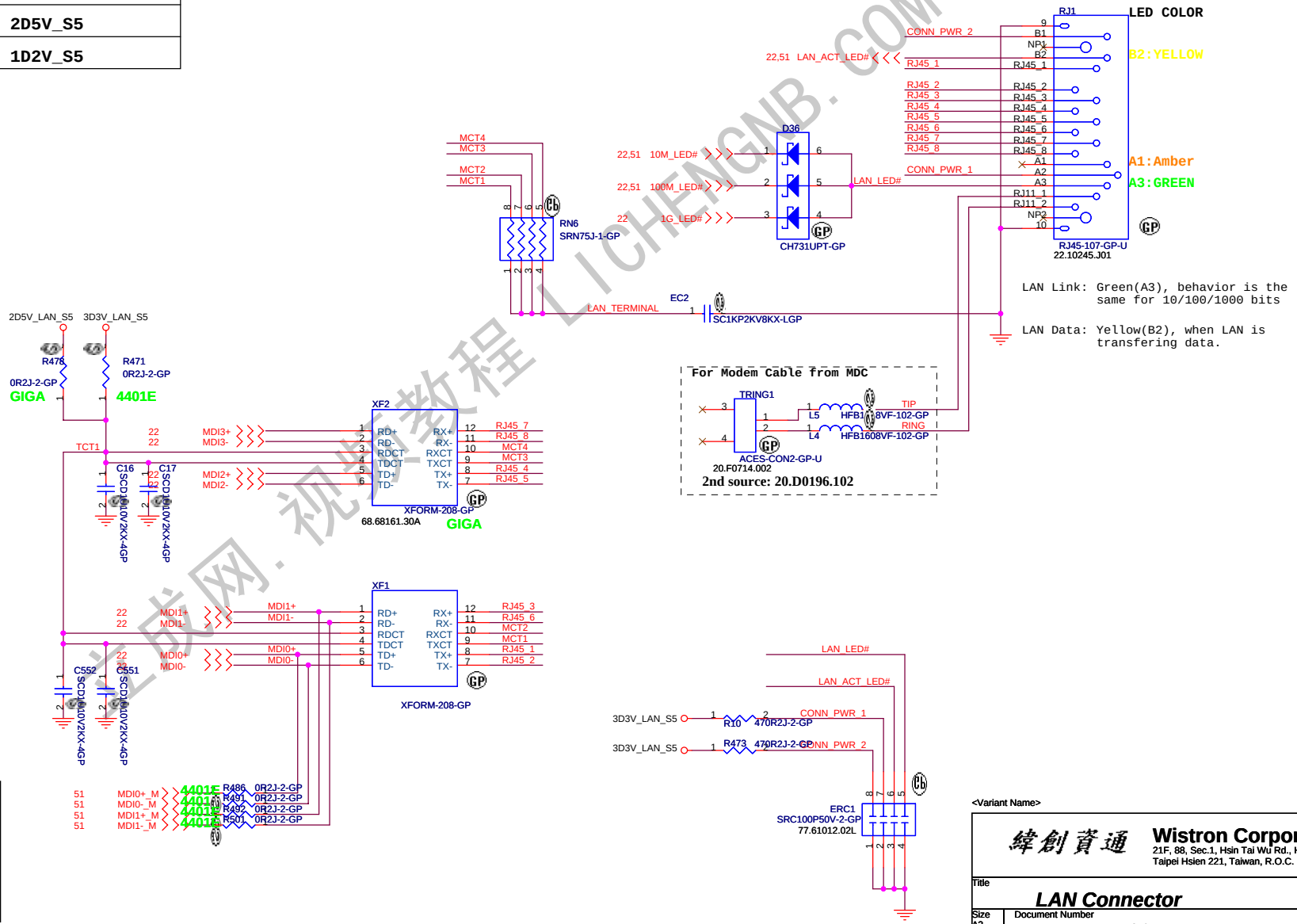
LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

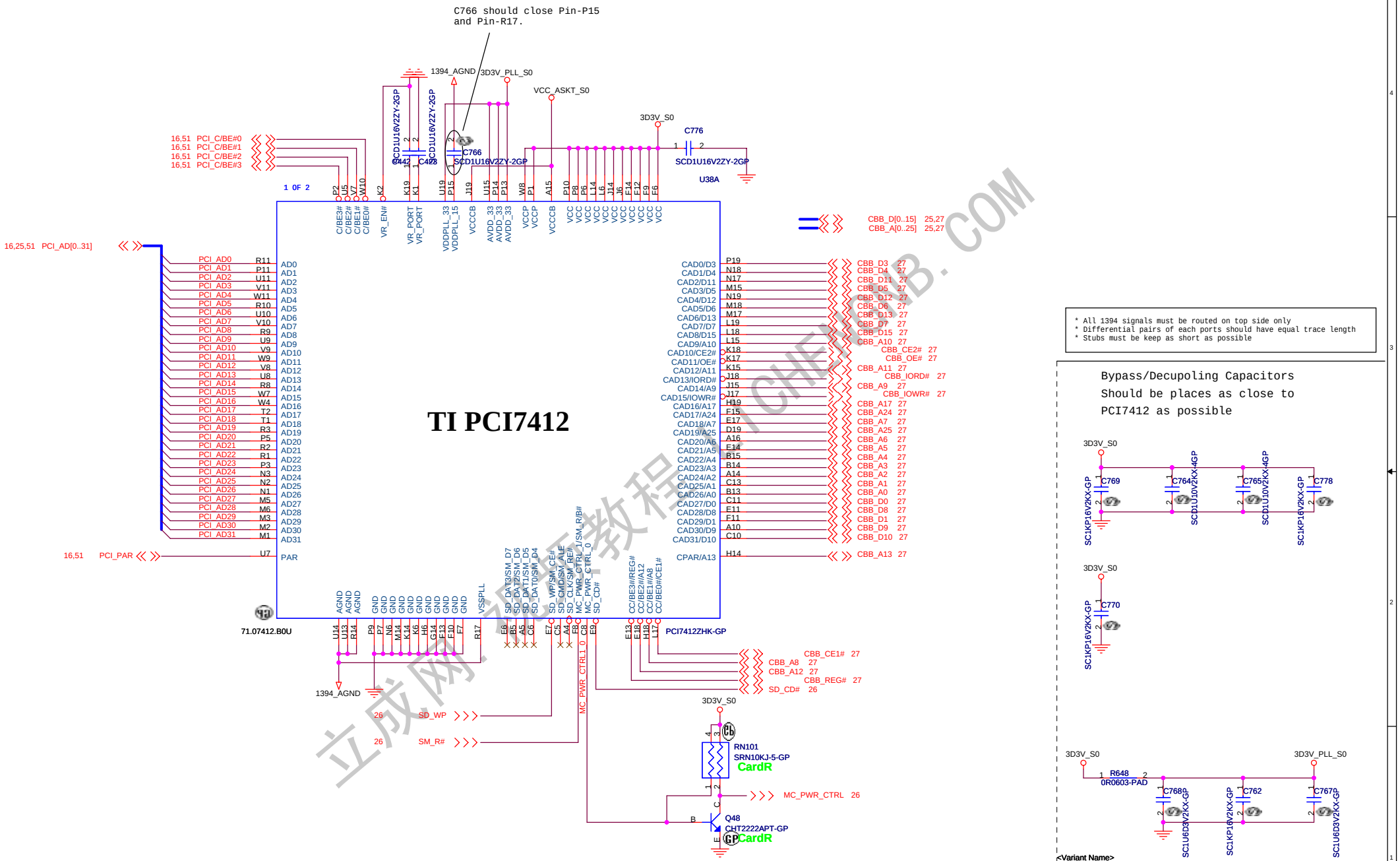
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Monday, June 12, 2006 | Sheet 23 of 52

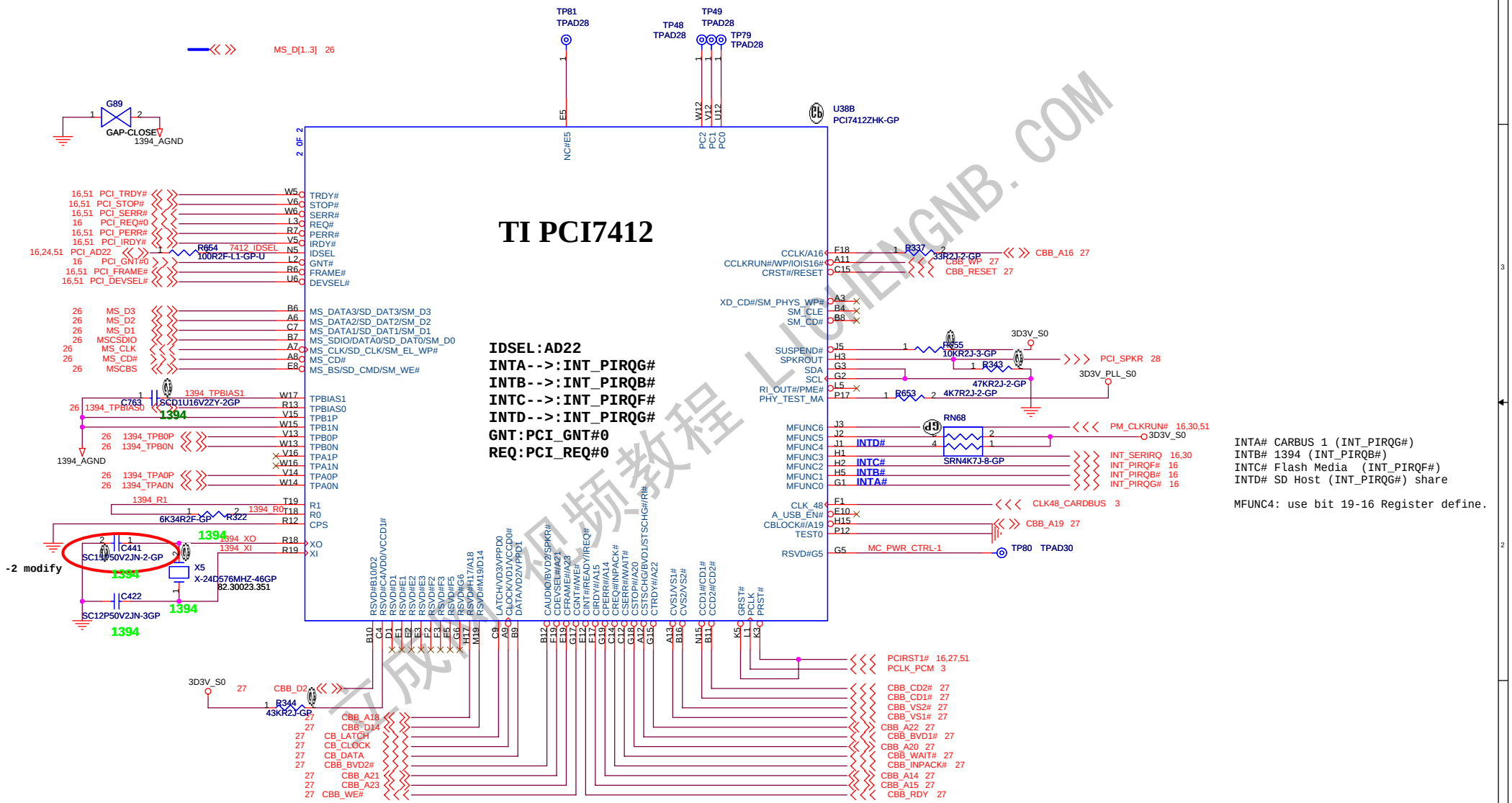


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TI PCI7412 (1 of 2)*

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 24 of 52

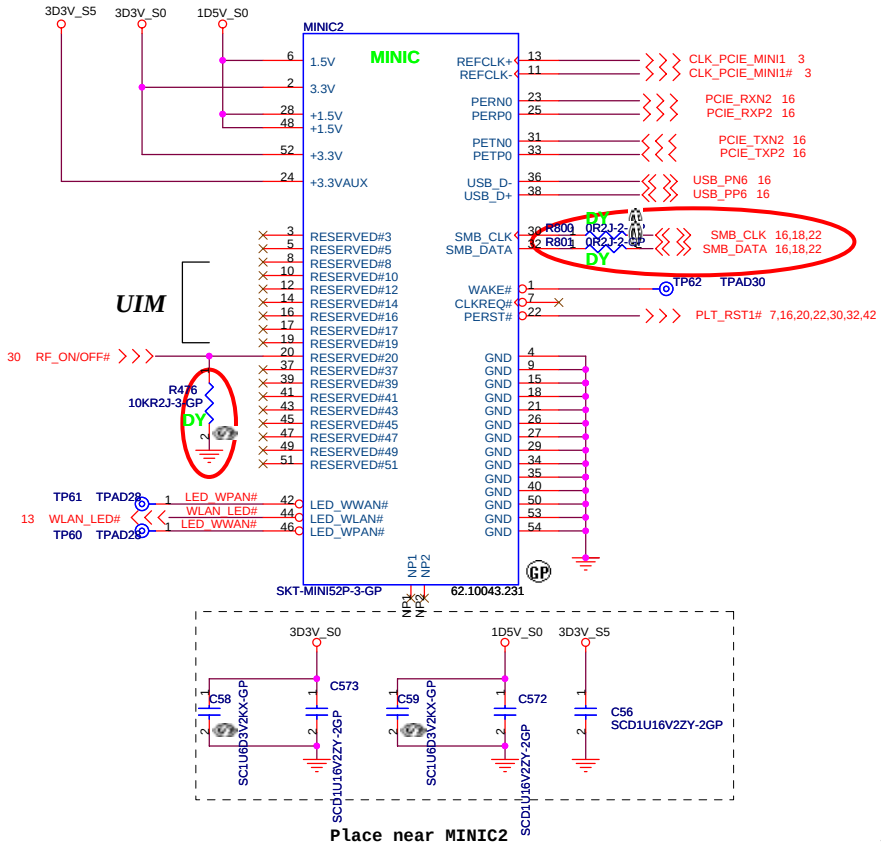


<Variant Name>

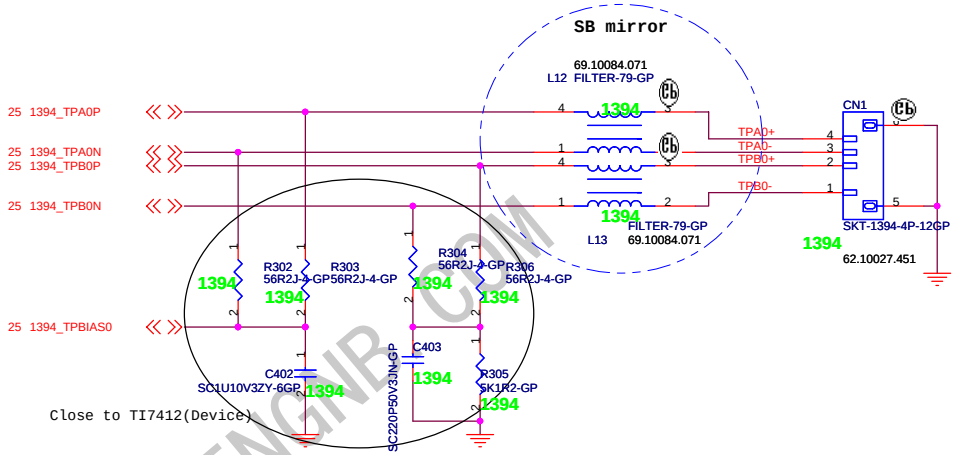
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

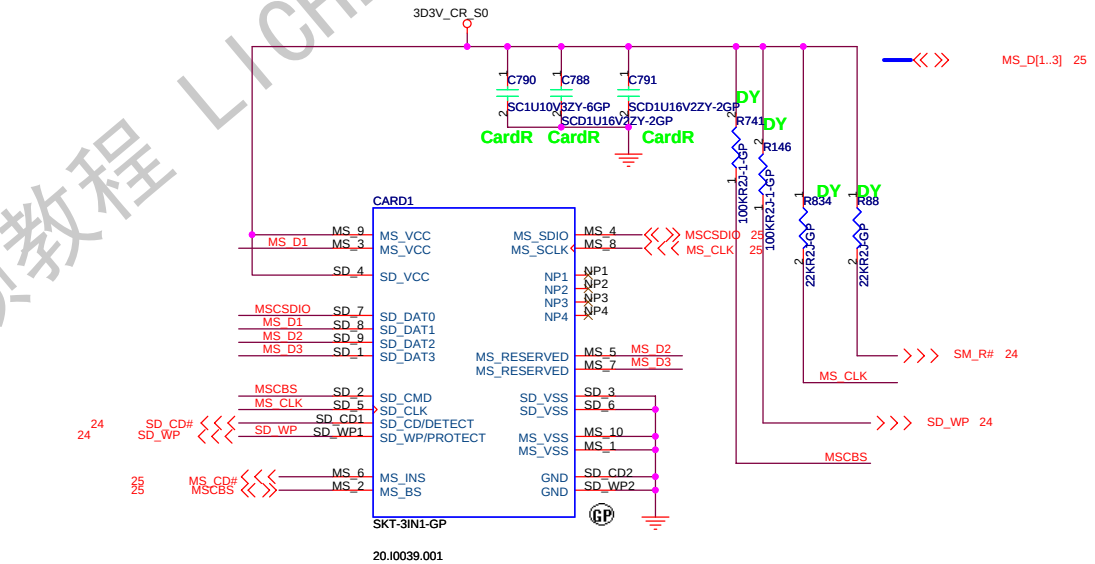
Title: TI PCI7412 (2 of 2)
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Saturday, June 10, 2006 | Sheet 25 of 52

Mini Card Connector



1394 Connector

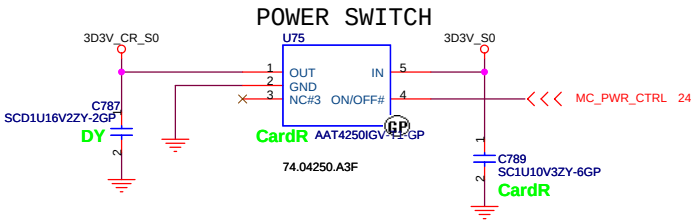




Bottom VIEW

1 36

Reader



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / 1394

Size	Document Number	Rev
A3	LWG2	SA

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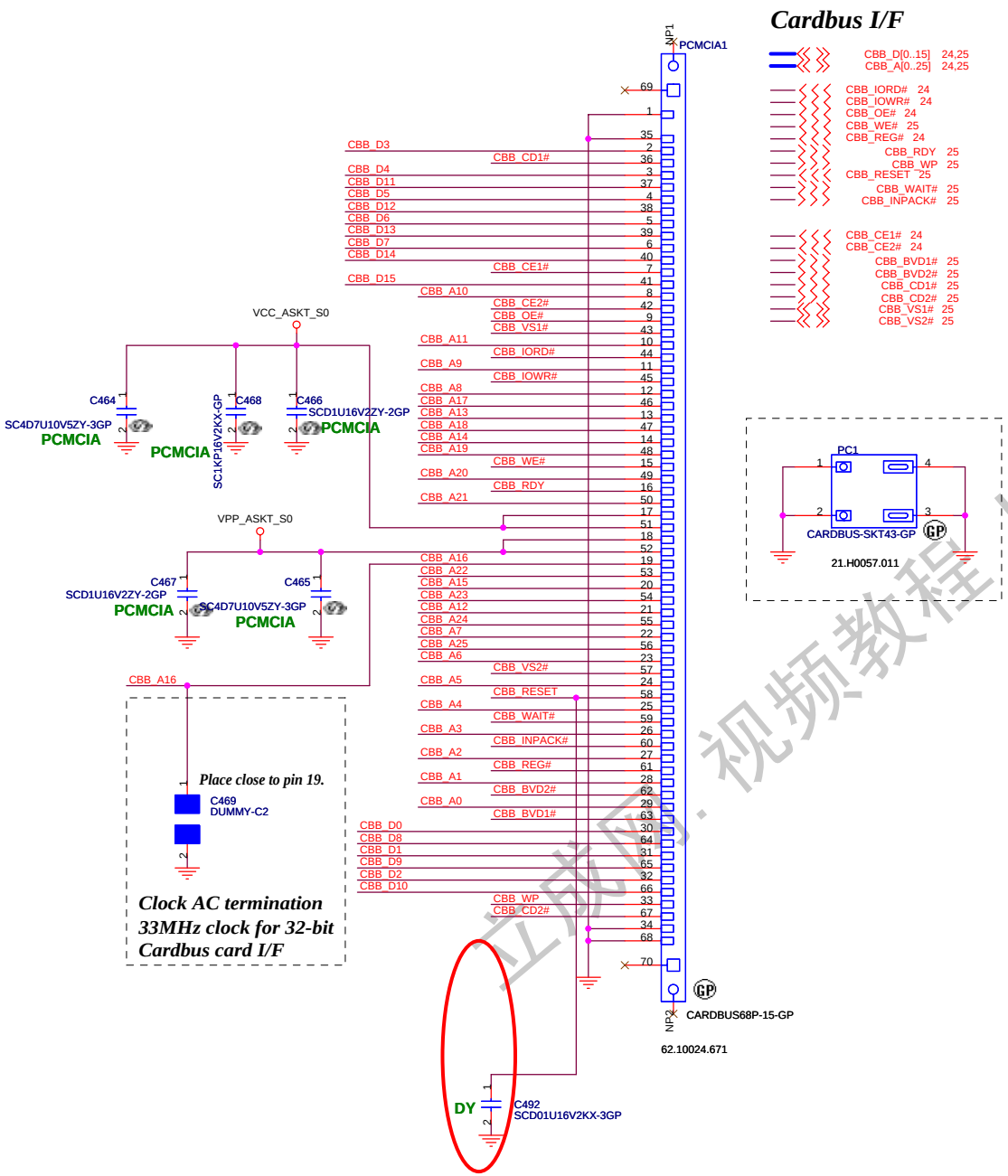
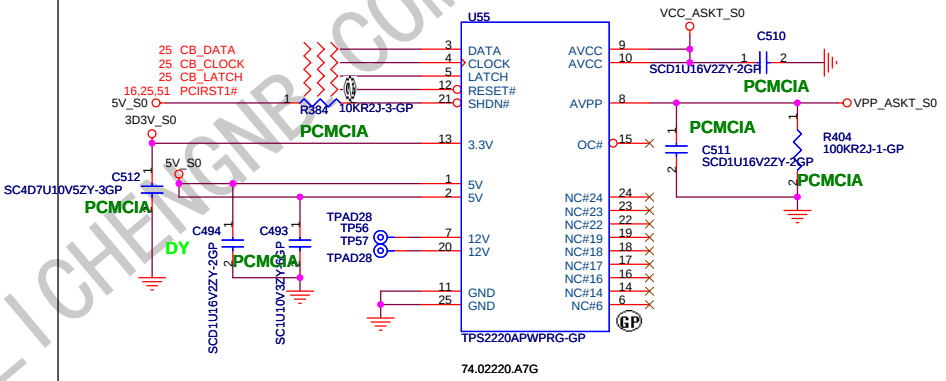
PCMCIA Socket



Cardbus I/F

Power switch



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA		
Size: A3	Document Number: LWG2	Rev: SA
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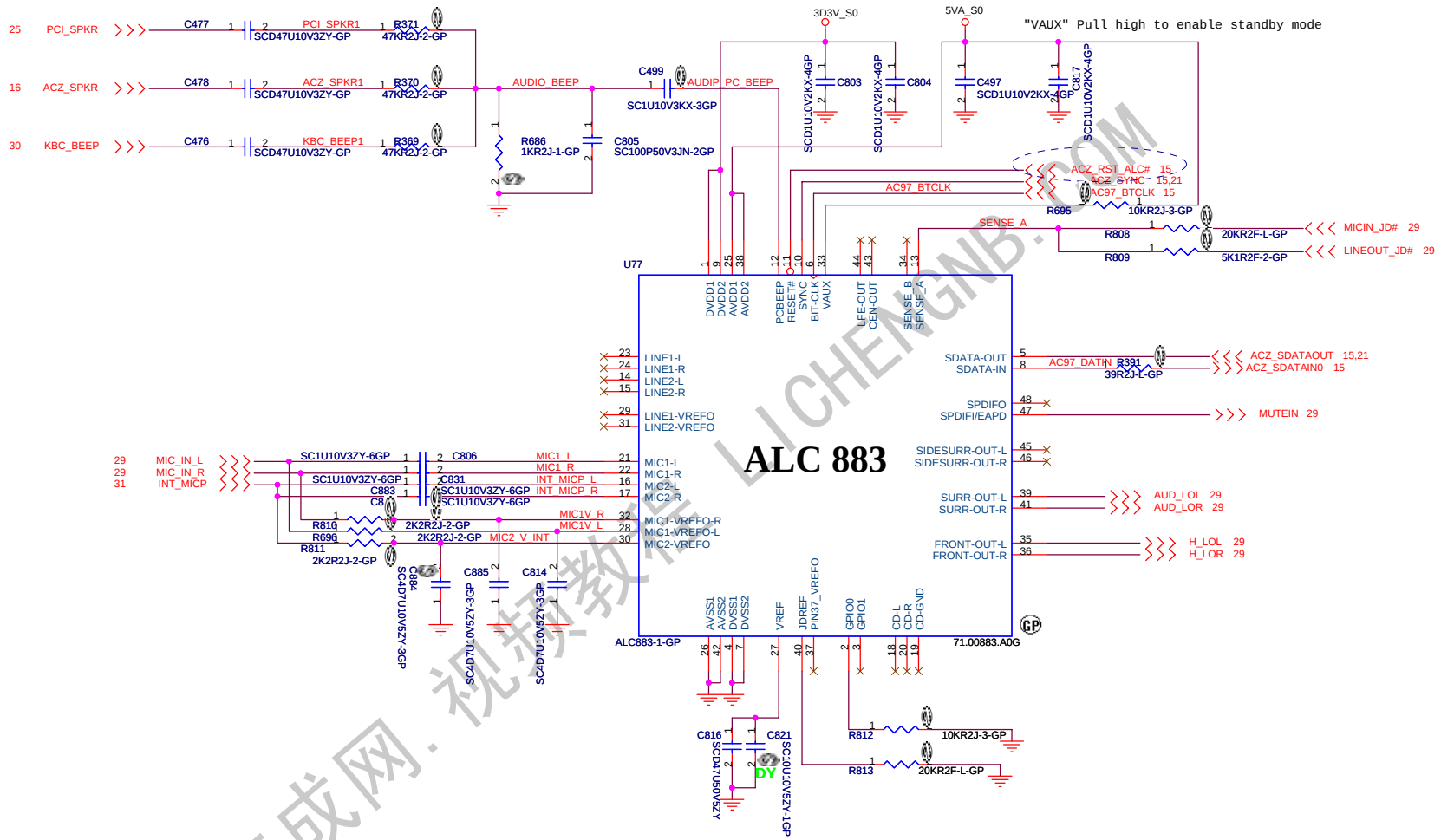


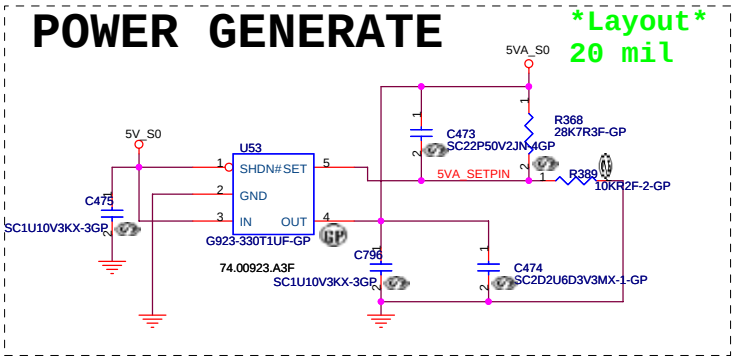
1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	*Symbol*	*Location*	*Re-tasking*
35/36	*FRONT*	*AMP,Jack1*	AMP output, line input
39/41	*SURR*	*X*	X
43/44	*CEN/LEFT*	*X*	SURR-VREFO-L/R
45/46	*SIDESURR*	*X*	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	*LINE1*	*Jack 2*	Line input, line output
21/22	*MIC1*	*Jack 3*	Mic input, line output
14/15	*LINE2*	*X*	X
16/17	*MIC2*	*Int. Mic*	Mic input

POWER GENERATE

Layout 20 mil



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC883***

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 28 of 52

AUDIO OP AMPLIFIER

I/P signal level need +5V level

5V_S0 R814 0R0603-PAD 5V_OP_S0

C503 SC1U10V5ZY-1GP, C528 SCD1U16V2ZY-2GP, C527 SCD1U16V2ZY-2GP, C886 SC1U10V5ZY-1GP DY

TP109 TPAD28

AMP_SHUTDOWN 30 → R815 10KR2J-3-GP

U85 G1432Q5U-GP

C887 SC1U10V3ZY-6GP

28 AUD_LOL → SOUND_L2 → R819 12KR2J-L-GP → SOUND_L_OP1 → R820 10KR2J-3-GP

SOUND_L_OP1 → DY C889 SC1U10V3ZY-6GP

SPKR_L+ SPKR_L-

LIN1 LIN2 LOUT+ LOUT- NC#6 NC#8 NC#23 VOL LVDD RVDD SHUTDOWN IN1#/IN2 RIN1 RIN2 ROUT+ ROUT- LBYPASS RBYPASS MUTE GND/HS GND GND

SPKR_R+ SPKR_R- → SOUND_R_OP1 → R821 → SOUND_R2 → 12KR2J-L-GP → C888 SC1U10V3ZY-6GP → AUD_LOR 28

SOUND_R_OP1 → R822 10KR2J-3-GP → DY C890 SC1U10V3ZY-6GP

C891 SC2D2U16V5ZY-2GP, C892 SC2D2U16V5ZY-2GP

28 MUTEIN → R823 DY 0R2J-2-GP → G1432_MUTE → R824 10KR2J-3-GP

28 H_LOL, 28 H_LOR → C895 SC1U10V3ZY-6GP, C894 SC1U10V3ZY-6GP → LINE_L1 R845 10KR2J-3-GP, LINE_R1 R846 10KR2J-3-GP

AMP_C1N C893 SC1U10V3KX-3GP AMP_C1P

LINE_L1_2 LINE_R1_2

R847 1KR2J-GP, R848 1KR2J-GP

C896 SC47P50V2JN-3GP, C897 SC47P50V2JN-3GP

U86 MAX4411ETP-1-GP

C1P C1N INL INR SVDD PVDD SHDNR# SHDNL# OUTL OUTR PVSS SVSS GND SGND PGND NC

C898 SC1U10V3ZY-6GP

DY R825 0R2J-2-GP

3D3V_S0_AU R816 1KR2J-1-GP → D43 CH3906PT-GP → R817 100KR2J-1-GP

SHDNL_R → R818 100KR2J-1-GP

SPKR_L+1 SPKR_R+1 30 AMP_SHUTDOWN

5V_S0 → U87 SHDN# SET GND IN OUT G923-330T1UF-GP

C899 SC1U10V3ZY-6GP

3D3V_S0 → DY R826 0R3-0-U-GP → 3D3V_S0_AU

C900 SC1U10V3ZY-6GP, C901 SC22P50V2JN-4GP, C902 SC2D2U16V5ZY-2GP

Internal SPKR

ERC4 SRC100P50V-2-GP

SPKR_R+ SPKR_R- SPKR_L+ SPKR_L-

SPKR1 ACES-CON4-1-GP 20.D0197.104

2nd source: 20.F0760.004

MIC-In

MIC1 PHONE-JK191 22.10133.901

28 MIC_IN_R → R827 10R3J-3-GP → MIC_R

28 MIC_IN_L → R697 10R3J-3-GP → MIC_L

28 MICIN_JD#

R835 22KR2J-GP, R836 22KR2J-GP

C820 SC100P50V3JN-2GP, C903 SC100P50V3JN-2GP, EC572 SCKP16V2KX-GP

Line-Out

LOUT1 PHONE-JK195 22.10133.931

28 LINEOUT_JD#

SPKR_R+1 → R703 22R2J-2-GP → HP_OUT_R_1

SPKR_L+1 → R707 22R2J-2-GP → HP_OUT_L_1

R706 1KR2J-1-GP, R702 1KR2J-1-GP

C826 SC680P50V2KX-2GP, C823 SC680P50V2KX-2GP, EC573 SCKP16V2KX-GP

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio AMP G1421B / Jack

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 29 of 52

For S/W Debug

Pin No.		Pin No.
1 3D3V_AUX_KBC	TP101 MODE1	2
3 H8_RESET#	TP102 MODE0	4
5 KBC_AC_IN#	TP104 H8_TXD1	6
7 LID_CLOSE#	TP106 H8_RXD1	8
9 PM_SLP_S3#	TP108 GND	10

TP103 TP75 TP74

1394/CardReader Detect Pin
H:non 1394/CardReader
L:has 1394/CardReader

non CardR R267 10KR2J-3-GP NAPA_U_V
-1 Modify
R268 10KR2J-3-GP CardR

RE144B

U73 RE144B-GP 71.00144.B0G

Place near KBC
(Near H11,Top side).

-2 modify

050510:For Battery switch fail issue

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

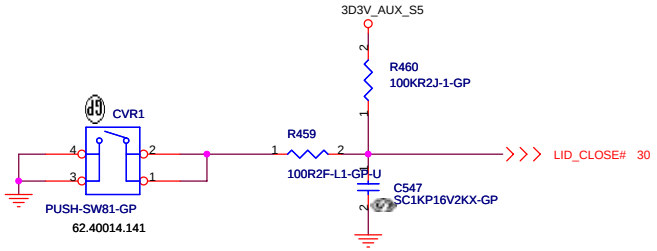
Title: KBC_RE144B

Size: A3 | Document Number: LWG2 | Rev: SA

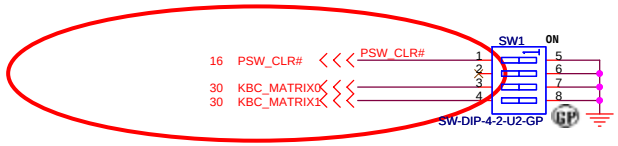
Date: Saturday, June 10, 2006 | Sheet 30 of 52

Internal KeyBoard Connector

COVER SWITCH

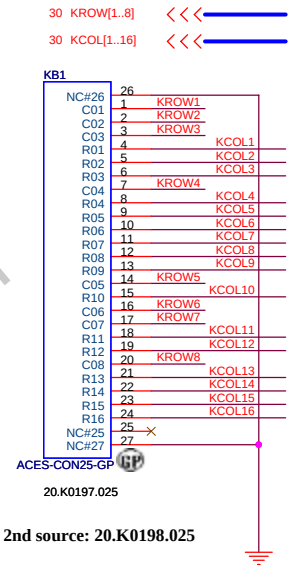


2nd source: 62.40010.151



Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



2nd source: 20.K0198.025

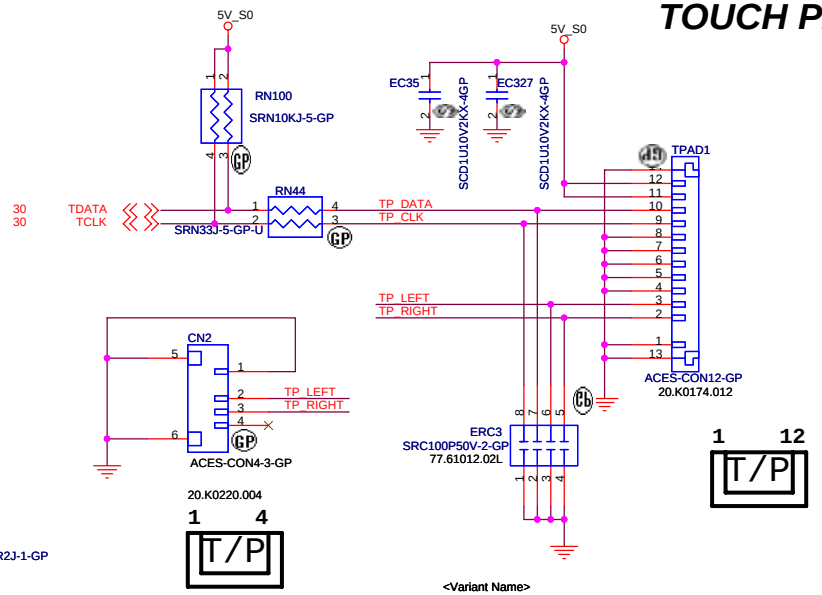
1 25

K/B

LAUNCH BD CONN

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

TOUCH PAD

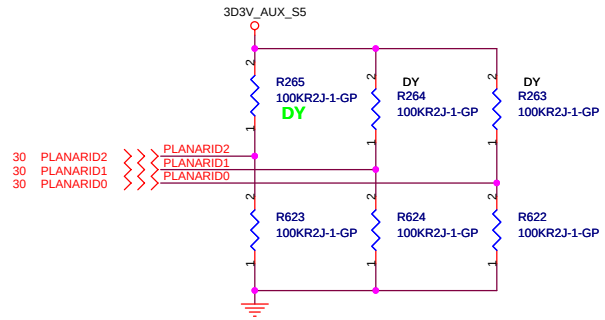


1 4

T/P

1 12

T/P



Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC,-1/-1m: 0,1,0
-2: 0,1,1

<Variant Name>

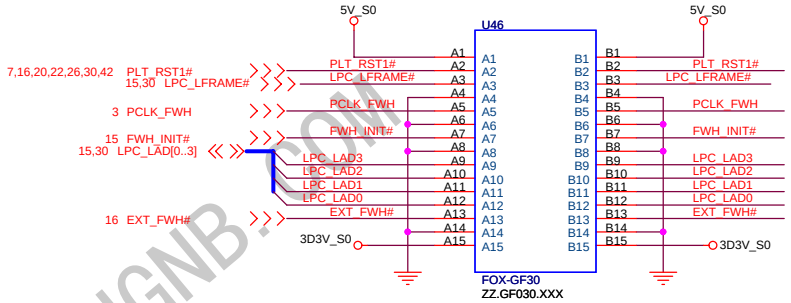
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCHPAD

Size: A3 | Document Number: LWG2 | Rev: SA

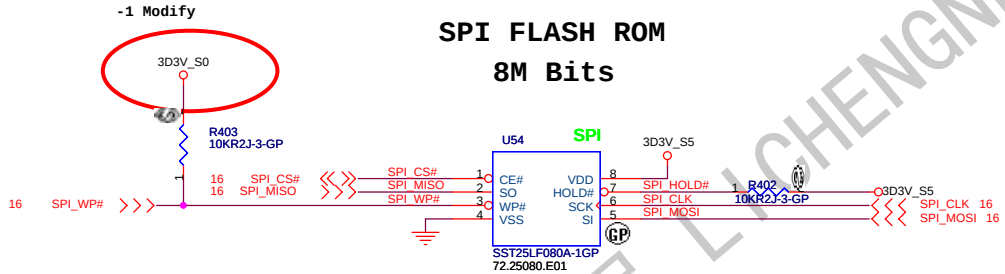
Date: Monday, June 12, 2006 | Sheet 31 of 52

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SPI FLASH ROM
8M Bits



SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS : SPI**

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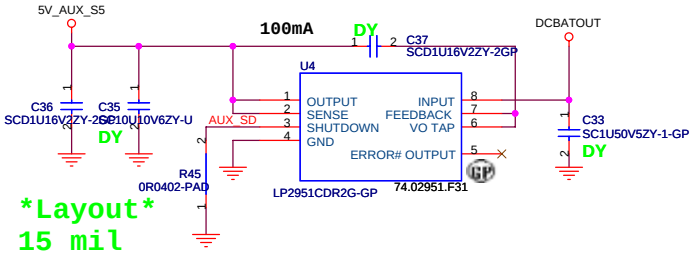
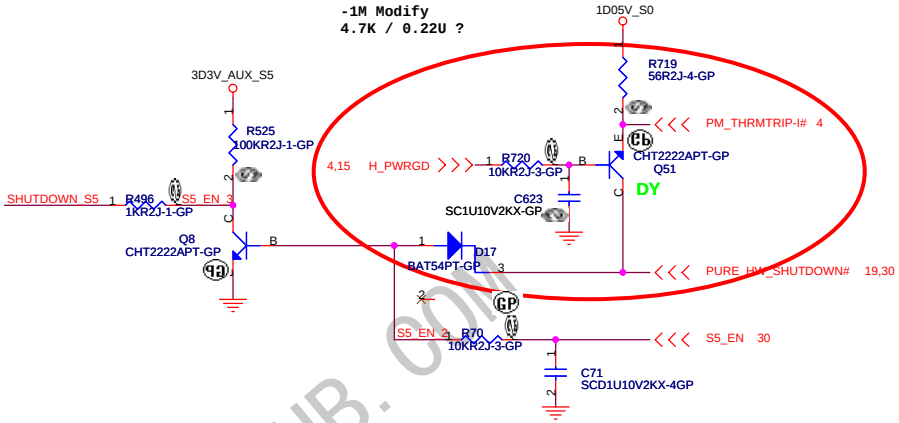
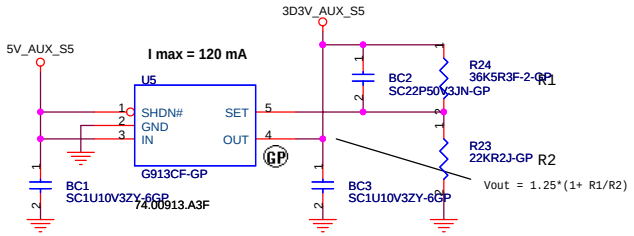
A3	LWG2	SA

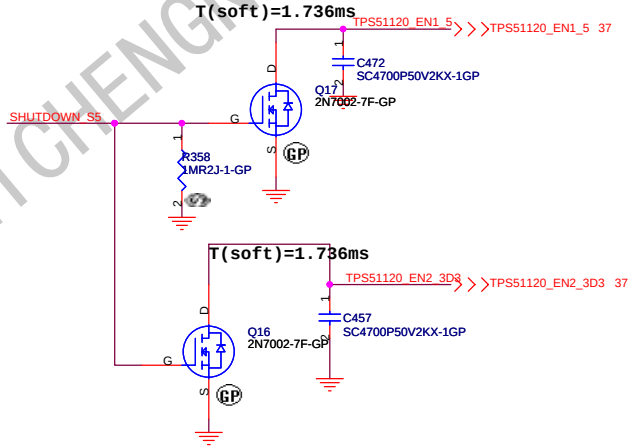
Date: Saturday, June 10, 2006 Sheet 32 of 52

Aux Power

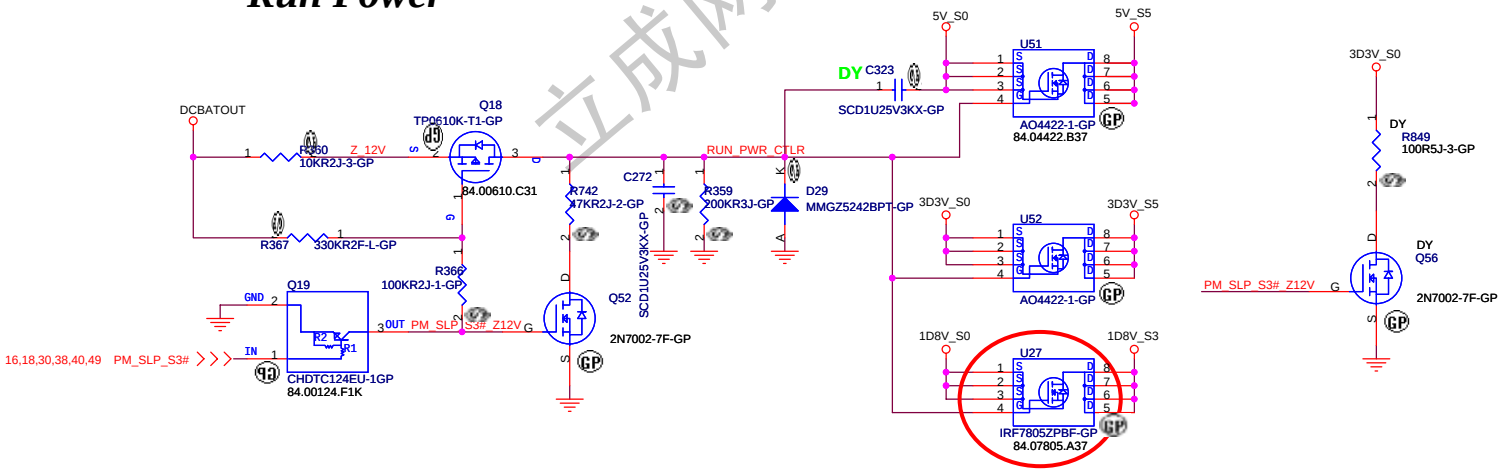








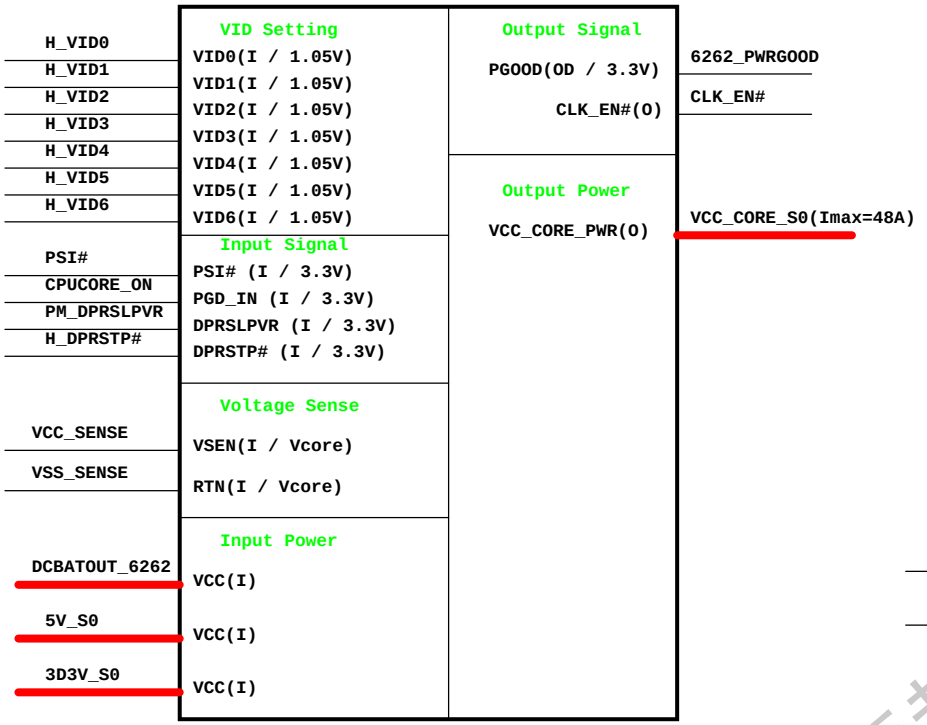
Run Power



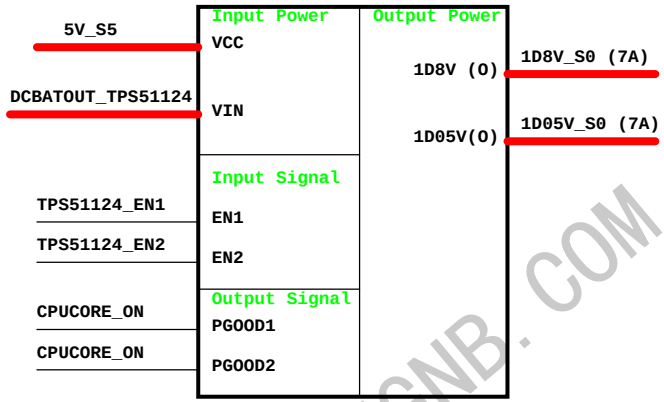
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN and AUX POWER	
Size A3	Document Number LWG2	Rev SA
Date: Saturday, June 10, 2006	Sheet 33 of 52	

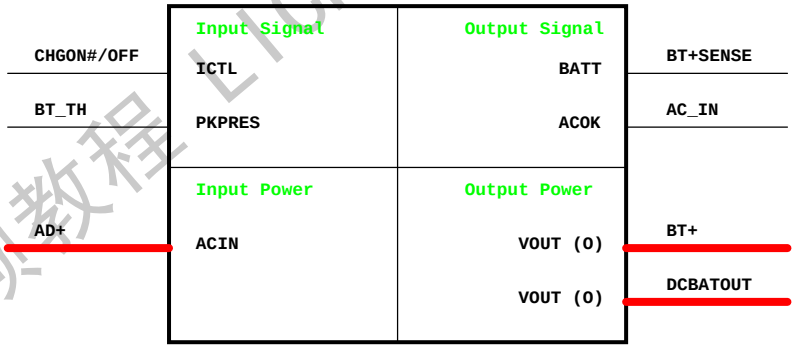
CPU_CORE
Intersil ISL6262



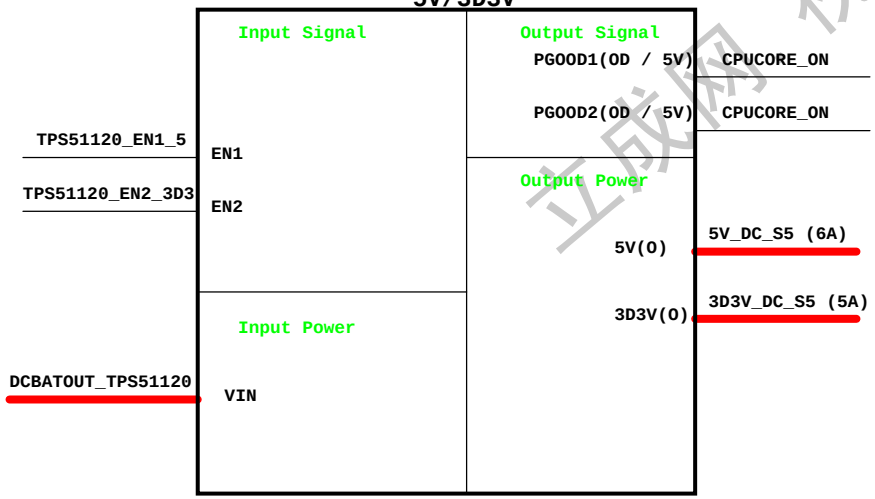
TPS51124
1D8V/1D05V



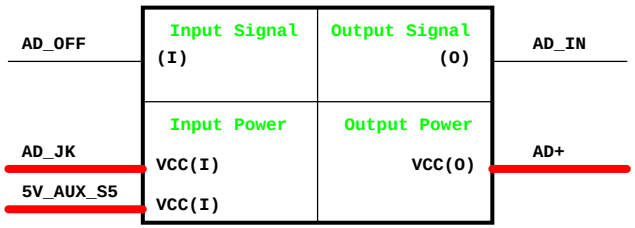
Charger Max8725



TPS51120
5V/3D3V



Adapter



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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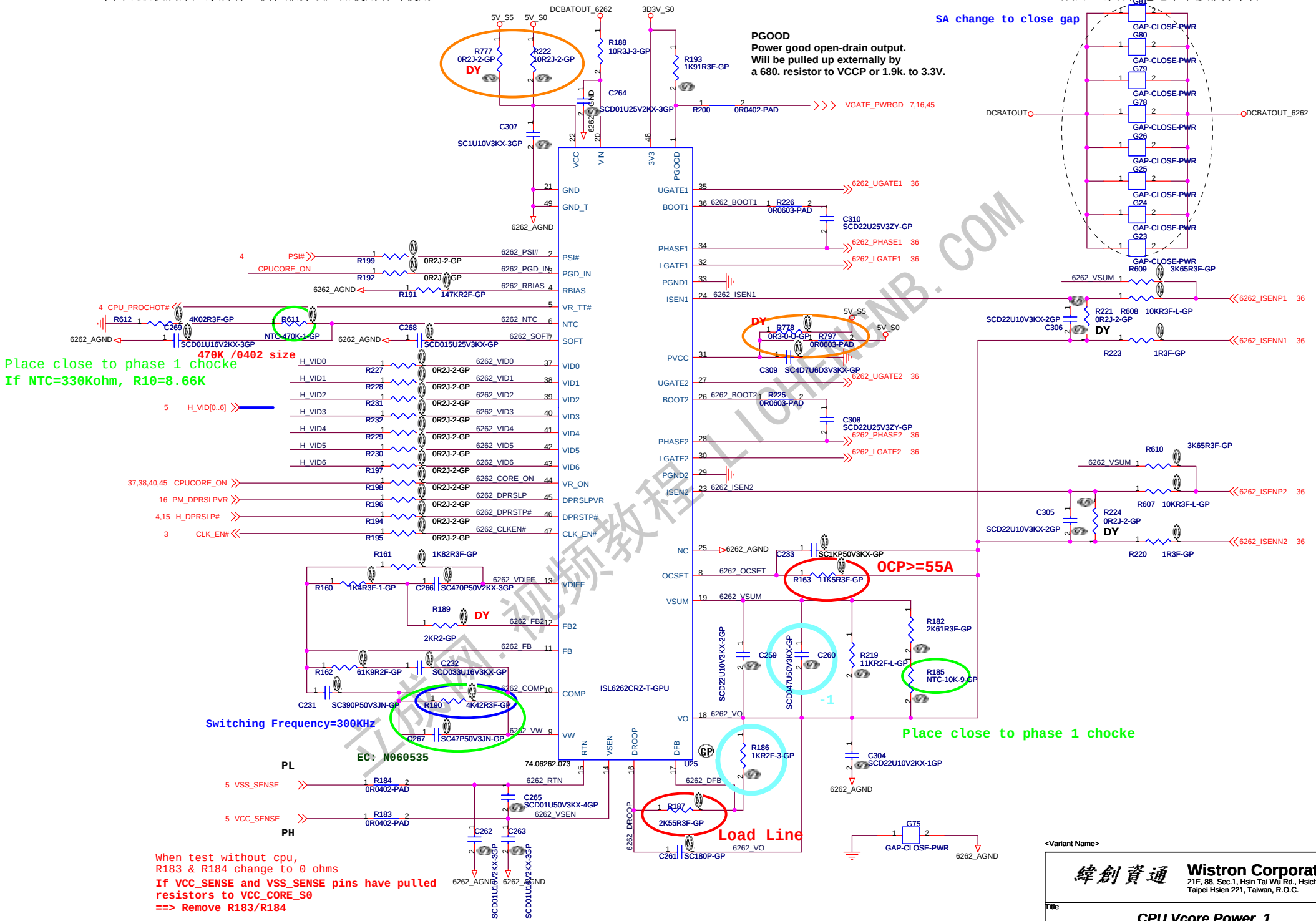


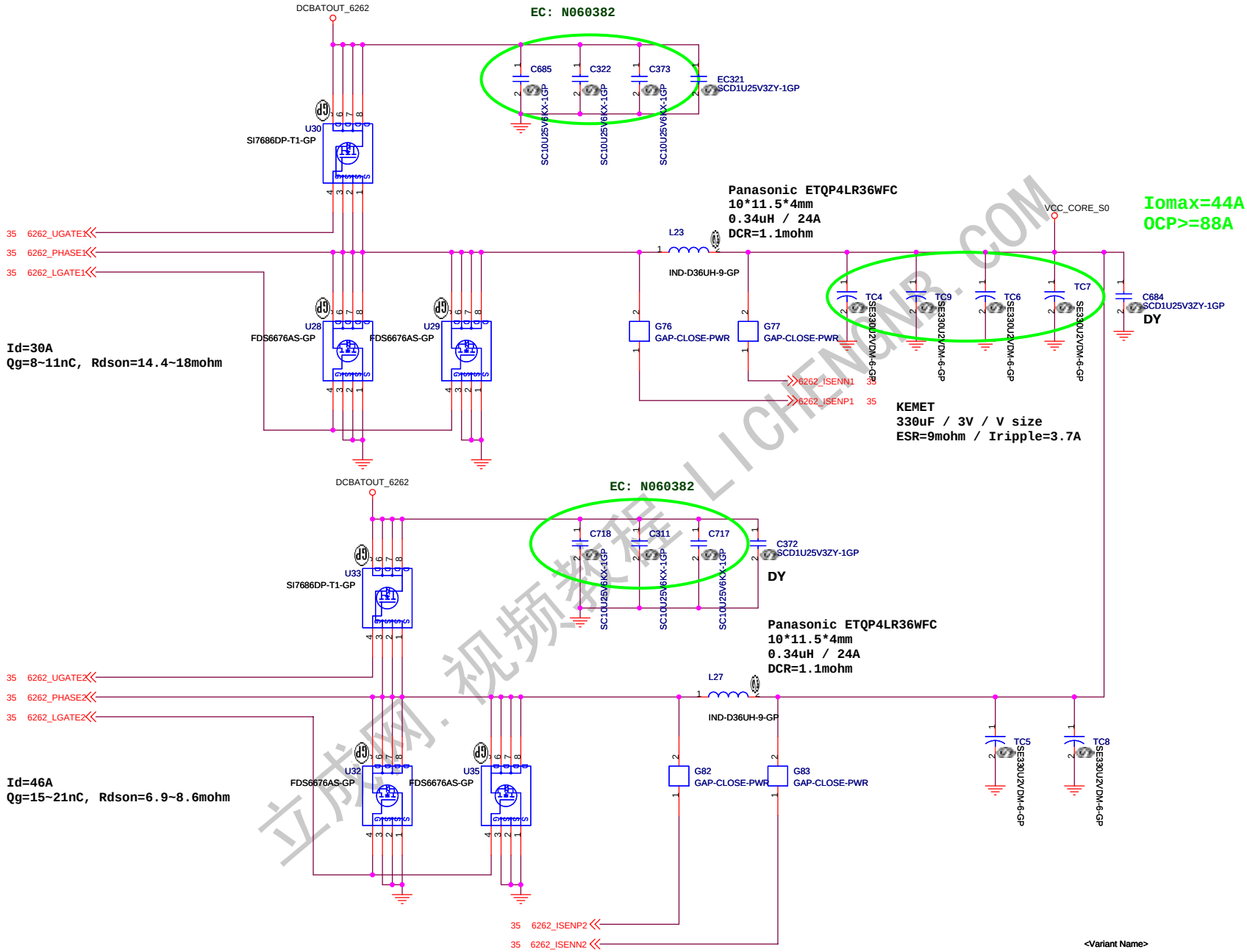
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 35 of 52



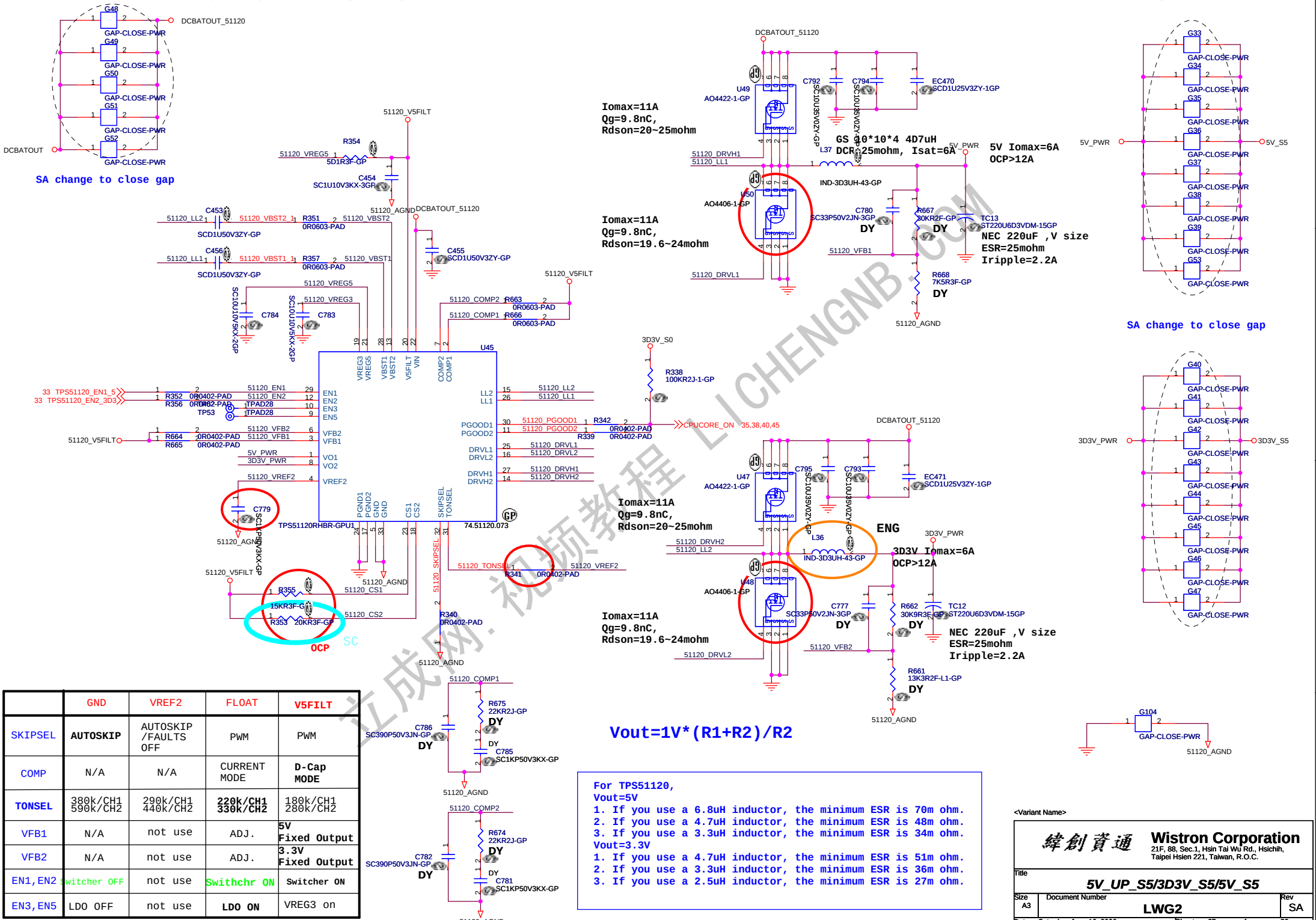
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_2

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 36 of 52



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **5V_UP_S5/3D3V_S5/5V_S5**

Size: A3 | Document Number: **LWG2** | Rev: SA

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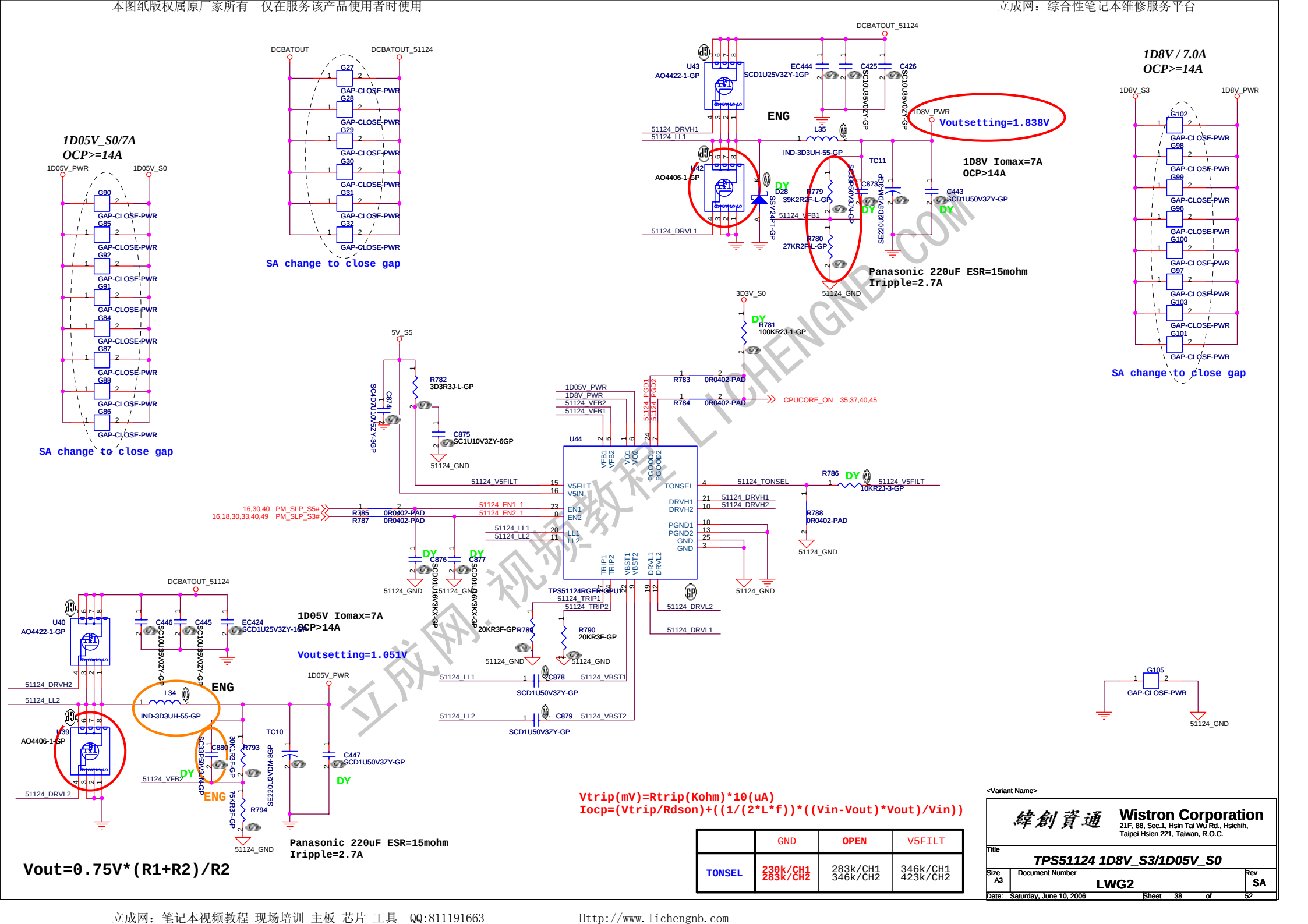

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V_S3/1D05V_S0

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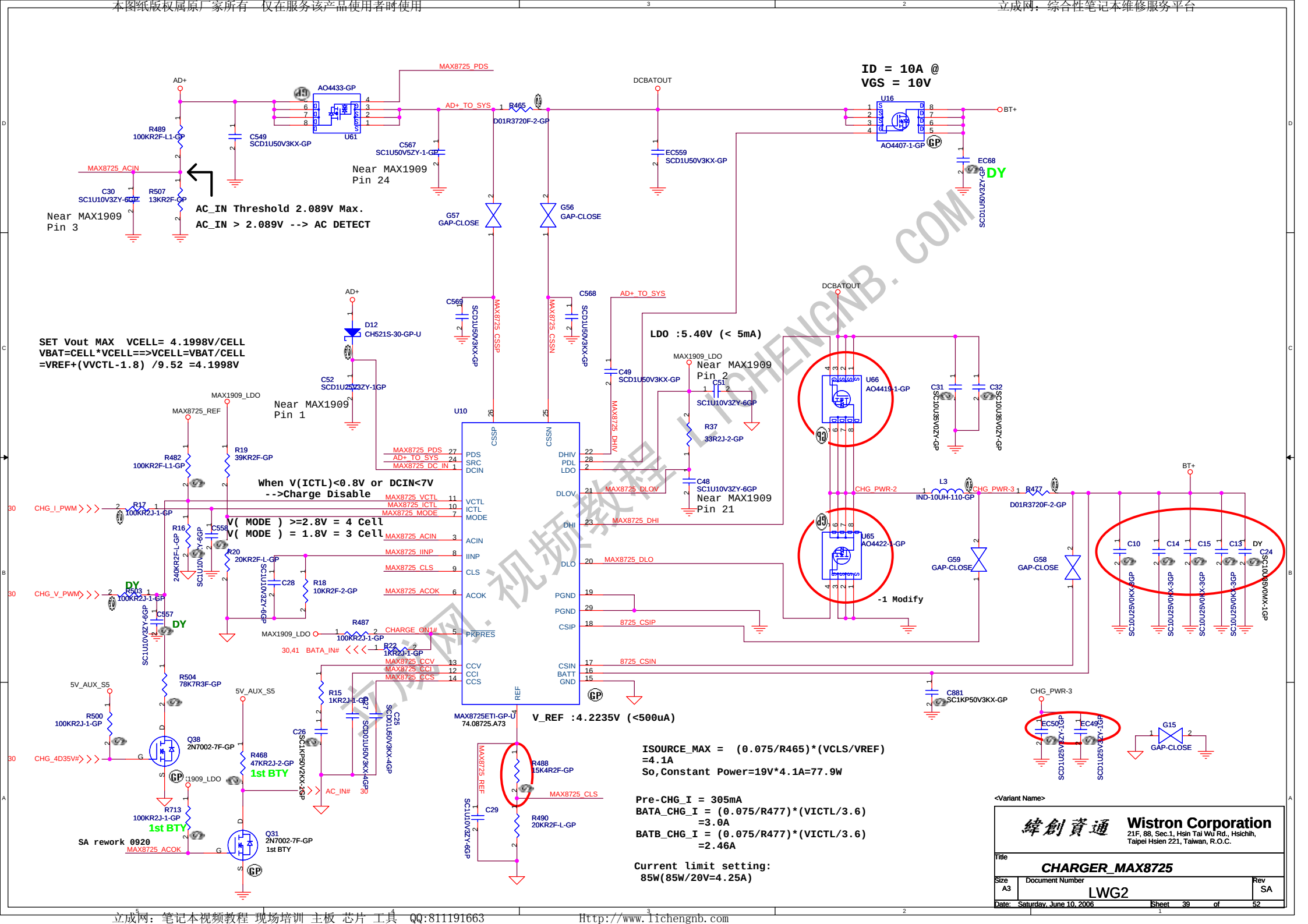

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER_MAX8725
Size: A3 | Document Number: LWG2 | Rev: SA
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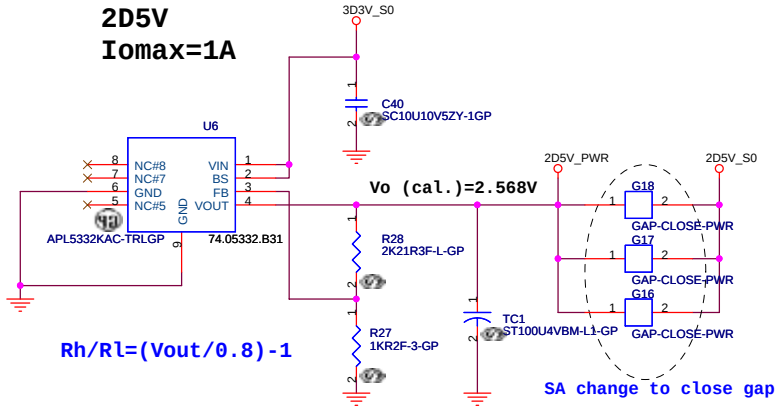
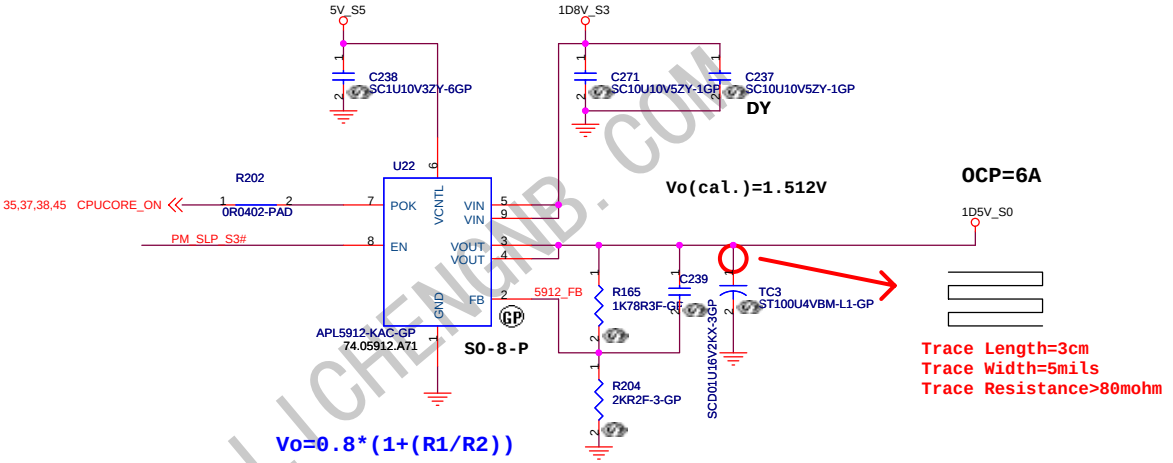
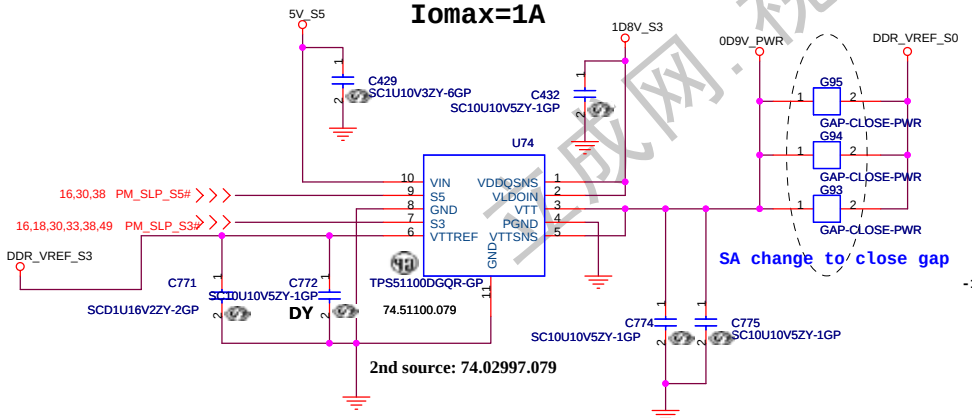
2D5V
Iomax=1A



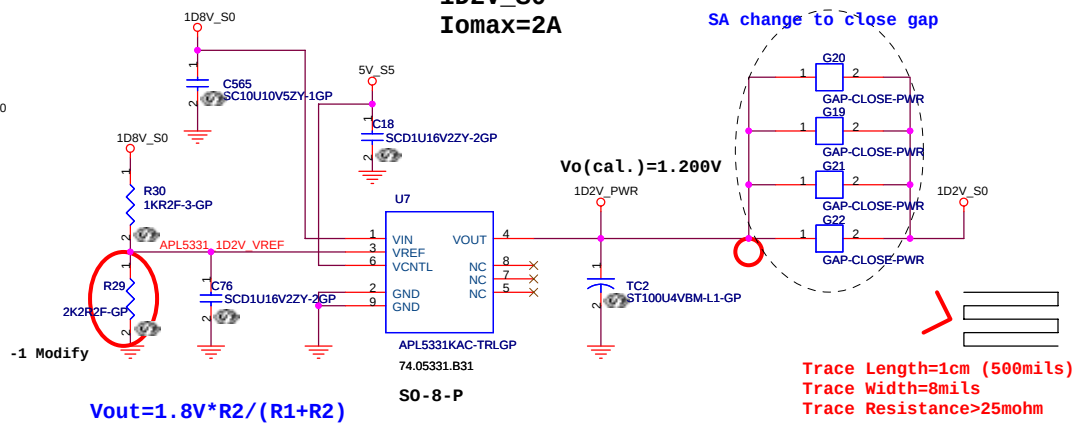
1D5V_S0
Iomax=4.0A



0D9V
Iomax=1A



1D2V_S0
Iomax=2A



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V/1D2V/1D5V/2D5V

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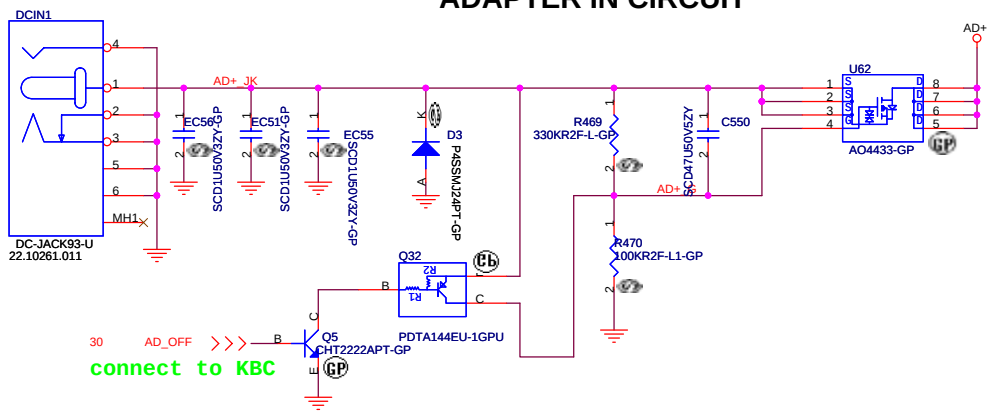
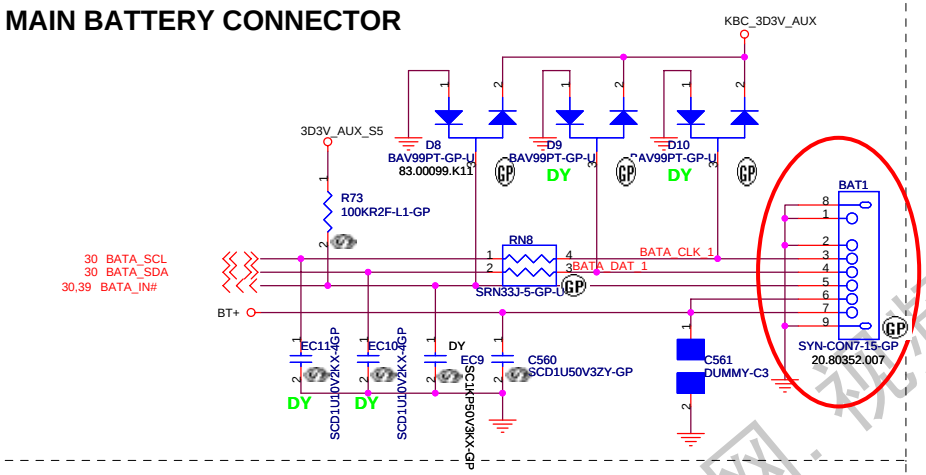
ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number LWG2	Rev SA
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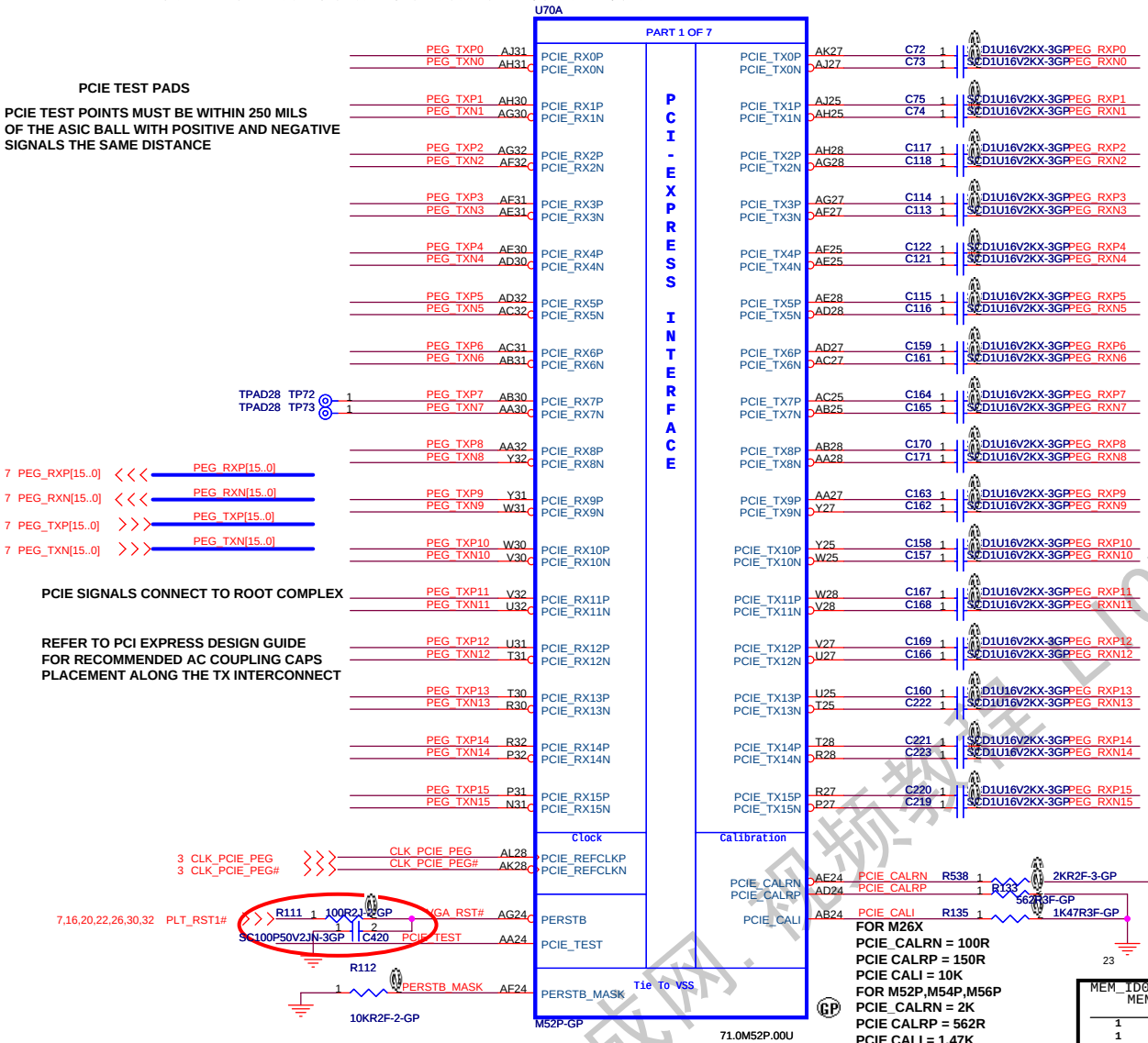
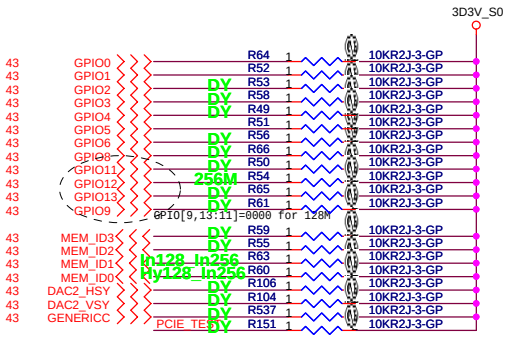


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO[9,13:11] GPIO[13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	1011 TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPS
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4



When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

VGA THERMAL SENSOR

Place near GPU

IT IS REQUIRED TO DESIGN IN A THERMAL SENSOR TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC

M54P:71.0M54P.A0U
M56P:71.0M56P.B0U

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P PCIE 1/4

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 42 of 52

Modulation Rate		
SEL1	SEL0	Center Spread
L	L	+-0.5%
L	H	+-1.0%
H	L	+-1.5%
H	H	No Spread

3D3V_S0
R520 0R2J-2-GP
R522 DUMMY-R2
DY
R493 0R2J-2-GP
R521 0R2J-2-GP
R114 0R2F-1-GP
VGA_XTALIN
R113 147R2F-GP
U67
SEL1 REFOUT SEL0 XOUT
CKOUT VDD VSS XIN
MB88154_XO
MB88154_XI
VGA_GPIO16
3D3V_SS_S0
MB88154PNF-JN-GP
71.88154.A0A
3D3V_S0
R518 0R3-0-U-GP
C576
SCD1U10V2KX-4GP

DVPCNTL,DVPDATA[23..0] FOR M26X ARE CONFIGURED FOR +3.3V SIGNALING MODE ON THIS DESIGN
CONNECT TO +1.8V OR VSS TO DEFINE DVO SIGNAL LEVEL FOR M52P,M54P,M56P NOT CONNECTED

C579 SC18P50V2JN-1-GP
R519 1MR2J-1-GP
X7 XTAL-27MHZ-39-GP 82.30034.281
MB88154_XI
MB88154_XO
C580 SC22P50V2JN-4GP
EC: N060188

R93 1KR2J-1-GP

ANY UNUSED GPIO CAN OPTIONALLY BE PANEL TYPE CONFIG STRAPS

3D3V_S0
RN14 SRN4K7J-8-GP
13 EDID_DAT
13 EDID_CLK
EDID_DAT
EDID_CLK

ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS

42 MEM_ID3
42 MEM_ID2
42 MEM_ID1
42 MEM_ID0

42 GPIO0
42 GPIO1
42 GPIO2
42 GPIO3
42 GPIO4
42 GPIO5
42 GPIO6
TPAD28 TP6
42 GPIO8
42 GPIO9
42 GPIO11
42 GPIO12
42 GPIO13
49 GPIO_PWRCNT
R484 10KR2J-3-GP
POW_SW
VGA_GPIO16
VGA_ALERT#
3D3V_S0
2K2R2J-2-GP

3D3V_S0
R91 499R2F-2-GP
R127 499R2F-2-GP
SCD1U10V2KX-4GP
C137
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC
VGA_VREF

FOR M26X PVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

19 G792_DXP3
19 G792_DXN3
C65 SC2200P50V2KX-2GP
VGA_PVDD
R57 0R0603-PAD
C66 SC10U10V5ZY-1GP
C98 SC1U6D3V2KX-GP
2D5V_S0
R591 0R0603-PAD
VGA_CORE_S0
VGA_MPVDD
C656 SC1U6D3V2KX-GP
C657 SCD1U10V2KX-4GP

FOR M26X MPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO VDDC

VGA_XTALIN
TPAD28 TP71
R132 1KR2J-1-GP
VGA_TESTEN
3D3V_S0
R94 10KR2J-3-GP
DY

VOLTAGE DIVIDER 3.3V MEM SS
MODOUT TO 1.2V XTALIN/OUT

adjust SWING at 1.2v

U70B
PART 2 OF 7

GPIO_34 GPIO_33 GPIO_32 GPIO_31 GPIO_30 GPIO_29 GPIO_28 GPIO_27 GPIO_26 GPIO_25 GPIO_24 GPIO_23 GPIO_22 GPIO_21 GPIO_20 GPIO_19 GPIO_18
Expand GPIO

NC_DVOVMODE_0
NC_DVOVMODE_1

DVPCNTL_0 DVPCNTL_1 DVPCNTL_2 DVPCLK
DVPDATA_0 DVPDATA_1 DVPDATA_2 DVPDATA_3 DVPDATA_4 DVPDATA_5 DVPDATA_6 DVPDATA_7 DVPDATA_8 DVPDATA_9 DVPDATA_10 DVPDATA_11 DVPDATA_12 DVPDATA_13 DVPDATA_14 DVPDATA_15 DVPDATA_16 DVPDATA_17 DVPDATA_18 DVPDATA_19 DVPDATA_20 DVPDATA_21 DVPDATA_22 DVPDATA_23
VIP Host/External TMDS

GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7_BLON GPIO_8 GPIO_9 GPIO_10 GPIO_11 GPIO_12 GPIO_13 GPIO_14 GPIO_15 GPIO_16 GPIO_17 NC_AB6
General Purpose I/O

VREFG
DPLUS DMINUS
Thermal Diode

PVDD PVSS MPVDD MPVSS XTALIN XTALOUT PLLTEST
PLL & XTAL

TESTEN
Test

ROMCSb
ROM

LVSSR_1 LVSSR_2 LVSSR_3 LVSSR_4 LVSSR_5 LVSSR_6 LVSSR_7
LVDS PLL and I/O GND

External SSC
GENERICC
LPVSS
LVDS PLL and I/O GND
LVSSR_10 LVSSR_9 LVSSR_8
M52P-GP

V I D E O & M U L T I M E D I A

Integrated TMDS
TXCM TXCP TX0M TX0P TX1M TX1P TX2M TX2P TX3M TX3P TX4M TX4P TX5M TX5P
TPVDD TPVSS
TXVDDR_1 TXVDDR_2 TXVDDR_3 TXVDDR_4
TXVSSR_1 TXVSSR_2 TXVSSR_3 TXVSSR_4 TXVSSR_5

DUAL LINK IS ONLY SUPPORTED ON M56P
DO NOT CONNECT TXM,P[3:5] WITH M52P,M54P,M26X

VGA_TPVDD
C582 SC1U6D3V2KX-GP
R524 0R0603-PAD
2D5V_S0

FOR M26X TPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

VGA_TXVDDR
C603 SC1U6D3V2KX-GP
C604 SCD1U10V2KX-4GP
C581 SCD1U10V2KX-4GP
R523 0R0603-PAD
2D5V_S0

FOR M26X TXVDDR
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

DAC / CRT
R G B
HSYNC VSYNC GENERICA GENERICB RSET
AVDD_1 AVDD_2
AVSSQ AVSSN_1 AVSSN_2
VDD1DI VSS1DI

ATI_RED 14
ATI_GREEN 14
ATI_BLUE 14
ATI_HSY 14
ATI_VSY 14
VGA_GENERICB R134 1KR2F-3-GP
VGA_CRT_RSET R105 510R2F-L-GP
VGA_AVDD
C107 SC1U6D3V2KX-GP
R539 HCB1608KF121T30-GP
2D5V_S0
VGA_VDD1DI
C103 SC1U6D3V2ZY-GP
C106 SC1U6D3V2ZY-GP
C104 SCD1U10V2KX-4GP
R108 0R0603-PAD
2D5V_S0

FOR M26X AVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X VDD1DI
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

DAC2 (TV/CRT2)
R2 G2 B2
H2SYNC V2SYNC
Y C COMP
R2SET
A2VDD_1 A2VDD_2
A2VSSN_1 A2VSSN_2
NC_A2VDDQ
A2VSSQ
VDD2DI
VSS2DI

DAC2_HSY 42
DAC2_VSY 42
DAC2 CAN BE TV SIGNALS OR SECONDARY CRT SIGNALS AS CONTROLLED BY AN INTERNAL MUX

ATI_TV_LUMA 14
ATI_TV_CRMA 14
ATI_TV_COMP 14
VGA_TV_RSET R102 715R2F-GP
VGA_A2VDD
C101 SCD1U10V2KX-4GP
C102 SC1U6D3V2KX-GP
R103 0R3-0-U-GP
2D5V_S0
TV
VGA_A2VDDQ
TPAD28 TP70
VGA_VDD2DI
C94 SC1U6D3V2KX-GP
C99 SC1U6D3V2ZY-GP
C100 SCD1U10V2KX-4GP
R62 0R3-0-U-GP
2D5V_S0

FOR M26X A2VDDQ
CONNECT TO +1.8V
FOR M52P,M54P,M56P
IT IS NO CONNECT

FOR M26X VDD2DI
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

Monitor Interface
HPD1
DDC1DATA DDC1CLK DDC2DATA DDC2CLK DDC3DATA DDC3CLK

R743 100KR2J-1-GP
ATI_DDCDAT 14
ATI_DDCCLK 14

For CRT

For DVI

For THERMAL SENSOR

GENERICC 42

FOR M26X GENERICC
NO CONNECT OR
EXT SPREAD SPECTRUM INPUT
FOR M52P,M54P,M56P
IT IS GPIO

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P IO 2/4
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Saturday, June 10, 2006 | Sheet 43 of 52

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Part 3 of 7

MEMORY INTERFACE A

DQA_0 DQA_1 DQA_2 DQA_3 DQA_4 DQA_5 DQA_6 DQA_7 DQA_8 DQA_9 DQA_10 DQA_11 DQA_12 DQA_13 DQA_14 DQA_15 DQA_16 DQA_17 DQA_18 DQA_19 DQA_20 DQA_21 DQA_22 DQA_23 DQA_24 DQA_25 DQA_26 DQA_27 DQA_28 DQA_29 DQA_30 DQA_31 DQA_32 DQA_33 DQA_34 DQA_35 DQA_36 DQA_37 DQA_38 DQA_39 DQA_40 DQA_41 DQA_42 DQA_43 DQA_44 DQA_45 DQA_46 DQA_47 DQA_48 DQA_49 DQA_50 DQA_51 DQA_52 DQA_53 DQA_54 DQA_55 DQA_56 DQA_57 DQA_58 DQA_59 DQA_60 DQA_61 DQA_62 DQA_63

MVREFD_0 MVREFS_0

MAA_0 MAA_1 MAA_2 MAA_3 MAA_4 MAA_5 MAA_6 MAA_7 MAA_8 MAA_9 MAA_10 MAA_11 MAA_12 MAA_13 MAA_14 MAA_15

DQMAb_0 DQMAb_1 DQMAb_2 DQMAb_3 DQMAb_4 DQMAb_5 DQMAb_6 DQMAb_7

read strobe: QSA_0 QSA_1 QSA_2 QSA_3 QSA_4 QSA_5 QSA_6 QSA_7

write strobe: QSA_0B QSA_1B QSA_2B QSA_3B QSA_4B QSA_5B QSA_6B QSA_7B

ODTA ODTA1

CLKA0 CLKA0b

CKEA0

RASA0b

CASA0b

WEA0b

CSA0b_0 CSA0b_1

CLKA1 CLKA1b

CKEA1

RASA1b

CASA1b

WEA1b

CSA1b_0 CSA1b_1

M52P-GP

Ch-A
FOR M52P,M54P,M26X
PIN B25 IS MA12 (BA0)
PIN C25 IS MA13 (BA1)
PIN E29 IS MA15 (BA2)
PIN E27 IS MA14
FOR M56P
PIN B25 IS MA14 (BA0)
PIN C25 IS MA15 (BA1)
PIN E29 IS MA13 (BA2)
PIN E27 IS MA12

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

U70D

Part 4 of 7

MEMORY INTERFACE B

DQB_0 DQB_1 DQB_2 DQB_3 DQB_4 DQB_5 DQB_6 DQB_7 DQB_8 DQB_9 DQB_10 DQB_11 DQB_12 DQB_13 DQB_14 DQB_15 DQB_16 DQB_17 DQB_18 DQB_19 DQB_20 DQB_21 DQB_22 DQB_23 DQB_24 DQB_25 DQB_26 DQB_27 DQB_28 DQB_29 DQB_30 DQB_31 DQB_32 DQB_33 DQB_34 DQB_35 DQB_36 DQB_37 DQB_38 DQB_39 DQB_40 DQB_41 DQB_42 DQB_43 DQB_44 DQB_45 DQB_46 DQB_47 DQB_48 DQB_49 DQB_50 DQB_51 DQB_52 DQB_53 DQB_54 DQB_55 DQB_56 DQB_57 DQB_58 DQB_59 DQB_60 DQB_61 DQB_62 DQB_63

MVREFD_1 MVREFS_1

DRAM_RST TEST_MCLK TEST_YCLK MEMTEST

MAB_0 MAB_1 MAB_2 MAB_3 MAB_4 MAB_5 MAB_6 MAB_7 MAB_8 MAB_9 MAB_10 MAB_11 MAB_12 MAB_13 MAB_14 MAB_15

DQMBb_0 DQMBb_1 DQMBb_2 DQMBb_3 DQMBb_4 DQMBb_5 DQMBb_6 DQMBb_7

read strobe: QSB_0 QSB_1 QSB_2 QSB_3 QSB_4 QSB_5 QSB_6 QSB_7

write strobe: QSB_0B QSB_1B QSB_2B QSB_3B QSB_4B QSB_5B QSB_6B QSB_7B

ODTB ODTB1

CLKB0 CLKB0b

CKEB0

RASB0b

CASB0b

WEB0b

CSB0b_0 CSB0b_1

CLKB1 CLKB1b

CKEB1

RASB1b

CASB1b

WEB1b

CSB1b_0 CSB1b_1

M52P-GP

Ch-B
FOR M52P,M54P,M26X
PIN H2 IS MAB12 (BA0)
PIN H3 IS MAB13 (BA1)
PIN D5 IS MAB15 (BA2)
PIN F5 IS MAB14
FOR M56P
PIN H2 IS MA14 (BA0)
PIN H3 IS MA15 (BA1)
PIN D5 IS MA13 (BA2)
PIN F5 IS MAB12

For GDDR2

1D8V_S0

R581 100R2F-L1-GP-U

C666 SCD1U25V2KX-4GP

R590 100R2F-L1-GP-U

1D8V_S0

R580 100R2F-L1-GP-U

C665 SCD1U25V2KX-4GP

R589 100R2F-L1-GP-U

RN15 SRN4K7J-8-GP

R714 243R3F-GP

SC Modify

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

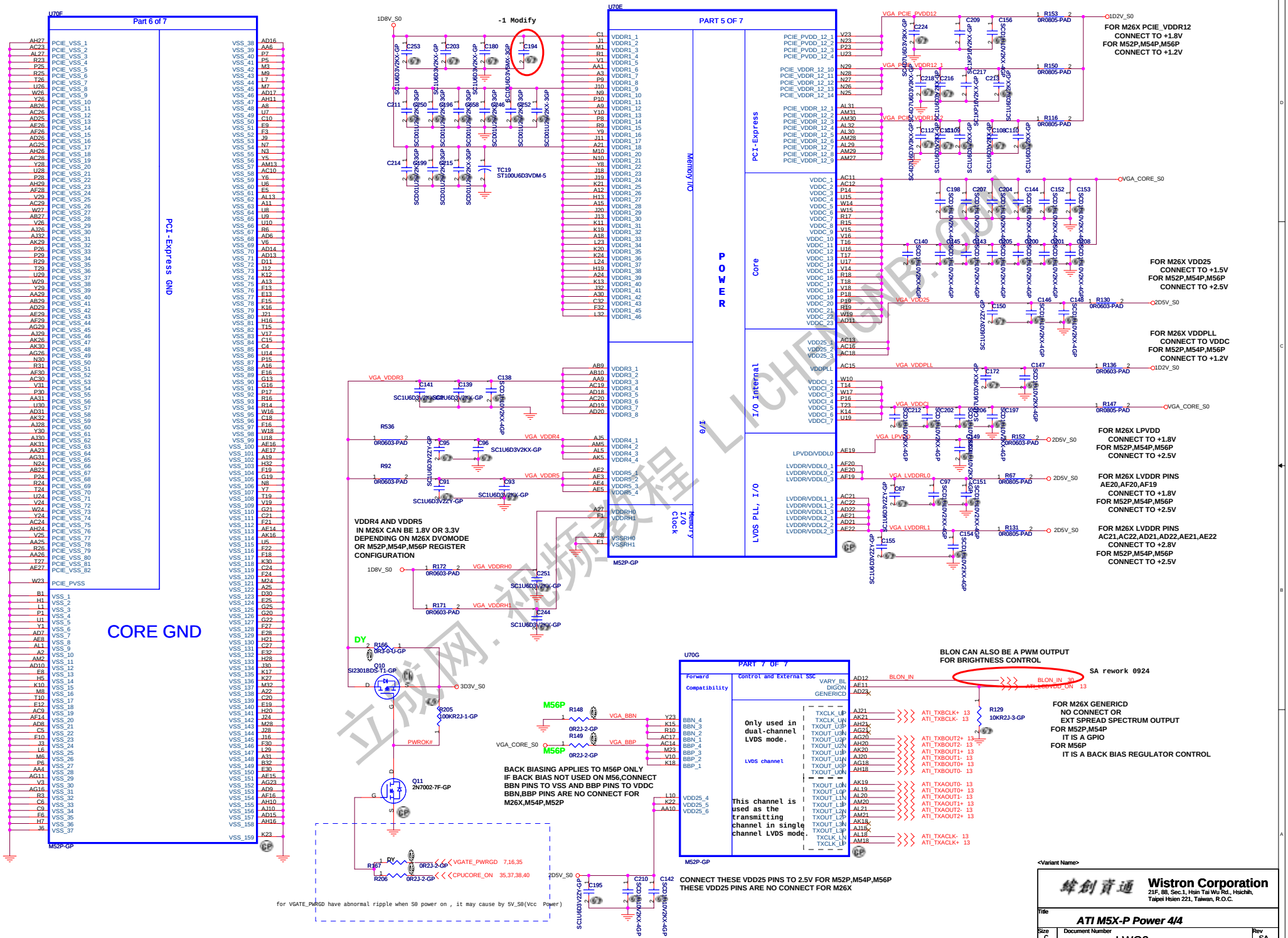
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M5X-P MEM 3/4**

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 44 of 52



<Variant Name>

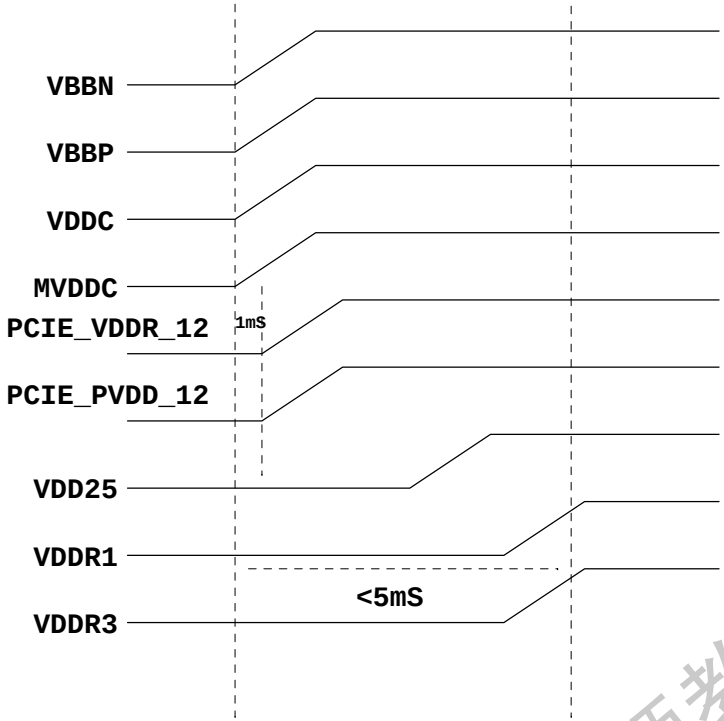
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P Power 4/4

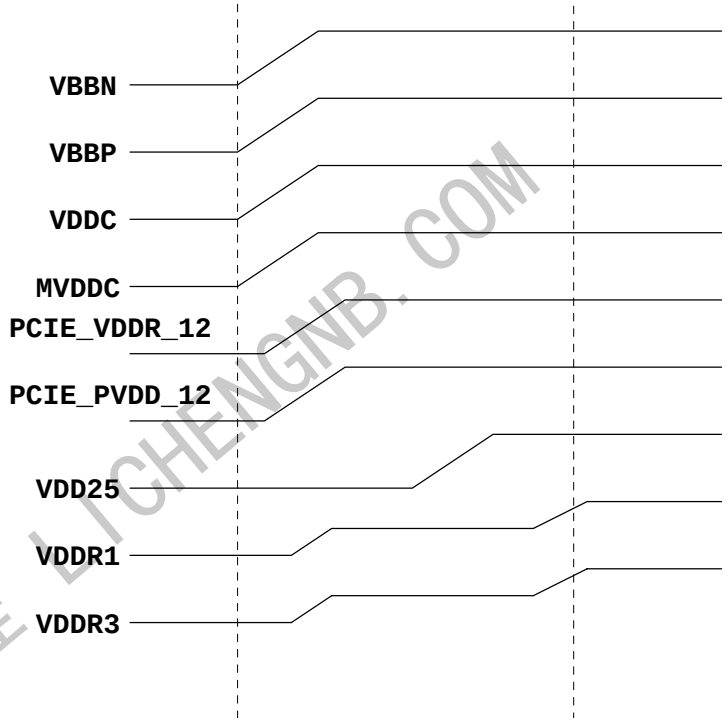
Size: C | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 45 of 52

Ideal Power Up Sequence



Real Power Up Sequence



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

General Guidelines:

- **BBN and BBP must ramp up before or at the same time as VDDC but not after.**
- **VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).**
- **All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).**
- **VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.**
- **The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.**

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>

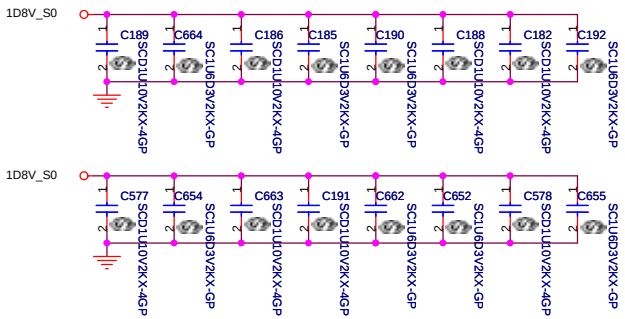
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

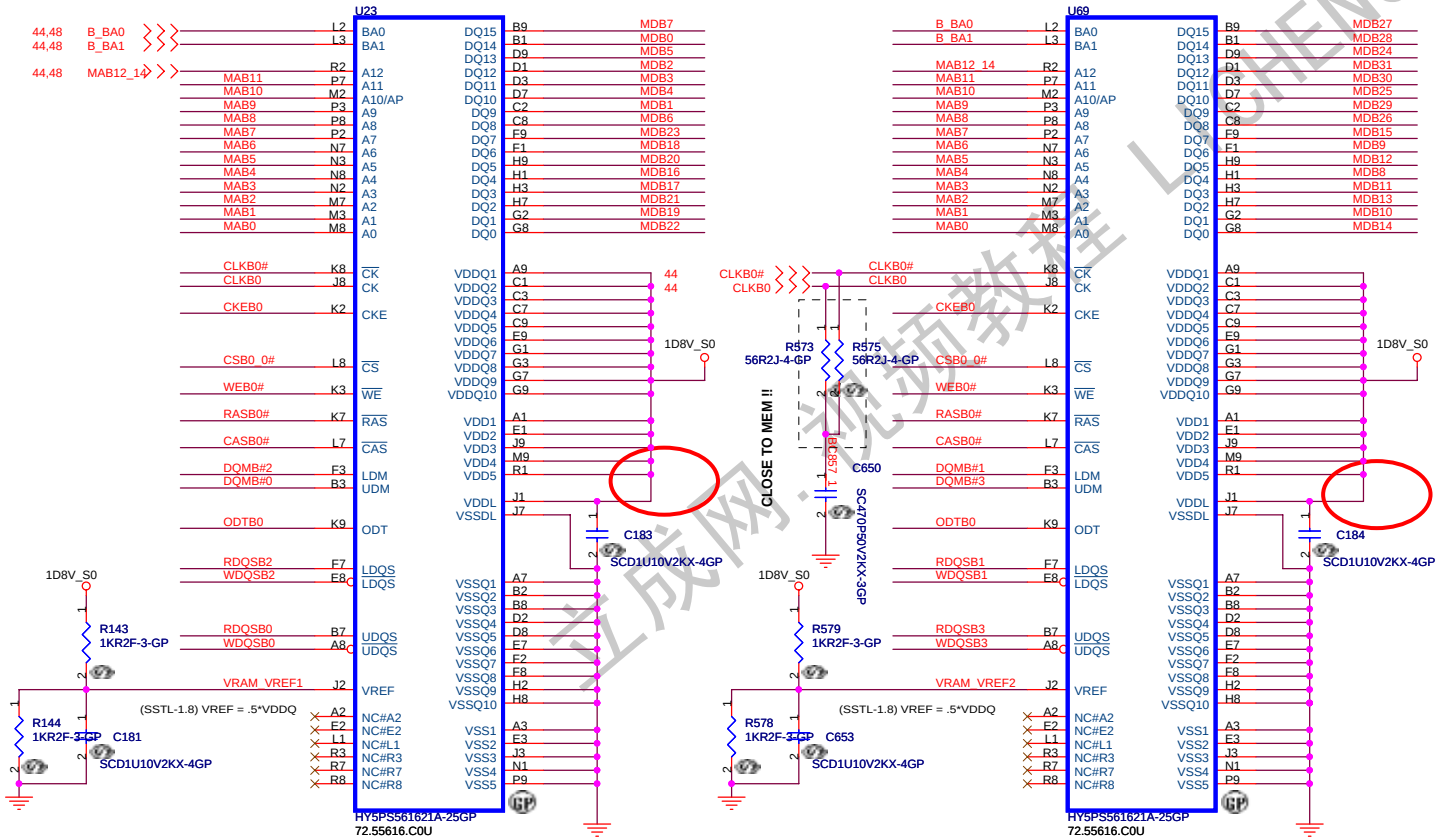
Title: ATI M5X-P POWER SEQUENCE

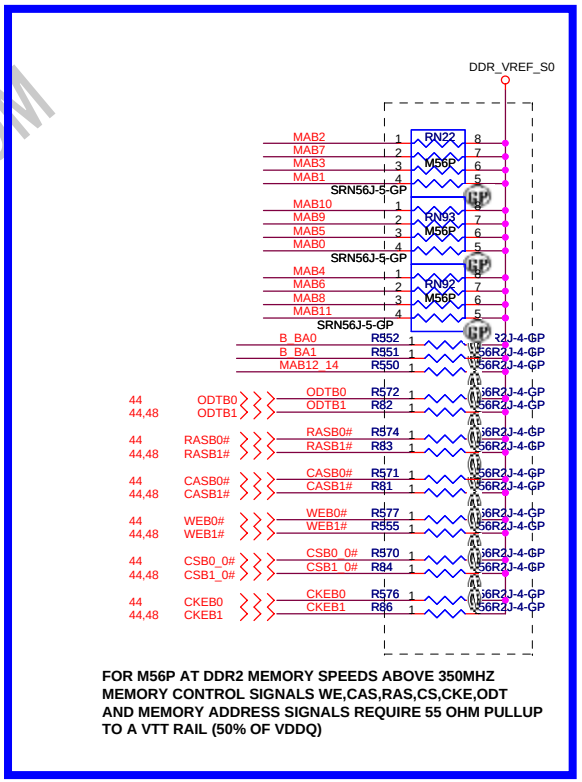
Size	Document Number	Rev
A3	LWG2	SA

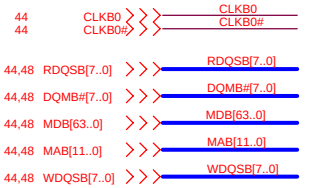
Date: Saturday, June 10, 2006 Sheet 46 of 52

CHAN B DDR2 84BGA 32MX16 MEMORY









72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 350Mhz) Hynix-128M
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M*16, 350Mhz) Infineon-128M
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M*16, 400Mhz) Infineon-256M

<Variant Name>

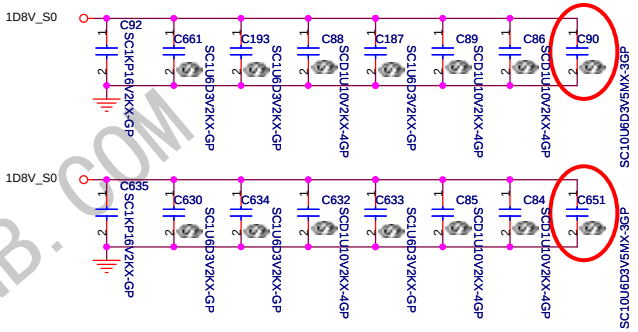
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

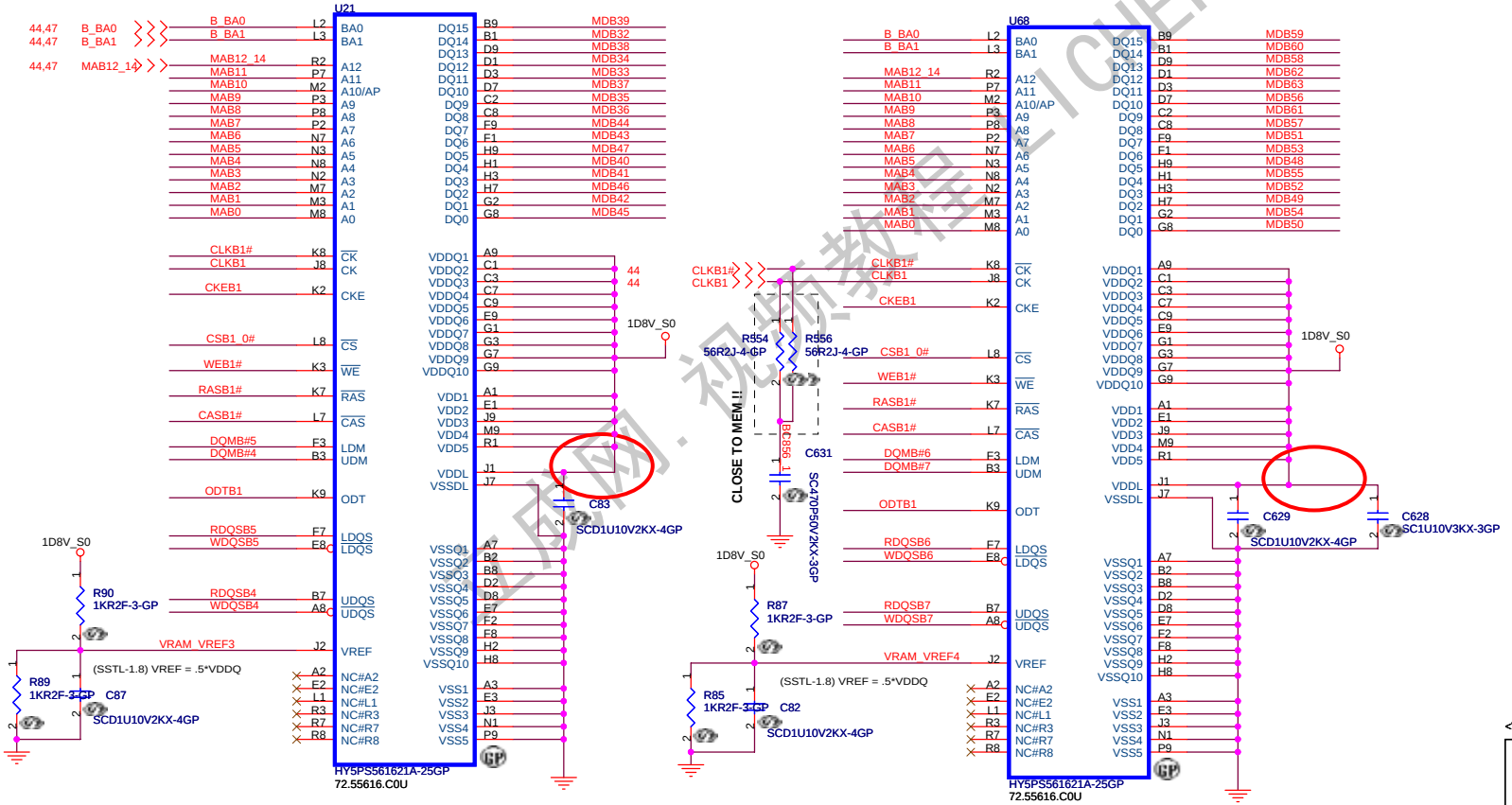
Title: VRAM 1/2

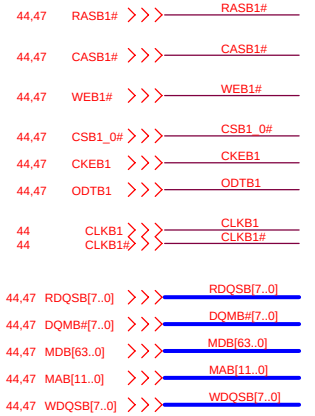
Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 47 of 52

-1 Modify







<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM 2/2

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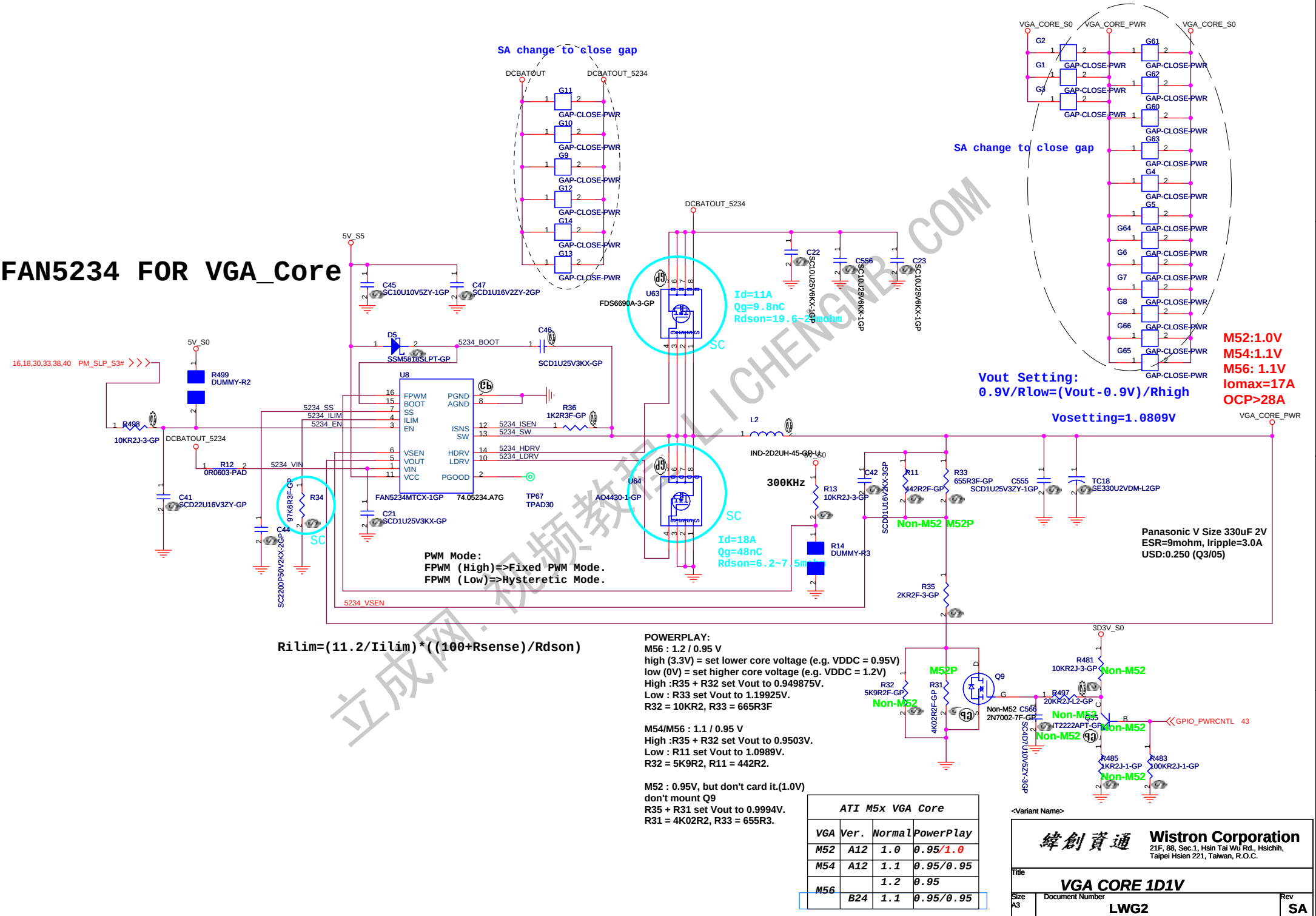
FAN5234 FOR VGA_Core



ATI M5x VGA Core			
VGA	Ver.	Normal	PowerPlay
M52	A12	1.0	0.95/1.0
M54	A12	1.1	0.95/0.95
M56		1.2	0.95
	B24	1.1	0.95/0.95

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Title: VGA CORE 1D1V
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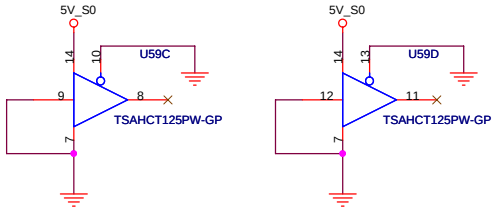
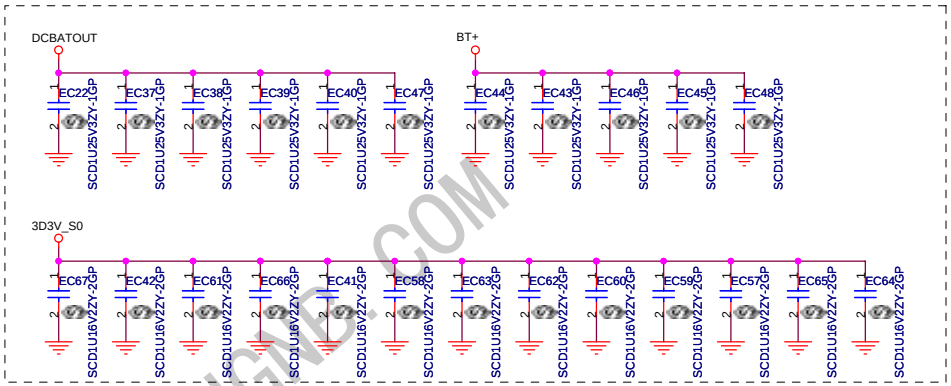
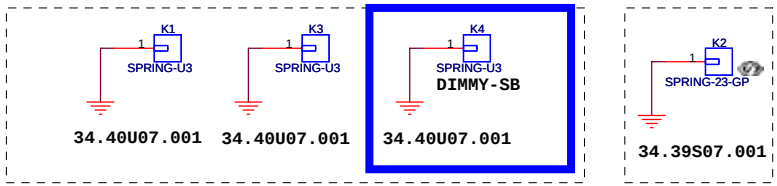
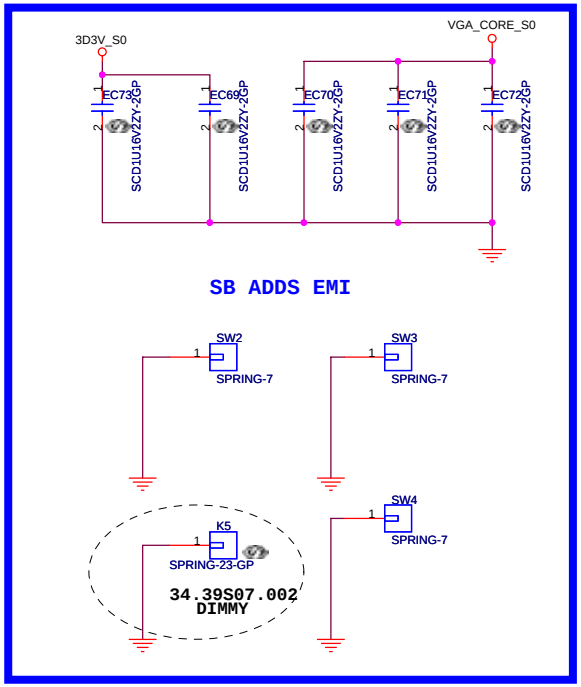
EMI CAP









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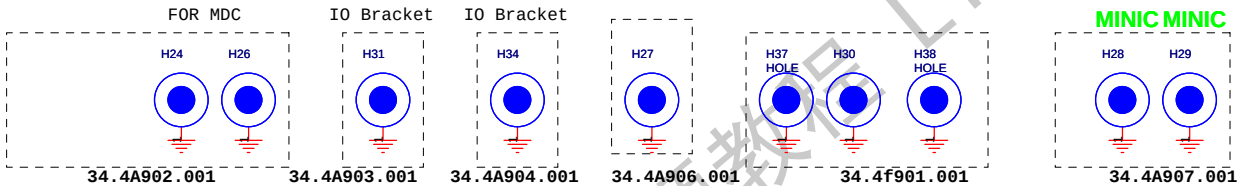

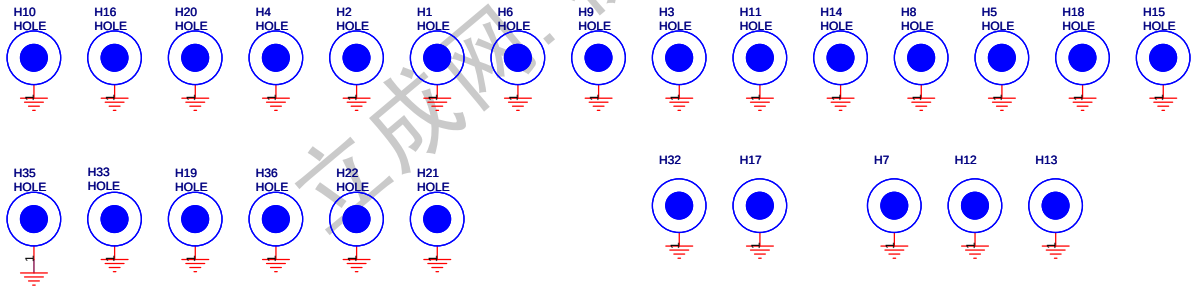

<Variant Name>

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Title: SPRING & BOSS

Size	Document Number	Rev
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Broadcom LAN

BCM4401E

IDSEL:AD23
INTA-->:INT_PIRQH#
GNT:PCI_GNT#2
REQ:PCI_REQ#2

CLOSE TO PHY PINS

Place PLLVDD/AVDDL CKT as close to chip as possible

BCM4401EKFBG-GP

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Title: BCM4401E
Size: A3 | Document Number: LWG2 | Rev: SA
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SA change to SB version change notes

1. Page 16 _ C773,C807,C811 for OC# cap -->Dimmy
3. Page 18 _ modify Q36/Q37 mirror
4. Page 50 _ Adds EMI Spring SW2,SW3, SW4 & K5 -- >34.49U26.001
5. Page 16 _ Adds R47 for MDC detect function -- > MDC_KILL# to SB GPIO24
6. Page 21 _ Adds R850,R844 for USB pull low
7. Page 21 _ Adds R25,R26,R38 for USB control to SB GPIO 25/26/27 pin (if use KBC GPIO then Dimmy)
8. Page 21 _ Adds R39,R40,R46 for USB control to KBC GPIO P-25/26/27 pin (if use SB GPIO then Dimmy)
9. Page 21 _ Add D44 for MDC_KILL#
10. Page 50 _ Adds EMI 5 pcs 0.1uF cap
11. Page 19 _ Adds TP118,TP119 tesr pad for test
12. Page 19 _ mirror L12,L13
13. Page 50 _ K4 Dimmy -- > BOM change
14. Page 14 _ L17,L18,L19 change to 47 Ohm -- >68.00084.271
15. Page 23 _ EC2 change to 78.1022N.24L
16. Page 15 _ adds R553 for ACZ_RST# signal to MDC & ALC883
    one signal ACZ_RST_ALC# to audio to page 28
    one signal ACZ_RST_MDC# to modem detect page 21
17. Page 21 _ adds R69 for D44 pull-hi-->63.10334.1DL
18. Page 35/37/38/40/49_Power Open Gap change to Power Close Gap
19. Page 31_ Wireless-BT & NOVO-BT pin change
20. Page 50_ K5 Dimmy

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
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