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FCB

# Compal Confidential

## IFTxx Schematics Document

**Intel Merom Processor with Crestline + DDRII + ICH8M  
(With nVIDIA MXM/B)**

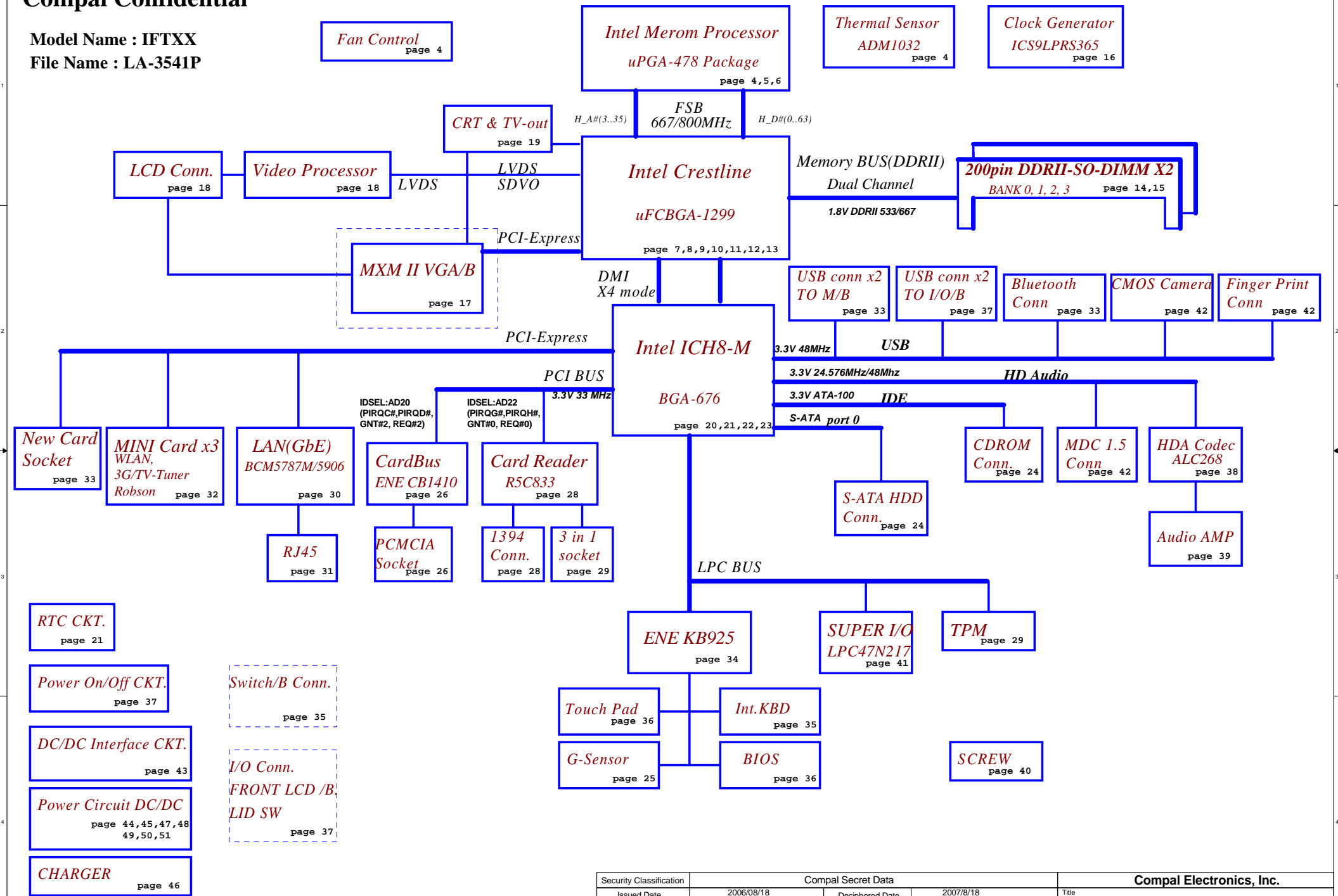
**2006-11-01**

**REV: 0.1**

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Model Name : IFTXX  
File Name : LA-3541P



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

## EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
NVIDIA NB8X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

## BOARD ID Table

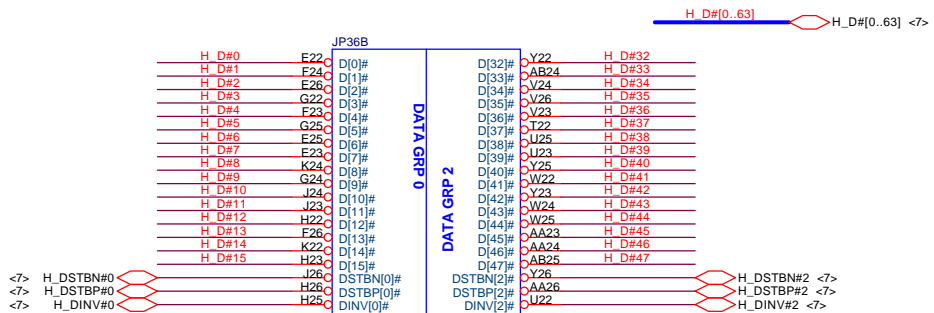
ID1	ID0	TEST
0 (R744)	0 (R745)	A-TEST
0 (R744)	1 (R742)	B-TEST
1 (R741)	0 (R745)	C-TEST

## PANEL ID Table

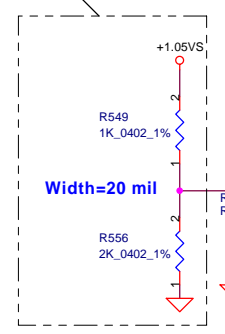
R	Size
Ra (R743)	15W
Rb (R740)	14W

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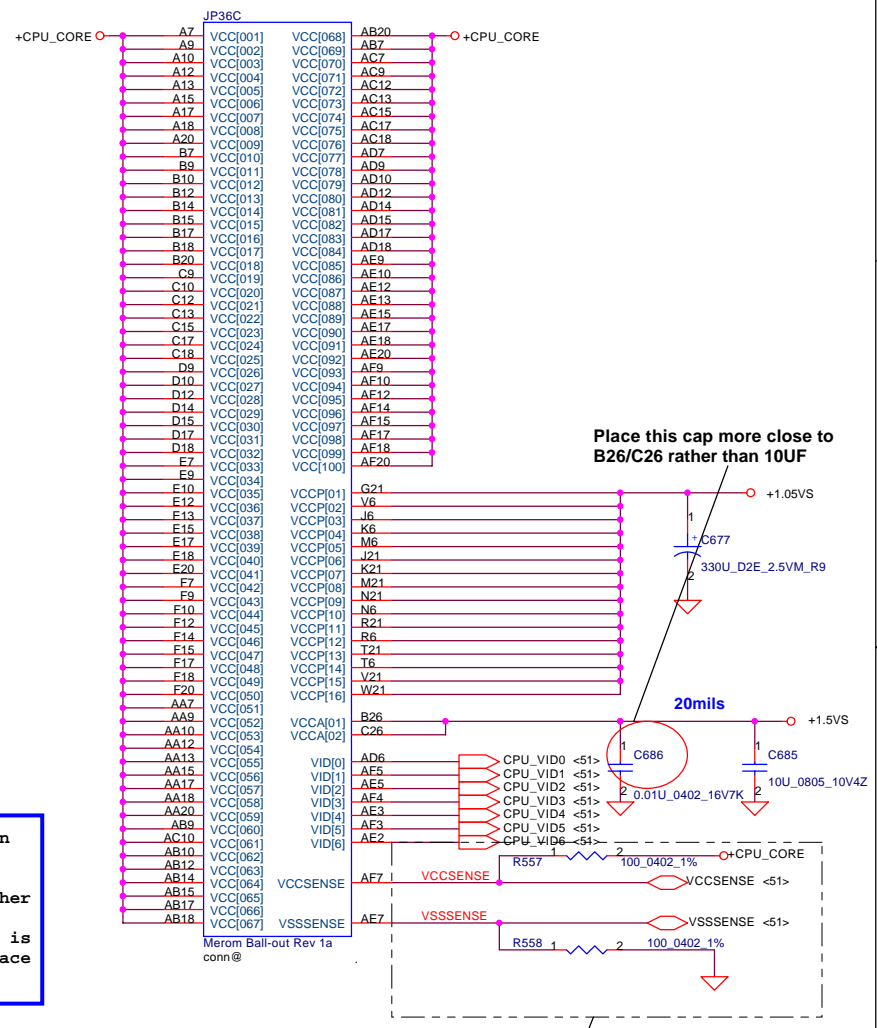
Close to CPU pin AD26 within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



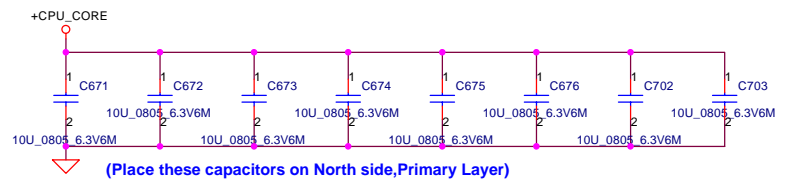
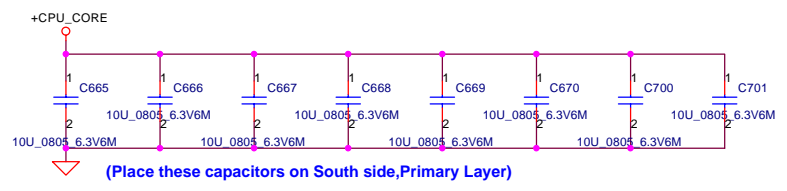
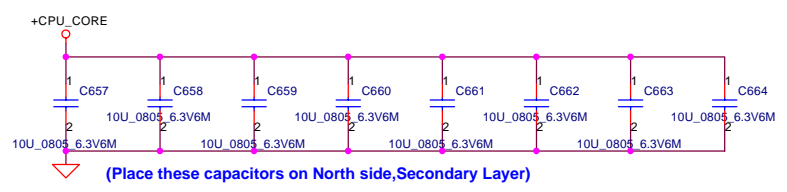
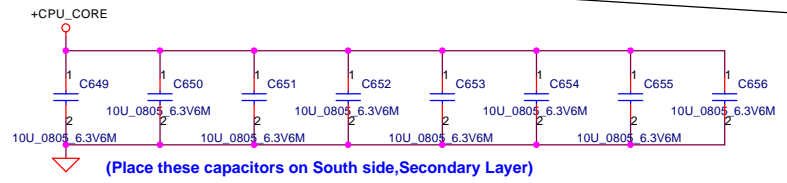
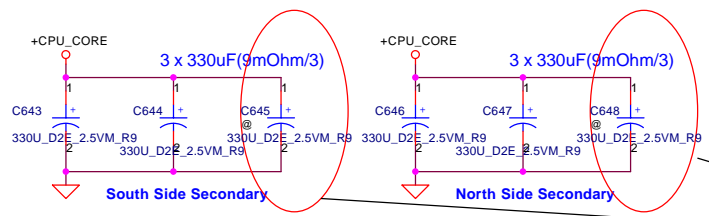
Place this cap more close to B26/C26 rather than 10UF

Length match within 25 mils. The trace width/space/other is 20/7/25.

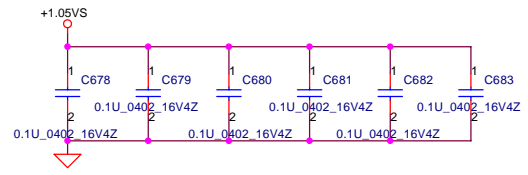
Close to CPU pin within 500mils.

JP36D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A26	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D8	VSS[027]	VSS[108]
D11	VSS[028]	VSS[109]
D13	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D23	VSS[032]	VSS[113]
D26	VSS[033]	VSS[114]
E3	VSS[034]	VSS[115]
E6	VSS[035]	VSS[116]
E8	VSS[036]	VSS[117]
E11	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[040]	VSS[121]
E21	VSS[041]	VSS[122]
F24	VSS[042]	VSS[123]
F5	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F2	VSS[049]	VSS[130]
F22	VSS[050]	VSS[131]
F25	VSS[051]	VSS[132]
G4	VSS[052]	VSS[133]
G1	VSS[053]	VSS[134]
G23	VSS[054]	VSS[135]
G26	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H21	VSS[058]	VSS[139]
H24	VSS[059]	VSS[140]
J2	VSS[060]	VSS[141]
J5	VSS[061]	VSS[142]
J22	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K23	VSS[066]	VSS[147]
K26	VSS[067]	VSS[148]
L3	VSS[068]	VSS[149]
L6	VSS[069]	VSS[150]
L21	VSS[070]	VSS[151]
L24	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M5	VSS[073]	VSS[154]
M22	VSS[074]	VSS[155]
M25	VSS[075]	VSS[156]
N1	VSS[076]	VSS[157]
N4	VSS[077]	VSS[158]
N23	VSS[078]	VSS[159]
N26	VSS[079]	VSS[160]
P3	VSS[080]	VSS[161]
	VSS[081]	VSS[162]
		VSS[163]

Merom Ball-out Rev 1a  
conn@



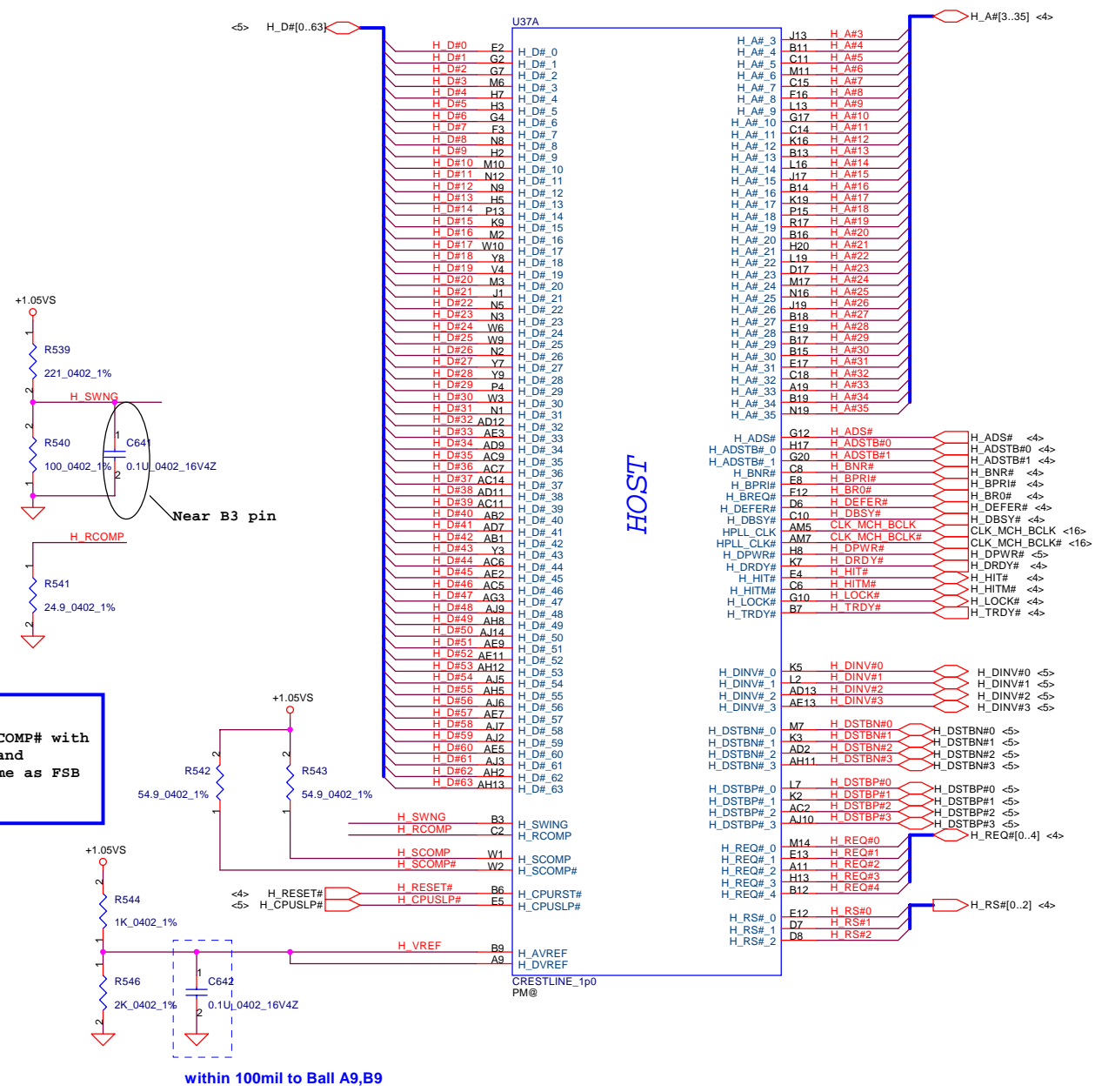
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



CRB no stuff. Reserved!

9/25 10U checked. OK for use!

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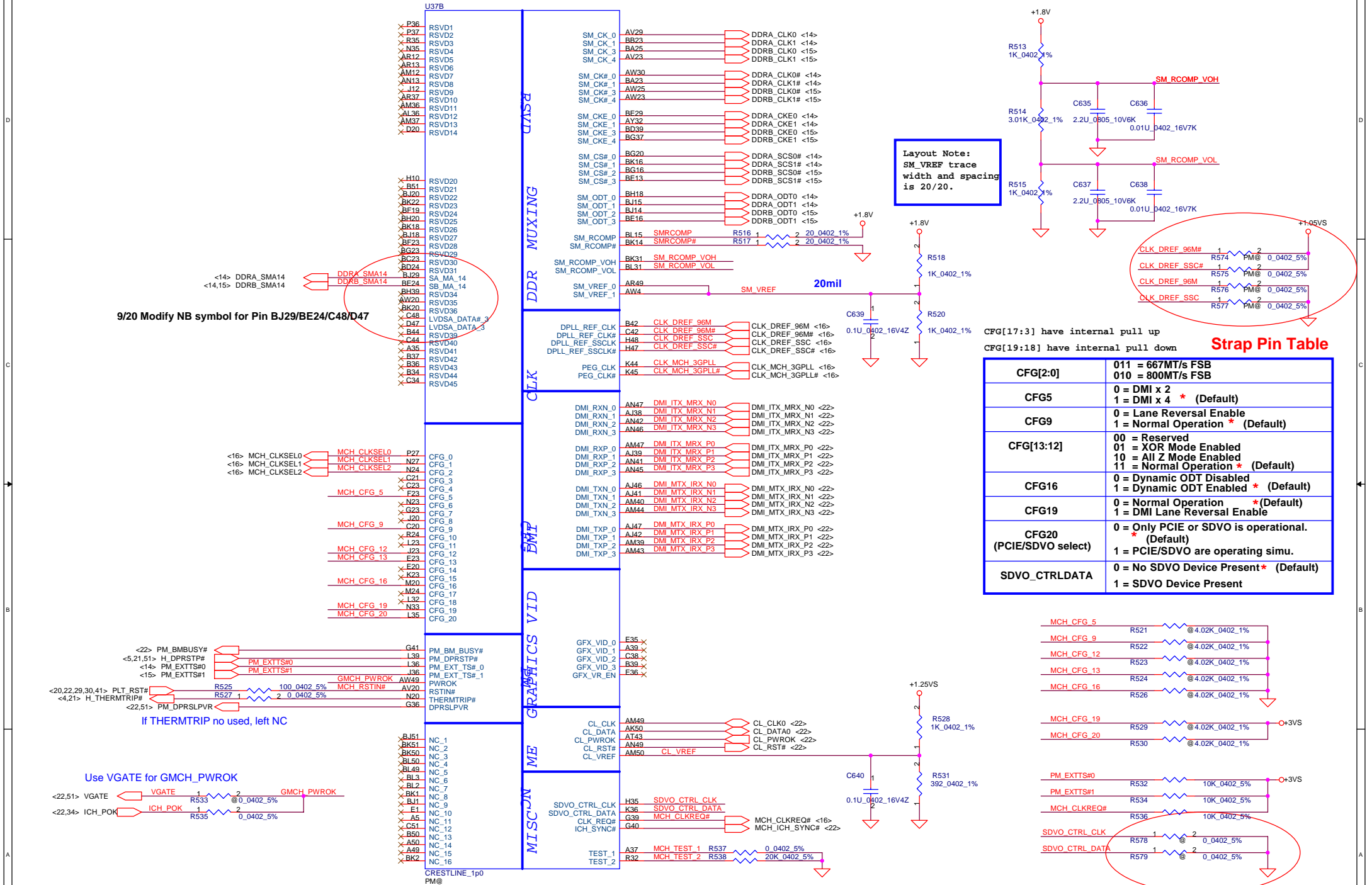


**layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

within 100mil to Ball A9,B9

**Layout Note:**  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

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<14> DDRA\_SDQ[0..63] DDRA\_SDQ[0..63]

<14> DDRA\_SDM[0..7] DDRA\_SDM[0..7]

<14> DDRA\_SMA[0..13] DDRA\_SMA[0..13]

<15> DDRB\_SDQ[0..63] DDRB\_SDQ[0..63]

<15> DDRB\_SDM[0..7] DDRB\_SDM[0..7]

<15> DDRB\_SMA[0..13] DDRB\_SMA[0..13]

U37D

DDRA\_SDQ0 AR43 SA\_DQ\_0

DDRA\_SDQ1 AW44 SA\_DQ\_1

DDRA\_SDQ2 BA45 SA\_DQ\_2

DDRA\_SDQ3 AY46 SA\_DQ\_3

DDRA\_SDQ4 AR45 SA\_DQ\_4

DDRA\_SDQ5 AR45 SA\_DQ\_5

DDRA\_SDQ6 AT42 SA\_DQ\_6

DDRA\_SDQ7 AW47 SA\_DM\_7

DDRA\_SDQ8 BB45 SA\_DQ\_8

DDRA\_SDQ9 BF48 SA\_DQ\_9

DDRA\_SDQ10 BG47 SA\_DQ\_10

DDRA\_SDQ11 BH47 SA\_DQ\_11

DDRA\_SDQ12 BB47 SA\_DQ\_12

DDRA\_SDQ13 BG50 SA\_DQ\_13

DDRA\_SDQ14 BH49 SA\_DQ\_14

DDRA\_SDQ15 BE45 SA\_DQ\_15

DDRA\_SDQ16 AW43 SA\_DQ\_16

DDRA\_SDQ17 BE44 SA\_DQ\_17

DDRA\_SDQ18 BG42 SA\_DQ\_18

DDRA\_SDQ19 BE40 SA\_DQ\_19

DDRA\_SDQ20 BF44 SA\_DQ\_20

DDRA\_SDQ21 BH45 SA\_DQ\_21

DDRA\_SDQ22 BG40 SA\_DQ\_22

DDRA\_SDQ23 BF40 SA\_DQ\_23

DDRA\_SDQ24 AR40 SA\_DQ\_24

DDRA\_SDQ25 AW40 SA\_DQ\_25

DDRA\_SDQ26 AT39 SA\_DQ\_26

DDRA\_SDQ27 AW36 SA\_DQ\_27

DDRA\_SDQ28 AW41 SA\_DQ\_28

DDRA\_SDQ29 AY41 SA\_DQ\_29

DDRA\_SDQ30 AV38 SA\_DQ\_30

DDRA\_SDQ31 AT38 SA\_DQ\_31

DDRA\_SDQ32 AV13 SA\_DQ\_32

DDRA\_SDQ33 AT13 SA\_DQ\_33

DDRA\_SDQ34 AW11 SA\_DQ\_34

DDRA\_SDQ35 AV11 SA\_DQ\_35

DDRA\_SDQ36 AU15 SA\_DQ\_36

DDRA\_SDQ37 AT11 SA\_DQ\_37

DDRA\_SDQ38 BA13 SA\_DQ\_38

DDRA\_SDQ39 BA11 SA\_DQ\_39

DDRA\_SDQ40 BE10 SA\_DQ\_40

DDRA\_SDQ41 BD10 SA\_DQ\_41

DDRA\_SDQ42 BD8 SA\_DQ\_42

DDRA\_SDQ43 AY9 SA\_DQ\_43

DDRA\_SDQ44 BG10 SA\_DQ\_44

DDRA\_SDQ45 AW9 SA\_DQ\_45

DDRA\_SDQ46 BD7 SA\_DQ\_46

DDRA\_SDQ47 BB9 SA\_DQ\_47

DDRA\_SDQ48 BB5 SA\_DQ\_48

DDRA\_SDQ49 AY7 SA\_DQ\_49

DDRA\_SDQ50 AT5 SA\_DQ\_50

DDRA\_SDQ51 AT7 SA\_DQ\_51

DDRA\_SDQ52 AY6 SA\_DQ\_52

DDRA\_SDQ53 BB7 SA\_DQ\_53

DDRA\_SDQ54 AR5 SA\_DQ\_54

DDRA\_SDQ55 AR8 SA\_DQ\_55

DDRA\_SDQ56 AR9 SA\_DQ\_56

DDRA\_SDQ57 AN3 SA\_DQ\_57

DDRA\_SDQ58 AM8 SA\_DQ\_58

DDRA\_SDQ59 AN10 SA\_DQ\_59

DDRA\_SDQ60 AT9 SA\_DQ\_60

DDRA\_SDQ61 AN9 SA\_DQ\_61

DDRA\_SDQ62 AM9 SA\_DQ\_62

DDRA\_SDQ63 AN11 SA\_DQ\_63

DDR SYSTEM MEMORY A

SA\_BS\_0 BB19 DDRA\_SBS0 <14>

SA\_BS\_1 BK19 DDRA\_SBS1 <14>

SA\_BS\_2 BF29 DDRA\_SBS2 <14>

SA\_CAS# BL17 DDRA\_SCAS# <14>

SA\_DM\_0 AT45 DDRA\_SDM0

SA\_DM\_1 BD44 DDRA\_SDM1

SA\_DM\_2 DD42 DDRA\_SDM2

SA\_DM\_3 AW38 DDRA\_SDM3

SA\_DM\_4 AW13 DDRA\_SDM4

SA\_DM\_5 BG8 DDRA\_SDM5

SA\_DM\_6 AV5 DDRA\_SDM6

SA\_DM\_7 AN6 DDRA\_SDM7

SA\_DQS\_0 AT46 DDRA\_SDQS0 DDRA\_SDQS0 <14>

SA\_DQS\_1 BE48 DDRA\_SDQS1 DDRA\_SDQS1 <14>

SA\_DQS\_2 BB43 DDRA\_SDQS2 DDRA\_SDQS2 <14>

SA\_DQS\_3 BC37 DDRA\_SDQS3 DDRA\_SDQS3 <14>

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SA\_DQS\_5 BH6 DDRA\_SDQS5 DDRA\_SDQS5 <14>

SA\_DQS\_6 BB2 DDRA\_SDQS6 DDRA\_SDQS6 <14>

SA\_DQS\_7 AP3 DDRA\_SDQS7 DDRA\_SDQS7 <14>

SA\_DQS#\_0 AT47 DDRA\_SDQS#0 DDRA\_SDQS#0 <14>

SA\_DQS#\_1 BC41 DDRA\_SDQS#1 DDRA\_SDQS#1 <14>

SA\_DQS#\_2 BA37 DDRA\_SDQS#2 DDRA\_SDQS#2 <14>

SA\_DQS#\_3 BA16 DDRA\_SDQS#3 DDRA\_SDQS#3 <14>

SA\_DQS#\_4 BH7 DDRA\_SDQS#4 DDRA\_SDQS#4 <14>

SA\_DQS#\_5 BC1 DDRA\_SDQS#5 DDRA\_SDQS#5 <14>

SA\_DQS#\_6 AP2 DDRA\_SDQS#6 DDRA\_SDQS#6 <14>

SA\_DQS#\_7 AP2 DDRA\_SDQS#7 DDRA\_SDQS#7 <14>

SA\_MA\_0 BJ19 DDRA\_SMA0

SA\_MA\_1 BD20 DDRA\_SMA1

SA\_MA\_2 BK27 DDRA\_SMA2

SA\_MA\_3 BH28 DDRA\_SMA3

SA\_MA\_4 BL24 DDRA\_SMA4

SA\_MA\_5 BK28 DDRA\_SMA5

SA\_MA\_6 BJ27 DDRA\_SMA6

SA\_MA\_7 BJ25 DDRA\_SMA7

SA\_MA\_8 BL28 DDRA\_SMA8

SA\_MA\_9 BA28 DDRA\_SMA9

SA\_MA\_10 BC19 DDRA\_SMA10

SA\_MA\_11 BE28 DDRA\_SMA11

SA\_MA\_12 BC30 DDRA\_SMA12

SA\_MA\_13 BJ16 DDRA\_SMA13

SA\_RAS# BE18 DDRA\_SRAS# <14>

SA\_RCVEN# AY20 SA\_RCVEN# PAD T18

SA\_WE# BA19 DDRA\_SWE# <14>

CRESTLINE\_1p0  
PM@

U37E

DDRB\_SDQ0 AP49 SB\_DQ\_0

DDRB\_SDQ1 AR51 SB\_DQ\_1

DDRB\_SDQ2 AW50 SB\_DQ\_2

DDRB\_SDQ3 AW51 SB\_DQ\_3

DDRB\_SDQ4 AN51 SB\_DQ\_4

DDRB\_SDQ5 AN50 SB\_DQ\_5

DDRB\_SDQ6 AV50 SB\_DQ\_6

DDRB\_SDQ7 AV49 SB\_DQ\_7

DDRB\_SDQ8 BA50 SB\_DQ\_8

DDRB\_SDQ9 BB50 SB\_DQ\_9

DDRB\_SDQ10 BA49 SB\_DQ\_10

DDRB\_SDQ11 BE50 SB\_DQ\_11

DDRB\_SDQ12 BA51 SB\_DQ\_12

DDRB\_SDQ13 AY49 SB\_DQ\_13

DDRB\_SDQ14 BF50 SB\_DQ\_14

DDRB\_SDQ15 BF49 SB\_DQ\_15

DDRB\_SDQ16 BJ50 SB\_DQ\_16

DDRB\_SDQ17 BJ44 SB\_DQ\_17

DDRB\_SDQ18 BJ43 SB\_DQ\_18

DDRB\_SDQ19 BL43 SB\_DQ\_19

DDRB\_SDQ20 BK47 SB\_DQ\_20

DDRB\_SDQ21 BK49 SB\_DQ\_21

DDRB\_SDQ22 BK43 SB\_DQ\_22

DDRB\_SDQ23 BK42 SB\_DQ\_23

DDRB\_SDQ24 BJ41 SB\_DQ\_24

DDRB\_SDQ25 BL41 SB\_DQ\_25

DDRB\_SDQ26 BJ37 SB\_DQ\_26

DDRB\_SDQ27 BJ36 SB\_DQ\_27

DDRB\_SDQ28 BK41 SB\_DQ\_28

DDRB\_SDQ29 BJ40 SB\_DQ\_29

DDRB\_SDQ30 BL36 SB\_DQ\_30

DDRB\_SDQ31 BK37 SB\_DQ\_31

DDRB\_SDQ32 BK13 SB\_DQ\_32

DDRB\_SDQ33 BE11 SB\_DQ\_33

DDRB\_SDQ34 BK11 SB\_DQ\_34

DDRB\_SDQ35 BC11 SB\_DQ\_35

DDRB\_SDQ36 BC13 SB\_DQ\_36

DDRB\_SDQ37 BF12 SB\_DQ\_37

DDRB\_SDQ38 BC12 SB\_DQ\_38

DDRB\_SDQ39 BG12 SB\_DQ\_39

DDRB\_SDQ40 BJ10 SB\_DQ\_40

DDRB\_SDQ41 BL9 SB\_DQ\_41

DDRB\_SDQ42 BK5 SB\_DQ\_42

DDRB\_SDQ43 BL5 SB\_DQ\_43

DDRB\_SDQ44 BK9 SB\_DQ\_44

DDRB\_SDQ45 BK10 SB\_DQ\_45

DDRB\_SDQ46 BJ8 SB\_DQ\_46

DDRB\_SDQ47 BJ6 SB\_DQ\_47

DDRB\_SDQ48 BF4 SB\_DQ\_48

DDRB\_SDQ49 BH5 SB\_DQ\_49

DDRB\_SDQ50 BG1 SB\_DQ\_50

DDRB\_SDQ51 BC2 SB\_DQ\_51

DDRB\_SDQ52 BK3 SB\_DQ\_52

DDRB\_SDQ53 BE4 SB\_DQ\_53

DDRB\_SDQ54 BD3 SB\_DQ\_54

DDRB\_SDQ55 BJ2 SB\_DQ\_55

DDRB\_SDQ56 BA3 SB\_DQ\_56

DDRB\_SDQ57 BC3 SB\_DQ\_57

DDRB\_SDQ58 AR1 SB\_DQ\_58

DDRB\_SDQ59 AT3 SB\_DQ\_59

DDRB\_SDQ60 AY2 SB\_DQ\_60

DDRB\_SDQ61 AY3 SB\_DQ\_61

DDRB\_SDQ62 AU2 SB\_DQ\_62

DDRB\_SDQ63 AT2 SB\_DQ\_63

DDR SYSTEM MEMORY B

SB\_BS\_0 AY17 DDRB\_SBS0 <15>

SB\_BS\_1 BG18 DDRB\_SBS1 <15>

SB\_BS\_2 BG36 DDRB\_SBS2 <15>

SB\_CAS# BE17 DDRB\_SCAS# <15>

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SB\_DM\_1 BD49 DDRB\_SDM1

SB\_DM\_2 BK45 DDRB\_SDM2

SB\_DM\_3 BL39 DDRB\_SDM3

SB\_DM\_4 BH17 DDRB\_SDM4

SB\_DM\_5 BE3 DDRB\_SDM5

SB\_DM\_6 BE3 DDRB\_SDM6

SB\_DM\_7 AW2 DDRB\_SDM7

SB\_DQS\_0 AT50 DDRB\_SDQS0 DDRB\_SDQS0 <15>

SB\_DQS\_1 BD50 DDRB\_SDQS1 DDRB\_SDQS1 <15>

SB\_DQS\_2 BK46 DDRB\_SDQS2 DDRB\_SDQS2 <15>

SB\_DQS\_3 BK39 DDRB\_SDQS3 DDRB\_SDQS3 <15>

SB\_DQS\_4 BJ12 DDRB\_SDQS4 DDRB\_SDQS4 <15>

SB\_DQS\_5 BL7 DDRB\_SDQS5 DDRB\_SDQS5 <15>

SB\_DQS\_6 BE2 DDRB\_SDQS6 DDRB\_SDQS6 <15>

SB\_DQS\_7 AV2 DDRB\_SDQS7 DDRB\_SDQS7 <15>

SB\_DQS#\_0 AU50 DDRB\_SDQS#0 DDRB\_SDQS#0 <15>

SB\_DQS#\_1 BC50 DDRB\_SDQS#1 DDRB\_SDQS#1 <15>

SB\_DQS#\_2 BL45 DDRB\_SDQS#2 DDRB\_SDQS#2 <15>

SB\_DQS#\_3 BK38 DDRB\_SDQS#3 DDRB\_SDQS#3 <15>

SB\_DQS#\_4 BK12 DDRB\_SDQS#4 DDRB\_SDQS#4 <15>

SB\_DQS#\_5 BK7 DDRB\_SDQS#5 DDRB\_SDQS#5 <15>

SB\_DQS#\_6 BF2 DDRB\_SDQS#6 DDRB\_SDQS#6 <15>

SB\_DQS#\_7 AV3 DDRB\_SDQS#7 DDRB\_SDQS#7 <15>

SB\_MA\_0 BC18 DDRB\_SMA0

SB\_MA\_1 BG28 DDRB\_SMA1

SB\_MA\_2 BG25 DDRB\_SMA2

SB\_MA\_3 AW17 DDRB\_SMA3

SB\_MA\_4 BE25 DDRB\_SMA4

SB\_MA\_5 BE25 DDRB\_SMA5

SB\_MA\_6 BA29 DDRB\_SMA6

SB\_MA\_7 BC28 DDRB\_SMA7

SB\_MA\_8 AY28 DDRB\_SMA8

SB\_MA\_9 BD37 DDRB\_SMA9

SB\_MA\_10 BG17 DDRB\_SMA10

SB\_MA\_11 BE37 DDRB\_SMA11

SB\_MA\_12 BA39 DDRB\_SMA12

SB\_MA\_13 BG13 DDRB\_SMA13

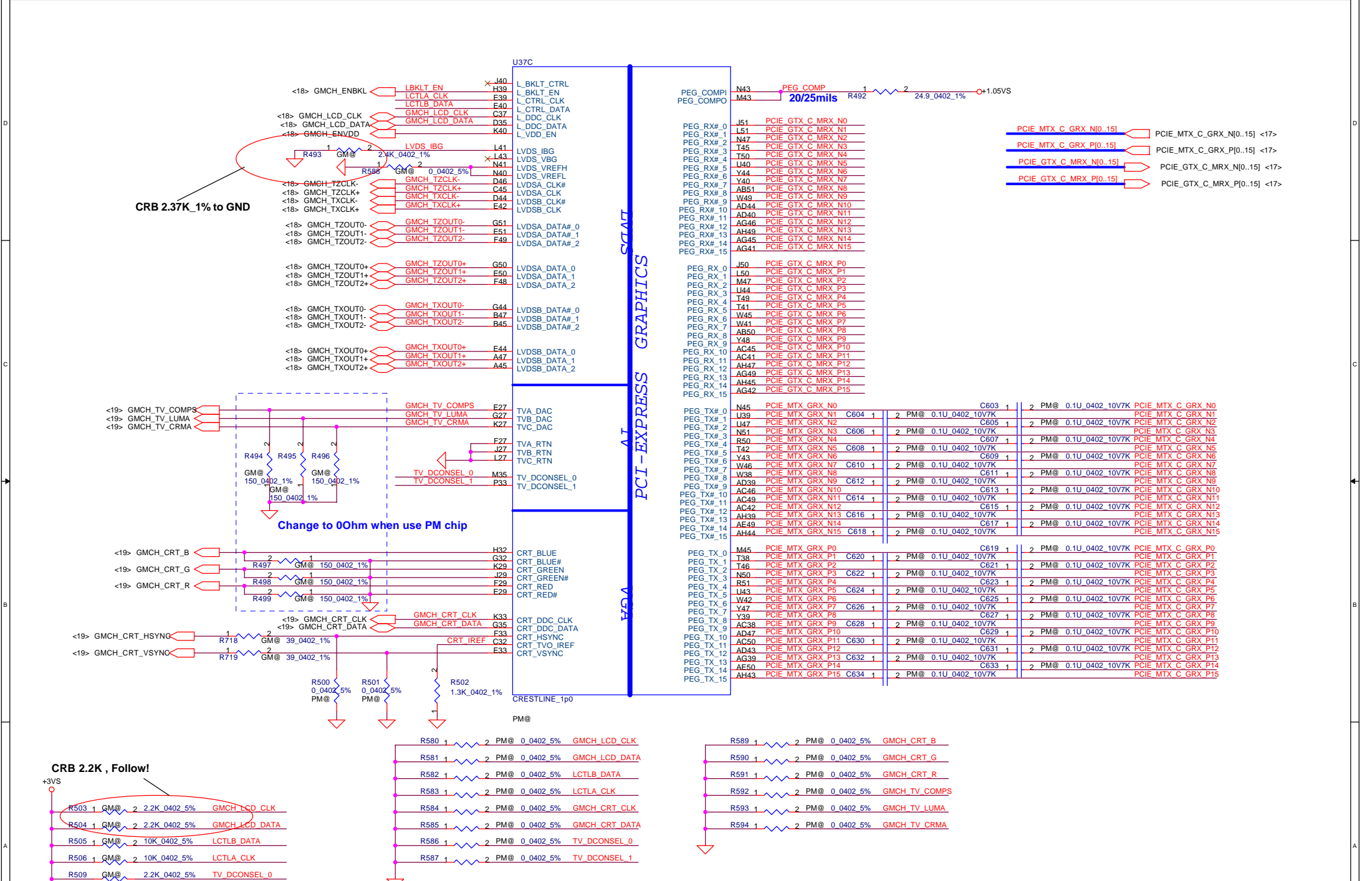
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SB\_RCVEN# AY18 SB\_RCVEN# PAD T17

SB\_WE# BC17 DDRB\_SWE# <15>

CRESTLINE\_1p0  
PM@

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Crestline (3/7)-DDR II
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Size B	Document Number	Date:		Rev 0
	IFTXX M/B LA-3541P Schematic	Wednesday, November 01, 2006		Sheet 9 of 52



PEG\_COMP1 N43 PEG COMP 1 24.9\_0402\_1% +1.05VS

- PCIE\_MTX\_C\_GRX\_N0[.15] <17>
- PCIE\_MTX\_C\_GRX\_P0[.15] <17>
- PCIE GTX C\_MRX\_N0[.15] <17>
- PCIE GTX\_C\_MRX\_P0[.15] <17>

- J51 PCIE GTX C\_MRX\_N0
- L51 PCIE GTX C\_MRX\_N1
- N47 PCIE GTX C\_MRX\_N2
- T45 PCIE GTX C\_MRX\_N3
- T50 PCIE GTX C\_MRX\_N4
- U40 PCIE GTX C\_MRX\_N5
- Y44 PCIE GTX C\_MRX\_N6
- Y40 PCIE GTX C\_MRX\_N7
- Y40 PCIE GTX C\_MRX\_N8
- AB51 PCIE GTX C\_MRX\_N9
- PEG\_RX#\_9
- AD44 PCIE GTX C\_MRX\_N10
- AD40 PCIE GTX C\_MRX\_N11
- AG46 PCIE GTX C\_MRX\_N12
- AG49 PCIE GTX C\_MRX\_N13
- AG45 PCIE GTX C\_MRX\_N14
- AG41 PCIE GTX C\_MRX\_N15

- PEG\_RX\_0
- PEG\_RX\_1
- PEG\_RX\_2
- PEG\_RX\_3
- PEG\_RX\_4
- PEG\_RX\_5
- PEG\_RX\_6
- PEG\_RX\_7
- PEG\_RX\_8
- PEG\_RX\_9
- PEG\_RX\_10
- PEG\_RX\_11
- PEG\_RX\_12
- PEG\_RX\_13
- PEG\_RX\_14
- PEG\_RX\_15

- N45 PCIE MTX GRX N0 C603 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N0
- L39 PCIE MTX GRX N1 C604 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N1
- L47 PCIE MTX GRX N2 C605 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N2
- N51 PCIE MTX GRX N3 C606 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N3
- R50 PCIE MTX GRX N4 C607 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N4
- T42 PCIE MTX GRX N5 C608 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N5
- Y43 PCIE MTX GRX N6 C609 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N6
- W46 PCIE MTX GRX N7 C610 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N7
- W38 PCIE MTX GRX N8 C611 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N8
- AD39 PCIE MTX GRX N9 C612 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N9
- AC46 PCIE MTX GRX N10 C613 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N10
- AC49 PCIE MTX GRX N11 C614 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N11
- AC42 PCIE MTX GRX N12 C615 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N12
- AH39 PCIE MTX GRX N13 C616 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N13
- AE49 PCIE MTX GRX N14 C617 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N14
- AH44 PCIE MTX GRX N15 C618 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_N15

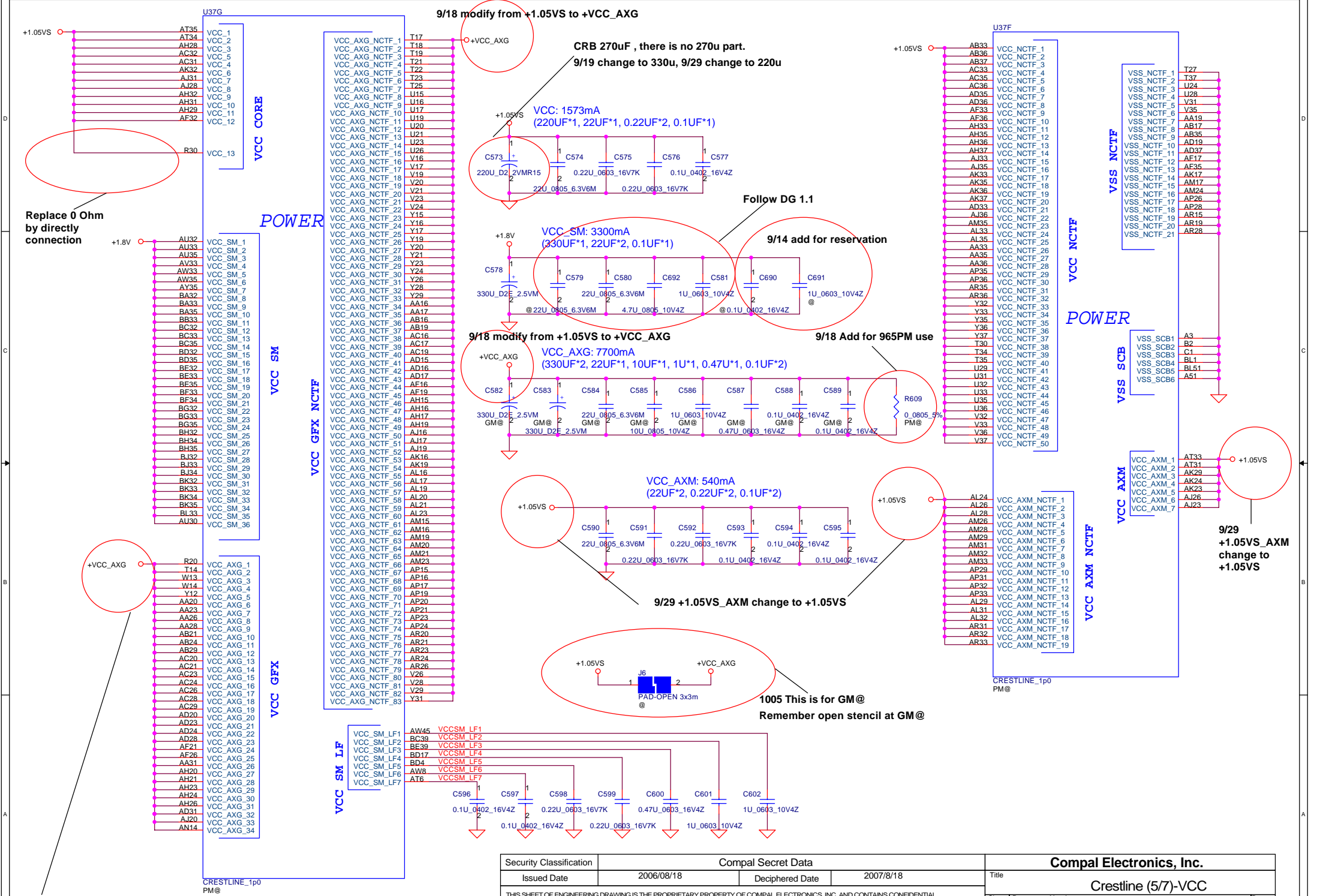
- M45 PCIE MTX GRX P0 C619 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P0
- T38 PCIE MTX GRX P1 C620 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P1
- T46 PCIE MTX GRX P2 C621 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P2
- N50 PCIE MTX GRX P3 C622 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P3
- R51 PCIE MTX GRX P4 C623 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P4
- L43 PCIE MTX GRX P5 C624 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P5
- W42 PCIE MTX GRX P6 C625 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P6
- Y47 PCIE MTX GRX P7 C626 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P7
- Y39 PCIE MTX GRX P8 C627 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P8
- AD38 PCIE MTX GRX P9 C628 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P9
- AD47 PCIE MTX GRX P10 C629 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P10
- AC50 PCIE MTX GRX P11 C630 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P11
- AD43 PCIE MTX GRX P12 C631 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P12
- AG39 PCIE MTX GRX P13 C632 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P13
- AE50 PCIE MTX GRX P14 C633 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P14
- AH43 PCIE MTX GRX P15 C634 1 2 PM@ 0.1U\_0402\_10V7K PCIE\_MTX\_C\_GRX\_P15

- CRB 2.2K , Follow!**
- K503 1 GM@ 2 2.2K 0402 5% GMCH\_LCD\_CLK
  - R504 1 GM@ 2 2.2K 0402 5% GMCH\_LCD\_DATA
  - R505 1 GM@ 2 10K 0402 5% LCTLB\_DATA
  - R506 1 GM@ 2 10K 0402 5% LCTLA\_CLK
  - R509 GM@ 2.2K 0402 5% TV\_DCONSEL\_0
  - R510 GM@ 2.2K 0402 5% TV\_DCONSEL\_1

- R580 1 2 PM@ 0.0402 5% GMCH\_LCD\_CLK
- R581 1 2 PM@ 0.0402 5% GMCH\_LCD\_DATA
- R582 1 2 PM@ 0.0402 5% LCTLB\_DATA
- R583 1 2 PM@ 0.0402 5% LCTLA\_CLK
- R584 1 2 PM@ 0.0402 5% GMCH\_CRT\_CLK
- R585 1 2 PM@ 0.0402 5% GMCH\_CRT\_DATA
- R586 1 2 PM@ 0.0402 5% TV\_DCONSEL\_0
- R587 1 2 PM@ 0.0402 5% TV\_DCONSEL\_1

- R589 1 2 PM@ 0.0402 5% GMCH\_CRT\_B
- R590 1 2 PM@ 0.0402 5% GMCH\_CRT\_G
- R591 1 2 PM@ 0.0402 5% GMCH\_CRT\_R
- R592 1 2 PM@ 0.0402 5% GMCH\_TV\_COMPS
- R593 1 2 PM@ 0.0402 5% GMCH\_TV\_LUMA
- R594 1 2 PM@ 0.0402 5% GMCH\_TV\_CRMA

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Size B	Document Number	IFTXX M/B LA-3541P Schematic		Rev 0
Date:	Wednesday, November 01, 2006	Sheet	10	of 52

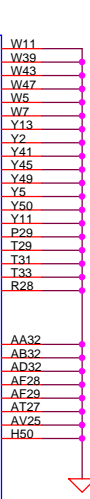
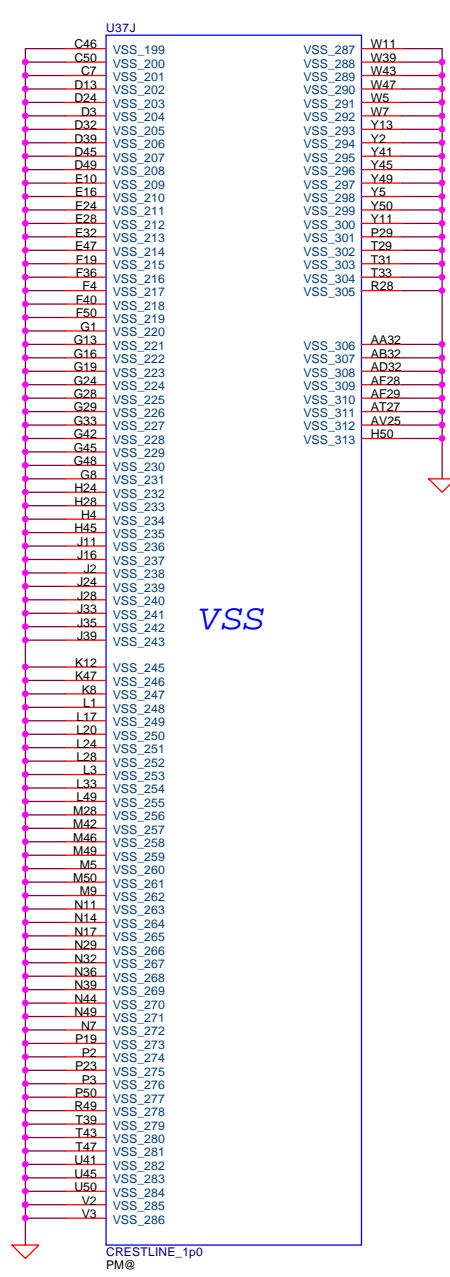
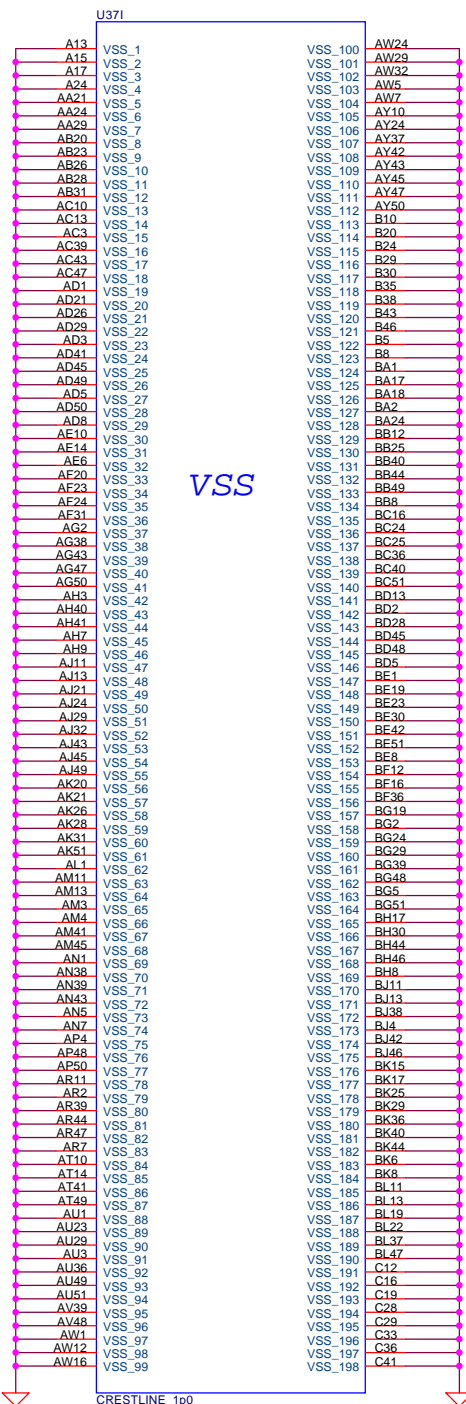


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Title	Crestline (5/7)-VCC			
Size	Document Number	IFTXX MB LA-3541P Schematic		Rev
B				0
Date:	Wednesday, November 01, 2006	Sheet	11	of 52

9/18 modify from +1.05VS to +VCC\_AXG

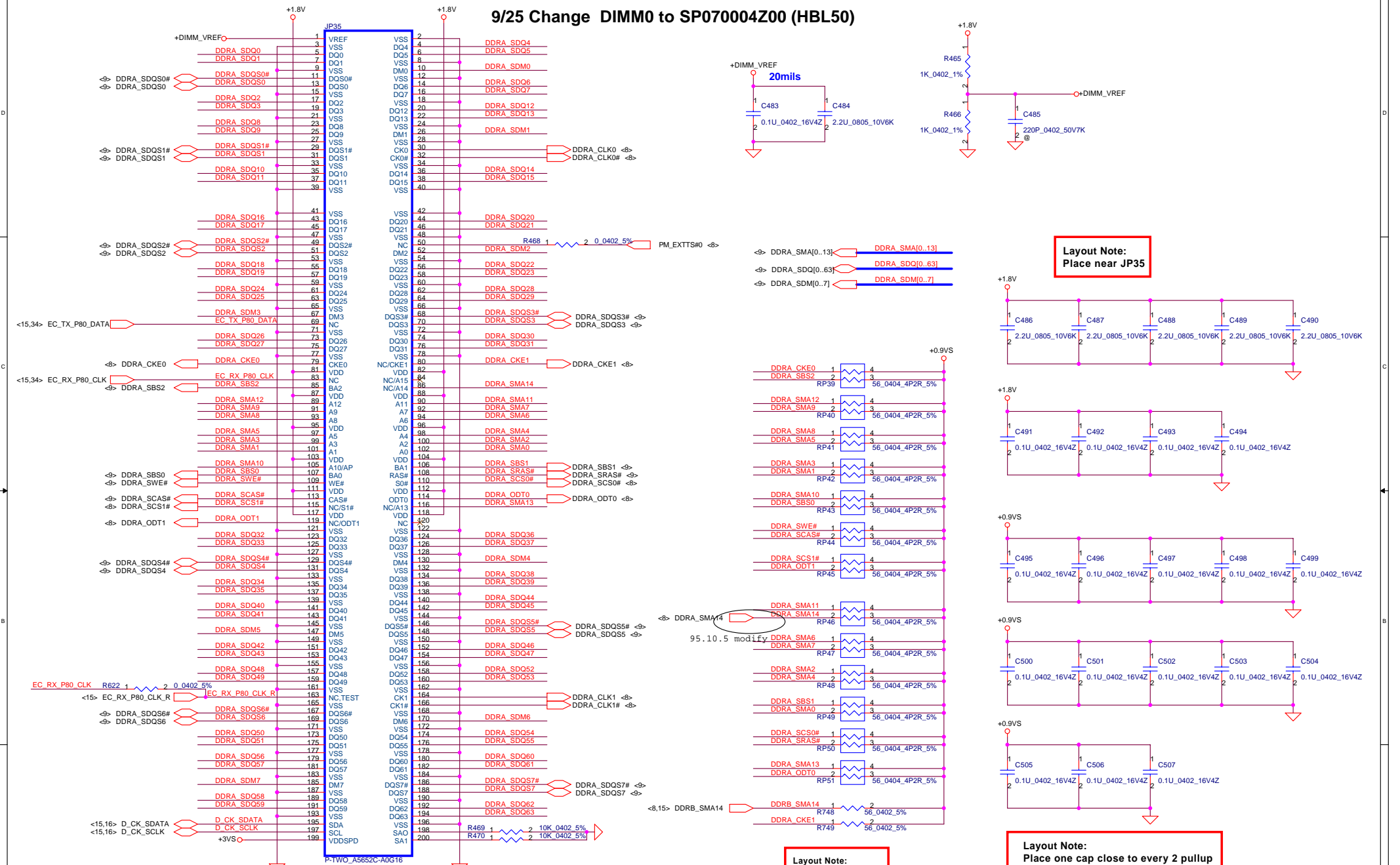
9/29 +1.05VS\_AXM change to +1.05VS





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Size B	Document Number	Rev 0		Date: Wednesday, November 01, 2006	
IFTXX M/B LA-3541P Schematic		Sheet 13 of 52		Date: Wednesday, November 01, 2006	

# 9/25 Change DIMM0 to SP070004Z00 (HBL50)



**Layout Note:**  
Place near JP35

**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

**Layout Note:**  
Place these resistor closely JP35, all trace length Max=1.5"

**DIMM0 STD H:5.2mm (BOT)**

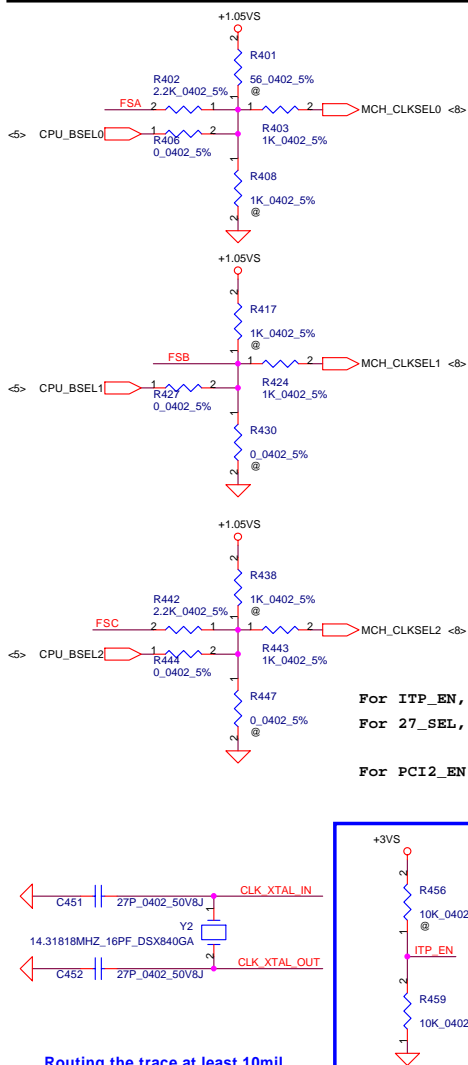
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	DDRII-SODIMMO	
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Date:	Wednesday, November 01, 2006	Sheet	14	of	52



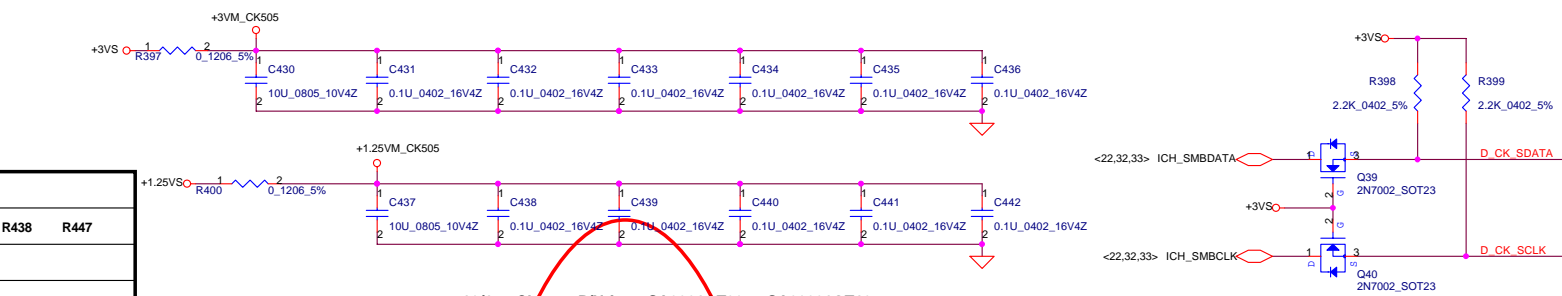
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

**FSB Frequency Selet:**

CPU Driven	Stuff	R401	R408	R417	R430	R438	R447
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447
	Stuff	R401	R417	R447			
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			

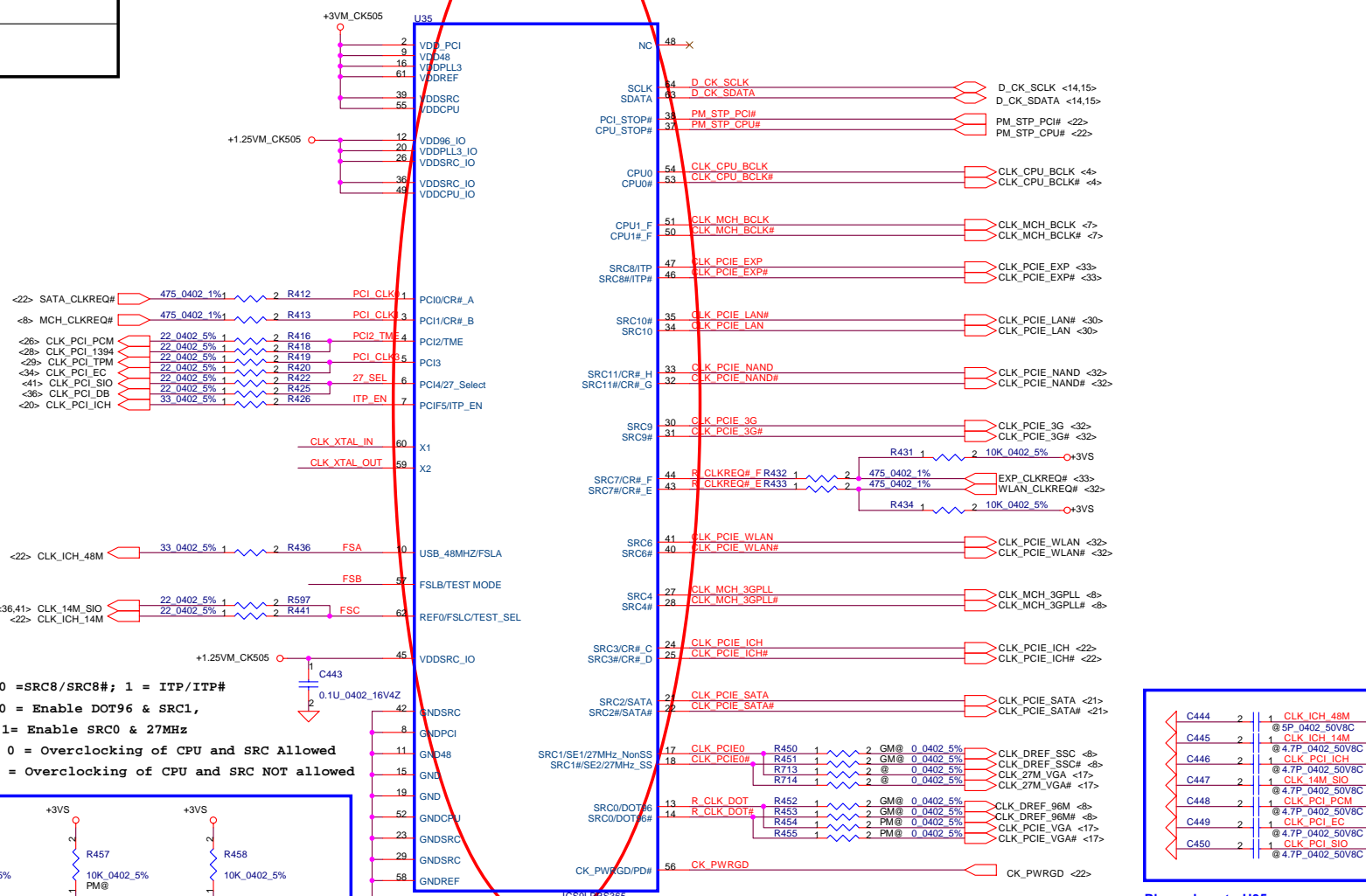


Routing the trace at least 10mil



10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol



C444	2	1	CLK_ICH_48M	@ 5P_0402_50V8C
C445	2	1	CLK_ICH_14M	@ 4.7P_0402_50V8C
C446	2	1	CLK_PCI_ICH	@ 4.7P_0402_50V8C
C447	2	1	CLK_14M_SIO	@ 4.7P_0402_50V8C
C448	2	1	CLK_PCI_PCM	@ 4.7P_0402_50V8C
C449	2	1	CLK_PCI_EC	@ 4.7P_0402_50V8C
C450	2	1	CLK_PCI_SIO	@ 4.7P_0402_50V8C

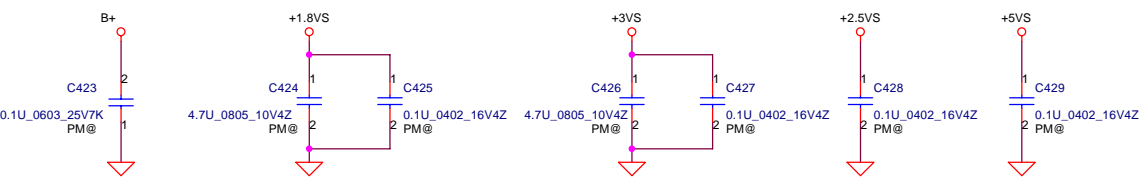
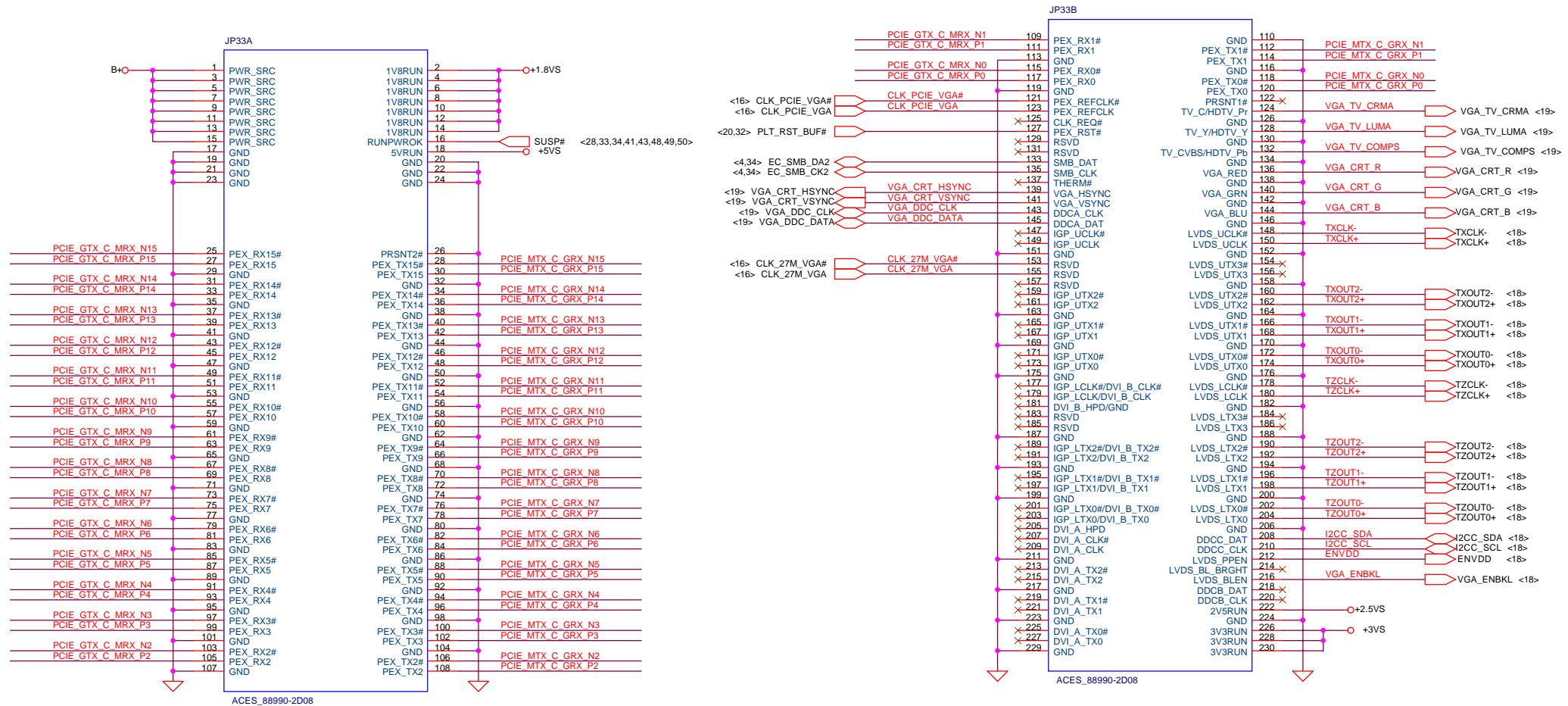
Place close to U35

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Date:	Wednesday, November 01, 2006	Sheet	16	of 52



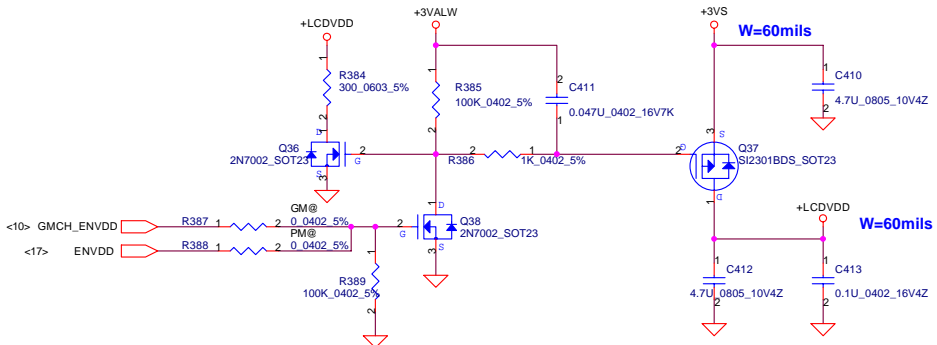
9/13 modify this footprint from ACES\_88990-2D08\_230P to ACES\_88990-2D28\_230P

- <10> PCIE\_MTX\_C\_GRX\_N[0..15] PCIE\_MTX\_C\_GRX\_N[0..15]
- <10> PCIE\_MTX\_C\_GRX\_P[0..15] PCIE\_MTX\_C\_GRX\_P[0..15]
- <10> PCIE\_GTX\_C\_MRX\_N[0..15] PCIE\_GTX\_C\_MRX\_N[0..15]
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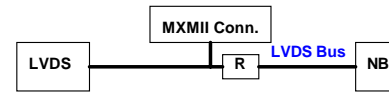


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Size	Document Number	Rev		
Custpm	IFTXX M/B LA-3541P Schematic	0		
Date:	Wednesday, November 01, 2006	Sheet	17	of 52

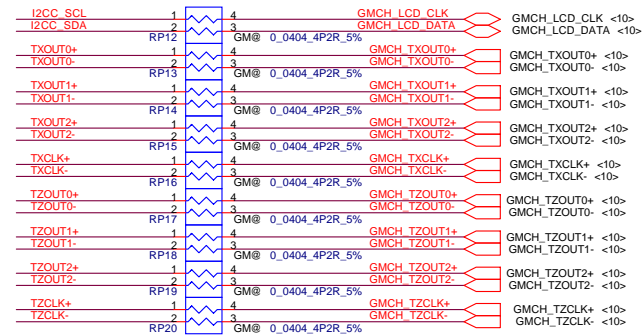
# LCD POWER CIRCUIT



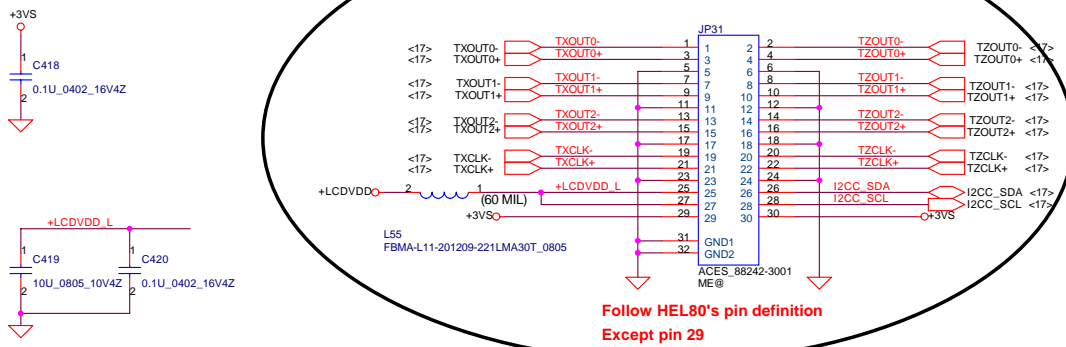
## Routing Diagram



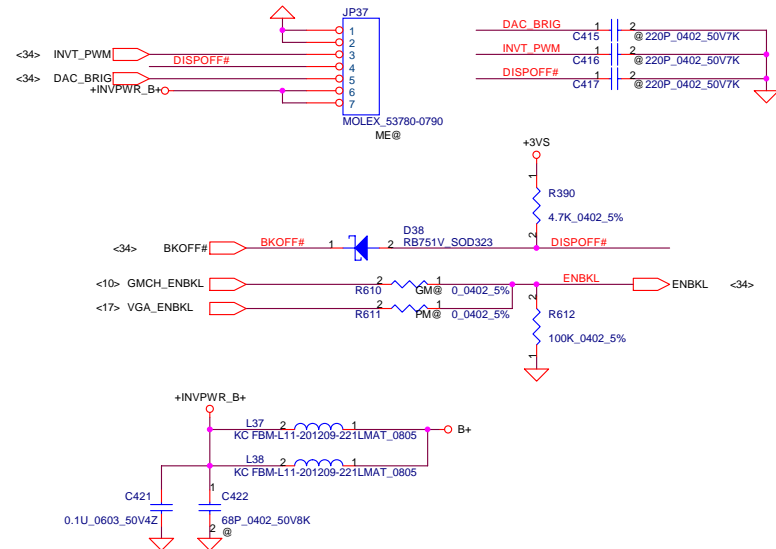
Use Daisy chain to route



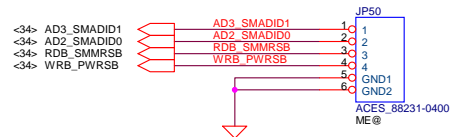
## LCD/PANEL BD. Conn.



## INVERTER Conn.

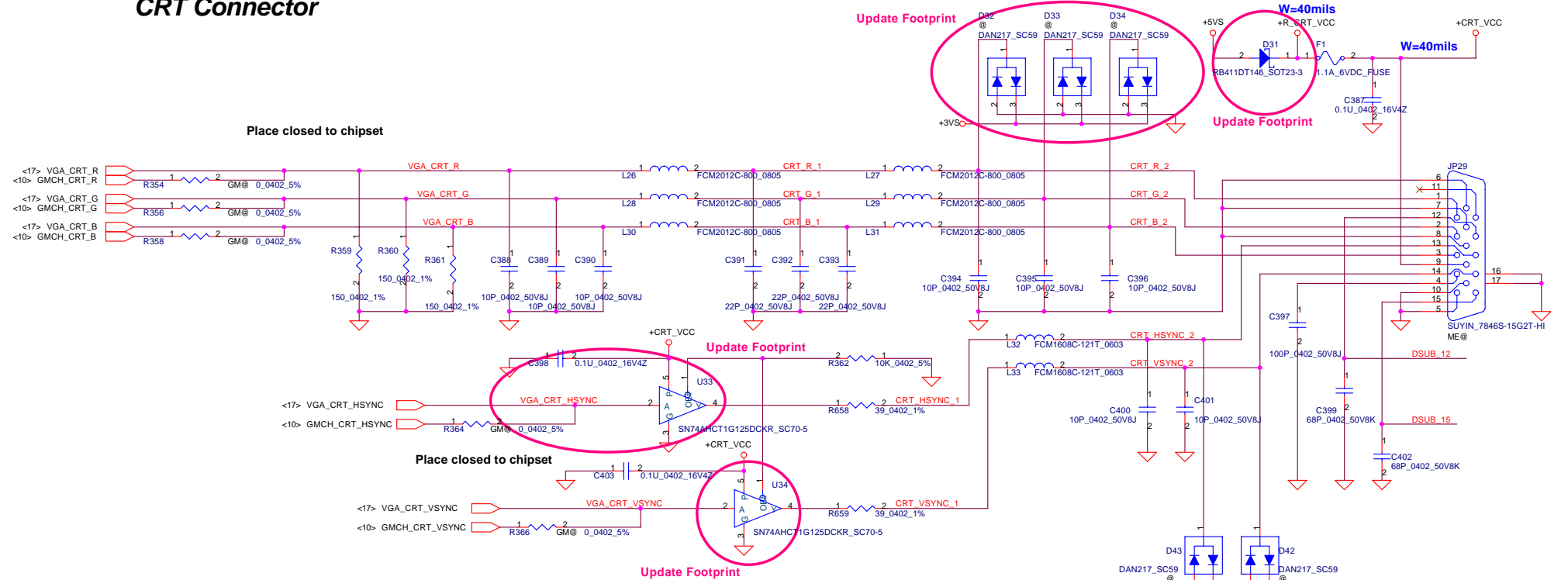


## JEPICO Conn.

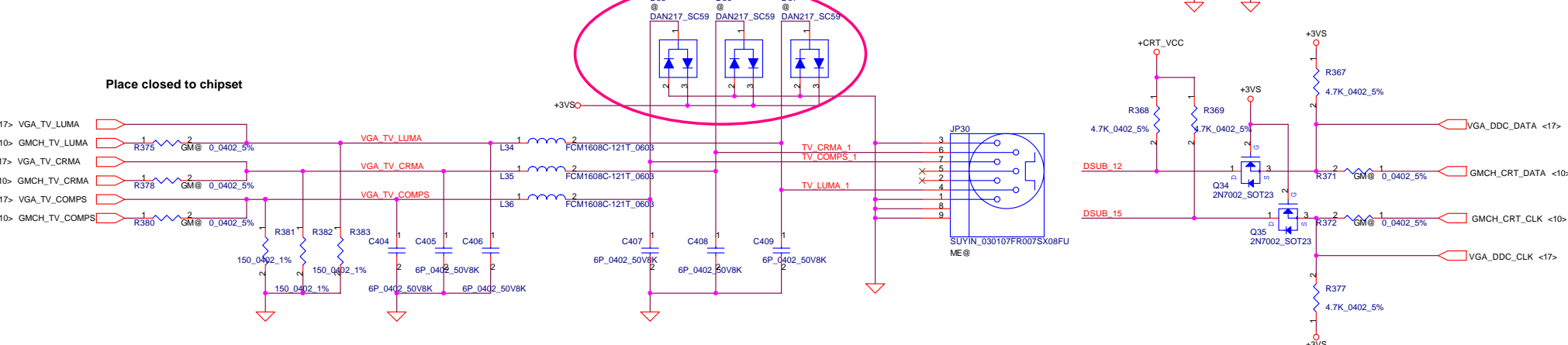


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			B	IFTXX/MB LA-3541P Schematic	0
			Date:	Wednesday, November 01, 2006	Sheet 18 of 52

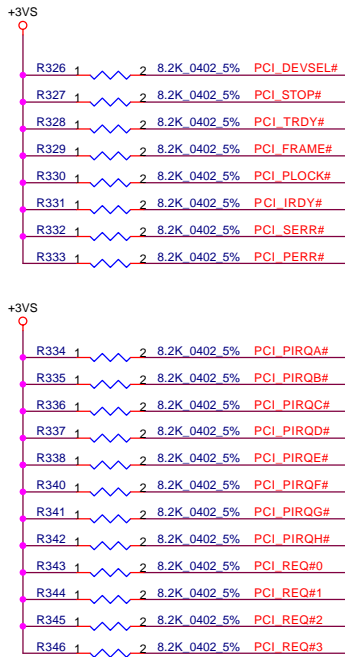
# CRT Connector



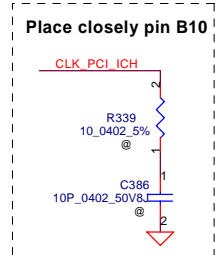
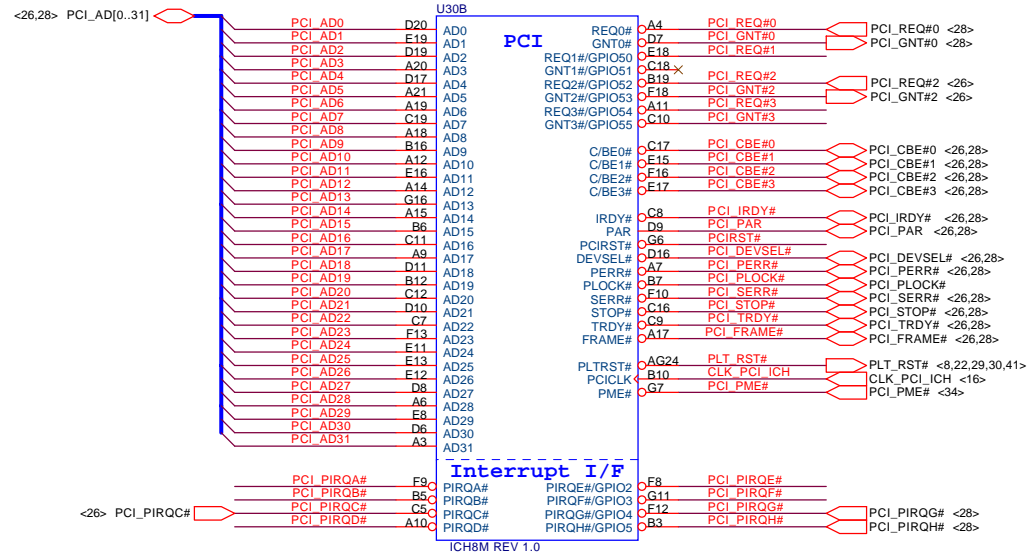
# TV-OUT Conn.



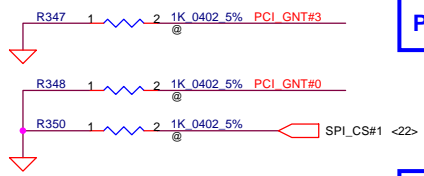
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	CRT & TV-OUT Connector
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Date: Wednesday, November 01, 2006				Sheet 19 of 52



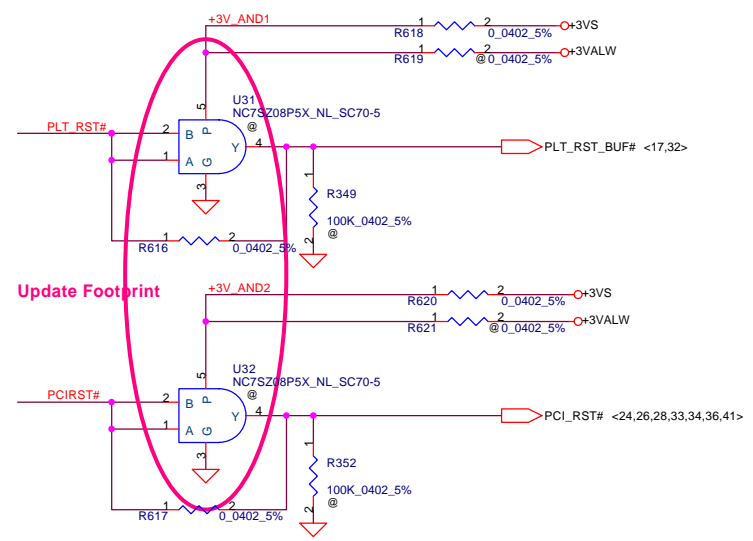
10/17 : Change P/N from SA000010G00 to SA00001JU10  
 10/17 : FootPrint : SA000010G00  
 BOM : SA00001JU10

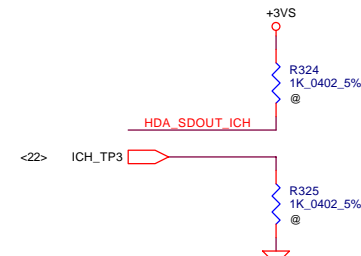
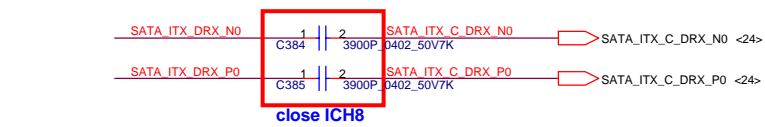
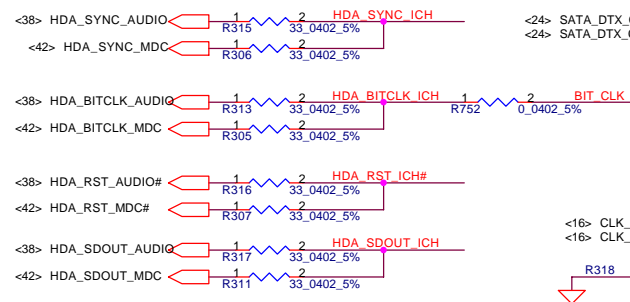
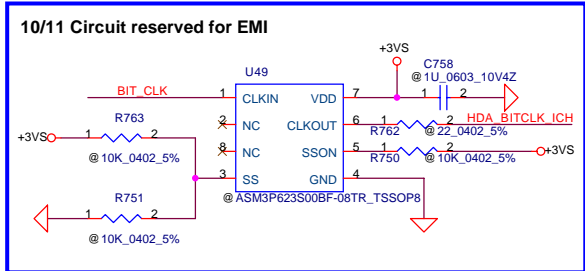
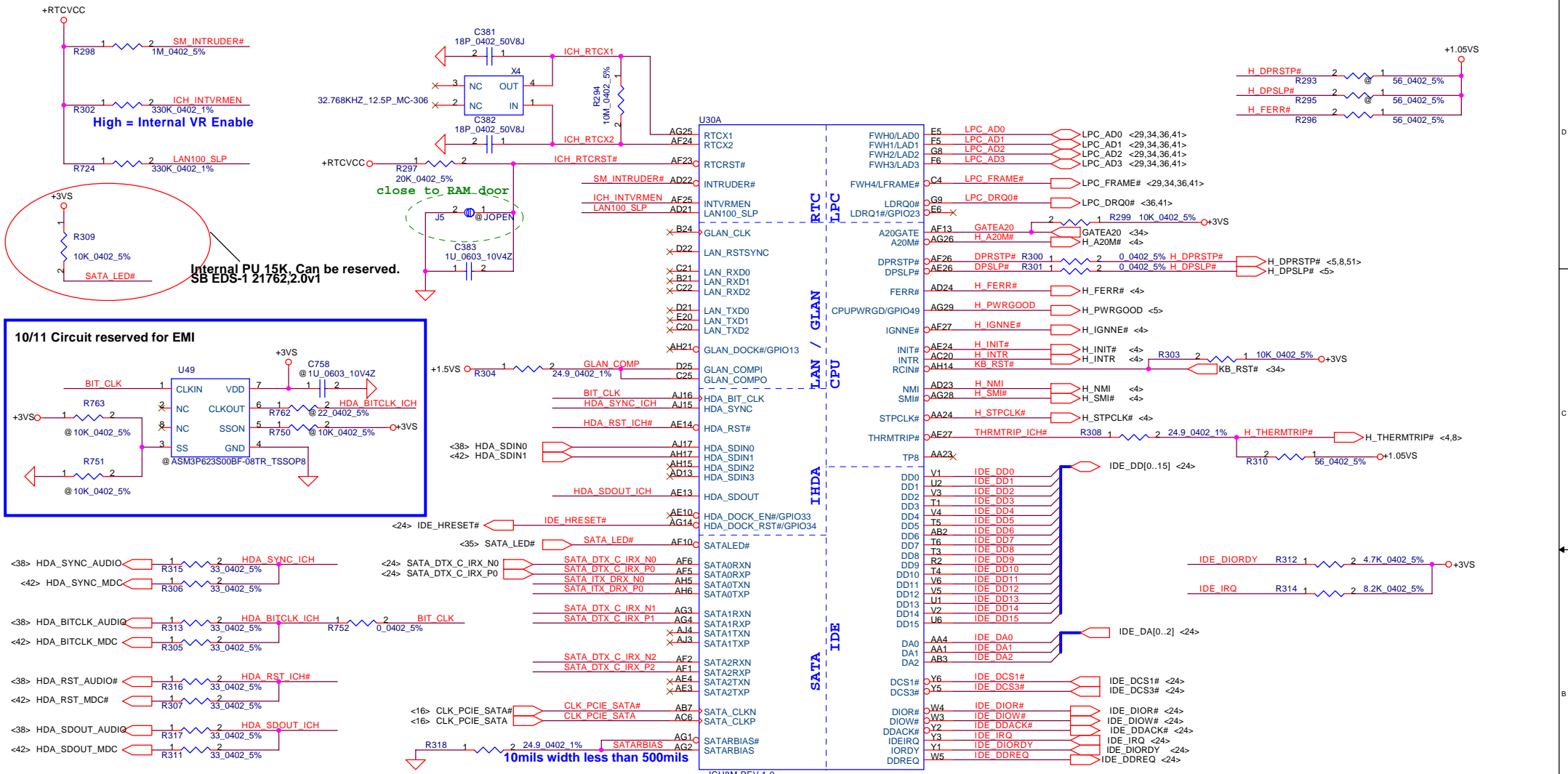


**A16 Swap Override Strap**  
 PCI\_GNT#3 Low= A16 swap override Enable  
 High= Default\*



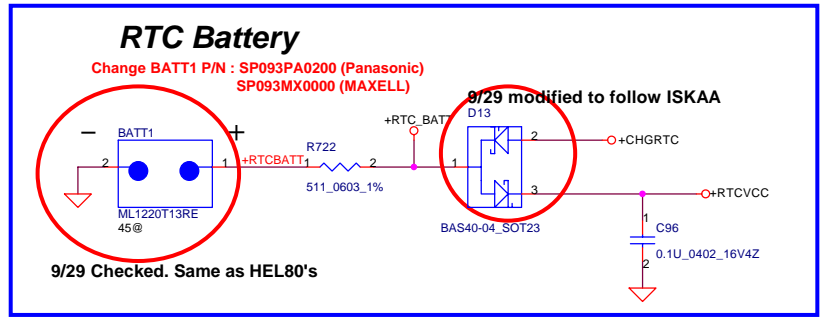
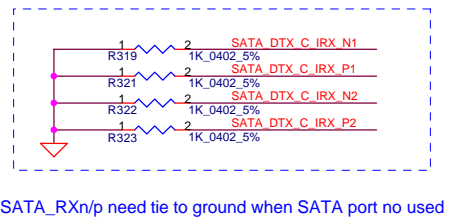
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

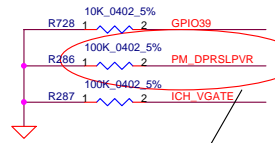
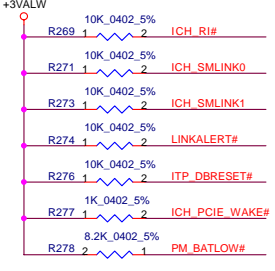
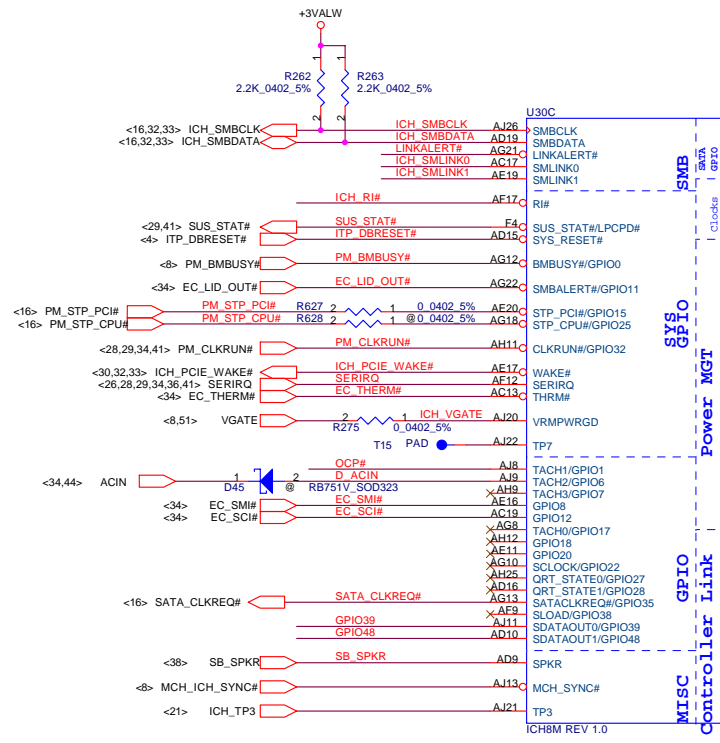
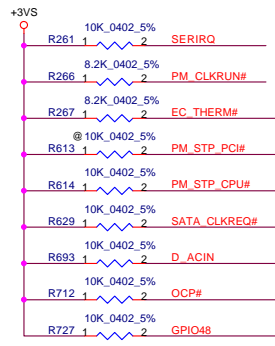




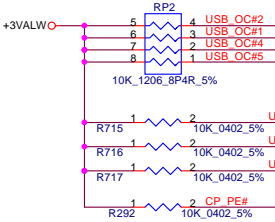
**XOR Chain Entrance Strap**

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1





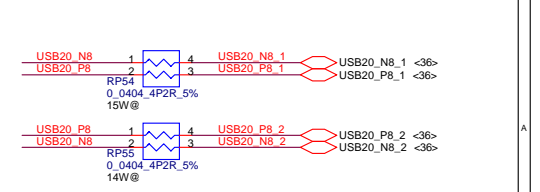
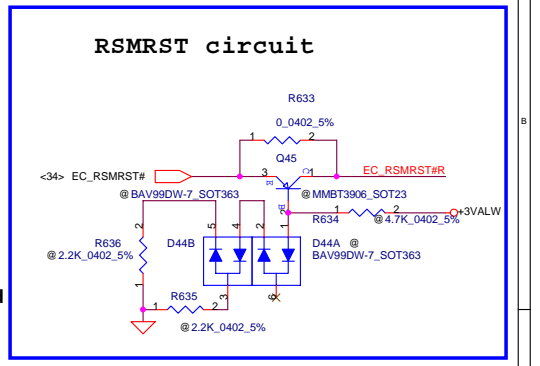
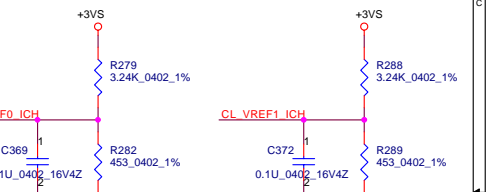
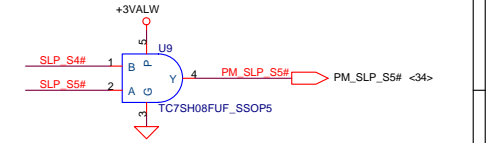
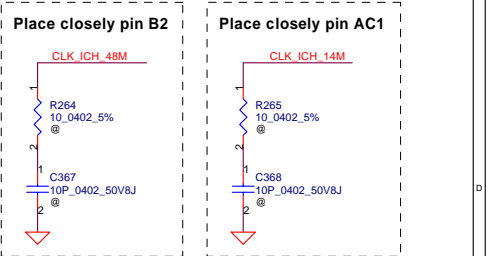
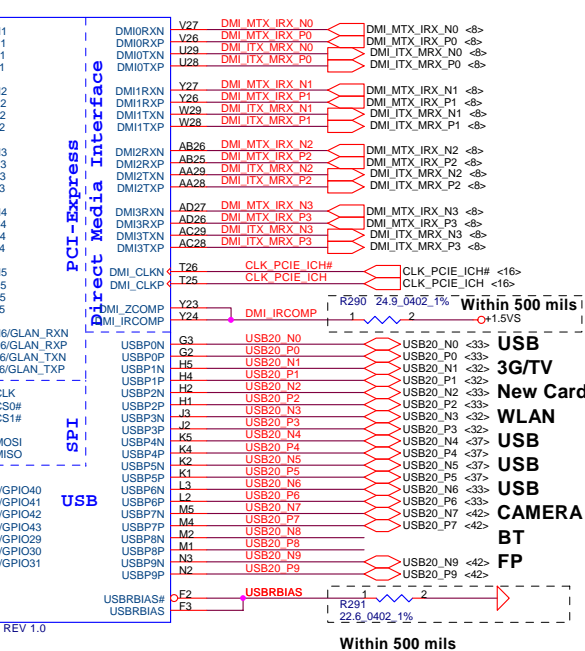
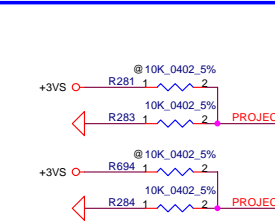
Not in CRB, Keep!



LAN  
NEW Card  
Robson  
3G  
WLAN

SPI not used, Left NC  
USB

Need to define PROJECT ID



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

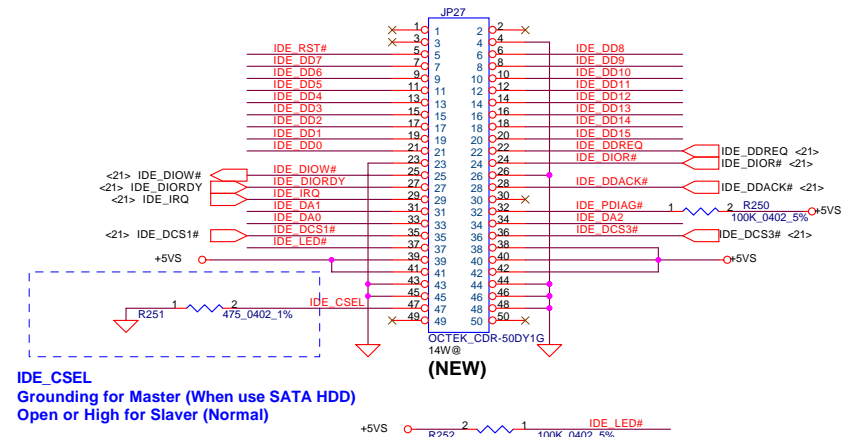
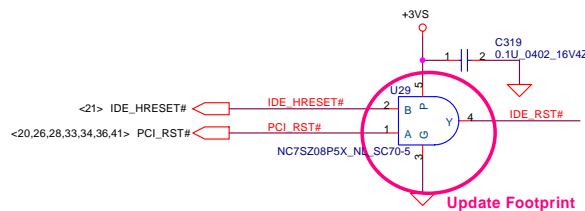
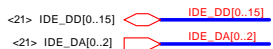
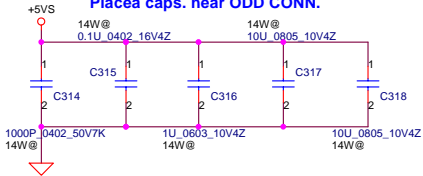
Title		Compal Electronics, Inc.	
ICH8M(3/4)-USB,GPIO,PCIE		Size	Document Number
Customer	IFTXX M/B LA-3541P Schematic	Date	Wednesday, November 01, 2006
Sheet	22	of	52

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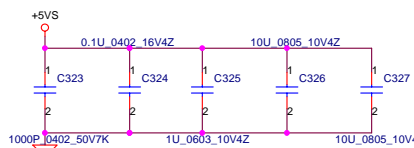
### 14W ODD Conn.

Place caps. near ODD CONN.



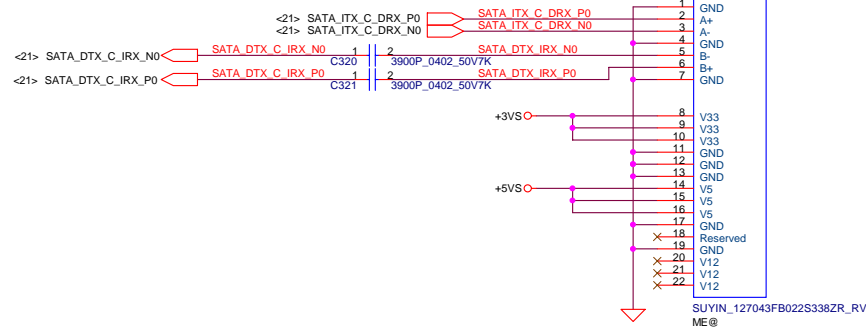
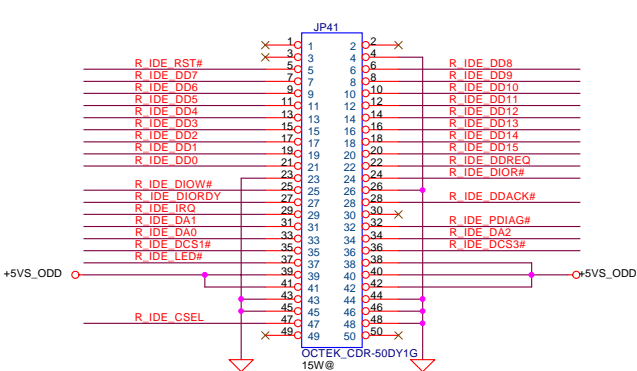
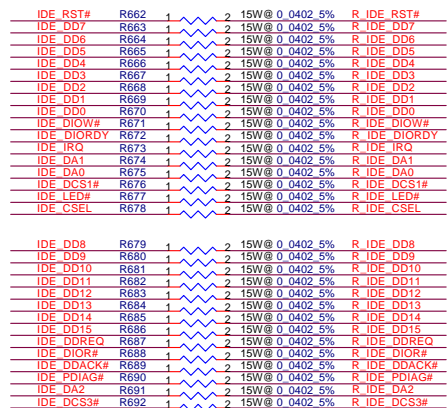
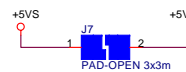
**IDE\_CSEL**  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)

### SATA HDD Conn.

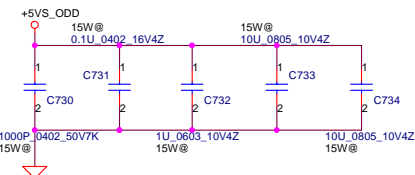


### 15W ODD Conn.

Remember Short at 15W@



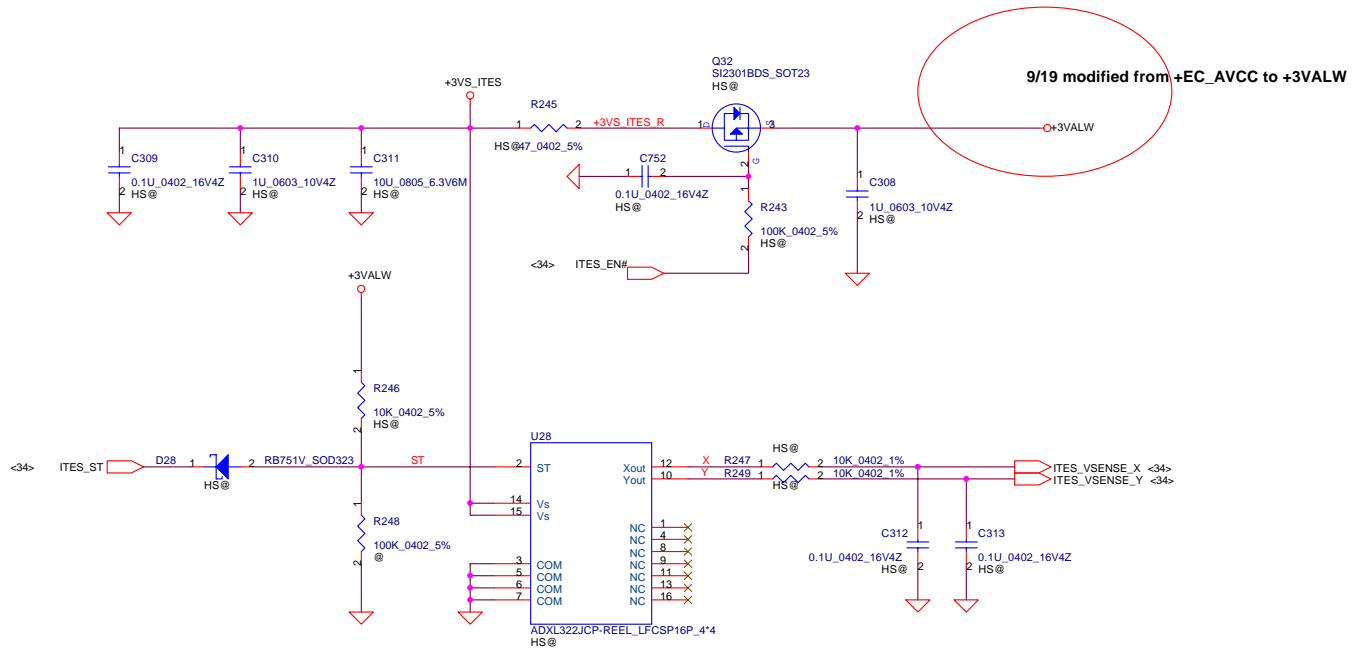
**(NEW)**  
Change Library



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Size	B	Document Number	IFTXX/MB LA-3541P Schematic	
Date:	Wednesday, November 01, 2006	Sheet	24	of 52



**Note : BOM structure HS@ is for Heng shan IFT10/11 this model**



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				Size B
Date:	Wednesday, November 01, 2006	Sheet	25 of 52	



5

4

3

2

1

D

D

C

C

B

B

A

A



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Wednesday, November 01, 2006	Sheet 27 of 52

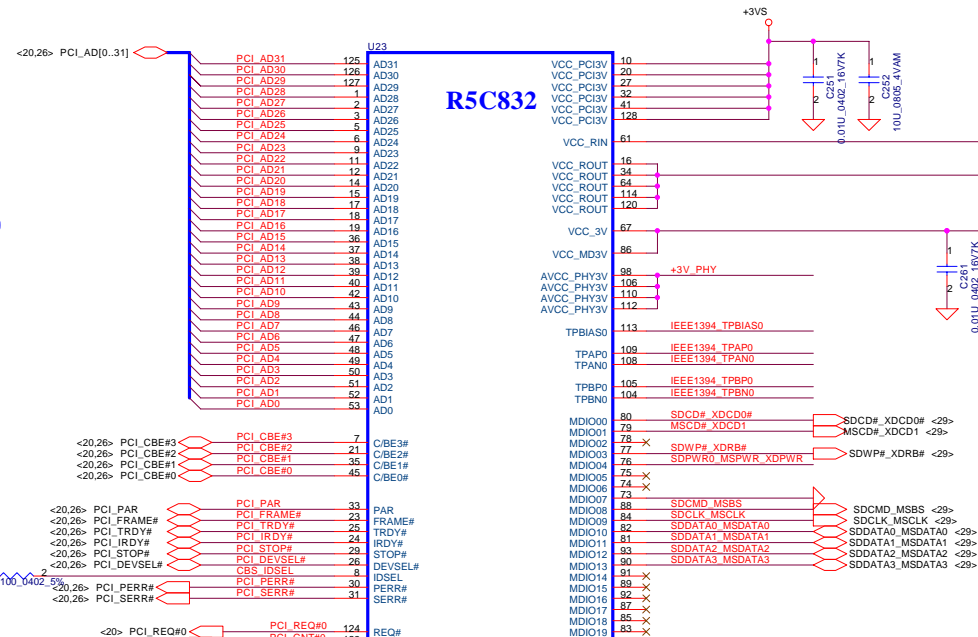
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4

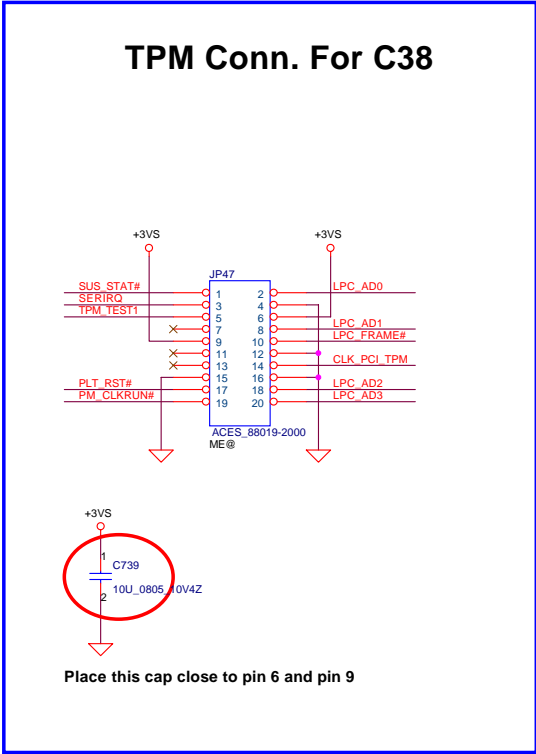
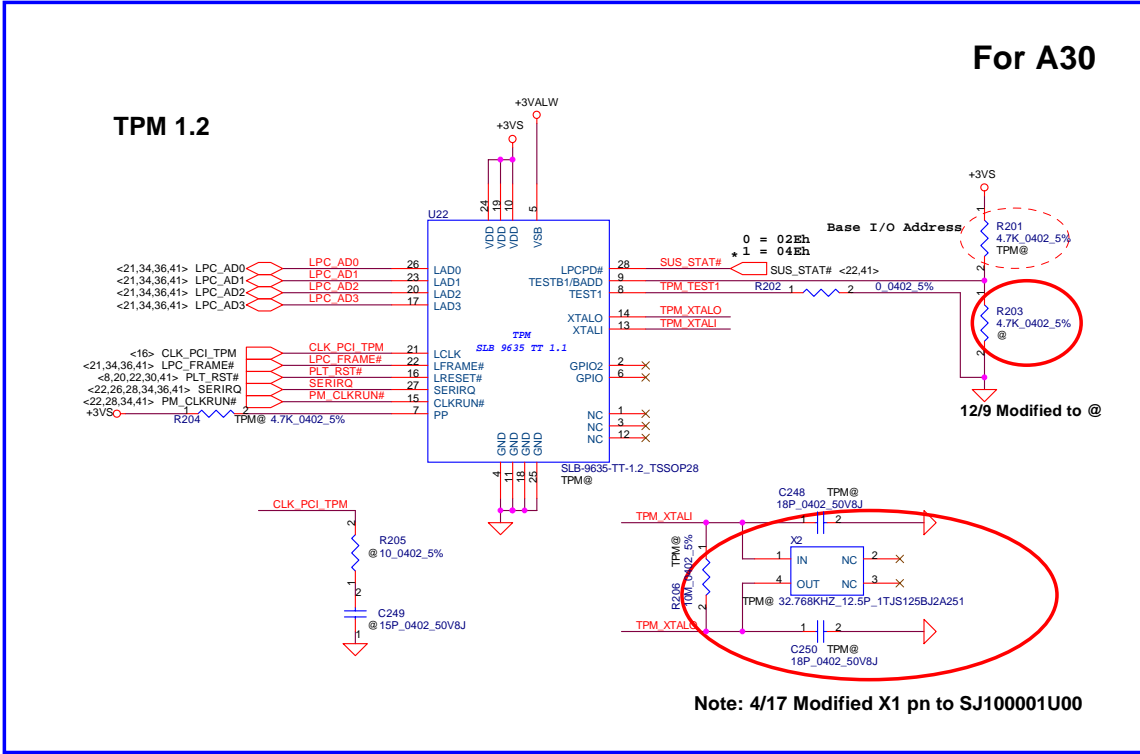
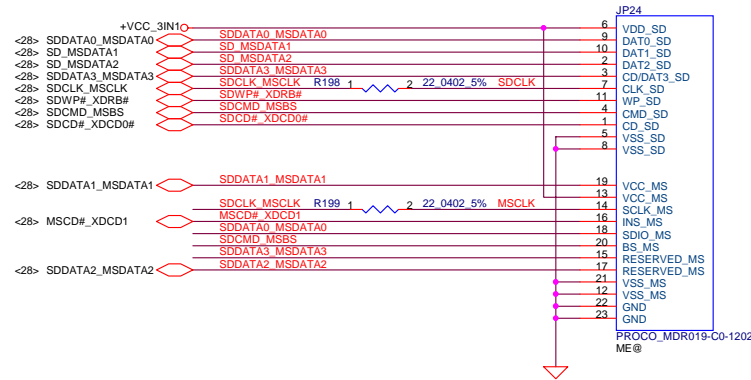
3

2

1

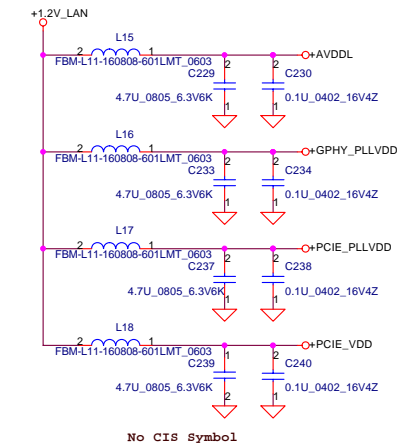
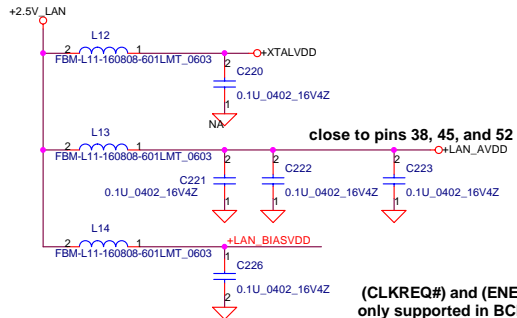


### 3 in 1 Card Reader

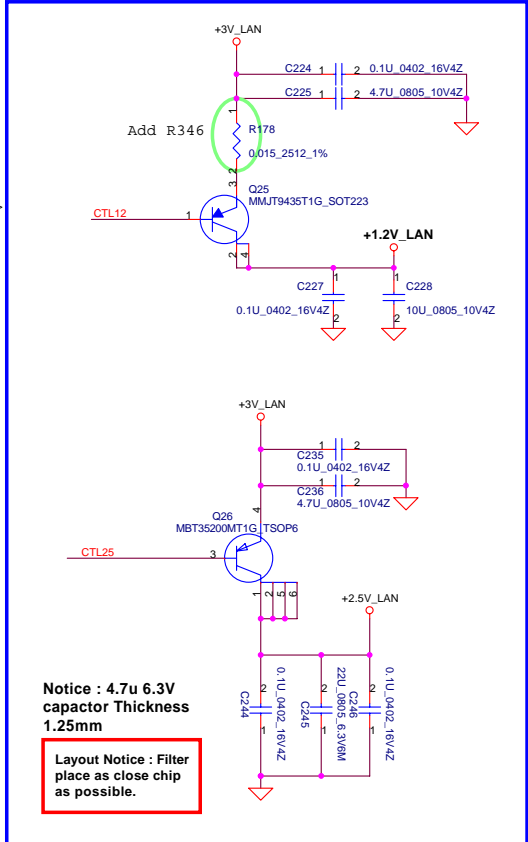
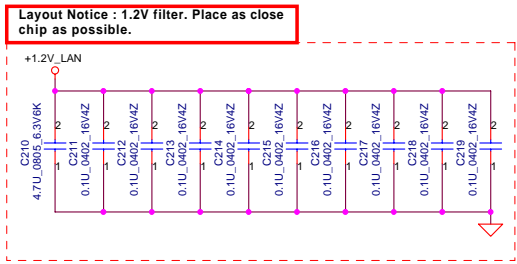
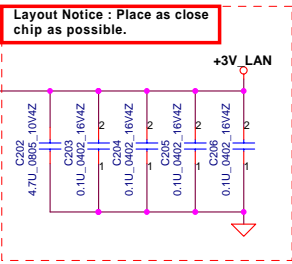
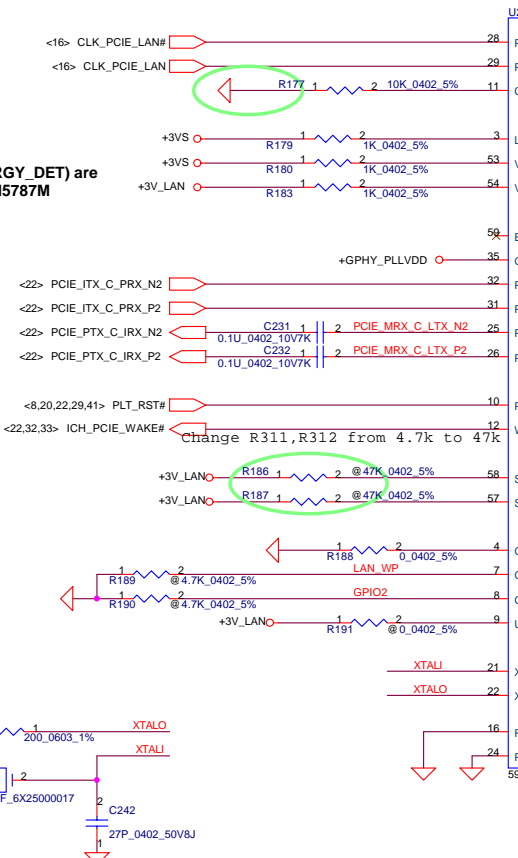


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Date: Wednesday, November 01, 2006				Rev 0.1
Sheet 29 of 52				

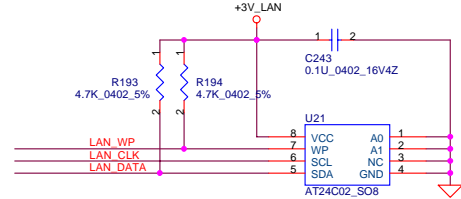
Layout Notice : Filter place as close chip as possible.



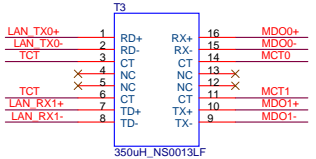
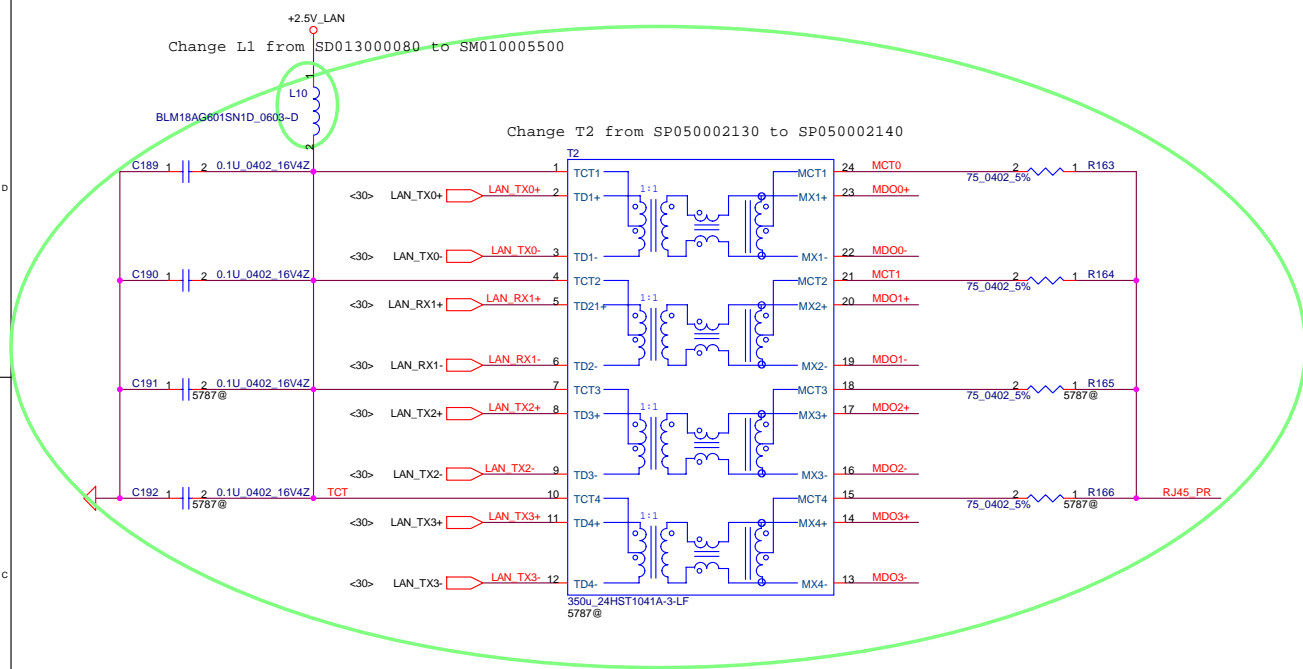
(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M



9/14 change from 1.24K to 1K (By broadcom James)

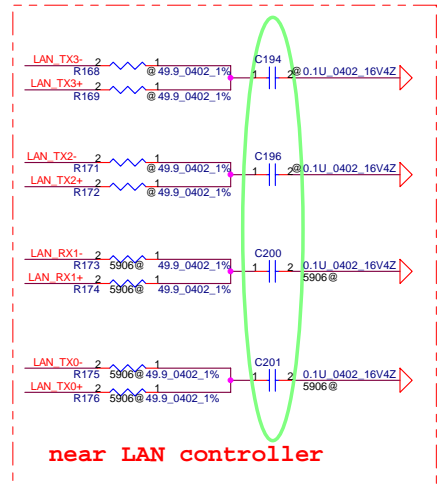


Security Classification				Compal Secret Data			
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	BCM5787MKML		
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				Custom	XXXXX LA-3541P	0.1	
				Date:	Wednesday, November 01, 2006	Sheet	30 of 52

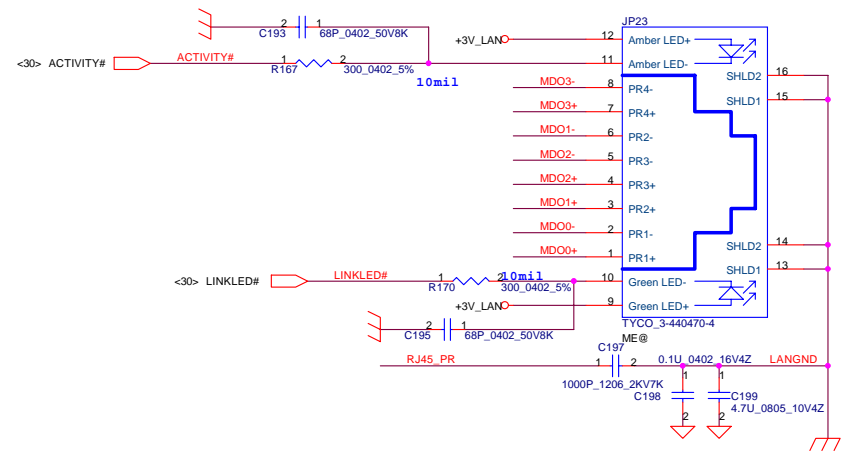


Change T1 from SP050001210 to SP050001210

Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

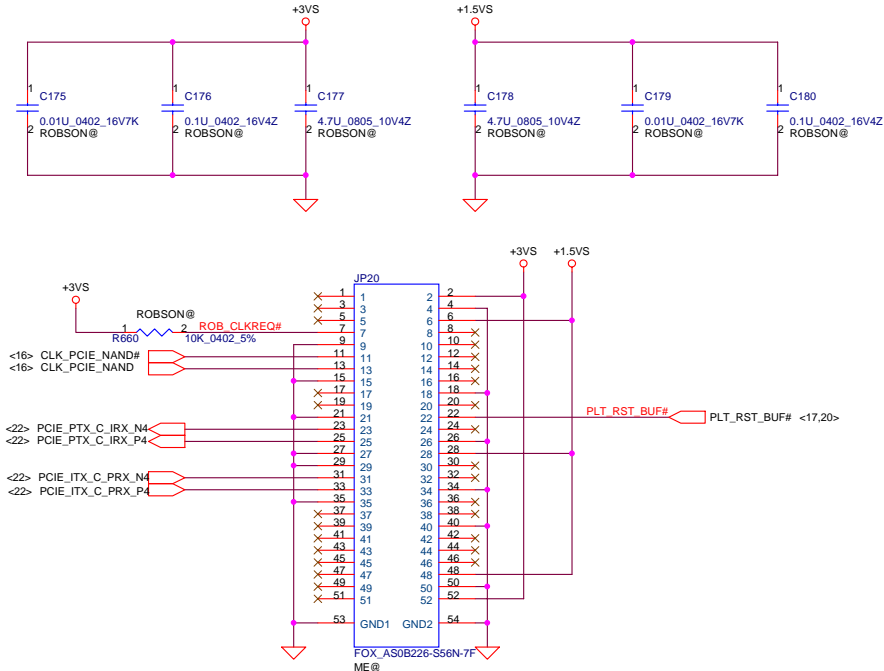


Lan Conn.

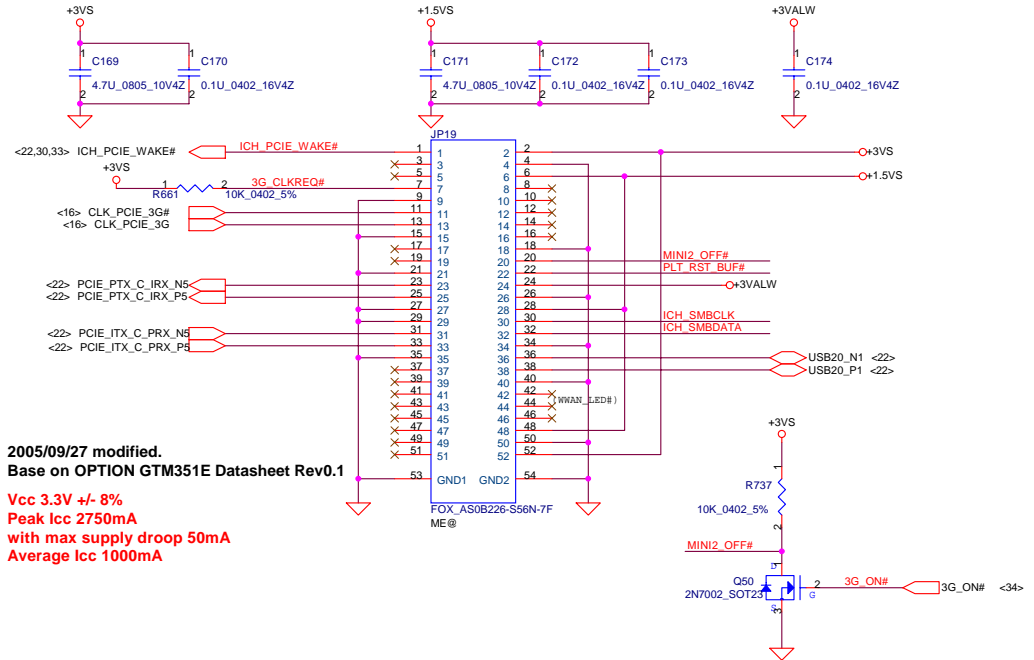


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Date:	Wednesday, November 01, 2006	Sheet	31	of	52	

# NAND mini Card(Robson support)

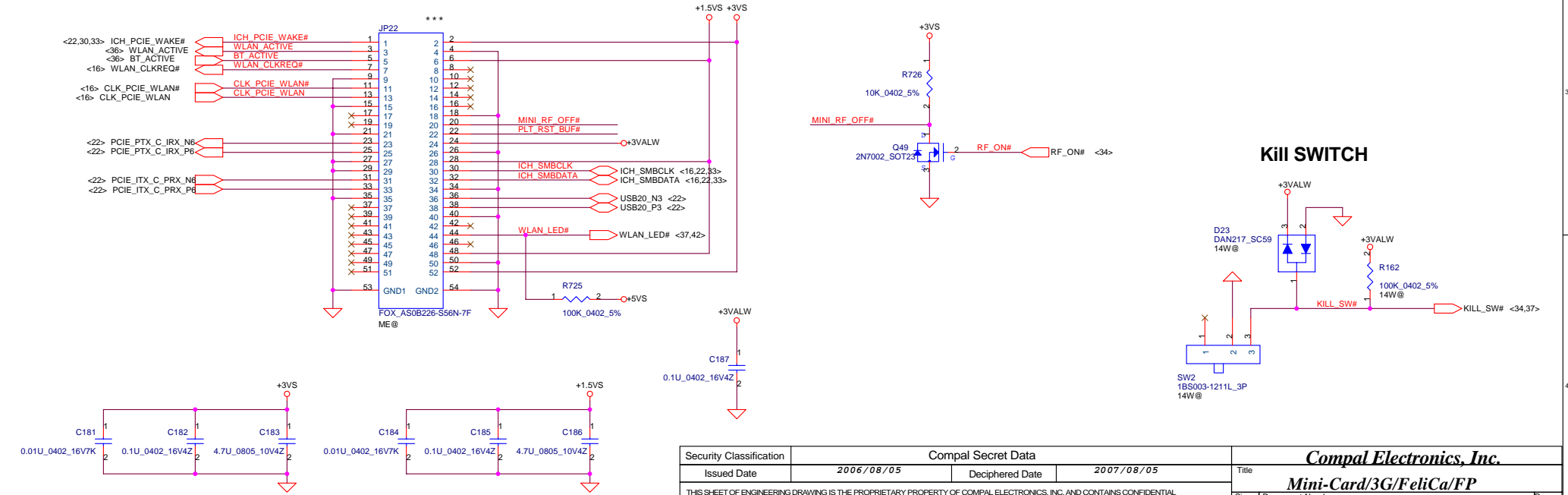


# Mini-Express Card for 3G Or TV Tuner



2005/09/27 modified.  
 Base on OPTION GTM351E Datasheet Rev.0.1  
**Vcc 3.3V +/- 8%**  
**Peak lcc 2750mA**  
**with max supply droop 50mA**  
**Average lcc 1000mA**

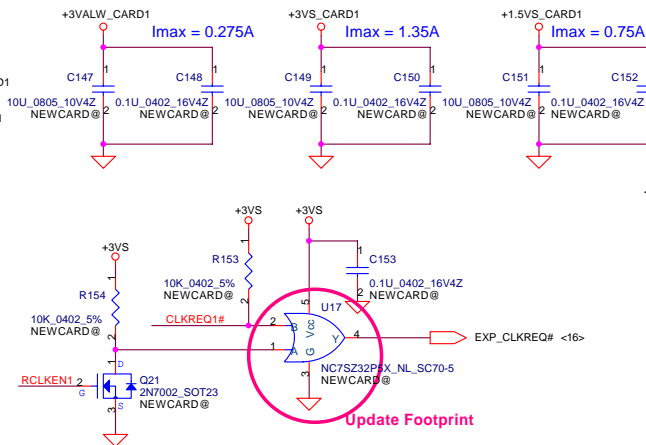
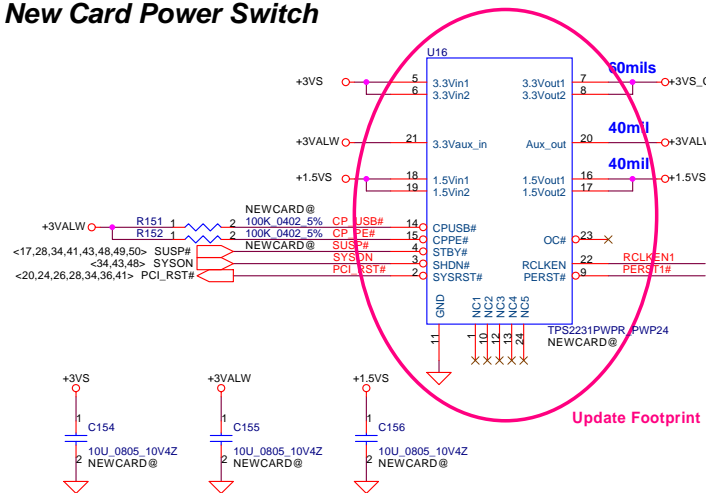
# Mini-Express Card for WLAN



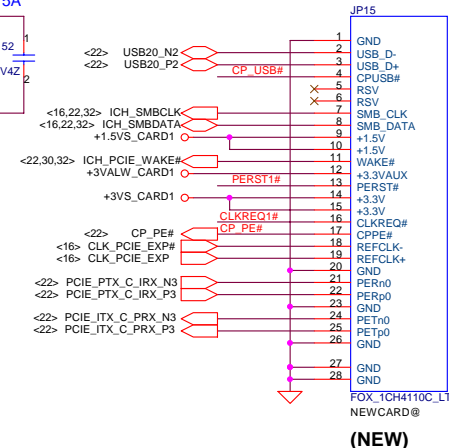
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Compal Electronics, Inc.	
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Size	Document Number	LA-3541P		Rev	0.1
Date:	Wednesday, November 01, 2006	Sheet	32	of	52



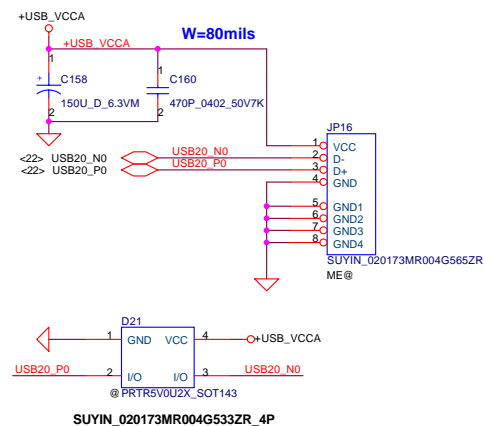
# New Card Power Switch



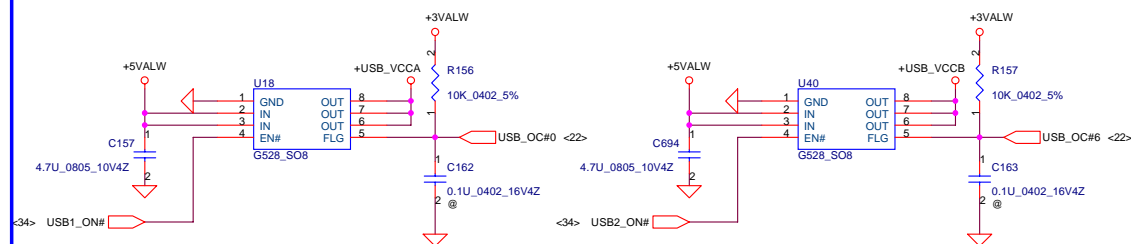
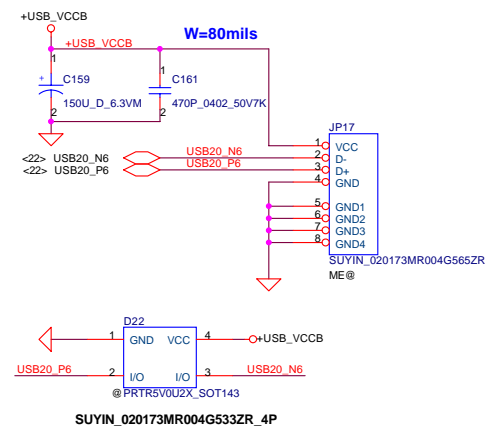
# New Card Socket (Left/TOP)



## USB CONN. 1

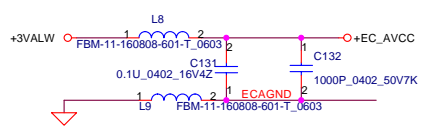


## USB CONN. 2

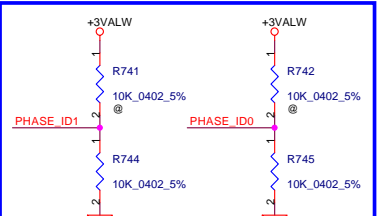
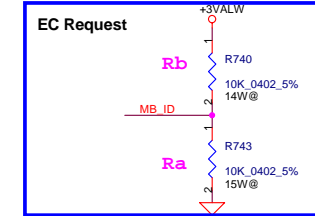
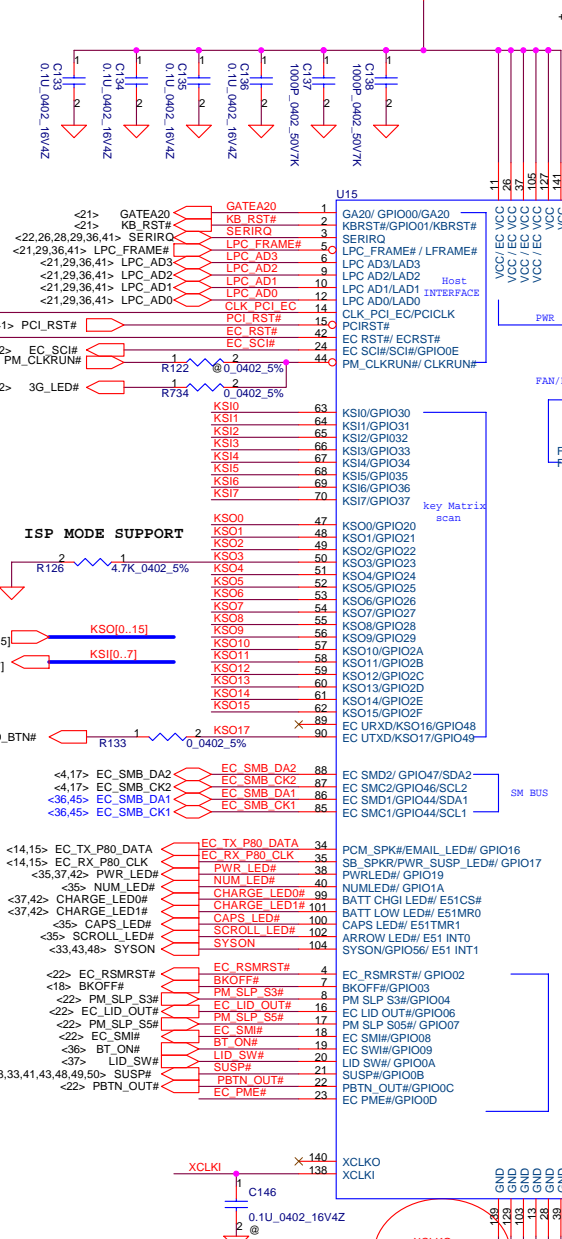
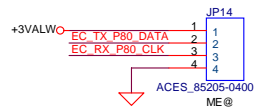


9/17 modified this block

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NEW CARD & USB Connector			Size B	Document Number
			IFITX M/B LA-3541P Schematic	
Date:	Wednesday, November 01, 2006	Sheet	33	of 52

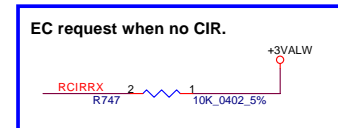
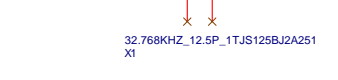
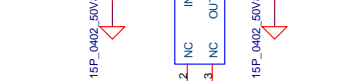
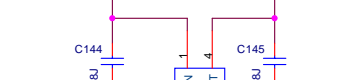
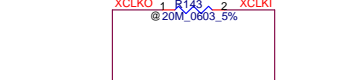
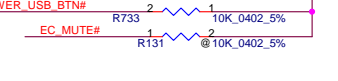
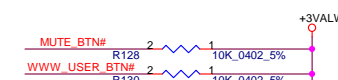
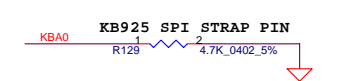


**EC DEBUB PORT**



ID1	ID0	Test Mode
0	0	A-Test
0	1	B-Test
1	0	C-Test

**EC Request**



10/17 : Change P/N from SA009100120 to SA00001HZ00  
 10/17 : FootPrint : SA009100120 BOM : SA00001HZ00

KB925 should use Data code 06361 which has fixed bonding issue  
 KB925 pin 139 is used for XCLKO, Pin 140 NC

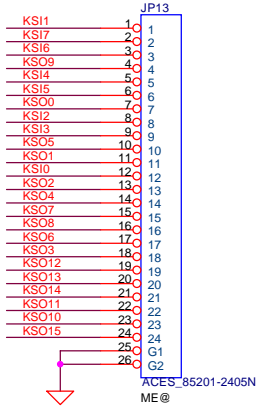
Security Classification	2006/08/04	Compal Secret Data	2006/10/06
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Title		Compal Electronics, Inc.	
E-Part Number		ENE-KB925	
Size	Document Number	Customer	IEL10 LA-3451P
Date:	Wednesday, 01/20/06	Sheet	34 of 52

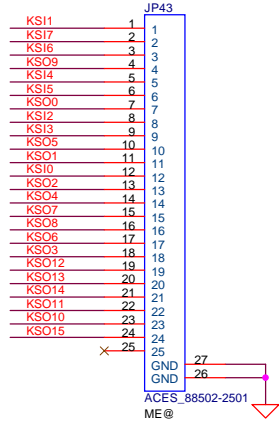
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# INT\_KBD Conn.

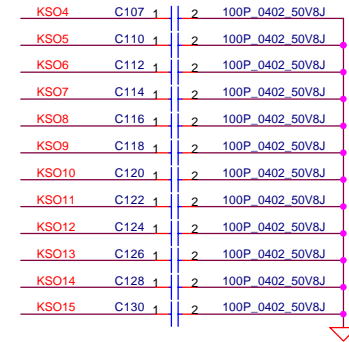
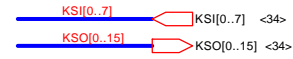
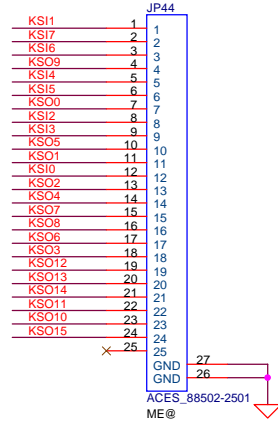
## For IFT10



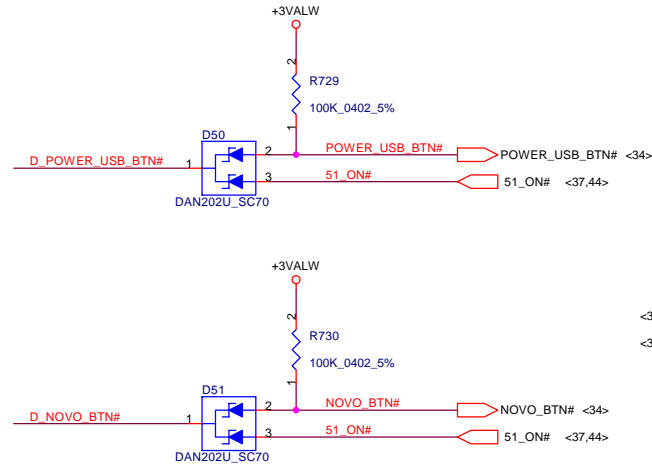
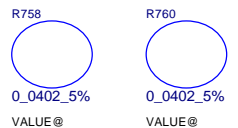
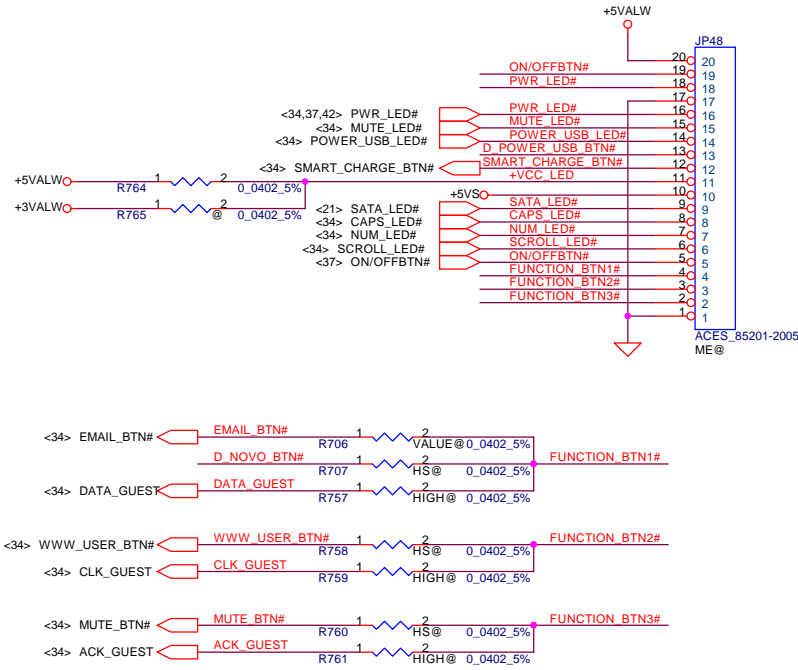
## For IFL90



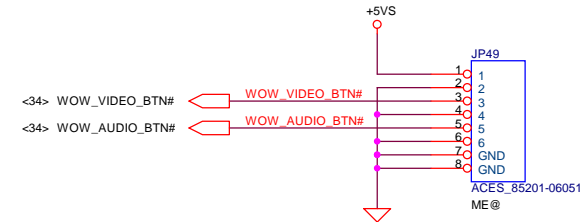
## For IFT00



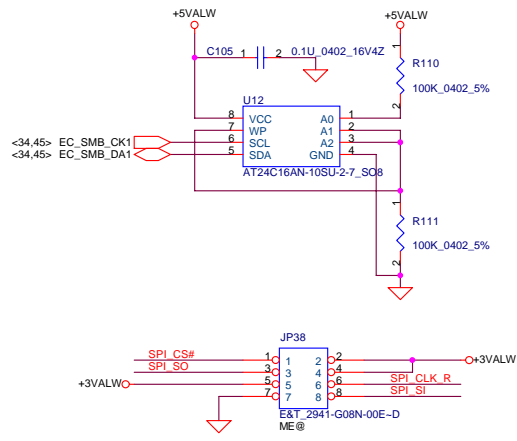
# Switch Board Conn.



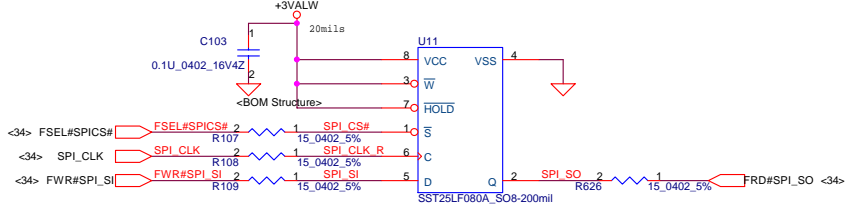
# Video Switch Board Conn.



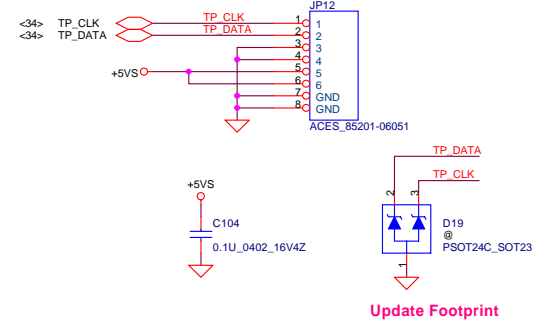
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	EC ENE KB910L(Reserved)
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				Document Number
				IFTXX M/B LA-3541P Schematic
				Rev 0
				Date: Wednesday, November 01, 2006
				Sheet 35 of 52



### 8M SPI ROM



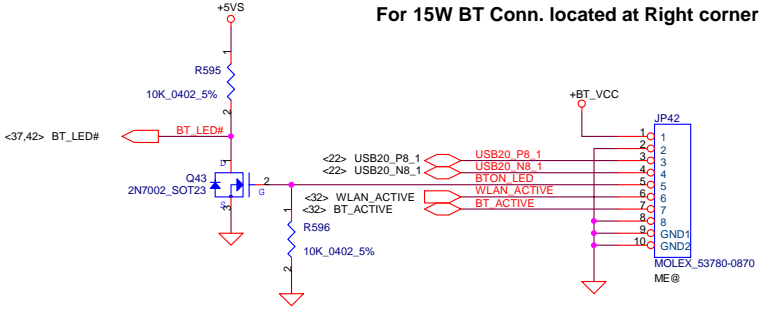
### To TP/B Conn.



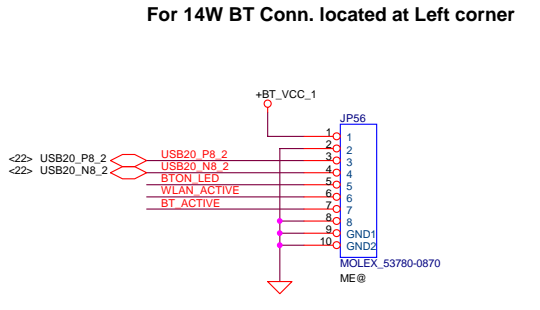
### Bluetooth Conn.

Need to check BT pin definition again!  
9/20 modified this block

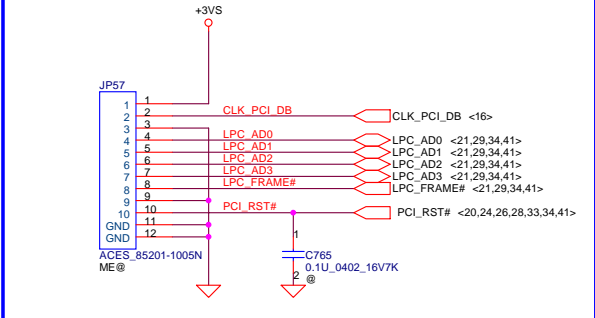
#### For 15W BT Conn. located at Right corner



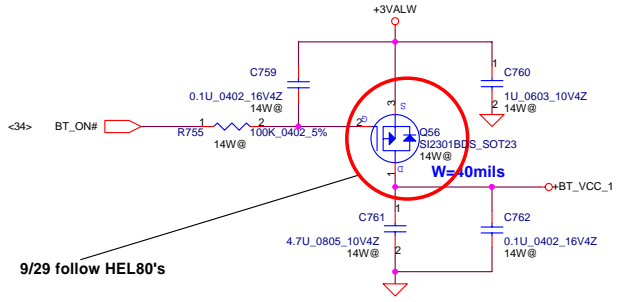
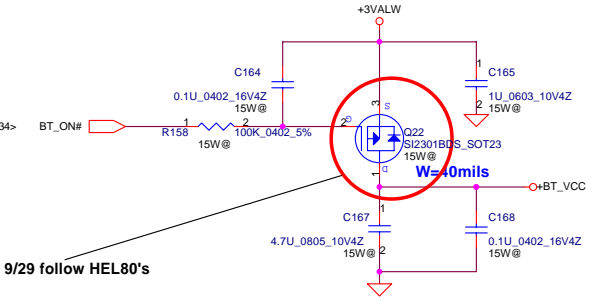
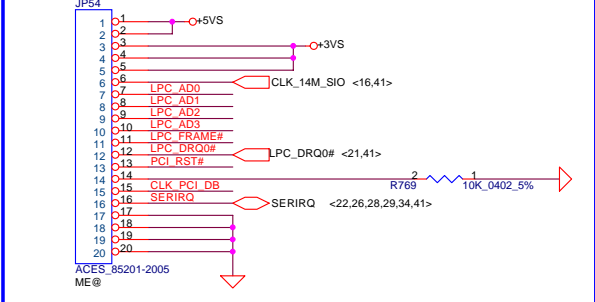
#### For 14W BT Conn. located at Left corner



### FOR LPC DEBUG PORT

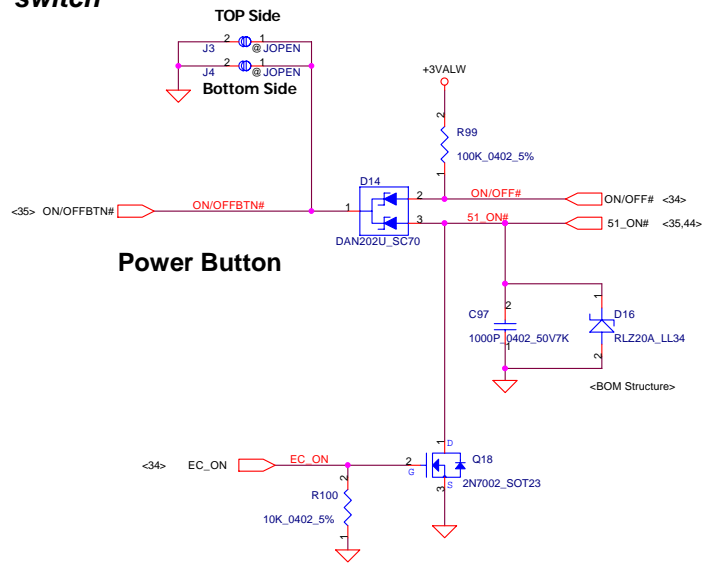


### FOR LPC SIO DEBUG PORT

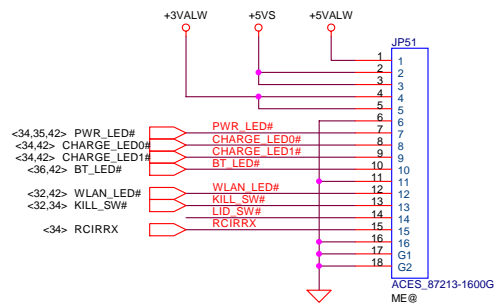


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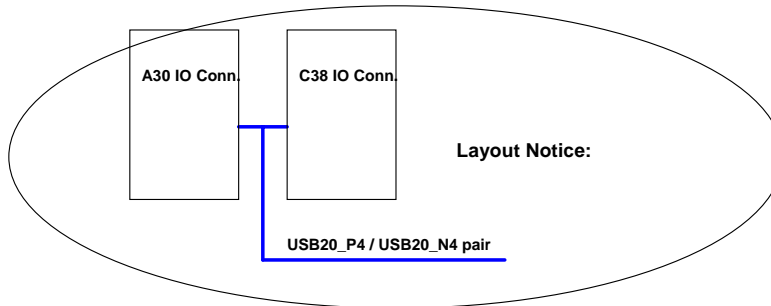
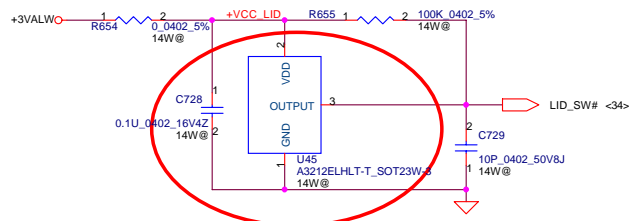
# ON/OFF switch



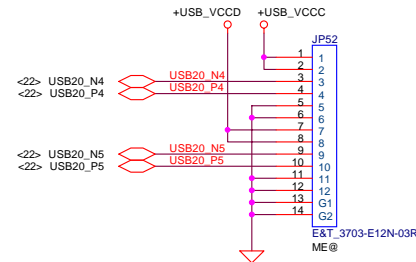
# Front LED Board



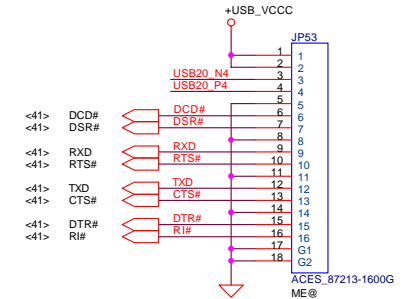
# Lid Switch



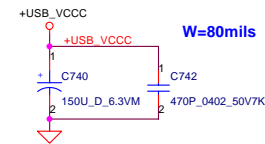
## For A30 IO Conn.



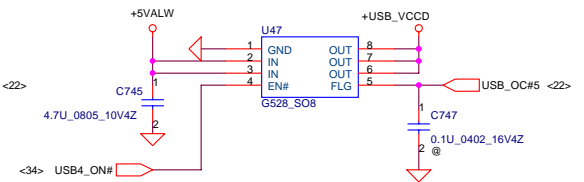
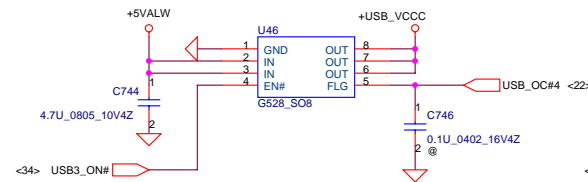
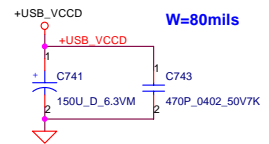
## For C38 IO Conn.



## To USB CONN. 3

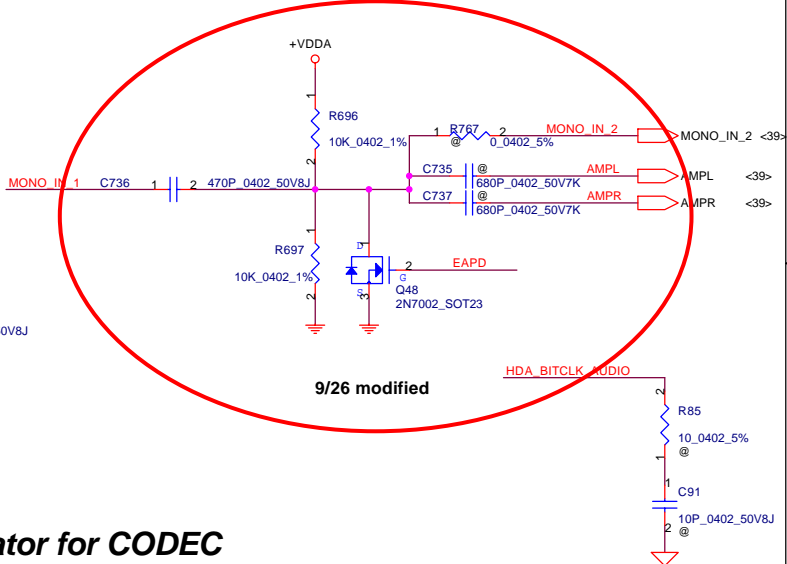
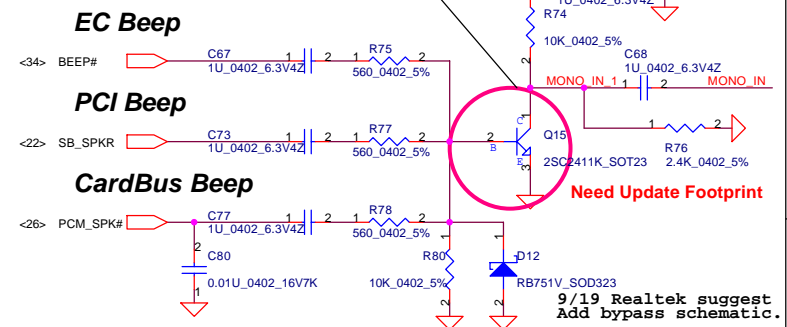
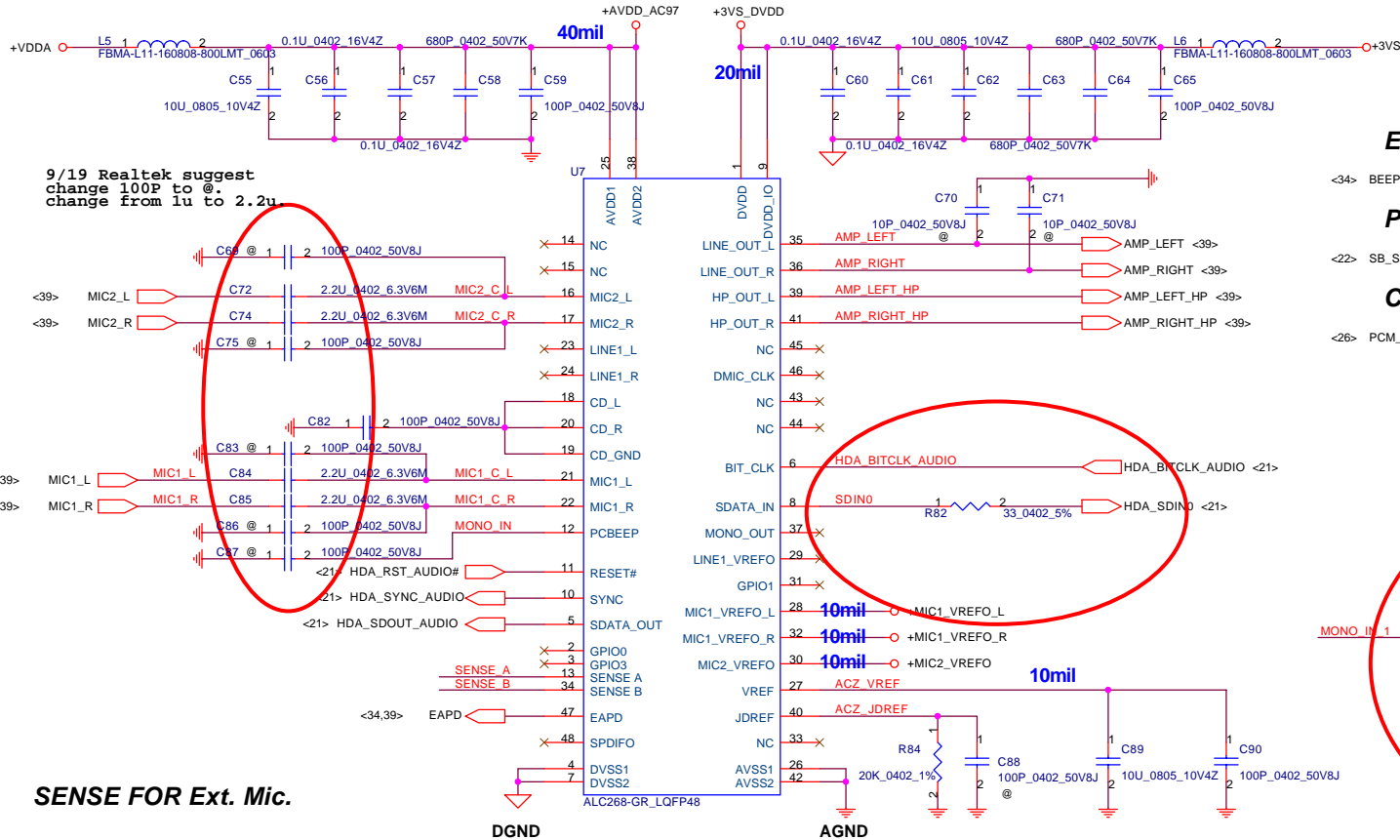


## To USB CONN. 4



Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Power OK, Reset and RTC Circuit, TP	
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				IFTXX MB LA-3541P Schematic	
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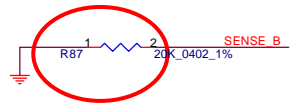
# HD Audio Codec



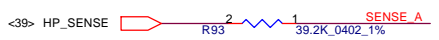
## SENSE FOR Ext. Mic.



## SENSE FOR Solo Int. Mic.

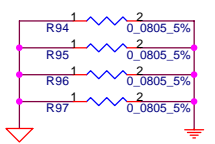


## SENSE FOR HP

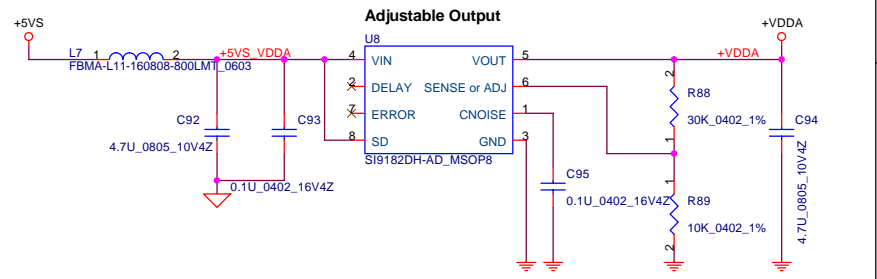


Sense Pin	Impedance	Codec Signals	Function
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
SENSE B	5.1K	PORT-D (PIN 35, 36)	LINE Out
	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

## Moat Bridge



## Regulator for CODEC



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Date: Wednesday, November 01, 2016				Sheet	38 of 52

### Compal Electronics, Inc.

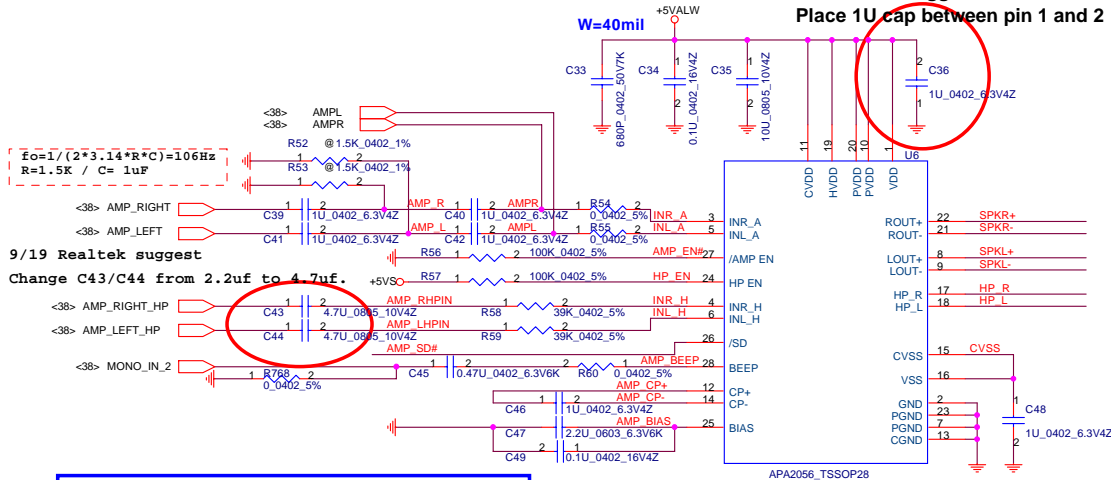
HD Audio Codec ALC268

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# APA2056 SPK/HP Amplifier

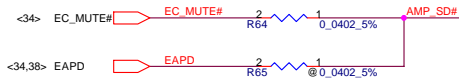
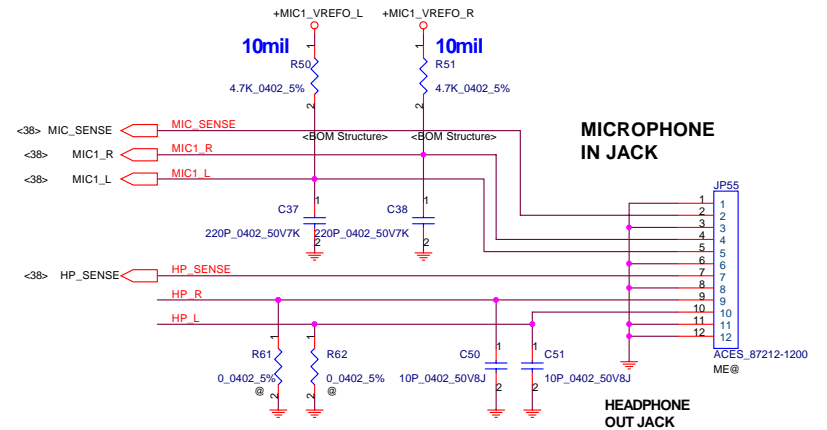
**9/5 ANPEC Suggest**  
Place 1U cap between pin 1 and 2



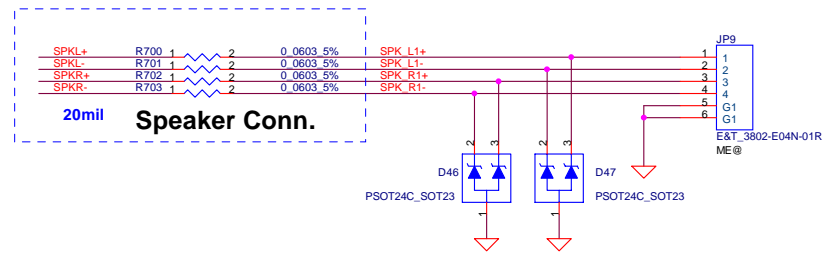
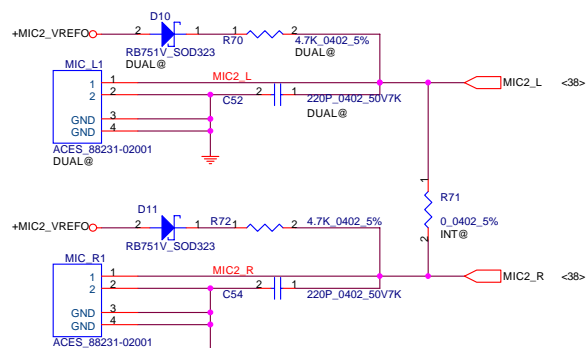
9/19 Realtek suggest  
Change C43/C44 from 2.2uF to 4.7uF.

9/5 If implement AMP BEEP, Swap C155 and R79.  
R79 change from 0 Ohm to 47K

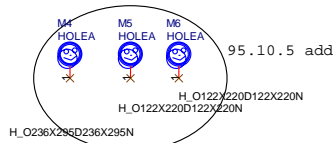
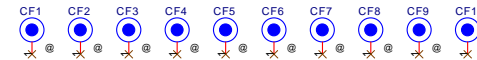
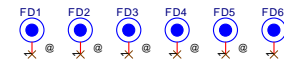
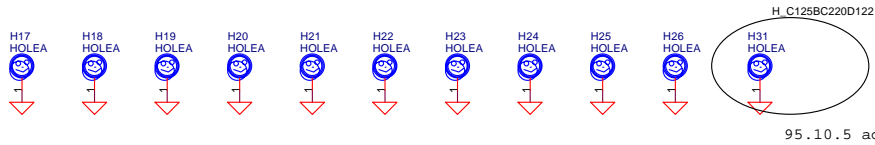
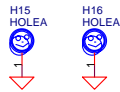
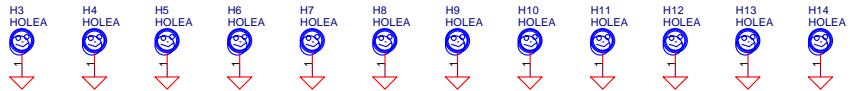
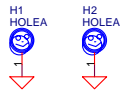
IN\_A Gain = 10dB (Internal Speaker)  
IN\_H Gain = 0dB (Headphone)



## SINGLE INT MIC/DUAL INT MIC



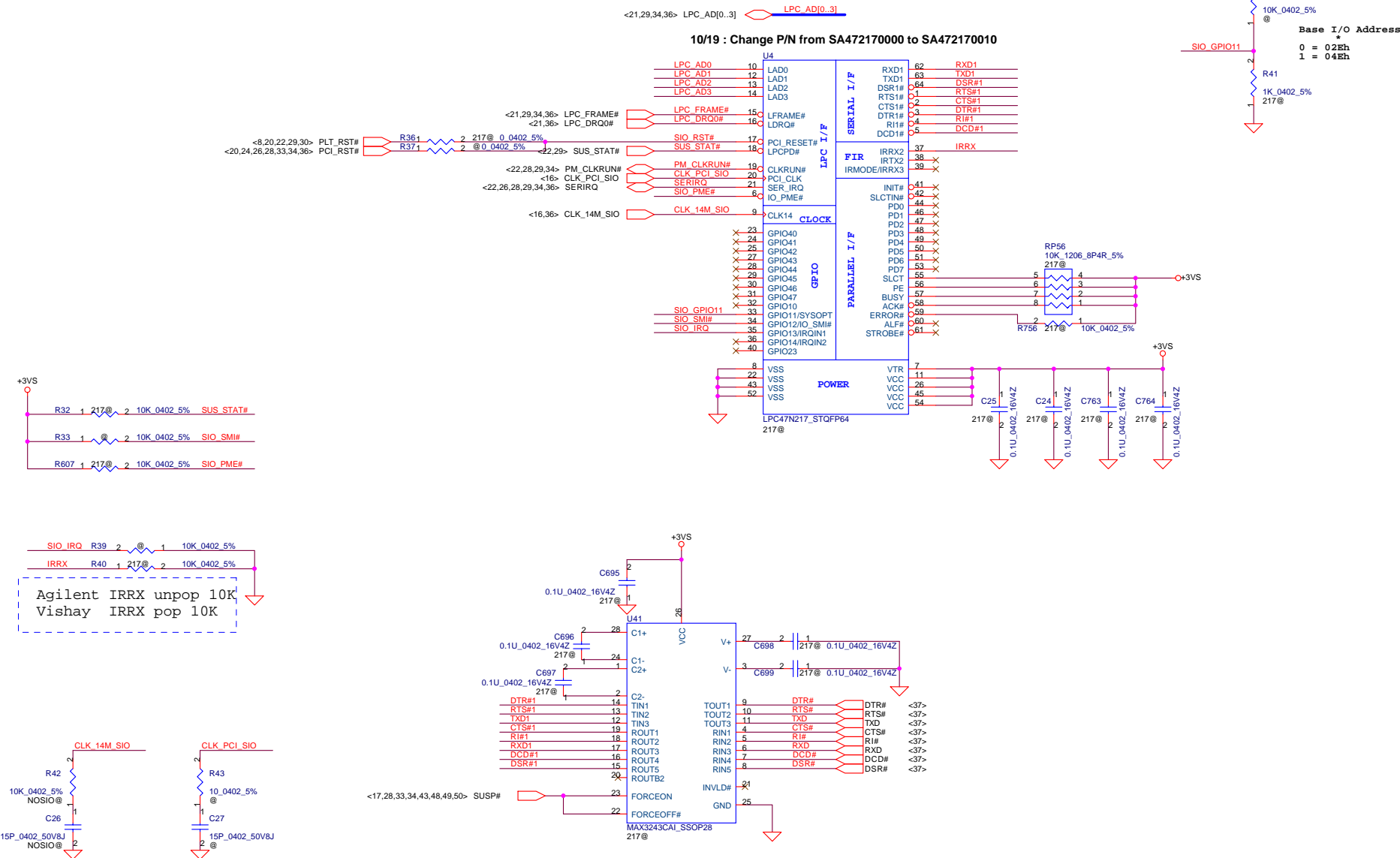
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	AMP/VR/Audio Jack/MIC
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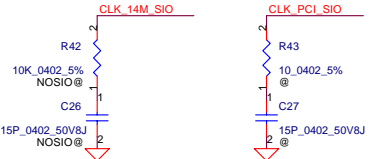
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title FAN & Screw Hole	
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# SUPER I/O SMsC LPC47N217



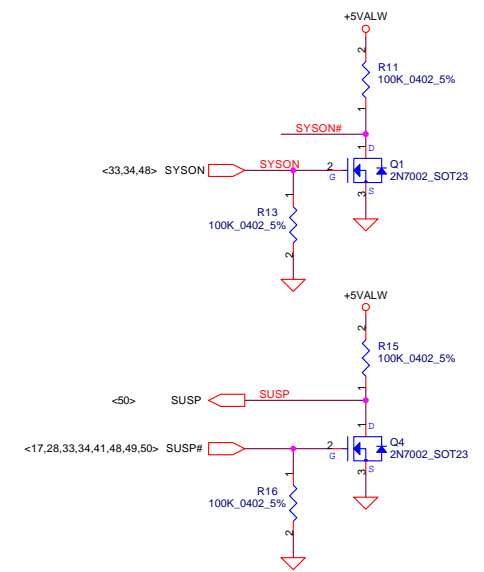
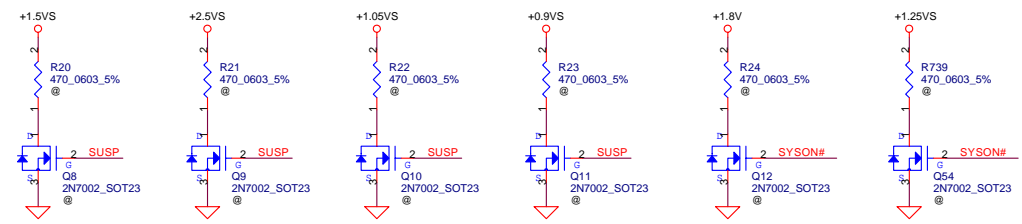
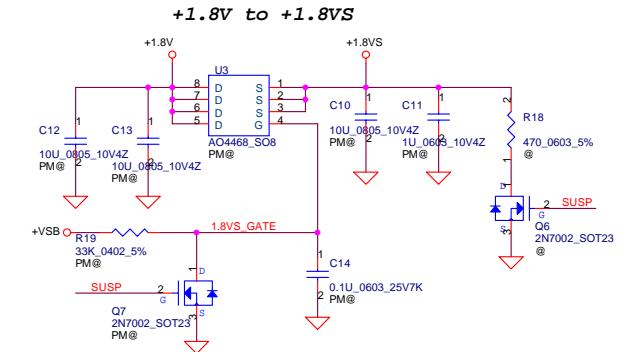
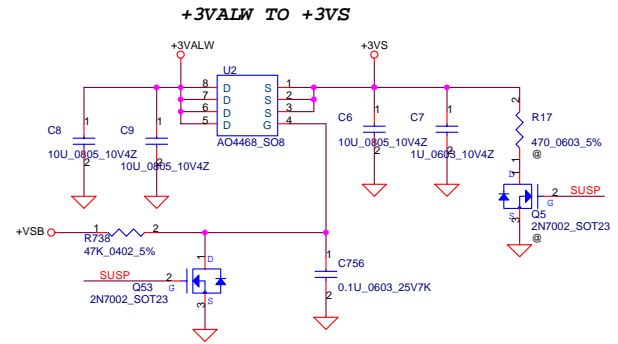
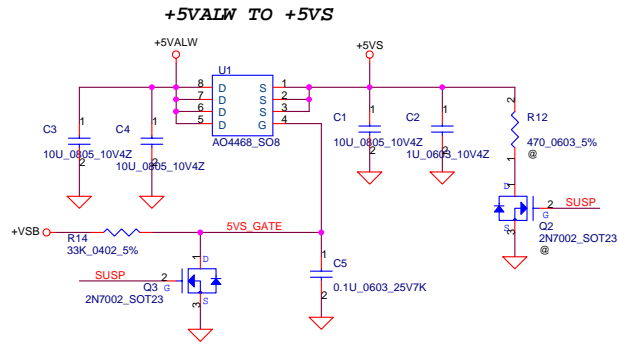
SIO IRQ R39 2 @ 1 10K 0402 5%  
 IRRX R40 1 217 @ 2 10K 0402 5%  
 Agilent IRRX unpop 10k  
 Vishay IRRX pop 10K



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Date: Wednesday, November 01, 2006				Sheet	41 of 52

9/18 modify this page following IGT1x





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Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC Interface	
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				IFTXX/MB LA-3541P Schematic	
				Date:	Wednesday, November 01, 2006
				Sheet	43 of 52