ZZZ1

PCB

Compal Confidential

IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

(With nVIDIA MXM/B)

2006-11-01

REV: 0.1

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Title: Cover Page

Size: B | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0.1

Date: Wednesday, November 01, 2006 | Sheet 1 of 52

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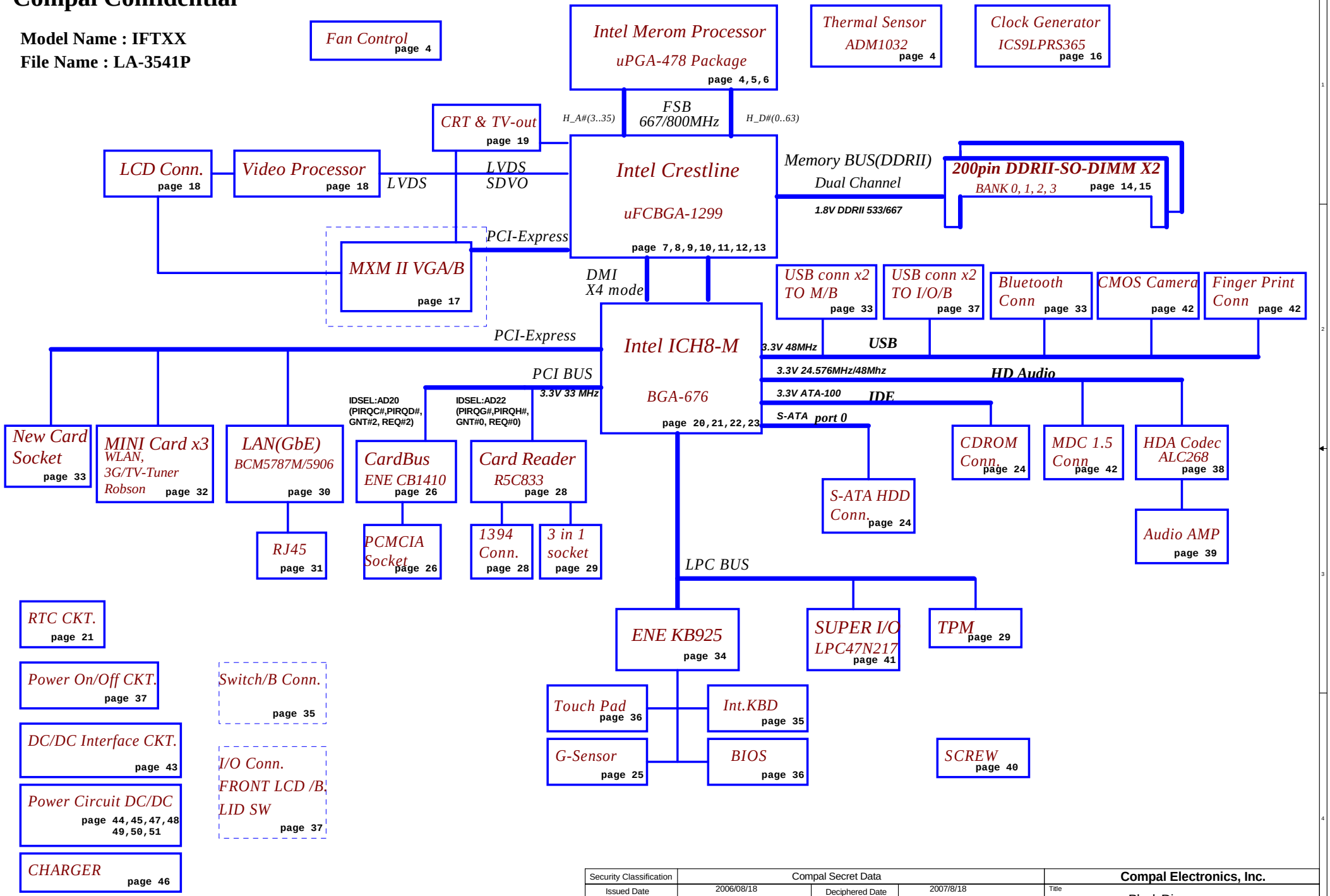
Model Name : IFTXX
File Name : LA-3541P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

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Title	Notes List		
Size B	Document Number IFTXX M/B LA-3541P Schematic		Rev 0
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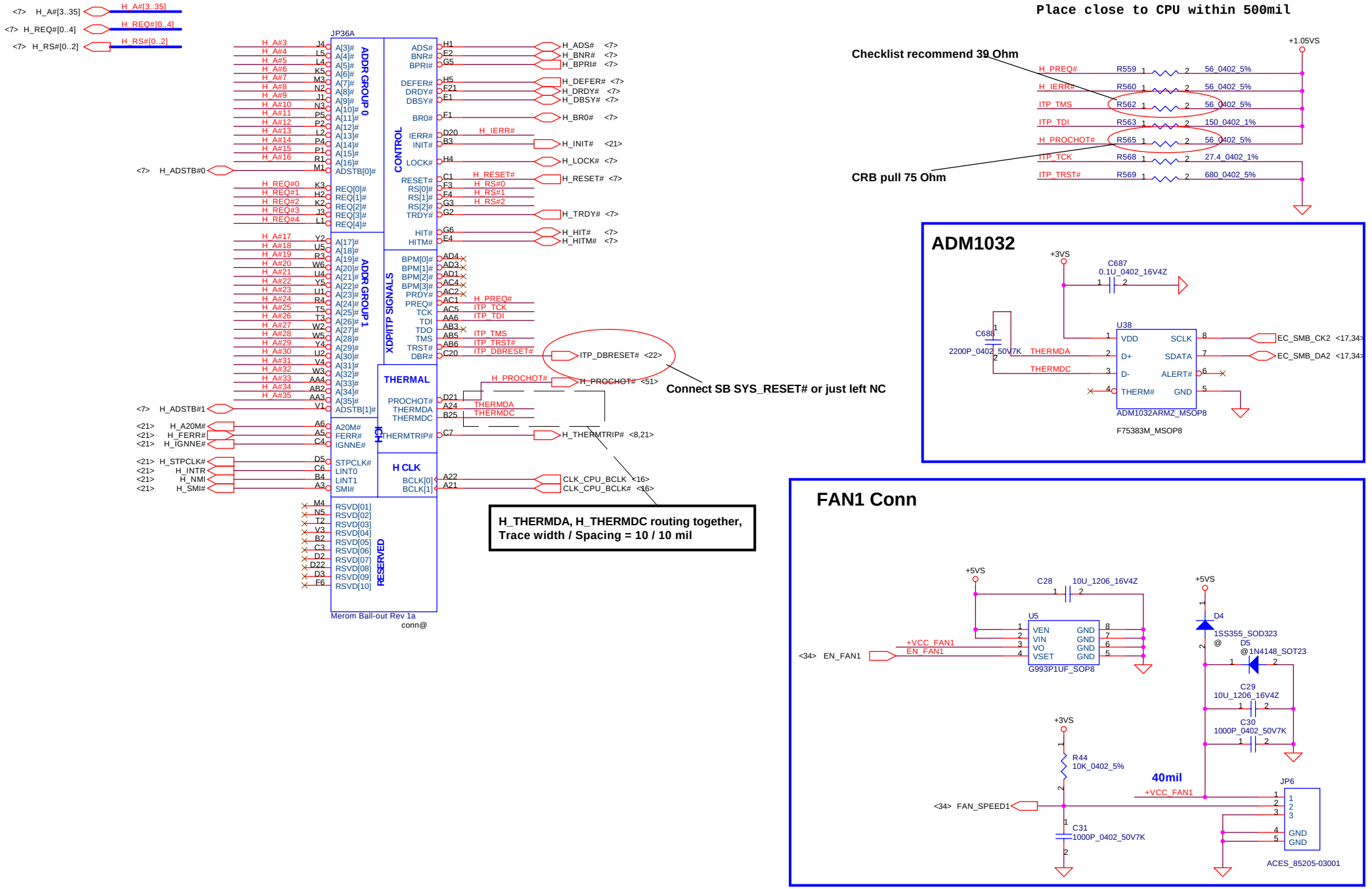

Security Classification	Compal Secret Data		
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Title: Merom (1/3)

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

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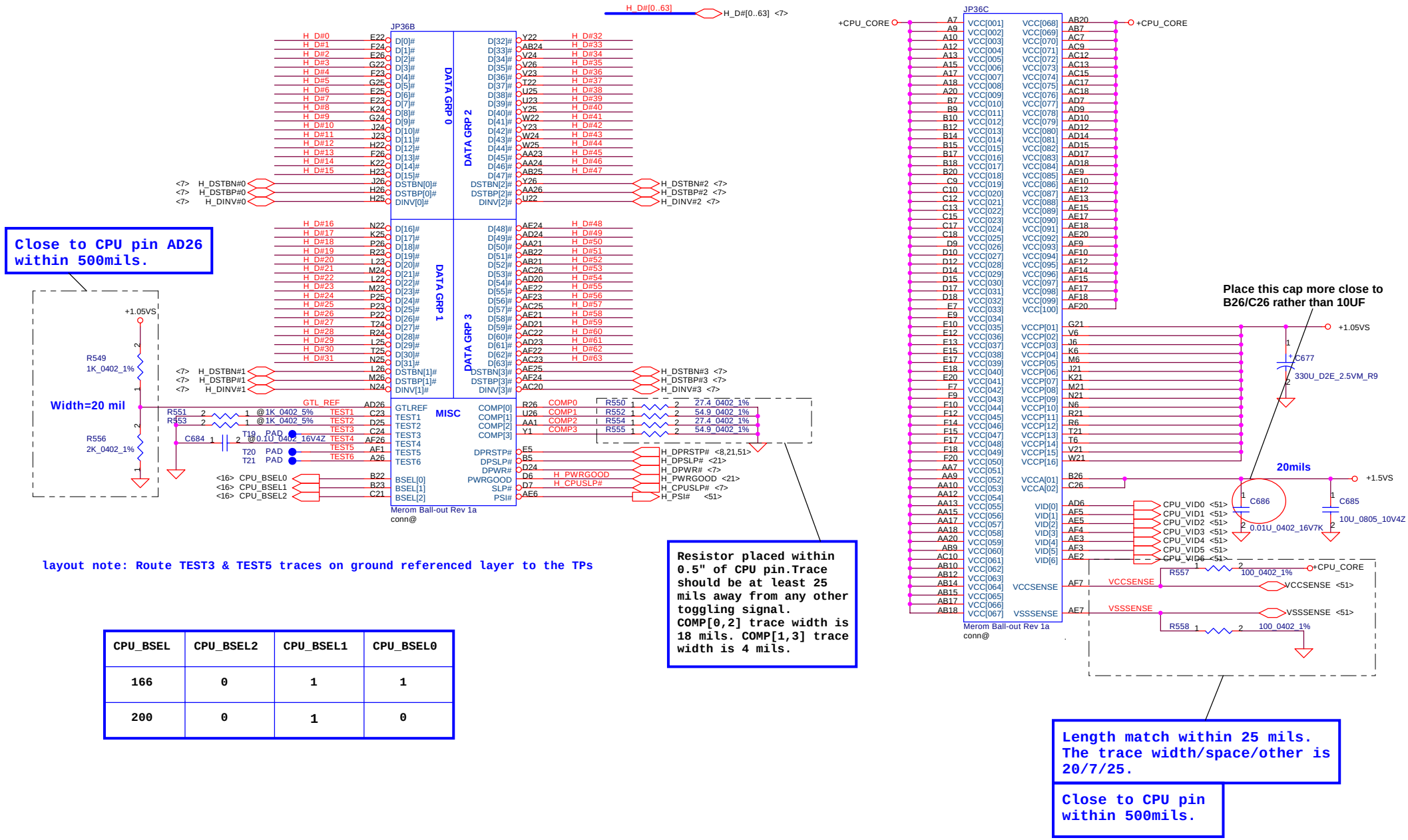

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: Merom (2/3)

Size: B | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

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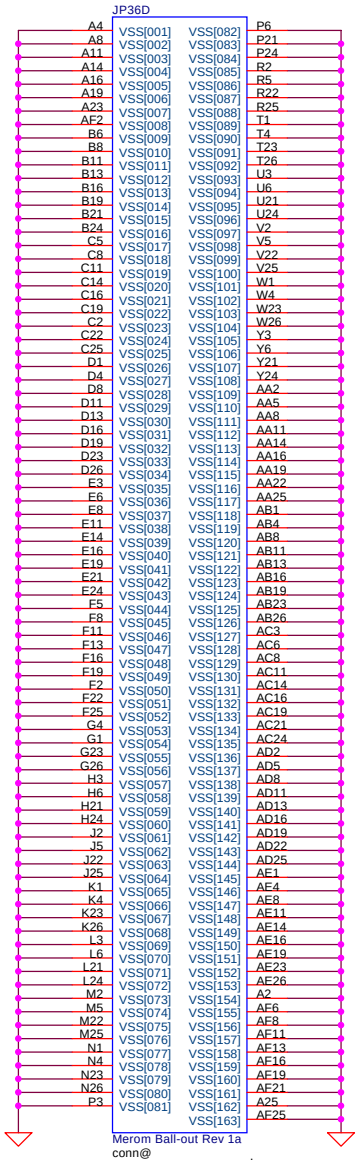

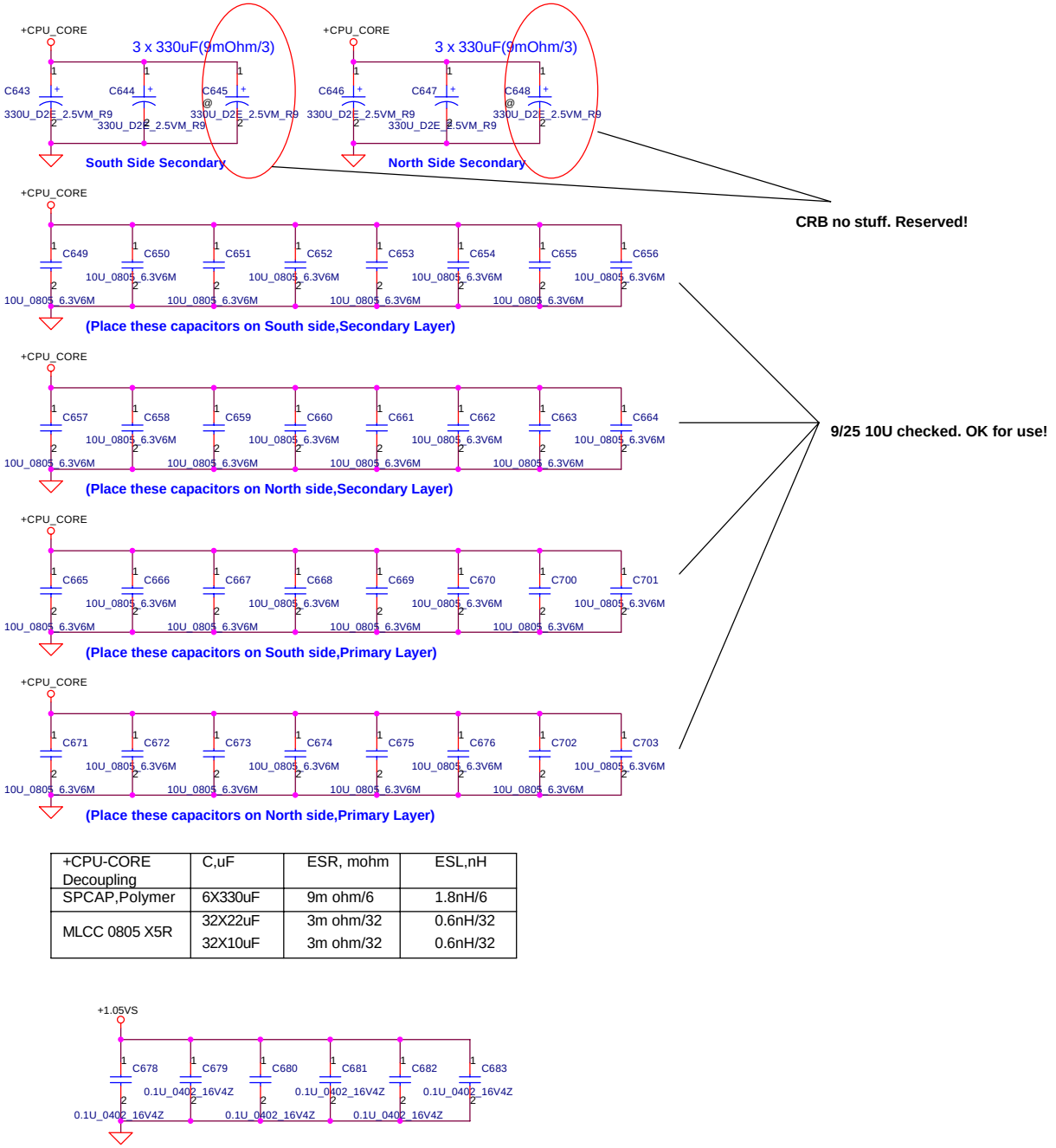

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF 32X10uF	3m ohm/32 3m ohm/32	0.6nH/32 0.6nH/32

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Title: Merom (3/3)

Size: B | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

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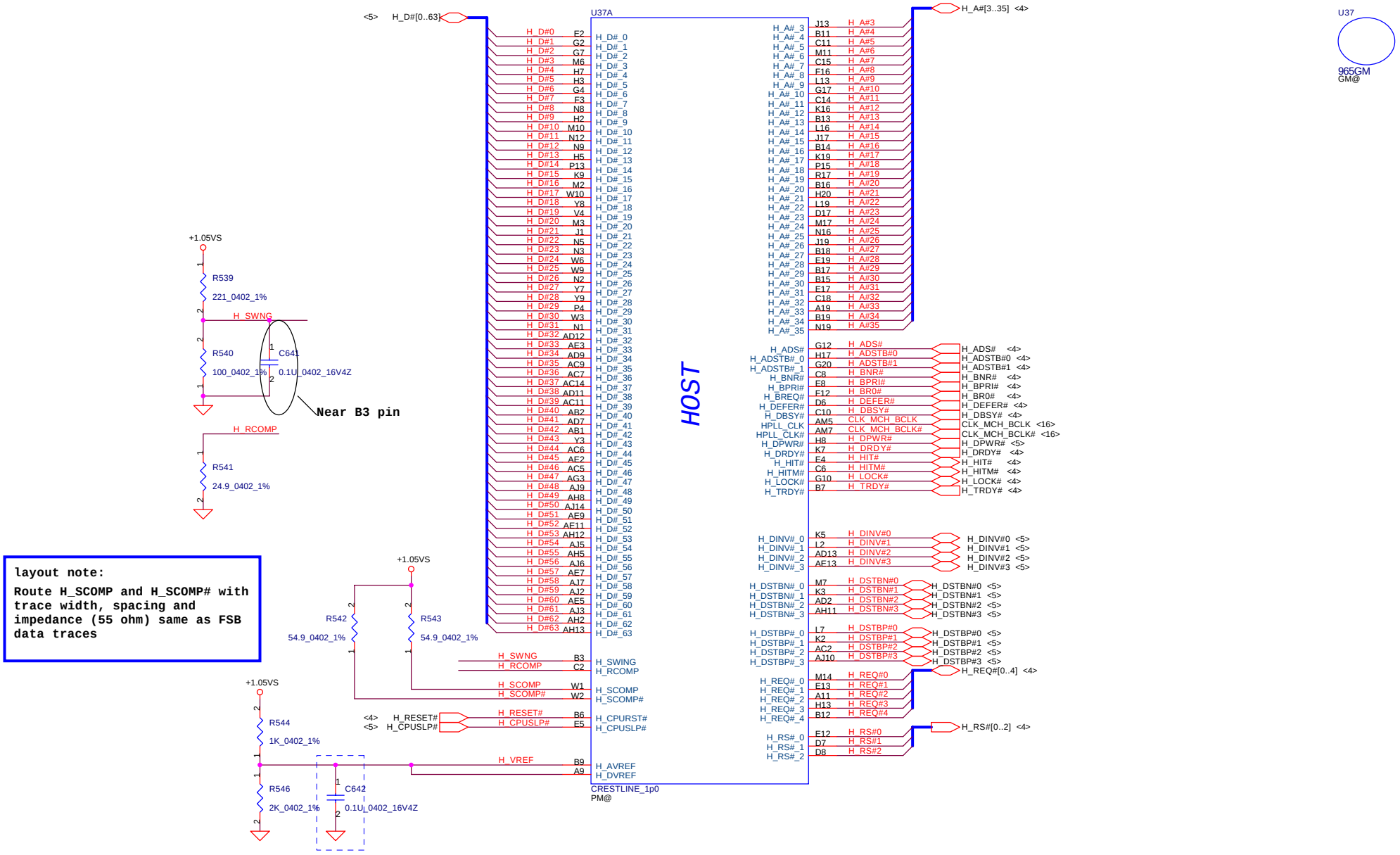

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Compal Electronics, Inc.

Title: Crestline (1/7)-GTL

Size: B | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

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U37B

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14

RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29 RSVD30 RSVD31 SA_MA_14 SB_MA_14 RSVD34 RSVD35 RSVD36 LVDSA_DATA#_3 LVDSA_DATA_3 RSVD39 RSVD40 RSVD41 RSVD42 RSVD43 RSVD44 RSVD45

<14> DDRA_SMA14
<14,15> DDRB_SMA14

9/20 Modify NB symbol for Pin BJ29/BE24/C48/D47

CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM_BM_BUSY#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR

If THERMTRIP no used, left NC

Use VGATE for GMCH_PWROK

NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16

CRESTLINE_1p0
PM@

DDR MUXING

SM_CK_0 SM_CK_1 SM_CK_3 SM_CK_4 → DDRA_CLK0 <14>, DDRA_CLK1 <14>, DDRB_CLK0 <15>, DDRB_CLK1 <15>

SM_CK#_0 SM_CK#_1 SM_CK#_3 SM_CK#_4 → DDRA_CLK0# <14>, DDRA_CLK1# <14>, DDRB_CLK0# <15>, DDRB_CLK1# <15>

SM_CKE_0 SM_CKE_1 SM_CKE_3 SM_CKE_4 → DDRA_CKE0 <14>, DDRA_CKE1 <14>, DDRB_CKE0 <15>, DDRB_CKE1 <15>

SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 → DDRA_SCS0# <14>, DDRA_SCS1# <14>, DDRB_SCS0# <15>, DDRB_SCS1# <15>

SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 → DDRA_ODT0 <14>, DDRA_ODT1 <14>, DDRB_ODT0 <15>, DDRB_ODT1 <15>

SM_RCOMP → SMRCOMP (R516 20_0402_1%)
SM_RCOMP# → SMRCOMP# (R517 20_0402_1%)

SM_RCOMP_VOH → SM_RCOMP_VOH
SM_RCOMP_VOL → SM_RCOMP_VOL

SM_VREF_0 SM_VREF_1 → SM_VREF

20mil

+1.8V
R518 1K_0402_1%
C639 0.1U_0402_16V4Z
R520 1K_0402_1%

CLK

DPLL_REF_CLK → CLK_DREF_96M <16>
DPLL_REF_CLK# → CLK_DREF_96M# <16>
DPLL_REF_SSCLK → CLK_DREF_SSC <16>
DPLL_REF_SSCLK# → CLK_DREF_SSC# <16>

PEG_CLK → CLK_MCH_3GPLL <16>
PEG_CLK# → CLK_MCH_3GPLL# <16>

DMI

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 → DMI_ITX_MRX_N0 <22>, DMI_ITX_MRX_N1 <22>, DMI_ITX_MRX_N2 <22>, DMI_ITX_MRX_N3 <22>

DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 → DMI_ITX_MRX_P0 <22>, DMI_ITX_MRX_P1 <22>, DMI_ITX_MRX_P2 <22>, DMI_ITX_MRX_P3 <22>

DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 → DMI_MTX_IRX_N0 <22>, DMI_MTX_IRX_N1 <22>, DMI_MTX_IRX_N2 <22>, DMI_MTX_IRX_N3 <22>

DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 → DMI_MTX_IRX_P0 <22>, DMI_MTX_IRX_P1 <22>, DMI_MTX_IRX_P2 <22>, DMI_MTX_IRX_P3 <22>

GRAPHICS VID

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VR_EN

MISC

CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF → CL_CLK0 <22>, CL_DATA0 <22>, CL_PWROK <22>, CL_RST# <22>

C640 0.1U_0402_16V4Z
R528 1K_0402_1%
R531 392_0402_1%
+1.25VS

SDVO_CTRL_CLK SDVO_CTRL_DATA → MCH_CLKREQ# <16>, MCH_ICH_SYNC# <22>

TEST_1 R537 0_0402_5%
TEST_2 R538 20K_0402_5%

Layout Note:
SM_VREF trace width and spacing is 20/20.

+1.8V
R513 1K_0402_1%
SM_RCOMP_VOH
C635 2.2U_0805_10V6K
C636 0.01U_0402_16V7K
R514 3.01K_0402_1%
SM_RCOMP_VOL
R515 1K_0402_1%
C637 2.2U_0805_10V6K
C638 0.01U_0402_16V7K

+1.05VS
CLK_DREF_96M# R574 PM@ 0_0402_5%
CLK_DREF_SSC# R575 PM@ 0_0402_5%
CLK_DREF_96M R576 PM@ 0_0402_5%
CLK_DREF_SSC R577 PM@ 0_0402_5%

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

Strap Pin Table

CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present

MCH_CFG_5 R521 @4.02K_0402_1%
MCH_CFG_9 R522 @4.02K_0402_1%
MCH_CFG_12 R523 @4.02K_0402_1%
MCH_CFG_13 R524 @4.02K_0402_1%
MCH_CFG_16 R526 @4.02K_0402_1%
MCH_CFG_19 R529 @4.02K_0402_1% +3VS
MCH_CFG_20 R530 @4.02K_0402_1%

PM_EXTTS#0 R532 10K_0402_5% +3VS
PM_EXTTS#1 R534 10K_0402_5%
MCH_CLKREQ# R536 10K_0402_5%
SDVO_CTRL_CLK R578 @ 0_0402_5%
SDVO_CTRL_DATA R579 @ 0_0402_5%

Security Classification	Compal Secret Data		
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Title: Crestline (2/7)-DMI/DDR

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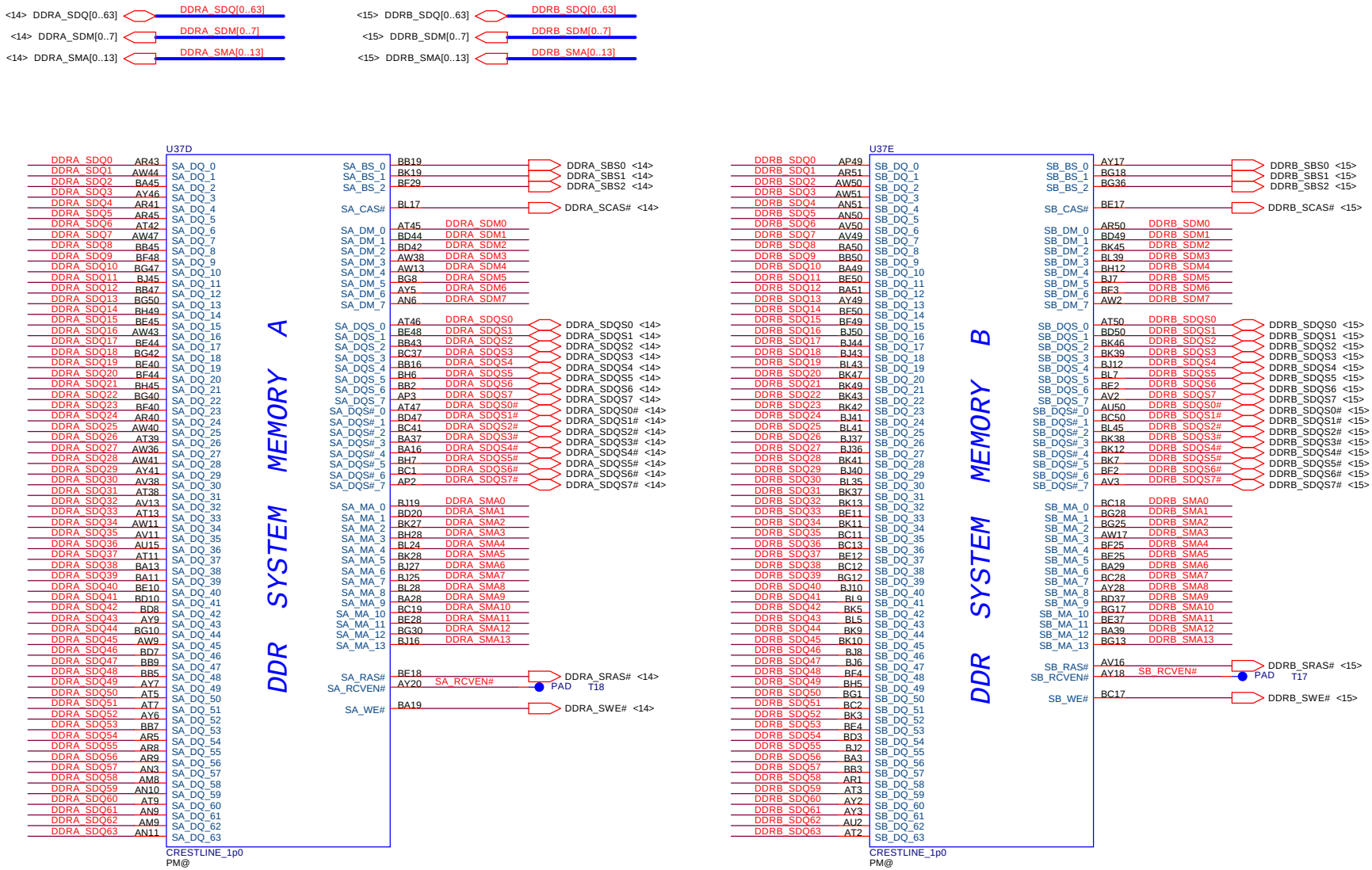

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Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Crestline (3/7)-DDRII

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

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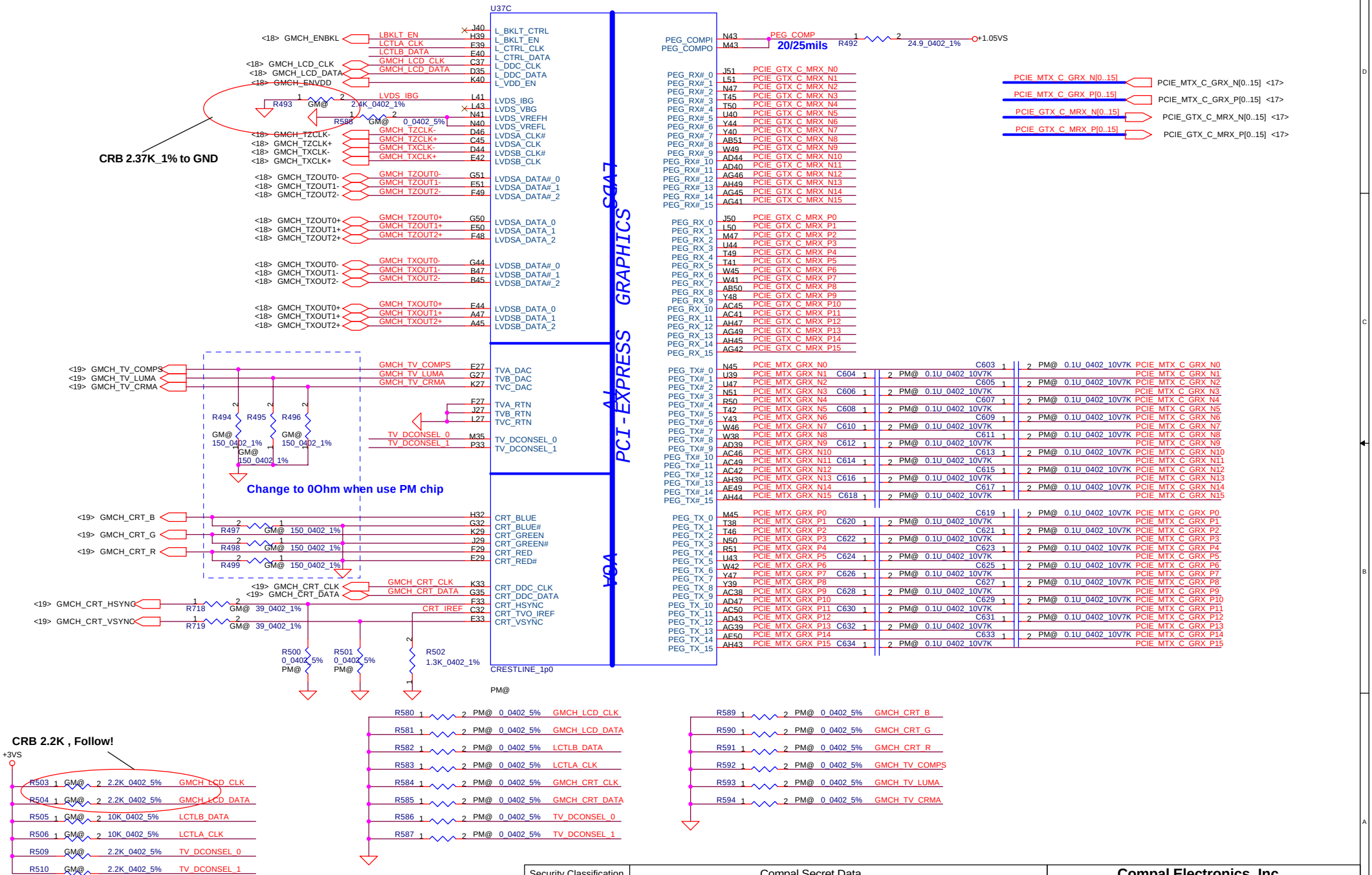

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Compal Electronics, Inc.

Title: Crestline (4/7)-VGA/LVDS/TV

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

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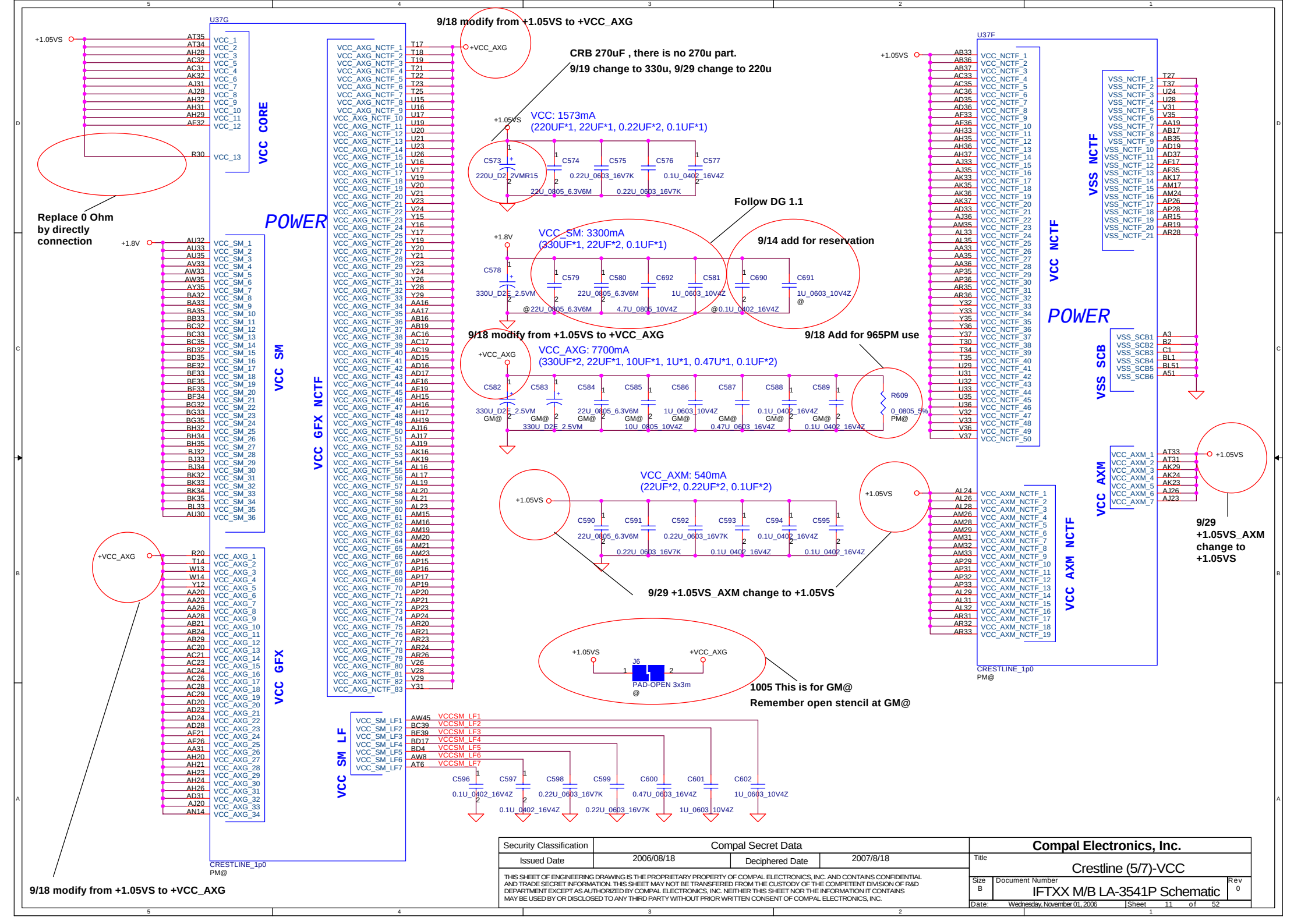

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Title: Crestline (5/7)-VCC

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

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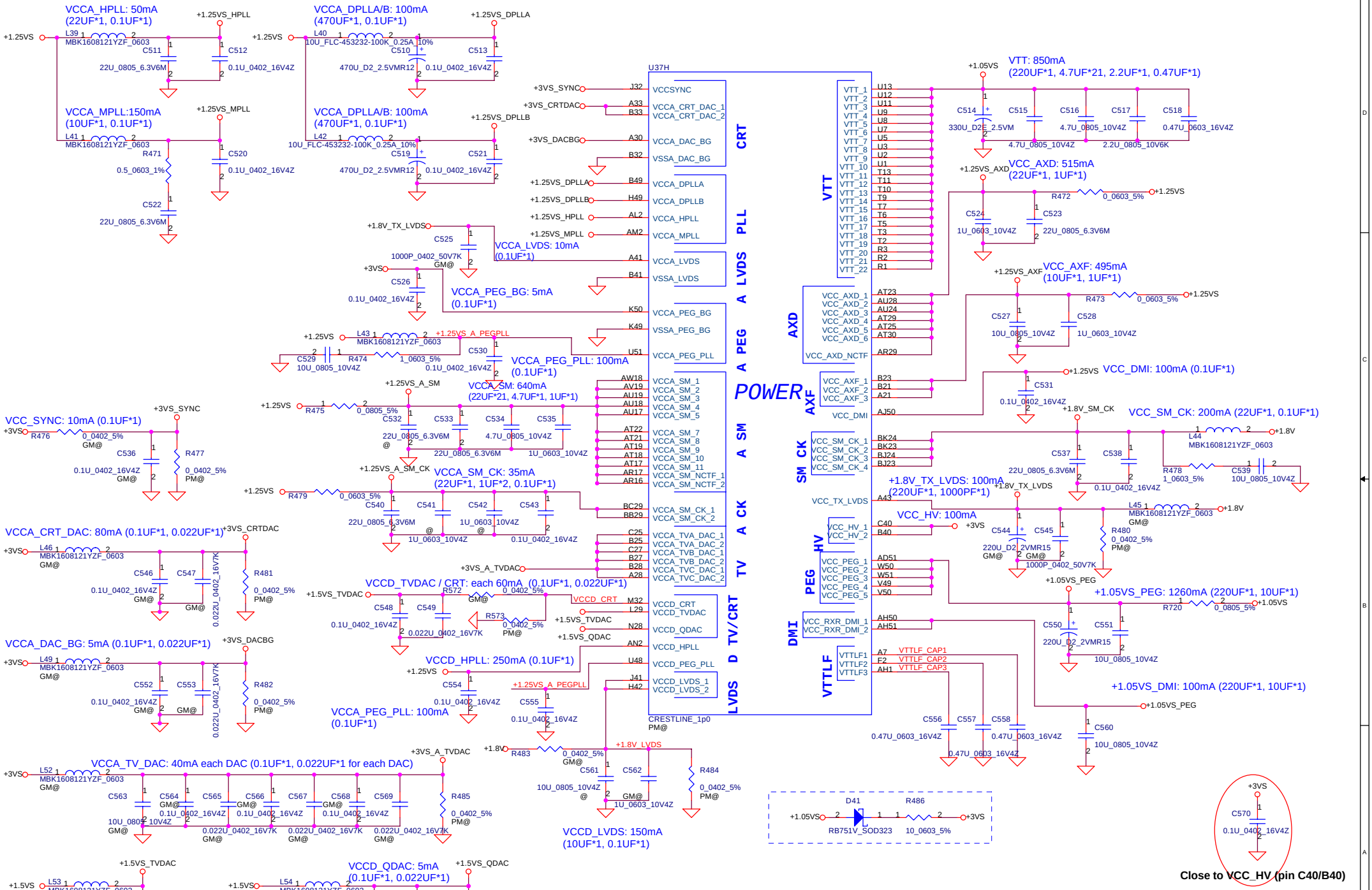

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Title: Crestline (6/7)-VCC

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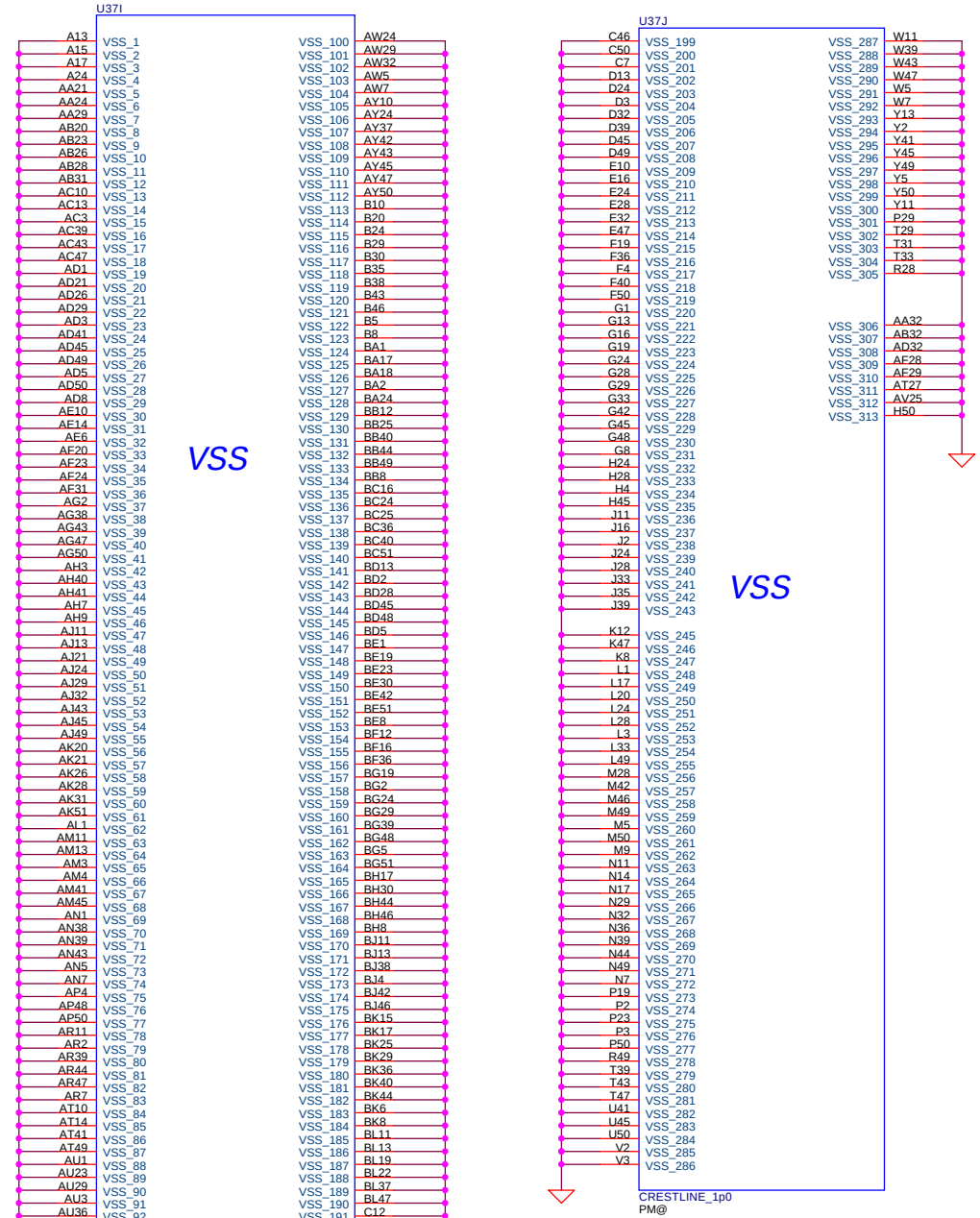

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Compal Electronics, Inc.

Title: Crestline (7/7)-GND

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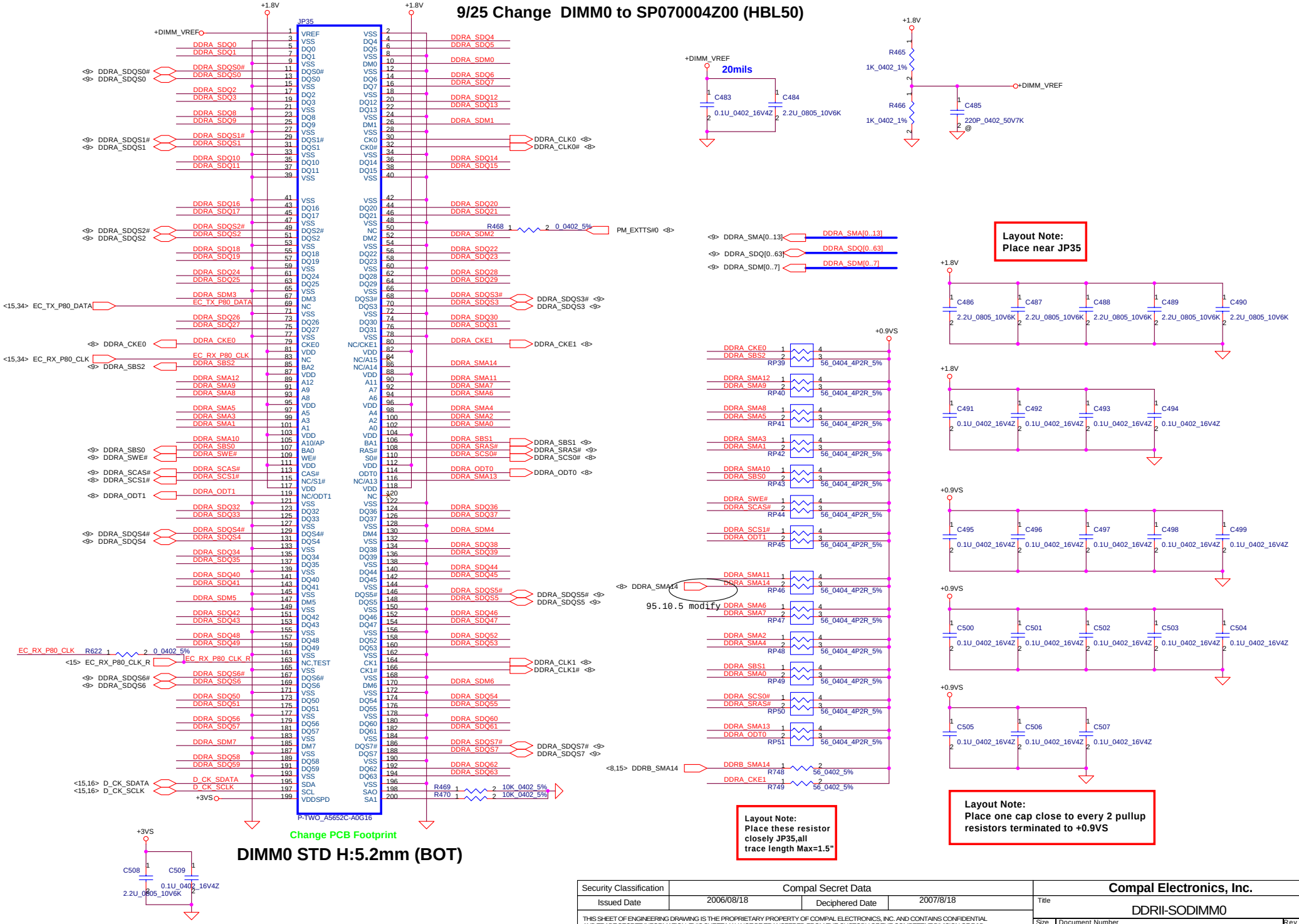
9/25 Change DIMM0 to SP070004Z00 (HBL50)



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DDRII-SODIMM0

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

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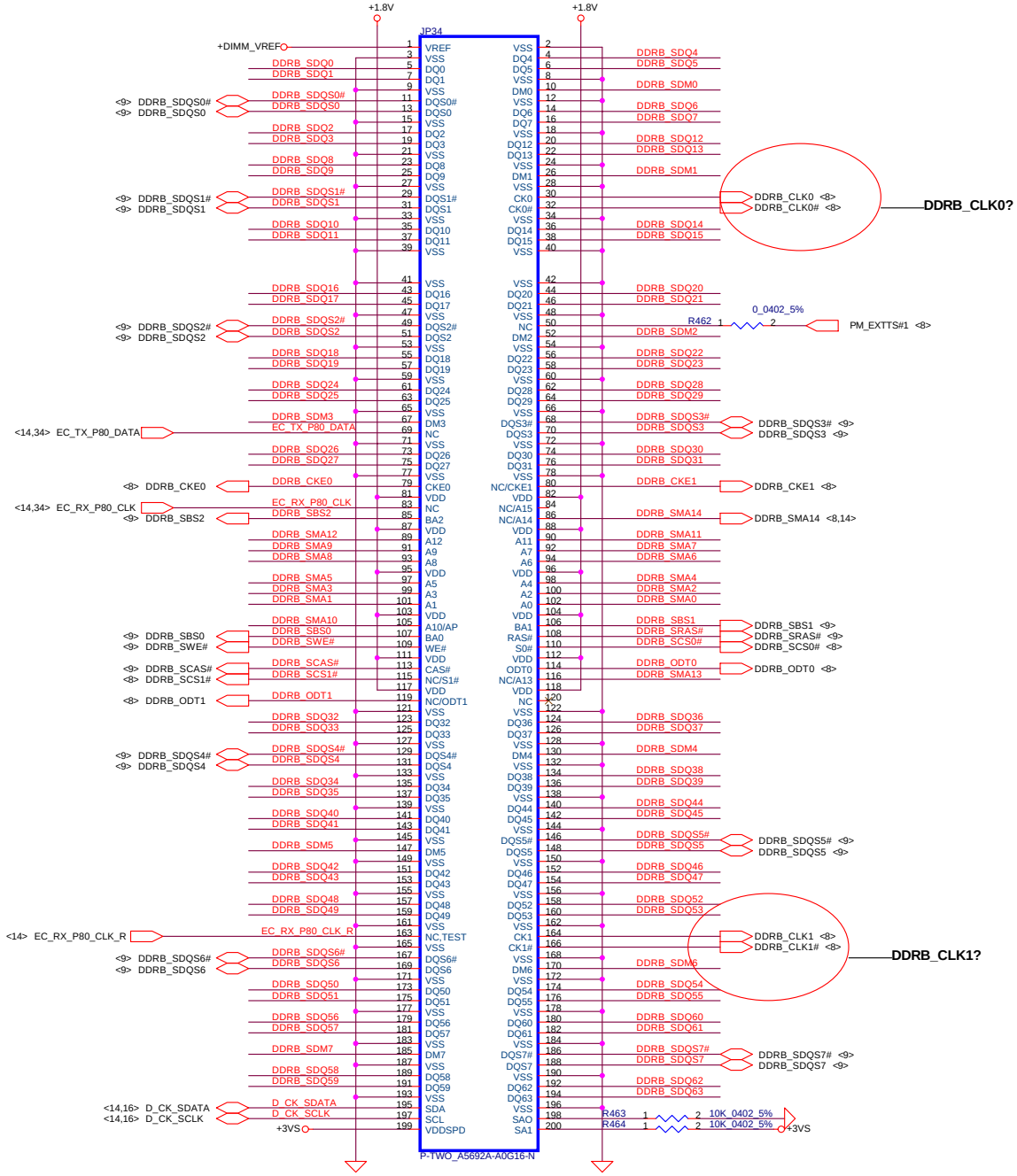
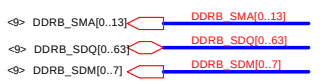
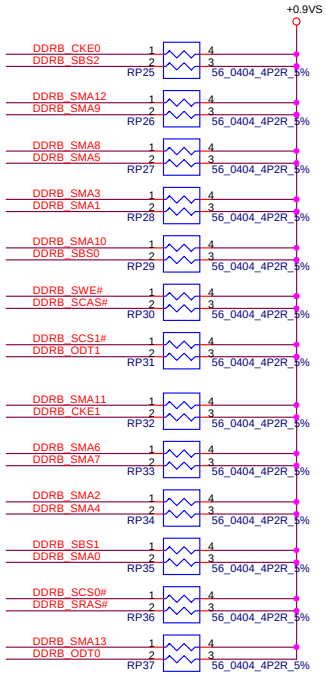
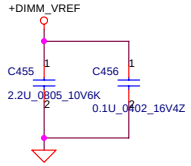
9/25 Change DIMM1 to SP070006F00

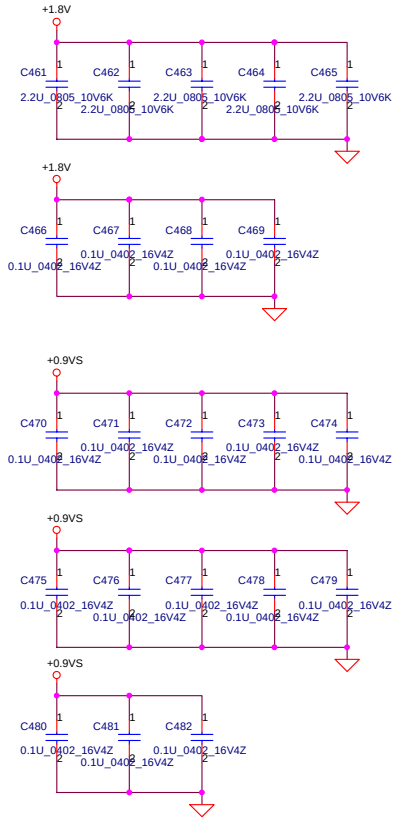








Layout Note:
Place near JP34



Layout Note:
Place these resistor closely JP35,all trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DIMM1 STD H:9.2mm (BOT)

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Title: DDRII-SODIMM1

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff						
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			

10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

Routing the trace at least 10mil

Place close to U35

ICS9LPRS365/SA00001GT00

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

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Title: Clock generator

Size: | Document Number: IXXXX LA-3XXXP | Rev: 0.1

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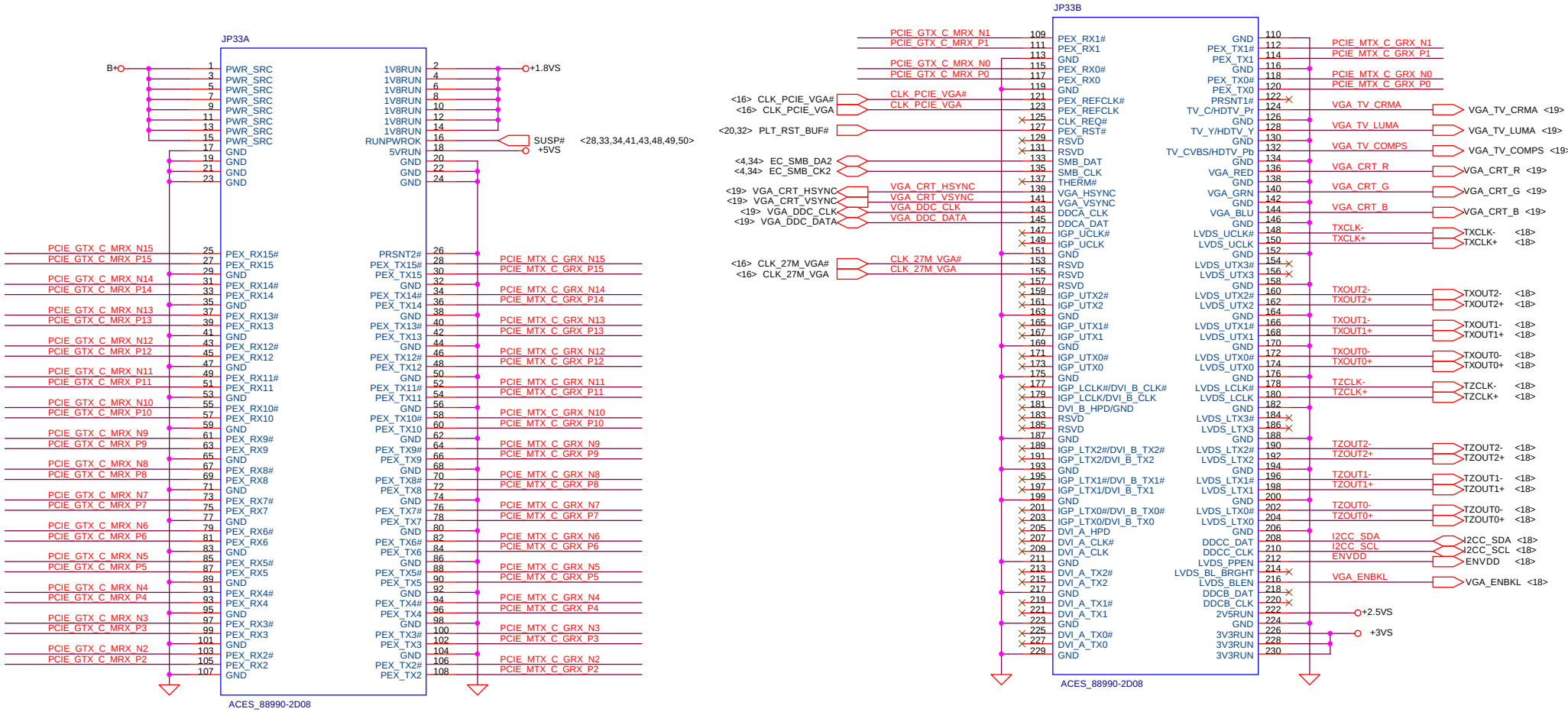
<10> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
<10> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
<10> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
<10> PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

9/13 modify this footprint from ACES_88990-2D08_230P to ACES_88990-2D28_230P



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Title: MXM Connector

Size: Custom | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

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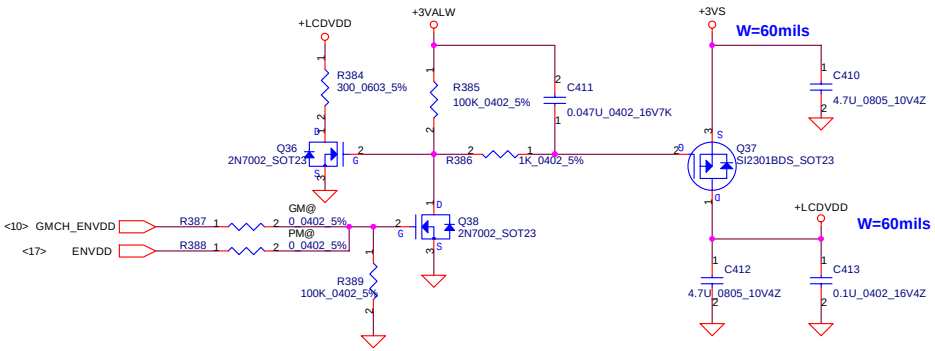
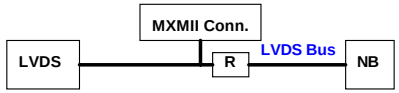
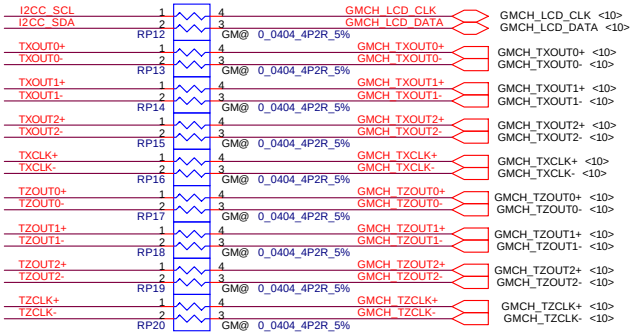
LCD POWER CIRCUIT



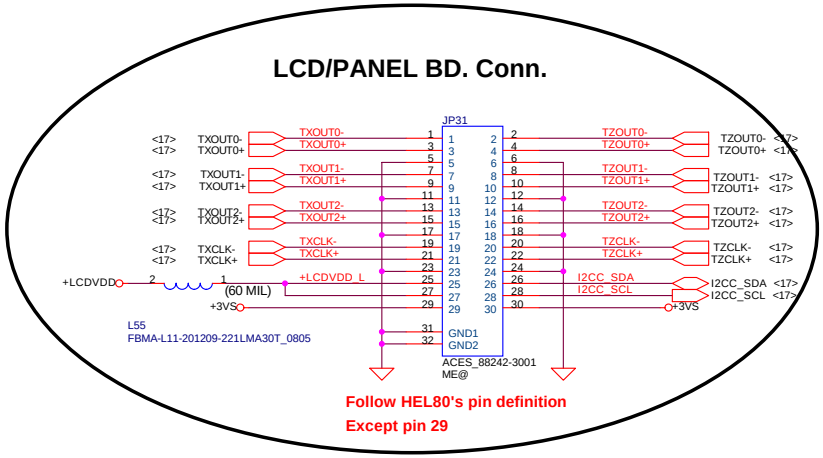
Routing Diagram



Use Daisy chain to route

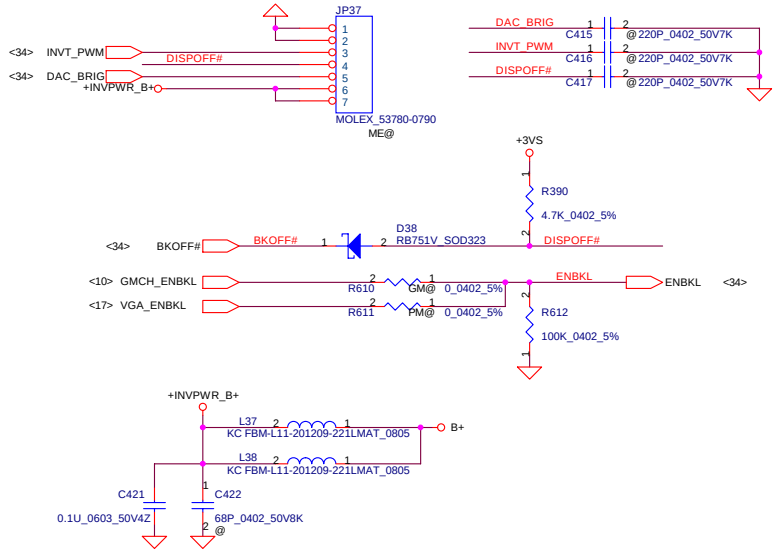


LCD/PANEL BD. Conn.

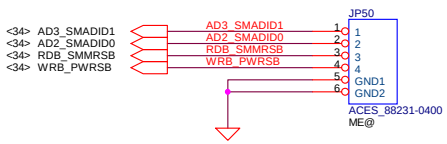


Follow HEL80's pin definition
Except pin 29

INVERTER Conn.



JEPICO Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

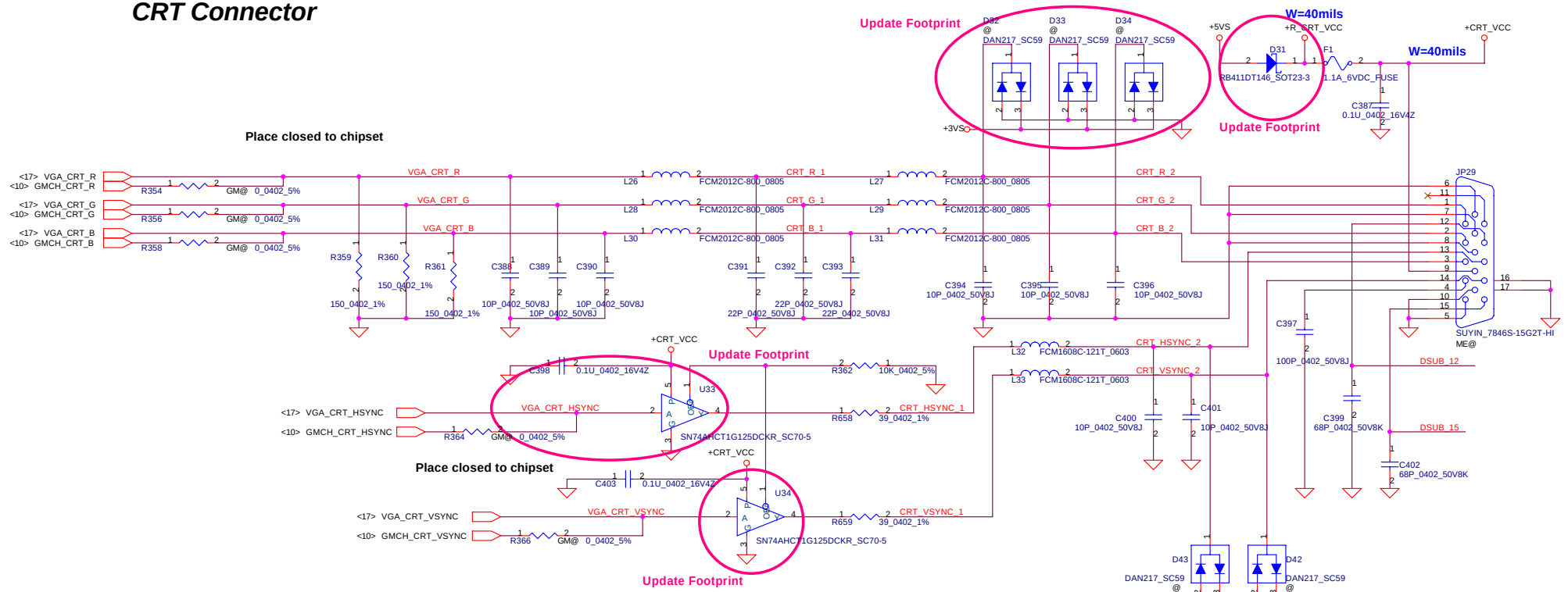
Compal Electronics, Inc.

Title: LVDS & DVI Connector

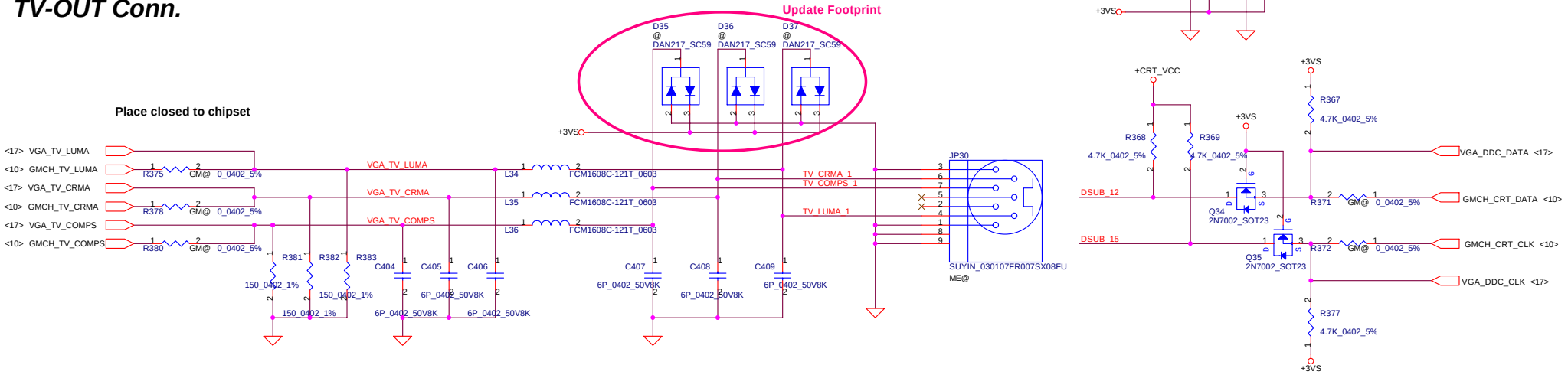
Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

Date: Wednesday, November 01, 2006 | Sheet 18 of 52

CRT Connector



TV-OUT Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

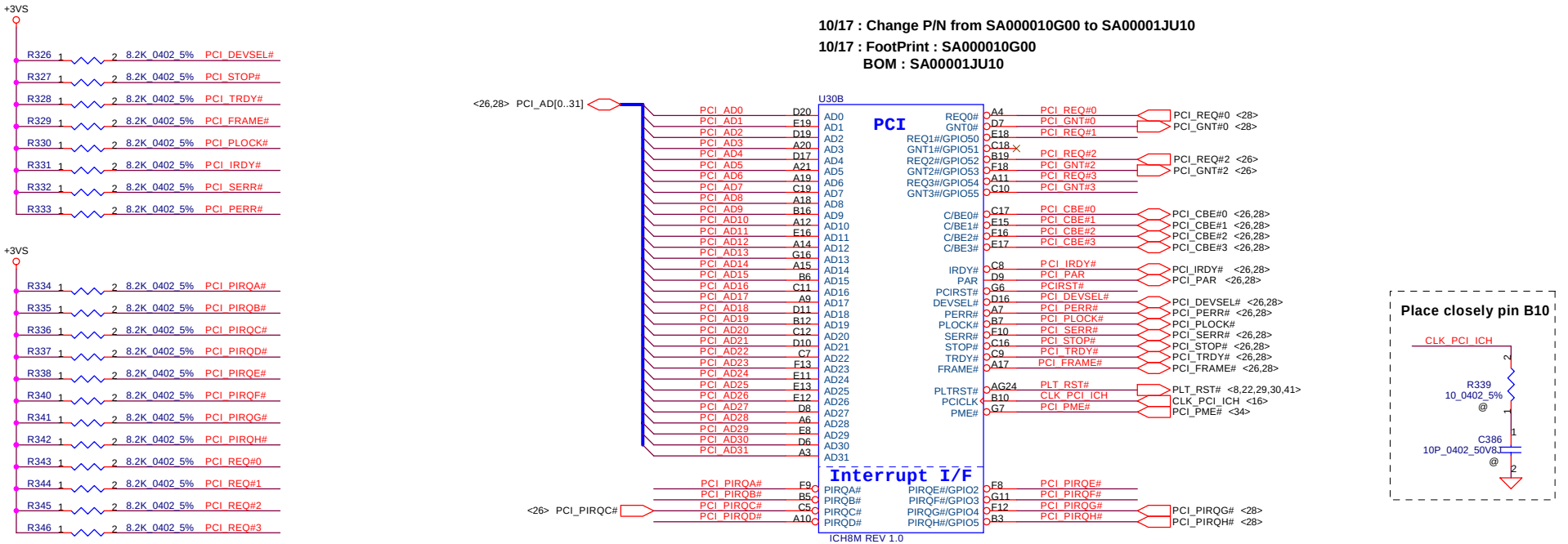
Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

Date: Wednesday, November 01, 2006 | Sheet 19 of 52

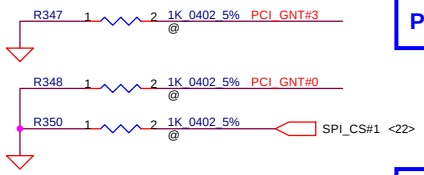
10/17 : Change P/N from SA000010G00 to SA00001JU10

10/17 : FootPrint : SA000010G00

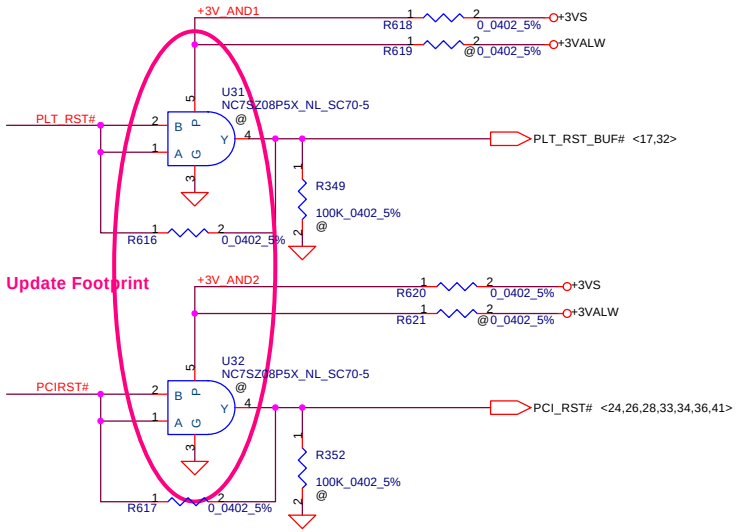
BOM : SA00001JU10



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



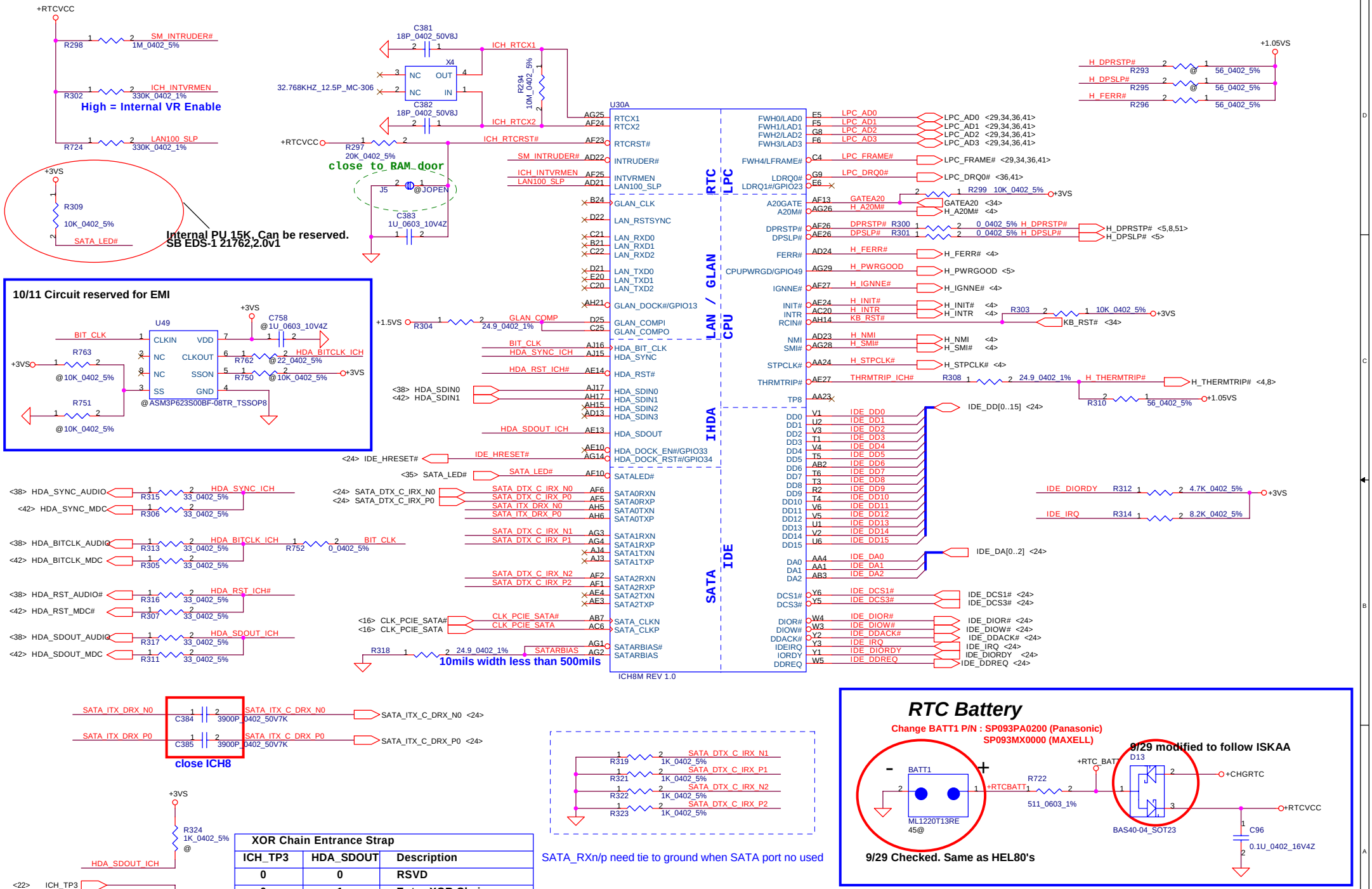
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: ICH8M(1/4)-PCI

Size | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

Date: Wednesday, November 01, 2006 | Sheet 20 of 52



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

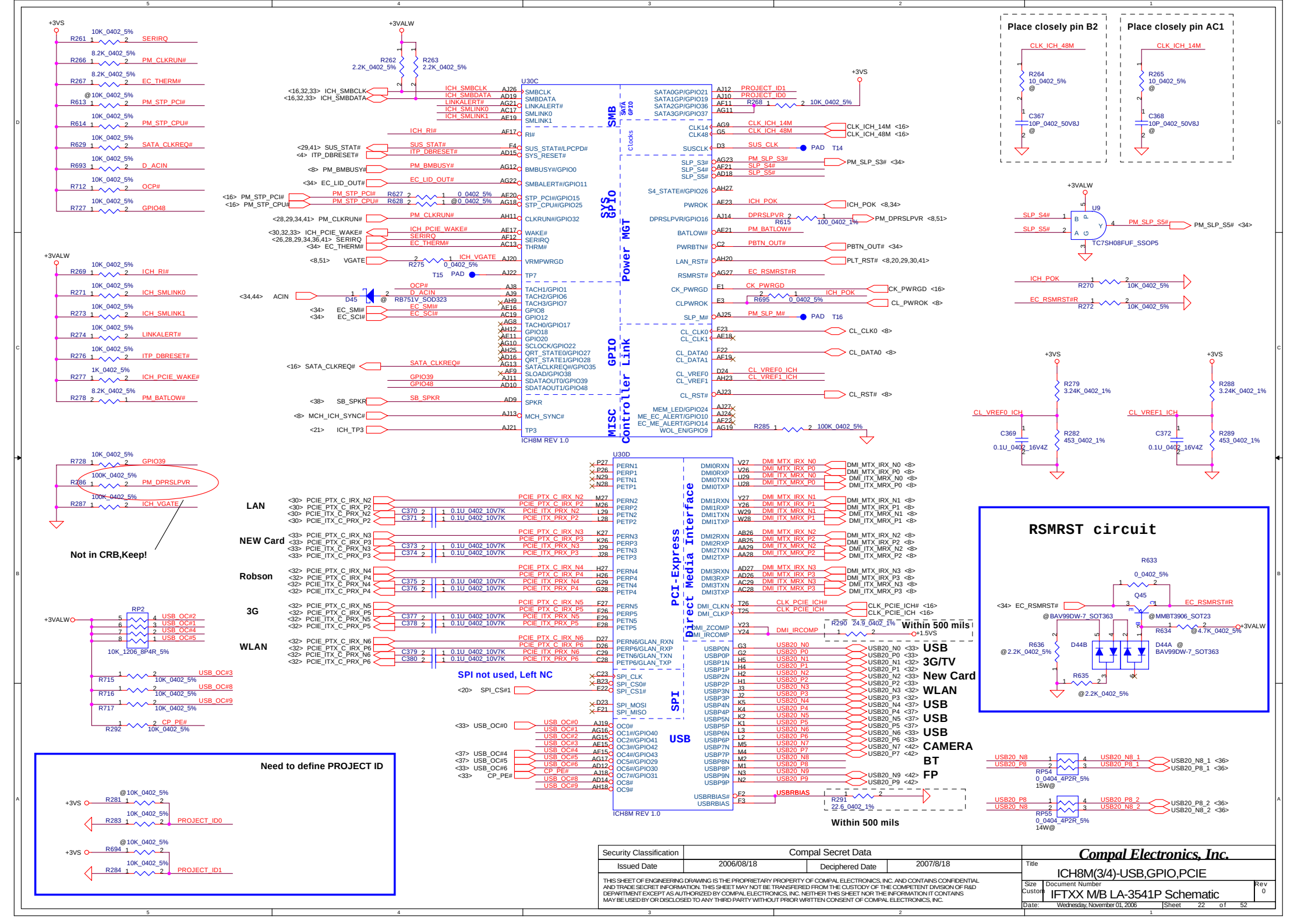
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: ICH8M(2/4)-LAN,IDELPC,RTC

Size: B | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

Date: Wednesday, November 01, 2006 | Sheet 21 of 52



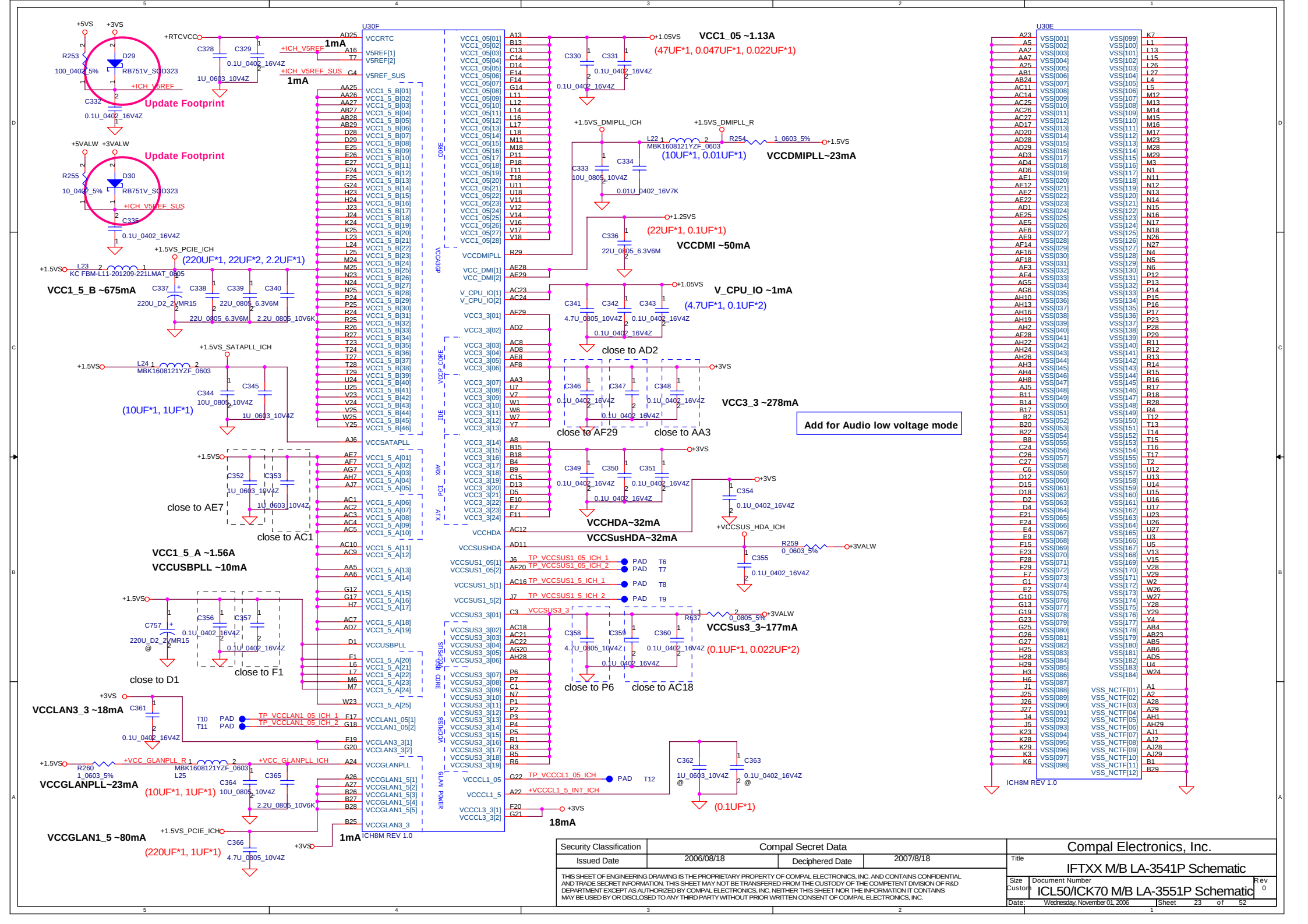
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: ICH8M(3/4)-USB,GPIO,PCIE

Size: Custom | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

Date: Wednesday, November 01, 2006 | Sheet 22 of 52



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

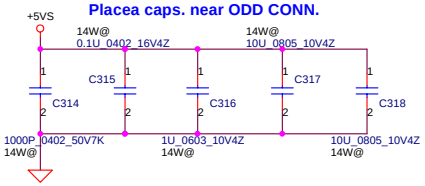
Title: IFTXX M/B LA-3541P Schematic

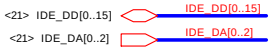
Size: Custom | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 0

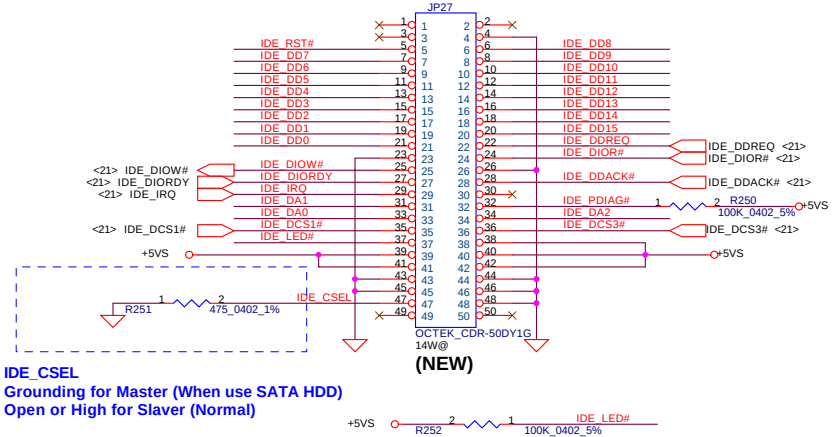
Date: Wednesday, November 01, 2006 | Sheet 23 of 52

14W ODD Conn.

Placea caps. near ODD CONN.

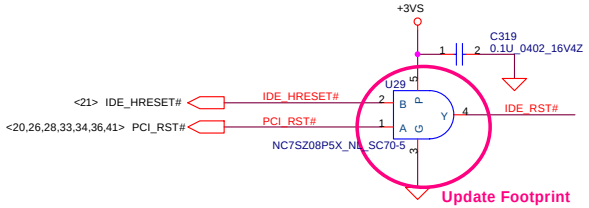






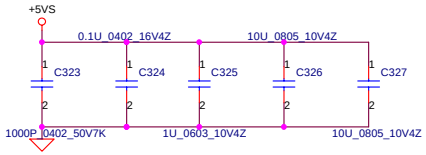
(NEW)

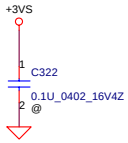
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

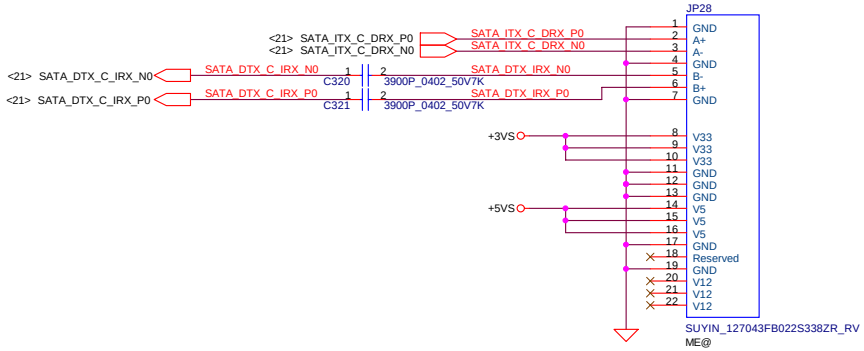


Update Footprint

SATA HDD Conn.



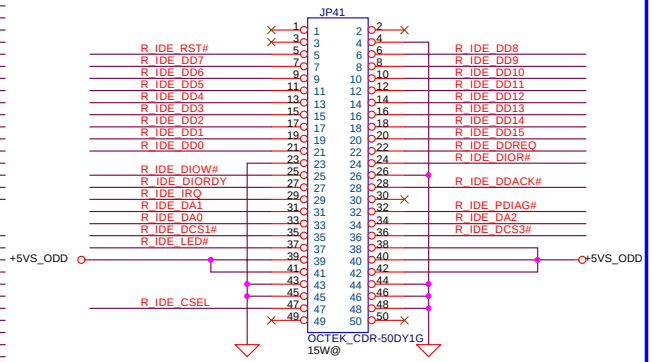


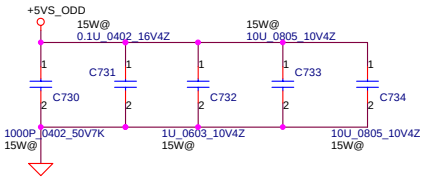


(NEW)
Change Library

15W ODD Conn.

Remember Short at 15W@





Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

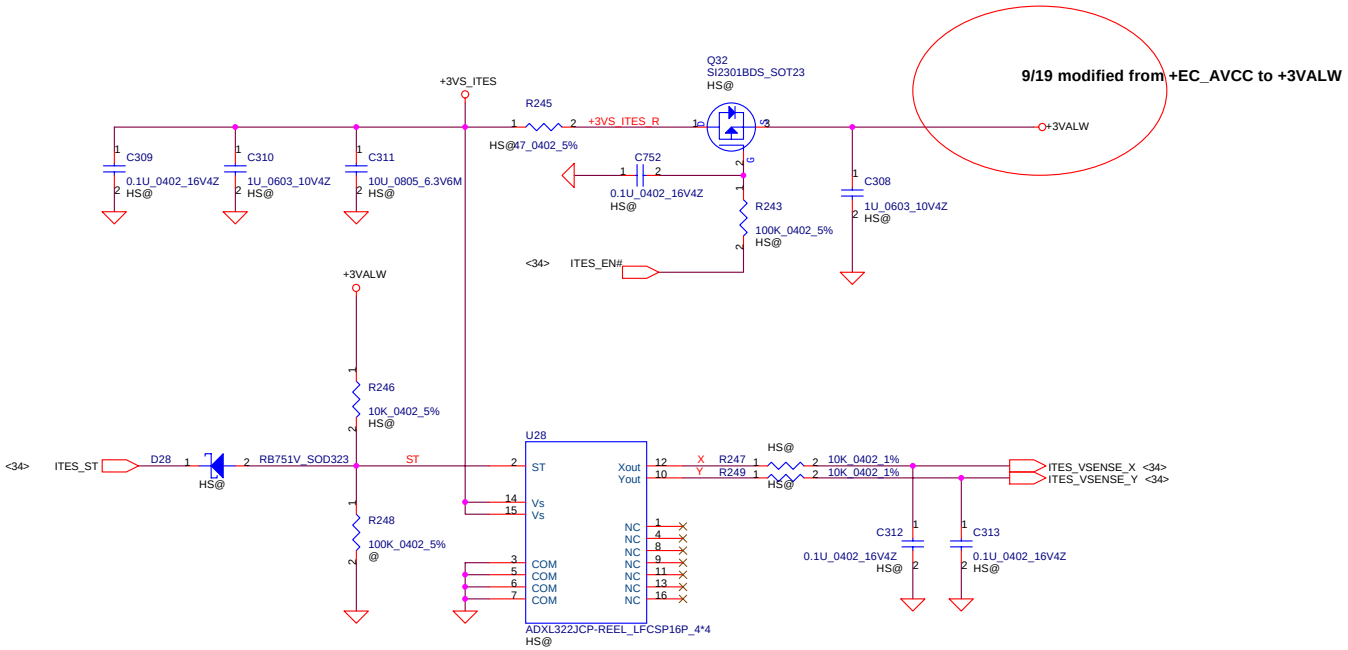
Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: B | Document Number: IFTXX M/B LA-3541P Schematic | Rev: 0

Date: Wednesday, November 01, 2006 | Sheet 24 of 52

Note : BOM structure HS@ is for Heng shan IFT10/11 this model



Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

Compal Electronics, Inc.

Title: CH7315A&HDMI Connector

Size	Document Number	Rev
B	LA-3541P	0.1

Date: Wednesday, November 01, 2006 | Sheet 25 of 52

IDSEL:AD20 (PIRQC#/D#, GNT#2, REQ#2)

PCMCIA Power Control

PCMCIA Socket

U44 — CB1410BFB0 LFBGA 144P — PCMCIA@

PCI Interface | CARDBUS | SD/MMC/MS/SM

NEED CHECK

10/17 : FootPrint : SA007140B10
BOM : SA014100310

CB1410 P/N: SA014100310

U43 — CP2211FD3_SSOP16 — PCMCIA@

JP40 — FOX_WZ221131-G2-8F_LT — PCMCIA@

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

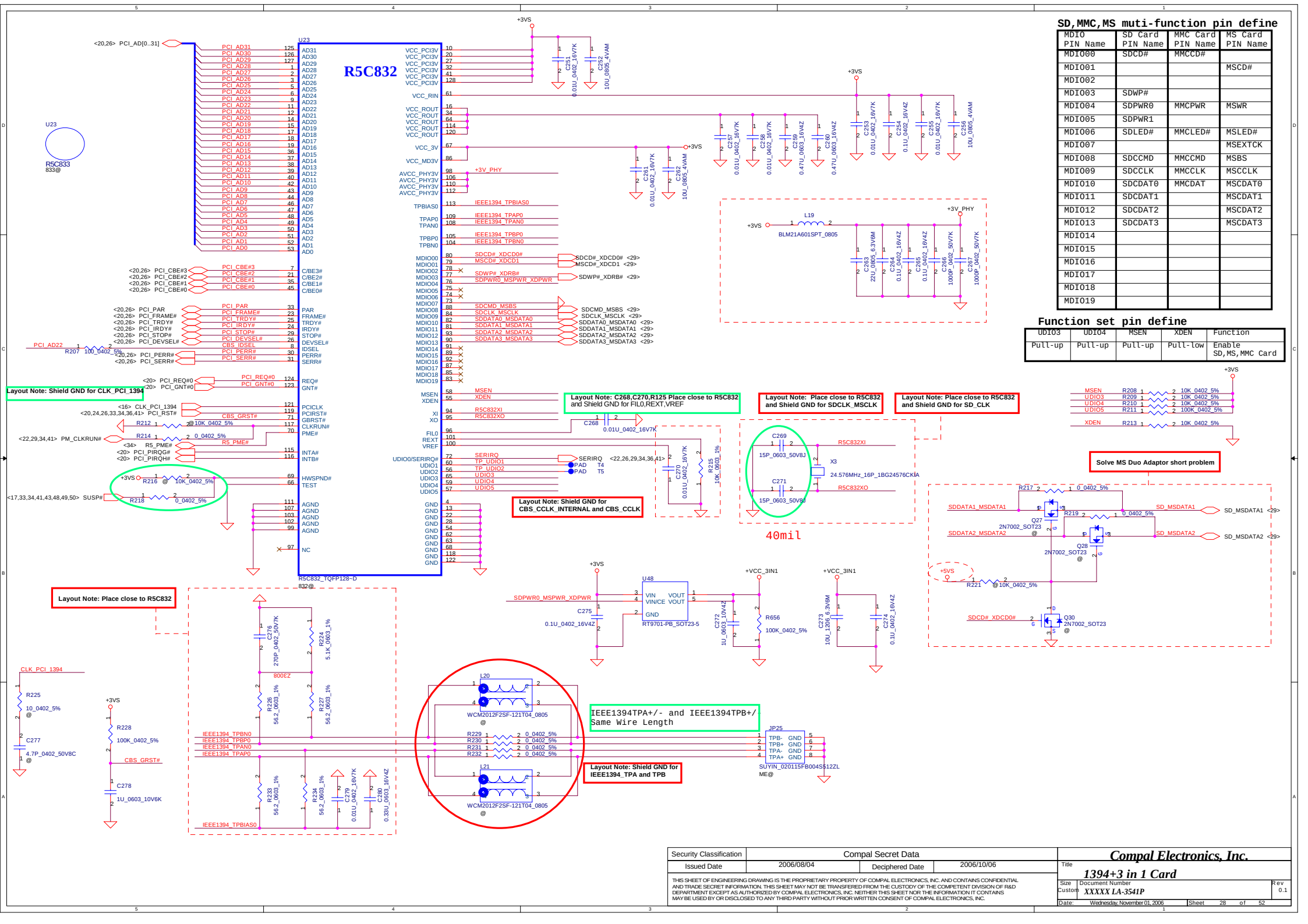
Compal Electronics, Inc.

Title: PCMCIA_ENE CB1410

Size: Custom | Document Number: IFTXX LA-3541P | Rev: 0.1

Date: Wednesday, November 01, 2006 | Sheet 26 of 52

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, November 01, 2006
Sheet	27 of 52


R5C832
U23
R5C833
833@
R5C832_TQFP128-D
832@
SD,MMC,MS muti-function pin define
MDIO PIN Name | SD Card PIN Name | MMC Card PIN Name | MS Card PIN Name
MDIO000 | SDCD# | MMCCD# |
MDIO001 | | | MSCD#
MDIO002 | | |
MDIO003 | SDWP# | |
MDIO004 | SDPWR0 | MMCPWR | MSWR
MDIO005 | SDPWR1 | |
MDIO006 | SDLED# | MMCLED# | MSLED#
MDIO007 | | | MSEXTCK
MDIO008 | SDCCMD | MMCCMD | MSBS
MDIO009 | SDCCLK | MMCCLK | MSCCLK
MDIO010 | SDCDAT0 | MMCDAT | MSCDAT0
MDIO011 | SDCDAT1 | | MSCDAT1
MDIO012 | SDCDAT2 | | MSCDAT2
MDIO013 | SDCDAT3 | | MSCDAT3
MDIO014
MDIO015
MDIO016
MDIO017
MDIO018
MDIO019
Function set pin define
UDIO3 | UDIO4 | MSEN | XDEN | Function
Pull-up | Pull-up | Pull-up | Pull-low | Enable SD,MS,MMC Card
Layout Note: Shield GND for CLK_PCI_1394
Layout Note: C268,C270,R125 Place close to R5C832 and Shield GND for FIL0,REXT,VREF
Layout Note: Place close to R5C832 and Shield GND for SDCLK_MSCLK
Layout Note: Place close to R5C832 and Shield GND for SD_CLK
Solve MS Duo Adaptor short problem
Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK
Layout Note: Place close to R5C832
40mil
IEEE1394TPA+/- and IEEE1394TPB+/- Same Wire Length
Layout Note: Shield GND for IEEE1394_TPA and TPB
Security Classification | Compal Secret Data
Issued Date | 2006/08/04 | Deciphered Date | 2006/10/06
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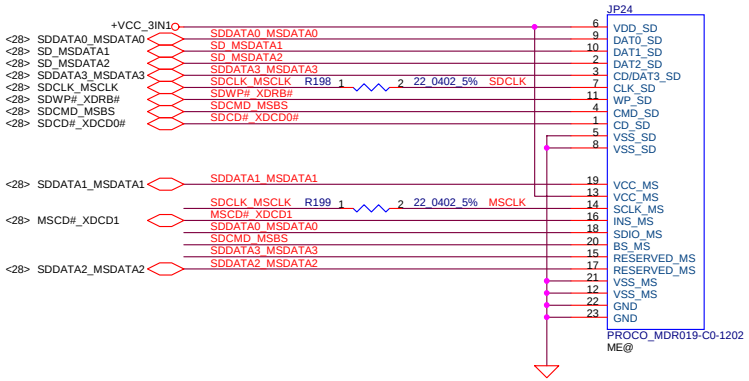
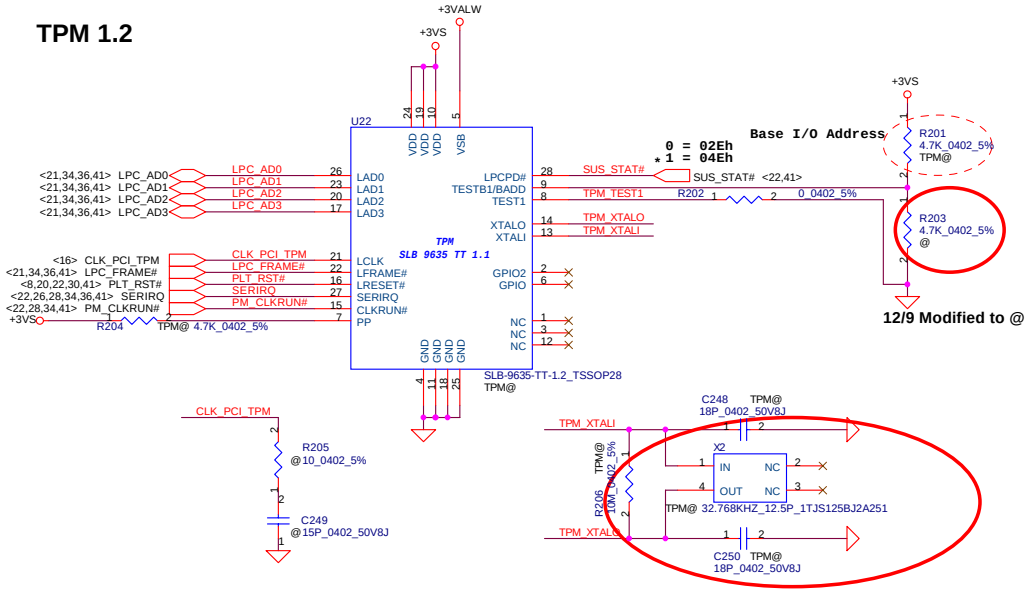
Compal Electronics, Inc.
Title: 1394+3 in 1 Card
Size: Custom | Document Number: XXXXX LA-3541P | Rev: 0.1
Date: Wednesday, November 01, 2006 | Sheet 28 of 52

3 in 1 Card Reader

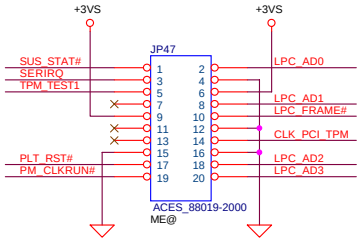


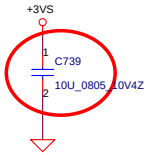
For A30

TPM 1.2



TPM Conn. For C38





Place this cap close to pin 6 and pin 9

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: INDICATE LED

Size	Document Number	Rev
Custom	XXXXX LA-3541P	0.1

Date: Wednesday, November 01, 2006 Sheet 29 of 52

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

Layout Notice : Filter place as close chip as possible.

close to pins 38, 45, and 52

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Change R311,R312 from 4.7k to 47k

9/14 change from 1.24K to 1K (By broadcom James)

No CIS Symbol

Add R346

Notice : 4.7u 6.3V capactor Thickness 1.25mm

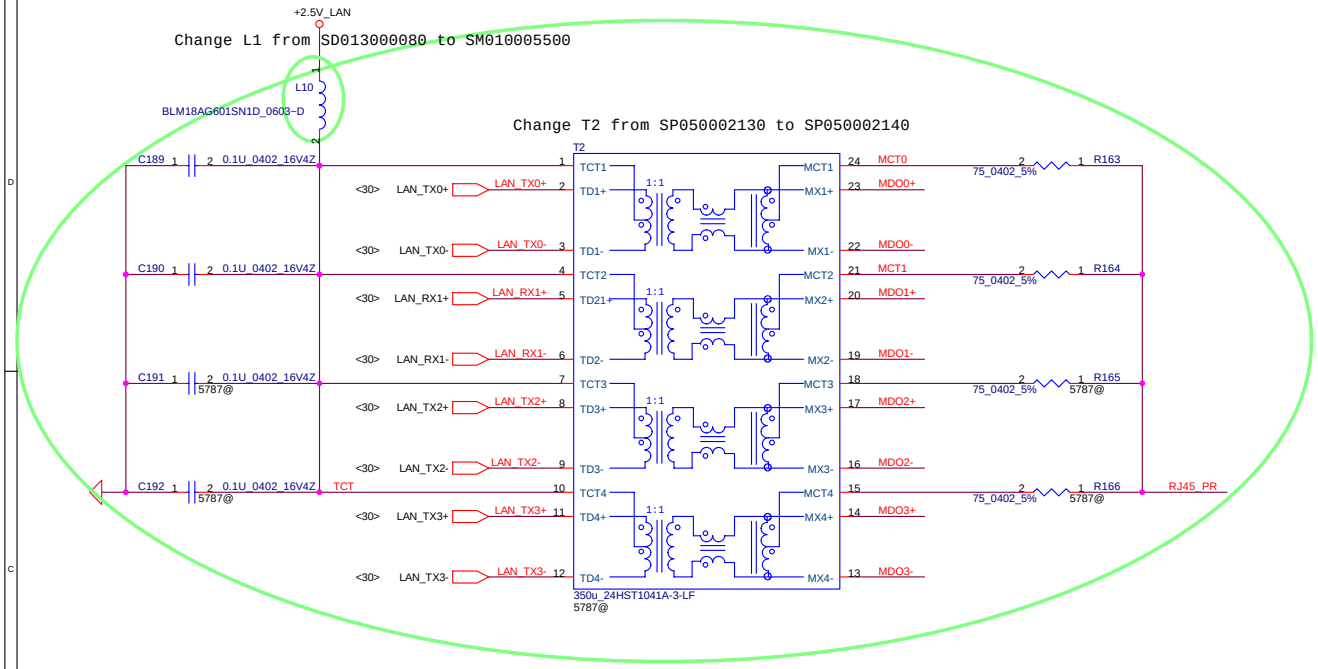
Layout Notice : Filter place as close chip as possible.

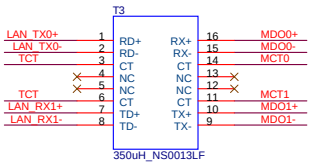
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Title	BCM5787MKML		
Size: Custom	Document Number: XXXXX LA-3541P		Rev: 0.1
Date: Wednesday, November 01, 2006	Sheet 30 of 52		

Change L1 from SD013000080 to SM010005500

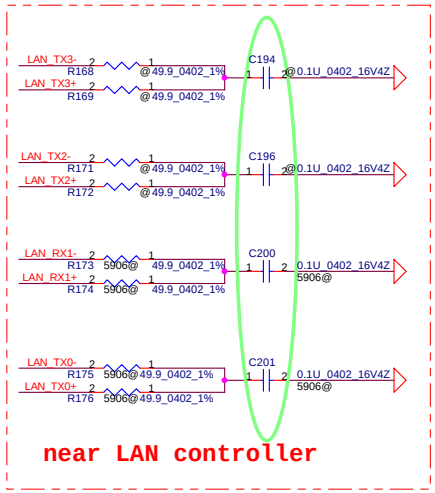
Change T2 from SP050002130 to SP050002140



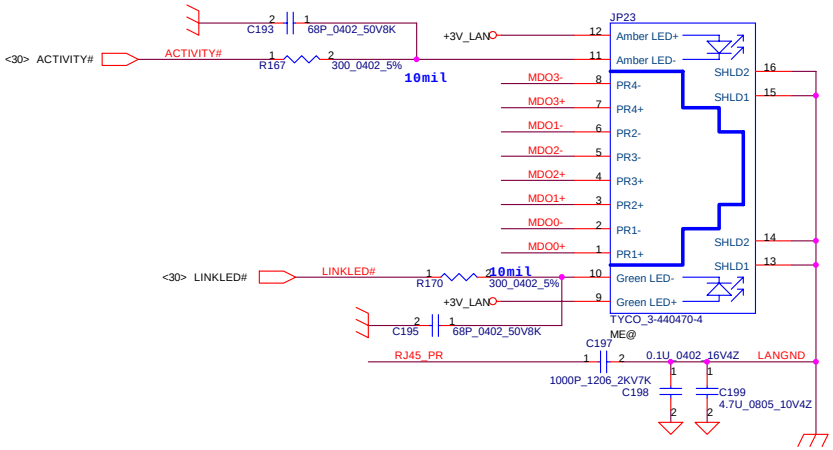


Change T1 from SP050001210 to SP050001210

Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



Lan Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

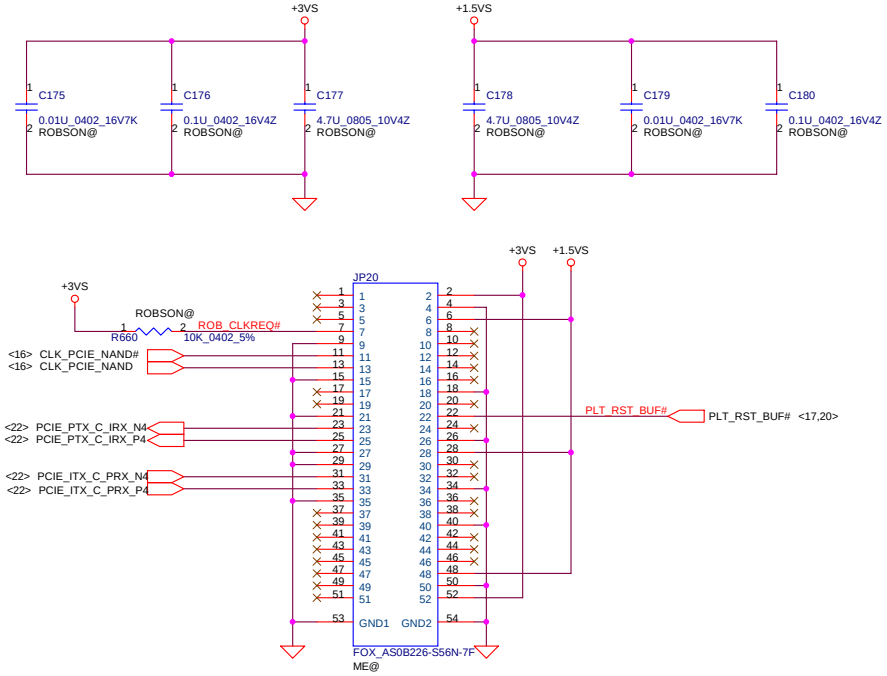
Compal Electronics, Inc.

Title: **LAN CONTROLLER**

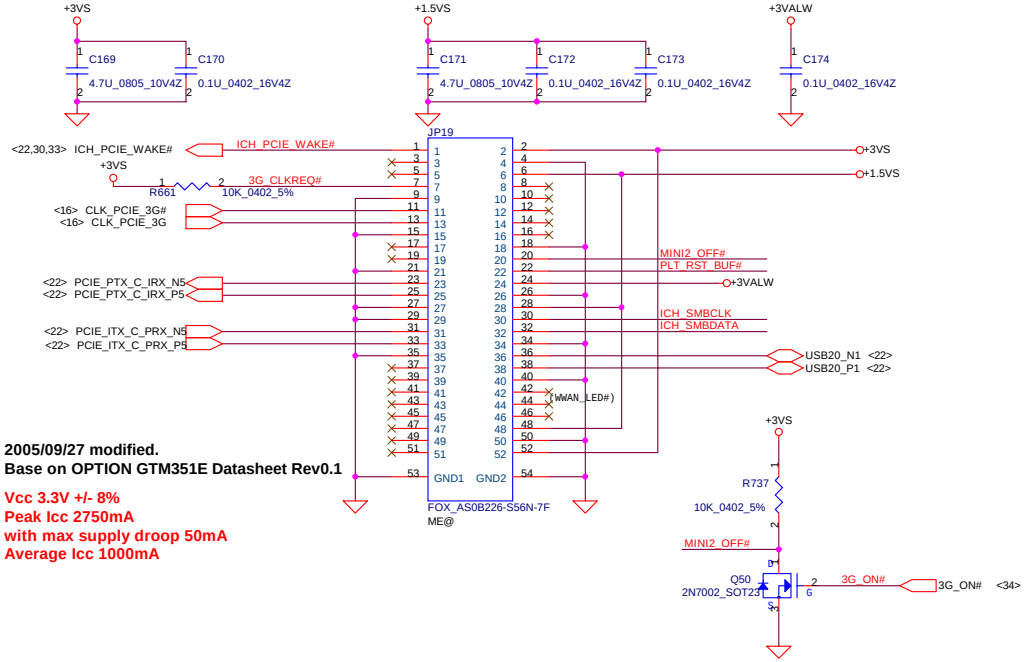
Size	Document Number	Rev
Custom	XXXXX LA-3541P	0.1

Date: Wednesday, November 01, 2006 | Sheet 31 of 52

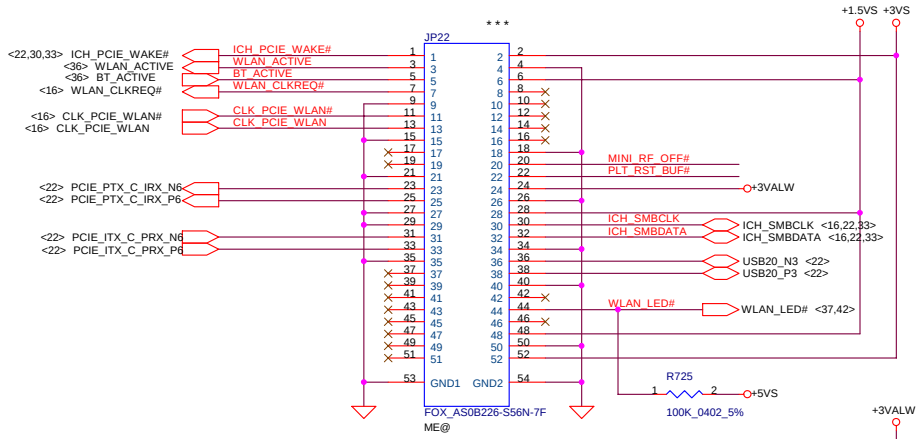
NAND mini Card(Robson support)

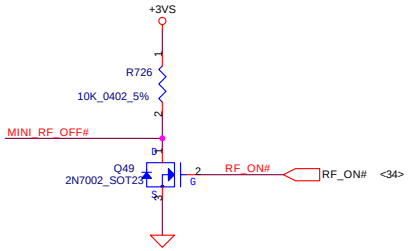


Mini-Express Card for 3G Or TV Tuner

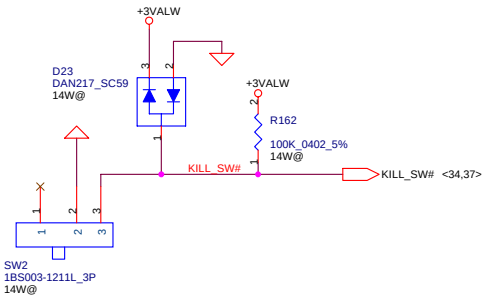


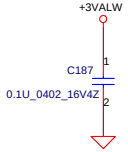
Mini-Express Card for WLAN

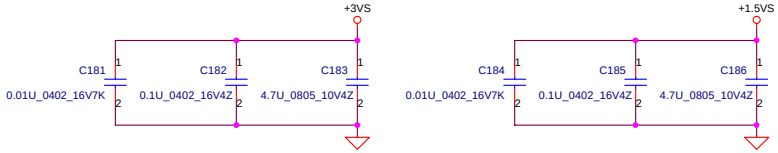




Kill SWITCH







Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

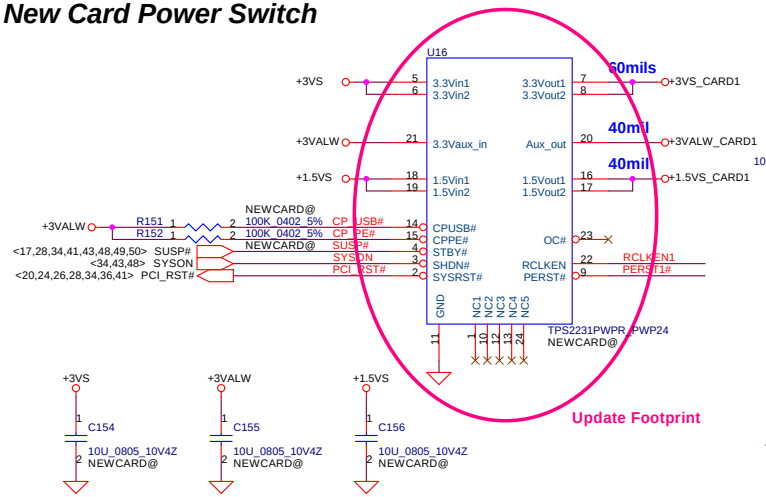
Compal Electronics, Inc.

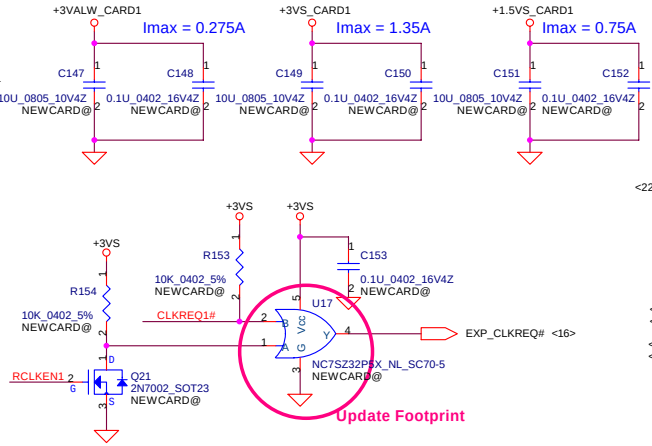
Title: **Mini-Card/3G/FeliCa/FP**

Size	Document Number	Rev
	LA-3541P	0.1

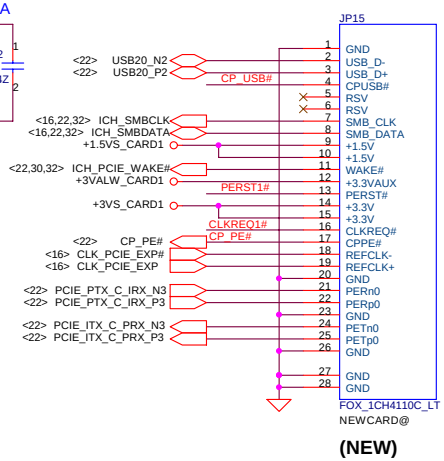
Date: Wednesday, November 01, 2006 | Sheet 32 of 52

New Card Power Switch



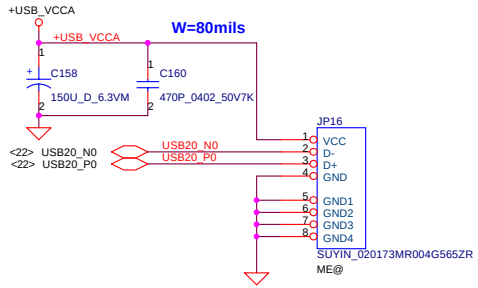


New Card Socket (Left/TOP)



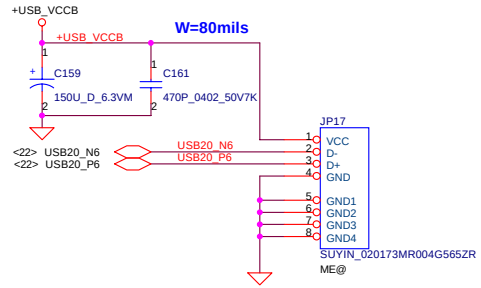
(NEW)

USB CONN. 1

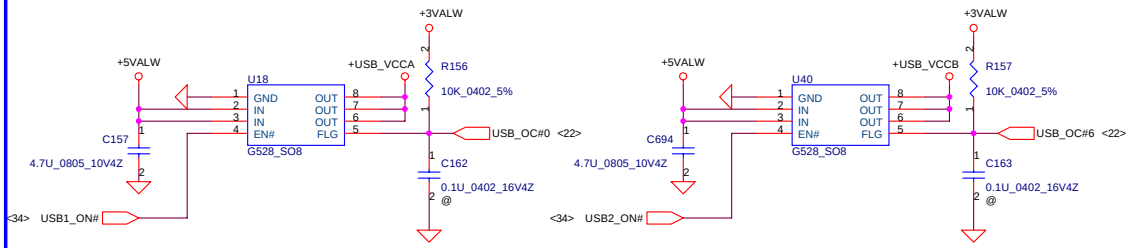


SUYIN_020173MR004G533ZR_4P

USB CONN. 2



SUYIN_020173MR004G533ZR_4P



9/17 modified this block

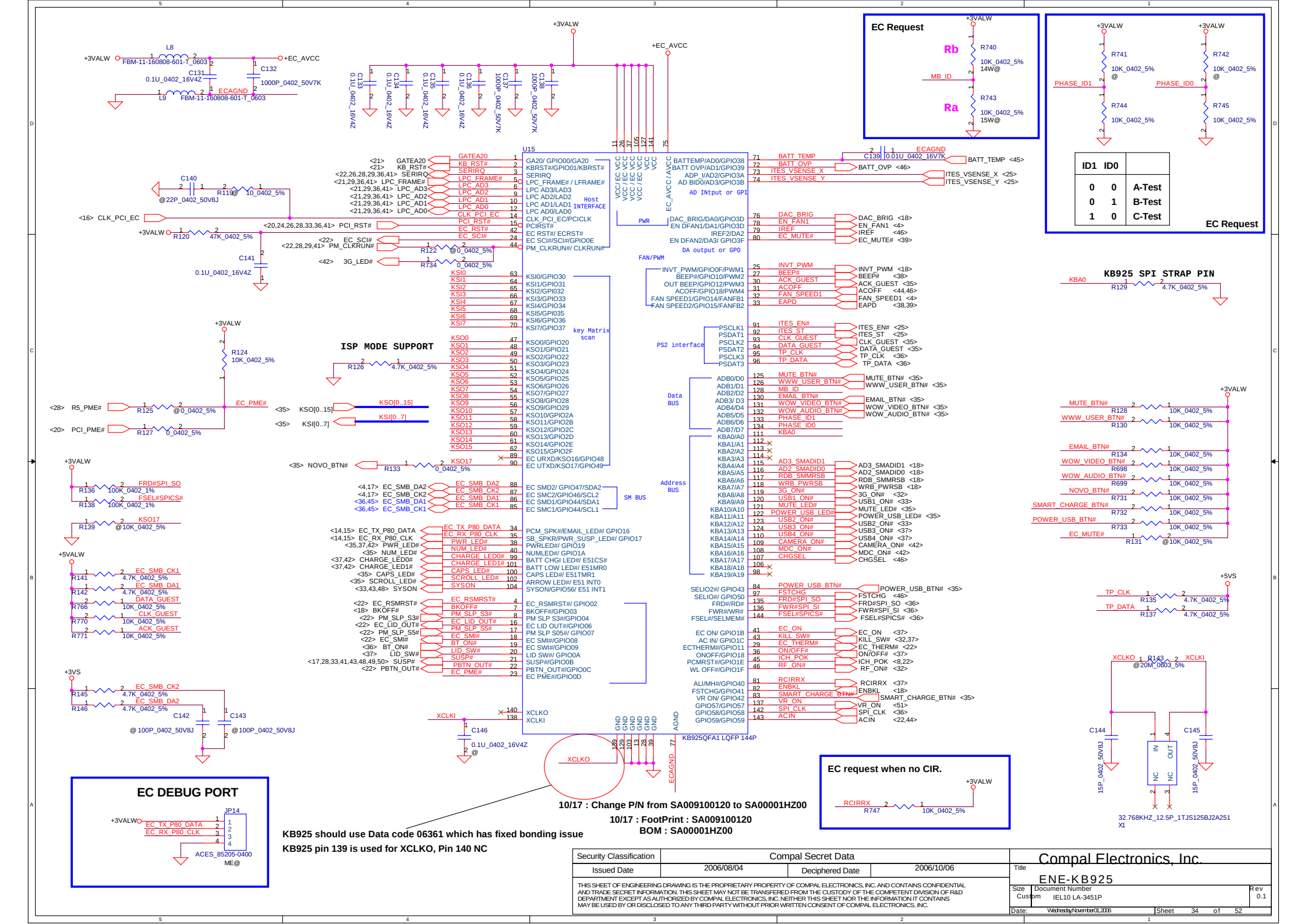
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: NEW CARD & USB Connector

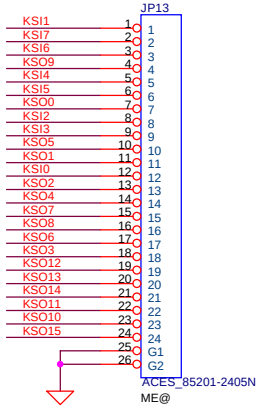
Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

Date: Wednesday, November 01, 2006 | Sheet 33 of 52

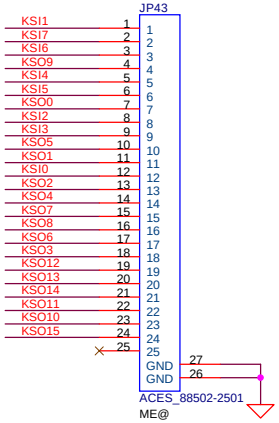

EC Request
Rb
R740
10K_0402_5%
14W@
MB_ID
Ra
R743
10K_0402_5%
15W@
+3VALW
PHASE_ID1
PHASE_ID0
R741
R742
R744
R745
10K_0402_5%
ID1 ID0
0 0 A-Test
0 1 B-Test
1 0 C-Test
EC Request
KB925 SPI STRAP PIN
KBA0
R129
4.7K_0402_5%
ISP MODE SUPPORT
U15
KB925QFA1 LQFP 144P
EC DEBUG PORT
JP14
ACES_85205-0400
ME@
EC request when no CIR.
RCIRRX
R747
10K_0402_5%
32.768KHZ_12.5P_1TJS125BJ2A251
X1
10/17 : Change P/N from SA009100120 to SA00001HZ00
10/17 : FootPrint : SA009100120
BOM : SA00001HZ00
KB925 should use Data code 06361 which has fixed bonding issue
KB925 pin 139 is used for XCLKO, Pin 140 NC
Security Classification
Compal Secret Data
Issued Date
2006/08/04
Deciphered Date
2006/10/06
Compal Electronics, Inc.
ENE-KB925
Size
Custom
Document Number
IEL10 LA-3451P
Rev
0.1
Date:
Wednesday, November 01, 2006
Sheet
34
of
52

INT_KBD Conn.

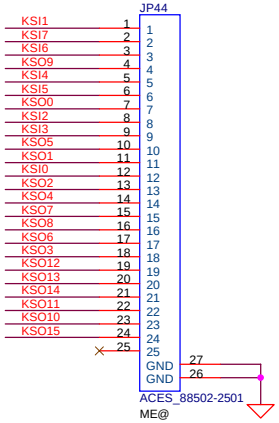
For IFT10

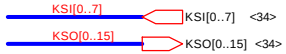


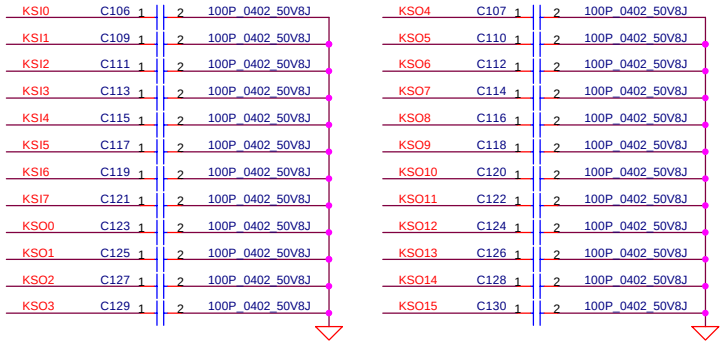
For IFL90



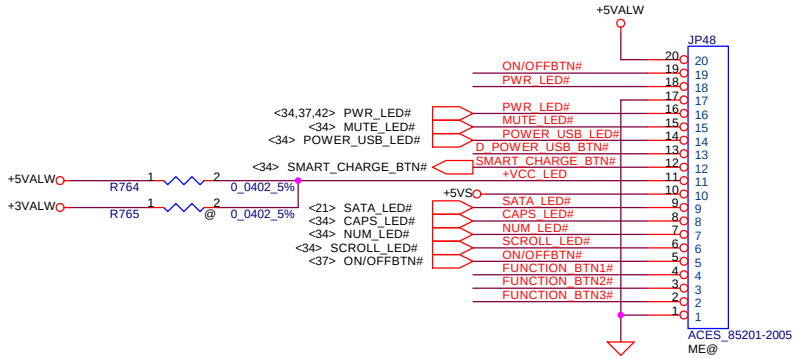
For IFT00

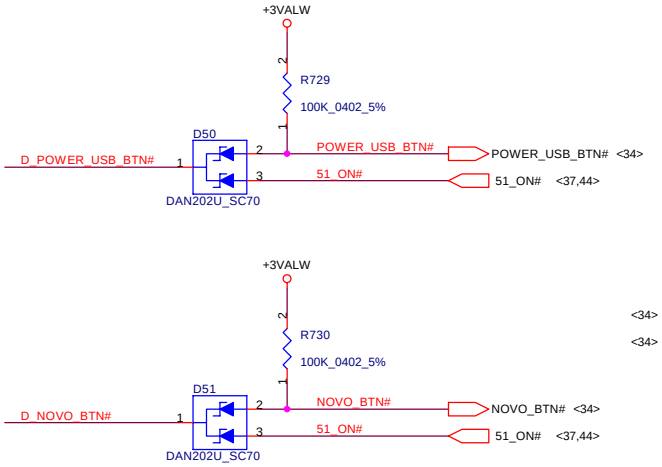


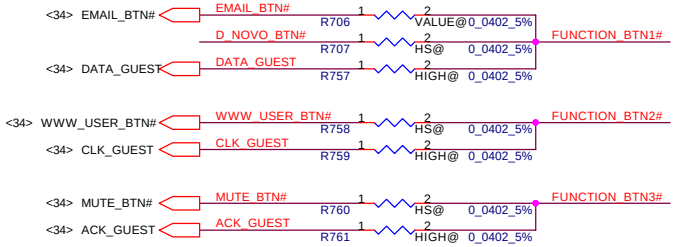


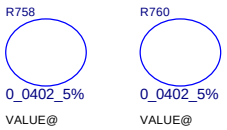


Switch Board Conn.

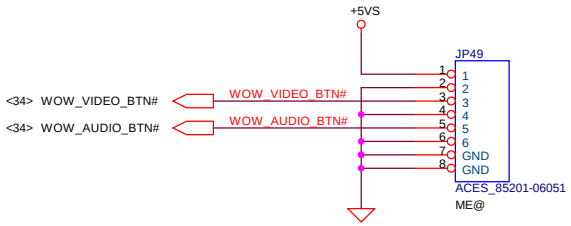








Video Switch Board Conn.



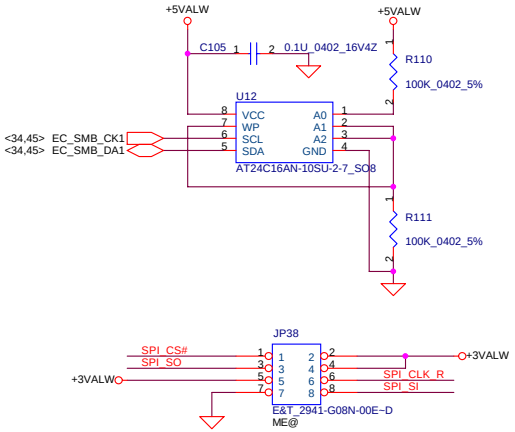
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

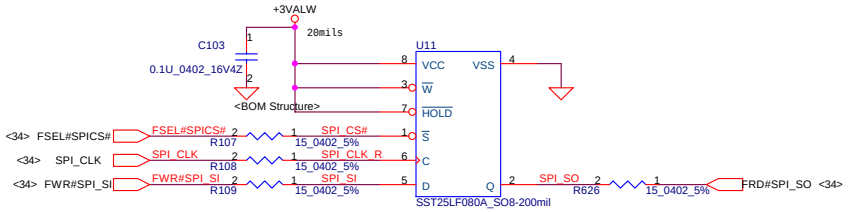
Title: EC ENE KB910L(Reserved)

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

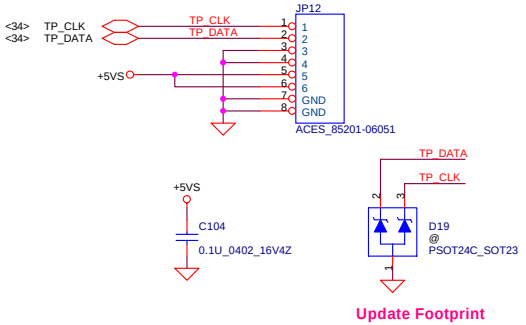
Date: Wednesday, November 01, 2006 Sheet 35 of 52



8M SPI ROM



To TP/B Conn.



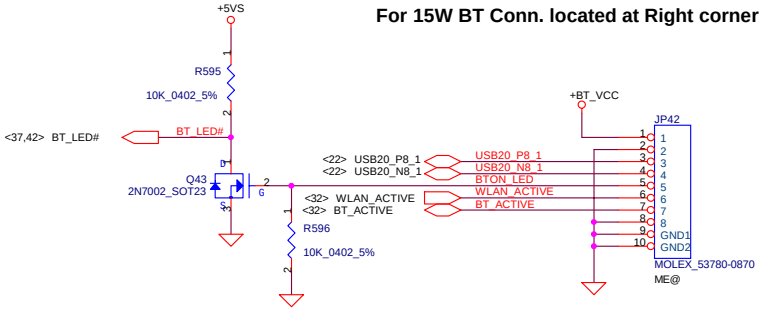
Update Footprint

Bluetooth Conn.

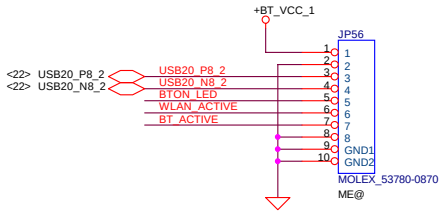
Need to check BT pin definition again!

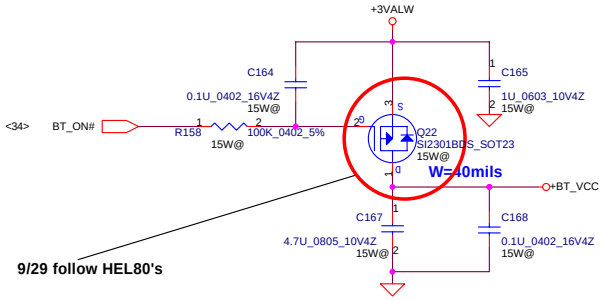
9/20 modified this block

For 15W BT Conn. located at Right corner

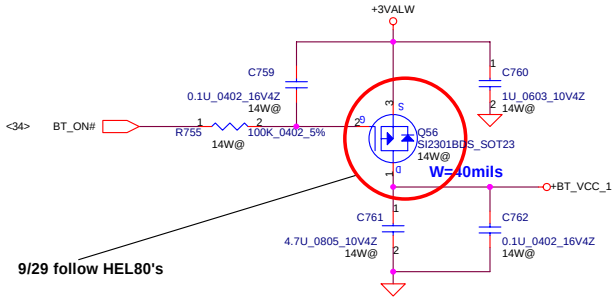


For 14W BT Conn. located at Left corner



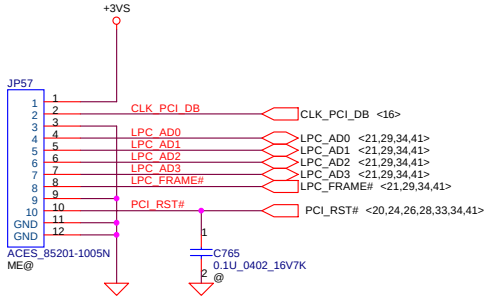


9/29 follow HEL80's

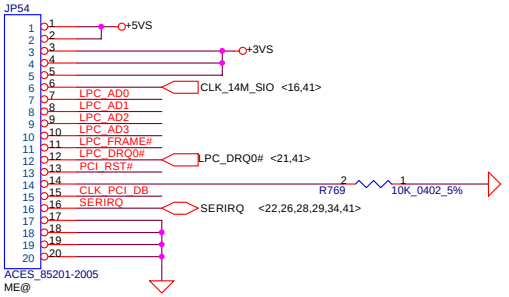


9/29 follow HEL80's

FOR LPC DEBUG PORT



FOR LPC SIO DEBUG PORT



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

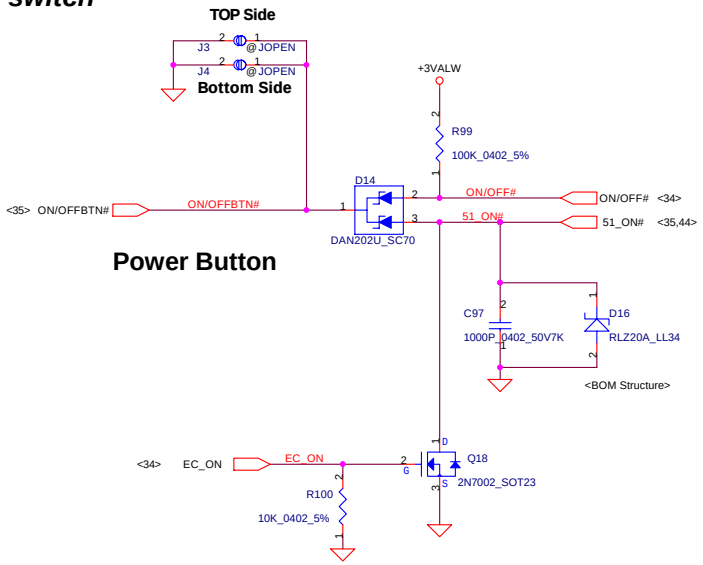
Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

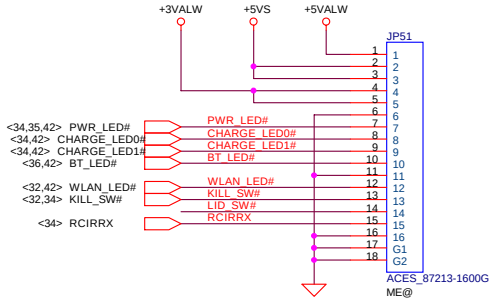
Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

Date: Wednesday, November 01, 2006 | Sheet 36 of 52

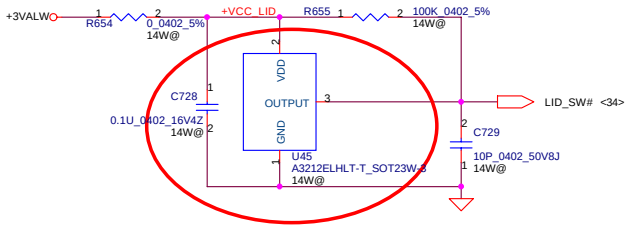
ON/OFF switch



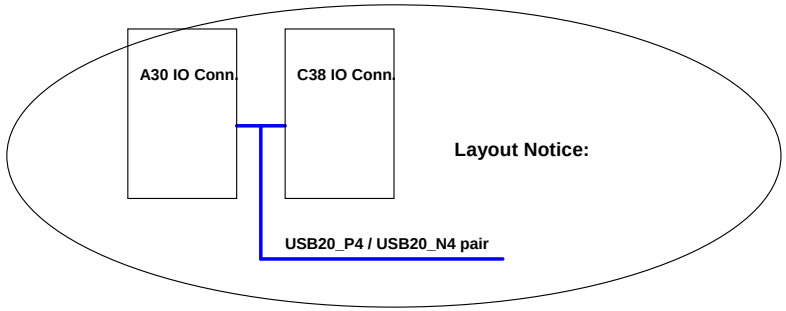
Front LED Board



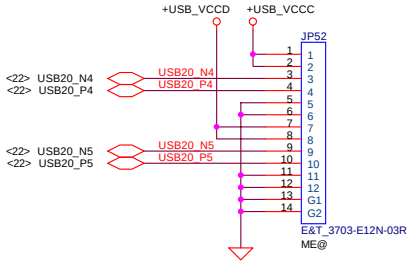
Lid Switch



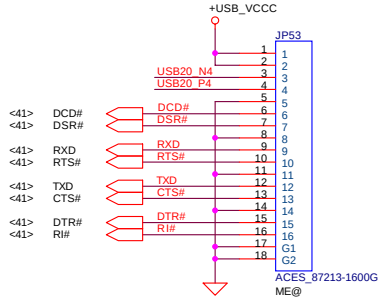
12/9 Change to SA032120010



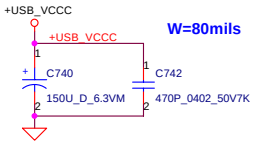
For A30 IO Conn.



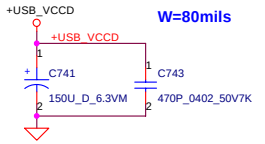
For C38 IO Conn.

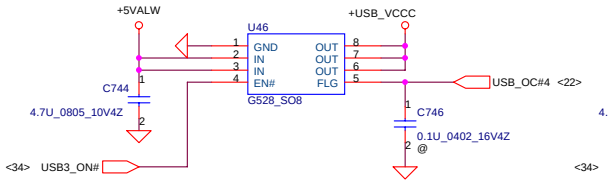


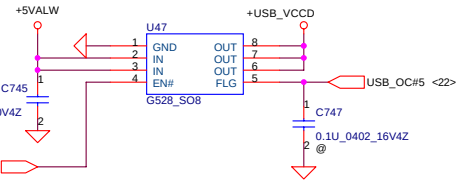
To USB CONN. 3



To USB CONN. 4







Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

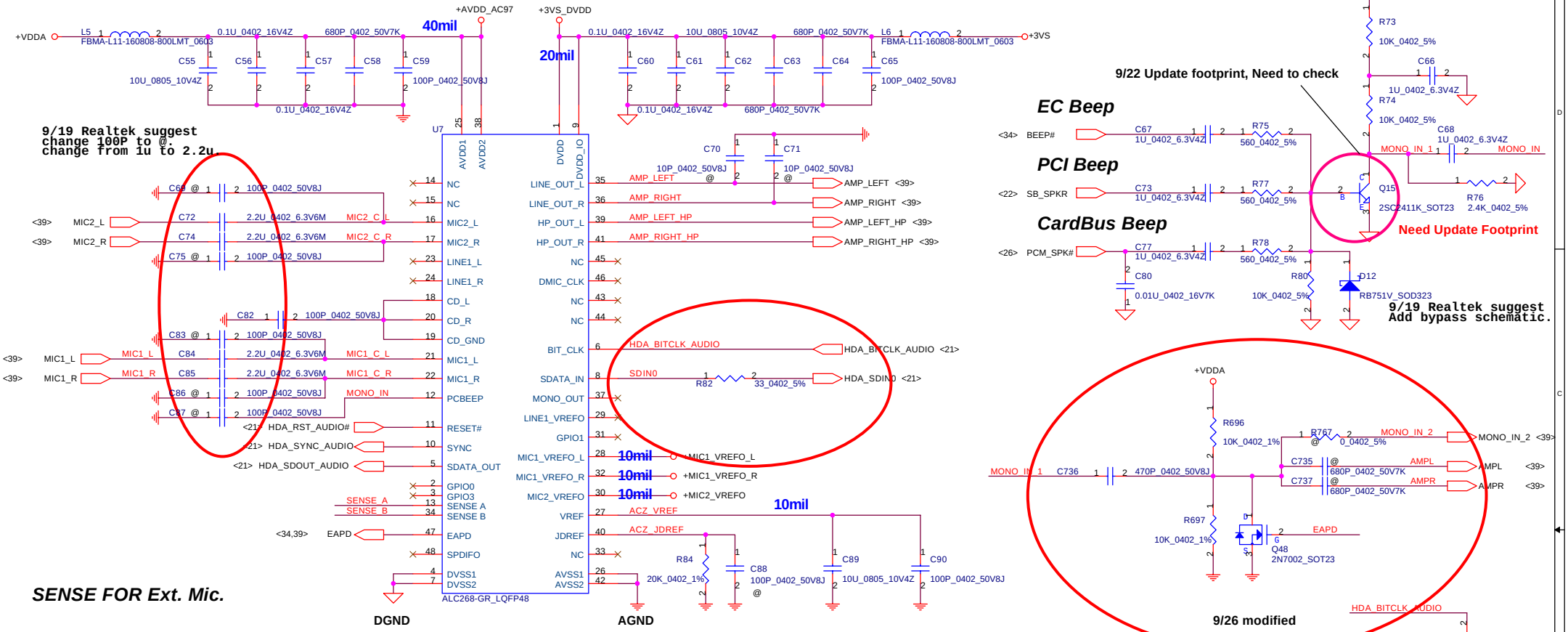
Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

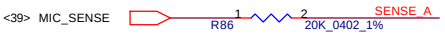
Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

Date: Wednesday, November 01, 2006 | Sheet 37 of 52

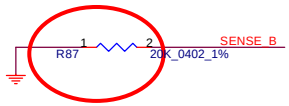
HD Audio Codec



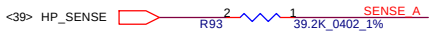
SENSE FOR Ext. Mic.



SENSE FOR Solo Int. Mic.

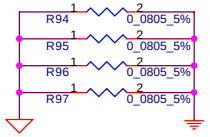


SENSE FOR HP



Sense Pin	Impedance	Codec Signals	Funnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE Out
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Moat Bridge

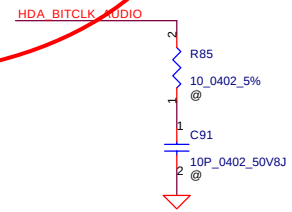


9/22 Update footprint, Need to check

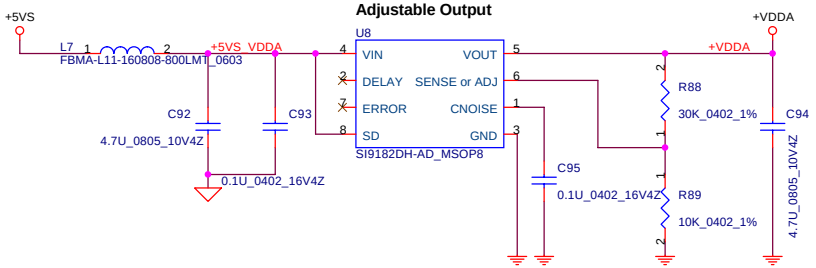
EC Beep

PCI Beep

CardBus Beep



Regulator for CODEC



Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

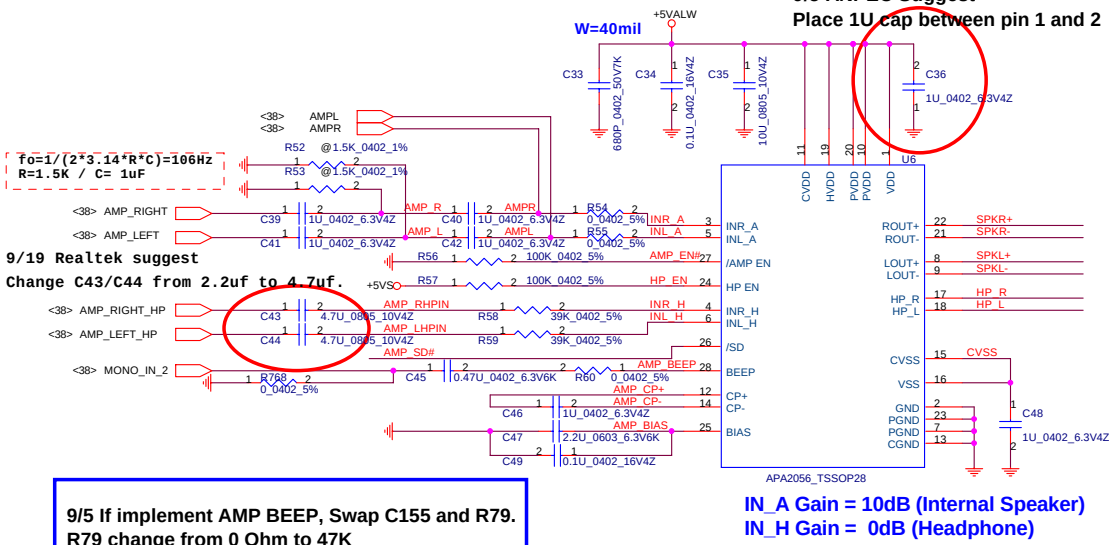
Compal Electronics, Inc.

Title: <Title> HD Audio Codec ALC268

Size: Custom | Document Number: LA-3541P | Rev: 0.1

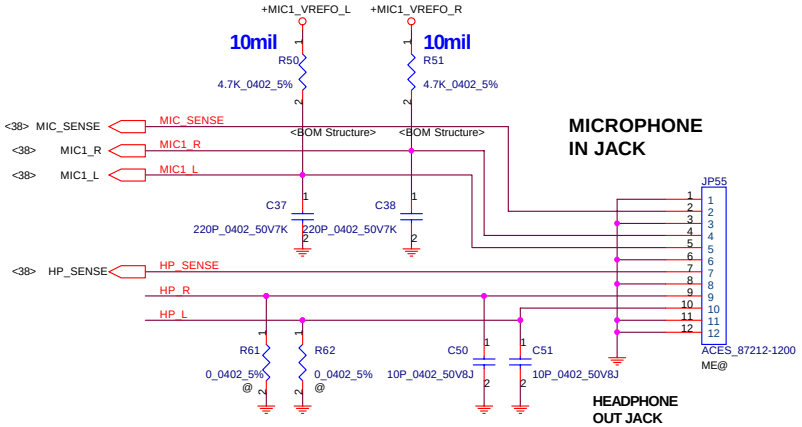
Date: Wednesday, November 01, 2006 | Sheet 38 of 52

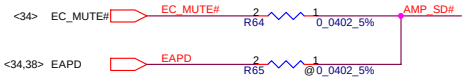
APA2056 SPK/HP Amplifier



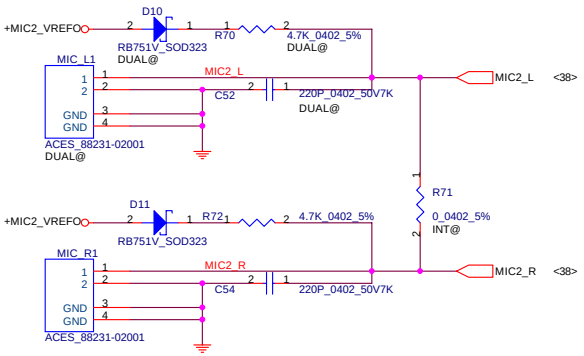
9/5 If implement AMP BEEP, Swap C155 and R79.
R79 change from 0 Ohm to 47K

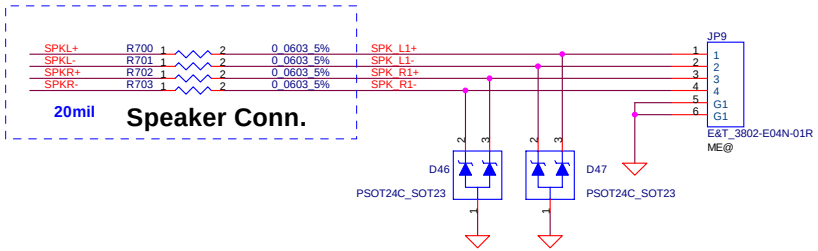
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)





SINGLE INT MIC/DUAL INT MIC





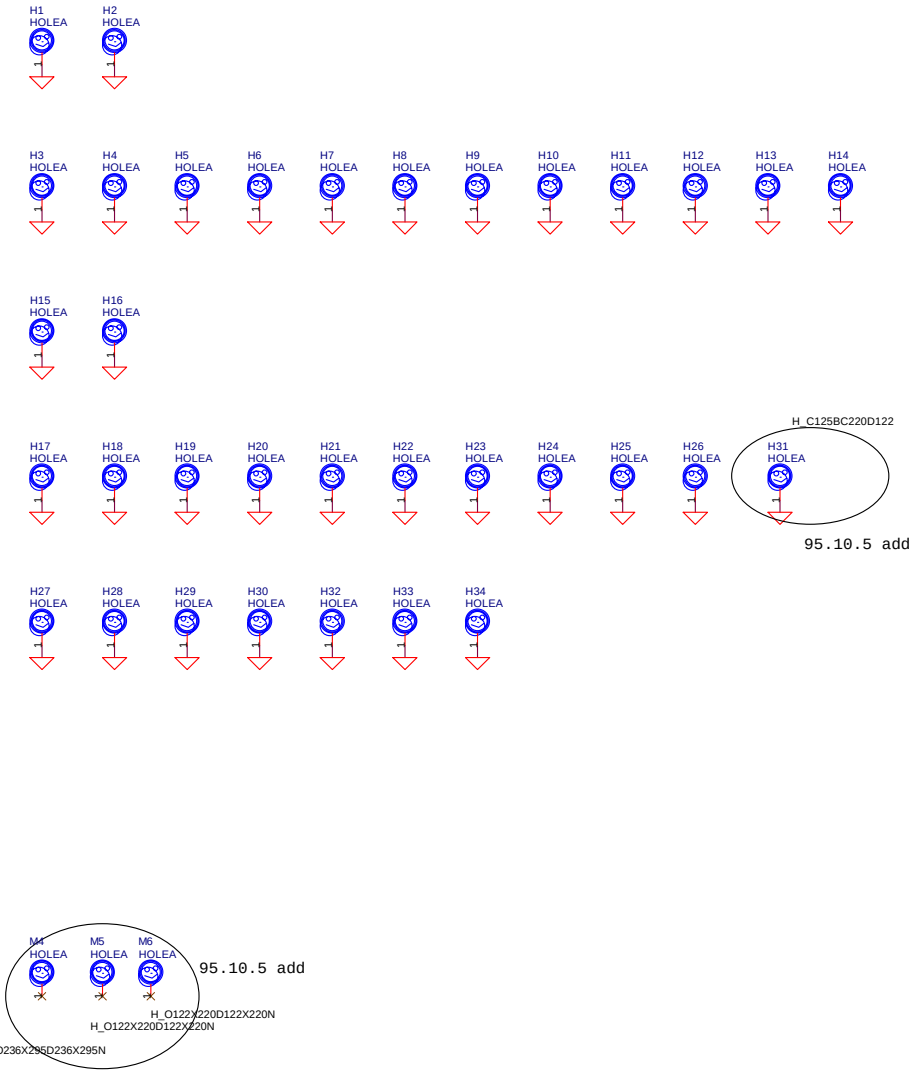
Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

Compal Electronics, Inc.

Title: AMP/VR/Audio Jack/MIC

Size	Document Number	Rev
Custom	LA-3541P	0.1

Date: Wednesday, November 01, 2006 | Sheet 39 of 52



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

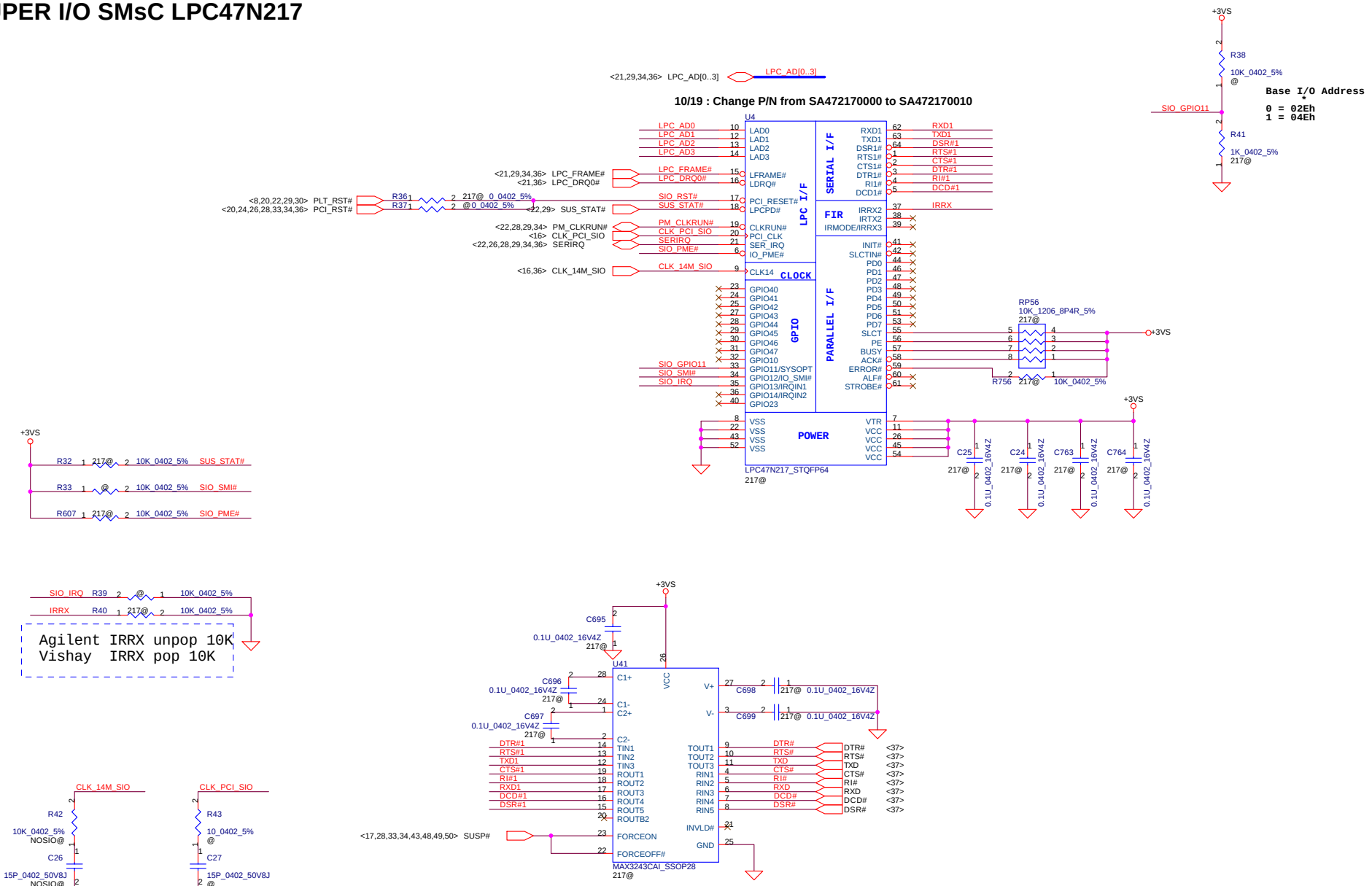
Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

Date: Wednesday, November 01, 2006 | Sheet 40 of 52

SUPER I/O SMsC LPC47N217

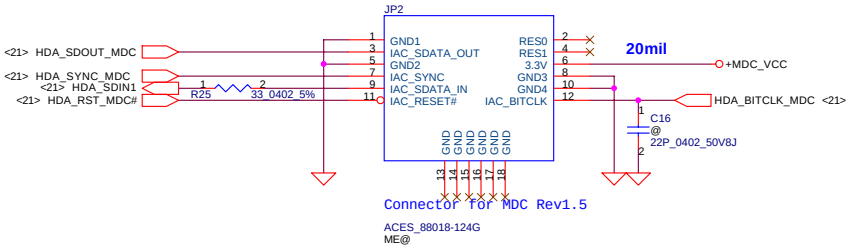


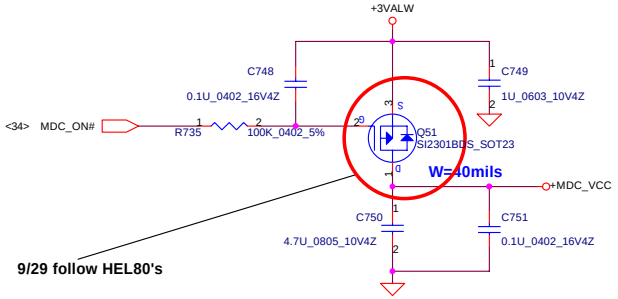
9/18 modify this page following IGT1x

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

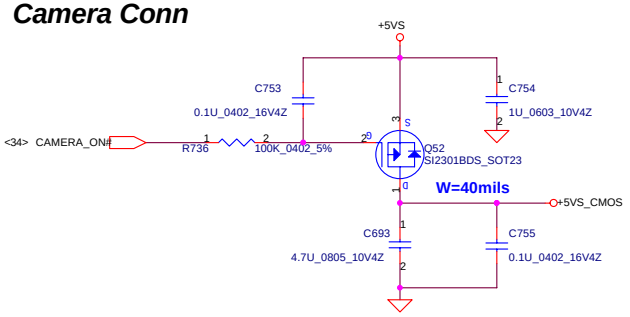
Compal Electronics, Inc.		
Title: SUPER I/O LPC47N217		
Size	Document Number: LA-3541P UMA	Rev: 0.2
Date: Wednesday, November 01, 2006	Sheet 41 of 52	

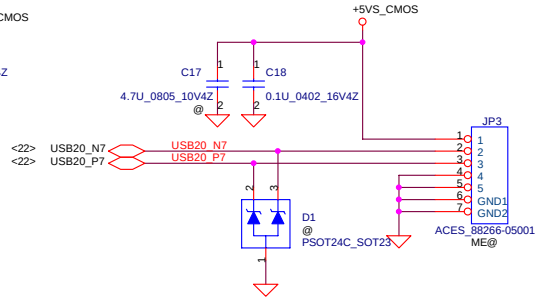
MDC Conn.



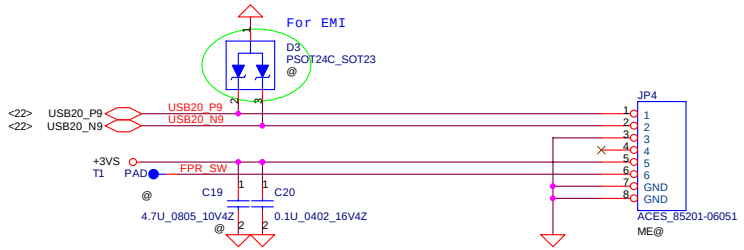


Camera Conn



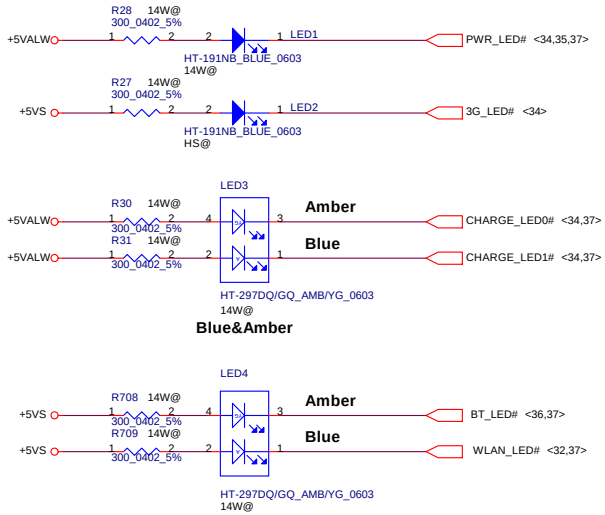


Finger Print board



Need to check pin definition

LED



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Title: MDC/CIR & LED

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B	IFTXX M/B LA-3541P Schematic	0

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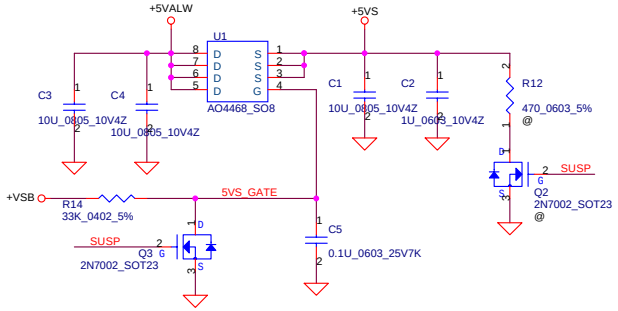
+5VALW TO +5VS



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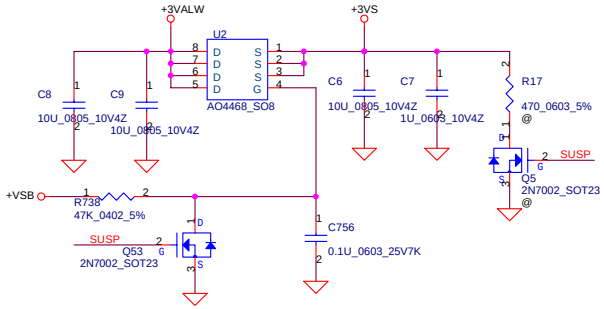
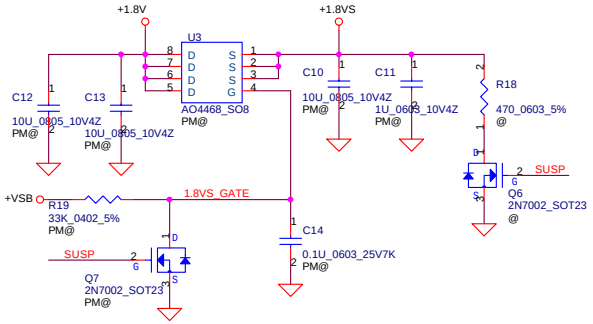
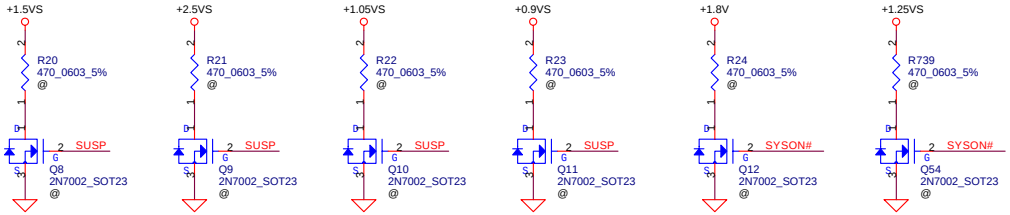
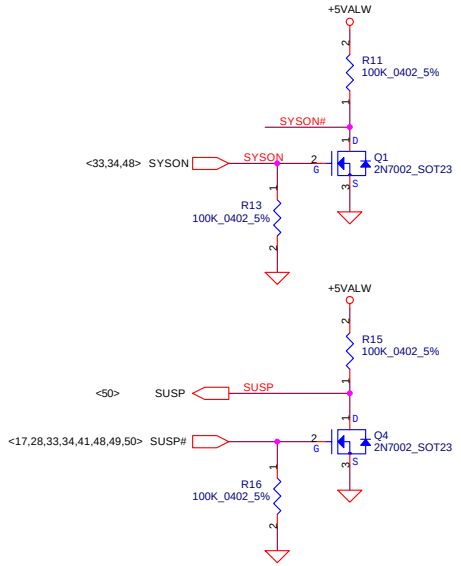


+1.8V to +1.8VS







Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	IFTXX M/B LA-3541P Schematic	0

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