

A-NOTE 2.0 Block Diagram

PCB Layer Stackup	
L1: Signal 1	
L2: VCC	
L3: Inner Signal 2	
L4: Inner Signal 3	
L5: GND	
L6: Signal 4	

Battery Charger	
ISL6255 44	
INPUT	OUTPUT
DCBATOUT	VGA_CORE_S0
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC	
TPS 51120 41	
INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC	
APL5332KAC 18	
INPUT	OUTPUT
3D3V_S5	ID2V_S5

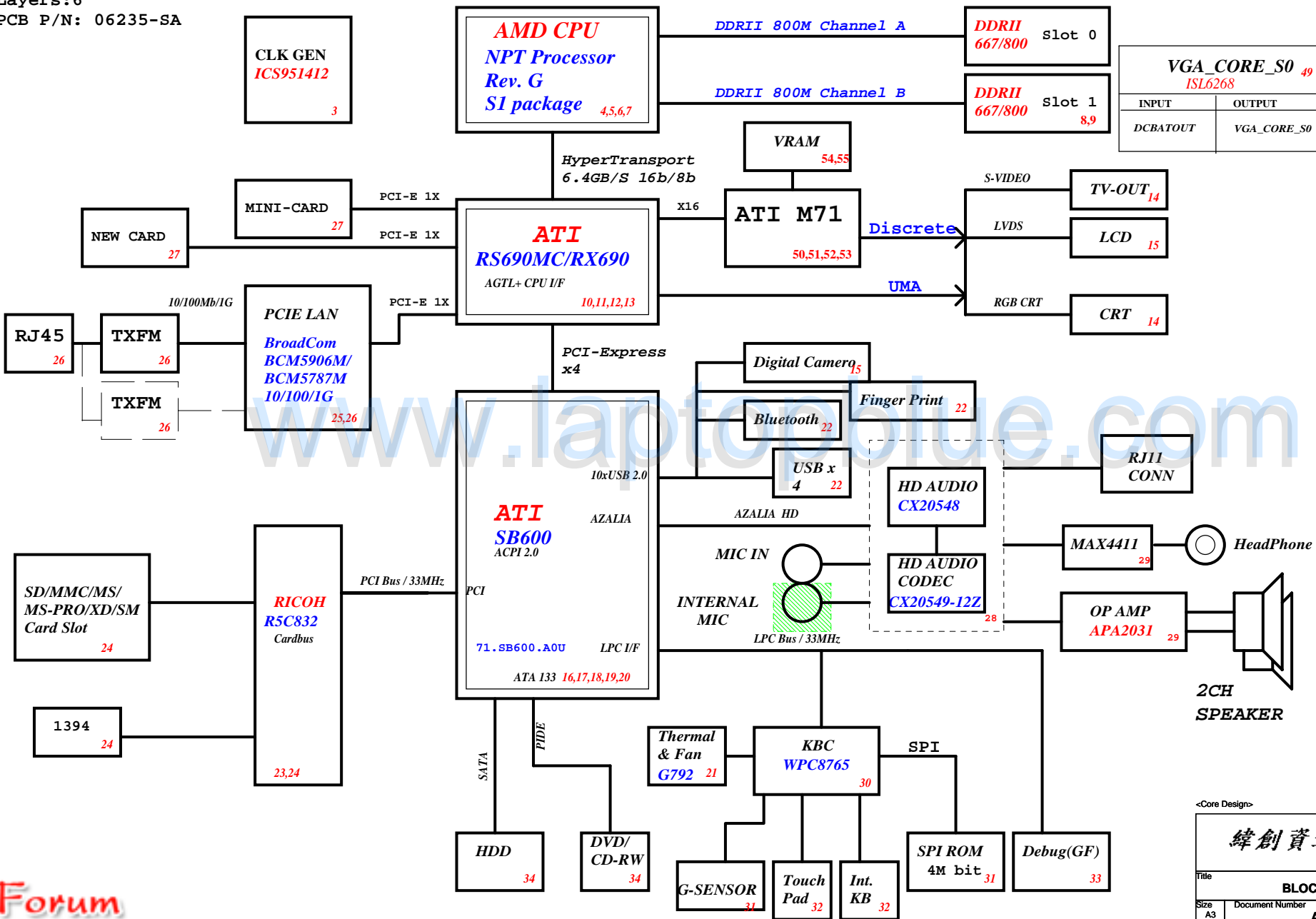
SYSTEM POWER	
TPS51116 42	
INPUT	OUTPUT
DCBATOUT	1D8V_S3 0D9V_S3

ID2V_S0	
ISL6268 43	
INPUT	OUTPUT
DCBATOUT	ID2V_S0

CPU V_CORE	
ISL6264 38,39	
INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER	
TPS 51120 41	
INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Project Code:91.4T001.001
 Layers:6
 PCB P/N: 06235-SA



<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **A-NOTE2.0-AMD** Rev: SA

Date: Tuesday, September 26, 2006 Sheet: 1 of 56

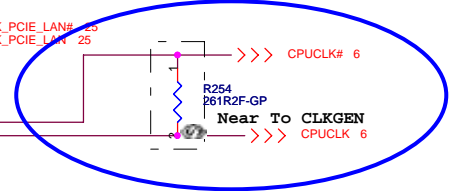
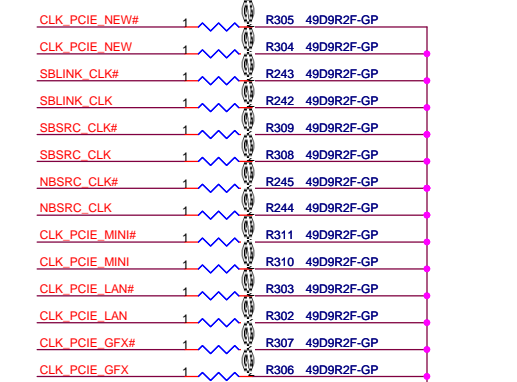
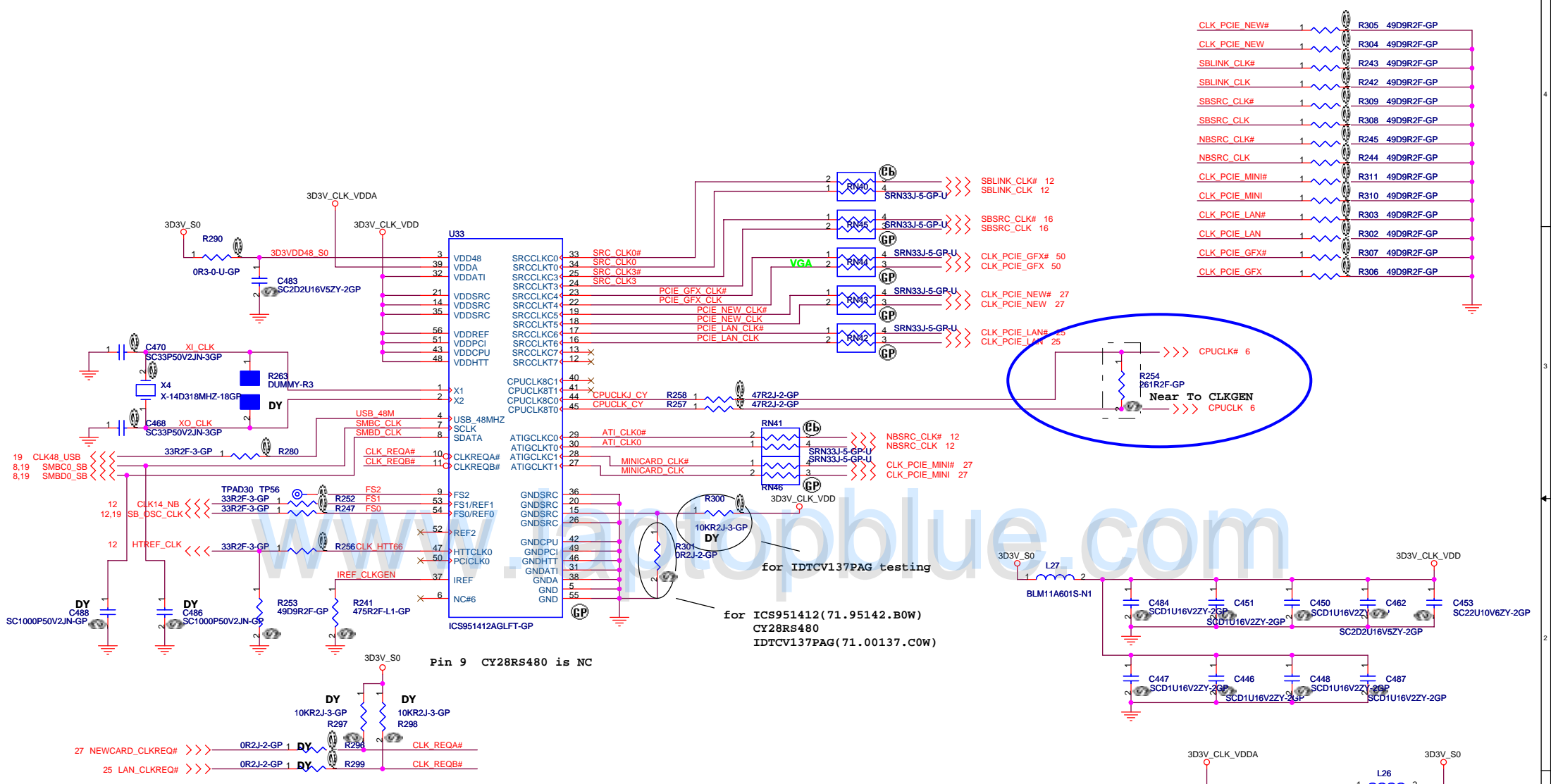
SA: 07/31/06 Start

www.laptopblue.com

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CHANGE HISTORY		
Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA
Date: Tuesday, September 26, 2006		Sheet 2 of 55

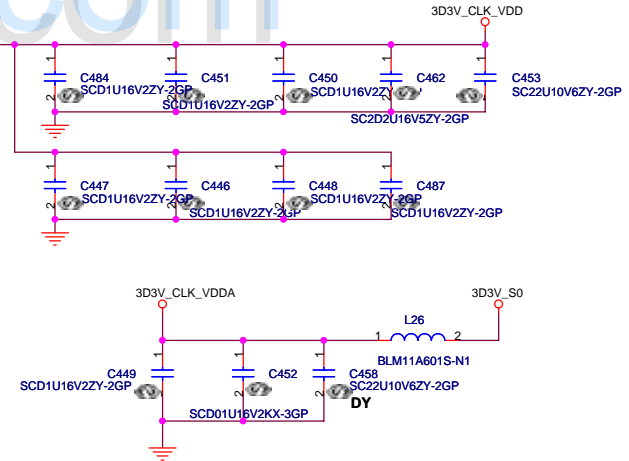


for IDTCV137PAG testing
 for ICS951412 (71.95142.B0W)
 CY28RS480
 IDTCV137PAG (71.00137.C0W)

Pin 9 CY28RS480 is NC

for ICS951412

FS2	FS1	FS0	CPU MHz	HTT MHz	PCI MHz
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	73.12	36.56
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33



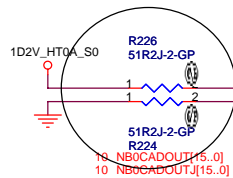
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Title: **CLKGEN_ICS951412**

Size: A3 | Document Number: **A-NOTE2.0-AMD** | Rev: SA

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10 NB0HTTCLKOUT1
10 NB0HTTCLKOUTJ1
10 NB0HTTCLKOUT0
10 NB0HTTCLKOUTJ0

10 NB0HTTCTLOUT
10 NB0HTTCTLOUTJ

10 NB0CADOUT[15..0]
10 NB0CADOUTJ[15..0]

NB0HTTCLKOUT1 J5
NB0HTTCLKOUTJ1 K5
NB0HTTCLKOUT0 J3
NB0HTTCLKOUTJ0 J2

CPUHTTCTLIN1 P3
CPUHTTCTLINJ1 P4
NB0HTTCTLOUT N1
NB0HTTCTLOUTJ P1

NB0CADOUT15 N5
NB0CADOUTJ15 P5
NB0CADOUT14 M3
NB0CADOUTJ14 M4
NB0CADOUT13 L5
NB0CADOUTJ13 M5
NB0CADOUT12 K3
NB0CADOUTJ12 K4
NB0CADOUT11 H3
NB0CADOUTJ11 H4
NB0CADOUT10 G5
NB0CADOUTJ10 H5
NB0CADOUT9 F3
NB0CADOUTJ9 F4
NB0CADOUT8 E5
NB0CADOUTJ8 F5

NB0CADOUT7 N3
NB0CADOUTJ7 N2
NB0CADOUT6 L1
NB0CADOUTJ6 M1
NB0CADOUT5 I3
NB0CADOUTJ5 L2
NB0CADOUT4 J1
NB0CADOUTJ4 K1
NB0CADOUT3 G1
NB0CADOUTJ3 H1
NB0CADOUT2 G3
NB0CADOUTJ2 G2
NB0CADOUT1 E1
NB0CADOUTJ1 F1
NB0CADOUT0 E3
NB0CADOUTJ0 E2

L0_CLKIN_H1
L0_CLKIN_L1
L0_CLKIN_H0
L0_CLKIN_L0

L0_CTLIN_H1
L0_CTLIN_L1
L0_CTLIN_H0
L0_CTLIN_L0

L0_CADIN_H15
L0_CADIN_L15
L0_CADIN_H14
L0_CADIN_L14
L0_CADIN_H13
L0_CADIN_L13
L0_CADIN_H12
L0_CADIN_L12
L0_CADIN_H11
L0_CADIN_L11
L0_CADIN_H10
L0_CADIN_L10
L0_CADIN_H9
L0_CADIN_L9
L0_CADIN_H8
L0_CADIN_L8

L0_CADIN_H7
L0_CADIN_L7
L0_CADIN_H6
L0_CADIN_L6
L0_CADIN_H5
L0_CADIN_L5
L0_CADIN_H4
L0_CADIN_L4
L0_CADIN_H3
L0_CADIN_L3
L0_CADIN_H2
L0_CADIN_L2
L0_CADIN_H1
L0_CADIN_L1
L0_CADIN_H0
L0_CADIN_L0

HYPERTRANSPORT

62.10055.111

L0_CLKOUT_H1
L0_CLKOUT_L1
L0_CLKOUT_H0
L0_CLKOUT_L0

L0_CTLOUT_H1
L0_CTLOUT_L1
L0_CTLOUT_H0
L0_CTLOUT_L0

L0_CADOUT_H15
L0_CADOUT_L15
L0_CADOUT_H14
L0_CADOUT_L14
L0_CADOUT_H13
L0_CADOUT_L13
L0_CADOUT_H12
L0_CADOUT_L12
L0_CADOUT_H11
L0_CADOUT_L11
L0_CADOUT_H10
L0_CADOUT_L10
L0_CADOUT_H9
L0_CADOUT_L9
L0_CADOUT_H8
L0_CADOUT_L8

L0_CADOUT_H7
L0_CADOUT_L7
L0_CADOUT_H6
L0_CADOUT_L6
L0_CADOUT_H5
L0_CADOUT_L5
L0_CADOUT_H4
L0_CADOUT_L4
L0_CADOUT_H3
L0_CADOUT_L3
L0_CADOUT_H2
L0_CADOUT_L2
L0_CADOUT_H1
L0_CADOUT_L1
L0_CADOUT_H0
L0_CADOUT_L0

U66A

Y4 CPUHTTCLKOUT1
Y3 CPUHTTCLKOUTJ1
Y1 CPUHTTCLKOUT0
W1 CPUHTTCLKOUTJ0

T5
R5
R2 CPUHTTCTLOUT0
R3 CPUHTTCTLOUTJ0

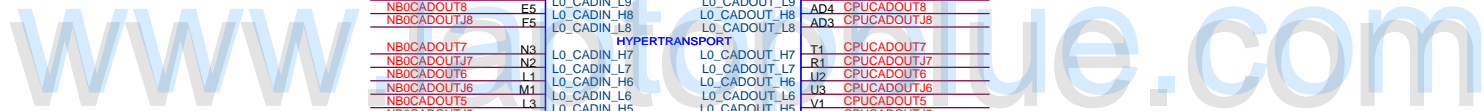
T4 CPUCADOUT15
T3 CPUCADOUTJ15
V5 CPUCADOUT14
U5 CPUCADOUTJ14
V4 CPUCADOUT13
V3 CPUCADOUTJ13
V5 CPUCADOUT12
W5 CPUCADOUTJ12
AB5 CPUCADOUT11
AA5 CPUCADOUTJ11
AB4 CPUCADOUT10
AB3 CPUCADOUTJ10
AD5 CPUCADOUT9
AC5 CPUCADOUTJ9
AD4 CPUCADOUT8
AD3 CPUCADOUTJ8

T1 CPUCADOUT7
R1 CPUCADOUTJ7
U2 CPUCADOUT6
U3 CPUCADOUTJ6
V1 CPUCADOUT5
U1 CPUCADOUTJ5
W2 CPUCADOUT4
W3 CPUCADOUTJ4
AA2 CPUCADOUT3
AA3 CPUCADOUTJ3
AB1 CPUCADOUT2
AA1 CPUCADOUTJ2
AC2 CPUCADOUT1
AC3 CPUCADOUT0
AD1 CPUCADOUTJ1
AC1 CPUCADOUT0

CPUHTTCLKOUT1 10
CPUHTTCLKOUTJ1 10
CPUHTTCLKOUT0 10
CPUHTTCLKOUTJ0 10

CPUHTTCTLOUT0 10
CPUHTTCTLOUTJ0 10

CPUCADOUT[15..0] 10
CPUCADOUTJ[15..0] 10



<Core Design>

緯創資通 Wistron Corporation
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Title: **CPU(1/4)_HyperTransport I/F**

Size A3	Document Number	Rev SA
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8 M_A_DQ[63..0]

U66B

MA0_CLK_H2	Y16	MA0_CLK_DDR2 8
MA0_CLK_L2	AA16	MA0_CLK_DDR2# 8
MA0_CLK_H1	E16	MA0_CLK_DDR1 8
MA0_CLK_L1	F16	MA0_CLK_DDR1# 8
MA0_CS_L3	V19	MA0_CS# 8,9
MA0_CS_L2	J22	MA0_CS2# 8,9
MA0_CS_L1	V22	MA0_CS1# 8,9
MA0_CS_L0	T19	MA0_CS0# 8,9
MA0_ODT1	V20	MA0_ODT1 8,9
MA0_ODT0	LH19	MA0_ODT0 8,9
MA_CAS_L	U20	MA_CAS# 8,9
MA_WE_L	T21	MA_WE# 8,9
MA_RAS_L	T20	MA_RAS# 8,9
MA_BANK2	K22	MA_BANK#2 8,9
MA_BANK1	R20	MA_BANK#1 8,9
MA_BANK0	T22	MA_BANK#0 8,9
MA_CKE1	J20	MA_CKE1 8,9
MA_CKE0	J21	MA_CKE0 8,9
MA_ADD15	K19	M A A15
MA_ADD14	K20	M A A14
MA_ADD13	V24	M A A13
MA_ADD12	K24	M A A12
MA_ADD11	L20	M A A11
MA_ADD10	R19	M A A10
MA_ADD9	L19	M A A9
MA_ADD8	L22	M A A8
MA_ADD7	L21	M A A7
MA_ADD6	M19	M A A6
MA_ADD5	M20	M A A5
MA_ADD4	M24	M A A4
MA_ADD3	M22	M A A3
MA_ADD2	N22	M A A2
MA_ADD1	N21	M A A1
MA_ADD0	R21	M A A0
MA_DQS_H7	W12	M A DQS7
MA_DQS_L7	W13	M A DQS#7
MA_DQS_H6	Y15	M A DQS6
MA_DQS_L6	W15	M A DQS#6
MA_DQS_H5	AB19	M A DQS5
MA_DQS_L5	AB20	M A DQS#5
MA_DQS_H4	AD23	M A DQS4
MA_DQS_L4	AC23	M A DQS#4
MA_DQS_H3	G22	M A DQS3
MA_DQS_L3	G21	M A DQS#3
MA_DQS_H2	C22	M A DQS2
MA_DQS_L2	G16	M A DQS1
MA_DQS_H1	G15	M A DQS#1
MA_DQS_L1	G13	M A DQS0
MA_DQS_H0	H13	M A DQS#0
MA_DQS_L0	H13	M A DQS#0
MA_DM7	Y13	M A DM7
MA_DM6	AB16	M A DM6
MA_DM5	Y19	M A DM5
MA_DM4	AC24	M A DM4
MA_DM3	F24	M A DM3
MA_DM2	F19	M A DM2
MA_DM1	C15	M A DM1
MA_DM0	E12	M A DM0

MEMORY INTERFACE

8 M_B_DQ[63..0]

U66C

M B DQ63	AD11	MB_DATA63
M B DQ62	AF11	MB_DATA62
M B DQ61	AF14	MB_DATA61
M B DQ60	AE14	MB_DATA60
M B DQ59	Y11	MB_DATA59
M B DQ58	AB11	MB_DATA58
M B DQ57	AC12	MB_DATA57
M B DQ56	AE13	MB_DATA56
M B DQ55	AF15	MB_DATA55
M B DQ54	AF16	MB_DATA54
M B DQ53	AC18	MB_DATA53
M B DQ52	AF19	MB_DATA52
M B DQ51	AD14	MB_DATA51
M B DQ50	AC14	MB_DATA50
M B DQ49	AE18	MB_DATA49
M B DQ48	AD18	MB_DATA48
M B DQ47	AD20	MB_DATA47
M B DQ46	AC20	MB_DATA46
M B DQ45	AF23	MB_DATA45
M B DQ44	AE24	MB_DATA44
M B DQ43	AE20	MB_DATA43
M B DQ42	AE20	MB_DATA42
M B DQ41	AD22	MB_DATA41
M B DQ40	AC22	MB_DATA40
M B DQ39	AE25	MB_DATA39
M B DQ38	AD26	MB_DATA38
M B DQ37	AE25	MB_DATA37
M B DQ36	AA26	MB_DATA36
M B DQ35	AE24	MB_DATA35
M B DQ34	AD24	MB_DATA34
M B DQ33	AA23	MB_DATA33
M B DQ32	AA24	MB_DATA32
M B DQ31	G24	MB_DATA31
M B DQ30	G23	MB_DATA30
M B DQ29	D26	MB_DATA29
M B DQ28	C26	MB_DATA28
M B DQ27	G26	MB_DATA27
M B DQ26	G25	MB_DATA26
M B DQ25	E24	MB_DATA25
M B DQ24	E24	MB_DATA24
M B DQ23	C24	MB_DATA23
M B DQ22	B24	MB_DATA22
M B DQ21	C20	MB_DATA21
M B DQ20	B20	MB_DATA20
M B DQ19	C25	MB_DATA19
M B DQ18	D24	MB_DATA18
M B DQ17	A21	MB_DATA17
M B DQ16	D20	MB_DATA16
M B DQ15	D18	MB_DATA15
M B DQ14	C18	MB_DATA14
M B DQ13	D14	MB_DATA13
M B DQ12	C14	MB_DATA12
M B DQ11	A20	MB_DATA11
M B DQ10	A19	MB_DATA10
M B DQ9	A16	MB_DATA9
M B DQ8	A15	MB_DATA8
M B DQ7	A13	MB_DATA7
M B DQ6	D12	MB_DATA6
M B DQ5	E11	MB_DATA5
M B DQ4	G11	MB_DATA4
M B DQ3	B14	MB_DATA3
M B DQ2	A14	MB_DATA2
M B DQ1	A11	MB_DATA1
M B DQ0	C11	MB_DATA0

MEMORY INTERFACE

MB0_CLK_H2	AF18	MB0_CLK_DDR2 8
MB0_CLK_L2	AF17	MB0_CLK_DDR2# 8
MB0_CLK_H1	A17	MB0_CLK_DDR1 8
MB0_CLK_L1	A18	MB0_CLK_DDR1# 8
MB0_CS_L3	Y26	MB0_CS# 8,9
MB0_CS_L2	J24	MB0_CS2# 8,9
MB0_CS_L1	W24	MB0_CS1# 8,9
MB0_CS_L0	U23	MB0_CS0# 8,9
MB0_ODT1	W23	MB0_ODT1 8,9
MB0_ODT0	W26	MB0_ODT0 8,9
MB_CAS_L	V26	MB_CAS# 8,9
MB_WE_L	U22	MB_WE# 8,9
MB_RAS_L	U24	MB_RAS# 8,9
MB_BANK2	K26	MB_BANK#2 8,9
MB_BANK1	T26	MB_BANK#1 8,9
MB_BANK0	U26	MB_BANK#0 8,9
MB_CKE1	H26	MB_CKE1 8,9
MB_CKE0	J23	MB_CKE0 8,9
MB_ADD15	J25	M B A15
MB_ADD14	J26	M B A14
MB_ADD13	W25	M B A13
MB_ADD12	L23	M B A12
MB_ADD11	L25	M B A11
MB_ADD10	U25	M B A10
MB_ADD9	L24	M B A9
MB_ADD8	M26	M B A8
MB_ADD7	L26	M B A7
MB_ADD6	N23	M B A6
MB_ADD5	N24	M B A5
MB_ADD4	N25	M B A4
MB_ADD3	N26	M B A3
MB_ADD2	P24	M B A2
MB_ADD1	P26	M B A1
MB_ADD0	T24	M B A0
MB_DQS_H7	AF12	M B DQS7
MB_DQS_L7	AE12	M B DQS#7
MB_DQS_H6	AE16	M B DQS#6
MB_DQS_L6	AD16	M B DQS#6
MB_DQS_H5	AF21	M B DQS5
MB_DQS_L5	AF22	M B DQS#5
MB_DQS_H4	AC25	M B DQS4
MB_DQS_L4	AC26	M B DQS#4
MB_DQS_H3	F26	M B DQS3
MB_DQS_L3	E26	M B DQS#3
MB_DQS_H2	A24	M B DQS2
MB_DQS_L2	A23	M B DQS#2
MB_DQS_H1	D16	M B DQS1
MB_DQS_L1	C16	M B DQS#1
MB_DQS_H0	C12	M B DQS0
MB_DQS_L0	B12	M B DQS#0
MB_DM7	AD12	M B DM7
MB_DM6	AC16	M B DM6
MB_DM5	AE22	M B DM5
MB_DM4	AB26	M B DM4
MB_DM3	E25	M B DM3
MB_DM2	A22	M B DM2
MB_DM1	B16	M B DM1
MB_DM0	A12	M B DM0

M_A_A[15..0] 8,9

M_B_A[15..0] 8,9

M_A_DQS[7..0] 8

M_B_DQS[7..0] 8

M_A_DQS#7[7..0] 8

M_B_DQS#7[7..0] 8

M_A_DM[7..0] 8

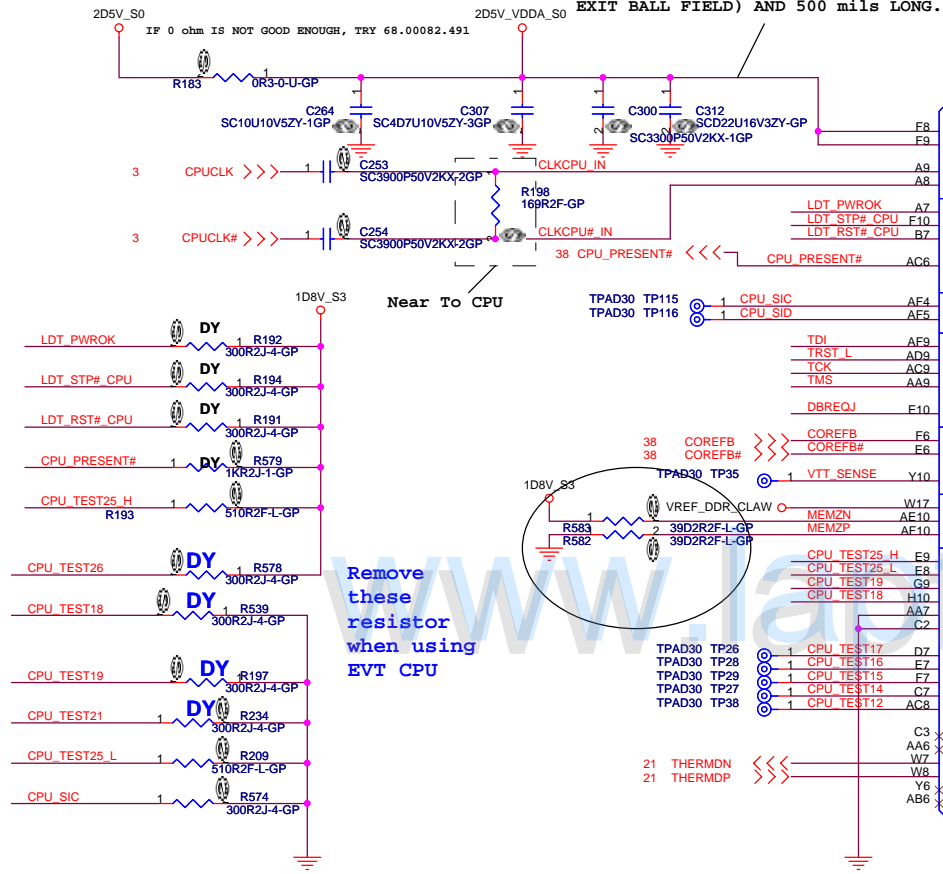
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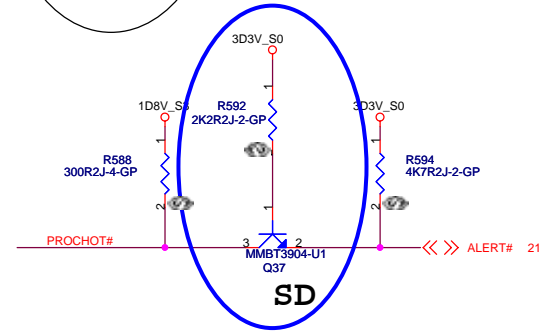
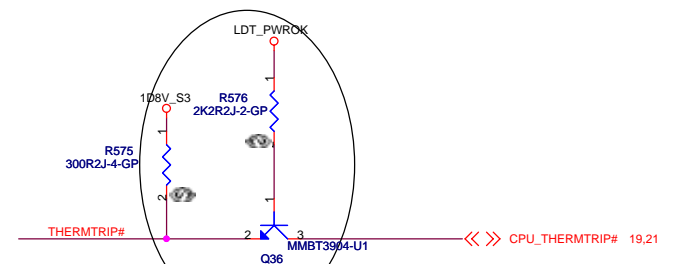
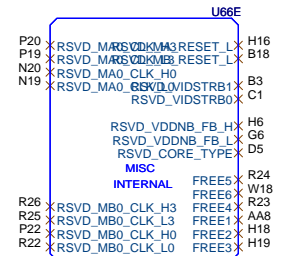
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU(2/4)_DDR	
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LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

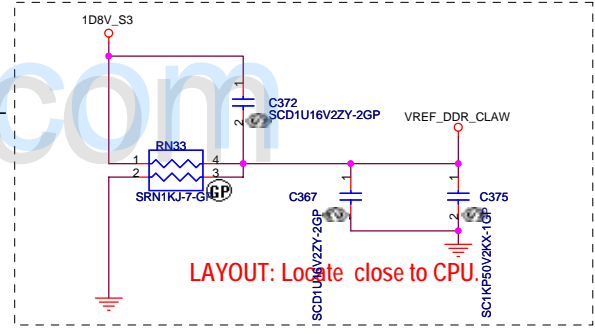


Remove these resistor when using EVT CPU

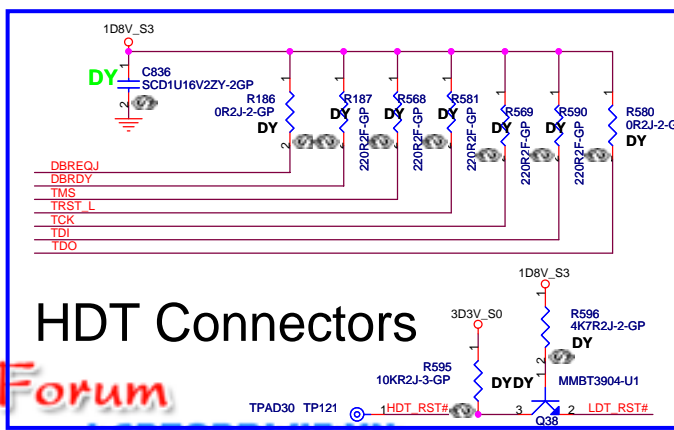


VREF_DDR_CLAW

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

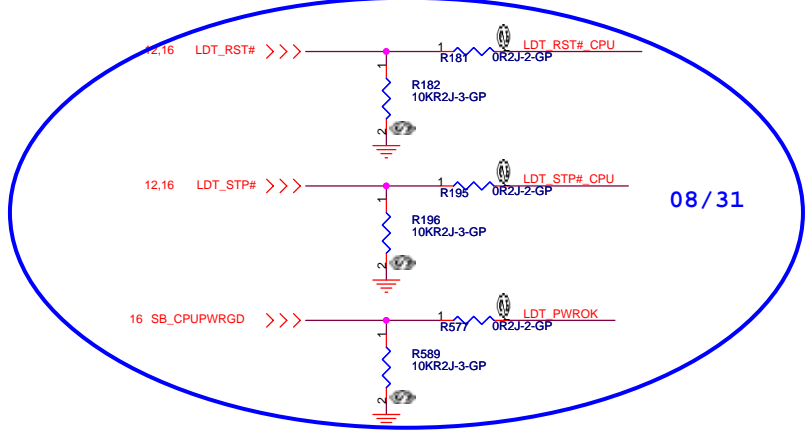


LAYOUT: Route close to CPU.



HDT Connectors

Forum



08/31

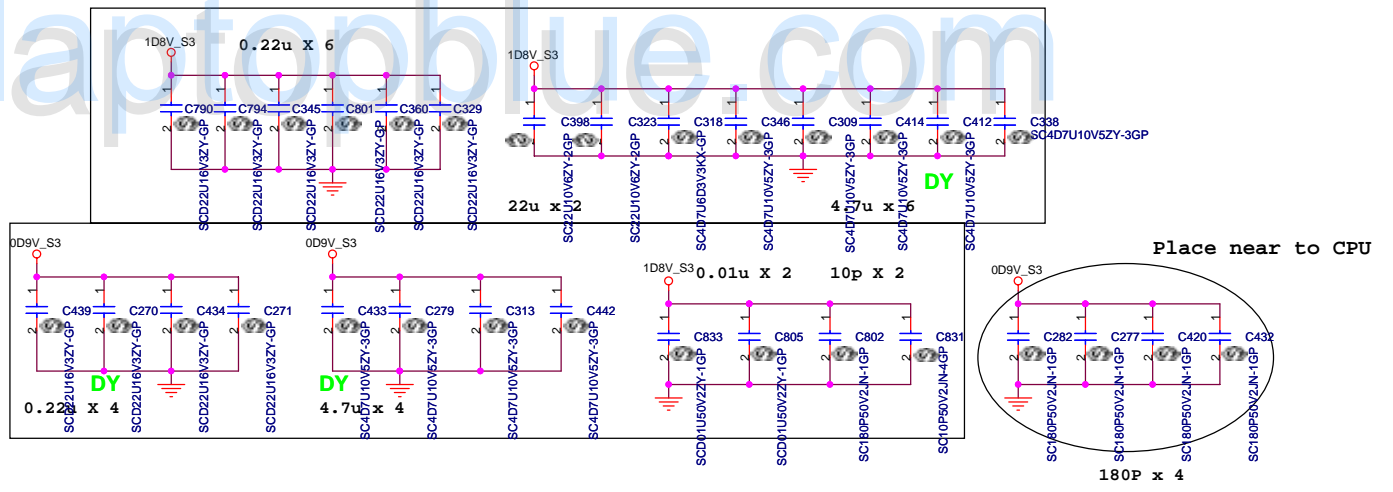
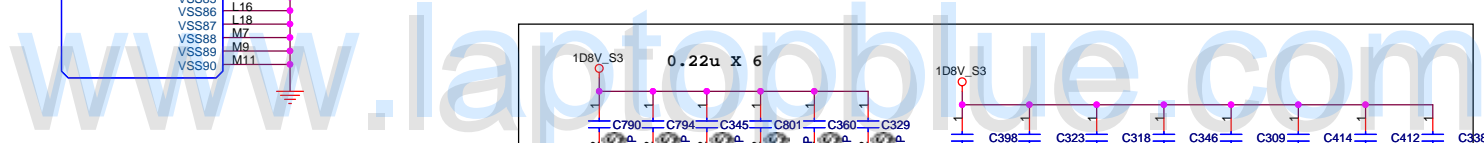
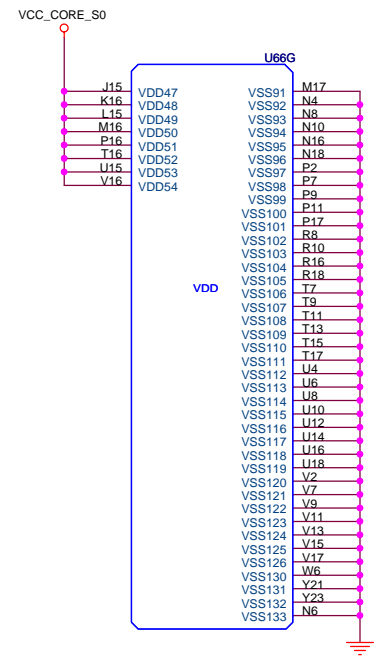
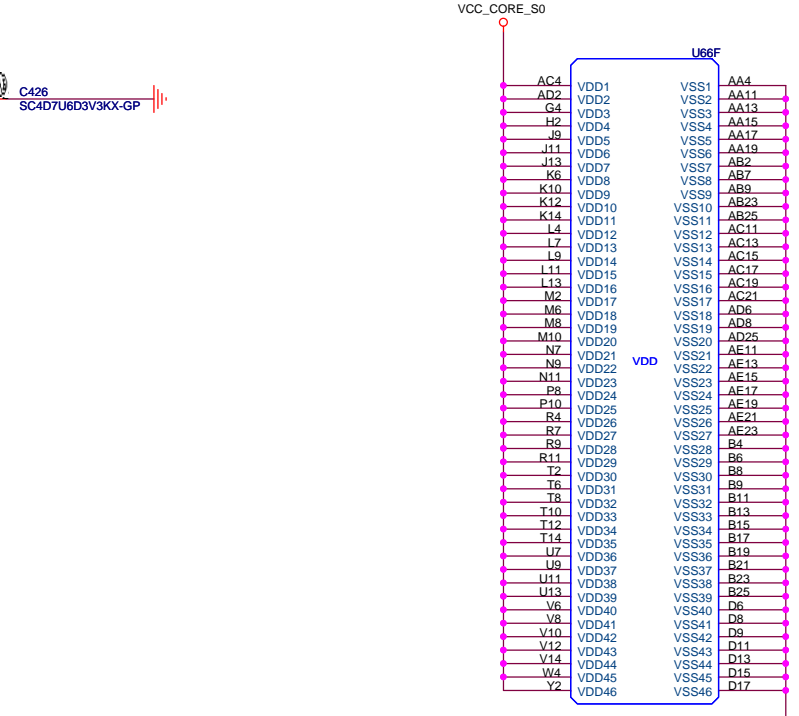
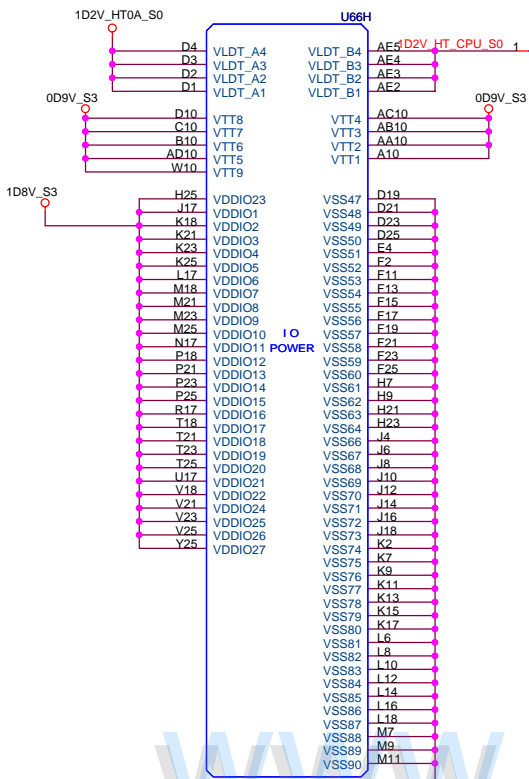
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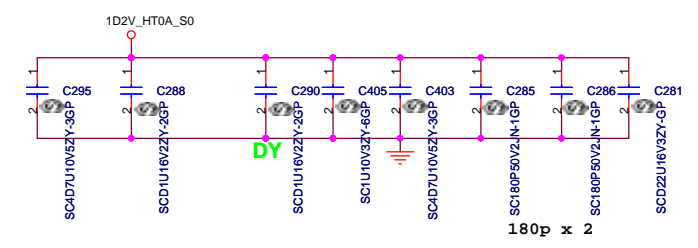
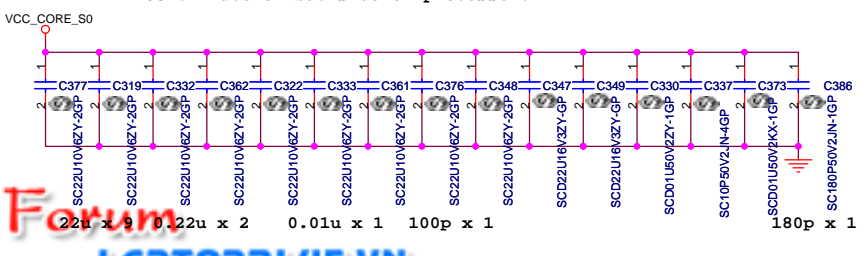
Title: **CPU(3/4) Control & Debug**

Size: A3 Document Number: **A-NOTE2.0-AMD** Rev: SA

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LAYOUT: Place on backside of processor.



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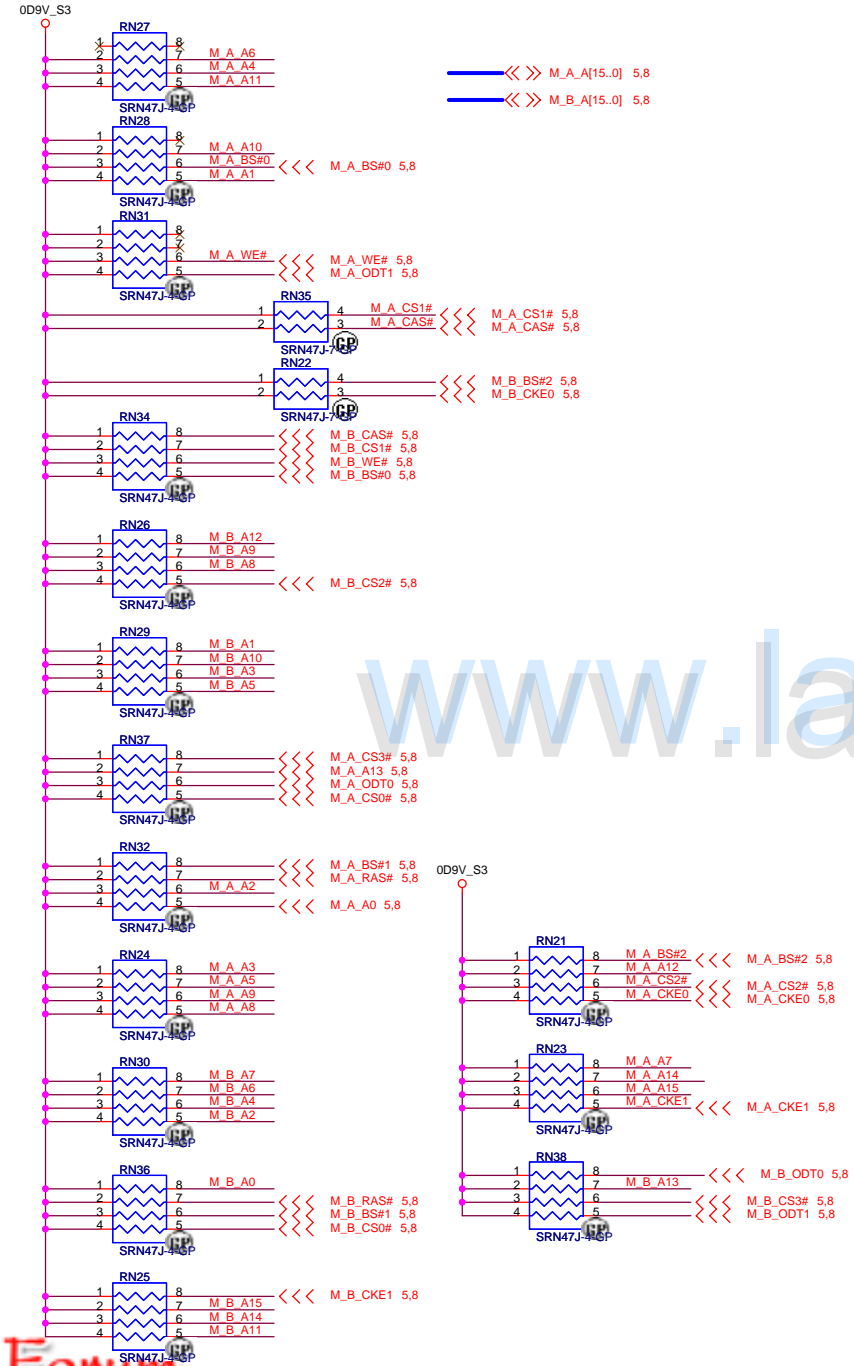
Title: **CPU(4/4) Power**

Size A3 Document Number: **A-NOTE2.0-AMD** Rev SA

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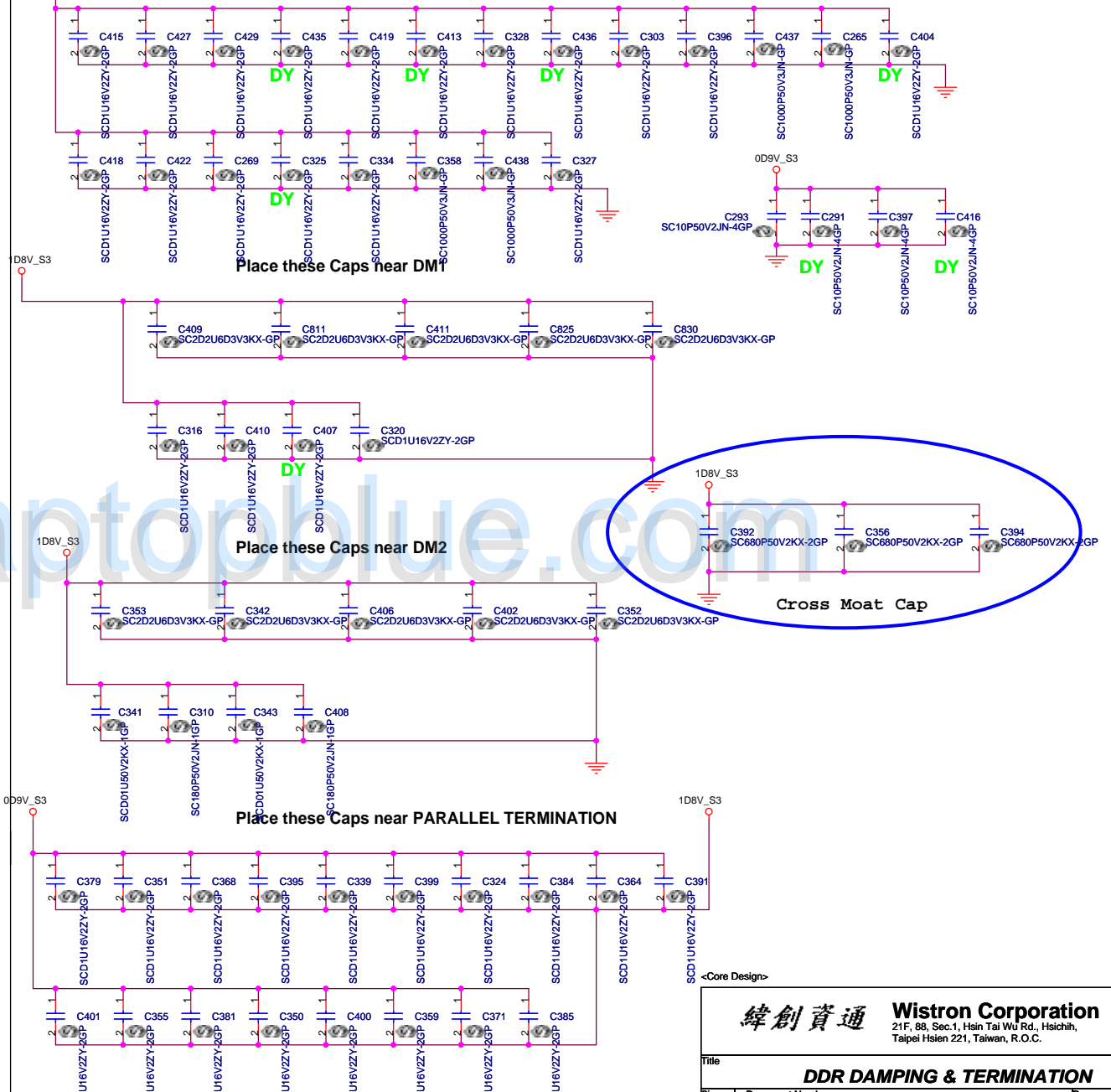
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

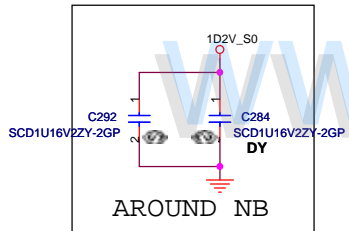
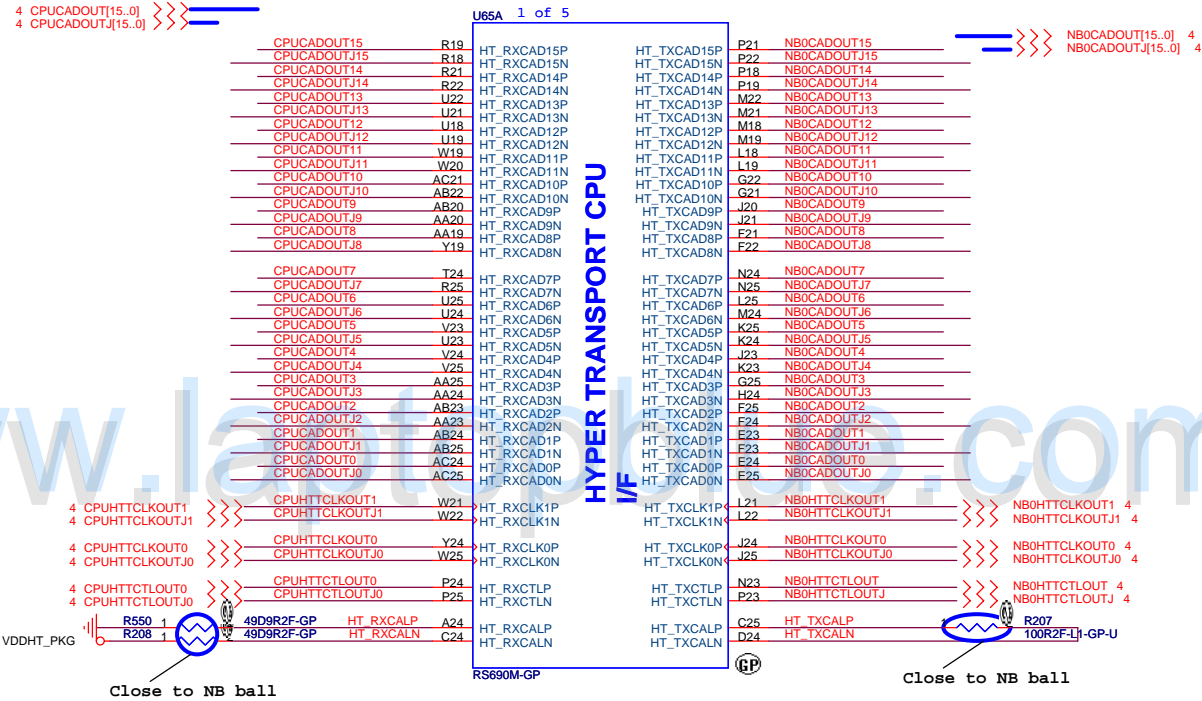
Title: **DDR DAMPING & TERMINATION**

Size A3 Document Number: **A-NOTE2.0-AMD** Rev SA

Date: Tuesday, September 26, 2006 Sheet 9 of 55

CLAW HAMMER TO NB

NB TO CLAW HAMMER



<Core Design>

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Title NB-RS690M HT

Size A3 Document Number A-NOTE2.0-AMD Rev SA

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50 PCIE_GFX_RXN[15..0] >>>

50 PCIE_GFX_RXP[15..0] >>>

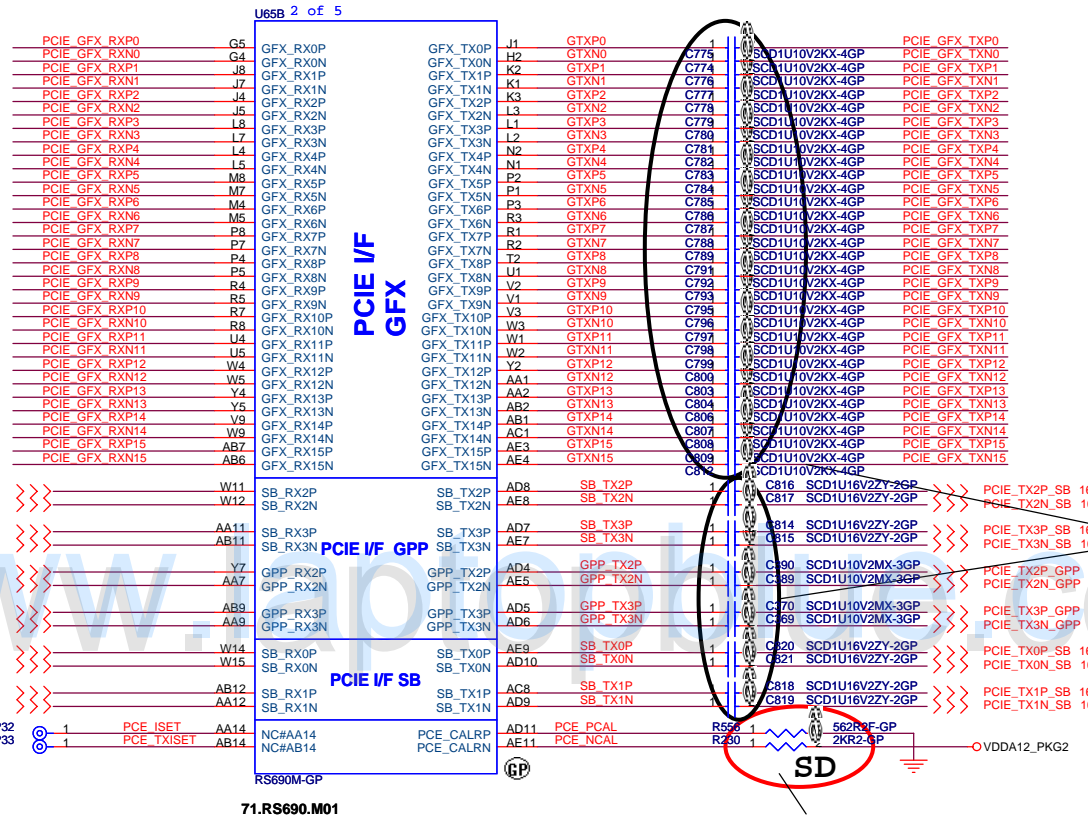
>>> PCIE_GFX_TXN[15..0] 50

>>> PCIE_GFX_TXP[15..0] 50

NEW-CARD

LAN

A-LINK



CLOSE TO NB

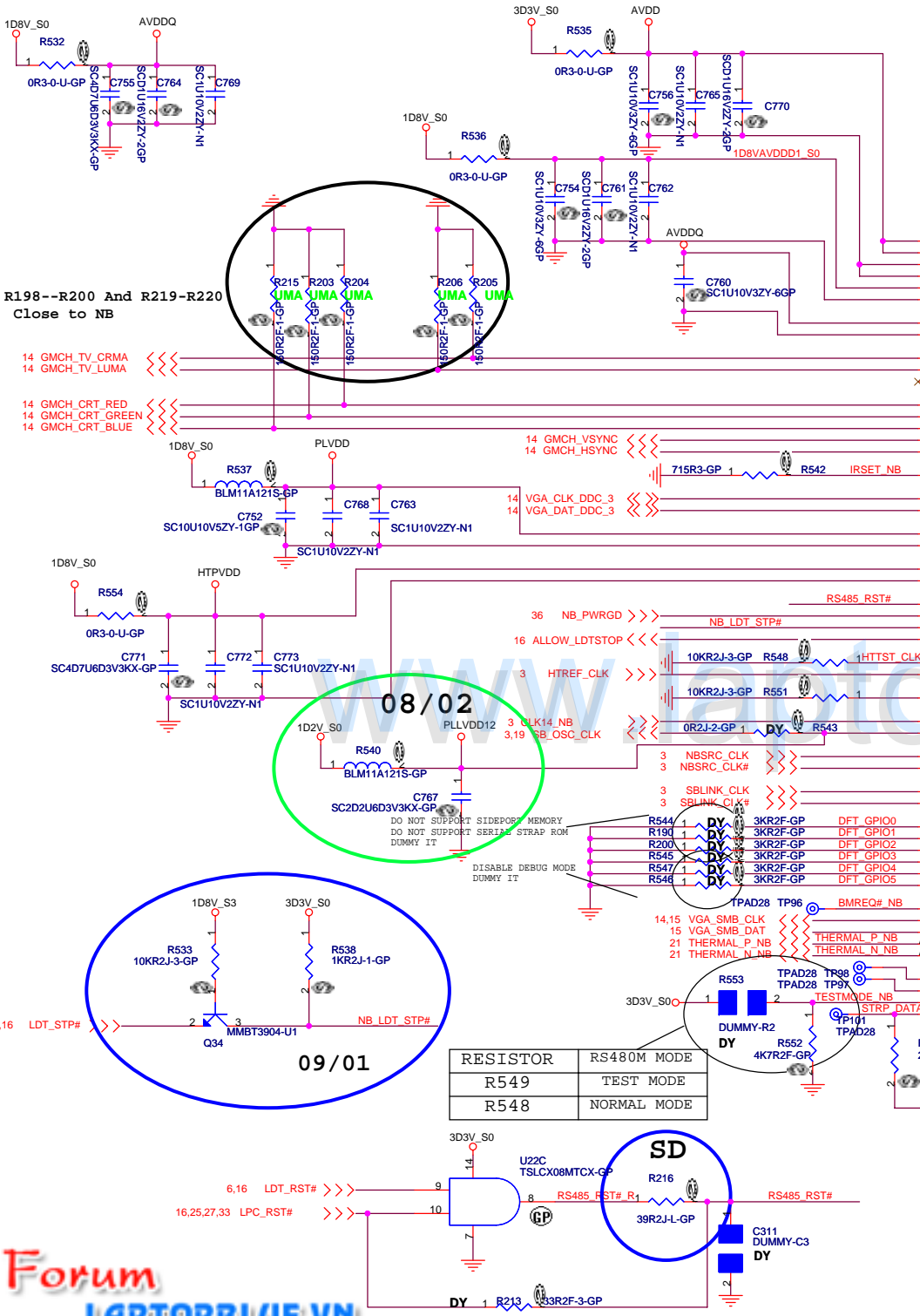
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NB-RS690M_MEM/PCIE_LINK I/F**

Size: A3 Document Number: **A-NOTE2.0-AMD** Rev: SA

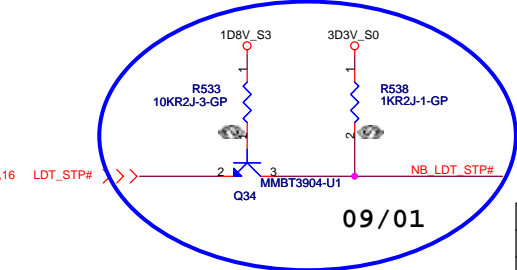
Date: Tuesday, September 26, 2006 Sheet: 11 of 55



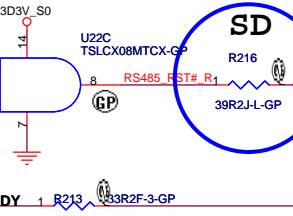
R198--R200 And R219-R220
Close to NB

- 14 GMCH_TV_CRMA
- 14 GMCH_TV_LUMA
- 14 GMCH_CRT_RED
- 14 GMCH_CRT_GREEN
- 14 GMCH_CRT_BLUE

- 36 NB_PWRGD >>>
- 16 ALLOW_LDTSTOP <<<
- 3 HTPREF_CLK >>>
- 3 BLK14_NB
- 3,19 NB_OSC_CLK

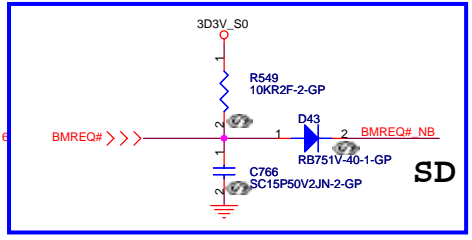


RESISTOR	RS480M MODE
R549	TEST MODE
R548	NORMAL MODE



- U65C 3 of 5
- B22 AVDD
 - C22 AVDD
 - G17 AVSSN
 - H17 AVSSN
 - A20 AVDDDI
 - B20 AVSSDI
 - A21 AVDDQ
 - A22 AVSSQ
 - C21 C
 - C20 Y
 - D19 COMP
 - F19 RED
 - F19 GREEN
 - F19 BLUE
 - C6 DACVSYNC
 - A5 DACHSYNC
 - B21 RSET
 - B6 DACSCL
 - A6 DACSDA
 - A10 PLLVDD18
 - B10 PLLVSS
 - B24 HTPVDD
 - B25 HTPVSS
 - C10 SYSRESET#
 - C11 POWERGOOD
 - C5 LDTSTOP#
 - B5 ALLOW_LDTSTOP
 - C23 HHTSTCLK
 - B23 HTPREFCLK
 - C2 TVCLKIN
 - B11 OSCIN
 - A11 PLLVDD12
 - F2 GFX_CLKP
 - E1 GFX_CLKN
 - G1 SB_CLKP
 - G2 SB_CLKN
 - D6 DFT_GPIO0
 - D7 DFT_GPIO1
 - D8 DFT_GPIO2
 - C7 DFT_GPIO3
 - B8 DFT_GPIO4
 - A8 DFT_GPIO5
 - B20 BMREQ#_NB
 - A2 I2C_CLK
 - A4 I2C_DATA
 - AA15 THERMALDIODE_P
 - AB15 THERMALDIODE_N
 - C14 TMD5_HPD
 - B3 DDC_DATA
 - C3 TESTMODE
 - A3 STRP_DATA
- CRT/TVOUT**
- PLL PWR**
- PM**
- CLOCKS**
- MIS.**

- B14 TXOUT_L0P
 - B15 TXOUT_L0N
 - B13 TXOUT_L1P
 - A13 TXOUT_L1N
 - H14 TXOUT_L2P
 - G14 TXOUT_L2N
 - D17 TXOUT_L3P
 - E17 TXOUT_L3N
 - A15 TXOUT_U0P
 - B16 TXOUT_U0N
 - C17 TXOUT_U1P
 - C18 TXOUT_U1N
 - B17 TXOUT_U2P
 - A18 TXOUT_U2N
 - B18 TXOUT_U3P
 - A18 TXOUT_U3N
 - E15 TXCLK_LP
 - D15 TXCLK_LN
 - G15 TXCLK_UP
 - G15 TXCLK_UN
 - D14 LPVDD
 - E14 LPVSS
 - A12 LVDDR18D
 - B12 LVDDR18D
 - C13 LVDDR33
 - A16 LVSSR
 - A14 LVSSR
 - D12 LVSSR
 - C19 LVSSR
 - C15 LVSSR
 - C16 LVSSR
 - F14 LVSSR
 - F15 LVSSR
 - E12 LVDS_DIGON
 - G12 LVDS_BLON
 - F12 LVDS_BLEN_NB
 - AD14 GPP_TX0P
 - AD15 GPP_TX0N
 - AE15 DEBUE6
 - AD16 GPP_RX0P
 - AE16 GPP_RX0N
 - AC17 DEBUE9
 - AD18 DEBUE10
 - AD19 GPP_TX1N
 - AD19 GPP_TX1P
 - AE20 GPP_RX1N
 - AD20 GPP_RX1P
 - AE21 DEBUE15
 - AD13 DEBUE0
 - AC13 DEBUE2
 - AE13 DEBUE1
 - AE17 DEBUE3
 - AD17 DEBUE4
 - B14 GMCH_TXAOUT0+
 - B15 GMCH_TXAOUT0-
 - B13 GMCH_TXAOUT1+
 - A13 GMCH_TXAOUT1-
 - H14 GMCH_TXAOUT2+
 - G14 GMCH_TXAOUT2-
 - D17 GMCH_TXAOUT3+
 - E17 GMCH_TXAOUT3-
 - A15 GMCH_TXBOUT0+
 - B16 GMCH_TXBOUT0-
 - C17 GMCH_TXBOUT1+
 - C18 GMCH_TXBOUT1-
 - B17 GMCH_TXBOUT2+
 - A18 GMCH_TXBOUT2-
 - B18 GMCH_TXBOUT3+
 - A18 GMCH_TXBOUT3-
 - E15 GMCH_TXACLK+
 - D15 GMCH_TXACLK-
 - G15 GMCH_TXBCLK+
 - G15 GMCH_TXBCLK-
 - A12 LVDDR18A_S0
 - B12 LVDDR18A_S0
 - C13 LVDDR18A_S0
 - A16 GPP_TX0P
 - AD15 GPP_TX0N
 - AE15 DEBUE6
 - AD16 GPP_RX0P
 - AE16 GPP_RX0N
 - AC17 DEBUE9
 - AD18 DEBUE10
 - AD19 GPP_TX1N
 - AD19 GPP_TX1P
 - AE20 GPP_RX1N
 - AD20 GPP_RX1P
 - AE21 DEBUE15
 - AD13 DEBUE0
 - AC13 DEBUE2
 - AE13 DEBUE1
 - AE17 DEBUE3
 - AD17 DEBUE4
- LVDS**
- DVO**



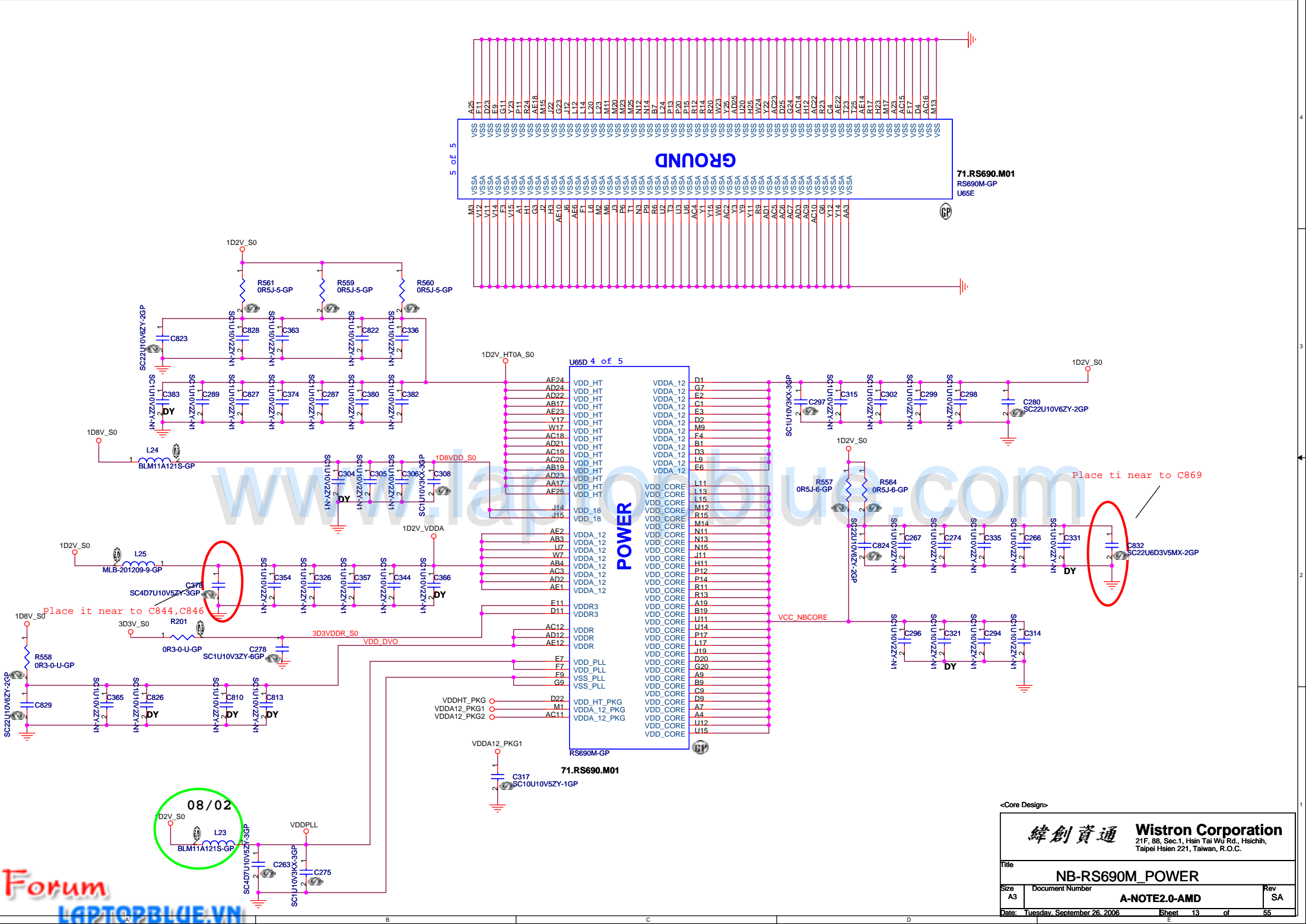
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **NB-RS690M_VIDEO/ CLOCK**

Size: A3	Document Number: A-NOTE2.0-AMD	Rev: SA
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08/02

<Core Design>

緯創資通 Wistron Corporation
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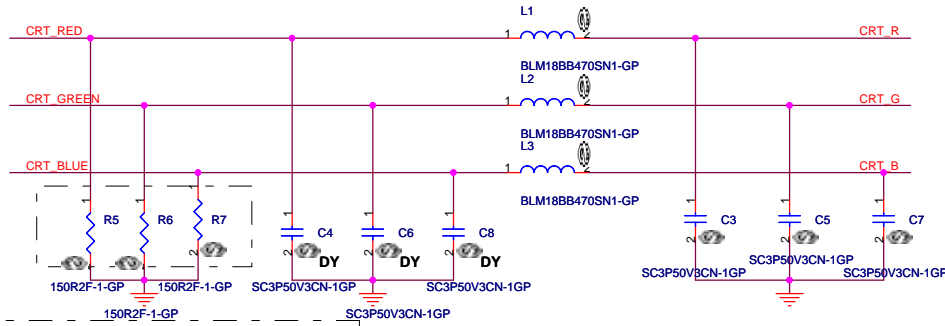
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Size: A3 Document Number: **A-NOTE2.0-AMD** Rev: SA

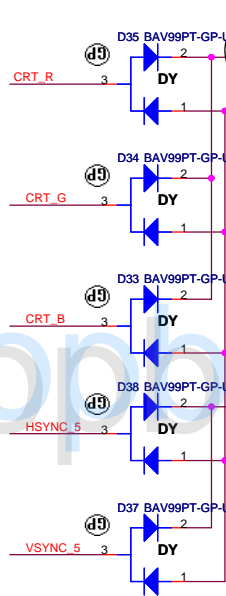
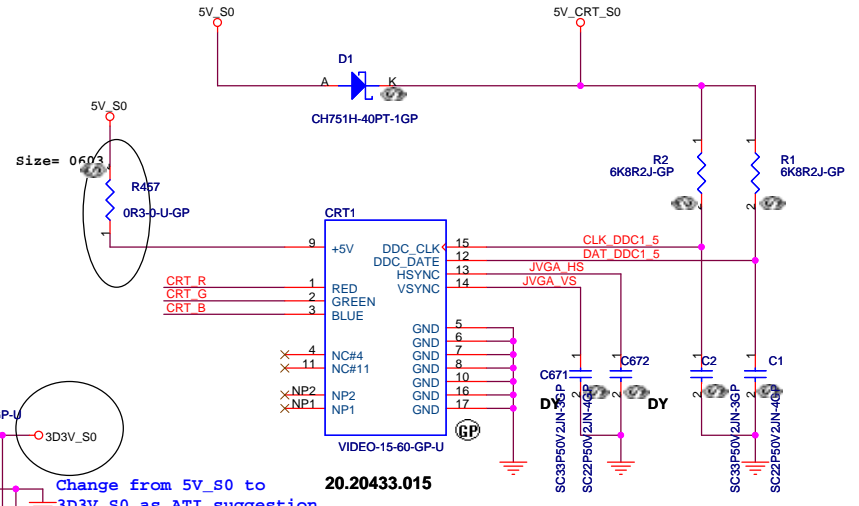
Date: Tuesday, September 26, 2006 Sheet 13 of 55

CRT I/F & CONNECTOR

Ferrite bead impedance: 47ohm@100MHz

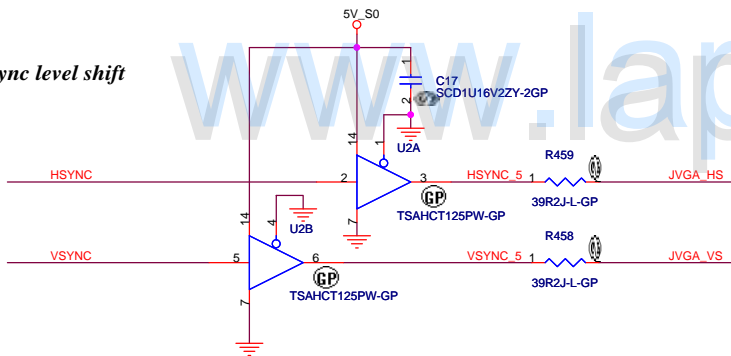


Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 R857--R859 Close to CRT Conn, the trace impedance between NB and 150ohm resistor should be 50ohm+/-15%, the trace impedance between 150ohm resistor and conn should be 75ohm+/-15%

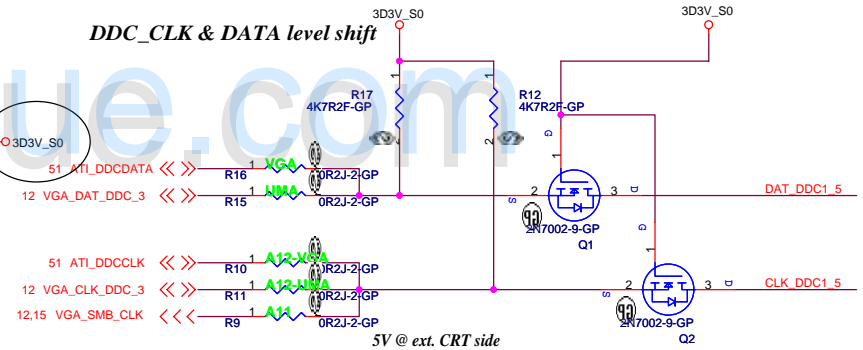


Change from 5V_S0 to 3D3V_S0 as ATI suggestion.
 20.20433.015

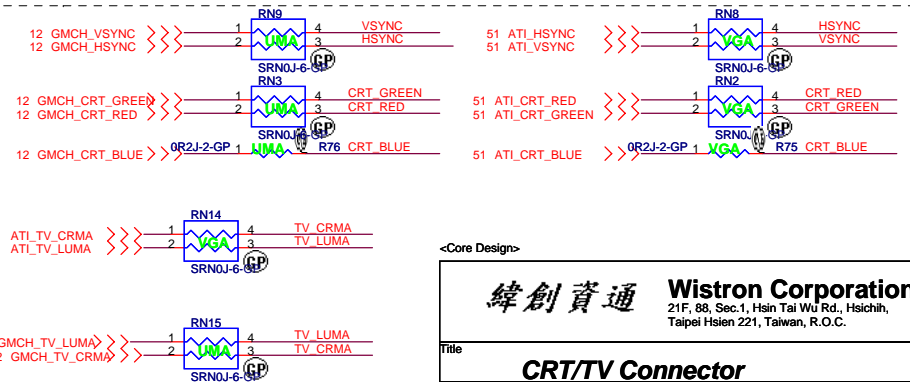
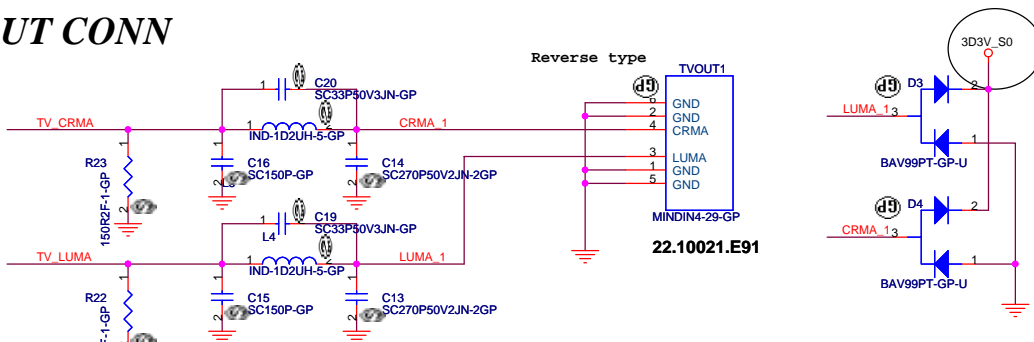
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV OUT CONN



<Core Design>

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Title: **CRT/TV Connector**

Size: A3	Document Number: A-NOTE2.0-AMD	Rev: SA
Date: Tuesday, September 26, 2006	Sheet: 14	of: 55

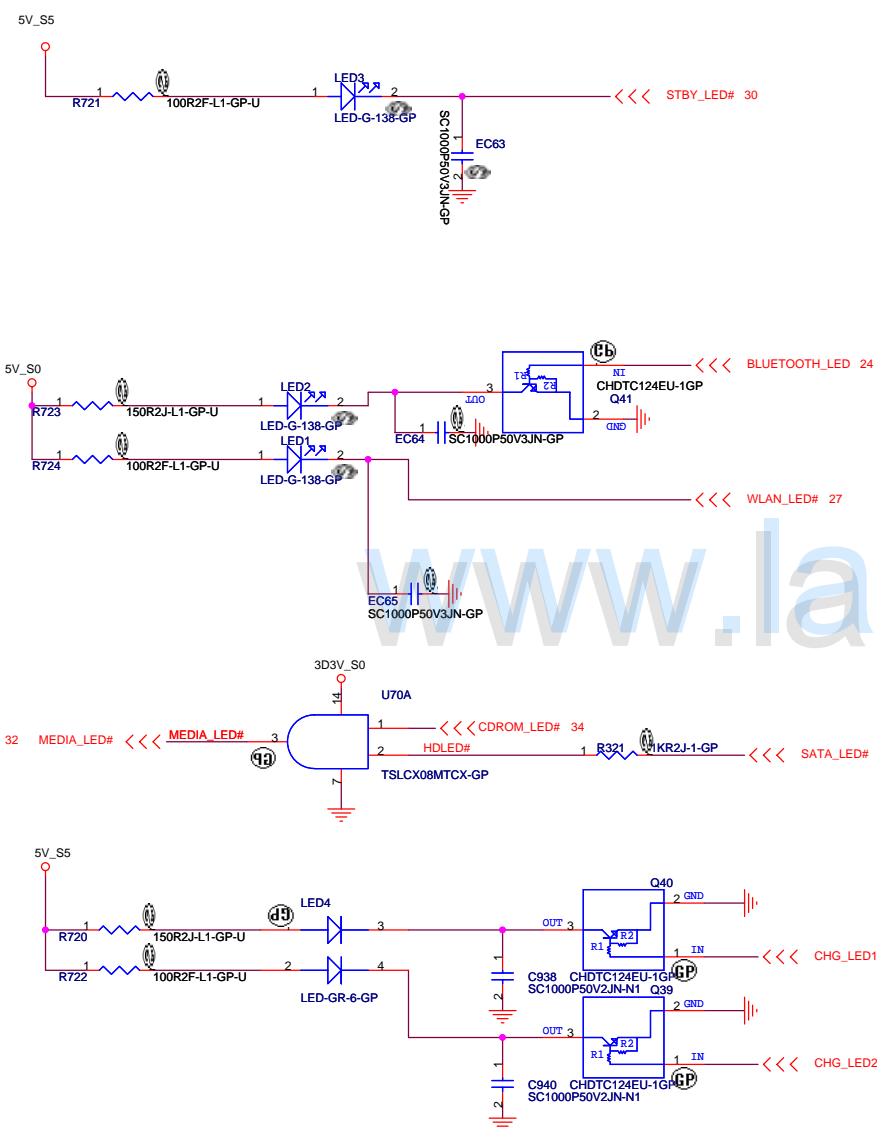
LED / INVERTER INTERFACE

LCD/INVERTER/CCD CONN

TOP VIEW

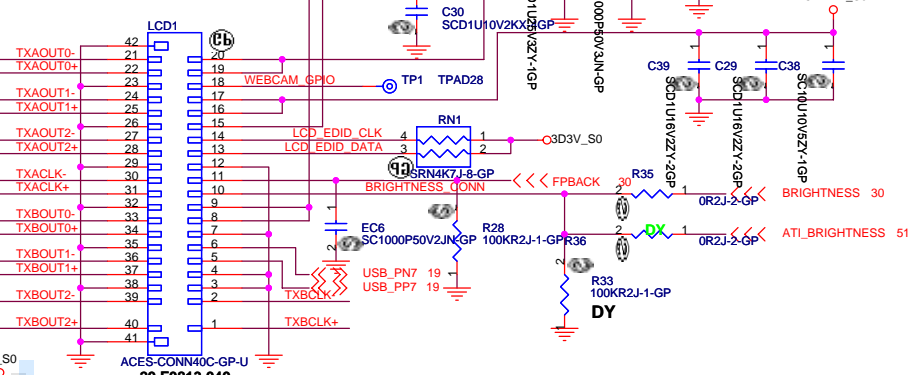
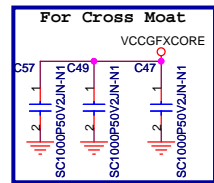
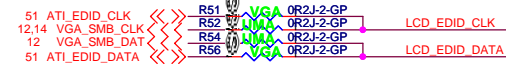
LCD

1

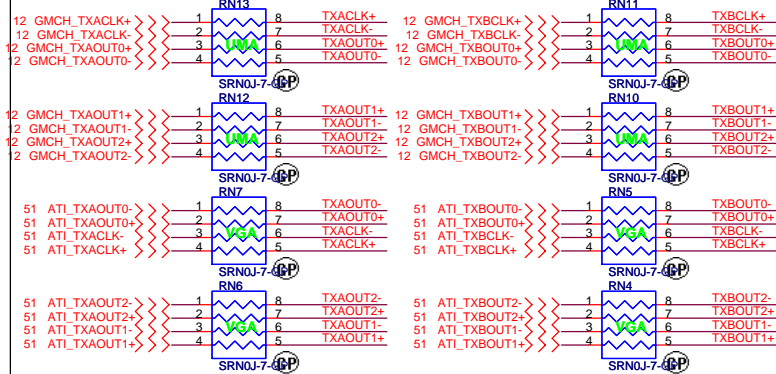
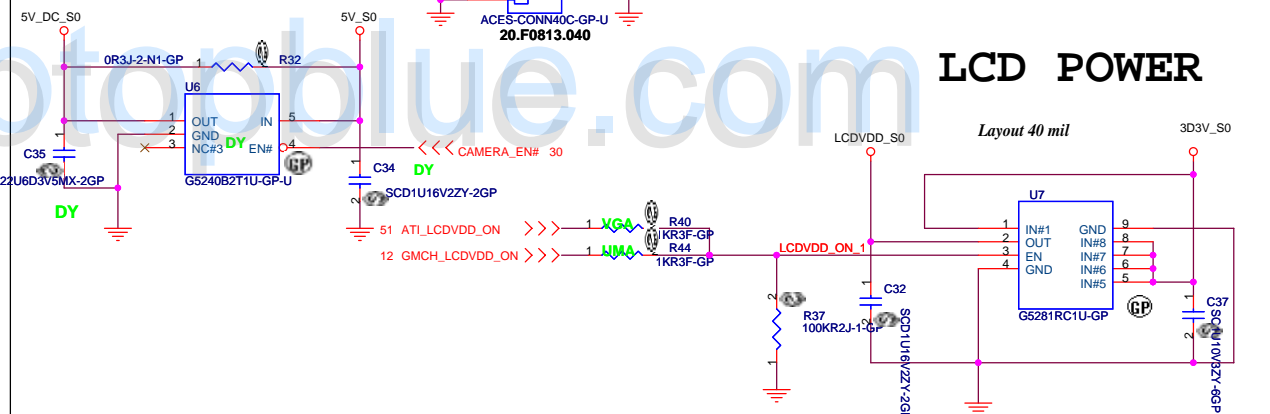


Pin	Symbol
1	5V
2	USB-
3	USB+
4	GPIO
5	GND

Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND



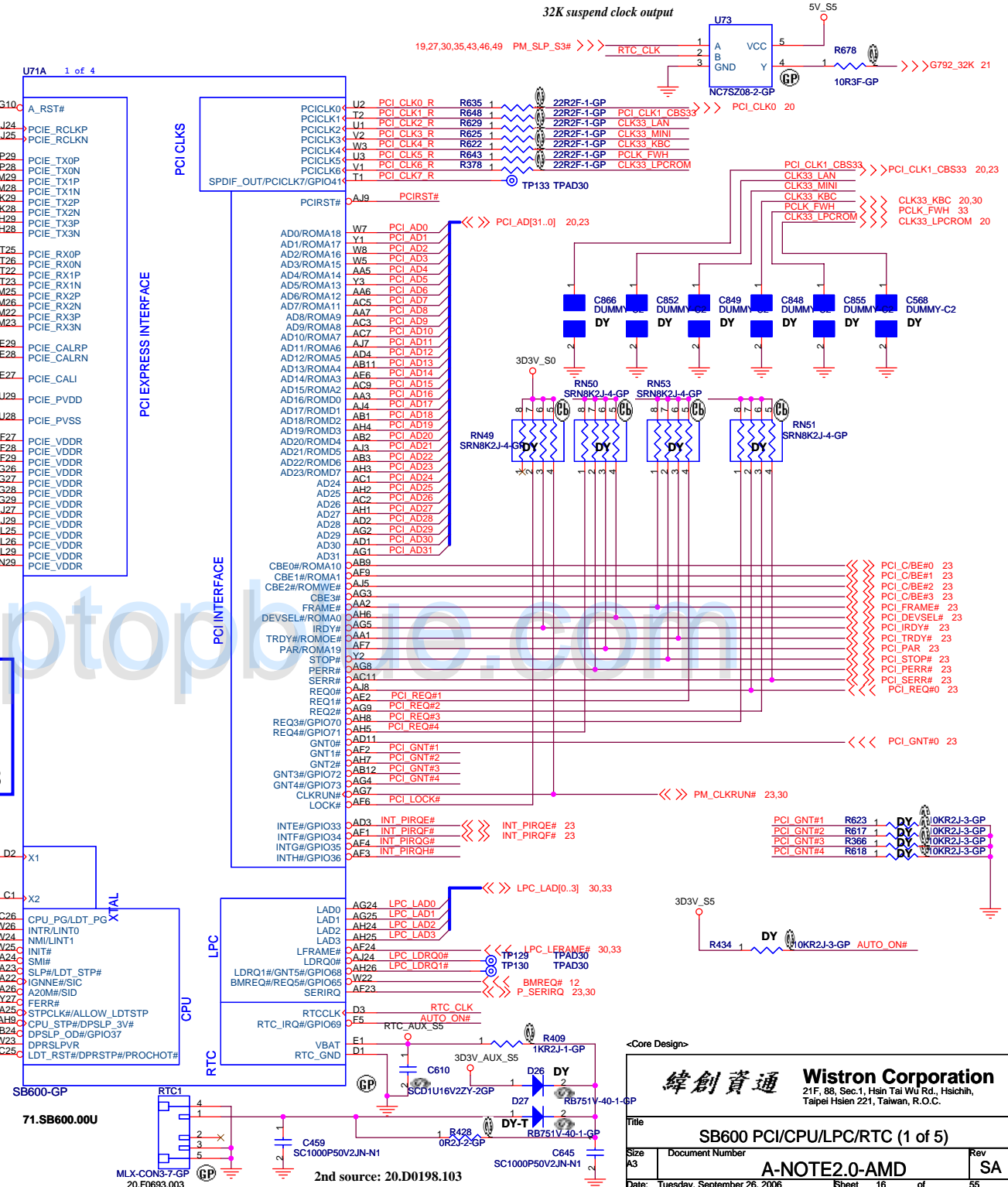
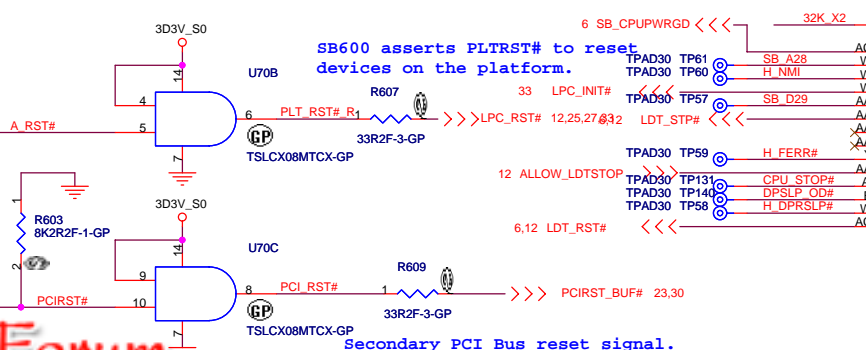
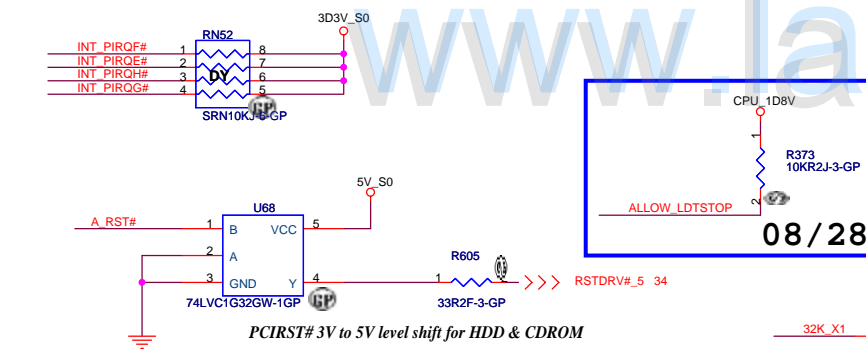
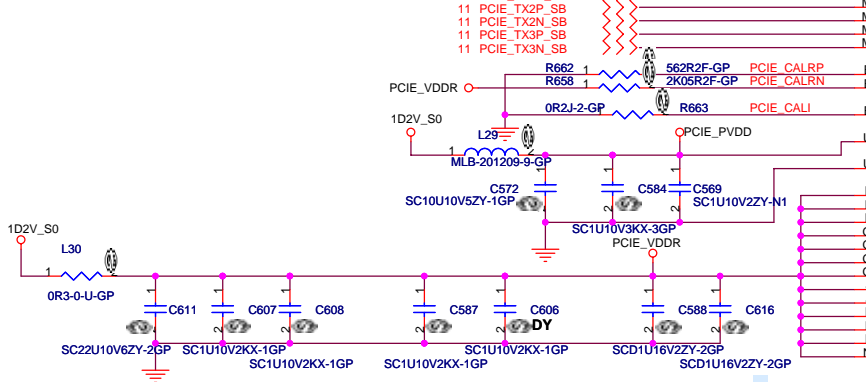
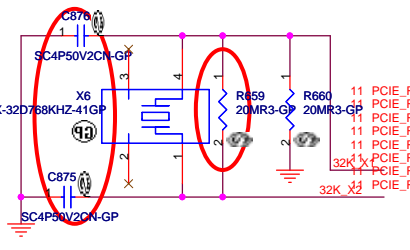
LCD POWER



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Title	INV / LCD	
Size	Document Number	Rev SA
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Place these components close to U13 and use ground guard for 32K_X1 and 32K_X2.



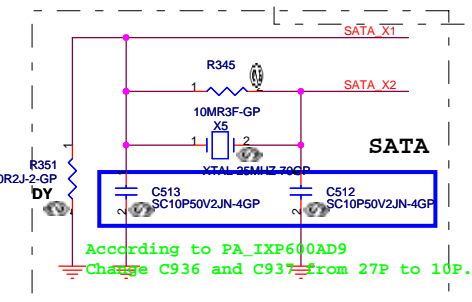
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

SB600 PCI/CPU/LPC/RTC (1 of 5)

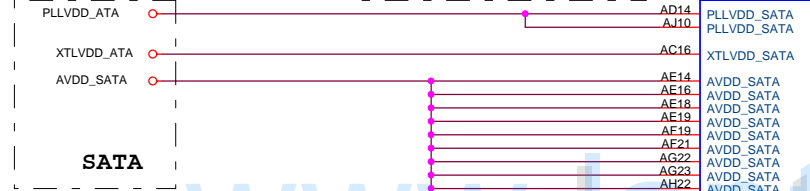
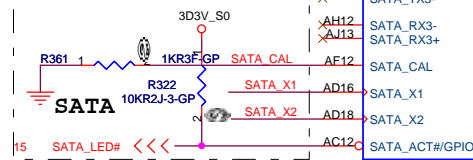
Size A3 Document Number A-NOTE2.0-AMD Rev SA

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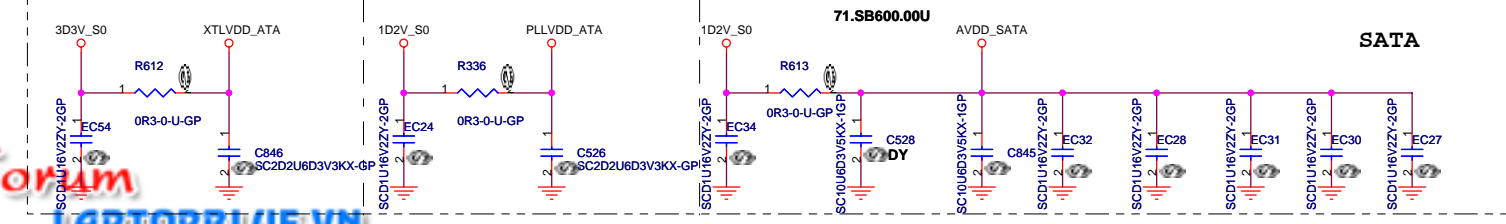
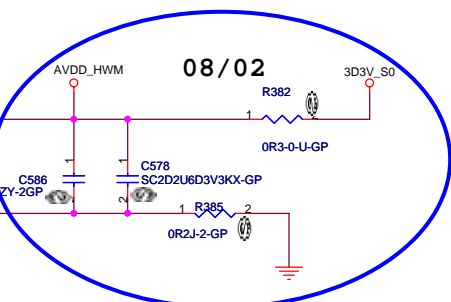
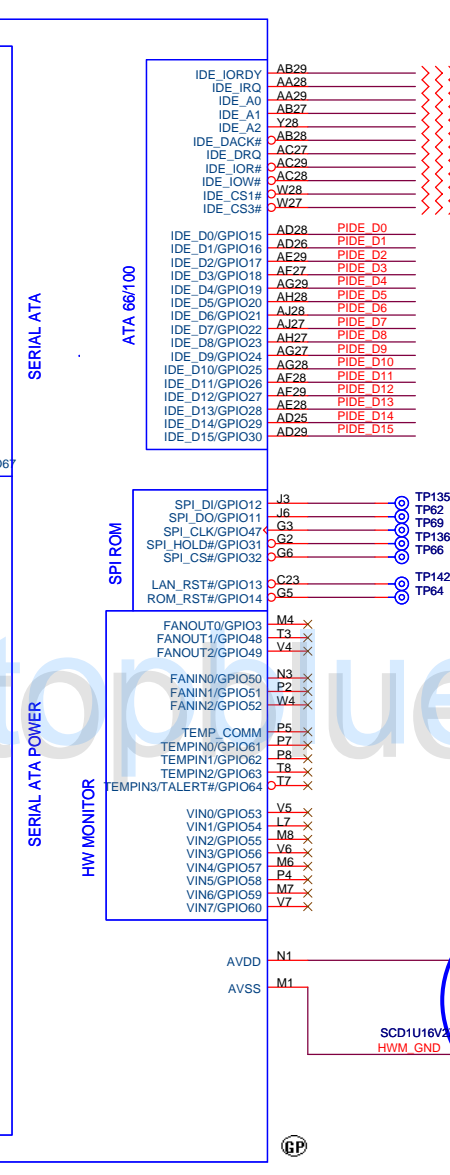
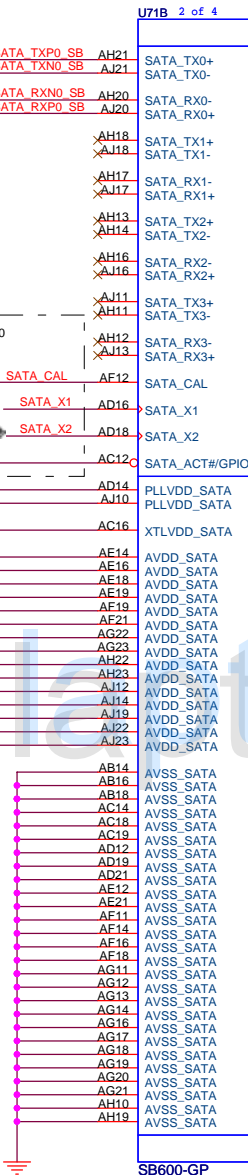
PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460



According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.



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<Core Design>

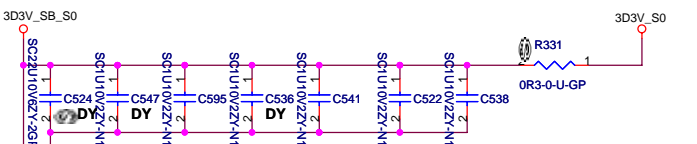
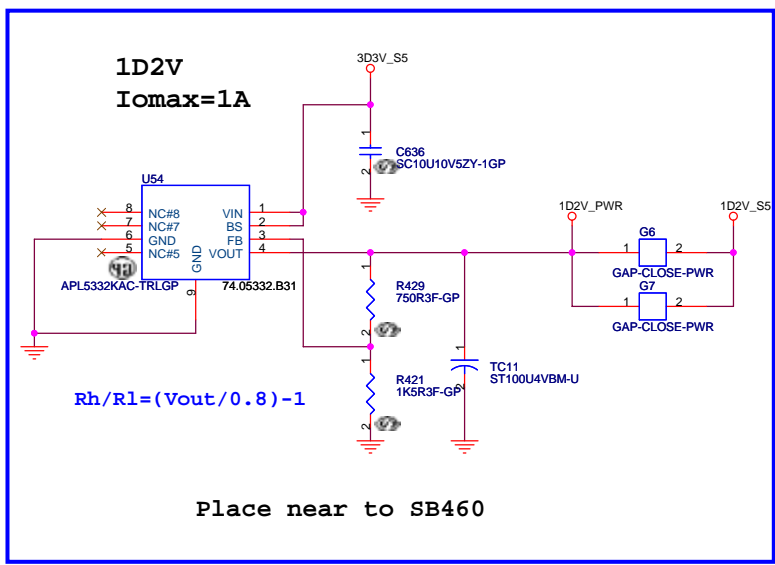
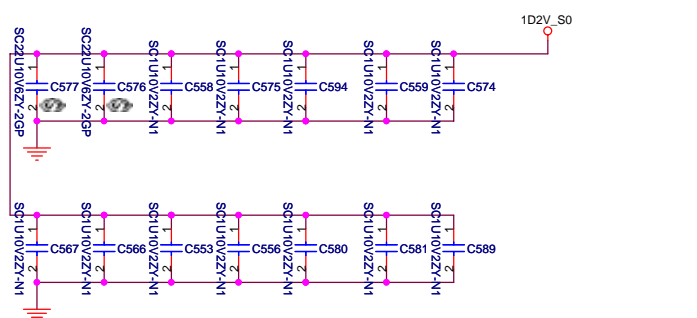
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)

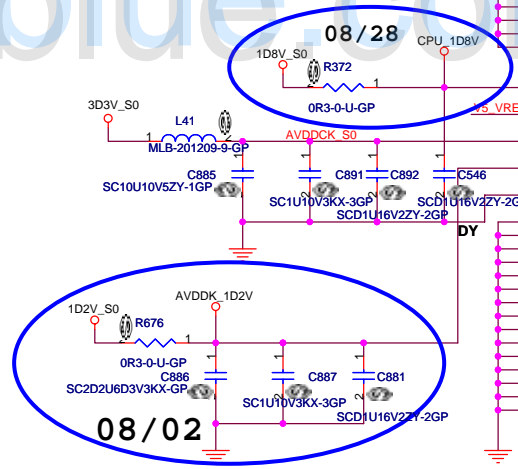
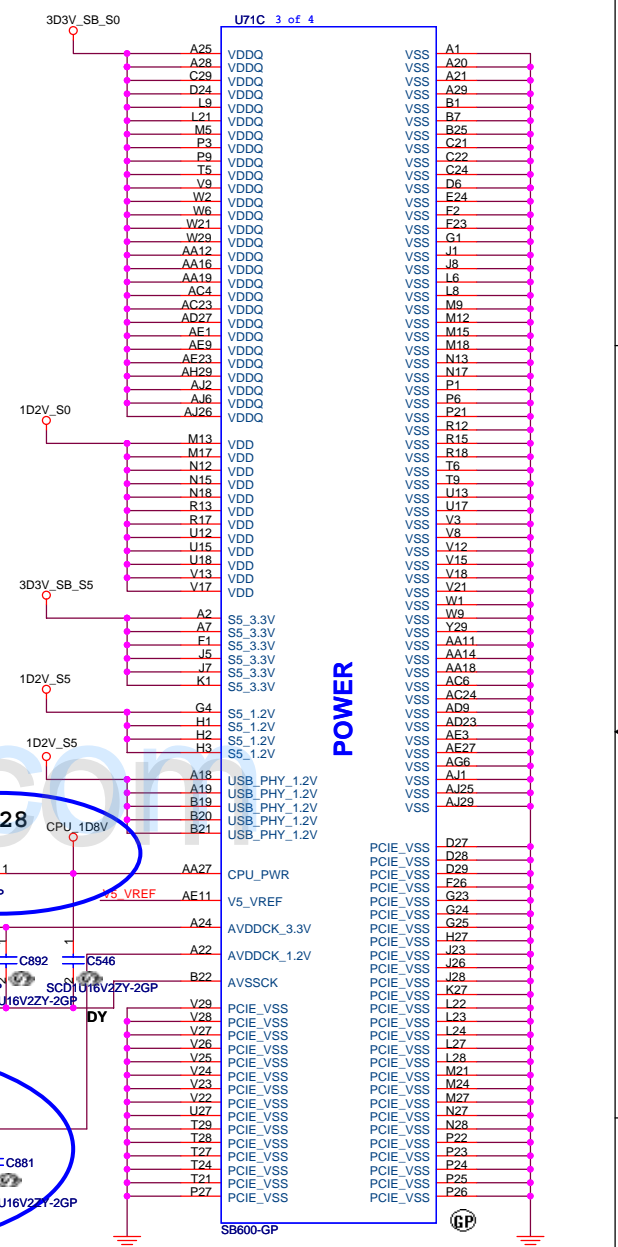
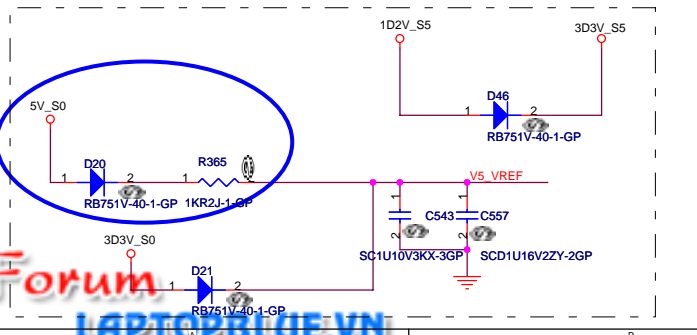
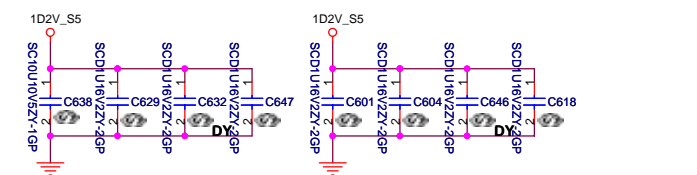
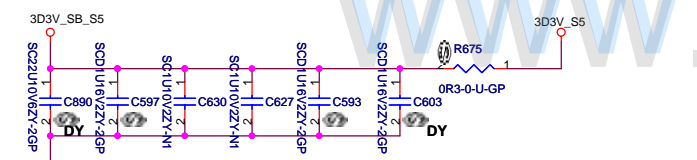
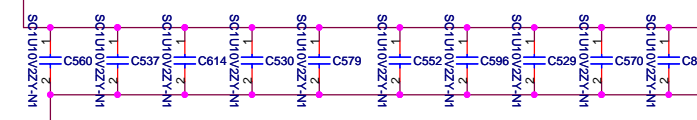
Size A3 Document Number A-NOTE2.0-AMD Rev SA

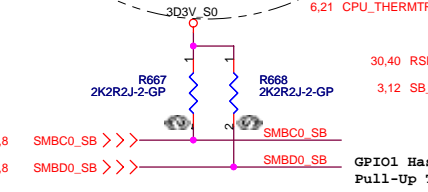
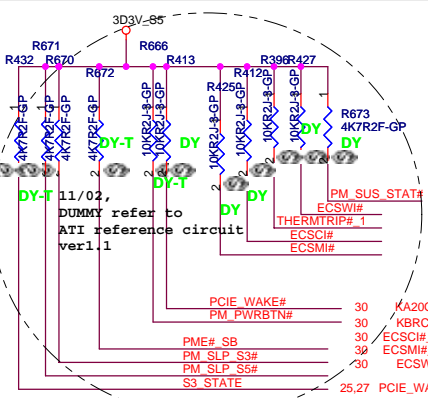
Date: Tuesday, September 26, 2006 Sheet 17 of 55

Forum LAPTOPBLUE.VN



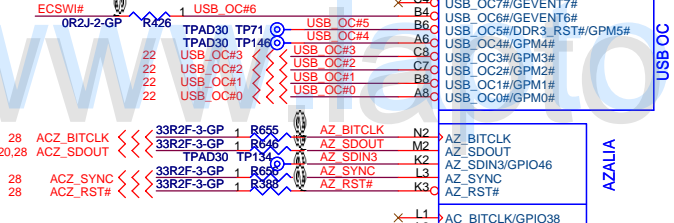
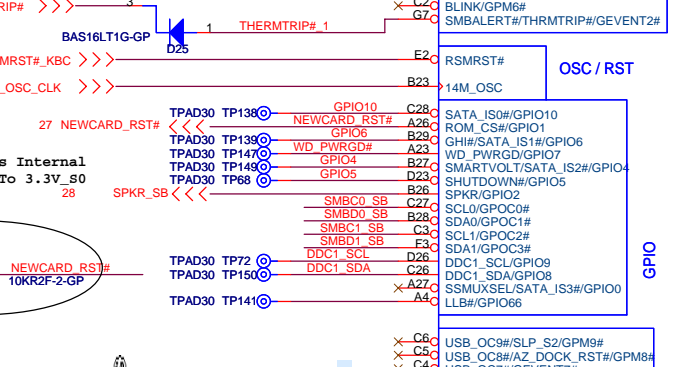
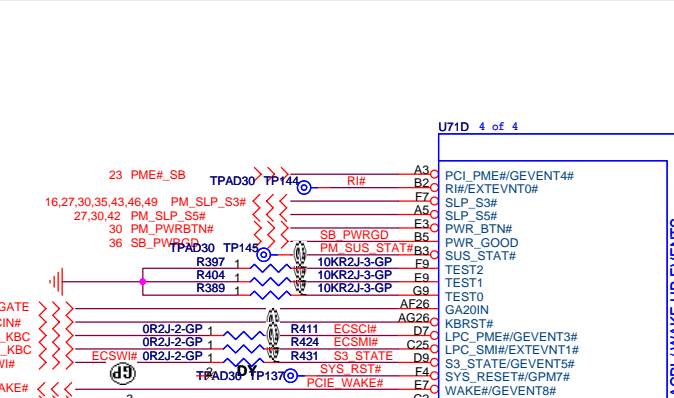
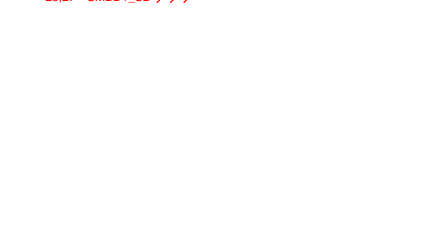
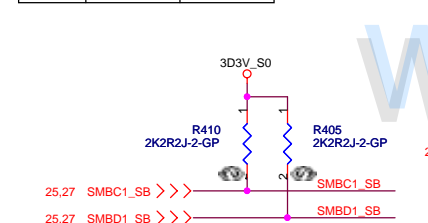
2Pin Use One Capacitance Uniformly.



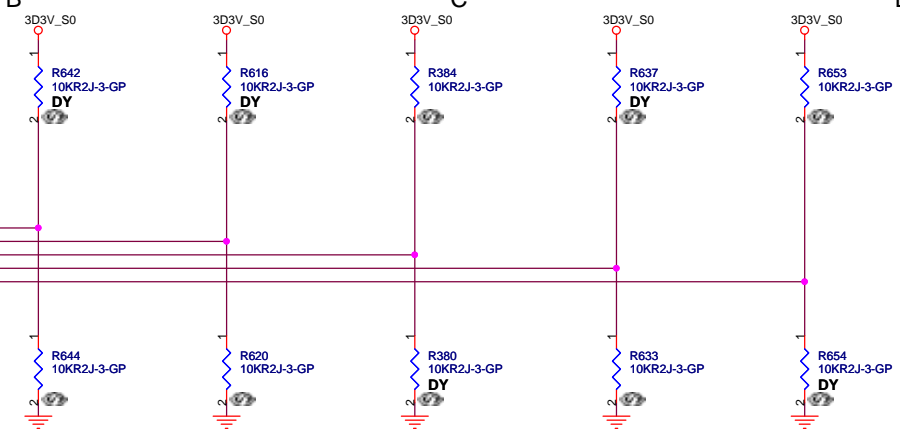


Lynx Board Version Setting

Ver.	PCB_VER0	PCB_VER1
SA	0	0
SB	0	1
SC	1	0
SD	1	1



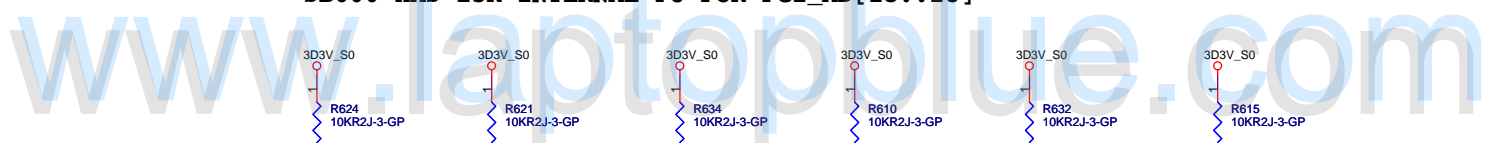
19,28 AC2_SDOUT
 16,30 CLK33_KBC
 16 CLK33_LPCROM
 16 PCI_CLK0
 16,23 PCI_CLK1_CBS33



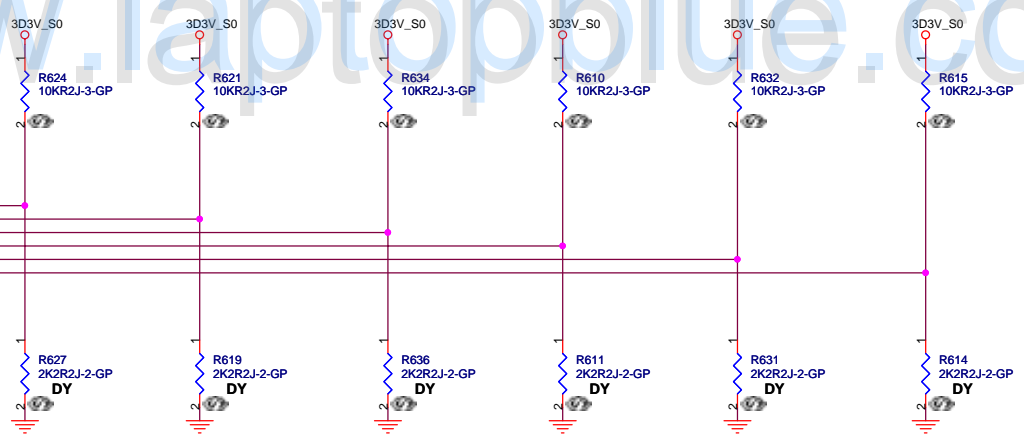
REQUIRED SYSTEM STRAPS

		AC_SDOUT	PCI_CLK0, PCI_CLK1_CBS33	PCI_CLK4	PCI_CLK6
STRAP HIGH		USE DEBUG STRAPS	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	USB INT PLL48	CPU I/F=K8 DEFAULT
STRAP LOW		IGNORE DEBUG STRAPS DEFAULT	L,H=LPC ROM II L,L=Firmware Hub ROM	USB EXT. 48MHZ DEFAULT	CPU I/F=P4

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



16,23 PCI_AD28
 16,23 PCI_AD27
 16,23 PCI_AD26
 16,23 PCI_AD25
 16,23 PCI_AD24
 16,23 PCI_AD23



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

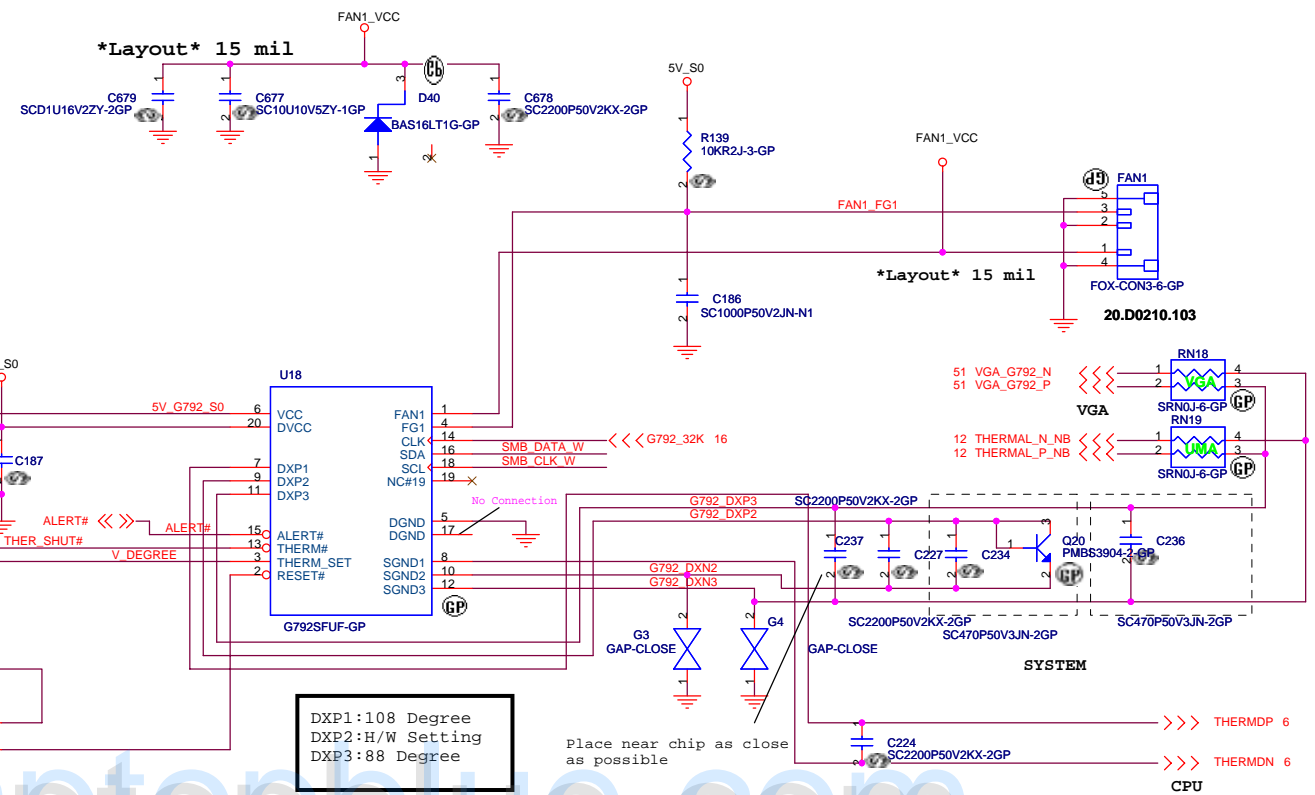
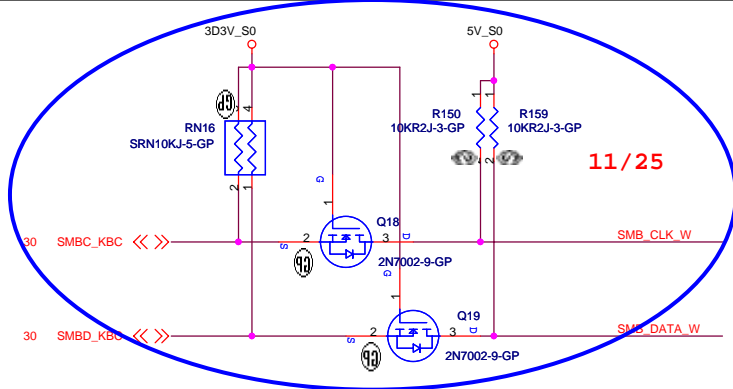
<Core Design>

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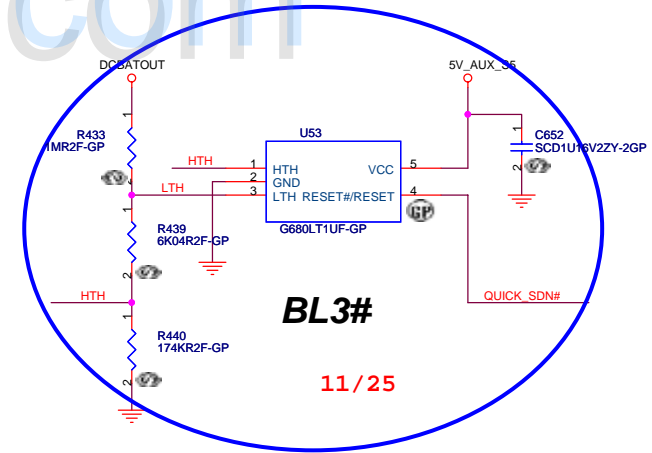
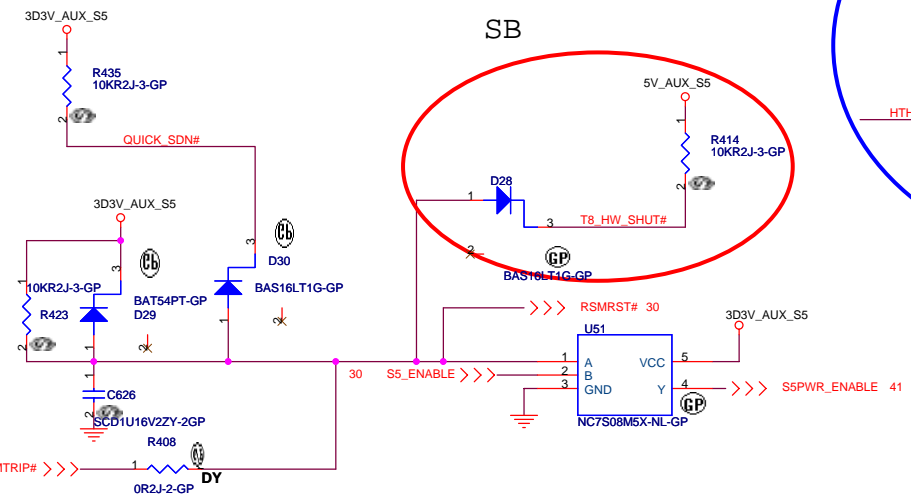
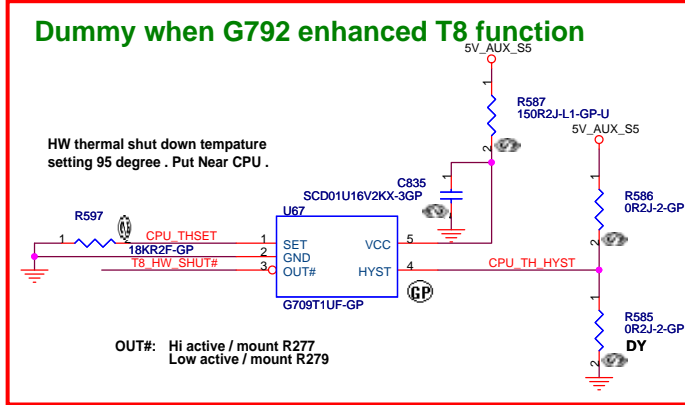
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Size A3 Document Number **A-NOTE2.0-AMD** Rev SA

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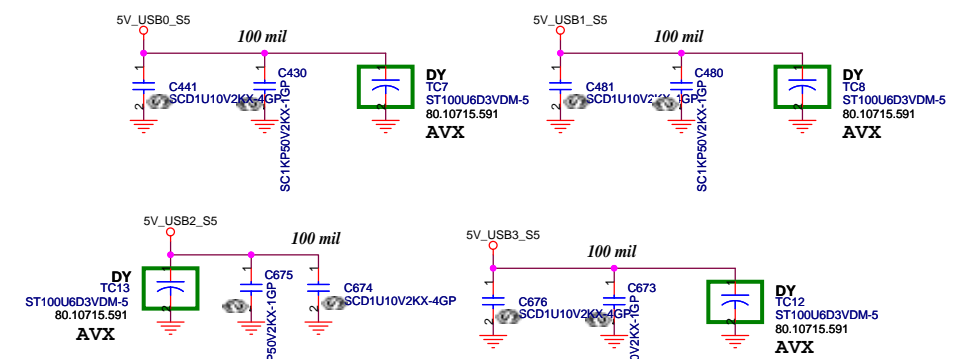
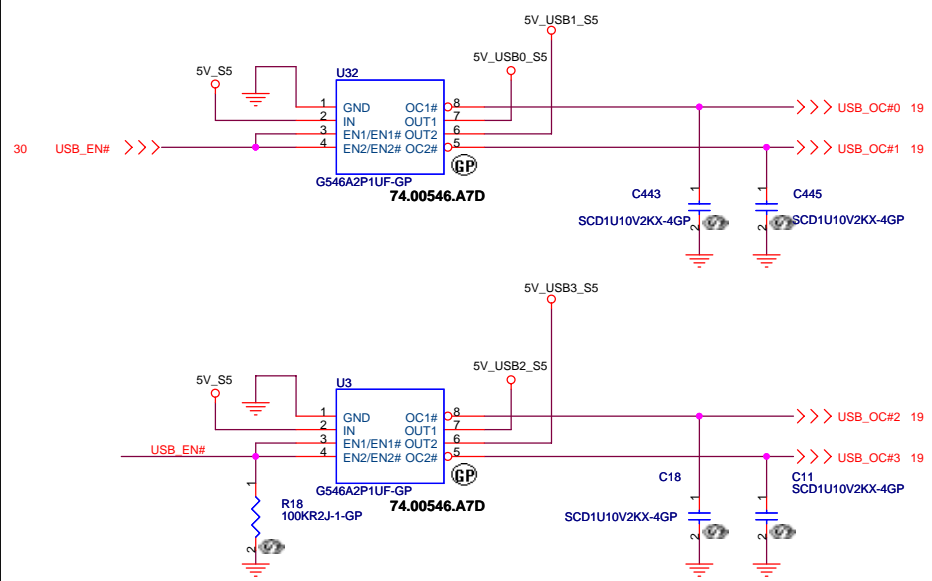


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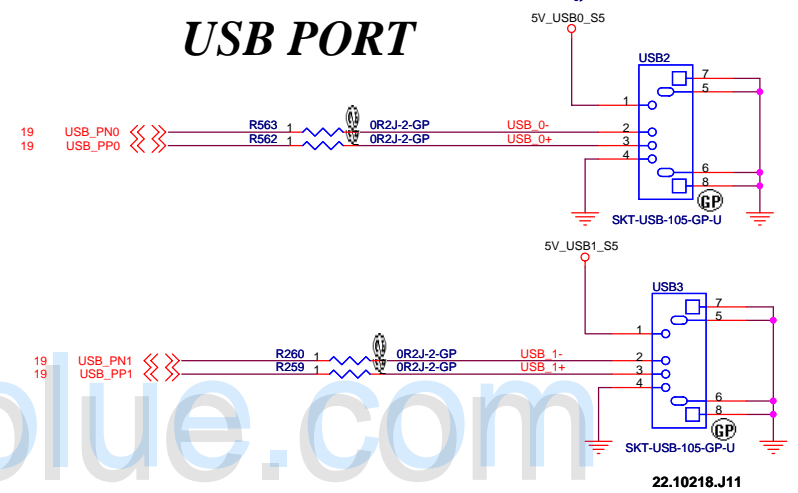


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G792			
Title			
Size A3	Document Number	Rev SA	
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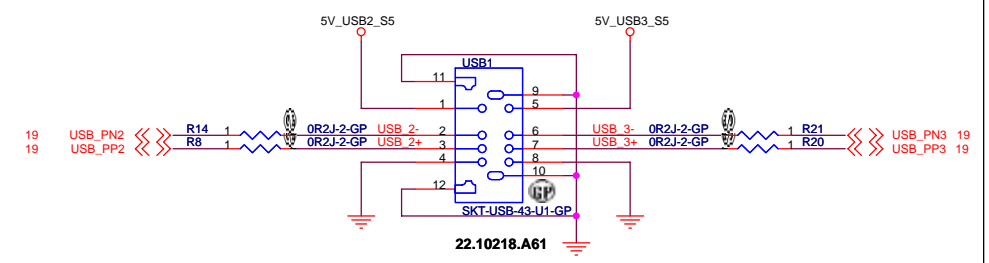
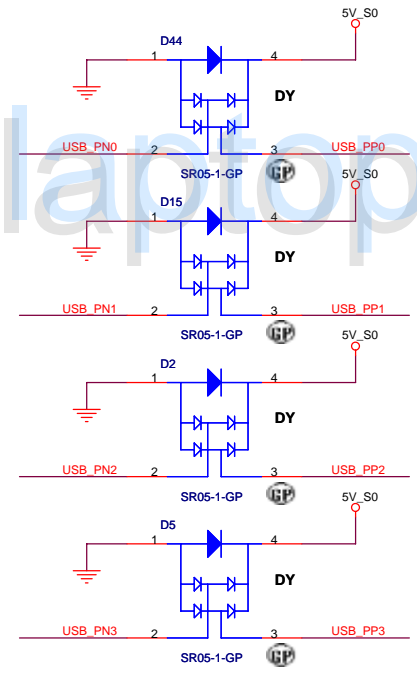
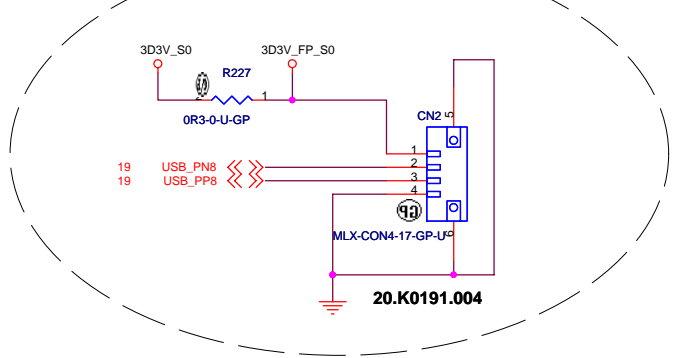


USB PORT



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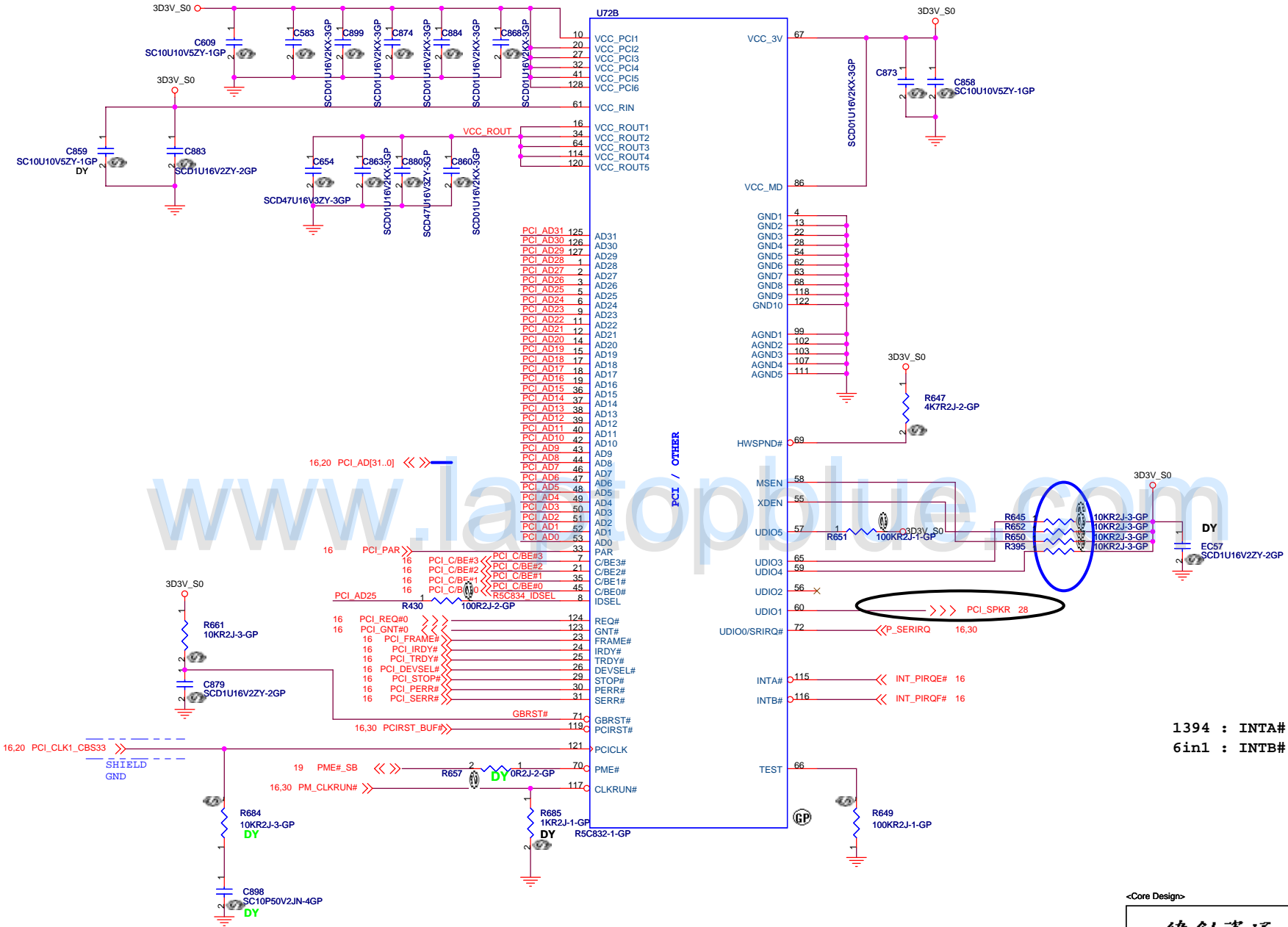
Finger Printer CNN



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title USB/MDC/BT and TV TURNER I/F		
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
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1394 : INTA#
6in1 : INTB#

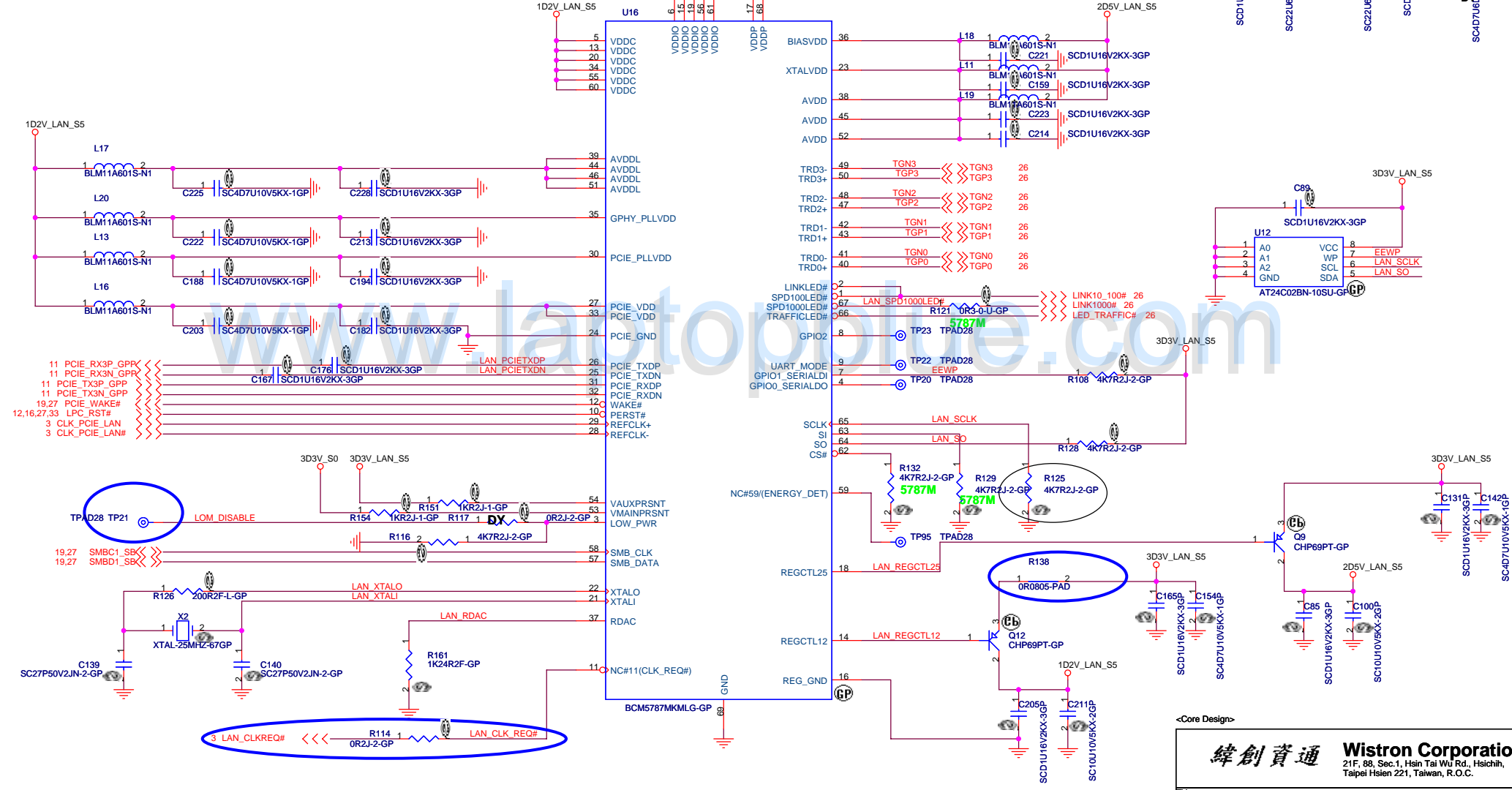
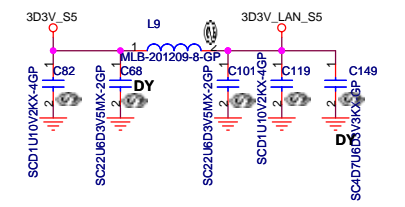
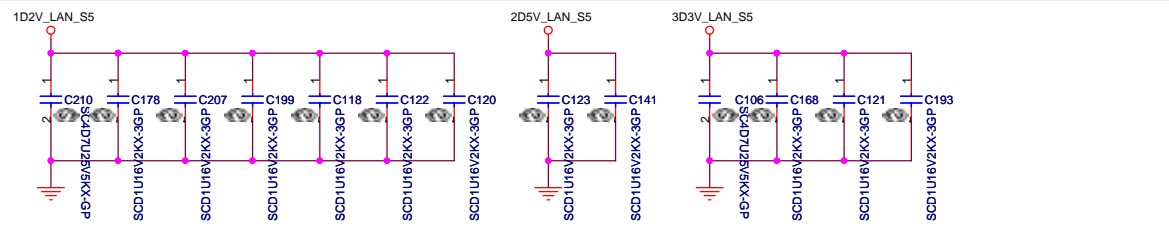
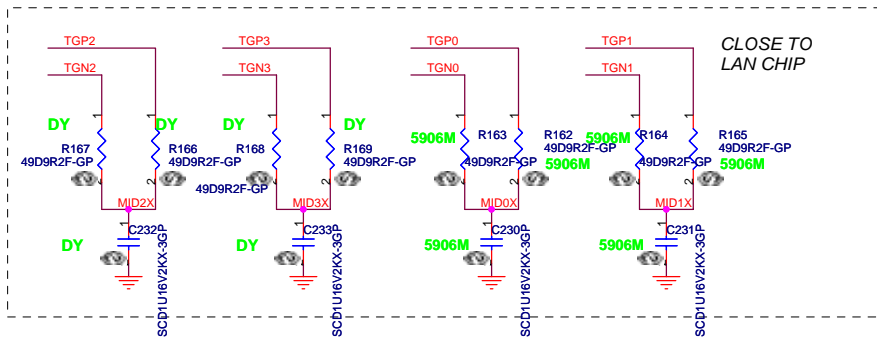
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Title: **RICOH R5C832(1/2)**

Size A3 Document Number: **A-NOTE2.0-AMD** Rev SA

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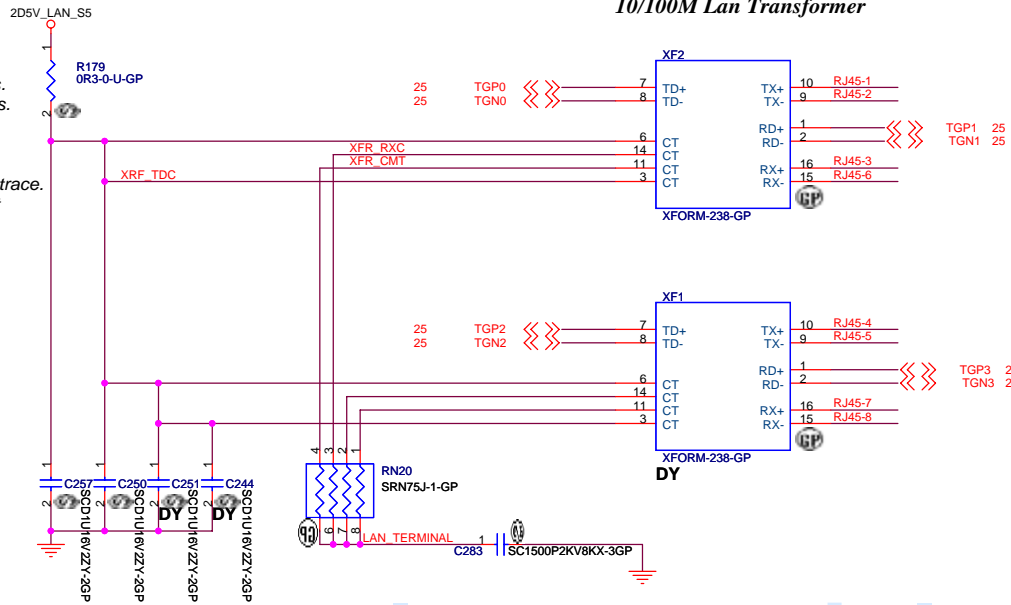


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緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title LAN BCM5787M/5906M	
Size A3	Document Number A-NOTE2.0-AMD
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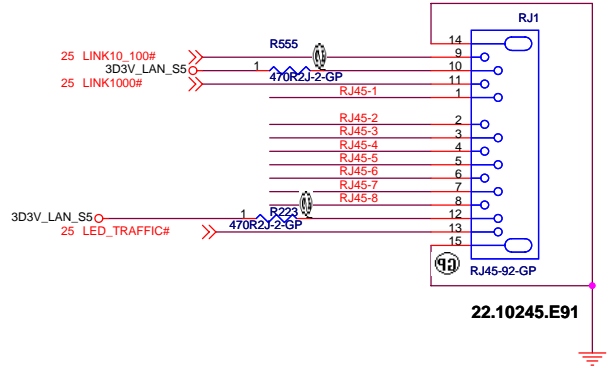
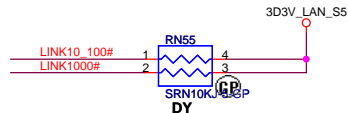
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

10/100M Lan Transformer



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PIN09 : GREEN
PIN11 : ORANGE



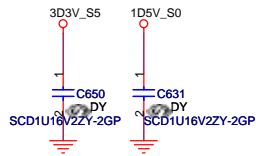
Green : Link up
Blinking : TX/RX activity

<Core Design>

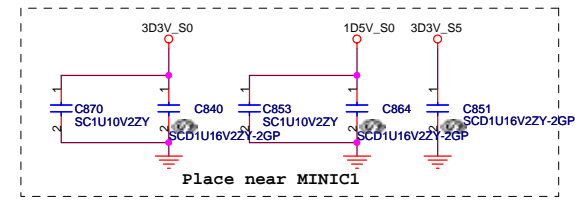
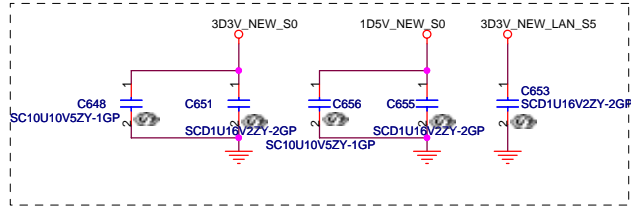
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LAN Connector	
Title	Rev
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NEWCARD Connector

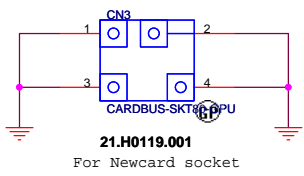
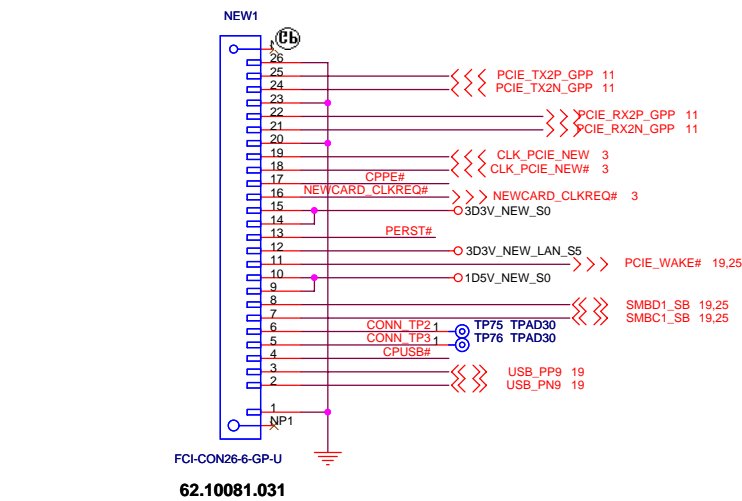
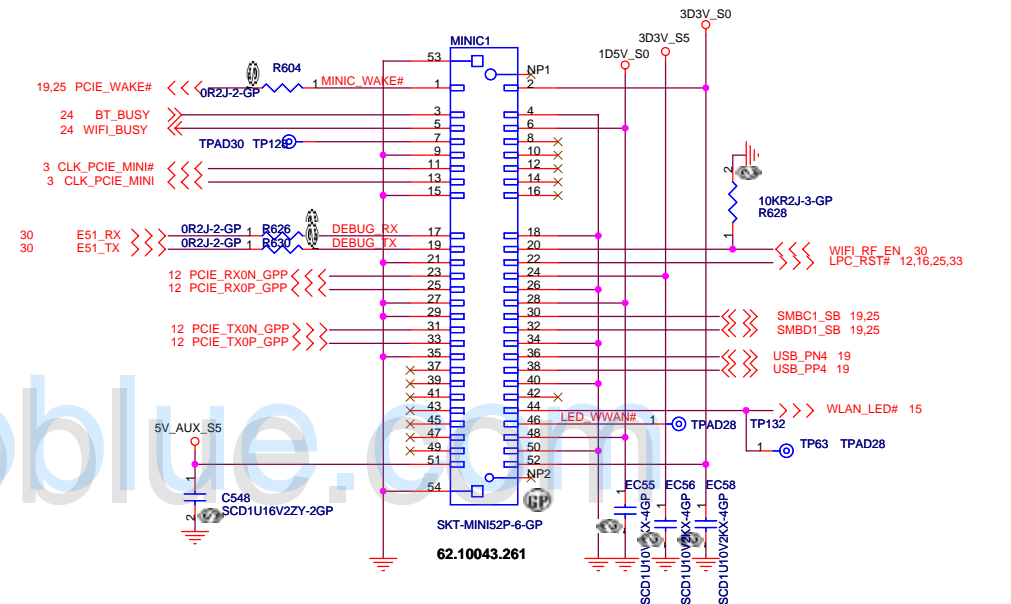
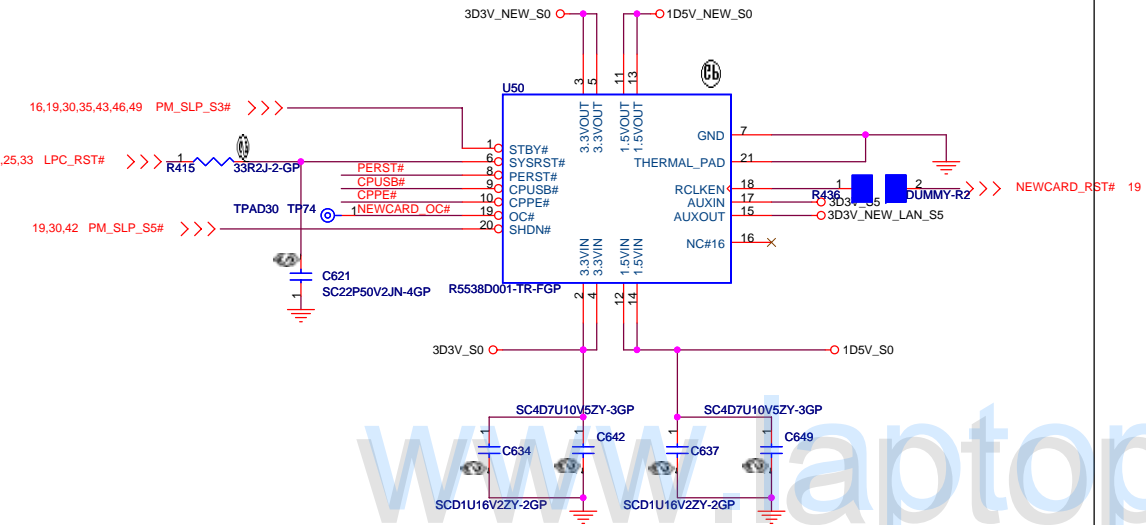
Place them Near to Chip



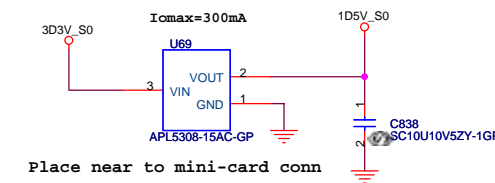
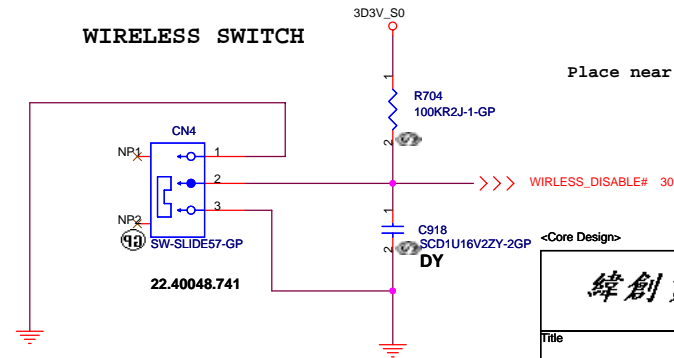
Place them Near to Connector



Mini Card Connector



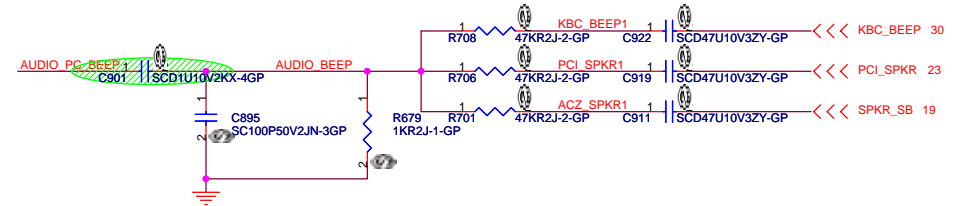
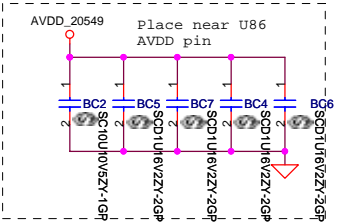
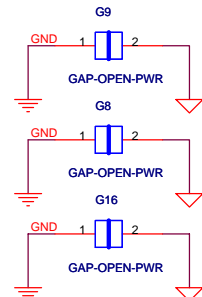
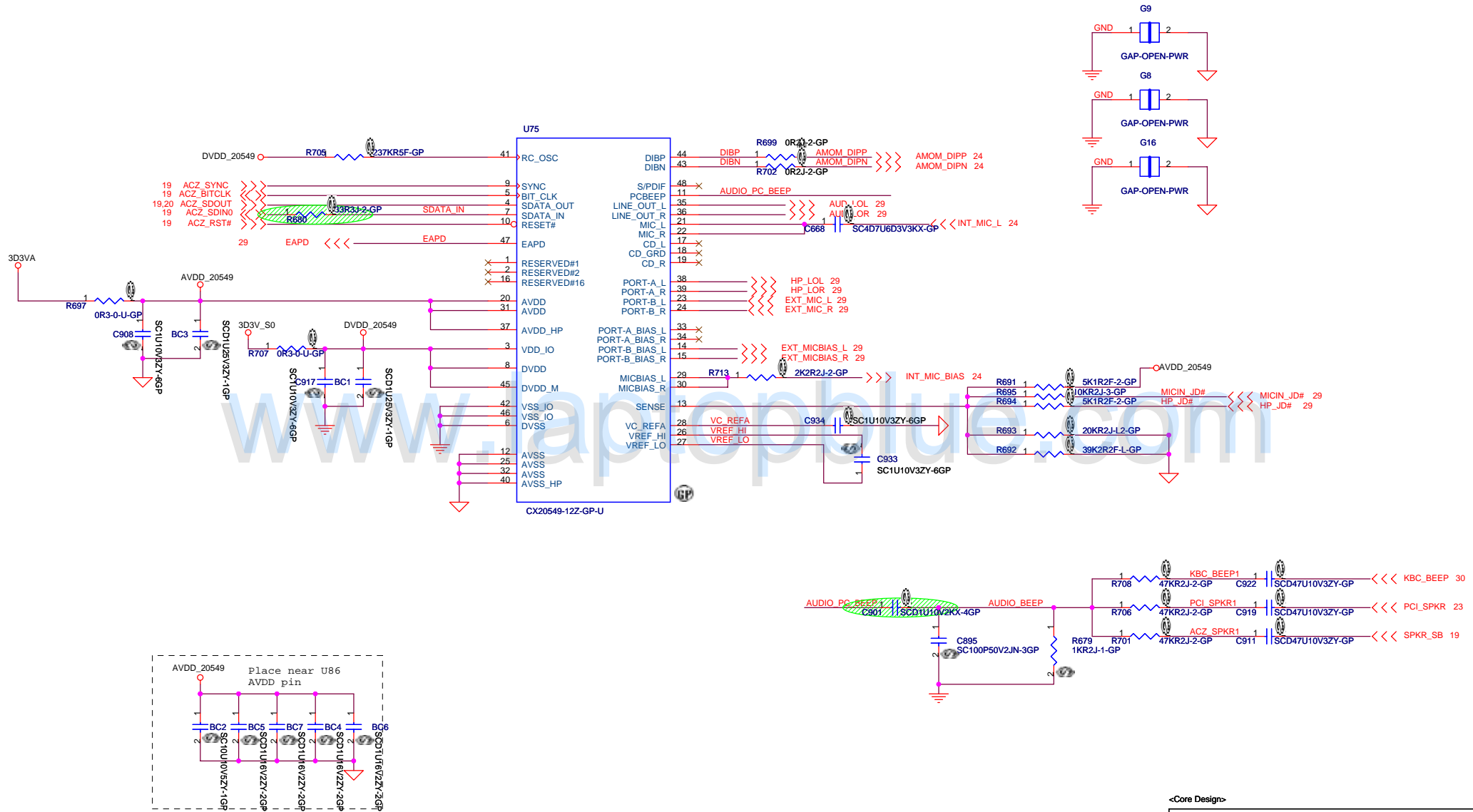
WIRELESS SWITCH



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MINI-PCIE
A-NOTE2.0-AMD

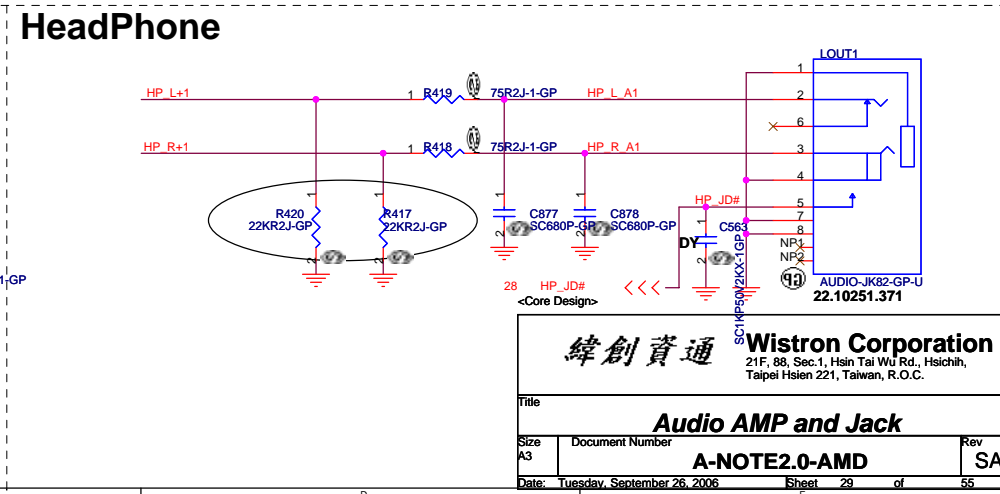
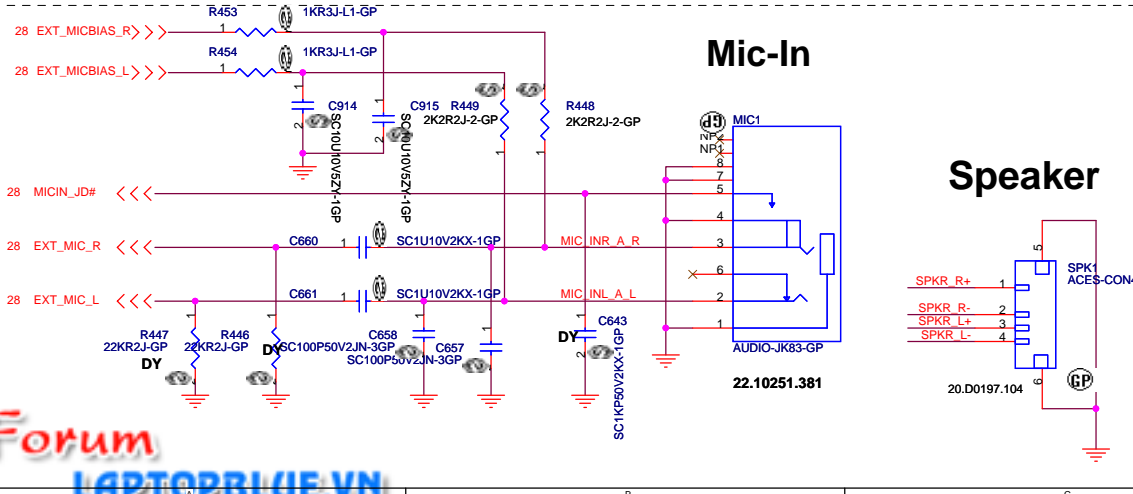
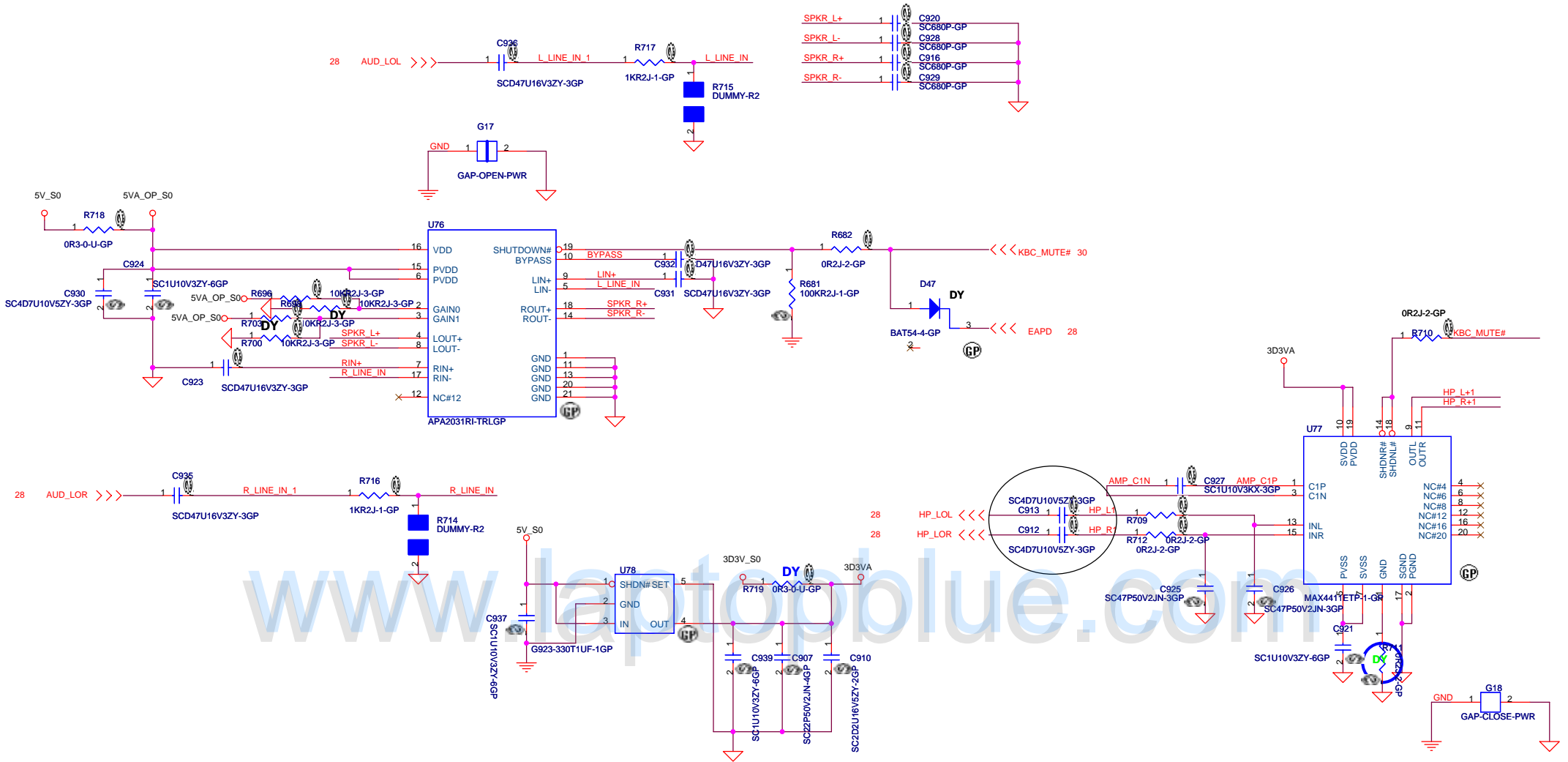
Title: SA
 Size: A3
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<Core Design>

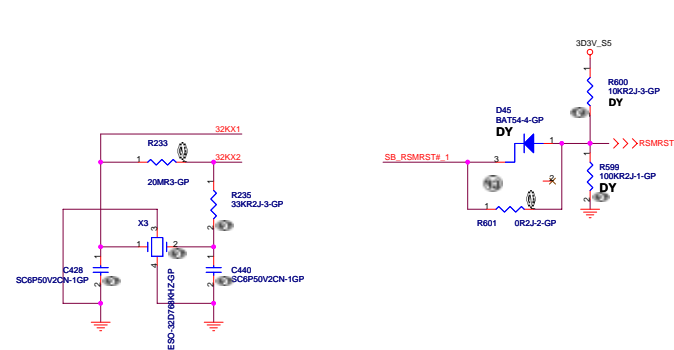
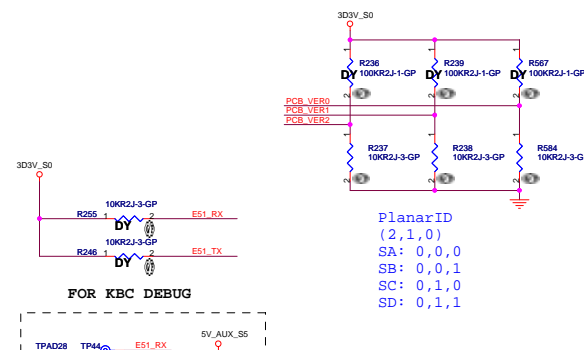
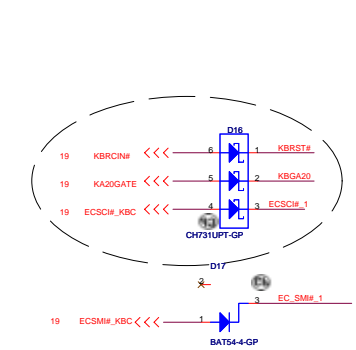
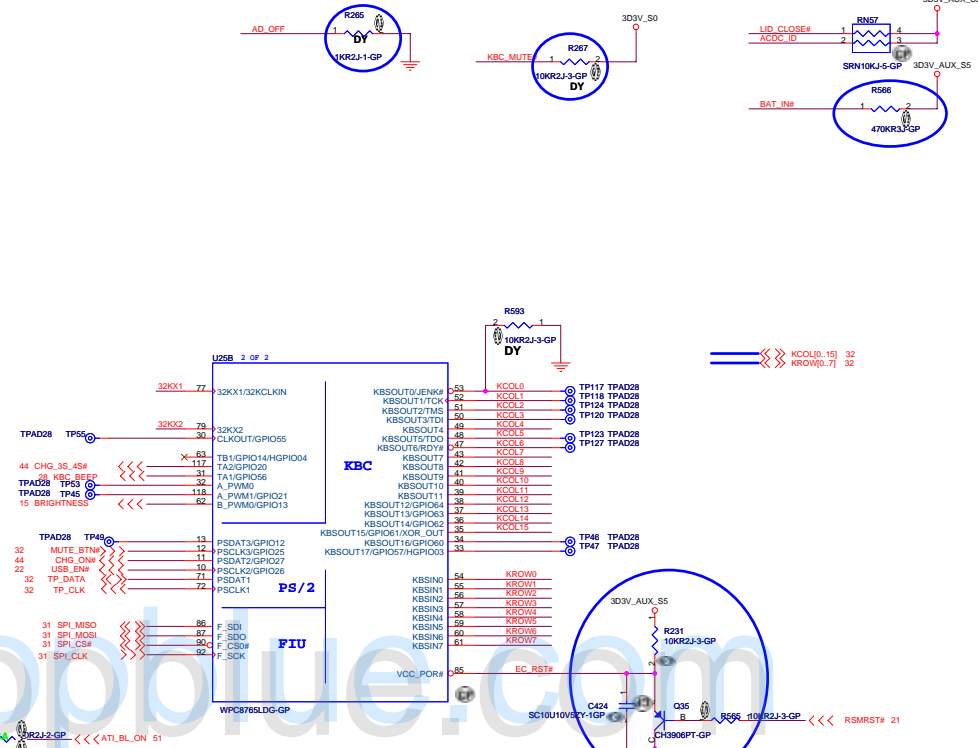
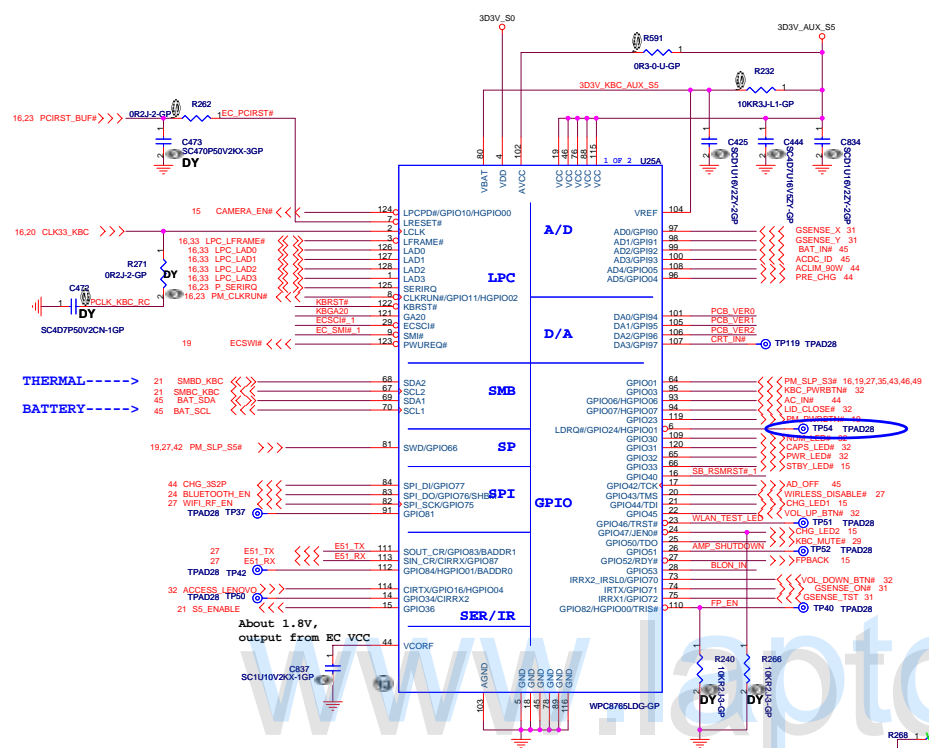
緯創資通 Wistron Corporation
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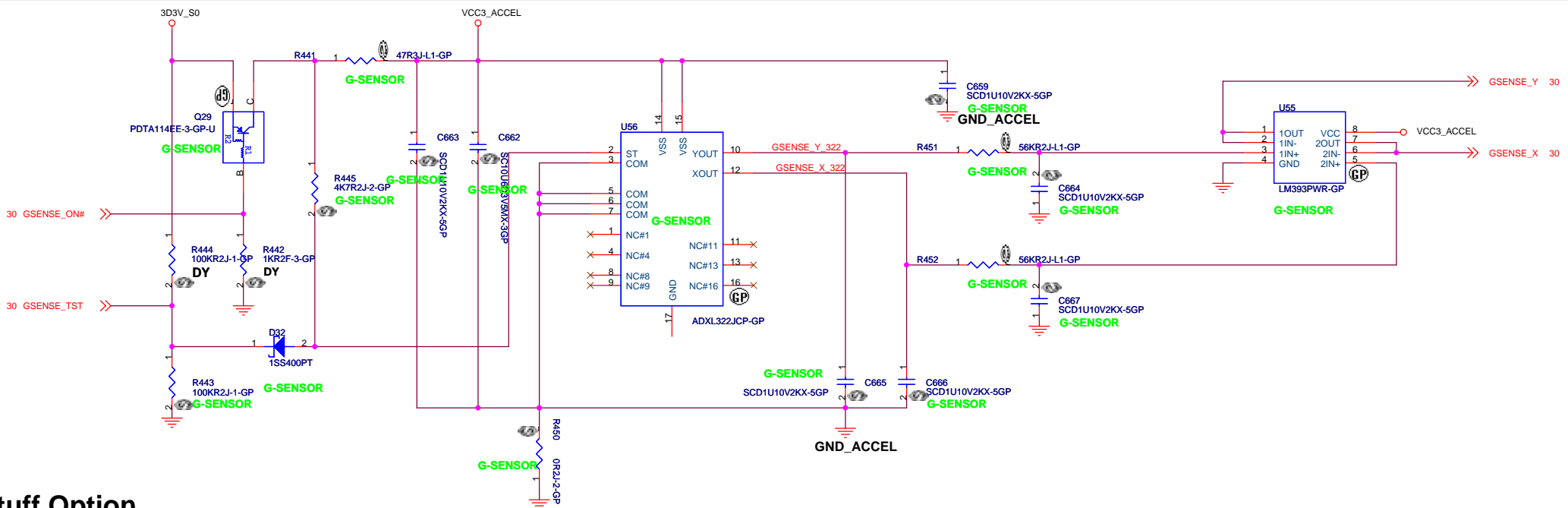
AUDIO (1/2) -- CODEC CX20549		
Title	Document Number	Rev
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Audio AMP and Jack
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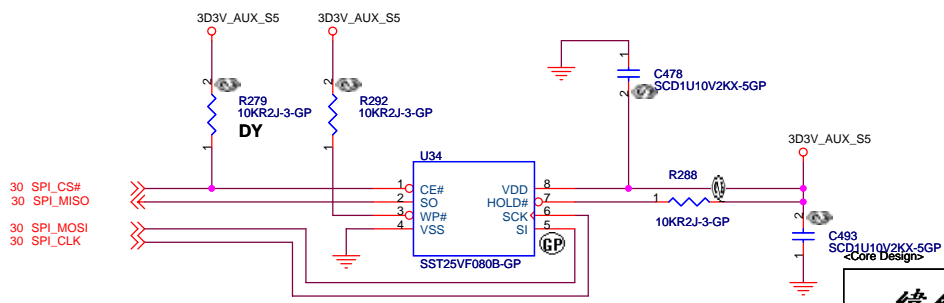
Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM



SPI ROM for System & KBC

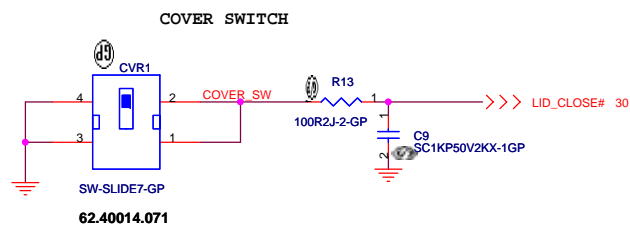
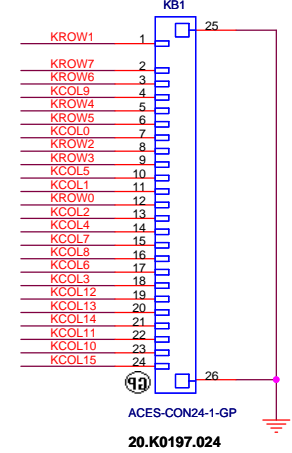
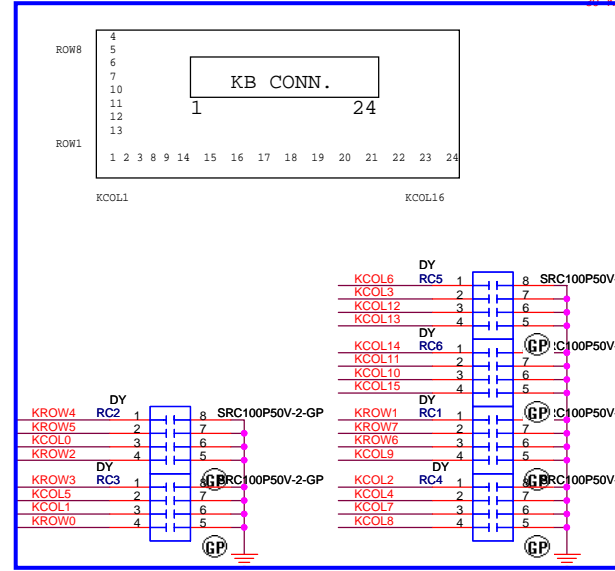
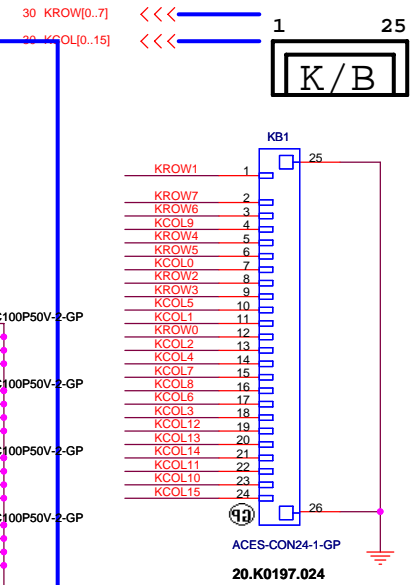


1. SST 25VF016B
2. Macronix MX25L1605A
3. SST 8Mbit 72.25080.G01

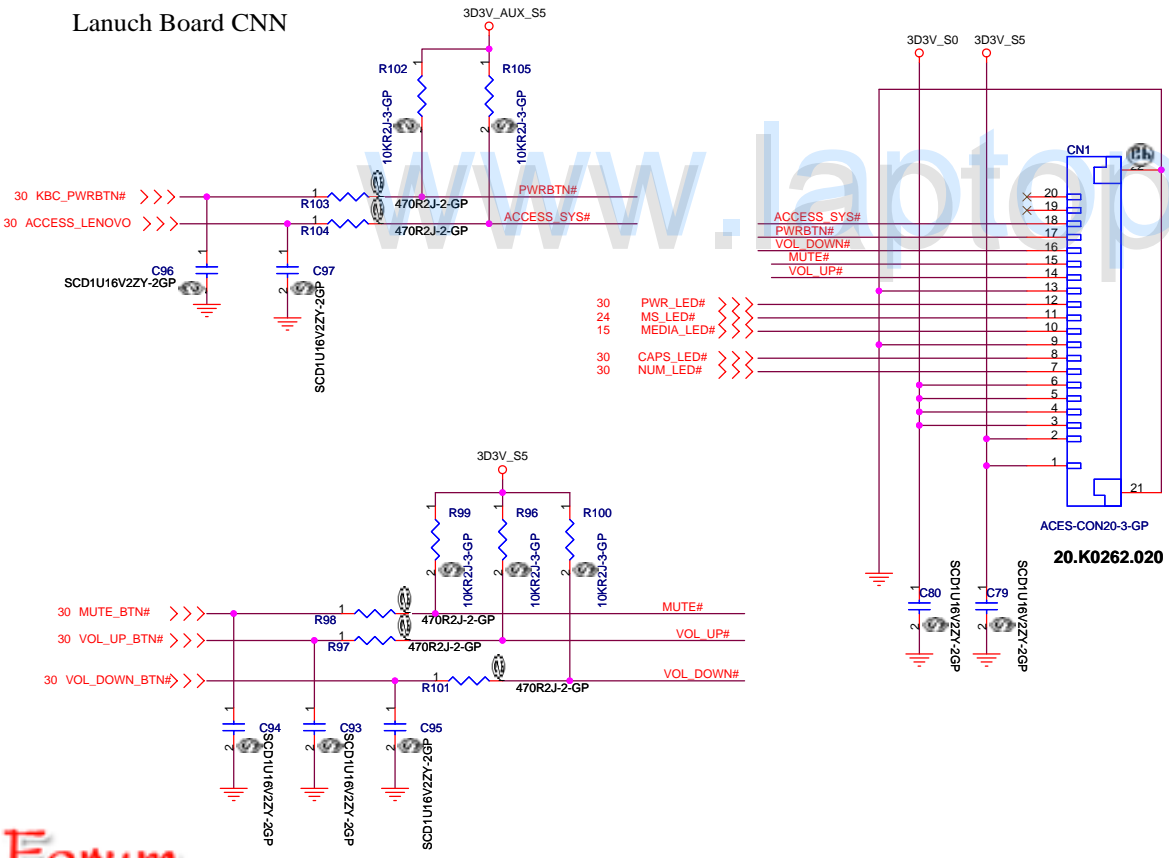
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Title: BIOS ROM/G-Sensor		
Size: A3	Document Number: A-NOTE2.0-AMD	Rev: SA
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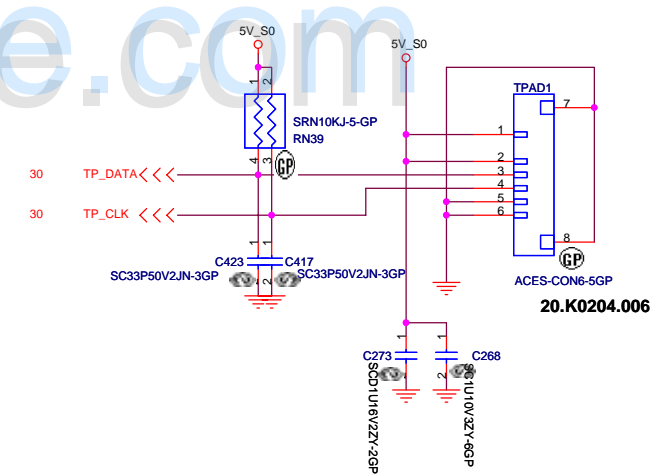
Internal KeyBoard Connector



Lanuch Board CNN



TOUCH PAD



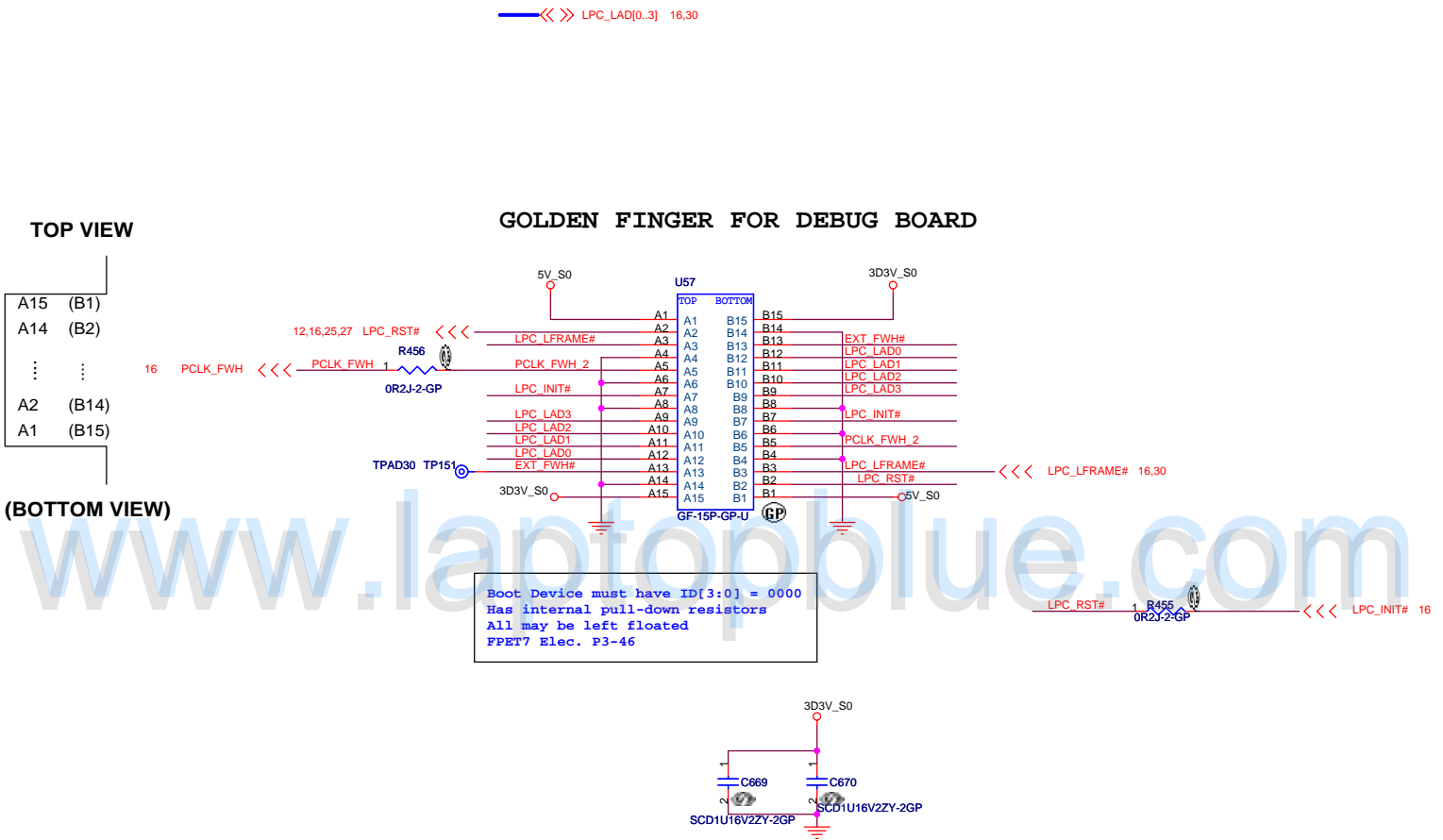
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Title: **LAUNCH / TOUCHPAD / KB CONN**

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TOP VIEW

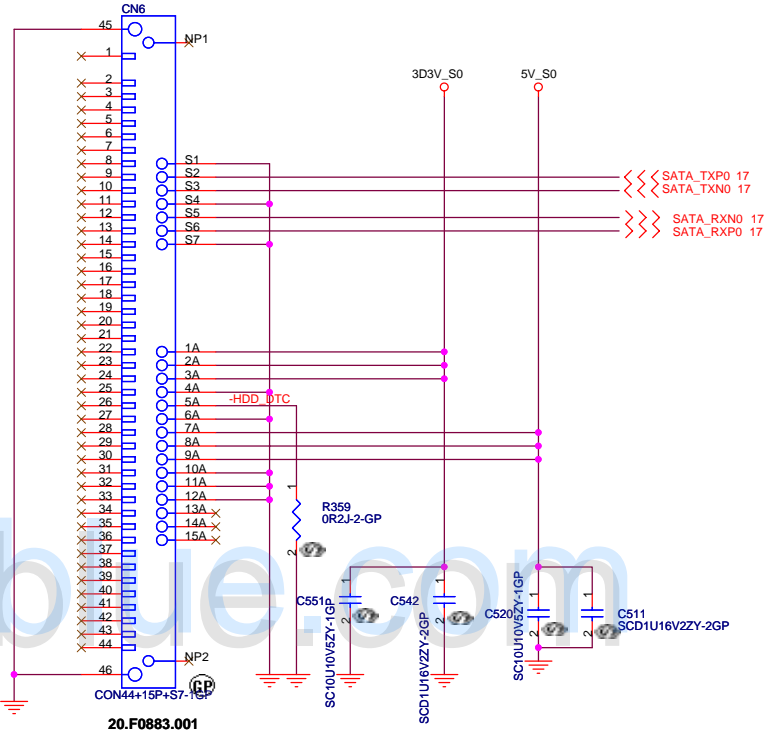
A15 (B1)
 A14 (B2)
 ⋮ ⋮
 A2 (B14)
 A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46

SATA HD Connector

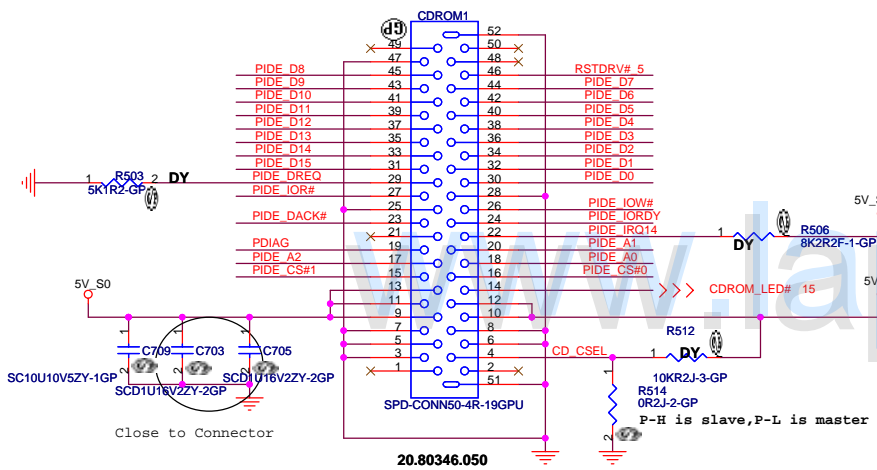


17 PIDE_D[15..0] <<>>

- 17 PIDE_A0 <>>>
- 17 PIDE_A1 <>>>
- 17 PIDE_A2 <>>>
- 17 PIDE_CS#0 <>>>
- 17 PIDE_CS#1 <>>>

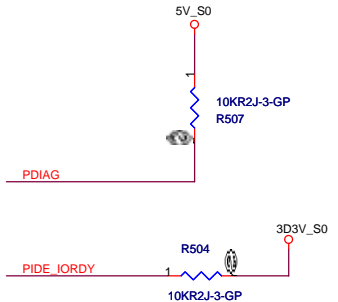
- <<<< RSTDRV#_5 16
- <<<< PIDE_IRQ14 17
- <<<< PIDE_IORDY 17
- <<<< PIDE_IOR# 17
- <<<< PIDE_IOW# 17
- <<<< PIDE_DREQ 17
- <<<< PIDE_DACK# 17

ODD Connector



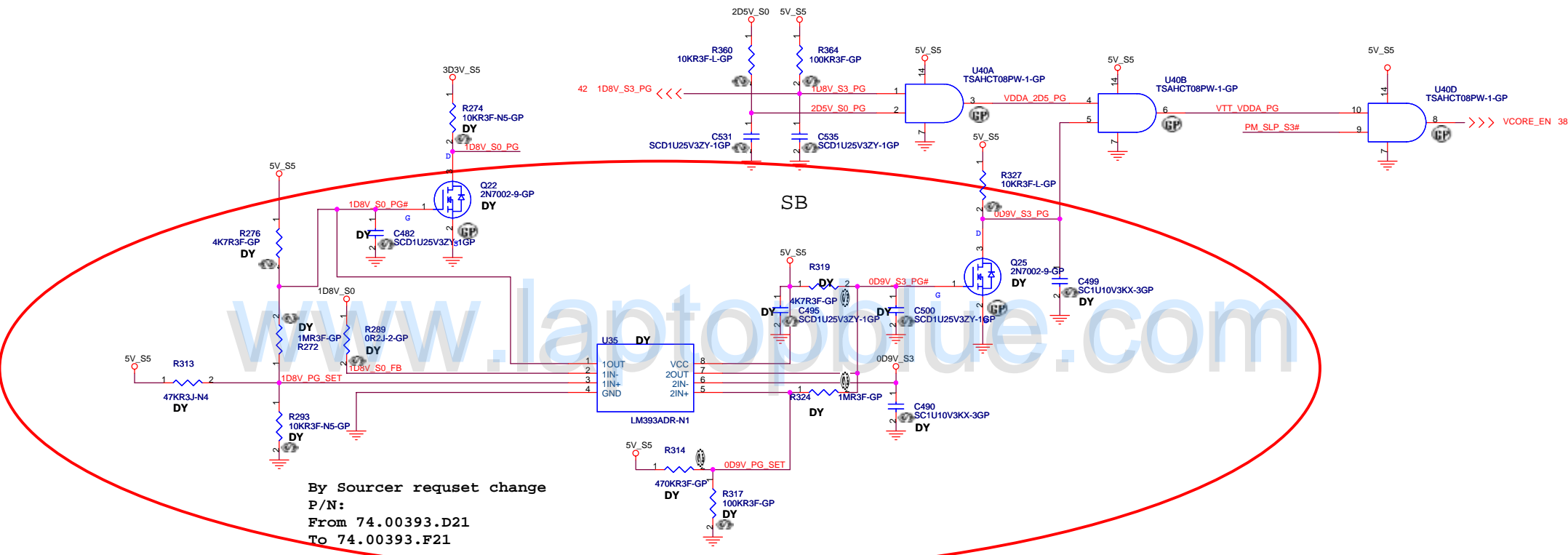
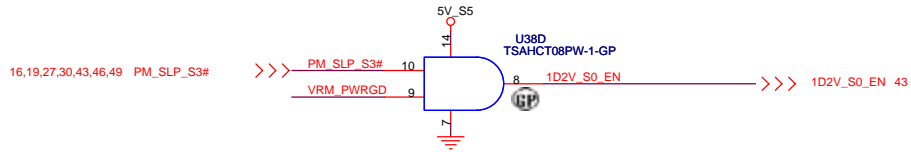
Close to Connector

20.80346.050

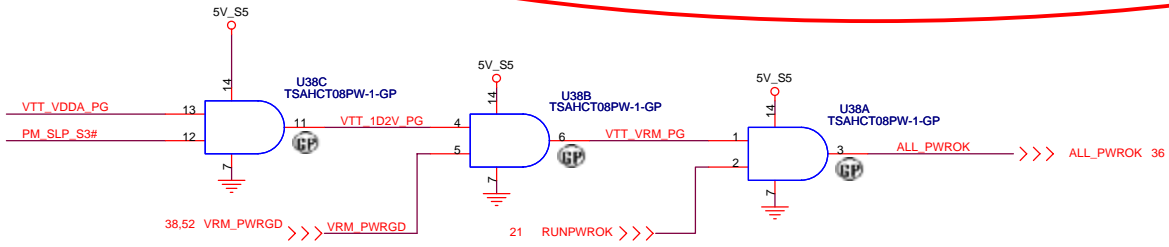


<Core Design>

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Title HDD/CDROM CONN			
Size A3	Document Number	Rev SA	
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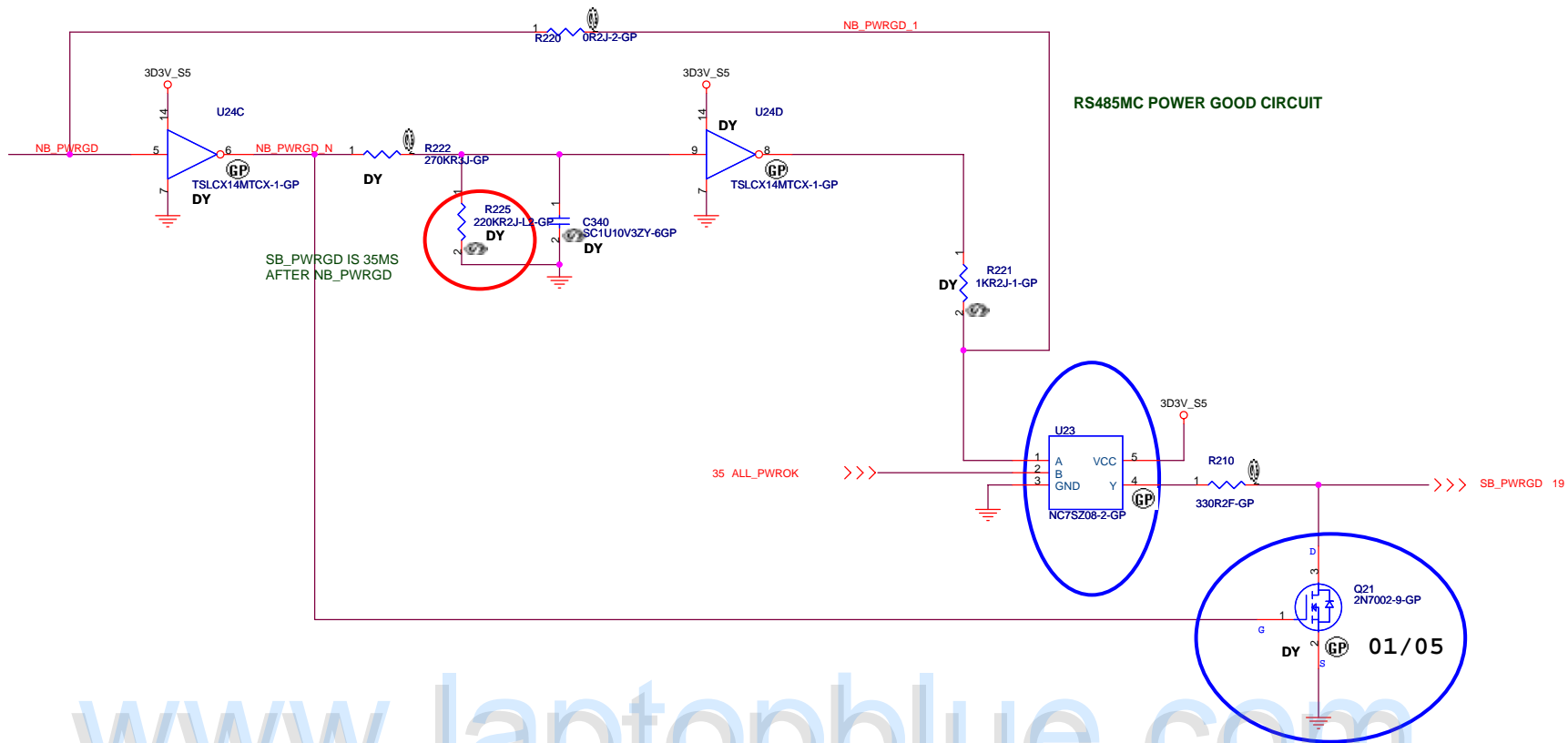


By Sourcer request change
 P/N:
 From 74.00393.D21
 To 74.00393.F21

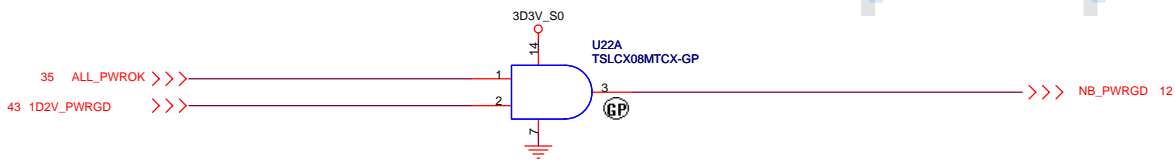


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
POWERGOOD&ENABLES(1/2)		
Title		
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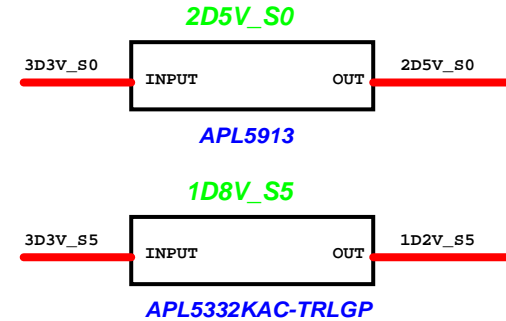
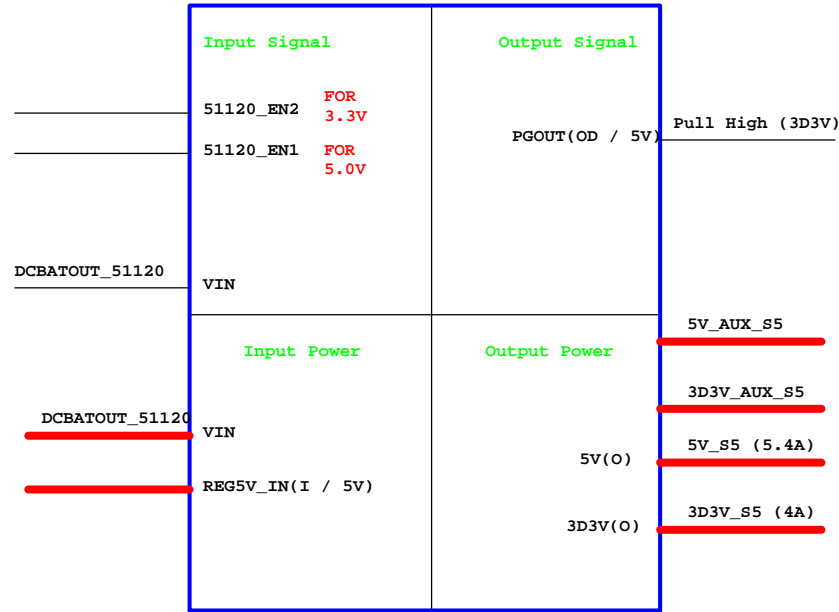
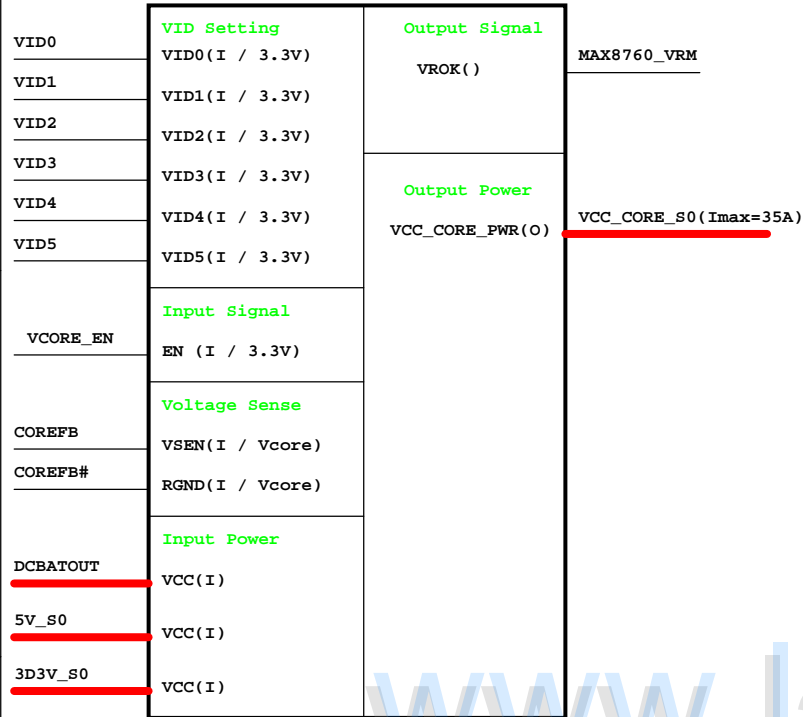


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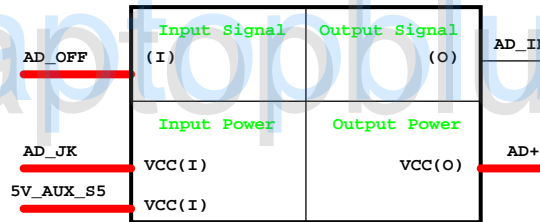
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: POWERGOOD&ENABLES(1/2)			
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TI TPS51120
3D3V/5V

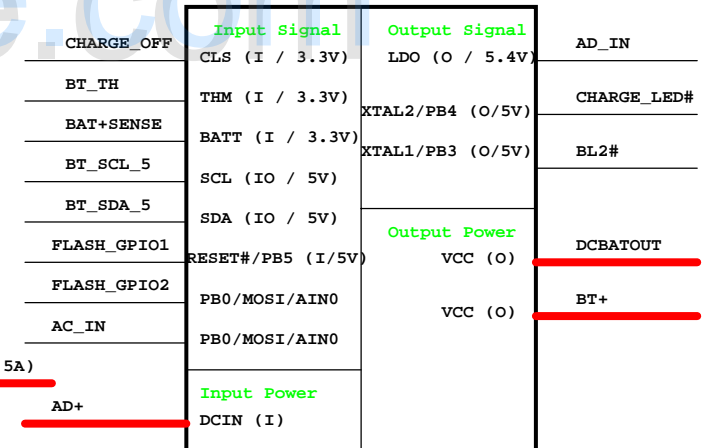
CPU_CORE
ISL6264CRZ



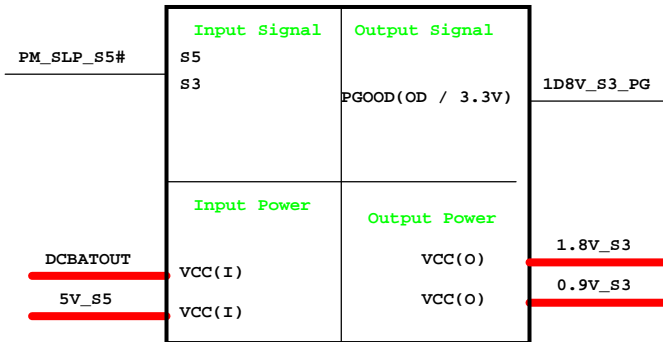
Adapter



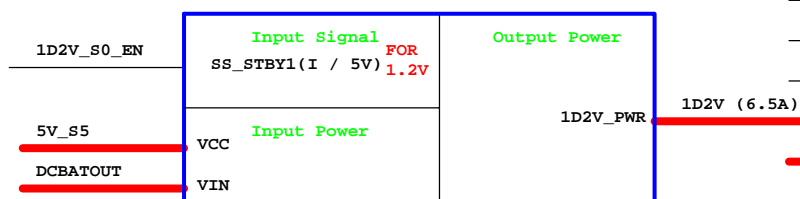
Charger_ISL6255



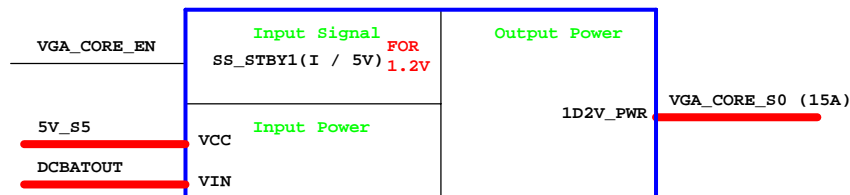
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



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Title: Power Block Diagram

Size A3 Document Number A-NOTE2.0-AMD Rev SA

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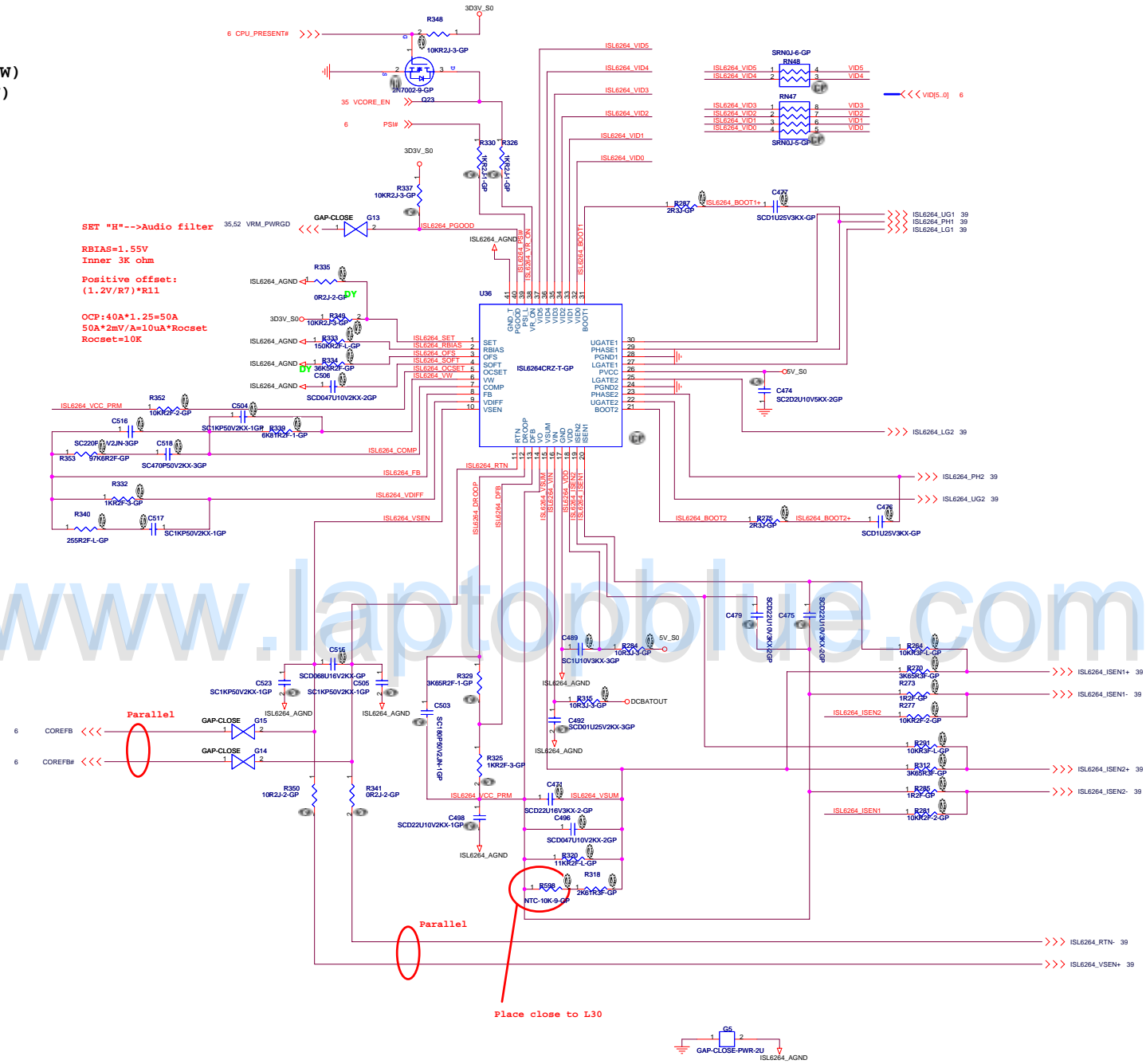
CPU_VCORE

VID=1.20V(25W)/1.15V(35W)
 Iomax=21A(25W)/35A (35W)
 OCP=40A~45A

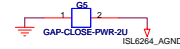
TABLE 1. VOLTAGE IDENTIFICATION CODES

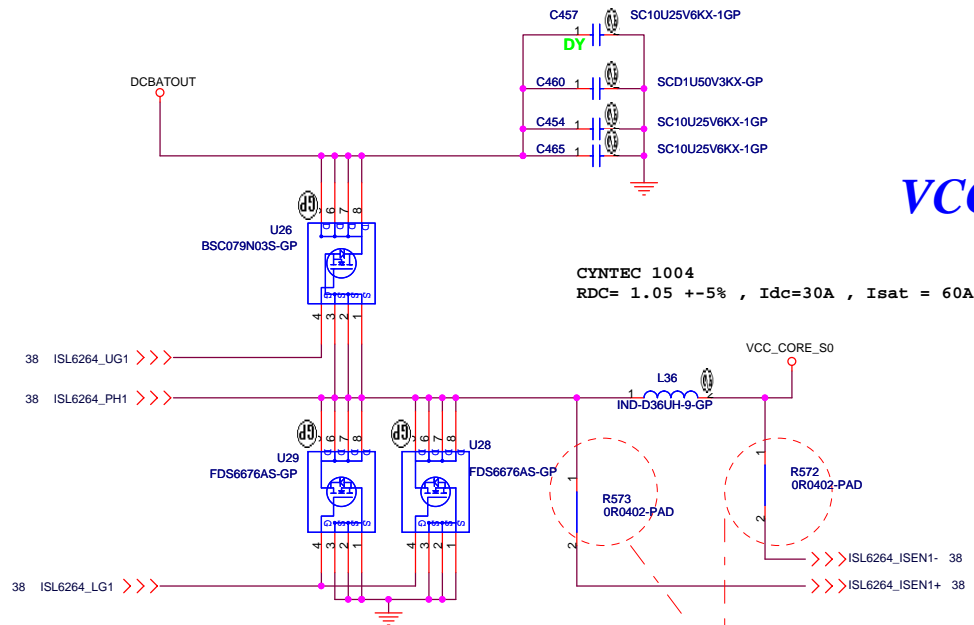
VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.750
1	0	0	0	0	1	0.725
1	0	0	0	1	0	0.700
1	0	0	0	1	1	0.675
1	0	0	1	0	0	0.650
1	0	0	1	0	1	0.625
1	0	0	1	1	0	0.600
1	0	0	1	1	1	0.575
1	0	1	0	0	0	0.550
1	0	1	0	0	1	0.525
1	0	1	0	1	0	0.500
1	0	1	0	1	1	0.475
1	0	1	1	0	0	0.450
1	0	1	1	0	1	0.425
1	0	1	1	1	0	0.400
1	0	1	1	1	1	0.375

SET "H"-->Audio filter
 RBIAS=1.55V
 Inner 3K ohm
 Positive offset:
 (1.2V/R7)*R11
 OCP:40A*1.25=50A
 50A*2mV/A=10uA*Rocset
 Rocset=10K



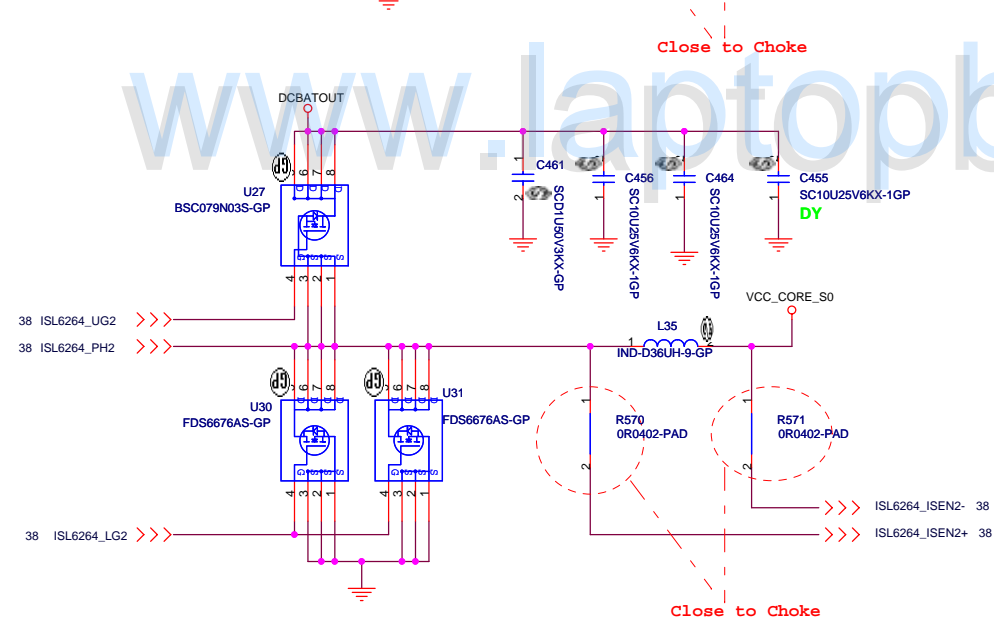
Place close to L30



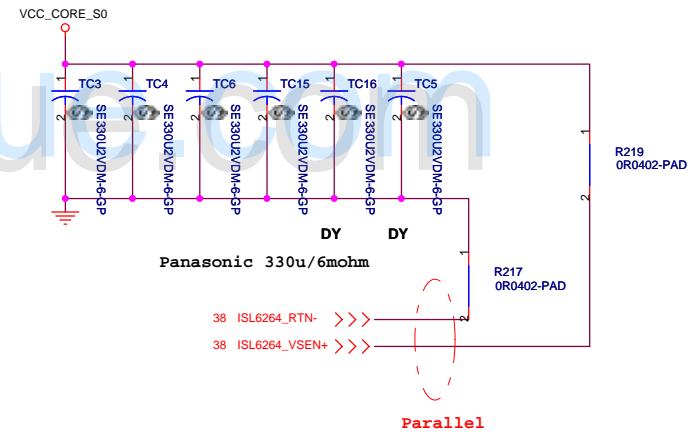


VCC_CORE_S0

CYNTEC 1004
RDC= 1.05 +-5% , Idc=30A , Isat = 60A



CYNTEC 1004
RDC= 1.05 +-5% , Idc=30A , Isat = 60A



38 ISL6264_RTIN- >>>
38 ISL6264_VSEN+ >>>

Parallel

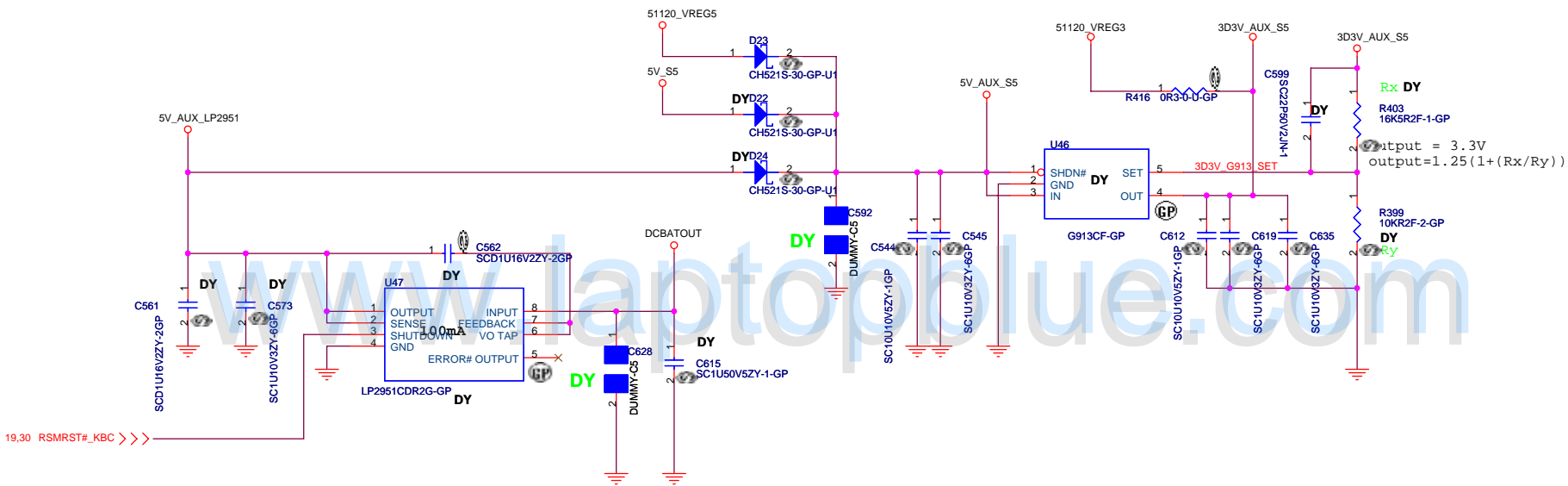
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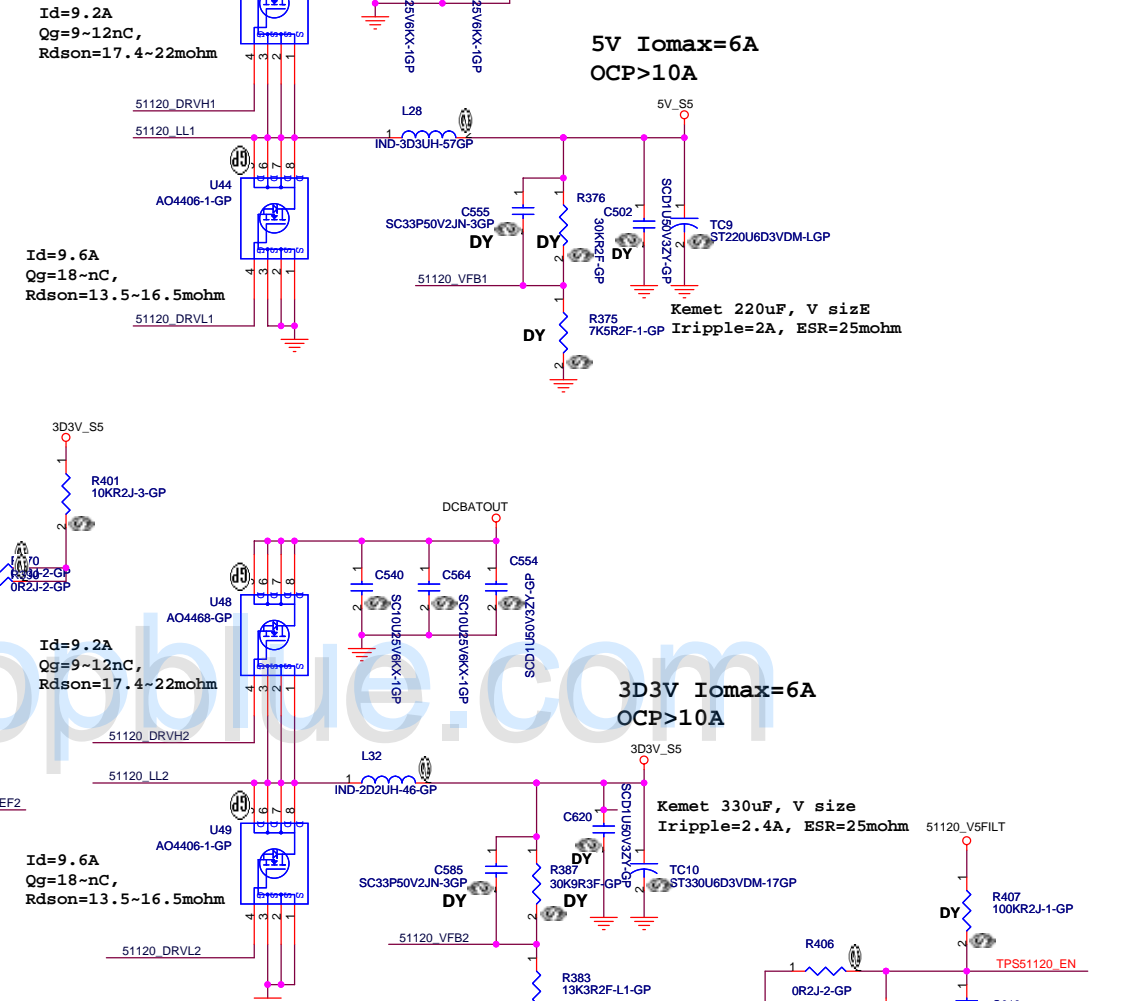
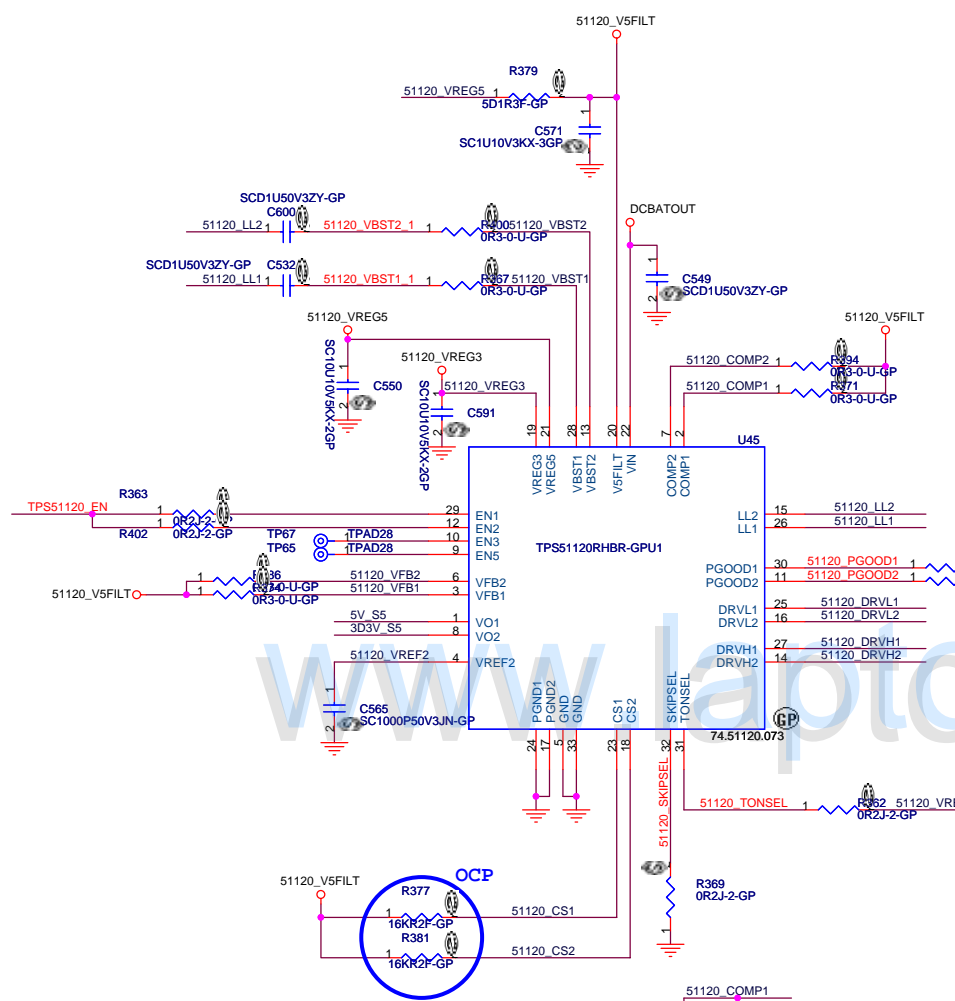
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Title			CPU Vcore Power_2		
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Aux Power

3D3V_AUX_S5





Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120, $V_{out} = 5V$

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

$V_{out} = 3.3V$

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

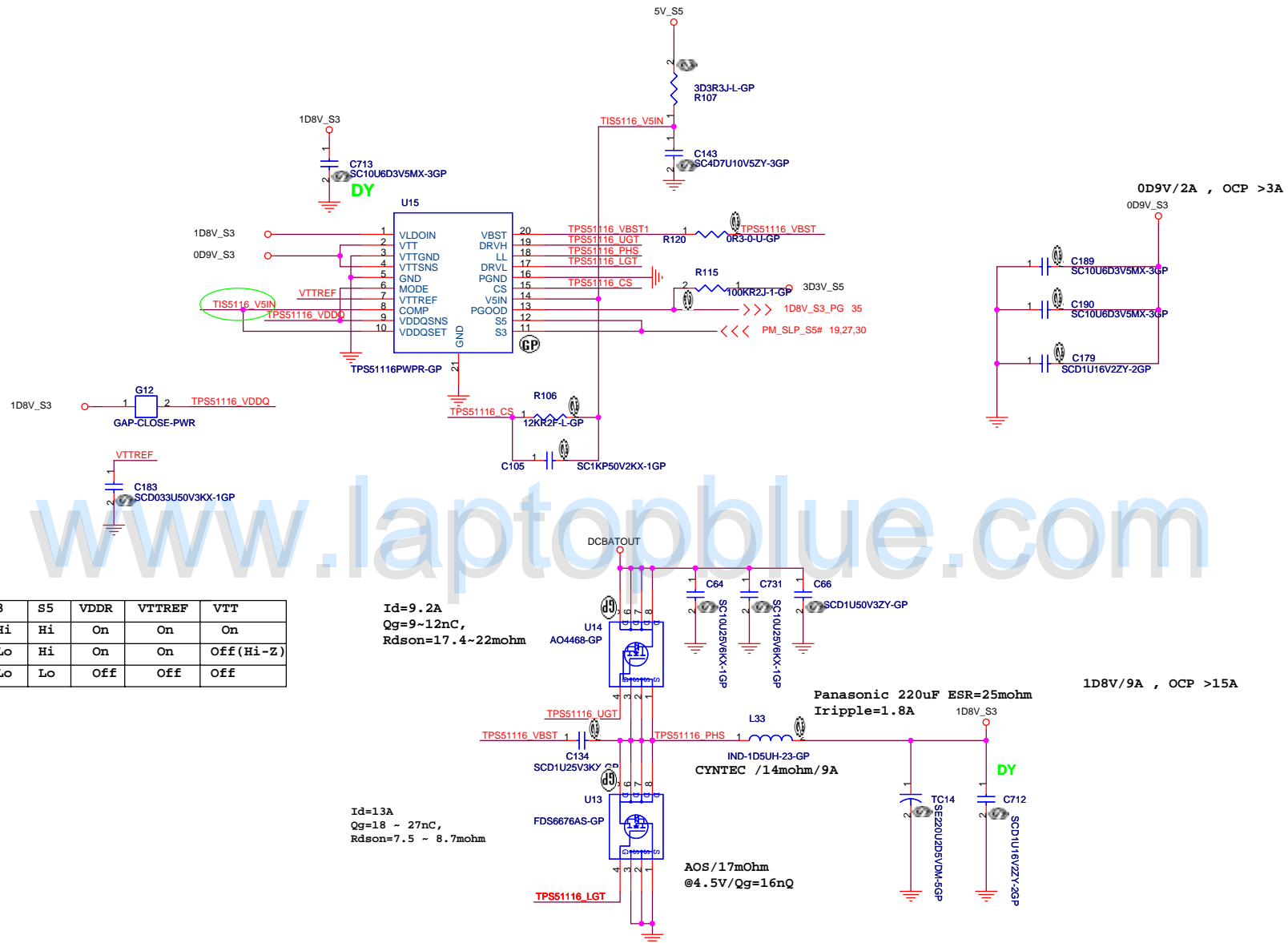
緯創資通 Wistron Corporation
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Title: **TI TPS51120 3D3V/5V**

Size: A3 Document Number: **A-NOTE2.0-AMD** Rev: **SA**

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TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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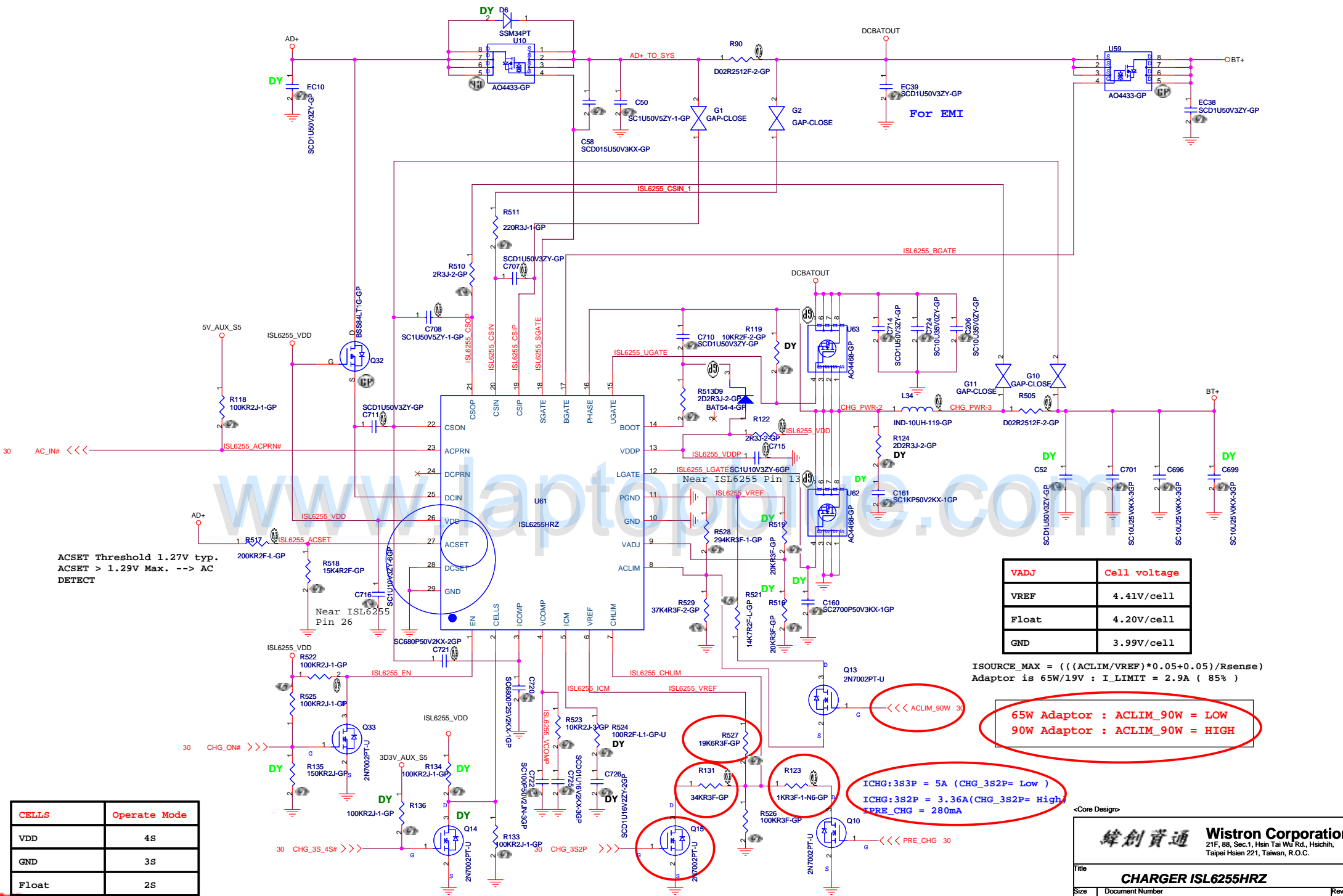
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Title: **TI TPS51116 1D8V / 0D9V**

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ACSET Threshold 1.27V typ.
 ACSET > 1.29V Max. --> AC
 DETECT

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
 Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

65W Adaptor : ACLIM_90W = LOW
 90W Adaptor : ACLIM_90W = HIGH

ICHG:3S3P = 5A (CHG_3S2P= Low)
 ICHG:3S2P = 3.36A(CHG_3S2P= High)
 IPRE_CHG = 280ma

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

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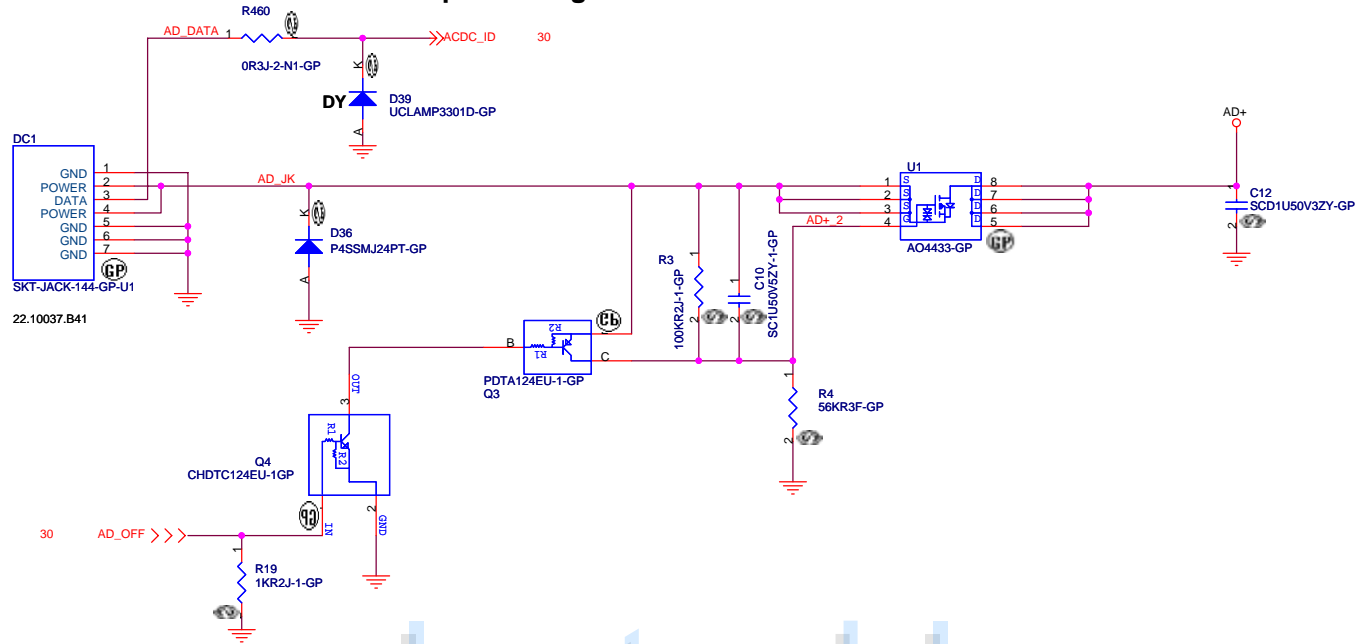
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER ISL6255HRZ**

Size: Document Number
 Custom: **A-NOTE2.0-AMD** Rev: SA

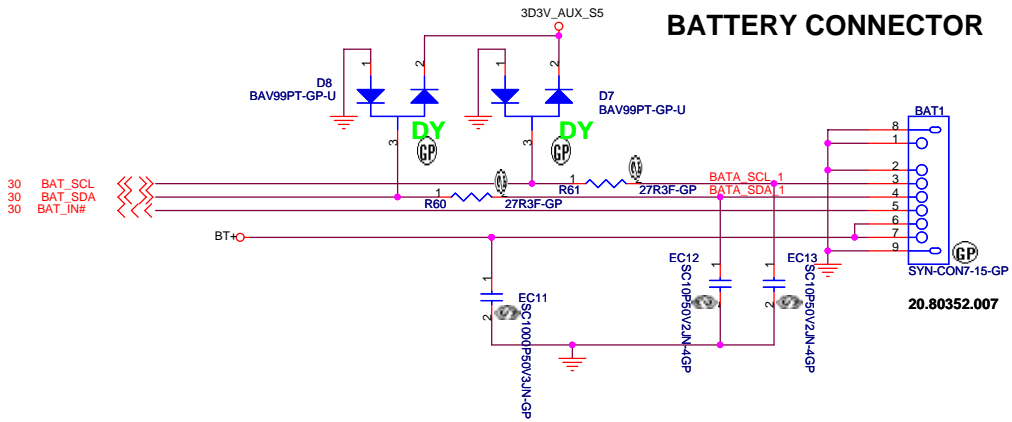
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Adaptor in to generate DCBATOUT

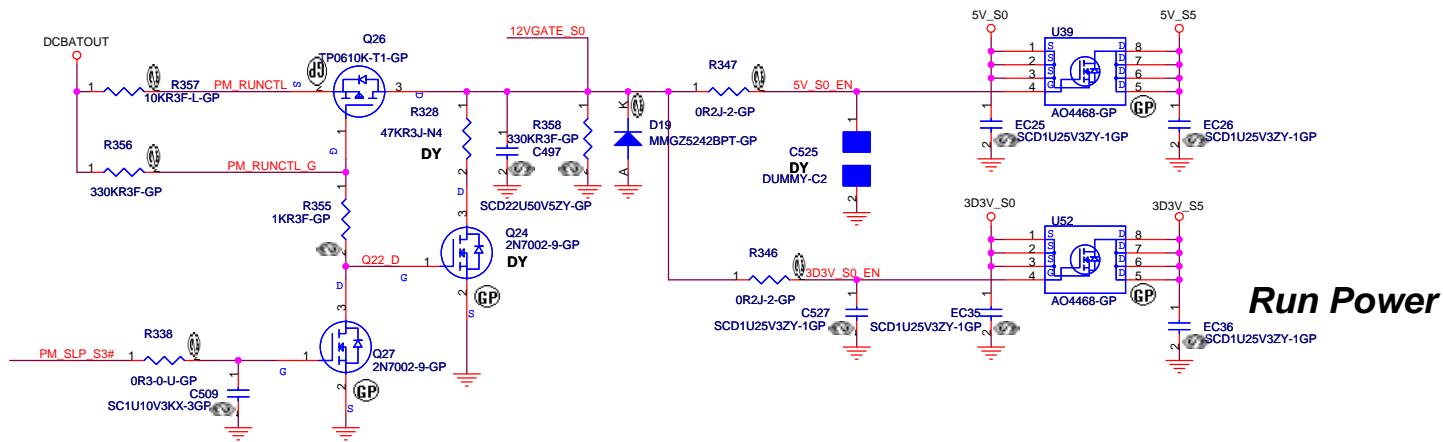


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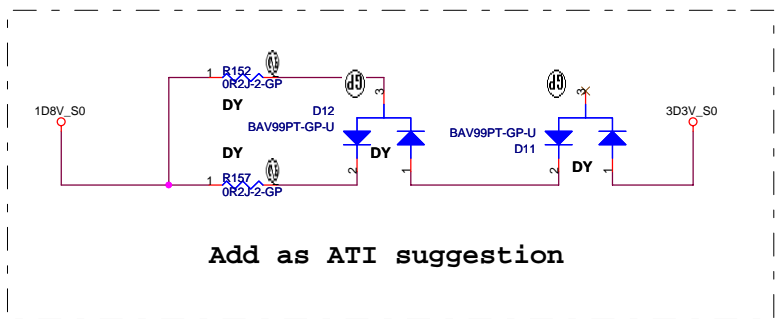
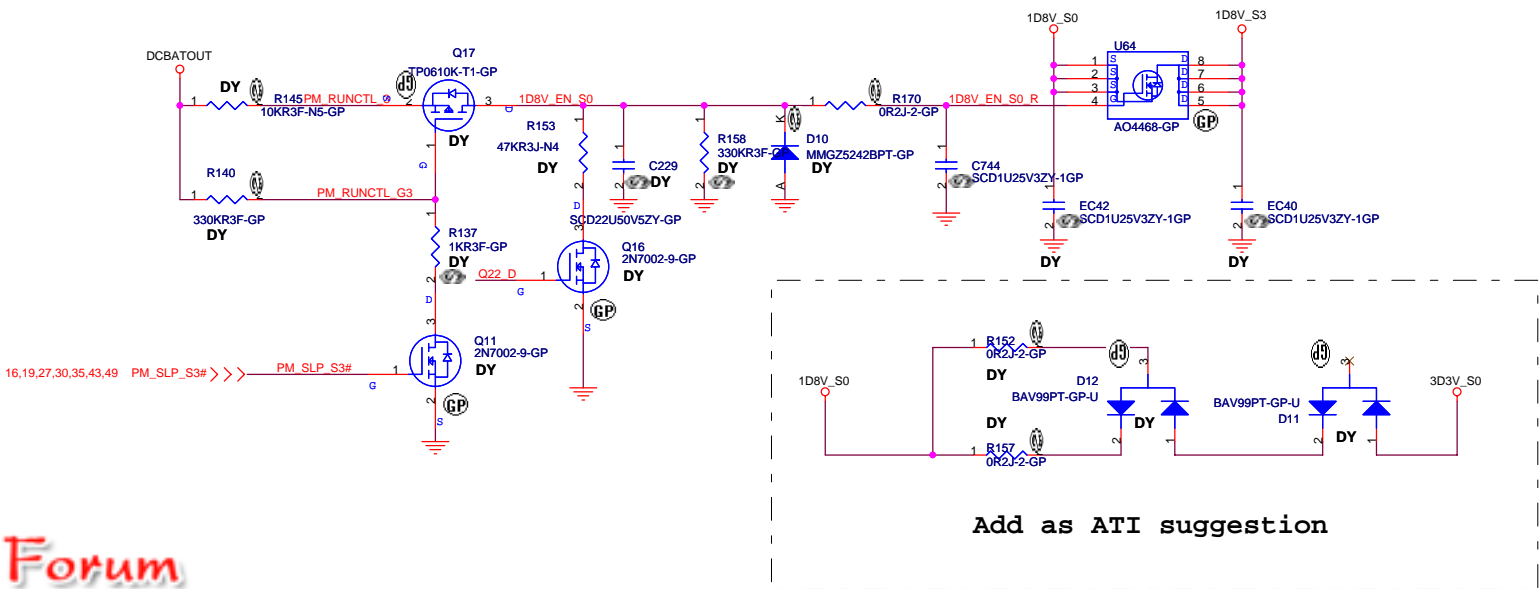
BATTERY CONNECTOR



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Title		
AD/BAT CONN		
Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA
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Add as ATI suggestion

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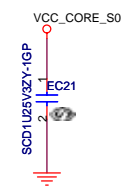
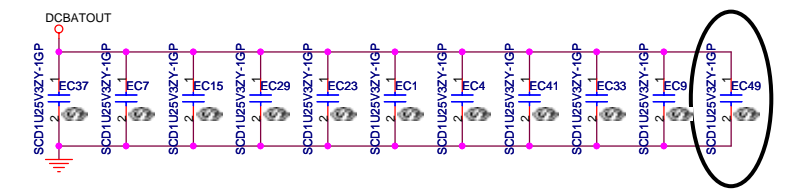
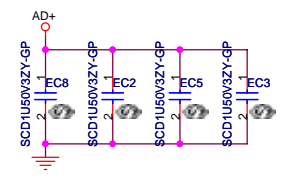
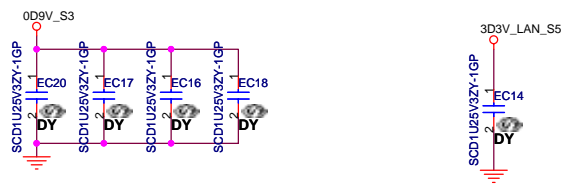
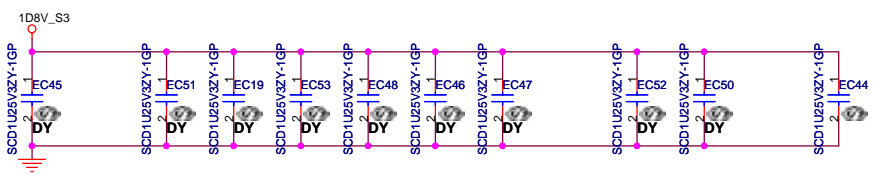
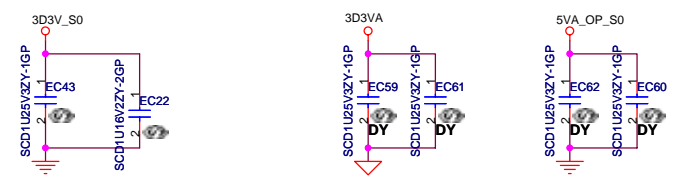
Power On Logic

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWR CTL LOGIC / PWR PLANE**

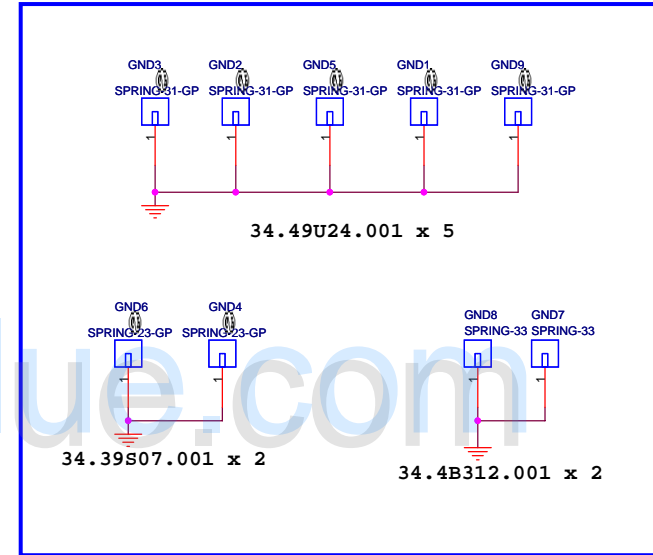
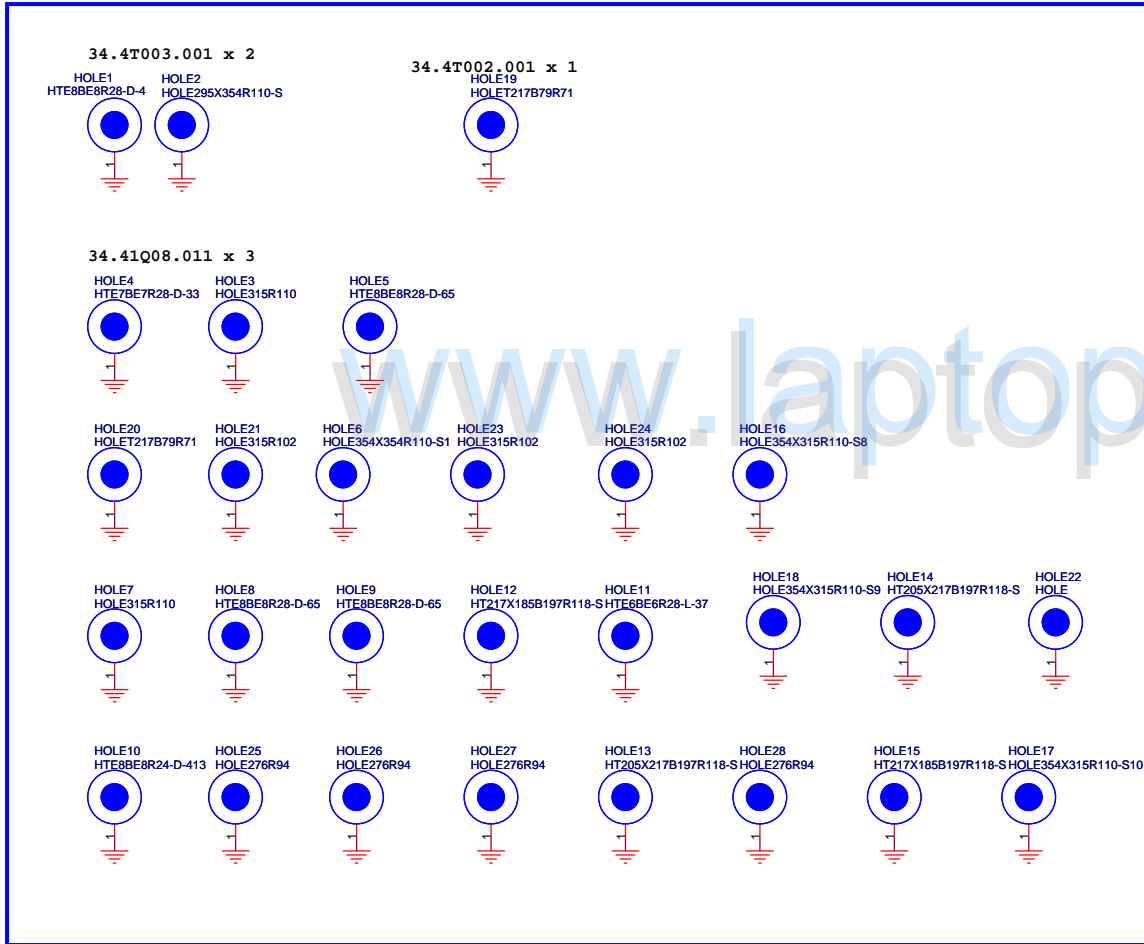
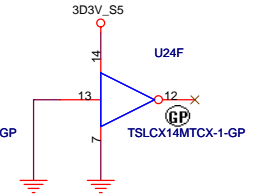
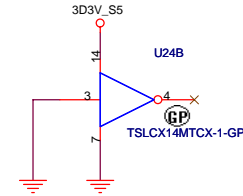
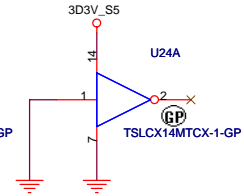
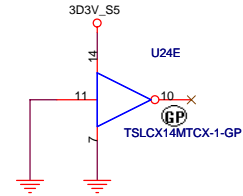
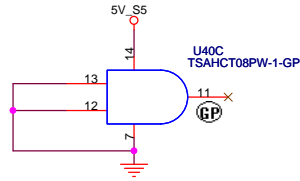
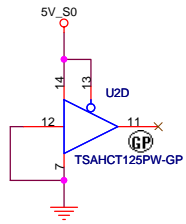
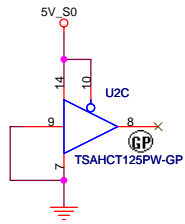
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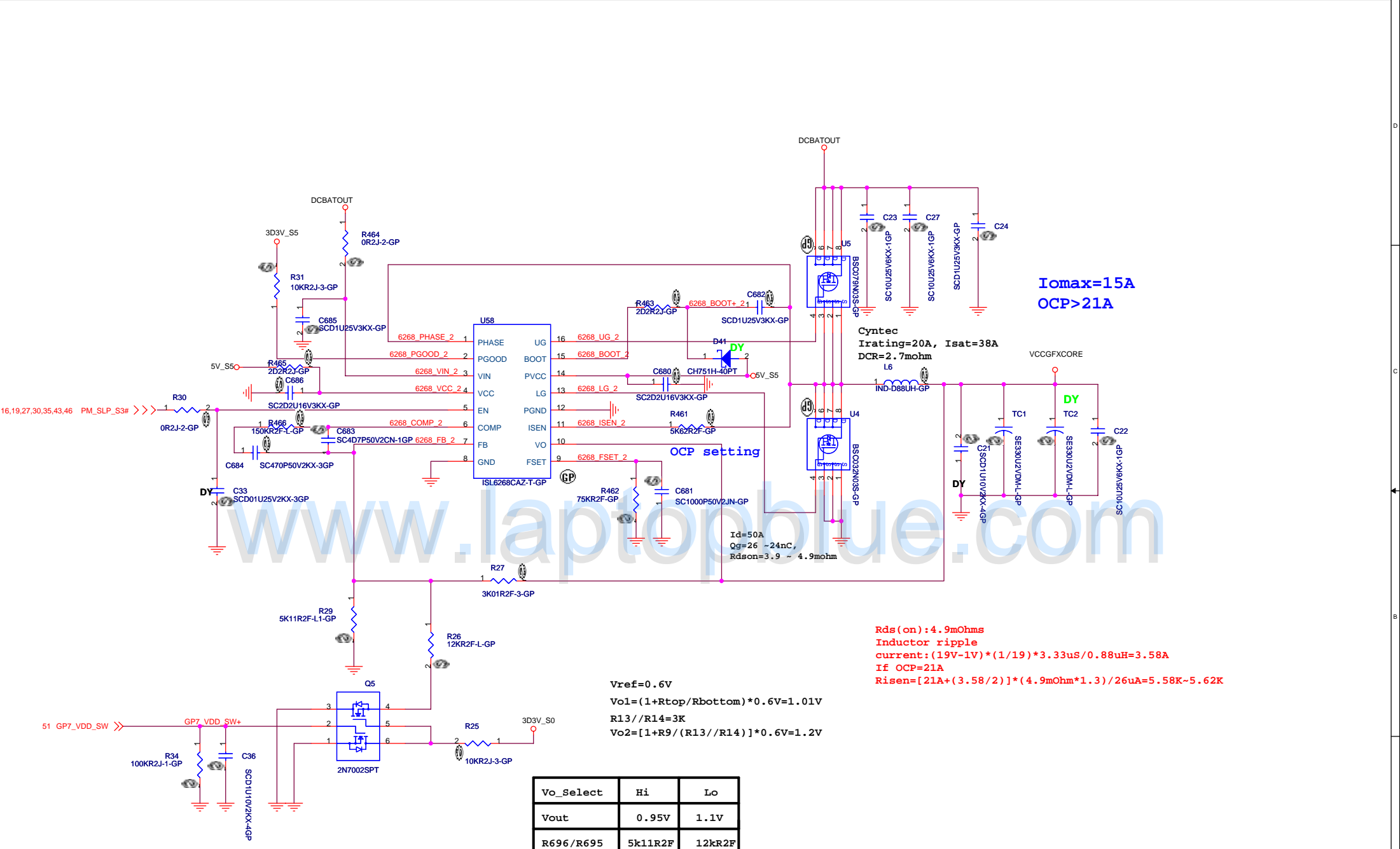
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<p>Title EMI COMPONENTS</p>	
Size A3	<p>Document Number A-NOTE2.0-AMD</p>
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Title MISC		
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**Iomax=15A
OCP>21A**

Cyntec
Irating=20A, Isat=38A
DCR=2.7mohm
L6

OCP setting

Id=50A
Og=26 ~24nC,
Rdson=3.9 ~ 4.9mohm

Rds(on) : 4.9mOhms
Inductor ripple
current: $(19V-1V) * (1/19) * 3.33\mu s / 0.88\mu H = 3.58A$
If OCP=21A
Risen = $[21A + (3.58/2)] * (4.9mOhm * 1.3) / 26\mu A = 5.58K \sim 5.62K$

Vref=0.6V
Vo1 = $(1 + Rtop/Rbottom) * 0.6V = 1.01V$
R13//R14=3K
Vo2 = $[1 + R9 / (R13 // R14)] * 0.6V = 1.2V$

Vo_Select	Hi	Lo
Vout	0.95V	1.1V
R696/R695	5k11R2F	12kR2F

Vo_Select	Hi	Lo
Vout	0.95V	1.2V
R696/R695	5k11R2F	7k15R2F

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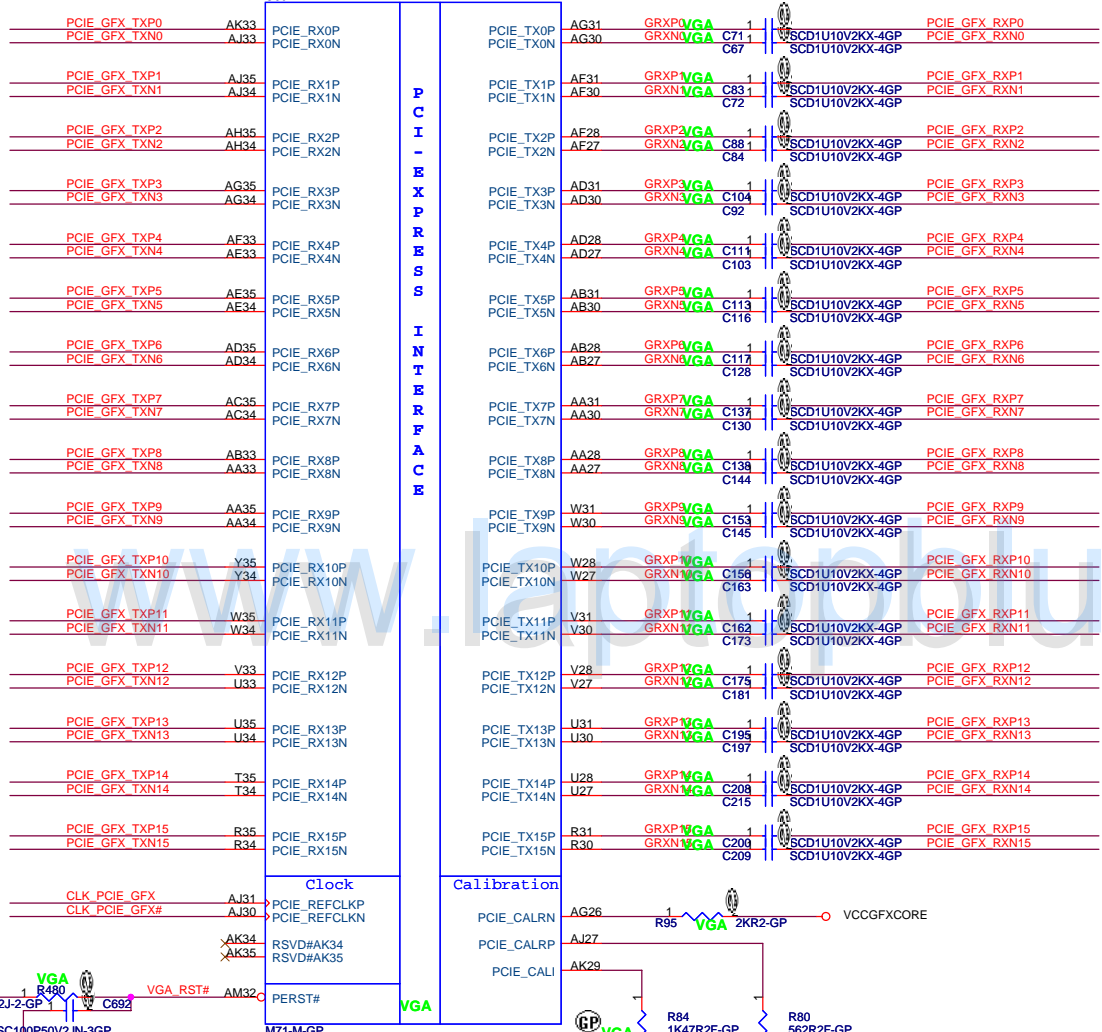
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Title: **VGA_CORE**

Size A3 Document Number: **A-NOTE2.0-AMD** Rev SA

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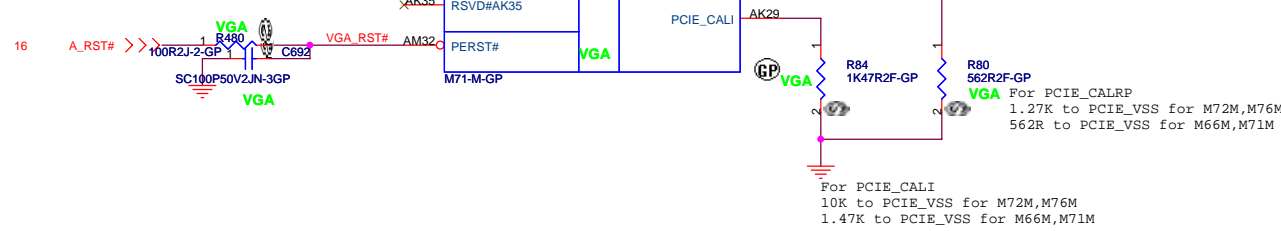
U60A 1 OF 7



CLK_PCIE_GFX
CLK_PCIE_GFX#

CLK_PCIE_GFX_3
CLK_PCIE_GFX#_3

PCIE_GFX_TXP[15..0] << PCIE_GFX_TXP[15..0] 11
PCIE_GFX_TXN[15..0] << PCIE_GFX_TXN[15..0] 11
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PCIE_GFX_RXN[15..0] >> PCIE_GFX_RXN[15..0] 11



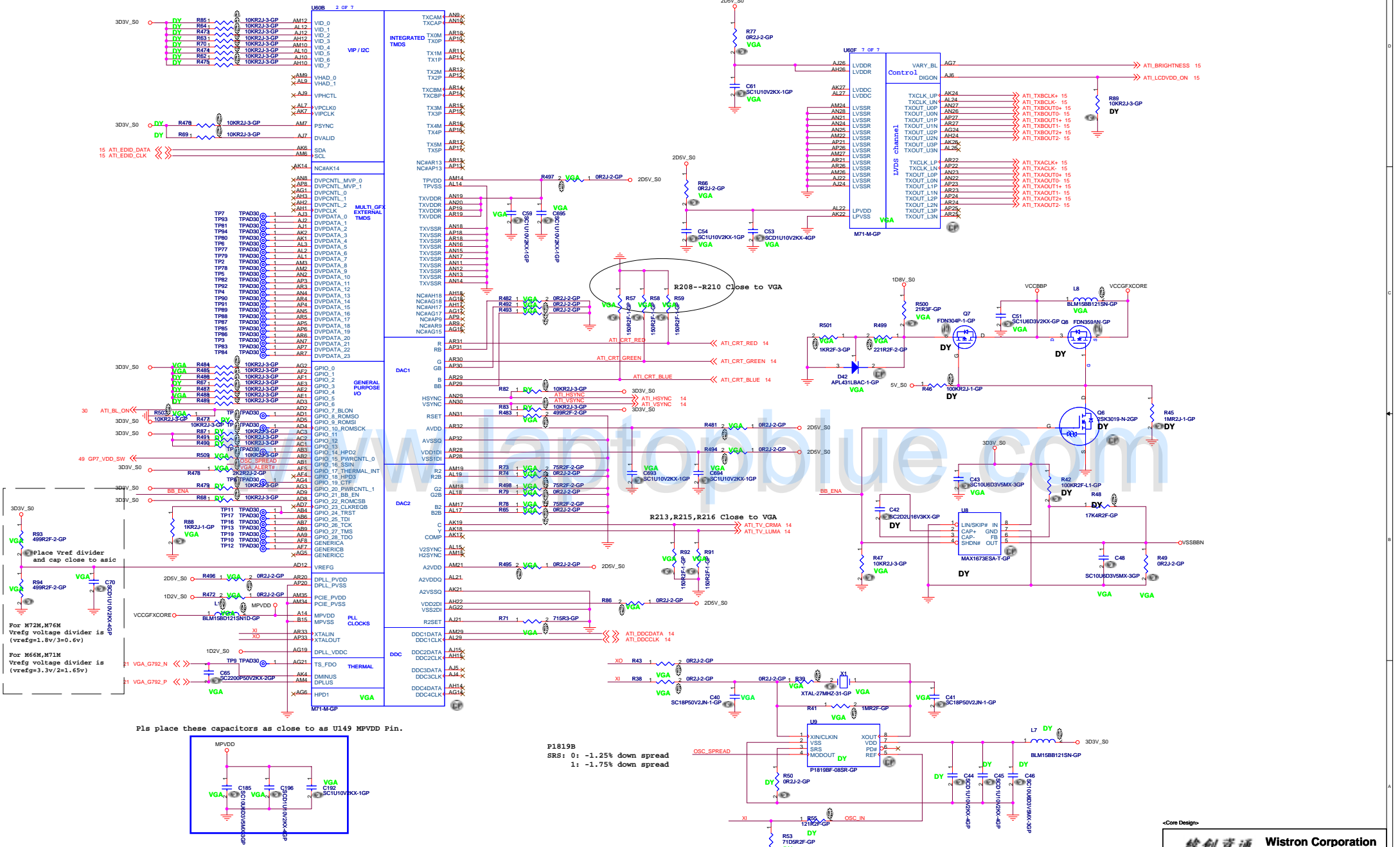
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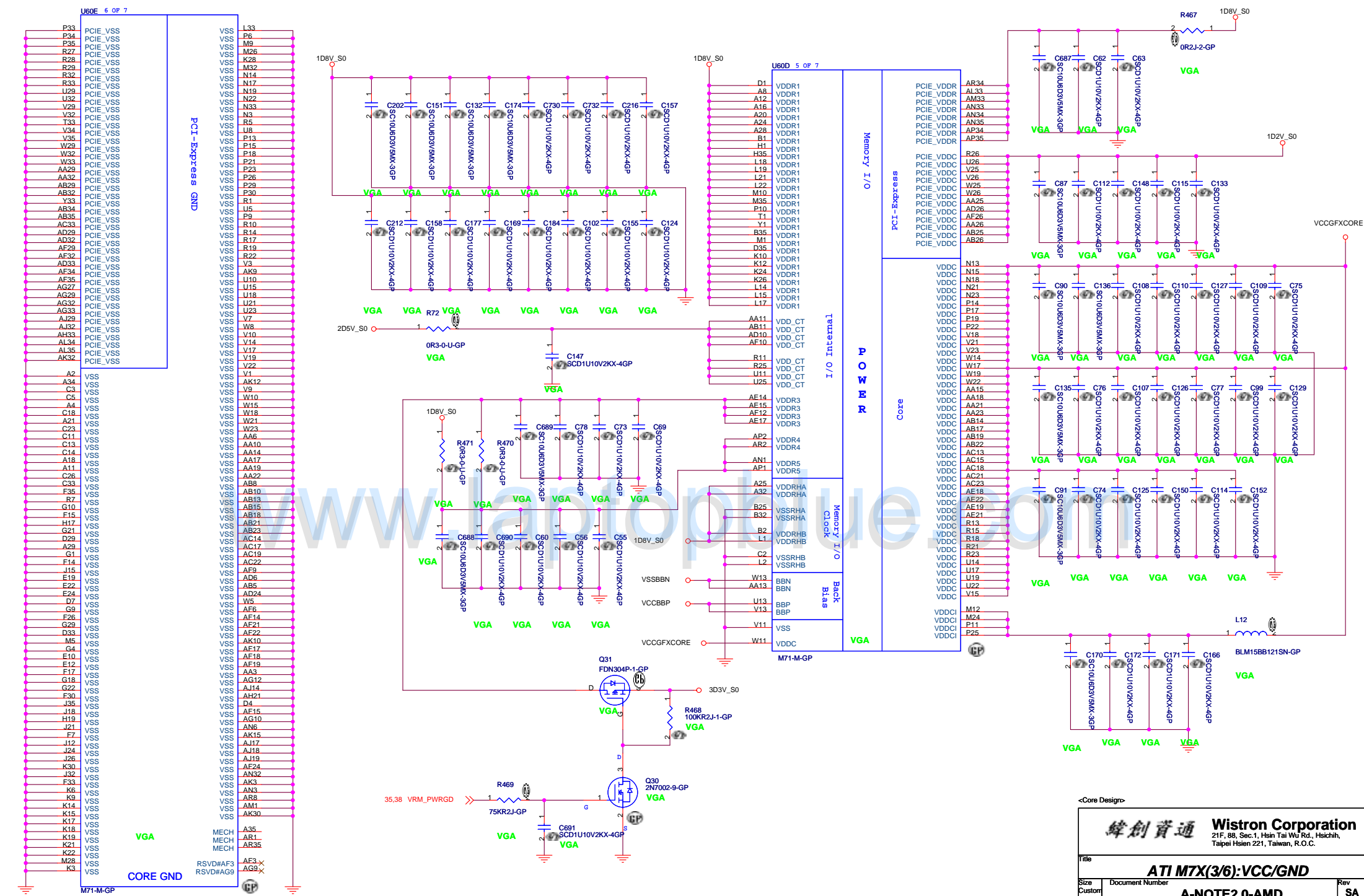
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Title: **ATI M7X(1/6):PCIE Interface**

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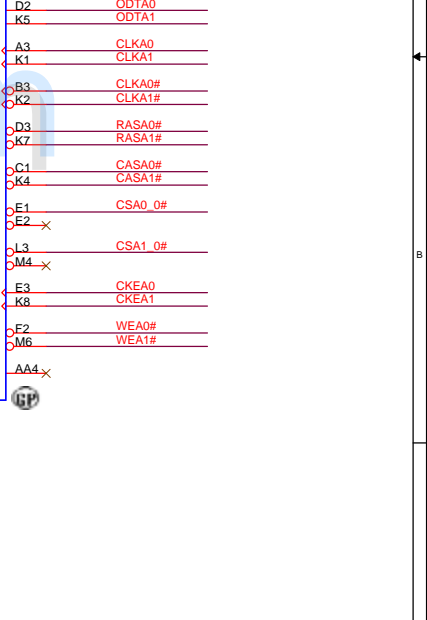
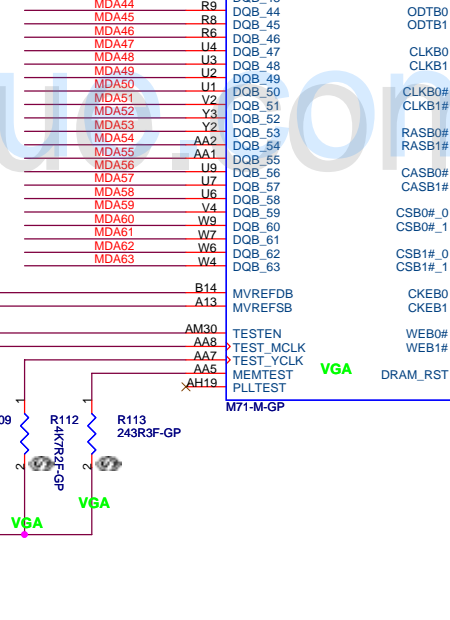
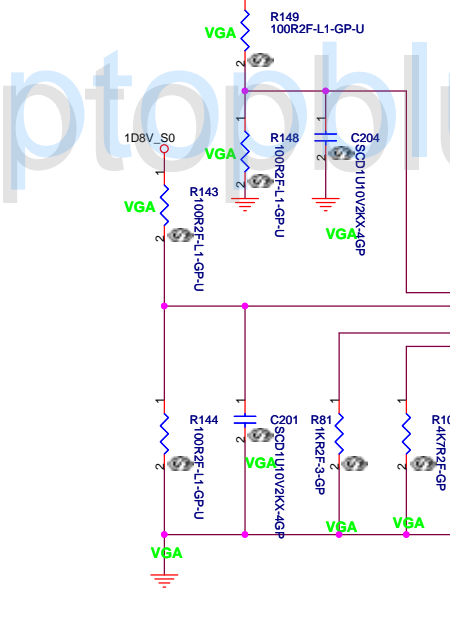
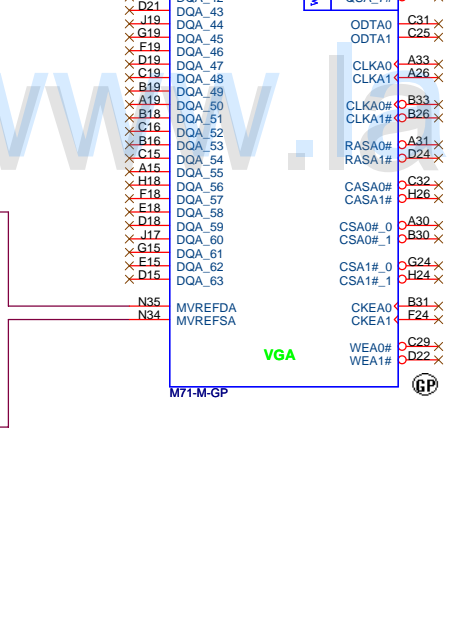
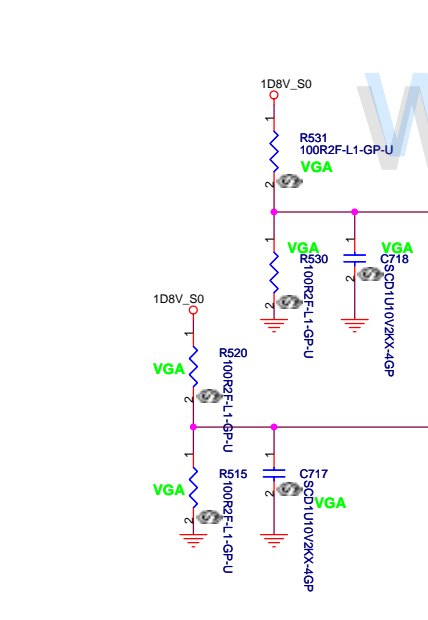
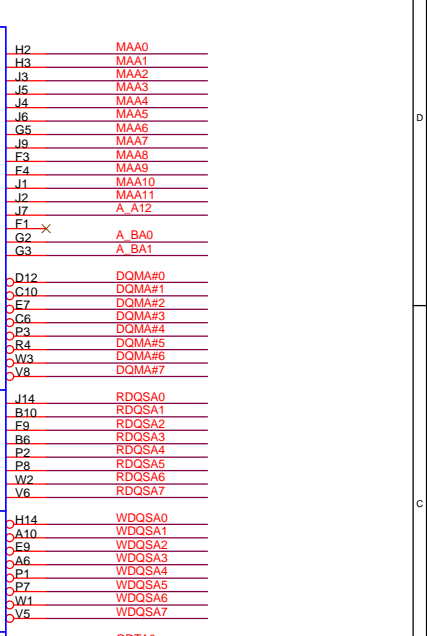
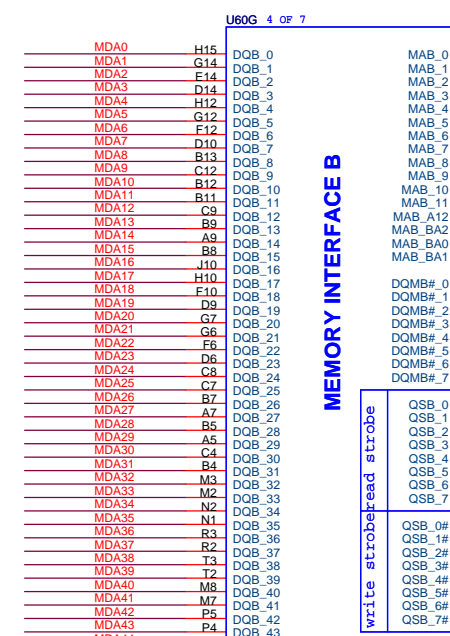
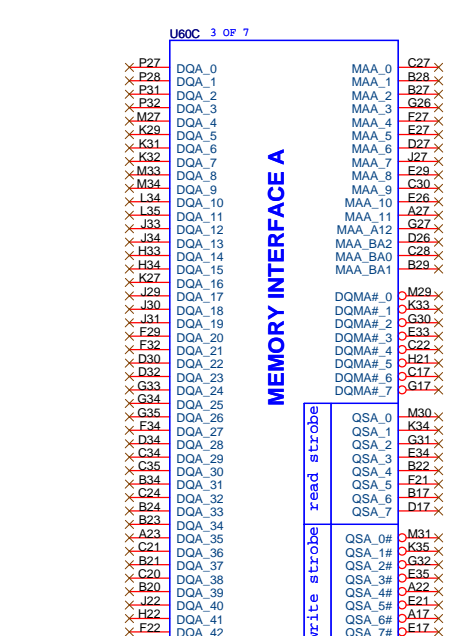
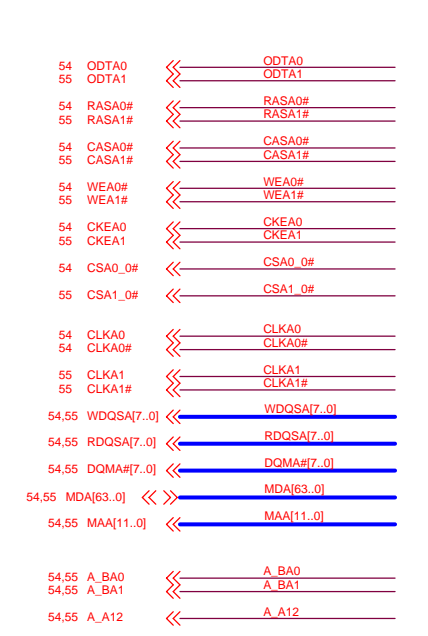


-Core Design-

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ATI M7X(3/6):VCC/GND

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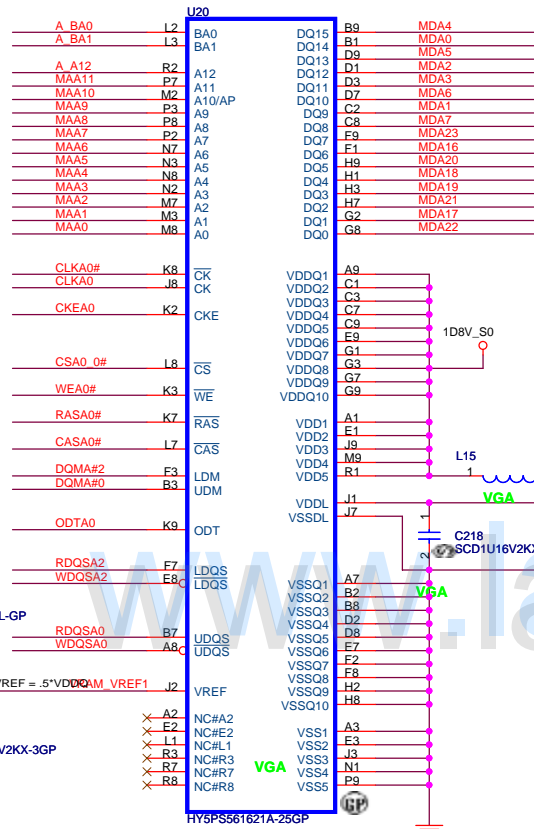
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M7X(4/6):Memory Interface**

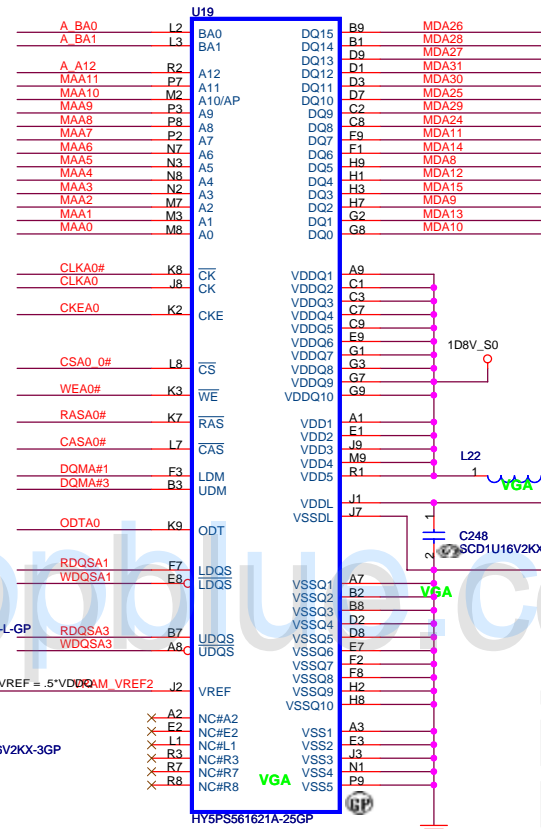
Size: A3 Document Number: **A-NOTE2.0-AMD** Rev: SA

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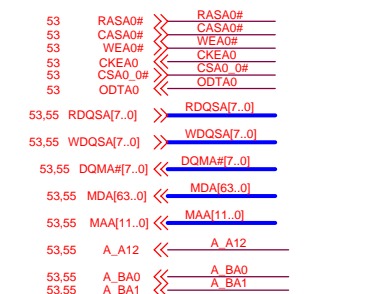
DDR2 BGA MEMORY



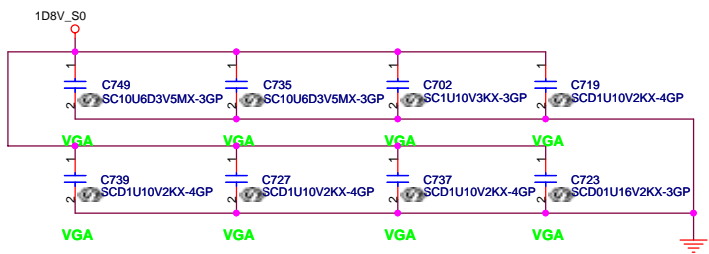
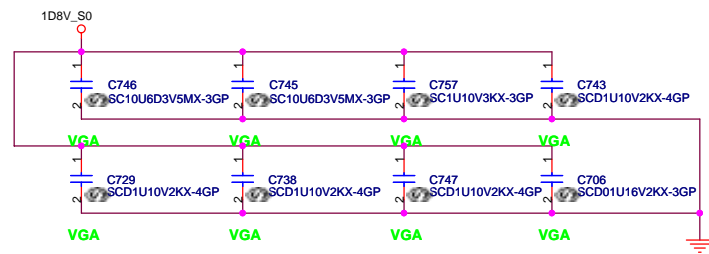
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72.55616.C0U



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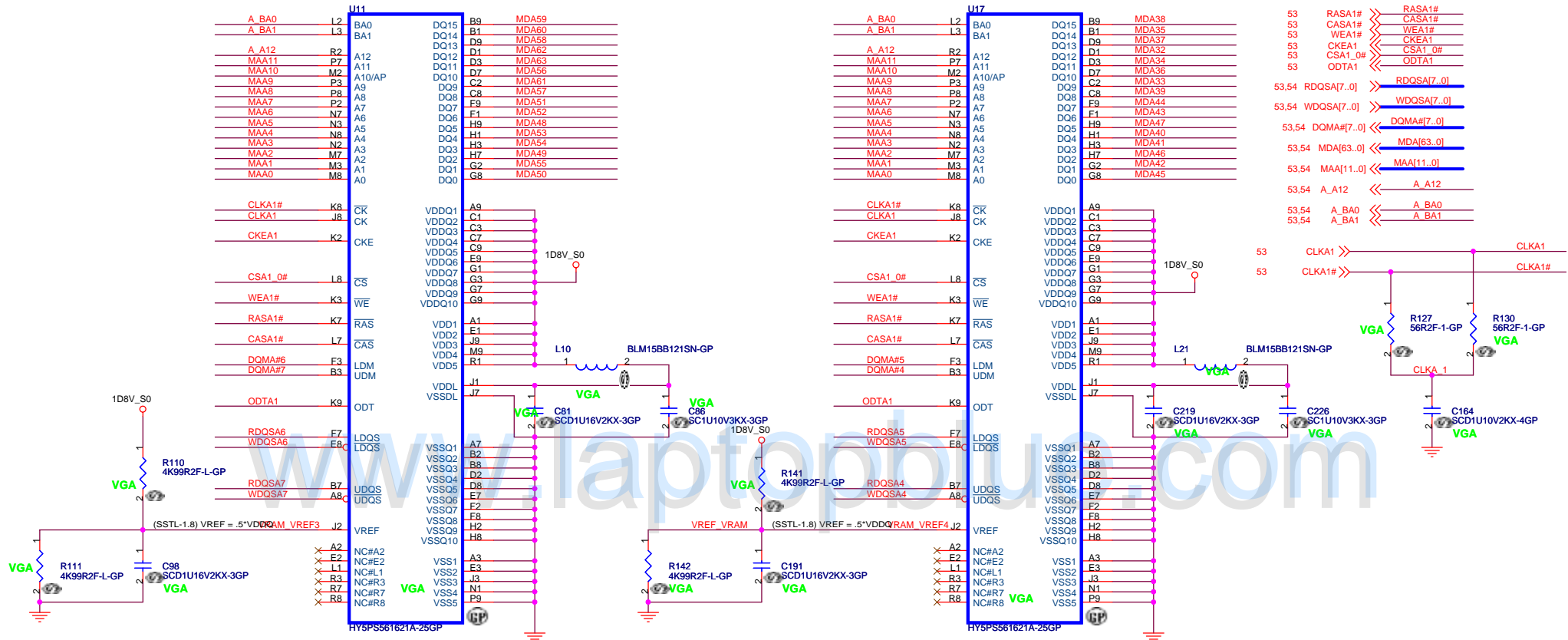


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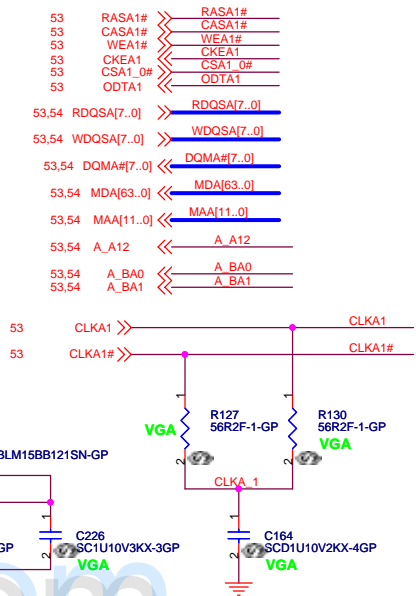
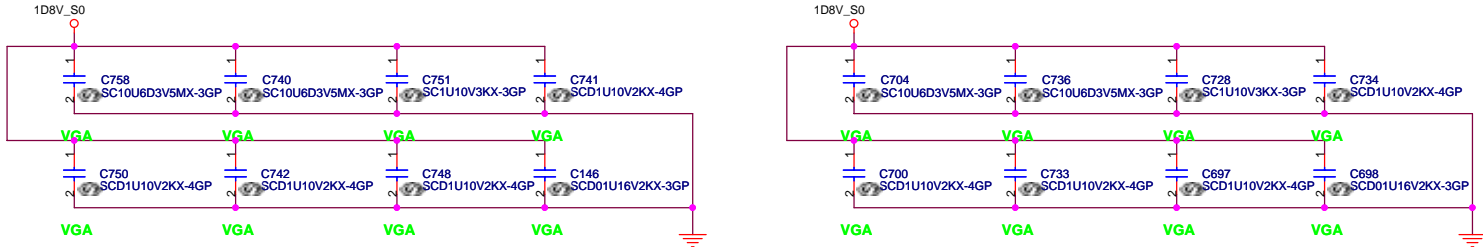
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DDR2 BGA MEMORY



72.55616.C0U
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