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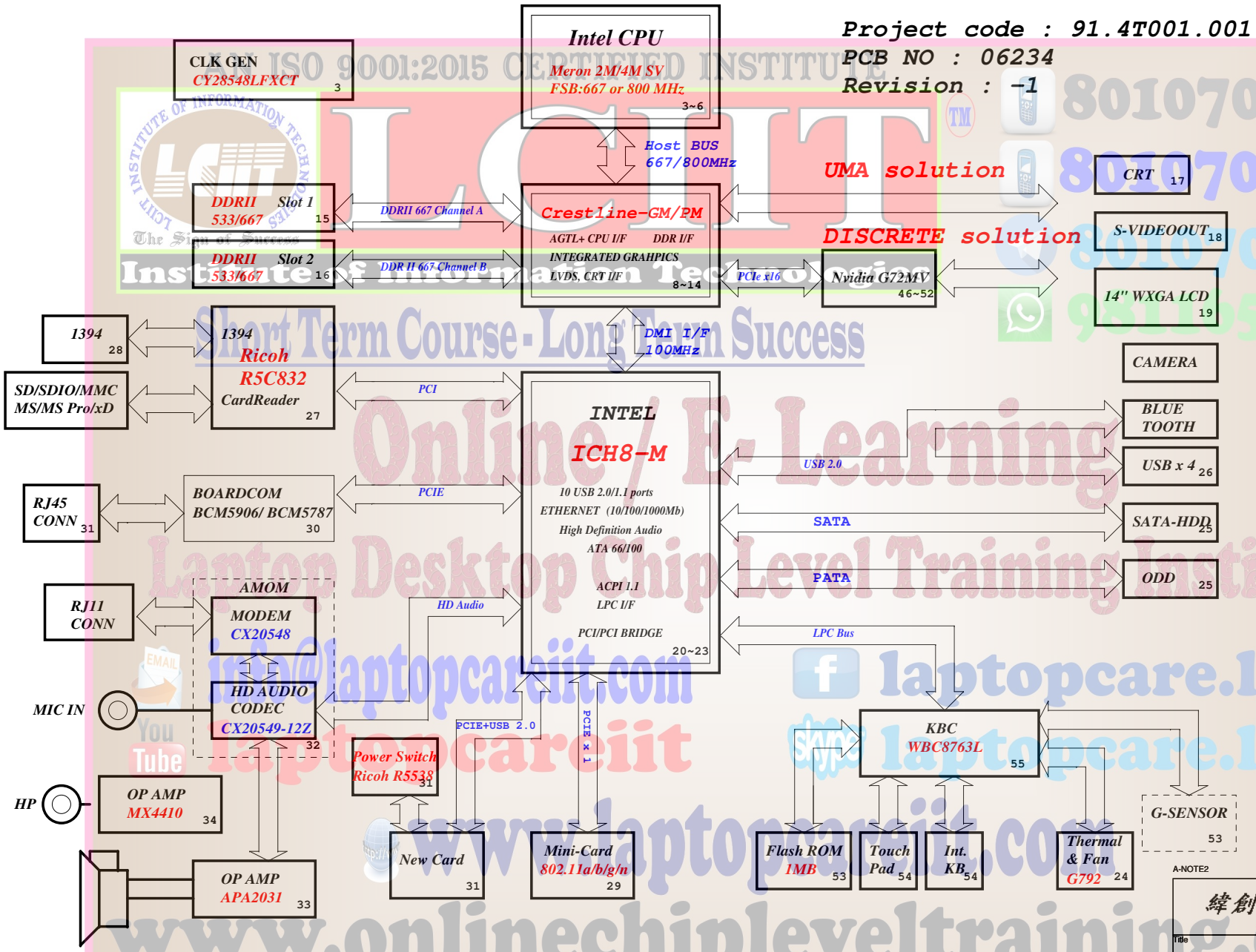
Anote2.0 Block Diagram

Project code : 91.4T001.001
PCB NO : 06234
Revision : -1



SYSTEM DC/DC TPS51120 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3D3V_S5

SYSTEM DC/DC ISL6268CAZ 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51116 40	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 0D9V_S0

CHARGER ISL6255	
INPUTS	OUTPUTS
DCBATOUT	BT+ 20V 3.0A 5V 100mA

CPU DC/DC ISL6262ACRZ 36,37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

PCB LAYER	
L1:	Signal 1
L2:	VCC
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	Signal 4

A-NOTE2

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Title: Block Diagram
Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1
Date: Thursday, March 22, 2007 | Sheet 1 of 56

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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD_tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable
high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule
High=No Reboot

8.2K PULL HIGH

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<21,23> +RTCVCC → +RTCVCC
<4,5,6,7,8,11,12,13,21,23,39,56> 1D05V_S0 → 1D05V_S0
<3,10,12,23,42> 1D25V_S0 → 1D25V_S0
<30> 1D2V_LAN_S5 → 1D2V_LAN_S5
<31,57> 1D5V_NEW_S0 → 1D5V_NEW_S0
<10,12,13,15,16,40,42,45> 1D8V_S3 → 1D8V_S3
<30,31> 2D5V_LAN_S5 → 2D5V_LAN_S5
<21,24,38,44,53,54,55> 3D3V_AUX_S5 → 3D3V_AUX_S5
<30,31> 3D3V_LAN_S5 → 3D3V_LAN_S5
<8,16,11,12,18,15,16,17,18,19,20,21,22,23,24,25,27,28,29,30,31,32,34,35,36,38,39,41,42,45,46,47,50,52,53,54,55,56,57,58> 3D3V_S0 → 3D3V_S0
<19,20,22,23,26,29,30,31,32,38,40,43,45,53,54,55,56,58> 3D3V_S5 → 3D3V_S5
<29,38,43> 5V_AUX_S5 → 5V_AUX_S5
<17,19,22,23,24,25,33,35,36,39,41,42,45,46,54,56,57> 5V_S0 → 5V_S0
<23,26,38,40,45,56> 5V_S5 → 5V_S5
<43,44> AD+ → AD+
<19,36,37,38,39,40,41,43,45,56> DCBATOUT → DCBATOUT
<10,15,16,40> DDR_VREF_S3 → DDR_VREF_S3
<19> LCDVDD_S0 → LCDVDD_S0
<5,6,37> VCC_CORE_S0 → VCC_CORE_S0

A-NOTE2

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Title: Table of Content

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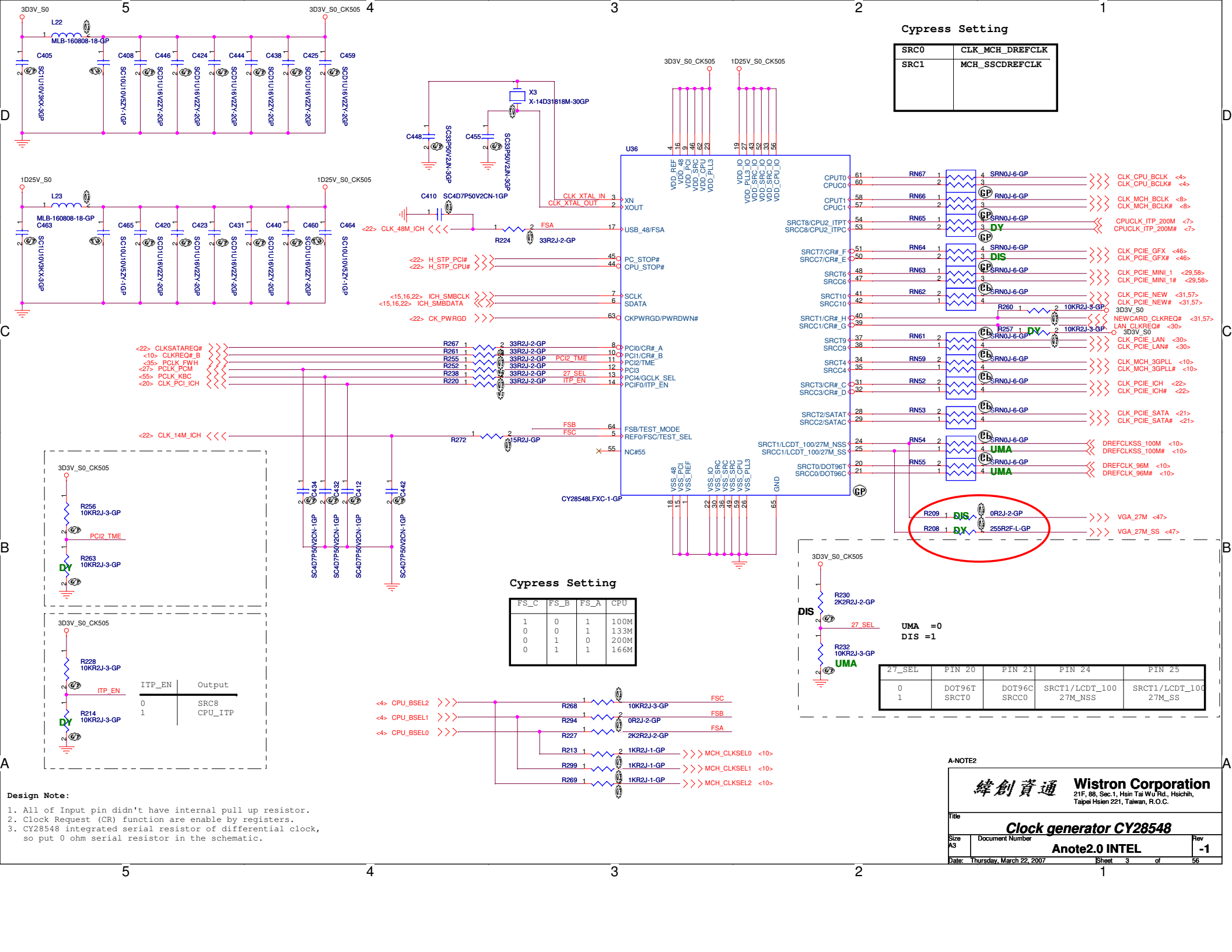
Cypress Setting
SRC0 CLK_MCH_DREFCLK
SRC1 MCH_SSCDREFCLK
U36
CY28548LFXC-1-GP
Cypress Setting
FS_C FS_B FS_A CPU
1 0 1 100M
0 0 1 133M
0 1 0 200M
0 1 1 166M
UMA =0
DIS =1
27_SEL PIN 20 PIN 21 PIN 24 PIN 25
0 DOT96T SRCT0 DOT96C SRCC0 SRCT1/LCDT_100 27M_NSS SRCT1/LCDT_100 27M_SS
1
ITP_EN Output
0 SRC8
1 CPU_ITP
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
A-NOTE2
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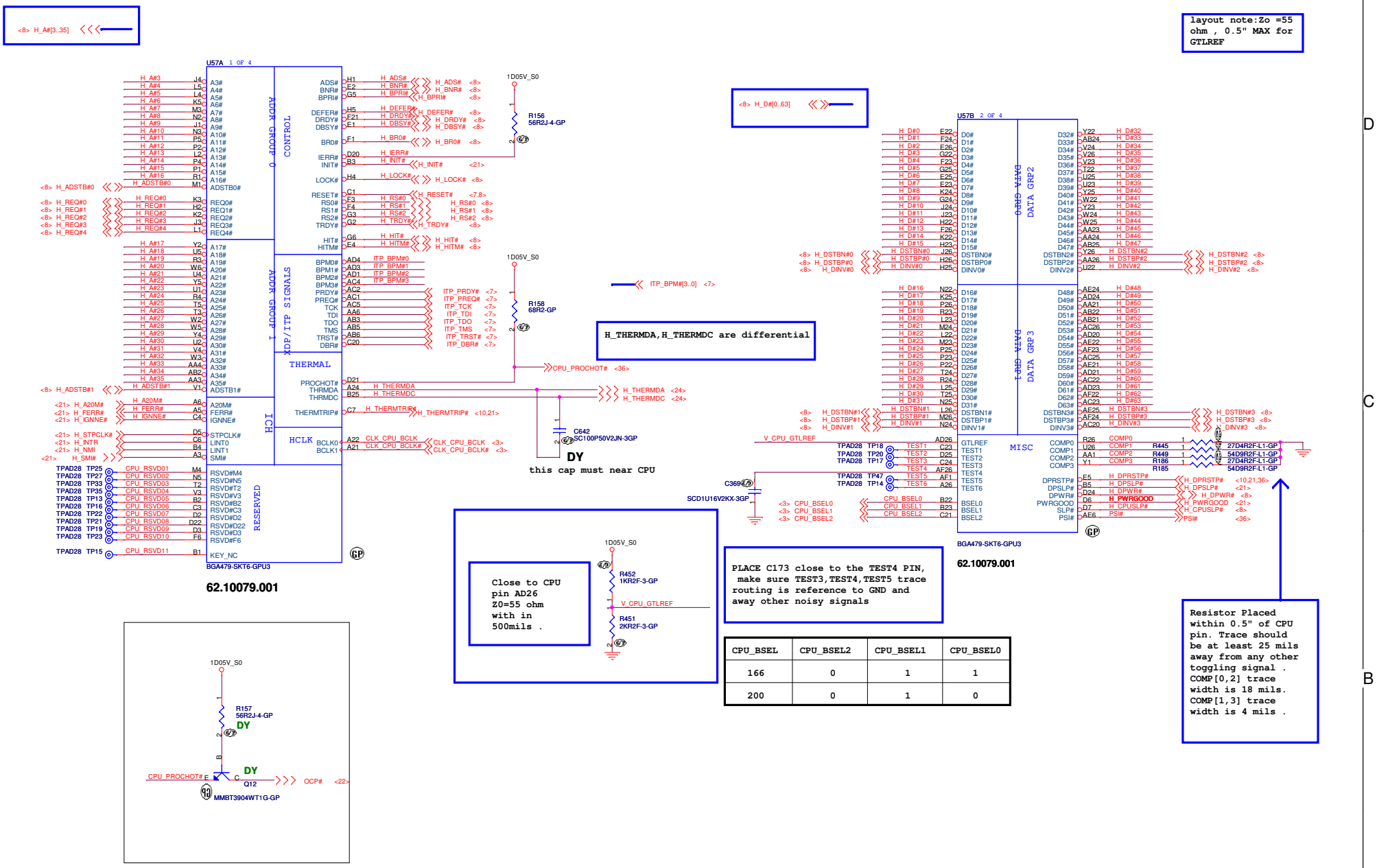
Title
Clock generator CY28548
Size A3
Document Number Anote2.0 INTEL
Rev -1
Date: Thursday, March 22, 2007 Sheet 3 of 56



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

A-NOTE2

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Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: Anote2.0 INTEL | Rev: -1

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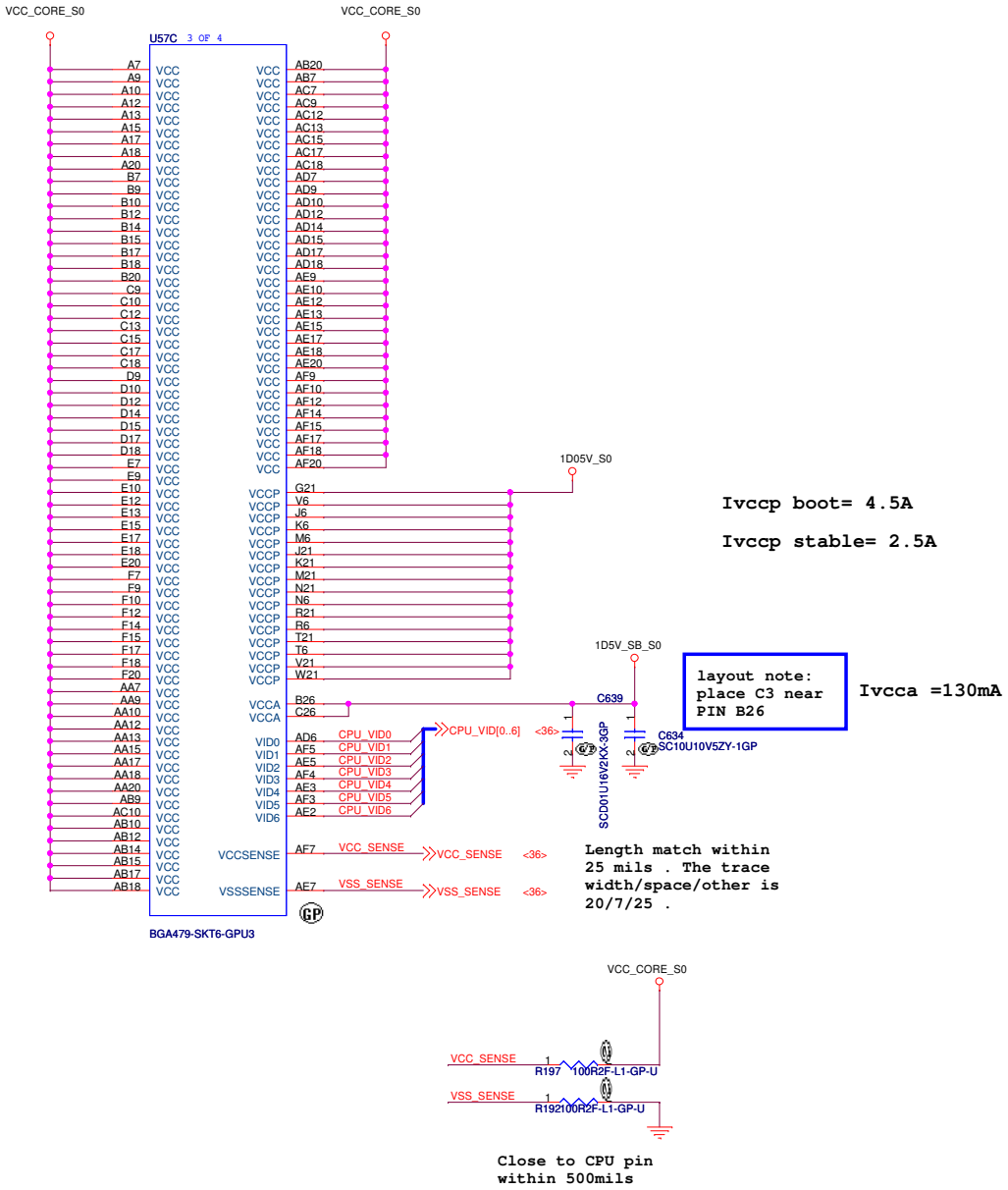

A-NOTE2

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Title: *Meron(2/3)-AGTL+/PWR*	
Size: A3	Document Number: Anote2.0 INTEL
Rev: -1	
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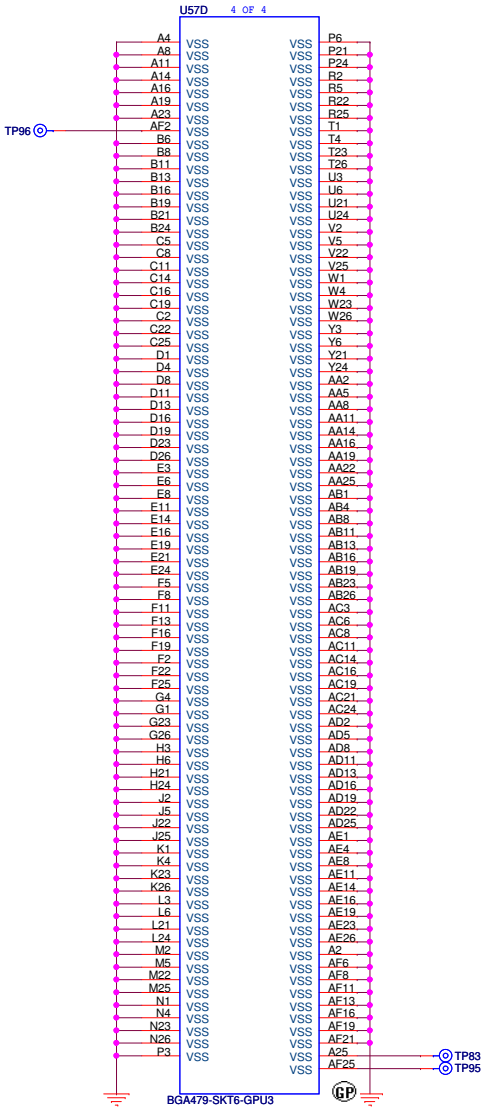

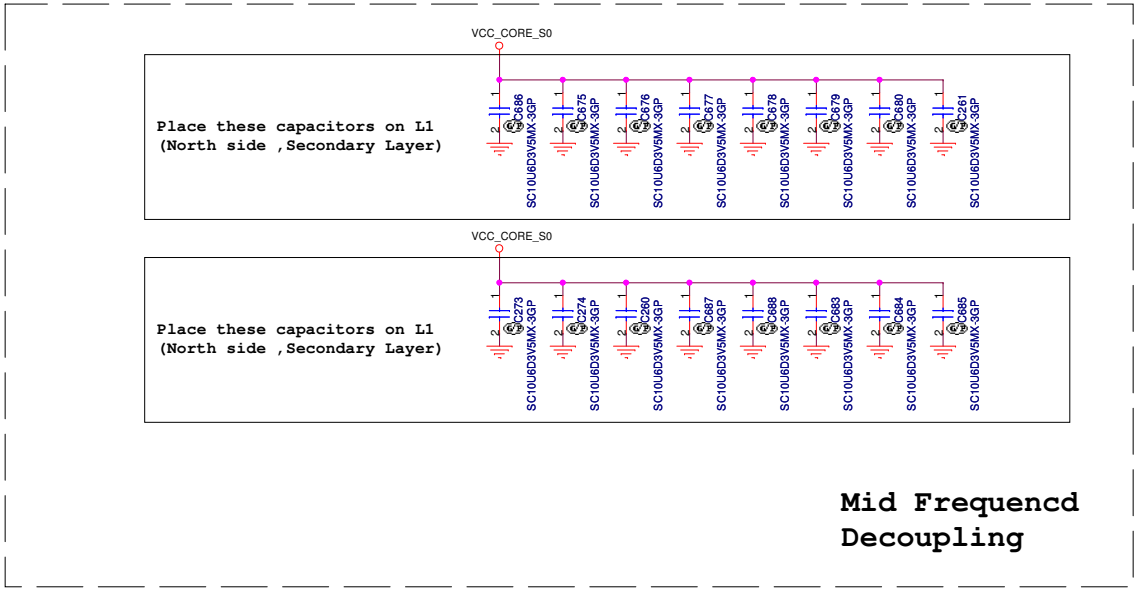

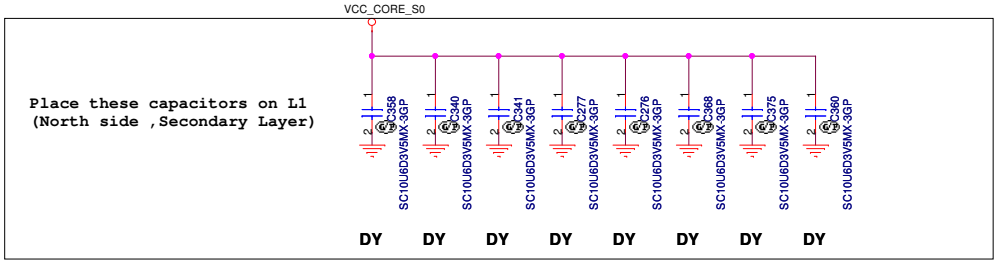

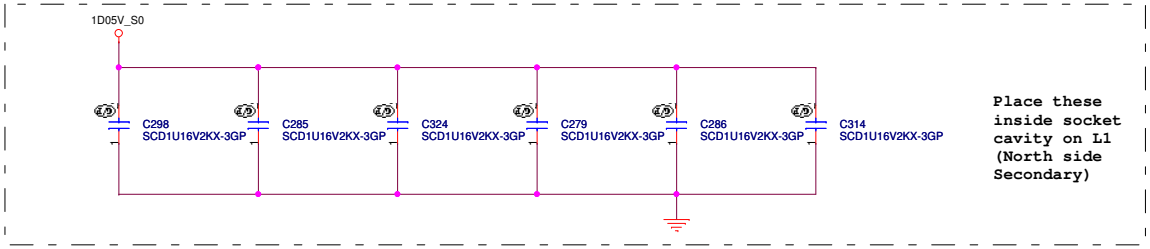

A-NOTE2

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Title: Meron(3/3)-GND&Bypass

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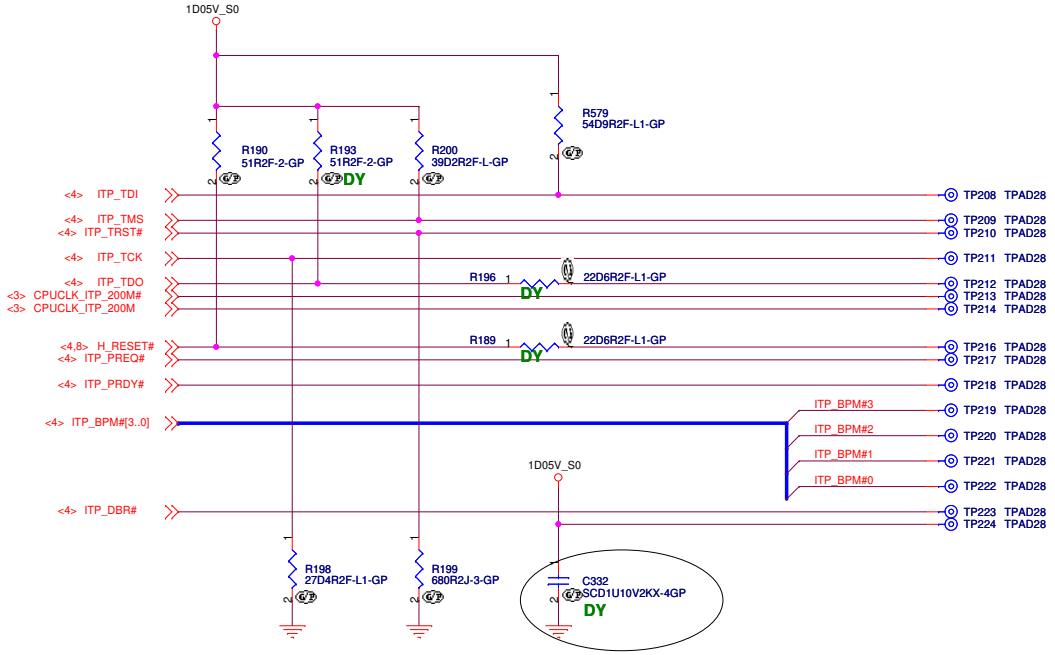
ITP Connector



A-NOTE2

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Title: ***Meron(3/3)-GND&Bypass***

Size	Document Number	Rev
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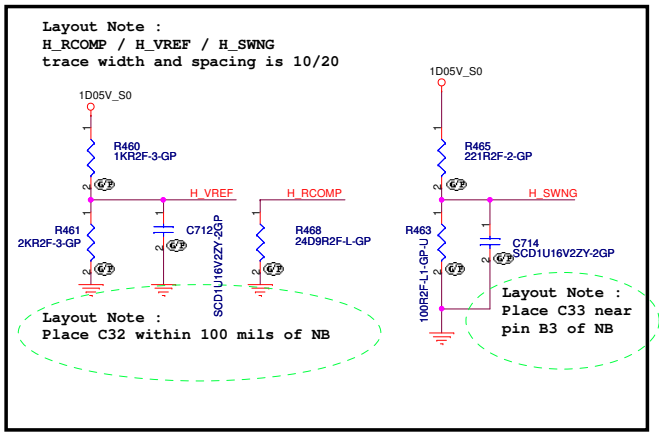
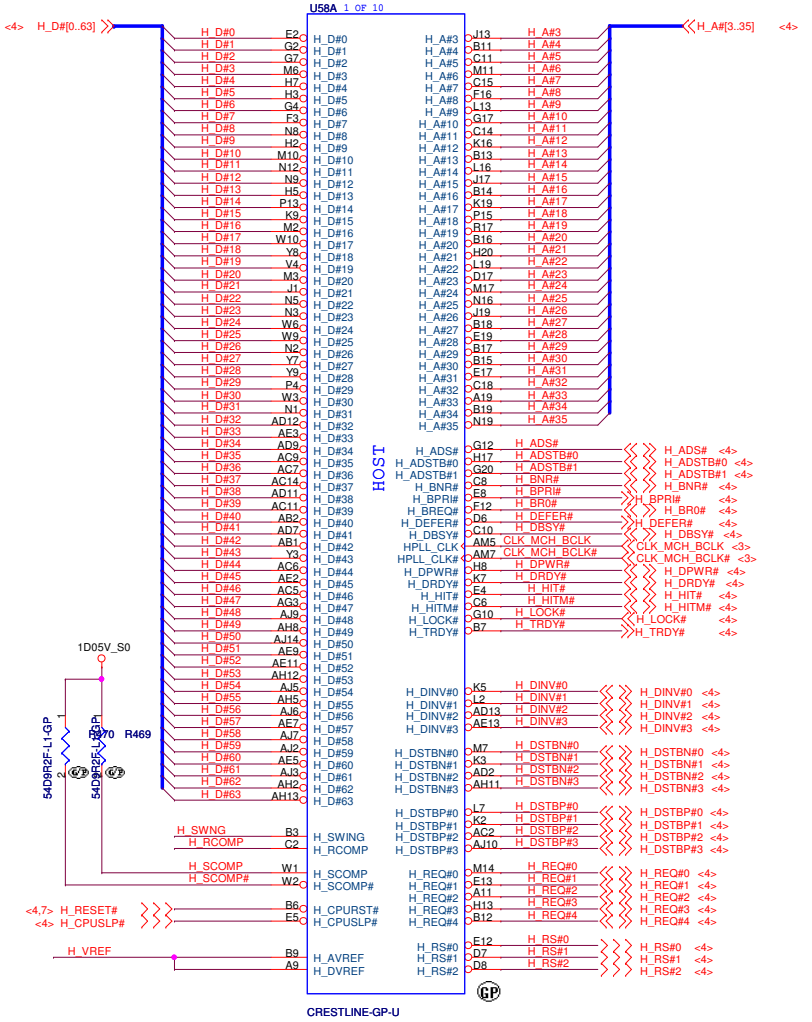
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces





A-NOTE2	
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CRESTLINE(1/7)-AGTL+/DMI/DDR2
Size: Custom	Document Number: Anote2.0 INTEL
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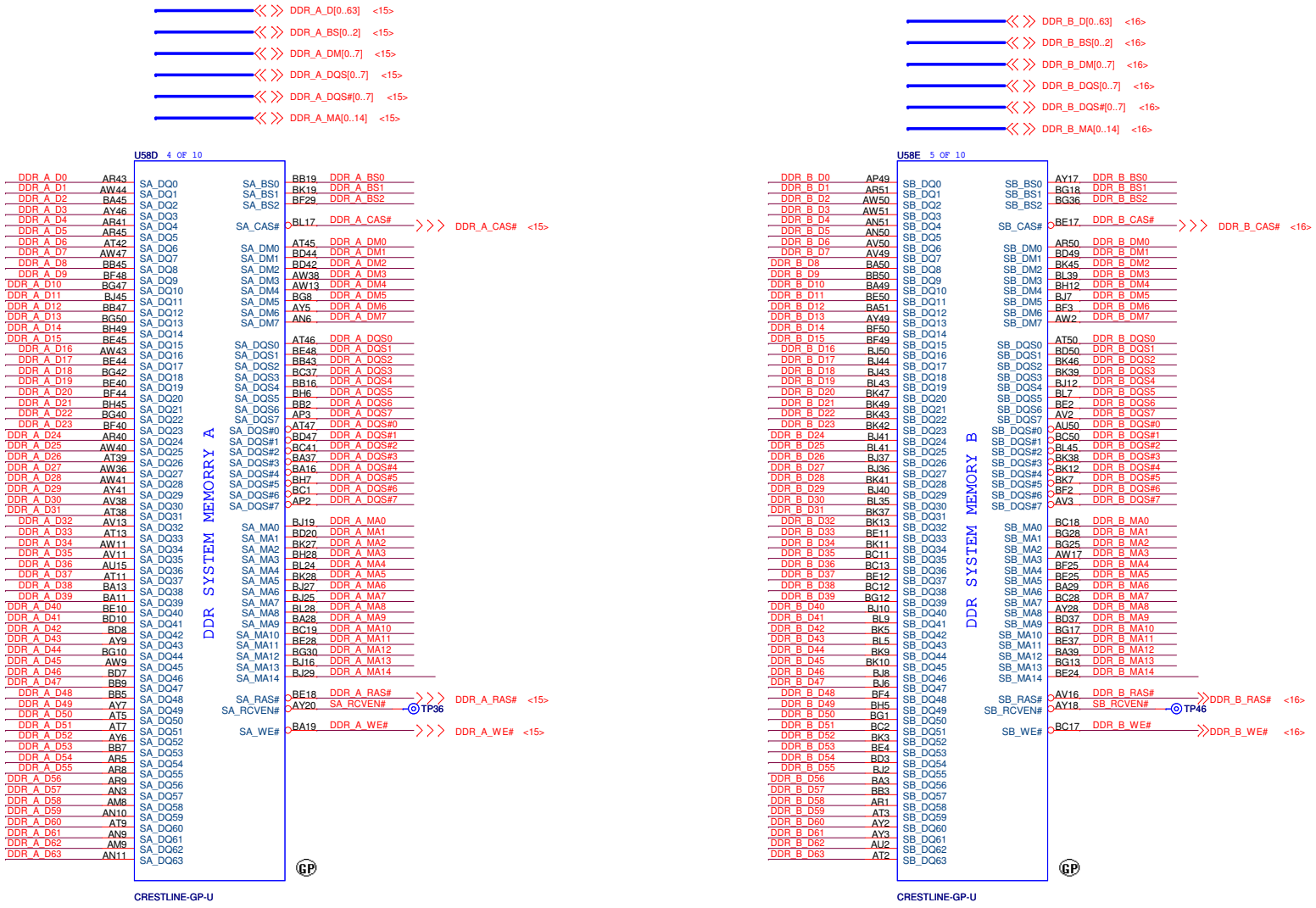

A-NOTE2

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Title
CRESTLINE(2/7)-DDR2 A/B CH

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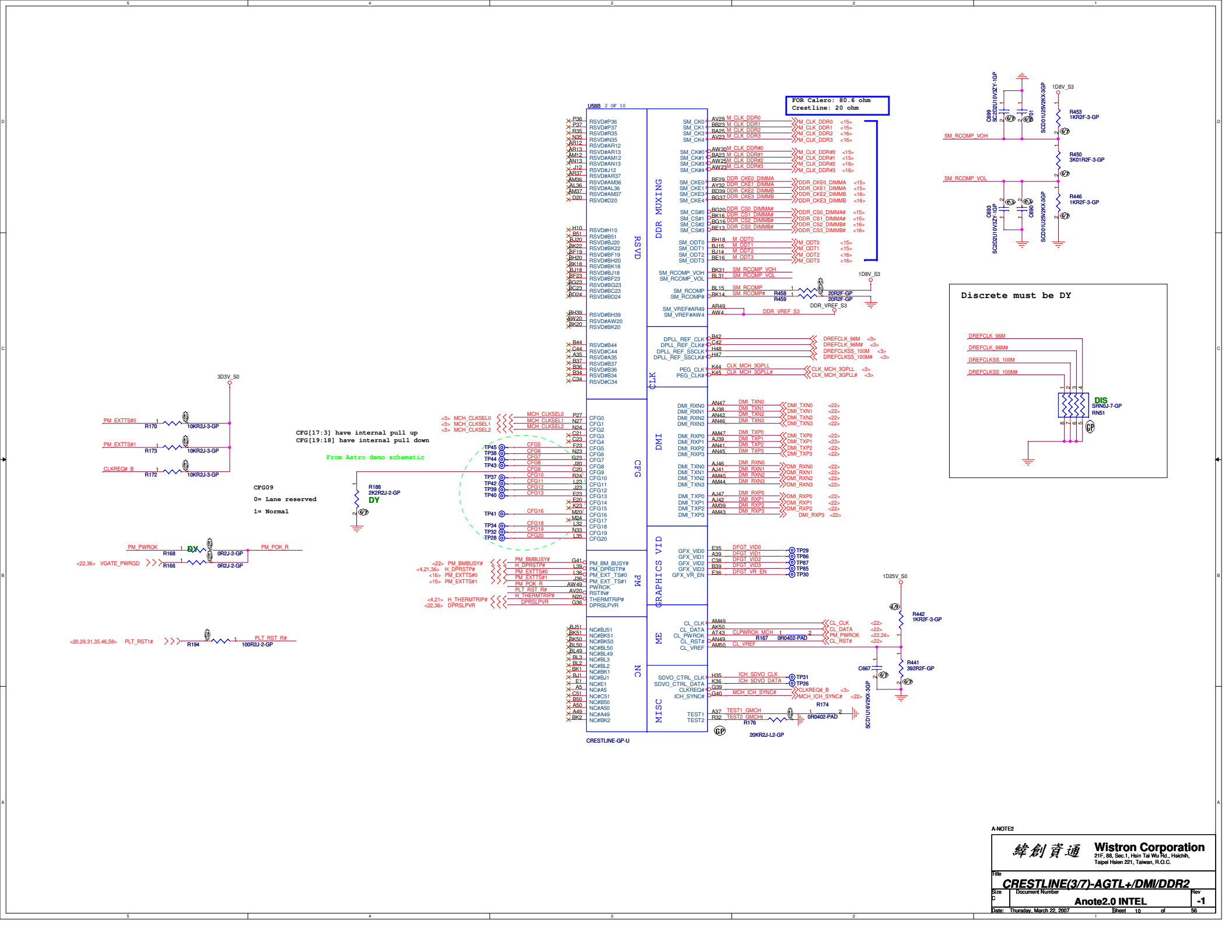
U58B 2 OF 10
FOR Calero: 80.6 ohm
Crestline: 20 ohm
RSVD
DDR MUXING
CLK
DMI
CFG
PM
GRAPHICS VID
ME
NC
MISC
Discrete must be DY
DIS
SRN0J-7-GP
RN51
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
From Astro demo schematic
CFG09
0= Lane reserved
1= Normal
DY
CRESTLINE-GP-U
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
CRESTLINE(3/7)-AGTL+/DMI/DDR2
Anote2.0 INTEL
Thursday, March 22, 2007
A-NOTE2

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

PEGCOMP trace width and spacing is 20/25 mils.

FOR Calero: 255 ohm
Crestline: 1.3k ohm

U58C 3 OF 10

CRESTLINE-GP-U

A-NOTE2

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Title: CRESTLINE(4/7)-VGA/LVDS/TV

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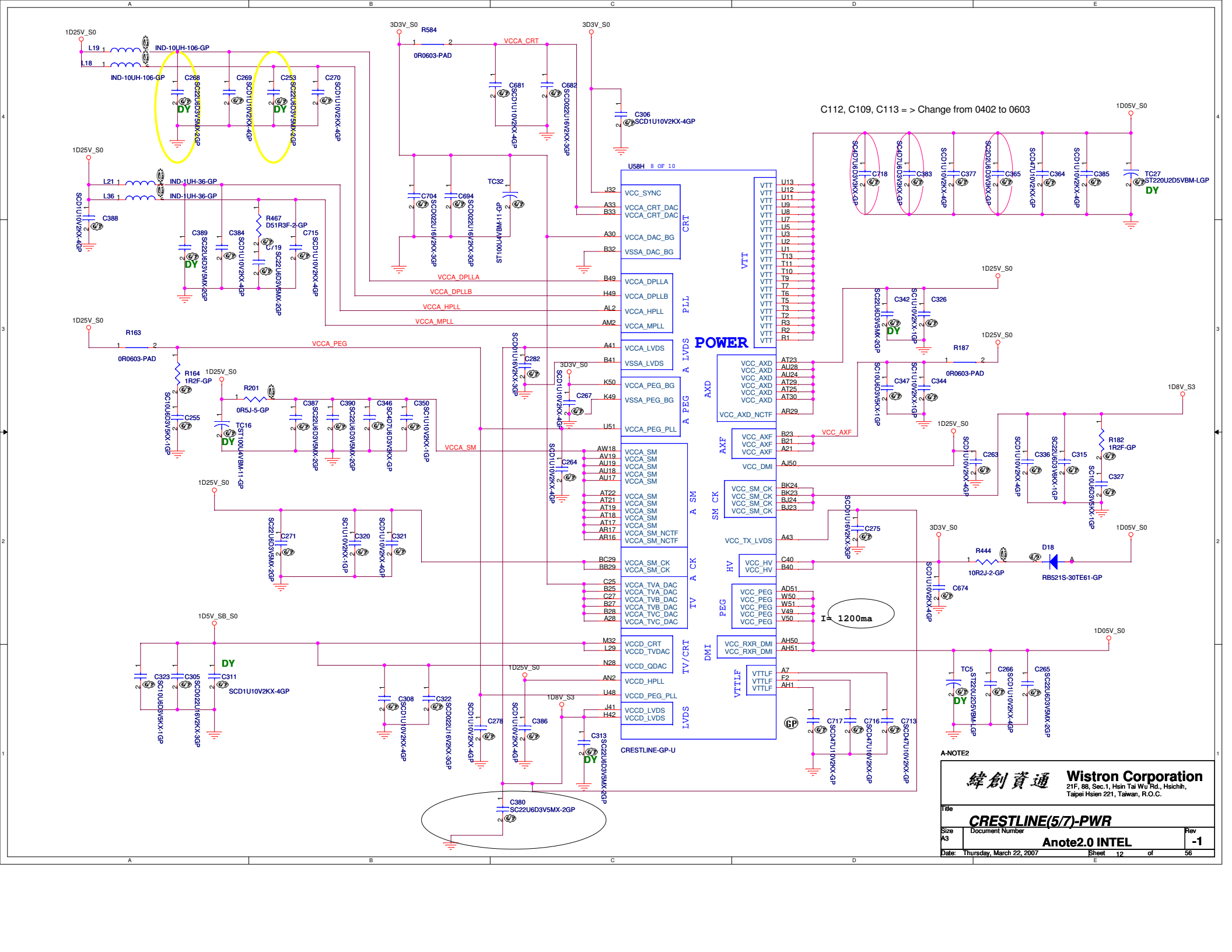
C112, C109, C113 = > Change from 0402 to 0603
POWER
I= 1200ma
CRESTLINE-GP-U
A-NOTE2
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Title
CRESTLINE(5/7)-PWR
Size A3
Document Number
Anote2.0 INTEL
Rev -1
Date: Thursday, March 22, 2007
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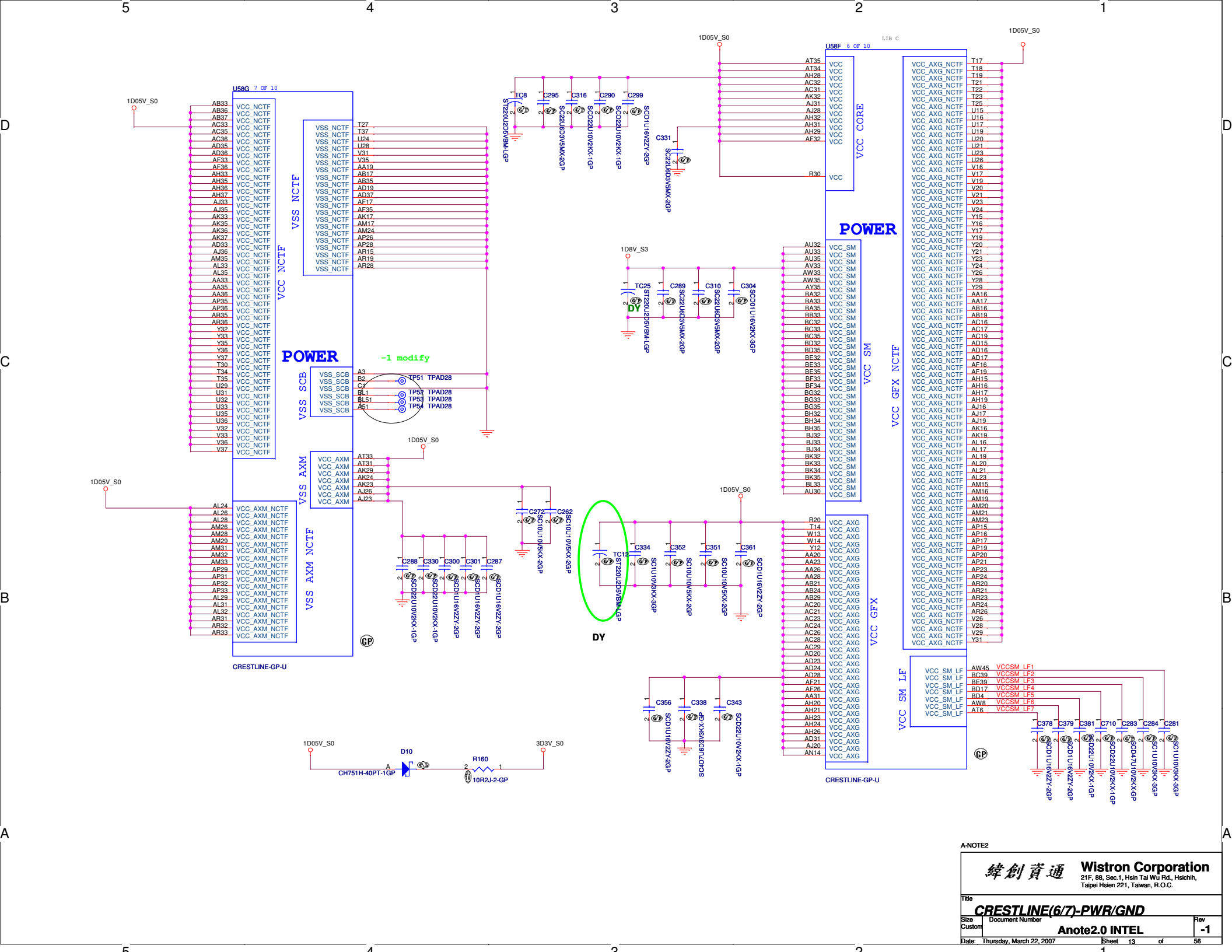

A-NOTE2

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Title: CRESTLINE(6/7)-PWR/GND

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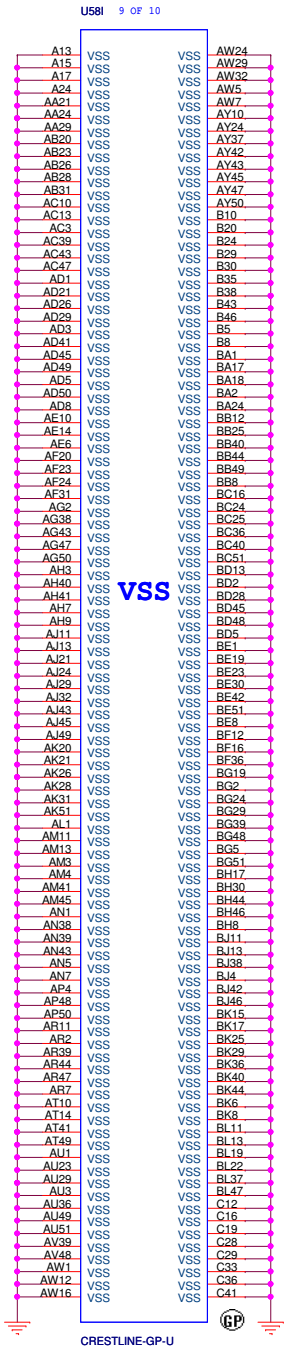

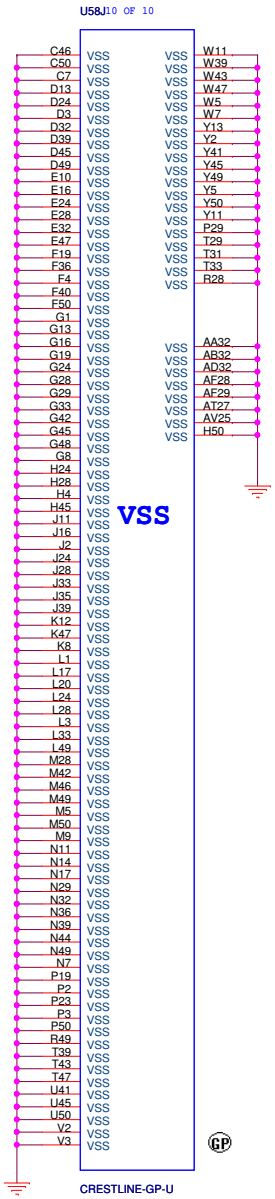

A-NOTE2

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Title
CRESTLINE(7/7)-PWR/GND

Size	Document Number	Rev
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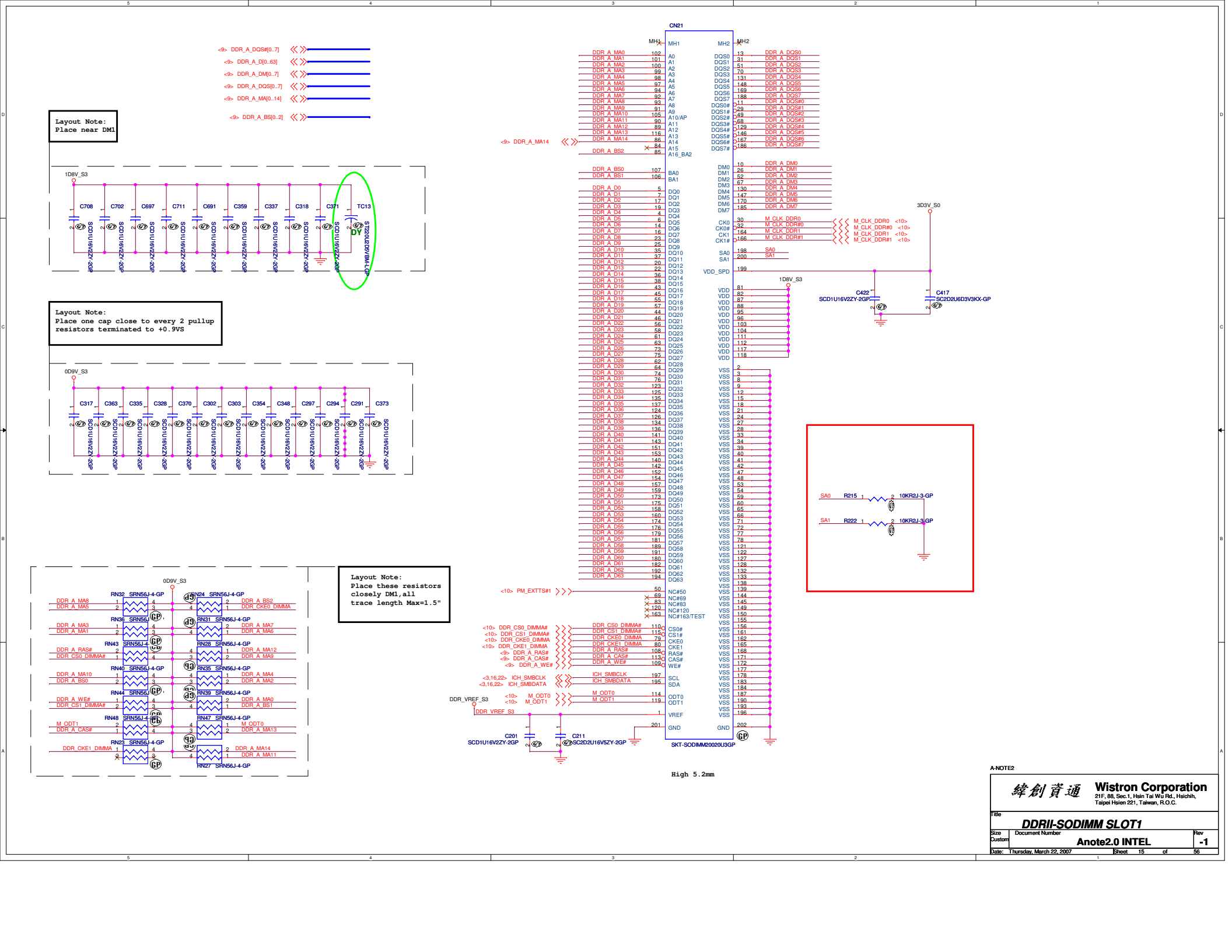
Date: Thursday, March 22, 2007 Sheet 14 of 56


Layout Note:
Place near DM1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
CN21
SKT-SODIMM20020U3GP
High 5.2mm
A-NOTE2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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DDRII-SODIMM SLOT1
Anote2.0 INTEL
Thursday, March 22, 2007
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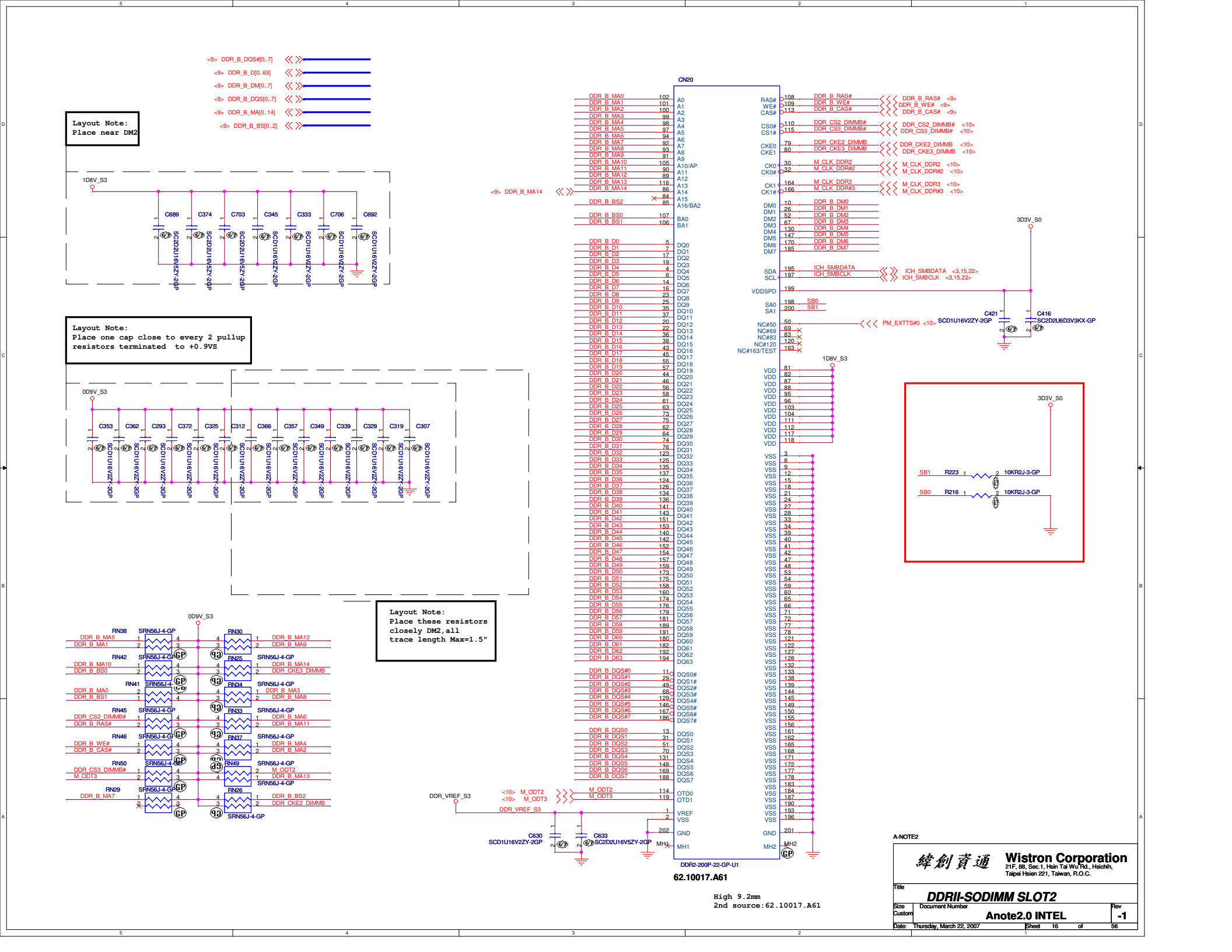
Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
CN20
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
2nd source:62.10017.A61
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
DDRII-SODIMM SLOT2
Anote2.0 INTEL
-1
Thursday, March 22, 2007
16
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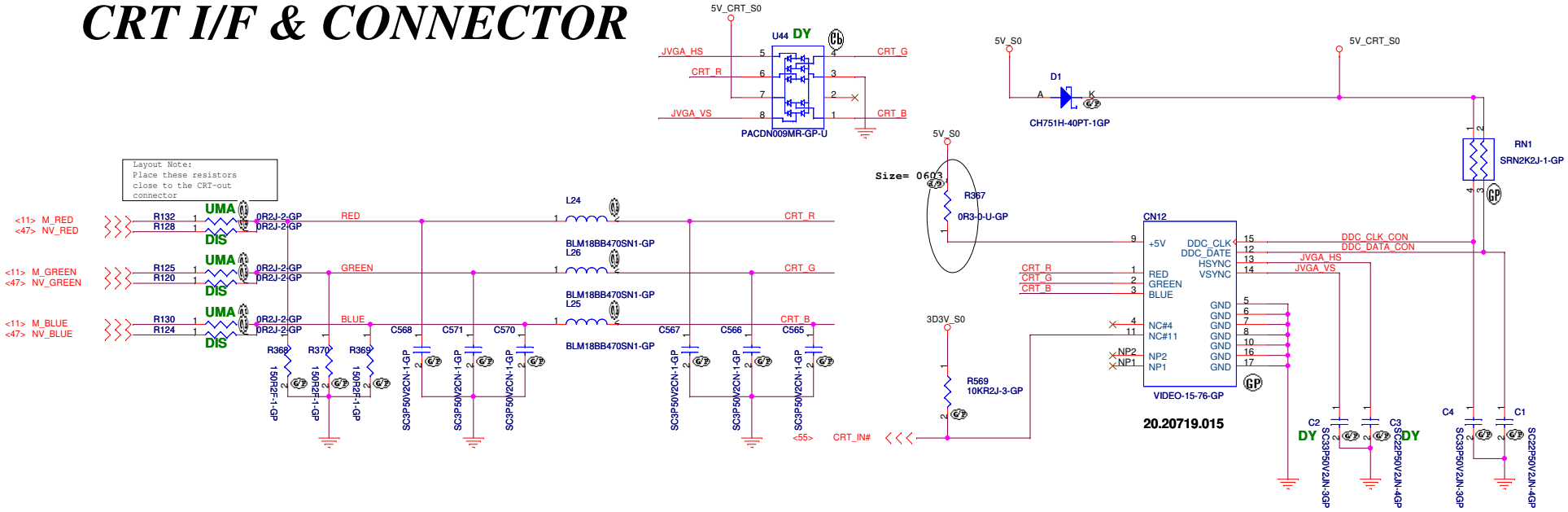
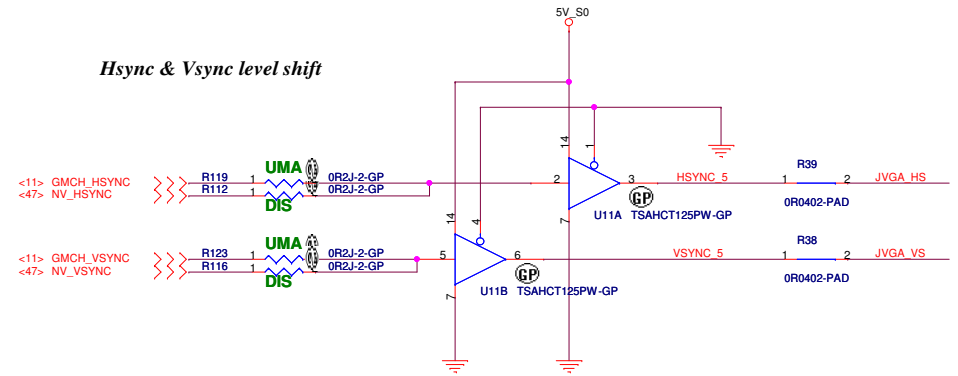
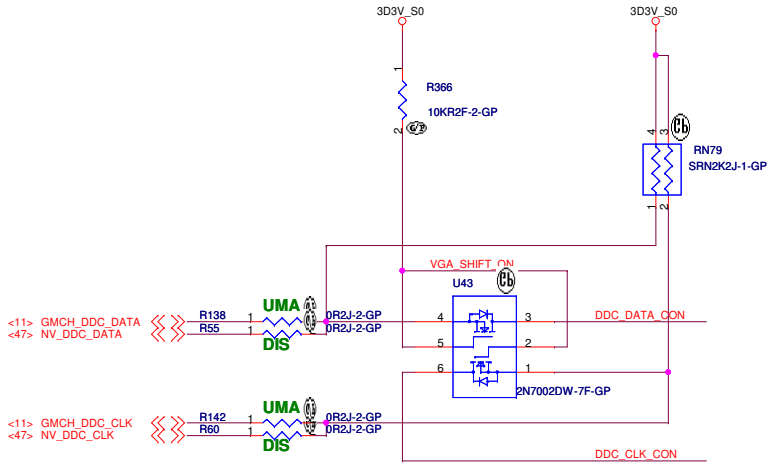
CRT I/F & CONNECTOR



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

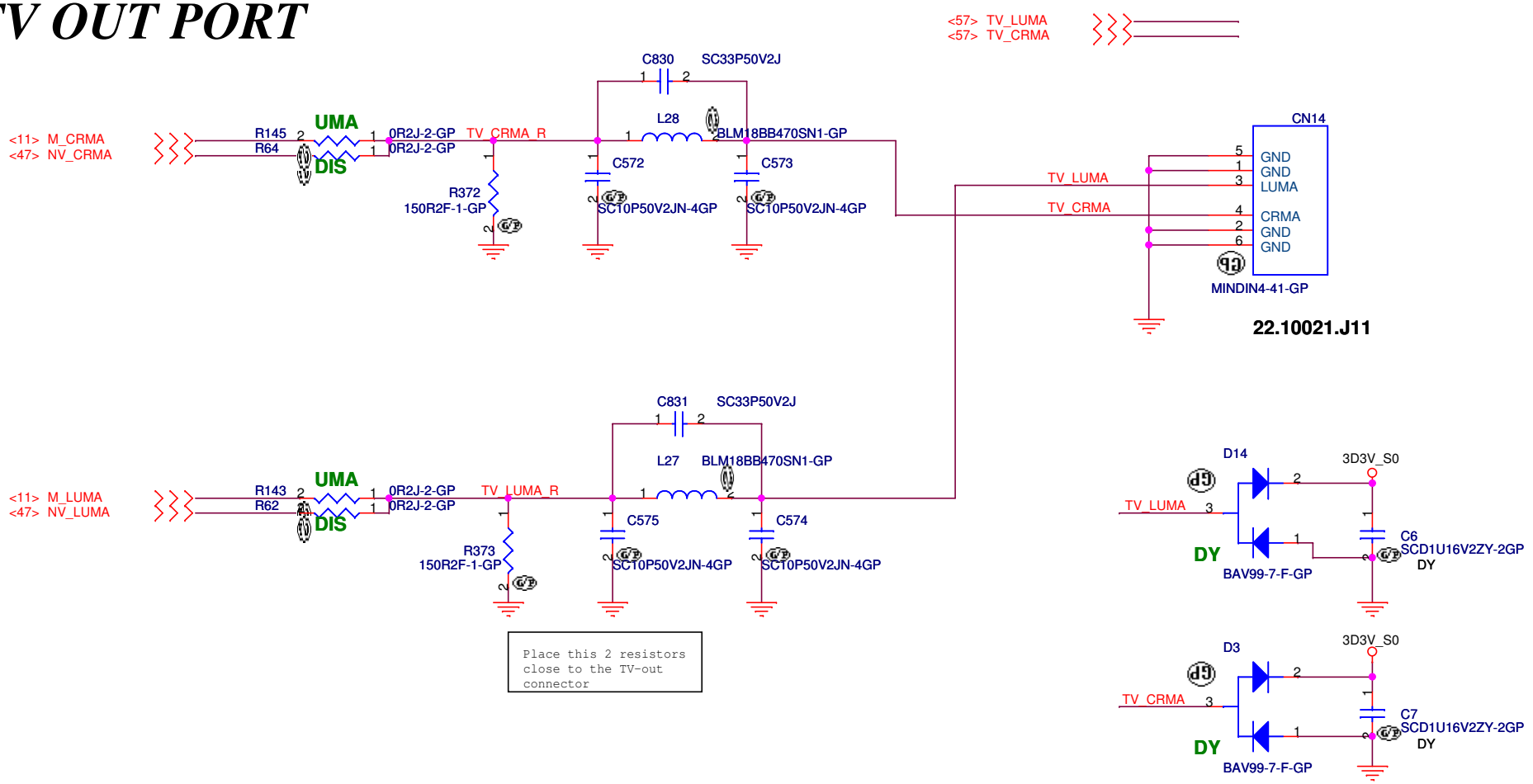




A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **CRT Connector**		
Size: A3	Document Number: **Anote2.0 INTEL**	Rev: -1
Date: Thursday, March 22, 2007	Sheet 17 of 56	

TV OUT PORT



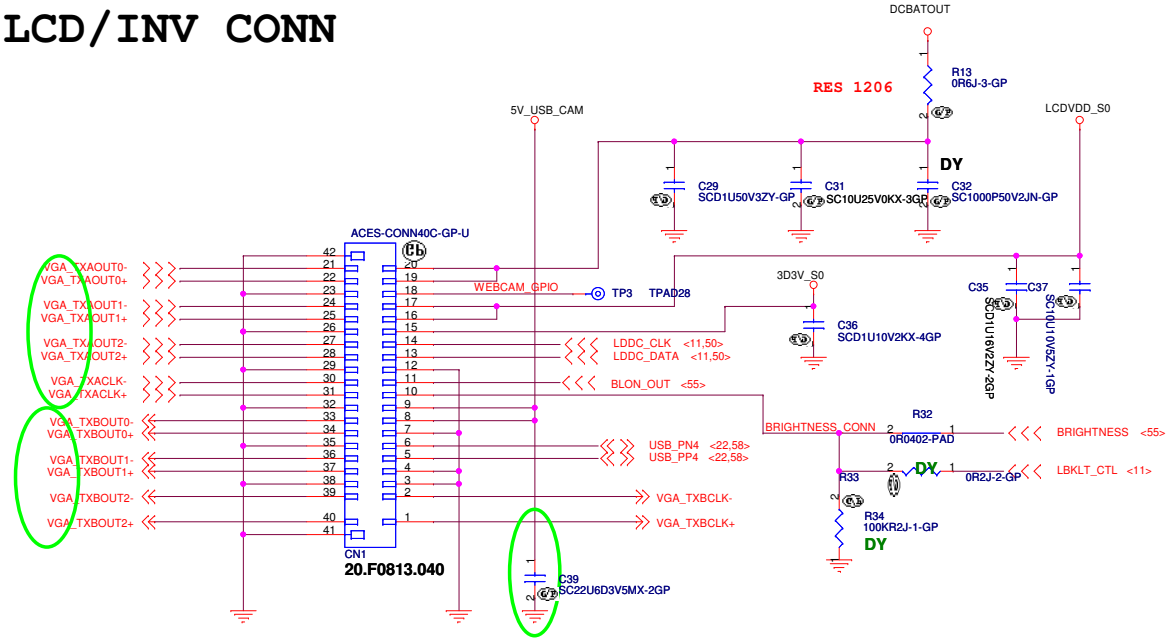
A-NOTE2

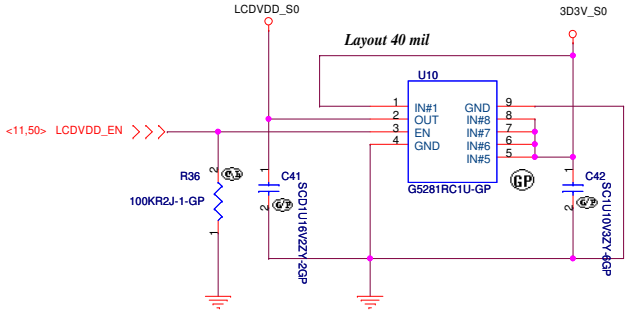
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

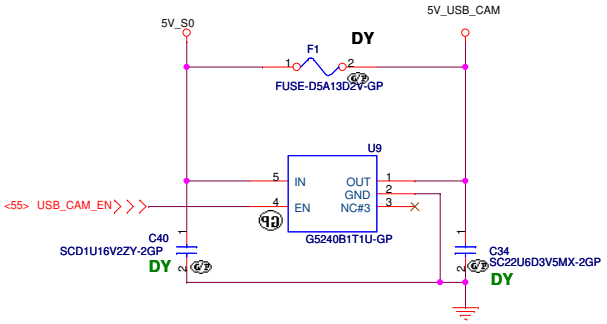
Title	***TV Connector***	
Size A4	Document Number **Anote2.0 INTEL**	Rev **-1**
Date: Thursday, March 22, 2007	Sheet 18 of 56	

LED / INVERTER INTERFACE

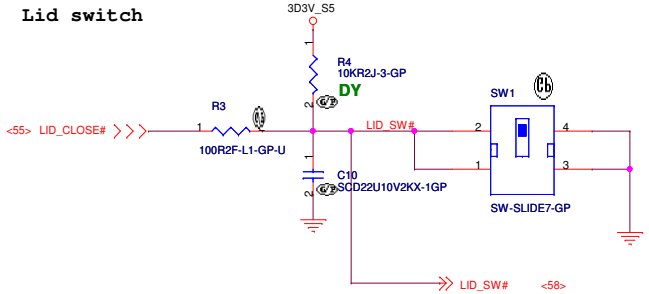
LCD/INV CONN



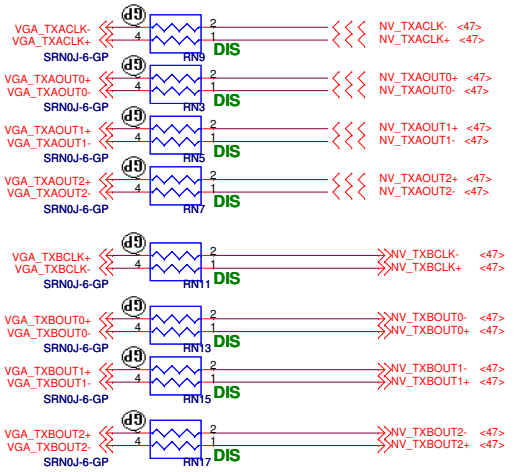




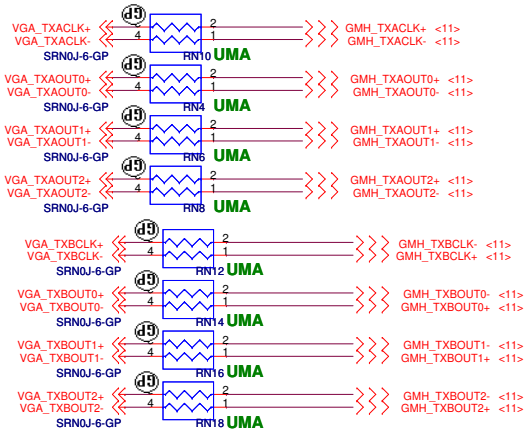
Lid switch



ATI LVDS INTERFACE



UMA LVDS INTERFACE



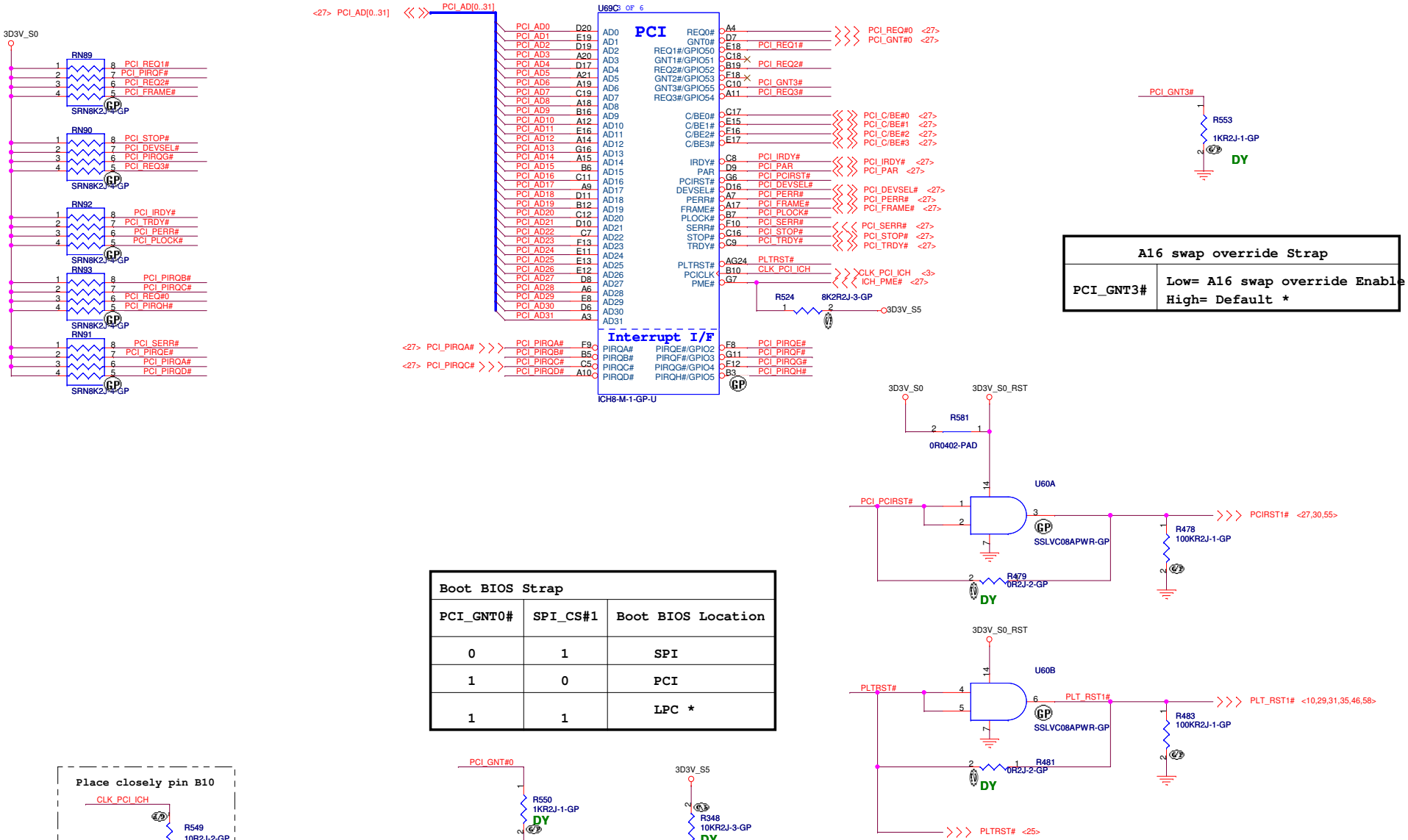
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 19 of 56



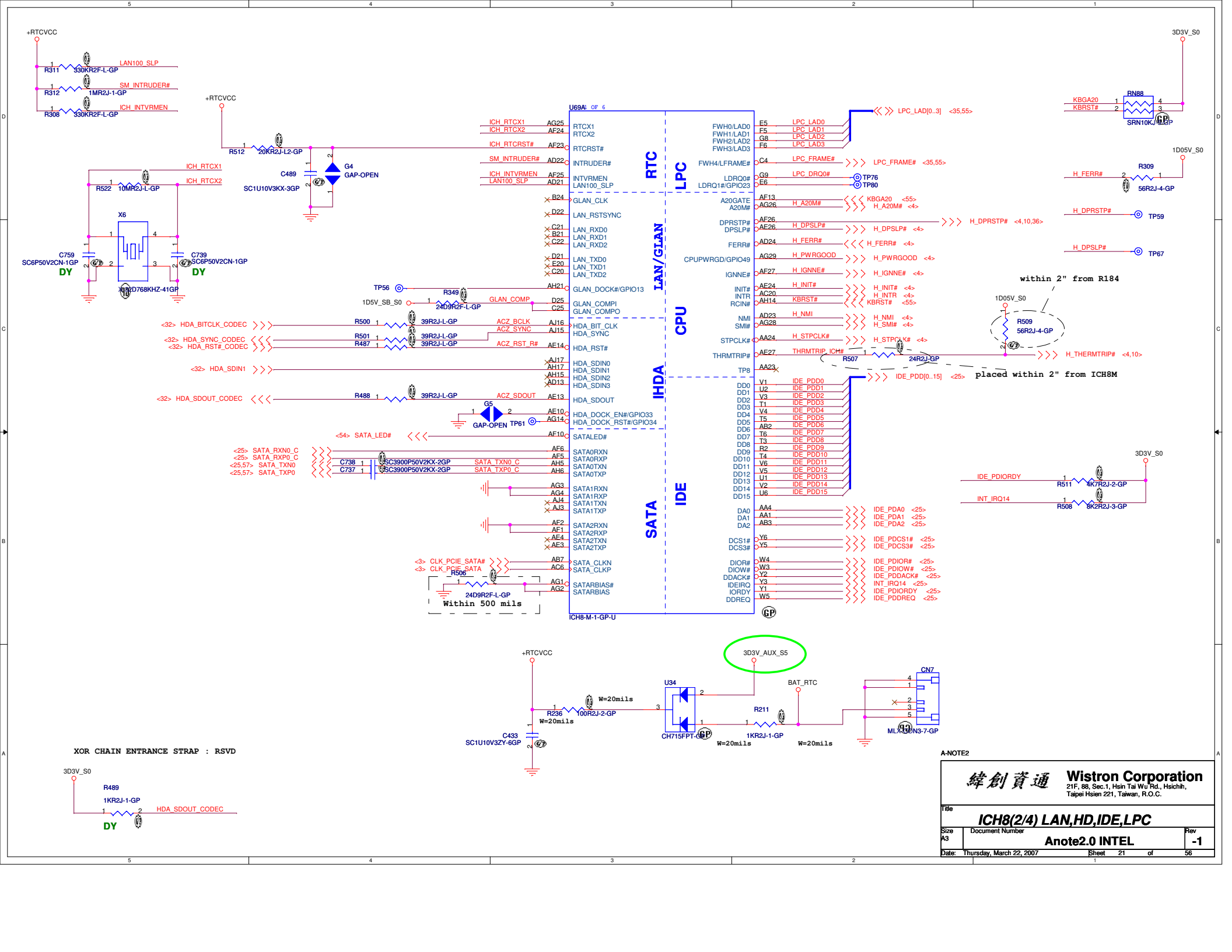
A-NOTE2

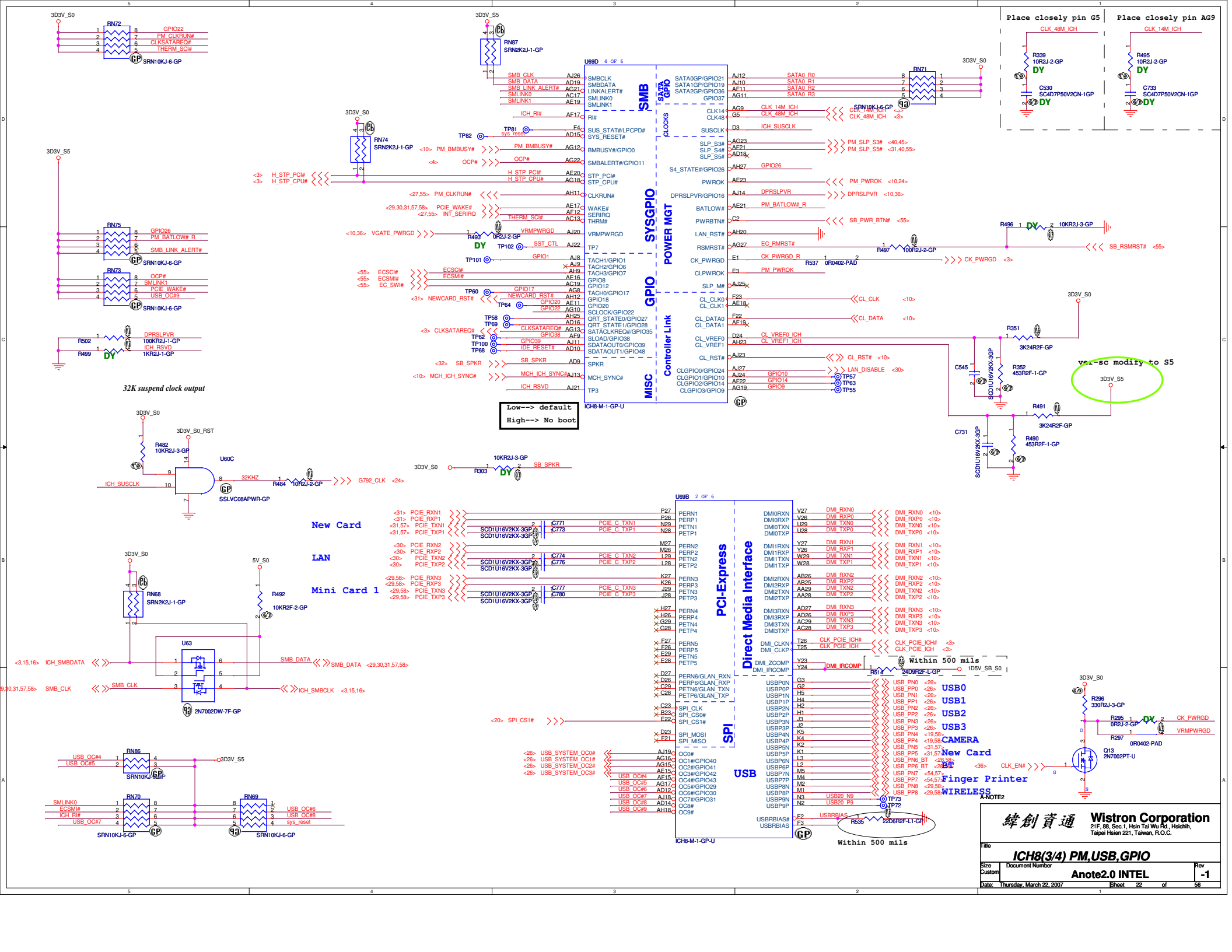
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

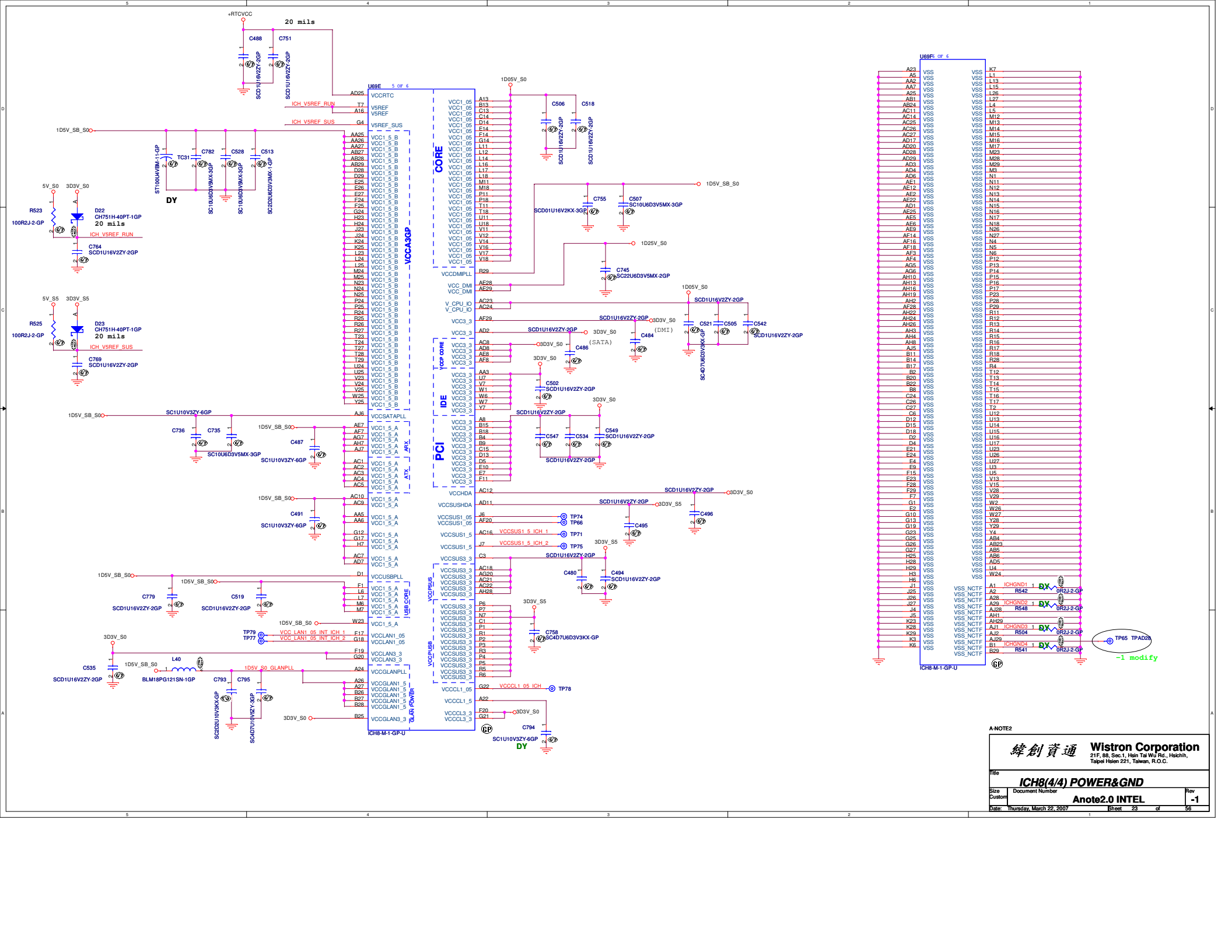
Title: ICH8(1/4)-PCI/INT

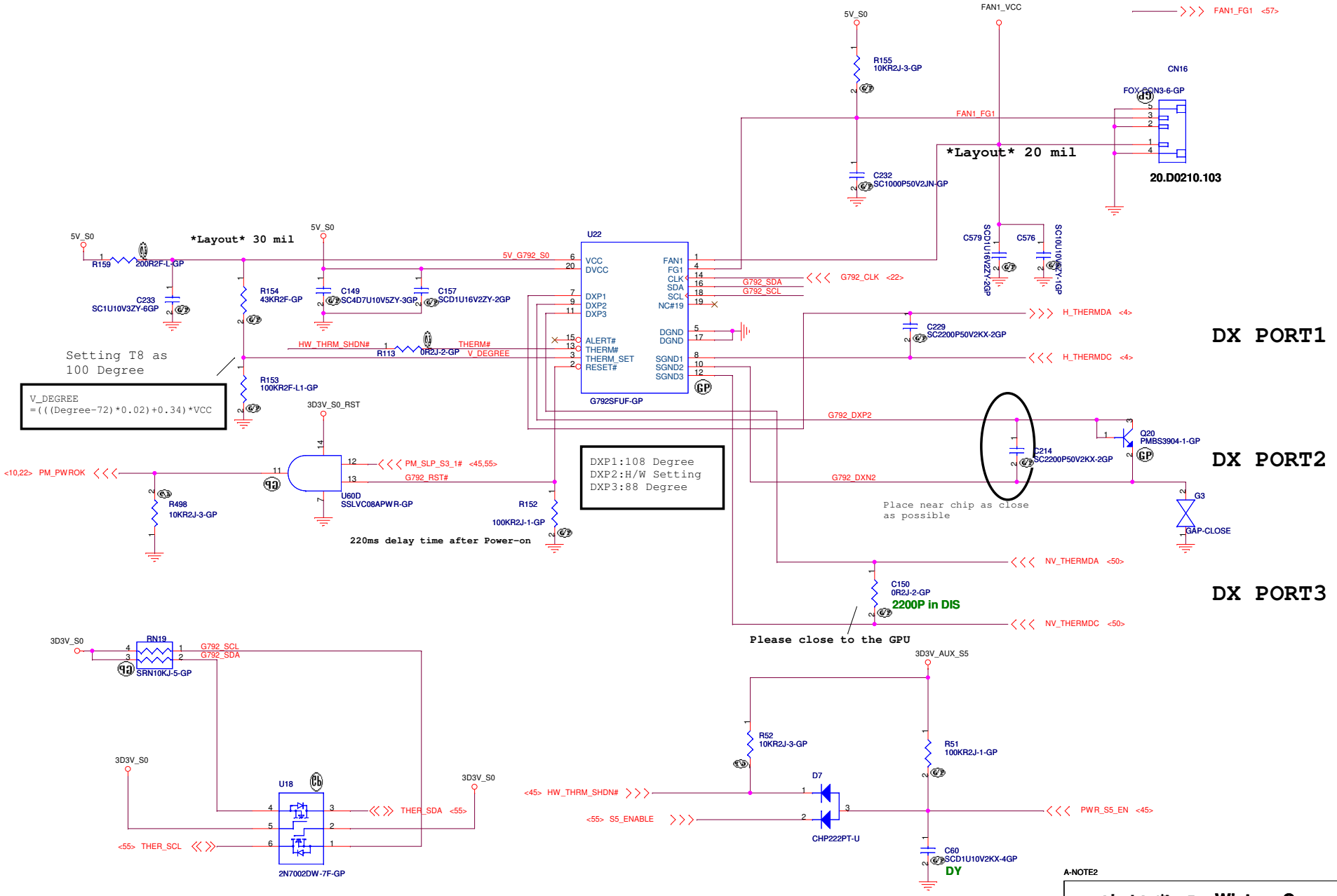
Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 20 of 56


+RTCVCC
R311 330KR2F-L-GP LAN100_SLP
R312 1MR2J-1-GP SM_INTRUDER#
R308 330KR2F-L-GP ICH_INTVRMEN
R512 20KR2J-L2-GP
C489 SC1U10V3KX-3GP
G4 GAP-OPEN
R522 10MR2J-L-GP ICH_RTCX1 ICH_RTCX2
X6 X32D768KHZ-41GP
C759 SC6P50V2CN-1GP DY
C739 SC6P50V2CN-1GP DY
U69A 5 OF 6
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE
ICH_RTCX1 AG25 RTCX1
ICH_RTCX2 AF24 RTCX2
ICH_RTCRST# AF23 RTCRST#
SM_INTRUDER# AD22 INTRUDER#
ICH_INTVRMEN AF25 INTVRMEN
LAN100_SLP AD21 LAN100_SLP
B24 GLAN_CLK
D22 LAN_RSTSYNC
C21 LAN_RXD0
B21 LAN_RXD1
C22 LAN_RXD2
D21 LAN_TXD0
E20 LAN_TXD1
C20 LAN_TXD2
TP56 R349 24D9R2F-L-GP 1D5V_SB_S0 GLAN_COMP
AH21 GLAN_DOCK#/GPIO13
D25 GLAN_COMPI
C25 GLAN_COMPO
<32> HDA_BITCLK_CODEC R500 39R2J-L-GP ACZ_BCLK AJ16 HDA_BIT_CLK
<32> HDA_SYNC_CODEC R501 39R2J-L-GP ACZ_SYNC AJ15 HDA_SYNC
<32> HDA_RST#_CODEC R487 39R2J-L-GP ACZ_RST_R# AE14 HDA_RST#
<32> HDA_SDIN1 AJ17 HDA_SDIN0
AH17 HDA_SDIN1
AH15 HDA_SDIN2
AD13 HDA_SDIN3
<32> HDA_SDOUT_CODEC R488 39R2J-L-GP ACZ_SDOUT AE13 HDA_SDOUT
G5 GAP-OPEN TP61 AE10 HDA_DOCK_EN#/GPIO33
AG14 HDA_DOCK_RST#/GPIO34
<54> SATA_LED# AE10 SATALED#
<25> SATA_RXN0_C AF6 SATA0RXN
<25> SATA_RXP0_C AF5 SATA0RXP
<25,57> SATA_TXN0 C738 SC3900P50V2KX-2GP SATA_TXN0_C AH5 SATA0TXN
<25,57> SATA_TXP0 C737 SC3900P50V2KX-2GP SATA_TXP0_C AH6 SATA0TXP
AG3 SATA1RXN
AG4 SATA1RXP
AJ4 SATA1TXN
AJ3 SATA1TXP
AF2 SATA2RXN
AF1 SATA2RXP
AE4 SATA2TXN
AE3 SATA2TXP
<3> CLK_PCIE_SATA# AB7 SATA_CLKN
<3> CLK_PCIE_SATA AC6 SATA_CLKP
R506 24D9R2F-L-GP Within 500 mils
AG1 SATARBIAS#
AG2 SATARBIAS
ICH8-M-1-GP-U
FWH0/LAD0 E5 LPC_LAD0
FWH1/LAD1 F5 LPC_LAD1
FWH2/LAD2 G8 LPC_LAD2
FWH3/LAD3 F6 LPC_LAD3
LPC_LAD[0..3] <35,55>
FWH4/LFRAME# C4 LPC_FRAME#
LPC_FRAME# <35,55>
LDRQ0# G9 LPC_DRQ0#
LDRQ1#/GPIO23 E6
TP76
TP80
A20GATE AF13 KBGA20 <55>
A20M# AG26 H_A20M# <4>
DPRSTP# AF26 H_DPRSTP# <4,10,36>
DPSLP# AE26 H_DPSLP# <4>
FERR# AD24 H_FERR# <4>
CPUPWRGD/GPIO49 AG29 H_PWRGOOD <4>
IGNNE# AF27 H_IGNNE# <4>
INIT# AE24 H_INIT# <4>
INTR AC20 H_INTR <4>
RCIN# AH14 KBRST# <55>
NMI AD23 H_NMI <4>
SMI# AG28 H_SMI# <4>
STPCLK# AA24 H_STPCLK# <4>
THRMTRIP# AE27 THRMTRIP_ICH#
R507 24R2J-GP
H_THERMTRIP# <4,10>
TP8 AA23
DD0 V1 IDE_PDD0
DD1 U2 IDE_PDD1
DD2 V3 IDE_PDD2
DD3 T1 IDE_PDD3
DD4 V4 IDE_PDD4
DD5 T5 IDE_PDD5
DD6 AB2 IDE_PDD6
DD7 T6 IDE_PDD7
DD8 T3 IDE_PDD8
DD9 R2 IDE_PDD9
DD10 T4 IDE_PDD10
DD11 V6 IDE_PDD11
DD12 V5 IDE_PDD12
DD13 U1 IDE_PDD13
DD14 V2 IDE_PDD14
DD15 U6 IDE_PDD15
IDE_PDD[0..15] <25>
DA0 AA4 IDE_PDA0 <25>
DA1 AA1 IDE_PDA1 <25>
DA2 AB3 IDE_PDA2 <25>
DCS1# Y6 IDE_PDCS1# <25>
DCS3# Y5 IDE_PDCS3# <25>
DIOR# W4 IDE_PDIOR# <25>
DIOW# W3 IDE_PDIOW# <25>
DDACK# Y2 IDE_PDDACK# <25>
IDEIRQ Y3 INT_IRQ14 <25>
IORDY Y1 IDE_PDIORDY <25>
DDREQ W5 IDE_PDDREQ <25>
3D3V_S0
RN88 SRN10KJ-5-GP
KBGA20
KBRST#
1D05V_S0
R309 56R2J-4-GP H_FERR#
H_DPRSTP# TP59
H_DPSLP# TP67
within 2" from R184
R509 56R2J-4-GP
placed within 2" from ICH8M
IDE_PDIORDY R511 4K7R2J-2-GP
INT_IRQ14 R508 8K2R2J-3-GP
+RTCVCC
W=20mils
R236 100R2J-2-GP
W=20mils
C433 SC1U10V3ZY-6GP
3D3V_AUX_S5
U34 CH715FPT-GP
BAT_RTC
R211 1KR2J-1-GP
W=20mils
W=20mils
CN7 MLX-SSW-SN3-7-GP
XOR CHAIN ENTRANCE STRAP : RSVD
3D3V_S0
R489 1KR2J-1-GP HDA_SDOUT_CODEC
DY
A-NOTE2
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size A3
Document Number
Anote2.0 INTEL
Rev -1
Date: Thursday, March 22, 2007
Sheet 21 of 56

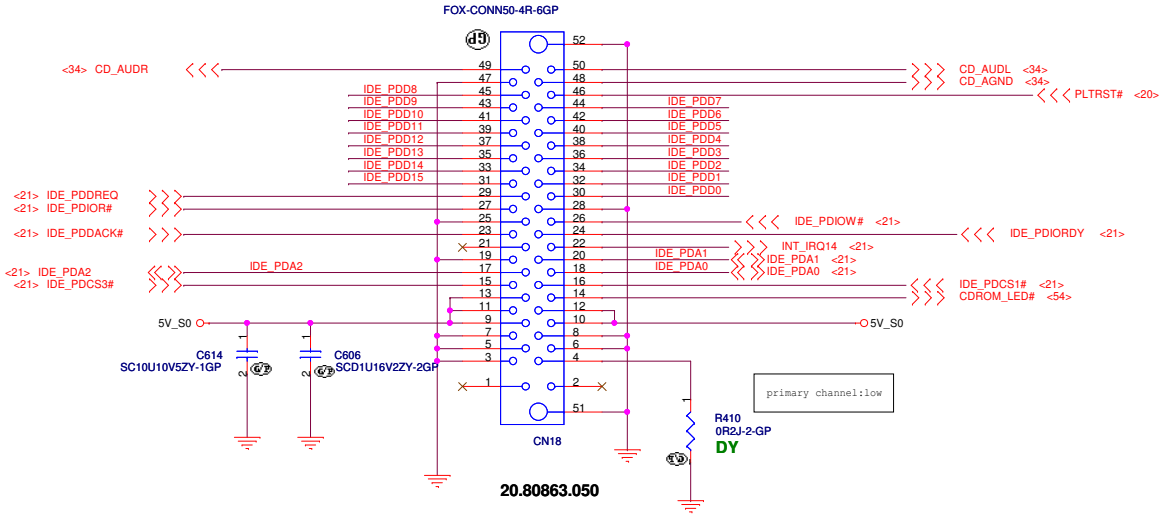

Place closely pin G5
Place closely pin AG9
CLK_48M_ICH
CLK_14M_ICH
R339 10R2J-2-GP DY
C530 SC4D7P50V2CN-1GP DY
R495 10R2J-2-GP DY
C733 SC4D7P50V2CN-1GP DY
RN72 GPIO22 PM_CLKRUN# CLKSATAREQ# THERM_SCI# SRN10KJ-6-GP
RN87 SRN2K2J-1-GP
U69D 4 OF 6
SMB_CLK SMB_DATA SMB_LINK_ALERT# SMLINK0 SMLINK1
ICH_RI#
TP82 TP81 sys_reset
RN74 SRN2K2J-1-GP
PM_BMBUSY# <10>
OCP# <4>
H_STP_PCI# <3>
H_STP_CPU# <3>
PM_CLKRUN# <27,55>
PCIE_WAKE# <29,30,31,57,58>
INT_SERIRQ <27,55>
THERM_SCI#
VGATE_PWRGD <10,36>
R493 0R2J-2-GP DY
VRMPWRGD
TP102 SST_CTL
TP101 GPIO1
ECSCI# <55>
ECSMI# <55>
EC_SWI# <55>
TP60 GPIO17 NEWCARD_RST# <31>
TP64 GPIO20 GPIO22
TP58 TP69 CLKSATAREQ# <3>
TP62 GPIO39
TP100 IDE_RESET#
TP68
SB_SPKR <32>
MCH_ICH_SYNC# <10>
ICH_RSVD
TP3
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
GPIO37
CLK14
CLK48
SUSCLK
SLP_S3# SLP_S4# SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0 CL_CLK1
CL_DATA0 CL_DATA1
CL_VREF0 CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
CLGPIO3/GPIO9
ICH8-M-1-GP-U
RN71 SRN10KJ-6-GP
SATA0_R0 SATA0_R1 SATA0_R2 SATA0_R3
CLK_14M_ICH CLK_48M_ICH
ICH_SUSCLK
PM_SLP_S3# <40,45>
PM_SLP_S5# <31,40,55>
GPIO26
PM_PWROK <10,24>
DPRSLPVR <10,36>
PM_BATLOW#_R
SB_PWR_BTN# <55>
R497 100R2J-2-GP
R537 0R0402-PAD
CK_PWRGD_R
CK_PWRGD <3>
R496 DY 10KR2J-3-GP
SB_RSMRST# <55>
CL_CLK <10>
CL_DATA <10>
CL_RST# <10>
LAN_DISABLE <30>
TP57 TP63 TP55
R351 3K24R2F-GP
R352 453R2F-1-GP
C545 SCD1U16V2KX-3GP
R491 3K24R2F-GP
R490 453R2F-1-GP
C731 SCD1U16V2KX-3GP
ver:sc modify to S5
3V_S5
RN75 GPIO26 PM_BATLOW# R SMB_LINK_ALERT# SRN10KJ-6-GP
RN73 OCP# SMLINK1 PCIE_WAKE# USB_OC#9 SRN10KJ-6-GP
R502 DPRSLPVR 100KR2J-1-GP
R499 DY ICH_RSVD 1KR2J-1-GP
32K suspend clock output
R482 10KR2J-3-GP
U60C
ICH_SUSCLK
32KHZ
R484 10R2J-2-GP
G792_CLK <24>
SSLVC08APWR-GP
R303 DY 10KR2J-3-GP
SB_SPKR
Low--> default
High--> No boot
New Card
LAN
Mini Card 1
U69B 2 OF 6
PCI-Express
Direct Media Interface
PCIE_RXN1 <31>
PCIE_RXP1 <31>
PCIE_TXN1 <31,57>
PCIE_TXP1 <31,57>
SCD1U16V2KX-3GP
C771 C773
PCIE_C_TXN1
PCIE_C_TXP1
PCIE_RXN2 <30>
PCIE_RXP2 <30>
PCIE_TXN2 <30>
PCIE_TXP2 <30>
C774 C776
PCIE_C_TXN2
PCIE_C_TXP2
PCIE_RXN3 <29,58>
PCIE_RXP3 <29,58>
PCIE_TXN3 <29,58>
PCIE_TXP3 <29,58>
C777 C780
PCIE_C_TXN3
PCIE_C_TXP3
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0
DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1
DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2
DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3
DMI_CLKN DMI_CLKP
CLK_PCIE_ICH# <3>
CLK_PCIE_ICH <3>
DMI_ZCOMP DMI_IRCOMP
R512 24D9R2F-L-GP
Within 500 mils
1D5V_SB_S0
SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO
SPI_CS1# <20>
USB
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P
USB_PN0 <26> USB_PP0 <26> USB0
USB_PN1 <26> USB_PP1 <26> USB1
USB_PN2 <26> USB_PP2 <26> USB2
USB_PN3 <26> USB_PP3 <26> USB3
USB_PN4 <19,58> USB_PP4 <19,58> CAMERA
USB_PN5 <31,57> USB_PP5 <31,57> New Card
USB_PN6_BT <29,58> USB_PP6_BT <29,58> BT
USB_PN7 <54,57> USB_PP7 <54,57> Finger Printer
USB_PN8 <29,58> USB_PP8 <29,58> WIRELESS
USB20_N9 USB20_P9
TP73 TP72
USBRBIAS USBRBIAS# R535 22D6R2F-L1-GP
Within 500 mils
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#
USB_SYSTEM_OC0# <26>
USB_SYSTEM_OC1# <26>
USB_SYSTEM_OC2# <26>
USB_SYSTEM_OC3# <26>
USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9
ICH8-M-1-GP-U
RN68 SRN2K2J-1-GP
R492 10KR2F-2-GP
U63
ICH_SMBDATA <3,15,16>
SMB_CLK <29,30,31,57,58>
SMB_DATA <29,30,31,57,58>
ICH_SMBCLK <3,15,16>
2N7002DW-7F-GP
RN86 USB_OC#4 USB_OC#5 SRN10KJ-6-GP
RN70 SMLINK0 ECSMI# ICH_RI# USB_OC#7 SRN10KJ-6-GP
RN69 USB_OC#6 USB_OC#8 sys_reset SRN10KJ-6-GP
R296 330R2J-3-GP
R295 0R2J-2-GP DY CK_PWRGD
R297 0R0402-PAD VRMPWRGD
Q13 2N7002PT-U
CLK_EN# <36>
A-NOTE2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(3/4) PM,USB,GPIO
Size Custom
Document Number
Anote2.0 INTEL
Rev -1
Date: Thursday, March 22, 2007
Sheet 22 of 56


+RTCVCC
20 mils
C488
C751
SCD1U16V2ZY-2GP
ICH_V5REF_RUN
ICH_V5REF_SUS
1D5V_SB_S0
U69E 5 OF 6
VCCRTC
V5REF
V5REF_SUS
VCCA3GP
CORE
VCCDMIPLL
VCC_DMI
V_CPU_IO
VCC3_3
VCCP CORE
IDE
PCI
VCCHDA
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCPSUS
VCCPUSB
VCCSUSPLL
VCCUSBPLL
USB CORE
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
GLAN POWER
VCCCL1_05
VCCCL3_3
VCCSATAPLL
ATX
ARX
ICH8-M-1-GP-U
1D05V_S0
1D25V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
R523
100R2J-2-GP
D22
CH751H-40PT-1GP
20 mils
C764
SCD1U16V2ZY-2GP
R525
D23
C769
DY
TC31
ST100U4VBM-1-GP
C782
C528
C513
SC10U6D3V5MX-3GP
SC22D2U6D3V5MX-1GP
C506
C518
C755
C507
SCD01U16V2KX-3GP
SC10U6D3V5MX-3GP
C745
SC22U6D3V5MX-2GP
C521
C505
C542
SC4D7U6D3V3KX-GP
C484
(DMI)
C486
(SATA)
C502
C547
C534
C549
C735
C736
C487
C491
C496
C495
C480
C494
C779
C519
C535
L40
BLM18PG121SN-1GP
C793
C795
SC22D2U10V3KX-GP
SCA7U1V2ZY-3GP
C758
SC4D7U6D3V3KX-GP
C794
SC1U10V3ZY-6GP
TP74
TP66
TP71
TP75
TP78
TP79
TP77
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
VCCCL1_05_ICH
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
U69F 6 OF 6
ICH8-M-1-GP-U
ICHGND1
ICHGND2
ICHGND3
ICHGND4
R542
R548
R504
R541
0R2J-2-GP
TP65
TPAD28
-1 modify
A-NOTE2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
Anote2.0 INTEL
Rev
-1
Date: Thursday, March 22, 2007
Sheet 23 of 56


5V_S0
FAN1_VCC
FAN1_FG1 <57>
R155
10KR2J-3-GP
CN16
FOX-CGN3-6-GP
FAN1_FG1
Layout 20 mil
20.D0210.103
C232
SC1000P50V2JN-GP
C579
SCD1U16V2ZY-2GP
C576
SC10U10V3ZY-1GP
Layout 30 mil
R159
200R2F-L-GP
C233
SC1U10V3ZY-6GP
R154
43KR2F-GP
C149
SC4D7U10V5ZY-3GP
C157
SCD1U16V2ZY-2GP
5V_G792_S0
U22
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
G792_SDA
G792_SCL
G792_CLK <22>
H_THERMDA <4>
H_THERMDC <4>
C229
SC2200P50V2KX-2GP
DX PORT1
HW_THRM_SHDN#
R113
0R2J-2-GP
THERM#
V_DEGREE
Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
R153
100KR2F-L1-GP
3D3V_S0_RST
G792_DXP2
Q20
PMBS3904-1-GP
C214
SC2200P50V2KX-2GP
DX PORT2
<10,22> PM_PWROK
PM_SLP_S3_1# <45,55>
G792_RST#
U60D
SSLVC08APWR-GP
R498
10KR2J-3-GP
R152
100KR2J-1-GP
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
G792_DXN2
G3
GAP-CLOSE
Place near chip as close
as possible
220ms delay time after Power-on
NV_THERMDA <50>
C150
0R2J-2-GP
2200P in DIS
DX PORT3
NV_THERMDC <50>
Please close to the GPU
3D3V_S0
RN19
G792_SCL
G792_SDA
SRN10KJ-5-GP
3D3V_AUX_S5
R52
10KR2J-3-GP
R51
100KR2J-1-GP
D7
<45> HW_THRM_SHDN#
<55> S5_ENABLE
CHP222PT-U
PWR_S5_EN <45>
C60
SCD1U10V2KX-4GP
DY
U18
THER_SDA <55>
<55> THER_SCL
2N7002DW-7F-GP
A-NOTE2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor G792
Size
Custom
Document Number
Anote2.0 INTEL
Rev
-1
Date: Thursday, March 22, 2007
Sheet 24 of 56

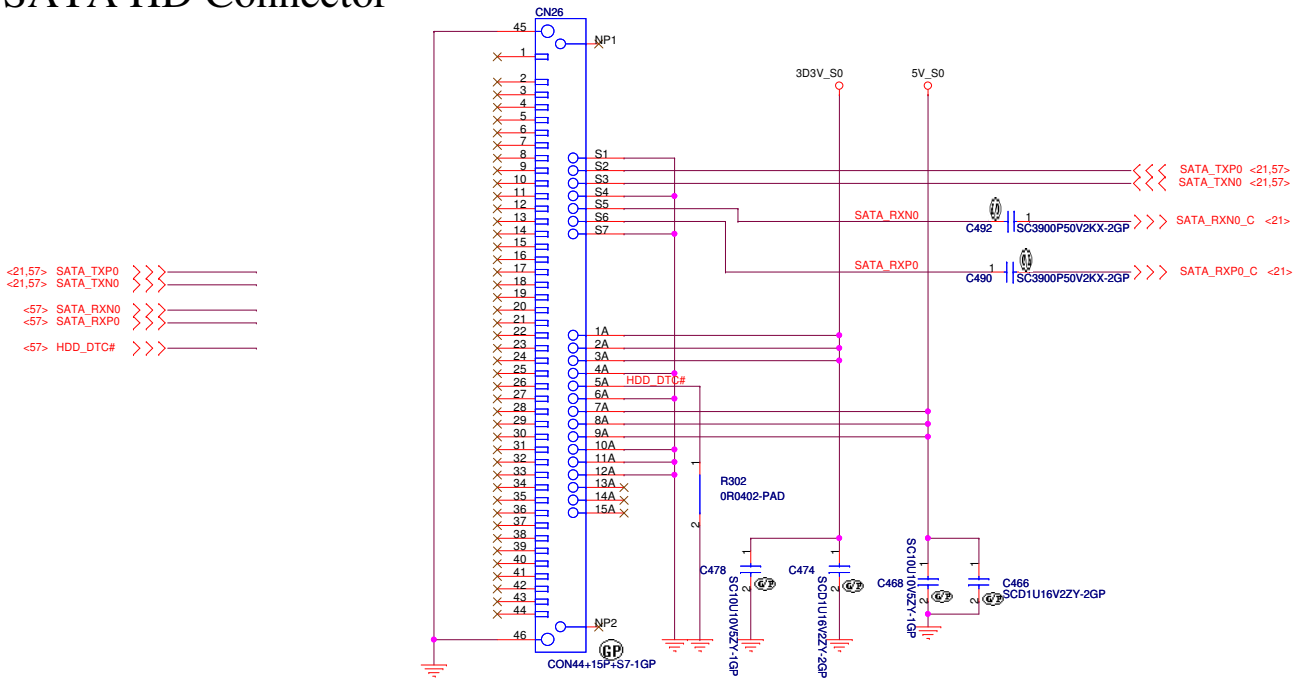
CD-ROM CONNECTOR

Lab1 20.80346.050
Lab2 20.80863.050



20.80863.050

SATA HD Connector



20.F0883.001

A-NOTE2

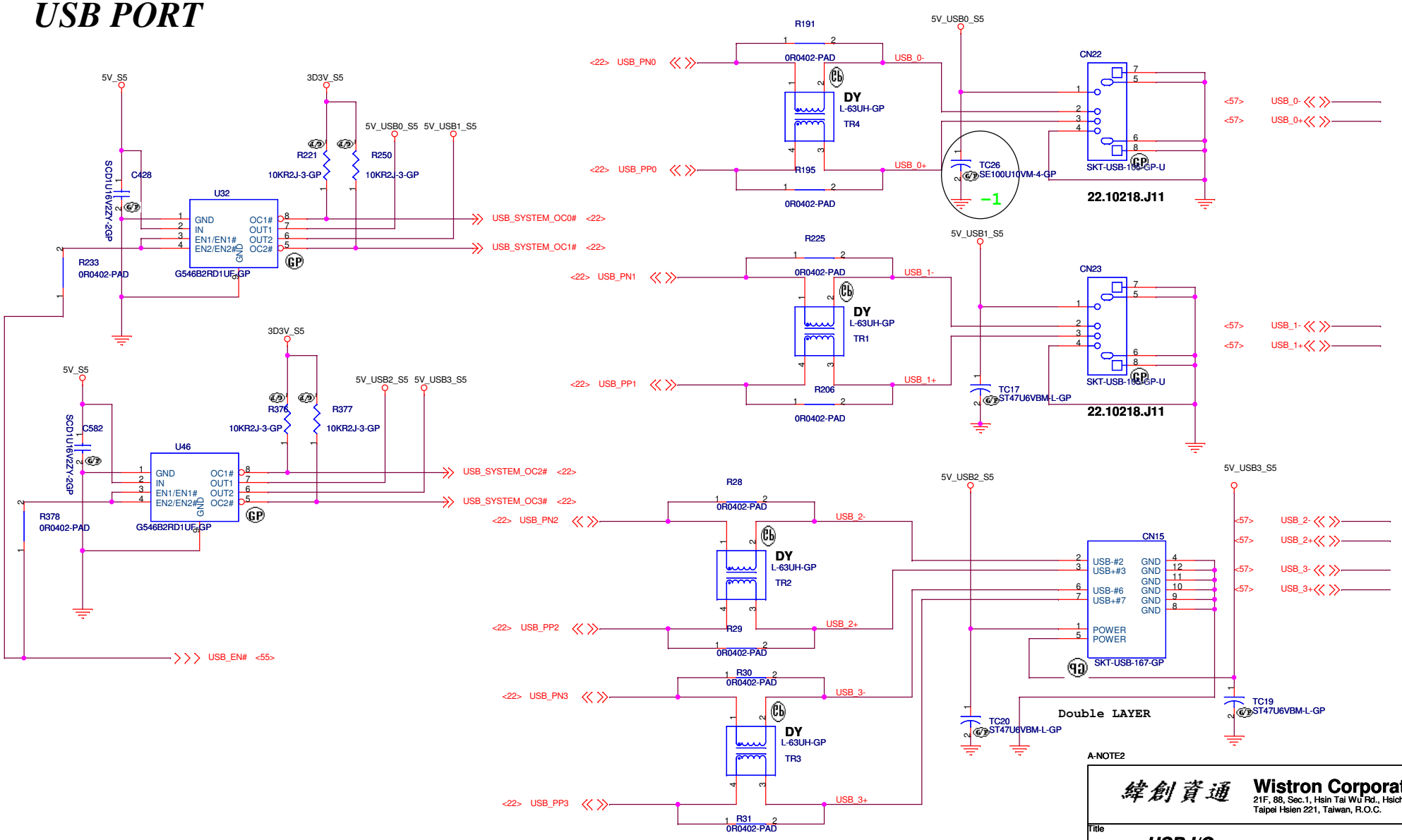
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HD/CDROM/USB

Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 25 of 56

USB PORT

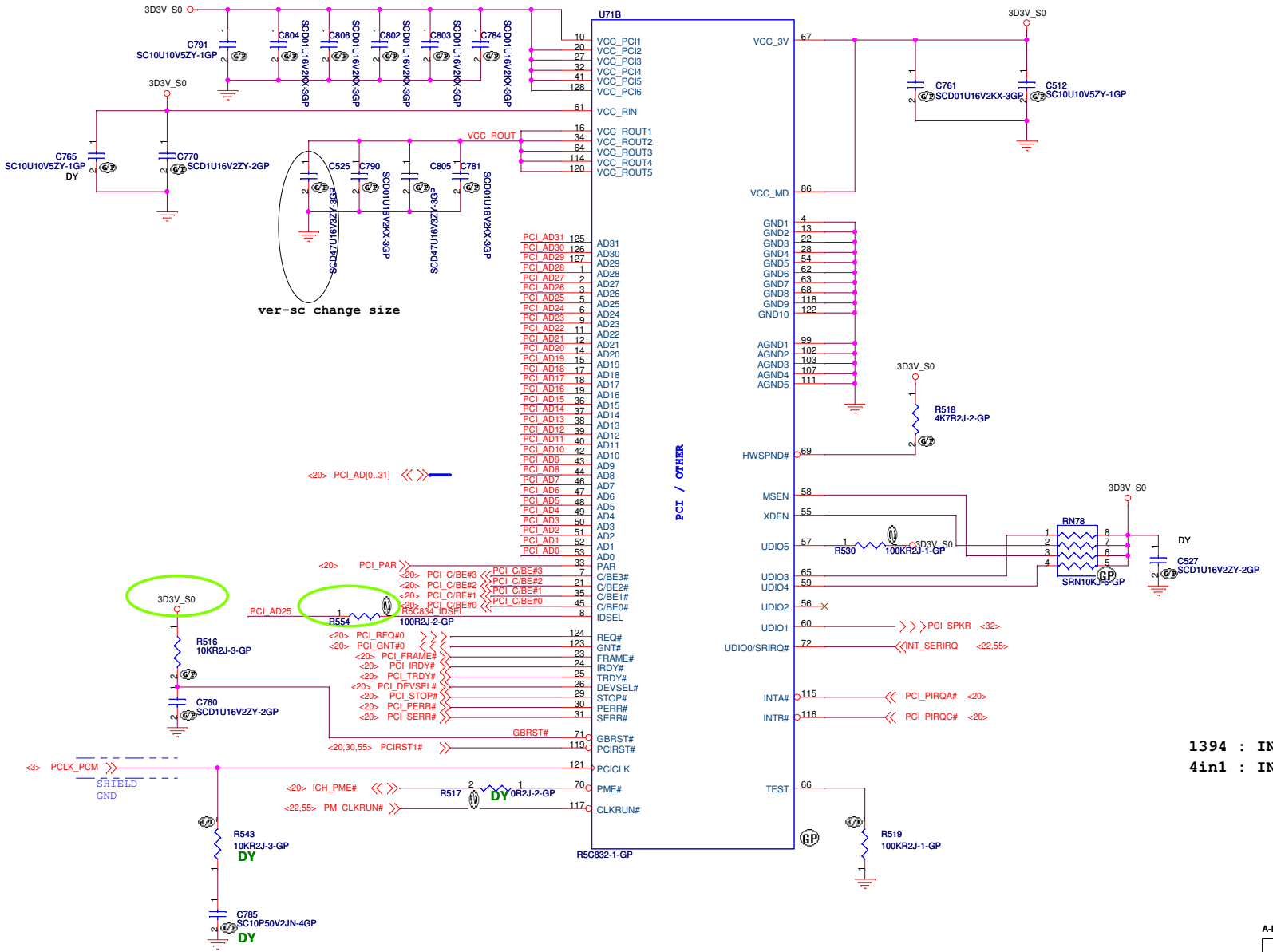


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB I/O**

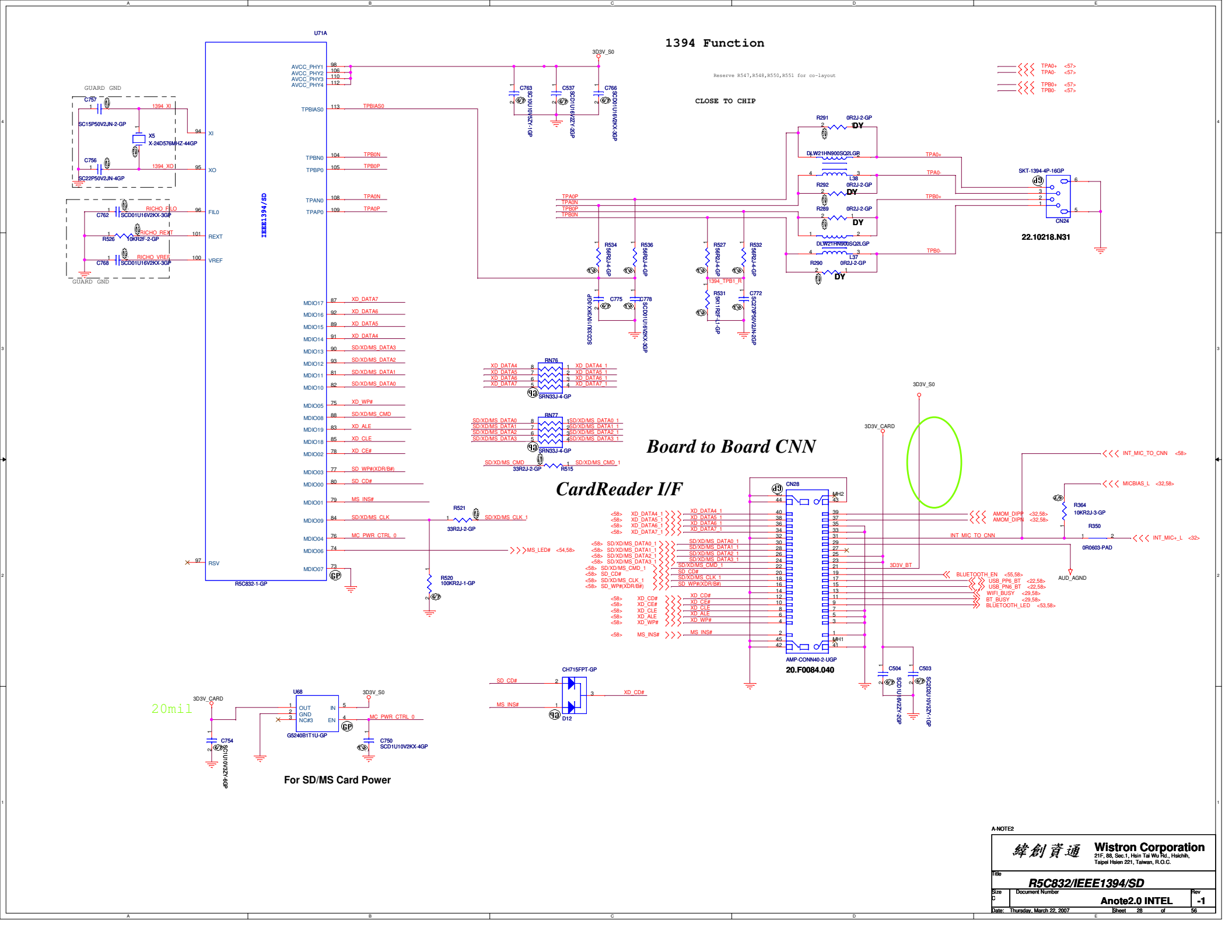
Size	Document Number	Rev
B	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 26 of 56



A-NOTE2

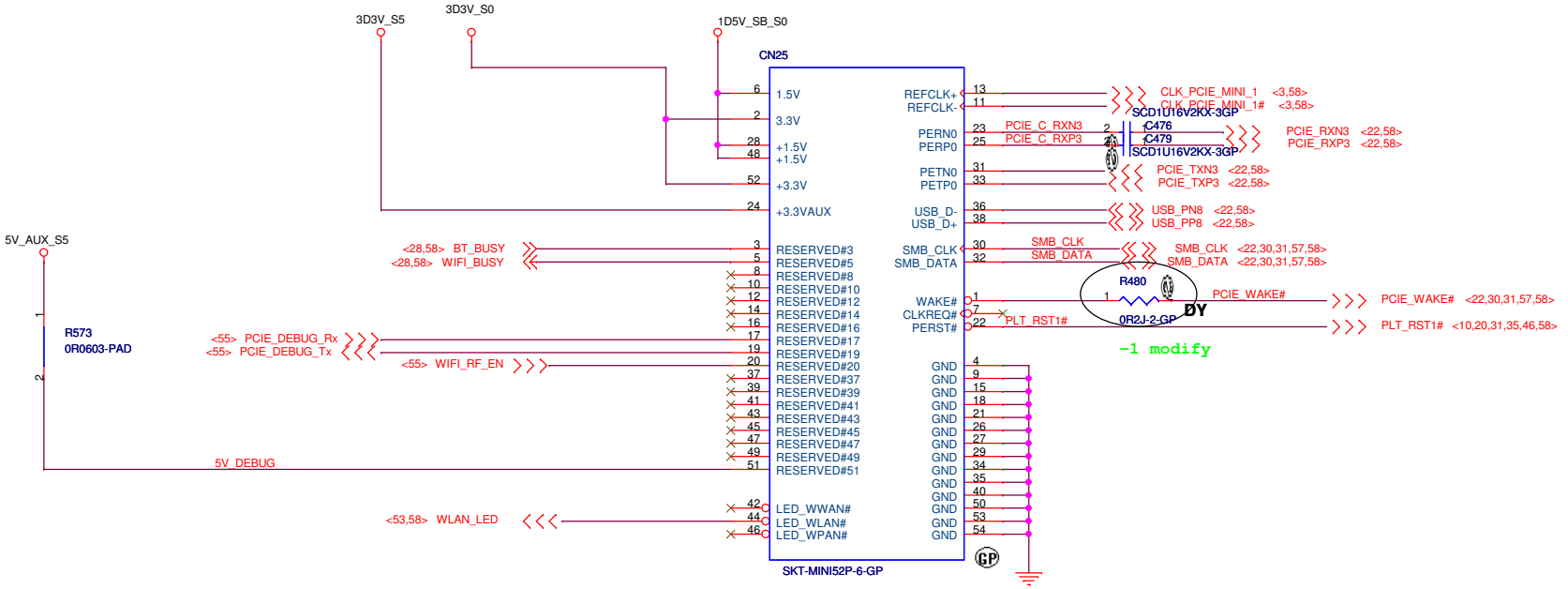
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: R5C832/PCI	
Size: A3	Document Number: Anote2.0 INTEL
Rev: -1	
Date: Thursday, March 22, 2007	Sheet 27 of 56


1394 Function
Reserve R547,R548,R550,R551 for co-layout
CLOSE TO CHIP
U71A
R5C832-1-GP
IEEE1394/SD
GUARD GND
C757
1394_XI
SC15P50V2JN-2-GP
X5
X-24D576MHZ-44GP
C756
1394_XO
SC22P50V2JN-4GP
C762
RICHO_FIL0
SCD01U16V2KX-3GP
R526
10KR2F-2-GP
RICHO_REXT
C768
RICHO_VREF
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
XI
XO
FIL0
REXT
VREF
RSV
3D3V_S0
C763
C537
C766
SCD1U16V2ZY-2GP
SCD1U16V2KX-3GP
TPA0+ <57>
TPA0- <57>
TPB0+ <57>
TPB0- <57>
R291 0R2J-2-GP DY
DLW21HN900SQ2LGP
L36
R292 0R2J-2-GP DY
R289 0R2J-2-GP DY
DLW21HN900SQ2LGP
L37
R290 0R2J-2-GP DY
SKT-1394-4P-16GP
CN24
22.10218.N31
R534 56R2J-4-GP
R536 56R2J-4-GP
R527 56R2J-4-GP
R532 56R2J-4-GP
1394_TPB1_R
R531 5K1FR2F-1-GP
C775
C778
C772
SC27P50V2JN-2GP
SCD01U16V2KX-3GP
MDIO17 XD_DATA7
MDIO16 XD_DATA6
MDIO15 XD_DATA5
MDIO14 XD_DATA4
MDIO13 SD/XD/MS_DATA3
MDIO12 SD/XD/MS_DATA2
MDIO11 SD/XD/MS_DATA1
MDIO10 SD/XD/MS_DATA0
MDIO05 XD_WP#
MDIO08 SD/XD/MS_CMD
MDIO19 XD_ALE
MDIO18 XD_CLE
MDIO02 XD_CE#
MDIO03 SD_WP#(XDR/B#)
MDIO00 SD_CD#
MDIO01 MS_INS#
MDIO09 SD/XD/MS_CLK
MDIO04 MC_PWR_CTRL_0
MDIO06
MDIO07
R521 33R2J-2-GP
SD/XD/MS_CLK_1
MS_LED# <54,58>
R520 100KR2J-1-GP
RN76 SRN33J-4-GP
XD_DATA4 XD_DATA5 XD_DATA6 XD_DATA7
XD_DATA4_1 XD_DATA5_1 XD_DATA6_1 XD_DATA7_1
RN77 SRN33J-4-GP
SD/XD/MS_DATA0 SD/XD/MS_DATA1 SD/XD/MS_DATA2 SD/XD/MS_DATA3
SD/XD/MS_DATA0_1 SD/XD/MS_DATA1_1 SD/XD/MS_DATA2_1 SD/XD/MS_DATA3_1
SD/XD/MS_CMD
SD/XD/MS_CMD_1
R515 33R2J-2-GP
Board to Board CNN
CardReader I/F
3D3V_S0
3D3V_CARD
CN28
AMP-CONN40-2-UGP
20.F0084.040
XD_DATA4_1 XD_DATA5_1 XD_DATA6_1 XD_DATA7_1
SD/XD/MS_DATA0_1 SD/XD/MS_DATA1_1 SD/XD/MS_DATA2_1 SD/XD/MS_DATA3_1
SD/XD/MS_CMD_1
SD_CD#
SD/XD/MS_CLK_1
SD_WP#(XDR/B#)
XD_CD# XD_CE# XD_CLE XD_ALE XD_WP#
MS_INS#
AMOM_DIPP <32,58>
AMOM_DIPN <32,58>
INT_MIC_TO_CNN <58>
MICBIAS_L <32,58>
R364 10KR2J-3-GP
R350 0R0603-PAD
INT_MIC+_L <32>
3D3V_BT
BLUETOOTH_EN <55,58>
USB_PP6_BT <22,58>
USB_PN6_BT <22,58>
WIFI_BUSY <29,58>
BT_BUSY <29,58>
BLUETOOTH_LED <53,58>
AUD_AGND
C504 SCD1U16V2ZY-2GP
C503 SC2R2U10V2ZY-1GP
CH715FPT-GP
D12
SD_CD#
MS_INS#
XD_CD#
U68
G5240B1T1U-GP
OUT GND NC#3 IN EN
MC_PWR_CTRL_0
C754 SCD1U10V2ZY-6GP
C750 SCD1U10V2KX-4GP
20mil
For SD/MS Card Power
A-NOTE2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size C
Document Number
Anote2.0 INTEL
Rev -1
Date: Thursday, March 22, 2007
Sheet 28 of 56

Mini PCI-E Connector

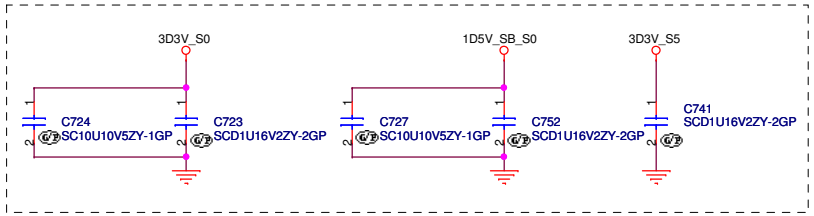
Port-1

Only port-1 support USB



62.10043.261

Note: 9/5 ME updata



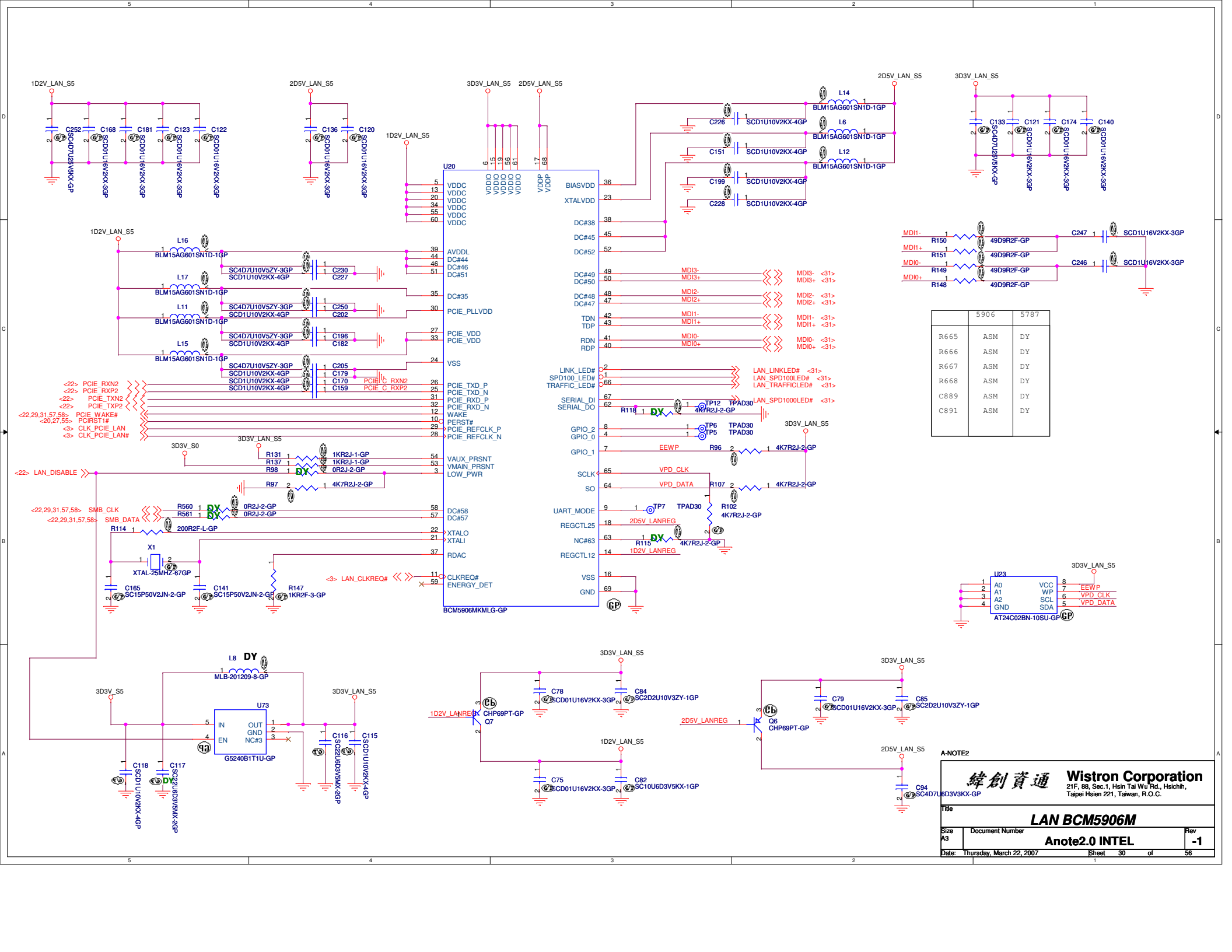
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size: B | Document Number: Anote2.0 INTEL | Rev: -1

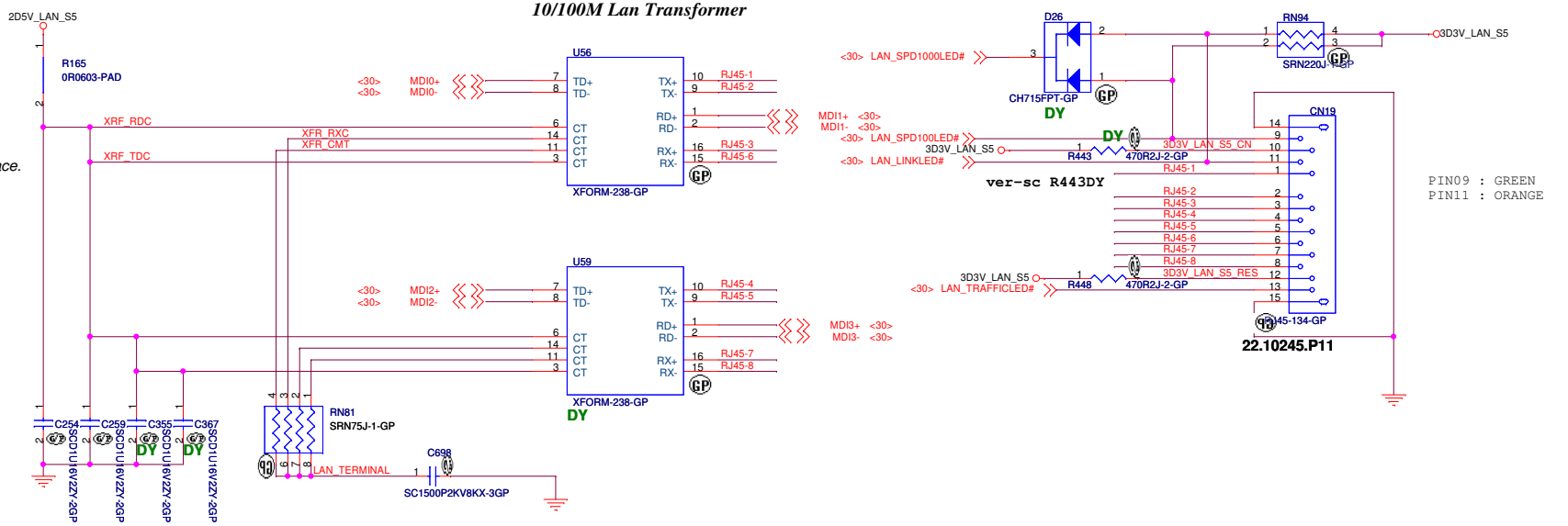
Date: Thursday, March 22, 2007 | Sheet 29 of 56



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

10/100M Lan Transformer

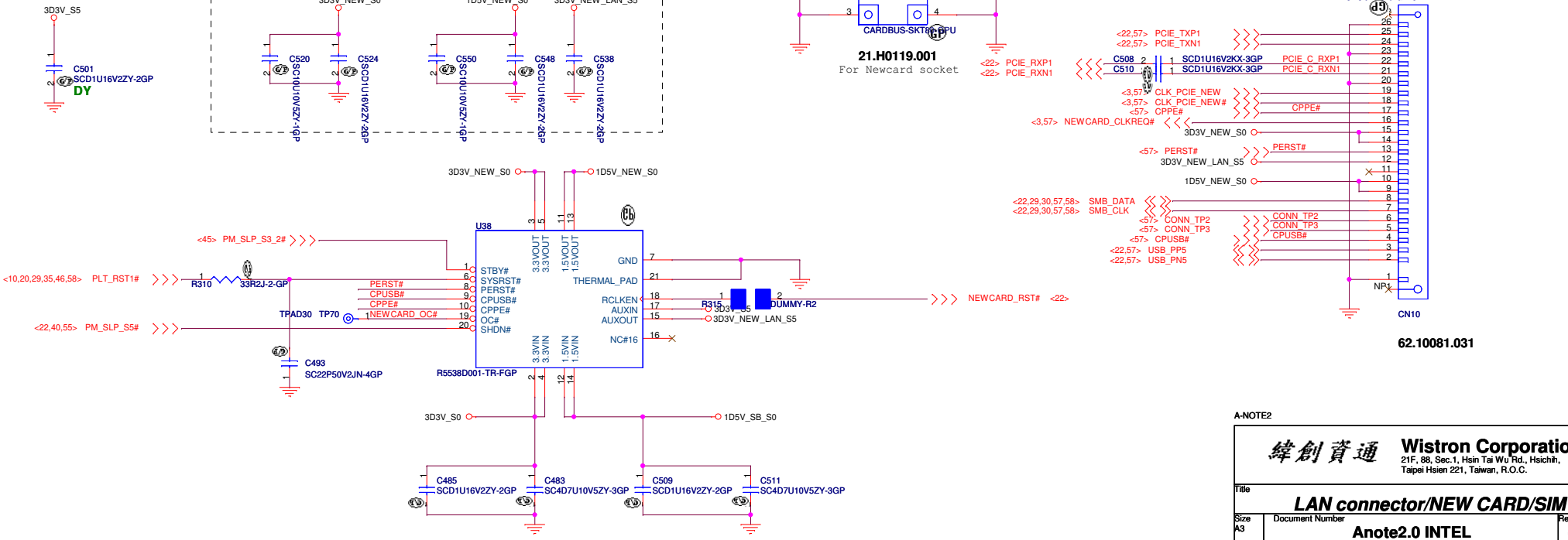
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



NEWCARD Connector

Place them Near to Chip

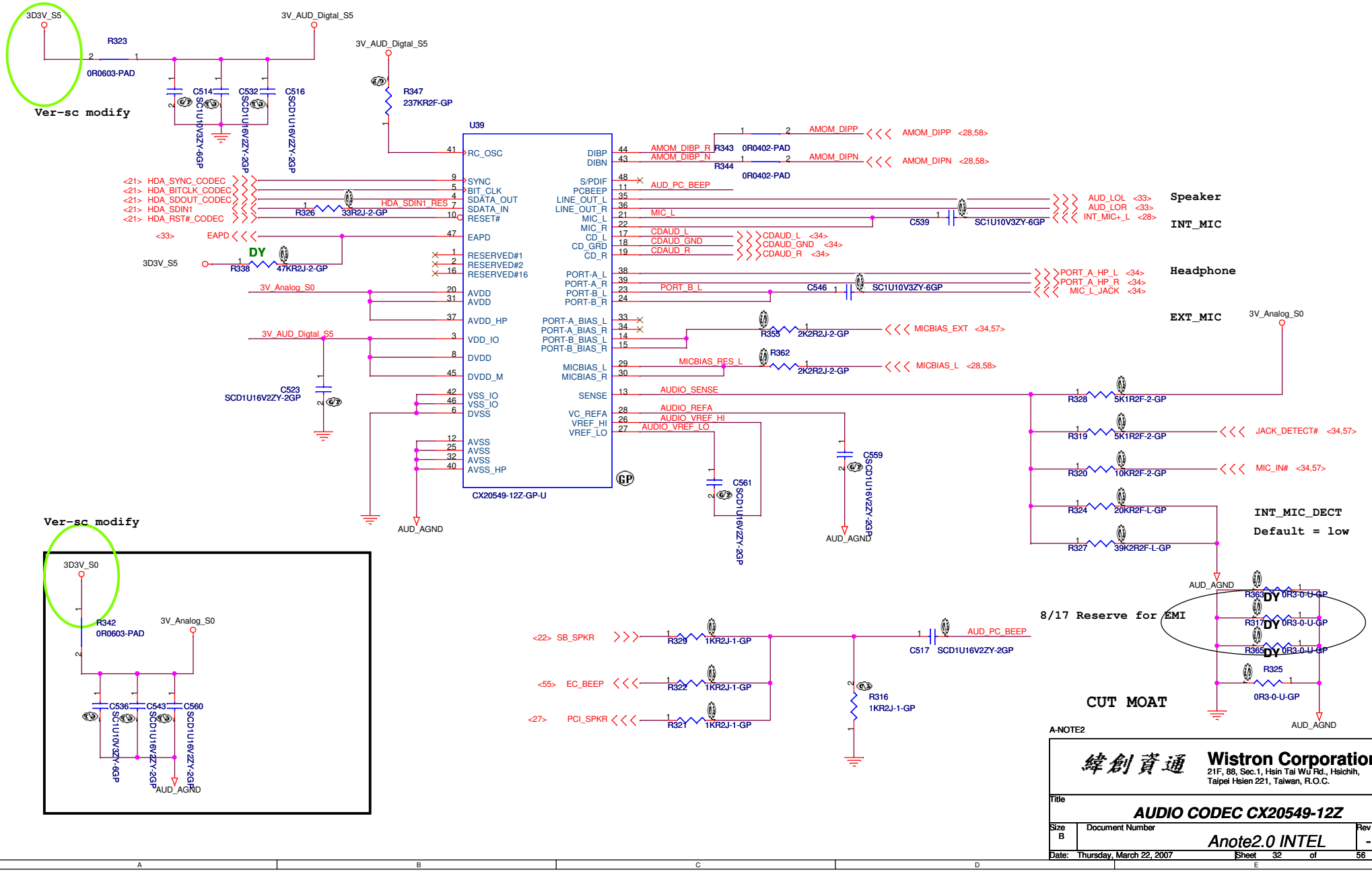
Place them Near to Connector

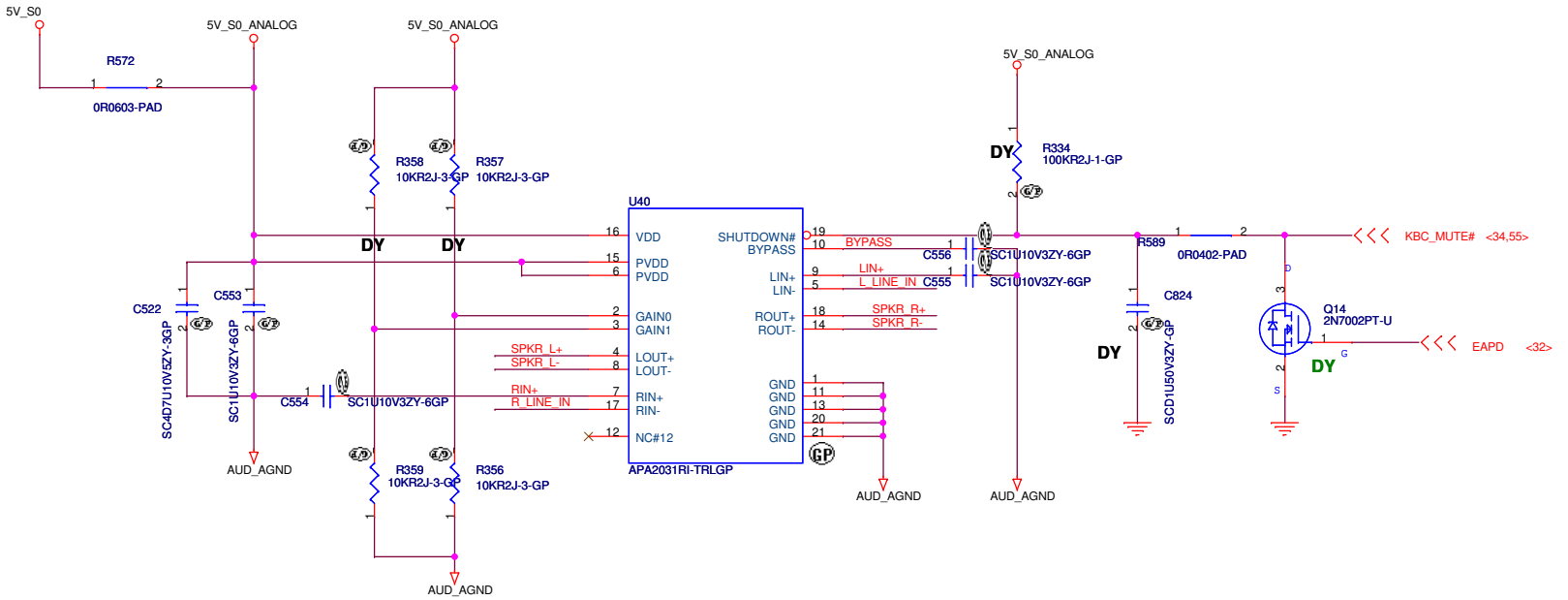


CLOSE TO TRANSFORMER

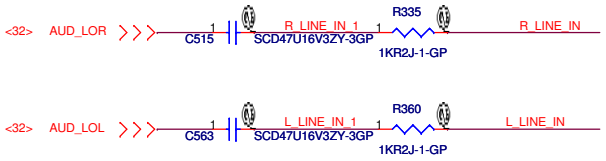
A-NOTE2

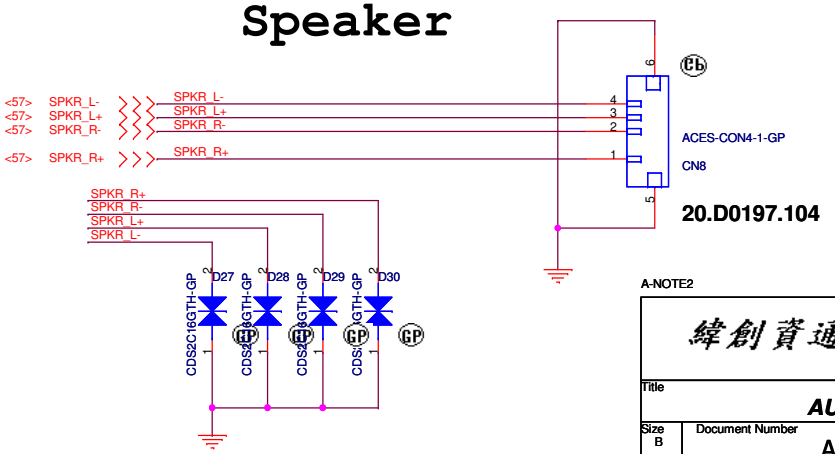
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN connector/NEW CARD/SIM
Size A3	Document Number: Anote2.0 INTEL
Rev	-1
Date: Thursday, March 22, 2007	Sheet 31 of 56


3D3V_S5
3V_AUD_Digtal_S5
R323
0R0603-PAD
Ver-sc modify
C514
C532
C516
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
R347
237KR2F-GP
U39
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
CX20549-12Z-GP-U
HDA_SYNC_CODEC
HDA_BITCLK_CODEC
HDA_SDOUT_CODEC
HDA_SDIN1
HDA_RST#_CODEC
HDA_SDIN1_RES
R326
33R2J-2-GP
DY
R338
47KR2J-2-GP
3V_Analog_S0
C523
SCD1U16V2ZY-2GP
AUD_AGND
AMOM_DIPP
AMOM_DIPN
R343
R344
0R0402-PAD
AUD_PC_BEEP
MIC_L
C539
SC1U10V3ZY-6GP
CDAUD_L
CDAUD_GND
CDAUD_R
PORT_B_L
C546
SC1U10V3ZY-6GP
R355
2K2R2J-2-GP
MICBIAS_RES_L
R362
2K2R2J-2-GP
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C561
C559
SCD1U16V2ZY-2GP
Speaker
INT_MIC
Headphone
EXT_MIC
R328
5K1R2F-2-GP
R319
5K1R2F-2-GP
R320
10KR2F-2-GP
R324
20KR2F-L-GP
R327
39K2R2F-L-GP
JACK_DETECT#
MIC_IN#
INT_MIC_DECT
Default = low
8/17 Reserve for EMI
R363
R317
R365
0R3-0-U-GP
R325
CUT MOAT
Ver-sc modify
3D3V_S0
R342
0R0603-PAD
3V_Analog_S0
C536
C543
C560
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
AUD_AGND
SB_SPKR
EC_BEEP
PCI_SPKR
R329
R322
R321
1KR2J-1-GP
C517
SCD1U16V2ZY-2GP
R316
1KR2J-1-GP
A-NOTE2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size
B
Document Number
Anote2.0 INTEL
Rev
-1
Date: Thursday, March 22, 2007
Sheet 32 of 56



Speaker





20.D0197.104

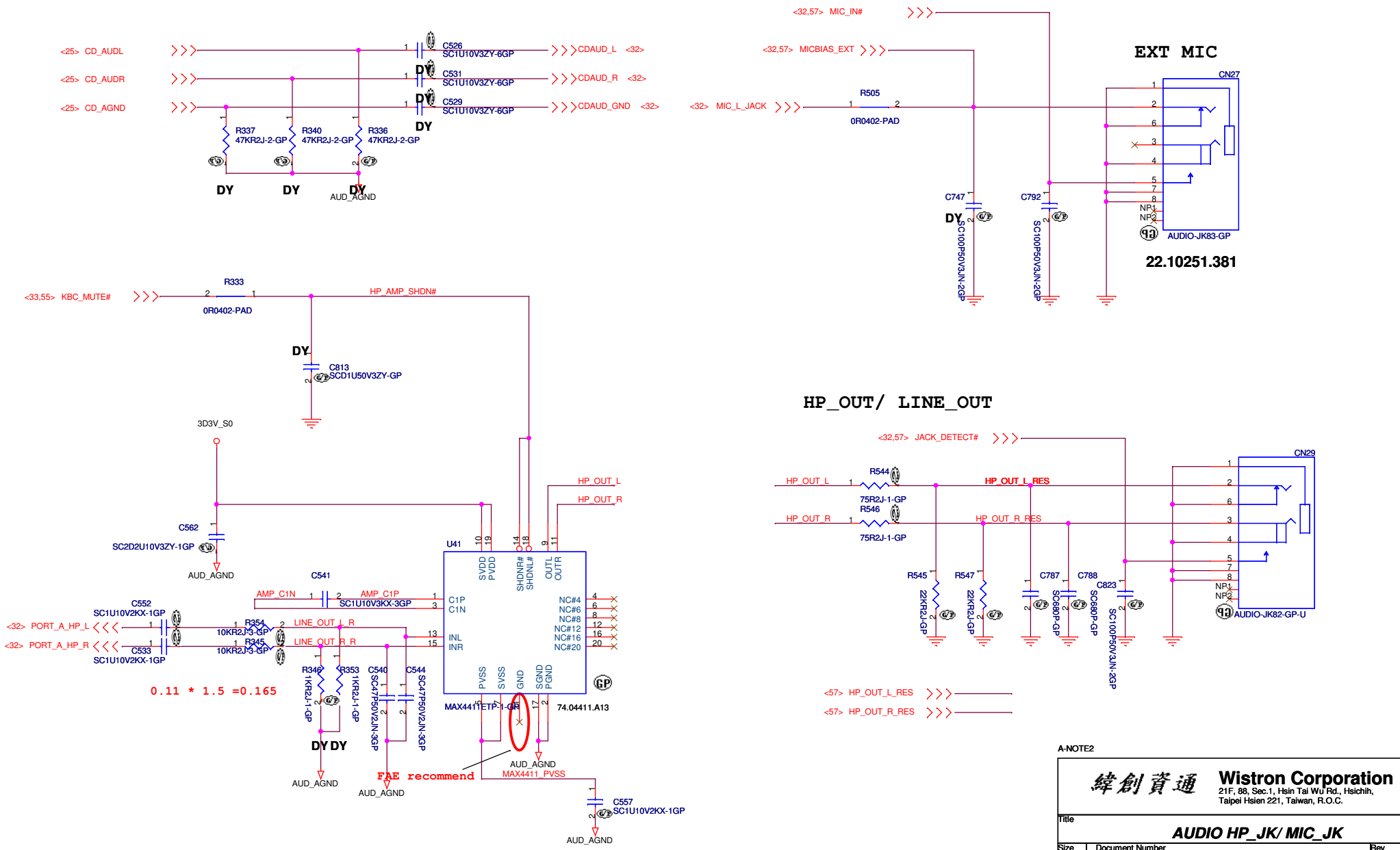
A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO AMP/SPEAKER***

Size	Document Number	Rev
B	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 33 of 56

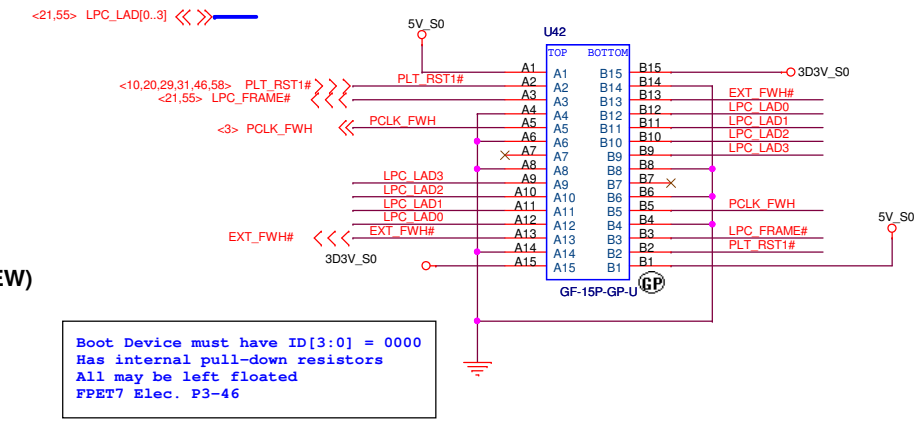

EXT MIC
HP_OUT/ LINE_OUT
0.11 * 1.5 =0.165
FAE recommend
MAX4411ETP+1-GR
74.04411.A13
22.10251.381
AUDIO-JK83-GP
AUDIO-JK82-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO HP_JK/ MIC_JK
Anote2.0 INTEL
A-NOTE2
Thursday, March 22, 2007
Sheet 34 of 56

GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

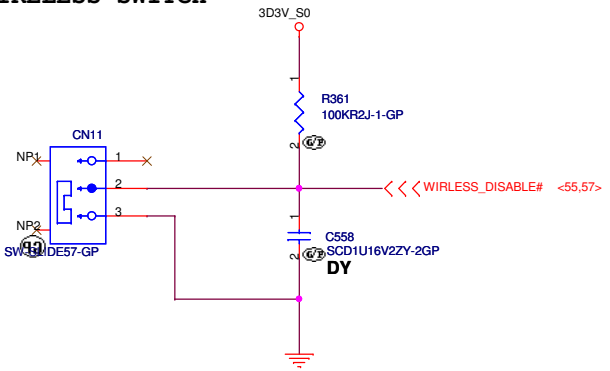
A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

WIRELESS SWITCH



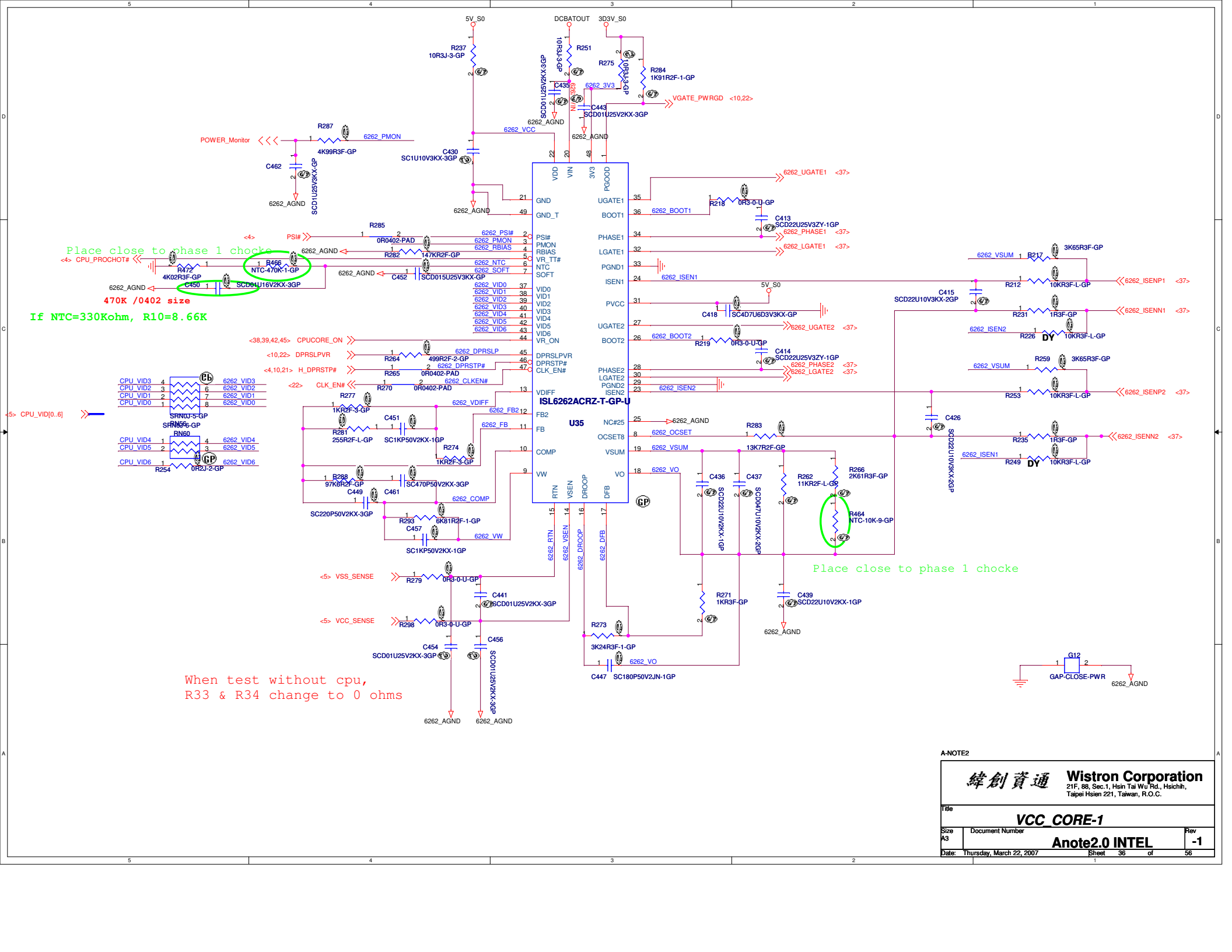
A-NOTE2

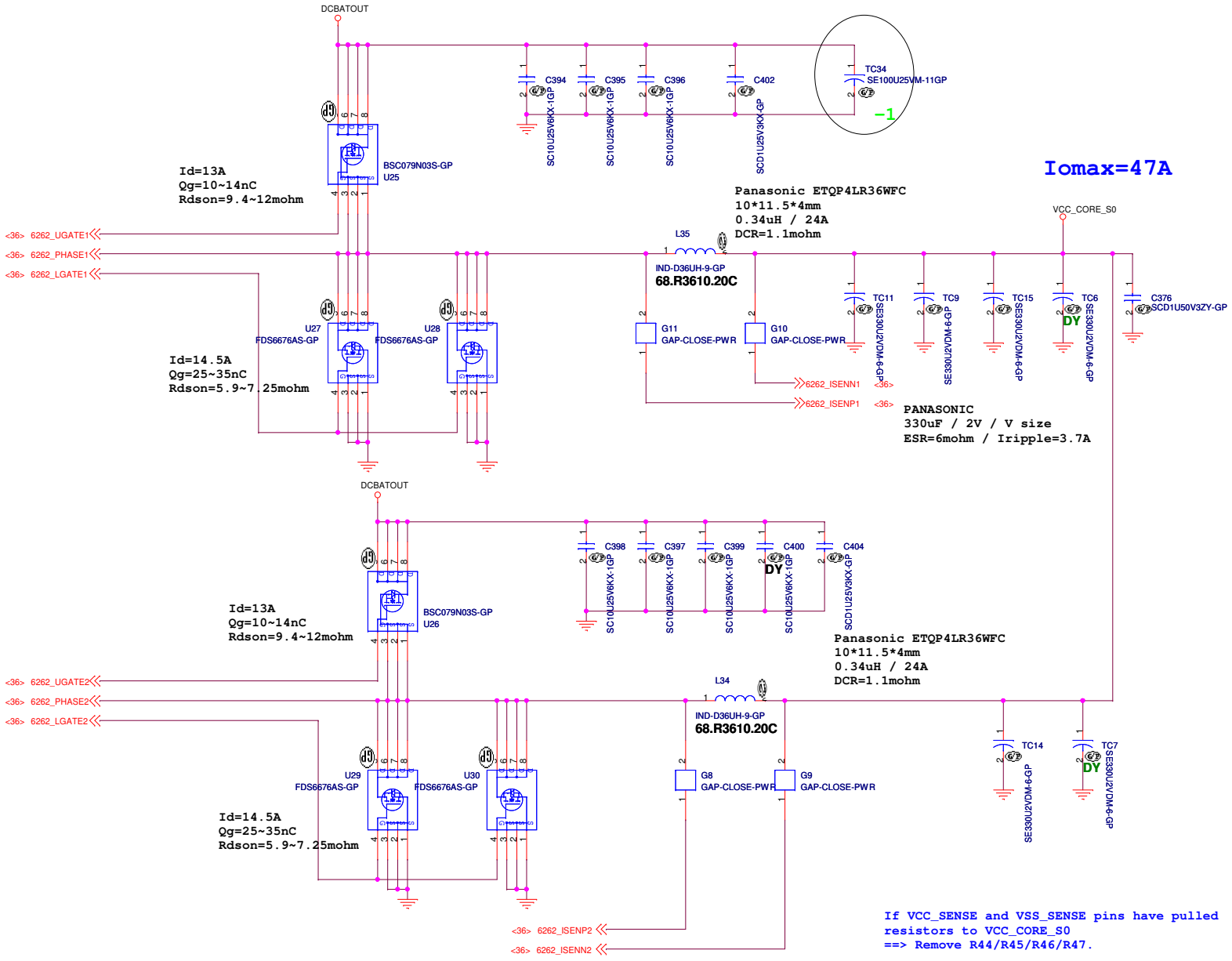
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FWH and Debug*

Size: B | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 35 of 56


ISL6262ACRZ-T-GP-U
U35
Place close to phase 1 chocke
470K /0402 size
If NTC=330Kohm, R10=8.66K
When test without cpu,
R33 & R34 change to 0 ohms
Place close to phase 1 chocke
A-NOTE2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE-1
Size A3
Document Number
Anote2.0 INTEL
Rev -1
Date: Thursday, March 22, 2007
Sheet 36 of 56



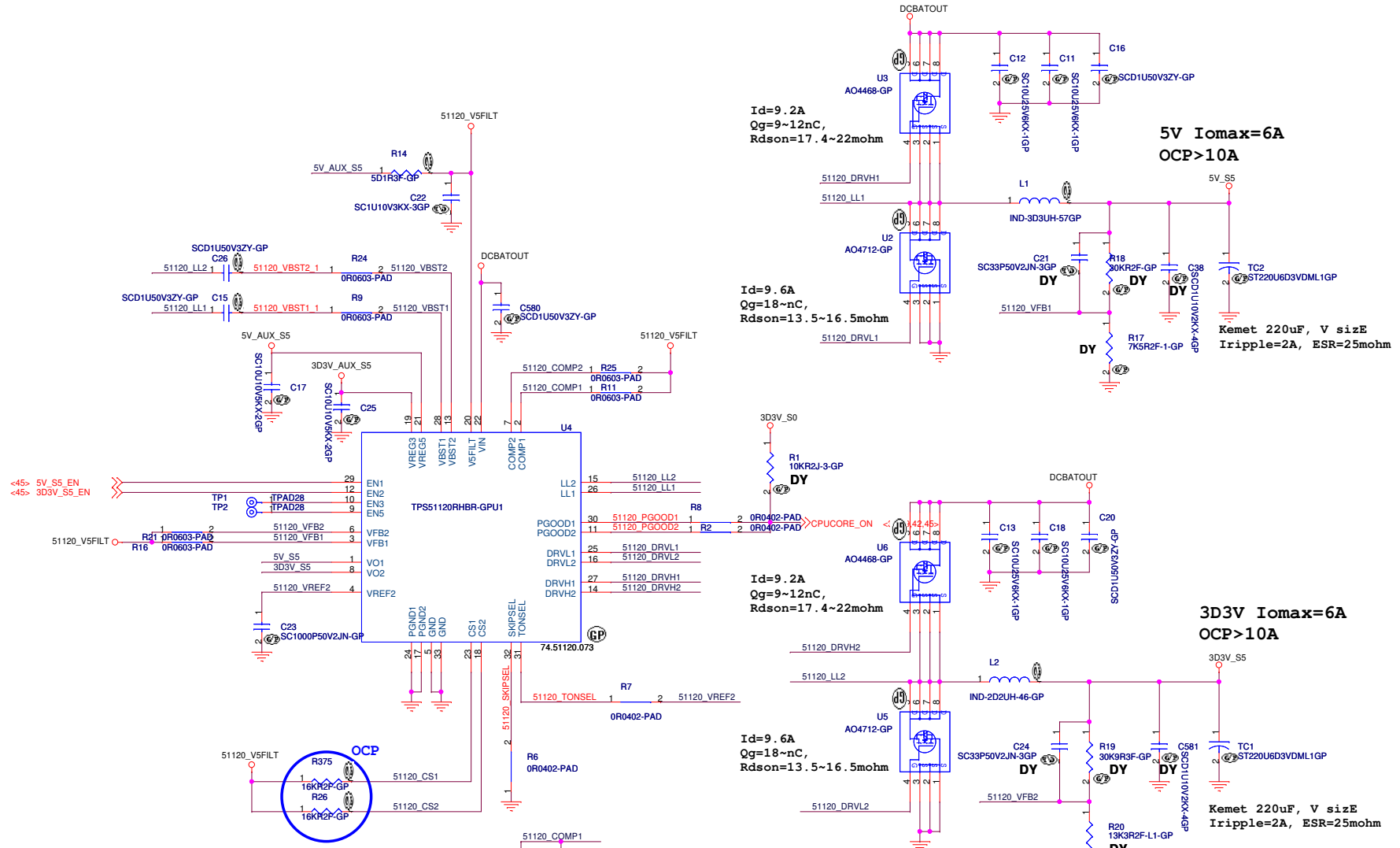
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCC_CORE_2

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 37 of 56



Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

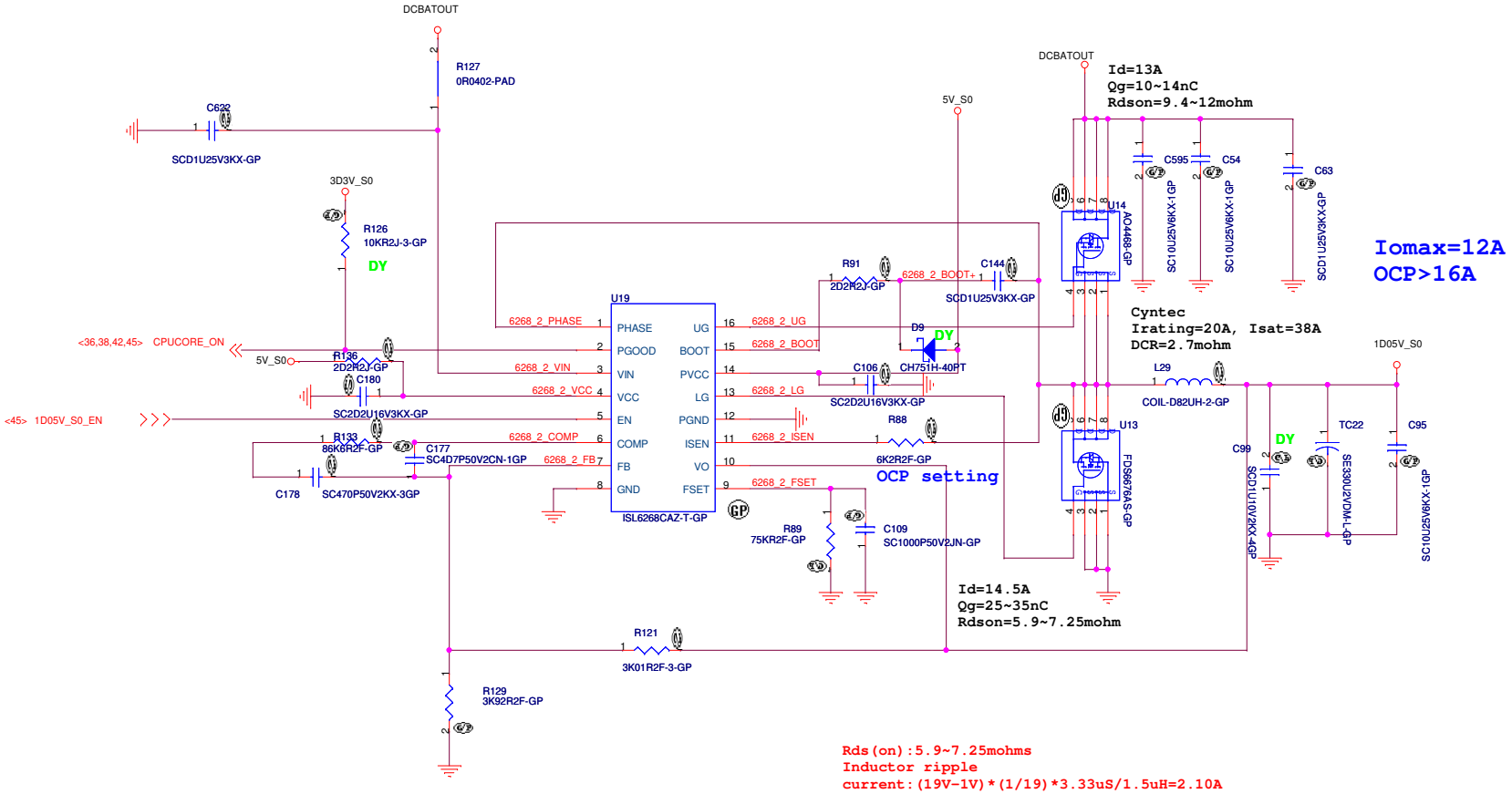
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 38 of 56



Rds(on):5.9~7.25mohms
Inductor ripple
current:(19V-1V)*(1/19)*3.33uS/1.5uH=2.10A
If OCP=16A
Risen=[16A+(2.1/2)]*(7.5mOhm*1.3)/26uA=6.18K

A-NOTE2

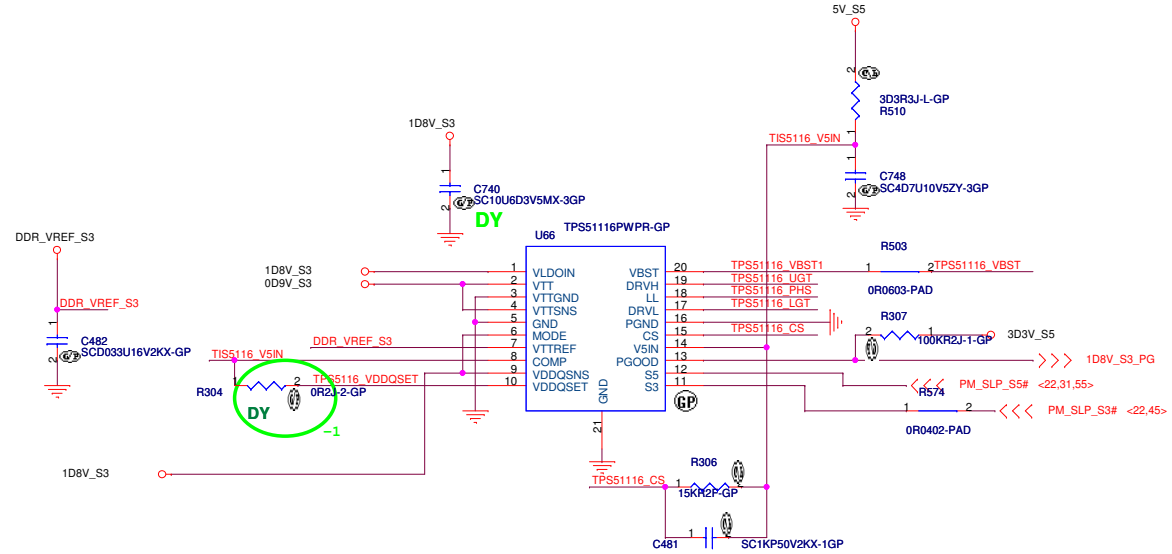
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D05V_S0_ISL6268

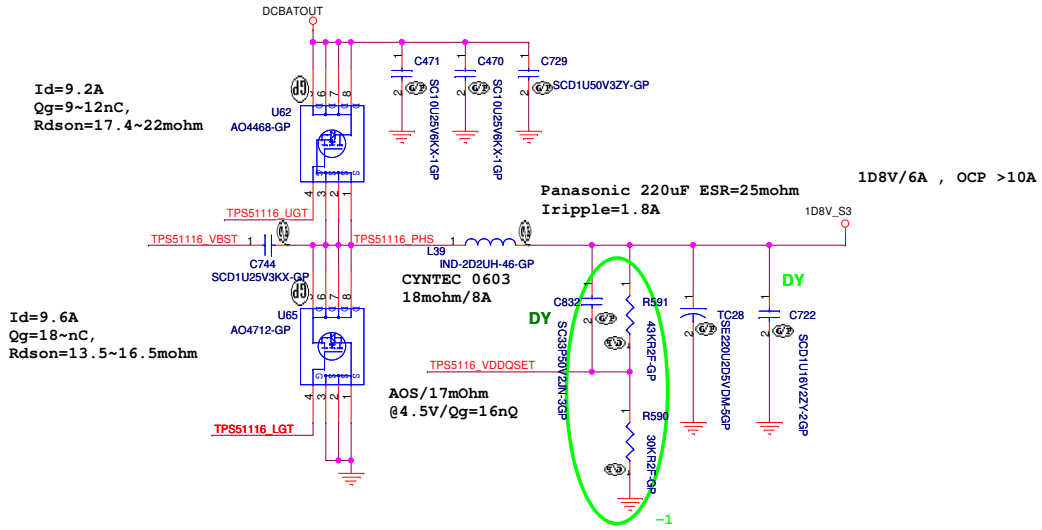
Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 39 of 56

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

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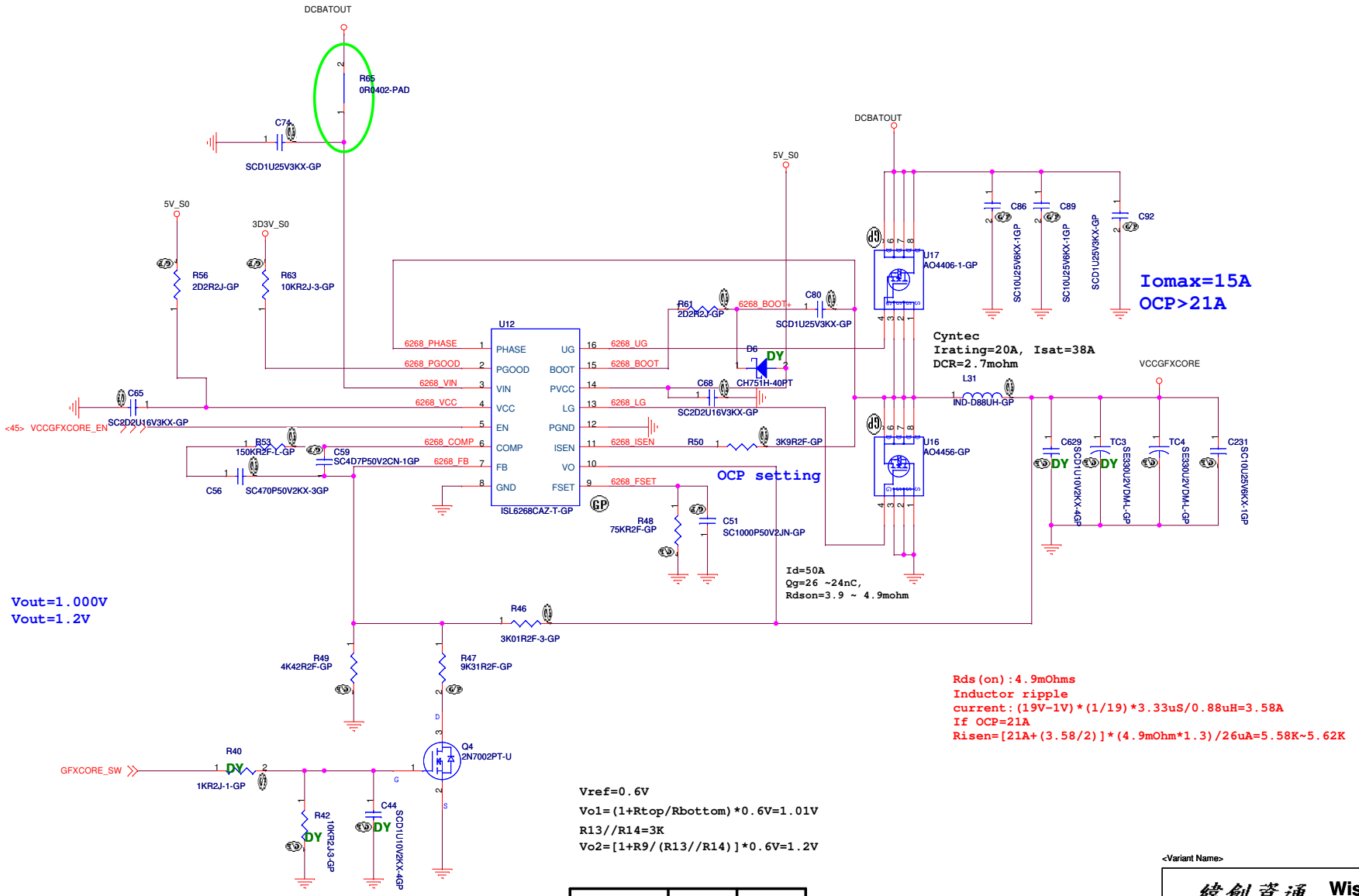
reserve for cost down



Vo_Select	Hi	Lo
Vout	1.2V	1.01V

<Variant Name>

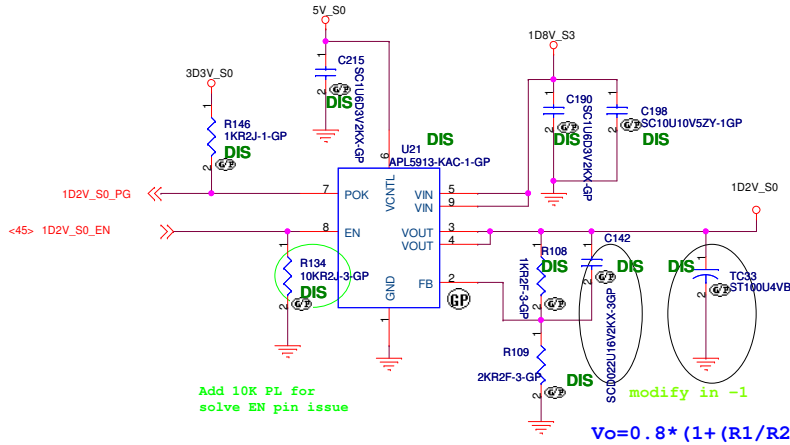
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCGFXCORE(ISL6268)

Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 41 of 56

VGA 1.2V Power

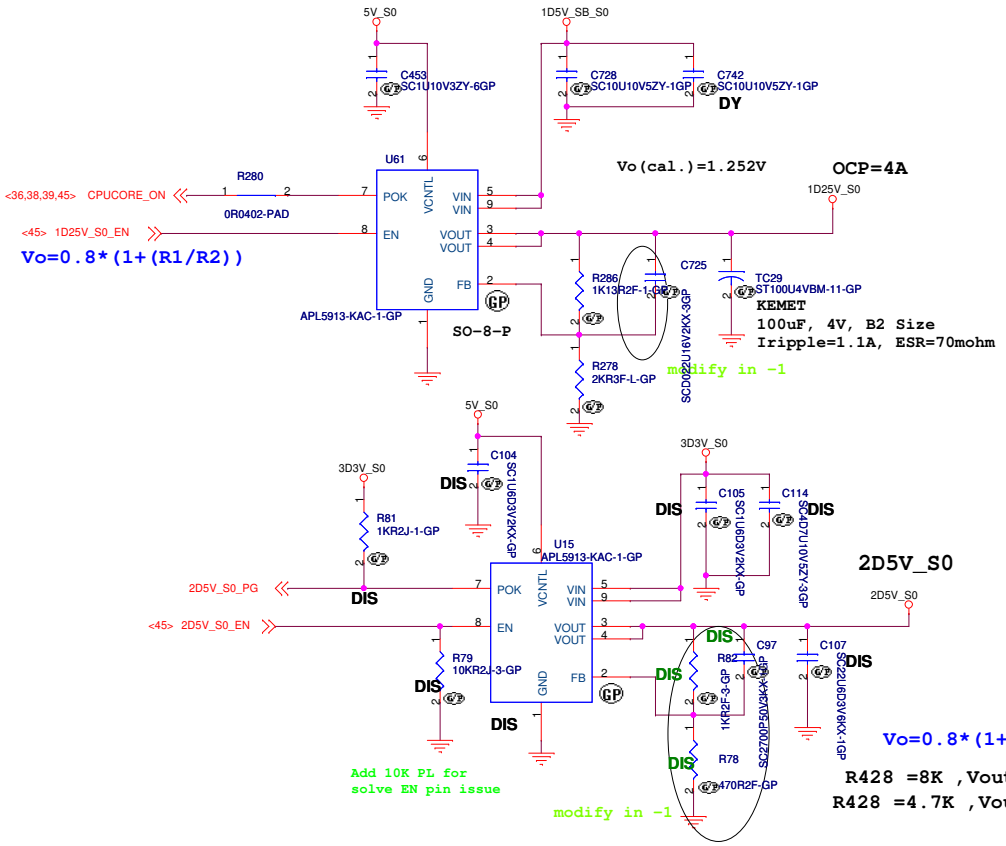


1D5V_NB

PS: SB del

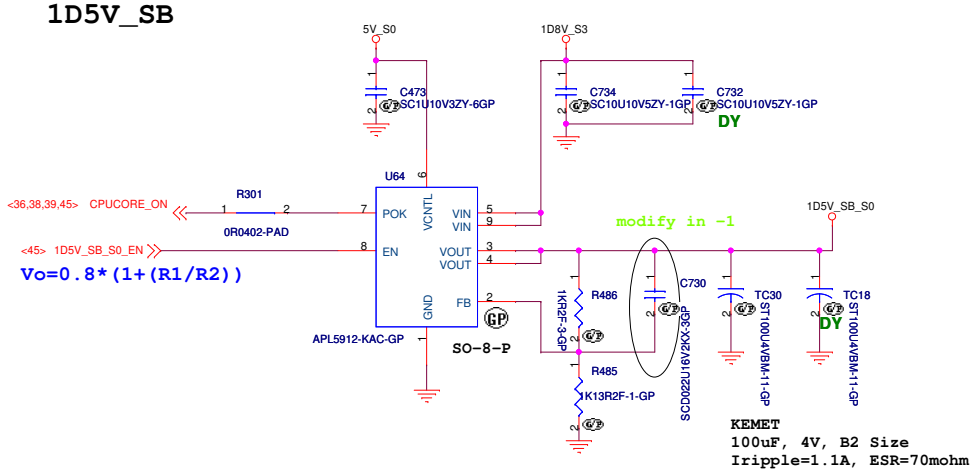
1D2V_S0
only for DISCRETE

1D25V_S0
Iomax=2.0A



2D5V_S0
only for DISCRETE

1D5V_SB



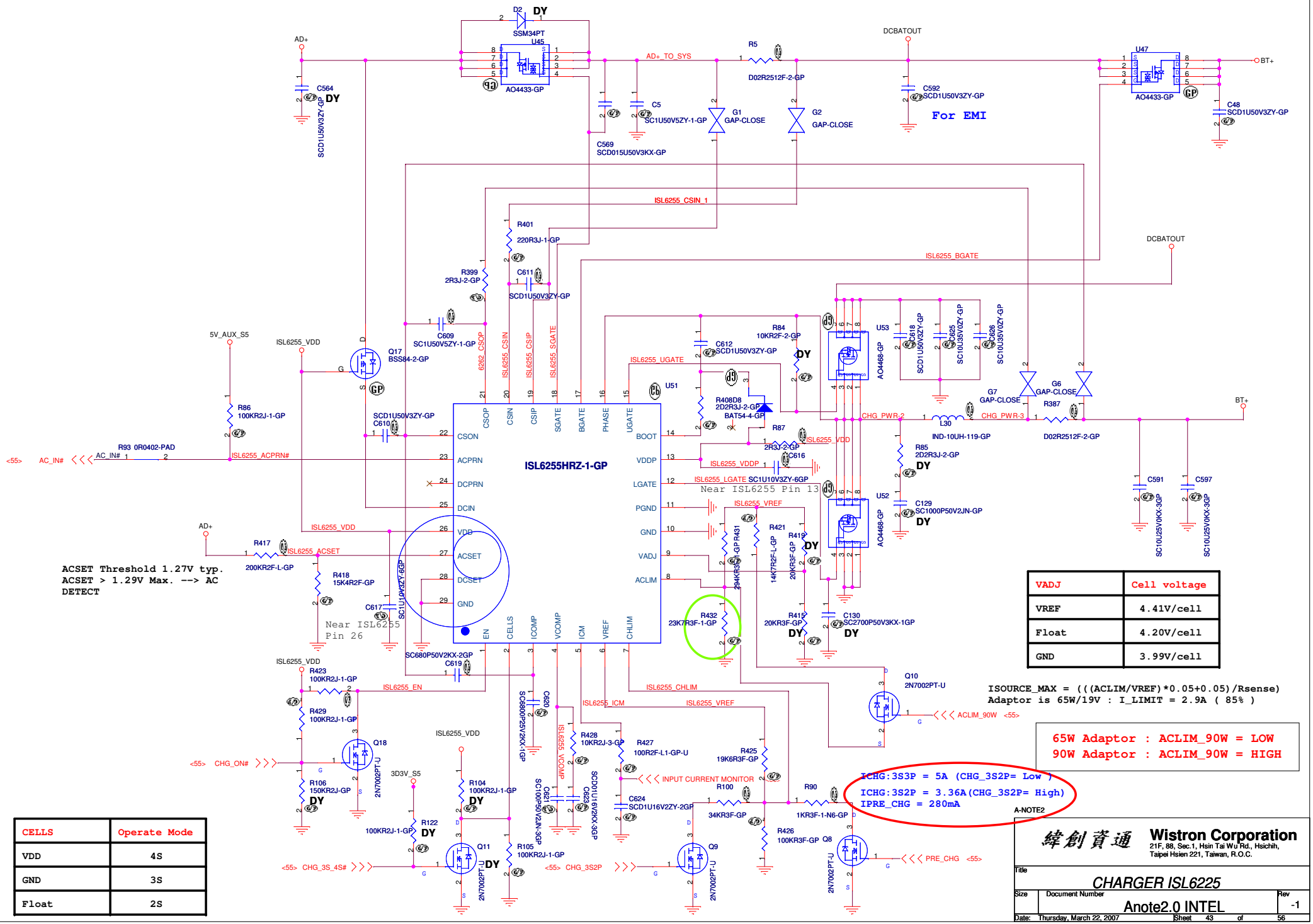
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D2V_VGA/2D5V/1D25V/1D5V LDO*

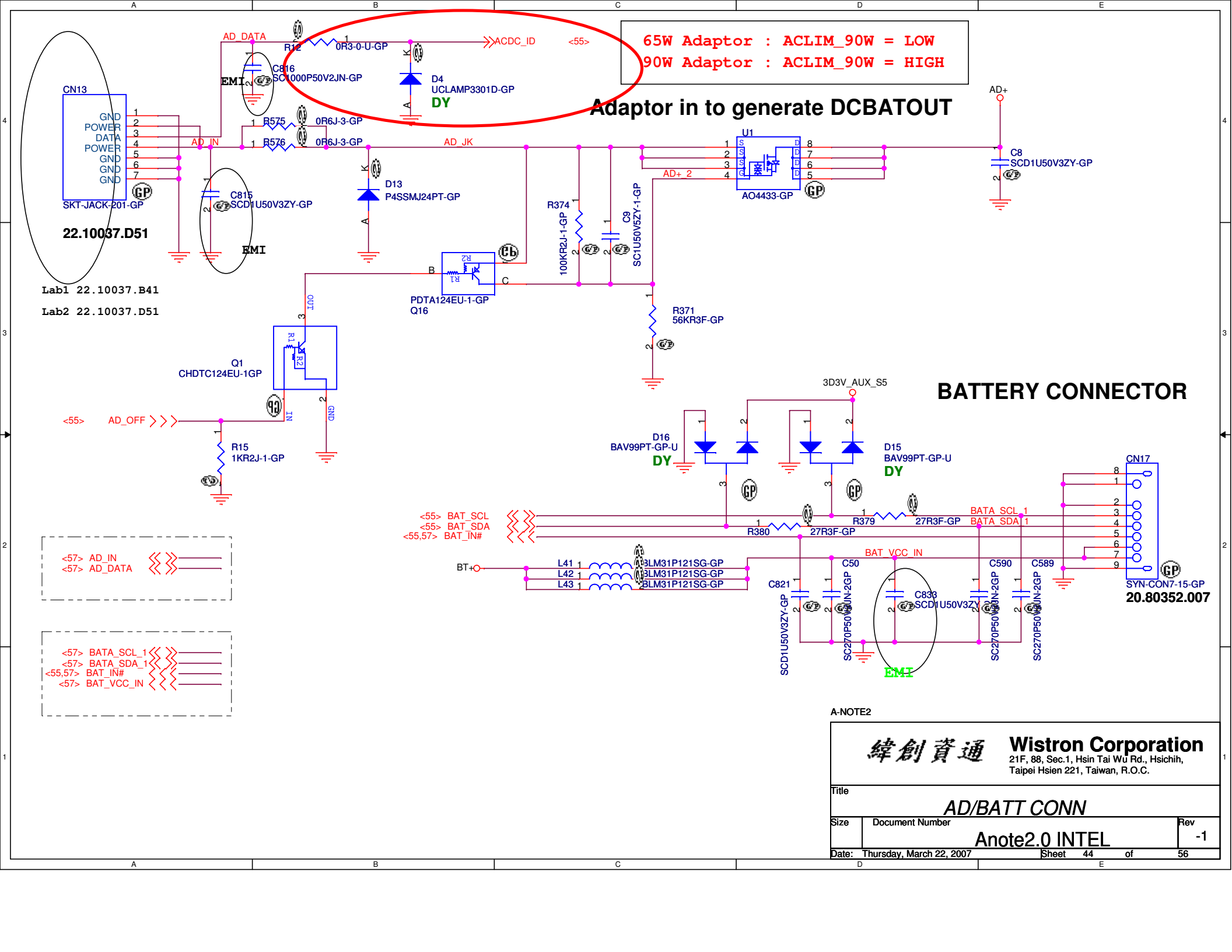
Size | Document Number: **Anote2.0 INTEL** | Rev: -1

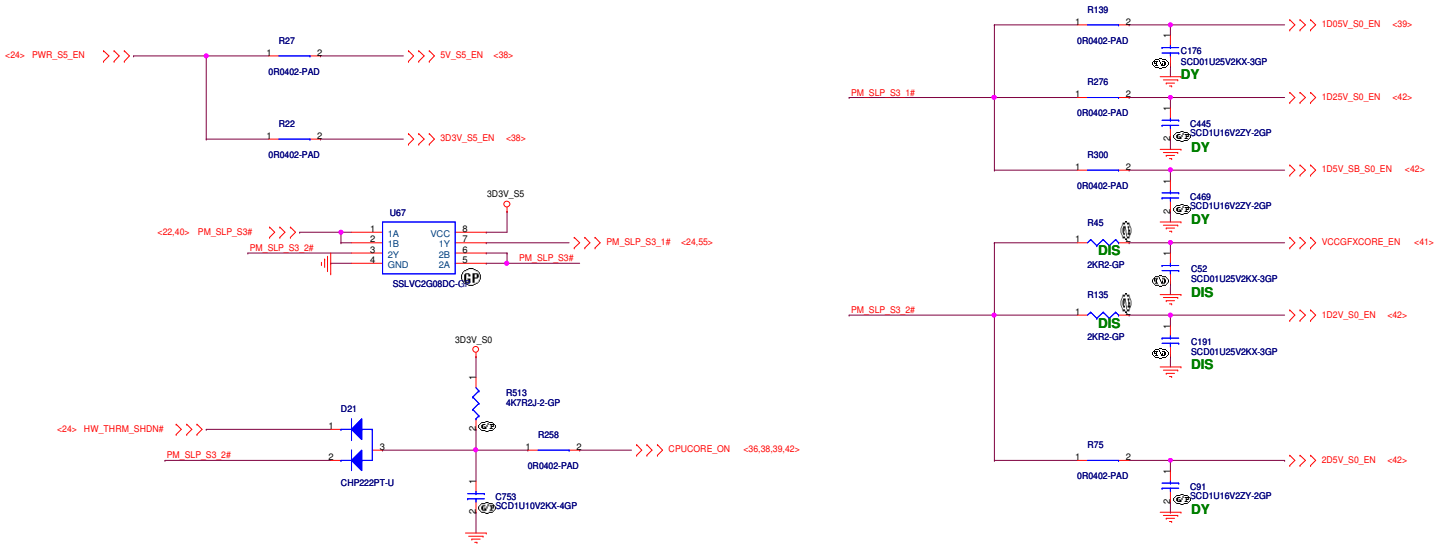
Date: Thursday, March 22, 2007 | Sheet 42 of 56



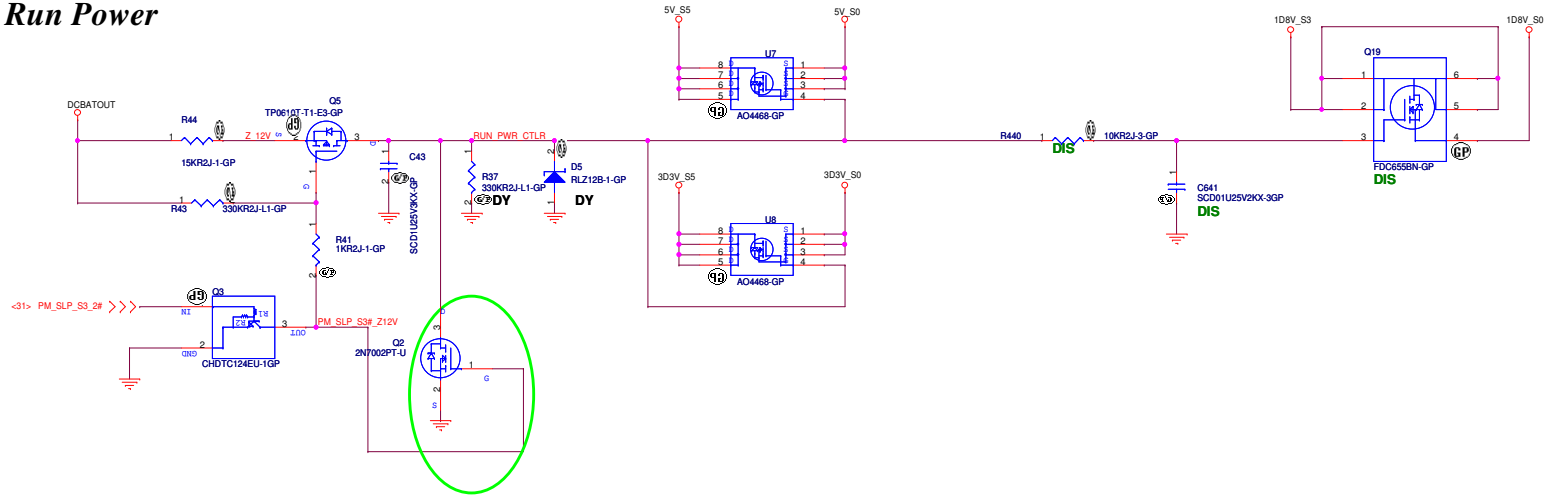
VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S


65W Adaptor : ACLIM_90W = LOW
90W Adaptor : ACLIM_90W = HIGH
Adaptor in to generate DCBATOUT
BATTERY CONNECTOR
CN13
SKT-JACK-201-GP
22.10037.D51
Lab1 22.10037.B41
Lab2 22.10037.D51
AD_DATA
AD_IN
AD_JK
ACDC_ID
R12 0R3-0-U-GP
C816 SC1000P50V2JN-GP
D4 UCLAMP3301D-GP
DY
R575 0R6J-3-GP
R576 0R6J-3-GP
C815 SCD1U50V3ZY-GP
D13 P4SSMJ24PT-GP
U1 AO4433-GP
AD+
AD+_2
C8 SCD1U50V3ZY-GP
R374 100KR2J-1-GP
C9 SC1U50V5ZY-1-GP
PDTA124EU-1-GP
Q16
R371 56KR3F-GP
Q1 CHDTC124EU-1GP
R15 1KR2J-1-GP
AD_OFF
3D3V_AUX_S5
D16 BAV99PT-GP-U
D15 BAV99PT-GP-U
R379 27R3F-GP
R380 27R3F-GP
BAT_SCL
BAT_SDA
BAT_IN#
BT+
L41 BLM31P121SG-GP
L42 BLM31P121SG-GP
L43 BLM31P121SG-GP
BAT_VCC_IN
C50 SC270P50VJN-2GP
C590 SC270P50VJN-2GP
C589 SC270P50VJN-2GP
C821 SCD1U50V3ZY-GP
C833 SCD1U50V3ZY
EMI
CN17
SYN-CON7-15-GP
20.80352.007
<57> AD_IN
<57> AD_DATA
<57> BATA_SCL_1
<57> BATA_SDA_1
<55,57> BAT_IN#
<57> BAT_VCC_IN
A-NOTE2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD/BATT CONN
Size
Document Number
Anote2.0 INTEL
Rev
-1
Date: Thursday, March 22, 2007
Sheet 44 of 56



Run Power



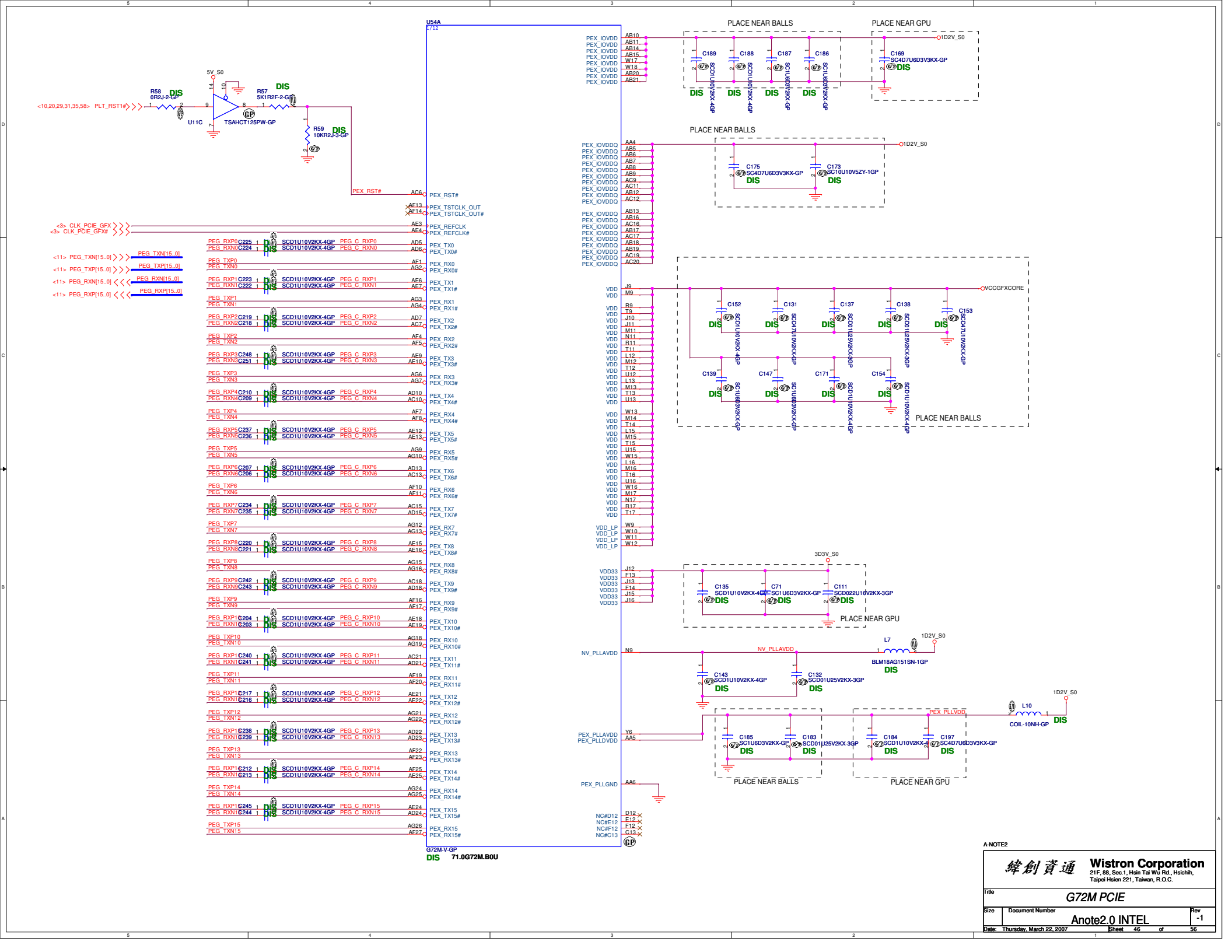
A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESET LOGIC***

Size	Document Number	Rev
C	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 45 of 56


U54A
1/12
G72M-V-GP
DIS
71.0G72M.B0U
PLACE NEAR BALLS
PLACE NEAR GPU
1D2V_S0
3D3V_S0
VCCGFXCORE
5V_S0
U11C
TSAHCT125PW-GP
PEX_RST#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_REFCLK
PEX_REFCLK#
NV_PLLAVDD
PEX_PLLVDD
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
L7
BLM18AG151SN-1GP
L10
COIL-10NH-GP
A-NOTE2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
G72M PCIE
Anote2.0 INTEL
Thursday, March 22, 2007
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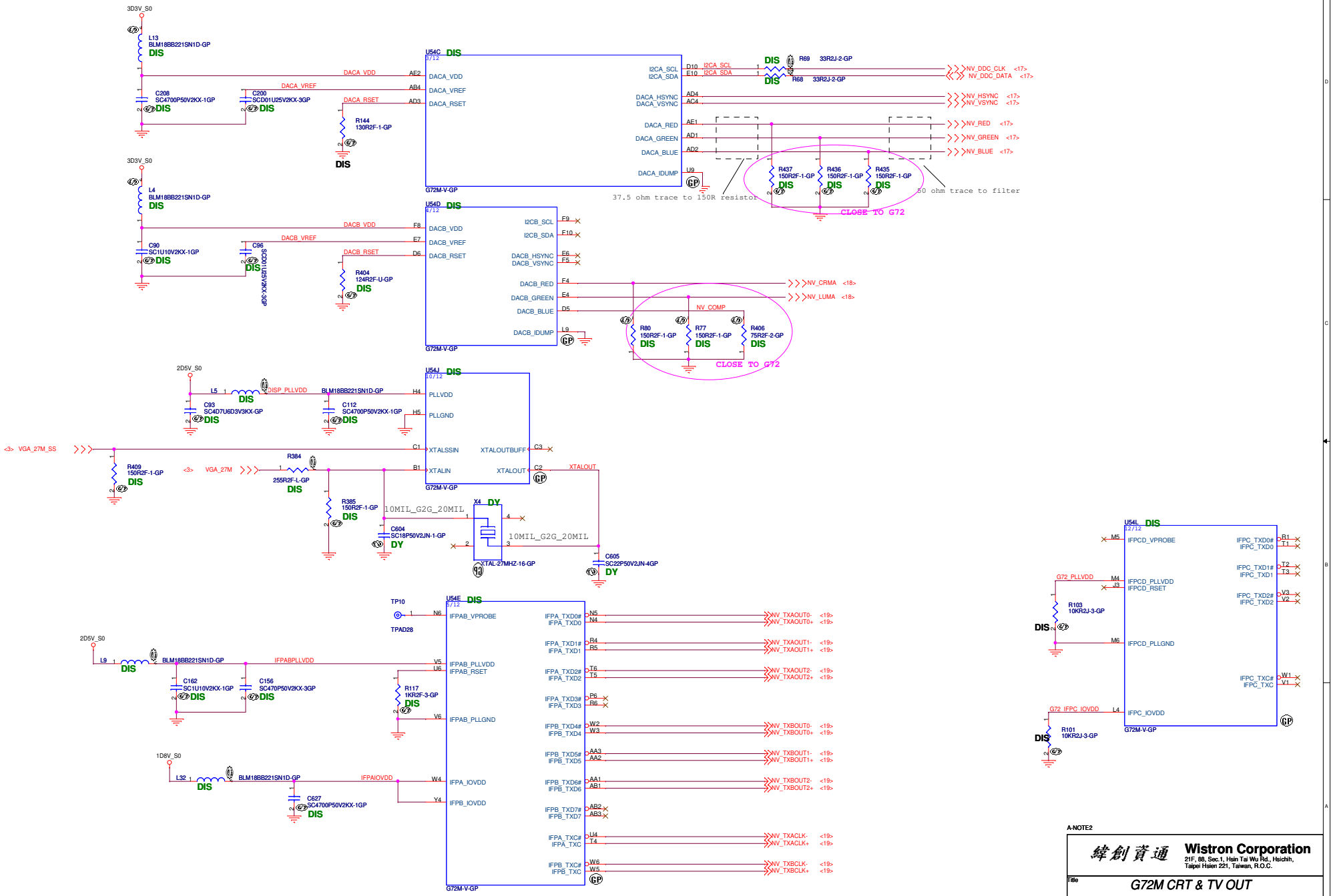
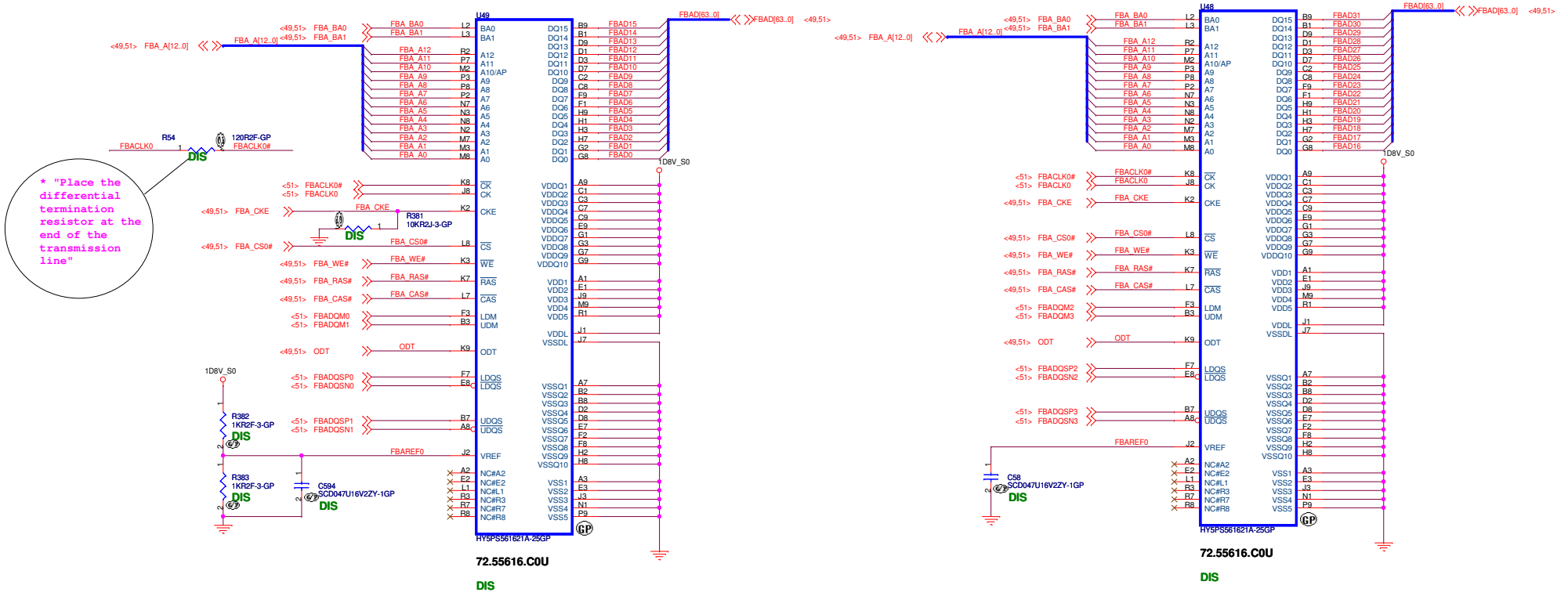
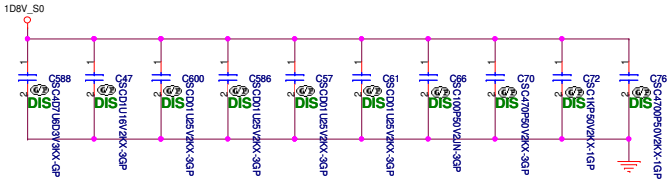


A-NOTE2

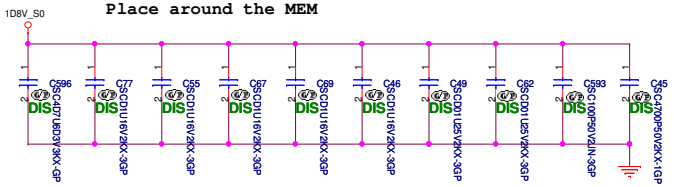
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G72M CRT & TV OUT	
Size	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet 47 of 56	



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)

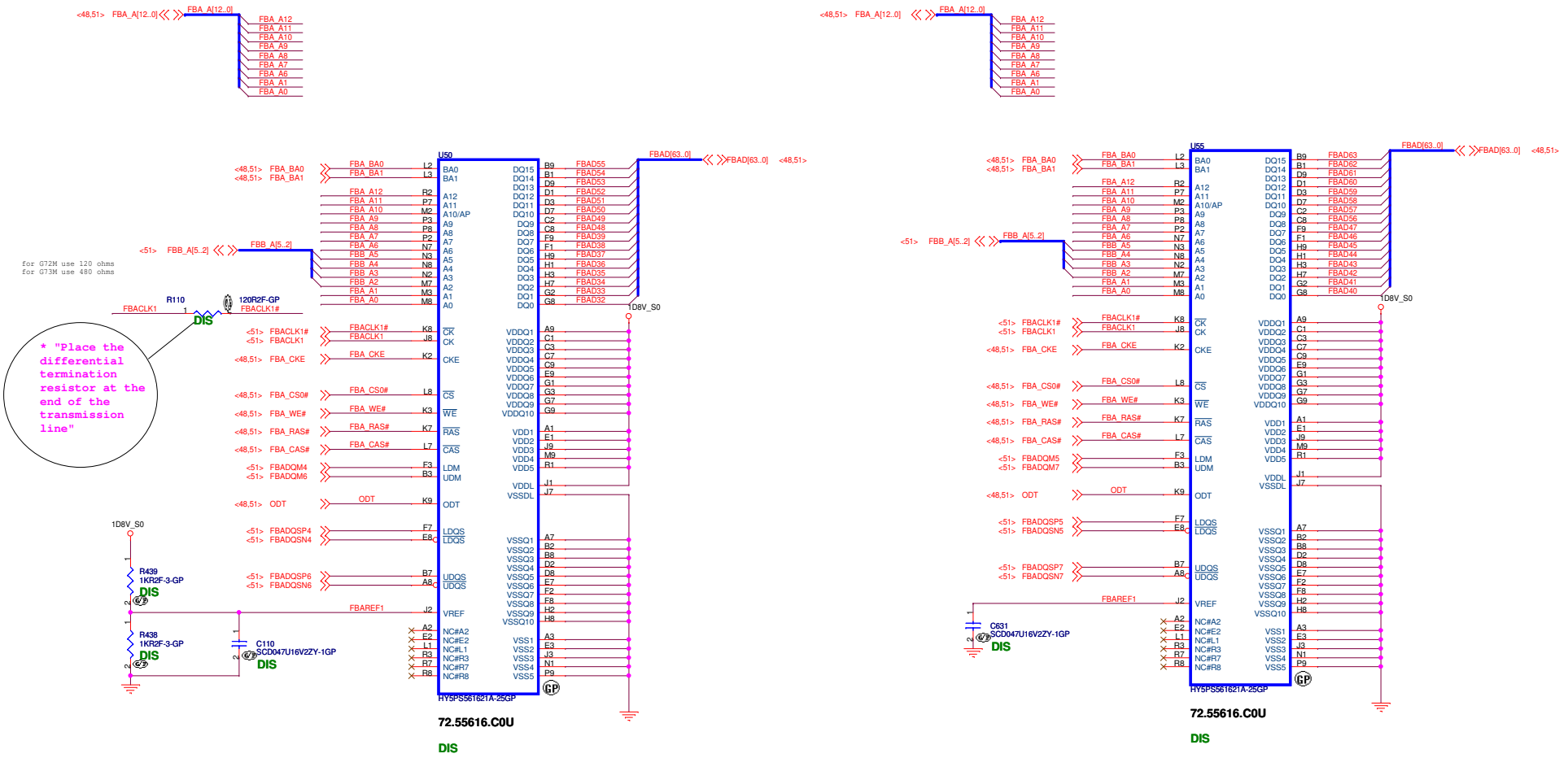
A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

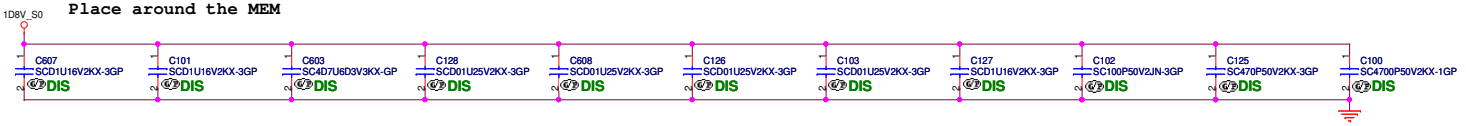
Title: *G72M VRAM (1ST 1/2)*

Size	Document Number	Rev
	Anote2.0 INTEL	-1

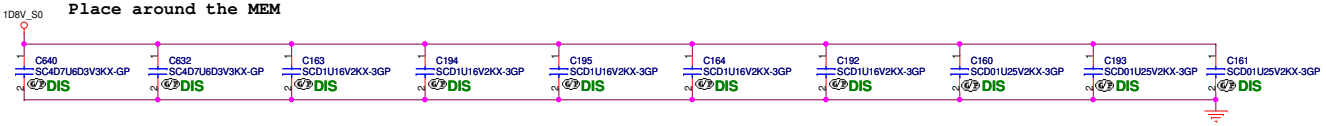
Date: Thursday, March 22, 2007 Sheet 48 of 56



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



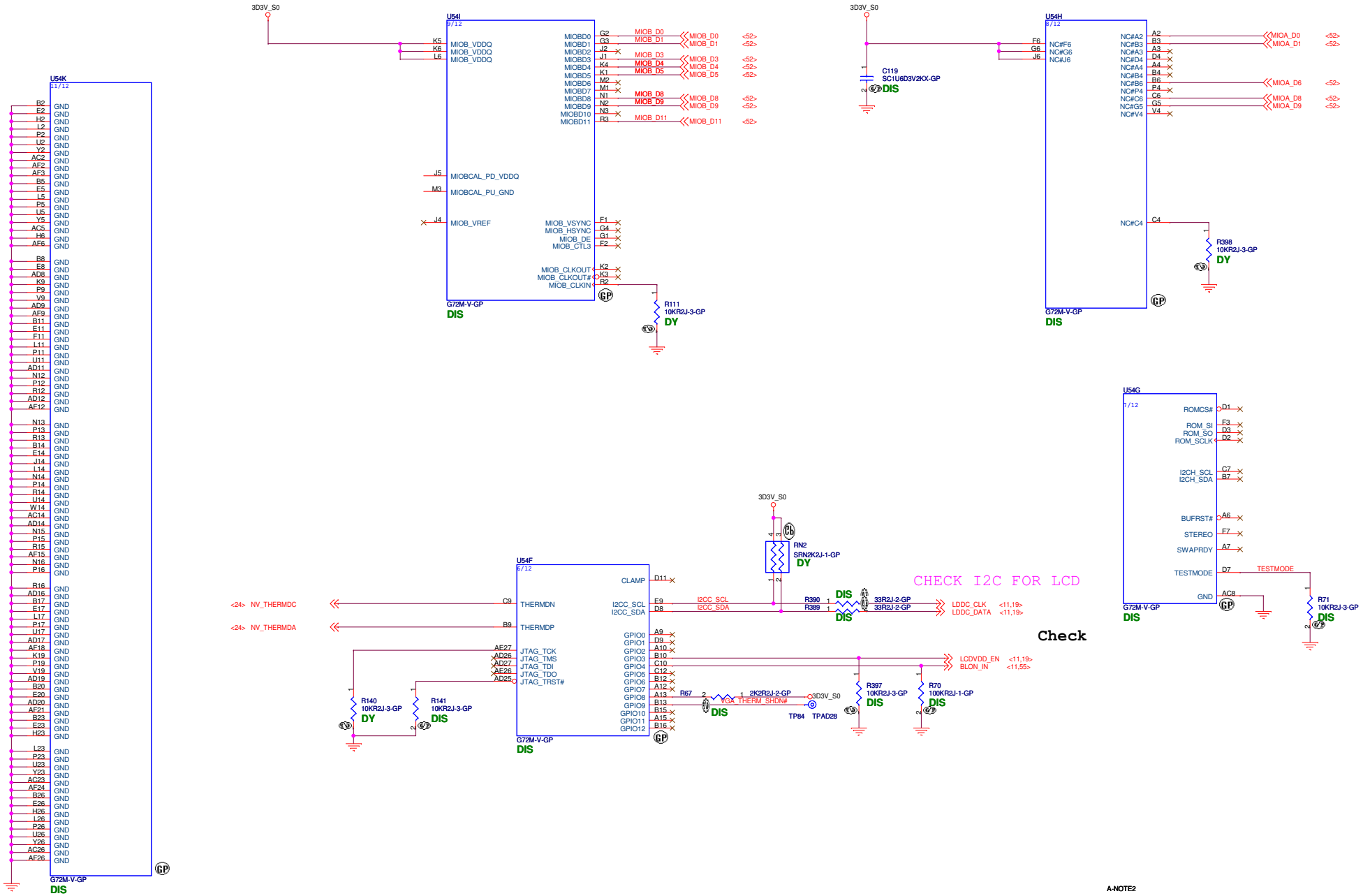
A-NOTE2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M VRAM (1ST 2/2)

Size | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 49 of 56



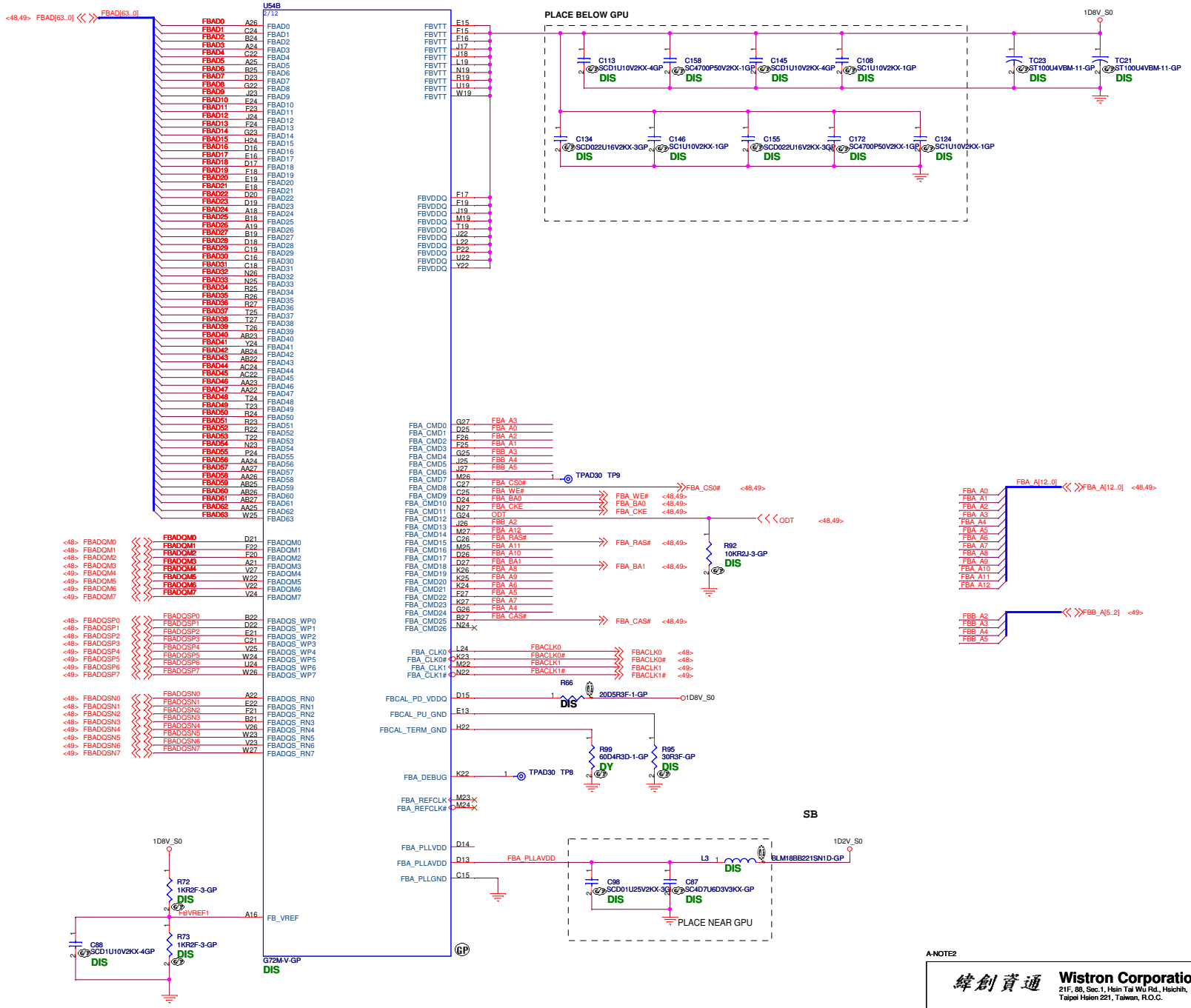
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M ROM & Spread Specturm

Size | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 50 of 56



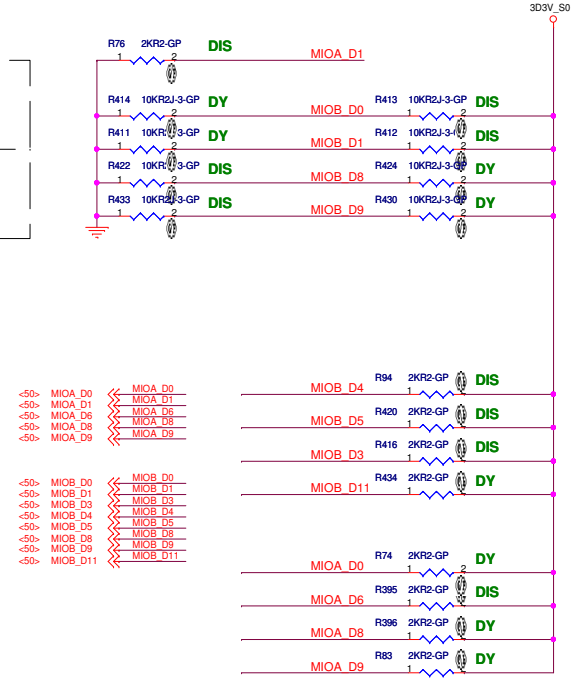
A-NOTE2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*G72M MEMORY IF 1*
Size	Document Number: Anote2.0 INTEL — Rev: -1
Date: Thursday, March 22, 2007	Sheet 51 of 56

STRAPS, Mechanical Parts

Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0



Bit	Signal	Values
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

RAM_CFG[9.8.1.0] RAM_CFG[3..0]	Config	FB Bus Width	Definitions
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

MIOB_D4:	PCI_DEVID_0	
MIOB_D5:	PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3:	PCI_DEVID_2	
MIOB_D11:	PCI_DEVID_3	0111 G72MV **G72MZ=6,G73=8**

MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT

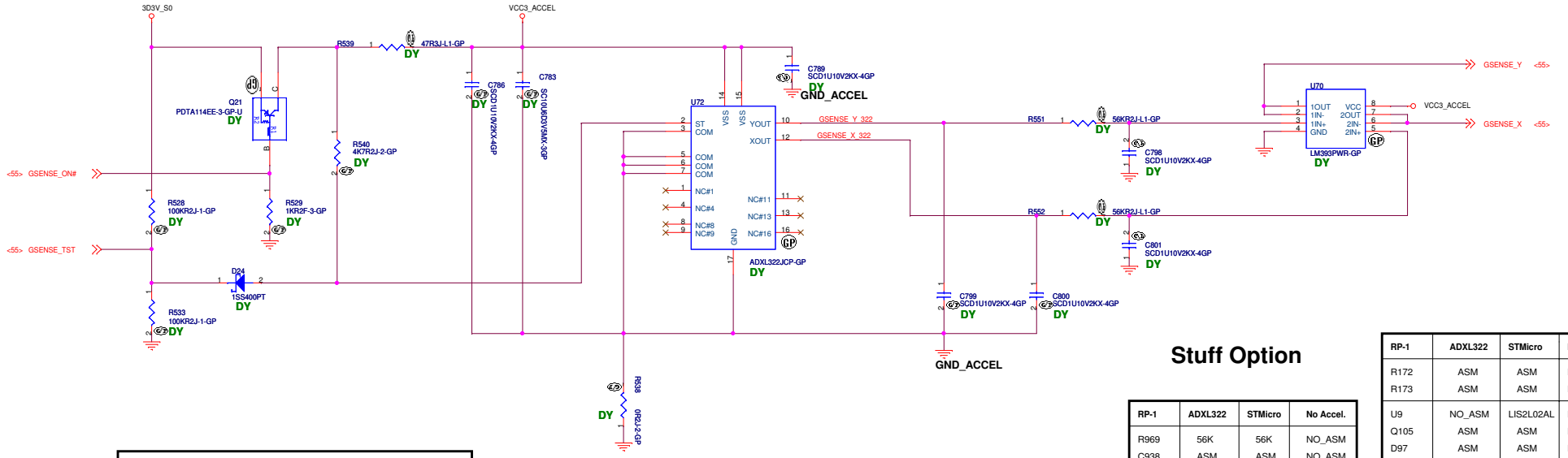
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G72M STRAPPING*

Size | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 52 of 56



Stuff Option

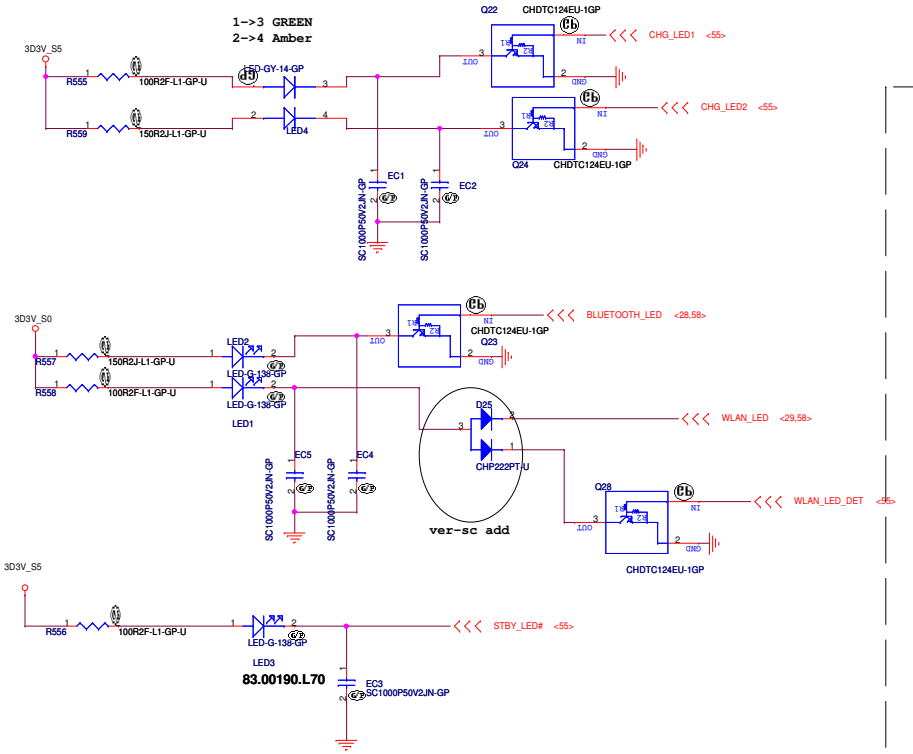
RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

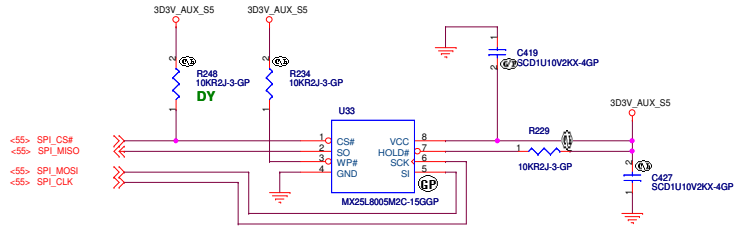
A-note 2.0 LED's Location and Sequence

Left side — Right side

WLAN Bluetooth Battery Suspend



SPI ROM for System & KBC



1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01

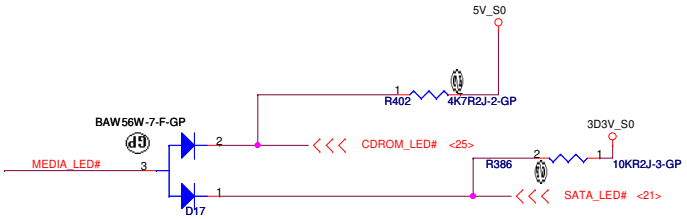
A-NOTE2

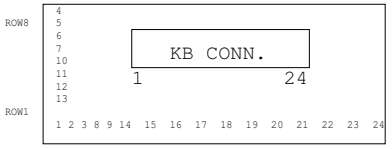
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-sensor / SPI / LEDs**

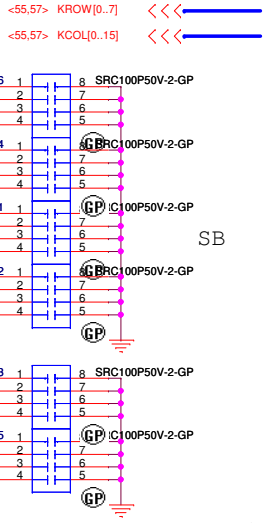
Size	Document Number	Rev
D	Anote2.0 INTEL	-1

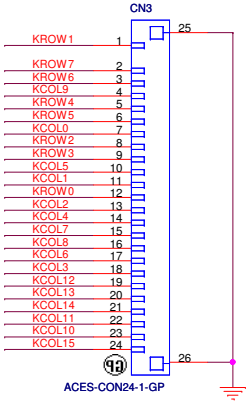
Date: Thursday, March 22, 2007 Sheet 53 of 56



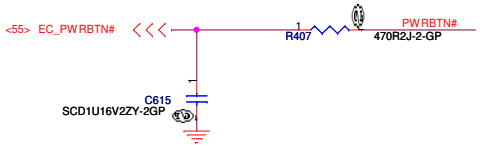


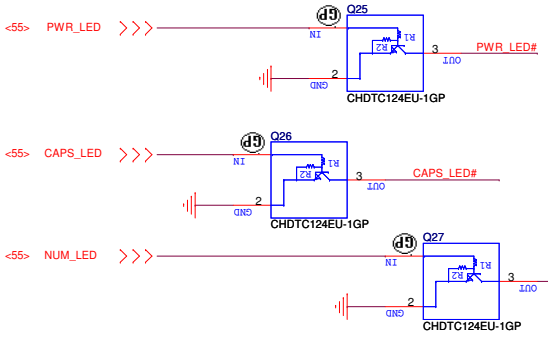
Internal KeyBoard Connector

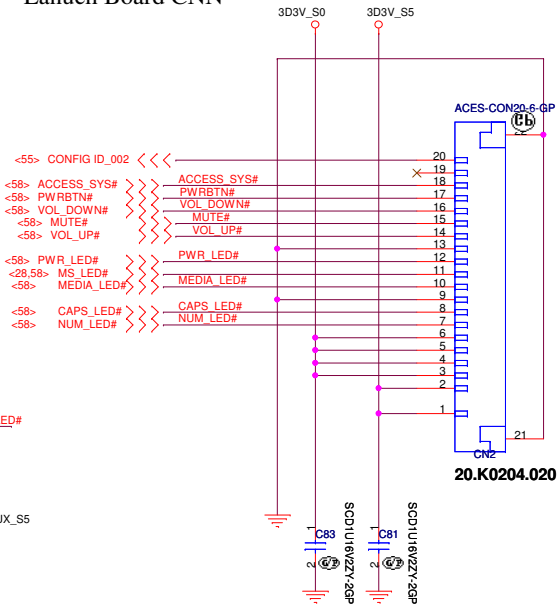




Lanuch Board CNN

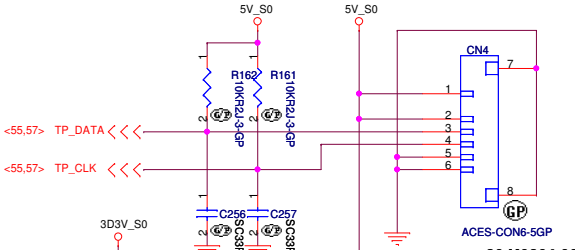


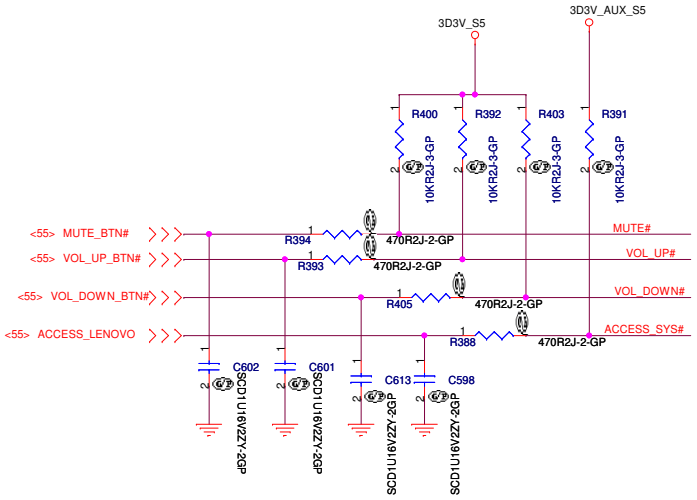




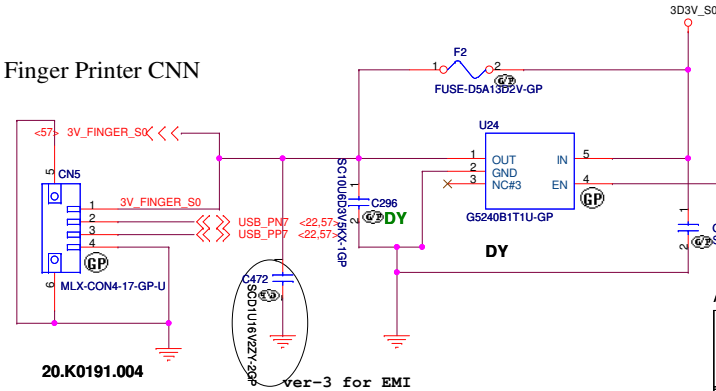
LAB2 20.K0204.020

TouchPad Connector





Finger Printer CNN



ver-3 for EMI

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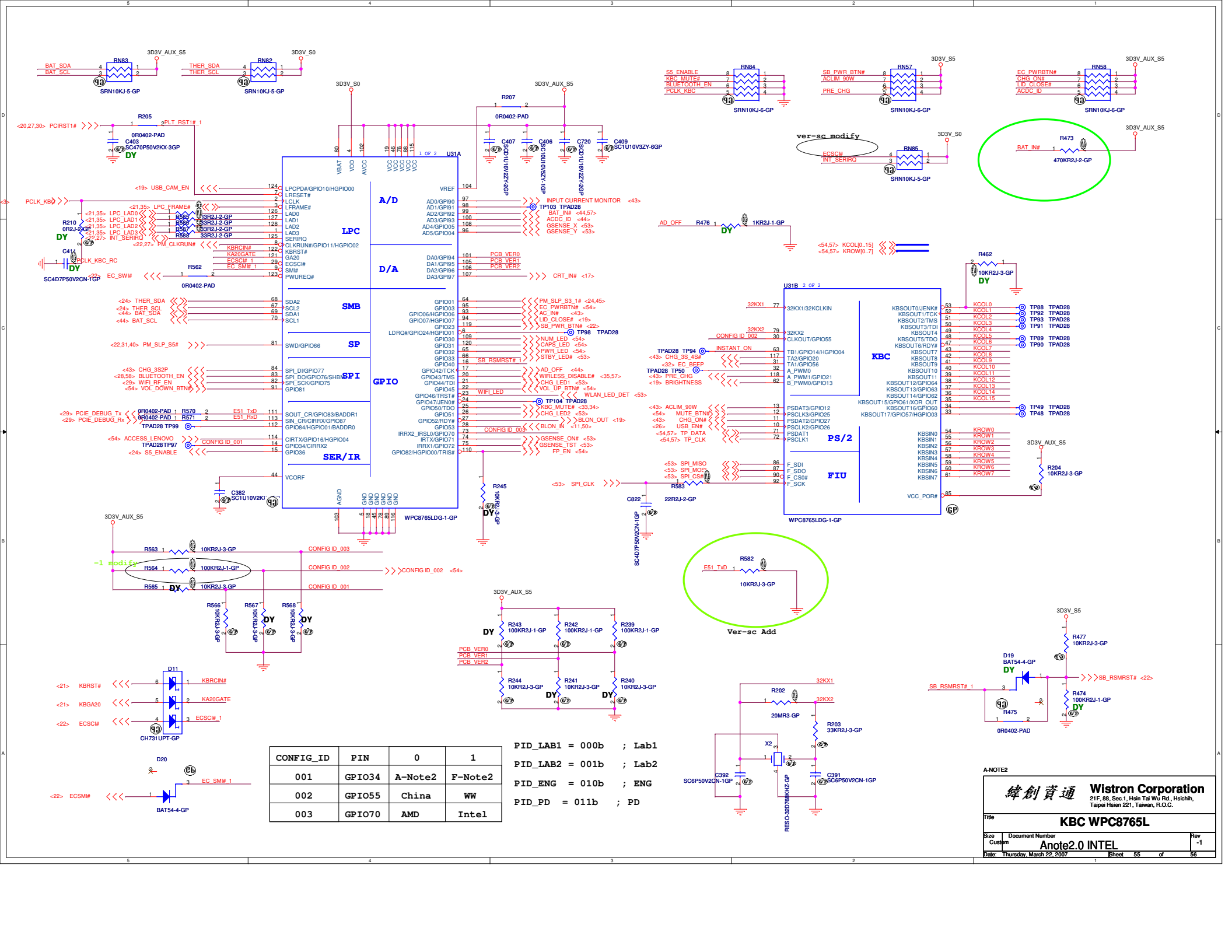

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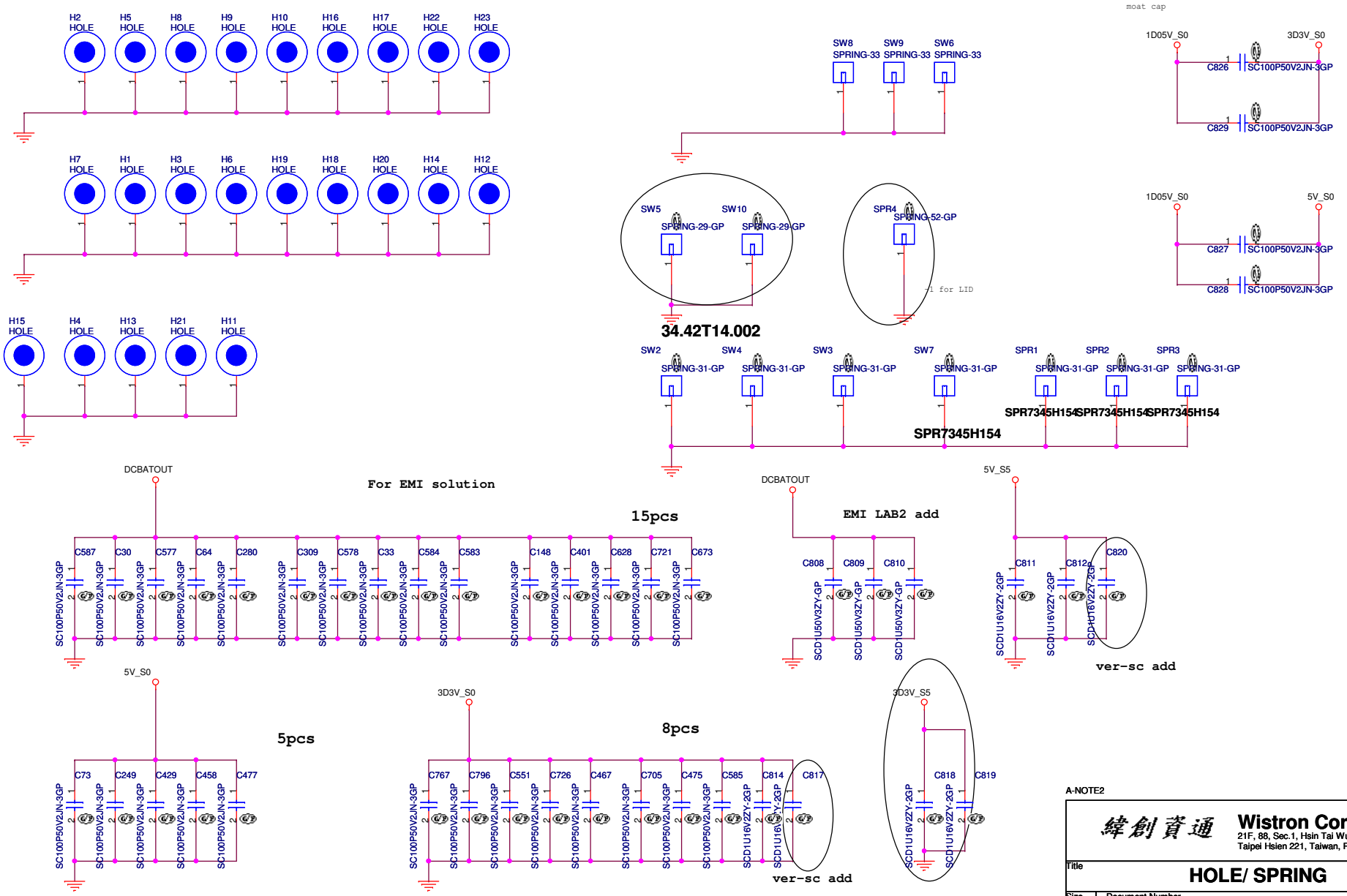
002	GPIO55	China	WW
003	GPIO70	AMD	Intel



A-NOTE2

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Title: **HOLE/ SPRING**

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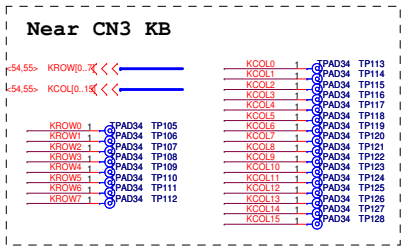

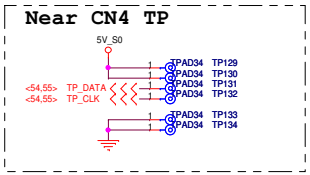

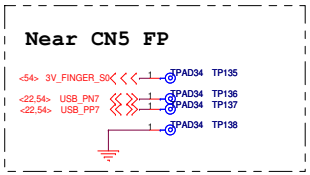

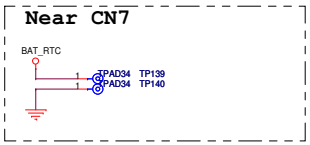

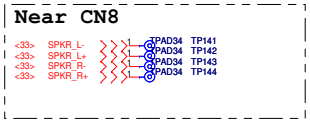

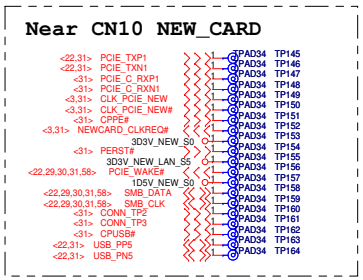

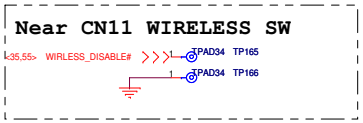

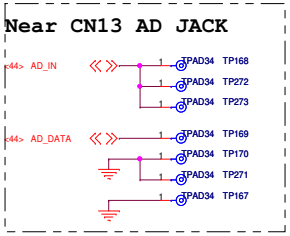

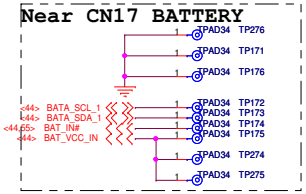

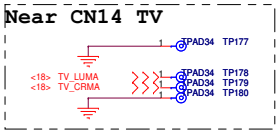

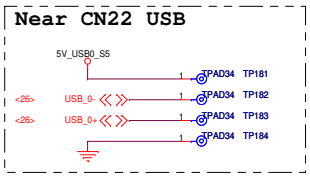

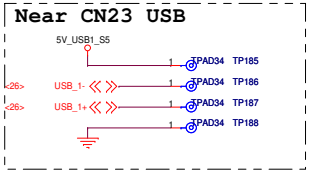

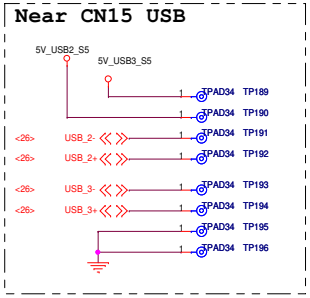

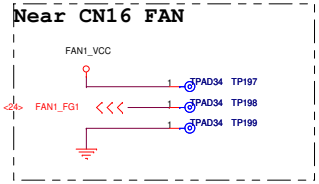

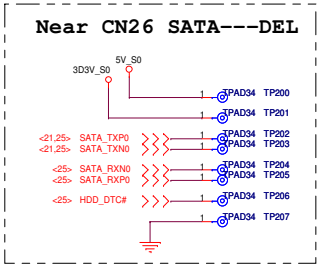

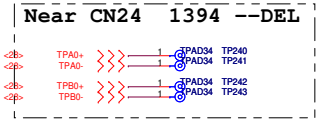

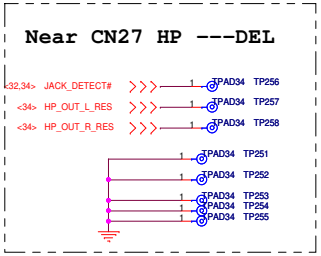

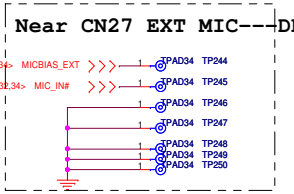

A-NOTE2

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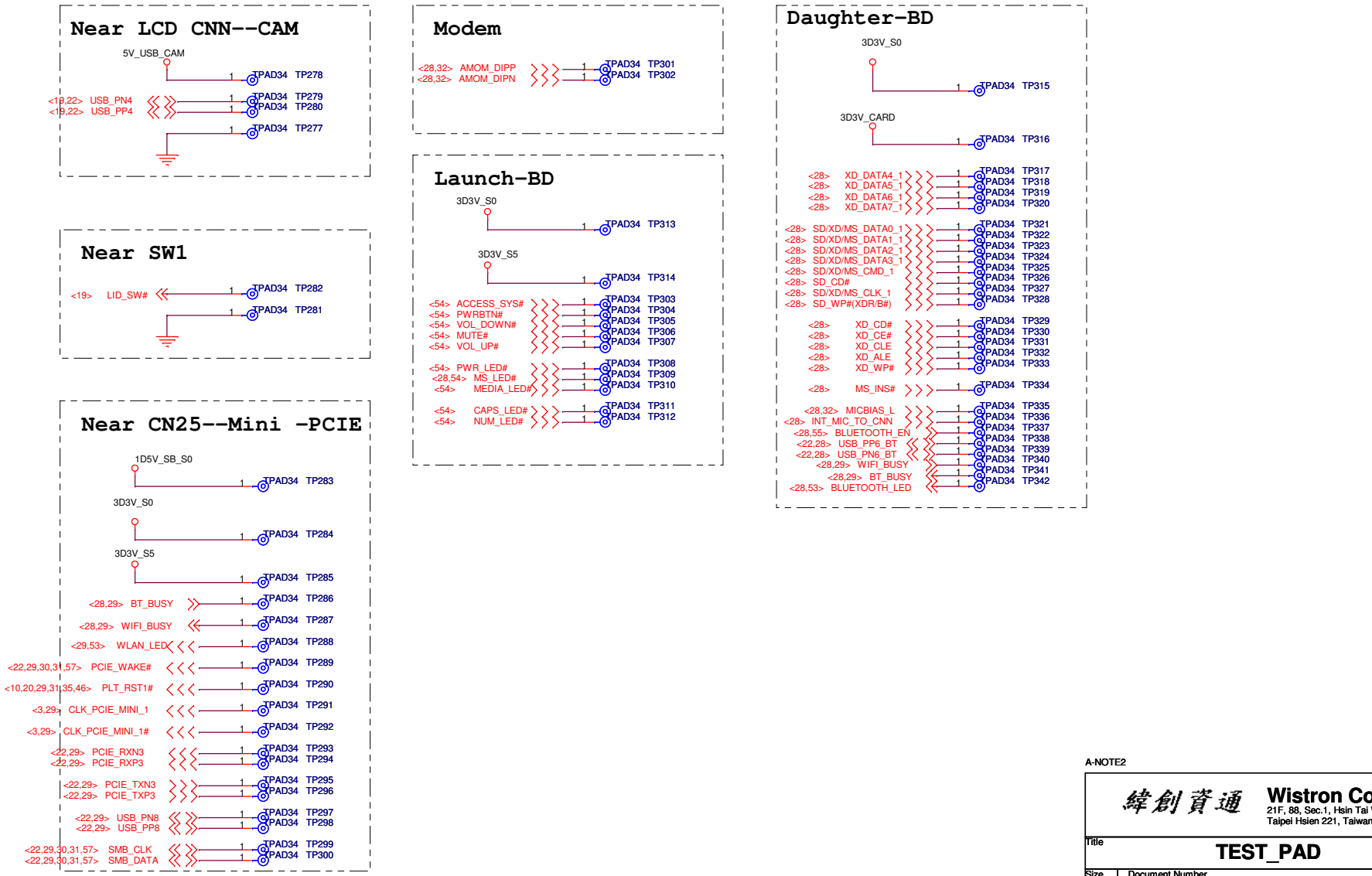

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Title: **TEST_PAD**

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