

# JIWA3/A4

## Compal Schematics Document

### Mobile Penryn uFCPGA

### Intel Cantiga\_GM/PM+ICH9-M

Wednesday, May 14, 2008

REV:1.0

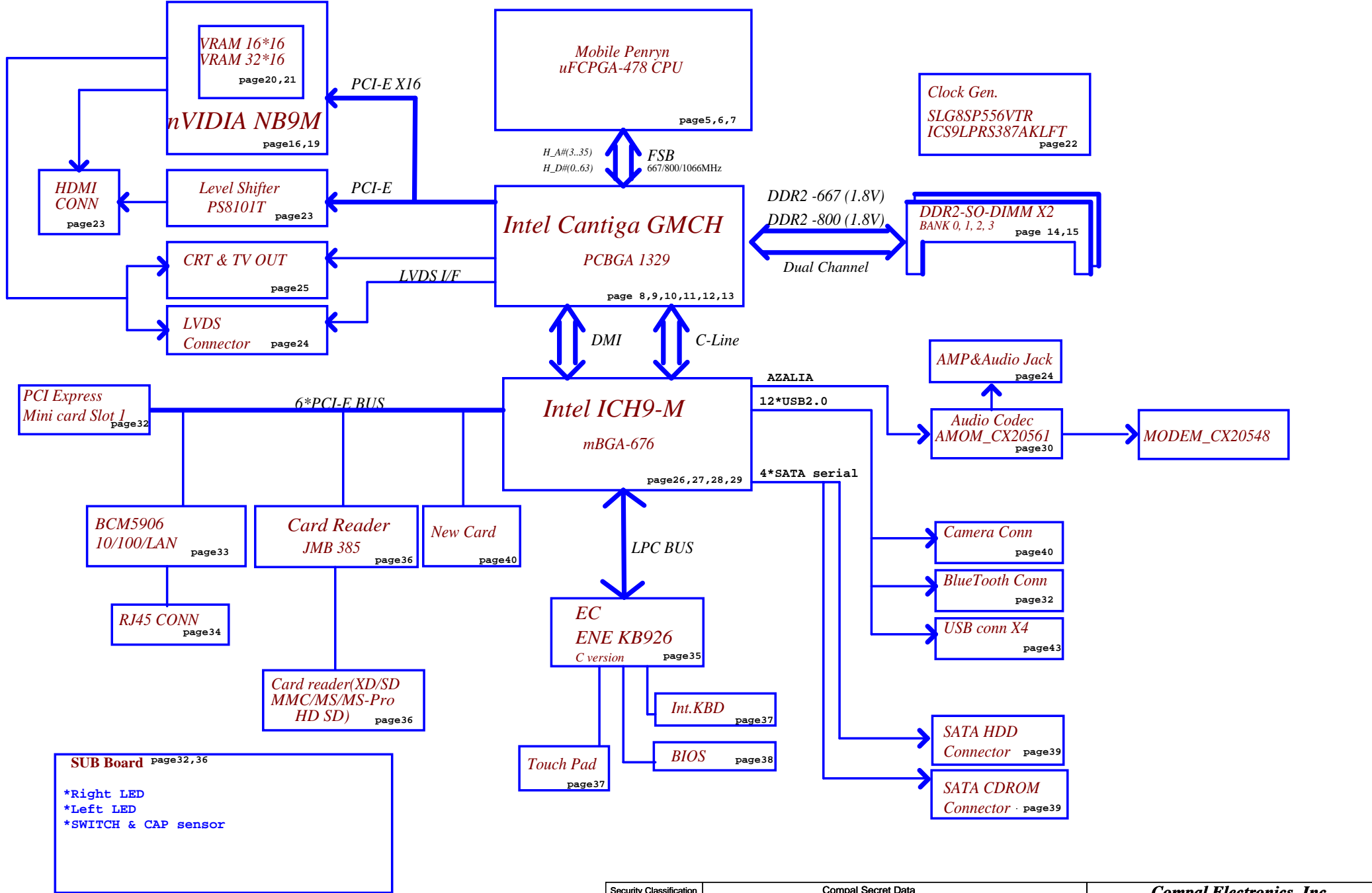
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<i>Compal Electronics, Inc.</i>
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size
				Document Number
Date:	JIWA3/A4_LA421P	Rev	1.0	
	Sheet 1 of 53			

zzz1  
15W\_PCB\_LA4212P

Right LED Board

Switch & CAP SENSE LEDs Board

Left LED Board



Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				MB Block Diagram	
Size	Document Number	Date		Rev	1.0
Custom	J1WA3/A4_LA-4212P	Monday, May 12, 2008		Sheet	2 of 53

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD	CAP BRD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@  
GM@  
X76@  
CARD@  
WLAN@  
HDMI@  
HDMI\_PM@  
HDMI\_GM@  
BT@

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>MB Notes List</b> Size B   Document Number: <b>J1WA3/A4_LA4212P</b>   Rev: 1.0 Date: Monday, May 12, 2008   Sheet 3 of 53

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

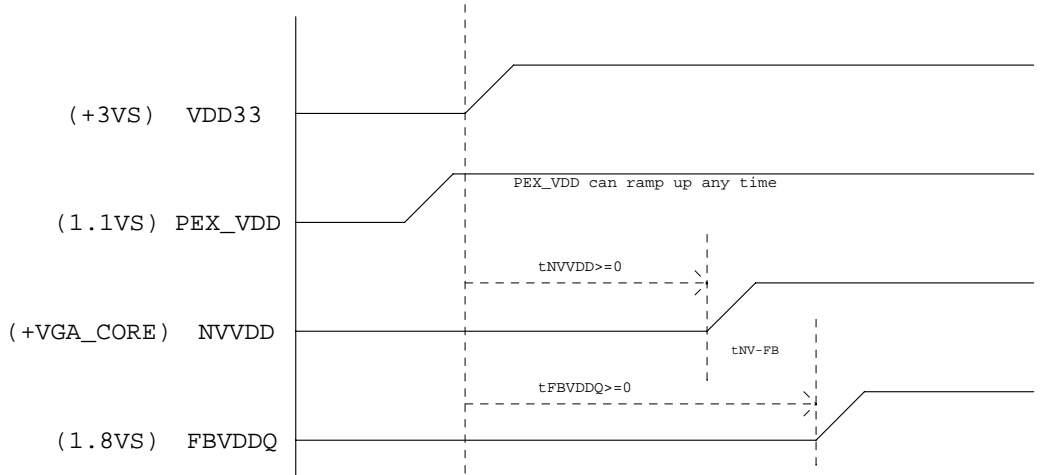
## EDP at Tj = 97C\*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)	Variable	GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVDD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
<b>TOTAL</b>	<b>1.1</b>	<b>3.225A</b>			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
<b>TOTAL</b>	<b>1.8</b>	<b>3.6A</b>	<b>2.24A</b>	<b>3.53A</b>	<b>2.2A</b>
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
<b>TOTAL</b>	<b>3.3</b>	<b>0.645A</b>			

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

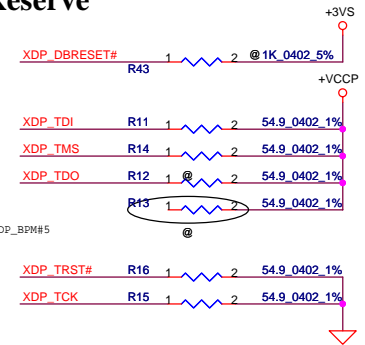
## POWER SEQUENCE

The ramp time for any rail must be more than 40us

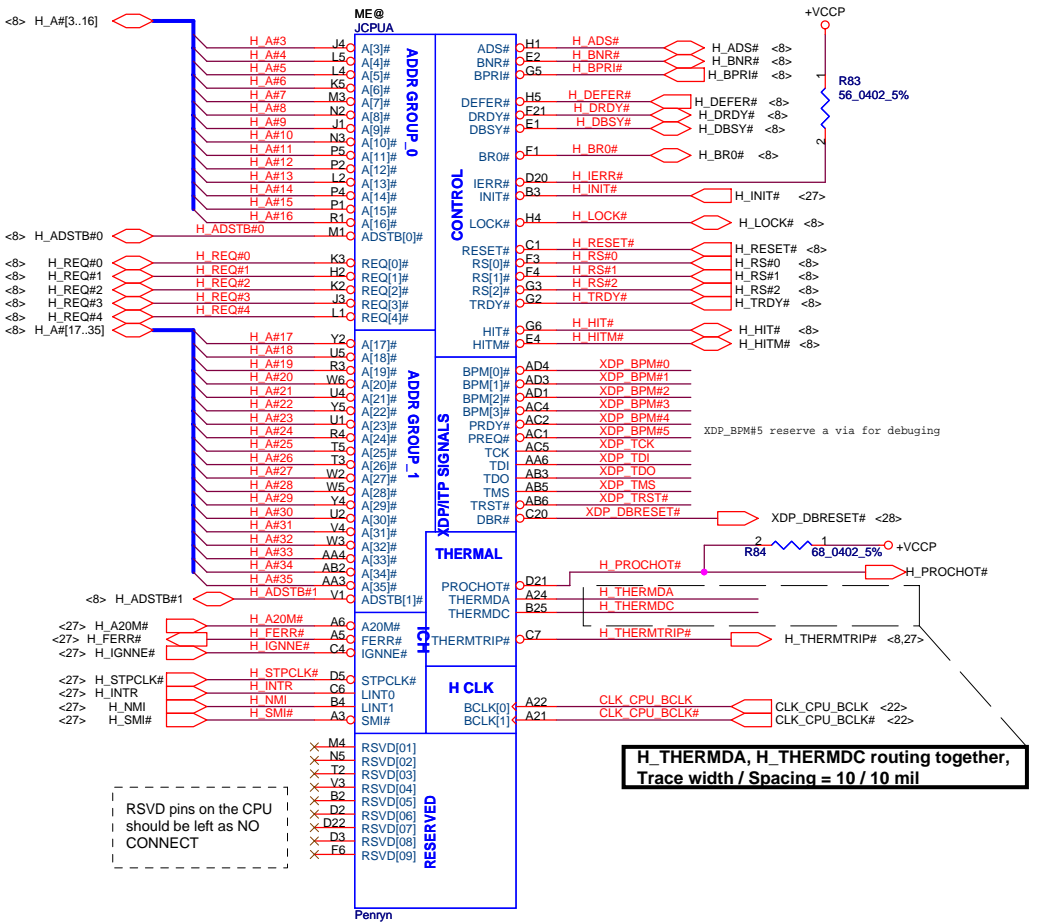
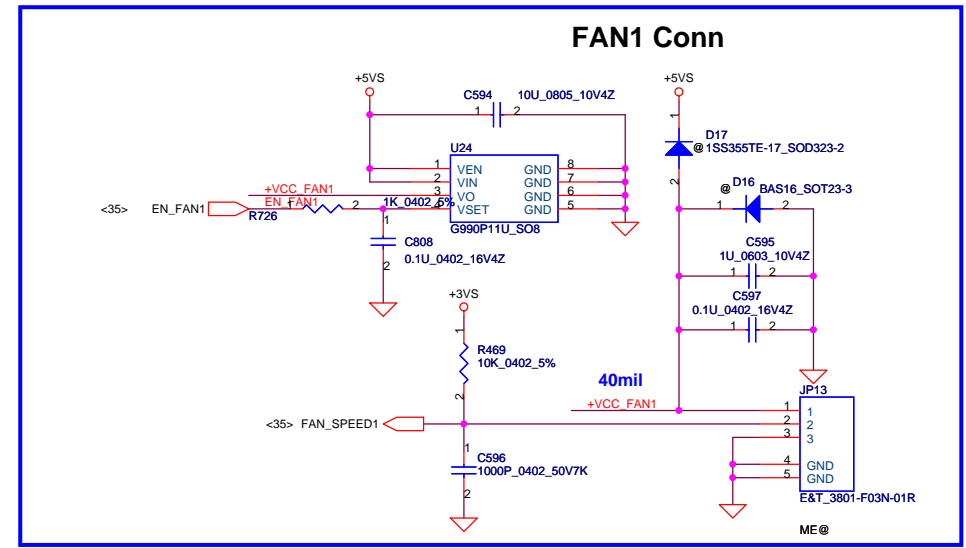
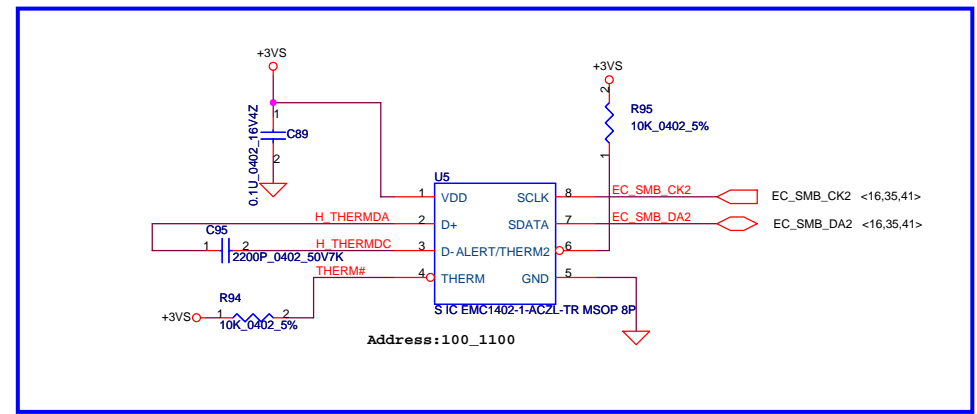


Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>Compal Electronics, Inc.</b> <b>VGA Notes List</b> Document Number: <b>J1WA3/A4_LA4212P</b> Date: Monday, May 12, 2008
Size B	Rev 1.0	Sheet 4	of 53	

# XDP Reserve



reserved by XDP\_BPM#5

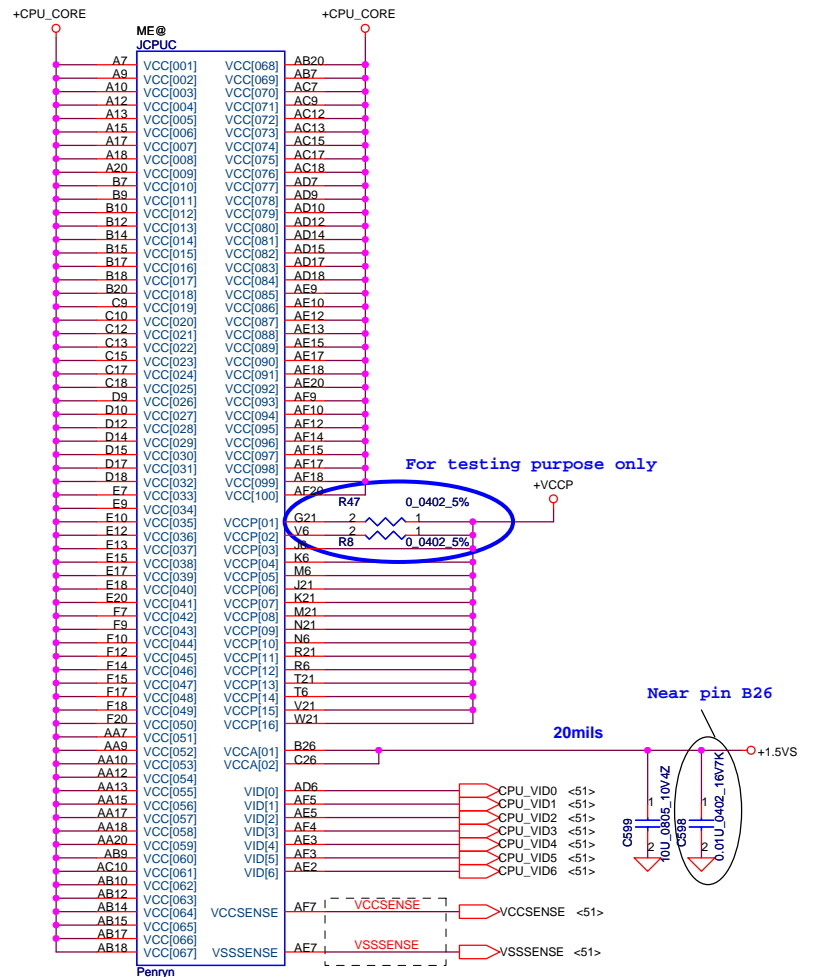
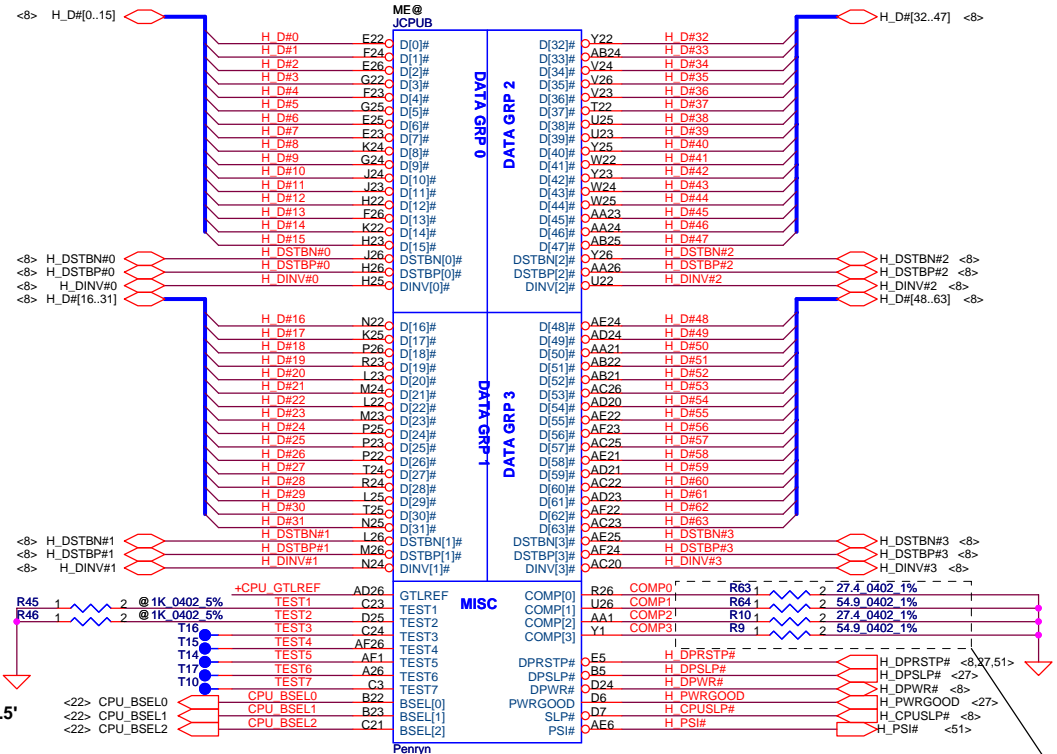


**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**

RSVD pins on the CPU should be left as NO CONNECT

Pennyn

Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Penryn (1/3)	
Size B	Document Number	Date:		Sheet	Rev
	J1WA3/A4_LA4212P	Wednesday, May 14, 2008		5	1.0
				of	53



Trace Close CPU < 0.5'

Width=4 mil,  
Spacing: 15mil  
(55Ohm)

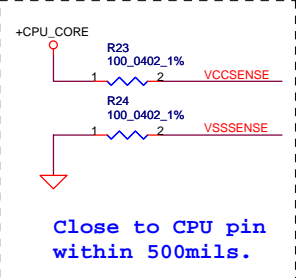
TRACE CLOSELY CPU < 0.5'  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

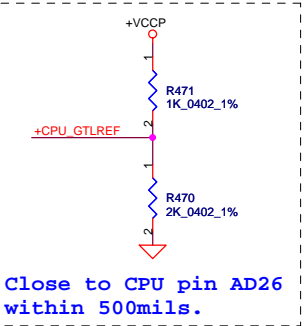
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.  
The trace width/space/other is 16/7/25.

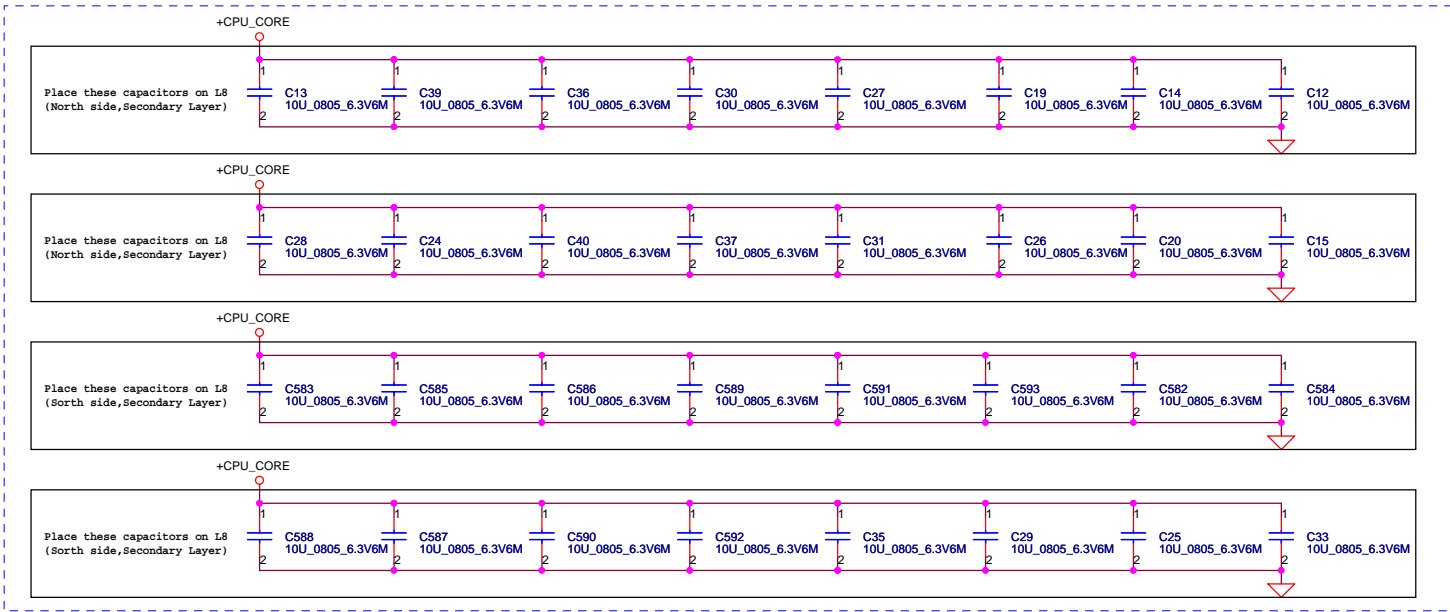
Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.



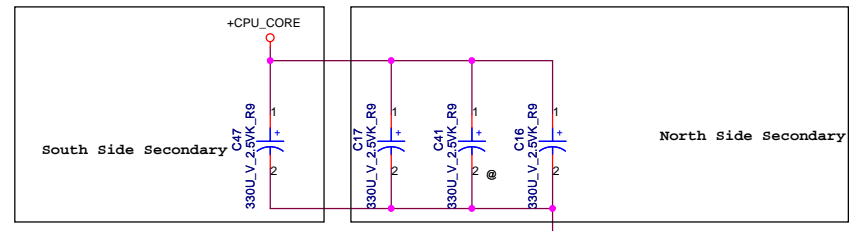
Layout note: Z0=55 ohm  
0.5" max for GTLREF.



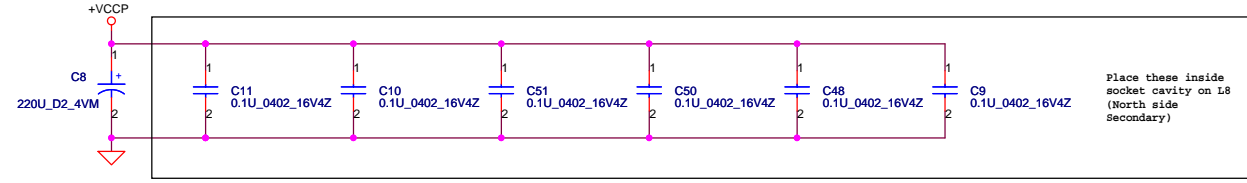
ME@		
JCPU0		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B8	VSS[009]	T4
B11	VSS[010]	T23
B13	VSS[011]	T26
B16	VSS[012]	U3
B19	VSS[013]	U6
B21	VSS[014]	U21
B24	VSS[015]	U24
C5	VSS[016]	V2
C8	VSS[017]	V5
C11	VSS[018]	V22
C14	VSS[019]	V25
C16	VSS[020]	V25
C19	VSS[021]	W1
C2	VSS[022]	W4
C22	VSS[023]	W23
C25	VSS[024]	W26
D1	VSS[025]	Y3
D4	VSS[026]	Y6
D8	VSS[027]	Y21
D11	VSS[028]	Y24
D13	VSS[029]	AA2
D16	VSS[030]	AA5
D19	VSS[031]	AA8
D23	VSS[032]	AA11
D26	VSS[033]	AA14
E3	VSS[034]	AA16
E6	VSS[035]	AA19
E8	VSS[036]	AA22
E11	VSS[037]	AA25
E14	VSS[038]	AB1
E16	VSS[039]	AB4
E19	VSS[040]	AB8
E21	VSS[041]	AB11
E24	VSS[042]	AB13
F5	VSS[043]	AB16
F8	VSS[044]	AB19
F11	VSS[045]	AB23
F13	VSS[046]	AB26
F16	VSS[047]	AC3
F19	VSS[048]	AC6
F2	VSS[049]	AC8
F22	VSS[050]	AC11
F25	VSS[051]	AC14
G4	VSS[052]	AC16
G1	VSS[053]	AC19
G23	VSS[054]	AC21
H3	VSS[055]	AC24
H6	VSS[056]	AD2
H21	VSS[057]	AD5
H24	VSS[058]	AD8
J2	VSS[059]	AD11
J5	VSS[060]	AD16
J22	VSS[061]	AD19
J25	VSS[062]	AD22
K1	VSS[063]	AD25
K4	VSS[064]	AE1
K23	VSS[065]	AE4
K26	VSS[066]	AE8
L3	VSS[067]	AE11
L6	VSS[068]	AE14
L21	VSS[069]	AE16
L24	VSS[070]	AE19
M2	VSS[071]	AE23
M5	VSS[072]	AE26
M22	VSS[073]	A2
M25	VSS[074]	AF6
N1	VSS[075]	AF8
N4	VSS[076]	AF11
N23	VSS[077]	AF13
N26	VSS[078]	AF16
P3	VSS[079]	AF19
	VSS[080]	AF21
	VSS[081]	A25
	VSS[082]	AF25
	VSS[083]	
	VSS[084]	
	VSS[085]	
	VSS[086]	
	VSS[087]	
	VSS[088]	
	VSS[089]	
	VSS[090]	
	VSS[091]	
	VSS[092]	
	VSS[093]	
	VSS[094]	
	VSS[095]	
	VSS[096]	
	VSS[097]	
	VSS[098]	
	VSS[099]	
	VSS[100]	
	VSS[101]	
	VSS[102]	
	VSS[103]	
	VSS[104]	
	VSS[105]	
	VSS[106]	
	VSS[107]	
	VSS[108]	
	VSS[109]	
	VSS[110]	
	VSS[111]	
	VSS[112]	
	VSS[113]	
	VSS[114]	
	VSS[115]	
	VSS[116]	
	VSS[117]	
	VSS[118]	
	VSS[119]	
	VSS[120]	
	VSS[121]	
	VSS[122]	
	VSS[123]	
	VSS[124]	
	VSS[125]	
	VSS[126]	
	VSS[127]	
	VSS[128]	
	VSS[129]	
	VSS[130]	
	VSS[131]	
	VSS[132]	
	VSS[133]	
	VSS[134]	
	VSS[135]	
	VSS[136]	
	VSS[137]	
	VSS[138]	
	VSS[139]	
	VSS[140]	
	VSS[141]	
	VSS[142]	
	VSS[143]	
	VSS[144]	
	VSS[145]	
	VSS[146]	
	VSS[147]	
	VSS[148]	
	VSS[149]	
	VSS[150]	
	VSS[151]	
	VSS[152]	
	VSS[153]	
	VSS[154]	
	VSS[155]	
	VSS[156]	
	VSS[157]	
	VSS[158]	
	VSS[159]	
	VSS[160]	
	VSS[161]	
	VSS[162]	
	VSS[163]	



Mid Frequency Decoupling



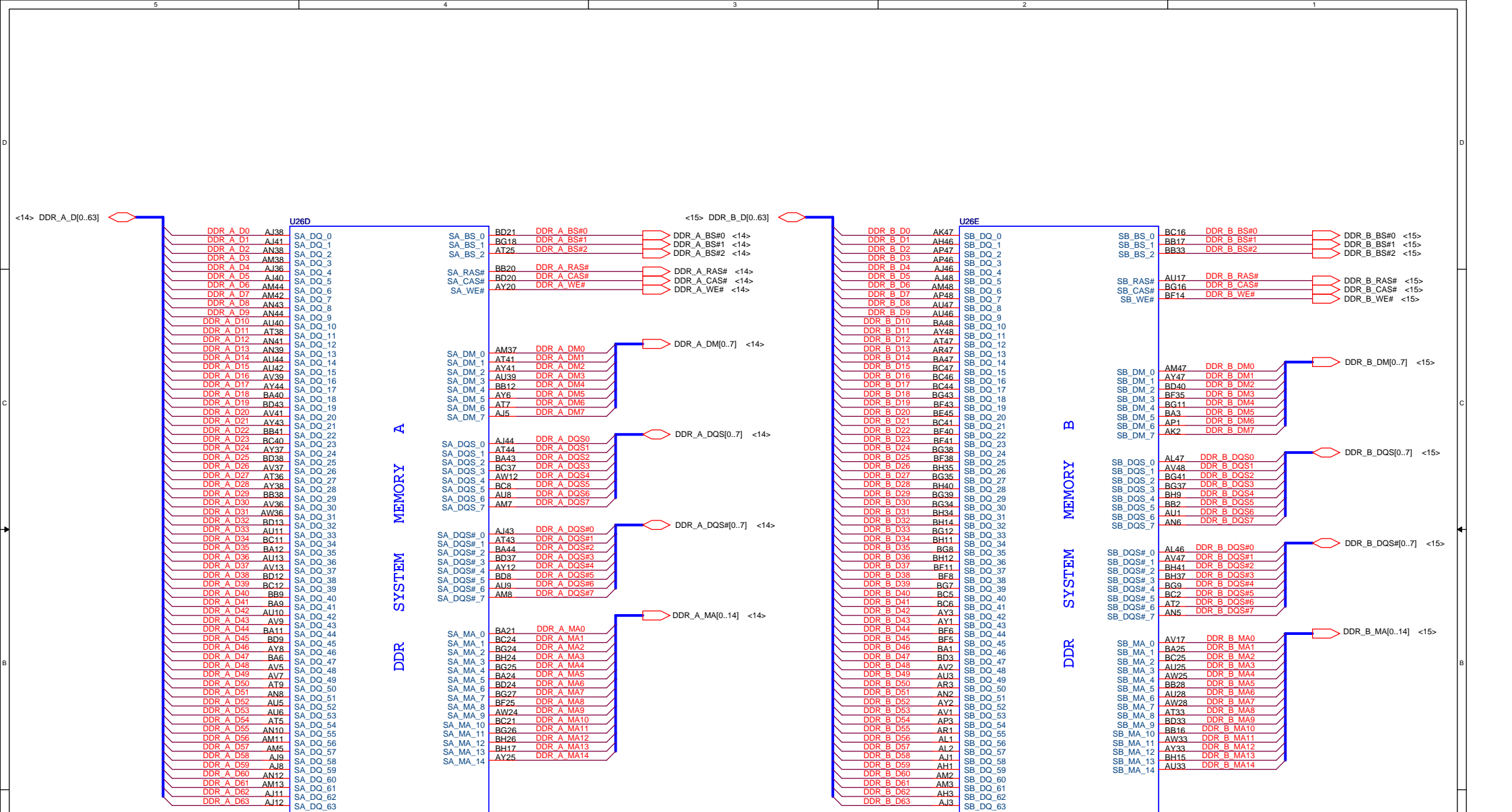
ESR <= 1.5m ohm  
Capacitor > 1980uF



Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Penryn (3/3)	
Size B	Document Number	Date		Rev	1.0
	J1WA3/A4_LA4212P	Monday, May 12, 2008	Sheet 7 of 53		







CANTIGA ES\_FCBGA1329

CANTIGA ES\_FCBGA1329

GM®

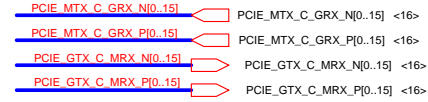
GM®

Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
				Cantiga GMCH (2/6)-DDRII	
Size	Document Number			Rev	
B	J1WA3/A4_LA4212P			1.0	
Date:	Wednesday, May 14, 2008	Sheet	9	of 53	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

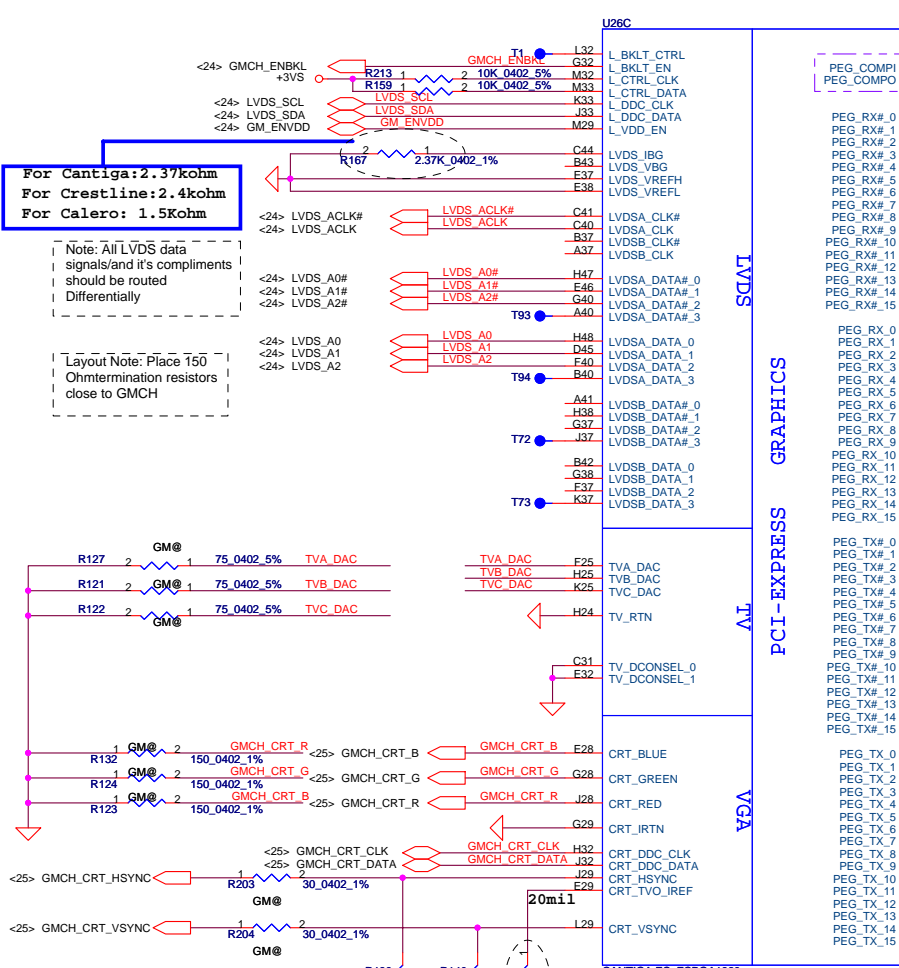
## Strap Pin Table

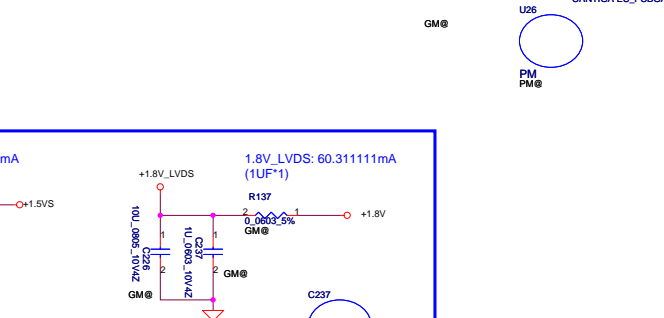
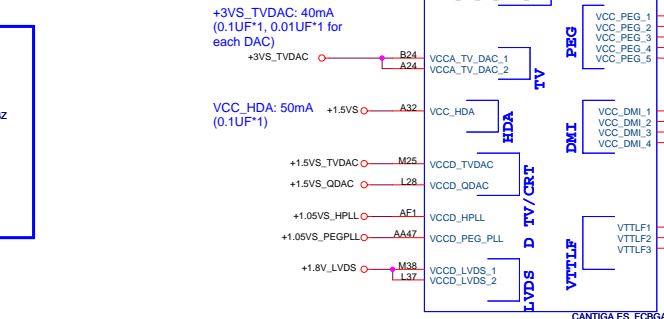
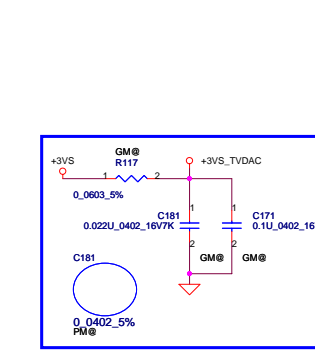
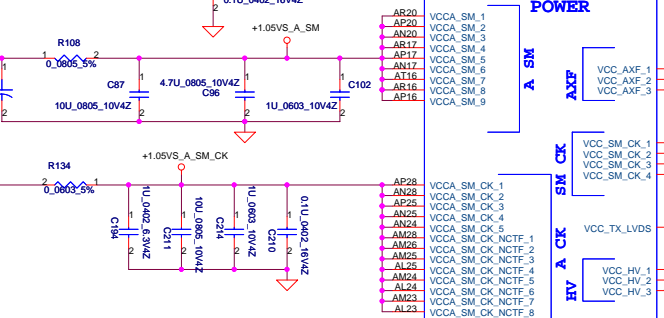
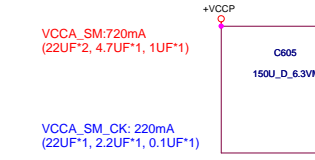
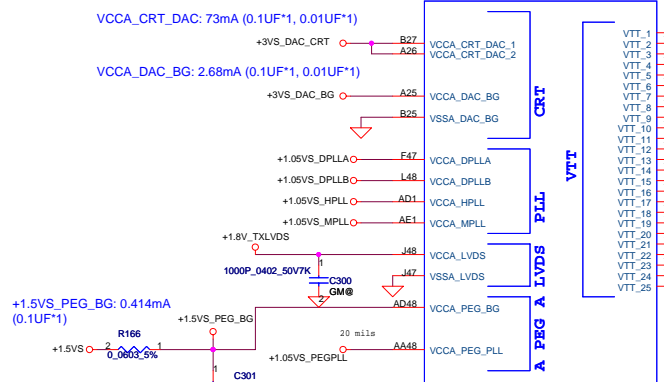
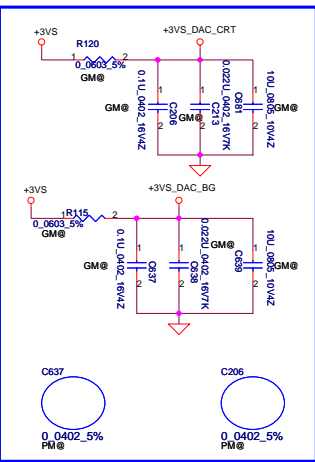
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipset suite with no confidentiality 1=(TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane (Lane number in Order)
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *

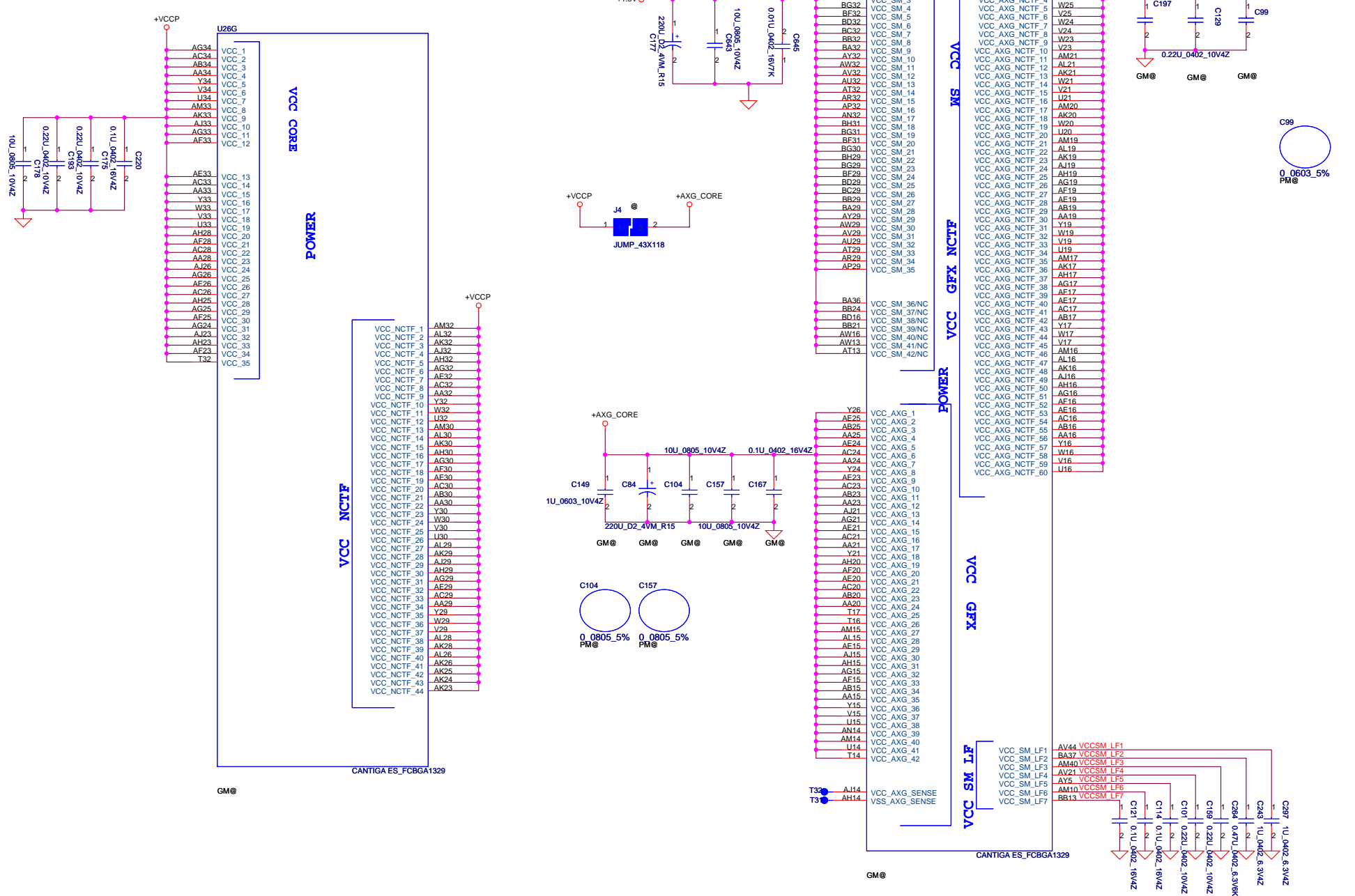


Place the resistor within 500mils (1.27mm) of the (G)MCH  
PEGCOMP trace width and spacing is 20/25 mils.

Please check Power source if want support IAMT

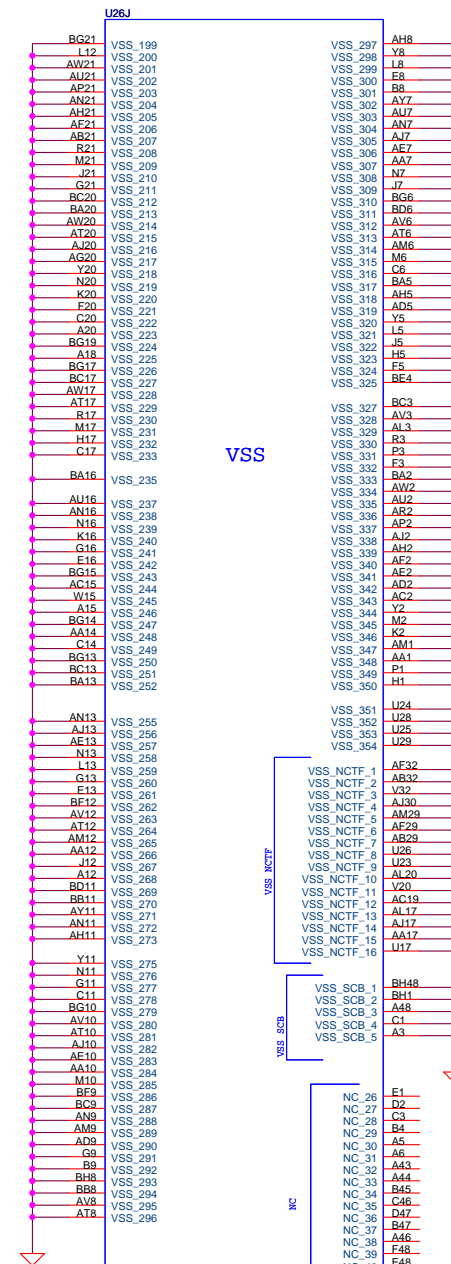
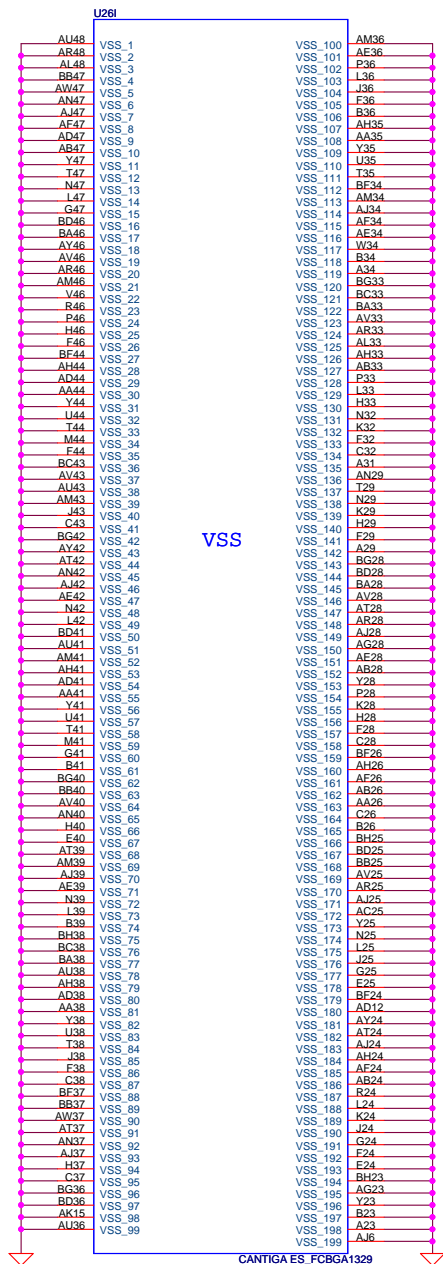






Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Crestline GMCH (5/6)-VCC	
Size	Document Number	Customer	Revision	Date	
	J1WA3/A4 LA4212P		1.0	Wednesday, May 14, 2008	
			Sheet	12	of 53

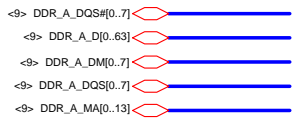
hexainf@hotmail.com  
gratuito - free of charge.



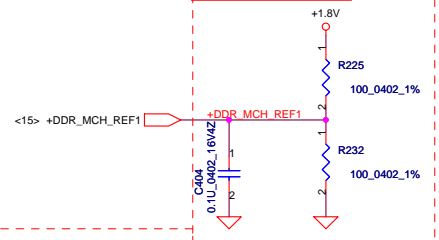
hexainf@hotmail.com  
gratuito - free of charge.

Security Classification		Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date	2008/10/15
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>			

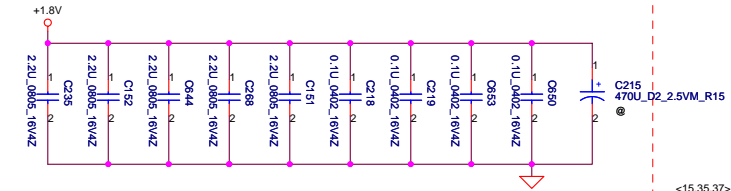
Compal Electronics, Inc.			
Title <b>Cantiga GMCH (6/6)-GND</b>			
Size	Document Number	Rev	
Custom	J1WA3/A4_LA4212P	1.0	
Date:	Wednesday, May 14, 2008	Sheet	13 of 53



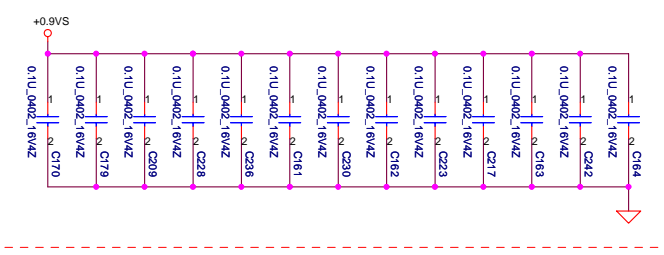
**Layout Note:**  
+DDR\_MCH\_REF trace width and spacing is 20/20.



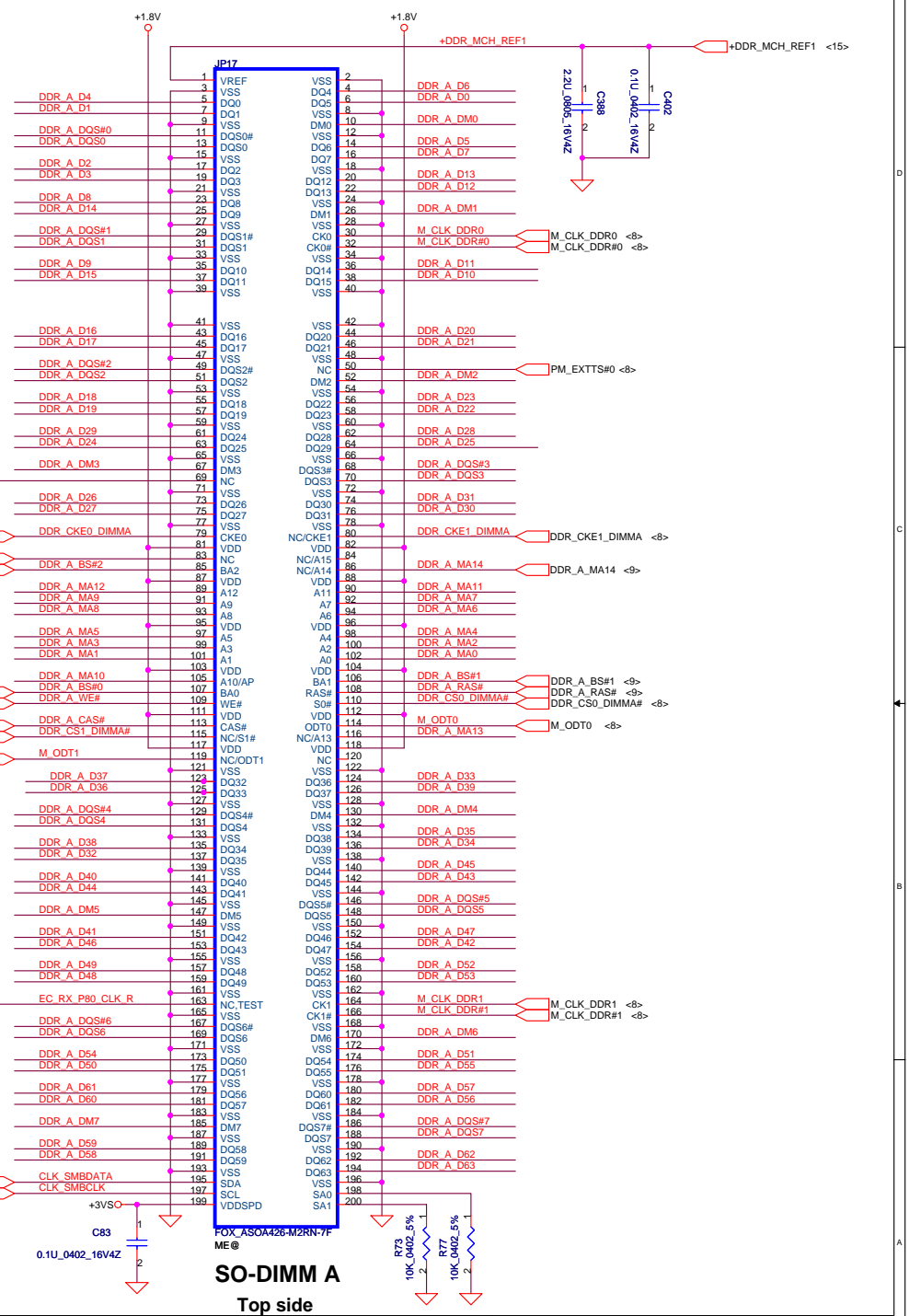
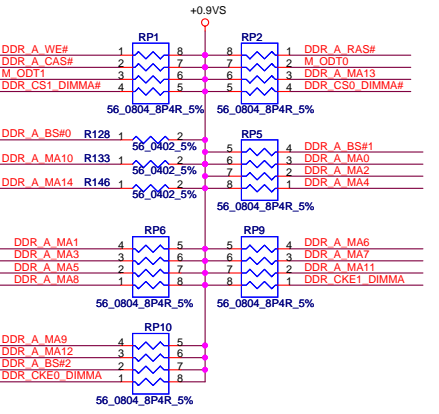
**Layout Note:**  
Place near JP41



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

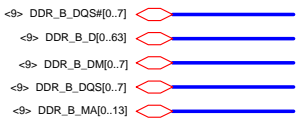


**Layout Note:**  
Place these resistor closely JP41, all trace length Max=1.5"

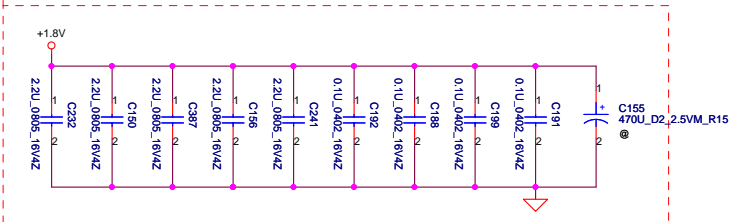


**SO-DIMM A**  
Top side

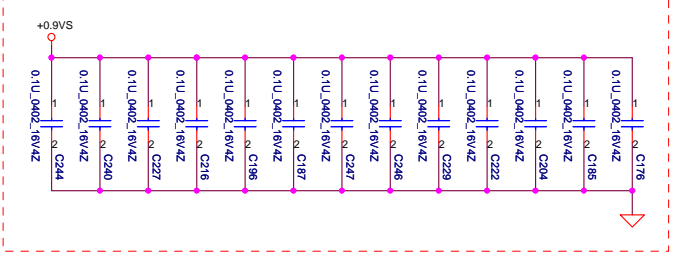
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b>
				<b>DDRII-SODIMM SLOT1</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Custort	Document Number <b>J1WA3/A4_LA421P</b>
			Date:	Monday, May 12, 2008
			Sheet	14 of 53
			Rev	1.0



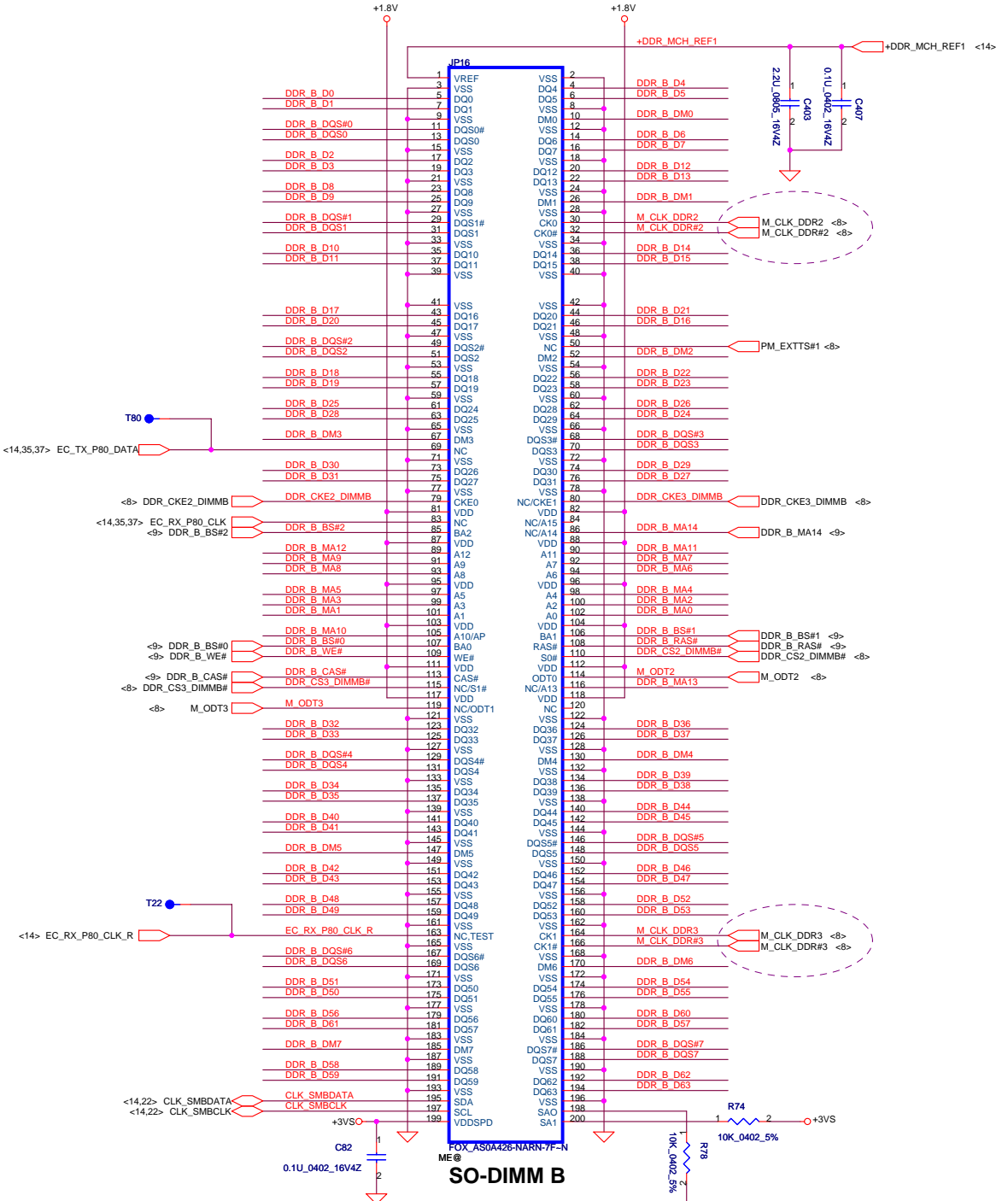
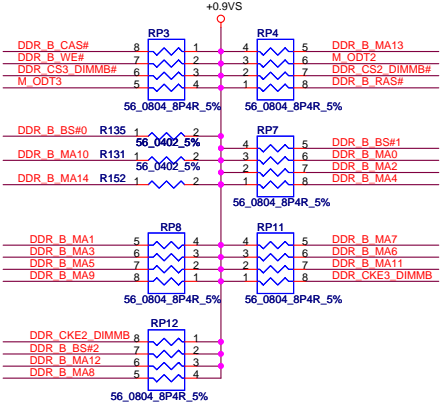
**Layout Note:**  
Place near JP42



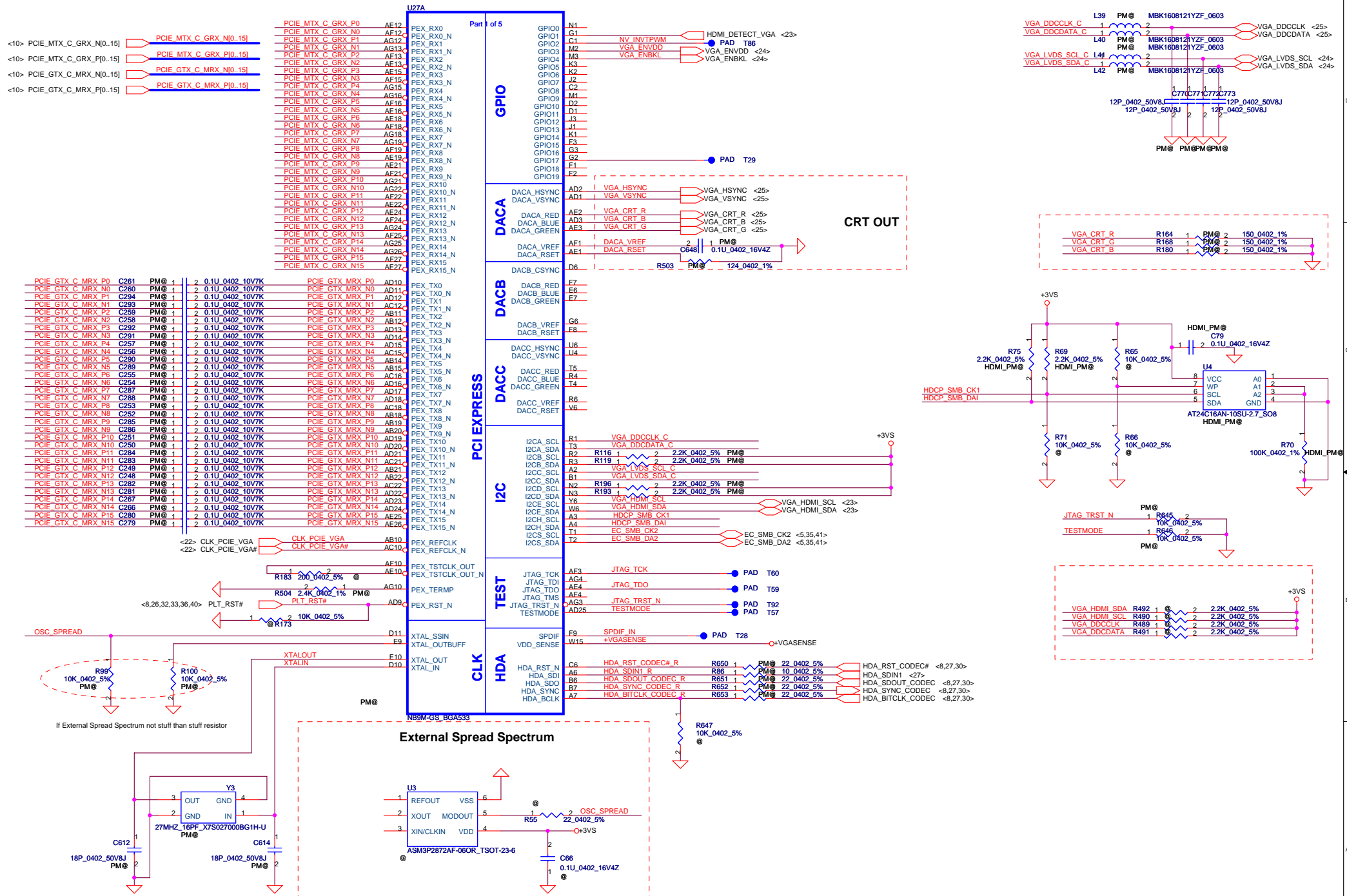
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP42, all trace length Max=1.5"



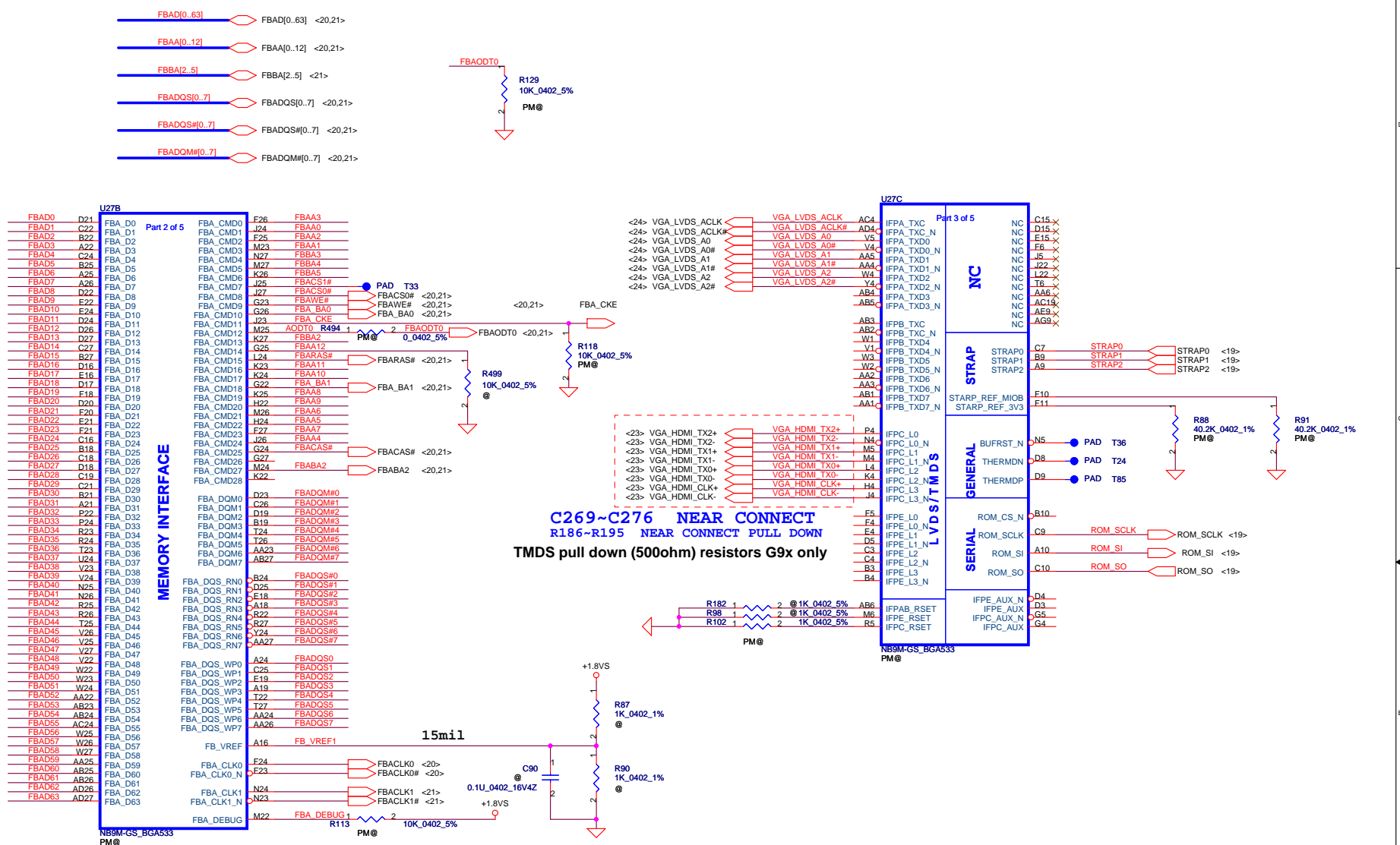
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b>	
				<b>DDRII-SODIMM SLOT2</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPANY OR DIVISION OF BOARD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				J1WA3/A4_LA4212P	
				Date:	Monday, May 12, 2008
				Sheet	15 of 53
				Rev	1.0



Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	NB9M-GS PCIE, LVDS, GPIO, CLK	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size B	Document Number	Date:		Rev	
J1W3/A4_LA4212P	Wednesday, May 14, 2008	[Sheet 16 of 53]		1.0	

hexainf@hotmail.com  
gratuito - free of charge.





**U27B**

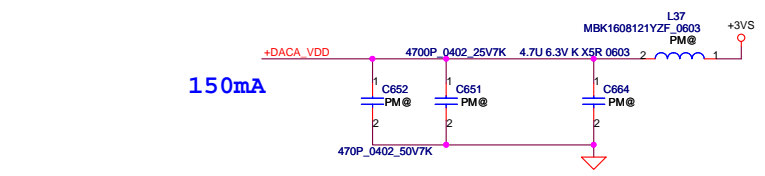
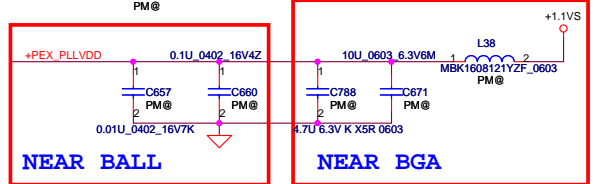
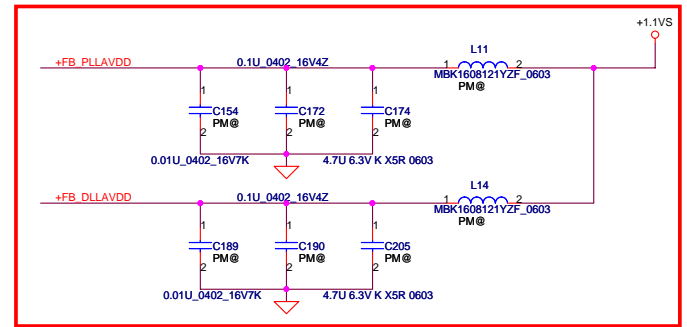
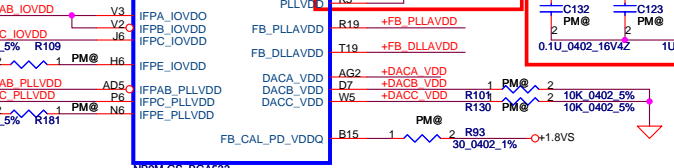
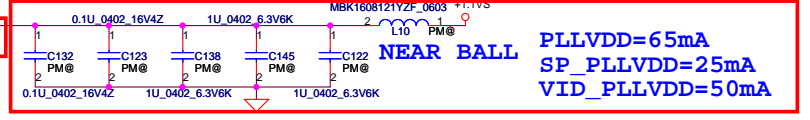
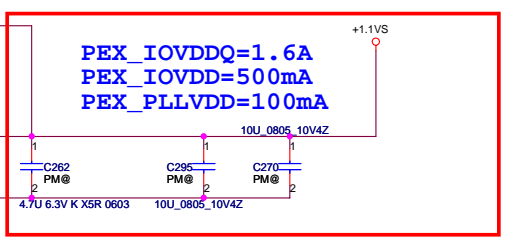
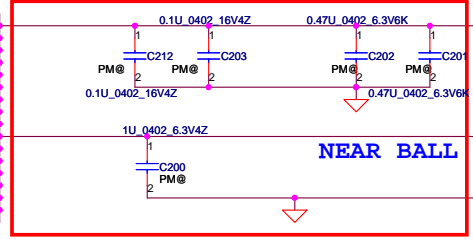
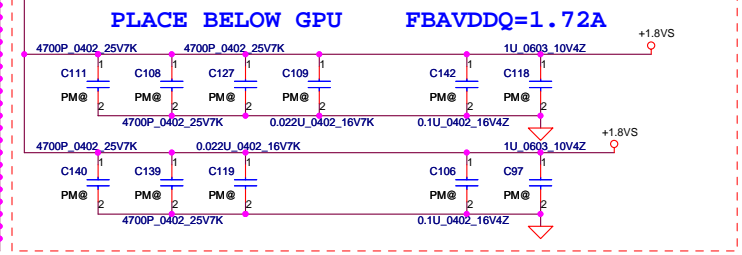
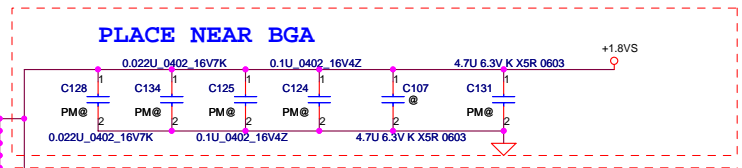
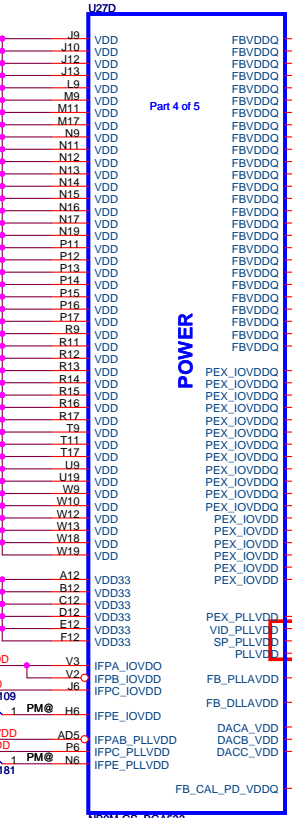
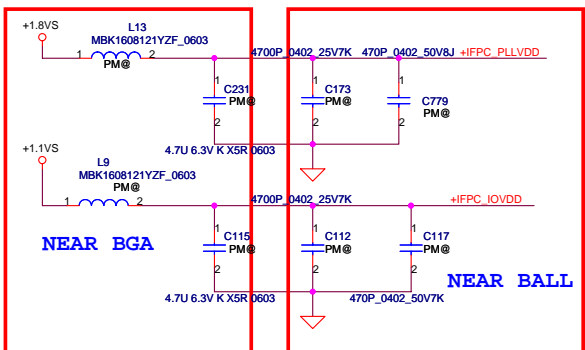
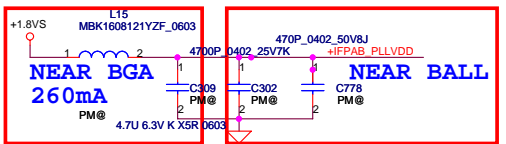
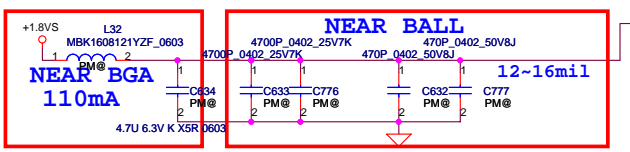
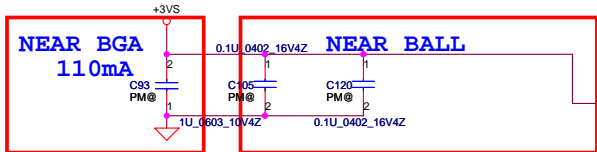
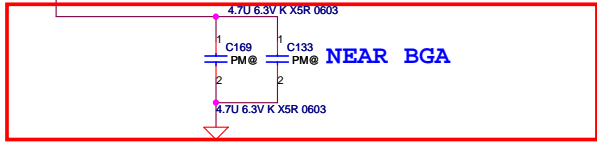
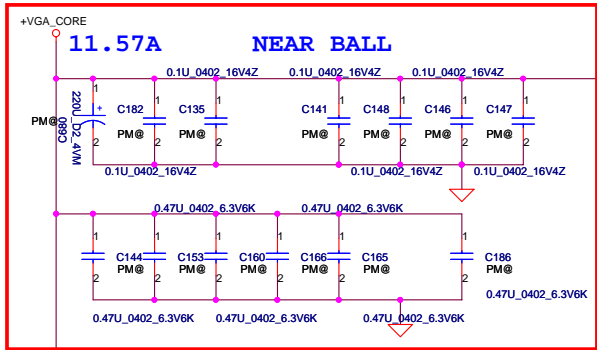
FBAD0	D21	FBA_D0
FBAD1	C22	FBA_D1
FBAD2	B22	FBA_D2
FBAD3	A22	FBA_D3
FBAD4	C24	FBA_D4
FBAD5	B25	FBA_D5
FBAD6	A25	FBA_D6
FBAD7	A26	FBA_D7
FBAD8	E22	FBA_D8
FBAD9	E22	FBA_D9
FBAD10	E24	FBA_D10
FBAD11	D24	FBA_D11
FBAD12	D26	FBA_D12
FBAD13	D27	FBA_D13
FBAD14	C27	FBA_D14
FBAD15	B27	FBA_D15
FBAD16	D16	FBA_D16
FBAD17	E16	FBA_D17
FBAD18	D17	FBA_D18
FBAD19	E18	FBA_D19
FBAD20	D20	FBA_D20
FBAD21	E20	FBA_D21
FBAD22	E21	FBA_D22
FBAD23	F21	FBA_D23
FBAD24	C16	FBA_D24
FBAD25	B18	FBA_D25
FBAD26	C18	FBA_D26
FBAD27	D18	FBA_D27
FBAD28	C19	FBA_D28
FBAD29	C21	FBA_D29
FBAD30	B21	FBA_D30
FBAD31	A21	FBA_D31
FBAD32	P22	FBA_D32
FBAD33	P24	FBA_D33
FBAD34	R23	FBA_D34
FBAD35	R24	FBA_D35
FBAD36	T23	FBA_D36
FBAD37	U24	FBA_D37
FBAD38	V23	FBA_D38
FBAD39	V24	FBA_D39
FBAD40	N25	FBA_D40
FBAD41	N26	FBA_D41
FBAD42	R25	FBA_D42
FBAD43	R26	FBA_D43
FBAD44	T25	FBA_D44
FBAD45	V26	FBA_D45
FBAD46	V25	FBA_D46
FBAD47	V27	FBA_D47
FBAD48	V22	FBA_D48
FBAD49	W22	FBA_D49
FBAD50	W23	FBA_D50
FBAD51	W24	FBA_D51
FBAD52	AA22	FBA_D52
FBAD53	AB23	FBA_D53
FBAD54	AB24	FBA_D54
FBAD55	AC24	FBA_D55
FBAD56	W25	FBA_D56
FBAD57	W26	FBA_D57
FBAD58	W27	FBA_D58
FBAD59	AA25	FBA_D59
FBAD60	AB25	FBA_D60
FBAD61	AB26	FBA_D61
FBAD62	AD26	FBA_D62
FBAD63	AD27	FBA_D63

**U27C**

FBA_CMD0	J24	FBA_A0
FBA_CMD1	E25	FBA_A2
FBA_CMD2	M23	FBA_A1
FBA_CMD3	N27	FBA_A3
FBA_CMD4	M27	FBA_A4
FBA_CMD5	K26	FBA_A5
FBA_CMD6	J25	FBA_C5#
FBA_CMD7	J27	FBA_C5#
FBA_CMD8	G23	FBA_WE#
FBA_CMD9	G26	FBA_BA0
FBA_CMD10	J23	FBA_CKE
FBA_CMD11	M25	AD0T0
FBA_CMD12	K27	FBA_A2
FBA_CMD13	G25	FBA_A12
FBA_CMD14	L24	FBA_RAS#
FBA_CMD15	K23	FBA_A11
FBA_CMD16	K24	FBA_A10
FBA_CMD17	G22	FBA_BA1
FBA_CMD18	K25	FBA_A8
FBA_CMD19	H22	FBA_A9
FBA_CMD20	M26	FBA_A6
FBA_CMD21	H24	FBA_A5
FBA_CMD22	E27	FBA_A7
FBA_CMD23	J26	FBA_A4
FBA_CMD24	G24	FBA_CAS#
FBA_CMD25	G27	FBA_CAS#
FBA_CMD26	M24	FBA_BA2
FBA_CMD27	M24	FBA_BA2
FBA_CMD28	K22	FBA_BA2
FBA_CMD29	D23	FBA_DQM#0
FBA_CMD30	C26	FBA_DQM#1
FBA_CMD31	D19	FBA_DQM#2
FBA_CMD32	B19	FBA_DQM#3
FBA_CMD33	T24	FBA_DQM#4
FBA_CMD34	T26	FBA_DQM#5
FBA_CMD35	AA23	FBA_DQM#6
FBA_CMD36	AB27	FBA_DQM#7
FBA_CMD37	R24	FBA_DQS#0
FBA_CMD38	D25	FBA_DQS#1
FBA_CMD39	E18	FBA_DQS#2
FBA_CMD40	A18	FBA_DQS#3
FBA_CMD41	R22	FBA_DQS#4
FBA_CMD42	R27	FBA_DQS#5
FBA_CMD43	Y24	FBA_DQS#6
FBA_CMD44	AA27	FBA_DQS#7
FBA_CMD45	A24	FBA_DQS#0
FBA_CMD46	C25	FBA_DQS#1
FBA_CMD47	E19	FBA_DQS#2
FBA_CMD48	A19	FBA_DQS#3
FBA_CMD49	T22	FBA_DQS#4
FBA_CMD50	T27	FBA_DQS#5
FBA_CMD51	AA24	FBA_DQS#6
FBA_CMD52	AA26	FBA_DQS#7
FBA_CMD53	A16	FBA_VREF1
FBA_CMD54	E24	FBA_CLK0
FBA_CMD55	E23	FBA_CLK0#
FBA_CMD56	N24	FBA_CLK1
FBA_CMD57	N23	FBA_CLK1#
FBA_CMD58	M22	FBA_DEBUG1

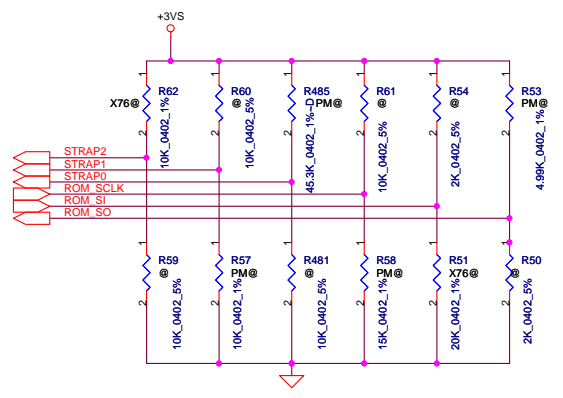
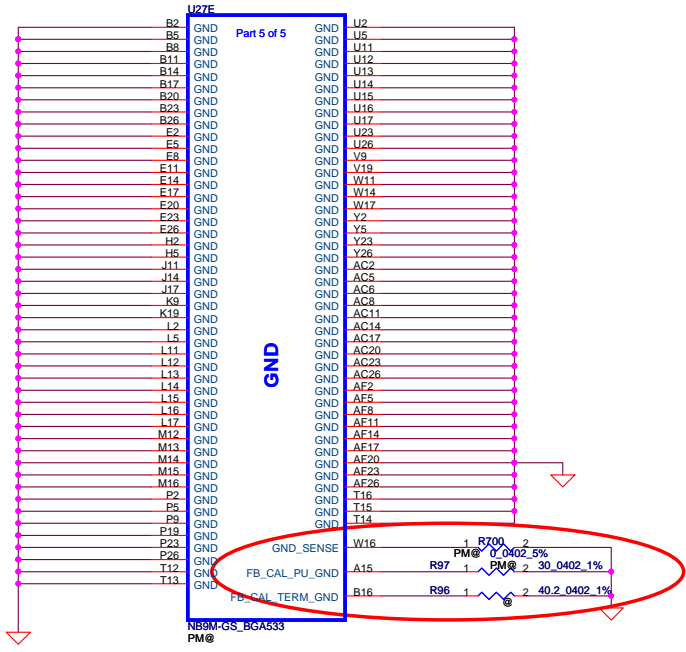
**C269-C276 NEAR CONNECT**  
**R186-R195 NEAR CONNECT PULL DOWN**  
**TMDs pull down (500ohm) resistors G9x only**

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>NB9M-GS Memory</b> Size B Document Number J1WA3/A4_LA4212P Date: Monday, May 12, 2008
				Rev 1.0 Sheet 17 of 53



Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 1.0	
Customer				JWJA3/A4_LA4212P	
Date:	Monday, May 12, 2008	Sheet	18	of 53	

A total of 8 signals are required for GB1 strapping this includes  
 2 reference signals  
 6 physical strapping pins  
 4 logical strapping bits  
 A total of 24 logical strapping bits are available

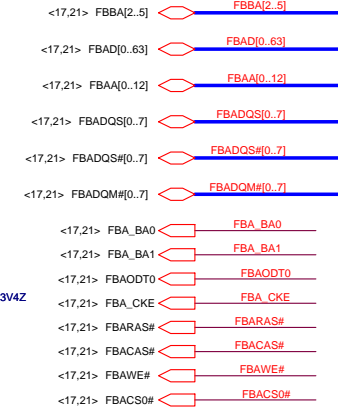
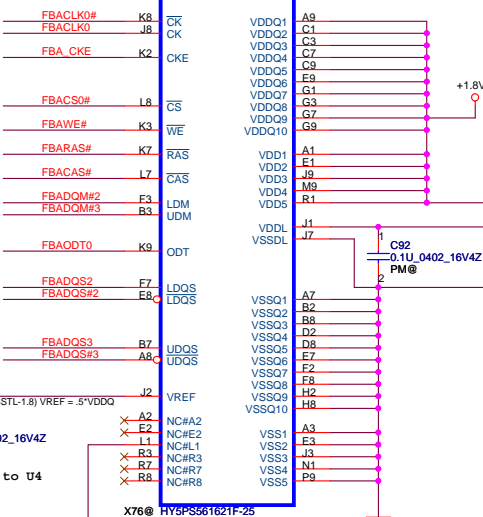
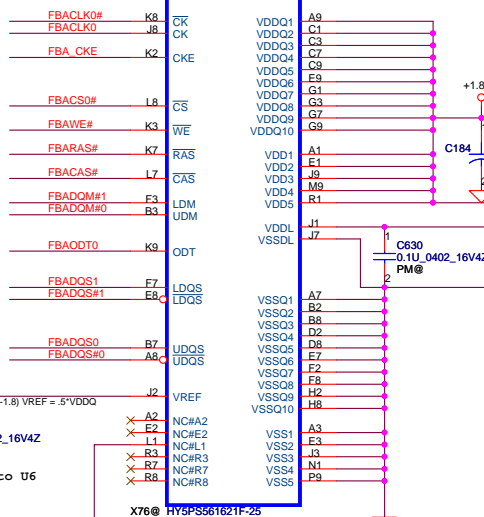
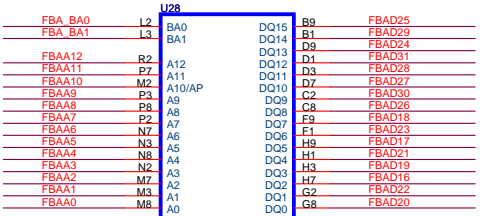
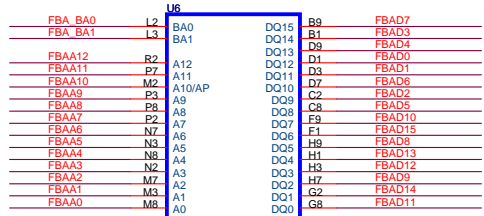


GB1 Family GPU Strap Options

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
NB9M-GS (0x06E9)	Samsung	32Mx16 (5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K
		64Mx16	PU 5K	PD 15K	PD 5K	PU 10K	PD 10K	PU 45K
	Hynix	32Mx16 (7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
		64Mx16	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	Qimonda	32Mx16 (6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K

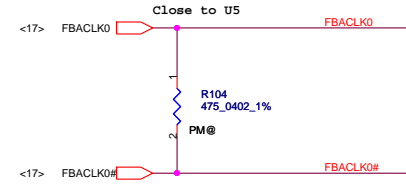
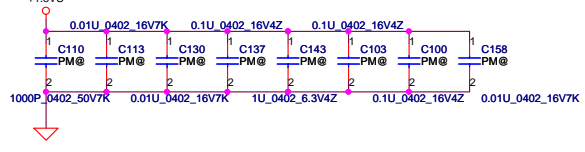
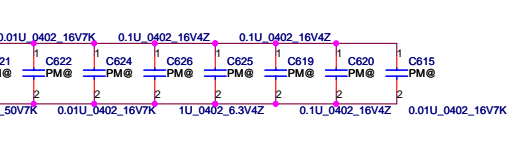
Component	Manufacturer	Compal PN
DDR2 VRAM (32M*16)	Hynix	SA00000FF30
	Qimonda	SA00000S820
	Samsung	SA00001VX10

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>NB9M-GE GND &amp; STRAP</b>		
Issued Date	2007/10/15	Deciphered Date	2008/10/15			
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size B	Document Number JIWA3/A4_LA4212P	Rev 1.0
				Date: Monday, May 12, 2008	Sheet 19 of 53	



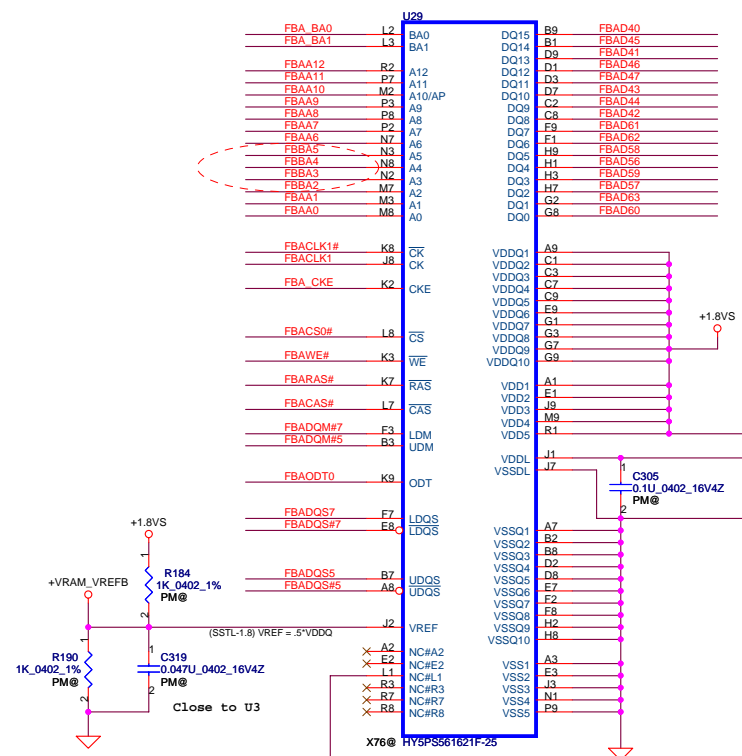
DDR2 BGA MEMORY

DDR2 BGA MEMORY

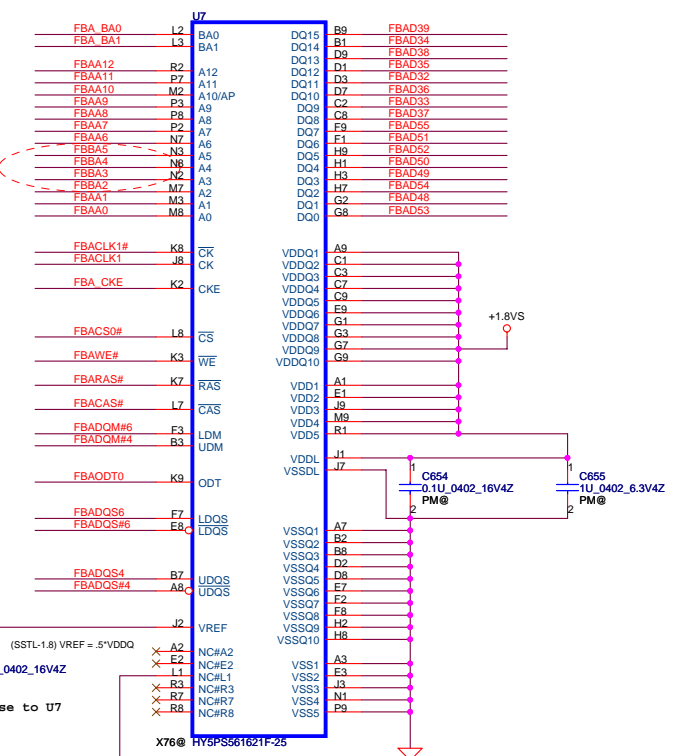


Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>		

<p align="center"><b>Compal Electronics, Inc.</b></p> <p align="center"><b>VRAM DDRA</b></p>		
Title	Size	Rev
	Custom	1.0
Date:	Monday, May 12, 2008	Sheet 20 of 53

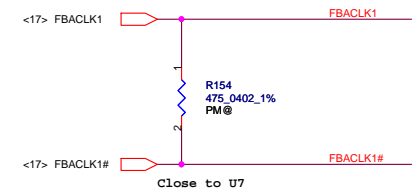
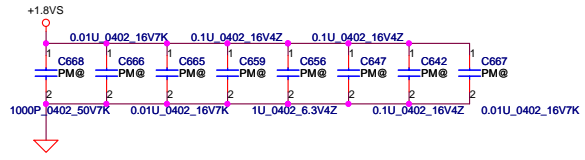
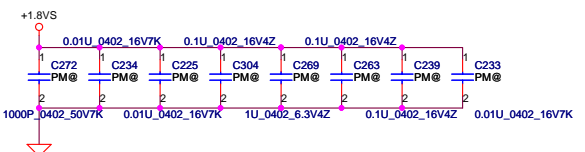


DDR2 BGA MEMORY



DDR2 BGA MEMORY

- <17,20> FBAD[0..63] FBAD[0..63]
- <17,20> FBAA[0..12] FBAA[0..12]
- <17> FBBA[2..5] FBBA[2..5]
- <17,20> FBADQS[0..7] FBADQS[0..7]
- <17,20> FBADQM[0..7] FBADQM[0..7]
- <17,20> FBA\_BA0 FBA\_BA0
- <17,20> FBA\_BA1 FBA\_BA1
- <17,20> FBAODT0 FBAODT0
- <17,20> FBA\_CKE FBA\_CKE
- <17,20> FBARAS# FBARAS#
- <17,20> FBACAS# FBACAS#
- <17,20> FBAWE# FBAWE#
- <17,20> FBACSO# FBACSO#

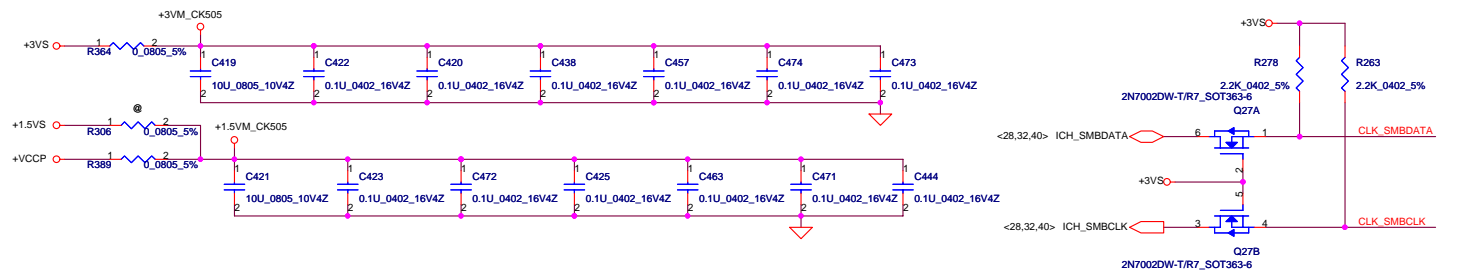


Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15

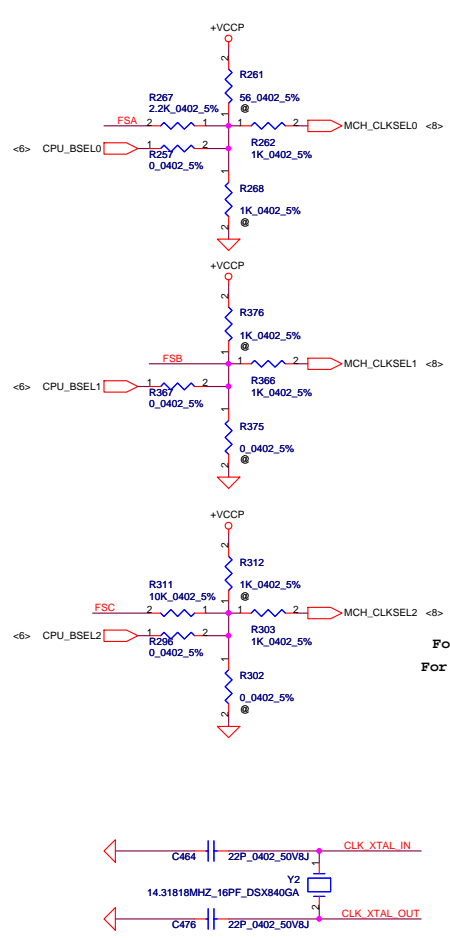
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title			<b>Compal Electronics, Inc.</b>	
			<b>VRAM DDRB</b>	
Size	Document Number		Rev	
Custom	J1WA3/A4_LA4212P		1.0	
Date:	Monday, May 12, 2008	Sheet	21	of 53

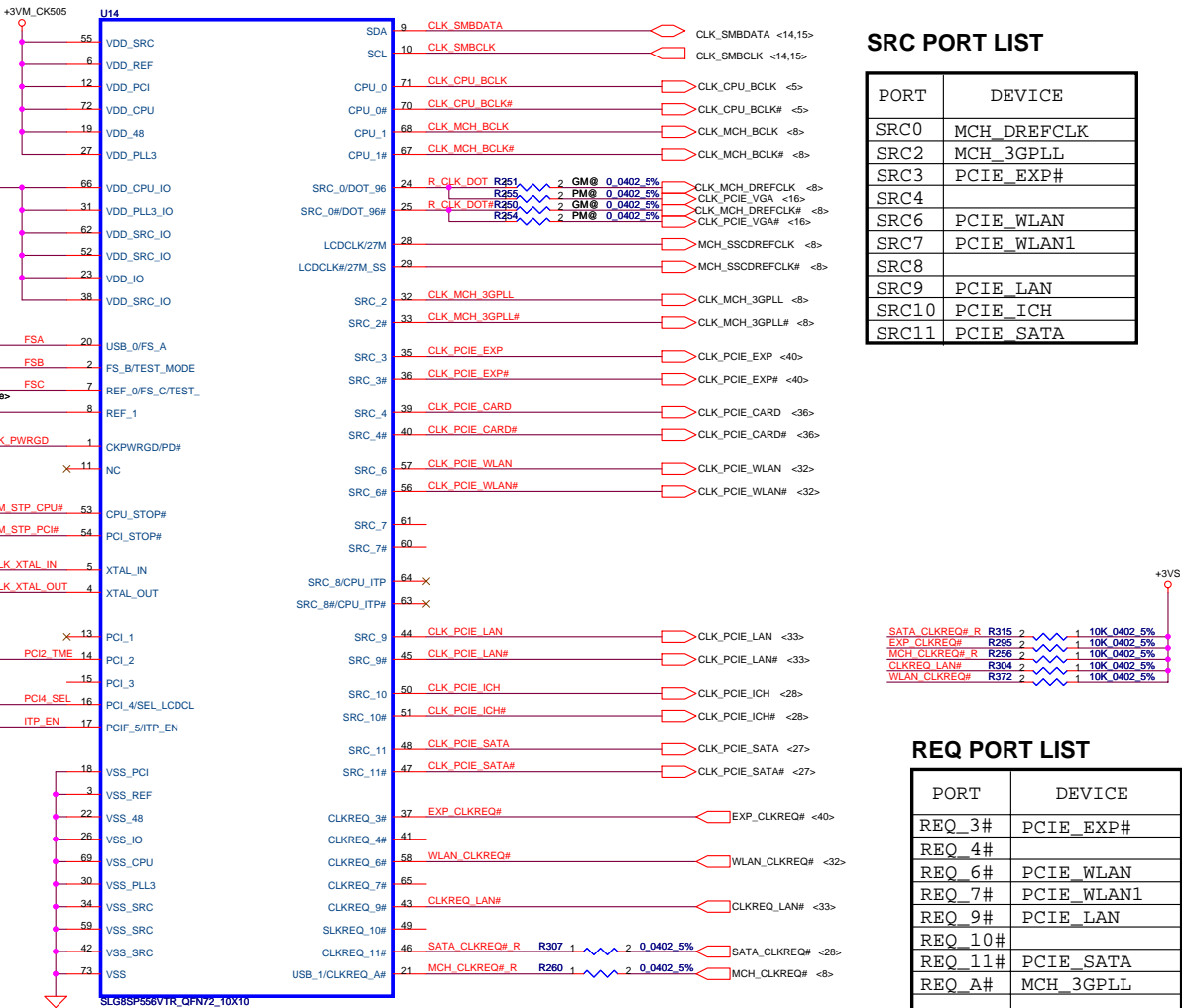
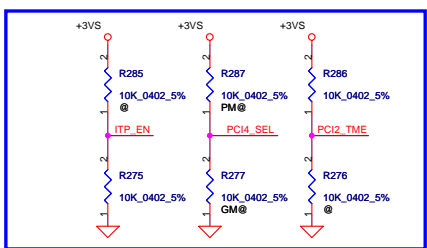
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



SA000020K00 (Silego : SLG8SP556VTR )  
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP\_EN, 0 = SRC8 / SRC8#; 1 = ITP / ITP#  
For PCI4\_SEL, 0 = Pin24 / 25 : DOT96 / DOT96#  
Pin28 / 29 : LCDCLK / LCDCLK#  
1 = Pin24 / 25 : SRC\_0 / SRC\_0#  
Pin28 / 29 : 27M / 27M\_SS



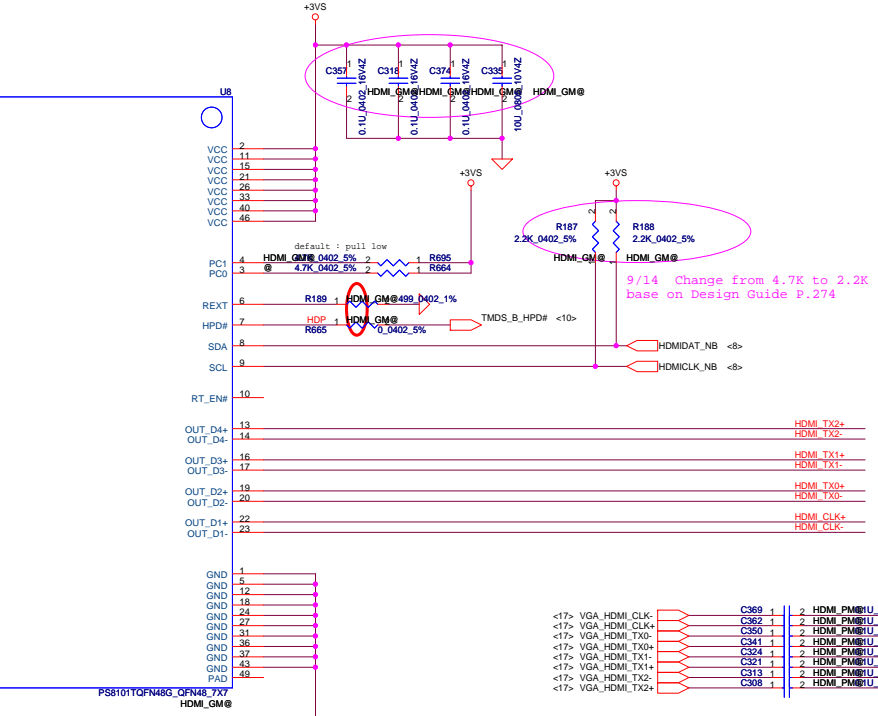
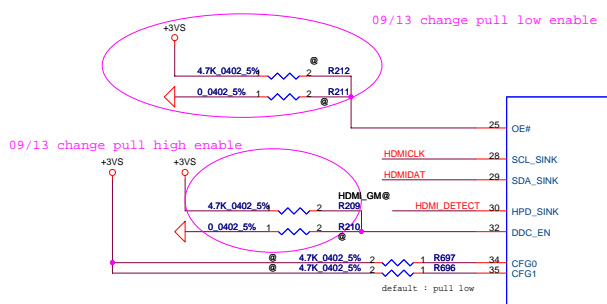
**SRC PORT LIST**

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

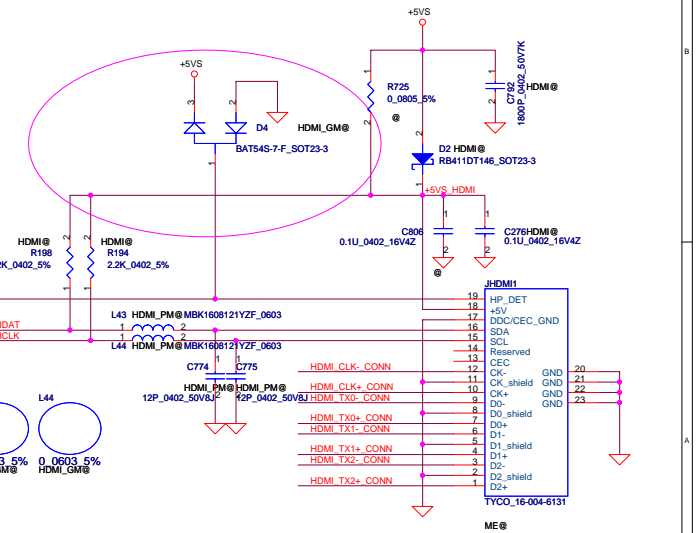
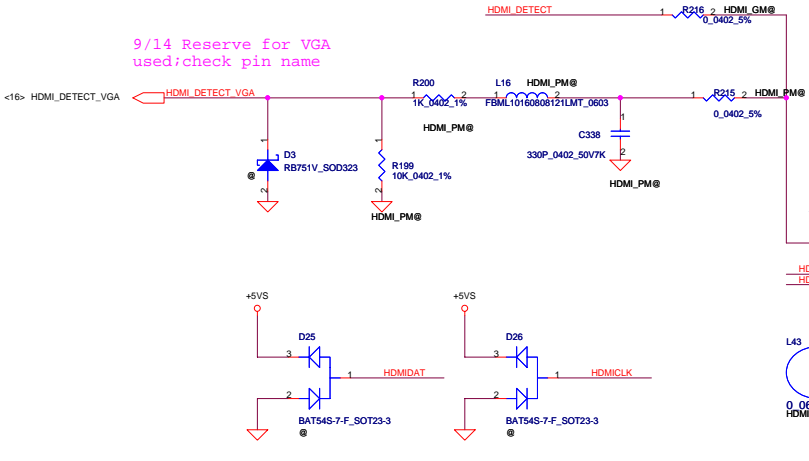
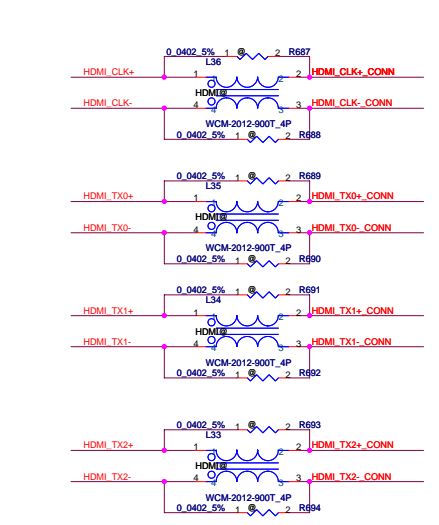
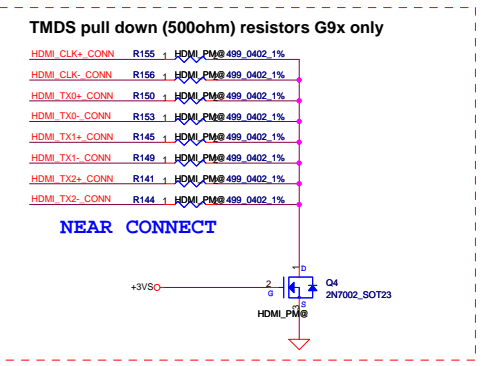
**REQ PORT LIST**

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
				<b>Clock generator</b>
				Size Document Number
				JIIWA3/A4_LA4212P
				Rev 1.0
				Date: Monday, May 12, 2008
				Sheet 22 of 53



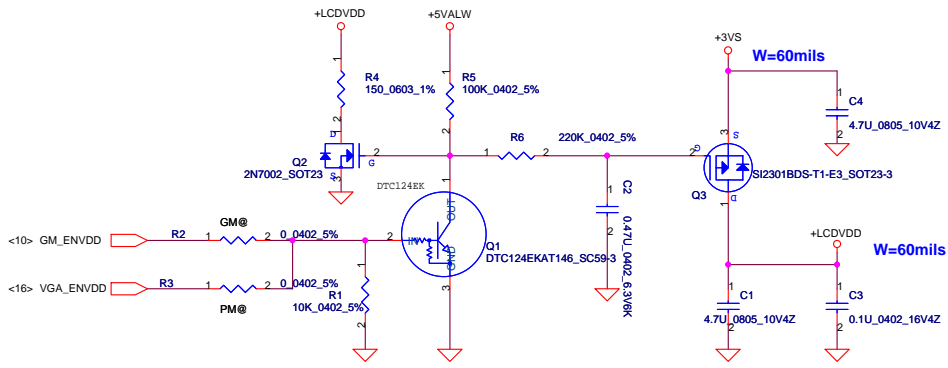
9/13 Add inverting level shift circuit base on Design Guide P.277



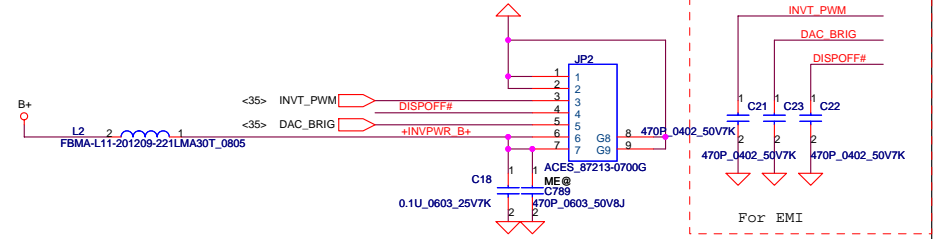
hexainf@hotmail.com  
gratuito - free of charge

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Level shifter-CH7318
Size	Document Number	Date	Thursday, May 22, 2008	Sheet 23 of 53
	J1WA3/A4_LA-4212P			Rev 1.0

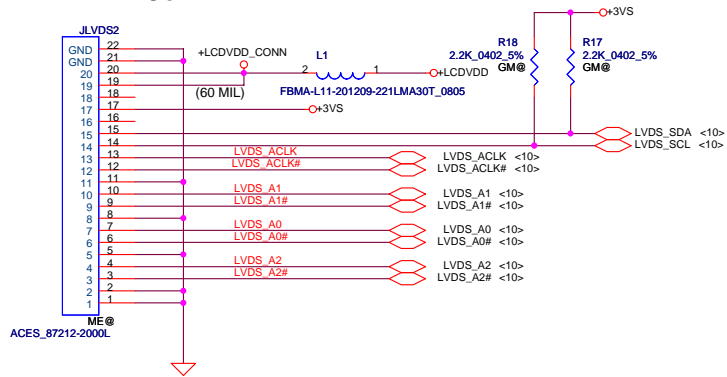
### LCD POWER CIRCUIT



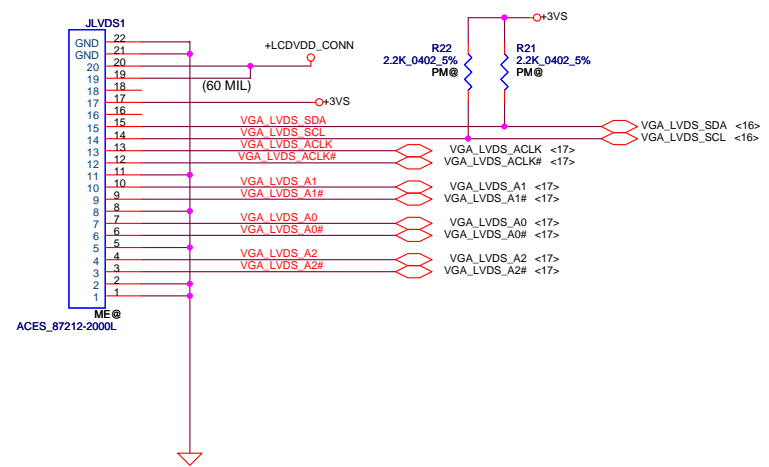
### INVERTER Conn.



### LCD/PANEL BD. Conn.



### LCD/PANEL BD. Conn.

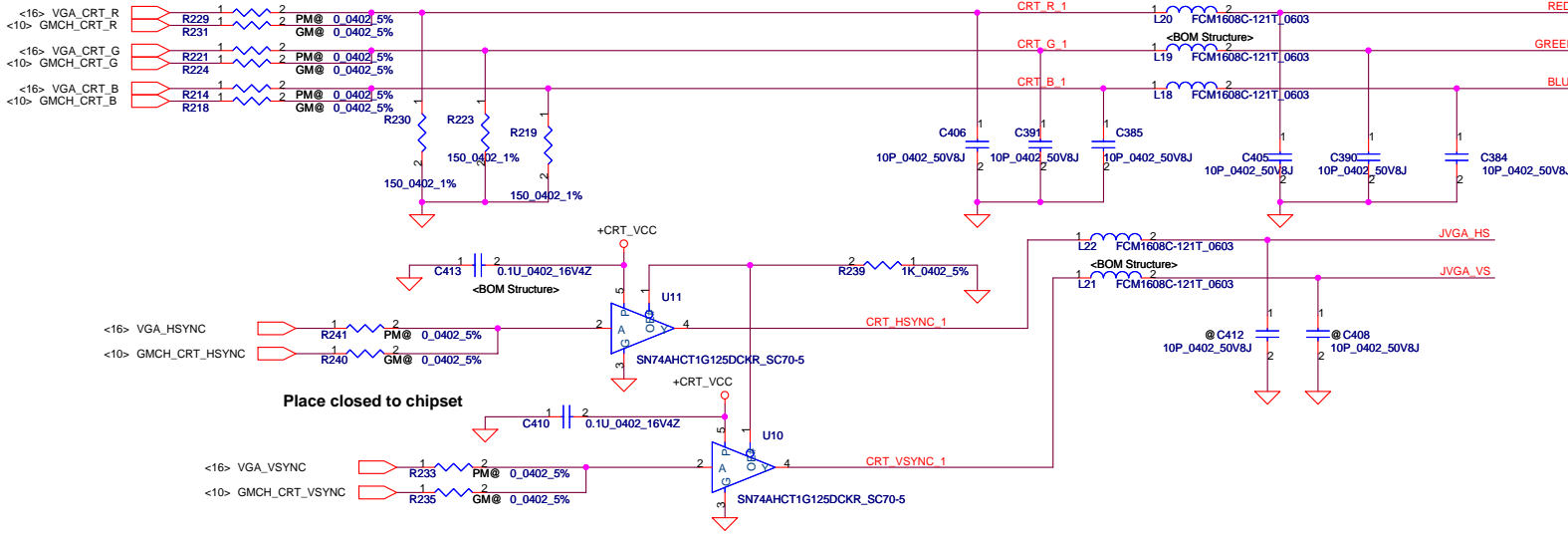


Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LVDS & DVI Connector	
Size B	Document Number	JIWA3/A4_LA4212P		Rev	1.0
Date:	Monday, May 12, 2008	Sheet	24	of	53

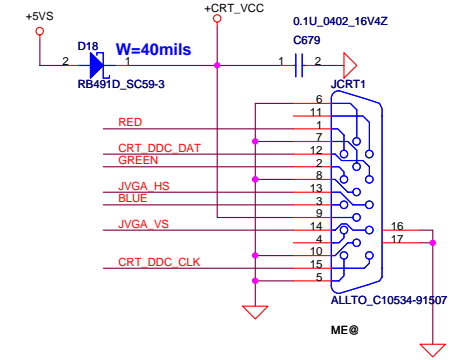
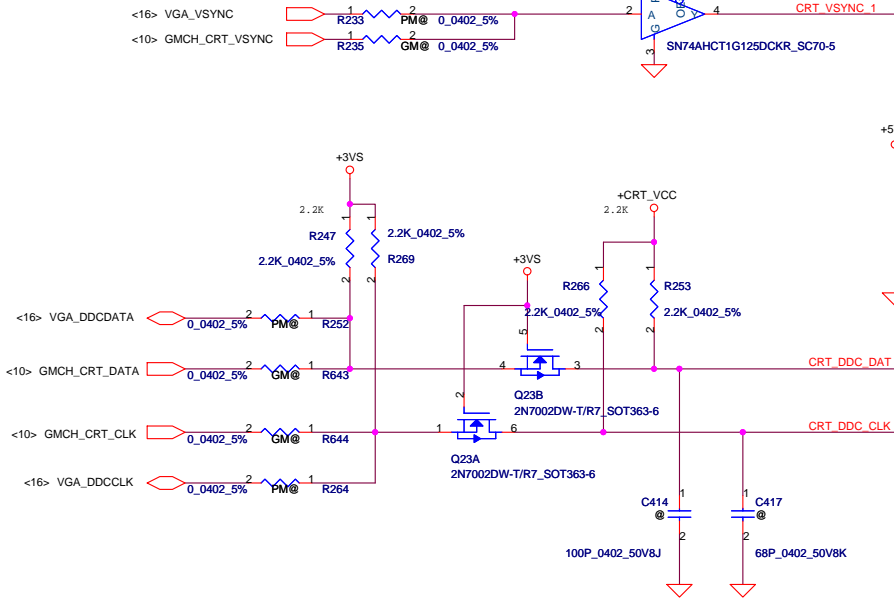


# CRT Connector

Place closed to chipset



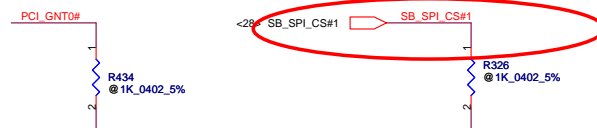
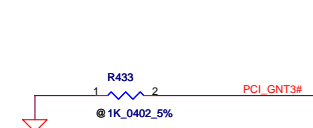
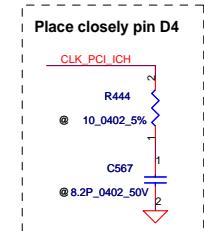
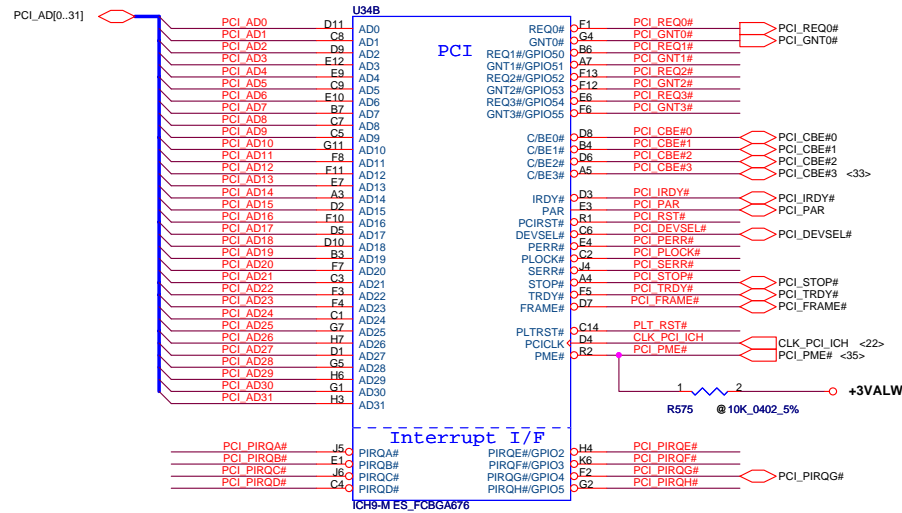
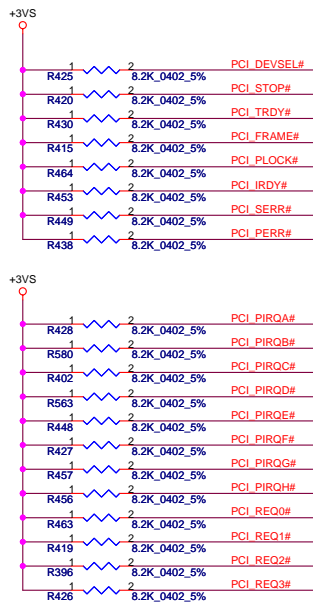
Place closed to chipset



## PIN ASSIGNMENT

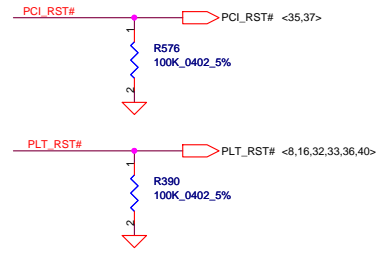
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

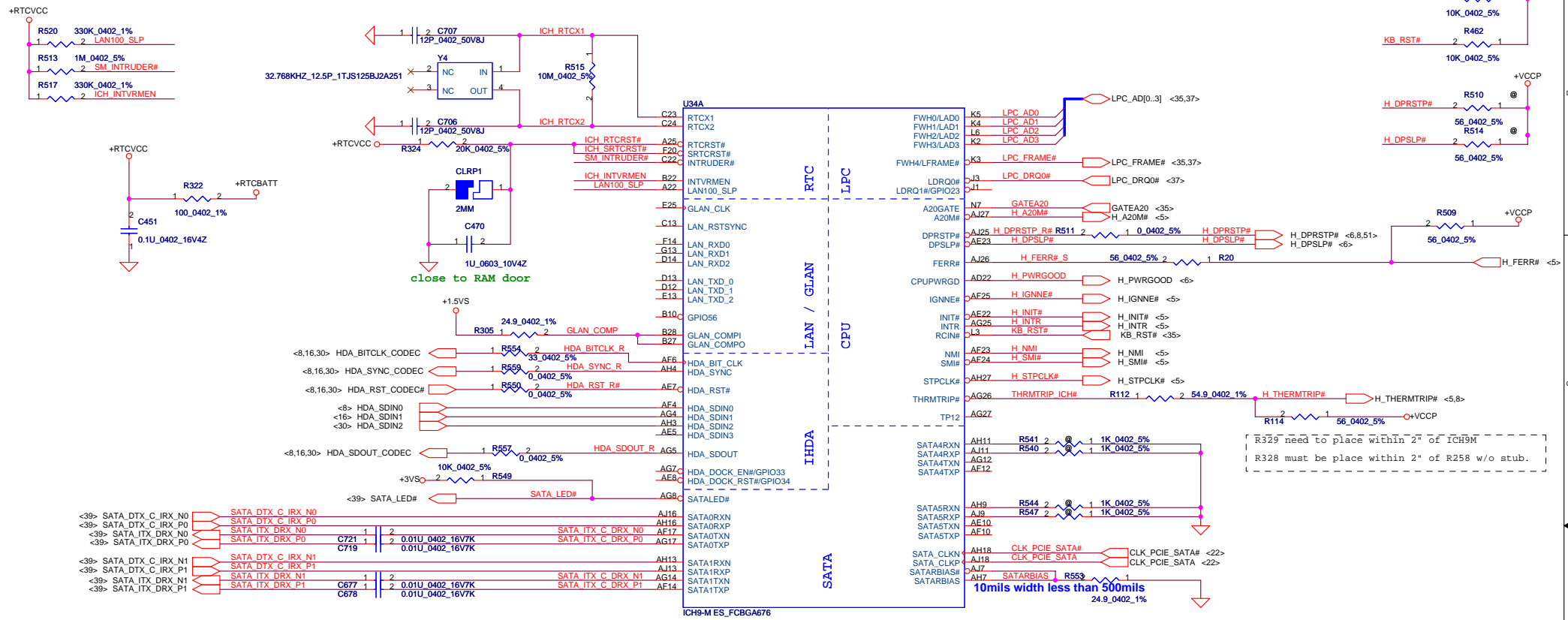
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			<b>Compal Electronics, Inc.</b> <b>CRT &amp; TV-OUT Connector</b>	
Size	Document Number	Rev		1.0
Custom	J1WA3/A4_LA4212P	Date:		Monday, May 12, 2008
		Sheet		25 of 53



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

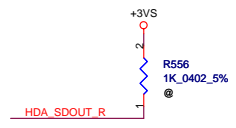
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*





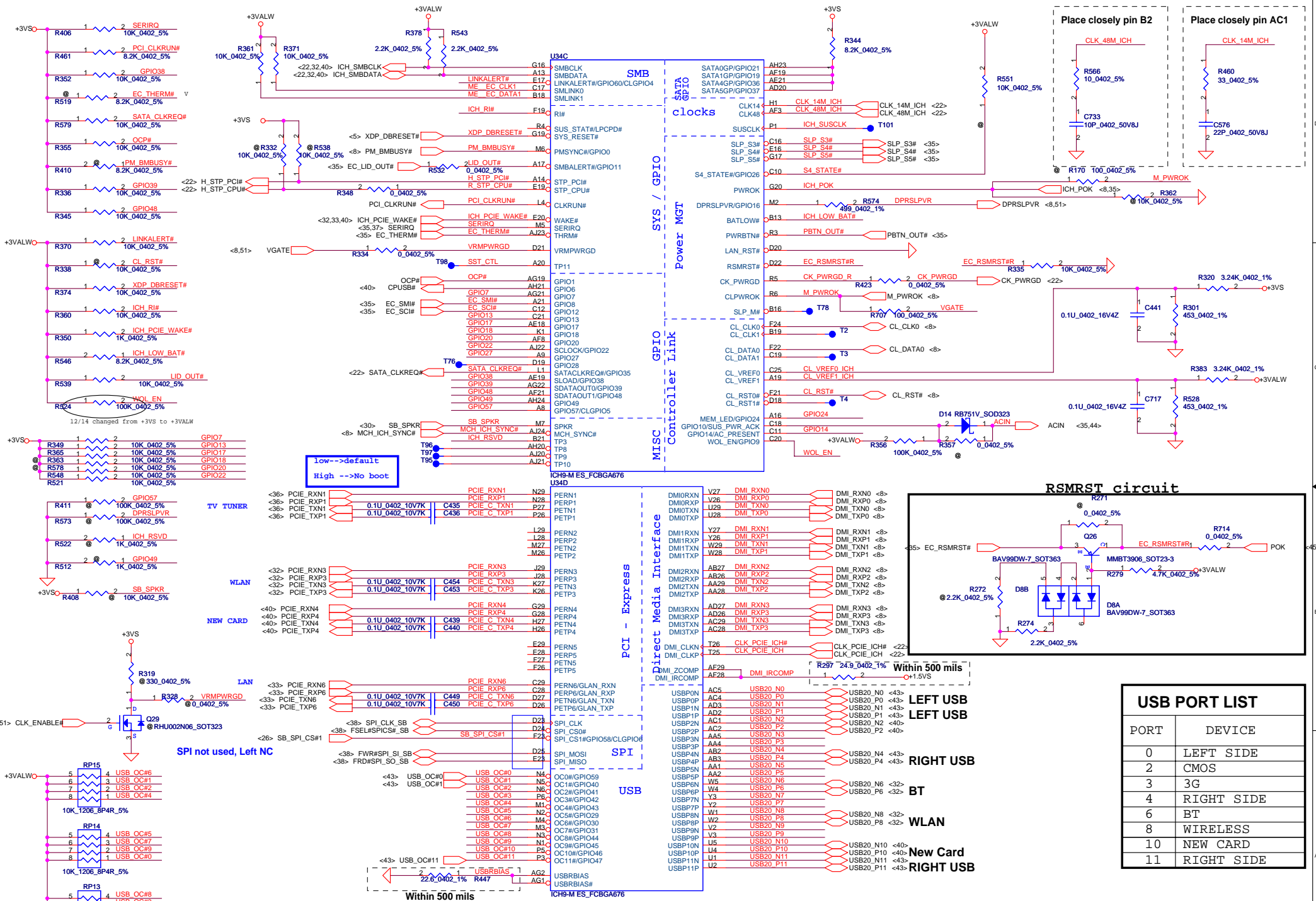
R329 need to place within 2" of ICH9M  
 R328 must be place within 2" of R258 w/o stub.

Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>ICH9M(2/4)-LAN, IDELPC, RTC</b> Size: JIWA3/A4_LA4212P Document Number: JIWA3/A4_LA4212P Date: Wednesday, May 14, 2008
				Rev: 1.0
				Sheet 27 of 53



USB PORT LIST	
PORT	DEVICE
0	LEFT SIDE
2	CMOS
3	3G
4	RIGHT SIDE
6	BT
8	WIRELESS
10	NEW CARD
11	RIGHT SIDE

Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15

Compal Electronics, Inc.		
Title		
ICH9M(3/4)-USB,GPIO,PCIE		
Size	Document Number	Rev
Customer	J1WA3/A4_LA421P	1.0
Date:	Wednesday, May 14, 2008	Sheet 28 of 53

hexainf@hotmail.com  
gratuito - free of charge.

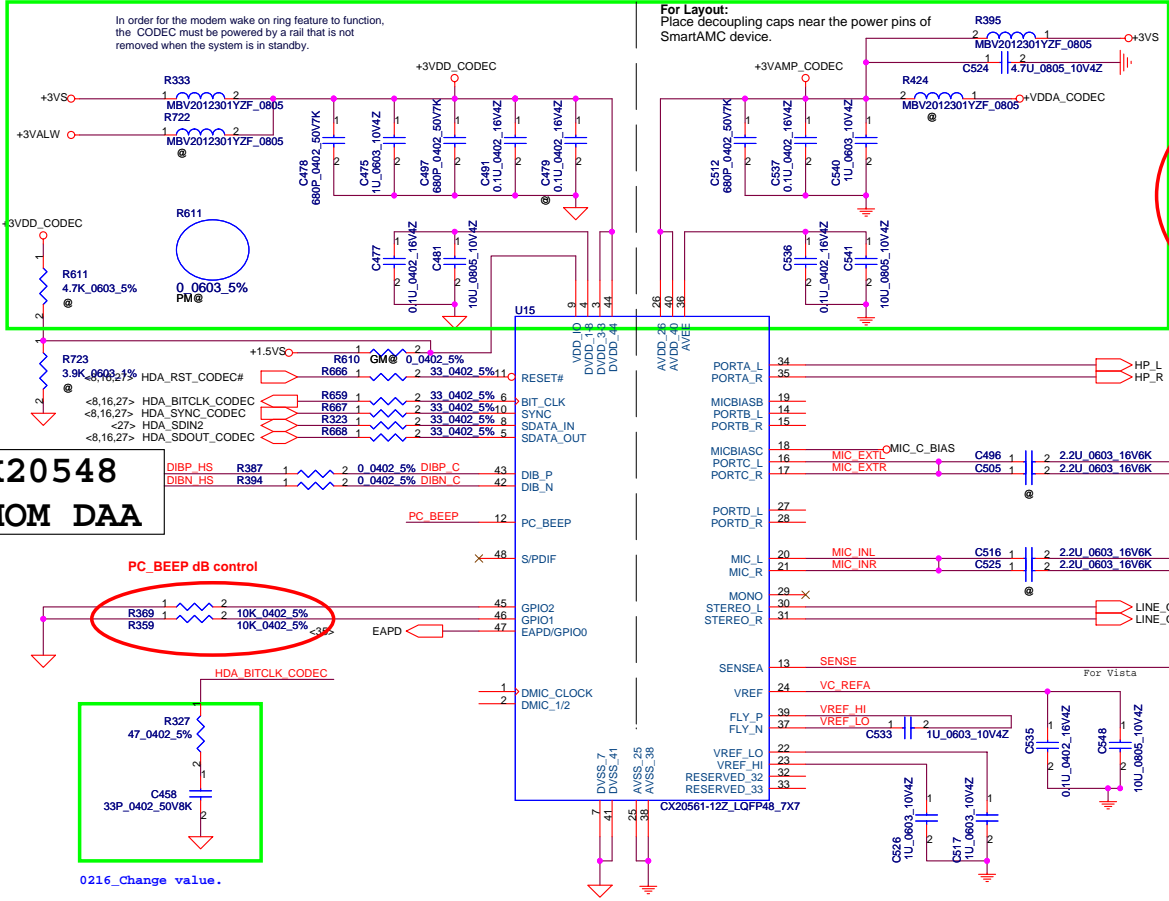
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



# AUDIO CODEC

0308\_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680pF

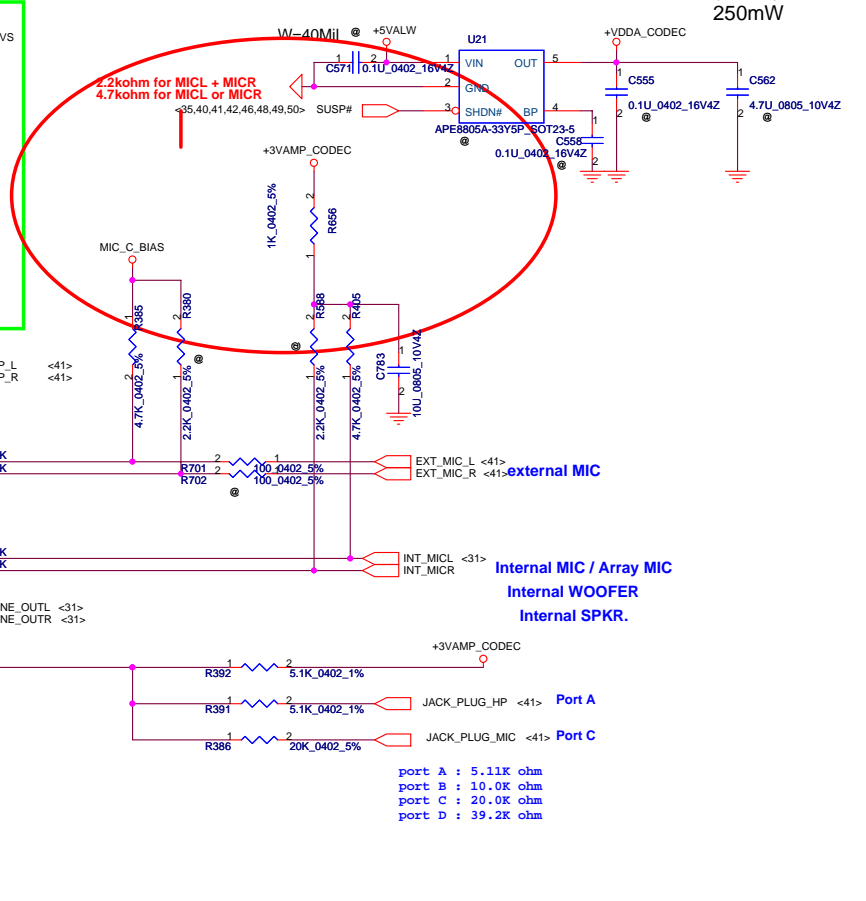
For Layout:  
Place decoupling caps near the power pins of SmartAMC device.



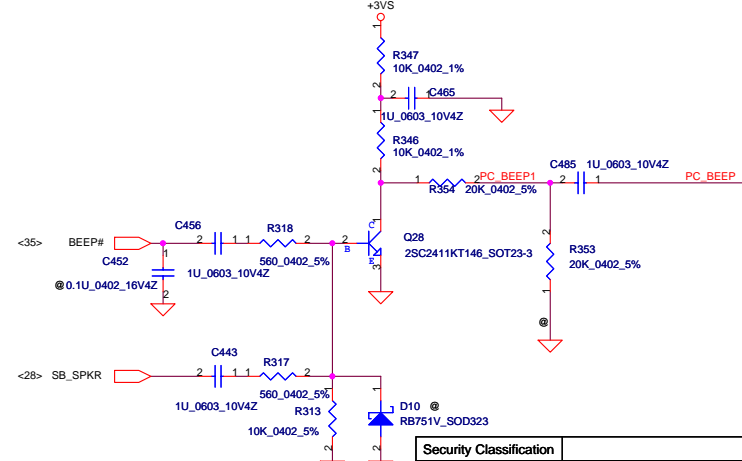
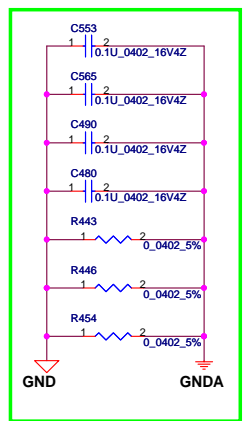
**CX20548  
AMOM DAA**

# CODEC POWER

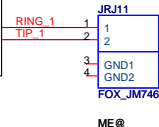
(3.33V)  
250mW



# DIGITAL ANALOG



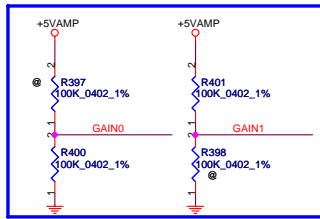
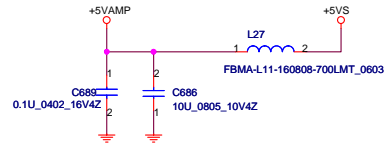
**CX20548  
AMOM DAA**



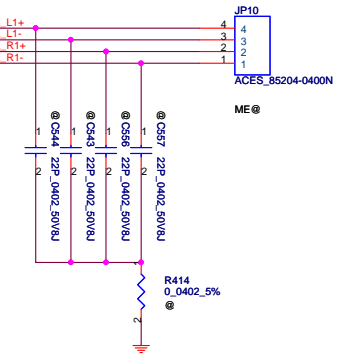
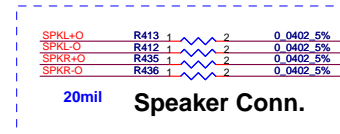
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>CX20561-AMOM Codec</b> Size: Document Number Custor: JIWA3/A4_LA4212P Date: Monday, May 12, 2008	
				Rev	1.0
				Sheet	30 of 53

# Speaker Amplifier

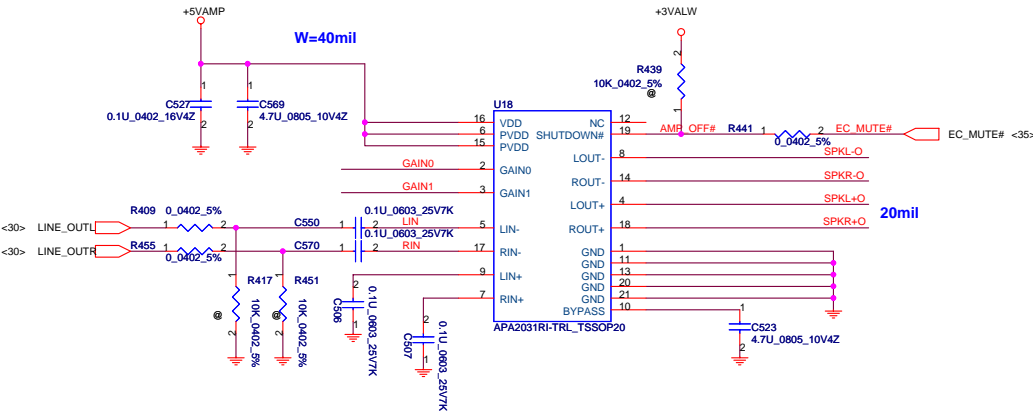
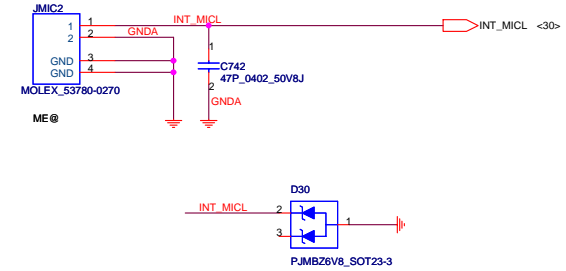
1nd = APA2031 (SA00001RZ00)  
 2nd = G1431F2U (SA000012Y00)



	GAIN0	GAIN1	
0	0	6dB	
0	1	10dB	
1	0	15.6dB	
1	1	21.6dB	



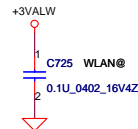
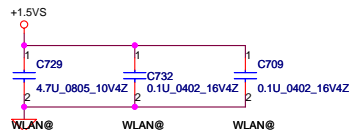
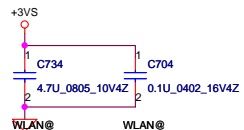
# INT MIC



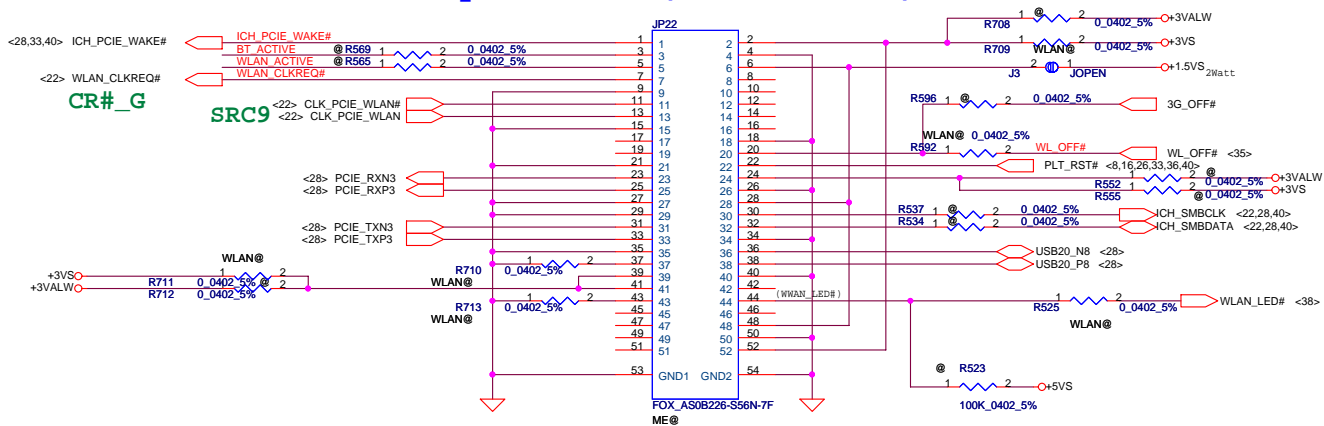
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Size	Document Number	Date		Rev
Custom	J1WA3/A4_LA4212P	Monday, May 12, 2008		1.0
Date		Monday, May 12, 2008	Sheet	31 of 53

hexainf@hotmail.com  
 gratuito - free of charge.

# Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN

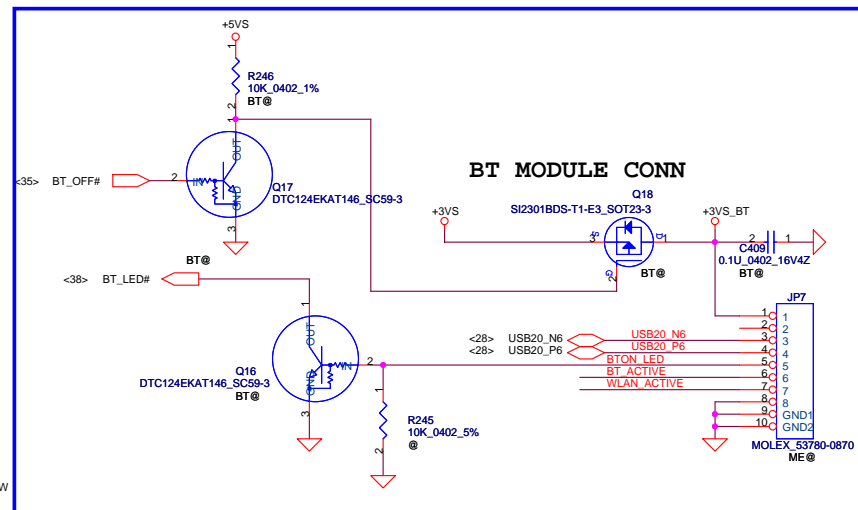


## Mini-Express Card (Slot 1-WLAN)



2005/09/27 modified.  
Base on OPTION GTM351E Datasheet Rev0.1

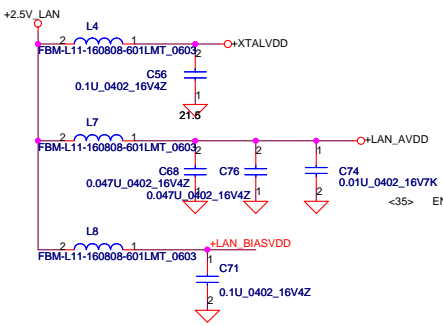
Vcc 3.3V +/- 8%  
Peak Icc 2750mA  
with max supply droop 50mA  
Average Icc 1000mA



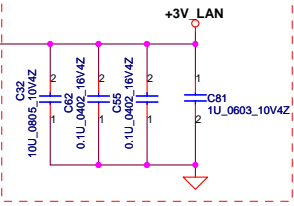
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Mini-Card/3G/FeliCa/BT	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number	J1WA3/A4_LA4212P		Rev	1.0
Date:	Tuesday, May 20, 2008	Sheet	32	of	53



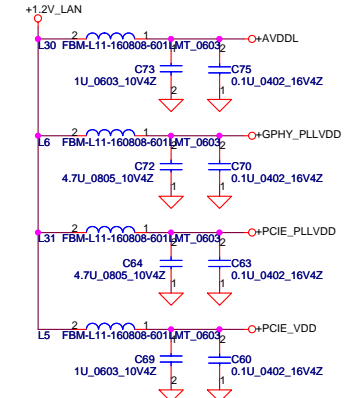
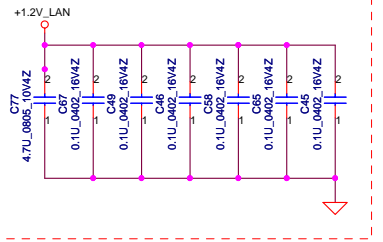
Layout Notice : Filter place as close chip as possible.



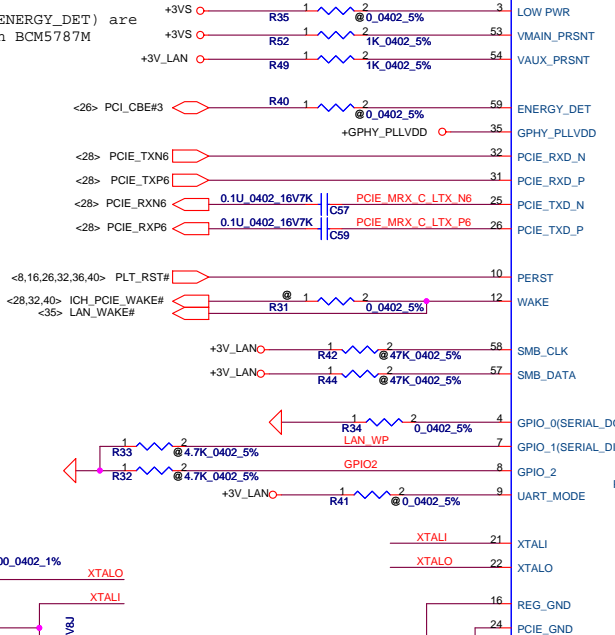
Layout Notice : Place as close chip as possible.



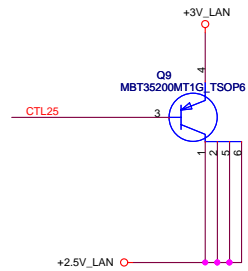
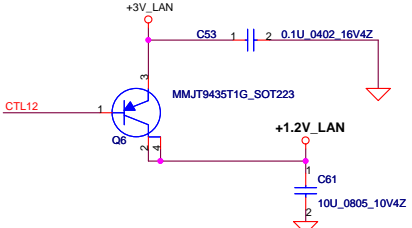
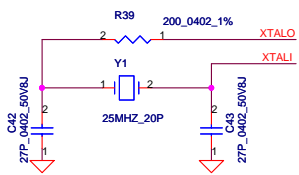
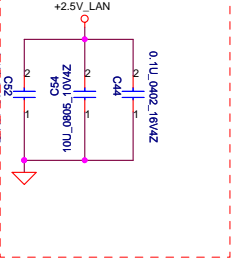
Layout Notice : 1.2V filter. Place as close chip as possible.



(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M

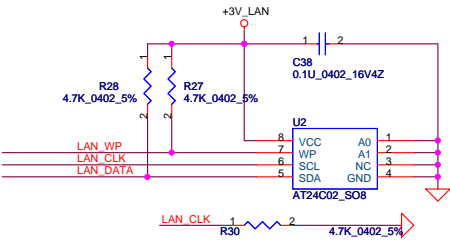


Layout Notice : Place as close chip as possible.



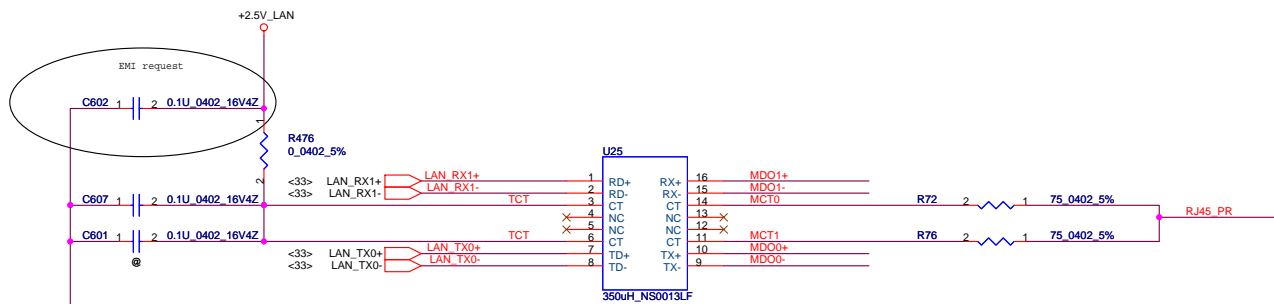
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

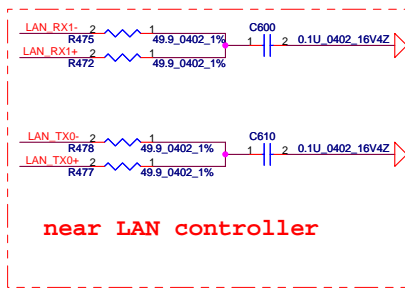


Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		

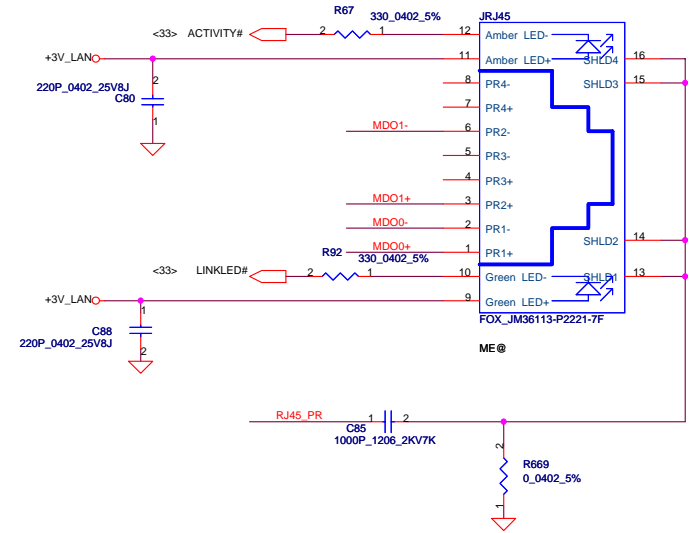
Title			Compal Electronics, Inc.		
			BCM5787MKML		
Size	Document Number				Rev
Custom	J1WA3/A4_LA4212P				1.0
Date:	Monday, May 12, 2008	Sheet	33	of	53



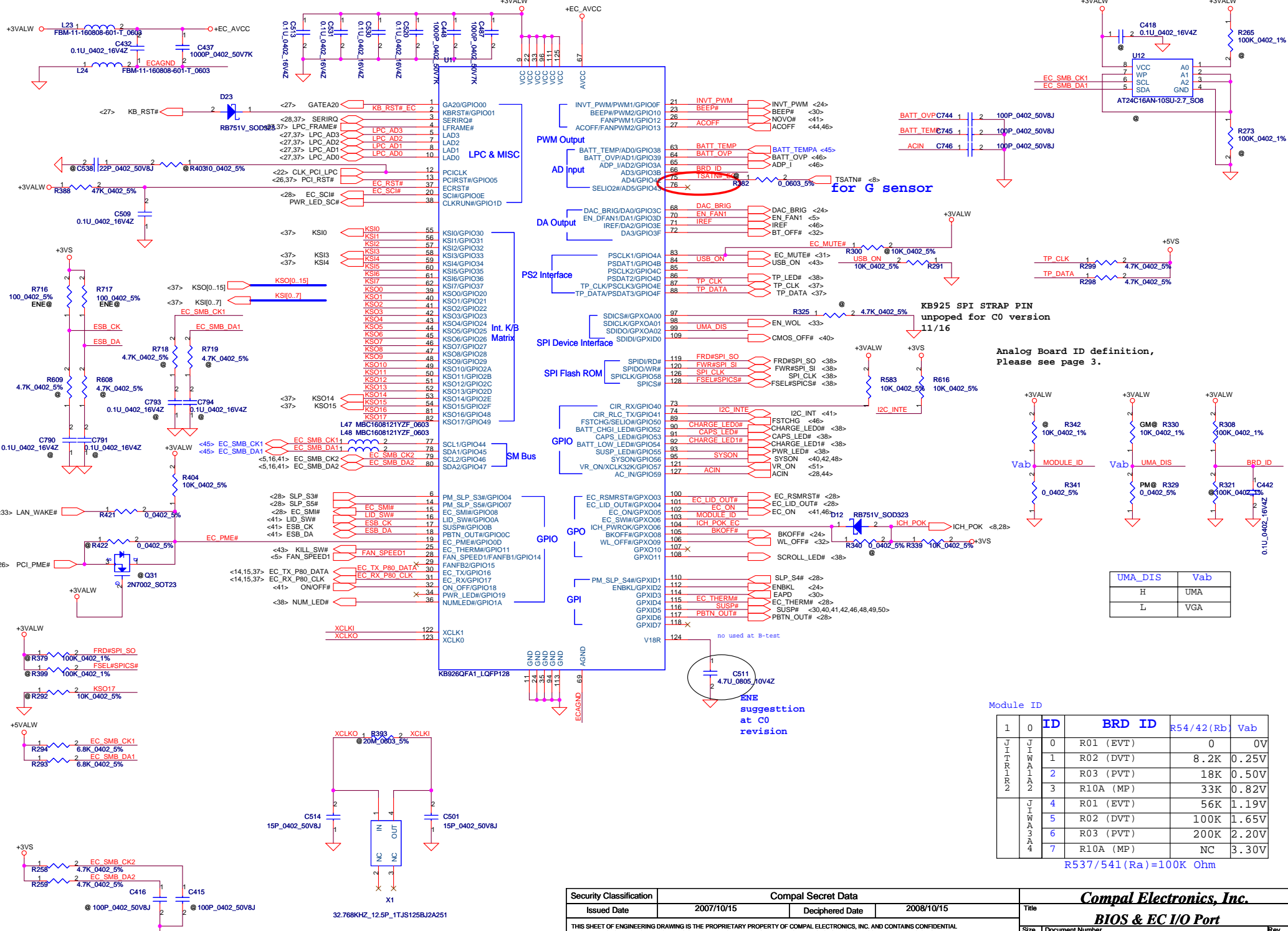
Change C468, C470, C473, C474, C475, C476 from 0.01uF to 0.1uF



### RJ45 CONN



Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LAN CONTROLLER	
Size	Document Number	Date:		Rev	1.0
Custort	JJWA3/A4_LA4212P	Monday, May 12, 2008		Sheet	34 of 53



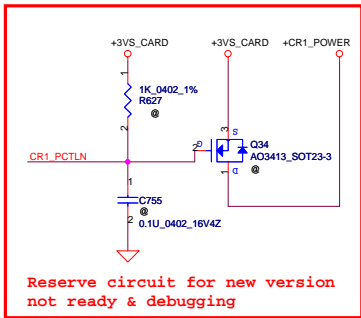
Analog Board ID definition, Please see page 3.

Vab	MODULE_ID	UMA_DIS	BRD_ID
	R341	R339	R321
	R342	R340	R320
	R343	R338	R319
	R344	R337	R318

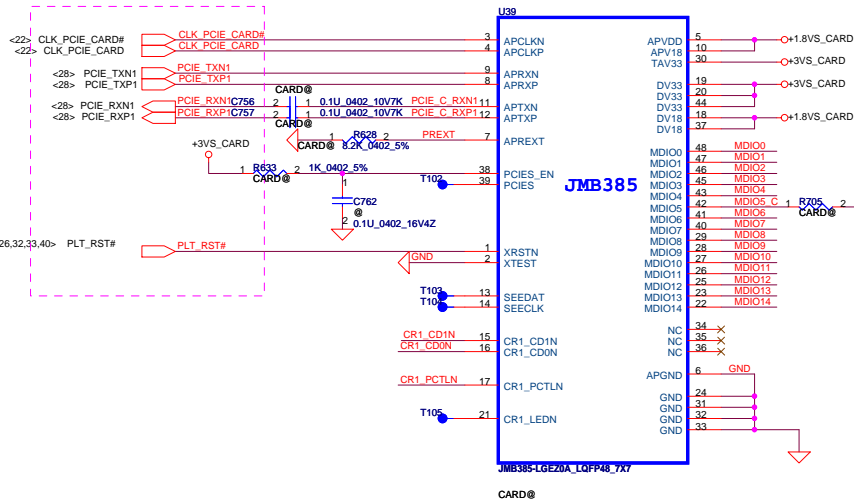
ID	BRD ID	R54/42 (Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03 (PVT)	18K	0.50V
3	R10A (MP)	33K	0.82V
4	R01 (EVT)	56K	1.19V
5	R02 (DVT)	100K	1.65V
6	R03 (PVT)	200K	2.20V
7	R10A (MP)	NC	3.30V

R537/541 (Ra)=100K Ohm

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b> <b>BIOS &amp; EC I/O Port</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Size	Document Number	Date		Rev
Custor	J1WA3/A4_LA4212P	Tuesday, May 20, 2008		1.0
Sheet			35	of 53

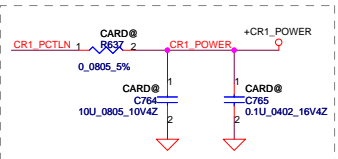
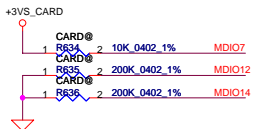
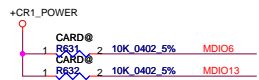


Need check CLK GEN & SB select pin & page



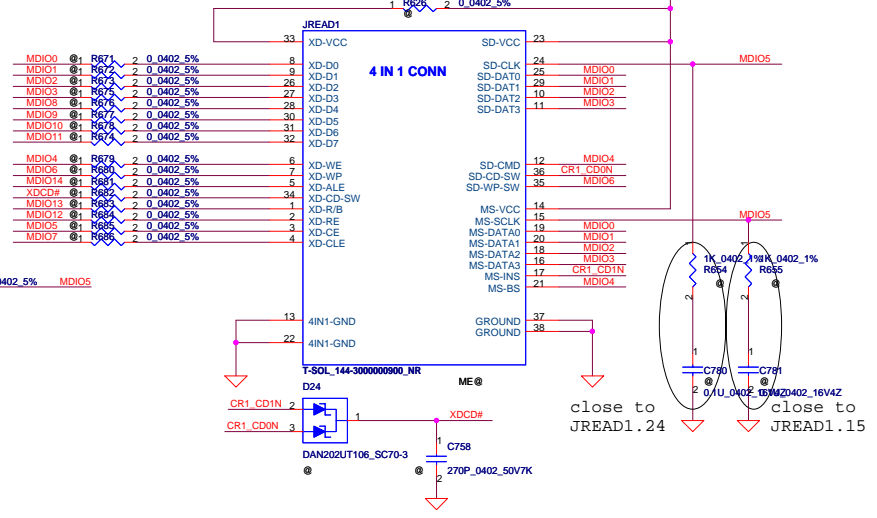
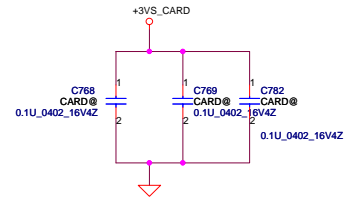
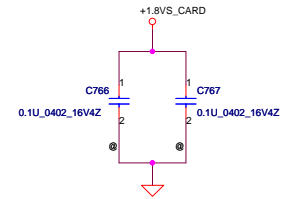
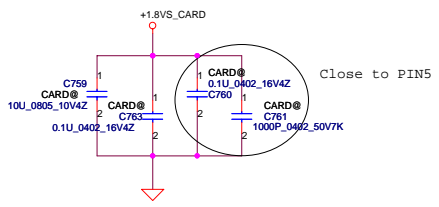
JMB385 Operation Modes

	Normal
XTEST	0
CR1_CDON	X
CR1_CDIN	X



Use 0805 type and over 20 mils trace width on both side

Card Reader power circuit



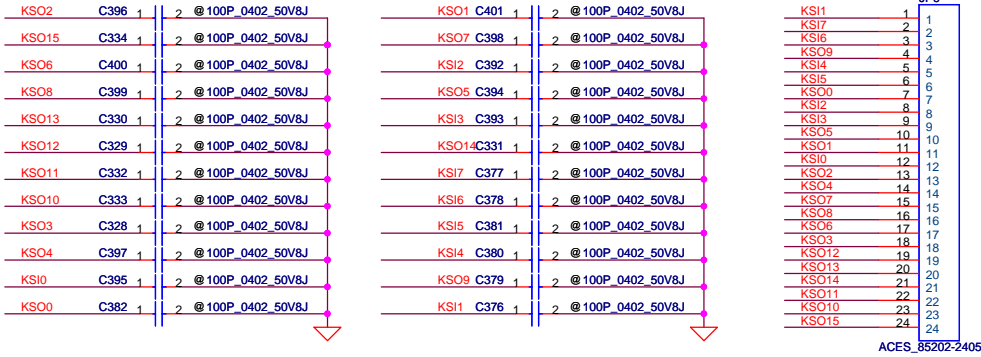
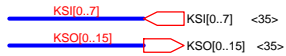
SD,MMC,MS,XD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

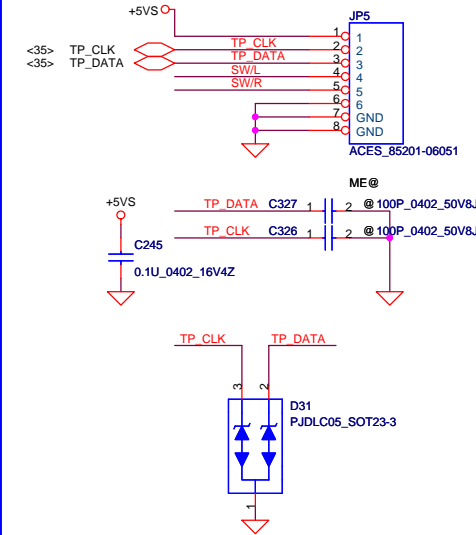
Cardreader contactor not support MMC & MS Bit 4~7

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date	2006/10/06	4 in 1 Card
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 1.0
Date: Monday, May 12, 2008			Sheet 36 of 53	

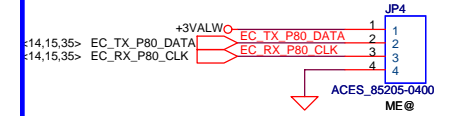
### INT\_KBD Conn.



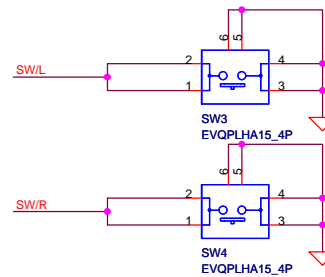
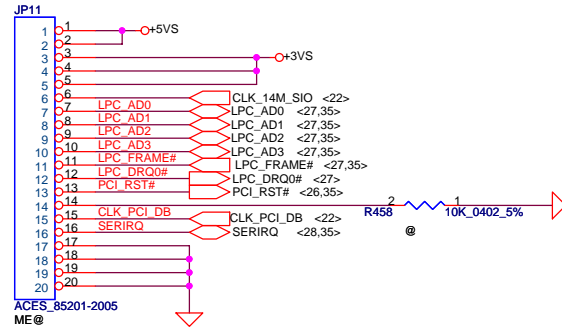
### To TP/B Conn.



### EC DEBUG PORT

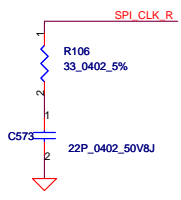
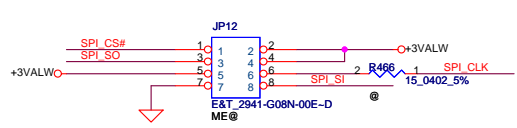
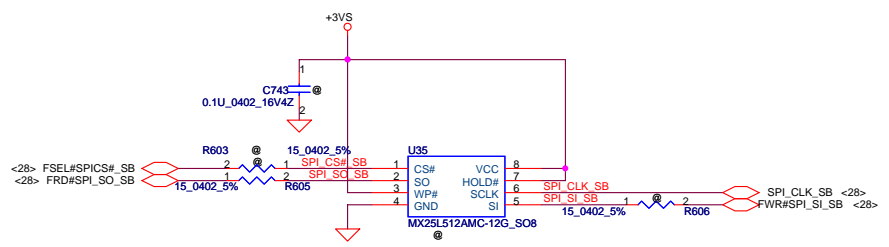
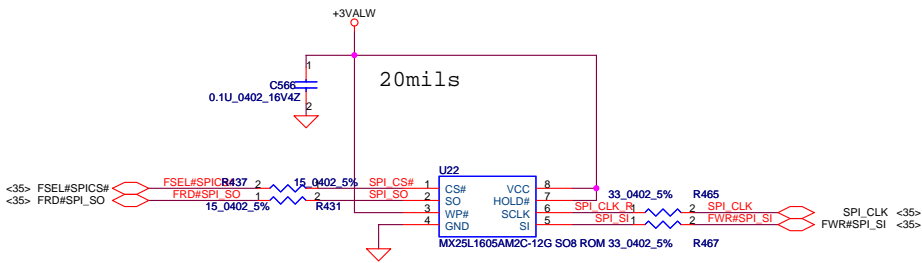


### FOR LPC SIO DEBUG PORT

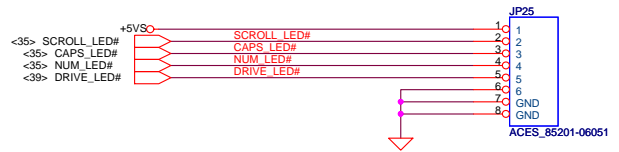
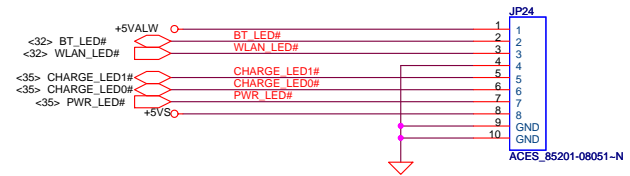
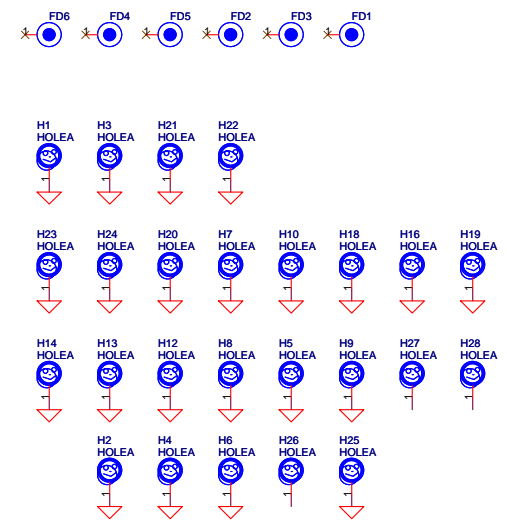


Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b> <b>KB /SW /LPC Debug Conn.</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Rev 1.0
Date:	Monday, May 12, 2008	Sheet	37	of	53

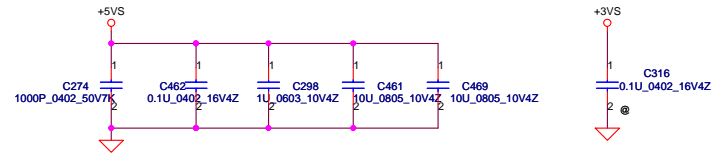
**FOR EC 8M SPI ROM**



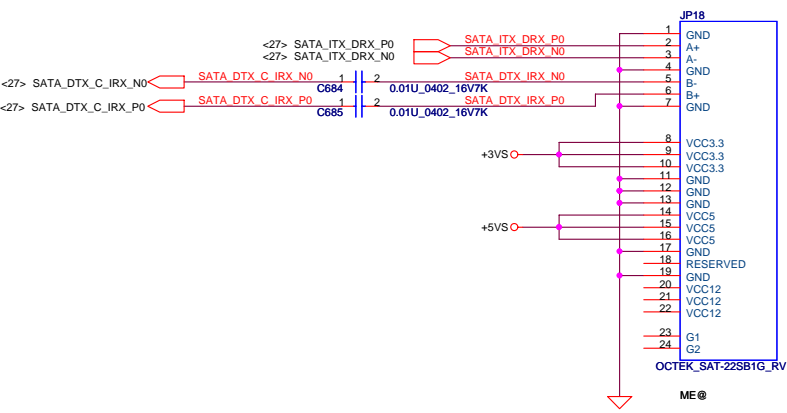
**LED**



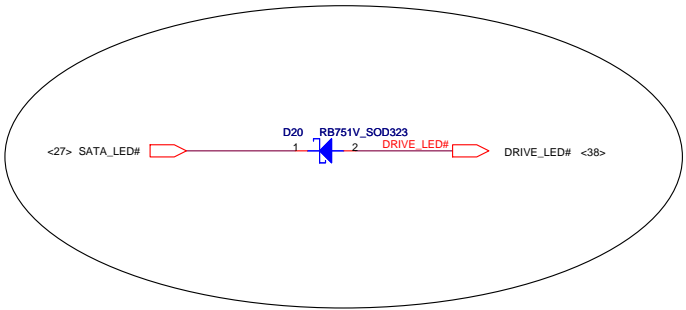
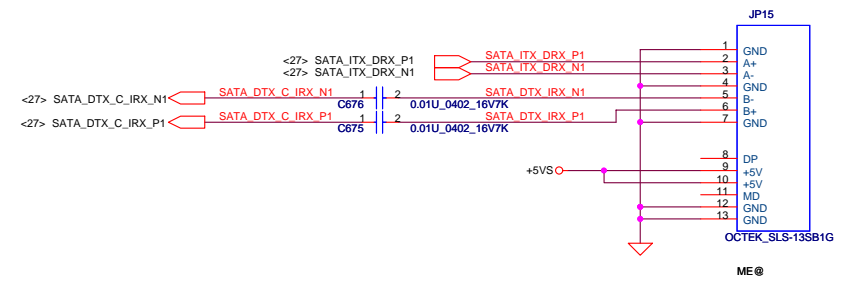
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>LED/EC SPI ROM</b>	
Issued Date	2007/10/15	Deciphered Date	2008/10/15		
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size B	Document Number
				J1WA3/A4_LA4212P	
				Date:	Wednesday, May 14, 2008
				Sheet	38 of 53
				Rev	1.0



**SATA HDD Conn.**



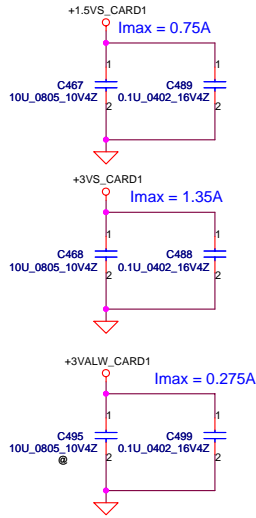
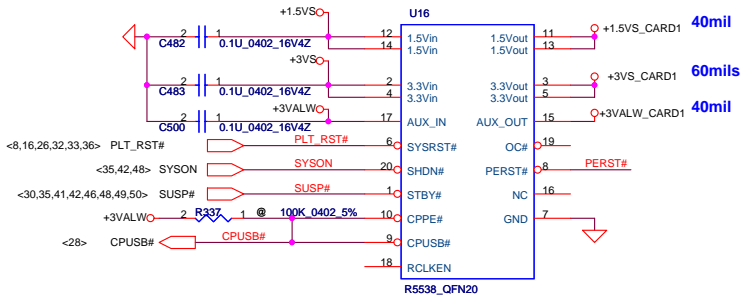
**SATA ODD Conn.**



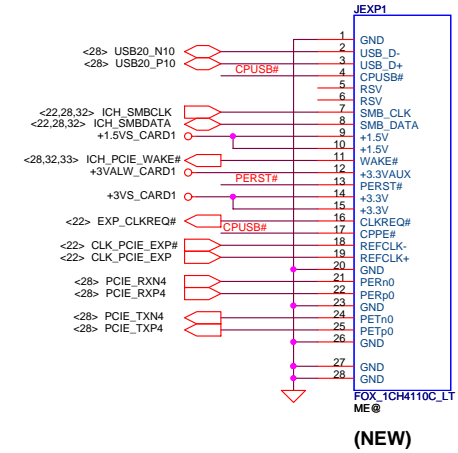
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>HDD &amp; ODD Connector</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size B	Document Number JIWA3/A4_LA4212P	Rev 1.0
			Date:	Monday, May 12, 2008	Sheet 39 of 53

hexainf@hotmail.com  
gratuito - free of charge.

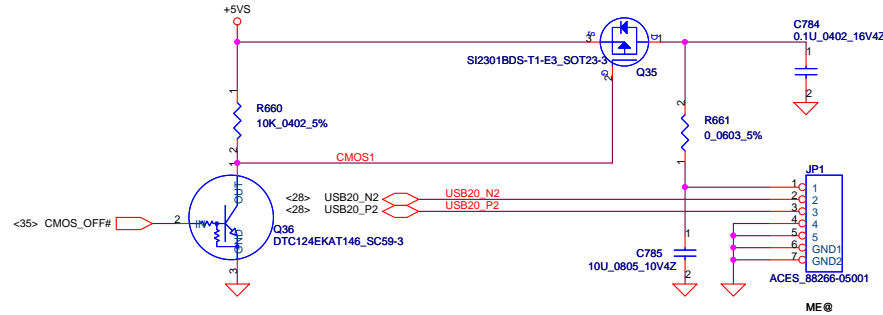
### Express Card Power Switch



### New Card Socket (Left/TOP)



### CMOS Camera Conn

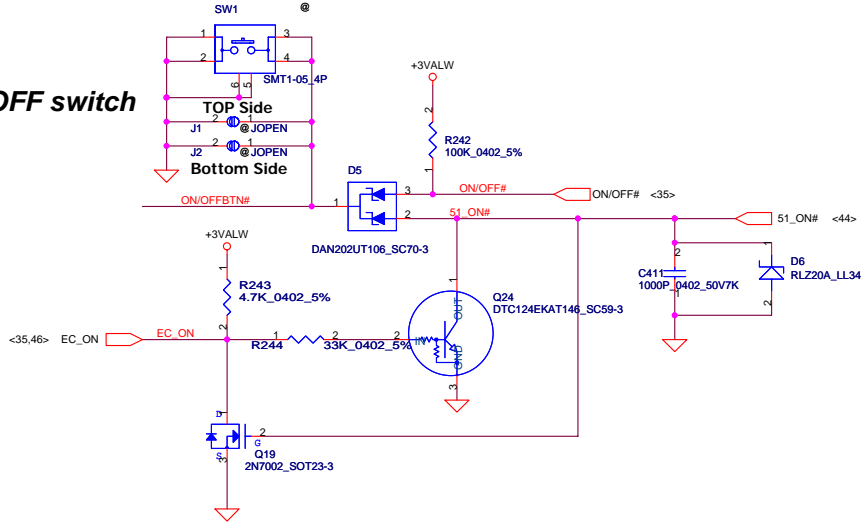


Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				NEW CARD & CMOS Connector	
Size B	Document Number	JIWA3/A4_LA4212P		Rev	1.0
Date:	Monday, May 12, 2008	Sheet	40	of	53

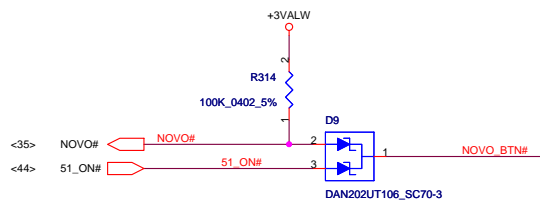
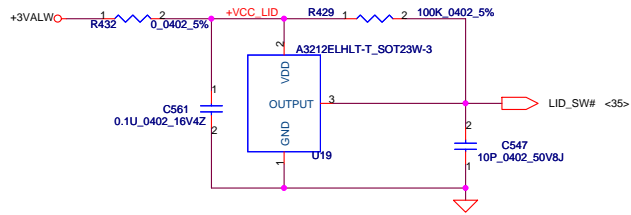


### Power Button

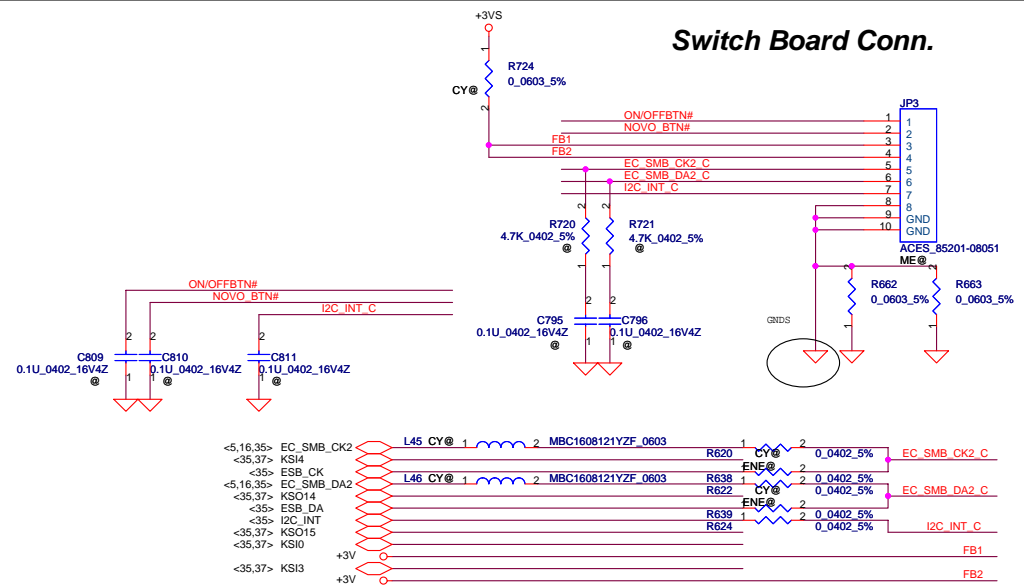
### ON/OFF switch



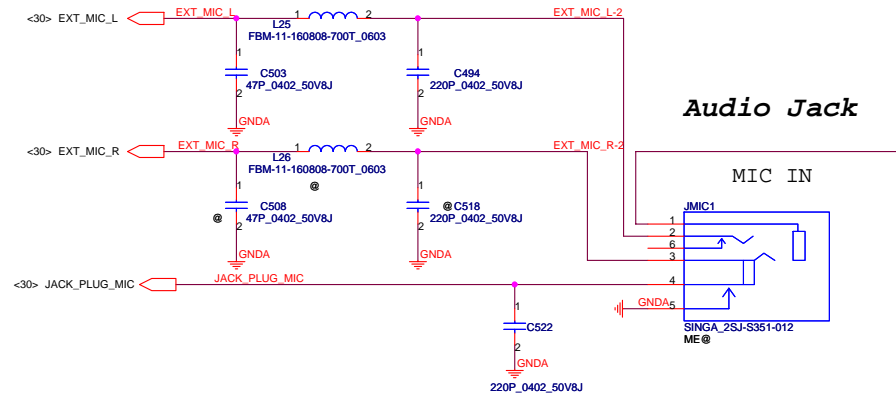
### Lid Switch



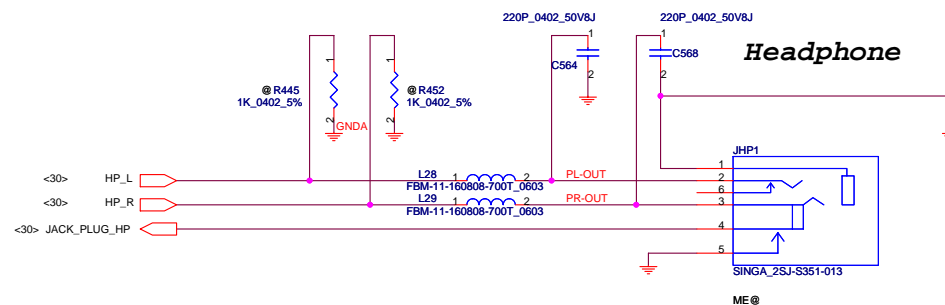
### Switch Board Conn.



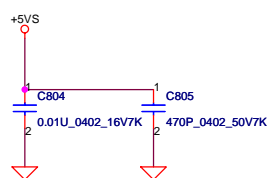
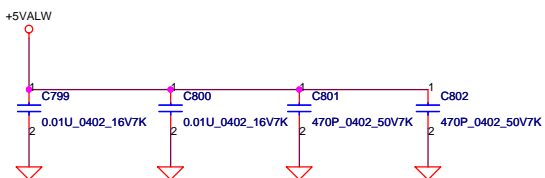
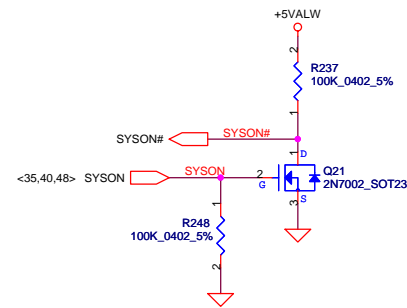
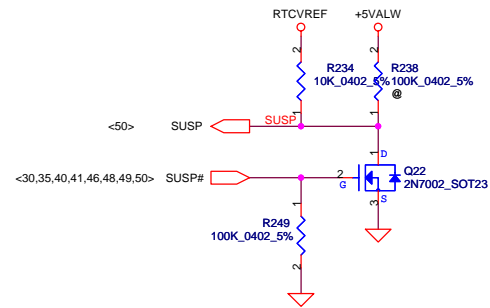
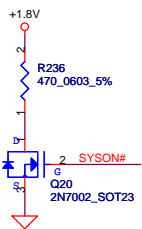
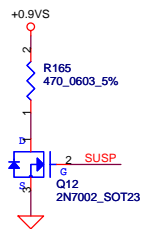
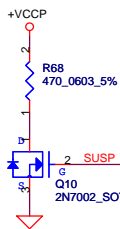
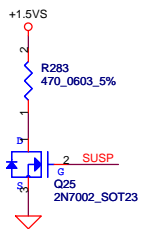
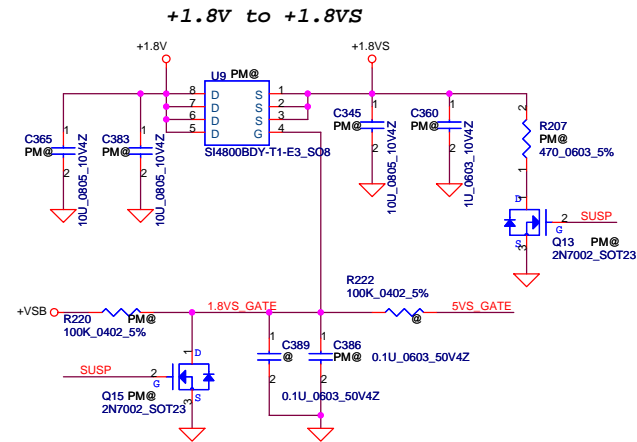
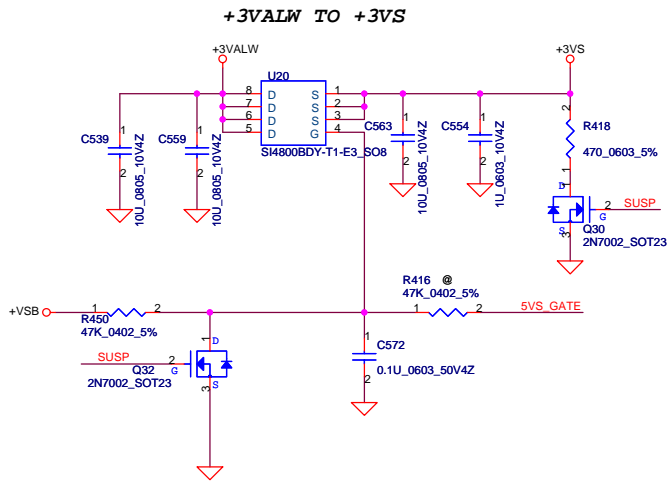
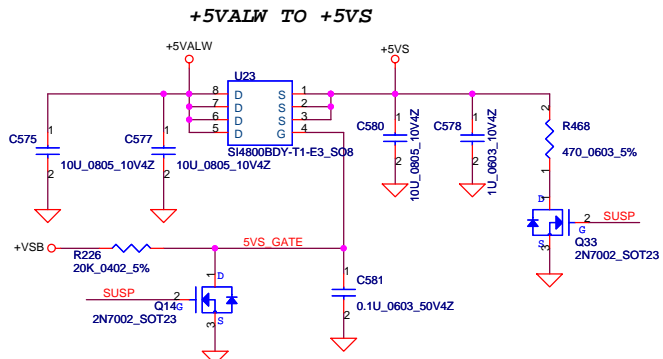
### Audio Jack



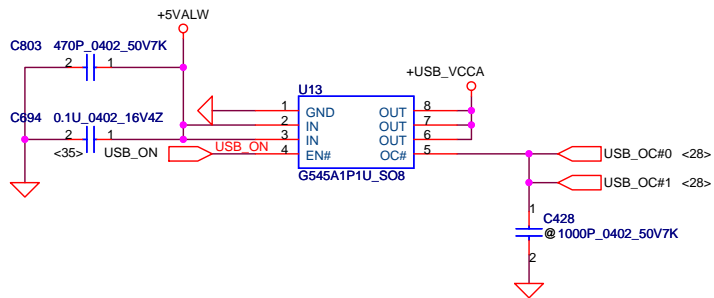
### Headphone



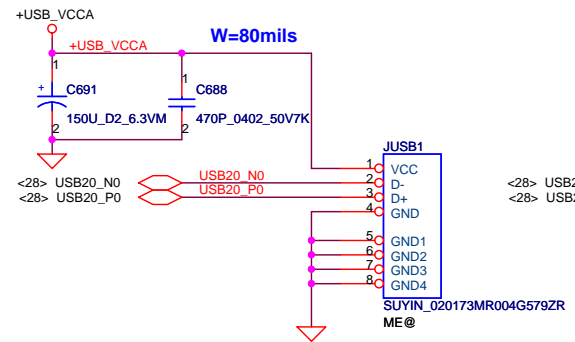
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
				<b>Audio Jack &amp; SW connector</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B
				Document Number
				J1WA3/A4_LA4212P
				Rev 1.0
				Date: Monday, May 12, 2008
				Sheet 41 of 53



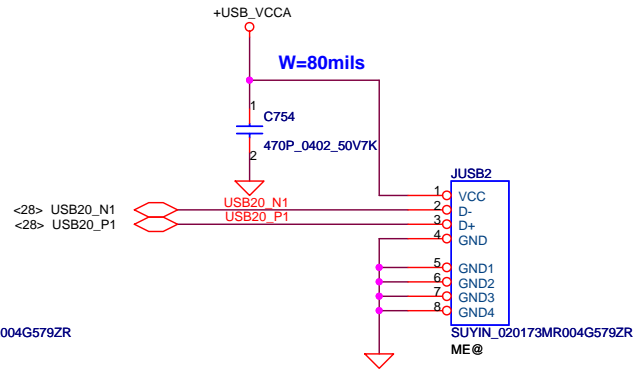
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2007/8/18	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DC Interface	
Size	Document Number			Rev	1.0
Custom	J1WA3/A4_LA4212P			Date	Monday, May 12, 2008
				Sheet	42 of 53



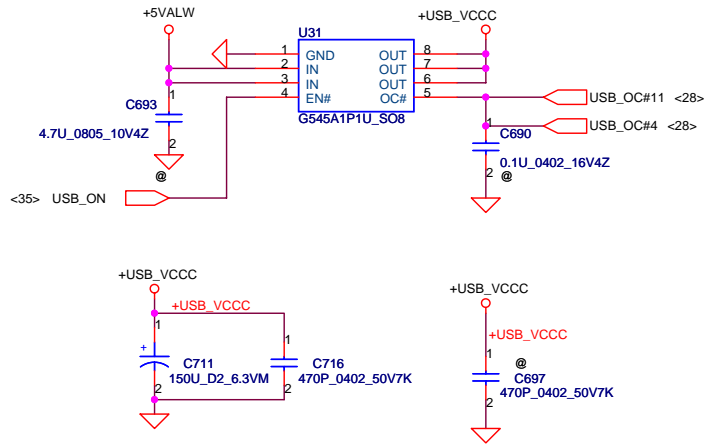
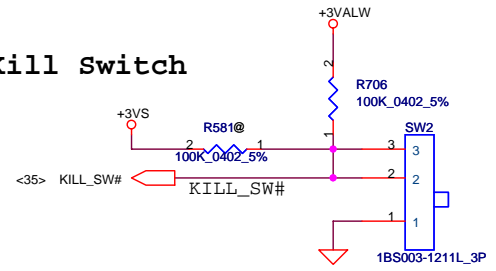
### LIFT USB CONN. 1



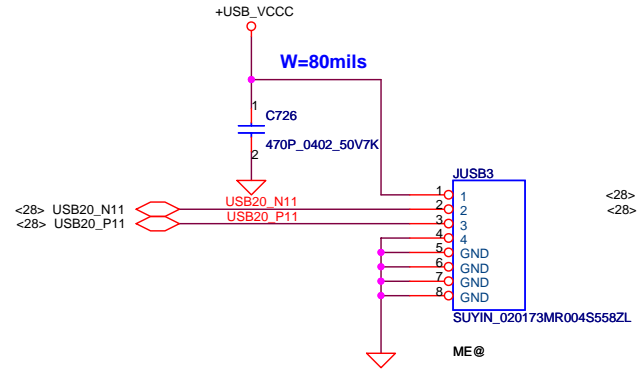
### LIFT USB CONN. 2



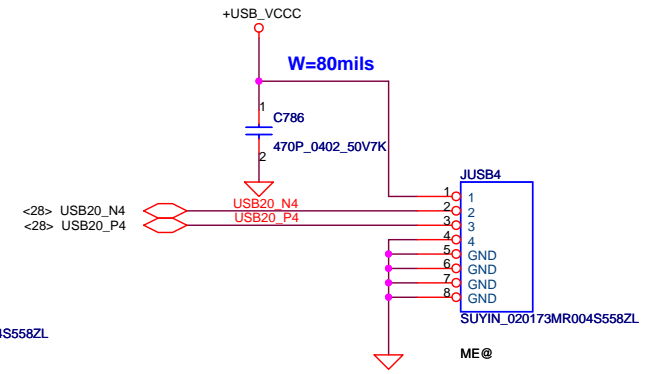
### Kill Switch



### RIGHT USB CONN. 3

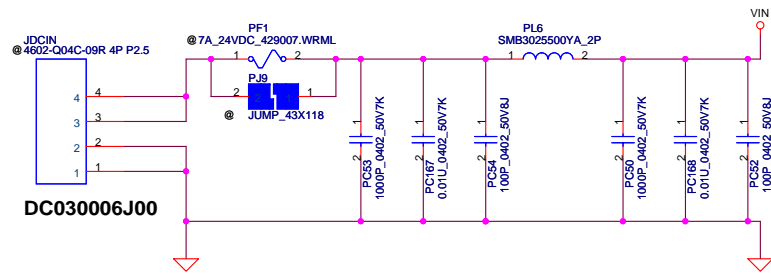


### RIGHT USB CONN. 4



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2007/8/18	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Power OK, Reset and RTC Circuit, TP	
Size	Document Number	Rev		Date	
Custom	JWA3/A4_LA4212P	1.0		Wednesday, May 14, 2008	
				Sheet 43 of 53	

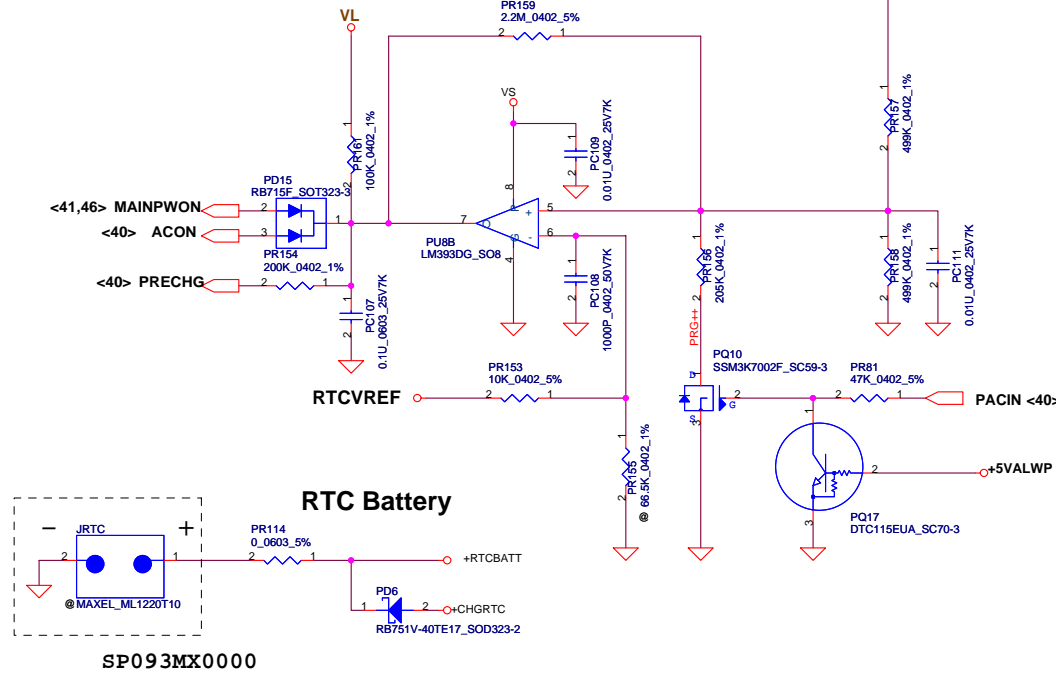
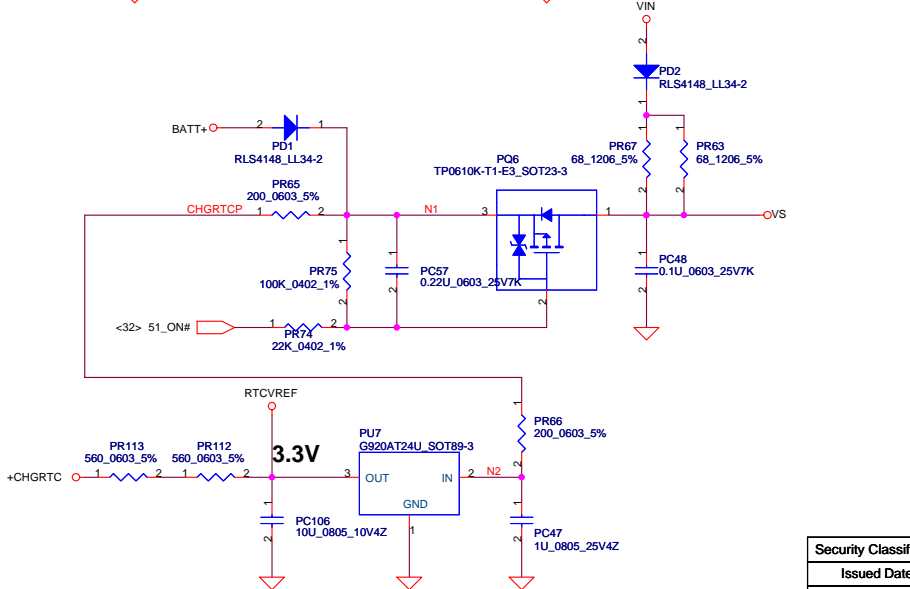
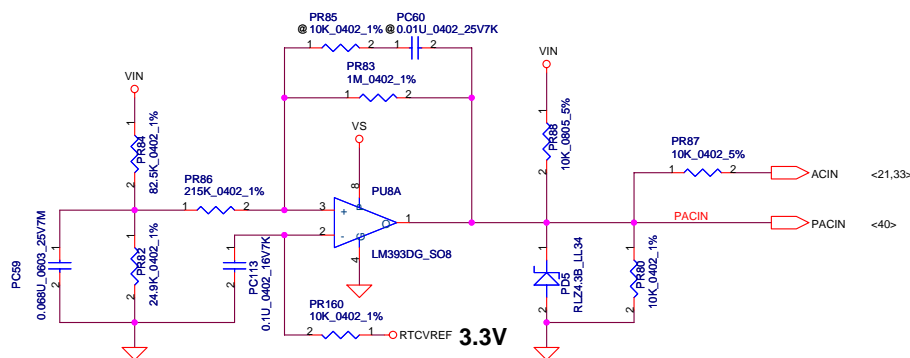
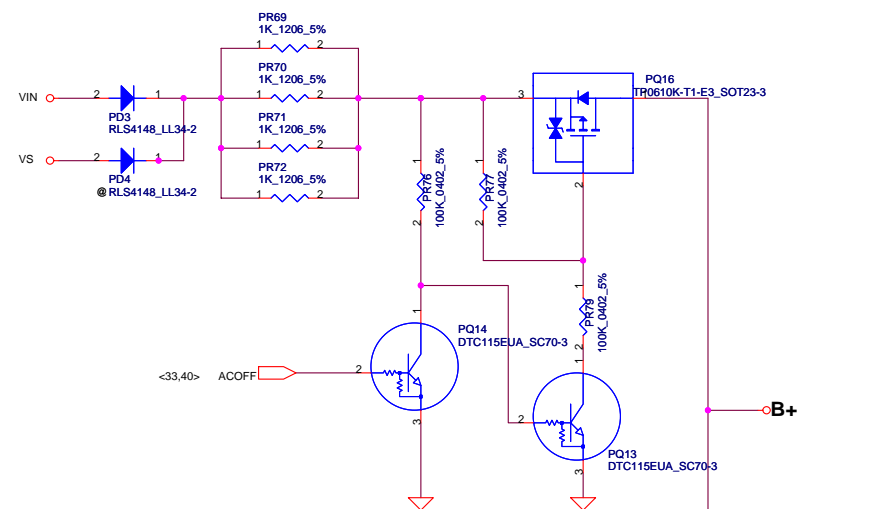
hexainf@hotmail.com  
gratuito - free of charge.



Vin Detector		
High	18.135	17.566
Low	14.866	14.355
	17.011	14.063

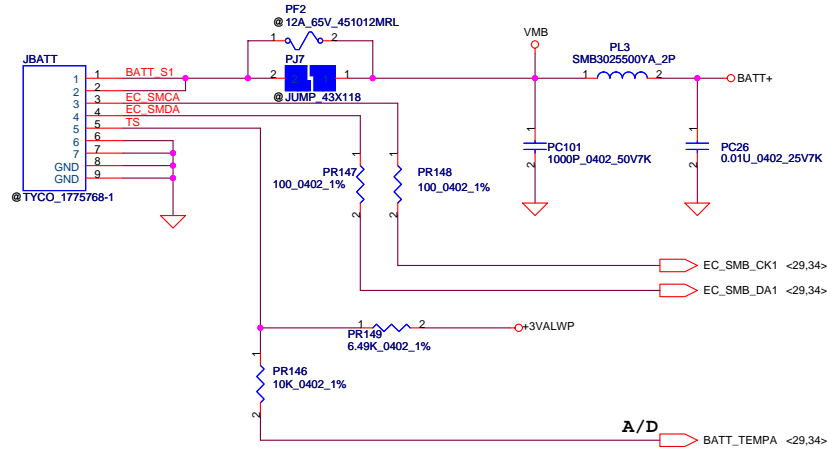
ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	13.843V	14.247V	14.636V
L-->H	14.936V	15.381V	15.814V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

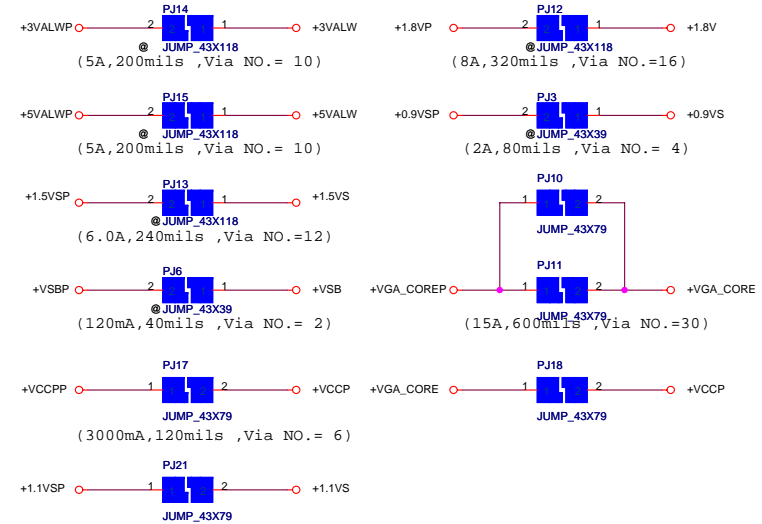
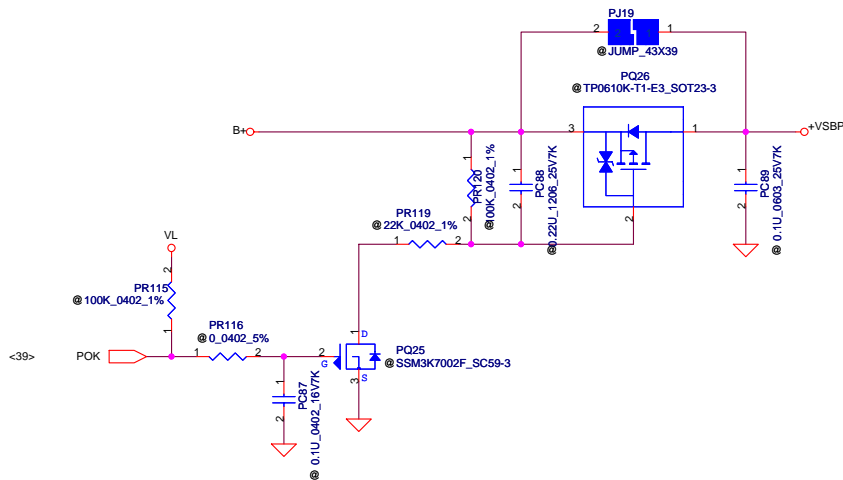
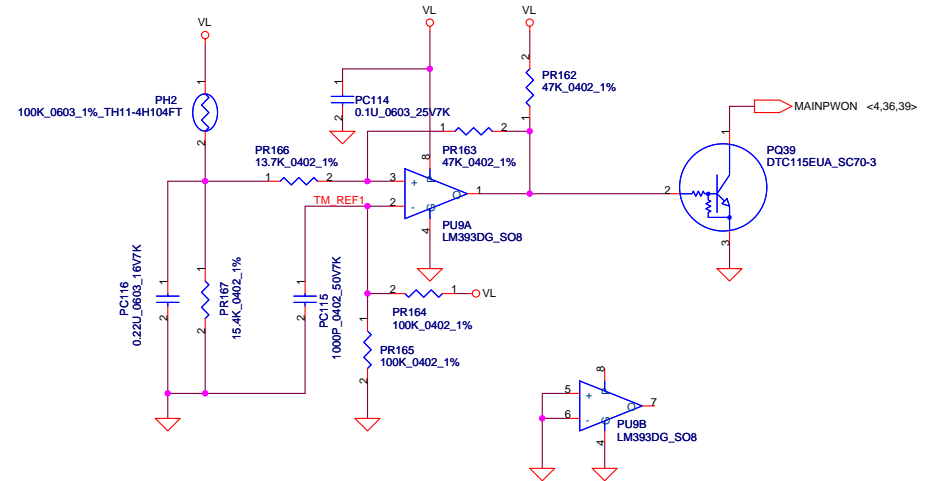


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/06/22	Deciphered Date	2008/06/22	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DCIN & DETECTOR
Size	Document Number	Rev		1.0
Date:	Monday, May 12, 2008	Sheet	44	of 53

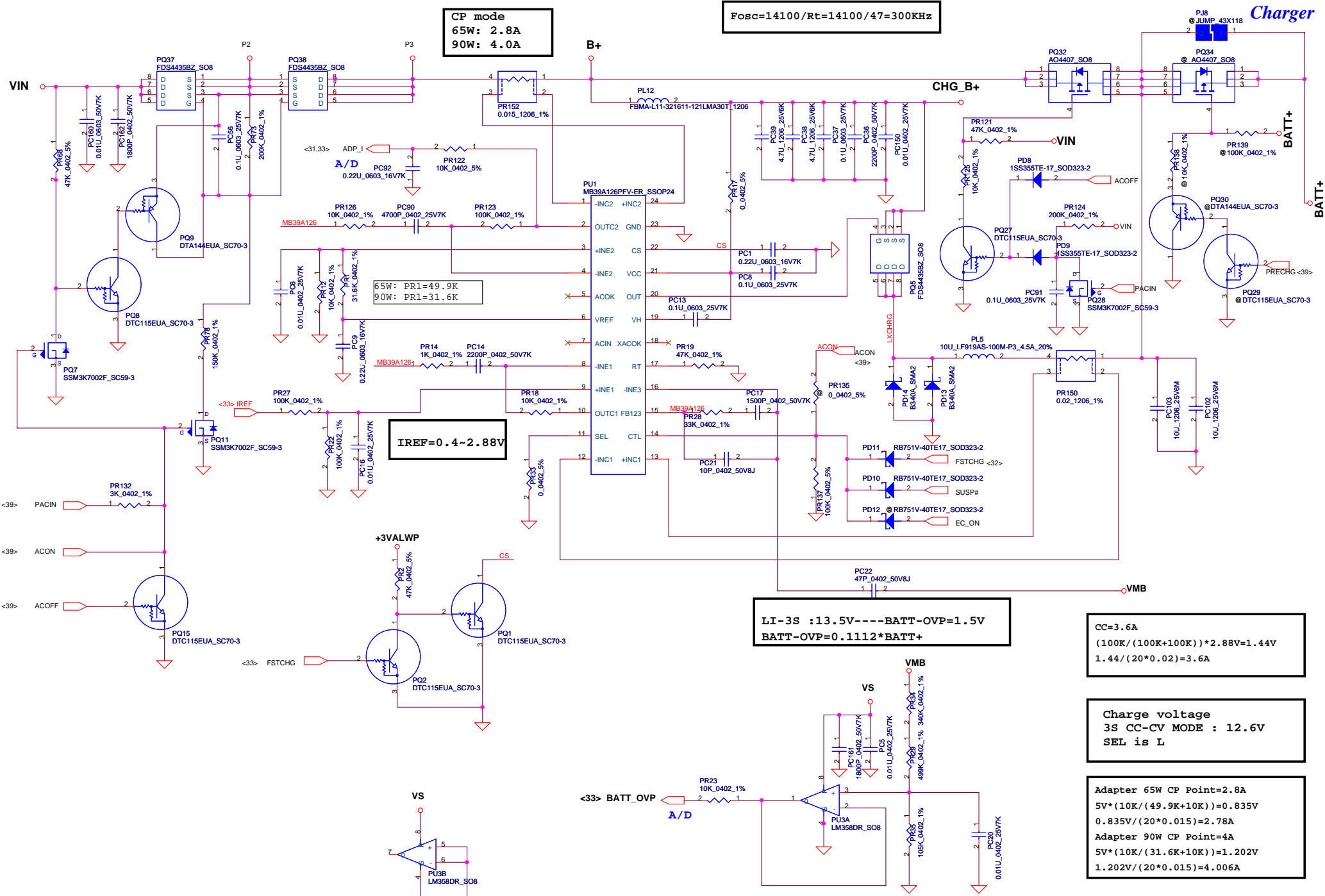
hexainf@hotmail.com  
gratuito - free of charge.



PH1 under CPU bottom side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title	BATTERY CONN / OTP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number				Rev 1.0
Date:	Monday, May 12, 2008	Sheet	45	of	53



**CP mode**  
 65W: 2.8A  
 90W: 4.0A

$F_{osc} = 14100 / R_t = 14100 / 47 = 300KHz$

$I_{REF} = 0.4 \sim 2.88V$

**LI-3S : 13.5V --- BATT-OVP = 1.5V**  
**BATT-OVP = 0.1112 \* BATT+**

CC=3.6A  
 $(100K / (100K + 100K)) * 2.88V = 1.44V$   
 $1.44V / (20 * 0.02) = 3.6A$

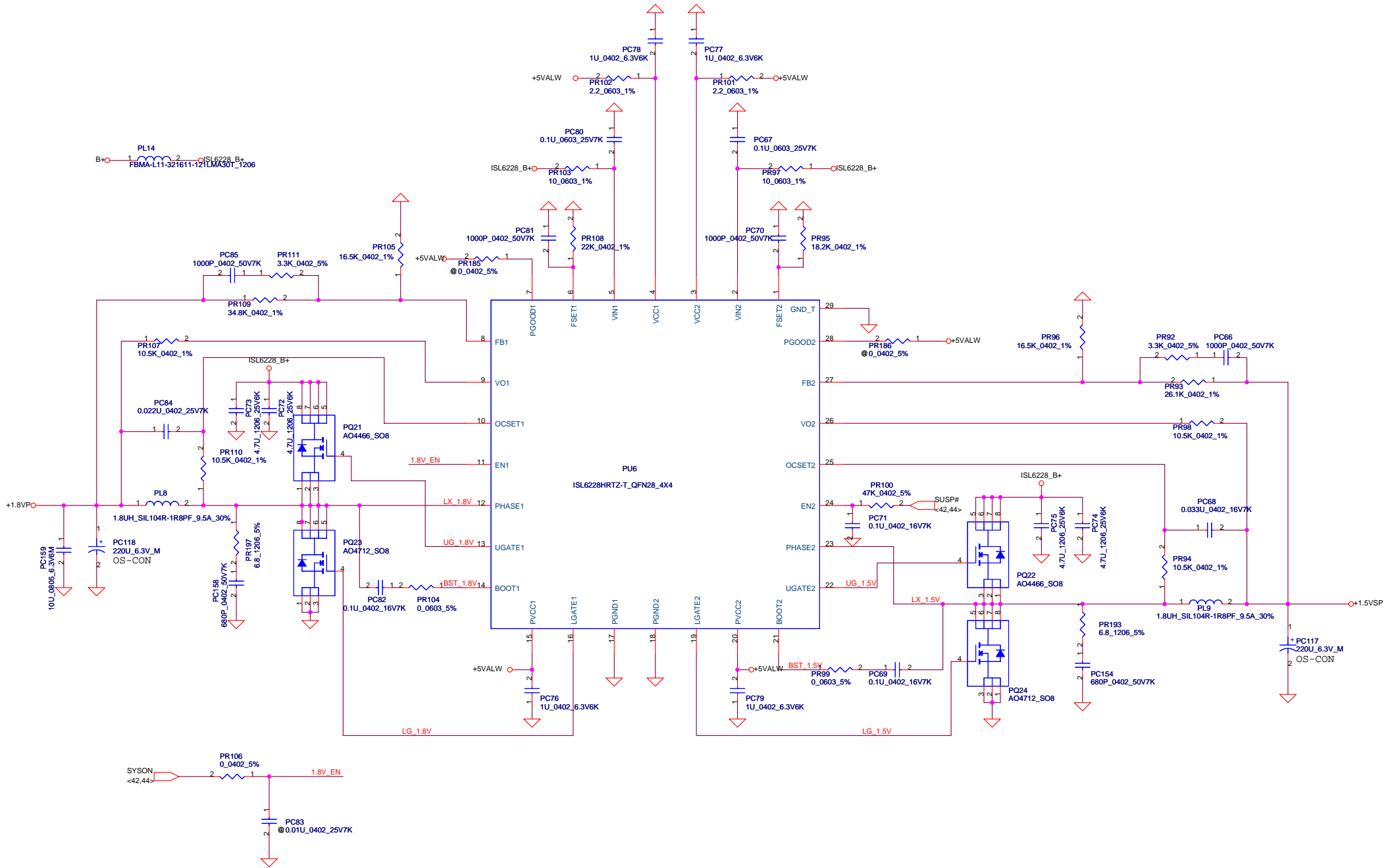
Charge voltage  
 3S CC-CV MODE : 12.6V  
 SEL is L

Adapter 65W CP Point=2.8A  
 $5V * (10K / (49.9K + 10K)) = 0.835V$   
 $0.835V / (20 * 0.015) = 2.78A$   
 Adapter 90W CP Point=4A  
 $5V * (10K / (31.6K + 10K)) = 1.202V$   
 $1.202V / (20 * 0.015) = 4.006A$

Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Compal Electronics, Inc.	
				<b>CHARGER</b>	
Size	Document Number	Date:	Monday, May 12, 2008	Sheet	46 of 53
B					Rev 1.0

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

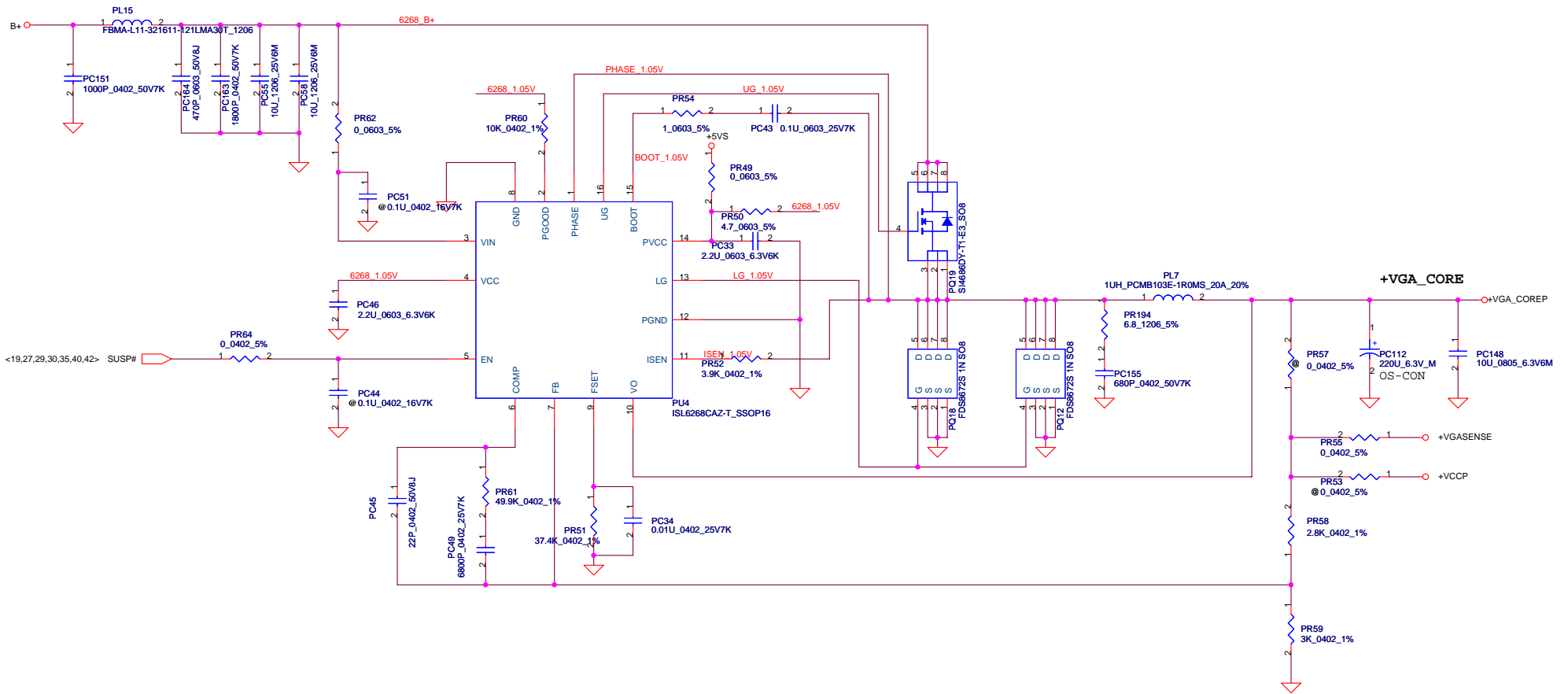




hexainf@hotmail.com  
gratuito - free of charge.

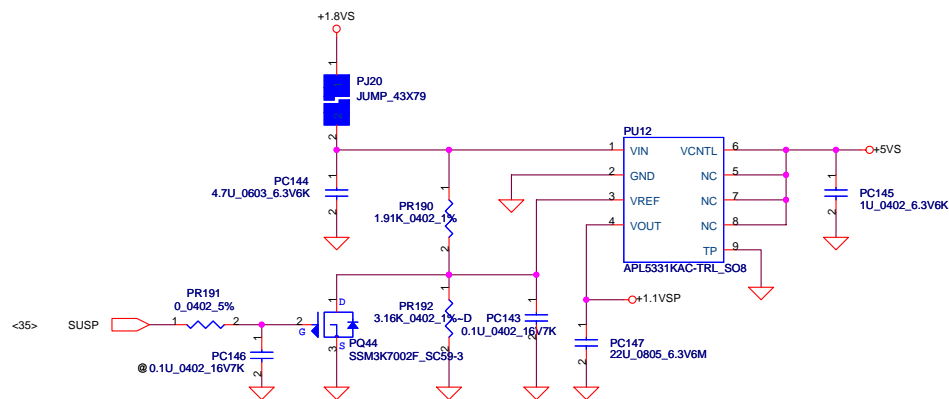
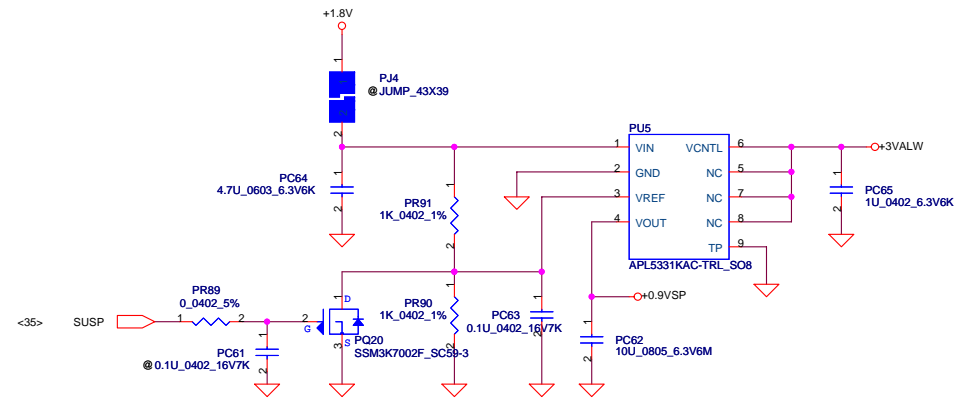
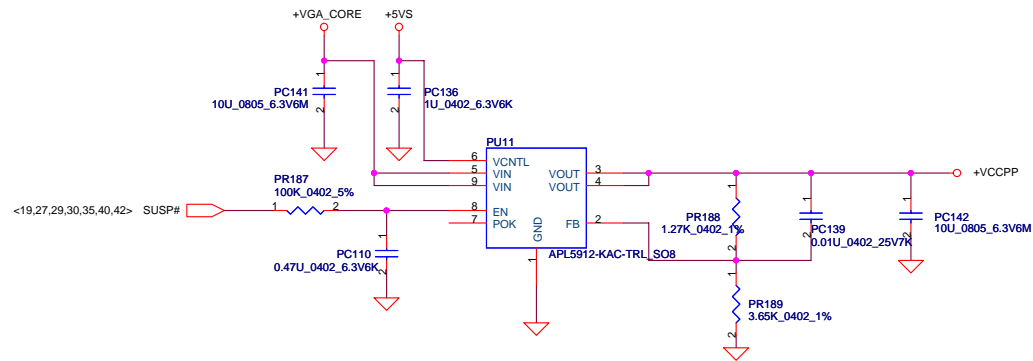
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/06/22	Deciphered Date	2008/06/22	Title	1.8V / 1.5V
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
Date:	Monday, May 12, 2008	Sheet	48	of	53



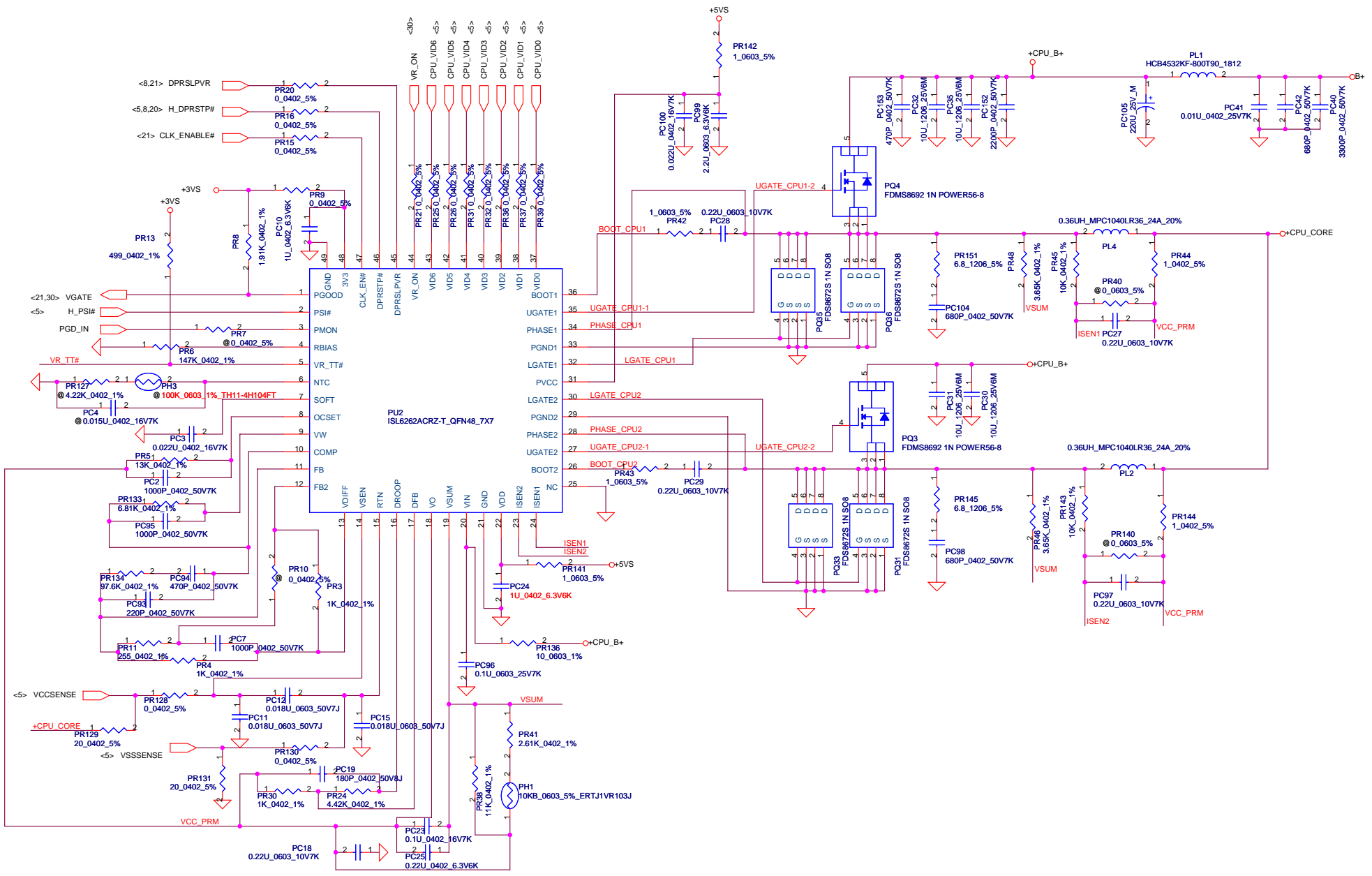


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				VGA_CORE	
Size	Document Number			Rev	1.0
Date: Monday, May 12, 2008		Sheet 49 of 53			

hexainf@hotmail.com  
gratuito - free of charge.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title VCCP/0.9V/1.1V	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date: Monday, May 12, 2008	Rev 1.0
				Sheet 50	of 53



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				+CPU_CORE
Size	Document Number	Rev		
Custom		1.0		
Date:	Monday, May 12, 2008	Sheet	51 of 53	

hexainf@hotmail.com  
gratuito - free of charge.

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

Security Classification		Compal Secret Data		Title	
Issued Date	2005/06/01	Deciphered Date	2006/06/01	<b>Compal Electronics, Inc.</b>	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size	Rev
				Document Number	
Date: Monday, May 12, 2008				Sheet 51 of 51	
				<b>Power PIR</b>	
				<b>J1WA3/A4 LA4212P</b>	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	P29	C615 change to R615 and BOM Structure change to PM@	Fix DIS Audio issue
2	12/10	P20, P21	R104 & R154 BOM Structure change to PM@	Reduce cost
3	12/10	P16	R86, R645, R646, R650, R651, R652 & R653 BOM Structure change to PM@	Reduce cost
4	12/10	P29	R614 change from 10K to 45.3ohm R615 change from 12K to 54.9ohm	Fix UMA Audio issue
5	12/10	P08	R79 change from 33 to 10ohm R80, R81, R82 & R85 change from 0 to 22 ohm	Fix UMA Audio issue
6	12/10	P30	The C783 links to GND	Fix Internal MIC issue
7	12/10	P41	Add L45 & L46 MBCL608121Y2F Bead	Fix F/B issue
8	01/02	P11	Change C126 package	
9	01/02	P28	Add R707 to connect VGATE to M_PWR0K	Modify power sequence
10	01/02	P16	Add R699 to connect +VGASENSE	
11	01/02	P16	Remove U3.P1	
12	01/02	P19	Add R700 to connect GND	
13	01/02	P11	Add C707	for +VCC_DMI
14	01/02	P16	Add C788	for nvidia request for +PEX_PLLVDD
15	02/27	P08	change R147 from 511 ohm 1% to 499 ohm 1%	
16	02/27	P23	change D4 location	
17	02/27	P23	Add D25 , D26 for ESD	
18	02/27	P25	Add D27 , D28 & D29 for ESD	
19	02/27	P29	Add R713 connect to 1.5V	
20	02/27	P31	change C550 , C570 , C506 & C507 to 0.1uF 0603	Fix pop noise issue
21	05/08	P05	Add R726 1k ohm & C808 0.1uF to fix issue.	
22	05/08	P16	Remove R48 for EMI request.	
23	05/08	P27	Change R554 from 0 ohm to 33 ohm for EMI request.	
24	05/08	P28	Add R566 10 ohm & C733 10pF for EMI request.	
25	05/08	P30	Add R327 47 ohm & C458 33pF for EMI request.	
26	05/08	P35	Change C501 & C514 from 15pF to 12pF	
27	05/08	P37	Add D31 (PJDLCO5_SOT23-3) for ESD request.	
28	05/08	P41	Add C494, C522, C564 & C568 220pF for EMI request	