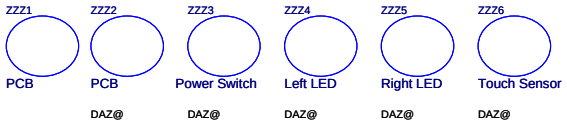

JIWA3/A4

Schematics Document

Mobile Penryn uFCPGA
Intel Cantiga_GM/PM+ICH9-M

Wednesday, May 14, 2008

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: JIWA3/A4_LA4212P	Rev: 1.0
Date:	Sheet 1 of 53	

Compal confidential
File Name :

ZZZ1
15W_PCB_LA4212P

Right LED Board

Swithch & CAP SENSE LEDs Board

Left LED Board

VRAM 16*16
VRAM 32*16
page20,21

nVIDIA NB9M
page16,19

PCI-E X16

Mobile Penryn
uFCPGA-478 CPU
page5,6,7

Clock Gen.
SLG8SP556VTR
ICS9LPRS387AKLFT
page22

H_A#(3..35)
H_D#(0..63)

FSB
667/800/1066MHz

HDMI CONN
page23

Level Shifter
PS8101T
page23

PCI-E

Intel Cantiga GMCH
PCBGA 1329
page 8,9,10,11,12,13

DDR2 -667 (1.8V)
DDR2 -800 (1.8V)

Dual Channel

DDR2-SO-DIMM X2
BANK 0, 1, 2, 3
page 14,15

CRT & TV OUT
page25

LVDS I/F

LVDS Connector
page24

DMI

C-Line

AMP&Audio Jack
page24

AZALIA

12*USB2.0

Audio Codec
AMOM_CX20561
page30

MODEM_CX20548

PCI Express
Mini card Slot 1
page32

6*PCI-E BUS

Intel ICH9-M
mBGA-676
page26,27,28,29

4*SATA serial

BCM5906
10/100/LAN
page33

Card Reader
JMB 385
page36

New Card
page40

LPC BUS

Camera Conn
page40

BlueTooth Conn
page32

USB conn X4
page43

RJ45 CONN
page34

EC
ENE KB926
C version
page35

Card reader(XD/SD
MMC/MS/MS-Pro
HD SD)
page36

Int.KBD
page37

BIOS
page38

Touch Pad
page37

SATA HDD
Connector
page39

SATA CDROM
Connector
page39

SUB Board page32,36

*Right LED
*Left LED
*SWITCH & CAP sensor

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **MB Block Diagram**

Size	Document Number	Rev
Custom	JIWA3/A4_LA-4212P	1.0

Date: Monday, May 12, 2008 | Sheet 2 of 53

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@
CARD@
WLAN@
HDMI@
HDMI_PM@
HDMI_GM@
BT@

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD	CAP BRD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X

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Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: MB Notes List

Size: B | Document Number: JIWA3/A4_LA4212P | Rev: 1.0

Date: Monday, May 12, 2008 | Sheet 3 of 53

Voltage Rails

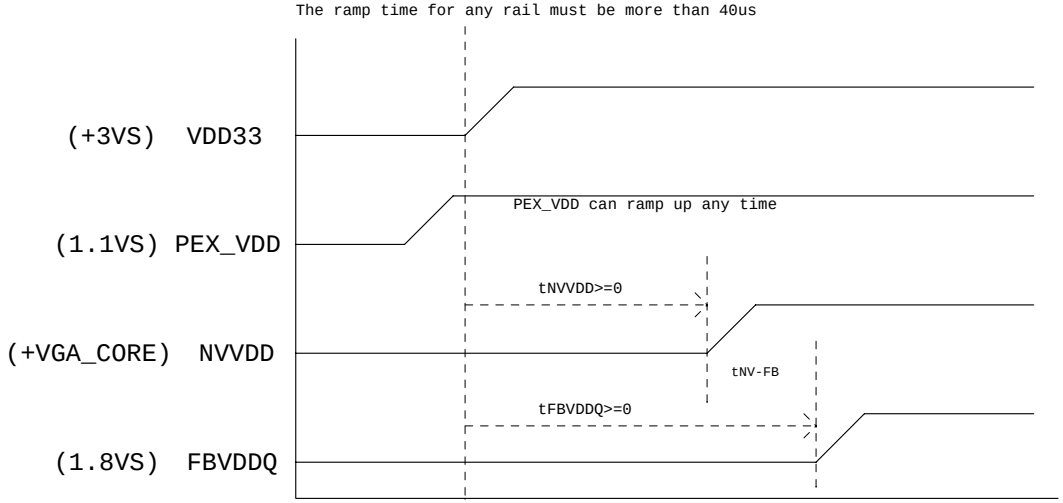
Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
	(V)	GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVDD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.225A			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
TOTAL	3.3	0.645A			

POWER SQUENCE



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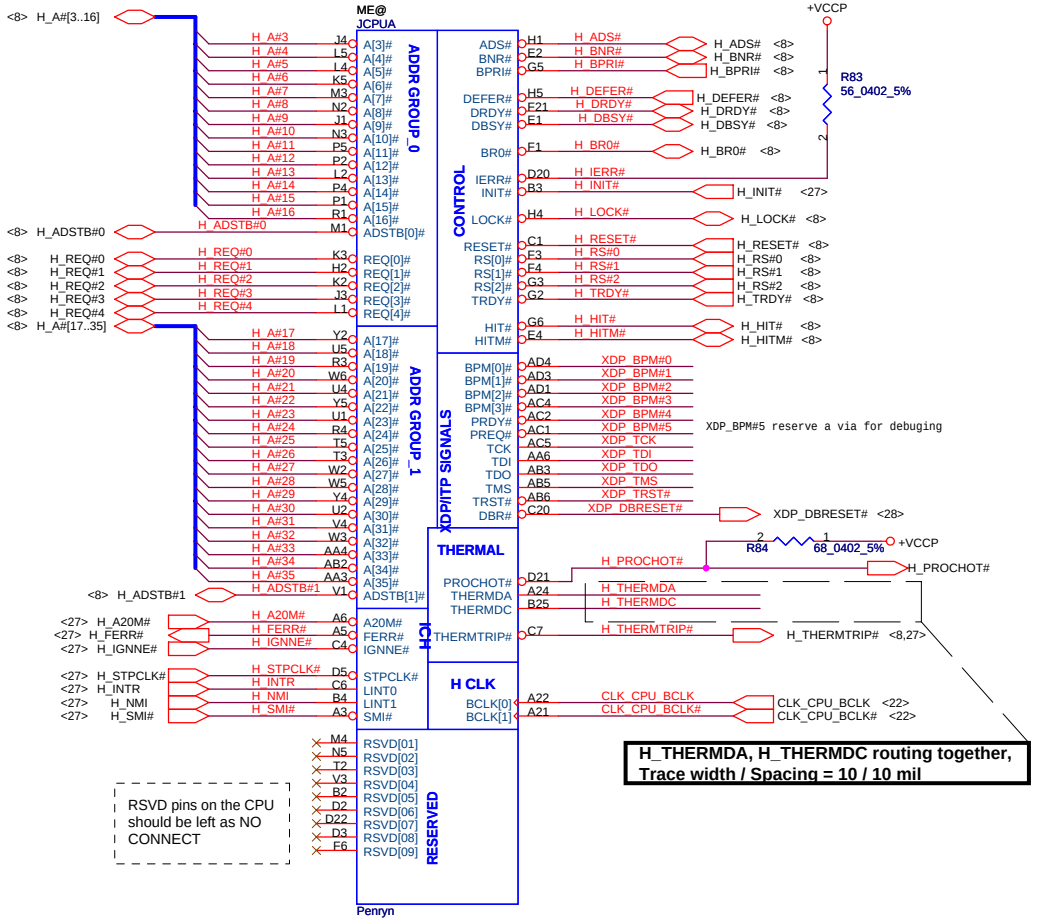
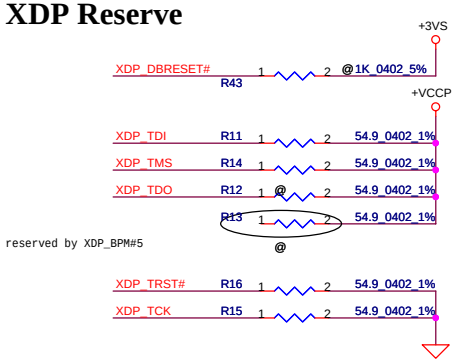
Title: VGA Notes List

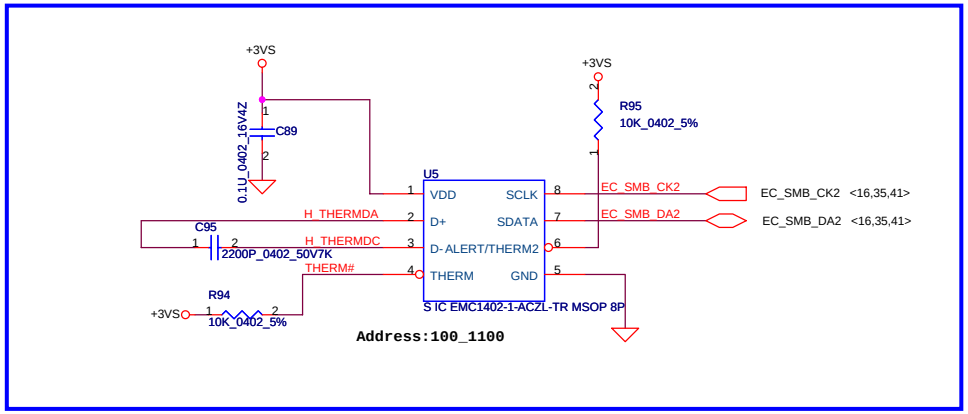
Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

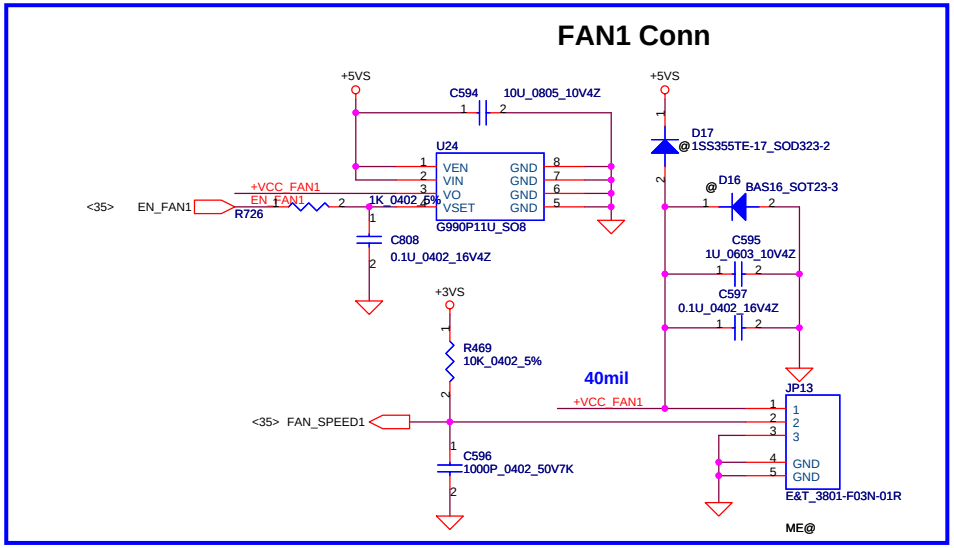
Date: Monday, May 12, 2008 Sheet 4 of 53



XDP Reserve







Security Classification	Compal Secret Data		
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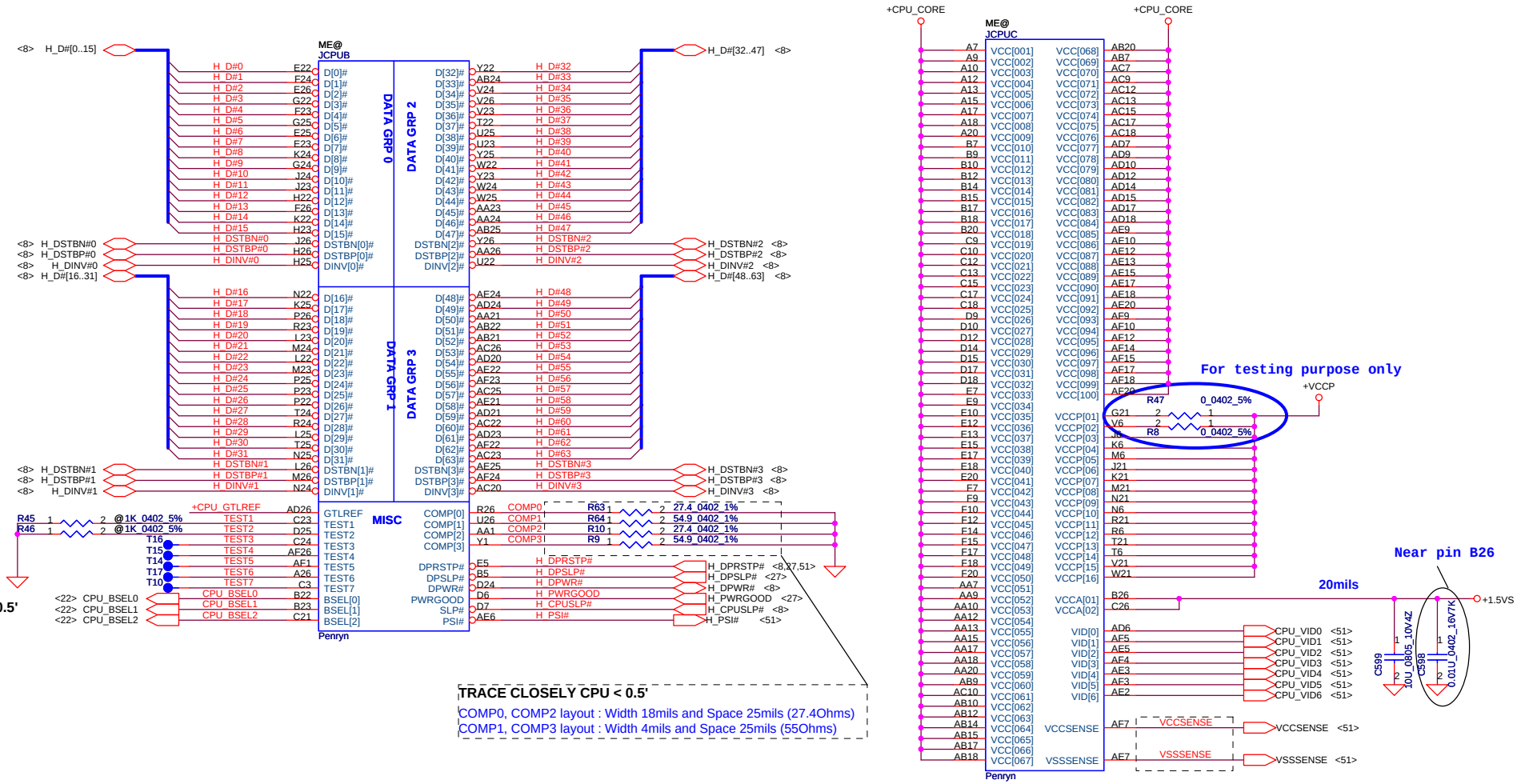
Compal Electronics, Inc.

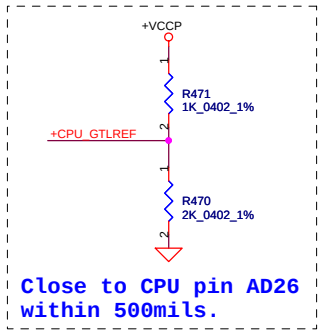
Title: **Penryn (1/3)**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 Sheet 5 of 53



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

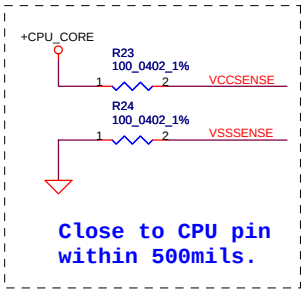


Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.
The trace width/space/other is 16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



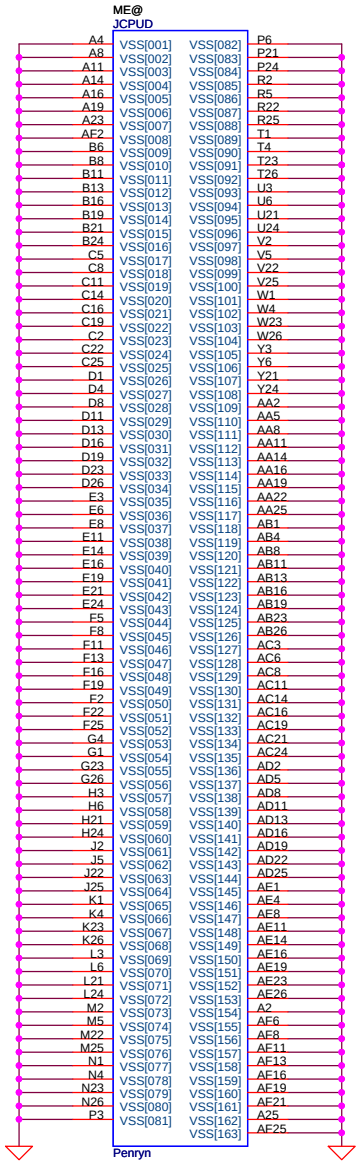
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

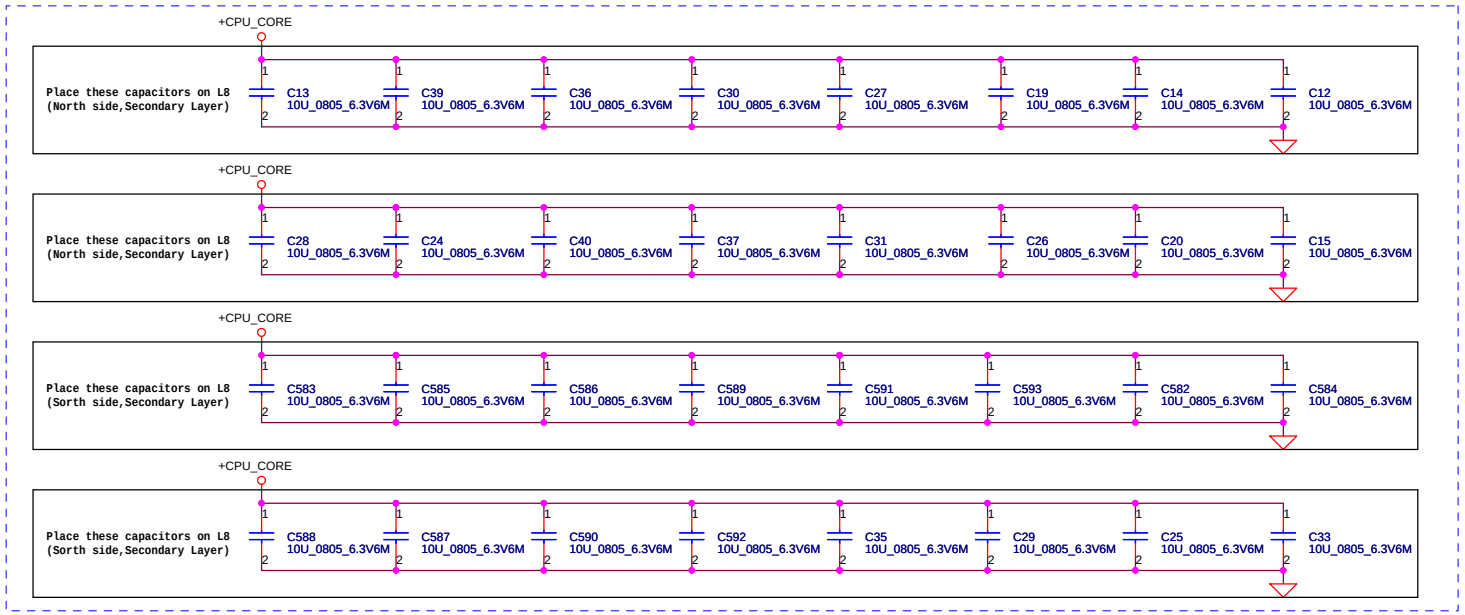
Compal Electronics, Inc.

Title: Penryn (2/3)

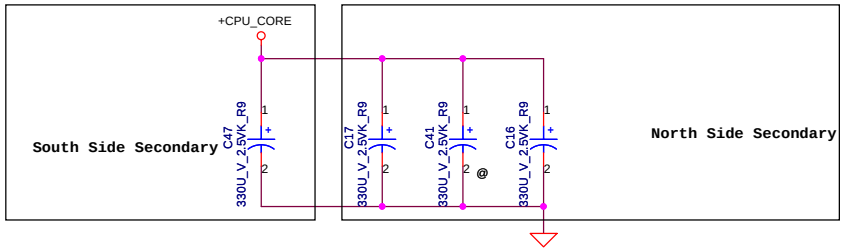
Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 6 of 53

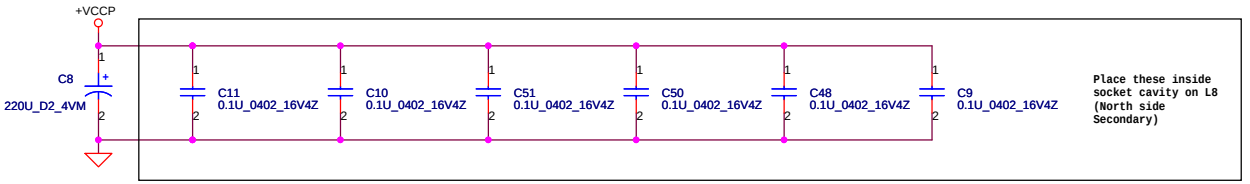




Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF



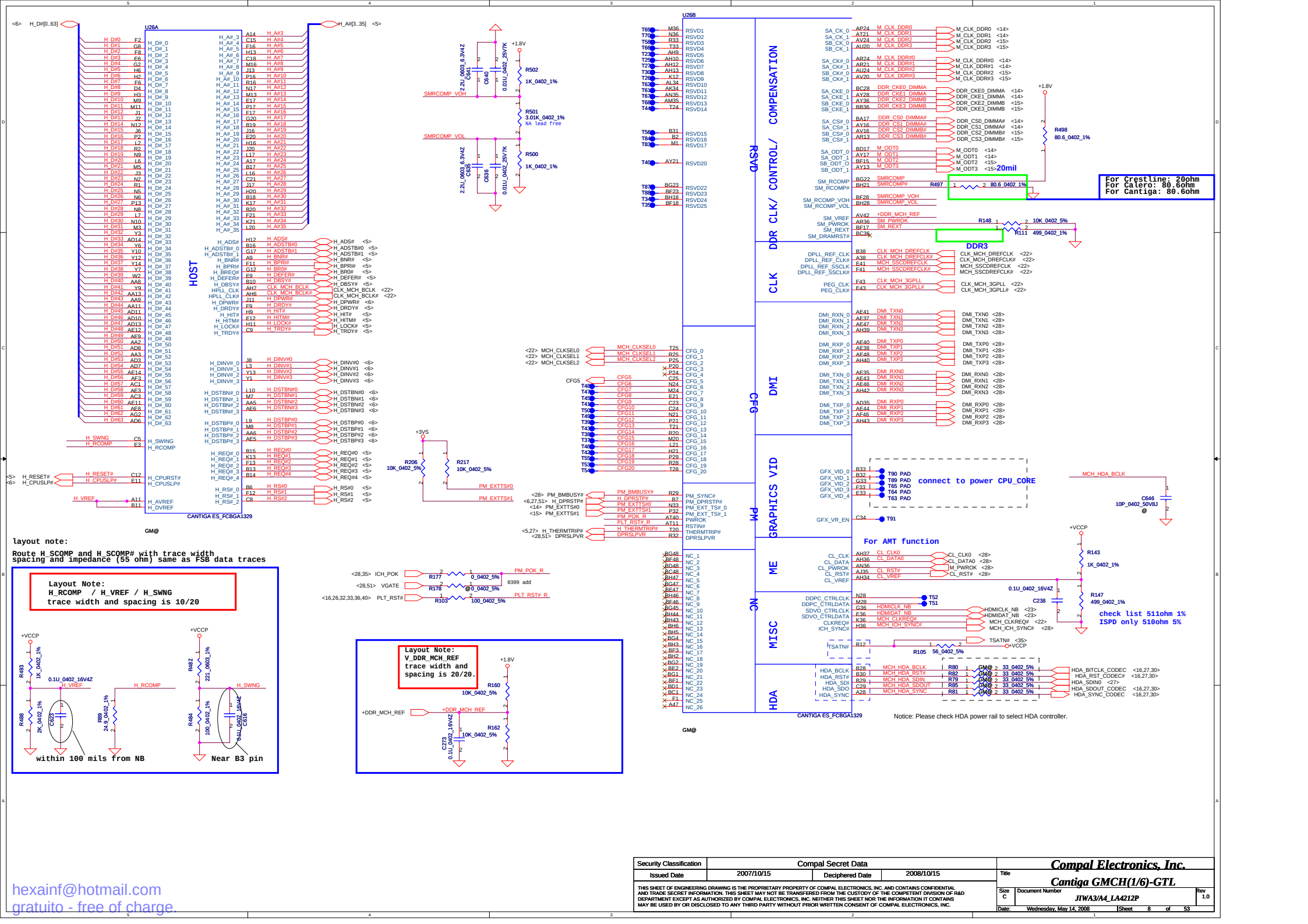
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Penryn (3/3)**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 7 of 53



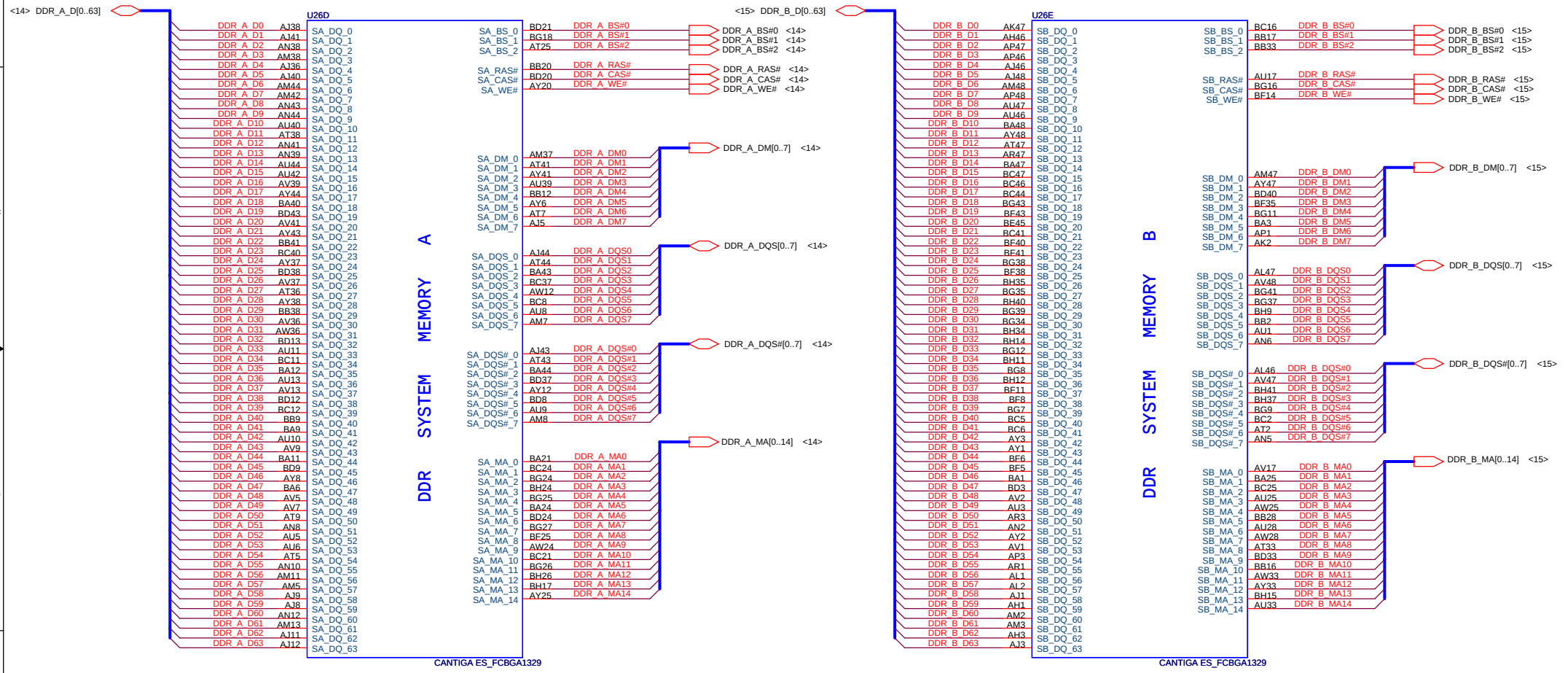
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Cantiga GMCH(1/6)-GTL

Size	Document Number	Rev
C	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 | Sheet 8 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

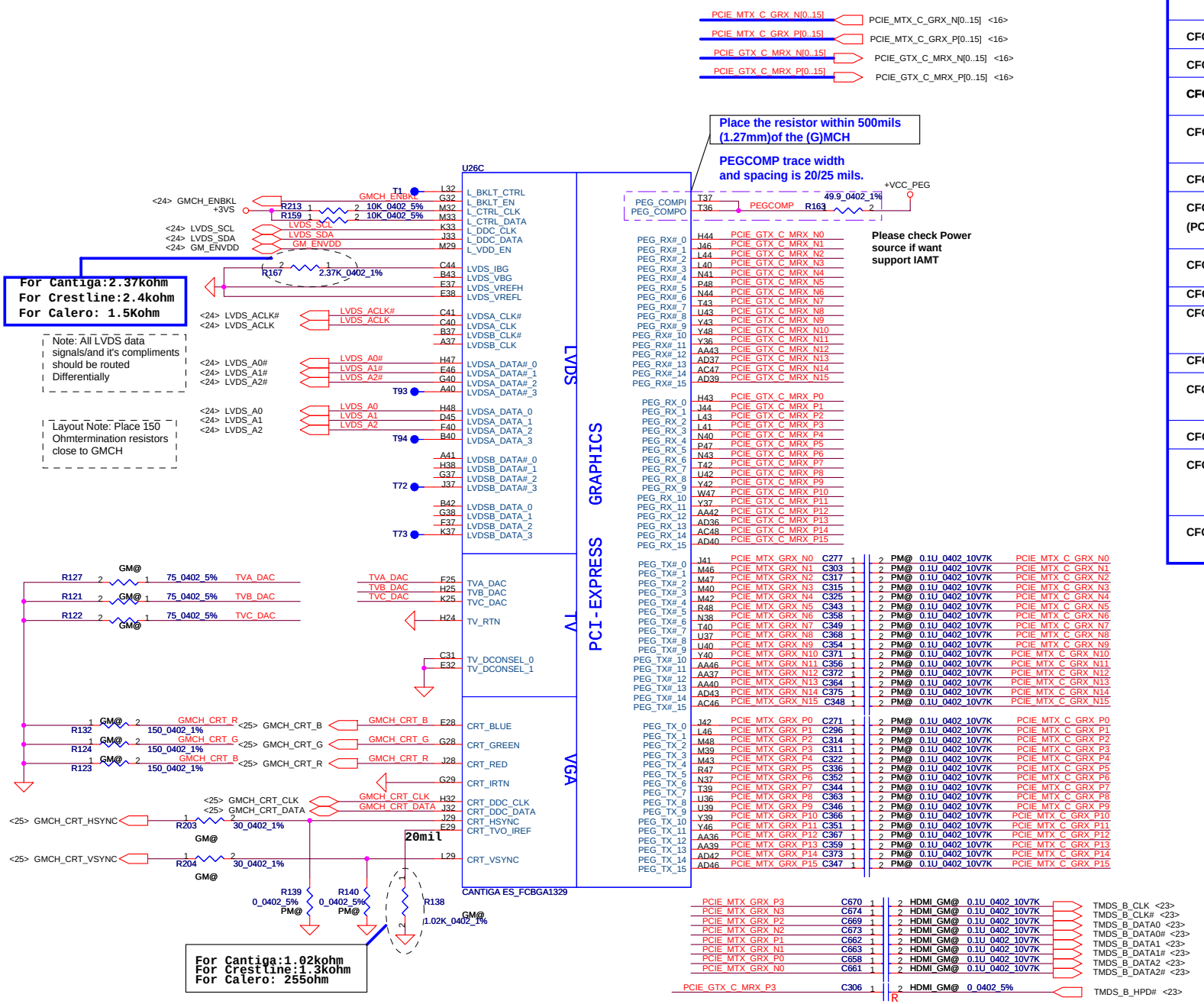
Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 Sheet 9 of 53

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



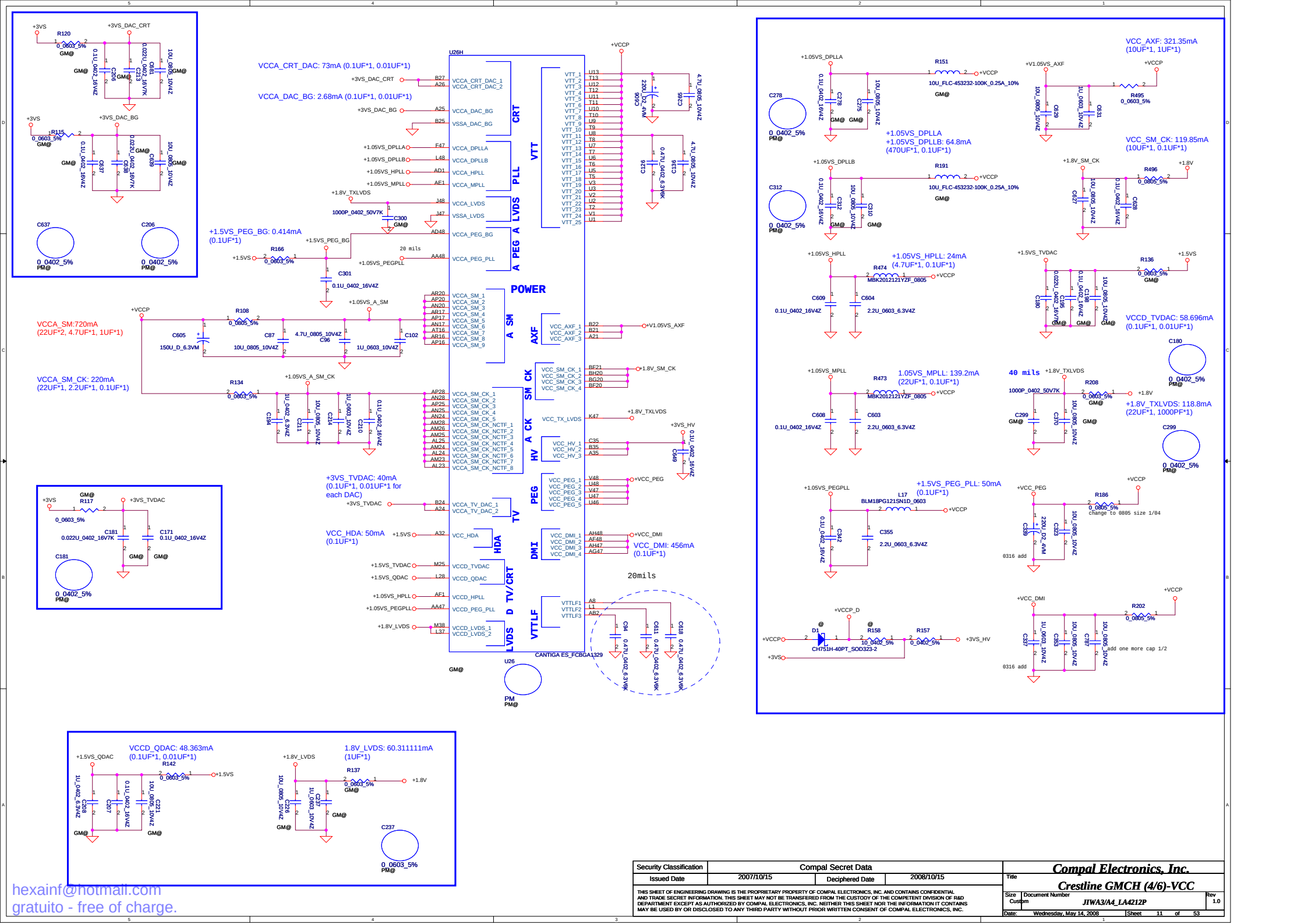
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (3/6)-VGA/LVDS/TV**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 | Sheet 10 of 53



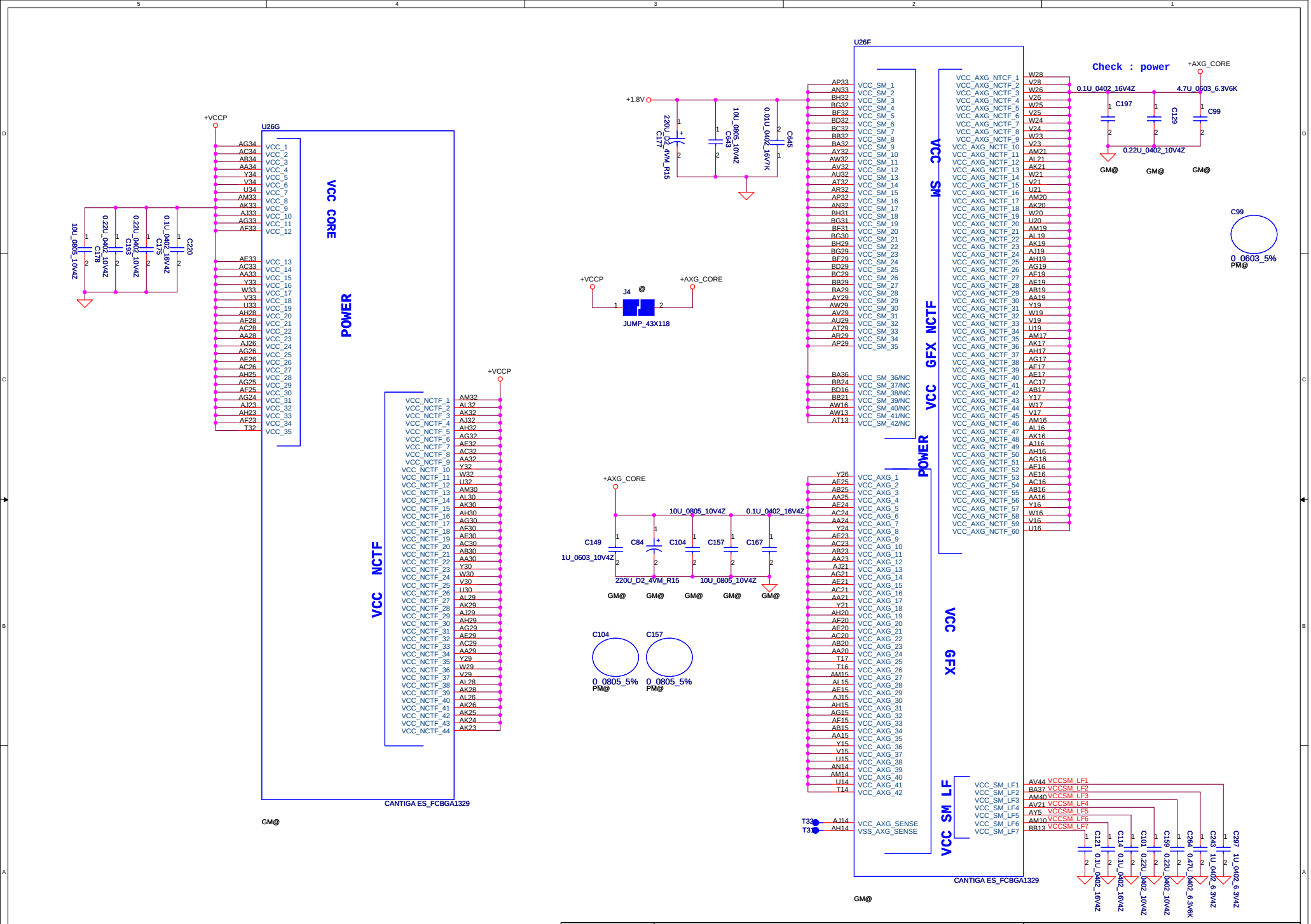
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (4/6)-VCC**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 | Sheet 11 of 53



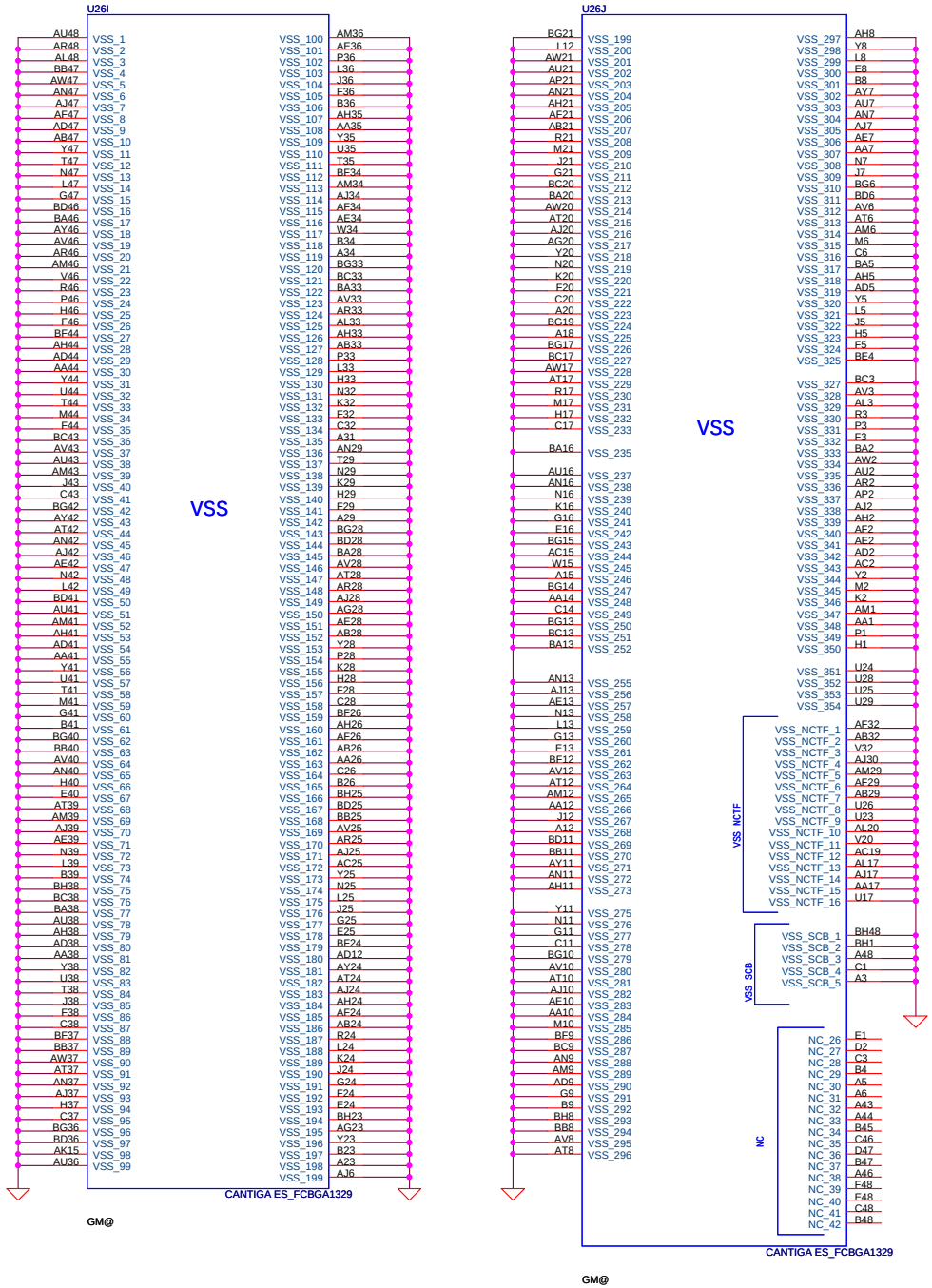
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 | Sheet 12 of 53



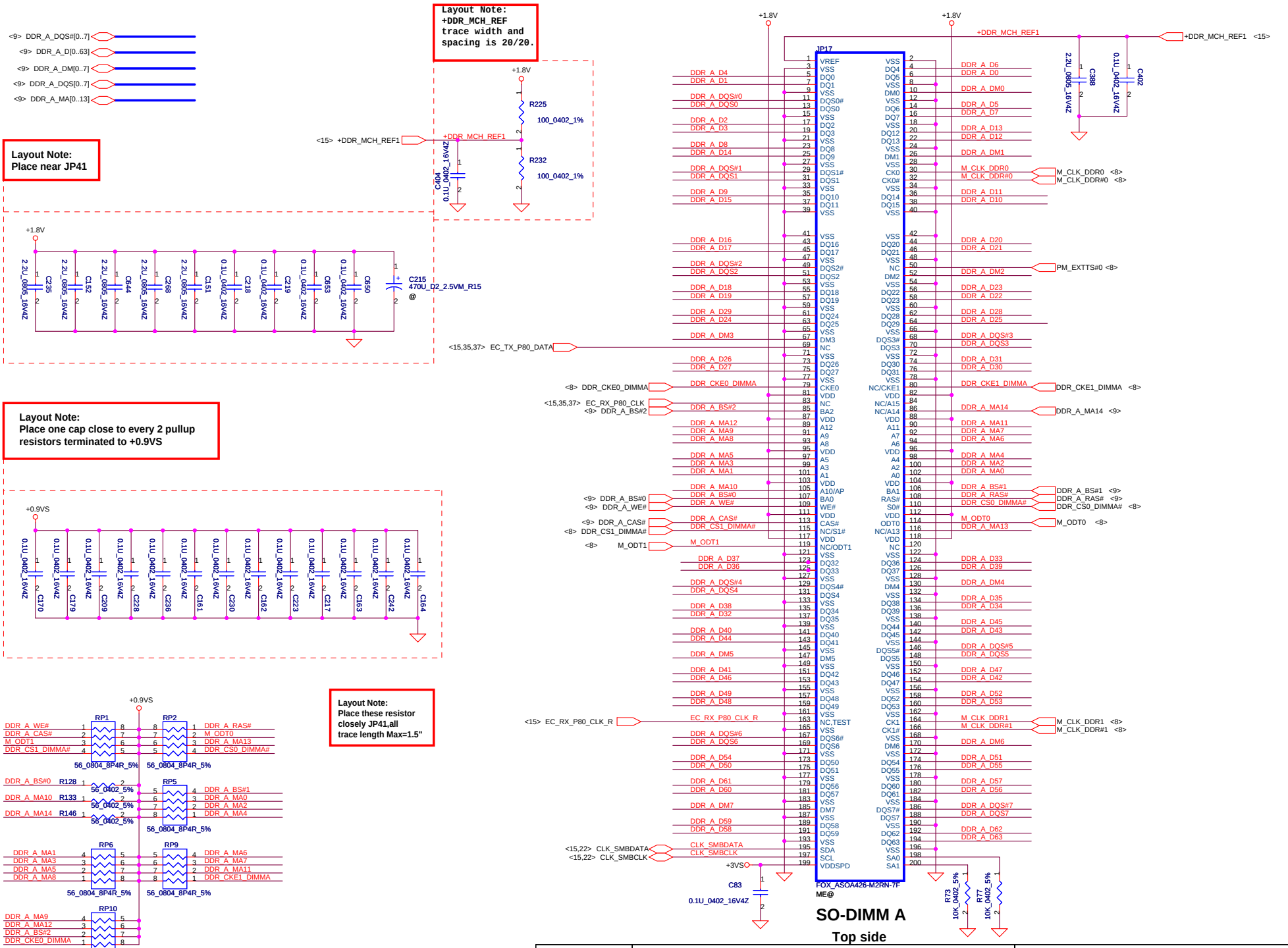
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 | Sheet 13 of 53



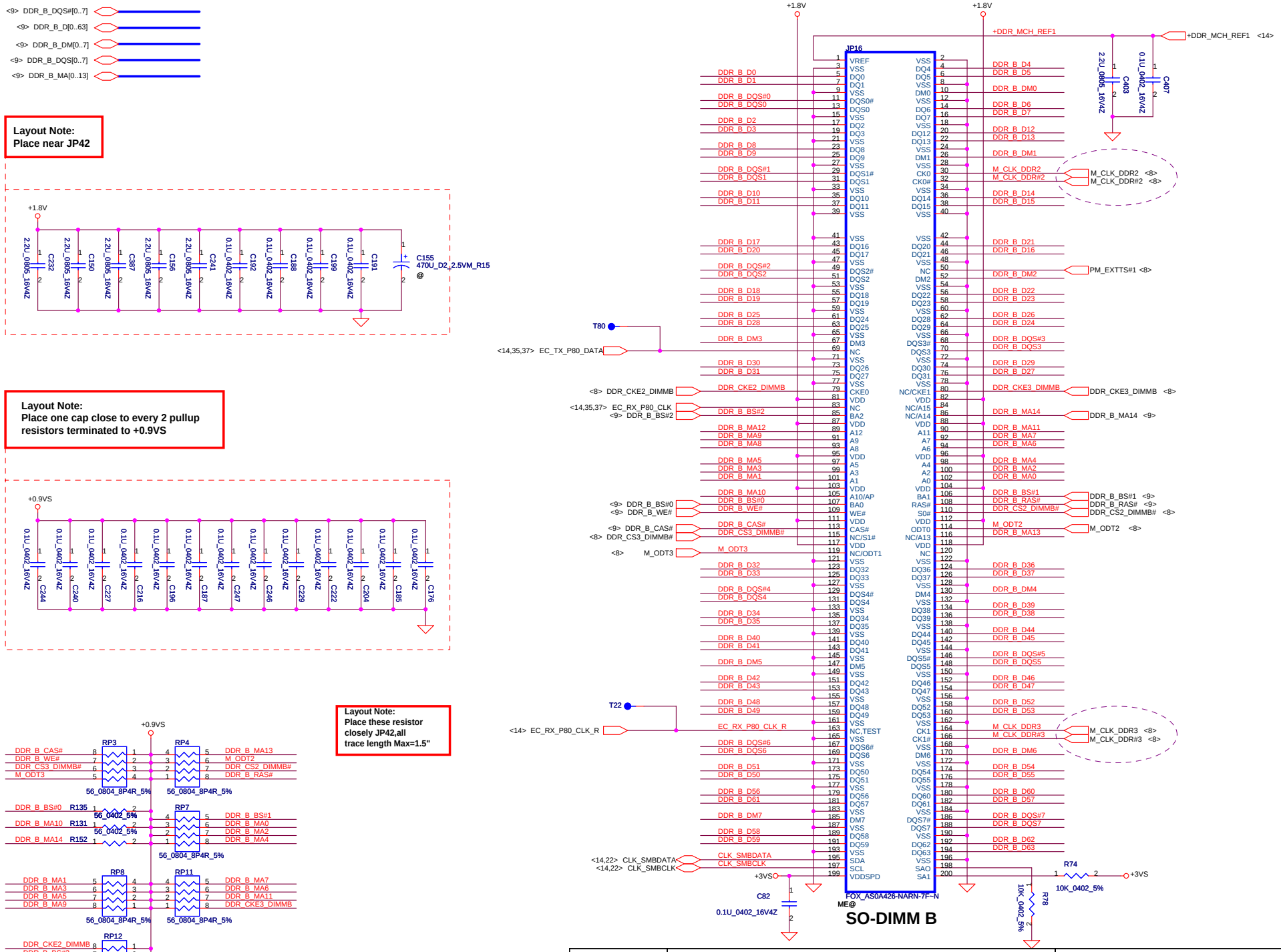
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

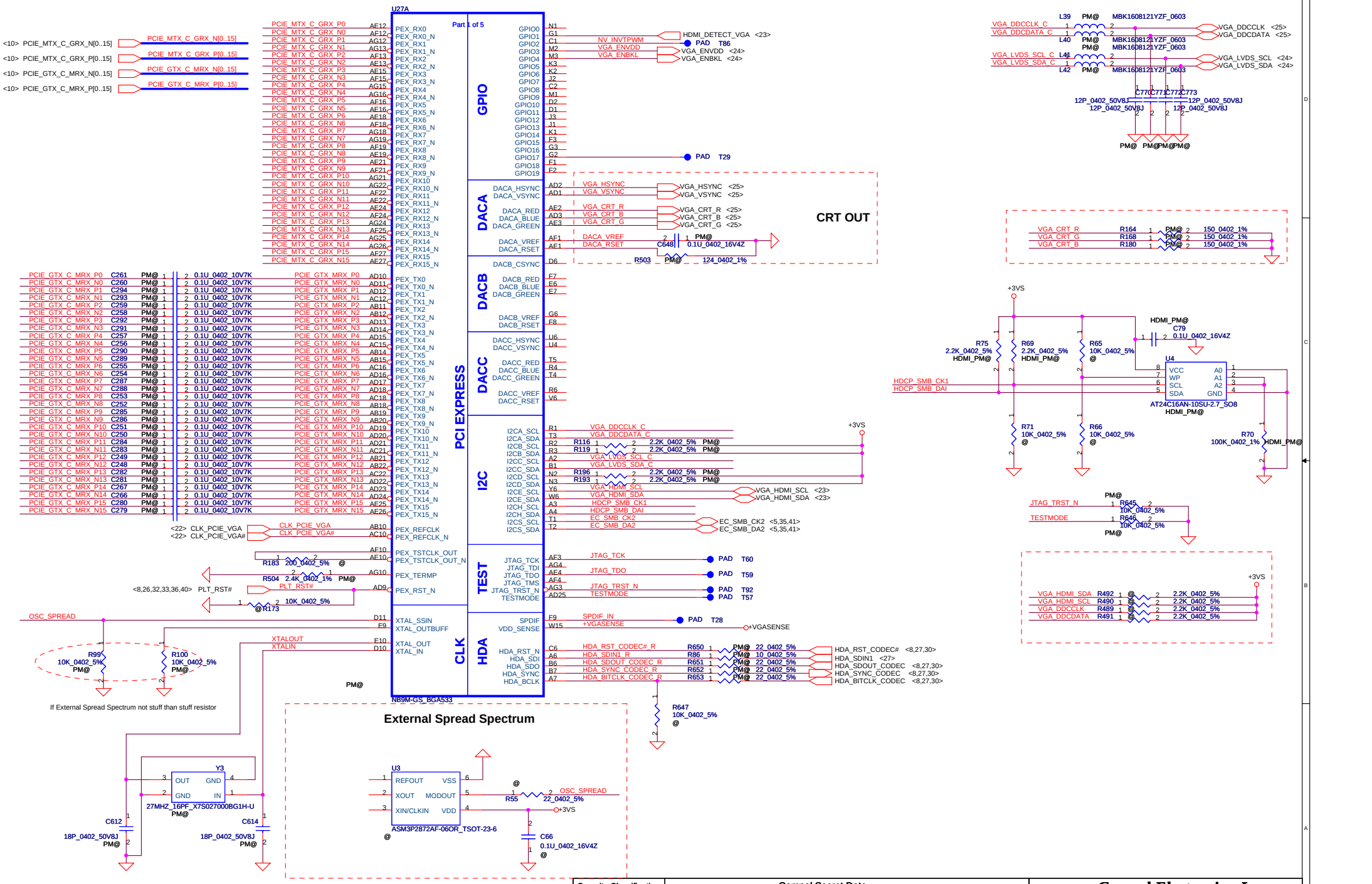
Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 14 of 53


Layout Note:
Place near JP42
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"
JP16
SO-DIMM B
FOX_AS0A426-NARN-7F--N
ME@
Compal Electronics, Inc.
DDRII-SODIMM SLOT2
Compal Secret Data
2007/10/15
2008/10/15
JIWA3/A4_LA4212P
Monday, May 12, 2008
15 of 53
hexainf@hotmail.com
gratuito - free of charge.



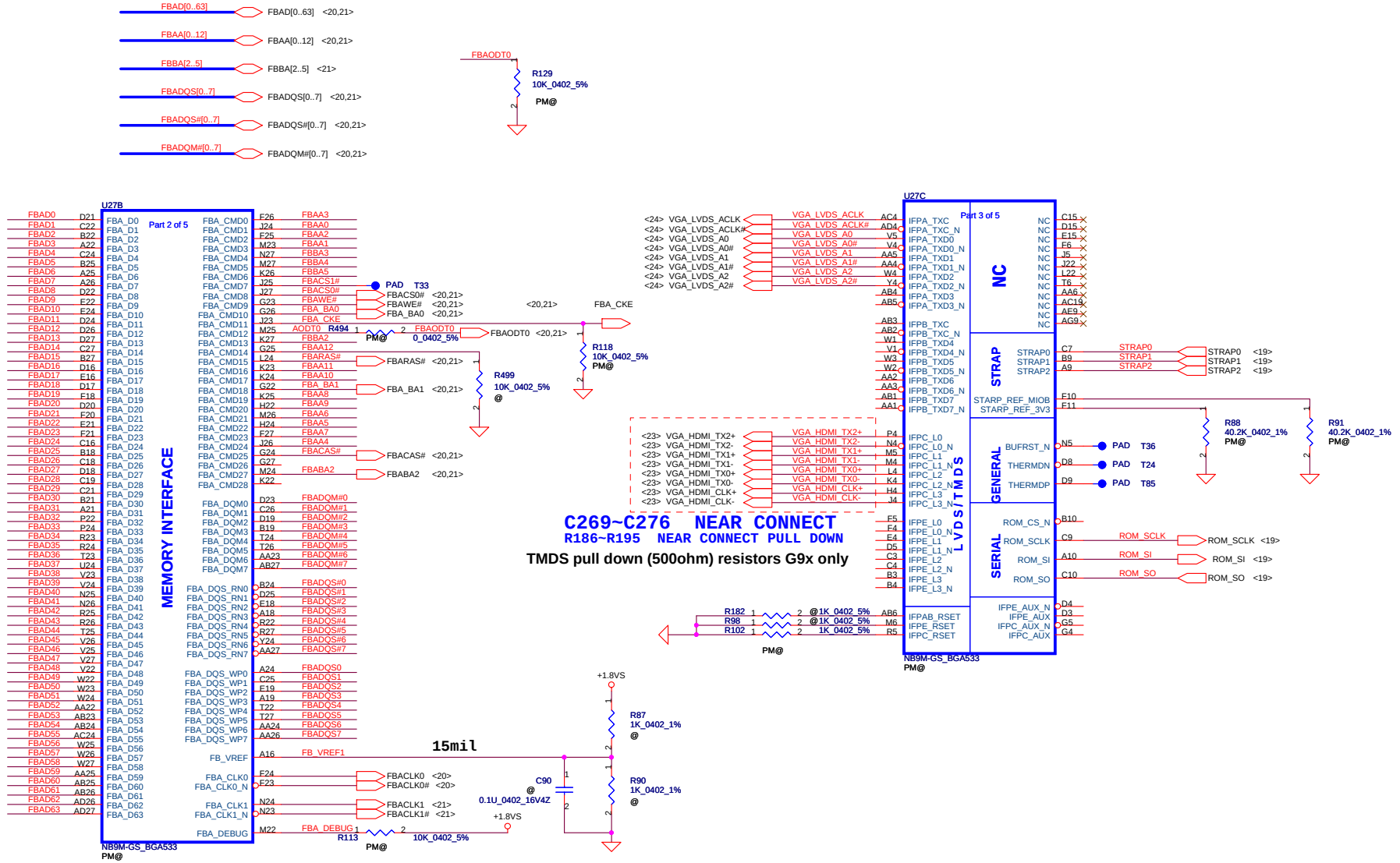
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GS PCIE,LVDS,GPIO,CLK

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 | Sheet 16 of 53



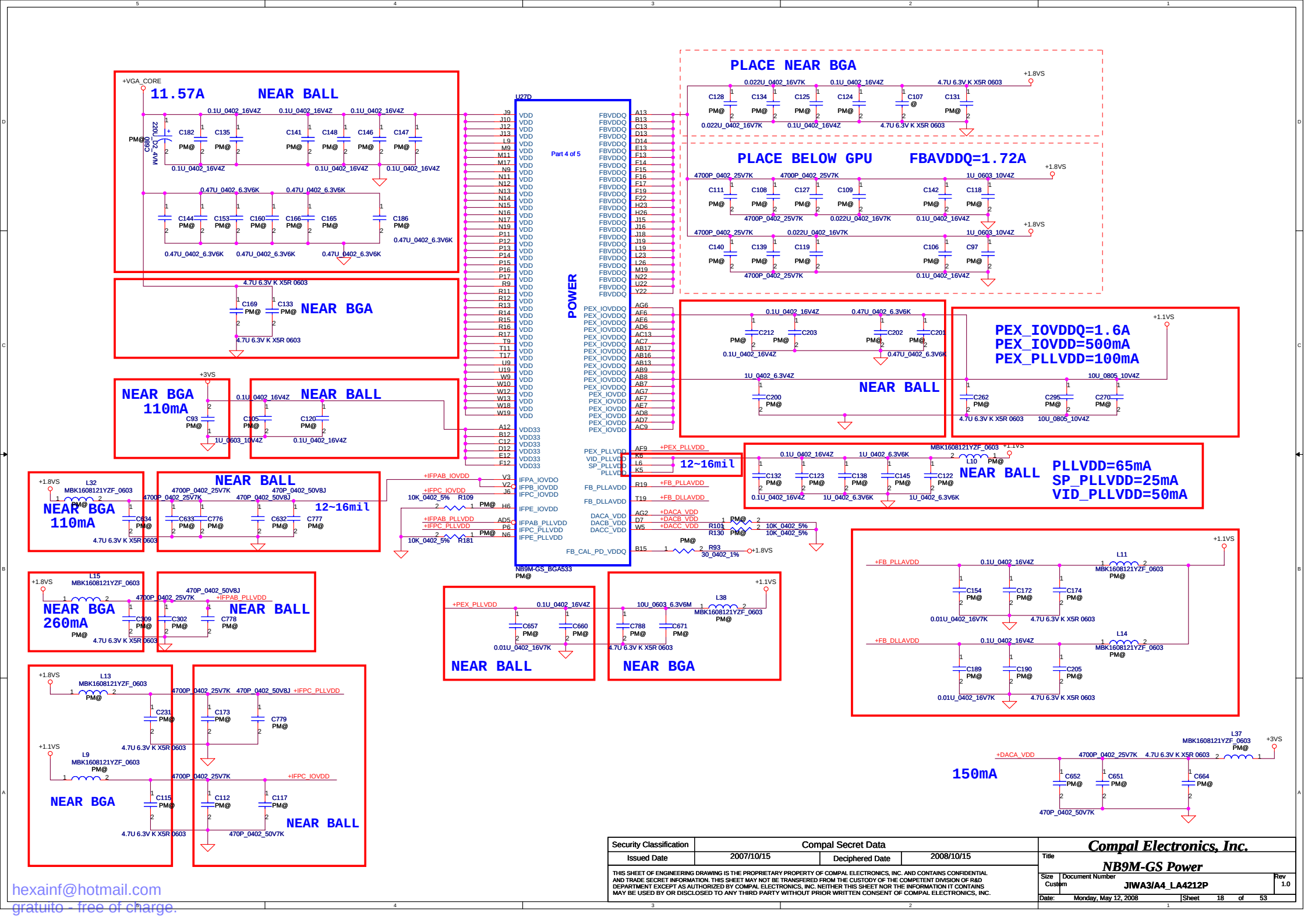
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **NB9M-GS Memory**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 17 of 53



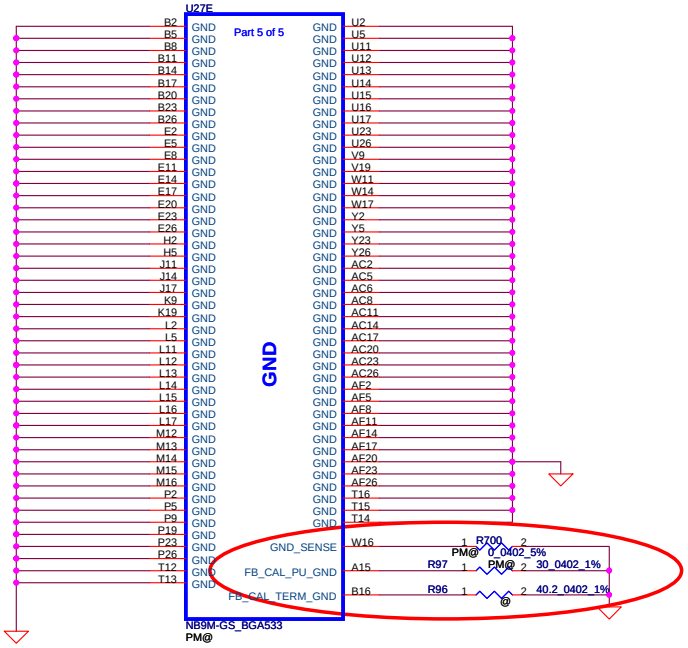
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

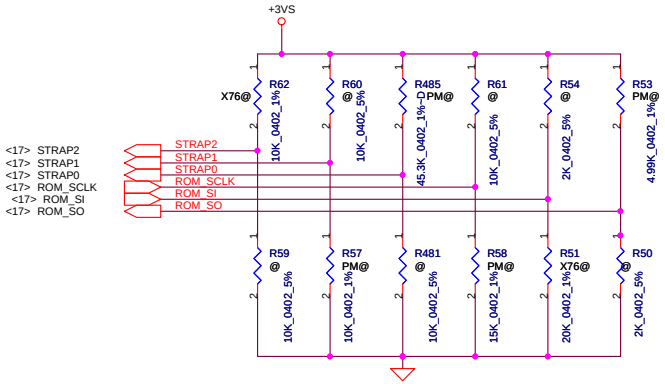
Title: NB9M-GS Power

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 18 of 53



A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



GB1 Family GPU Strap Qptions

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K
		64Mx16	PU 5K	PD 15K	PD 5K	PU 10K	PD 10K	PU 45K
	Hynix	32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
		64Mx16	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	Qimonda	32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K

Component	Manufacturer	Compal PN	
DDR2 VRAM (32M*16)	Hynix	SA00000FF30	
	Qimonda	SA00000S820	
	Samsung	SA00001VX10	

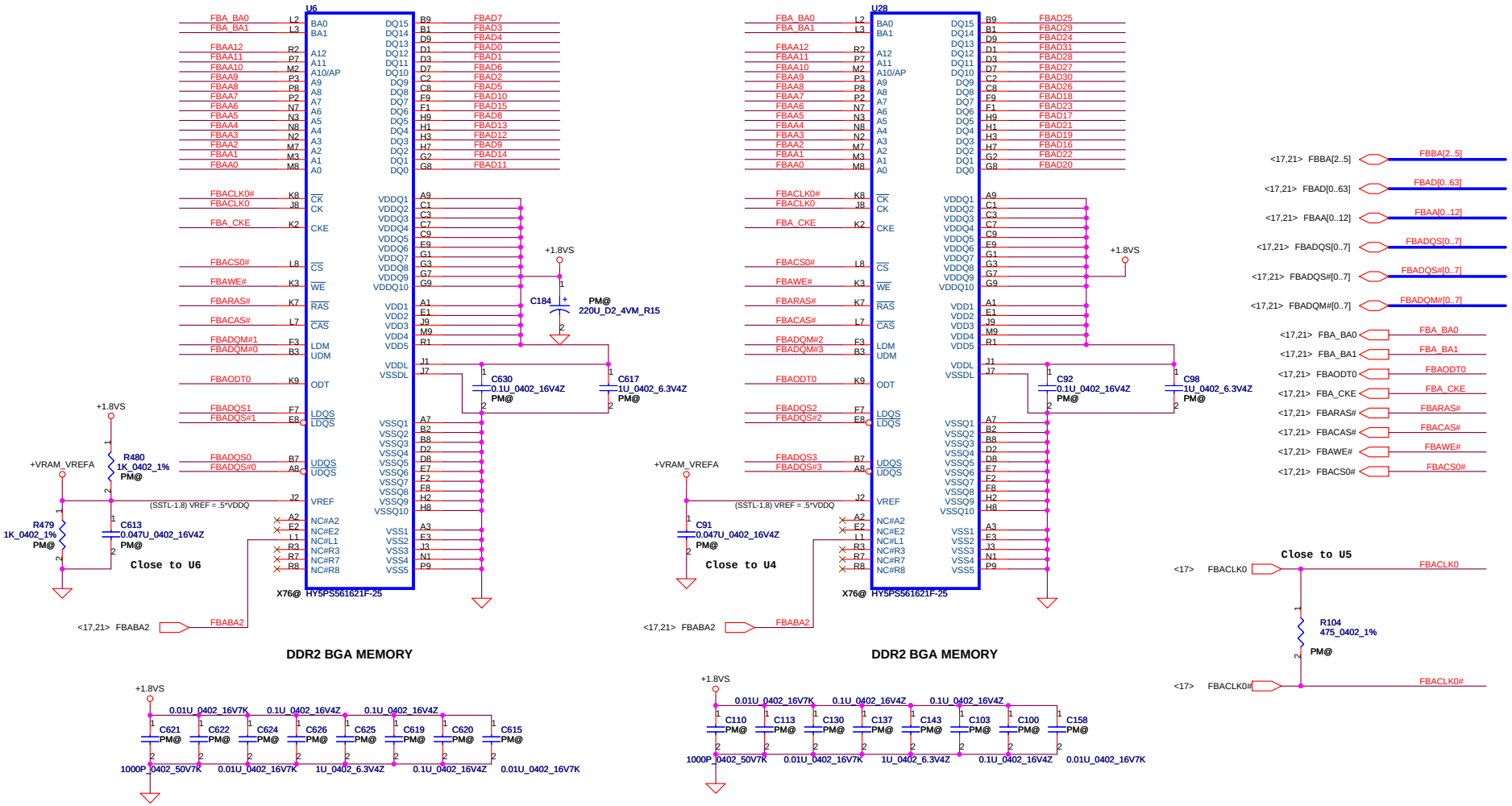
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GE GND & STRAP

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 19 of 53



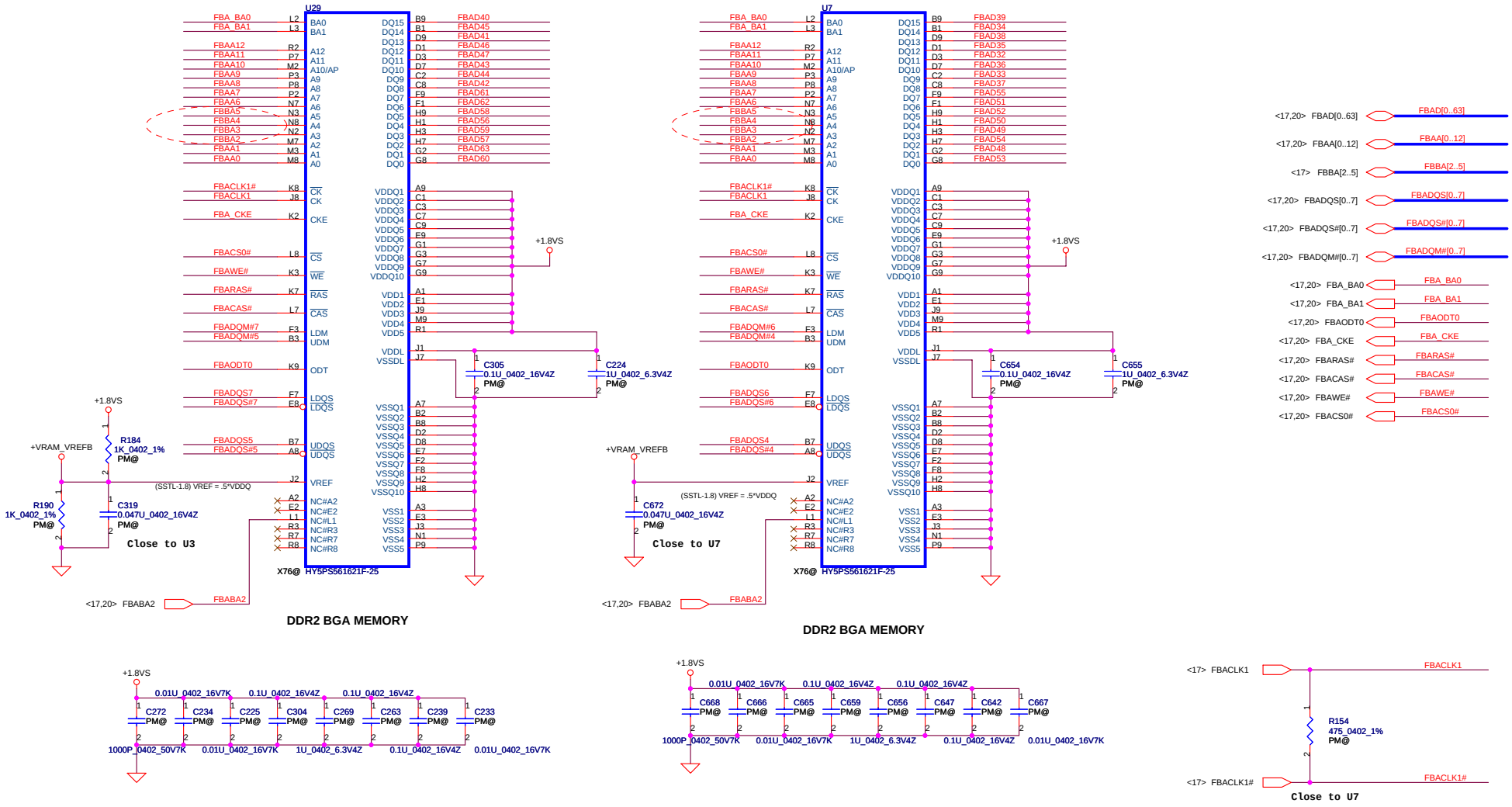
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDRA**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 20 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

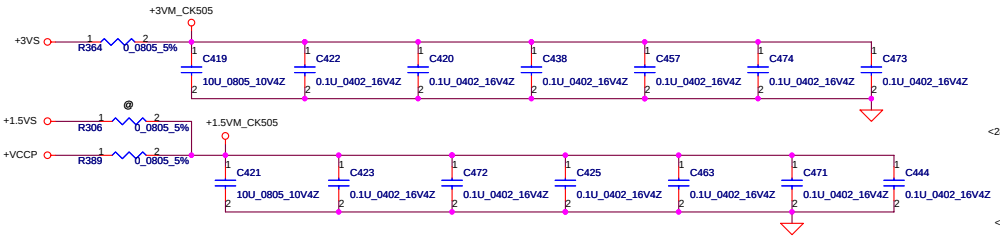
Compal Electronics, Inc.

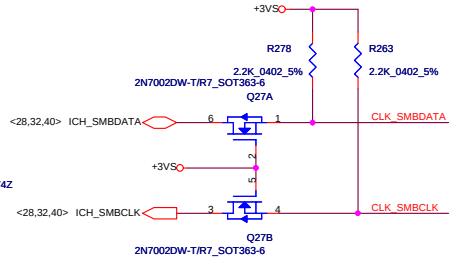
Title: **VRAM DDRB**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 21 of 53

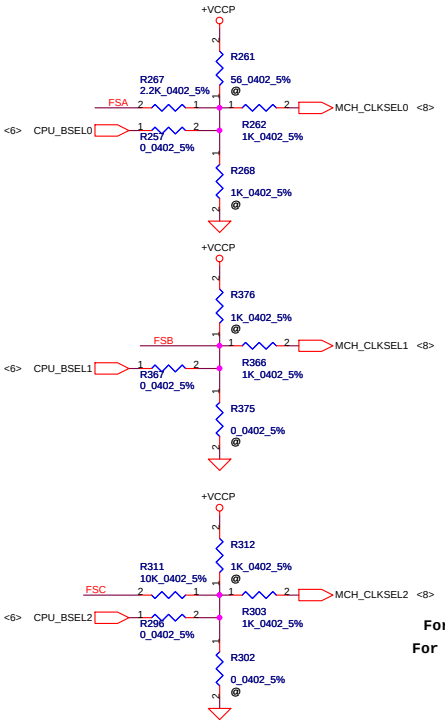
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



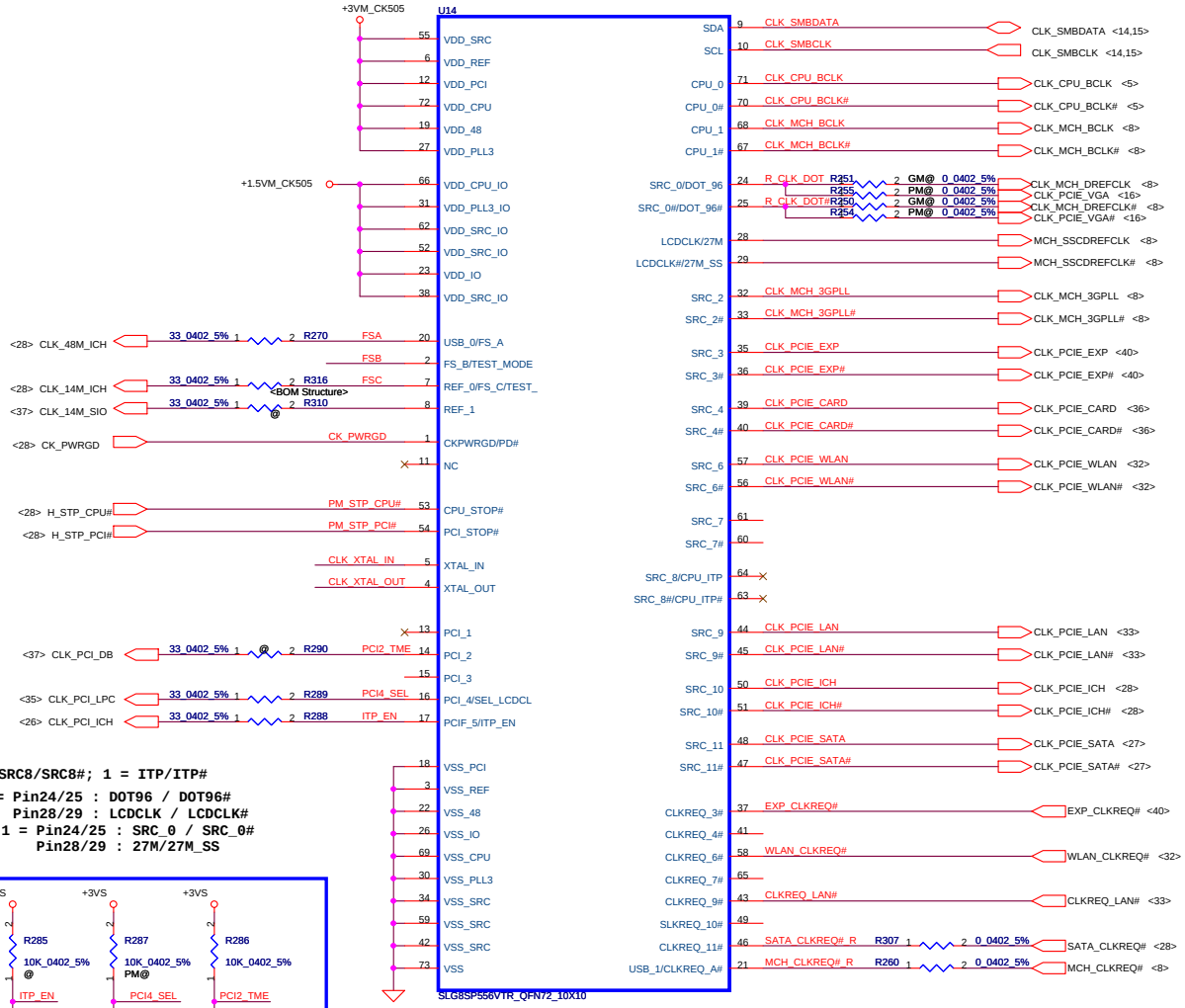


SA000020K00 (Silego : SLG8SP556VTR)

SA000020H00 (ICS : ICS9LPRS387AKLFT)

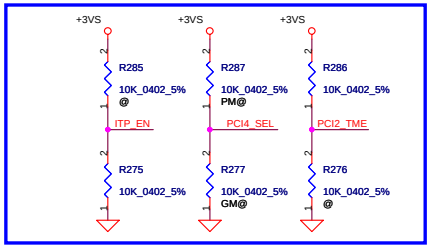


Routing the trace at least 10mil



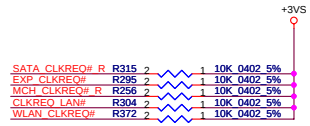
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Clock generator**

Size	Document Number	Rev
	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 22 of 53

09/13 change pull low enable

09/13 change pull high enable

9/14 Change from 4.7K to 2.2K base on Design Guide P.274

9/13 Add inverting lavel shift circuit base on Design Guide P.277

9/14 Reserve for VGA used;check pin name

TMDS pull down (500ohm) resistors G9x only

NEAR CONNECT

U8 PS8101TQFN48G_QFN48_7X7 HDMI_GM@

JHDMI1 TYCO_16-004-6131 ME@

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

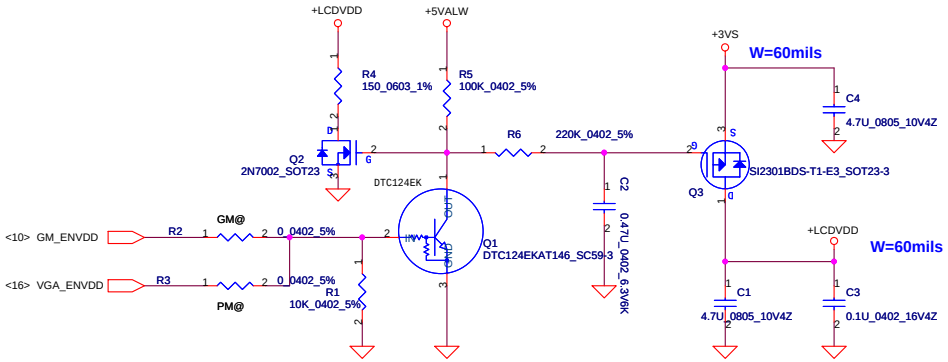
Compal Electronics, Inc.

Title: Level shifter-CH7318

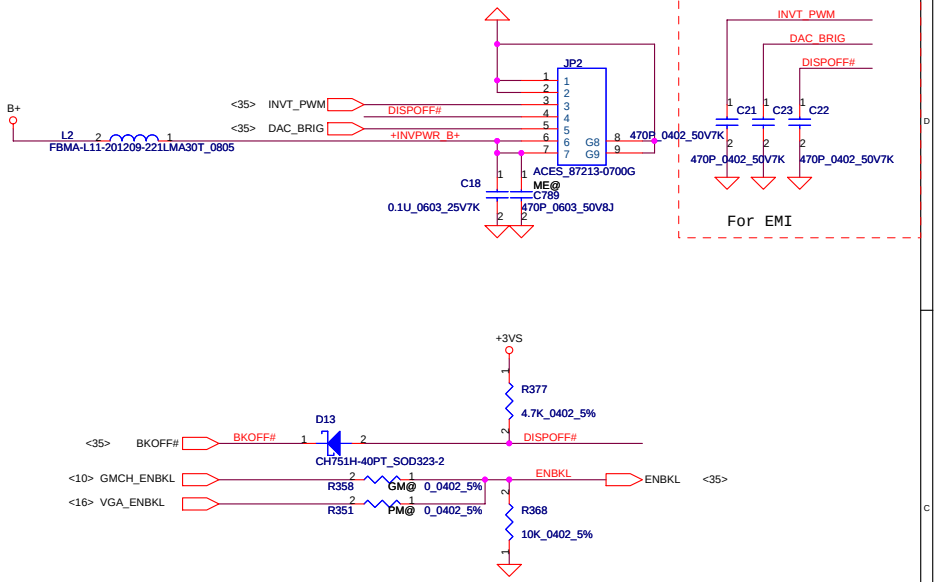
Size | Document Number: JIWA3/A4_LA-4212P | Rev: 1.0

Date: Thursday, May 22, 2008 | Sheet 23 of 53

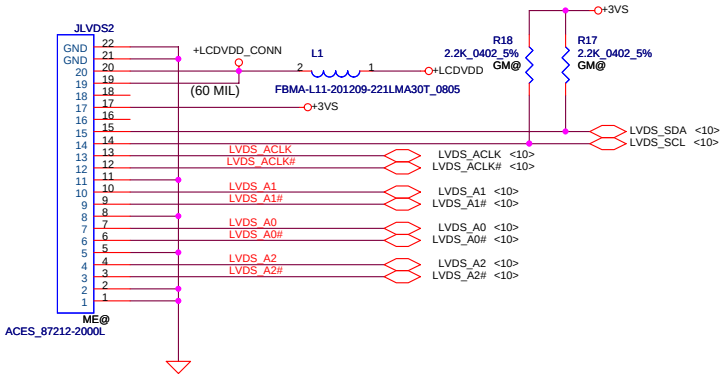
LCD POWER CIRCUIT



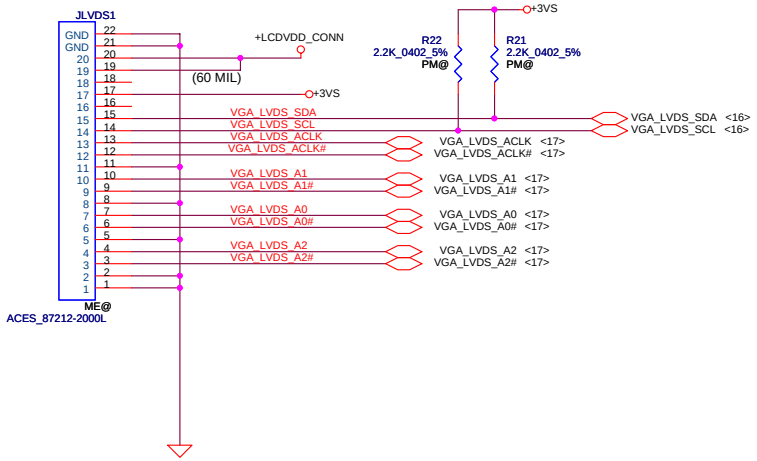
INVERTER Conn.



LCD/PANEL BD. Conn.



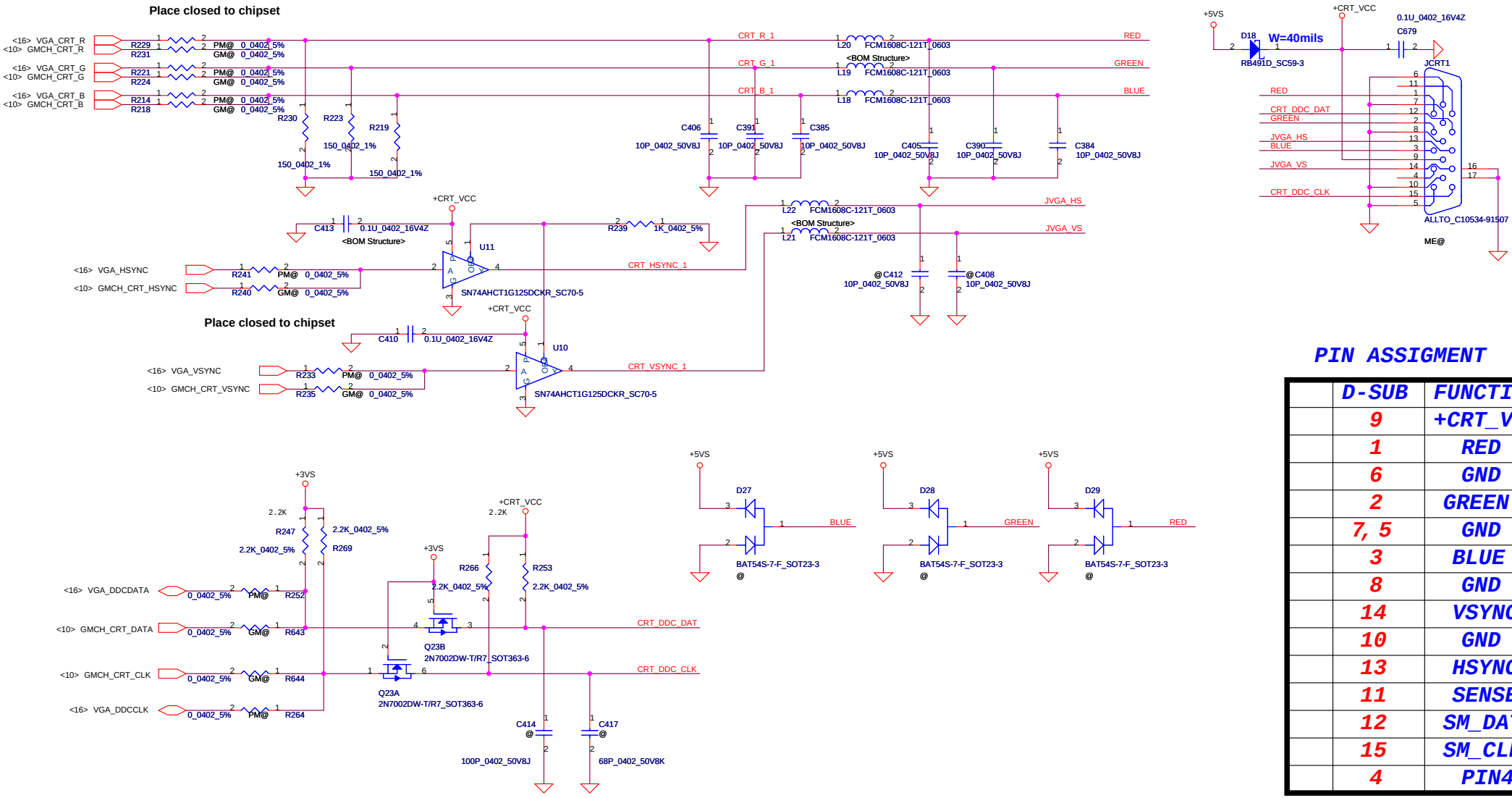
LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: LVDS & DVI Connector			
Size: B	Document Number: JIWA3/A4_LA4212P		Rev: 1.0
Date: Monday, May 12, 2008	Sheet 24 of 53		

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

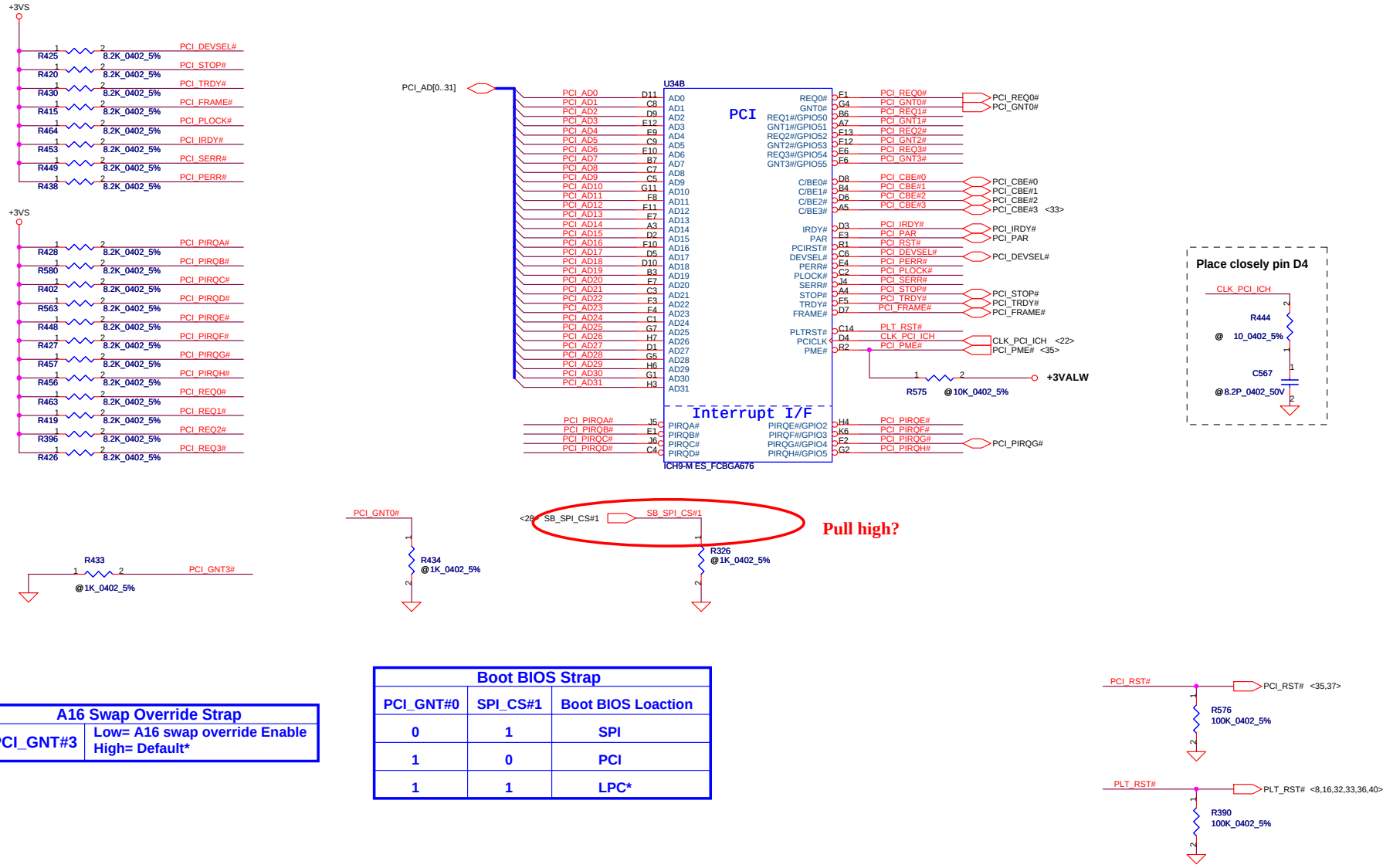
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **CRT & TV-OUT Connector**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 25 of 53



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

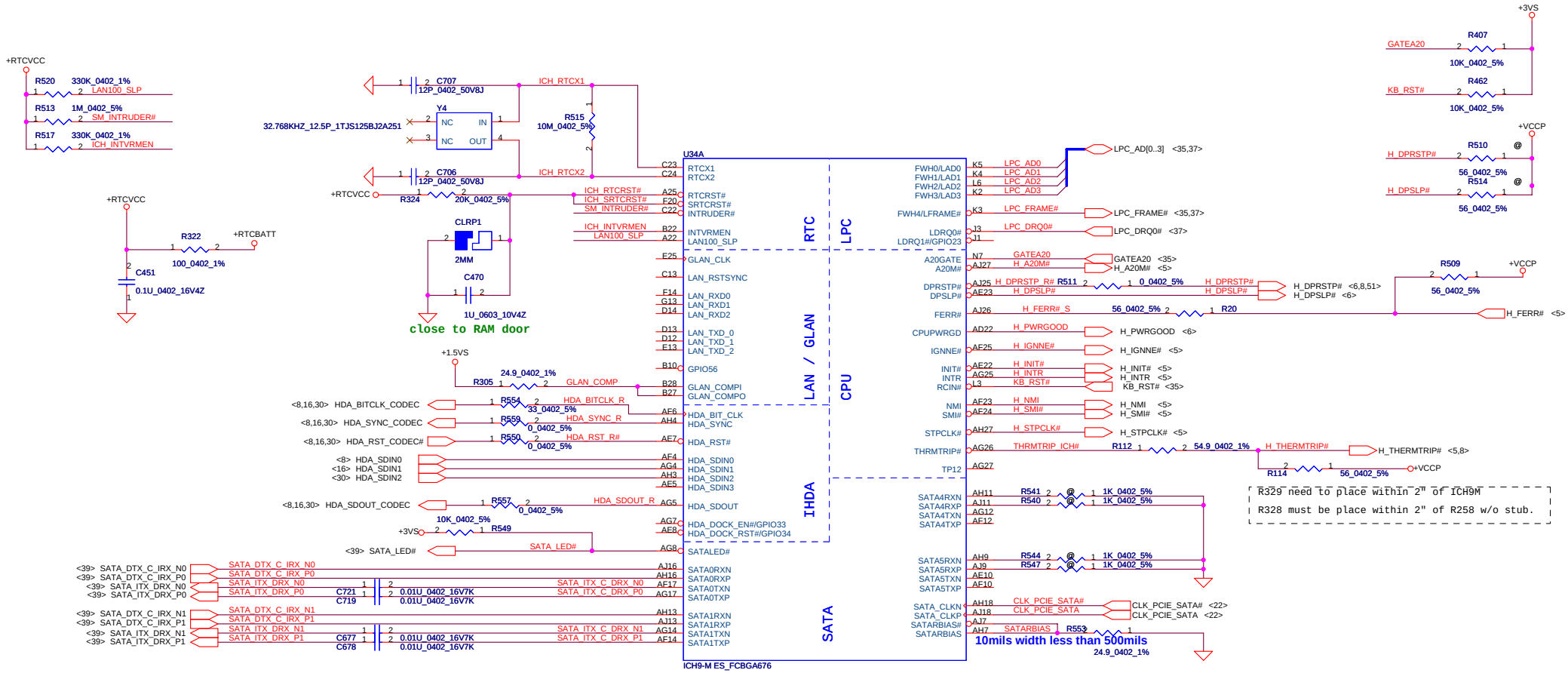
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size | Document Number: JIWA3/A4_LA4212P | Rev: 1.0

Date: Wednesday, May 14, 2008 | Sheet 26 of 53



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

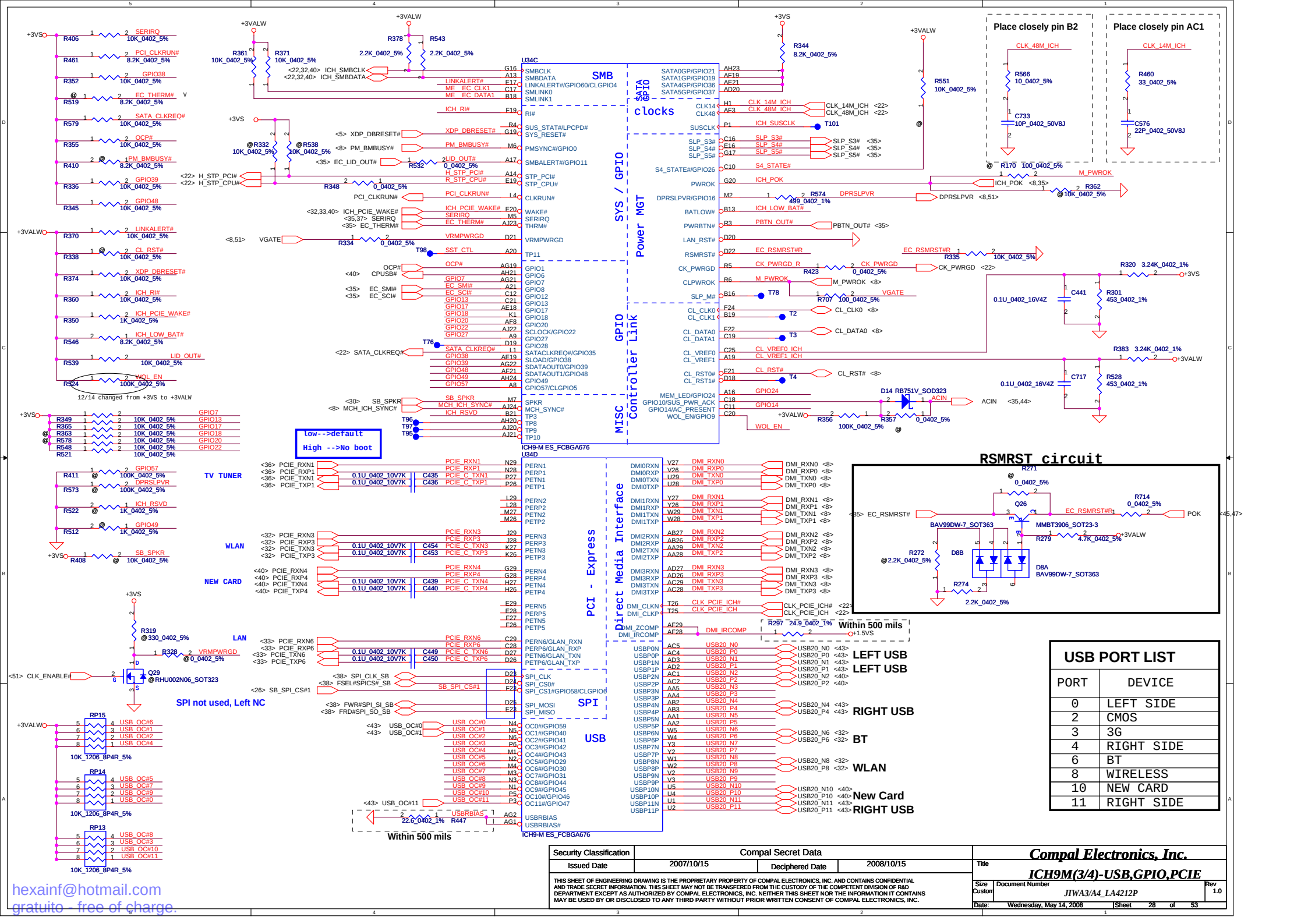
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 Sheet 27 of 53

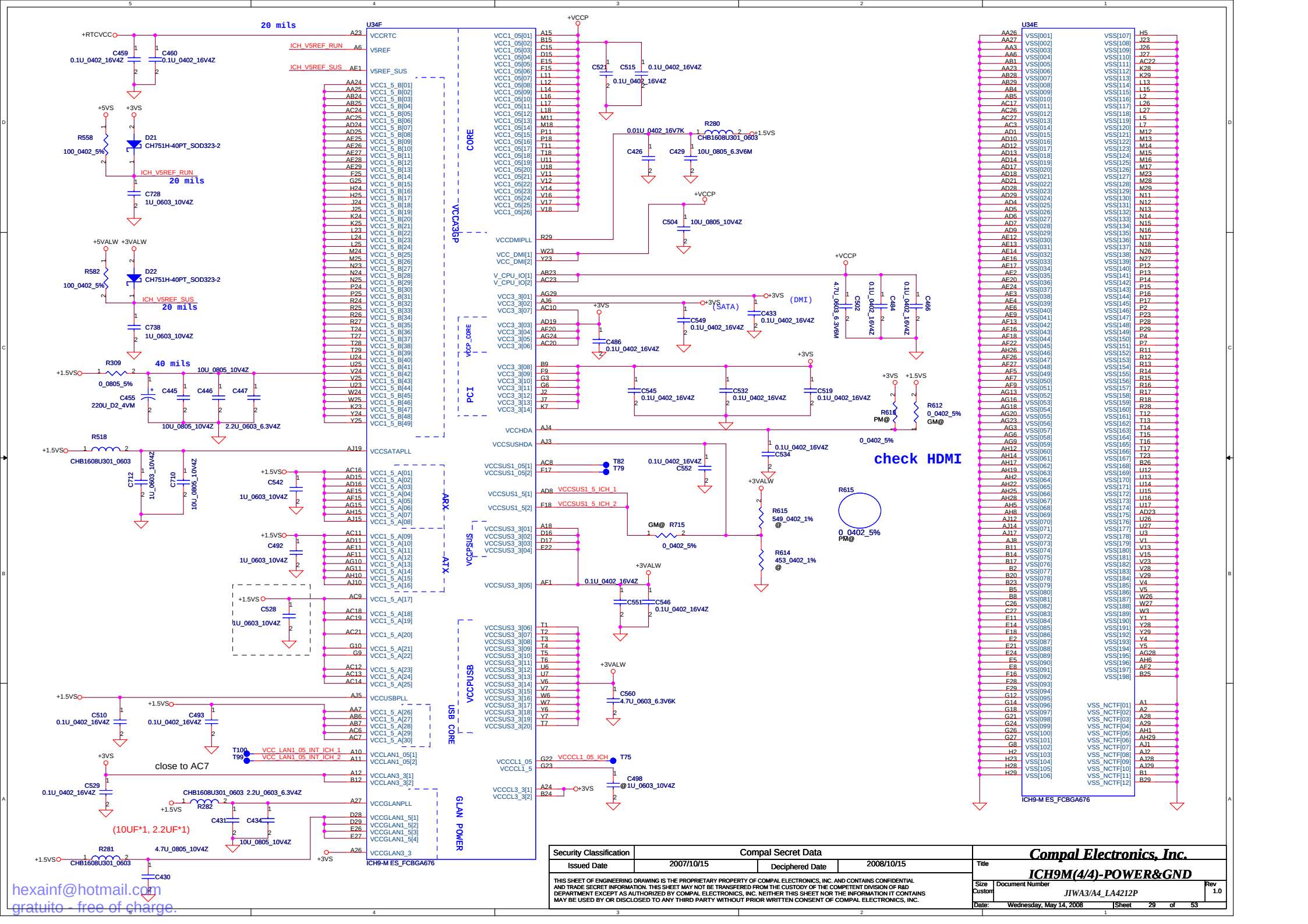


USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
2	CMOS
3	3G
4	RIGHT SIDE
6	BT
8	WIRELESS
10	NEW CARD
11	RIGHT SIDE

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	ICH9M(3/4)-USB,GPIO,PCIE		
Size: Custom	Document Number: JIWA3/A4_LA4212P		Rev: 1.0
Date: Wednesday, May 14, 2008	Sheet 28 of 53		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	ICH9M(4/4)-POWER&GND		
Size: Custom	Document Number: JIWA3/A4_LA4212P		Rev: 1.0
Date: Wednesday, May 14, 2008	Sheet 29 of 53		

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CODEC POWER

(3.33V)
250mW

W=40Mil @

2.2kohm for MICL + MICR
4.7kohm for MICL or MICR

U21 APE8805A-33Y5P_SOT23-5

CX20548 AMOM DAA

PC_BEEP dB control

external MIC

Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

0216_Change value.

U15 CX20561-12Z_LQFP48_7X7

DIGITAL ANALOG

GND GNDA

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate.

CX20548 AMOM DAA

JRJ11 FOX_JM74613-P2002-7F

ME@

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

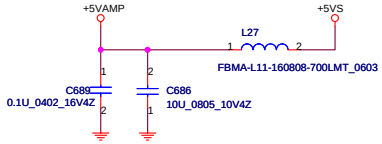
Title: CX20561-AMOM Codec

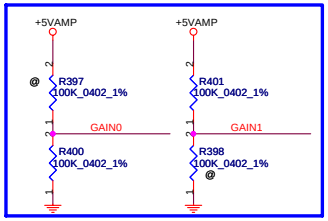
Size: Custom | Document Number: JIWA3/A4_LA4212P | Rev: 1.0

Date: Monday, May 12, 2008 | Sheet 30 of 53

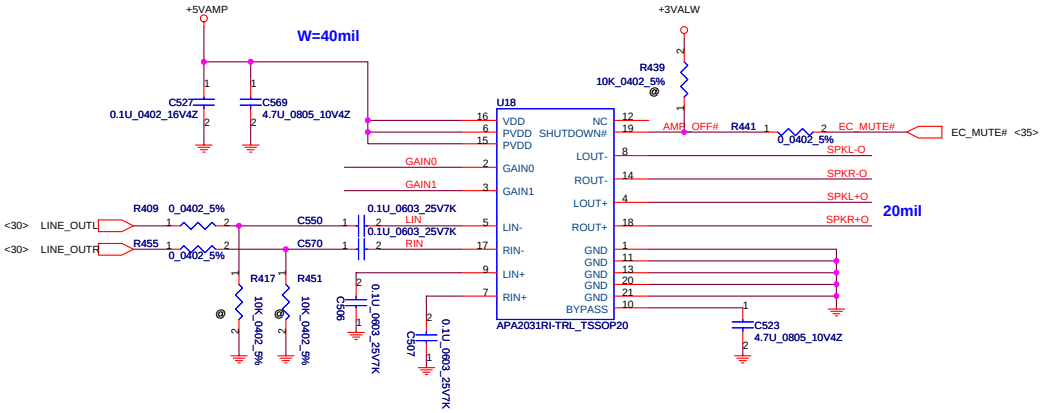
Speaker Amplifier

1nd = APA2031 (SA00001RZ00)
2nd = G1431F2U (SA000012Y00)

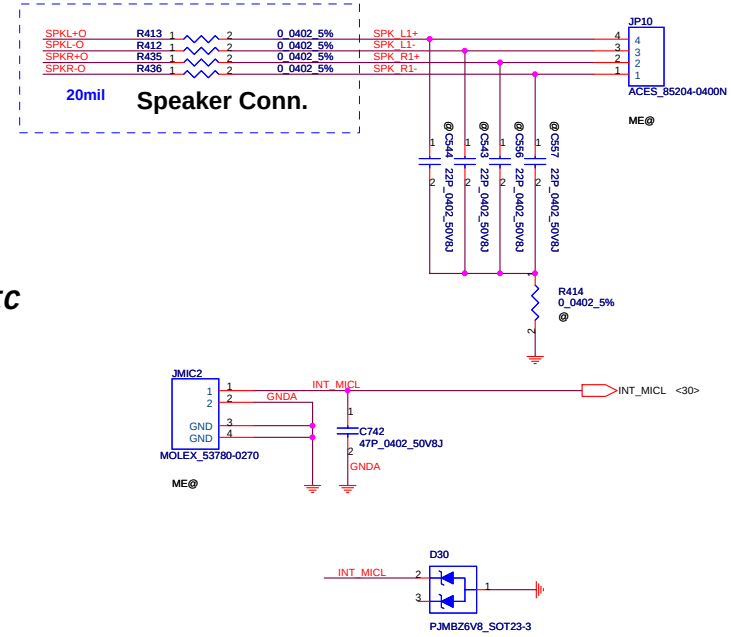




GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



INT MIC



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

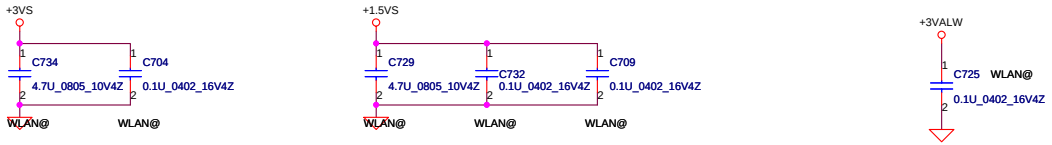
Compal Electronics, Inc.

Title: **AMP/VR/Audio Jack/MIC**

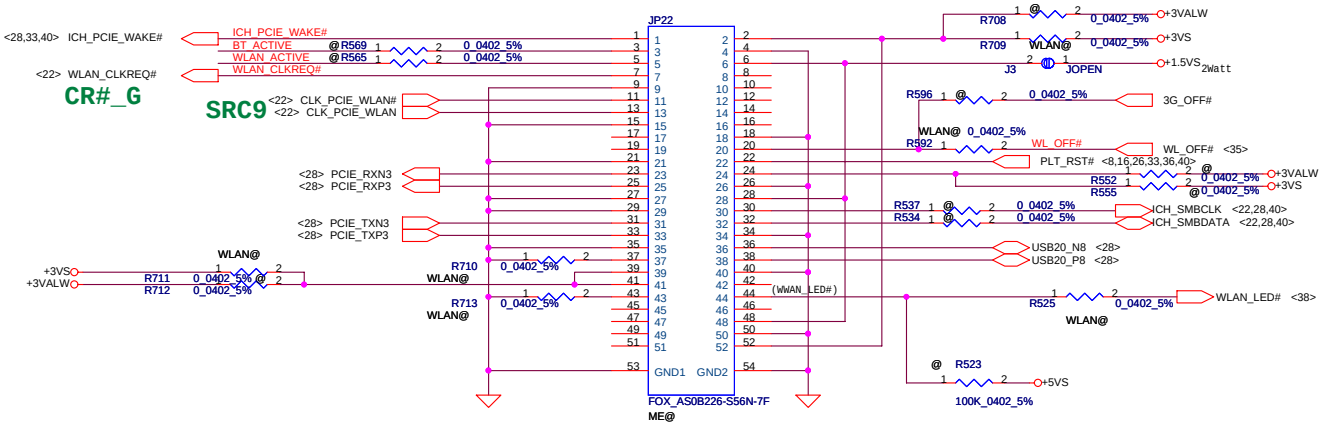
Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 31 of 53

Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN

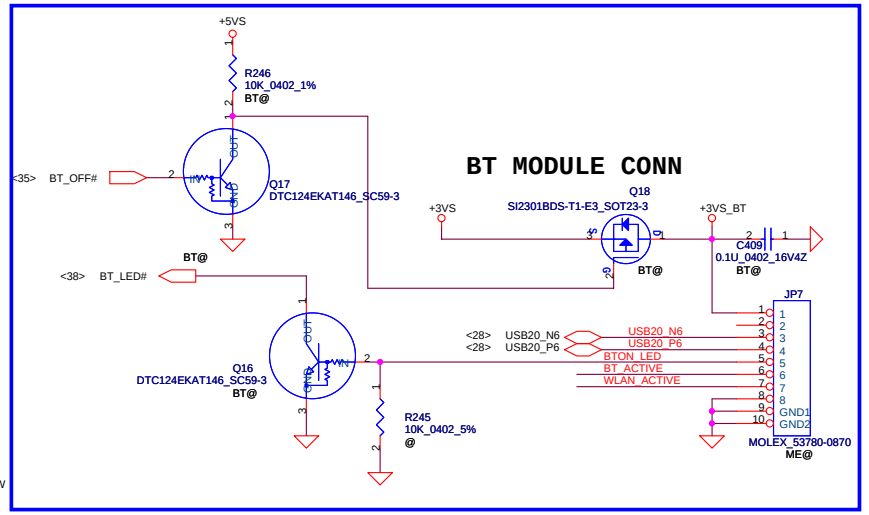


Mini-Express Card(Slot 1-WLAN)



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Mini-Card/3G/FeliCa/BT			
Size	Document Number: JIWA3/A4_LA4212P		Rev: 1.0
Date: Tuesday, May 20, 2008	Sheet 32 of 53		

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : Filter place as close chip as possible.

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

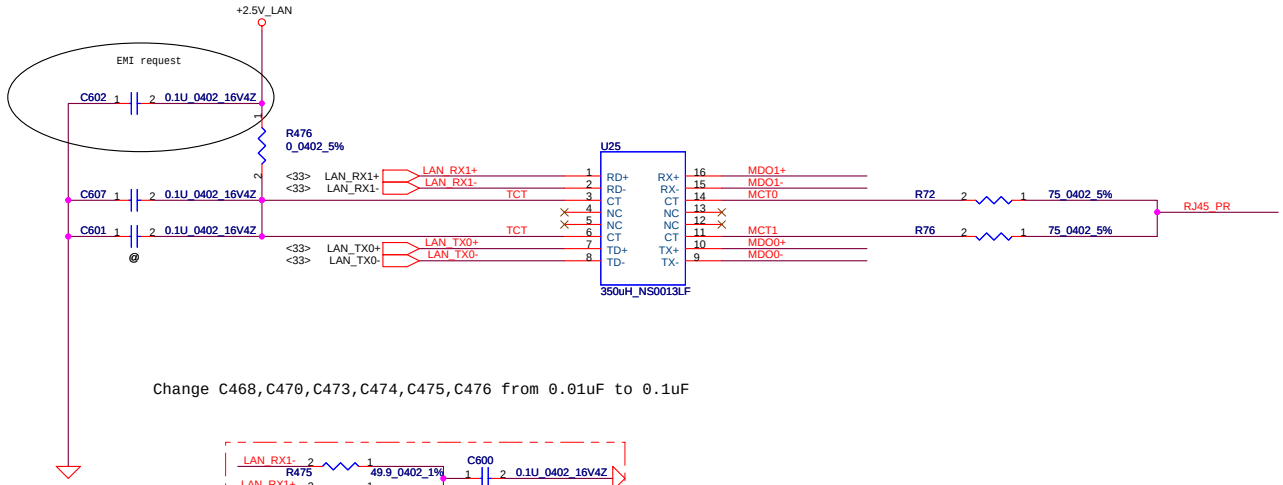
Compal Electronics, Inc.

Title: BCM5787MKML

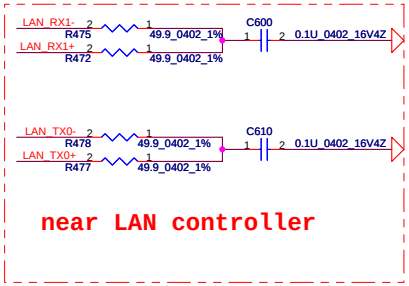
Size: Custom | Document Number: JIWA3/A4_LA4212P | Rev: 1.0

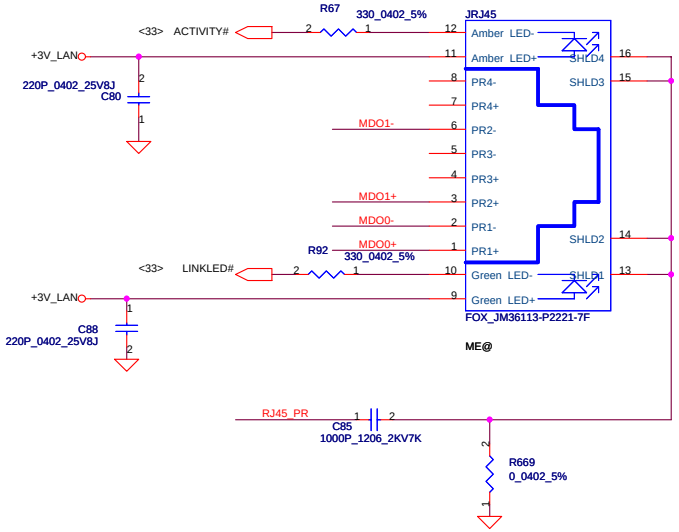
Date: Monday, May 12, 2008 | Sheet 33 of 53

RJ45 CONN



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF





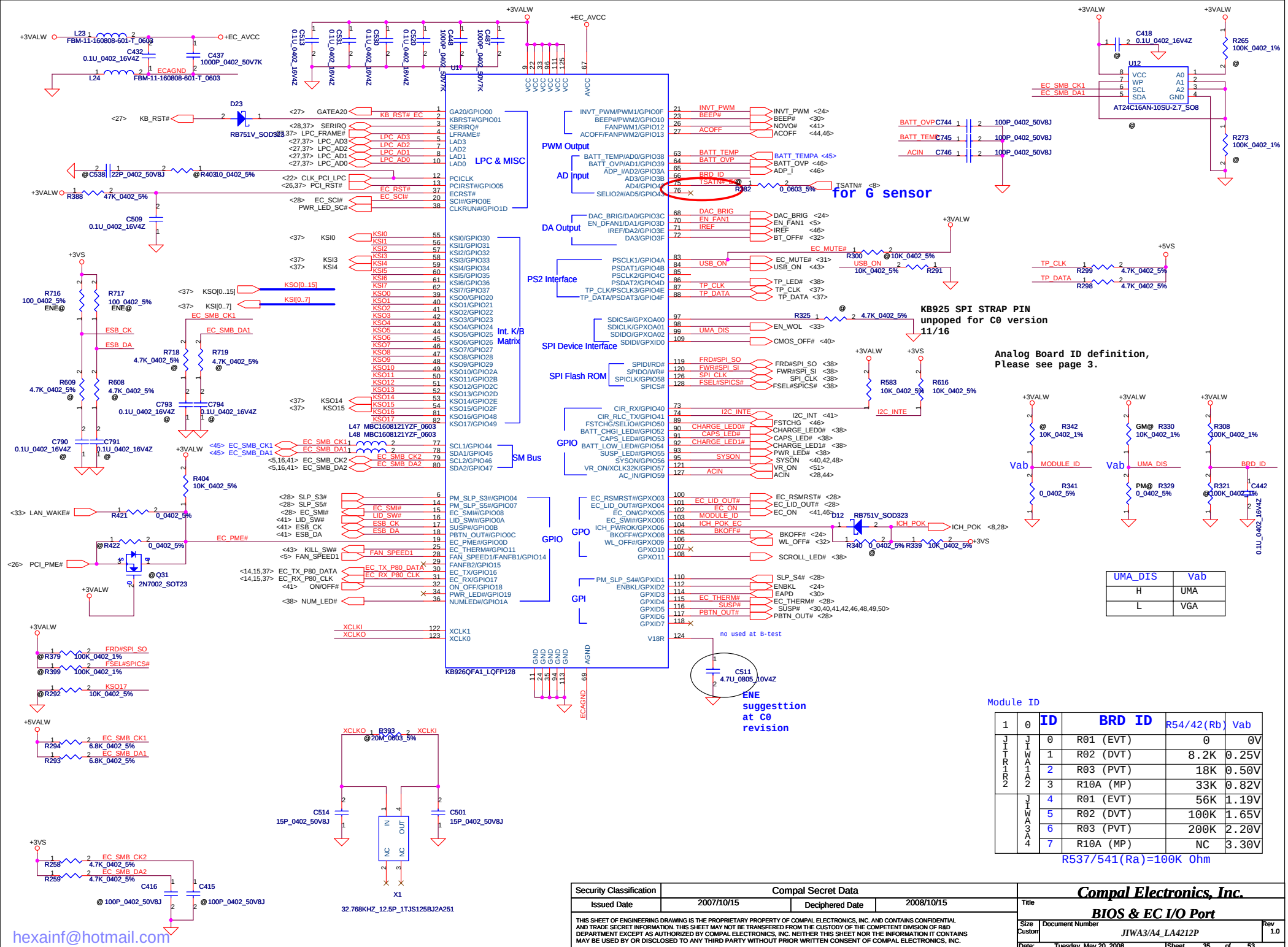
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LAN CONTROLLER**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 34 of 53



UMA_DIS	Vab
H	UMA
L	VGA

Module ID

		ID	BRD ID	R54/42(Rb)	Vab
1	0				
JITR12	JIWA1A2	0	R01 (EVT)	0	0V
		1	R02 (DVT)	8.2K	0.25V
		2	R03 (PVT)	18K	0.50V
		3	R10A (MP)	33K	0.82V
	JIWA3A4	4	R01 (EVT)	56K	1.19V
		5	R02 (DVT)	100K	1.65V
		6	R03 (PVT)	200K	2.20V
		7	R10A (MP)	NC	3.30V

R537/541(Ra)=100K Ohm

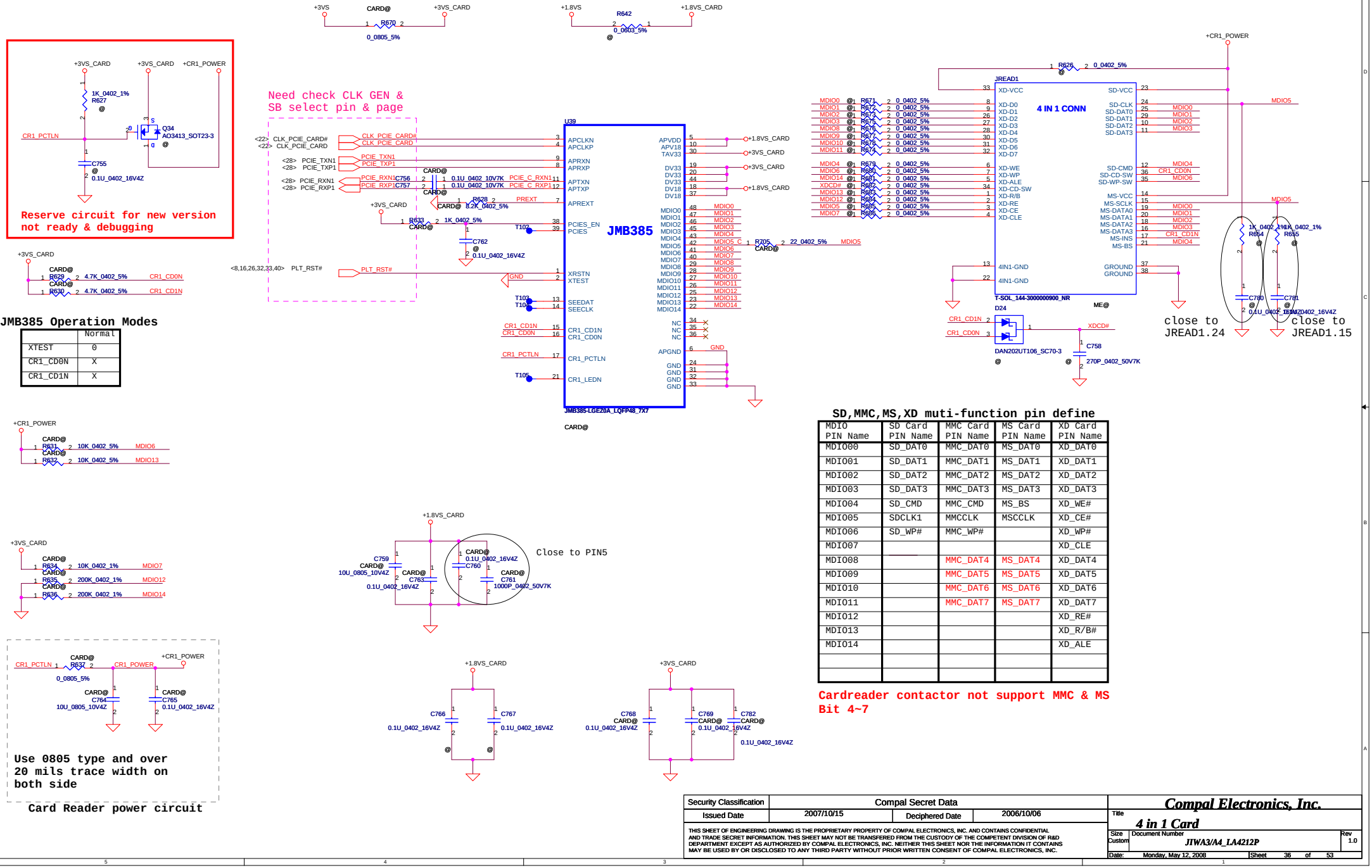
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Tuesday, May 20, 2008 | Sheet 35 of 53



JMB385 Operation Modes

	Normal
XTEST	0
CR1_CD0N	X
CR1_CD1N	X

SD,MMC,MS,XD muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

Cardreader contactor not support MMC & MS Bit 4~7

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2006/10/06

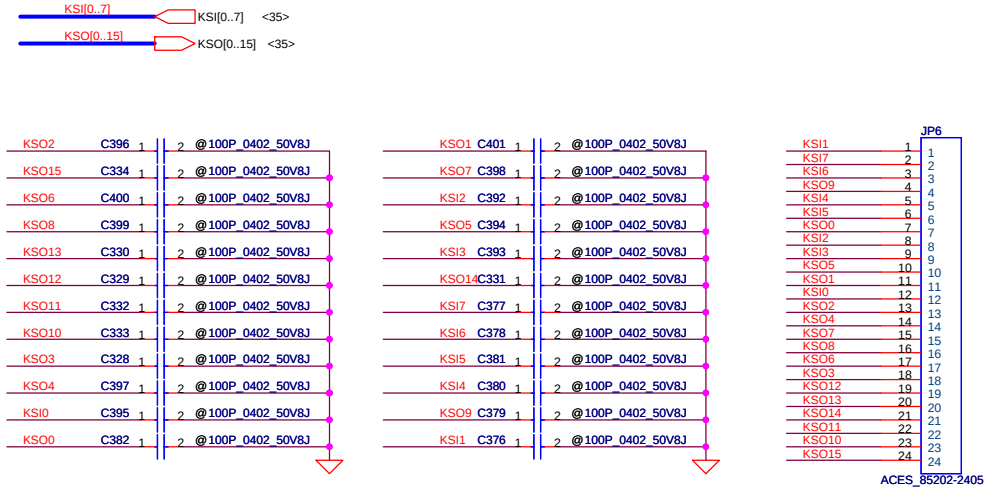
Compal Electronics, Inc.

Title: 4 in 1 Card

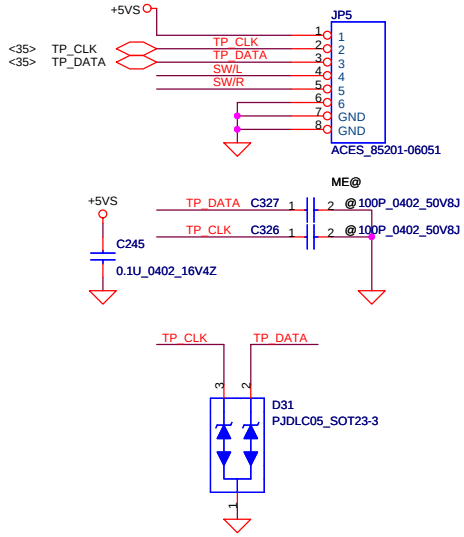
Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 36 of 53

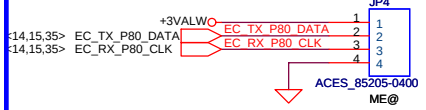
INT_KBD Conn.

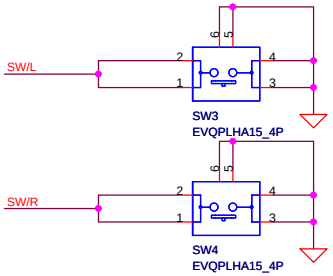


To TP/B Conn.

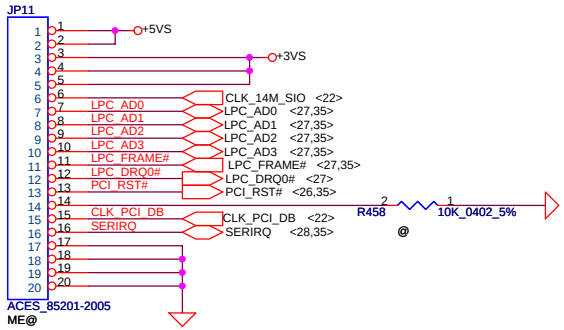


EC DEBUG PORT





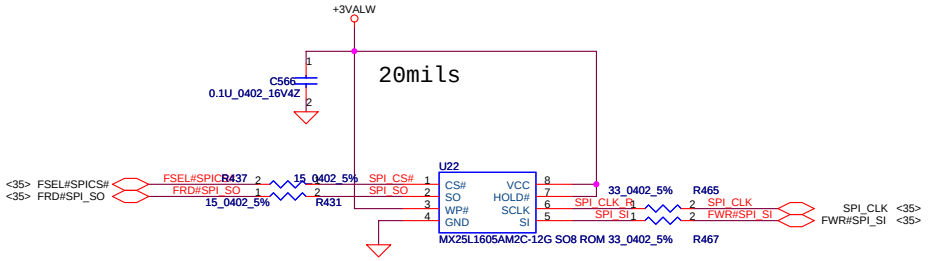
FOR LPC SIO DEBUG PORT

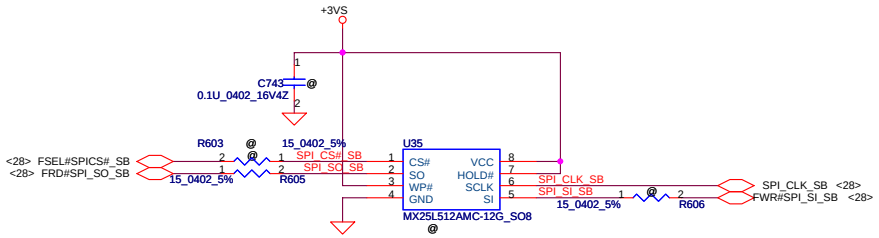


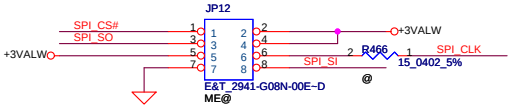
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

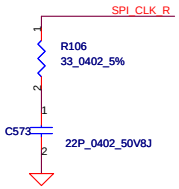
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: JIWA3/A4_LA4212P		Rev: 1.0
Date: Monday, May 12, 2008	Sheet 37 of 53		

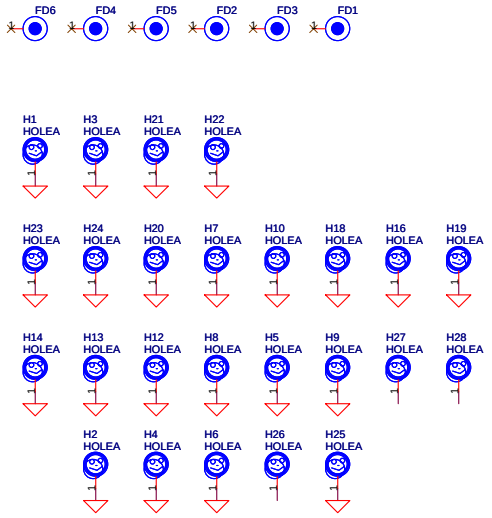
FOR EC 8M SPI ROM



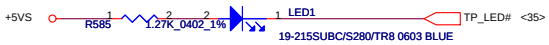


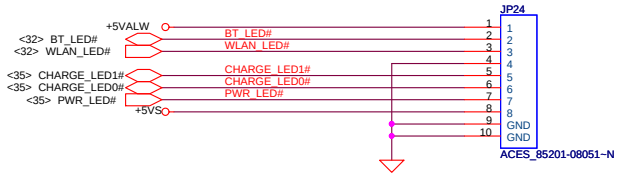


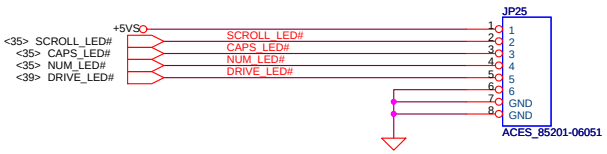




LED







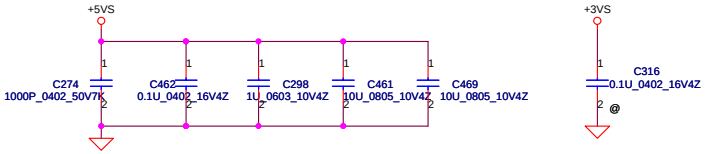
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

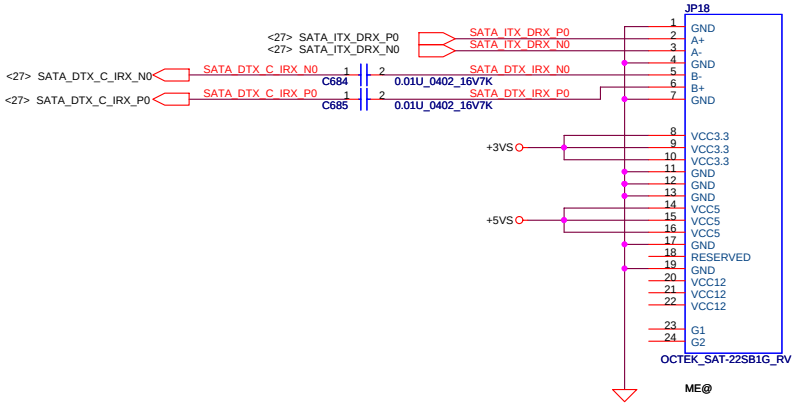
Title: **LED/EC SPI ROM**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

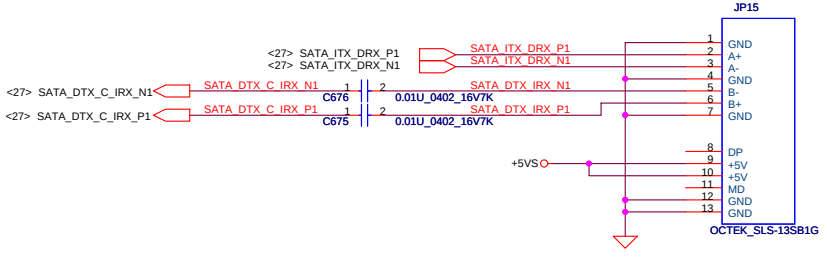
Date: Wednesday, May 14, 2008 | Sheet 38 of 53

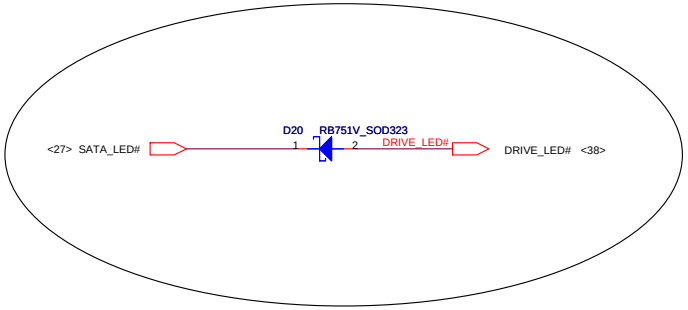


SATA HDD Conn.



SATA ODD Conn.





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

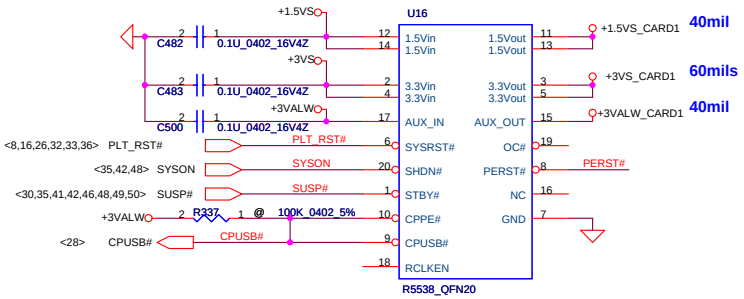
Compal Electronics, Inc.

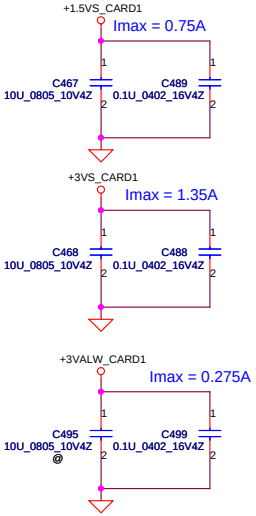
Title: **HDD & ODD Connector**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

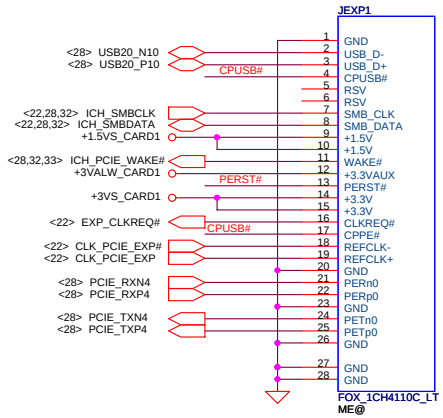
Date: Monday, May 12, 2008 | Sheet 39 of 53

Express Card Power Switch



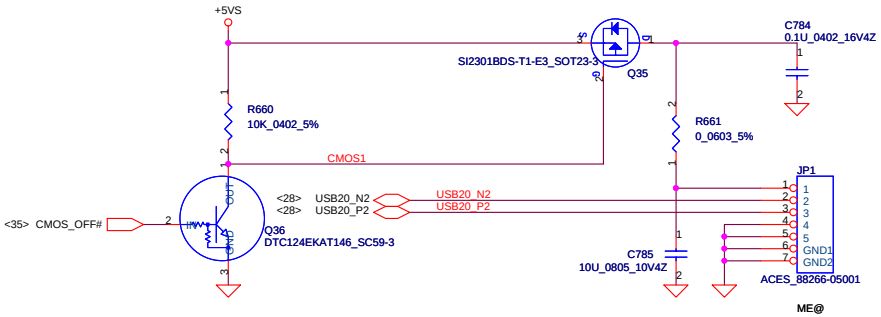


New Card Socket (Left/TOP)



(NEW)

CMOS Camera Conn



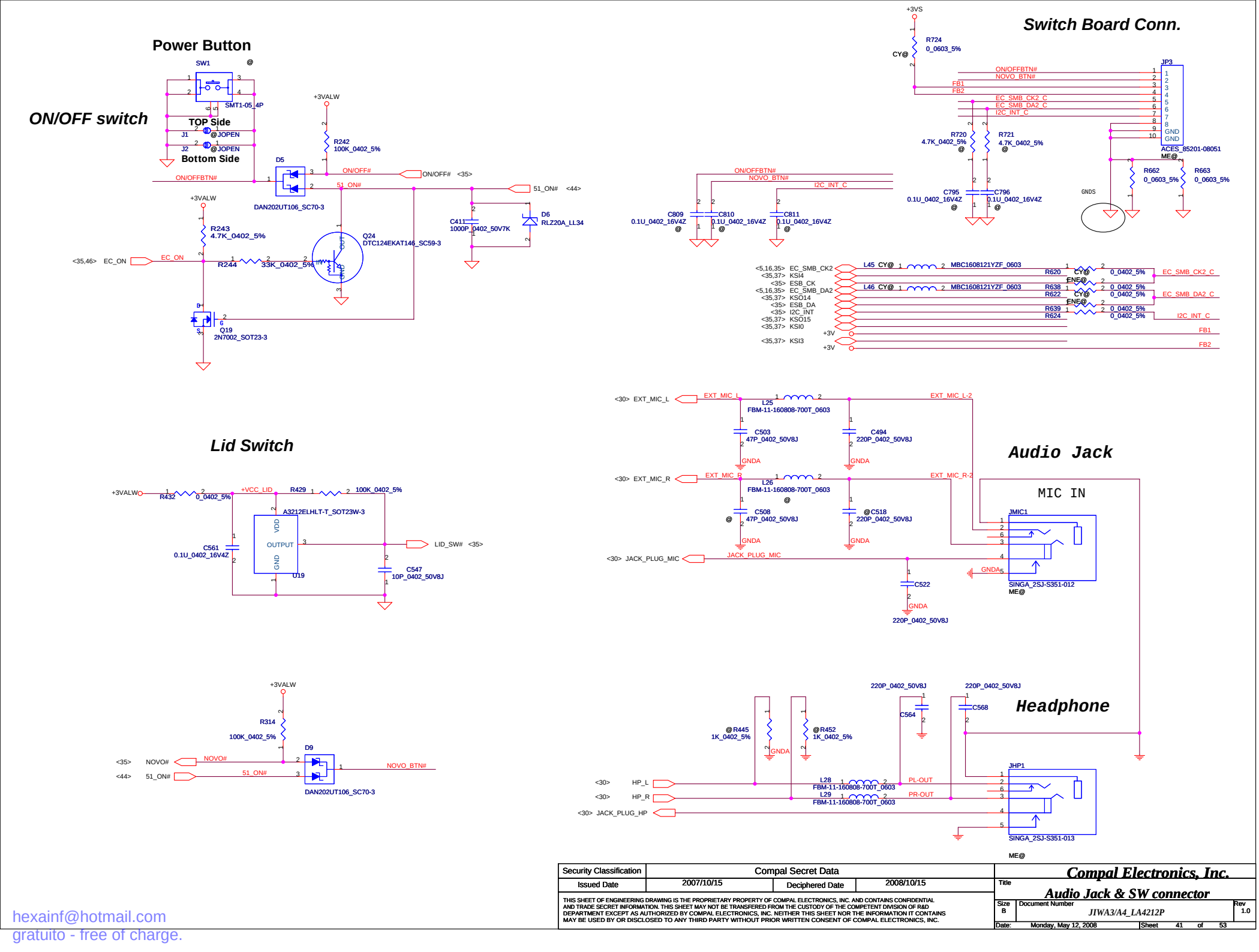
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **NEW CARD & CMOS Connector**

Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 40 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

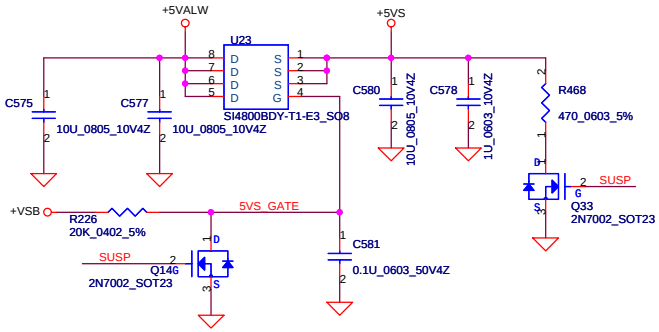
Compal Electronics, Inc.

Title: **Audio Jack & SW connector**

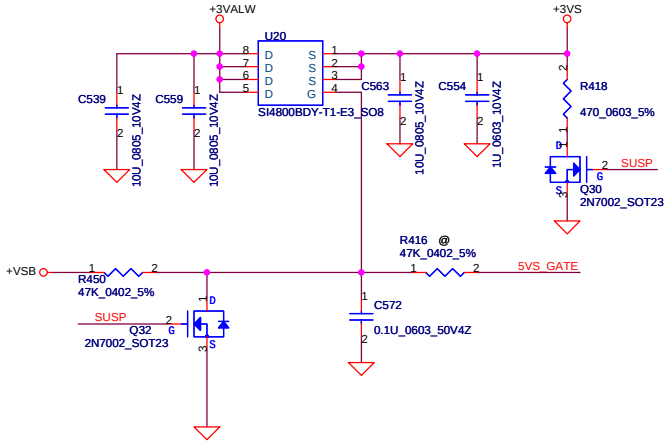
Size	Document Number	Rev
B	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 Sheet 41 of 53

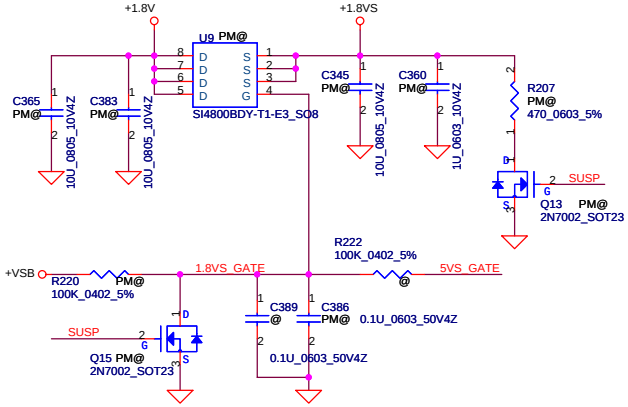
+5VALW TO +5VS

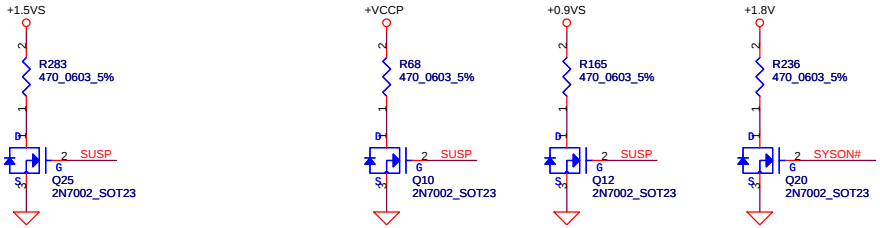


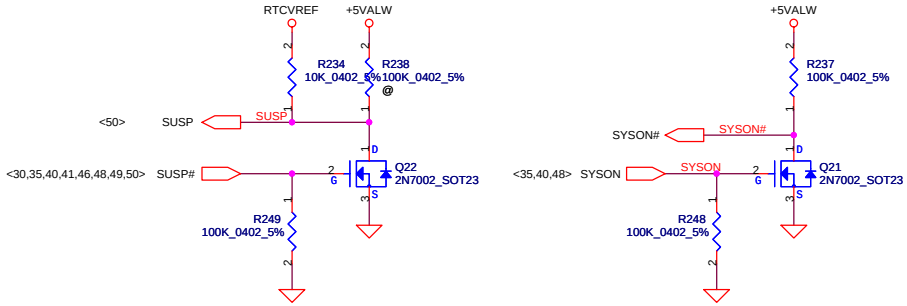
+3VALW TO +3VS

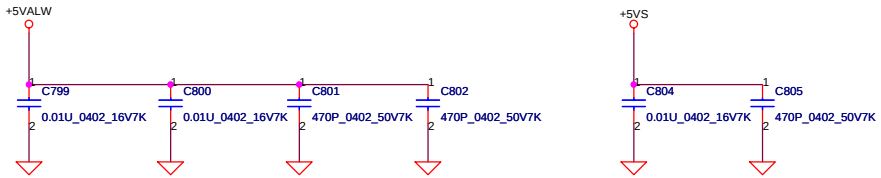


+1.8V to +1.8VS









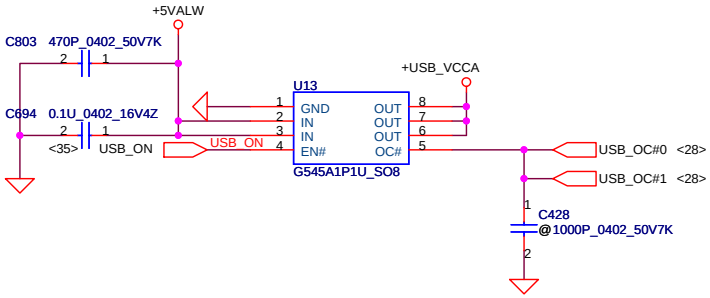
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2007/8/18

Compal Electronics, Inc.

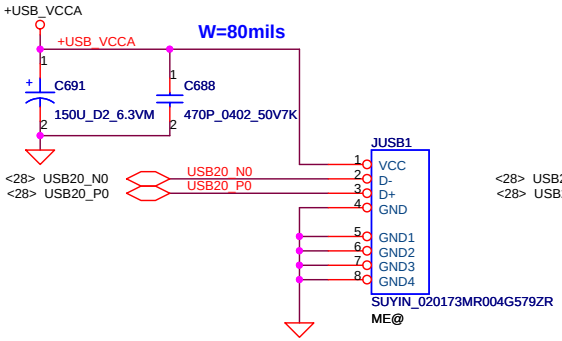
Title: DC Interface

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

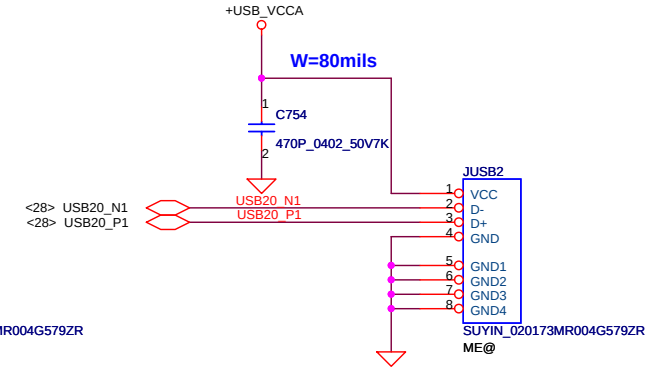
Date: Monday, May 12, 2008 Sheet 42 of 53



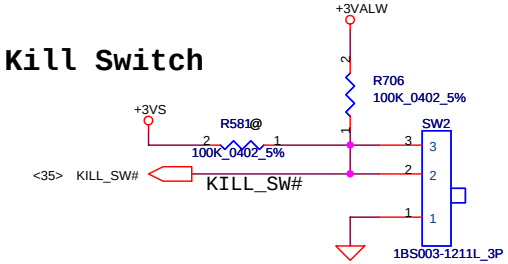
LIFT USB CONN. 1

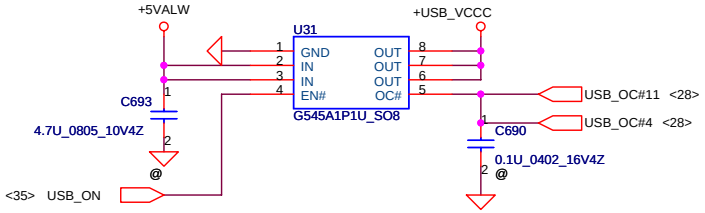


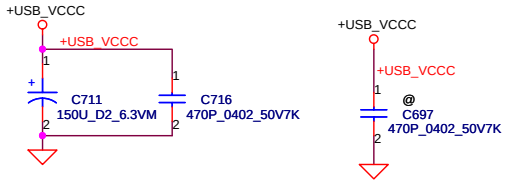
LIFT USB CONN. 2



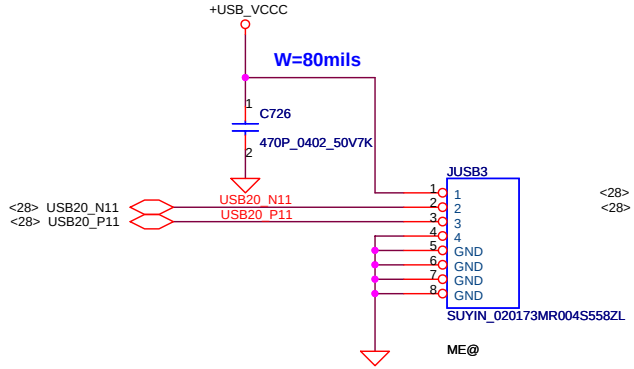
Kill Switch



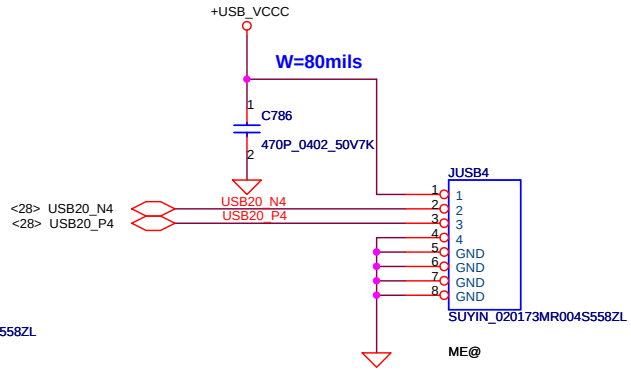




RIGHT USB CONN. 3



RIGHT USB CONN.4



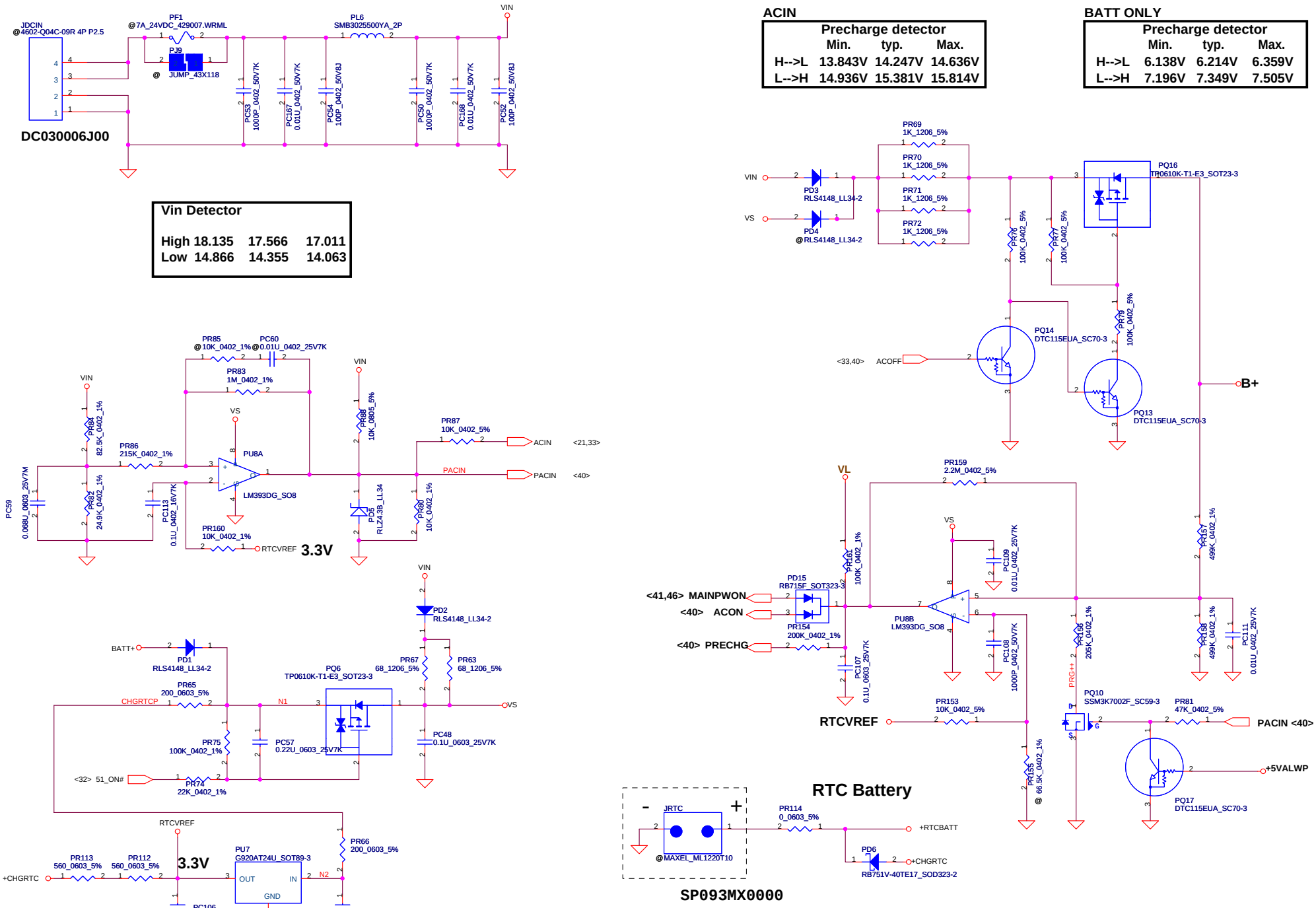
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
Custom	JIWA3/A4_LA4212P	1.0

Date: Wednesday, May 14, 2008 Sheet 43 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

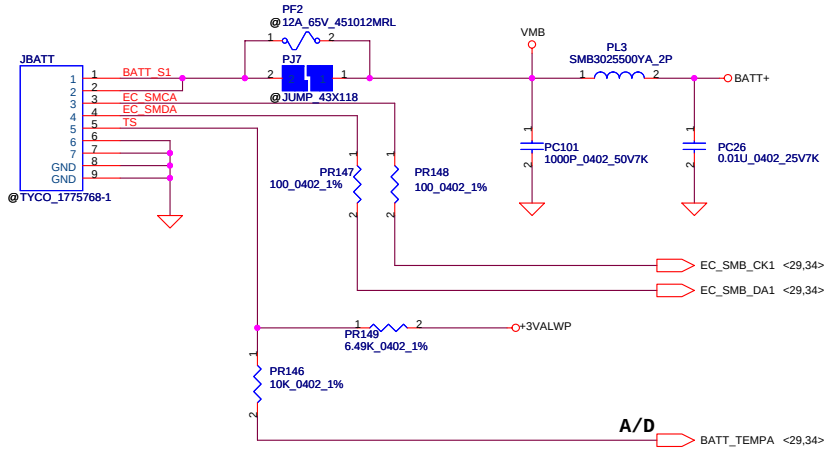
Compal Electronics, Inc.

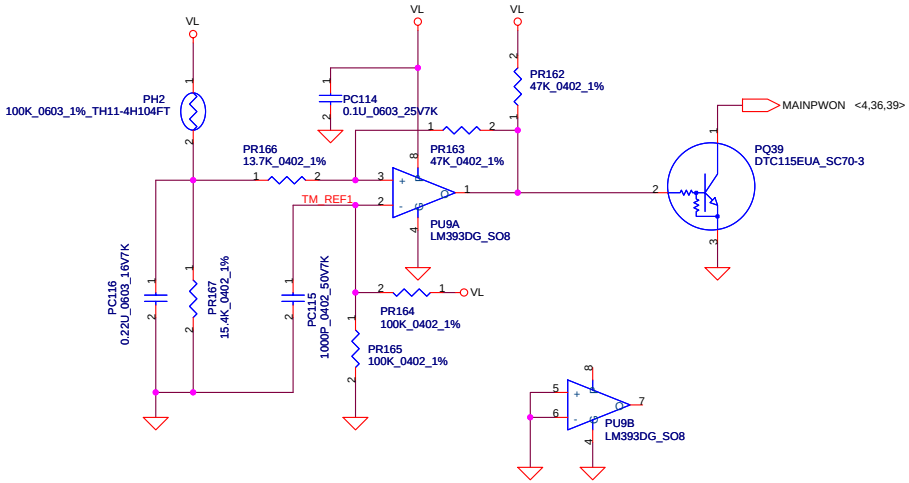
Title: DCIN & DETECTOR

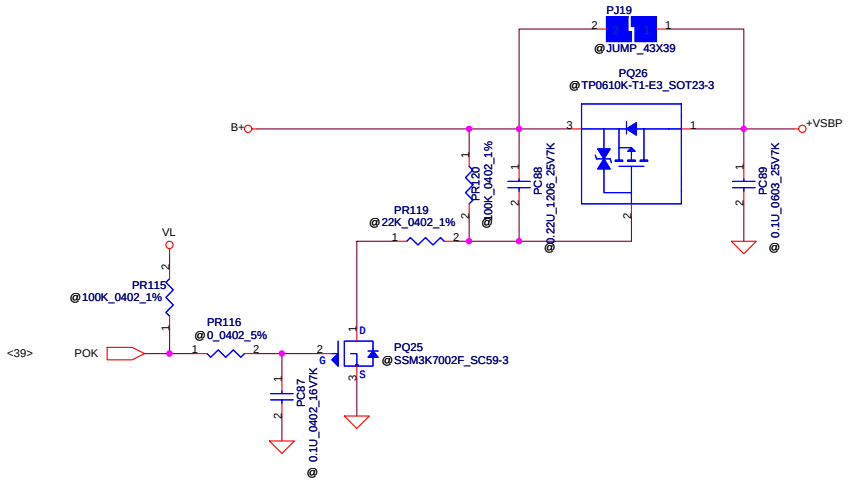
Size | Document Number | Rev 1.0

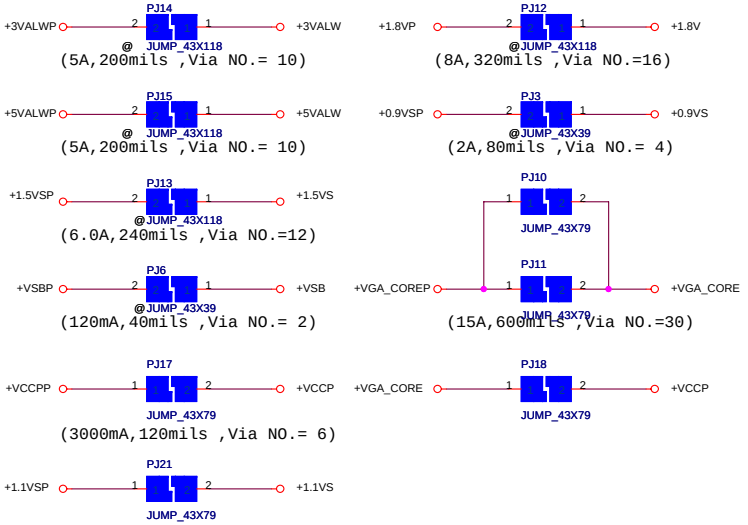
Date: Monday, May 12, 2008 | Sheet 44 of 53

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C









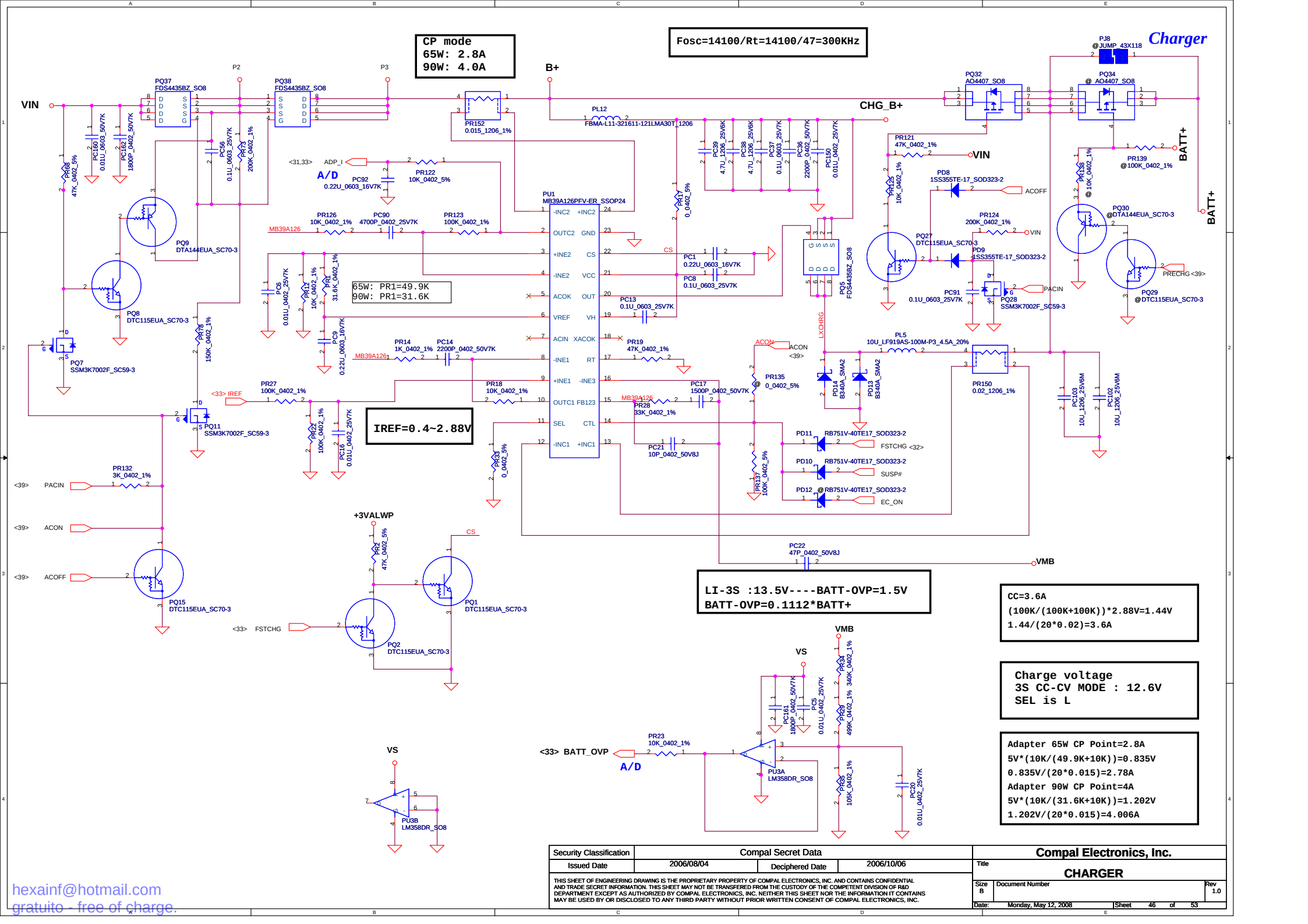
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		1.0

Date: Monday, May 12, 2008 | Sheet 45 of 53



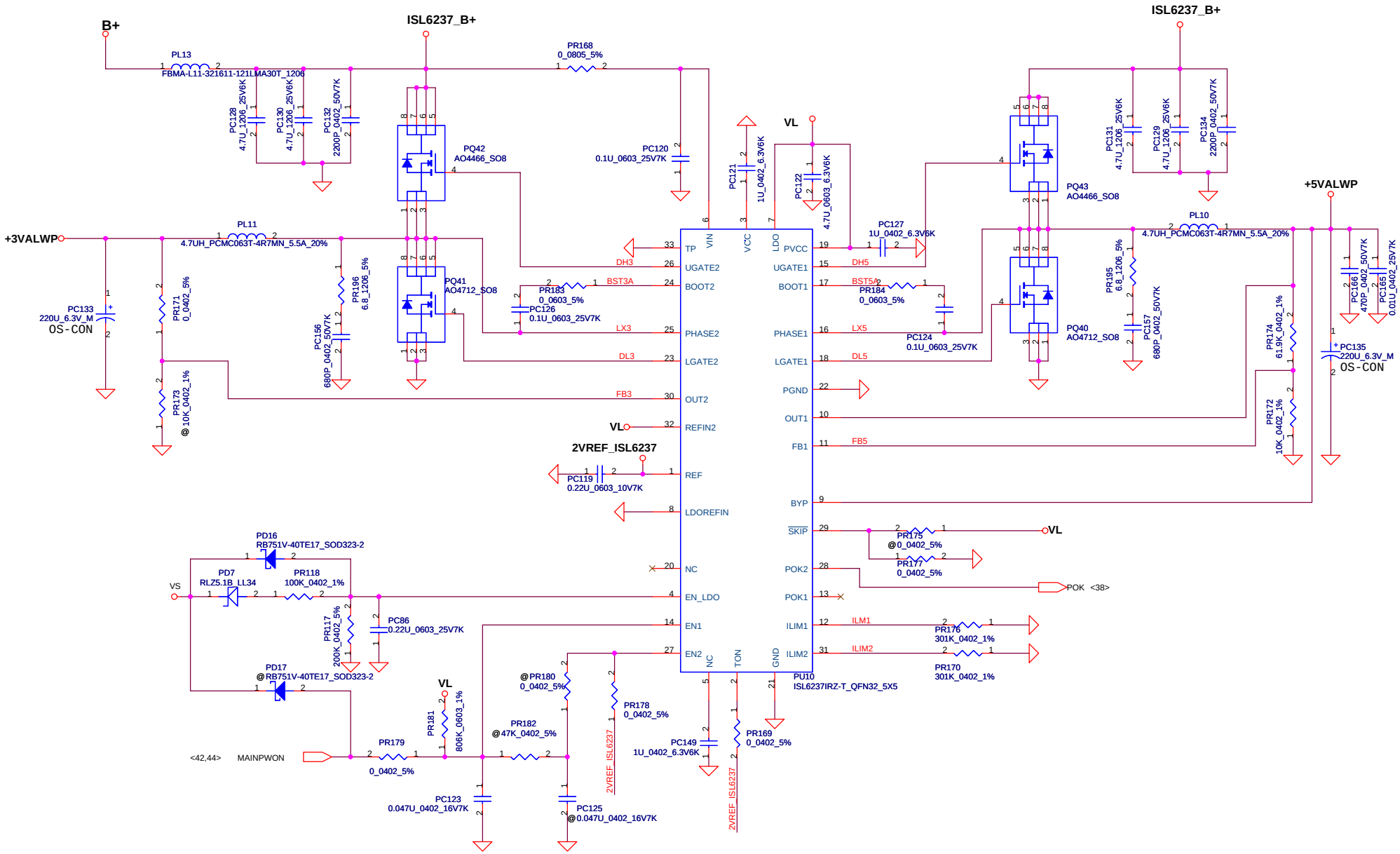
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
B		1.0

Date: Monday, May 12, 2008 Sheet 46 of 53



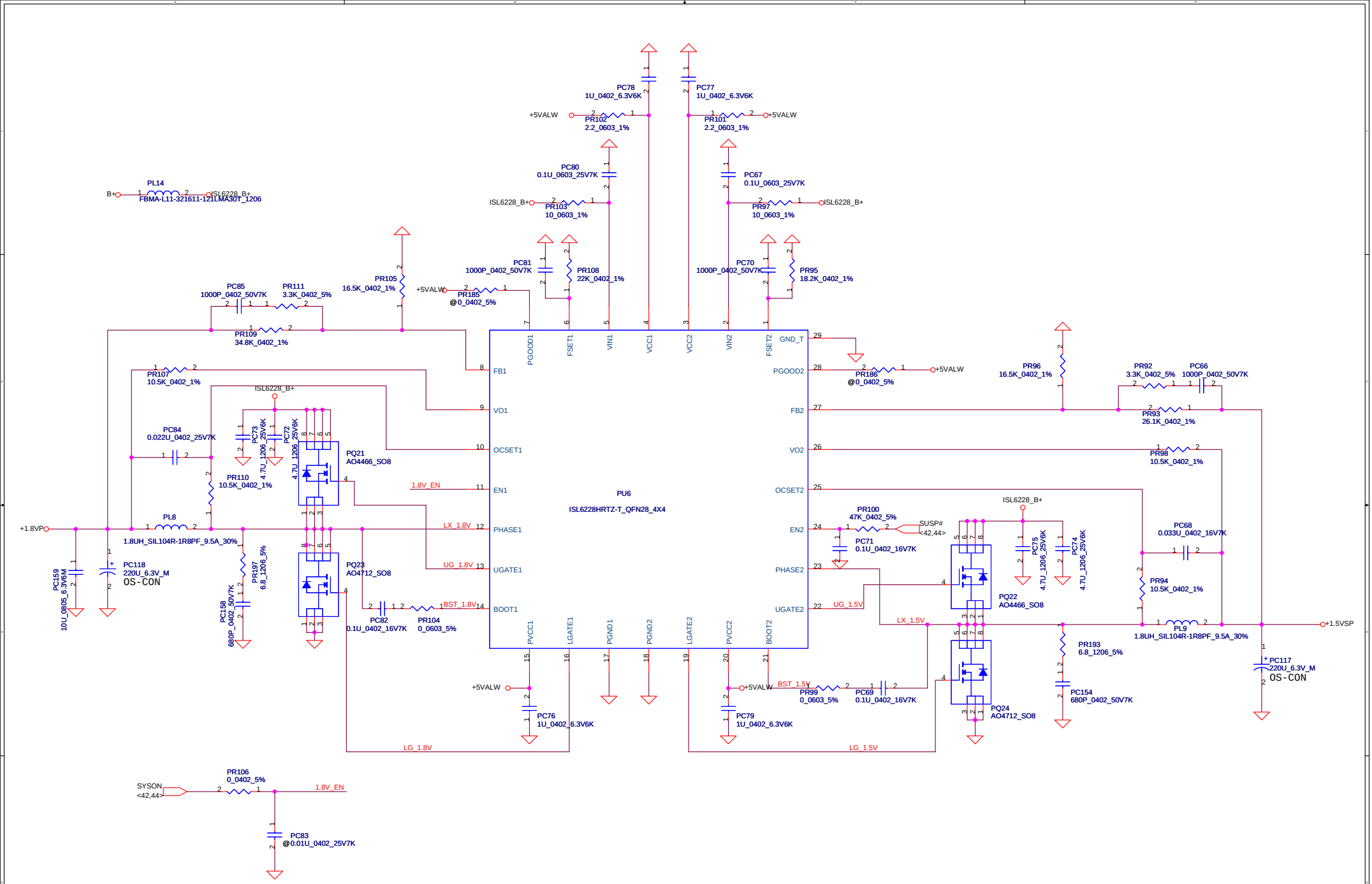
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: **+5V/+3V**

Size: Custom | Document Number | Rev: 1.0

Date: Monday, May 12, 2008 | Sheet 47 of 53



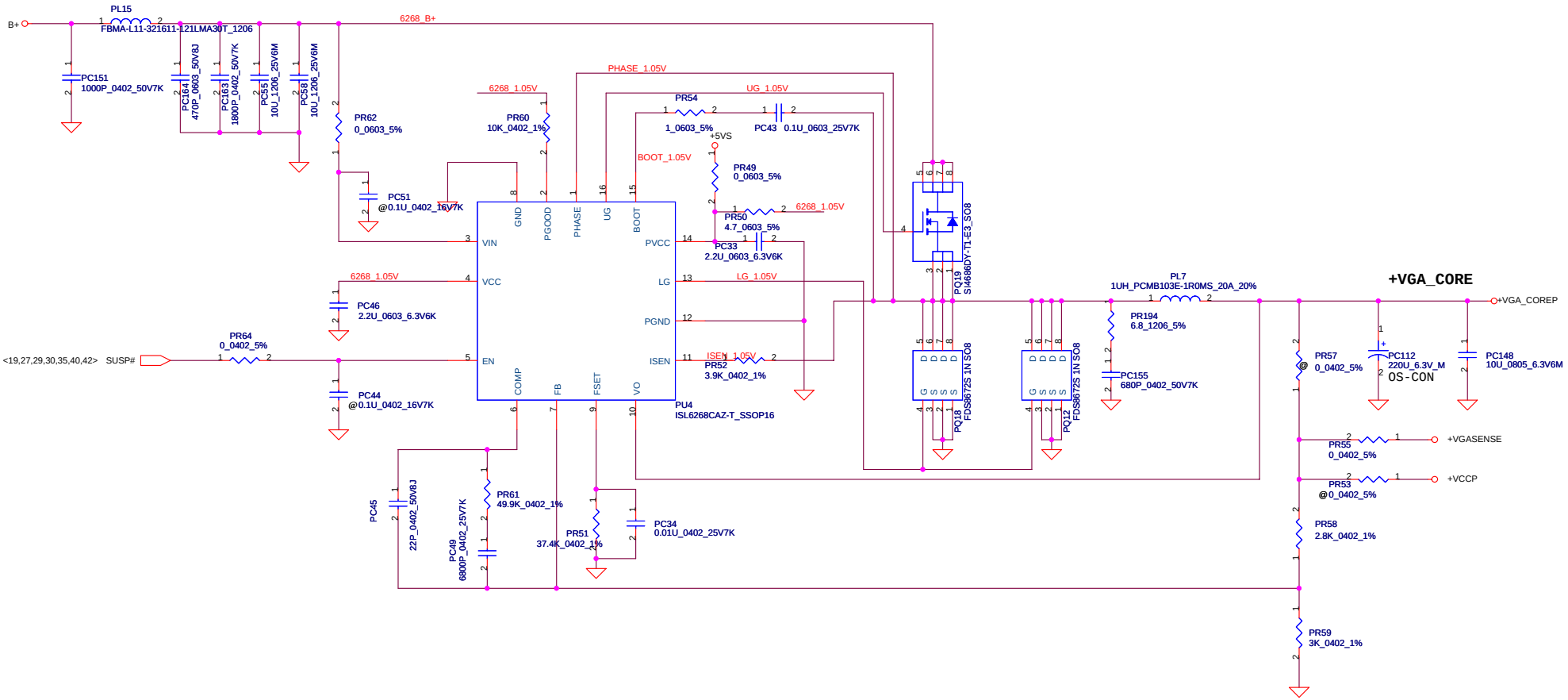
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 1.8V / 1.5V

Size	Document Number	Rev
		1.0

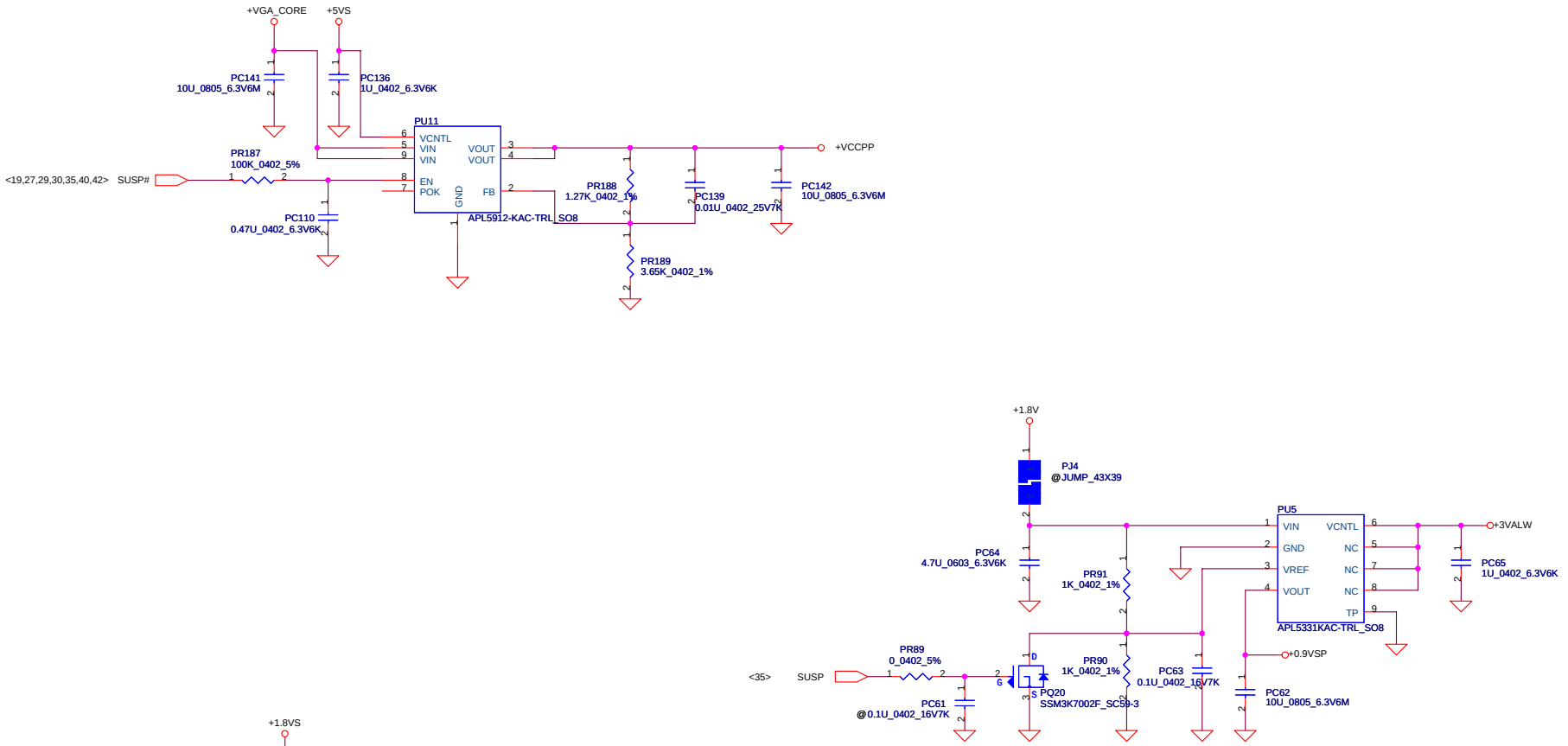
Date: Monday, May 12, 2008 | Sheet 48 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title	VGA_CORE
Size	Document Number
Rev	1.0
Date:	Monday, May 12, 2008
Sheet	49 of 53



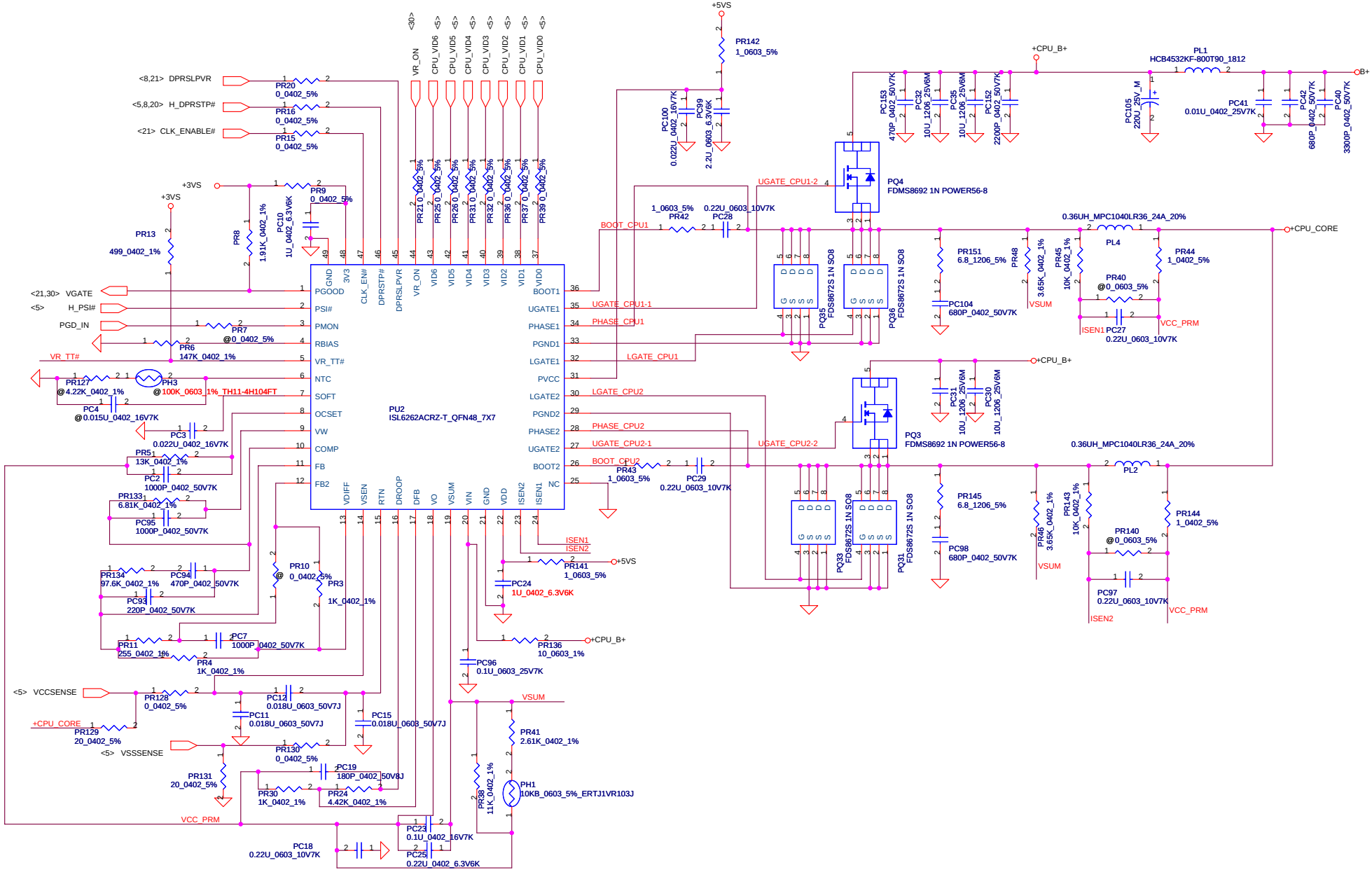
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: VCCP/0.9V/1.1V

Size | Document Number | Rev 1.0

Date: Monday, May 12, 2008 | Sheet 50 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

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Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number | Rev: 1.0

Date: Monday, May 12, 2008 | Sheet 51 of 53

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	10/12	P48	Add PR185, PR186	Reserve for debug use.
	10/12	P49	Delete PC110	Because HW reserve enough CAP.
	10/17	P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
	10/17	P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

Compal Electronics, Inc.

Title: **Power PIR**

Size	Document Number	Rev
	JIWA3/A4_LA4212P	1.0

Date: Monday, May 12, 2008 | Sheet 51 of 51

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	P29	C615 change to R615 and BOM Structure change to PM@	Fix DIS Audio issue
2	12/10	P20、P21	R104 & R154 BOM Structure change to PM@	Reduce cost
3	12/10	P16	R86、R645、R646、R650、R651、R652 & R653 BOM Structure change to PM@	Reduce cost
4	12/10	P29	R614 change from 10K to 45.3ohm R615 change from 12K to 54.9ohm	Fix UMA Audio issue
5	12/10	P08	R79 change from 33 to 10ohm R80、R81、R82 & R85 change from 0 to 22 ohm	Fix UMA Audio issue
6	12/10	P30	The C783 links to GND	Fix Internal MIC issue
7	12/10	P41	Add L45 & L46 MBC1608121YZF Bead	Fix F/B issue
8	01/02	P11	Change C126 package	
9	01/02	P28	Add R707 to connect VGATE to M_PWROK	Modify power sequence
10	01/02	P16	Add R699 to connect +VGASENSE	
11	01/02	P16	Remove U3.P1	
12	01/02	P19	Add R700 to connect GND	
13	01/02	P11	Add C707	for +VCC_DMI
14	01/02	P16	Add C788	for nvidia request for +PEX_PLLVDD
15	02/27	P08	change R147 from 511 ohm 1% to 499 ohm 1%	
16	02/27	P23	change D4 location	
17	02/27	P23	Add D25 , D26 for ESD	
18	02/27	P25	Add D27 , D28 & D29 for ESD	
19	02/27	P29	Add R713 connect to 1.5V	
20	02/27	P31	change C550 , C570 , C506 & C507 to 0.1uF 0603	Fix pop noise issue
21	05/08	P05	Add R726 1k ohm & C808 0.1uF to fix issue.	
22	05/08	P16	Remove R48 for EMI request.	
23	05/08	P27	Change R554 from 0 ohm to 33 ohm for EMI request.	
24	05/08	P28	Add R566 10 ohm & C733 10pF for EMI request.	
25	05/08	P30	Add R327 47 ohm & C458 33pF for EMI request.	
26	05/08	P35	Change C501 & C514 from 15pF to 12pF	
27	05/08	P37	Add D31 (PJDLC05_SOT23-3) for ESD request.	
28	05/08	P41	Add C494、C522、C564 & C568 220pF for EMI request	

Title	<Title>	
Size	Document Number CustomJIWA3/A4_LA4212P	Rev 1.0
Date: Monday, May 12, 2008	Sheet 53 of 53	