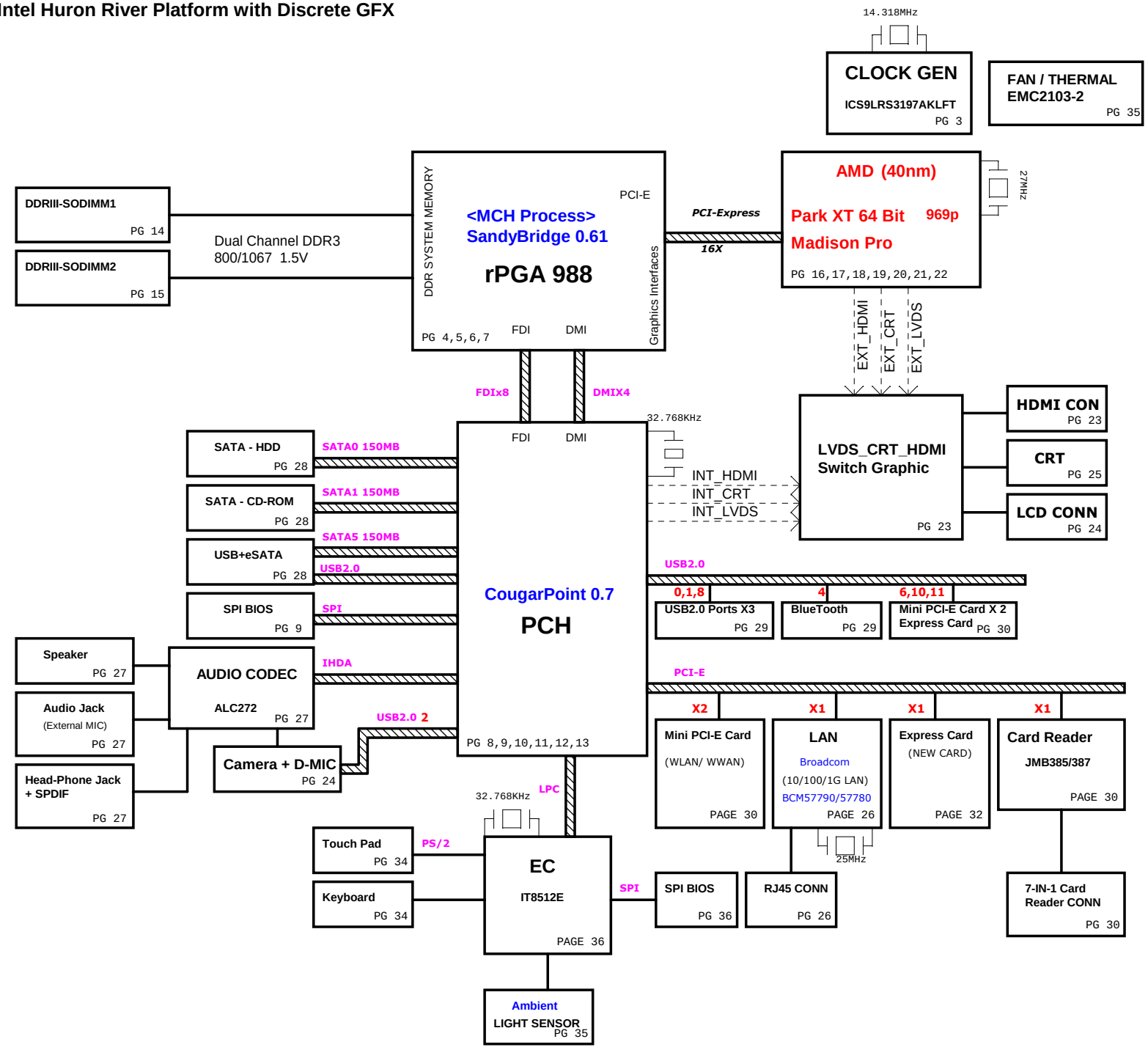
KL3E Intel Huron River Platform with Discrete GFX

01



POWER

Discharge	PG 38
RUN POWER SW 3VSUS, 5VSUS, 3V_S5, 5V_S5 +3V, +5V	PG 38
AC/BATT CONNECTOR	PG 42
BATT CHARGER	PG 39
REGULATOR (DDR3) 1.5VSUS, 0.75VSMDDR_VTERM,1.5V 1.5V_GPU,1.5V_CPU	PG 40
REGULATOR +1.05V_VTT,+1.8V	PG 41
DC/DC 3VPCU, 5VPCU, +15V	PG 42
CPU Core	PG 43
VGA Core Discrete 1.8V_GPU, 1V_GFX_PCIE	PG 44
VGA Core UMA	PG 45

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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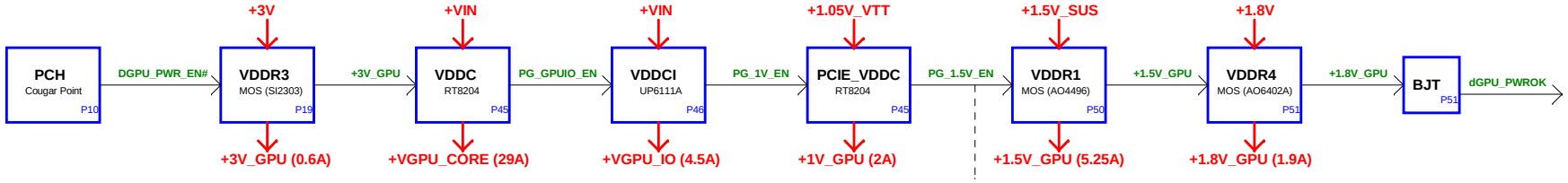
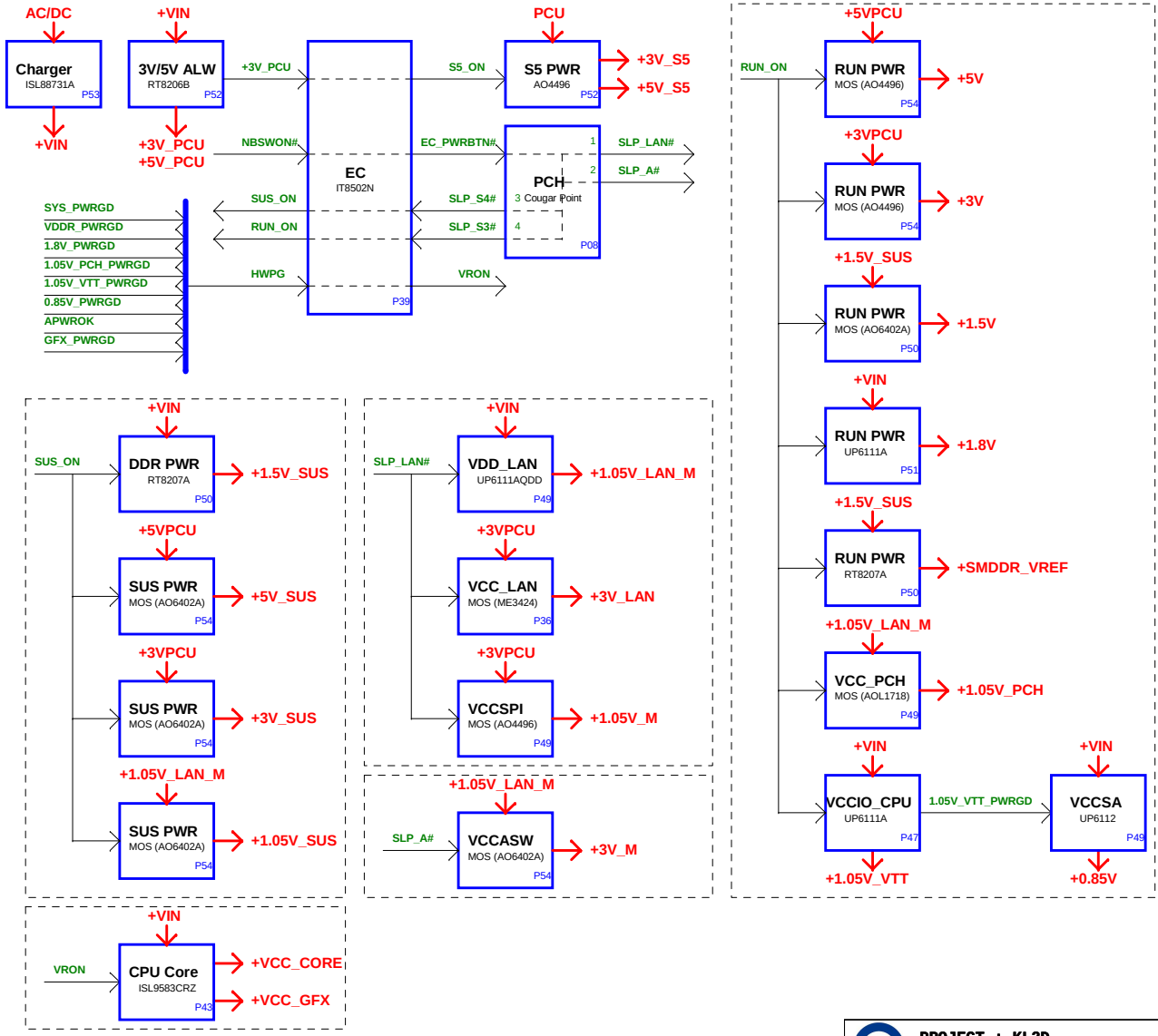
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



Main Power Rails

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+0.75V_DDR_VTT	+0.75V	DDR3 reference voltage	RUN_ON	
+0.85V	+0.9V	Intel new power rail	1.05V_VTT_PWRGD	
+1.05V_LAN_M	+1.05V	LAN M power for iAMT	SLP_LAN#	
+1.05V_M	+1.05V	ME power for iAMT	SLP_A#	
+1.05V_PCH	+1.05V	PCH core power	RUN_ON	
+1.05V_SUS	+1.05V	USB3.0 chip power	SUSD	
+1.05V_VTT	+1.05V	CPU core logic power	RUN_ON	
+1.5V	+1.5V	I/O module power	RUN_ON	
+1.5V_CPU	+1.5V	CPU DDR3 controller power	RUN_ON_D	
+1.5V_GPU	+1.5V	GPU DDR3 controller power	PG_1.5V_EN	
+1.5V_SUS	+1.5V	DDR3 SODIMM power	SUS_ON	
+1.8V	+1.8V	CPU/PCH/LVDS power	RUN_ON	
+1.8_GPU	+1.8V	GPU power	+1.5V_GPU	
+1V_GPU	+1V	GPU PCIE VDDC power	PG_1V_EN	
+3V	+3.3V	I/O power	RUN_ON	
+3V_GPU	+3.3V	GPU power	DGPU_PWR_EN#	
+3V_M	+3.3V	PCH/SPI power for iAMT	SLP_A#	
+3V_S5	+3.3V	3V power sequence	S5_ON	
+3V_SUS	+3.3V	USB3.0 chip power	SUSD	
+3VPCU	+3.3V	Always power	SYS_SHDN#	
+5V	+5V	I/O power	RUN_ON	
+5V_S5	+5V	5V power sequence	S5_ON	
+5V_SUS	+5V	USB2.0 power	SUSD	
+5VPCU	+5V	Always power	SYS_SHDN#	
+15V_ALW	+15V	Power sequence		
+SMDDR_VREF	+0.75V	DDR3 reference power	RUN_ON	
+VCC_CORE	+1.1V	CPU Core power	VRON	
+VCC_GFX	+1.52V	Internal GPU Core power	VRON	
+VGPU_CORE	+1V	GPU Core power	DGPU_VRON	
+VGPU_IO	+1V	GPU I/O controller power	PG_GPUIO_EN	
+VIN	+19V	AC power input		



EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-C-01	41	08/26	PR319	Add PR319. Change +0.75V contral signal
EC-C-02	36	08/26		Change LED power to +3V_S5
EC-C-03	24	08/26		Change HDMI pull high to +3V
EC-C-04	23	08/30		Remove MUX for LVDS and CRT. Change for Resistor option.
EC-C-05	18	09/01	C91	Change C91 to 0603 part. The same as C594
EC-C-06	10	09/01	Q47, R725, R726	Del reserve schematic
EC-C-07	9	09/01	R538	Change value to 1K
EC-C-08	9	09/02	C814	Reserve for RF
EC-A-09	35,37	09/07	C483, C355, C356	Mount CYAVLC18B02 for ESD

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
	Clock Generator	1A

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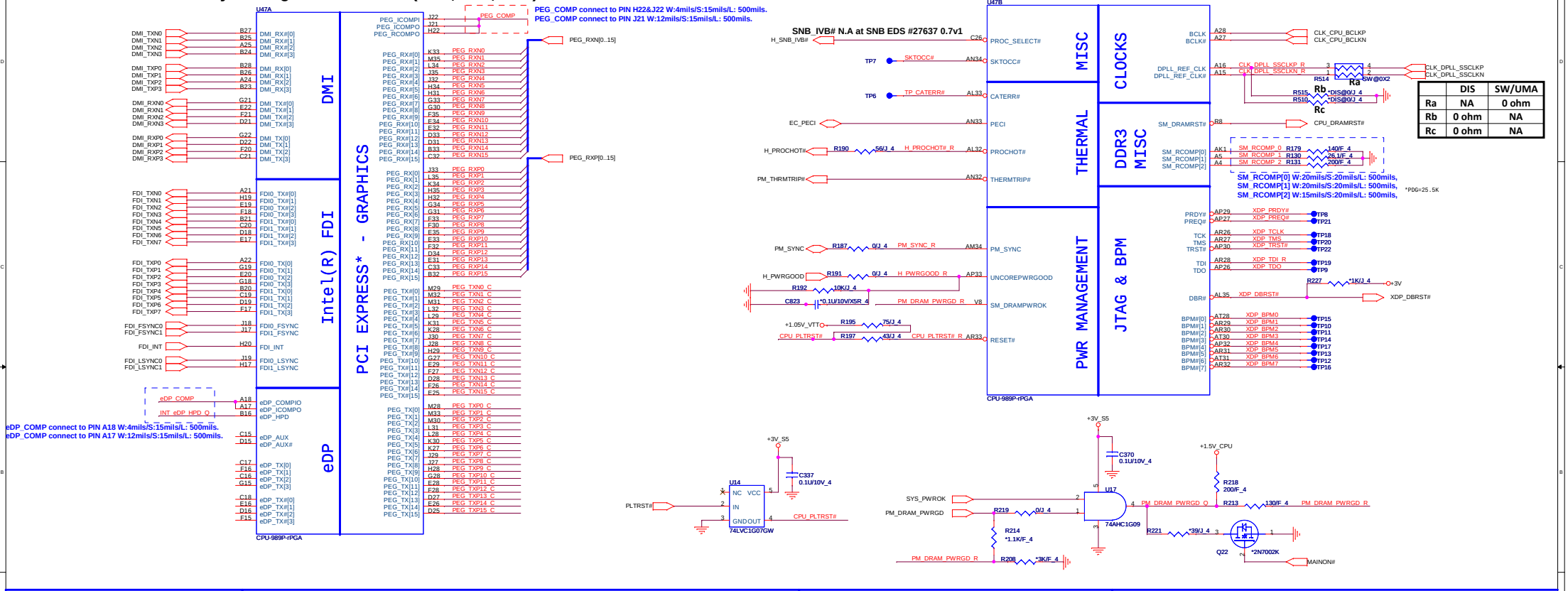
Sandy Bridge Processor (DMI,PEG,FDI)

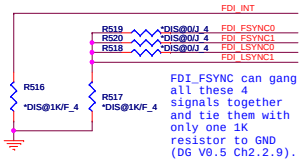
Sandy Bridge Processor (CLK,MISC,JTAG)

04



	DIS	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

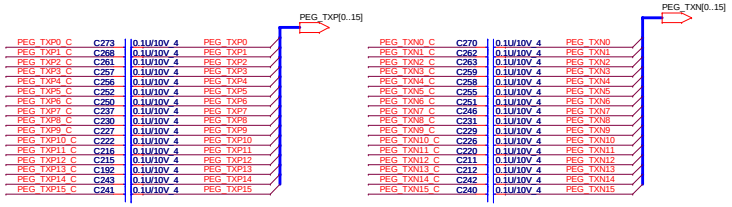
FDI Disable



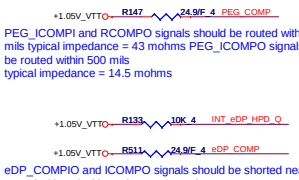
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 (UMA Non-stuff)

0.22uF for PCIE GEN 3 support in feture support.



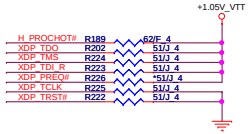
DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Sandy Bridge 1/4	1A

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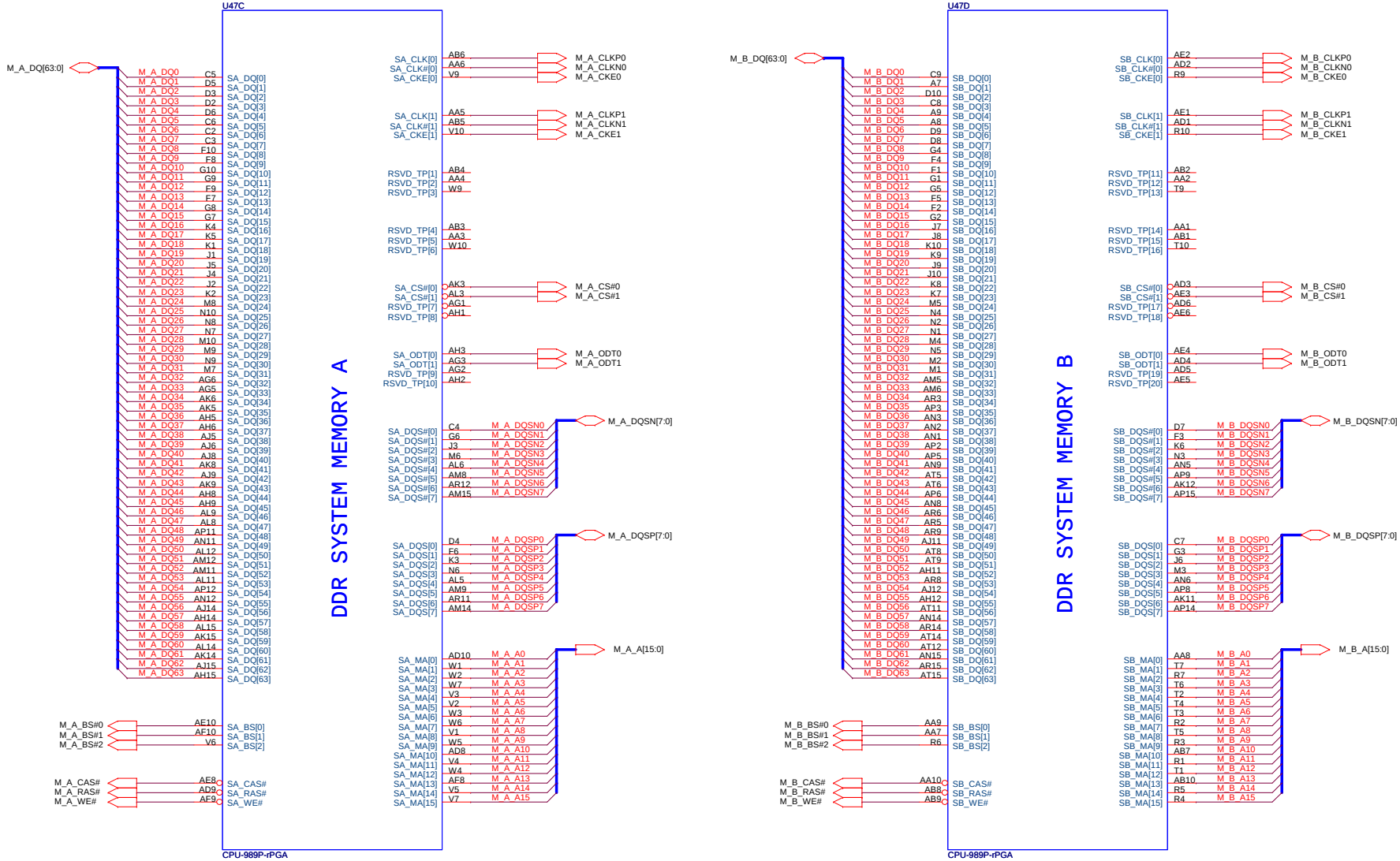
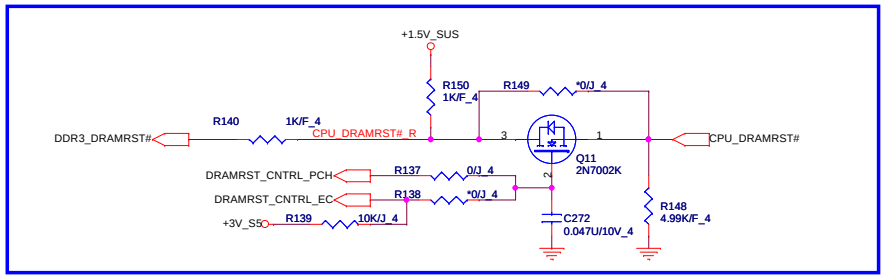
Sandy Bridge Processor (DDR3)





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Quanta Computer Inc.		
Size	Document Number: Sandy Bridge 2/4	Rev: 1A
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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
VREF
SA RAIL
1.8V RAIL
MISC

U47F
CPU-989P-rPGA
U47G
CPU-989P-rPGA

Reserved

Layout note: need routing together and ALERT need between CLK and DATA

Place PU resistor close to CPU
SVID CLK
Close to VR
SVID DATA
Close to VR
Place PU resistor close to CPU
SVID ALERT

4.5A
JP1 SHORT PAD
Q13 AO4496
Q12 DMN601K-7
3/26 DB add for Intel. Placement close to CPU.

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

Ra	DIS	SW
Ra	0 ohm	NA

PROJECT : KL2D
Quanta Computer Inc.
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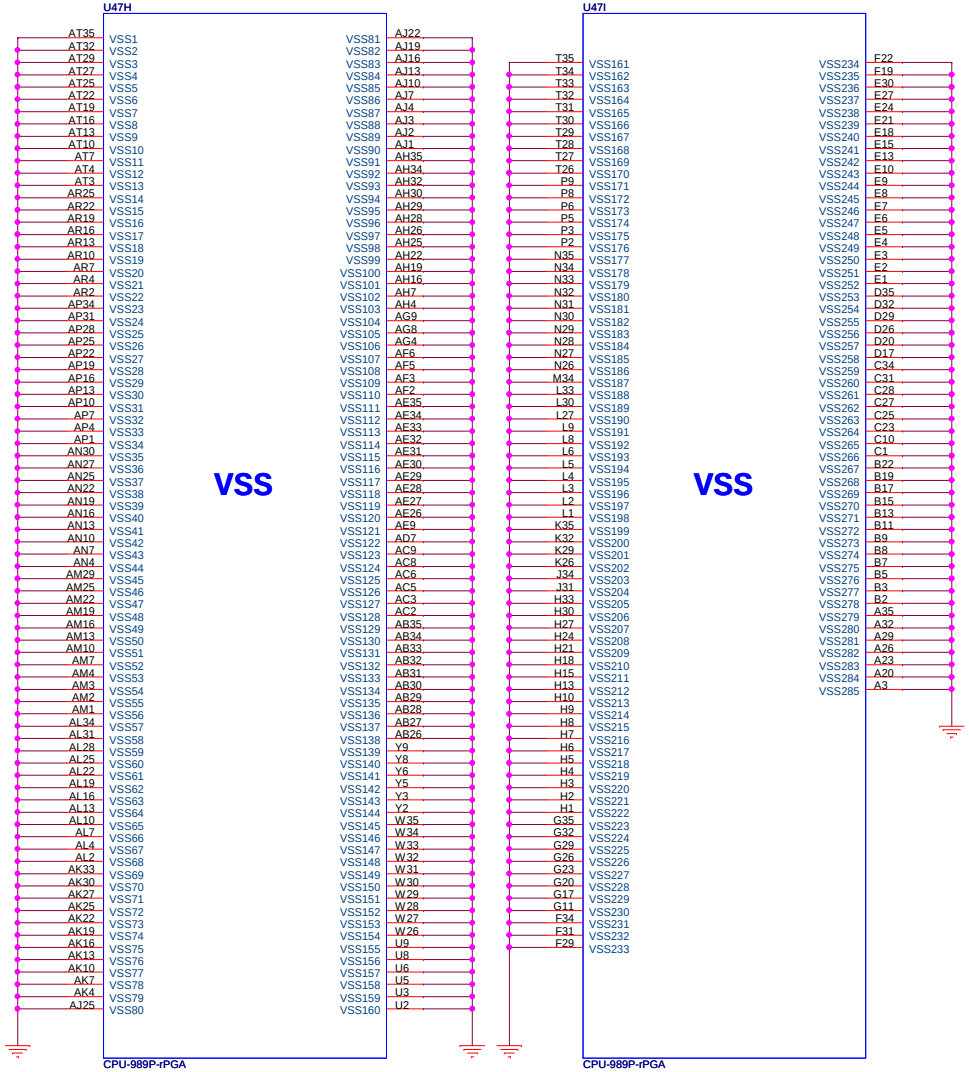
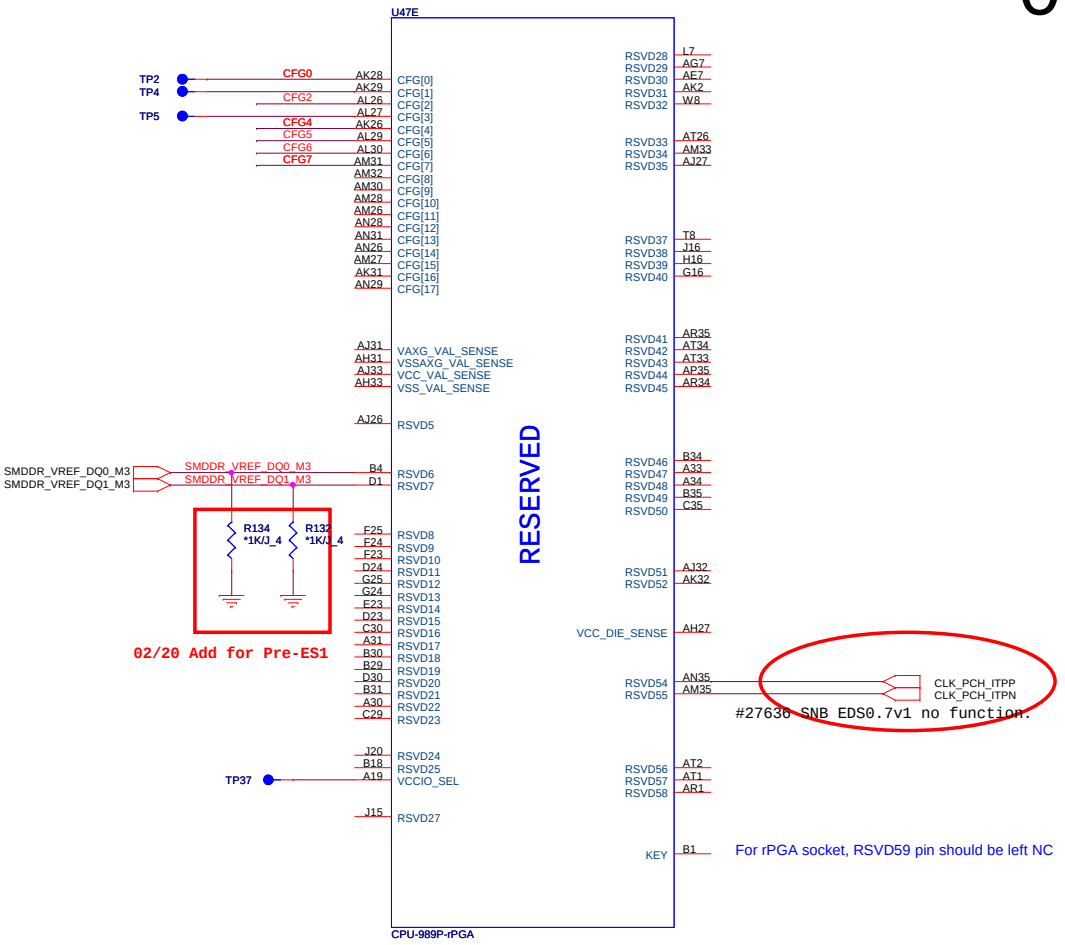
Sandy Bridge Processor (GND)



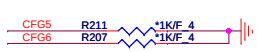
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP Leave NC for disable	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Quanta Computer Inc.

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
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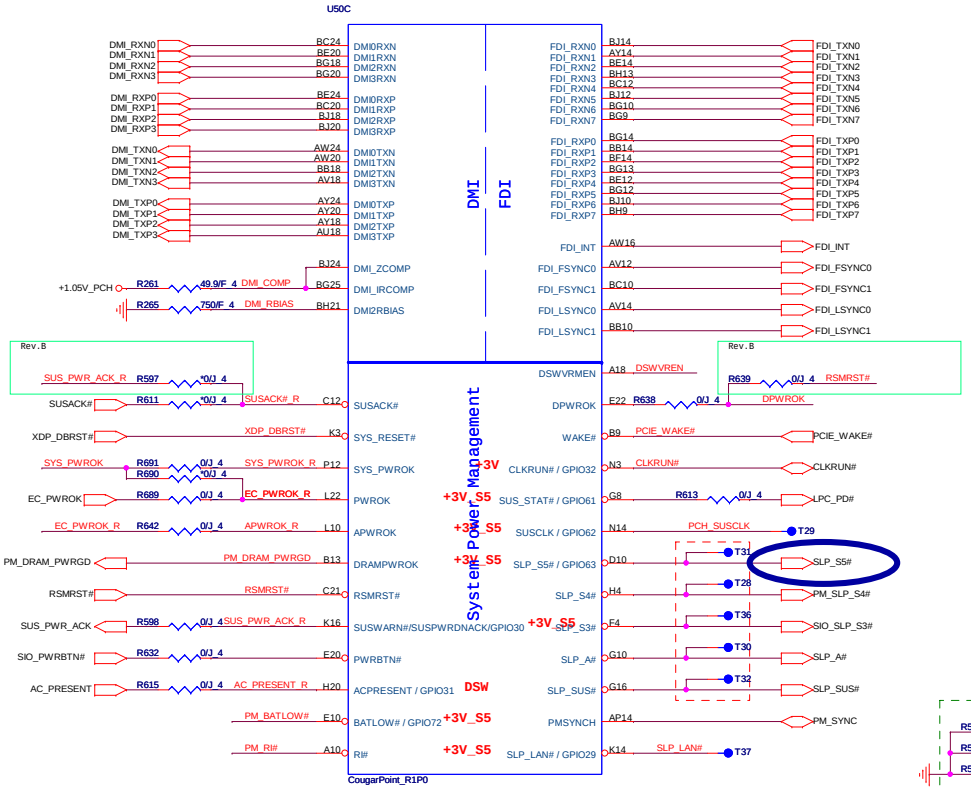
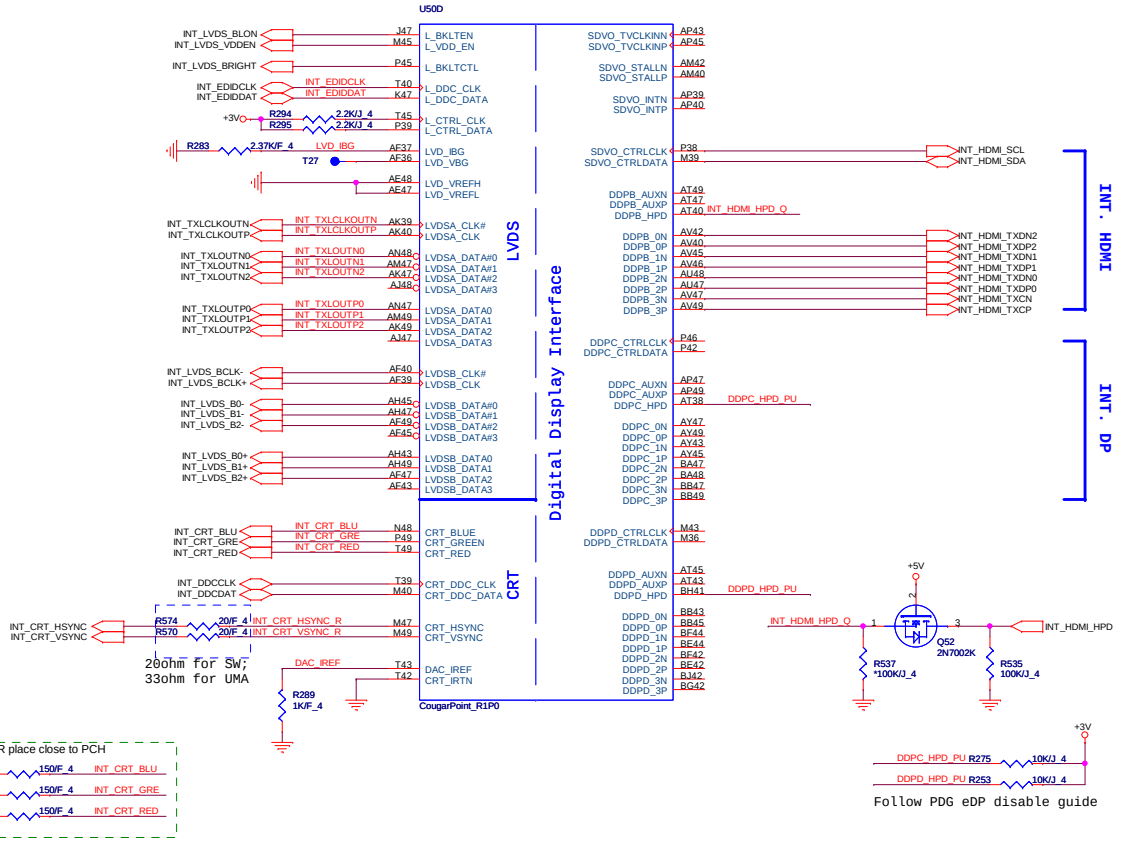
Cougar Point (DMI,FDI,PM)



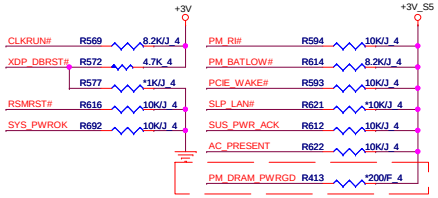
Cougar Point (LVDS,DDI)



R place close to PCH

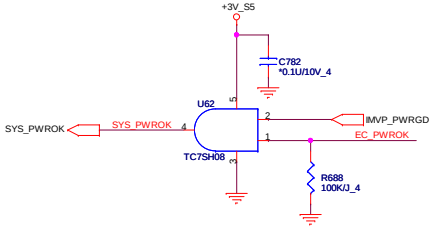
R566	150/F_4	INT_CRT_BLU
R563	150/F_4	INT_CRT_GRE
R560	150/F_4	INT_CRT_RED

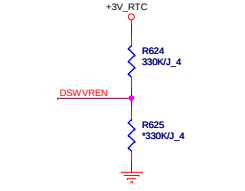
PCH Pull-high/low(CLG)



3/16 Change topology; 200ohm PU to +3V_S5

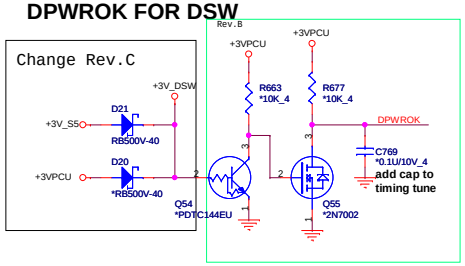
System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW



Deep sleep option	Support	Not support
SUS_PWR_ACK	To PCH SUSACK# (Pop R597)	EC or NC (Non-pop R597)
DPWROK	DSWPWRGD (Pop Q54, R663, Q55, R677)	RSMRST (Pop R639)
SLP_SUS	EC	NC

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Quanta Computer Inc.

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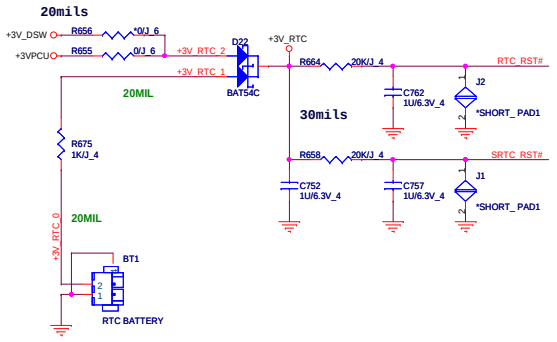
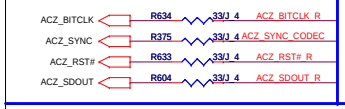
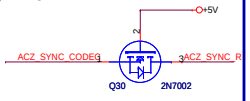
RTC Circuitry(RTC)



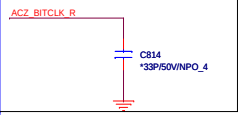
HDA Bus(CLG)



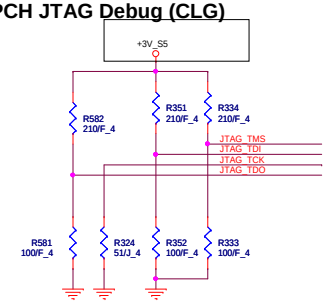
To Separate Codec Sync by PD3



Reserve for RF

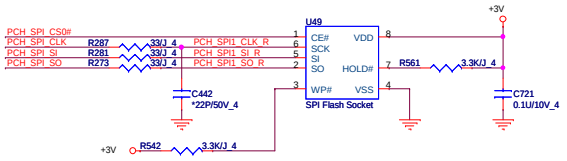


PCH JTAG Debug (CLG)



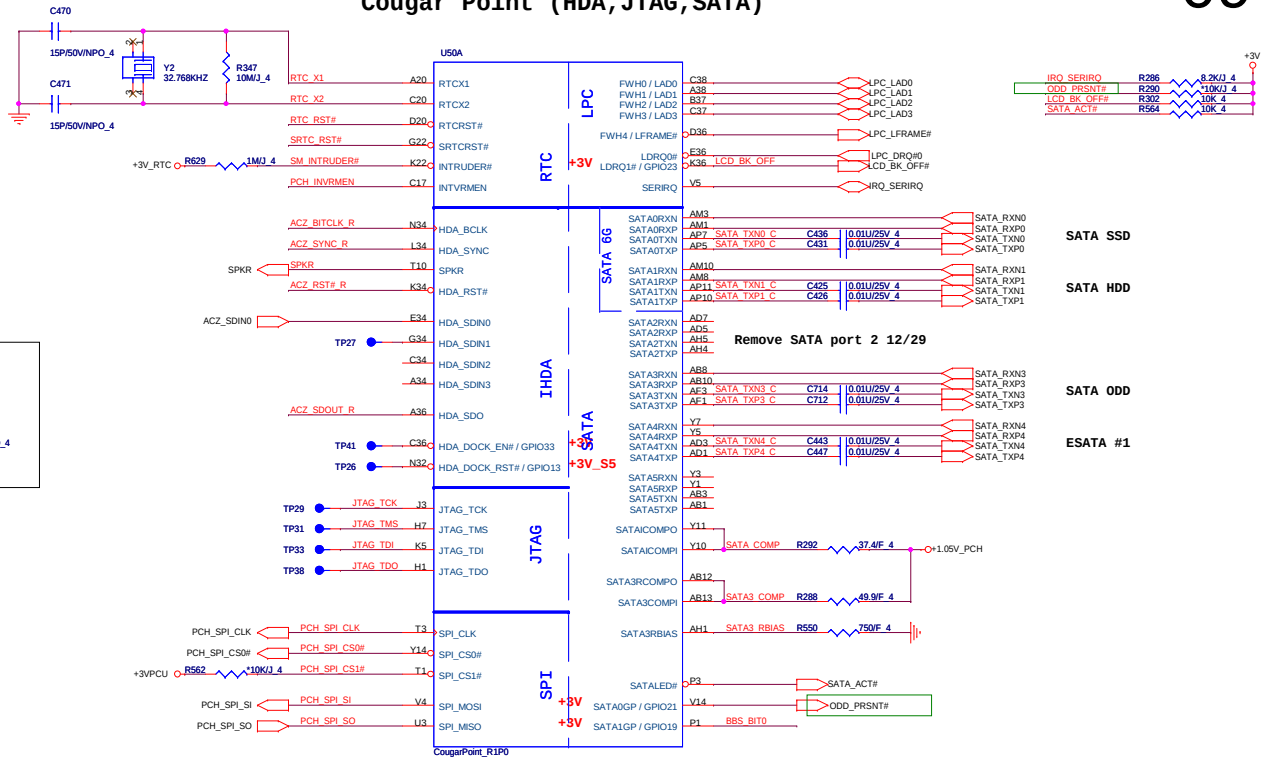
PCH Dual SPI (CLG)

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R307 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R608 *1K/J_4 PCI_GNT3#
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R592 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] R609 *1K/J_4 BBS_BIT1 R565 *1K/J_4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R590 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R536 2.2K/J_4 +1.8V R538 1K/F_4 DF_TVS H_SNB_IVB#
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R636 *1K/J_4 PLL_ODVR_EN
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R374 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R282 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 2/6	1A

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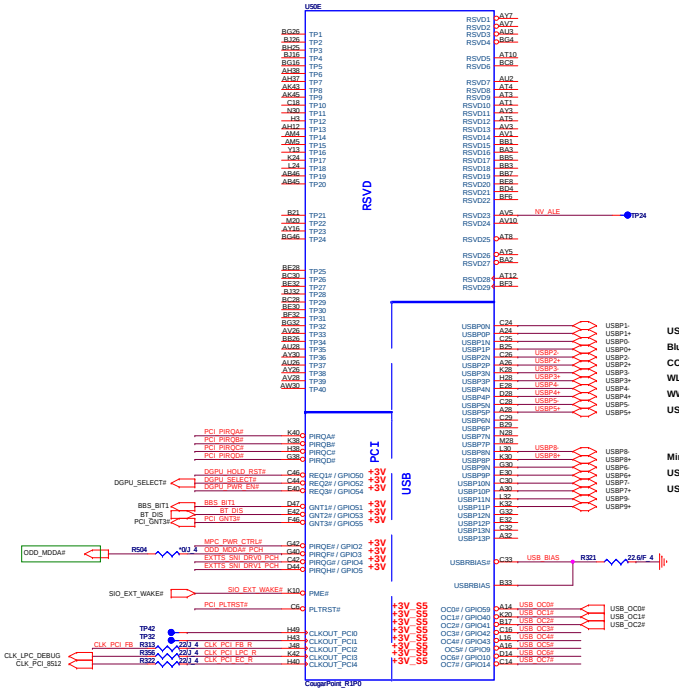
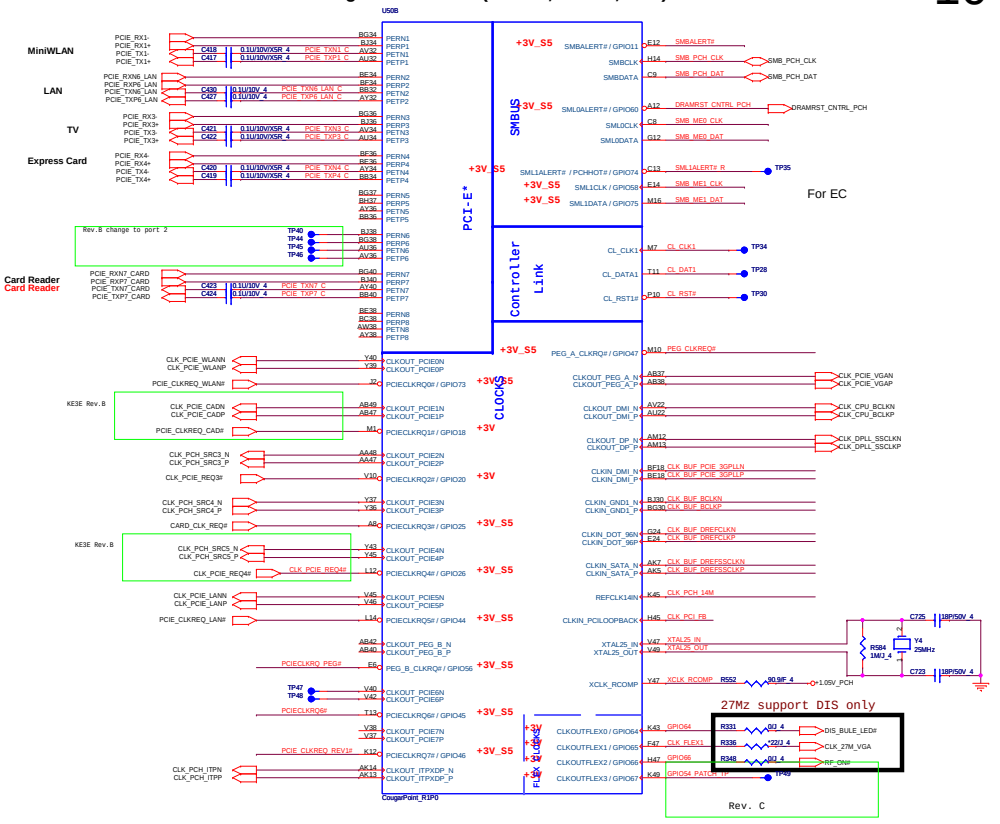
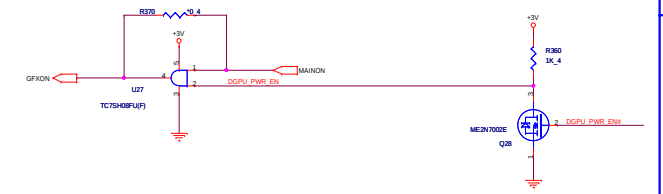
Cougar Point-M (PCI,USB,NVRAM)



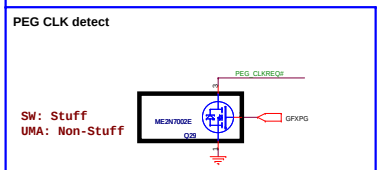
Cougar Point-M (PCI-E,SMBUS,CLK)



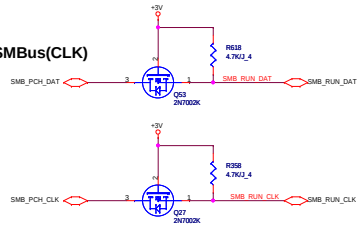
DGPU Power ON



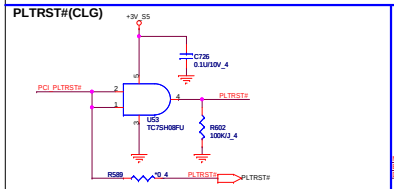
PEG CLK detect



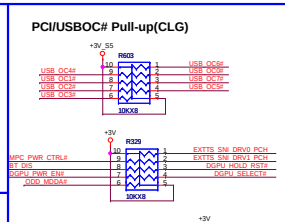
SMBus(CLK)



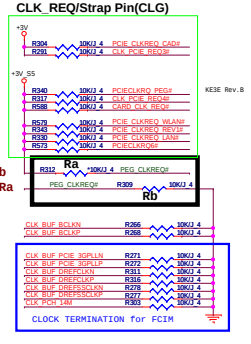
PLTRST#(CLG)



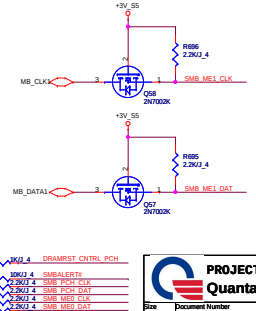
PCI/USBOC# Pull-up(CLG)



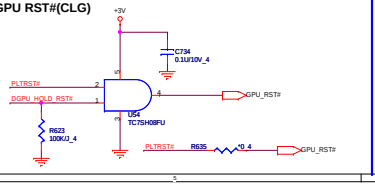
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



GPU RST#(CLG)



MPC Switch Control

MPC_PWR_CTRL#	LOW = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R320 *1KJ_4

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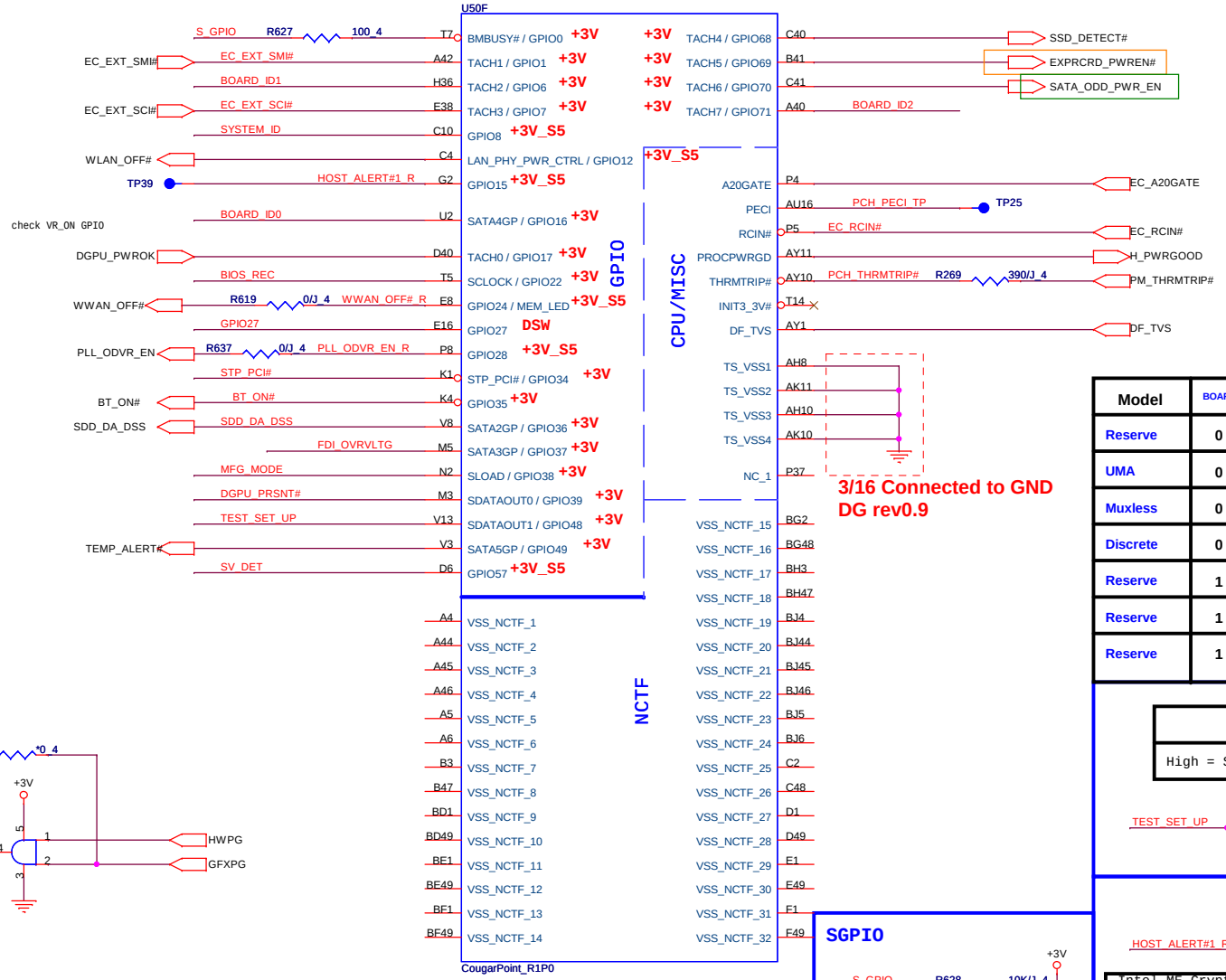
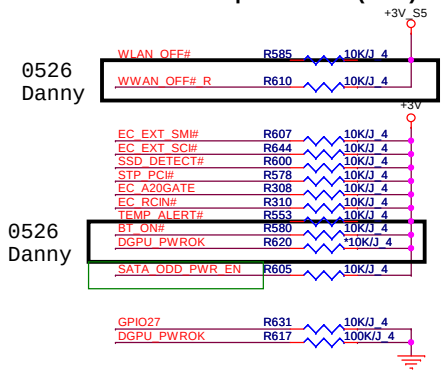
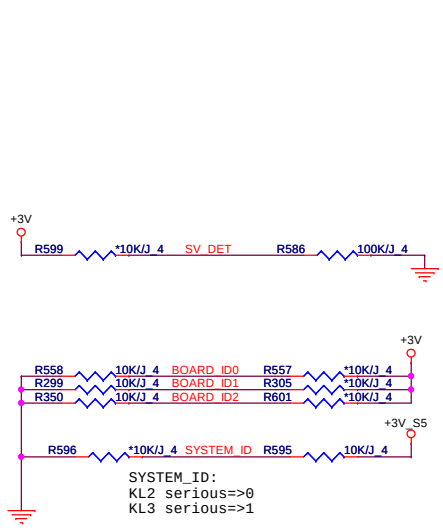
Cougar Point (GPIO,VSS_NCTF,RSVD)



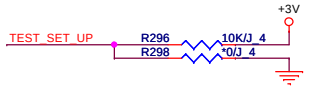
GPIO Pull-up/Pull-down(CLG)

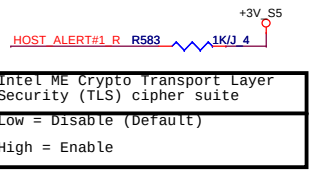


Model	BOARD_ID2	BOARD_ID1	BOARD_ID0
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0



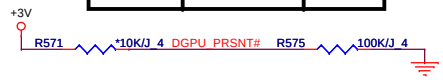
SV_SET_UP
High = Strong (Default)



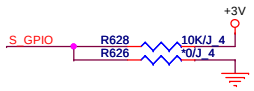


Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

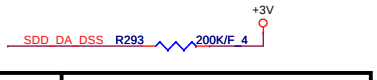
	SWITCHABLE	UMA
Stuff	R575	R571
No Stuff	R8490	R8489



SGPIO



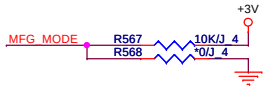
FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST



PROJECT : KL2D

Quanta Computer Inc.

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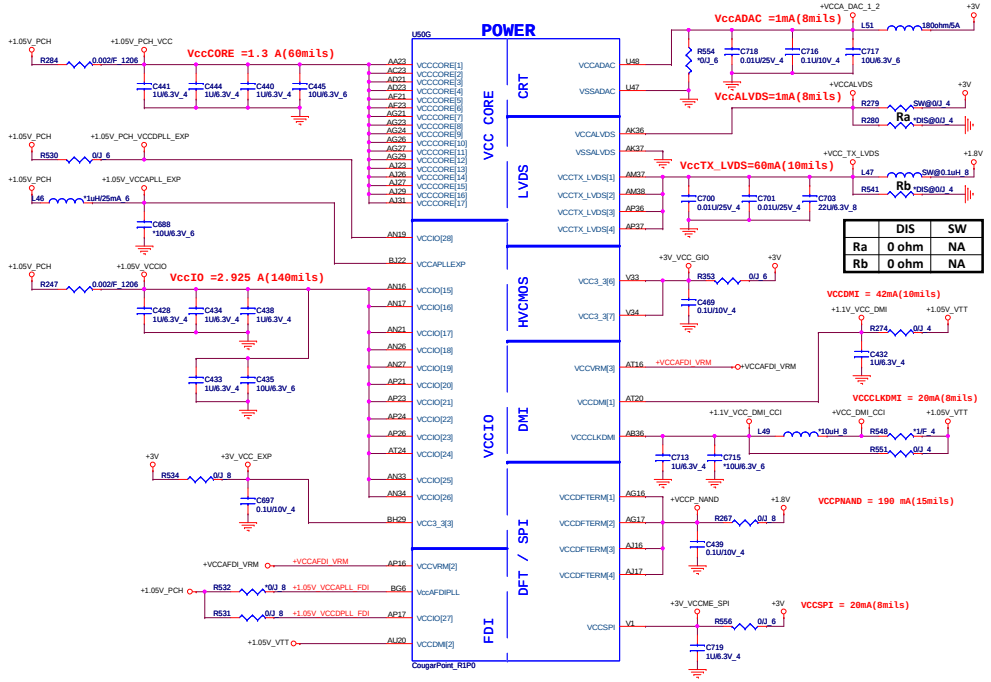
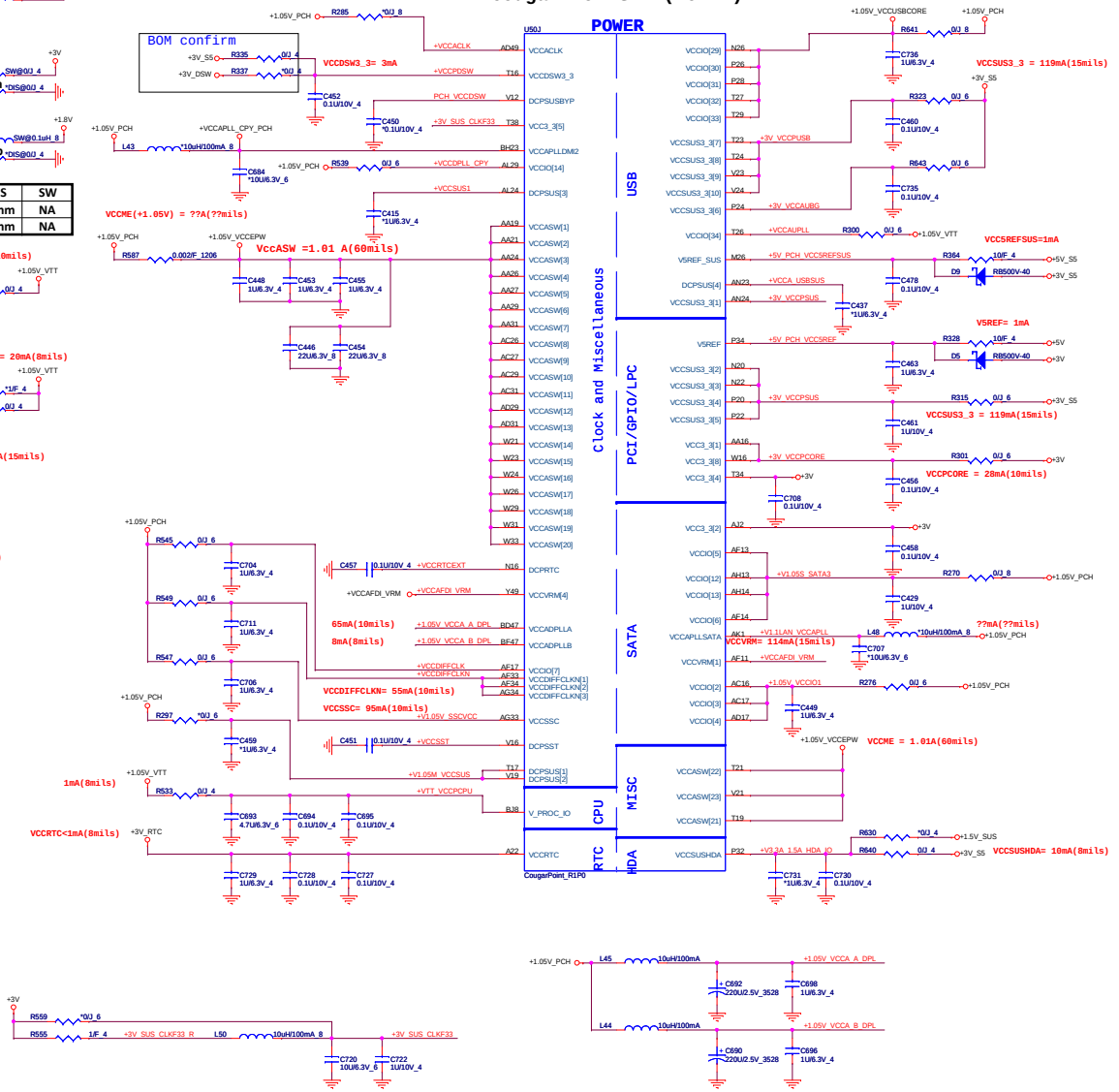
COUGAR POINT (POWER)



Cougar Point-M (POWER)



	DIS	SW
Ra	0 ohm	NA
Rb	0 ohm	NA

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Quanta Computer Inc.
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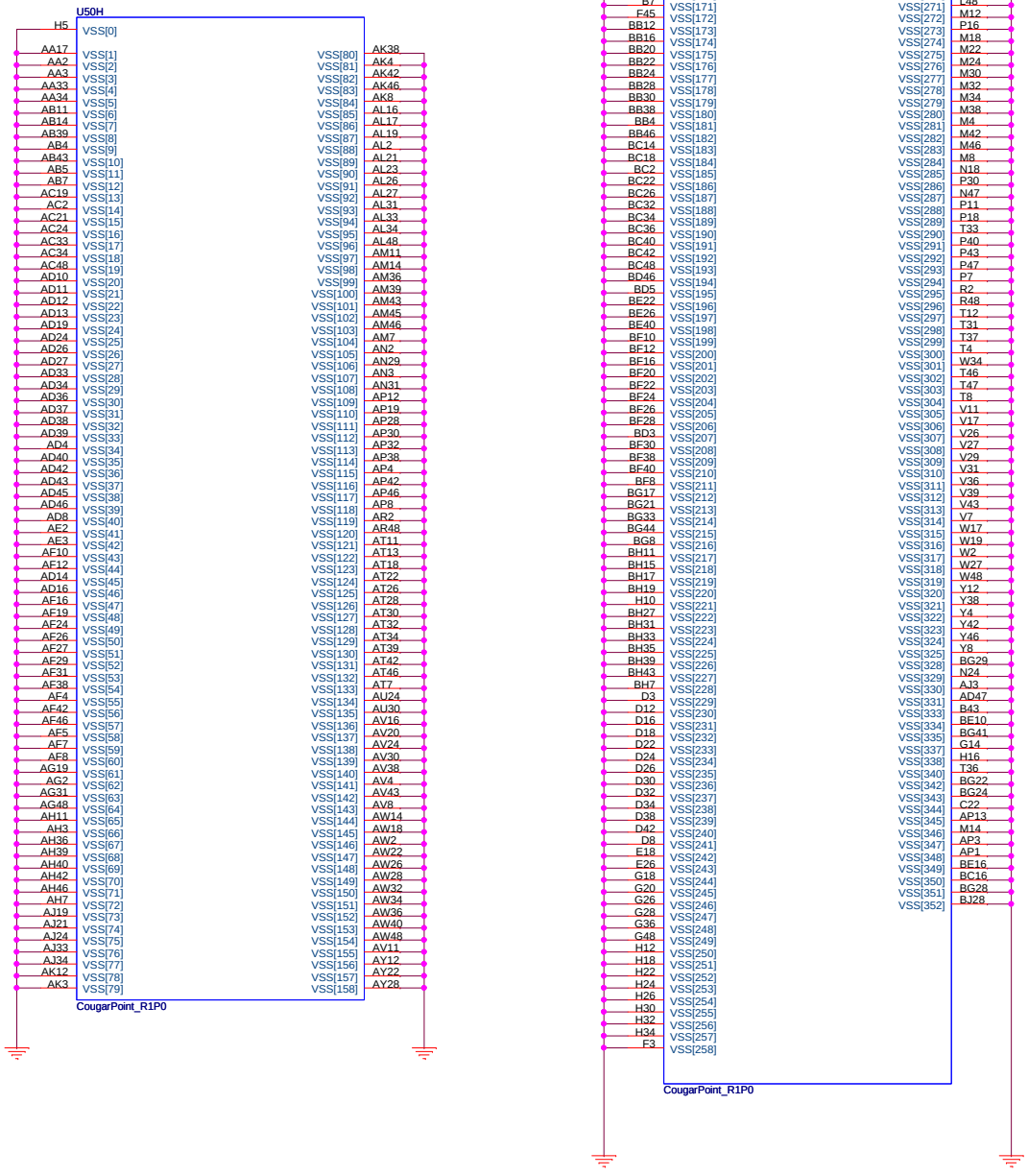
IBEX PEAK-M (GND)



PROJECT : KL2D

Quanta Computer Inc.

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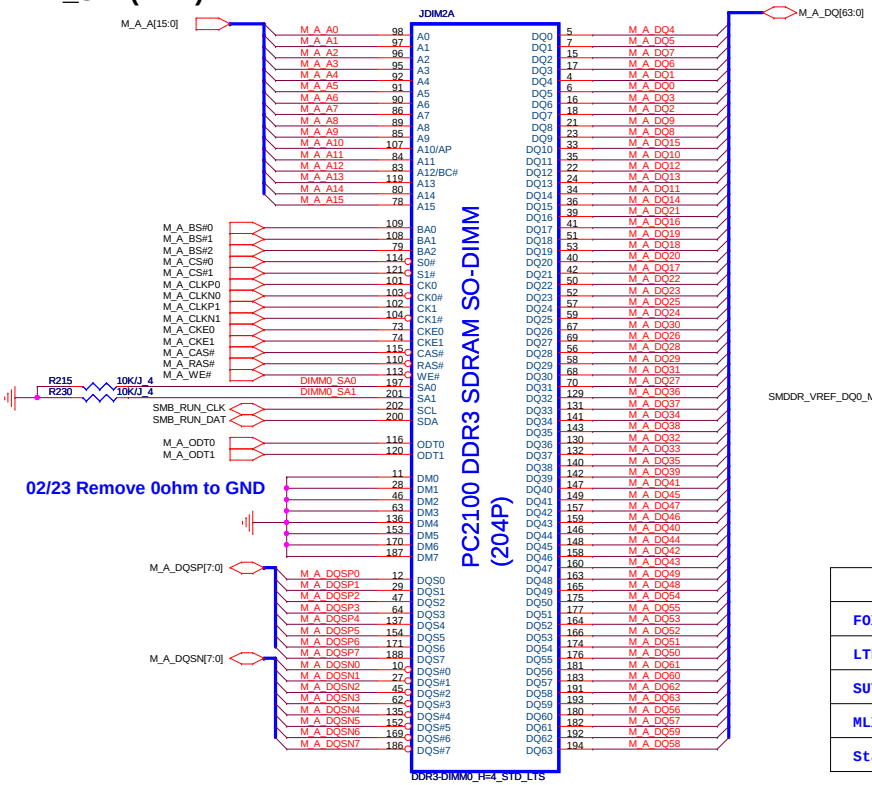
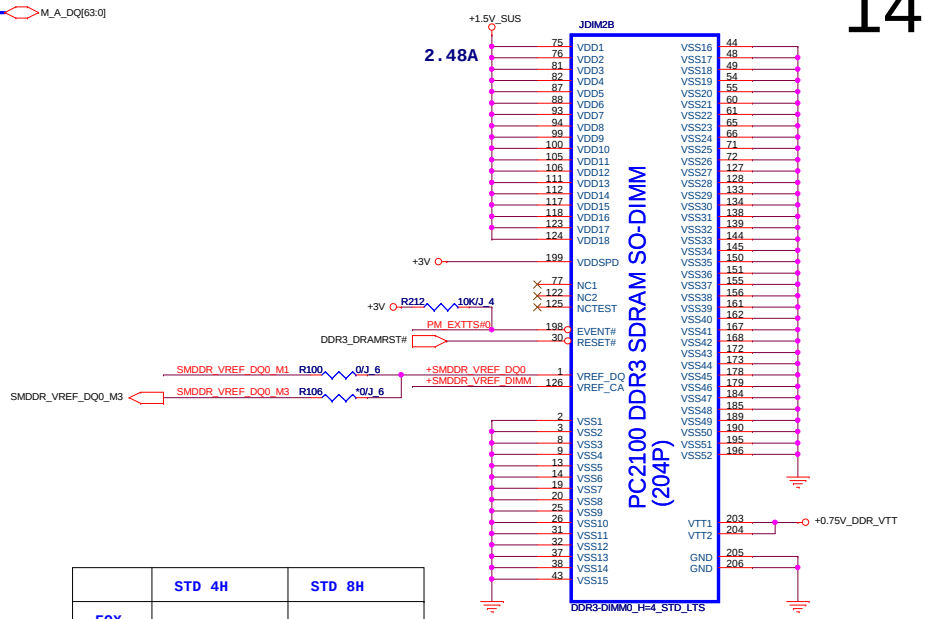
DDR_STD(DDR)



02/23 Remove 0ohm to GND

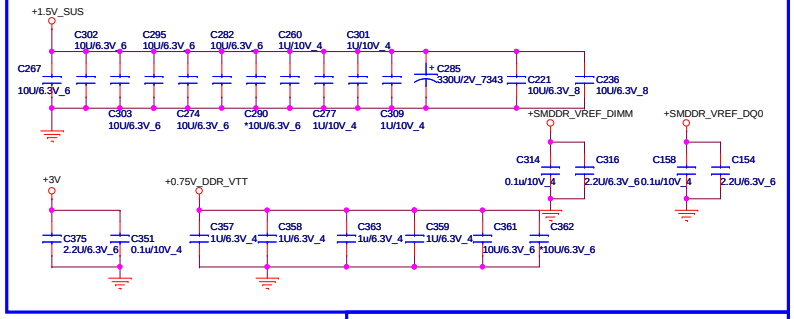


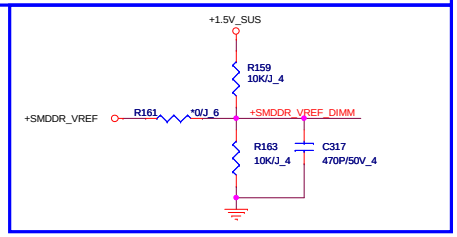
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR-C-2013289-204p

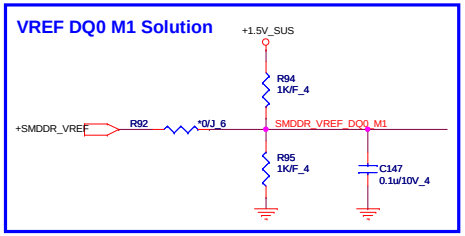
Rev. B Remove M2 schematic

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



PROJECT : KL2D

Quanta Computer Inc.

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	DDRIII SO-DIMM-0	1A
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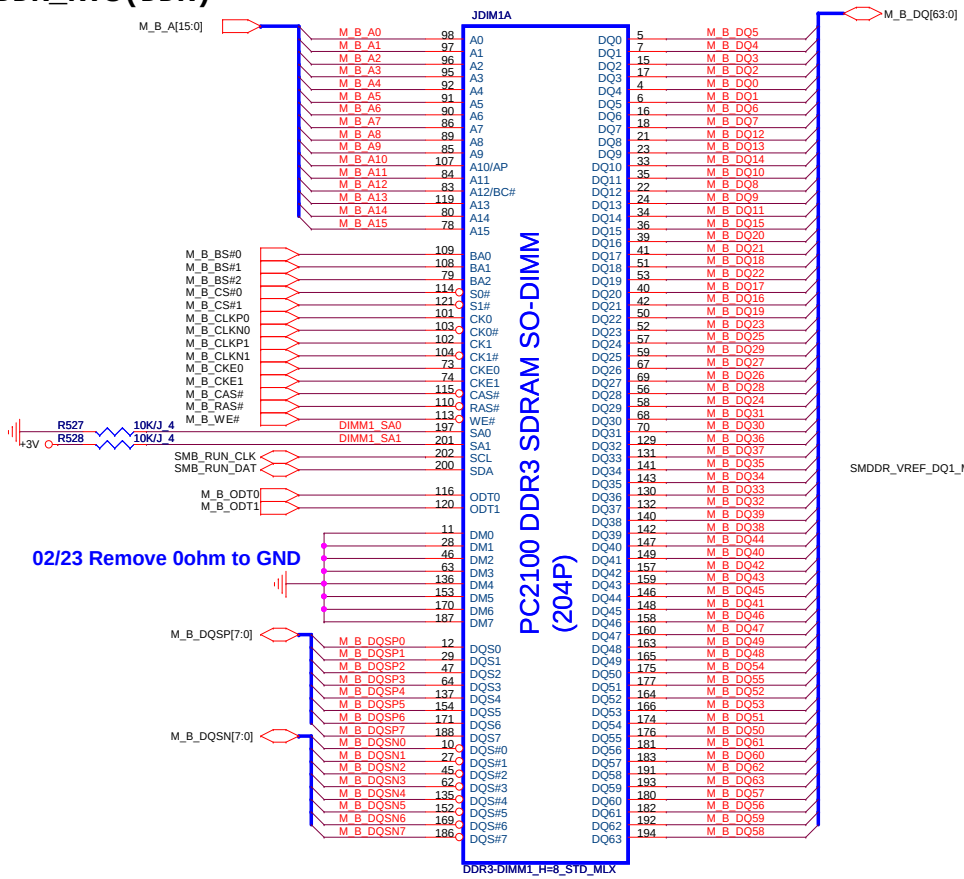
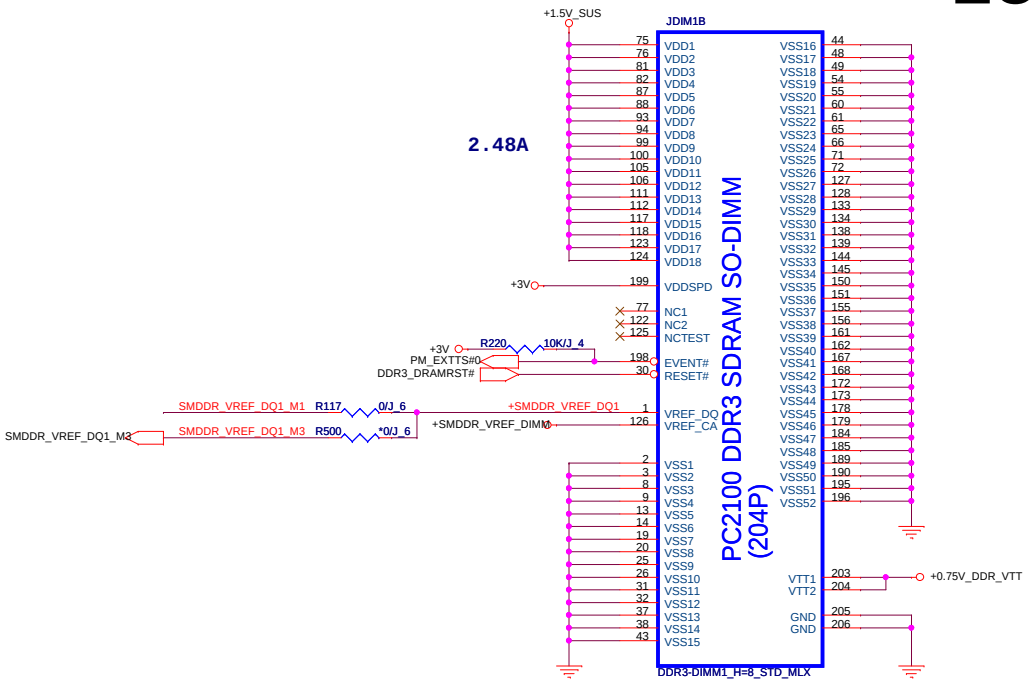
DDR_RVS(DDR)

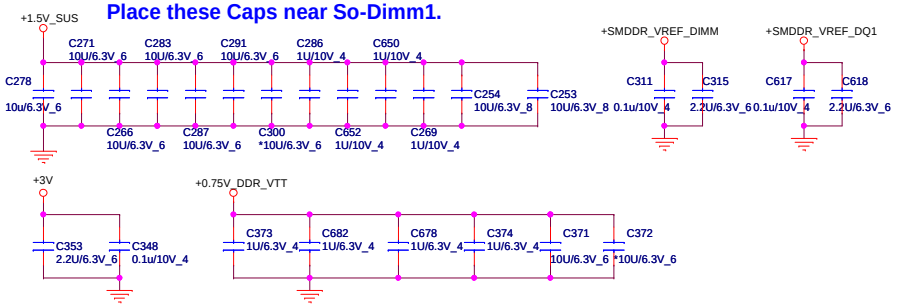


02/23 Remove 0ohm to GND

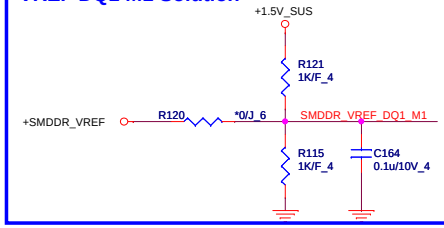


Rev. B Remove M2 schematic

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

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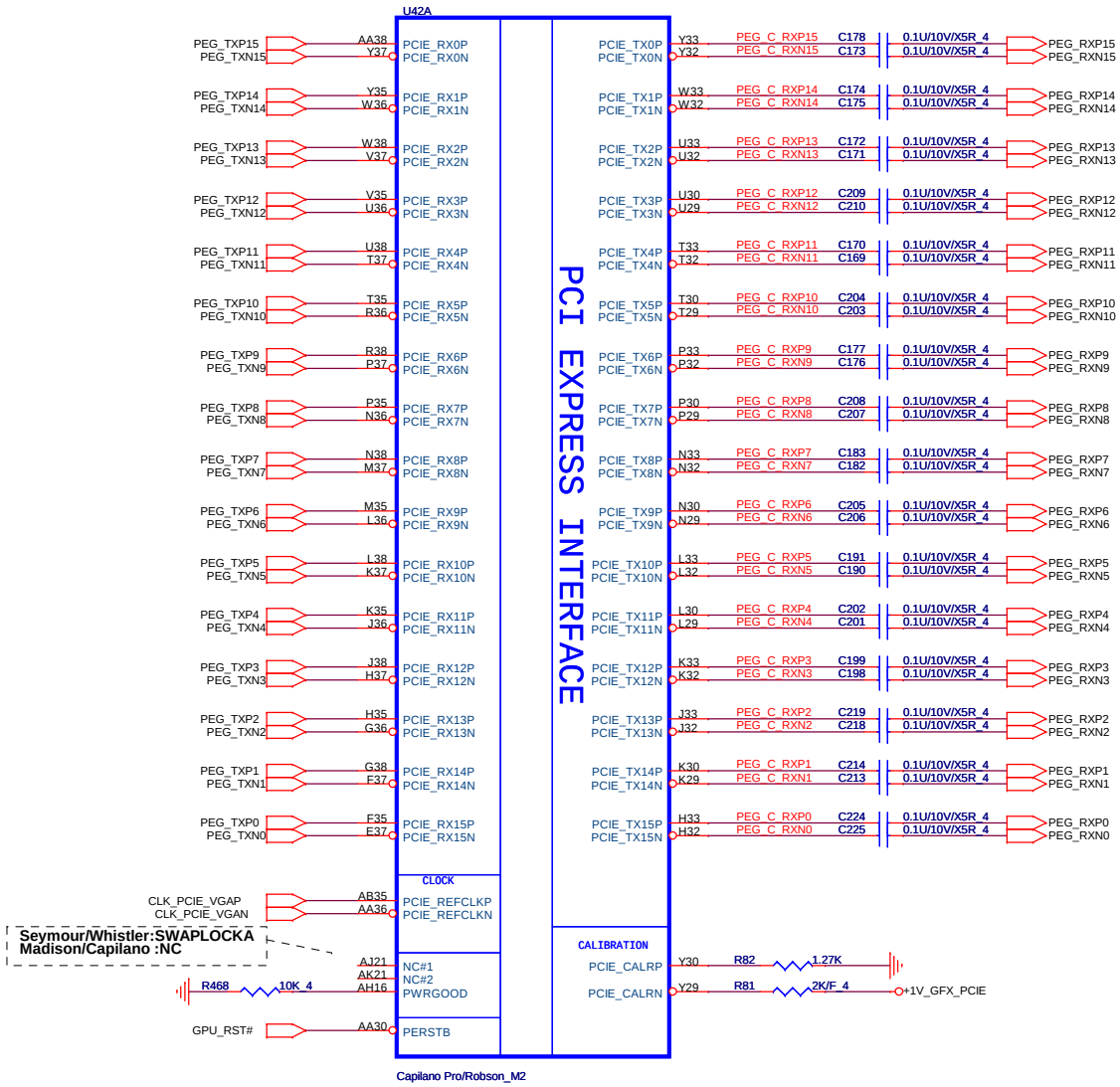

PROJECT : KL2D		
Quanta Computer Inc.		
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Memory Straps		RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
		0	0	1	0
		0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

C.F modify 07.21

Accss to SCL and SDA is mandatory on BACO design for debug purposes.

NC FOR PARK

NC FOR PARK

NC FOR PARK

LVDS

Power PWM config

GenericF/G is NC on PARK

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

NC on Seymour/Whistler

HDMI

CRT

!!! NC when M92-M2/PARK

!!! NC when M92-M2/PARK

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

Use 27Mhz Crystal for A test Danny0518

Capilano Pro/Robson_M2

PROJECT : KL2D
Quanta Computer Inc.

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C	Madison_IO&STRAP	1A

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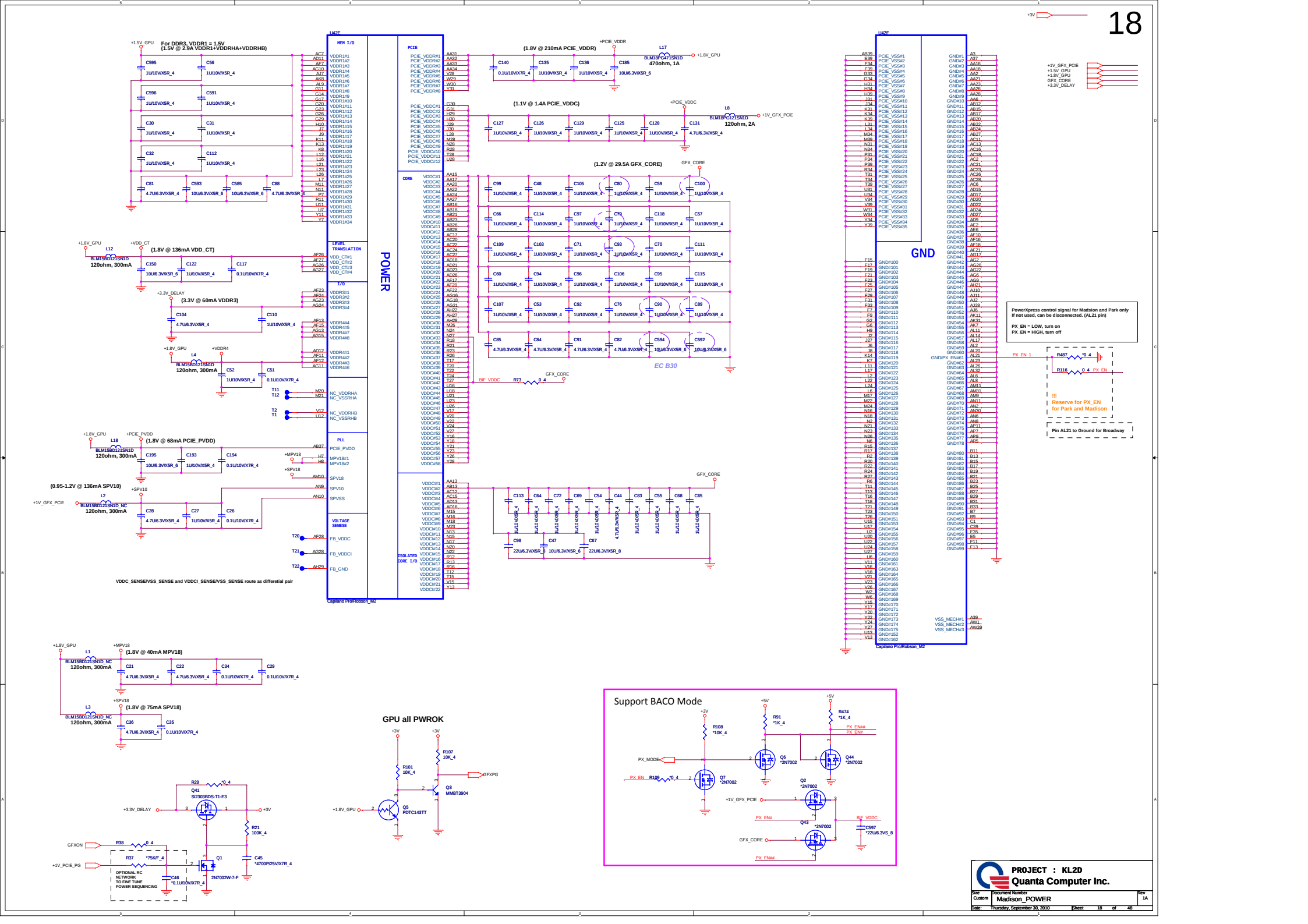

PROJECT	KL2D
Quanta Computer Inc.	
Size	Custom
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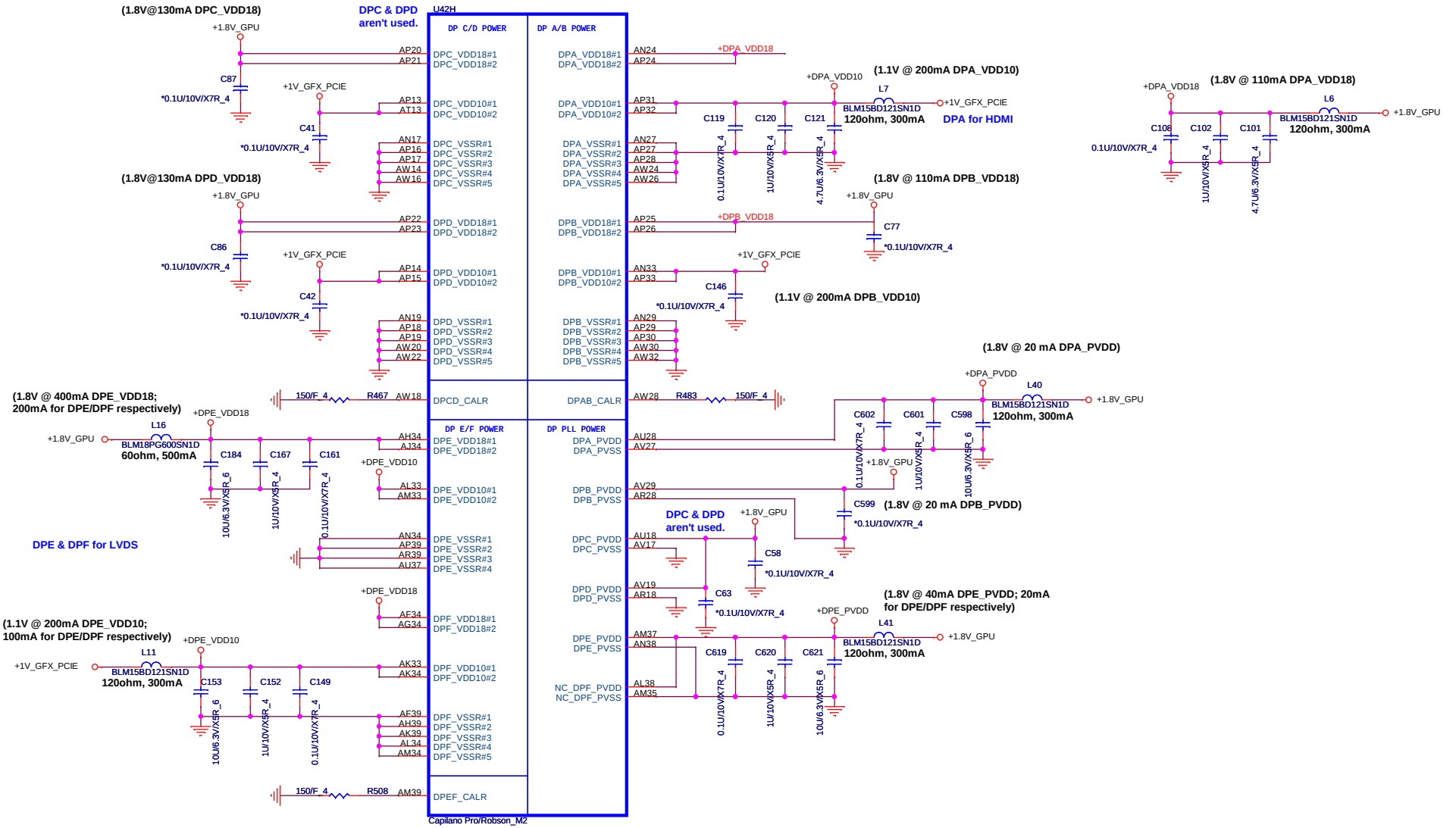
+1V_GFX_PCIE
+1.8V_GPU

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V



Size: Custom	Document Number: Madison_DP_POWER		Rev: 1A
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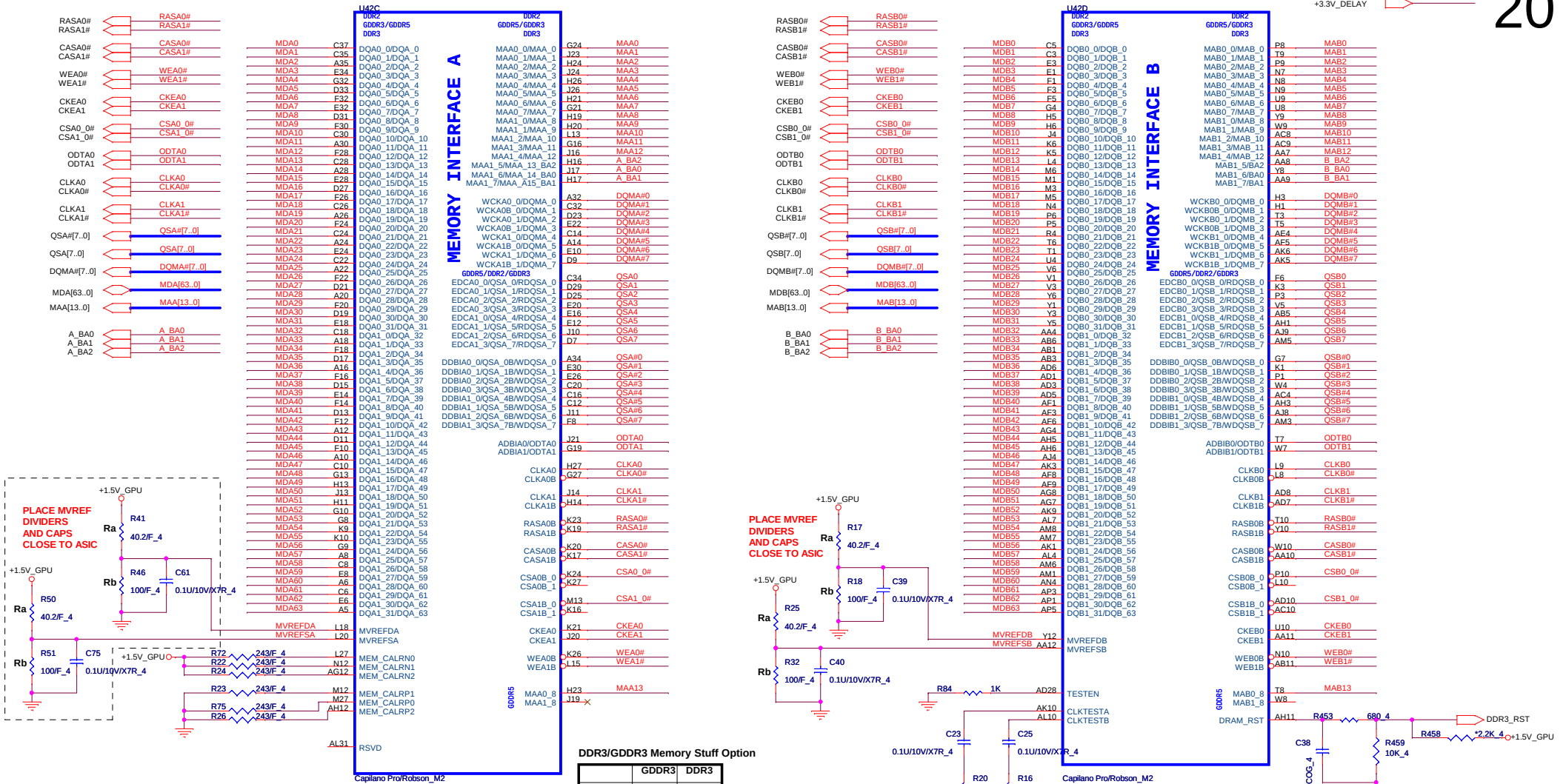
Quanta Computer Inc.

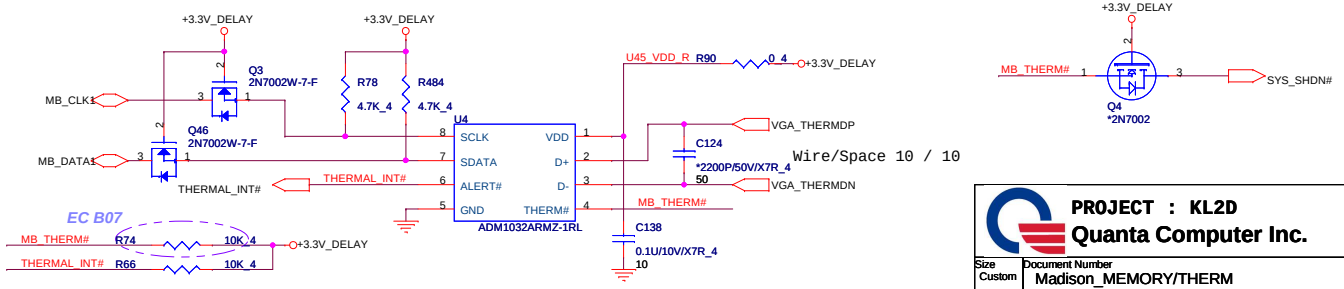


MVREF=VDDR1*0.7 for DDR3. Martin.

DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

THERMAL MONITOR



Wire/Space 10 / 10

PROJECT : KL2D
Quanta Computer Inc.

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Custom	Madison_MEMORY/THERM	1A

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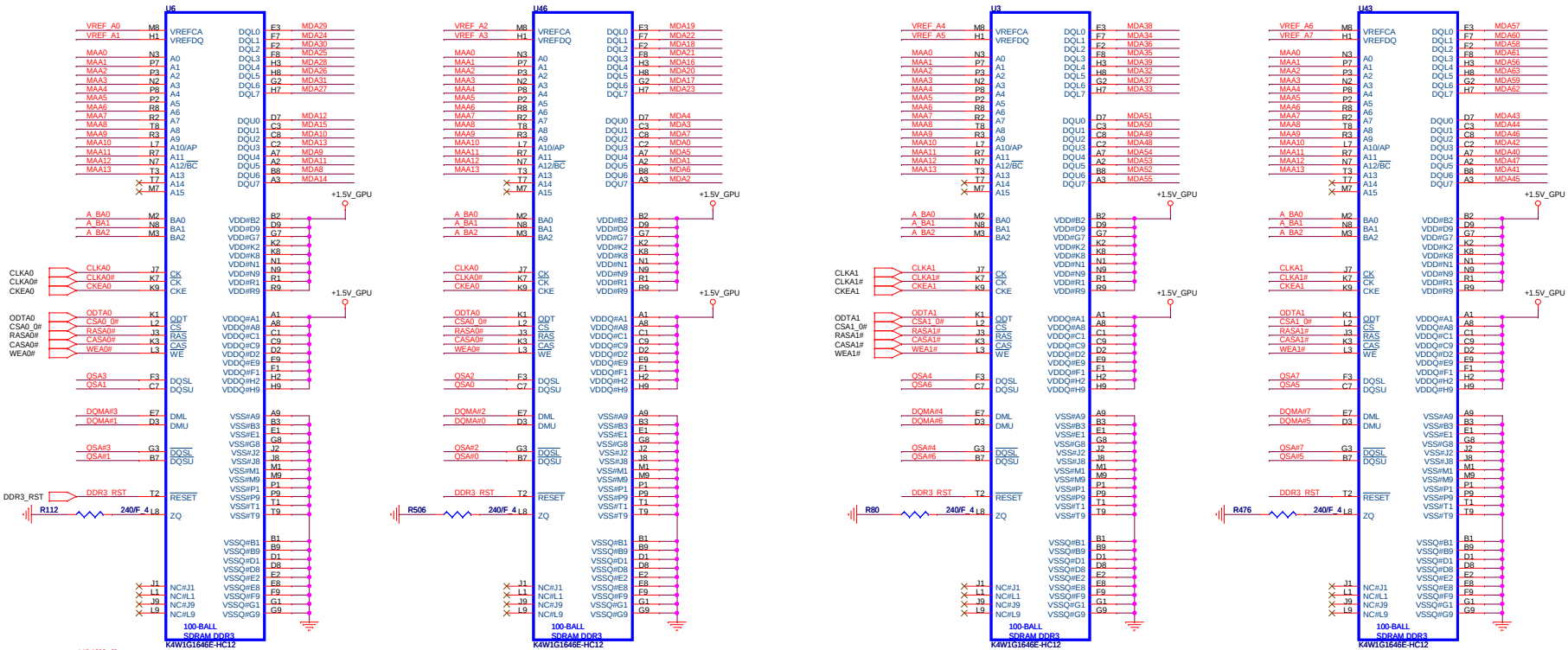
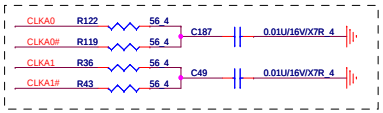
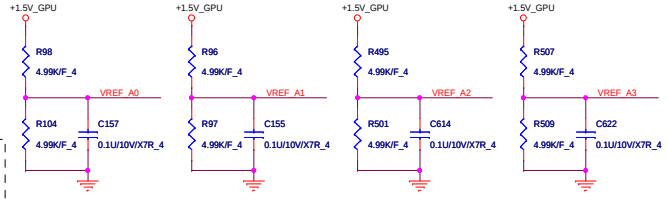
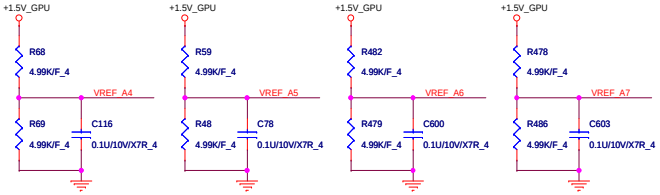
DDR3 64MX16, CH A : 512MB



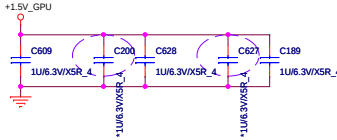
Placement has to be close to VRAM



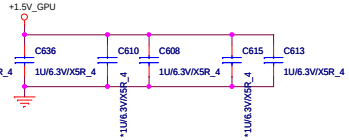




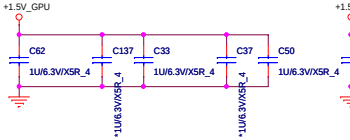
Close to U4



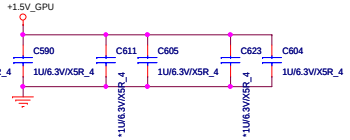
Close to U44



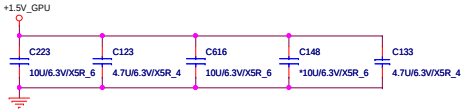
Close to U3



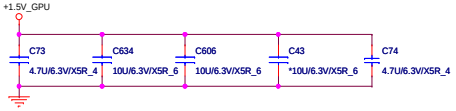
Close to U41



Close to U4 & U44



Close to U3 & U41



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Quanta Computer Inc.			
Size: C	Document Number: Madison_DDR3_A_512M		Rev: 1A
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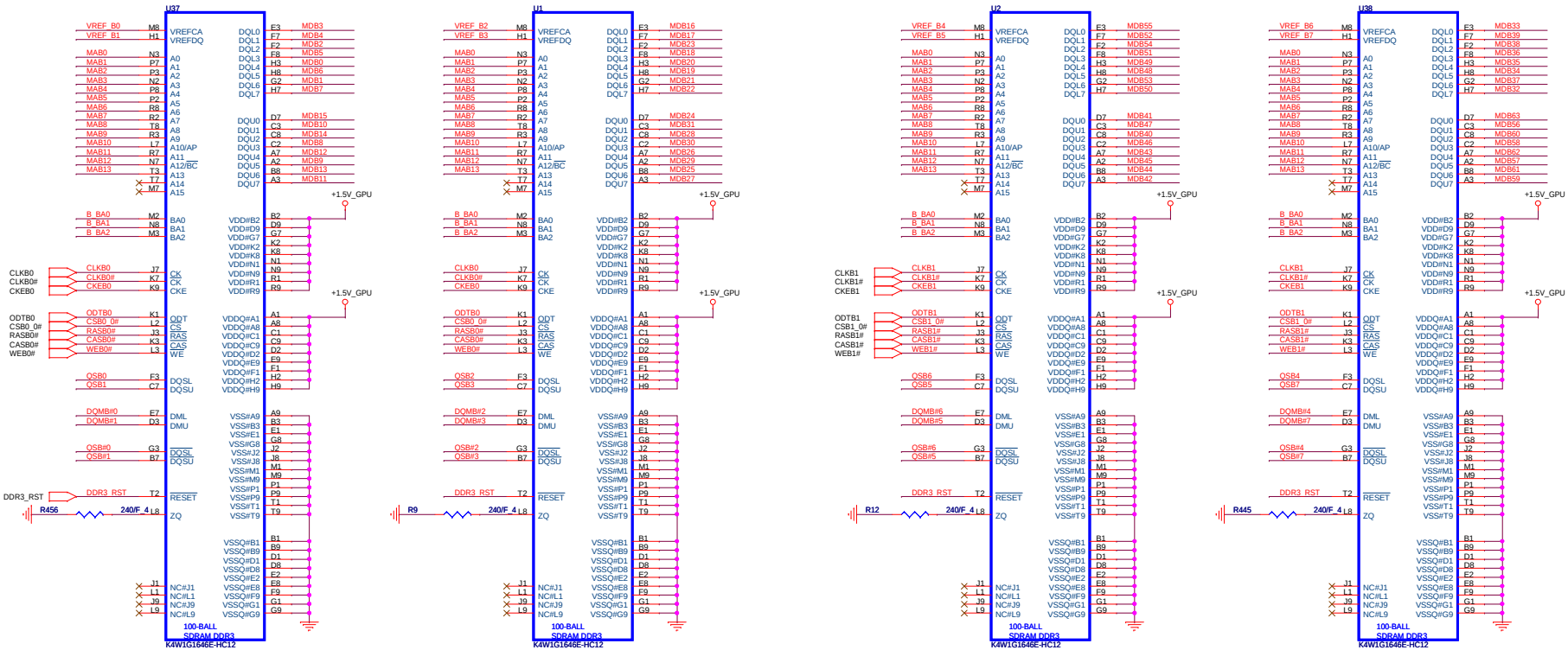
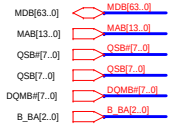
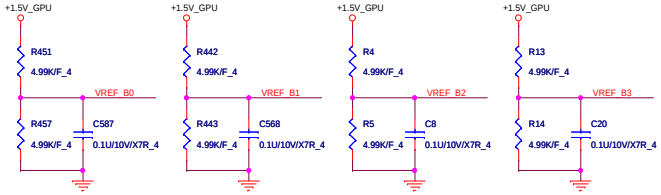
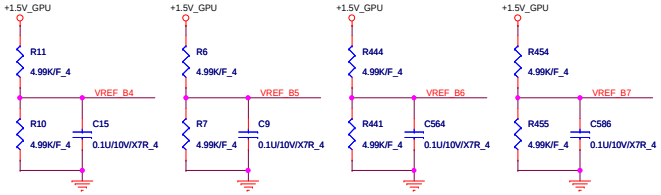
DDR3 64MX16, CH B : 512MB

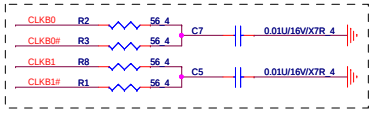




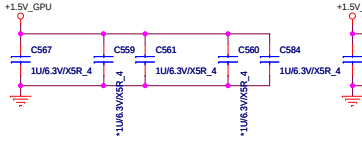




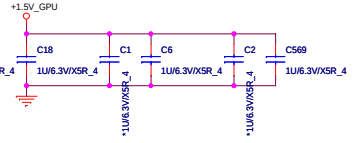
Placement has to be close to VRAM



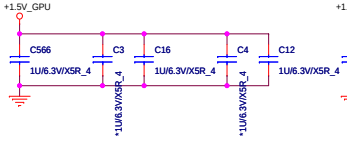
Close to U35



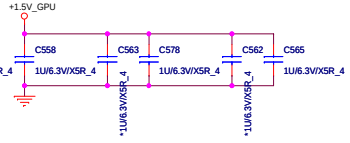
Close to U1



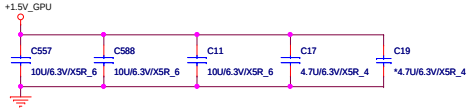
Close to U2



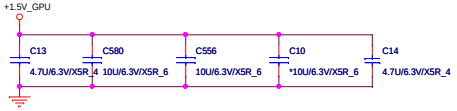
Close to U36



Close to U35 & U1



Close to U2 &U36



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
C	Madison_DDR3_B_512M	1A

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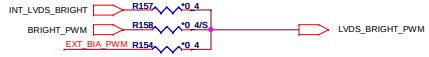
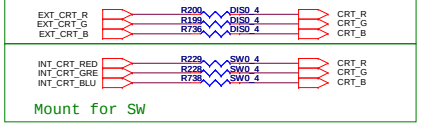


Remove MUX

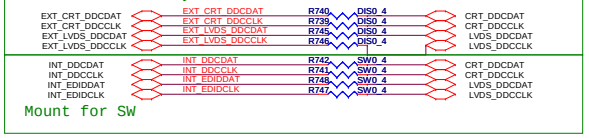
CRT

Mount for DIS only



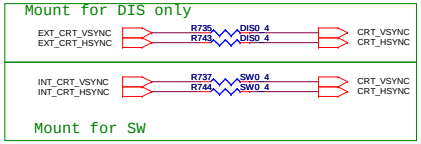
Mount for SW

Mount for DIS only

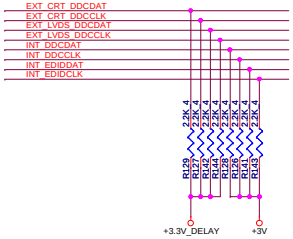


Mount for SW

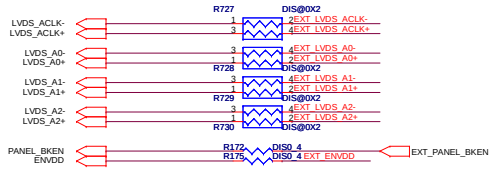
Mount for DIS only



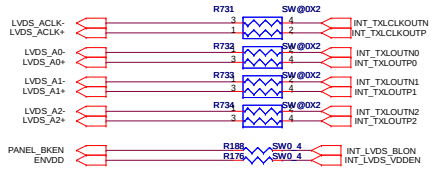
Mount for SW



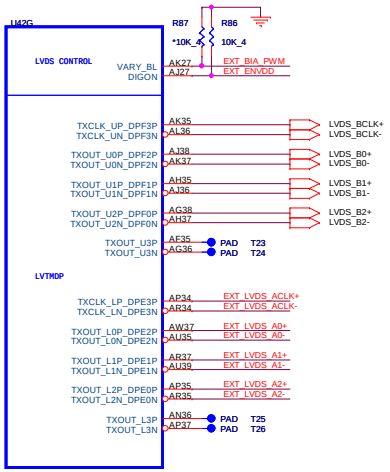
Mount for DIS only



Mount for SW



Create new page for HDMI function....By Danny 0510



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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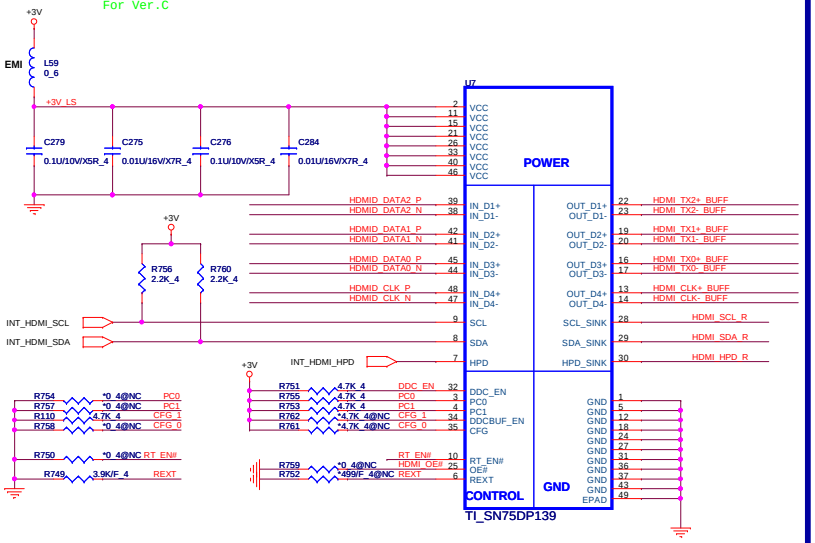
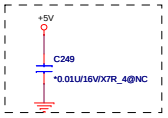
For Ver.C



EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

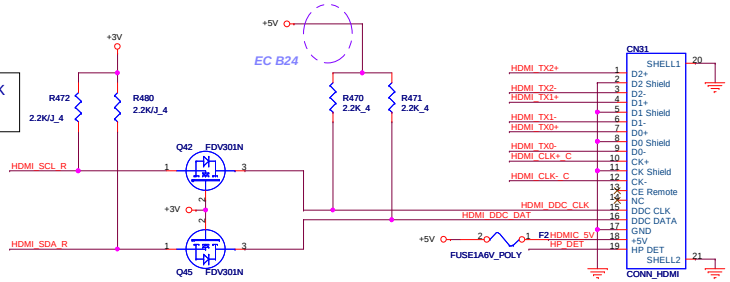
PS8101 Pin34/35 is NC

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

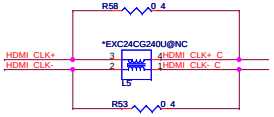


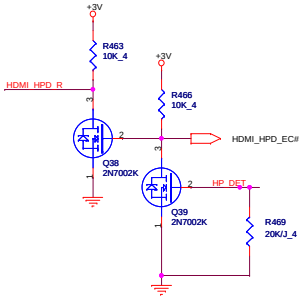
for EMI request

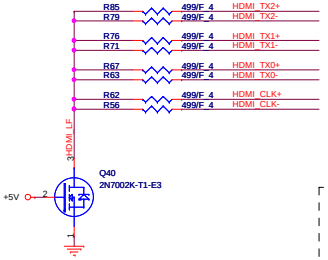
For Intel PCH request =>2.2K
ATI=>4.7K



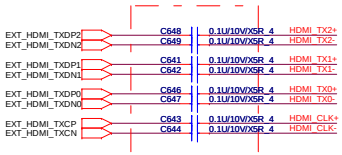
HDMI Hot-PLUG to EC and GPU

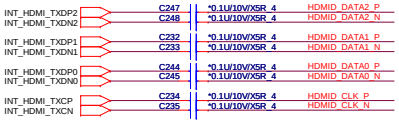


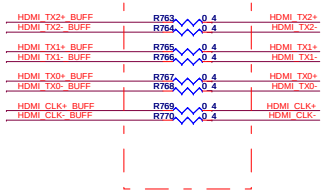




DIS/SG HDMI

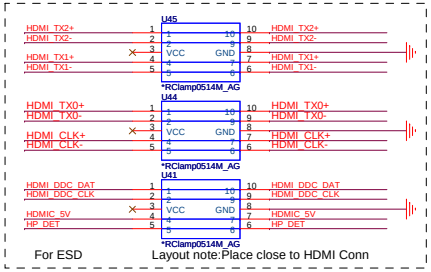






UMA Only HDMI

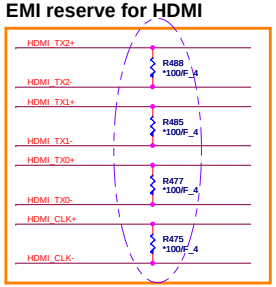
Co-lay with TOP/BOT placement.
No any trace length allow.



For ESD

Layout note:Place close to HDMI Conn

EMI reserve for HDMI



+5V
+3V
+3.3V_DELAY

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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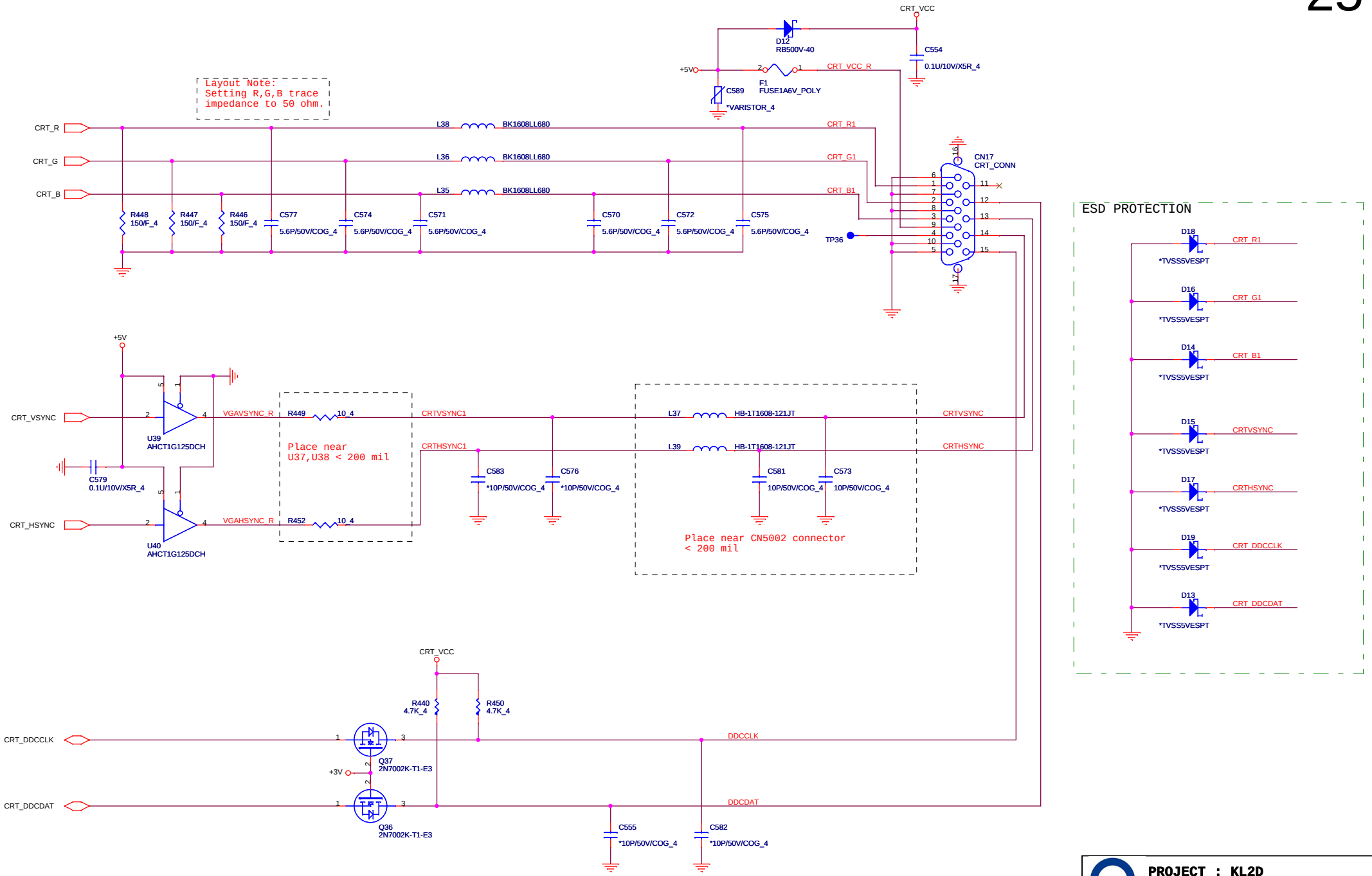
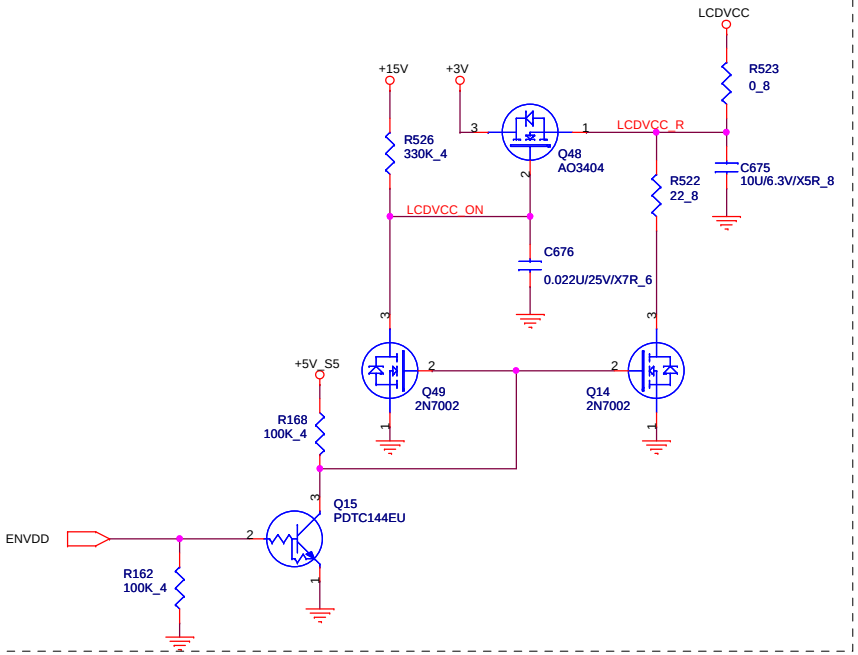
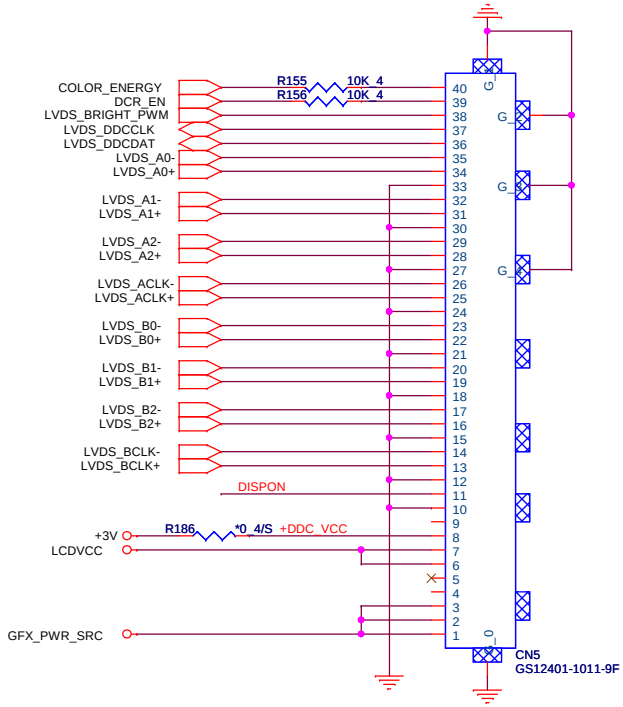
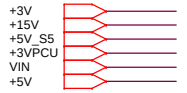


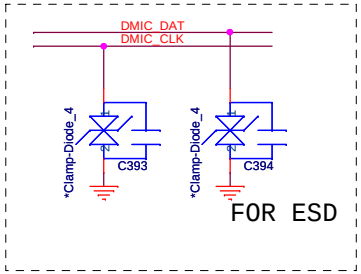
PROJECT : KL2D		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT CONN	Rev: 1A
Date: Thursday, September 30, 2010	Sheet 25 of 48	

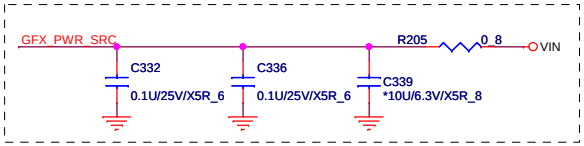
LCDVCC



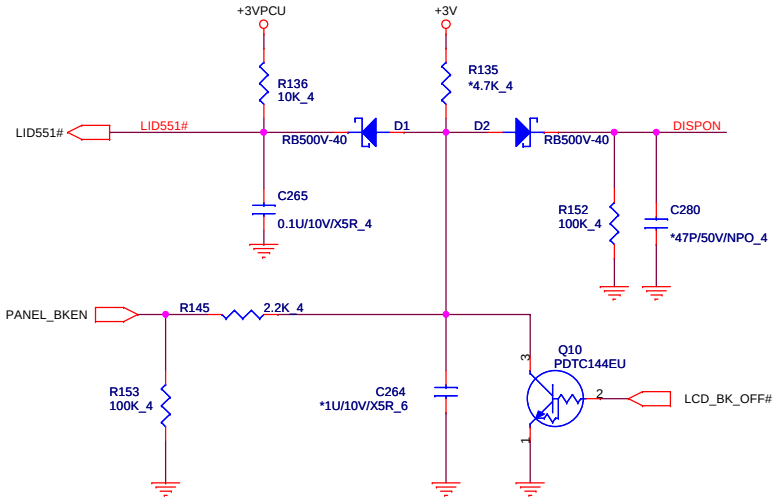


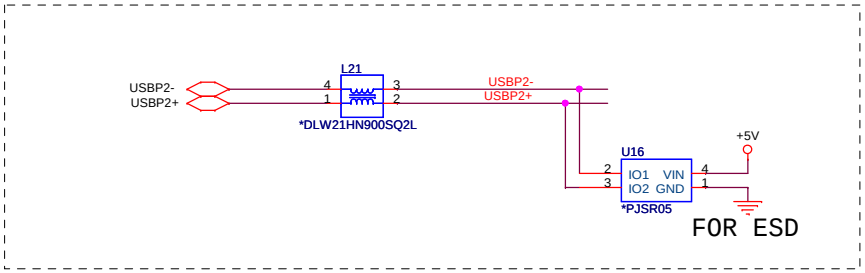




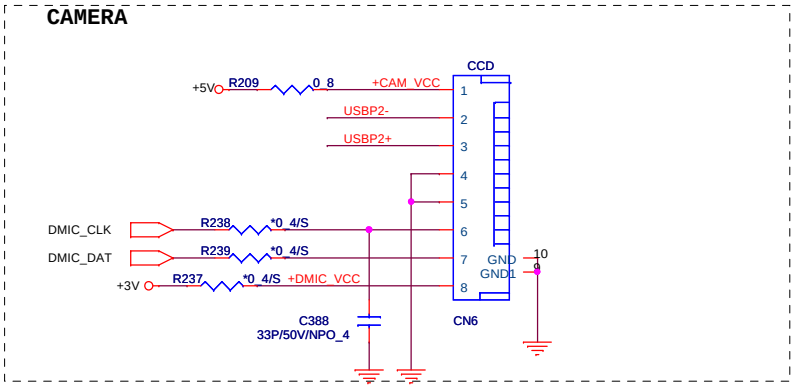


back light





CAMERA



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
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Core Power Decoupling

VDDIO Power Decoupling

U22

BCM57780

7mm x 7mm

48-Pin QFN

Package Body

Transformer

U19 LFE9292A-R

U21 *CM1293A-04SO

U18 *CM1293A-04SO

RJ45 Connector

CN22 JM36113-N4525-7F

3.3V LANVCC

Q23 AO6402

Q24 PDTC144EU

Q25 PDTC144EU

U23 *74AHCT1G08GW

U24 *M24C02-WMN6TP

Rev.B change
For EXT EEPROM both pull high
For INT EEPROM = 10

3.3V Device ONLY

Rev. B Change straping.
Remove U24. Use internal ROM.

PROJECT :	KL2D
Quanta Computer Inc.	
Size: Custom	Document Number: LAN (BCM57780, RJ45)
Rev: 1A	
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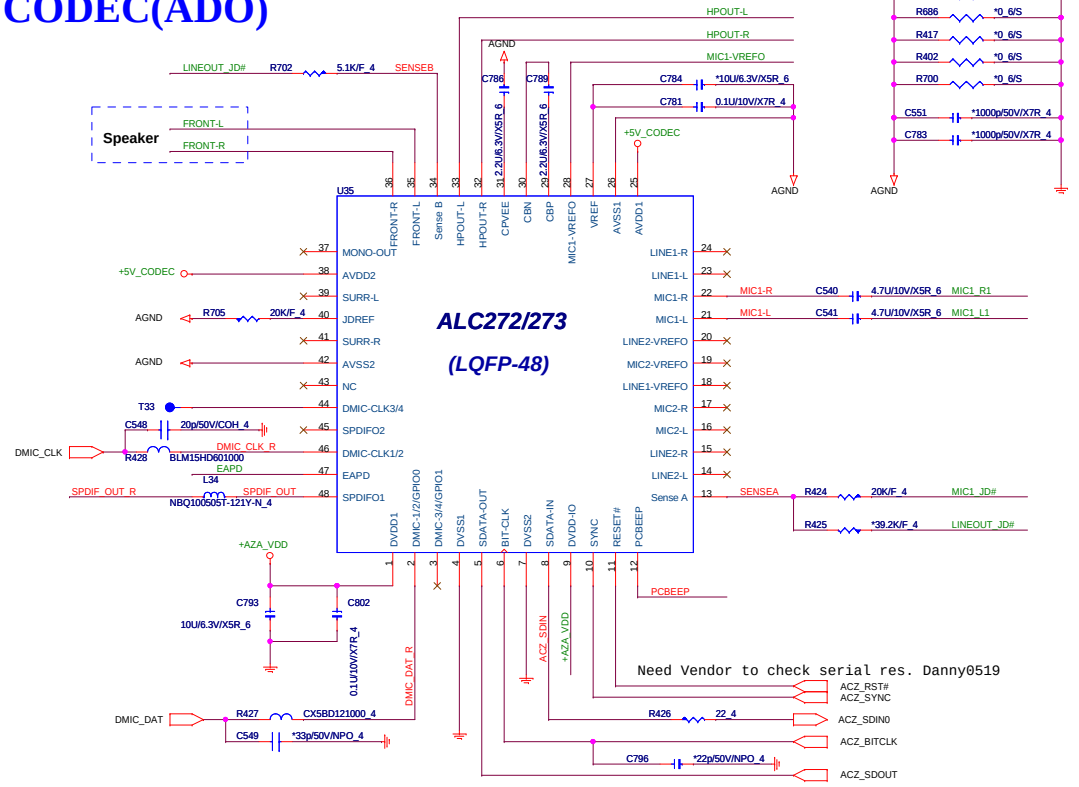
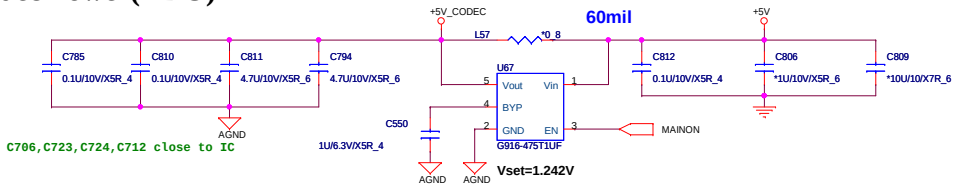
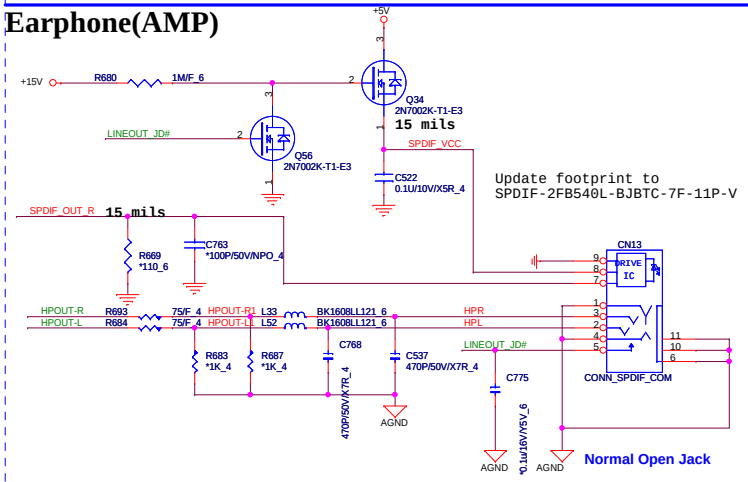
CODEC(ADO)



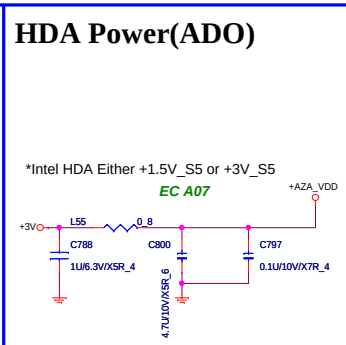
Codec Power(ADO)



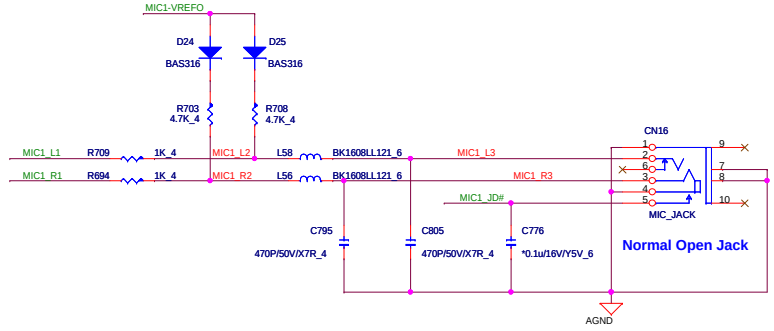
Earphone(AMP)



HDA Power(ADO)

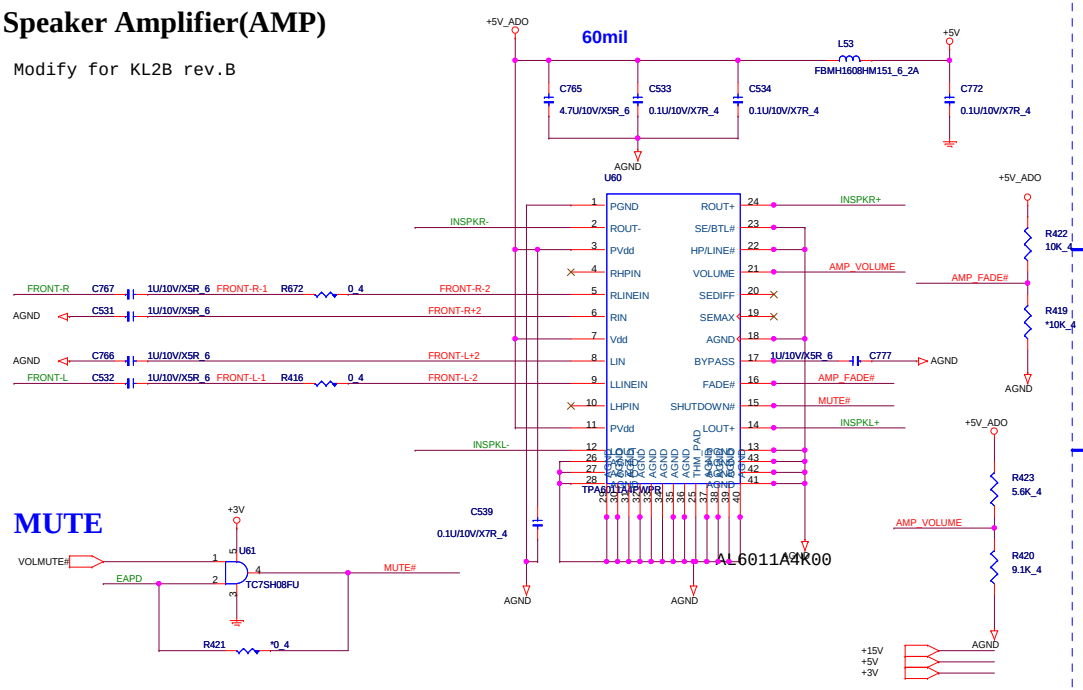


System MIC(AMP)



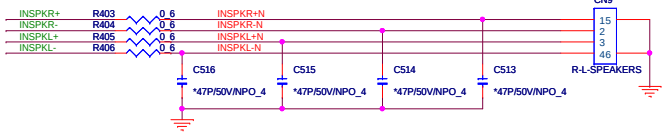
Speaker Amplifier(AMP)

Modify for KL2B rev.B

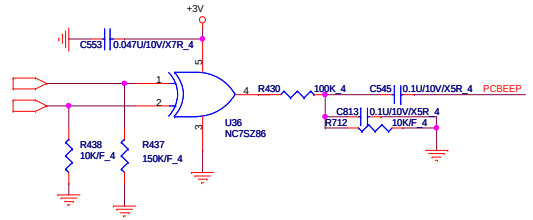


MUTE

Speaker(AMP)



PC BEEP



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AL272/AMP/MIC/LINE-OUT	1A

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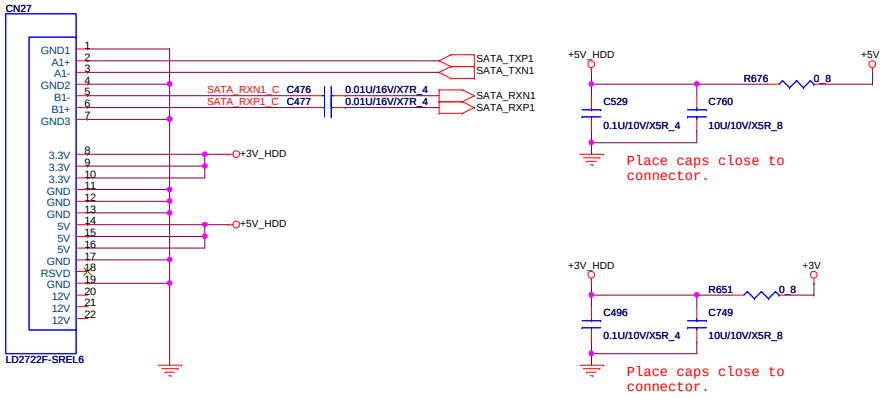
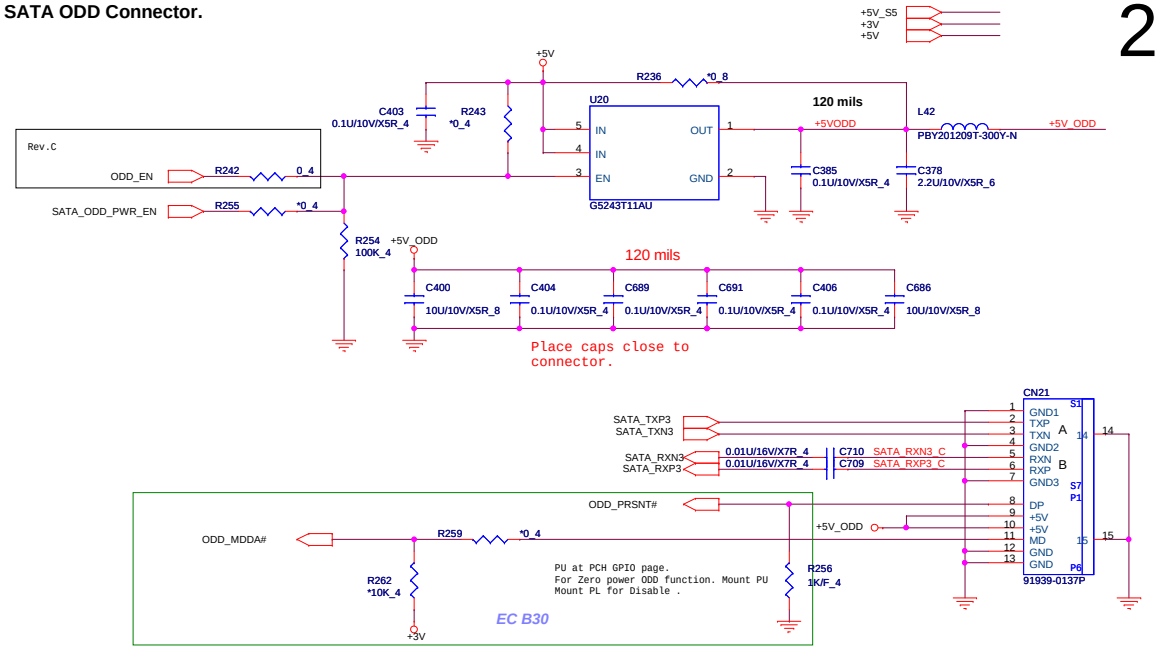
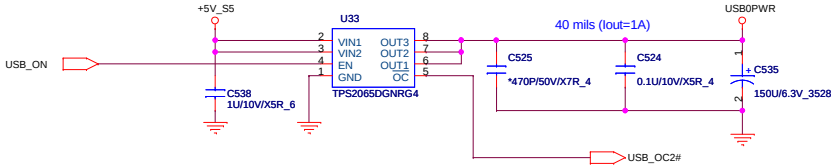
SATA HDD Connector.

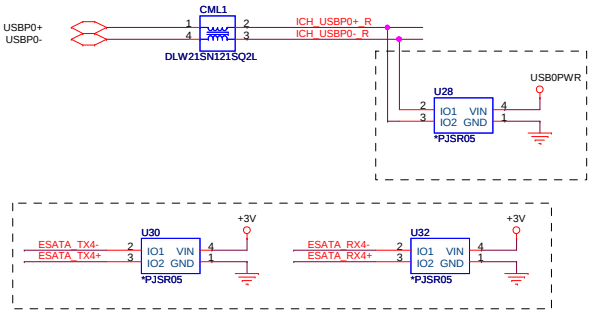


SATA ODD Connector.

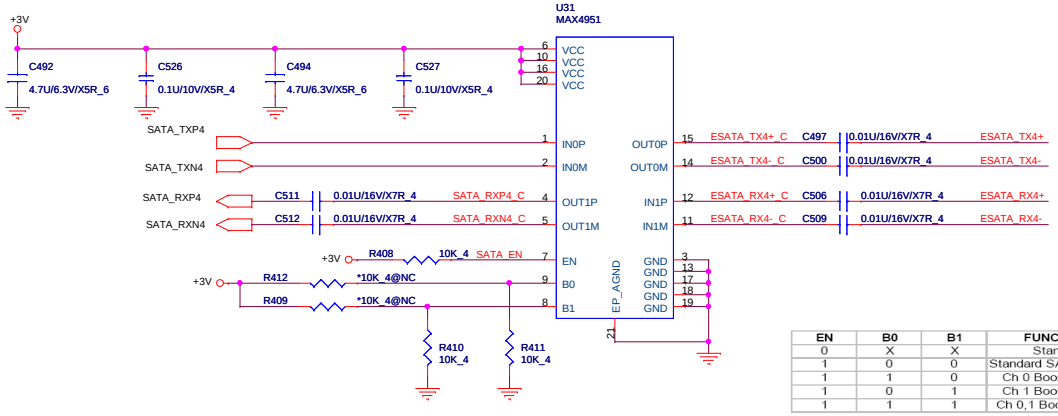


USB + E-SATA

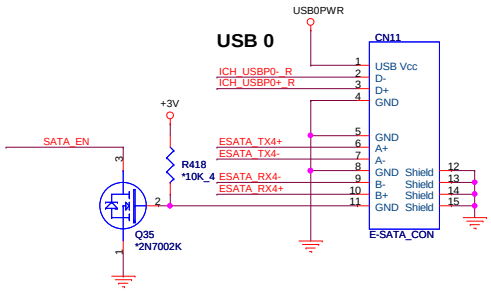




E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

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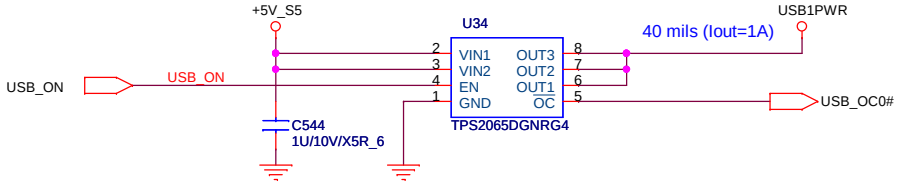
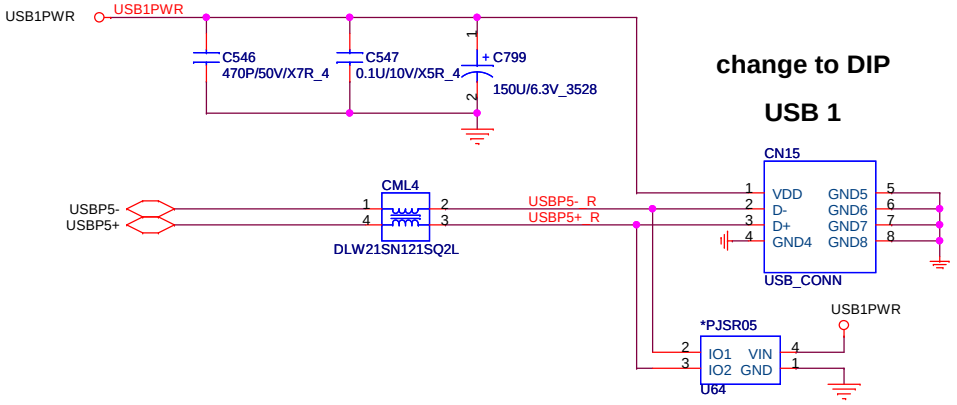
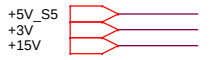
USBX3

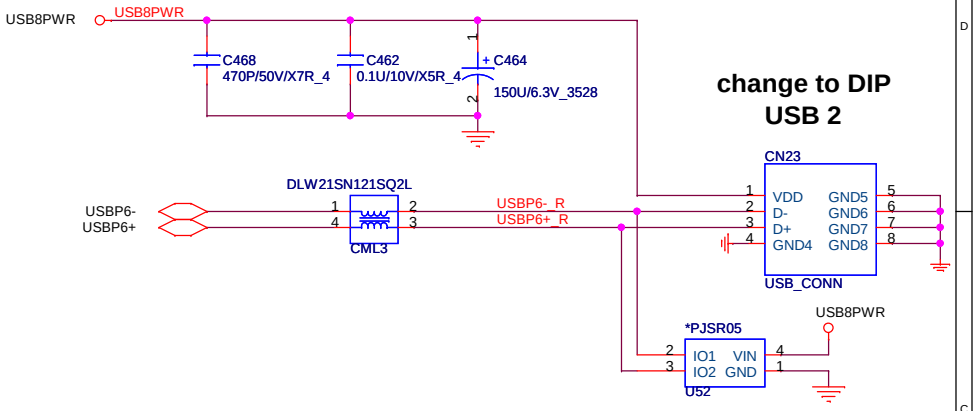


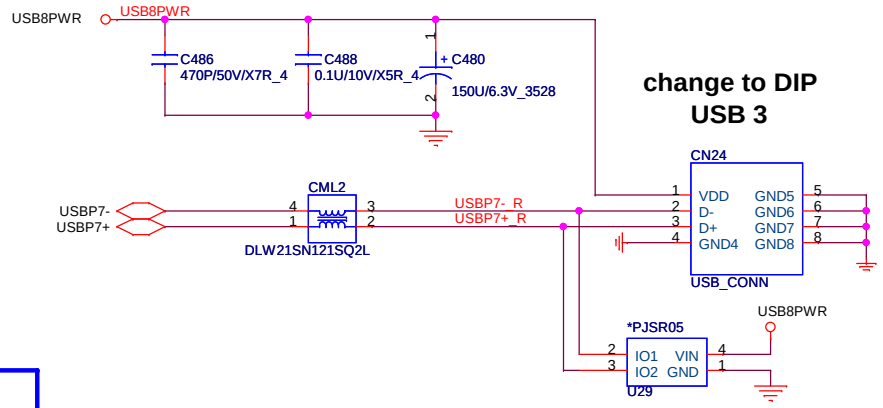


USB 1

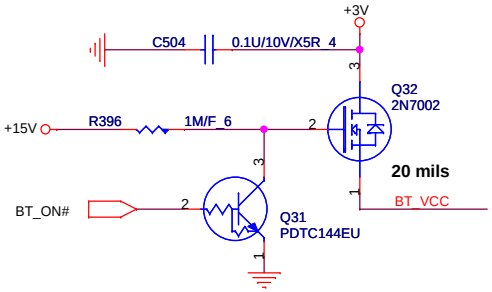


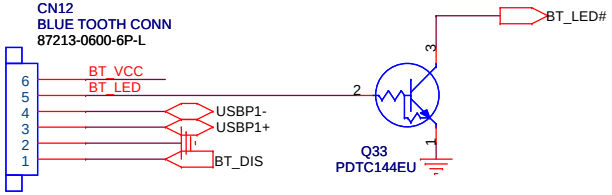
29

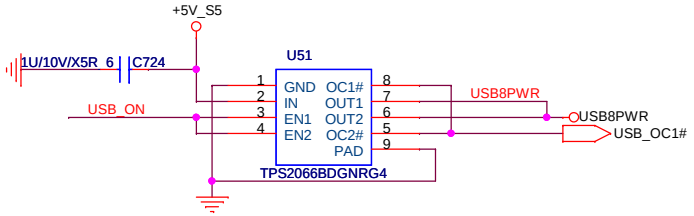




BLUETOOTH







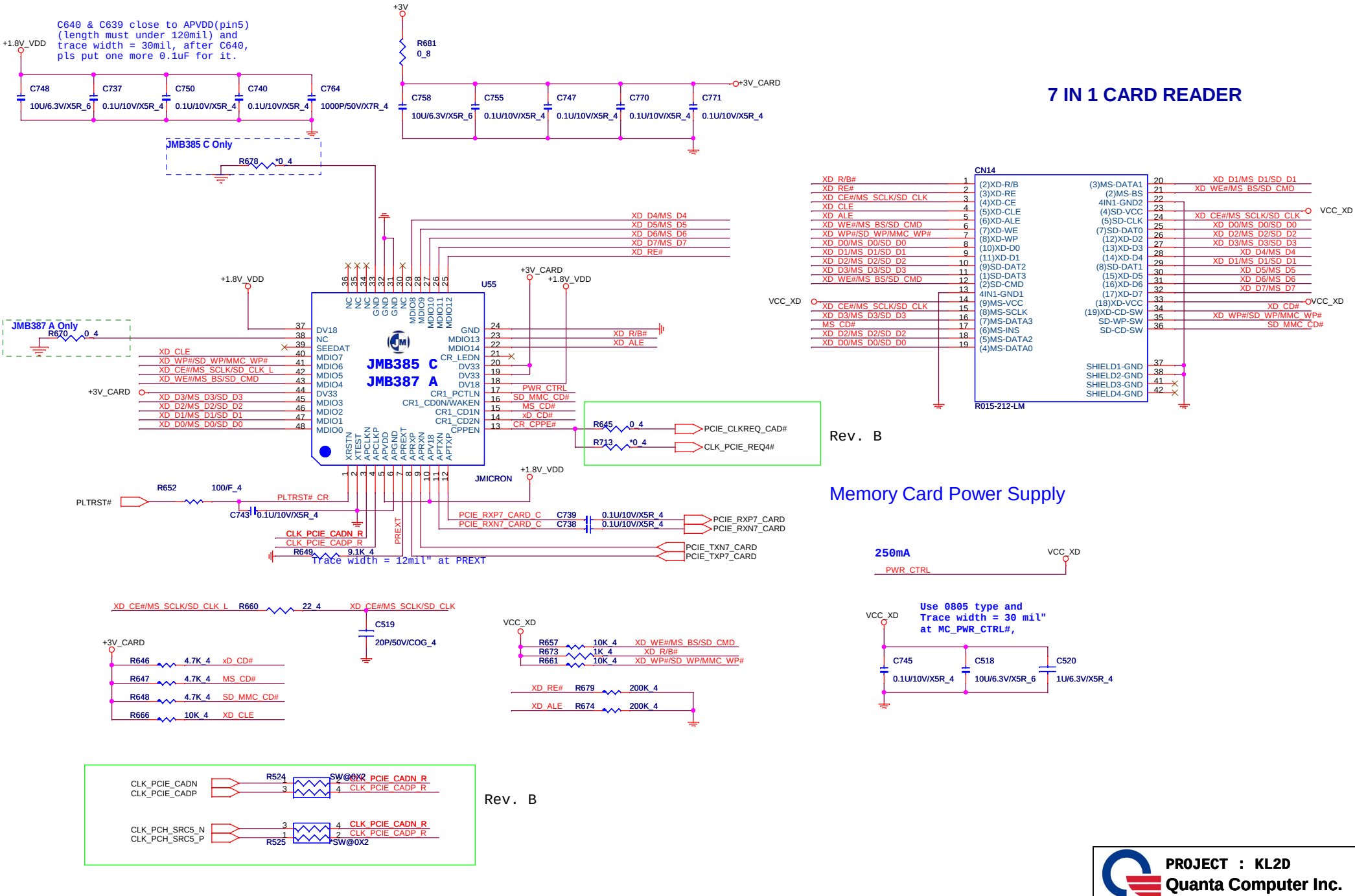
PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB X3/BT	1A

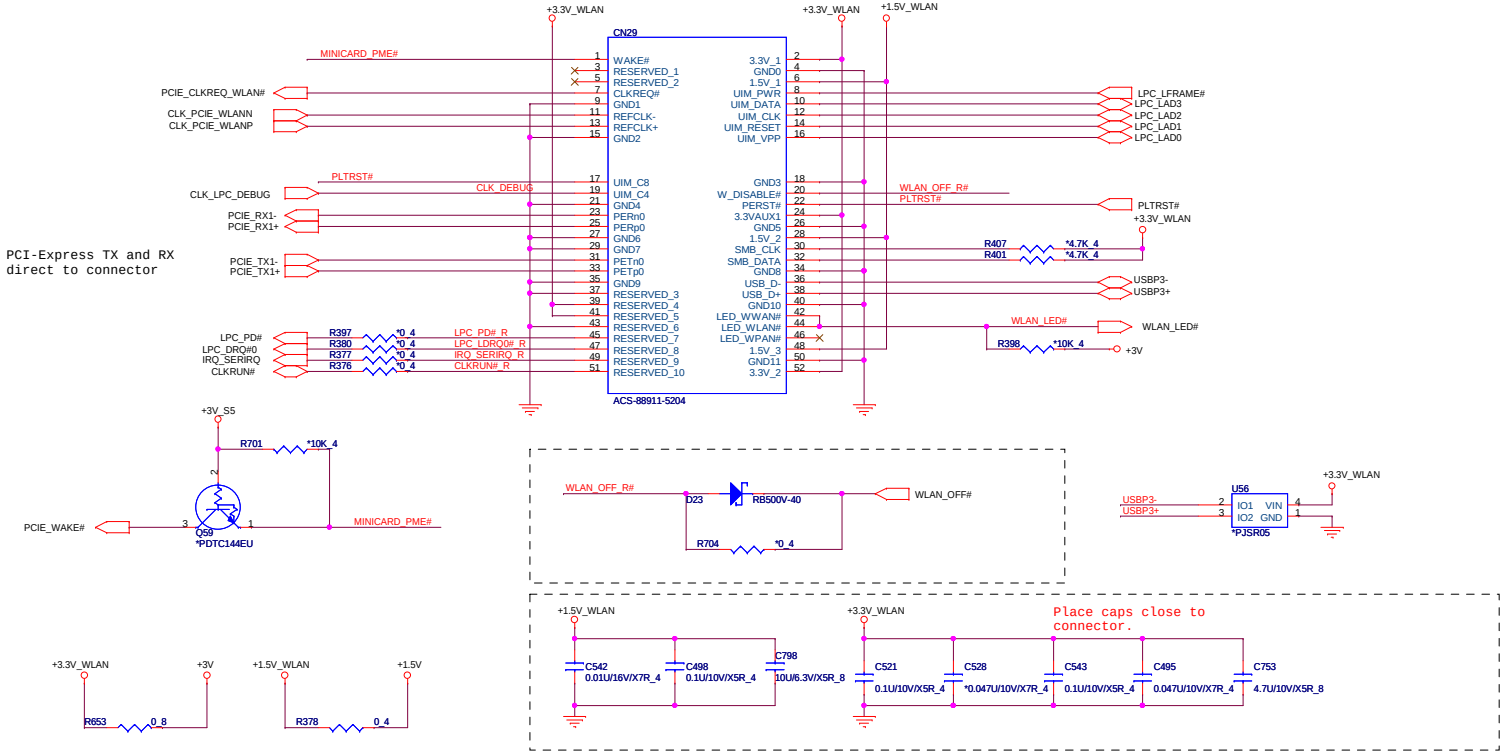
Date: Thursday, September 30, 2010 Sheet 30 of 48

7 IN 1 CARD READER

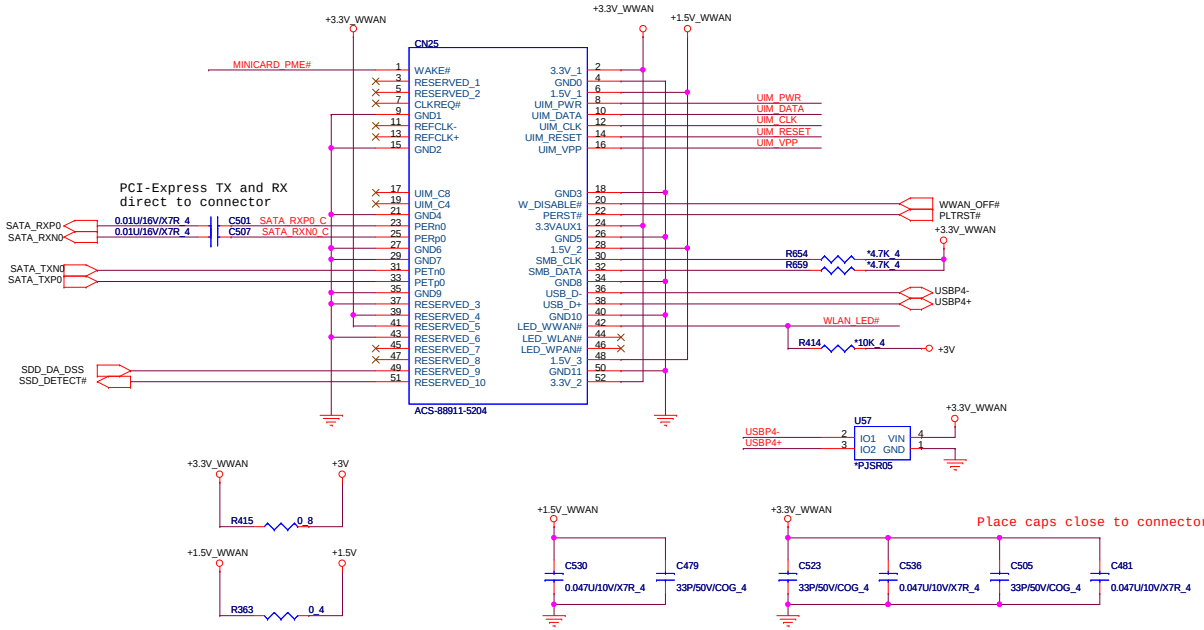


PROJECT :	KL2D
Quanta Computer Inc.	
Size: Custom	Document Number: JMB385/387 Card Reader
Rev: 1A	
Date: Thursday, September 30, 2010	Sheet 31 of 48

MiniCard WLA connector



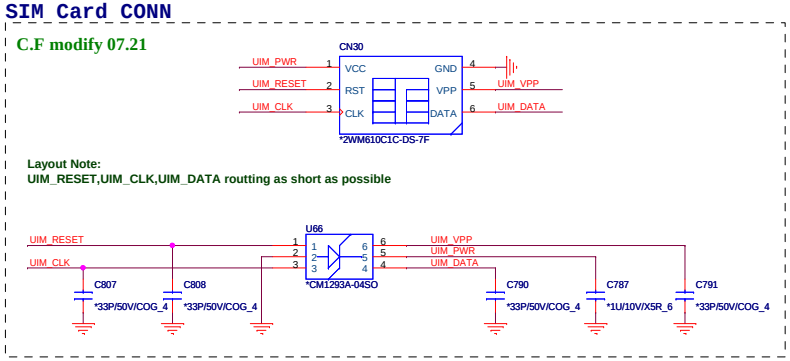
MiniCard WWAN/SATA SSD connector



SIM Card CONN

SIM Card CONN

C.F modify 07.21



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (WLAN/WWAN)	1A

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FAN CONTROL

33

+3V
+5V

NOTE:
Place C625 near Q37

NOTE:
Place C623 near Q38

NOTE:
Place C624 near U48

NOTE:
Place C627 near Q39

NOTE:
Place C626 near U48

Q9
SST3904
C228
*100P/50V/X7R_4
DDR3

Q51
SST3904
C699
*100P/50V/X7R_4
WLAN-ONFI

C331
2200P/50V/X7R_4

R180
2.05K_4

+5V
R529
0_8
+5V_FAN
C683
1U/10V/X5R_6
C685
0.1U/10V/X5R_4

+3V
R203 10K_4
R210 10K_4
R217 10K_4
R201 10K_4
R193 10K_4
R196 10K_4

+5V
R194
10K_4

R181
6.8K/F_4

U13
EMC2103-2
DN
DP
VDD
GPIO1
DP2/DN3
DN2/DP3
TRIP_SET
SHDN_SEL
GND
PWM
TACH
SMCLK
GPIO2
ALERT#
SYS_SHDN#
SMDATA

C687
*100P/50V/X7R_4
Q50
SST3904
CPU

C335
2200P/50V/X7R_4

+3V
R198
22_4
+3V_FAN
C338
0.1U/10V/X5R_4

D3
RB500V-40
+5V_FAN
FANSIG
FAN_PWM

CN20
FAN_CON

C816
C815
*/EMI_0.1U/10V/X5R_4
*/EMI_0.1U/10V/X5R_4

Q18
2N7002
MB_CLK1

Q20
2N7002
MB_DATA1

Q21
2N7002
SYS_SHDN-1#
SYS_SHDN#

D4
*RB500V-40
TEMP_FAIL

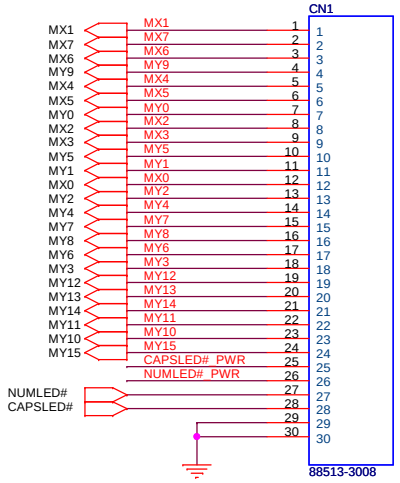
MB_ALRET#
R204
*0_4
TEMP_ALERT#

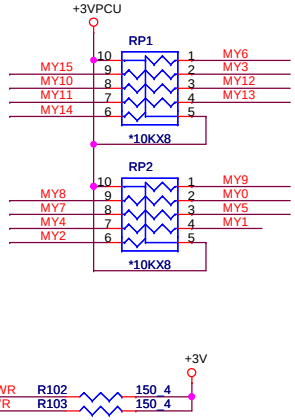
PROJECT : KL2D
Quanta Computer Inc.

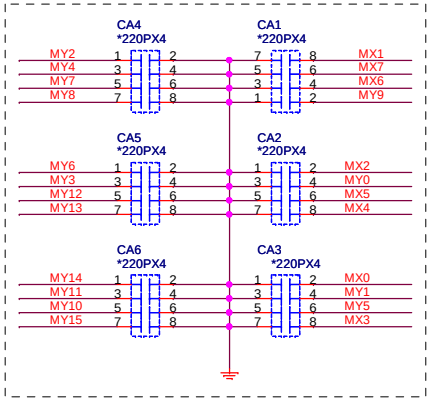
Size	Document Number	Rev
Custom	FAN /THERMAL	1A

Date: Thursday, September 30, 2010 Sheet 33 of 48

KEYBOARD

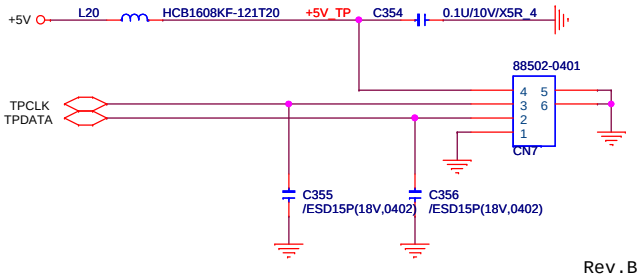






For EMI request

Touch pad



Rev.B

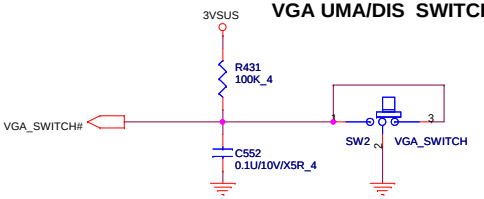
09/07 ESD request
CYAVLC18B02 for C355, C356

Backlight Keybaord Con.

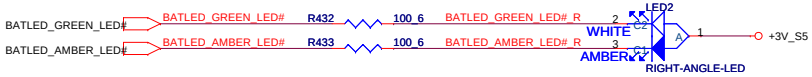
Remove KB LED Schematic
Danny0513

PROJECT : KL2D		
Quanta Computer Inc.		
Size: Custom	Document Number: K/B, T/P	Rev: 1A
Date: Thursday, September 30, 2010	Sheet 34 of 48	

VGA UMA/DIS SWITCH

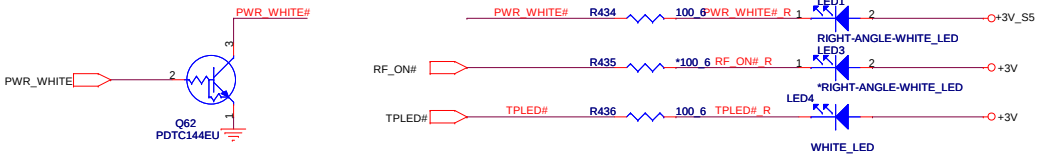


VGA



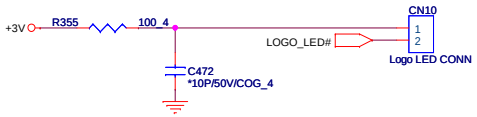
Battery

Power/suspend LED



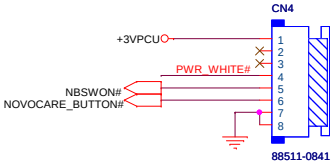
RF

TP

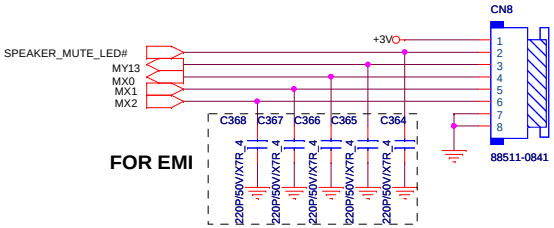


Logo LED CONN

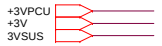
LEFT POWER BOARD



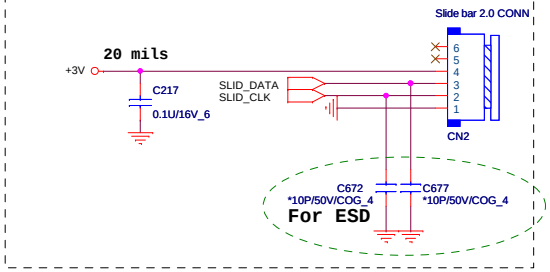
RIGHT VOLUME BOARD



FOR EMI



Slide bar 2.0



UP LED BOARD

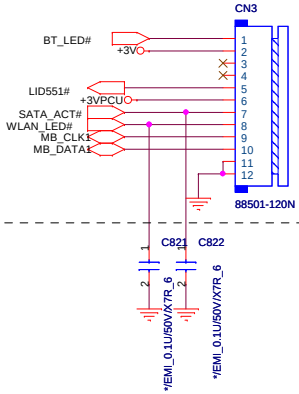
BT

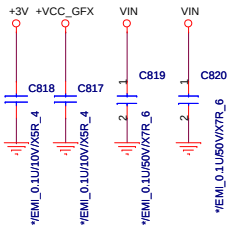
LID SWITCH

HDD

WLAN

LIGHT SENSOR





IT8518
IT8519

RF ON/OFF SWITCH

3VSUS, R707 100K_4, RF_SW#, SW1 RF_SLIDE_SWITCH, C803 0.1U/10V/X5R_4

POWER SWITCH/ NOVO BUTTON

+3VPCU, +3.3V_EC, R400 10K_4, R325 10K_4, NBSWON#, NOVOCARE_BUTTON#, C517 0.1U/10V/X5R_4, C467 0.1U/10V/X5R_4

16Mbit (2M Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

U59 MX25L1605A, R685 10K_4, R662 10K_4, C761 0.1U/10V/X5R_4

Borad ID

+3VPCU, R332 10K_4, BORAD_ID, R327 *10K_4

DIS =>R275
UMA=>R274

Check Part number!!!

PROJECT :	KL2D
Quanta Computer Inc.	
Size: Custom	Document Number: KBC IT8512E
Rev: 1A	
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MiniCard WLAN

HOLE30 H-TC205I4BC146D146P2
HOLE33 H-TC205I4BC146D146P2

MiniCard WWAN

HOLE28 H-TC205I119BC79D79P2
HOLE31 H-TC205I119BC79D79P2

Hole for PCH support

HOLE27 H-TC205I99BC59D59P2
HOLE26 H-TC205I99BC59D59P2

Drink Hole

ESD for ESATA

Hole for CPU support

HOLE5 *h-tc236i157bc157d157pt
HOLE10 *h-tc236i157bc157d157pt
HOLE11 *h-tc236i157bc157d157pt
HOLE6 *h-tc236i157bc157d157pt

VGA nut

HOLE24 H-TC197BC157I146D126P2
HOLE25 H-TC197BC157I146D126P2

MiniCard TV

HOLE32 H-TC205I119BC79D79P2
HOLE29 H-TC205I119BC79D79P2

Boundary Hole

HOLE12 *H-C315D106P2
HOLE20 *H-C315D106P2
HOLE4 *H-TC197BC315D106P2
HOLE17 *H-C315D106P2
HOLE22 *H-C315D106P2
HOLE1 *H-C315D106P2
HOLE8 *H-C315D106P2
HOLE23 *H-C315I126D106P2
HOLE21 *H-C315D106P2
HOLE3 *H-C315D106P2

Boundary Hole

HOLE2 *H-TC197BC315D106P2
HOLE14 *H-TC197BC315D106P2
HOLE9 *H-O157X375D157X375N
HOLE19 *H-C118D118N
HOLE18 *H-C118D118N
HOLE7 *H-C1811D1811NA1851
HOLE15 *O-KL3A-1

Break Hole

Boundary Hole (ODD)

HDD PAD

ESD PAD

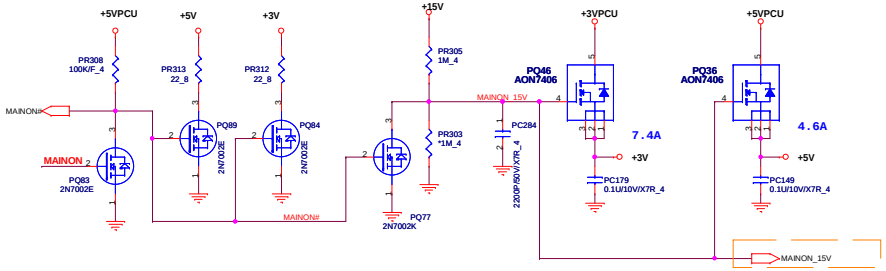
GP1 *spad-KL3A-1
GP9 *spad-KL3A-1
GP10 *spad-KL3A-2
GP11 *spad-KL3A-3
GP2 *spad-KL3A-4
GP4 *spad-KL3A-5
GP5 *spad-KL3A-6
GP3 *SPAD-KL3A-13

PROJECT KL3 NOTE Calpella DIS

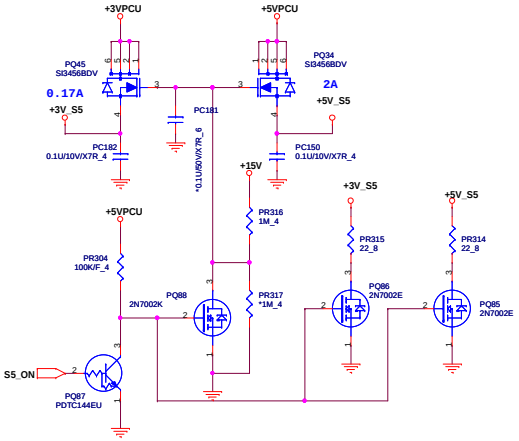
Quanta Computer Inc.

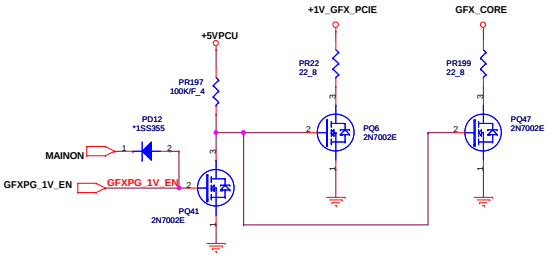
Size	Document Number	Rev
Custom	HOLD & SKEW	1A
Date: Thursday, September 30, 2010	Sheet 37 of 48	

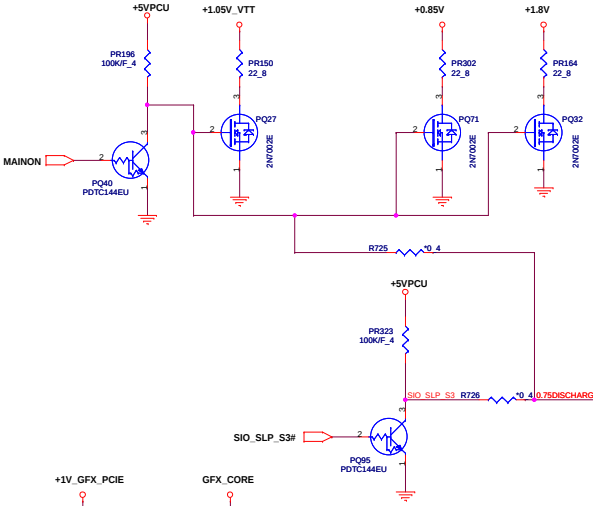
+3V, +5V

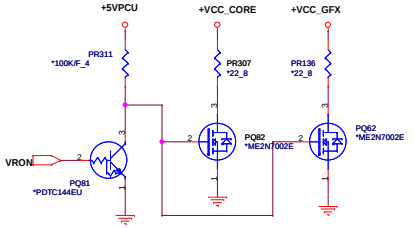


3V_S5, 5V_S5

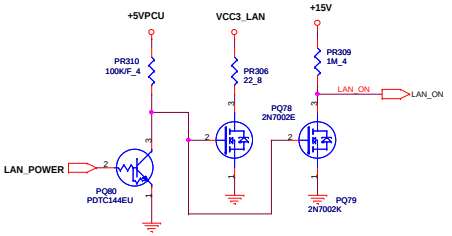




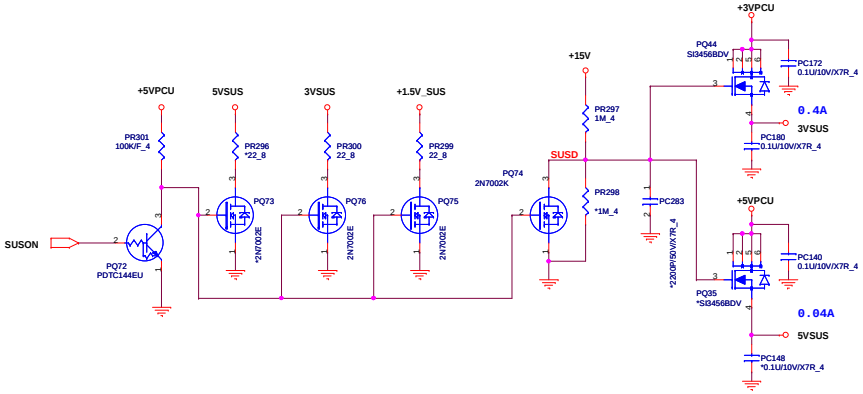


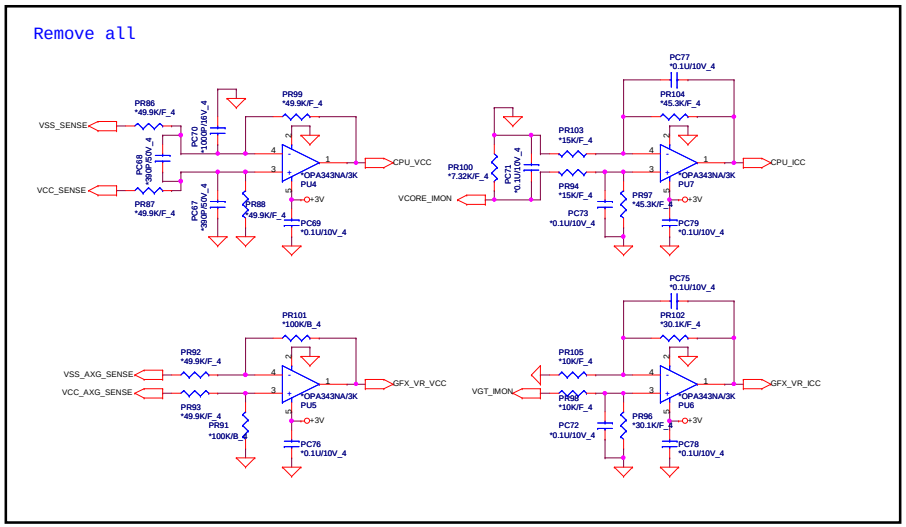


LANVCC



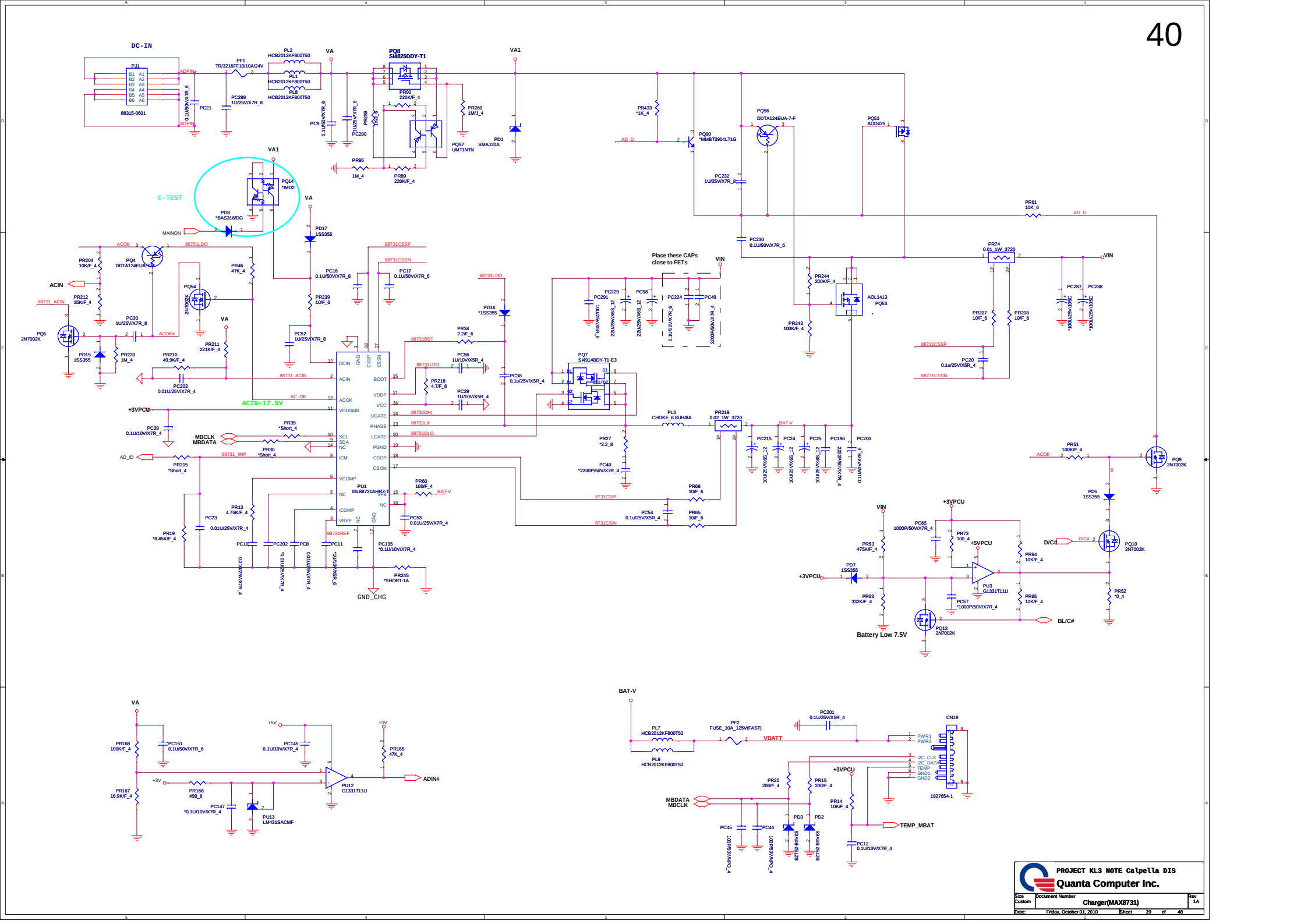
3VSUS, 5VSUS

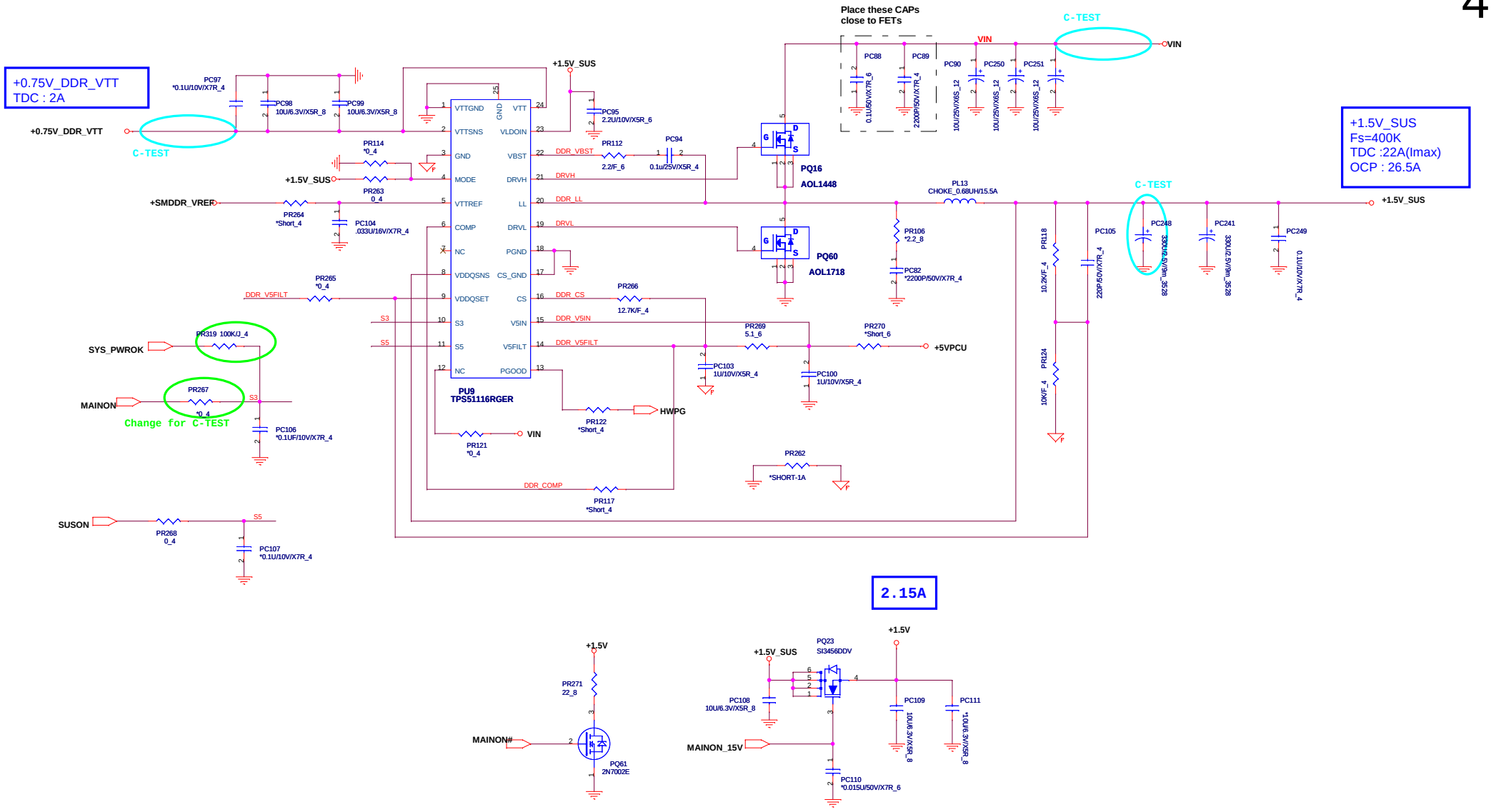


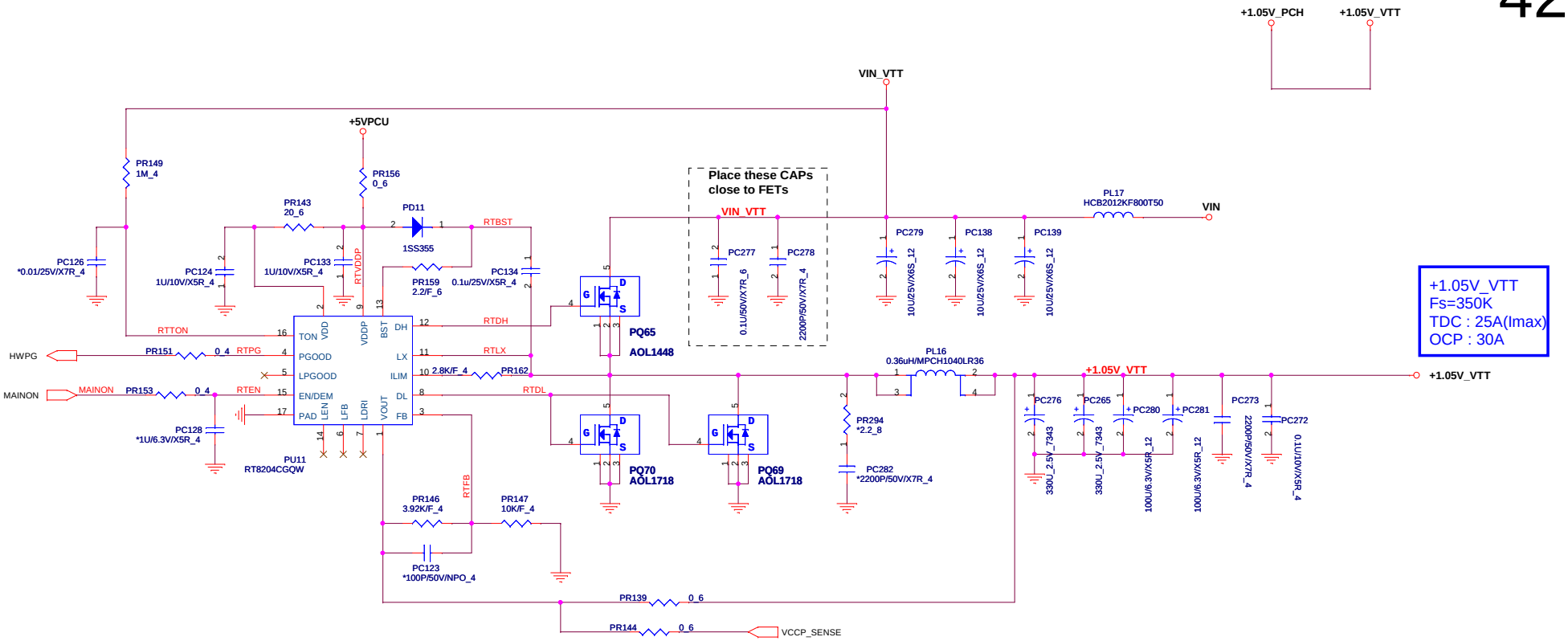


PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A
Date: Thursday, September 30, 2010	Sheet 38 of 48	


DC-IN
C-TEST
Place these CAPs close to FETs
ACIN=17.5V
Battery Low 7.5V
GND_CHG
PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.
Charger(MAX8731)
Friday, October 01, 2010


+0.75V_DDR_VTT
TDC : 2A
+1.5V_SUS
Fs=400K
TDC :22A(Imax)
OCP : 26.5A
Place these CAPs
close to FETs
C-TEST
VIN
+0.75V_DDR_VTT
+1.5V_SUS
+SMDDR_VREF
DDR_V5FILT
SYS_PWROK
MAINON
Change for C-TEST
SUSON
PU9
TPS51116RGER
PQ16
AOL1448
PQ60
AOL1718
PL13
CHOKE_0.68UH/15.5A
+5VPCU
HWPG
DDR_VBST
DDR_LL
DDR_CS
DDR_V5IN
DDR_COMP
2.15A
PQ23
SI3456DDV
PQ61
2N7002E
+1.5V
MAINON#
MAINON_15V

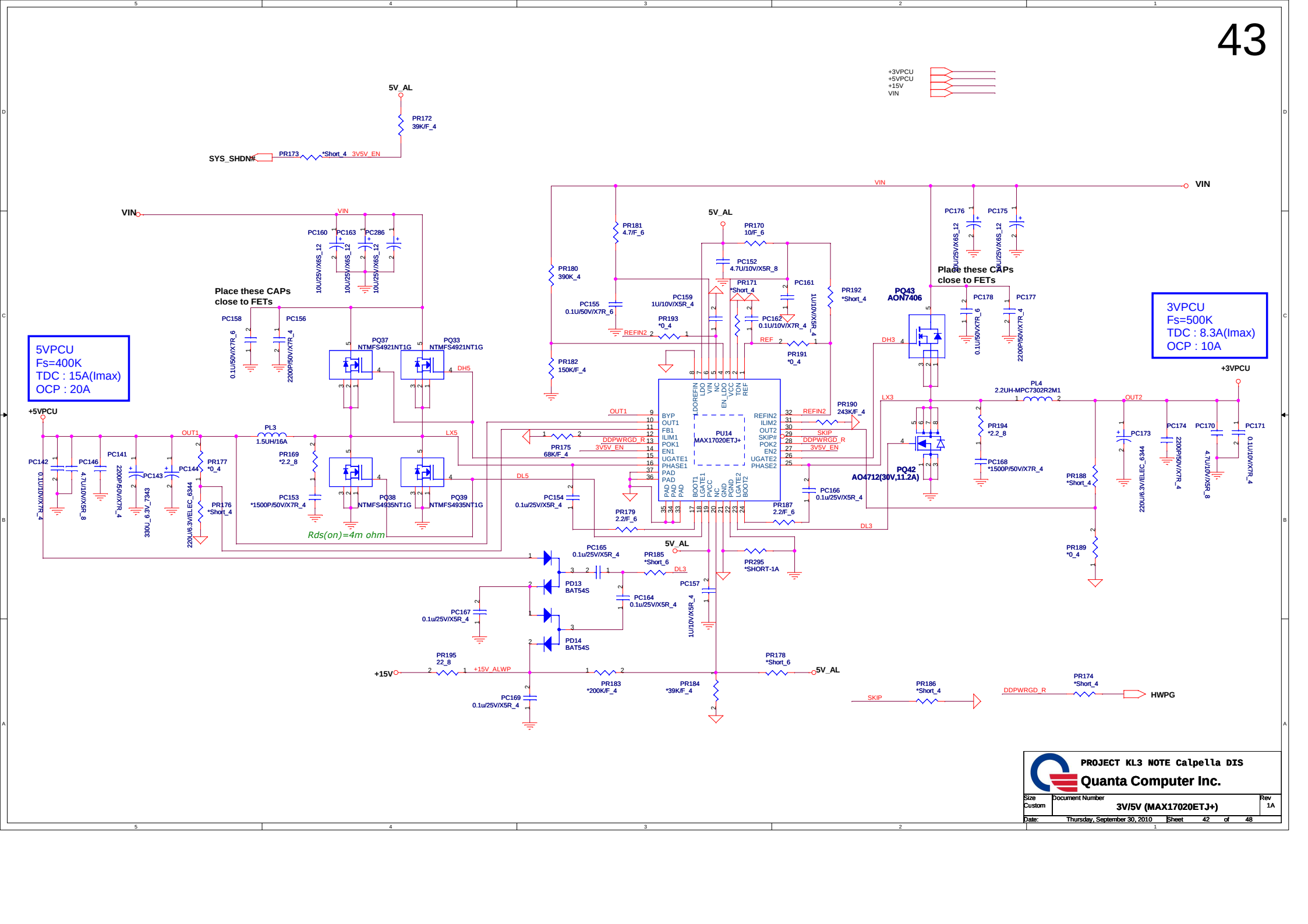


PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.1V_VTT(RT8204)	1A

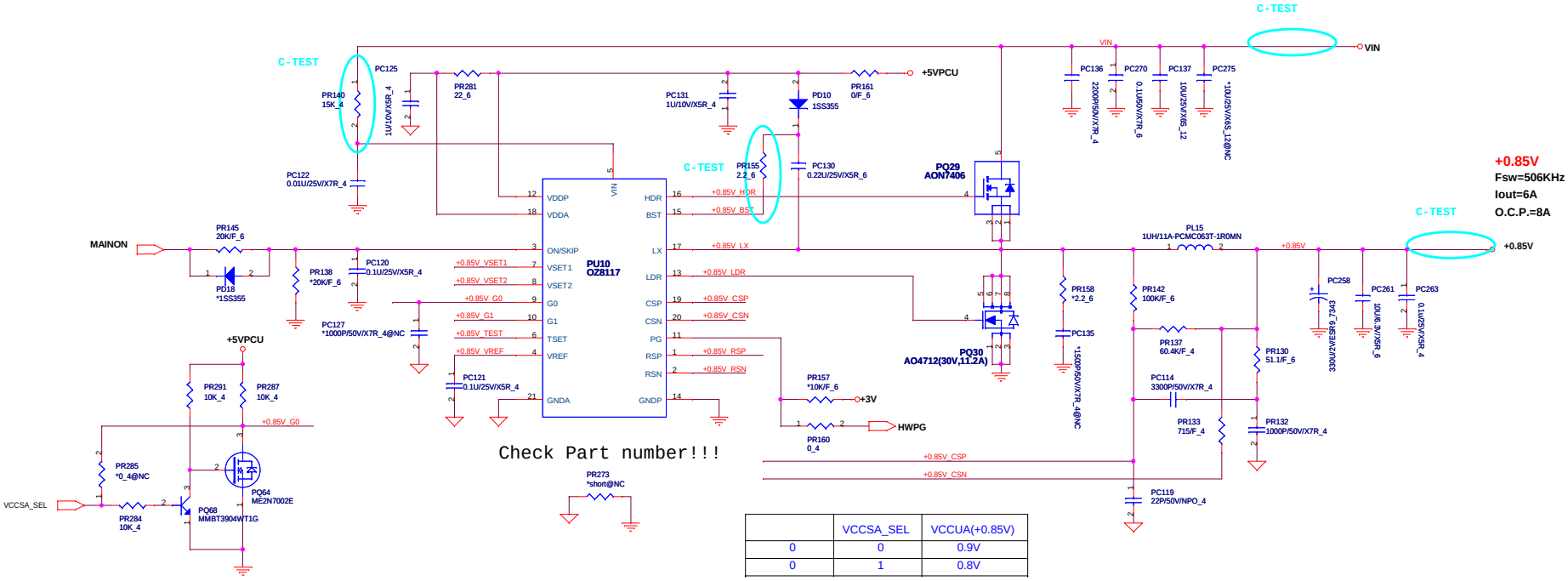
Date: Thursday, September 30, 2010 Sheet 41 of 48



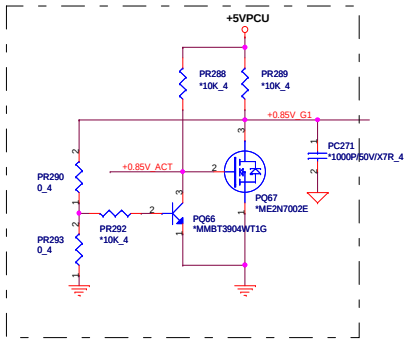
PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

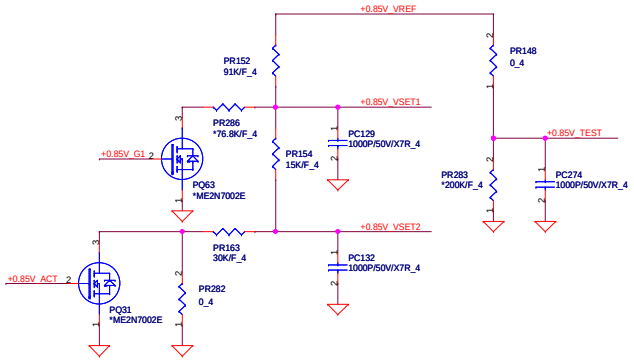
Size	Document Number	Rev
Custom	3V/5V (MAX17020ETJ+)	1A
Date: Thursday, September 30, 2010	Sheet 42 of 48	

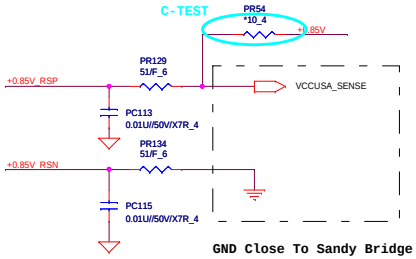


	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

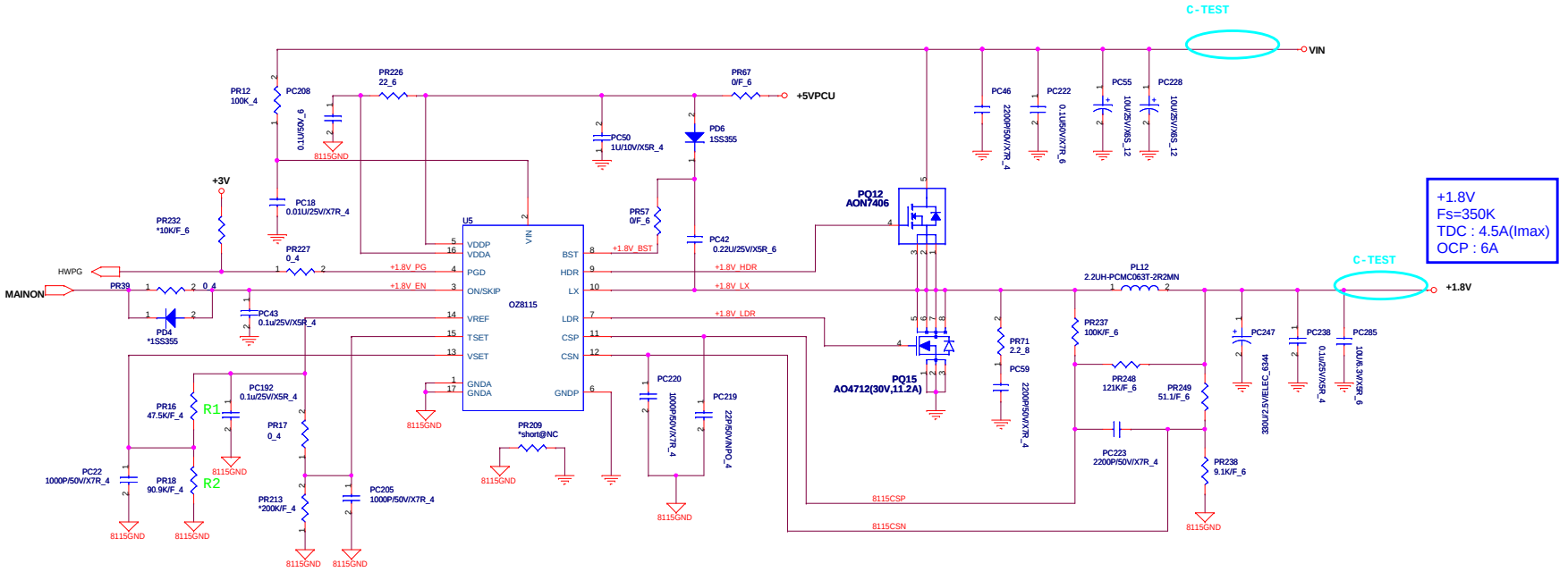


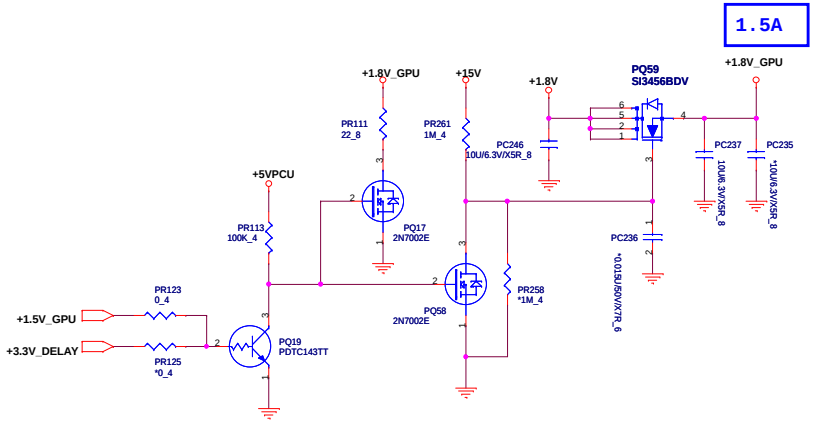
For Sandy Bridge And IV Bridge VID Select





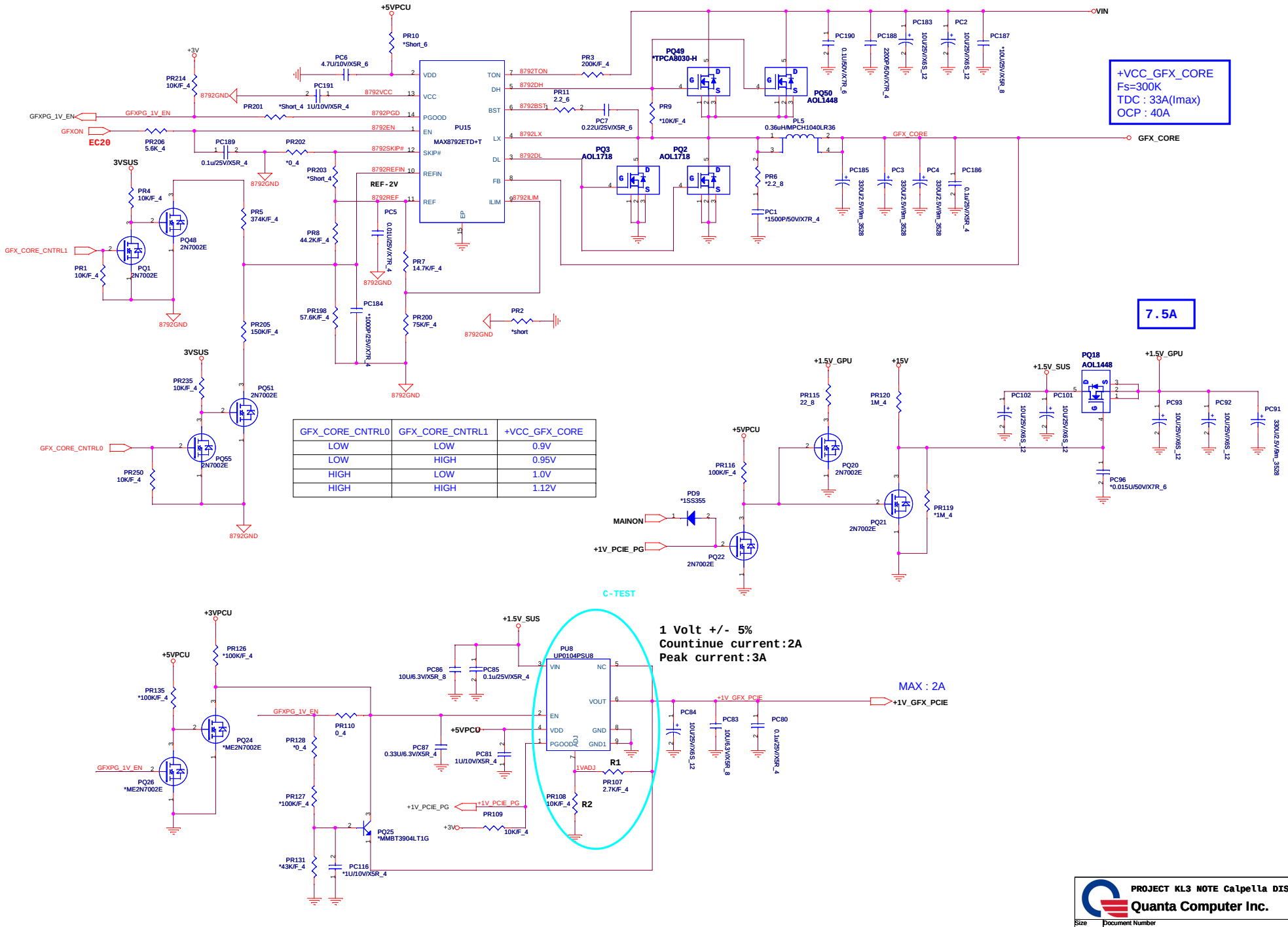
GND Close To Sandy Bridge Processor (POWER) Side





PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
C	DIS_1.8V_RUN (OZ8116LN)	1A
Date: Thursday, September 30, 2010	Sheet 44 of 48	



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	0.95V
HIGH	LOW	1.0V
HIGH	HIGH	1.12V

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DIS_GFX_VCC (MAX8792)	1A

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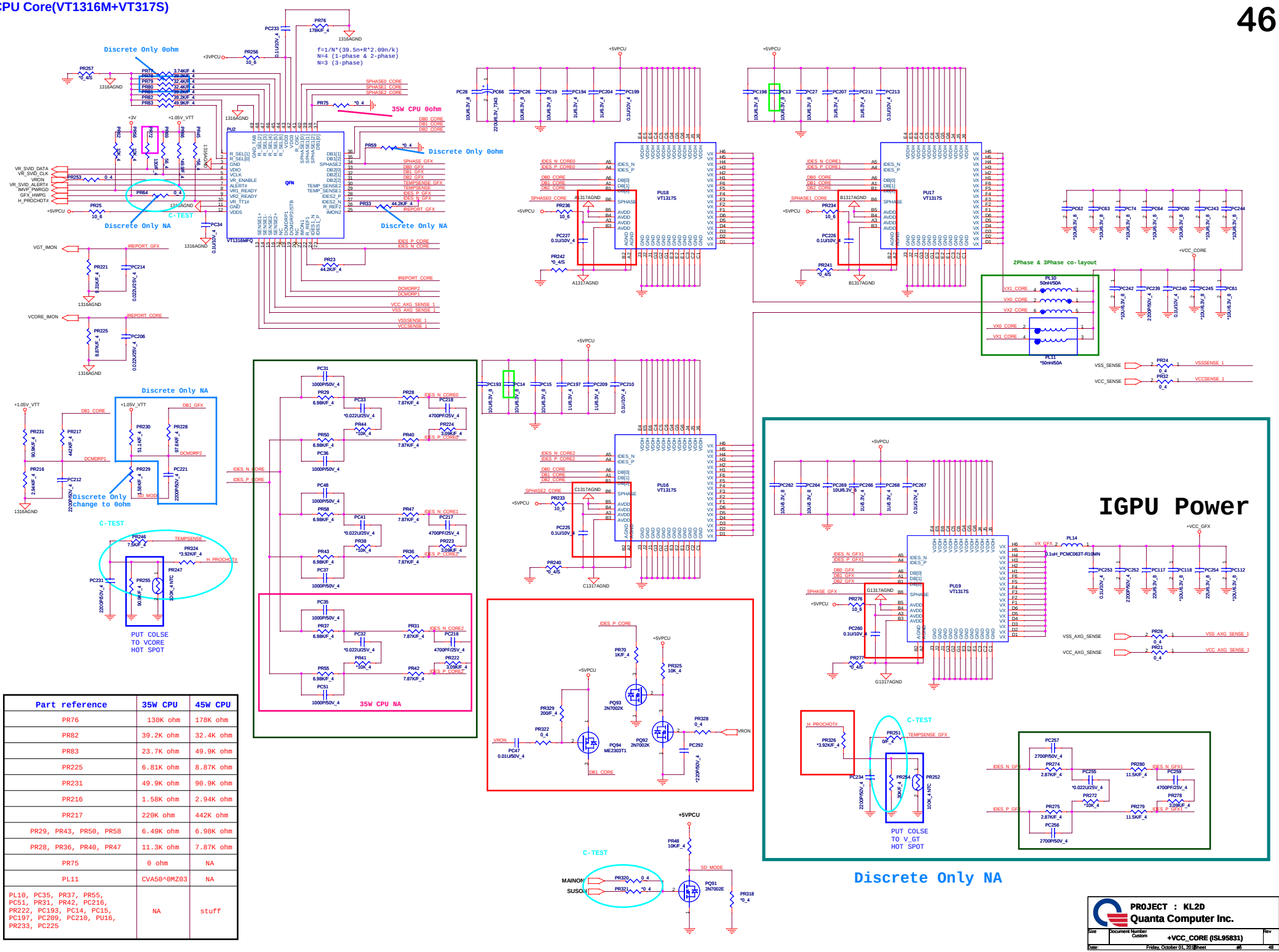

Part reference	35W CPU	45W CPU
PR76	130K ohm	178K ohm
PR82	39.2K ohm	32.4K ohm
PR83	23.7K ohm	49.9K ohm
PR225	6.81K ohm	8.87K ohm
PR231	49.9K ohm	90.9K ohm
PR216	1.58K ohm	2.94K ohm
PR217	220K ohm	442K ohm
PR29, PR43, PR50, PR58	6.49K ohm	6.98K ohm
PR28, PR36, PR40, PR47	11.3K ohm	7.87K ohm
PR75	0 ohm	NA
PL11	CVA50^0MZ03	NA
PL10, PC35, PR37, PR55, PC51, PR31, PR42, PC216, PR222, PC193, PC14, PC15, PC197, PC209, PC210, PU16, PR233, PC225	NA	stuff

PROJECT : KL2D
Quanta Computer Inc.
+VCC_CORE (ISL95831)
Size: Custom | Document Number | Rev: 1A
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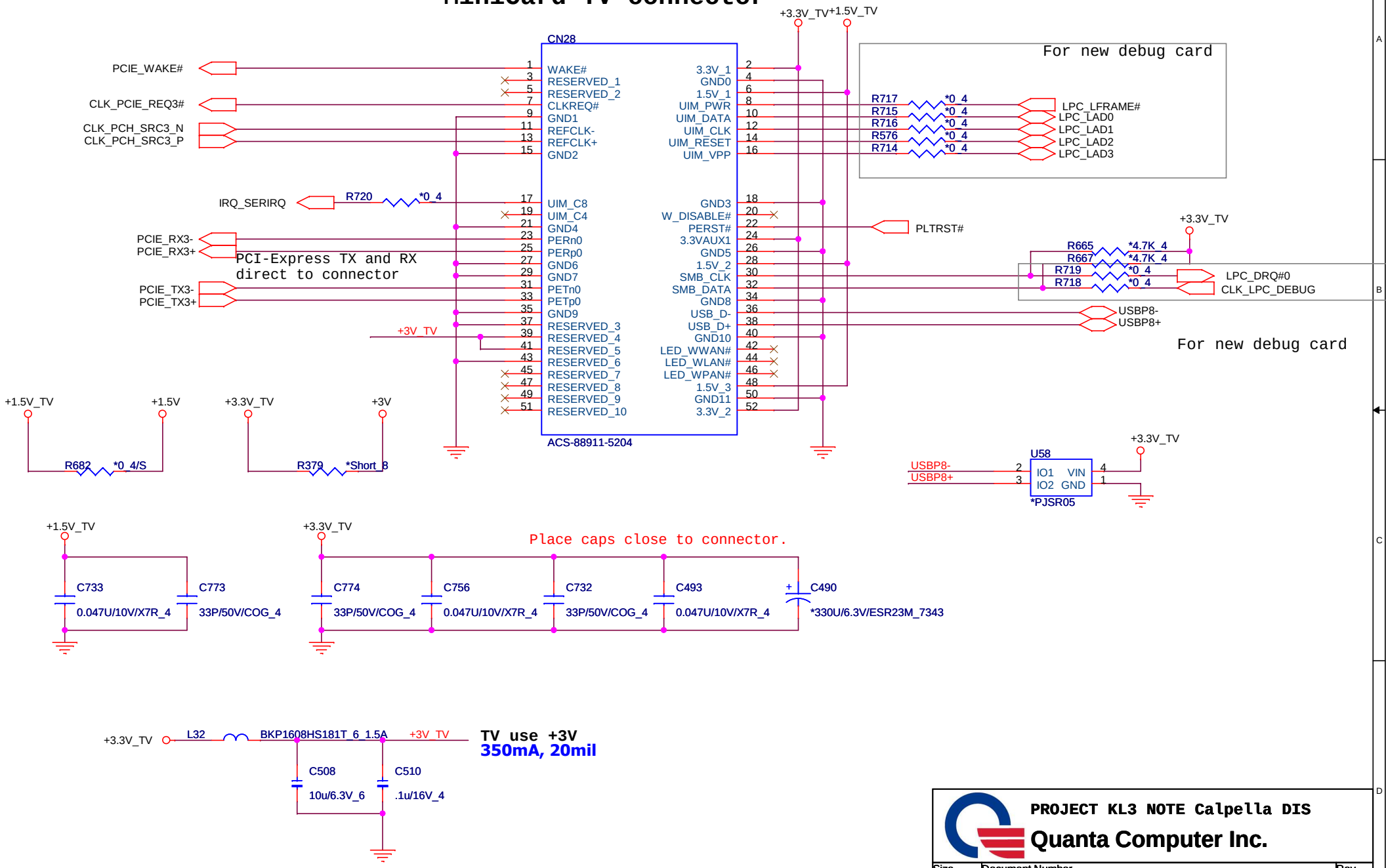
+3V
+1.5V

MiniCard TV connector



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (TV)	1A
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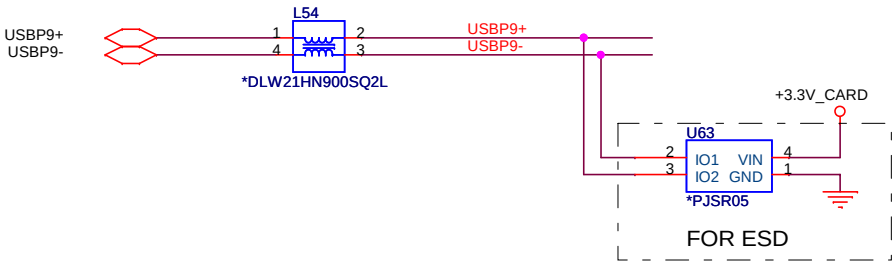
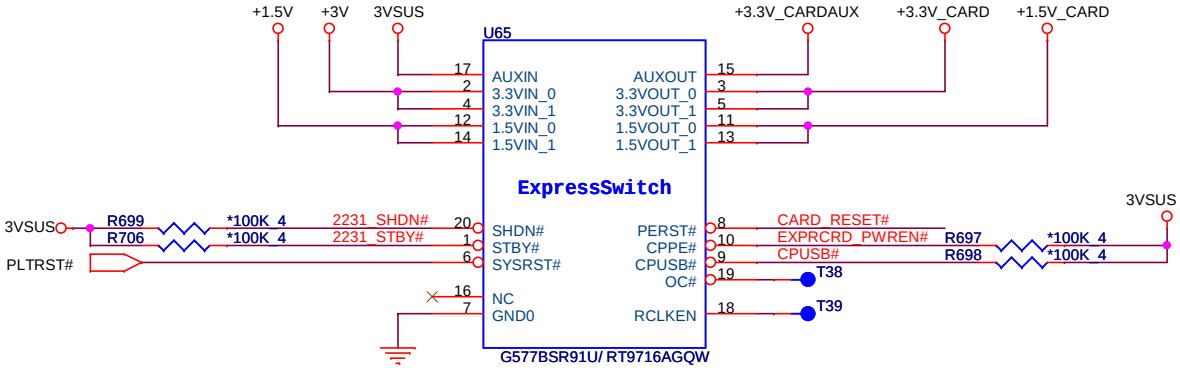
Express Card

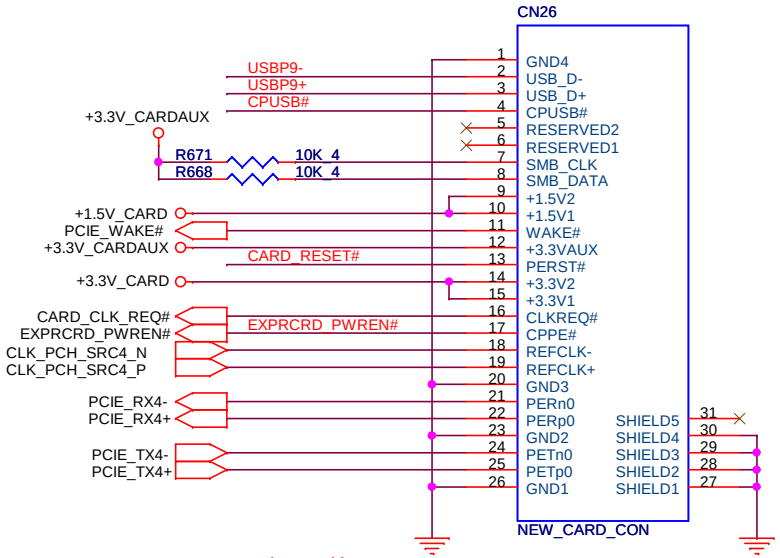
33

+3V
+1.5V
3VSUS

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.

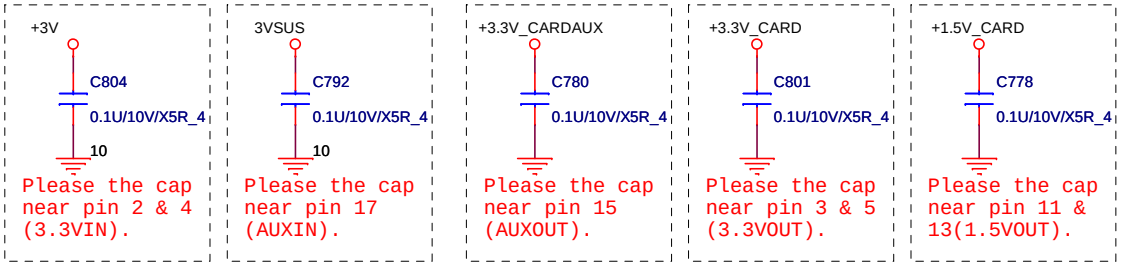


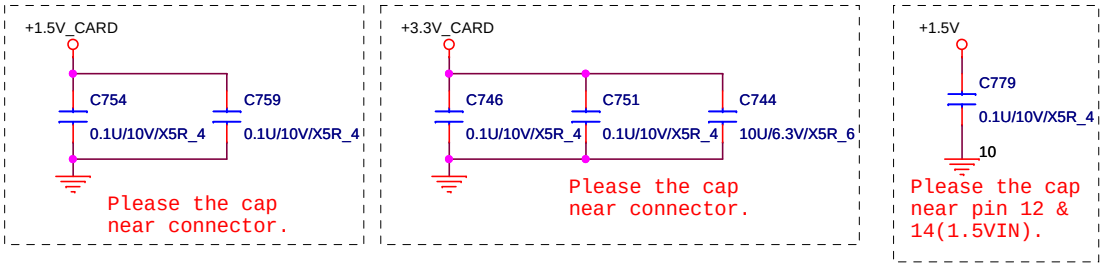




PCI-Express TX and RX direct to connector.

JAE PX10FS16PH-26P





PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Express Card	1A
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