Compal Confidential

MODEL NAME : ZIVY1

PCB NO : LA-B131P

BOM P/N : SKU1_4519RY38L05 (I5-4200U 1.6GHZ - Hynix 2G)
SKU2_4519RY38L05 (I5-4200U 1.6GHZ - Micro 2G)
SKU3_4519RY38L08 (I7-4500U 1.8GHZ - Hynix 4G) FAI
SKU3_4519RY38L08 (I7-4510U 1.8GHZ - Hynix 4G) main SMT
SKU4_4519RY38L07 (I2-4200U 1.6GHZ - Micro 4G)
SKU5_4519RY38L05 (I5-4200U 1.6GHZ - Samsung 2G)
SKU6_4519RY38L07 (I5-4200U 1.6GHZ - Samsung 4G)

Compal Confidential

Lamborghini Y40 M/B Schematics Document

Intel Haswell / Broadwell ULT Processor + AMD Venus XTX

2014-03-03

REV:1.0

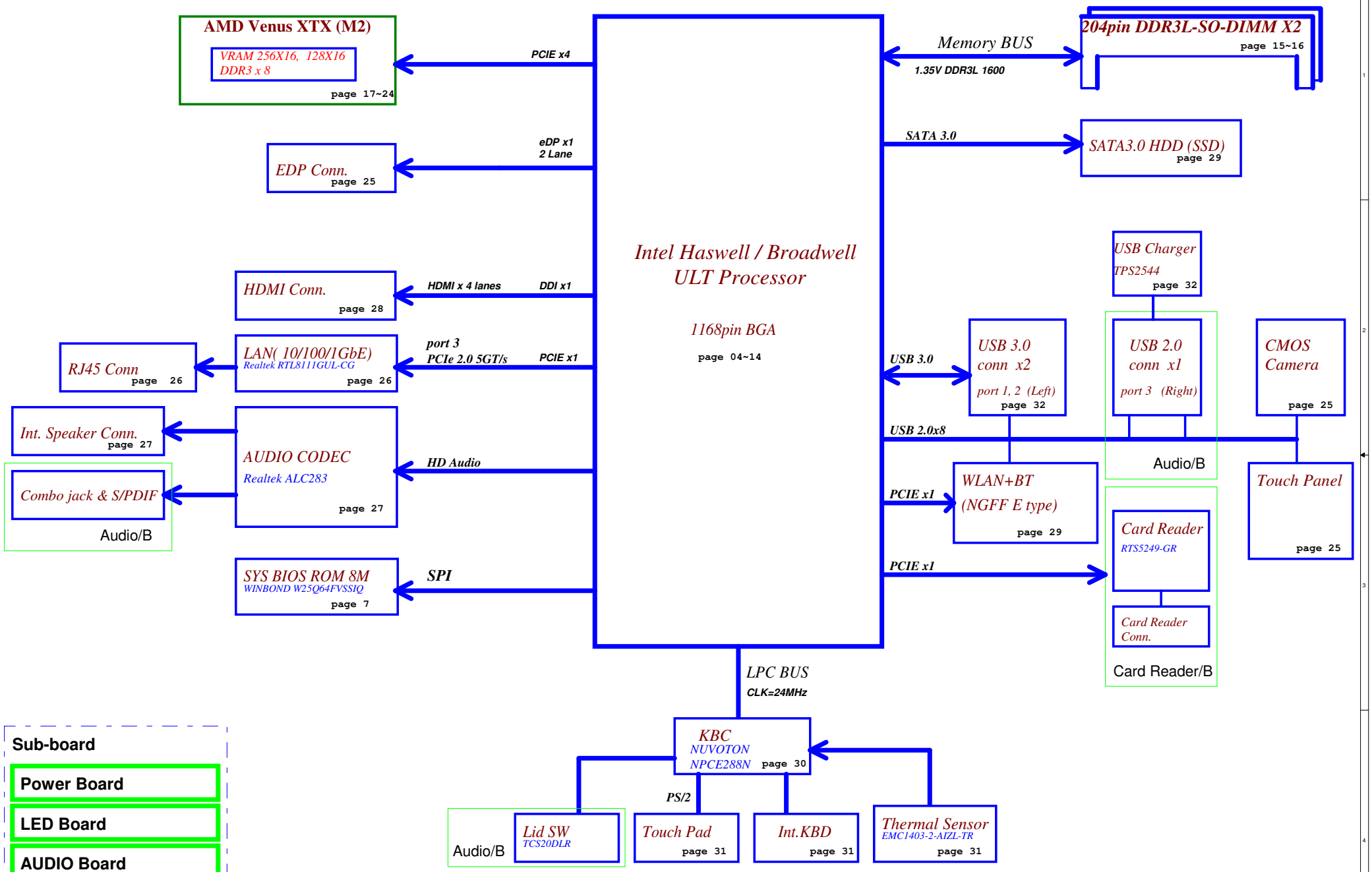
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: *Cover Sheet*

Size: Custom | Document Number: *LA-B131P* | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 1 of 52



Sub-board

- Power Board
- LED Board
- AUDIO Board
- Card Reader Board

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: Block Diagram			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 2 of 52		

Voltage Rails

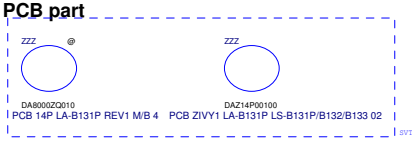
State \ power plane	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +CPU_CORE +0.675VS +VGA_CORE +MEM_GFX +3VGA +1.8VGA +VGA_PCIE
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BTO Item	BOM Structure
Unpop	@ @CONN@ / @DIS@ @EMI@ / @ESD@
CPU OPTION	CPU1@ ~ CPU4@
AMD Venus XTX	DIS@
VRAM Option	V2G@ / V4G@ HYN2@ / HYN4@ SAM2@ / SAM4@ MIC2@ / MIC4@
Platform	BDW@ / HSW@
DS3	DS3@
NODS3	NODS3@
LAN RTL8111GUS	SWR@ / LDO@
EMI PART	EMI@
ESD PART	ESD@
Crystal	NOGCLK@
Green CLK	GCLK@
SATA Repeater	TI@ / Parade@
EC	9022@ / 9012@
Connector	CONN@

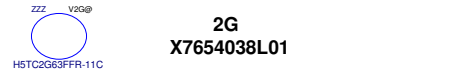
PCB part



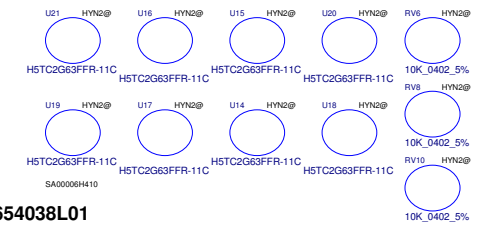
CPU part (R1)

HSW	U9 CPU3@ R3 — I5-4200U 1.6G SA00006SMC0 U9 CPU1@ R1 — I5-4210U 1.7GHZ SA00007LC10 U9 CPU2@ R3 — I7-4500U 1.8G SA00006SLA0 U9 CPU4@ R1 — I7-4510U 2GHZ SA00007M700 SVT
BDW	

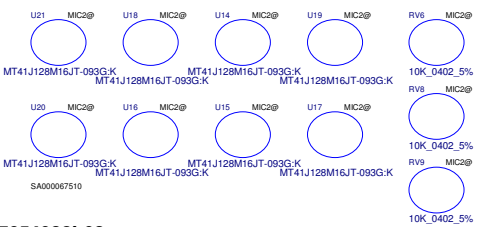
VRAM * 8 (R1)



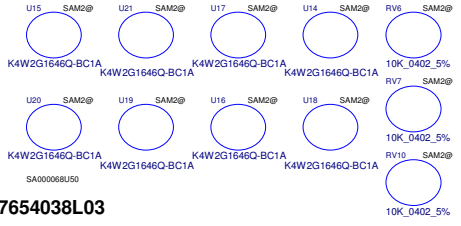
2G
X7654038L01



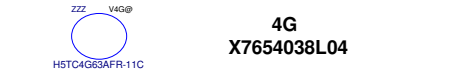
Hynix_X7654038L01



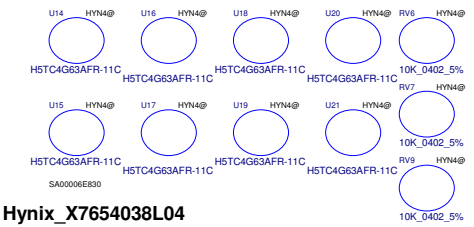
Micron_X7654038L02



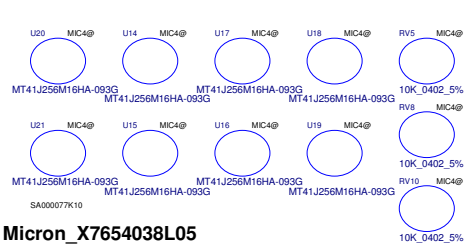
Samsung_X7654038L03



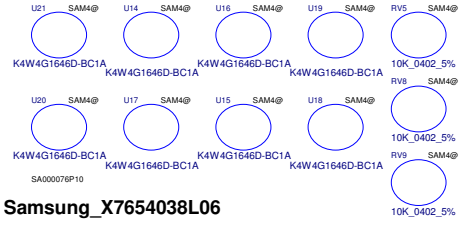
4G
X7654038L04



Hynix_X7654038L04



Micron_X7654038L05



Samsung_X7654038L06

EC SM Bus1 address

Device	Address
Smart Battery	0001 0010

EC SM Bus2 address

Device	Address
Thermal Sensor	1001 101xb

PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
DDR_JDIMM2	1010 010x A4h
TP module	

SMBUS Control Table

	SOURCE	BATT	VGA	SODIMM	EC-KB9022	TP	Smart Charge	Thermal Sensor
SMB_EC_CK1 SMB_EC_DA1	EC	V	X	X	X	X	V	X
SMBCLK SMBDATA	PCH	X	X	V	X	V	X	X
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	V	X	V	X	X	V

USB2.0

Port	0	1	2	3	4	5	6	7
	Left USB3.0	Left USB3.0	Right USB2.0		Touch Panel	Camera	BT (NGFF)	

Flexible I/O Capable Ports

HSIO Port	1	2	3	4	5	6	7	8	9	10	11	12	13	14
USB 3.0	1 USB3.0_1	2 USB3.0_2												
PCIe			1	2 CardReader	3 LAN	4 WLAN	5-L0 GPU_Venus	5-L1 GPU_Venus	5-L2 GPU_Venus	5-L3 GPU_Venus	6-L0	6-L1	6-L2	6-L3
SATA											3	2	1	0 HDD(SSD)

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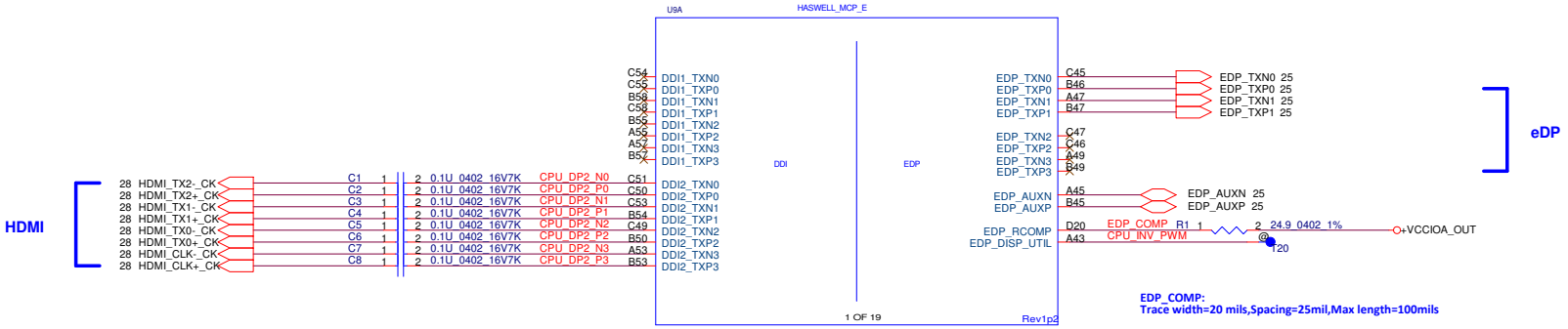
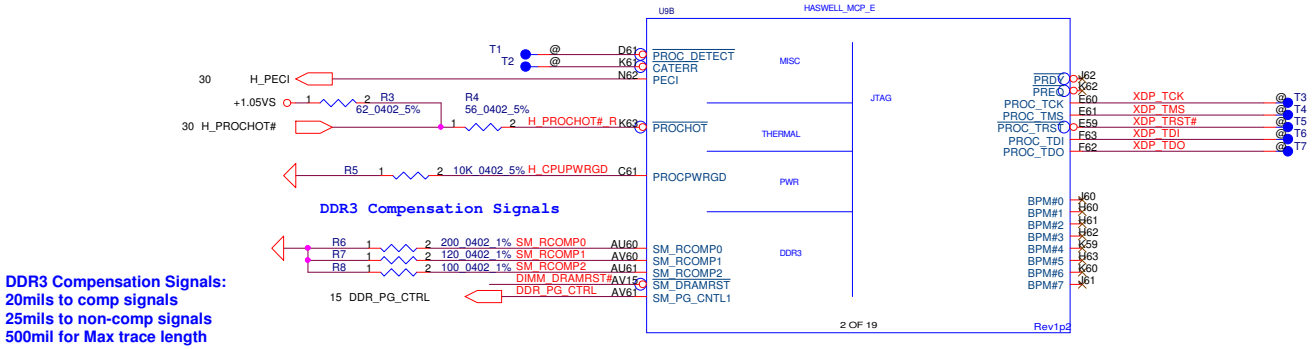
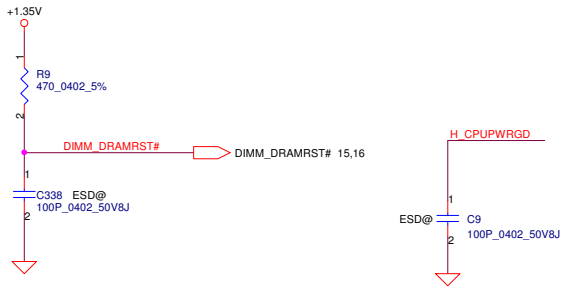
Issued Date	2014/03/03	Deciphered Date 2015/03/03	Title: Notes List
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 3 of 52		

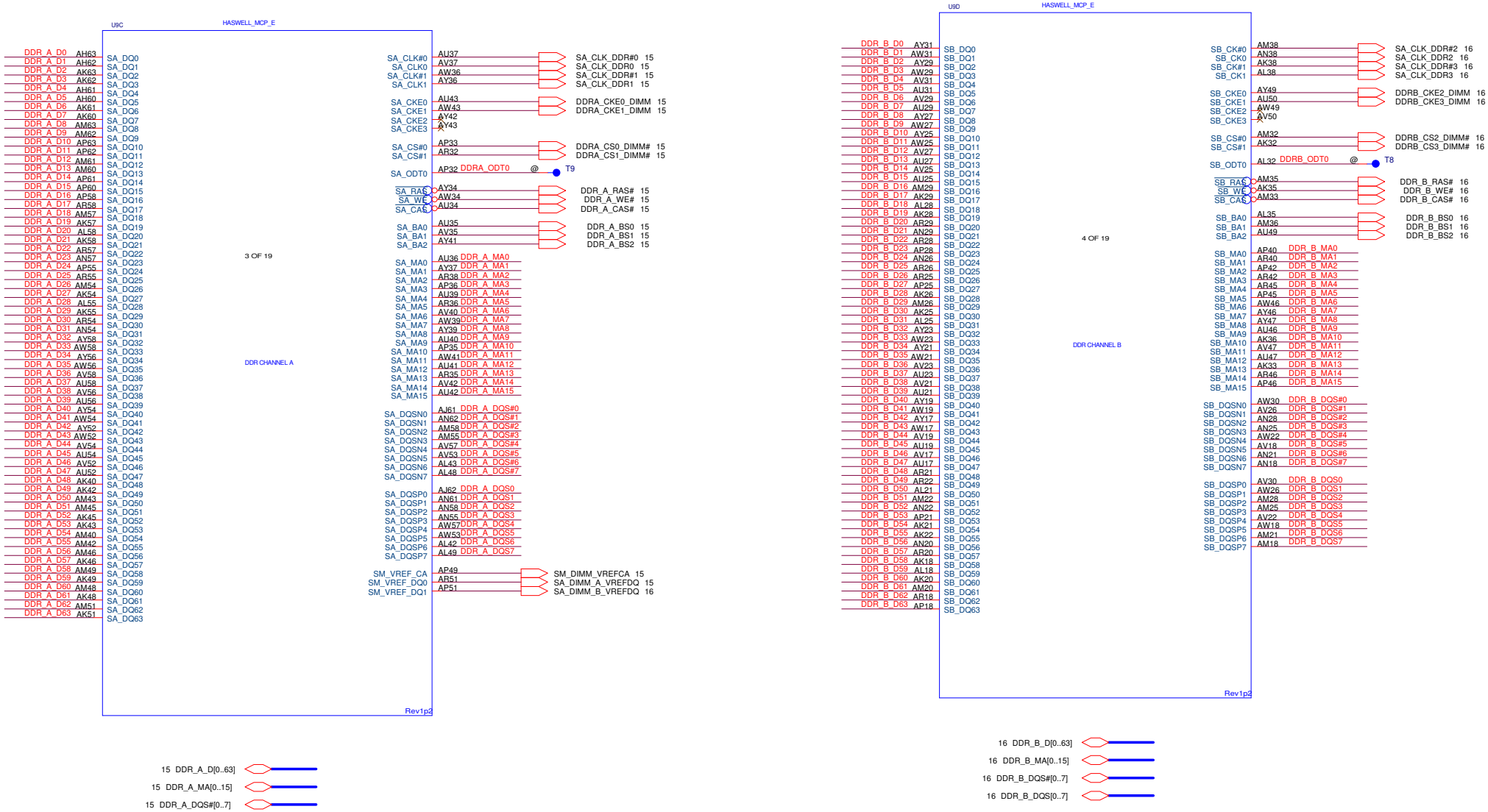






Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.	
Title	BDW ULT(1/11) DDI,MSIC,XDP
Size: Custom	Document Number: LA-B131P
Rev: 1.0	
Date: Tuesday, March 04, 2014	Sheet 4 of 52



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.		
Title: BDW ULT(2/11) DDRIII		
Size: Custom	Document Number: LA-B131P	Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 5 of 52	

GCLK (RG3 close to Y1.1)

34 CPU_RTCX1_GCLK — RG3 1 — 2 0_0402_5% — PCH_RTCX1 (SVT)

PCH_RTCX1 — NOGCLK@ R10 10M_0402_5% — PCH_RTCX2

Y1 32.768KHZ 12.5PF 9H03200031 NOGCLK@

C12 NOGCLK@ 15P_0402_50V8J

C13 NOGCLK@ 15P_0402_50V8J

+RTCVCC — C11 1U_0603_10V6K — JME2 SHORT PADS @ (SVT) **Clear ME (TOP)**

R11 20K_0402_1%

R12 20K_0402_1%

C10 1U_0603_10V6K — JME1 SHORT PADS @ (CMOS) **Clear CMOS (BOT)**

+RTCVCC — R13 1 — 2 1M_0402_5%

PCH_INTVRMEN — R14 1 — 2 330K_0402_5% — R15 1 @ 2 330K_0402_5%

INTVRMEN (+1.05VA)
* H : Integrated VRM enable
L : Integrated VRM disable

U9E HASWELL_MCP_E

PCH_RTCX1	AW5	RTCX1	RTC
PCH_RTCX2	AY5	RTCX2	
SM_INTRUDER#	AU6	INTRUDER	
PCH_INTVRMEN	AV7	INTVRMEN	
PCH_SRTCRST#	AV6	SRTCRST	
PCH_RTCRST#	AU7	RTCRST	
HDA_BIT_CLK	AW8	HDA_BCLK/I2S0_SCLK	AUDIO
HDA_SYNC	AV11	HDA_SYNC/I2S0_SFRM	
HDA_RST#	AU8	HDA_RST/I2S_MCLK	
HDA_SDIN0	AY10	HDA_SDI0/I2S0_RXD	
	AU12	HDA_SDI1/I2S1_RXD	
HDA_SDOUT	AU11	HDA_SDO/I2S0_TXD	
	AW10	HDA_DOCK_EN/I2S1_TXD	
	AV10	HDA_DOCK_RST/I2S1_SFRM	
	AY8	I2S1_SCLK	
@T10 PCH_JTAG_RST#	AU62	PCH_TRST	JTAG
@T11 PCH_JTAG_TCK	AE62	PCH_TCK	
@T12 PCH_JTAG_TDI	AD61	PCH_TDI	
@T13 PCH_JTAG_TDO	AE61	PCH_TDO	
PCH_JTAG_TMS	AD62	PCH_TMS	
	AL11	RSVD	
	AC4	RSVD	
@T14 PCH_TCK_JTAGX	AE63	JTAGX	
@T91 PCH_RSVD	AV2	RSVD	

5 OF 19

27 HDA_SDIN0

SATA_RN0/PERN6_L3	J5	SATA_PRX_DTX_N0 29	SATA
SATA_RP0/PERP6_L3	H5	SATA_PRX_DTX_P0 29	
SATA_TN0/PETN6_L3	B15	SATA_PTX_DRX_N0 29	
SATA_TP0/PETP6_L3	A15	SATA_PTX_DRX_P0 29	
SATA_RN1/PERN6_L2	J8		
SATA_RP1/PERP6_L2	H8		
SATA_TN1/PETN6_L2	A17		
SATA_TP1/PETP6_L2	B17		
SATA_RN2/PERN6_L1	J6		
SATA_RP2/PERP6_L1	H6		
SATA_TN2/PETN6_L1	B14		
SATA_TP2/PETP6_L1	C15		
SATA_RN3/PERN6_L0	E5		
SATA_RP3/PERP6_L0	E5		
SATA_TN3/PETN6_L0	C17		
SATA_TP3/PETP6_L0	D17		
SATA0GP/GPIO34	V1	PCH_GPIO34	
SATA1GP/GPIO35	U1	PCH_GPIO35	PCH_GPIO35 9
SATA2GP/GPIO36	V6	PCH_GPIO36	PCH_GPIO36 9
SATA3GP/GPIO37	AC1	PCH_GPIO37	PCH_GPIO37 9
SATA_IREF	A12		+1.05VS_ASATA3PLL
RSVD	L11		
RSVD	K10		
SATA_RCOMP	C12	SATA_RCOMP	within 500 mils
SATALED#	U3	PCH_SATALED#	R16 1 — 2 3.01K_0402_1% — PCH_SATALED# 9,33

Rev1p2

HDD(SSD)

RTC CONN place to PWR side

RTC Battery

W=20mils +RTCVCC — R17 1 — 2 0_0402_5% (SIV) — W=20mils +RTCBATT

C14 1U_0402_6.3V6K

+3V_PCH — R18 1 @ 2 1K_0402_5% — HDA_SDOUT

HDA_SDOUT

* ME debug mode,this signal has a weak internal PD
Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

27 HDA_SDOUT_AUDIO
27 HDA_SYNC_AUDIO
27 HDA_RST_AUDIO#
27 HDA_BITCLK_AUDIO

RP1 EMI@ 33_0804_8P4R_5%

1	8	
2	7	HDA_SDOUT
3	6	HDA_SYNC
4	5	HDA_RST#
		HDA_BIT_CLK

C15 @EMI@ 68P_0402_50V8J

30 ME_EN — R21 1 — 2 0_0402_5% (SIV)

+3VS — R19 1 — 2 10K_0402_5% — PCH_GPIO34

PCH_JTAG_TCK — R20 1 @ 2 51_0402_5%

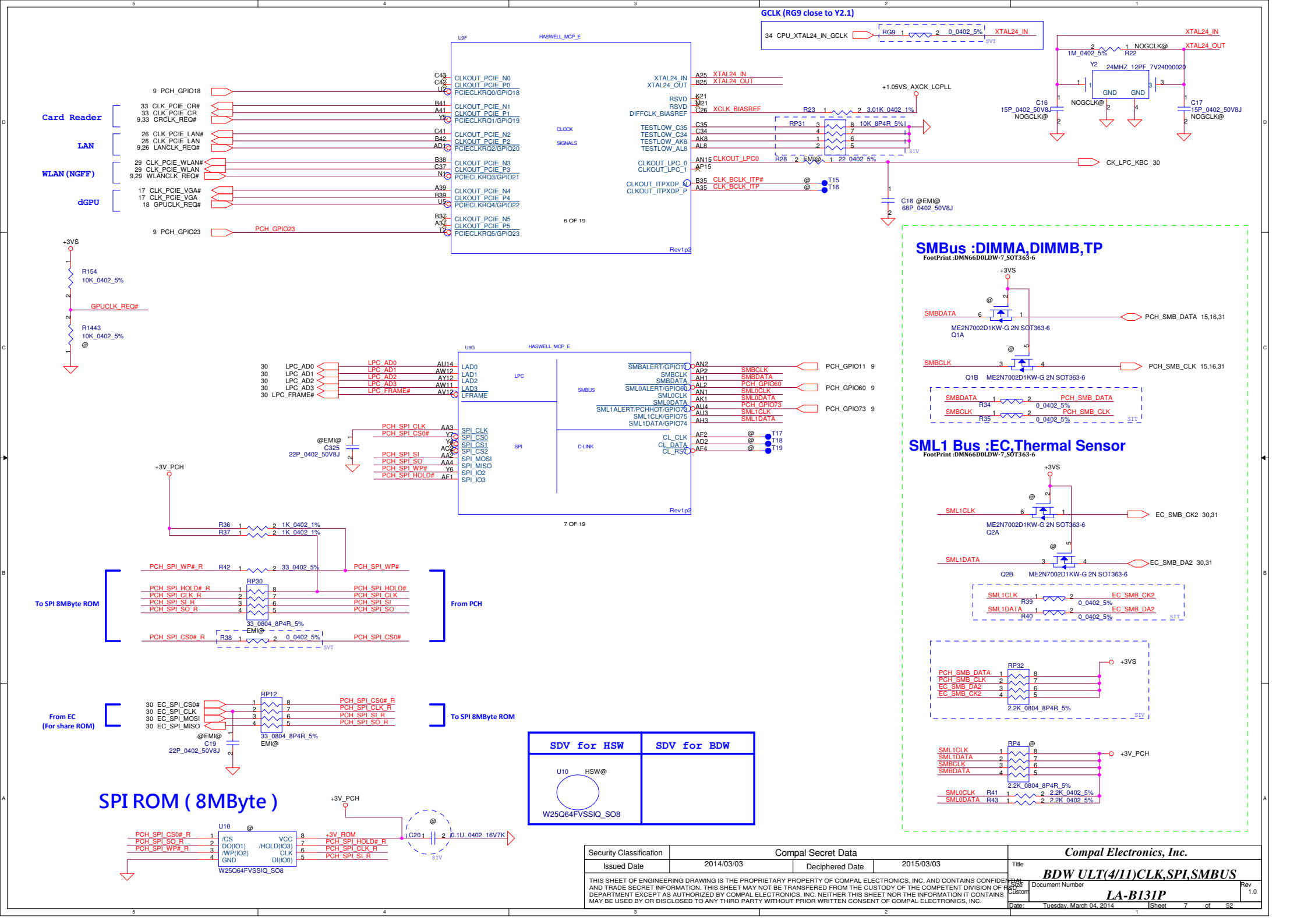
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: BDW ULT(3/11)RTC,SATA,JTAG

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 6 of 52



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: BDW ULT(4/11)CLK,SPI,SMBUS			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
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Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit

CAN be NC ,if not support Deep Sx

DPWROK: Tired toghter with RSMRST# that do not support Deep Sx

DSWODVREN - On Die DSW VR Enable
(*) H : Enable(DEFAULT)
( ) L : Disable

ESD

U9H HASWELL_MCP_E SYSTEM POWER MANAGEMENT

8 OF 19 Rev1p2

U9I HASWELL_MCP_E

9 OF 19 Rev1p2

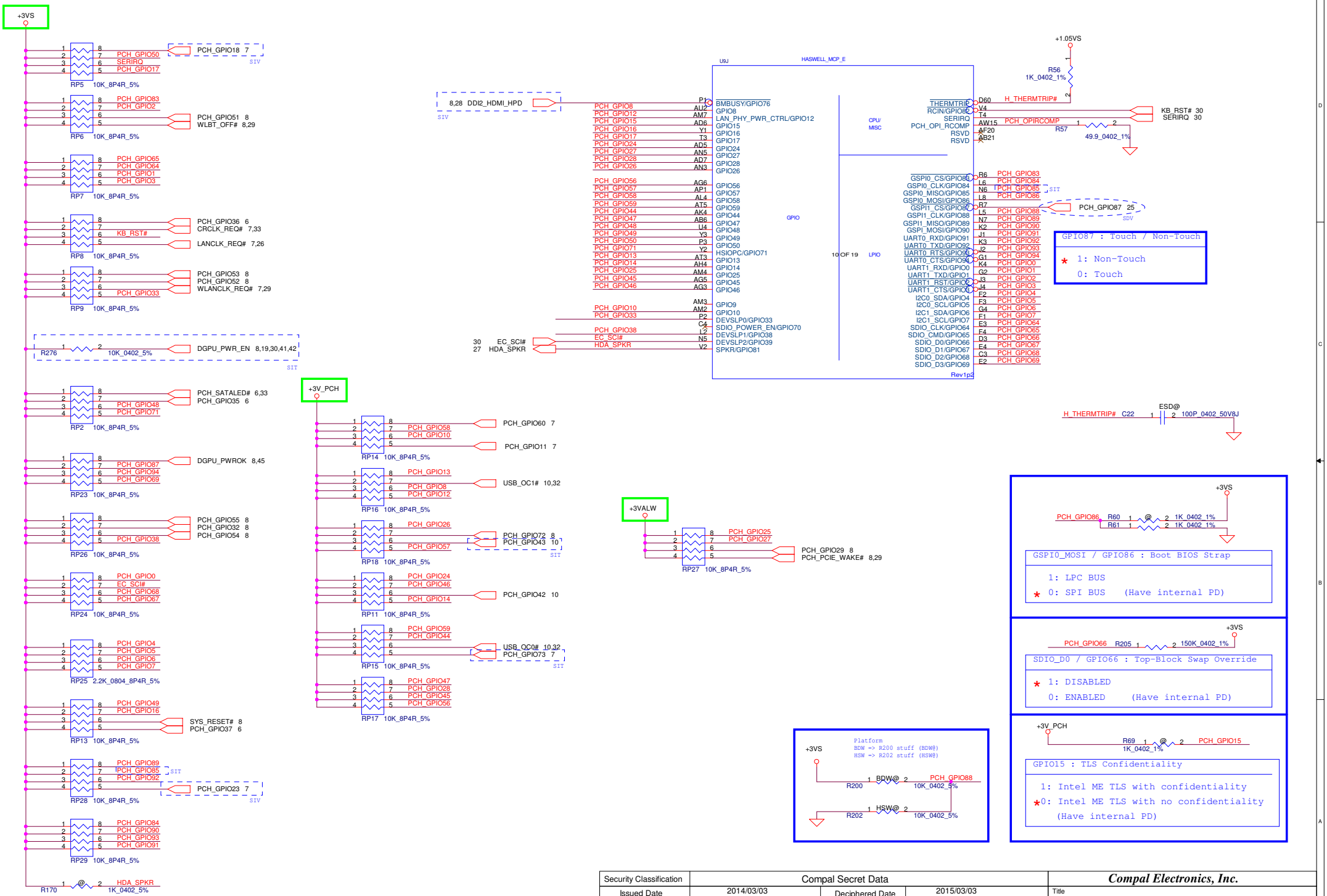
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: BDW ULT(5/11) PM,GPIO,DDI

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 8 of 52



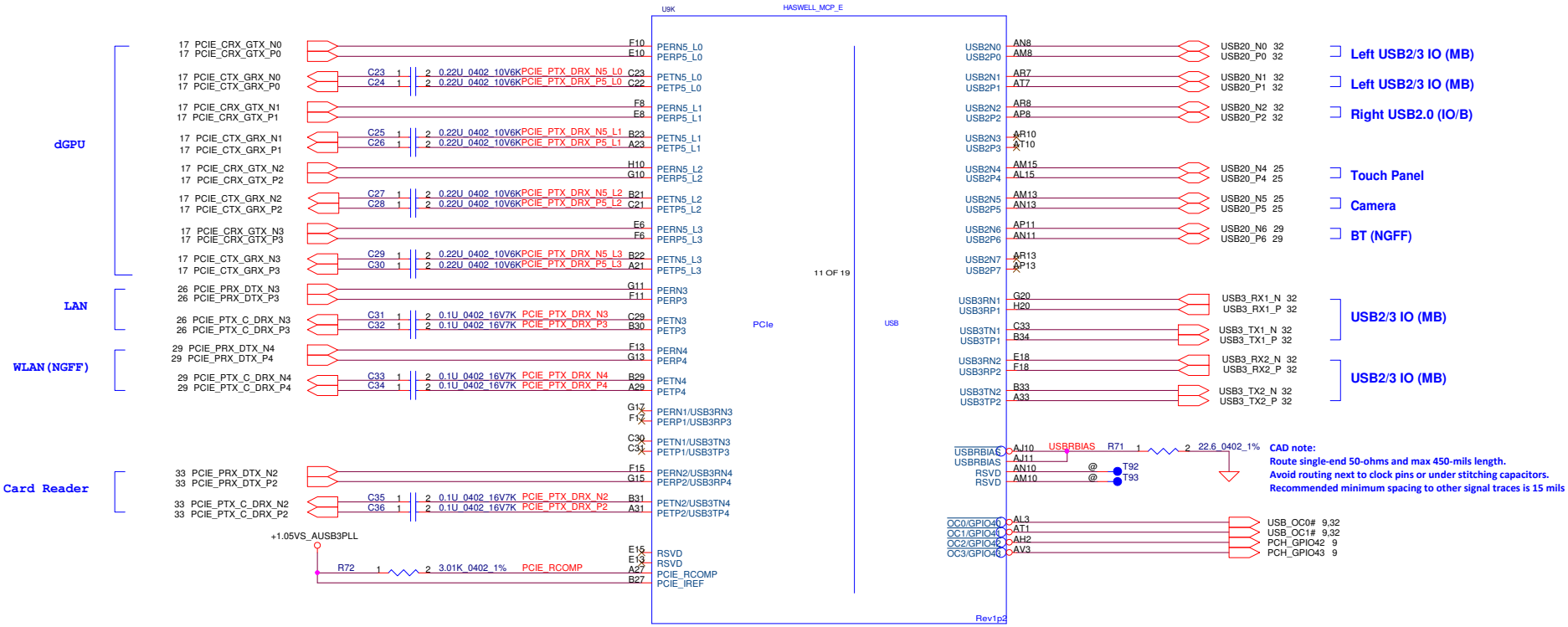
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: BDW ULT(6/11) GPIO,LPIO

Size	Document Number	Rev
Custom	LA-B131P	1.0

Date: Tuesday, March 04, 2014 Sheet 9 of 52



USB2.0

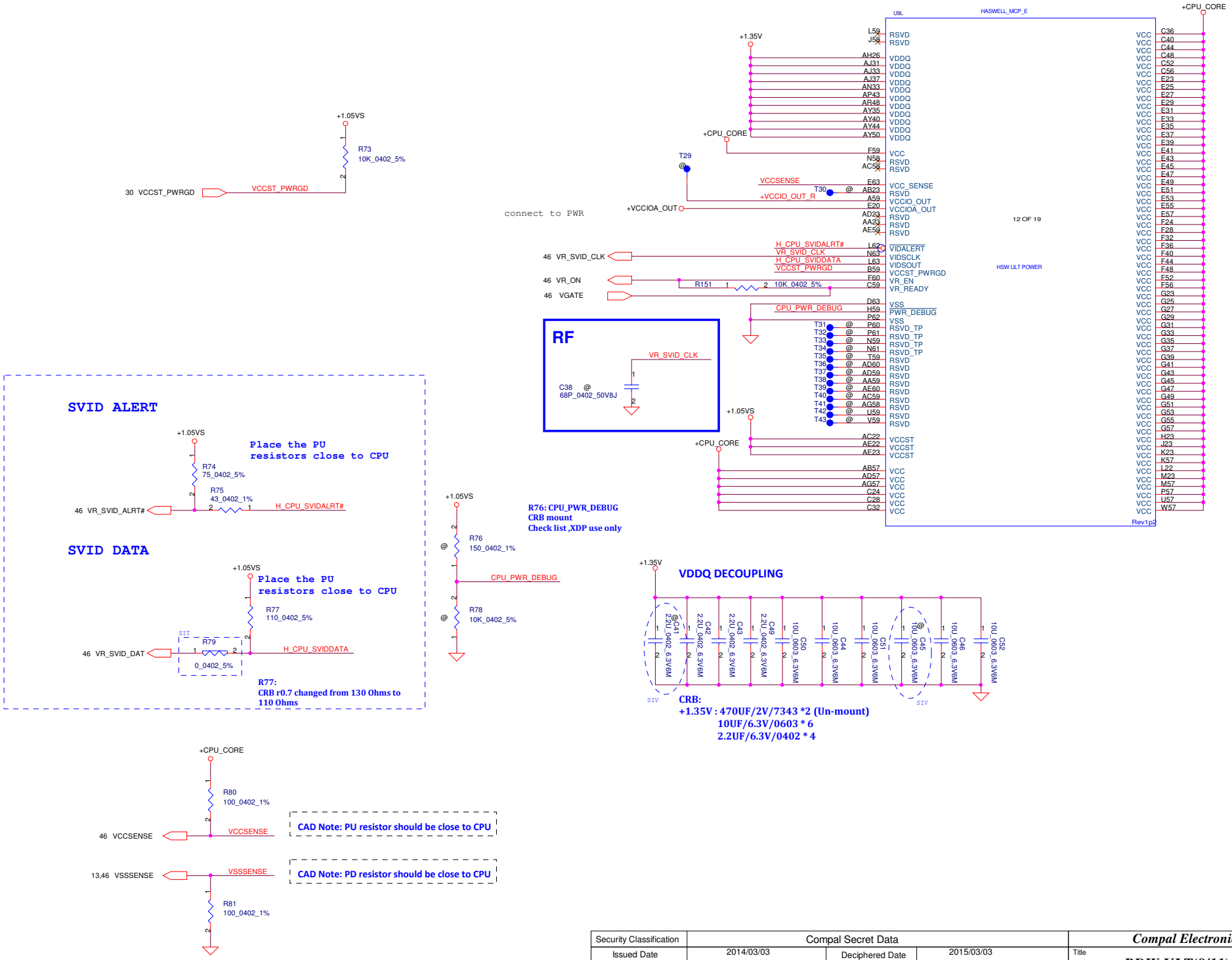
Port	0	1	2	3	4	5	6	7
	Left USB3.0	Left USB3.0	Right USB2.0		Touch Panel	Camera	BT (NGFF)	

Flexible I/O Capable Ports

HSIO Port	1	2	3	4	5	6	7	8	9	10	11	12	13	14
USB 3.0	1 USB3.0_1	2 USB3.0_2												
PCIe			1	2 CardReader	3 LAN	4 WLAN	5-L0 GPU_Venus	5-L1 GPU_Venus	5-L2 GPU_Venus	5-L3 GPU_Venus	6-L0	6-L1	6-L2	6-L3
SATA											3	2	1	0 HDD(SSD)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date 2015/03/03	Title: BDW ULT(7/11) PCIE,USB

Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 10 of 52		



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	BDW ULT(8/11) Power		
Size	Document Number		Rev
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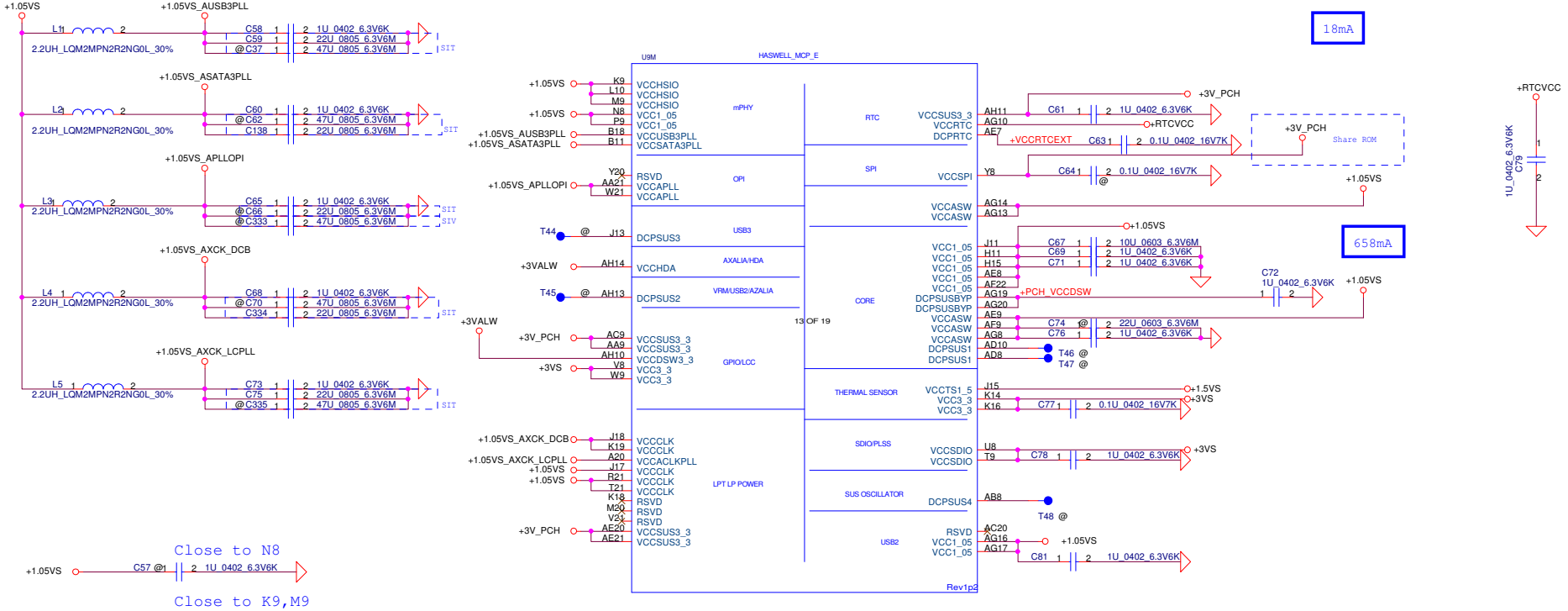
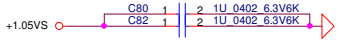
Check Power Source



Close to N8

Close to K9,M9

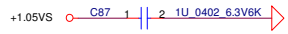


Close to AC9/AA9/AE20/AE21

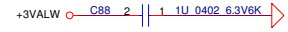
Close to V8

Close to J17

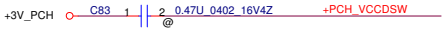
Close to R21



Close to AH14

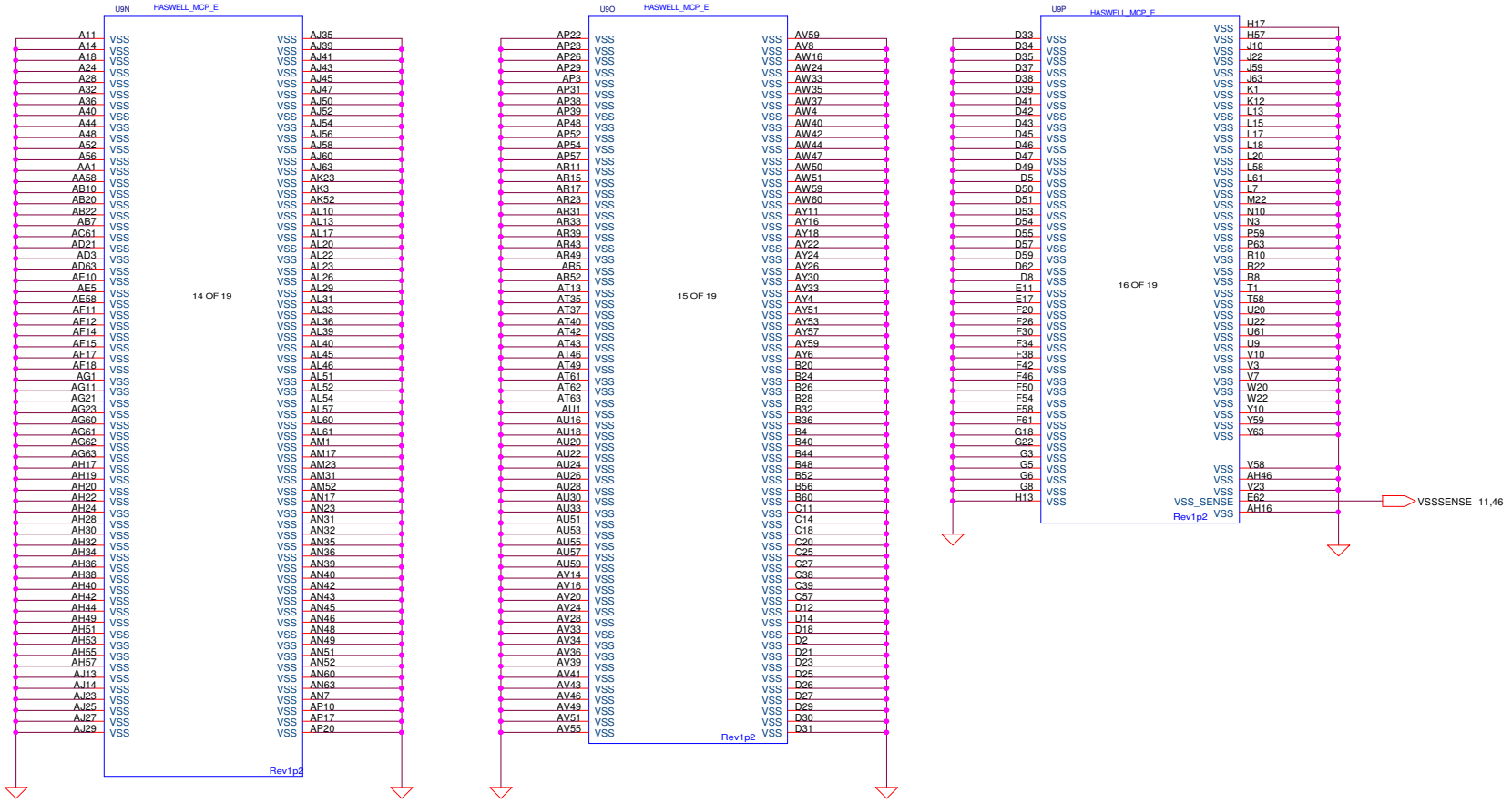


V1.0



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: BDW ULT(9/11) Power			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 12 of 52		



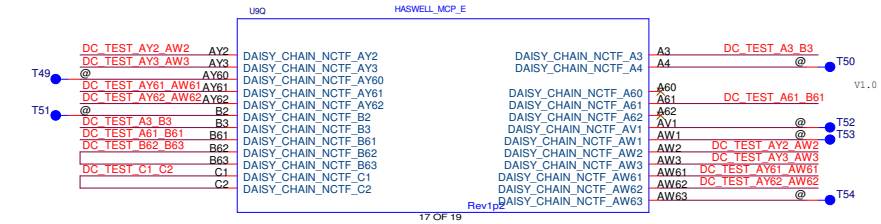
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

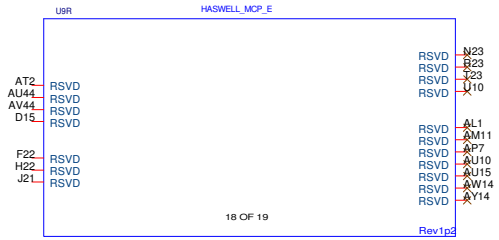
Compal Electronics, Inc.

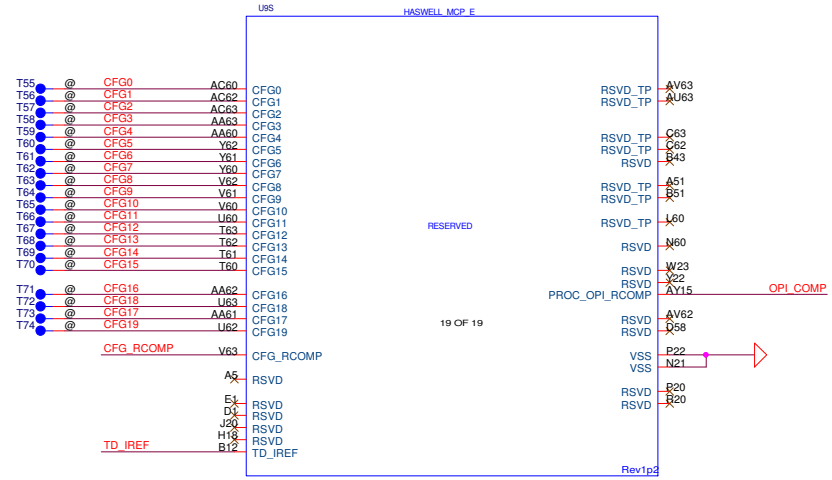
Title: **BDW ULT(10/11) GND**

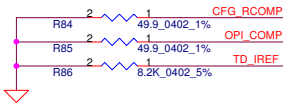
Size: Custom | Document Number: **LA-B131P** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 13 of 52

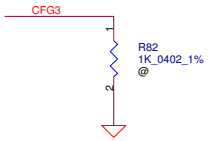




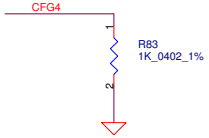




CFG Straps for Processor



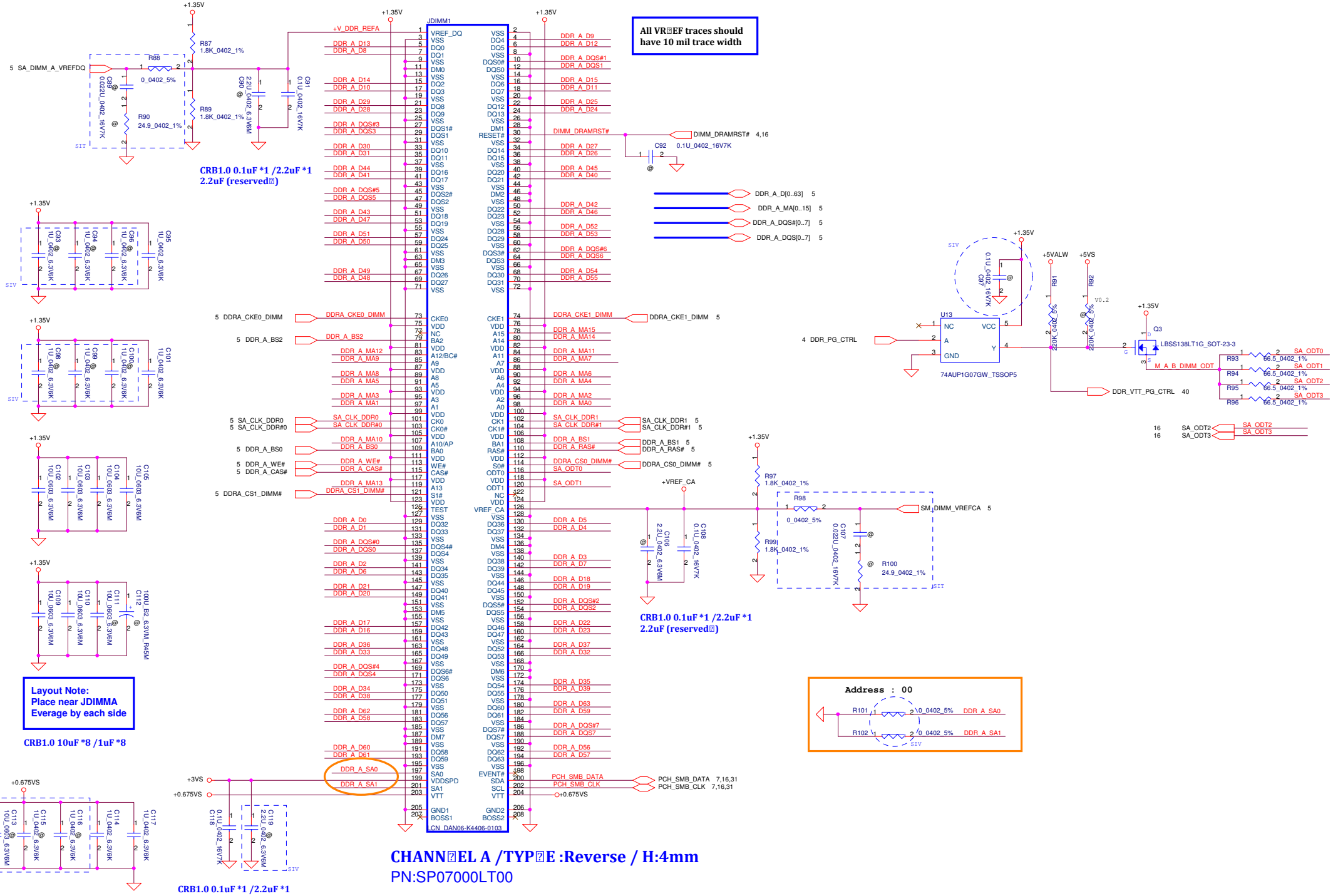
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

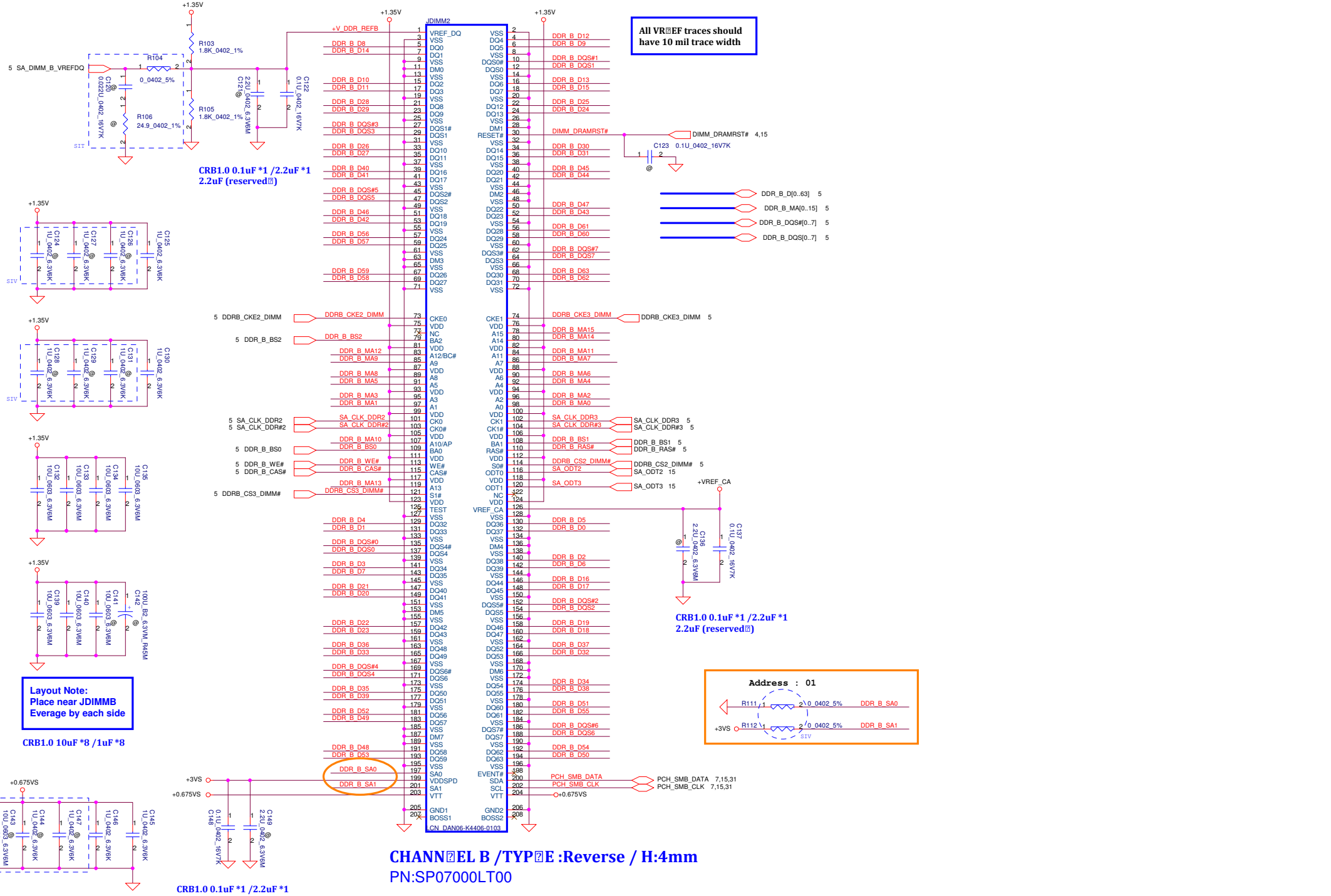
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: BDW ULT(11/11) RSVD			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 14 of 52		



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: DDR3L_DIMMA			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 15 of 52		



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	DDR3L_DIMMB		
Size	Document Number		Rev
Custom	LA-B131P		1.0
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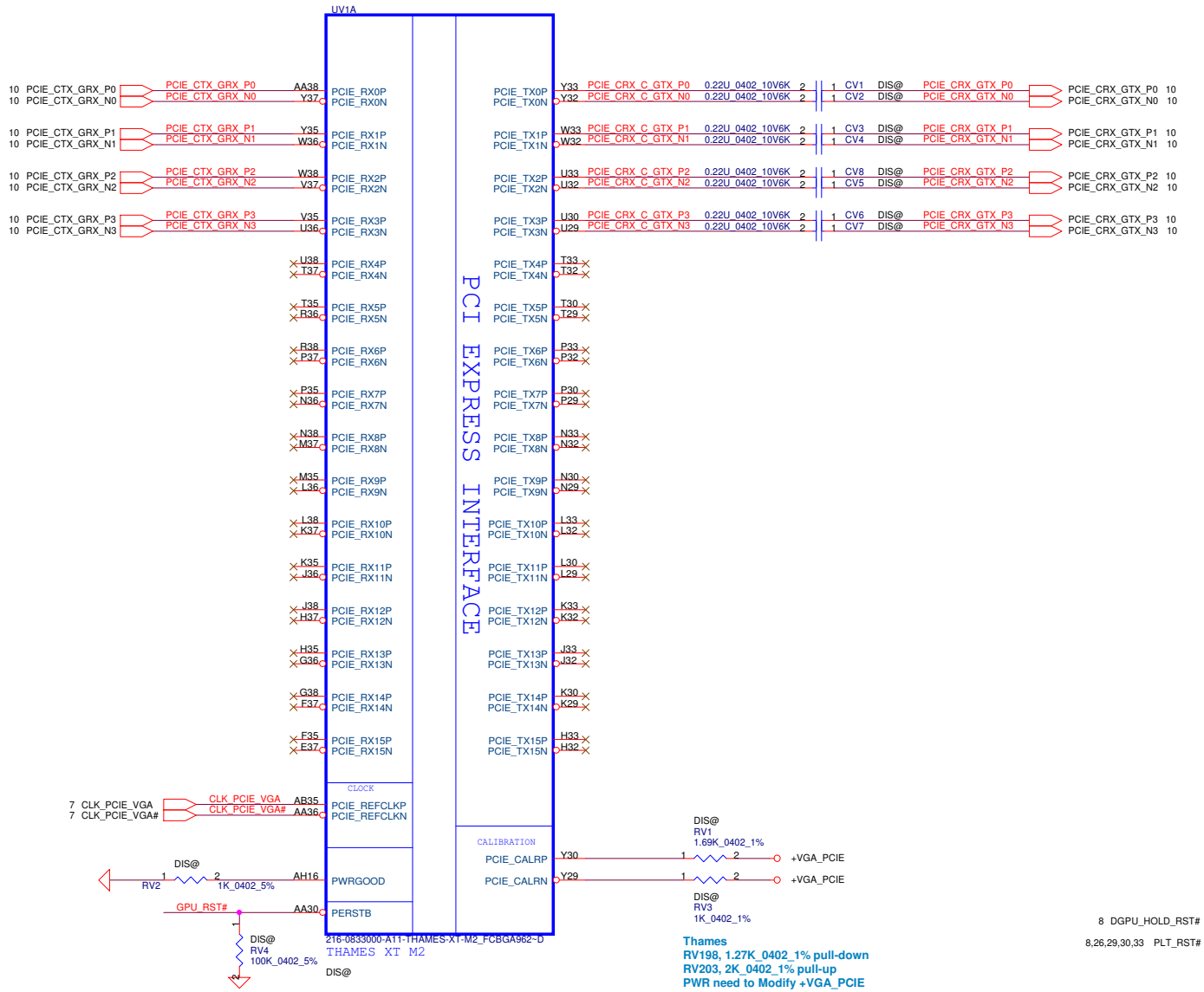
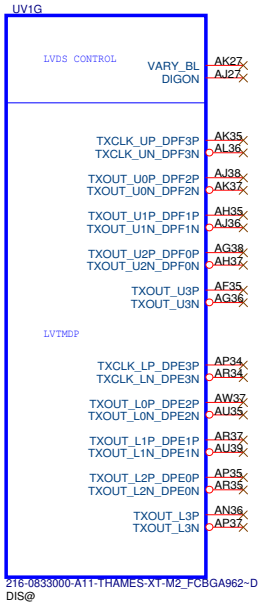
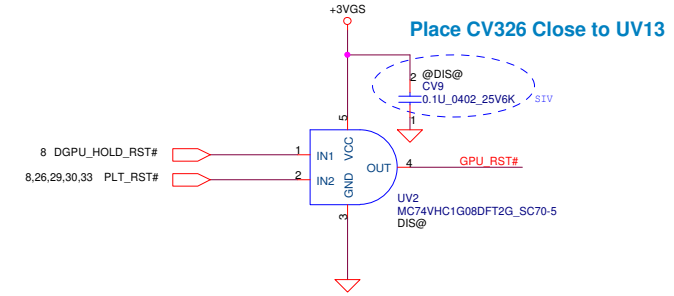
GFX PCIE LANE REVERSAL



Thames
RV198, 1.27K_0402_1% pull-down
RV203, 2K_0402_1% pull-up
PWR need to Modify +VGA_PCIE

LVDS Interface





Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	Venus XTX(1/8) PCIE/PWRseq		
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 17 of 52		

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BIF_VGA DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	H2SYNC			0
RSVD	GENERICC			0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

VENUS MLPs
PS_3 used default

PS0_[1] = 1
PS0_[2] = 0 For a 256-MB aperture size, PS_0[3:1] is set to 001
PS0_[3] = 0
PS0_[4] = 1 Must be 1 at reset.
PS0_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.

PS1_[1] = 1 PCIe GEN3 is supported = 1
PS1_[2] = 0 Must be 0 at reset.
PS1_[3] = 0 Must be 0 at reset.
PS1_[4] = 1 Full Tx output swing = 1
PS1_[5] = 1 Tx deemphasis enabled = 1

PS2_[1] = 0 Reserved
PS2_[2] = 0 Reserved
PS2_[3] = 0 Disable the external BIOS ROM device = 1
PS2_[4] = 1 The device will not be recognized as the system's VGA controller = 1
PS2_[5] = 1 Reserved

PS3_[1] = 0 Reserved
PS3_[2] = 0 Reserved
PS3_[3] = 0 Reserved
PS3_[4] = 1 Audio-capable display outputs. 111 = No usable endpoints.
PS3_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.

SUN internal VGA Thermal Sensor
Address 0x714

NC_TSVSSQ should be tied to GND

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hy SA00006H410	RV6 0	RV8 0	RV10 0
Micron 2Gb SA000067510	RV6 0	RV8 0	RV9 1
Samsung 2Gb SA000068U50	RV6 0	RV7 1	RV10 0
Hy SA00006y	RV6 0	RV7 1	RV9 1
Micron 4Gb SA000077K10	RV5 1	RV8 0	RV10 0
Samsung 4Gb SA000076P10	RV5 1	RV8 0	RV9 1

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.
Title: Venus XTX(2/8) Main Gen
Size: D
Document Number: LA-B131P
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Date: Tuesday, March 04, 2014
Sheet 18 of 52

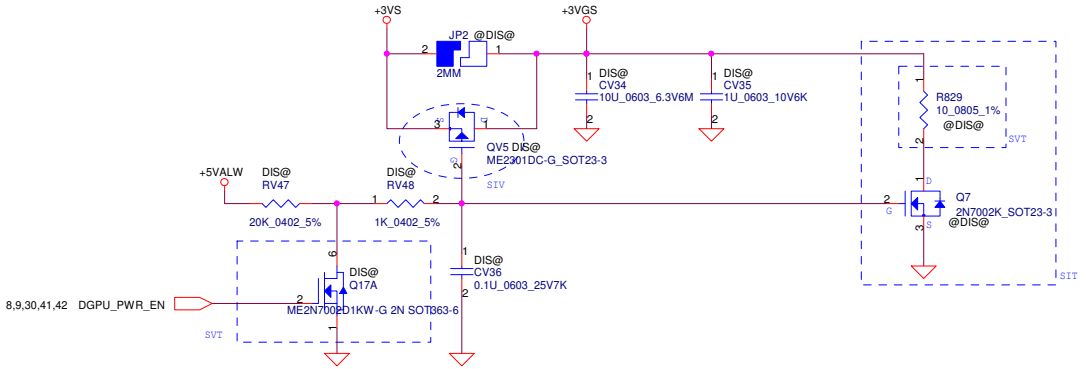
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

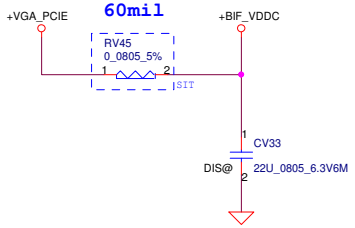
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

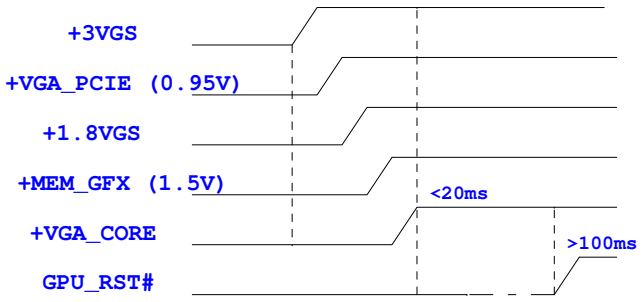
Switch circuits in BACO desingns for Thames/Seymour only 55mA@1.0V, in BACO mode

+3VS TO +3VGS

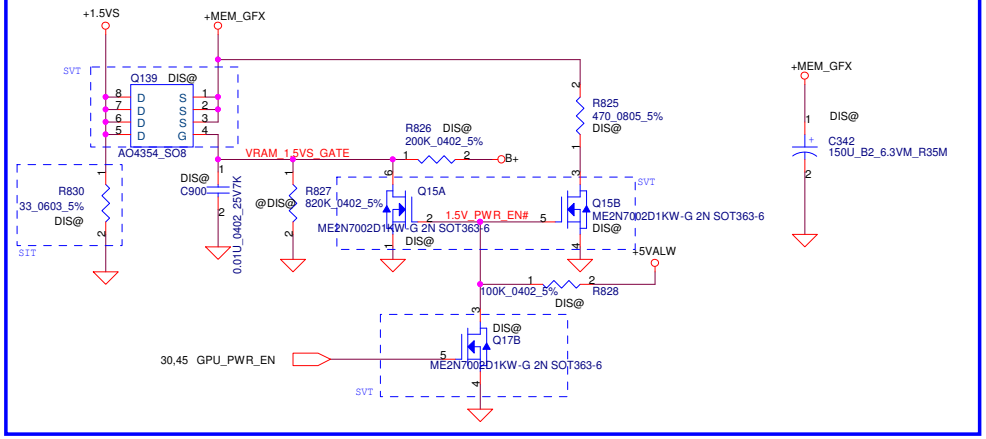




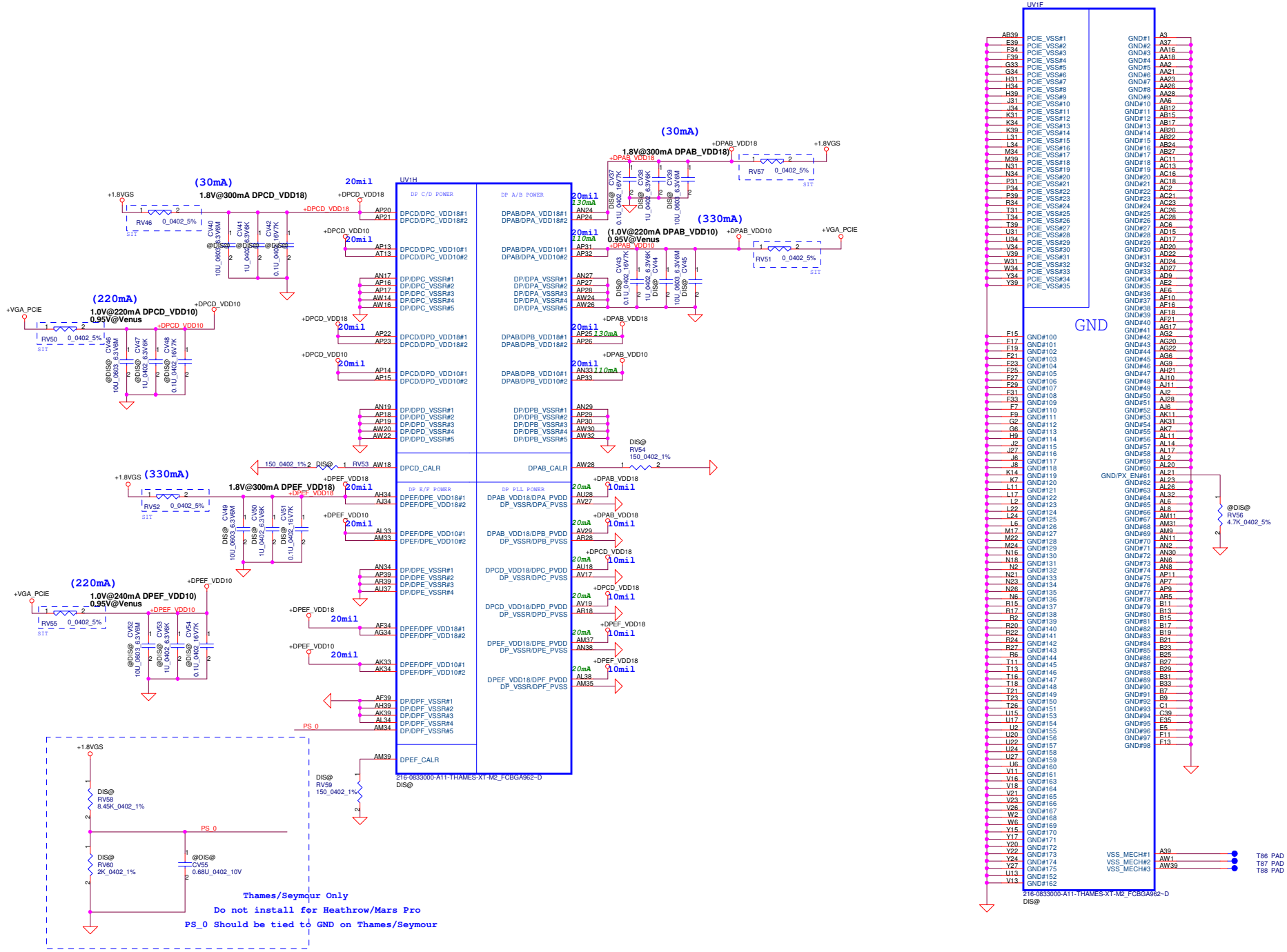
Power seguence of Venus XTX



+1.5VS to +MEM_GFX



Compal Electronics, Inc.	
Title	Venus XTX(3/8) DC/DC POWER
Size: Custom	Document Number: LA-B131P
Rev	1.0
Date: Tuesday, March 04, 2014	Sheet 19 of 52



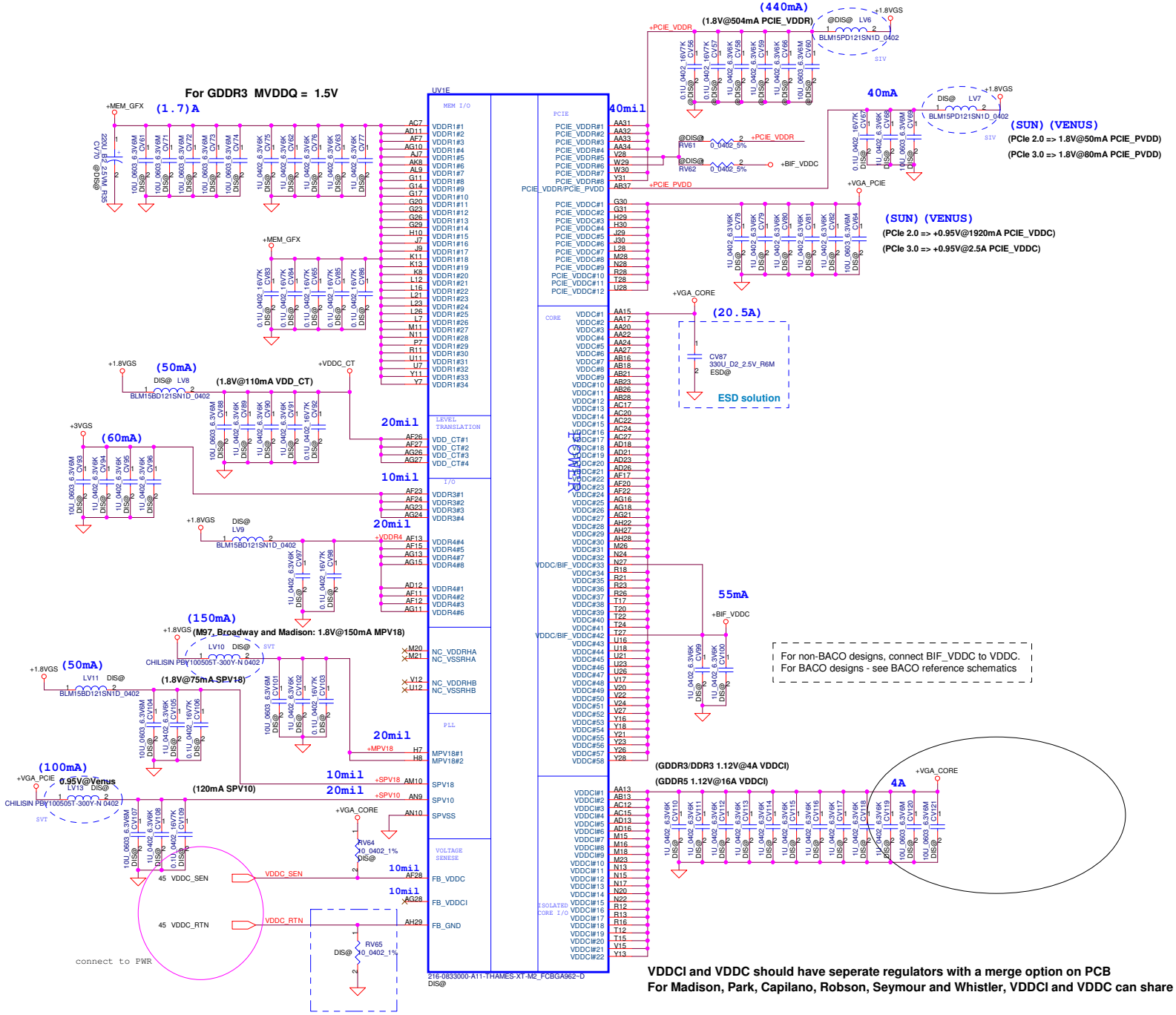
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **Venus XTX(4/8)DPX Power/GND**

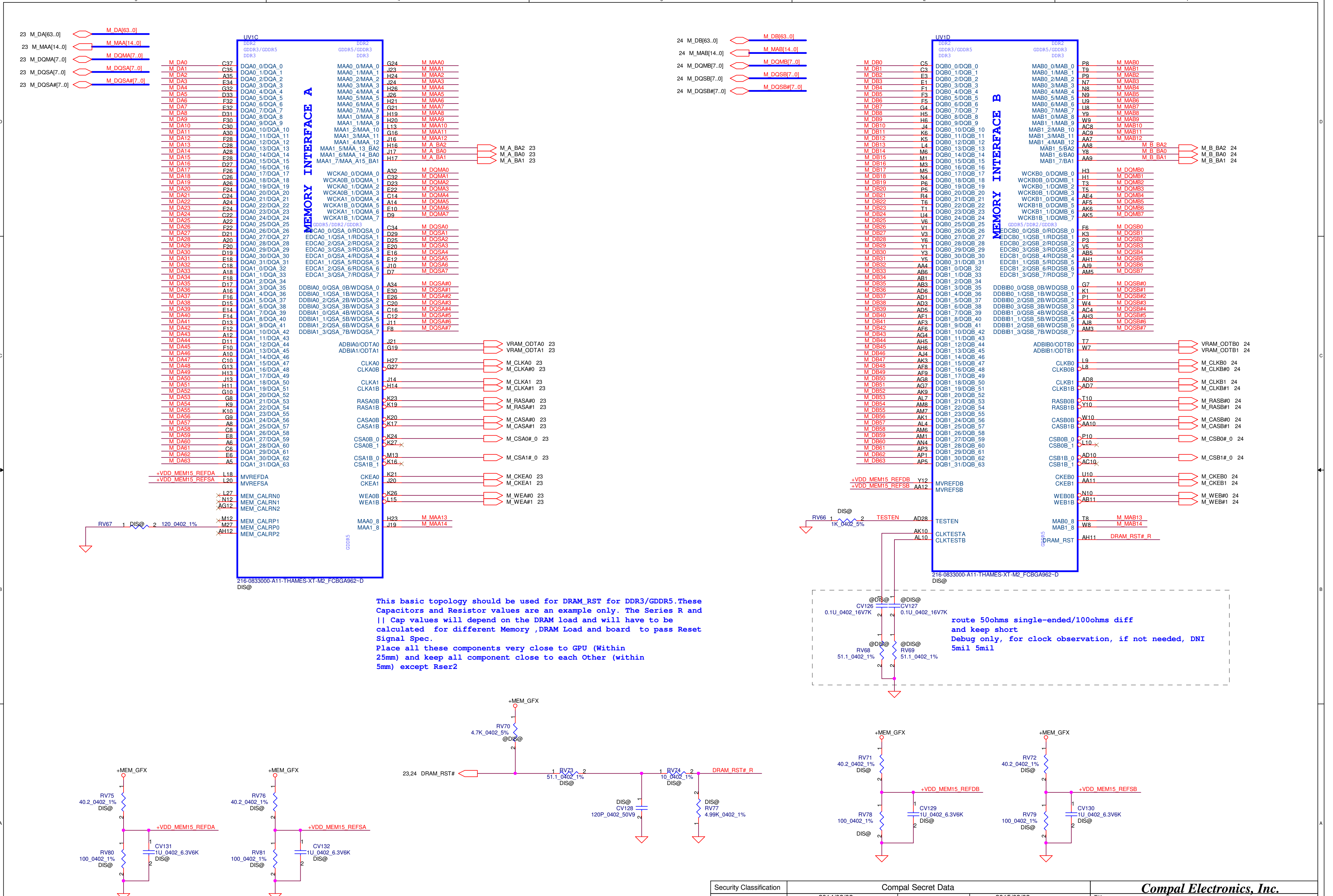
Size: Custom | Document Number: **LA-B131P** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 20 of 52



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: Venus XTX(5/8) Power			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 21 of 52		



This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors or Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

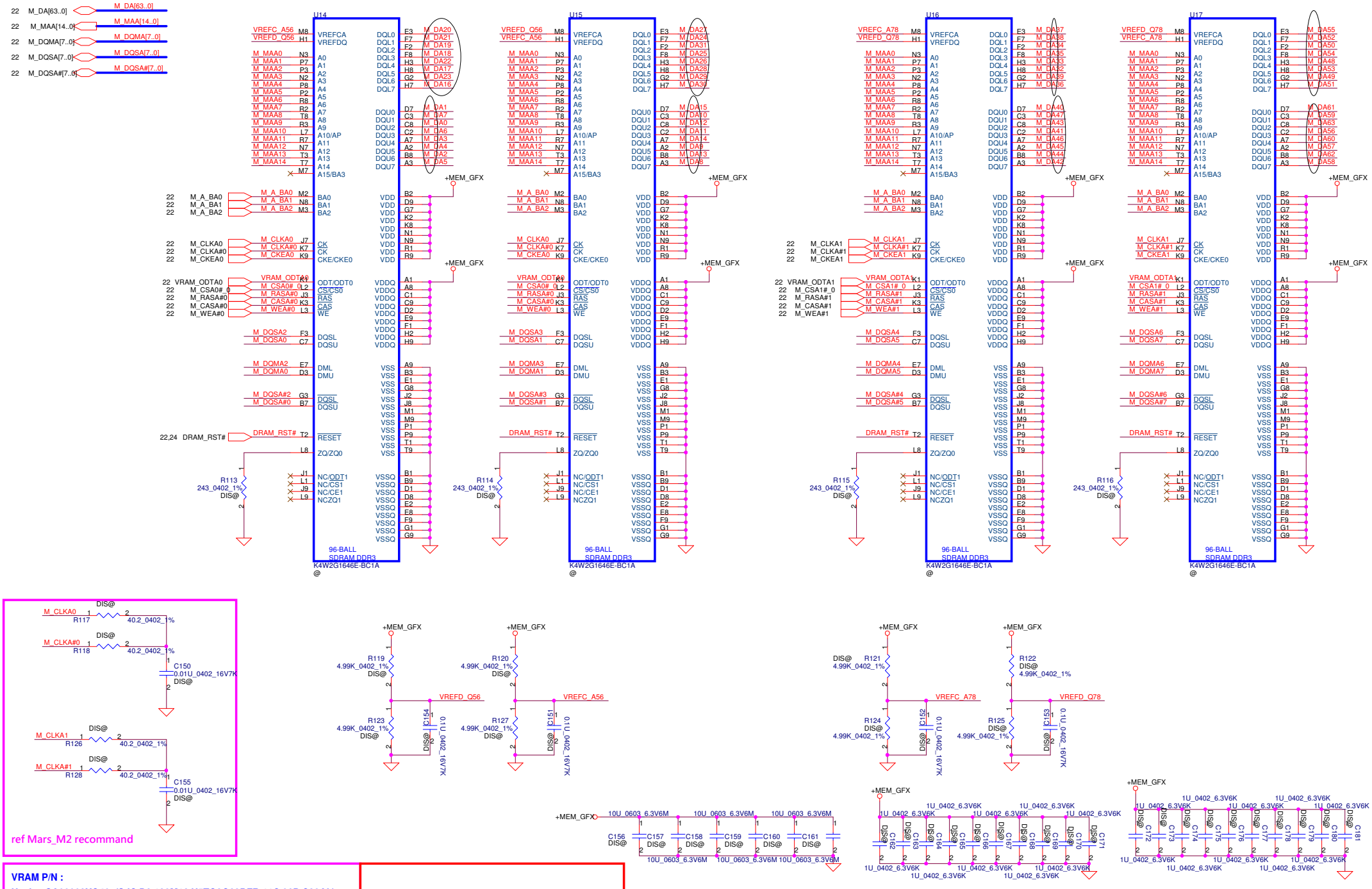
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

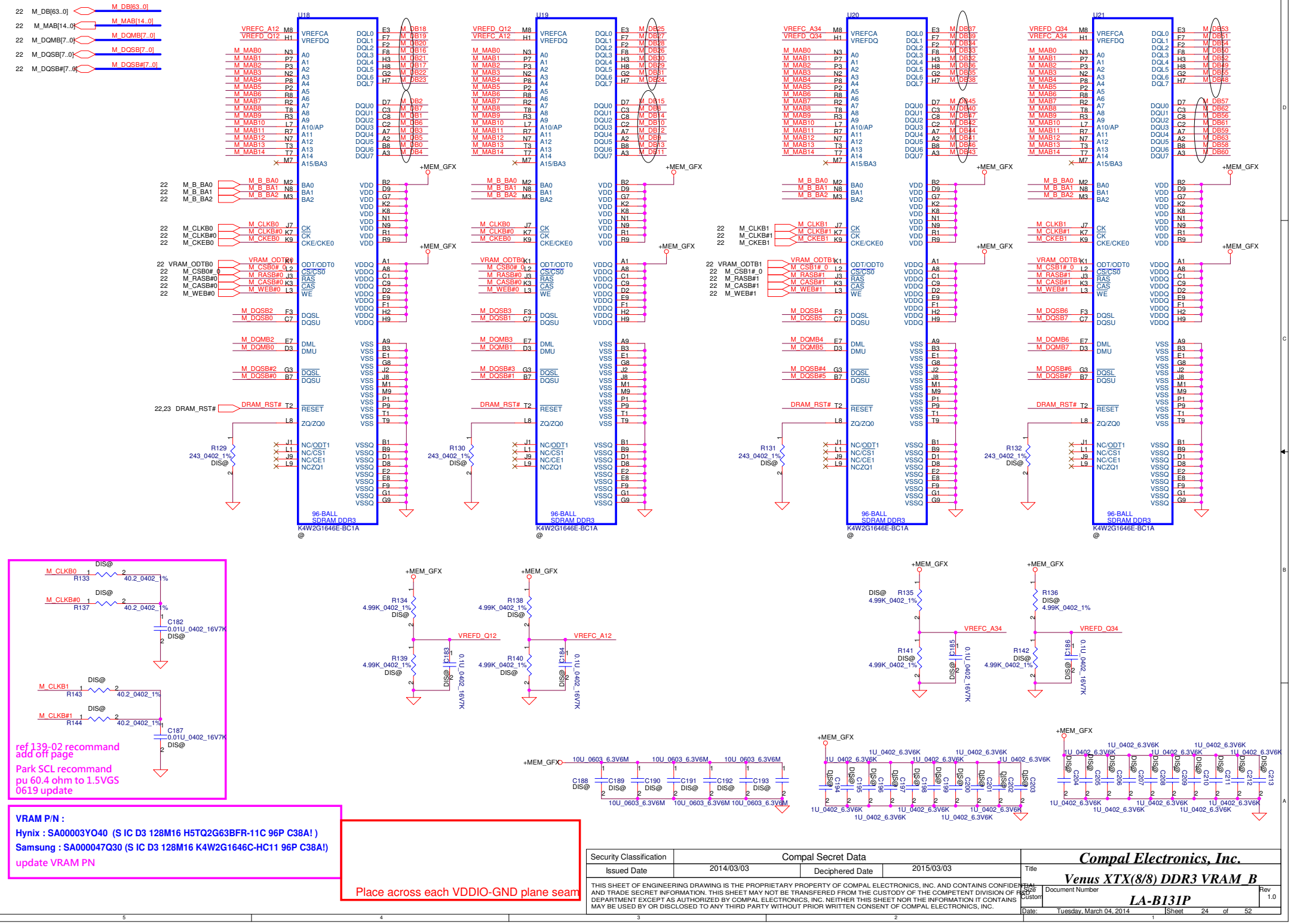
Title: Venus XTX(6/8)MEM Interface

Size: Custom | Document Number: LA-B131P | Rev: 1.0



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.		
Title: Venus XTX(7/8) DDR3 VRAM_A		
Size: Custom	Document Number: LA-B131P	Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 23 of 52	



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **Venus XTX(8/8) DDR3 VRAM_B**

Size	Document Number	Rev
Custom	LA-B131P	1.0

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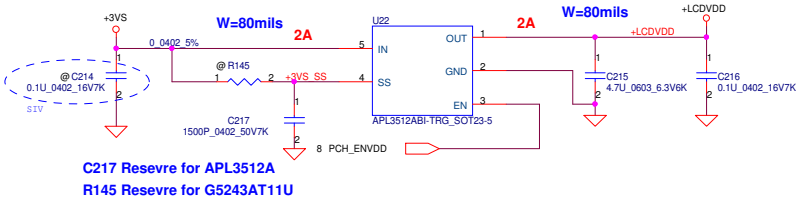
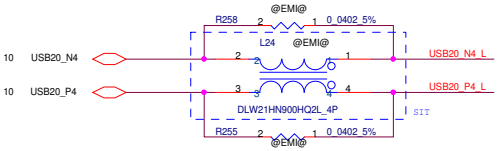
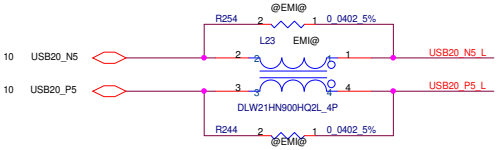
LCD POWER CIRCUIT



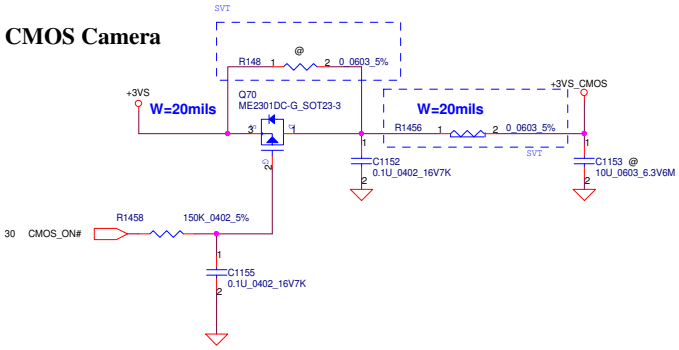
C217 Resevre for APL3512A

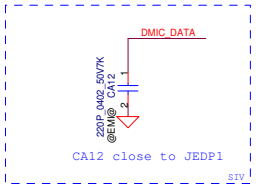
R145 Resevre for G5243AT11U

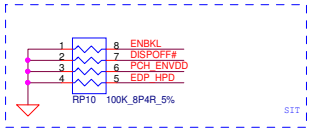




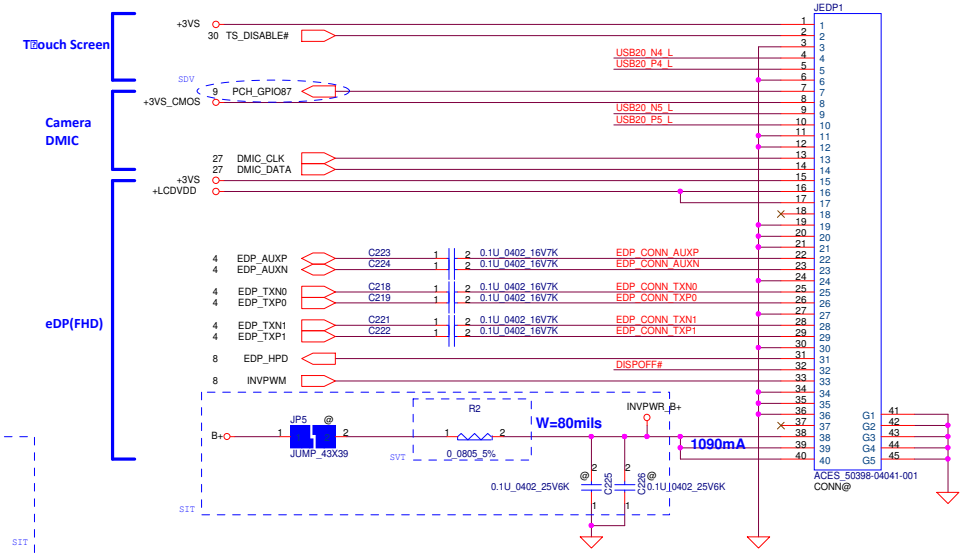
CMOS Camera

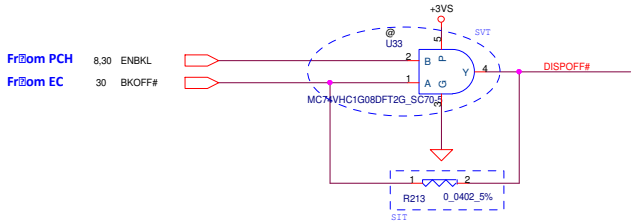


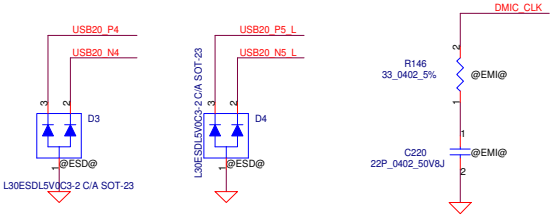




eDP(FHD) + TOUCH + Camera







Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: eDP LCD / Camera / Touch

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 25 of 52

RTL8111GS	L7	C230 C232	C298 C237	R147	C229
SWR mode	O	O	O	X	X

RTL8111G	L7	C230 C232	C298 C237	R147	C229
LDO mode	X	X	X	O	O

+3_LAN Rising time (10%~90%) >1mS and <100mS

+3VALW — W=60mils — J2 @ JUMP_43X39 — 370mA — +3V_LAN

GCLK (RG6 close to Y3.1)

34 LAN_XTLI_GCLK — RG6 0_0402_5% SVT — XTLI

C239 15P_0402_50V8J NOGCLK@ — XTLI

Y3 25MHZ_12PF_7V25000012 NOGCLK@ (GND, GND)

C242 15P_0402_50V8J NOGCLK@ — XTLO

Layout Notice : Place as close chip as possible.

+3V_LAN

C298 SWR@ 4.7U_0603_6.3V6K — C237 SWR@ 0.1U_0402_16V7K

These caps close to U23 : Pin 23

LDO@ R147 0_0603_5%

+LAN_REGOUT W=60mils

LDO@ C229 0.1U_0402_16V7K

L7 SWR@ 2.2UH +-5% NLC252018T-2R2J-N

SWR@ C230 4.7U_0603_6.3V6K

SWR@ C232 0.1U_0402_16V7K

(Should be place within 200 mils)

These components close to U23 : Pin 24

LDO mode

SWR mode

+LAN_VDD10 W=60mils

C231 1U_0402_6.3V6K @ — C233 C234 C235 C236 0.1U_0402_16V7K

close to pin 22

These components close to U23 : Pin 3,8,22,30

1uF reserved on Pin 22

+3V_LAN

C222 4.7U_0603_6.3V6K @ — C227 0.1U_0402_16V7K @ — C228 C223 0.1U_0402_16V7K

These caps close to U23 : Pin 11,32

DVDD33

U23

MDI0+ 1 — MDI0- 2 — +LAN_VDD10 3 — MDI1+ 4 — MDI1- 5 — MDI2+ 6 — MDI2- 7 — +LAN_VDD10 8 — MDI3+ 9 — MDI3- 10 — +3V_LAN 11 — 12

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33 CLKREQB HSIP HSIN REFCLK_P REFCLK_N

7,9 LANCLK_REQ#

10 PCIE_PTX_C_DRX_P3

10 PCIE_PTX_C_DRX_N3

7 CLK_PCIE_LAN

7 CLK_PCIE_LAN#

HSOP 17 — HSON 18 — PERSTB 19 — ISOLATEB 20 — MDIP1 21 — LANWAKEB 22 — DVDD10 23 — VDDREG 24 — REGOUT 25 — LED2 26 — LED1/GPIO 27 — LED0 28 — CKXTAL1 29 — CKXTAL2 30 — AVDD10 31 — RSET 32 — AVDD33 33 — GND

These caps close to U11

PCIE_PRX_C_DTX_P3 C240 0.1U_0402_16V7K PCIE_PRX_DTX_P3

PCIE_PRX_C_DTX_N3 C241 0.1U_0402_16V7K PCIE_PRX_DTX_N3

PCIE_PRX_DTX_P3 10

PCIE_PRX_DTX_N3 10

PLT_RST# 8,17,29,30,33

ISOLATEB

PCIE_LAN_WAKE# 29,30

+LAN_VDD10 — +3V_LAN — +LAN_REGOUT

T89 — T90

LED1_GPIO — RL17 @ 10K_0402_5%

+3V_LAN

reserved GPIO pin

XTLO — XTLI — +LAN_VDD10 — LAN_RSET — +3V_LAN

R152 2.49K_0402_1%

RTL8111GUL-CG QFN 32P

SA00006ML10

+3VS — R149 1K_0402_5% — ISOLATEB — R153 15K_0402_5%

TS1

TCT — MCT

MDI0+ 2 — MDI0- 3 — MDI1+ 5 — MDI1- 6 — MDI2+ 8 — MDI2- 9 — MDI3+ 11 — MDI3- 12

TCT1 TD1+ TD1- TCT2 TD2 TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-

MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-

MDO0+ 23 — MDO0- 22 — MDO1+ 20 — MDO1- 19 — MDO2+ 17 — MDO2- 16 — MDO3+ 14 — MDO3- 13

NS892407 1G

SP050006800

SIV

C292 0.01U_0402_16V7K

R168 75_0805_5% — EMI@ C290 10P_0603_50V8-J — CHASSIS1_GND

DL2 BS4200N-C-LV_SMB-F2 EMI@ SCV00001D00

D5 EMI@ — MDI1- — MDI1+ — MDI3+ — MDI3-

RCLAMP3304N.TCT_SLP2626P10-10

Place Close to TS1

D6 EMI@ — MDI0- — MDI0+ — MDI2+ — MDI2-

RCLAMP3304N.TCT_SLP2626P10-10

Place Close to TS1

SIV (EMI suggestion)

JRJ1 CONN@

MDO0+ 1 — MDO0- 2 — MDO1+ 3 — MDO2+ 4 — MDO2- 5 — MDO1- 6 — MDO3+ 7 — MDO3- 8

PR1+ PR1- PR2+ PR3+ PR3- PR2- PR4+ PR4-

GND 12 — GND 11 — GND 10 — GND 9

CHASSIS1_GND

SANTA_130460-3

DC231112261

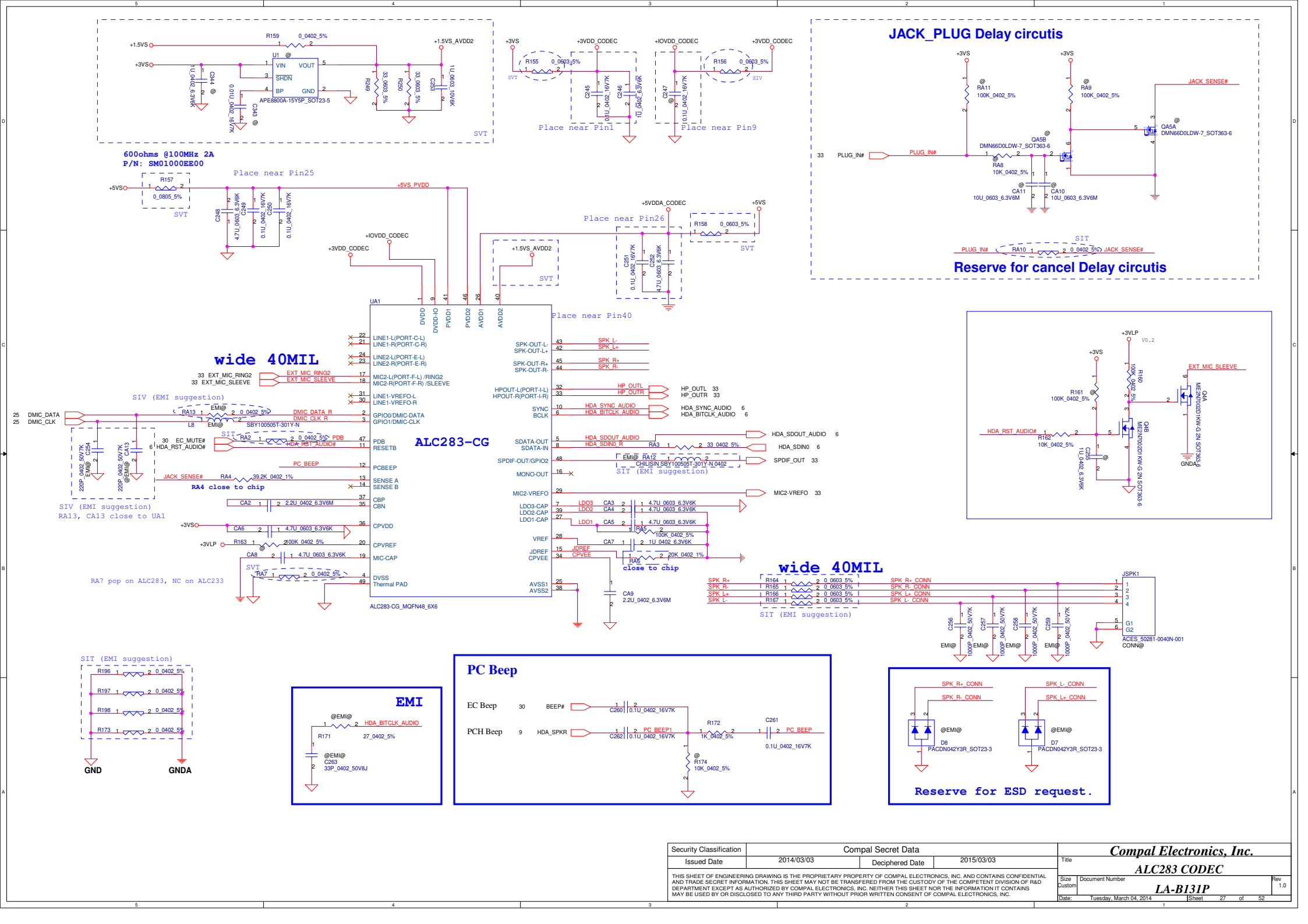
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: LAN_RTL8111G-CG

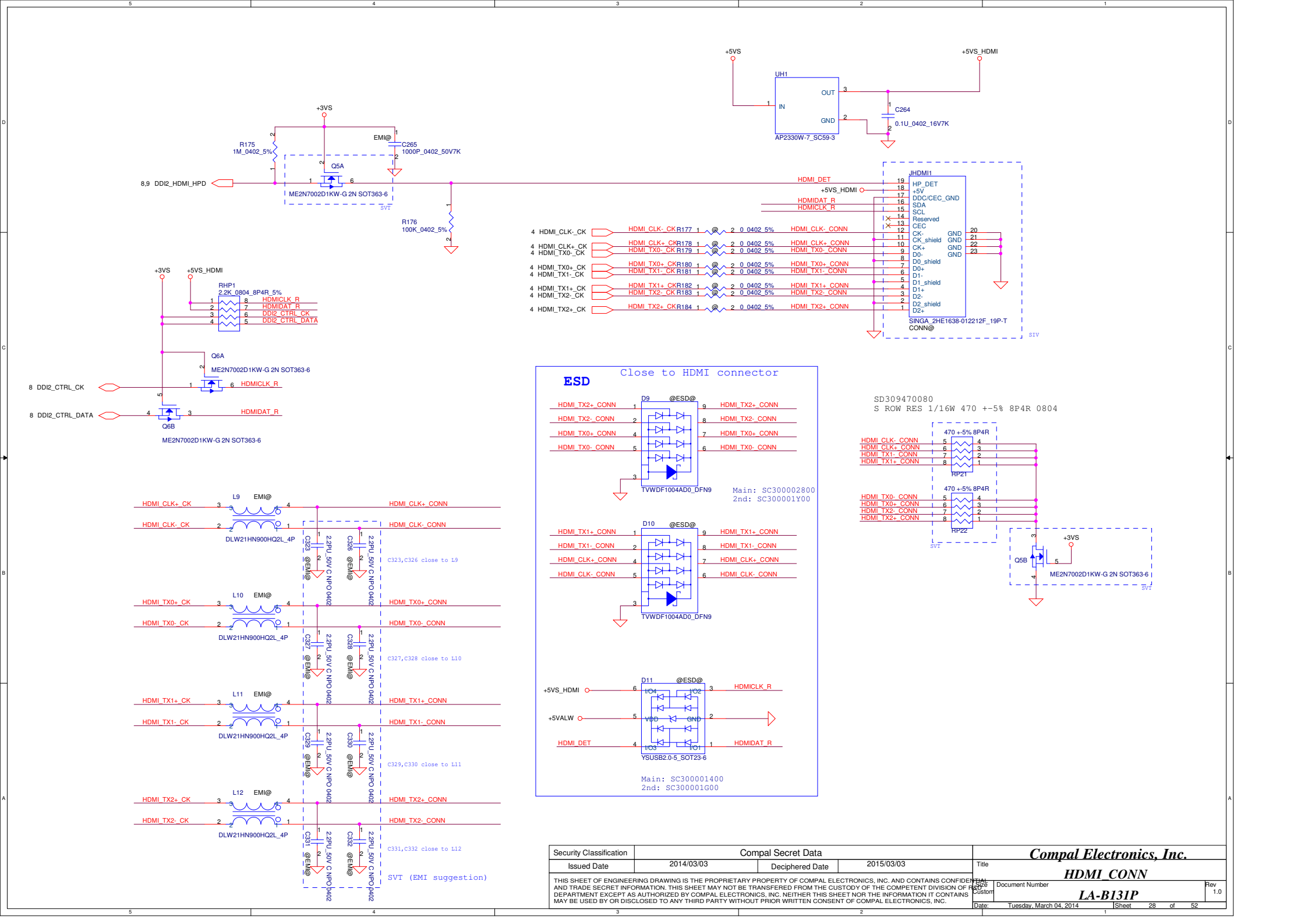
Size: Custom — Document Number: LA-B131P — Rev: 1.0

Date: Tuesday, March 04, 2014 — Sheet 26 of 52



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	ALC283 CODEC		
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 27 of 52		



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Title	Compal Electronics, Inc.		
	HDMI_CONN		
Size: Custom	Document Number: LA-B131P		Rev: 1.0
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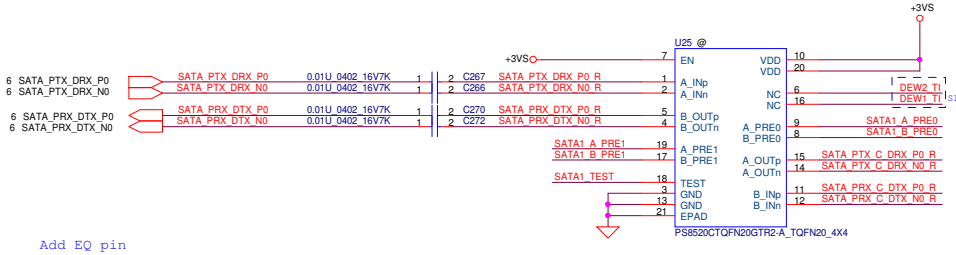
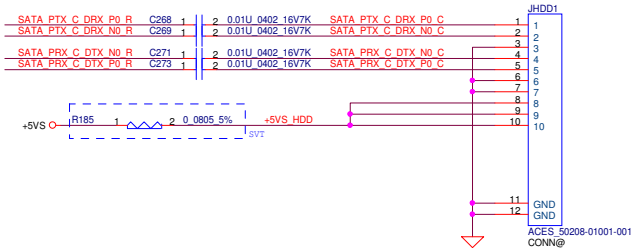
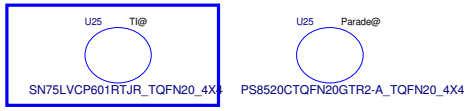
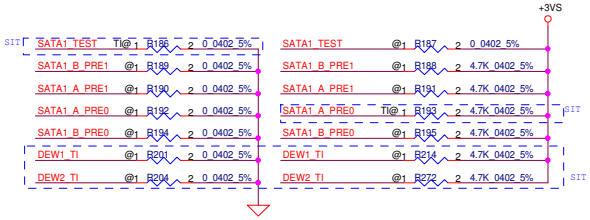
SATA HDD (SSD) CONN.

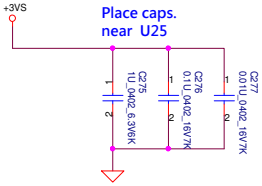


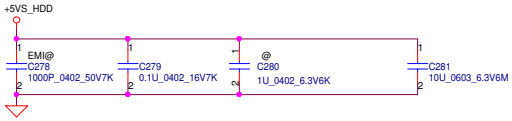


Add EQ pin

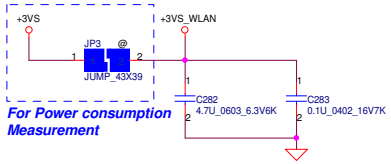


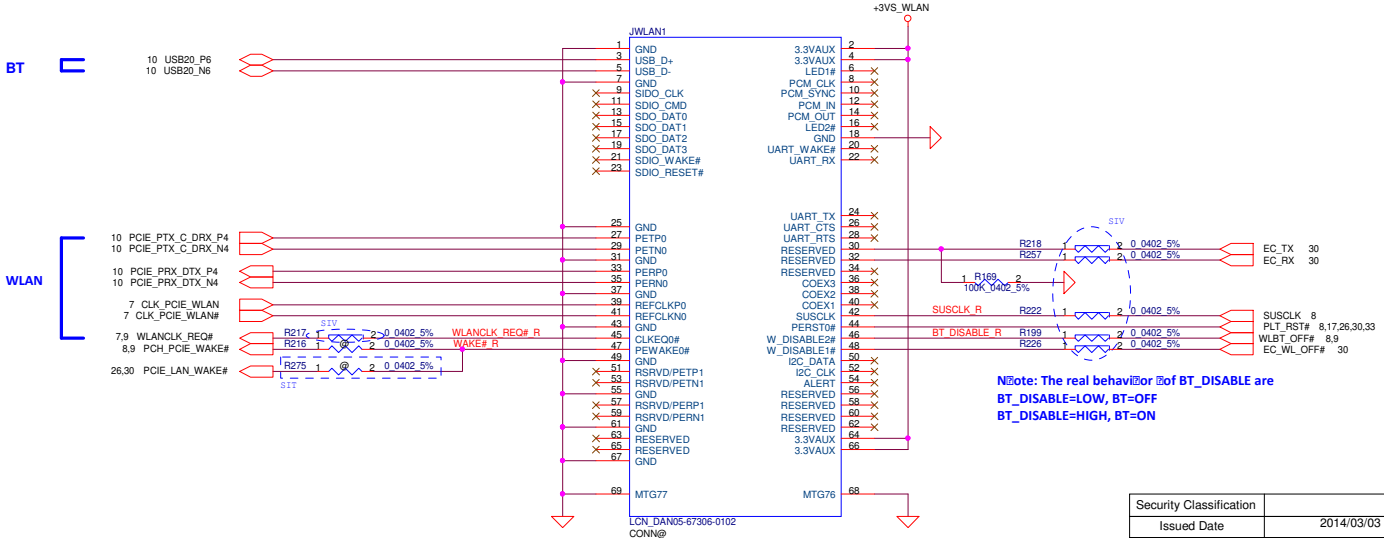






NGFF for WLAN+BT





Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	HDD/NGFF(WLAN+BT)		
Size: Custom	Document Number: LA-B131P		Rev: 1.0
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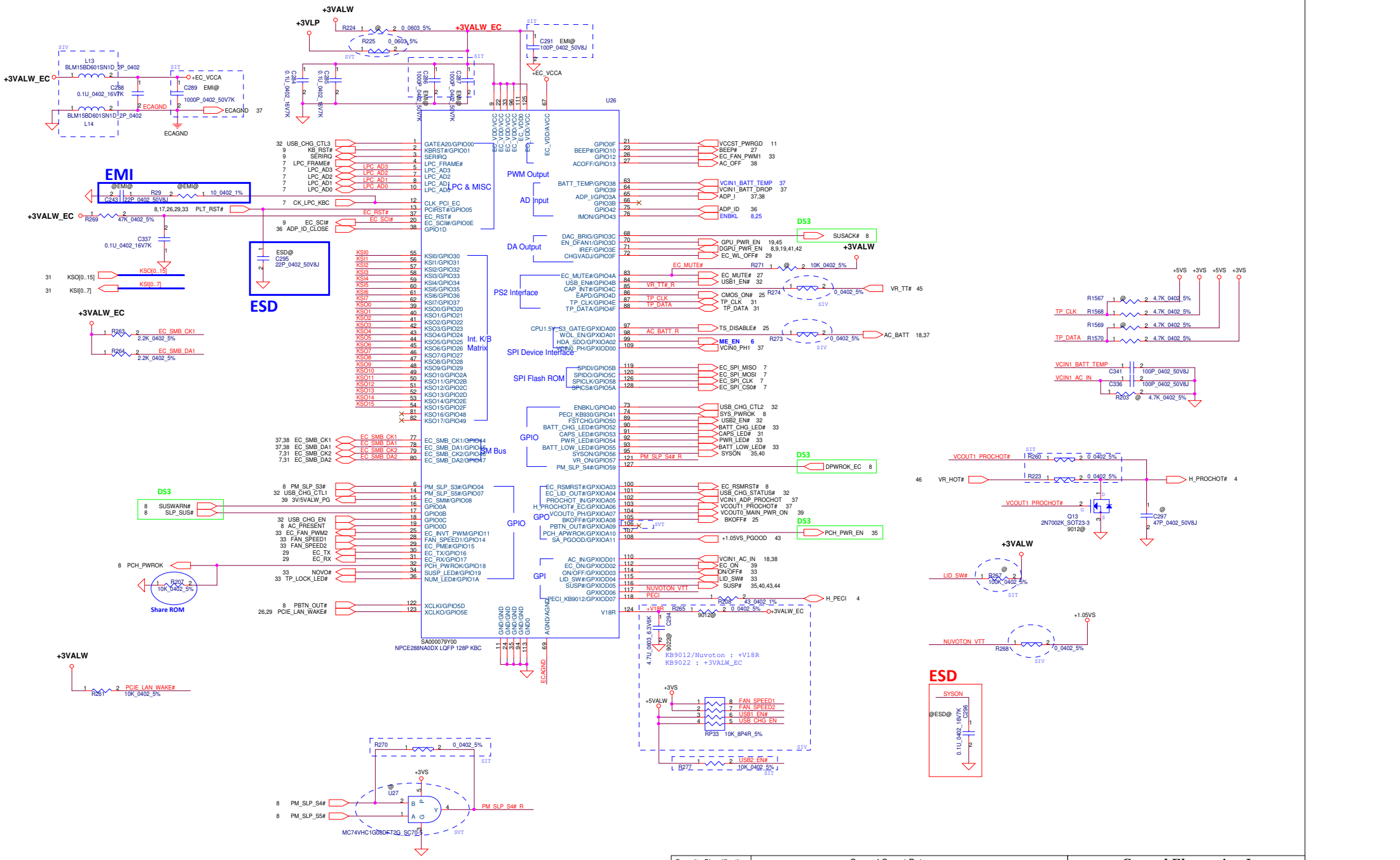

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.	
Title	BIOS & EC I/O Port
Size	C
Document Number	LA-B131P
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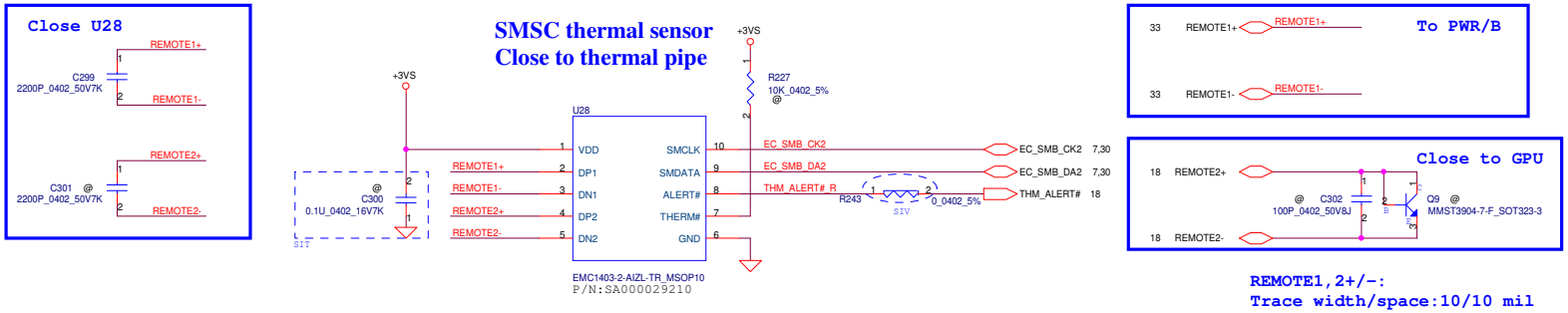
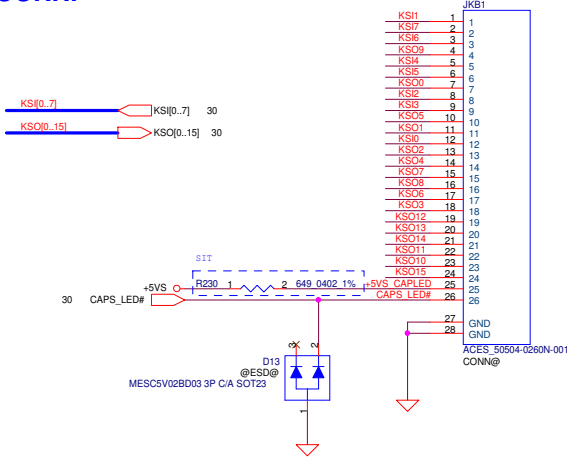
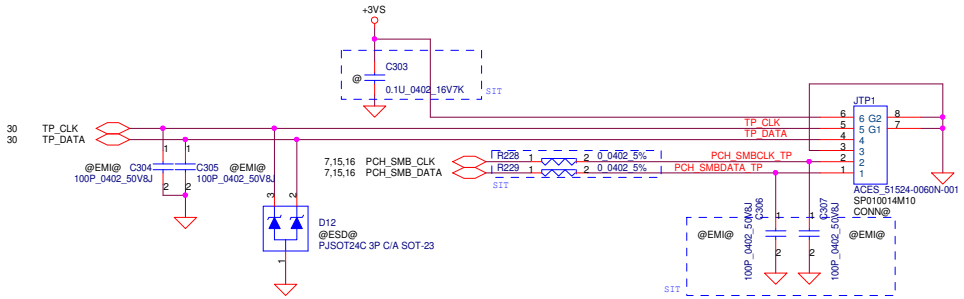
Thermal Sensor



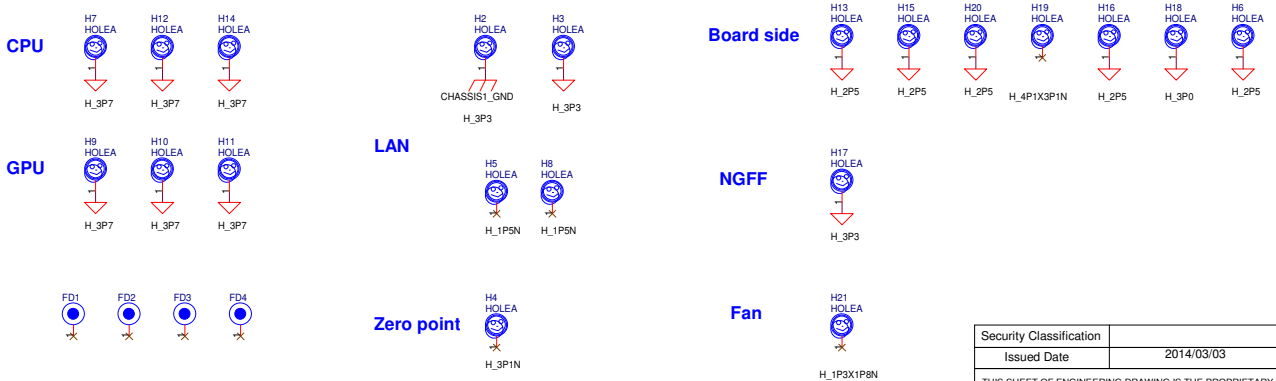
KB CONN.



TP CONN.



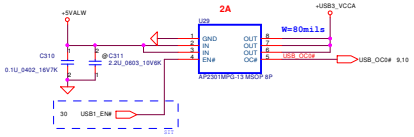
Screw

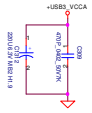


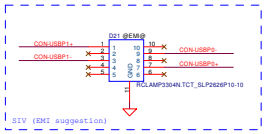
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

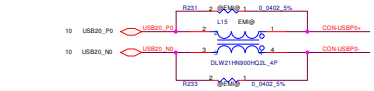
Compal Electronics, Inc.			
Title: KB/TP/Thermal Sensor			
Size: Custom	Document Number: LA-B131P		Rev: 1.0
Date: Tuesday, March 04, 2014	Sheet 31 of 52		

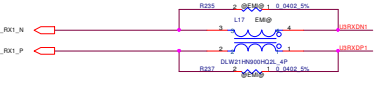
USB3.0 <Port1>

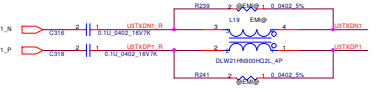


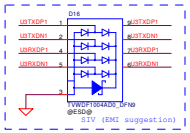


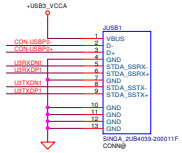




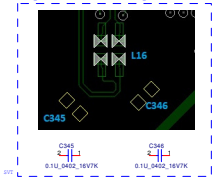








Pseudo Cap(C345, C346) to protect L16



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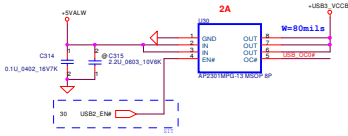
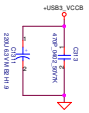
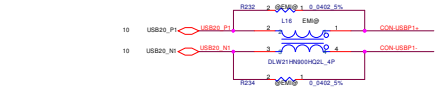
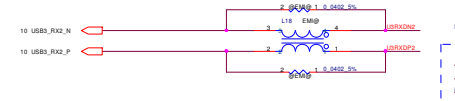
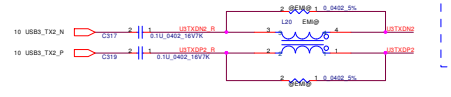
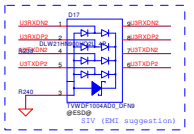


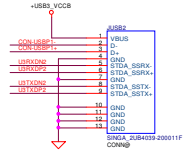




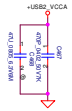


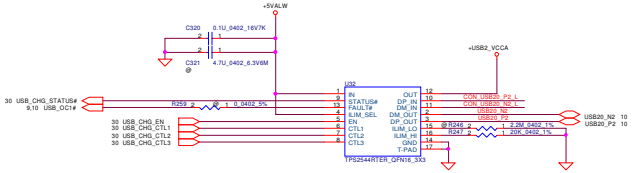


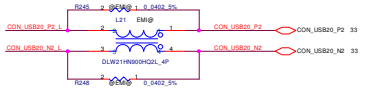




USB2.0 + Charger







Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	USB2.0/3.0		
Size	Document Number		Rev
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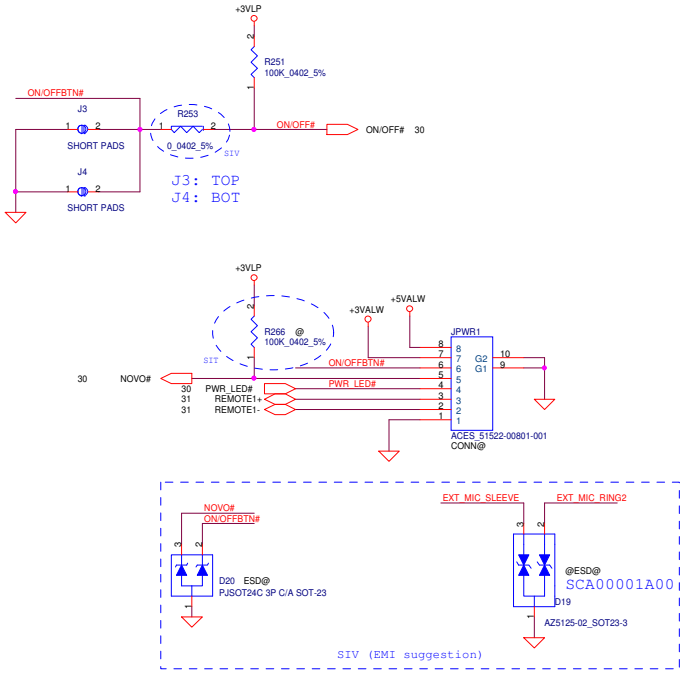
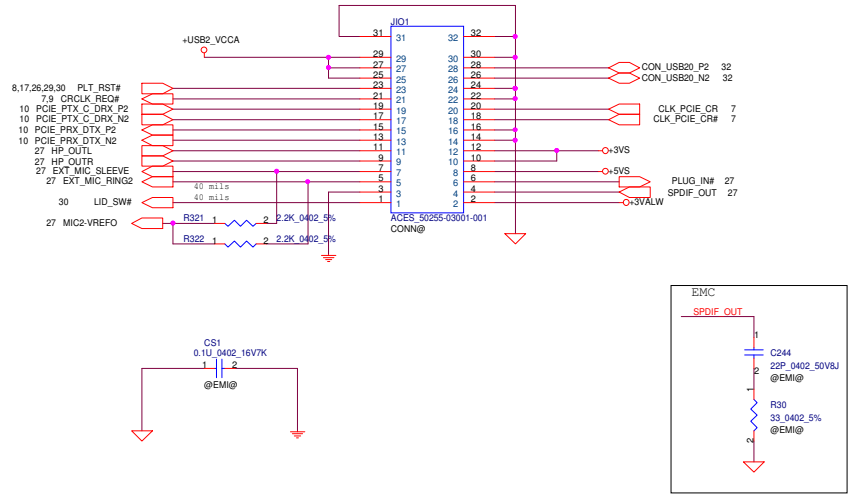
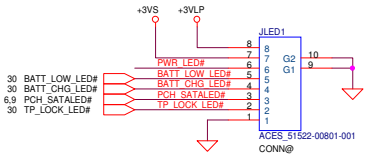
Power Board CONN.



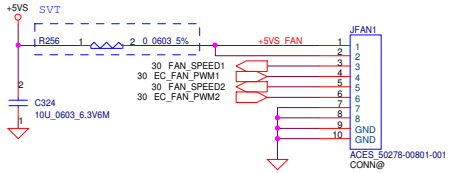
I/O Board CONN.

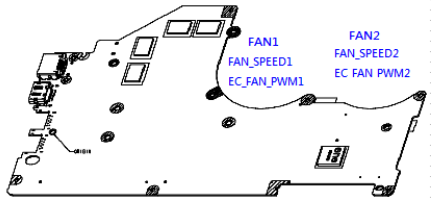


LED Board CONN.



FAN1 Conn





FAN1	FAN2
FAN_SPEED1 EC_FAN_PWM1	FAN_SPEED2 EC_FAN_PWM2

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.	
Title	FAN/PWR/LED/IO Board
Size: C	Document Number: LA-B131P
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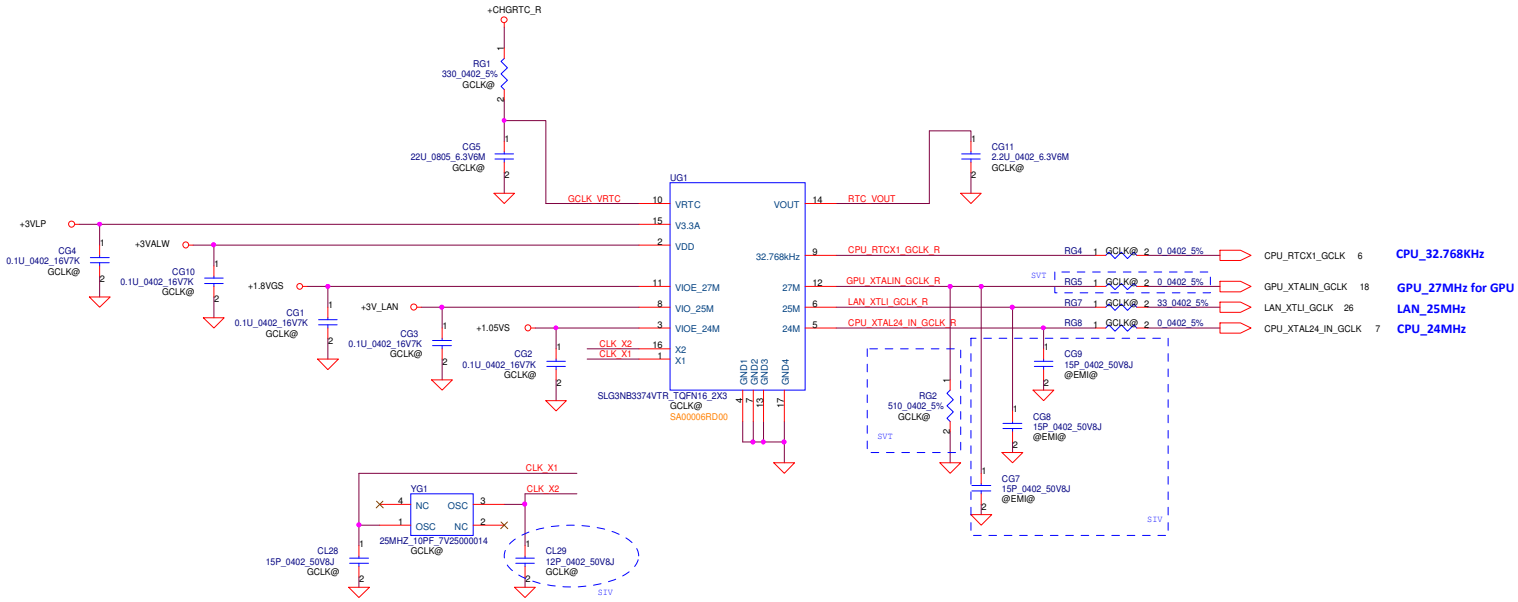
Date: Tuesday, March 04, 2014	Sheet 33 of 52



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **GCLK**

Size	Document Number	Rev
	LA-B131P	1.0

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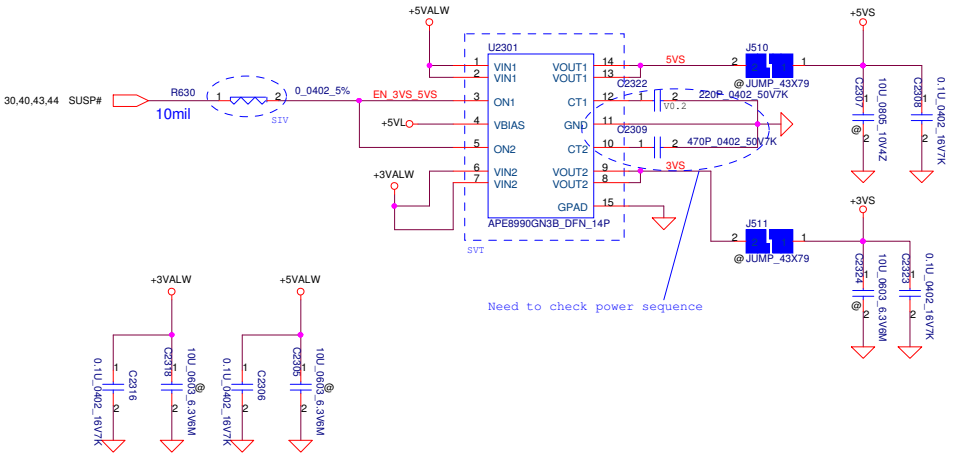
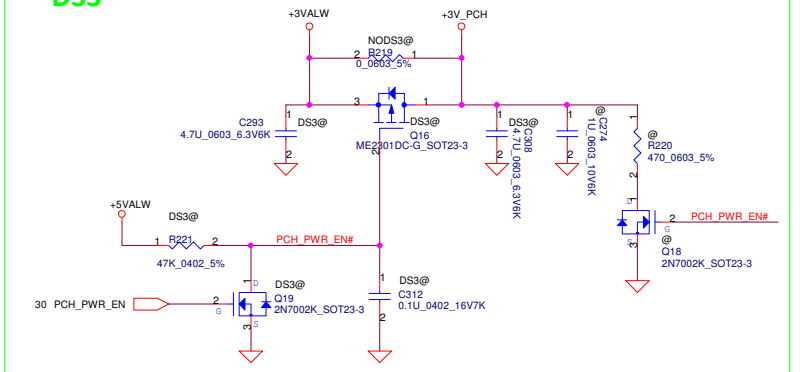
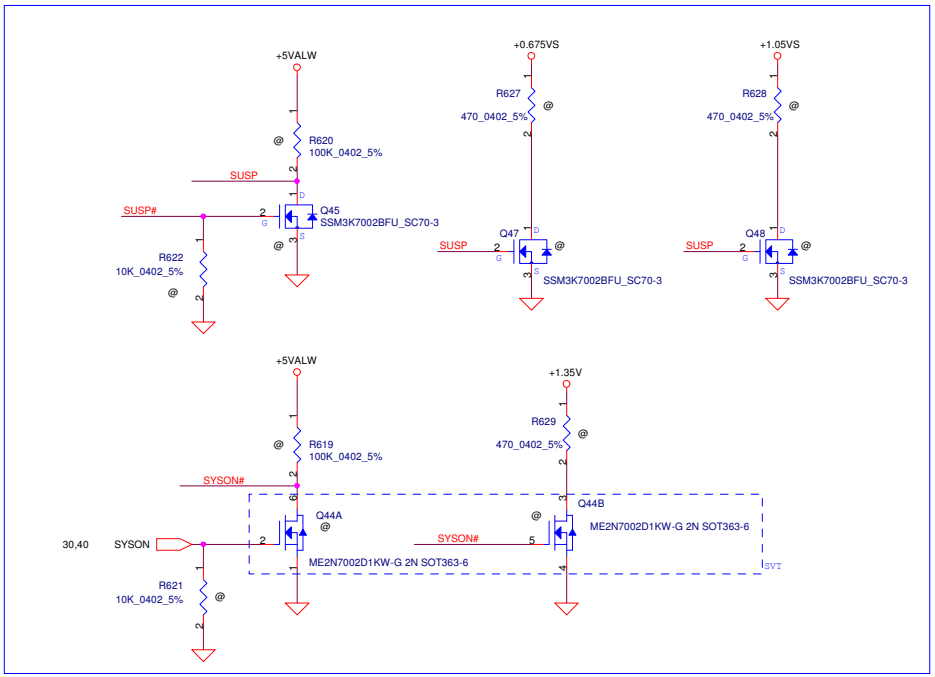
+5VALW TO +5VS
+3VALW TO +3VS



DS3

+3VALW t?o +3V_PCH





Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: DC/DC Interface

Size	Document Number	Rev
Custom	LA-B131P	1.0

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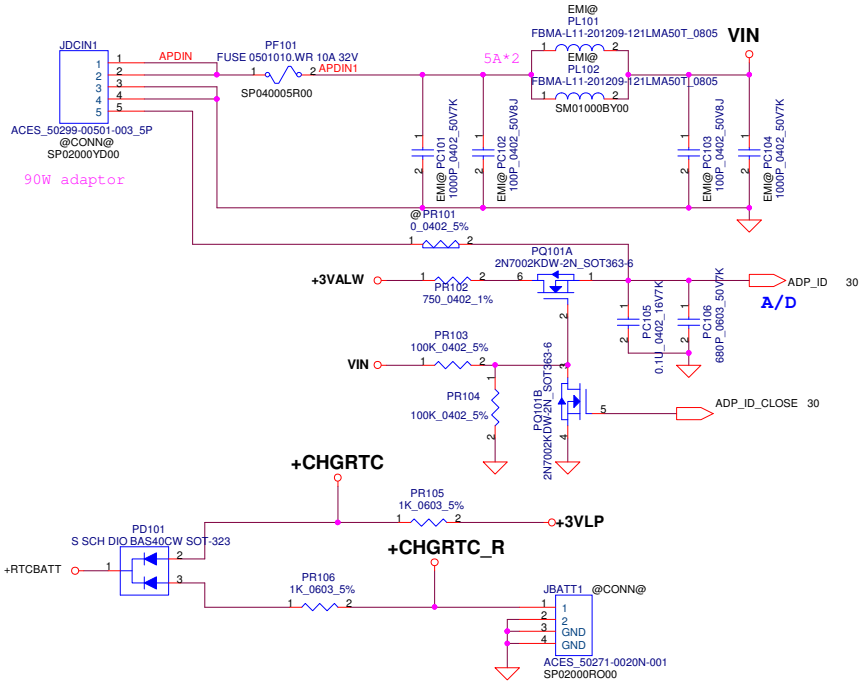

RTC Battery

GC02001DR00
BATT CR2032 3V 210MAH MB 5 W/C 30MM

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

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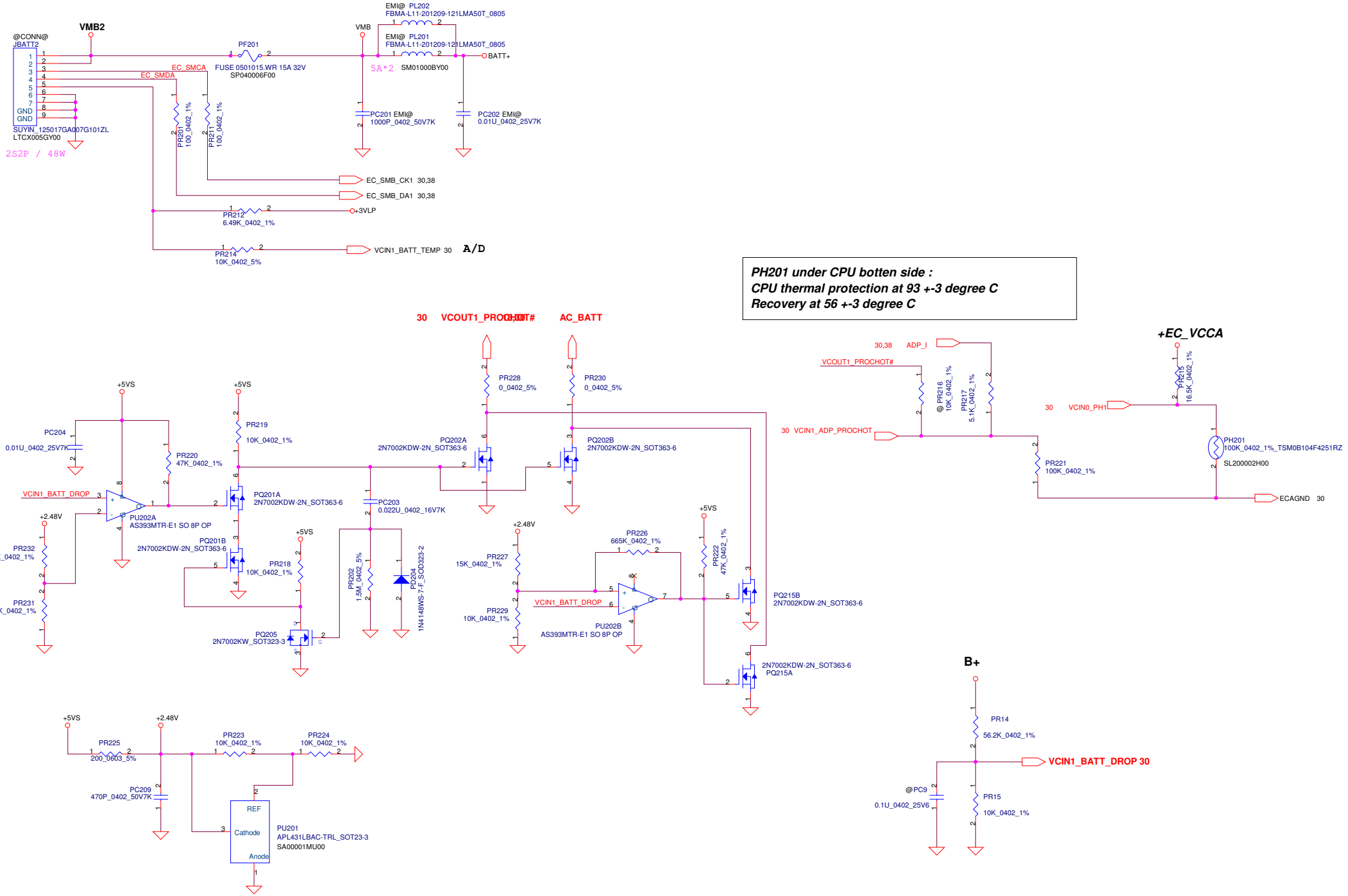

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	BE_BDW	1.0
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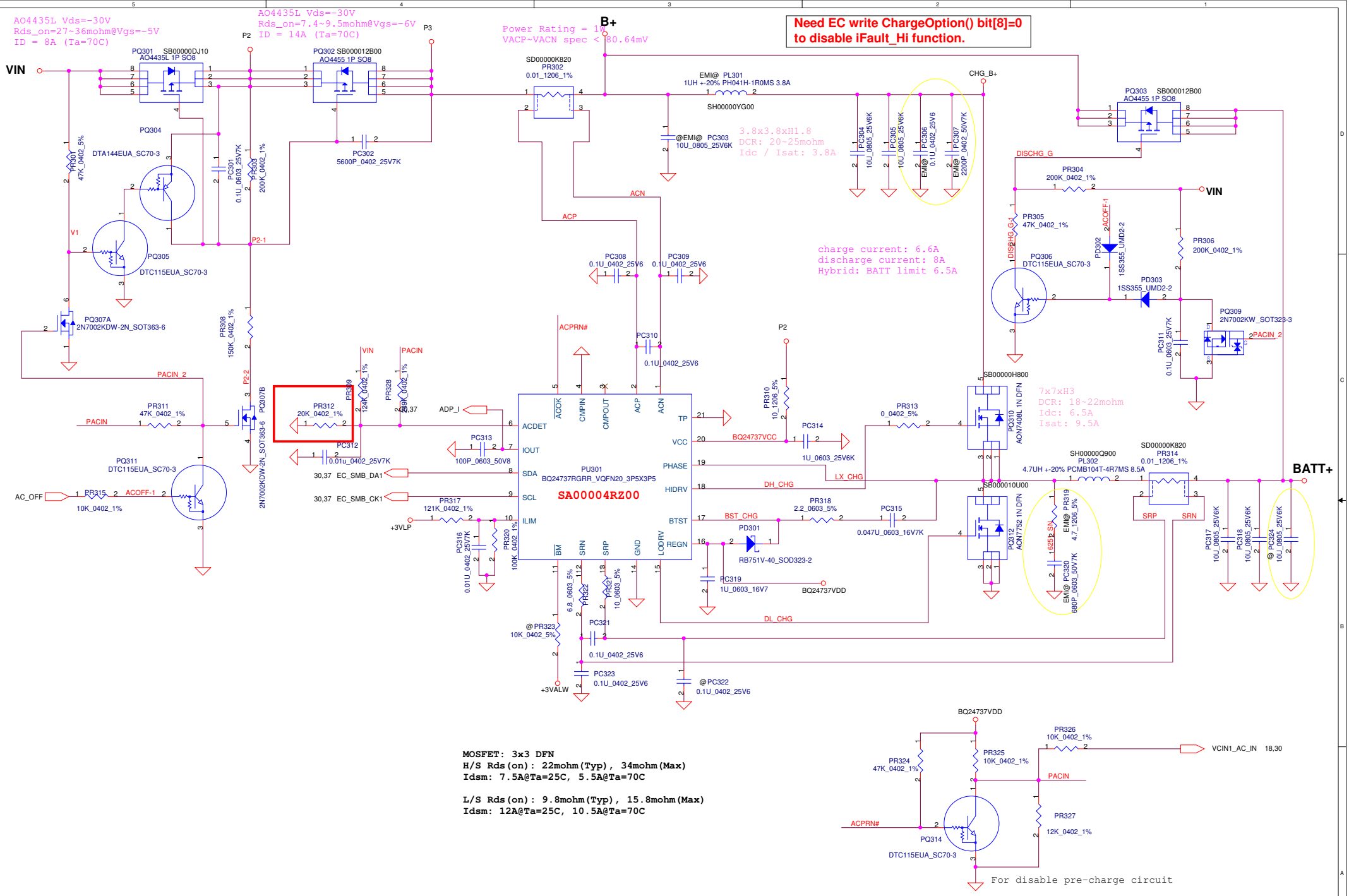
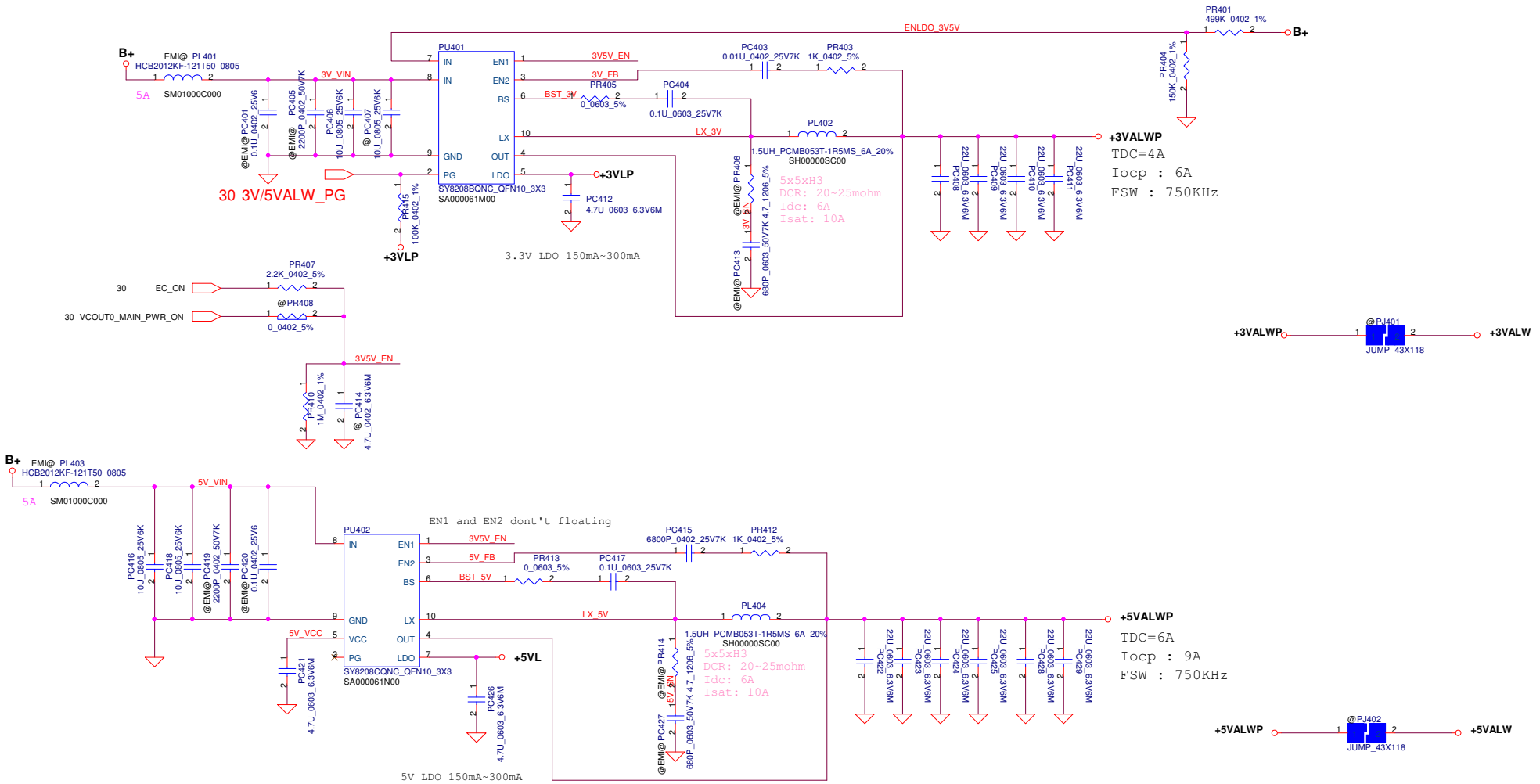


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	Charger_BQ24737		
Size	Document Number		Rev
	BE_BDW		1.0
Date: Tuesday, March 04, 2014	Sheet 38 of 52		



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: BE_BDW | Rev: 1.0

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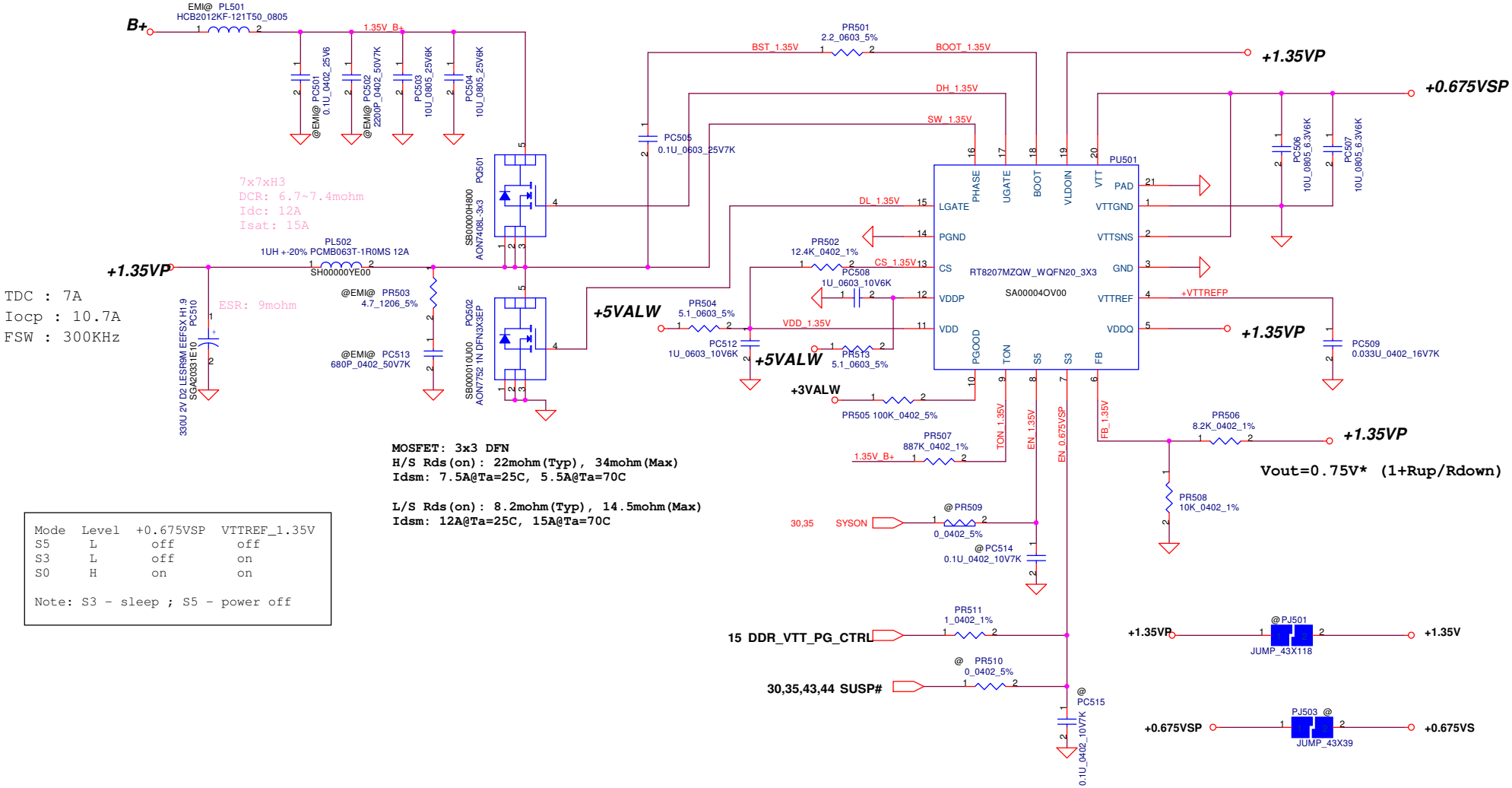

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: RT8207M

Size: Custom | Document Number: BE_BDW | Rev: 1.0

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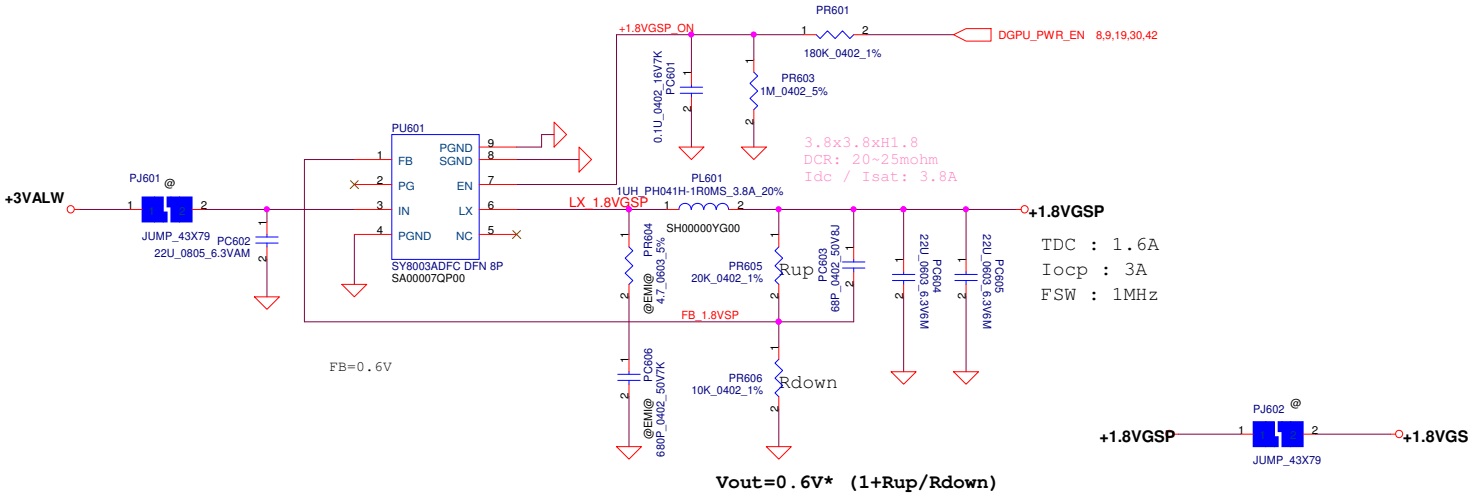

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **+1.8VGS**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

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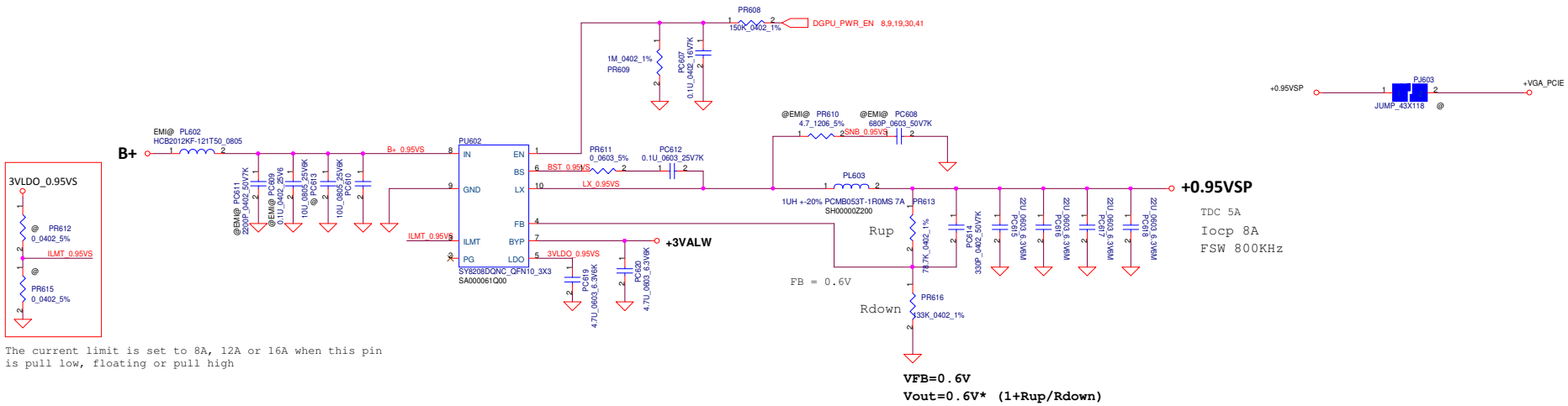

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **0.95VS**

Size	Document Number	Rev
C	BE_BDW	1.0

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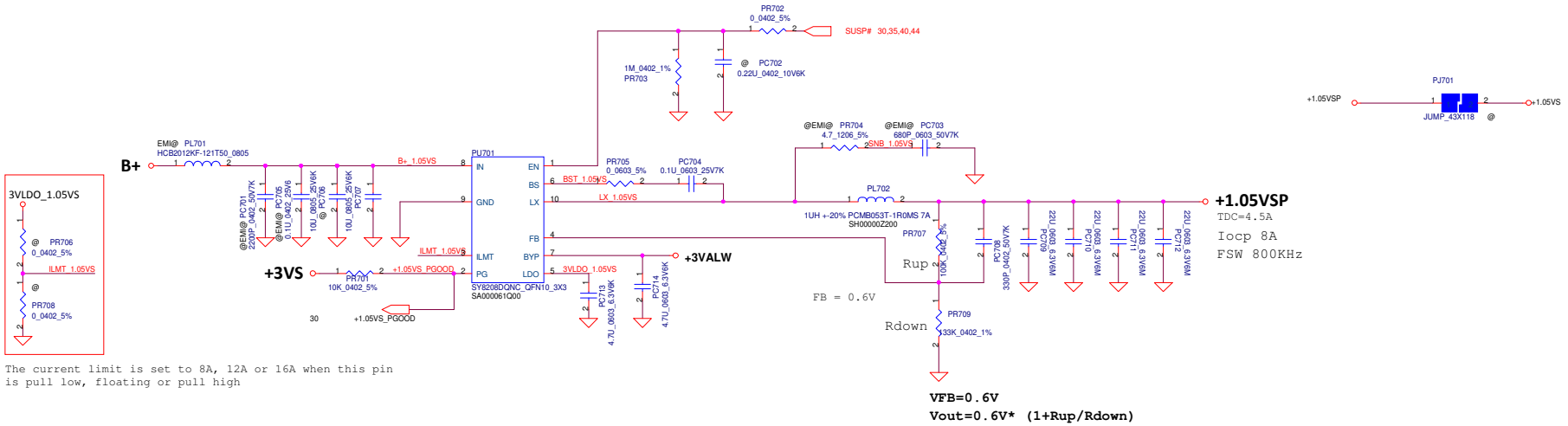


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

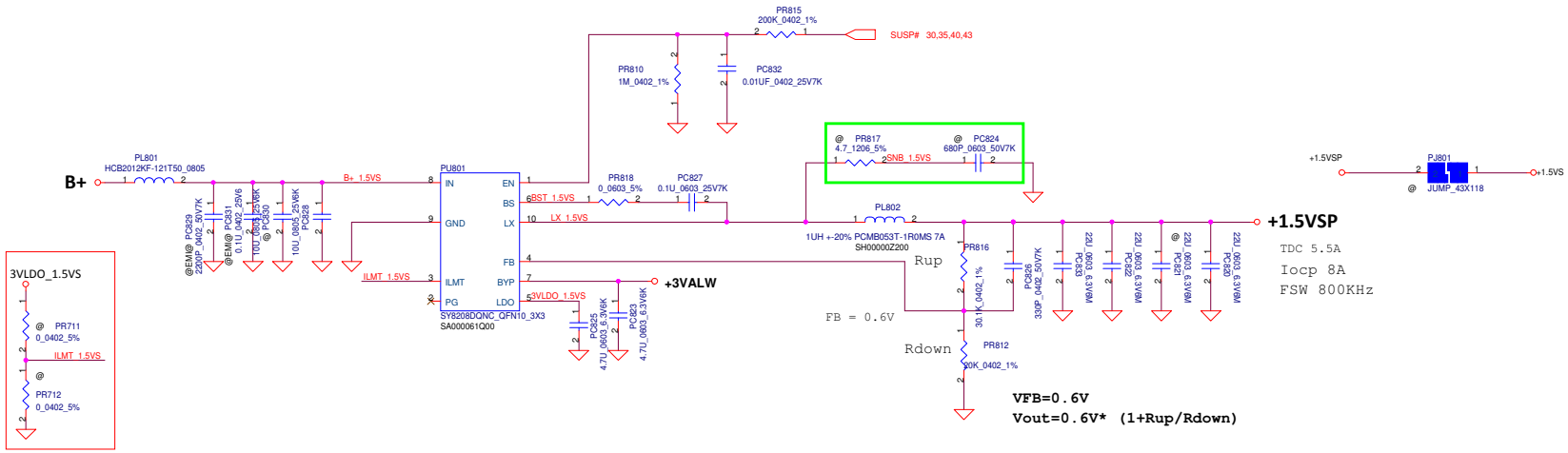
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **+1.05VS**

Size	Document Number	Rev
C	BE_BDW	1.0

Date: Tuesday, March 04, 2014 Sheet 43 of 52



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **+1.5VSP**

Size	Document Number	Rev
C	LA-A321PR01	1.0

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MOSFET: dual N / 5x6 DFN
H/S Rds(on): 5mohm(Typ), 8.5mohm(Max)
Idsm: 22A@Ta=25C, 17A@Ta=70C

L/S Rds(on): 2.4mohm(Typ), 3.2mohm(Max)
Idsm: 36A@Ta=25C, 29A@Ta=70C

Vboot regulation

7x7xH3
DCR: 0.98mohm
Idc / Isat: 28A

Venus / XTX (45W)
Maximum Current: 52A
Peck Current: 78A
OCP setting: 93.6A
Frquency: 450KHz
Load line: 1.5mV/A

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.

Title: ISL62883C

Size | Document Number | Rev 1.0

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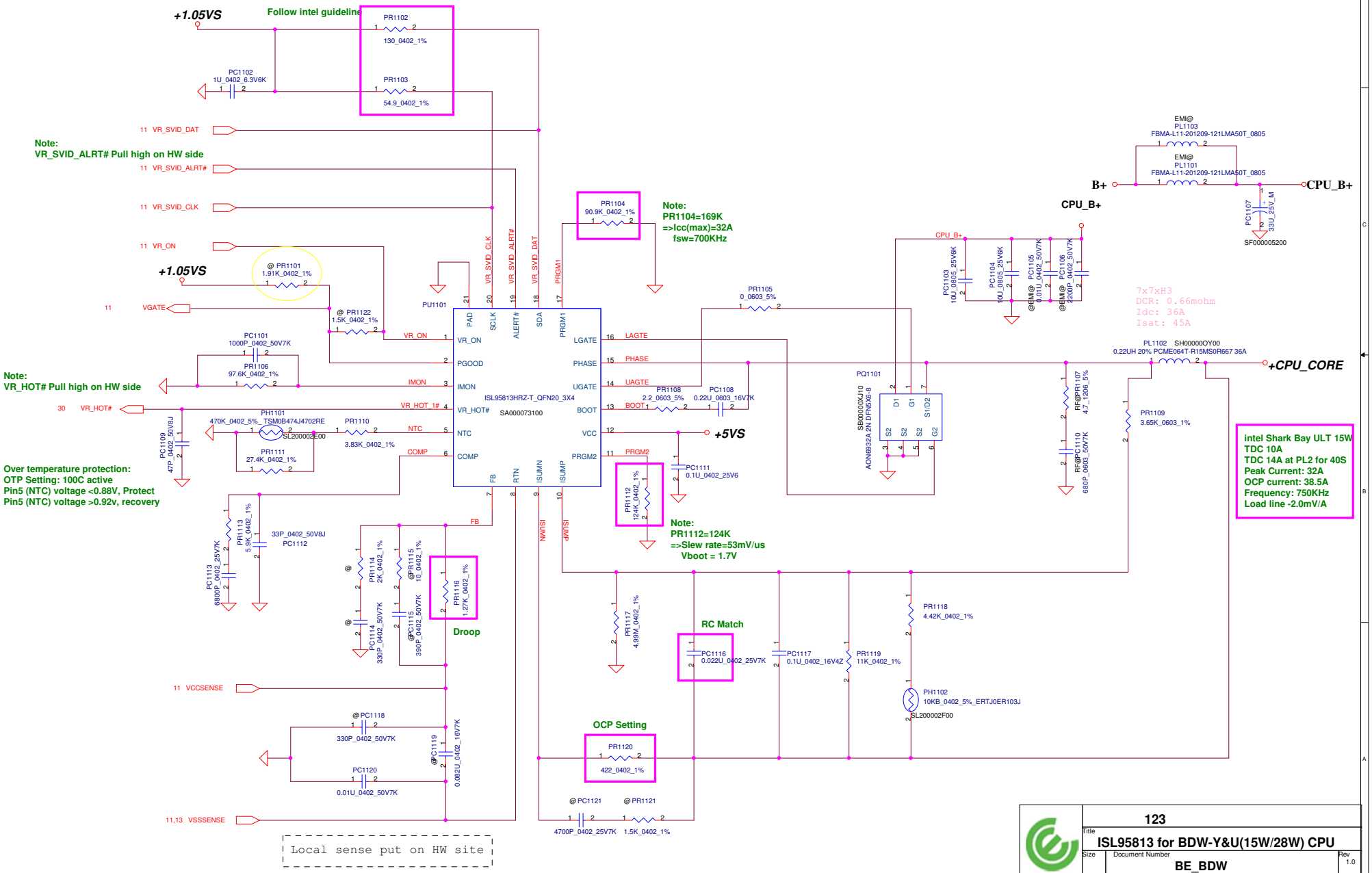

	123	
Title	ISL95813 for BDW-Y&U(15W/28W) CPU	
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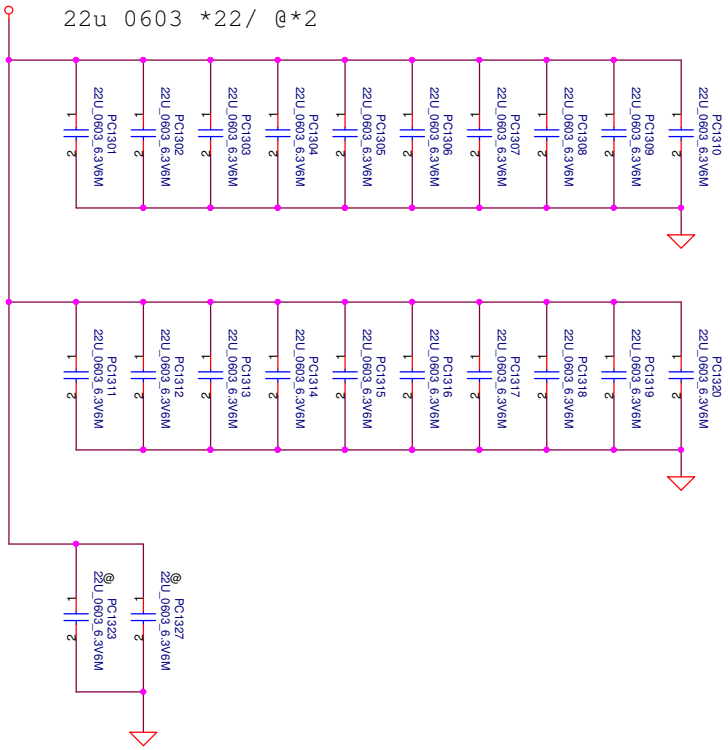
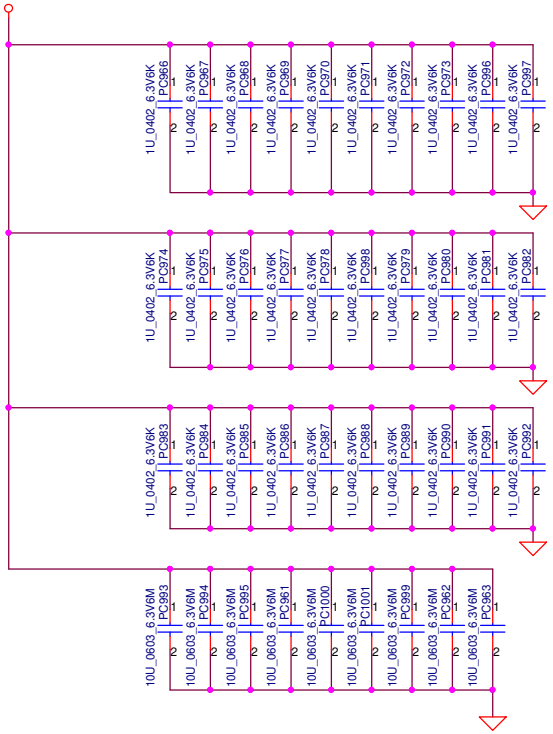
+CPU_CORE



+VGA_CORE



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: **PWR-PROCESSOR_DECOUPLING**

Size	Document Number	Rev
Custom	BE_BDW	1.0

Date: Tuesday, March 04, 2014 Sheet 47 of 52

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	link with HW side	45	change net name +3VS_VGA or +3VGS	11/15	SIV
2	modify VCORE setting	46	1. Change the PR1120 from 280 Ohm to 287 Ohm. 2. Change the PR1117 from @ to 4.99MOhm. 3. Change the PR1118 from 2.61kOhm to 4.42kOhm. 4. Change the PC1101 from @ to 1000pF. 5. Change the PR1106 from @ to 97.5kOhm. 6. Change the PR1114 from 2kOhm to @. 7. Change the PC1114 from 330pF to @.	11/15	SIV
3	for RF request	45	PR953, PC935, PR919, PC910, PR938, PC929 change to mount	11/19	SIV
4	for RF request	46	PR1107, PC1110 change to mount	11/19	SIV
5	SIV MEMO	46	PR1101 change to NA	12/24	SIT
6	Valure modify	45	PC916 change to 150p	12/24	SIT
7	AC detect valure setting	38	PR309 is changed from 392K_0402_1% to 124K_0402_1% (SD034124380) PR312 is changed from 59K_0402_1% to 20K_0402_1% (SD034200280) Add a resistor 249K_0402_1% (SD034249380) between pin 6 of PU301 and PACIN. PC312 is changed from 2200pF_0402_25V_X7R to 0.01uF_0402_25V_X7R (SE075103K80)	12/24	SIT
8	for EMI request	38	Add 2caps to GND, Add 1 SNUB (PC320=0603 680pF, PR319=1206 4.7ohm, PC306=0.1uF, PC307=2200pF)	12/24	SIT
9	battery can't be remove	37	del PC206, PD201, PC205, PR307, PQ306, PQ313	12/24	SIT
10	modify VCORE setting	46	Change PR1120 to 422ohm. Change PR1104 to 90.9Kohm.	02/20	SVT
11	modify VCORE setting	47	Add PC1320 22uF.	02/20	SVT

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW design	09	Change U9J.P1 from PCH_GPIO76 to DDI2_HDMI_HPD	10/02	SIV
2	EMI recommend	26	Change D5, D6 from SC300001G00 to SC300001J00 Change D5, D6 from @EMI@ to EMI@	10/29	SIV
3	EMI recommend	27	Change RA12 from SD028000080 to SM01000DF00 Change C254 from SE071220J80 to SE074221K80 Change C254 from @EMI@ to EMI@	10/29	SIV
4	EMI recommend	32	Change D21 from SC300001G00 to SC300001J00	10/29	SIV
5	HW design	07	Change C20 to @ Remove R201	11/06	SIV
6	HW design	11	Change C41, C45 to @	11/06	SIV
7	HW design	15	Change C97,C119,C113,C115,C116 to @ Change C93,C94,C96,C98,C99,C100 to @	11/06	SIV
8	HW design	16	Change C124,C126,C127,C128,C129,C131 to @ Change C149,C143,C144,C147 to @	11/06	SIV
9	HW design	17	Change CV9 to @DIS@	11/06	SIV
10	HW design	25	Change C214 to @ Remove R722,R721	11/06	SIV
11	Vendor recommend	34	Change CL29 form 15p to 12p	11/06	SIV
12	HW design	06	Change R17,R21 to short pad	11/07	SIV
13	HW design	07	Change R24,R25,R26,R27 to RP31 Change R31,R33,R32,R55 to RP32	11/07	SIV
14	HW design	15	Change R101,R102 to short pad	11/07	SIV
15	HW design	16	Change R111,R112 to short pad	11/07	SIV
16	HW design	18	Remove RV17 Move GPU_GPIO1 to RP19.7	11/07	SIV
17	HW design	25	Add PCH_GPIO87 to JEDP1.7	11/07	SIV
18	HW design	27	Change R156 to short pad	11/07	SIV
19	EMI recommend	27	Add RA13 for EMI@ Add CA12 for @EMI@	11/07	SIV
20	HW design	29	Change R217,R218,R257,R222,R199,R226 to short pad	11/07	SIV
21	HW design	30	Change R273,R274,R268 to short pad Remove R266,R276,R214,R272 Move USB_CHG_EN#, USB_EN#, FAN_SPEED2, FAN_SPEED1 to RP33	11/07	SIV
22	HW design	31	Change R243 to short pad	11/07	SIV
23	HW design	33	Change R253 to short pad	11/07	SIV
24	HW design	35	Change R630 to short pad	11/07	SIV
25	EMI recommend	28	Add C323,C326,C327,C328,C329,C330,C331,C332 for @EMI@	11/07	SIV
26	HW design	32	Add R249,R250	11/10	SIV

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Item	Reason for change	PG#	Modify List	Date	Phase
27	HW design	09	Change PCH_GPIO85 to PCH_USB_EN#	11/10	SIV
28	HW design	18	Add RV13 for THM_ALERT#	11/10	SIV
29	ME recommend	28	Change JHDMI1 footprint to SINGA_2HE1638-012212F_19P-T	11/10	SIV
30	HW design	12	Change C59,C62,C66,C70,C75 from SE000000O000 to SE00000PL00 Add C37,C138,C333@,C334,C335 SE00000PL00	11/10	SIV
31	HW design	07	RP31.1 & RP31.3 swap RP31.2 & RP31.4 swap => modify RP31 symbol RP32.1 & RP32.2 swap RP32.3 & RP32.4 swap	11/10	SIV
32	EMI recommend	27	Add CA13 close to UA1	11/11	SIV
33	HW design	30 32	Change USB_CHG_EN# to USB_CHG_EN	11/11	SIV
34	HW design	09	Remove DGPU_PWR_EN, DGPU_HOLD_RST# Change PCH_GPIO18 from RP10.5 to RP5.8 Change PCH_GPIO23 from RP10.6 to RP28.5 Remove RP10	11/12	SIV
35	HW design	25	Remove JP5	11/15	SIV
36	Busyer suggestion	19	Change QV5 from SB000007H10 to SB00000QP00	11/15	SIV
37	Busyer suggestion	21	Change LV6, LV7 from SM01000BZ00 to SM01000FF00	11/15	SIV
38	Busyer suggestion	30	Change L13,L14 from SM010016810 to SM01000LP00	11/15	SIV
39	HW design	32	swap D21 (Pin1=>Pin9, Pin3=>Pin1, Pin7=>Pin3, Pin9=>Pin7)	11/18	SIV
40	EMI recommend	26	Change TS1 from SP050006F00 to SP050006800	11/20	SIV
41	EMI recommend	25	Change CA12 from 2.2u to 220P	12/02	SIV
42	EMI recommend	27	Change RA3 from 45.1 to 10.6 Change CA13 from 2.2u to 220P	12/02	SIV
43	EMI recommend	28	Change C323,C326,C327,C328,C329,C330,C331,C332 from 0.1u to 2.2P	12/02	SIV
44	EMI recommend	32	Change D16, D17 from ESD@ to @ESD@	12/02	SIV
45	EMI recommend	33	Change D19 from ESD@ to @ESD@ Change D20 from @ESD@ to ESD@	12/02	SIV

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW design	33	Add R266(@) 100K pull-high to +3VLP for NOVO#	12/05	SIT
2	HW design	29	Add NET: DEW1_TI / DEW2_TI	12/09	SIT
3	HW design	09	Add R276 10K pull-high to +3VS for DGPU_PWR_EN	12/19	SIT
4	Vendor recommend	29	Change R186, R193 from @ to TI@	12/20	SIT
5	HW design	25	Change +12VS_Panel to B+ Add JP5 Delete R215, R504, R148 for RP10 Add RP10 Change R213 to short pad	12/20	SIT
6	HW design	30	Change R267 to @ Change net name from USB_EN# to USB1_EN# Add USB2_EN# to U26.89 Add R277 (10K) pull-high +5VALW Change R270 to short pad	12/20	SIT
7	HW design	32	Change net name from USB_EN# to USB1_EN# by U29.4 Change net name from USB_EN# to USB2_EN# by U30.4 Delete R249, R250	12/20	SIT
8	HW design	09	Change PCH_USB_EN# to PCH_GPIO85 Delete R252,R262	12/20	SIT
9	HW design	08	Delete R206 for RP10 Change R46,R51,R53 to short pad	12/20	SIT
10	HW design	07	Change R34, R35, R39, R40 to short pad	12/20	SIT
37	HW design	11	Change R79 to short pad	12/20	SIT
38	HW design	15	Change R88, R98 to short pad	12/20	SIT
39	HW design	16	Change R104 to short pad	12/20	SIT
40	HW design	18	Change RV44,RV32 to short pad	12/20	SIT
41	HW design	19	Change RV45 to short pad	12/20	SIT
42	HW design	20	Change RV46, RV50, RV52, RV55, RV57, RV51 to short pad	12/20	SIT
43	HW design	28	Delete Q5, Q7 Add Q5A, Q5B	12/20	SIT
44	EMI recommend	32	Change C306, C307 from 0.1u to100P	12/20	SIT
45	HW design	33	Change R230 from 300 ohm to 649 ohm	12/23	SIT
46	Busyer suggestion	21	(X1 code) Change LV10, LV13 from SM01000BL00 to SM01000GG00	12/23	SIT
47	Busyer suggestion	08	(X1 code) Change U11 from SA00006QR00 to SA741080400	12/23	SIT
48	Busyer suggestion	25	(X1 code) Change U33 from SA00006QR00 to SA741080400	12/23	SIT
49	Busyer suggestion	30	(X1 code) Change U27 from SA00006QR00 to SA741080400	12/24	SIT
50	EMI recommend	27	Change RA12 from 120 ohm(SM01000DF00) to 300 ohm (SM01000I000)	12/24	SIT
51	HW design	27	Change RA2, RA10 to short pad	12/24	SIT
52	EMI recommend	30	Change C286, C287, C289, C291 from @ to EMI@	12/24	SIT
53	HW design	30	Change R260, R223 to short pad	12/24	SIT
54	HW design	31	Change R228, R229 to short pad	12/24	SIT
55	HW design	19	Change R260, R223 to short pad	12/25	SIT
56	HW design	25	Change L24 from EMI@ to @EMI@	12/25	SIT

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
57	HW design	29	Change R275 to @	12/27	SIT
58	HW design	28	Change C323, C326, C327, C328, C329, C330, C331, C332 from @EMI@ to EMI@	12/27	SIT
59	HW design	31	Change R230 from 649 ohm 5% to 649 ohm 1%.	12/31	SIT
60	Vendor recommend	21	Change LV10, LV13 from SM01000GG00 to SM01000I300.	01/03	SIT
61	HW design	12	Change C59, C138, C66, C334, C75 from 47uF to 22uF	01/07	SIT
62	HW design	15	Change C89, R90, C107, R100 to @	01/07	SIT
63	HW design	16	Change C120, R106 to @	01/07	SIT
64 65 66	HW design	25	Change R1456 to short pad Change C225, C226 to @ Change L6 from SM010014520 to SD002000080 (0 ohm) and change location to R2	01/07	SIT
67	HW design	31	Change C300, C303 to @	01/07	SIT
68	HW design	33	Change R256 to short pad	01/07	SIT
69	HW design	12	Change C37, C62, C70, C335 to @	01/03	SIT
1	HW design	25	Change location L6 to R2	01/12	SVT
2	HW design	19	Change location C989 to R830	01/12	SVT
3	EMI recommend	28	Change C327, C328, C329, C330, C331, C332, C323, C326 from EMI@ to @EMI@	01/14	SVT
4	HW design	27	Add U1(LDO), C344, C343	01/20	SVT
5	DFx recommend	32	Add C345, C346	01/22	SVT
6	Busyer suggestion	21	Change LV10, LV13 from SM01000I300 to SM01000F100	01/22	SVT
7	HW design	27	Add R249, R250 Change C253 from 1uF_0402 tp 1uF_0603	01/22	SVT
8	HW design	06	Change RG3 to short pad	01/22	SVT
9	HW design	07	Change RG9, R38 to short pad	01/22	SVT
10	HW design	25	Change R2 to short pad	01/22	SVT
11	HW design	18	Change RV187 to short pad	01/22	SVT
12	HW design	29	Change R185 to short pad	01/22	SVT
13	HW design	27	Change R155, R157, R158 to short pad	01/22	SVT
14	HW design	26	Change RG6 to short pad	01/22	SVT
15	HW design	30	Change R225 to short pad	01/22	SVT
16	HW design	18	Change RV25 from 100K to 1K	02/10	SVT
17	HW design	28	Change RP21, PR22 from 680 ohm to 470 ohm	02/12	SVT
18	HW design	25	Add R148	02/19	SVT
19	HW design	30	Delete net: BATT_LEN#	02/20	SVT
20	HW design	19	Change R829 from 470 ohm to 10 ohm	02/21	SVT
21	HW design	18	Change RV187 from short pad to 0 ohm	02/21	SVT
22	EMI recommend	27	Change R164, R165, R166, R167 from 0 ohm to short pad Change R196, R197, R198, R173 from 0 ohm to short pad	02/21	SVT
23	Busyer suggestion	19	Change Q139 from SB000003W00 to SB00000ZN00	02/21	SVT
24	Vendor recommend	34	Add RG2 Change RG5 from 10 ohm to 0 ohm	02/24	SVT
25	DFx recommend	32	Change C346@ to C346	02/26	SVT

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