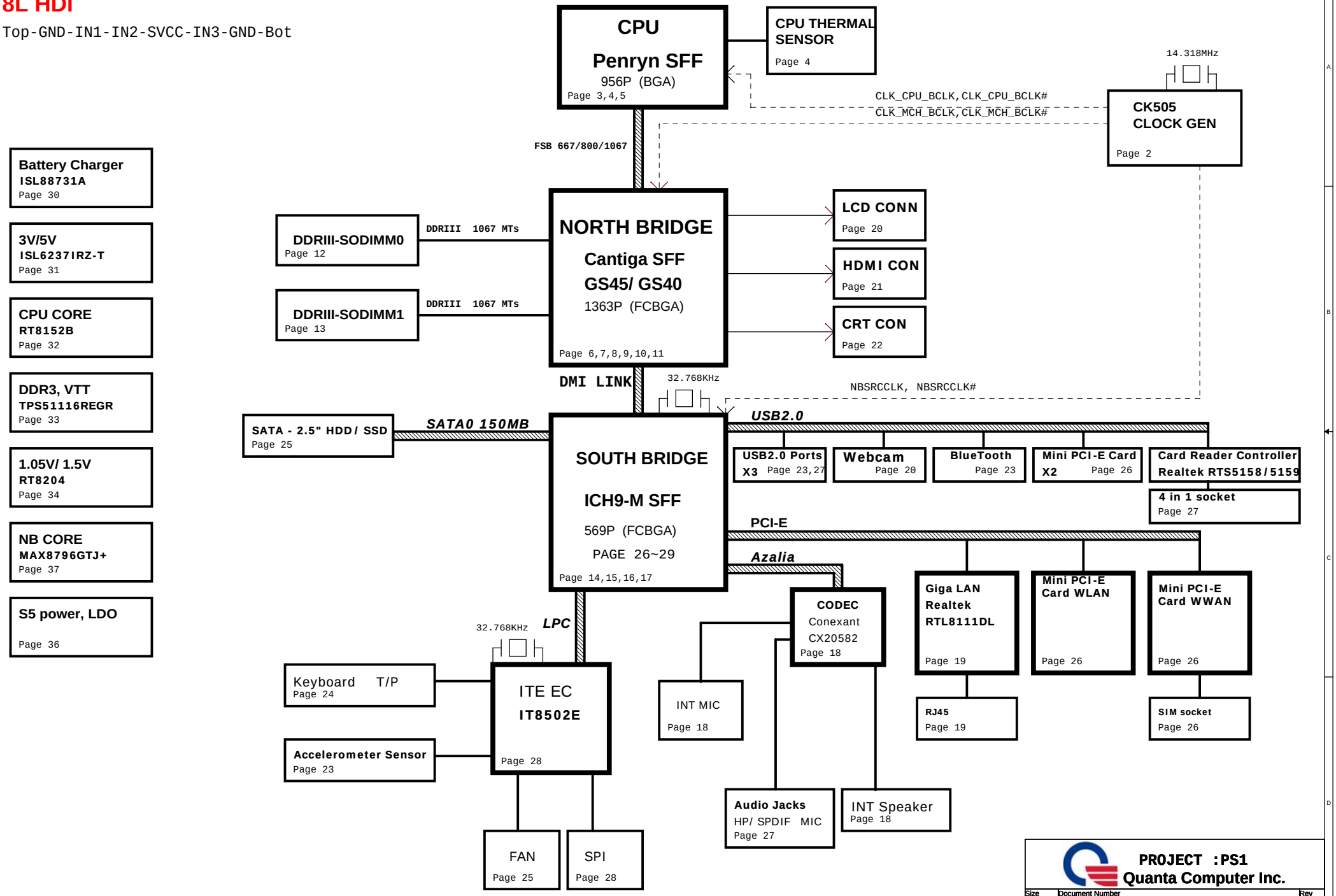
PCB STACK UP

8L HDI

Top-GND-IN1-IN2-SVCC-IN3-GND-Bot

PS-Note, CULV BLOCK DIAGRAM

01

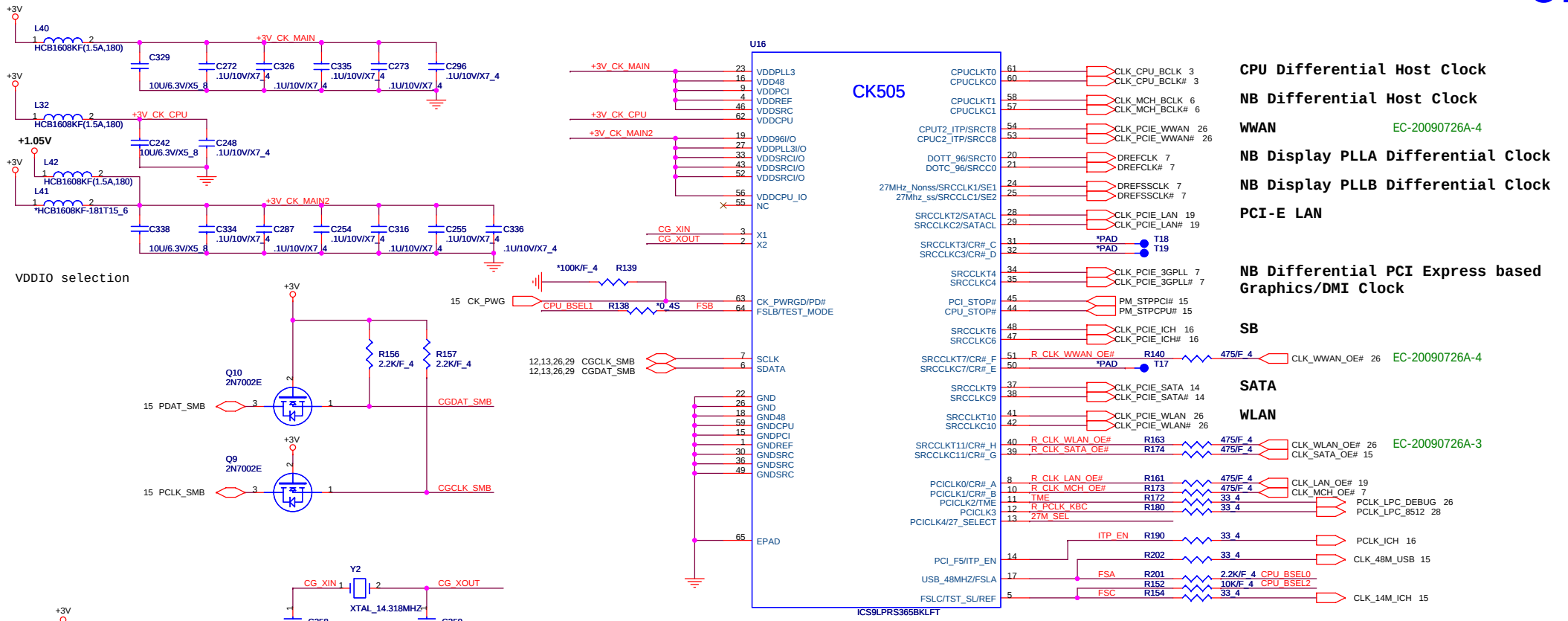


PROJECT : PS1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Block Diagram	1A
Date: Saturday, October 31, 2009	Sheet 1 of 41	

4,7,10,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,31,32,34,35,37 +3V
3,4,5,6,7,9,10,14,17,34,35,37 +1.05V



CPU Differential Host Clock

NB Differential Host Clock

WWAN EC-20090726A-4

NB Display PLLA Differential Clock

NB Display PLLB Differential Clock

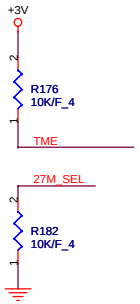
PCI-E LAN

NB Differential PCI Express based Graphics/DMI Clock

SB

SATA

WLAN EC-20090726A-3

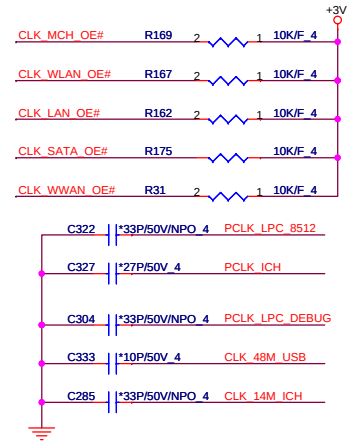


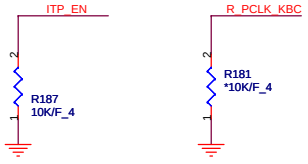
TME=High
OC of CPU and SRC are not allowed.

27M_SEL= LOW UMA

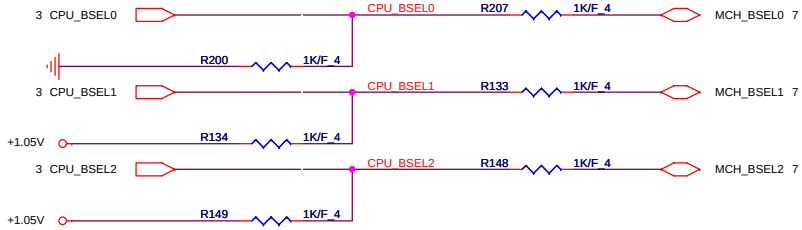
CLKREQ	SRC Port		
CR#_B	SRC 1,4	CLK_MCH_OE#	SRC4
CR#_A	SRC 0,2	CLK_LAN_OE#	SRC2
CR#_G	SRC 9	CLK_SATA_OE#	SRC9
CR#_H	SRC 10	CLK_MINI_OE#	SRC10
CR#_F	SRC 8	CLK_WWAN_OE#	SRC 8

EC-20090726A-3





Disable ITP.

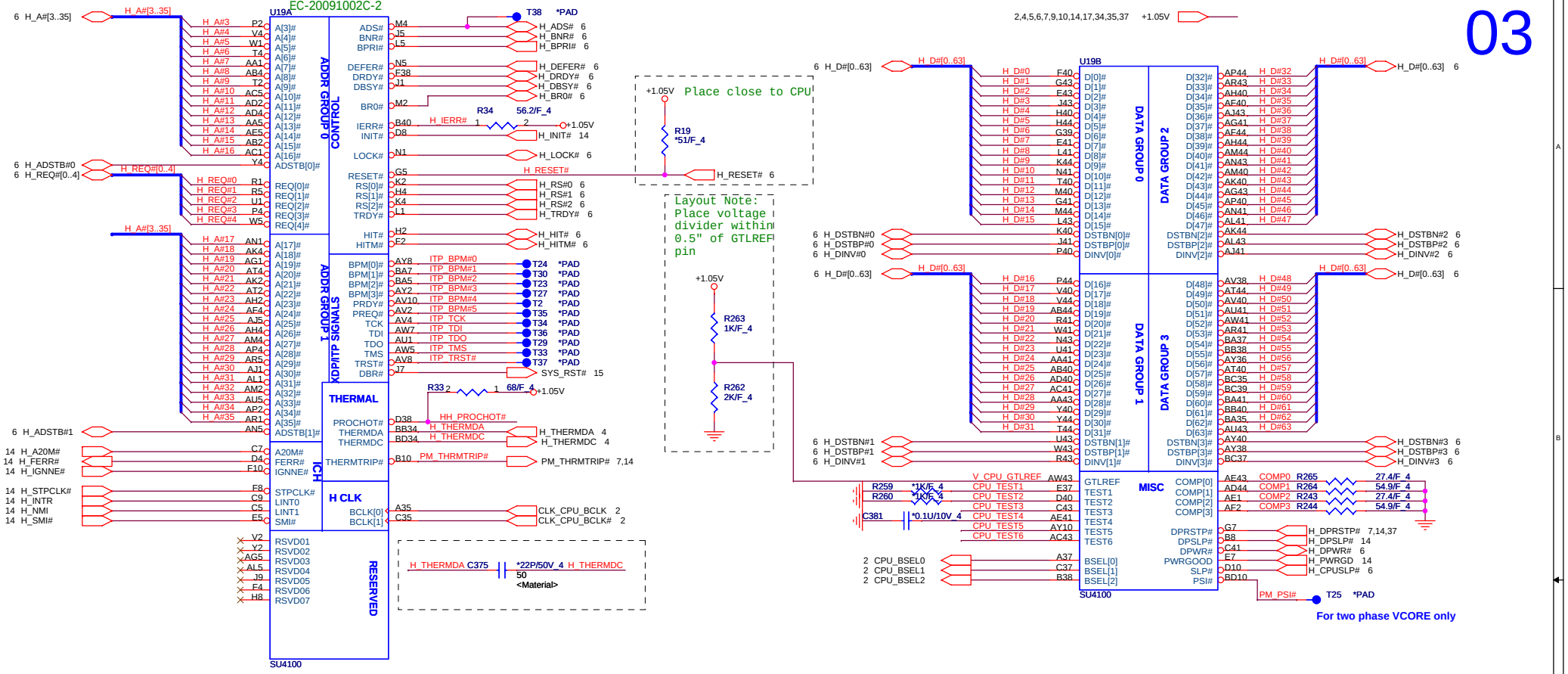


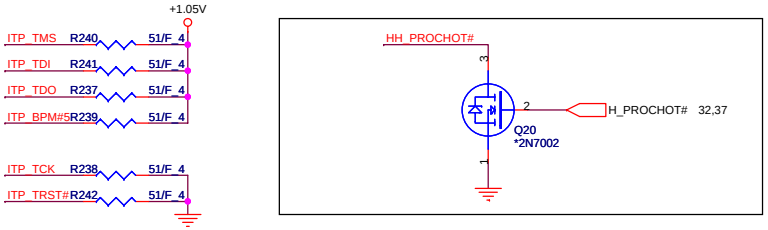
PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Clock Generator	1A
Date: Saturday, October 31, 2009	Sheet 2 of 41	

EC-20091002C-2

03





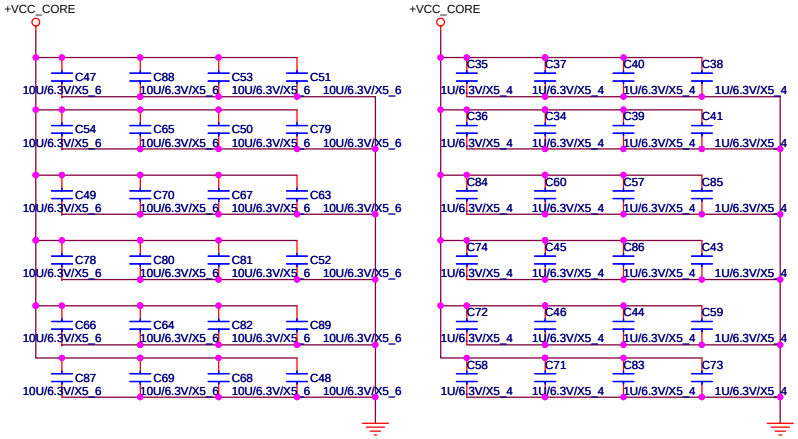
*PAD T40 — CPU_TEST3
*PAD T31 — CPU_TEST5
*PAD T41 — CPU_TEST6

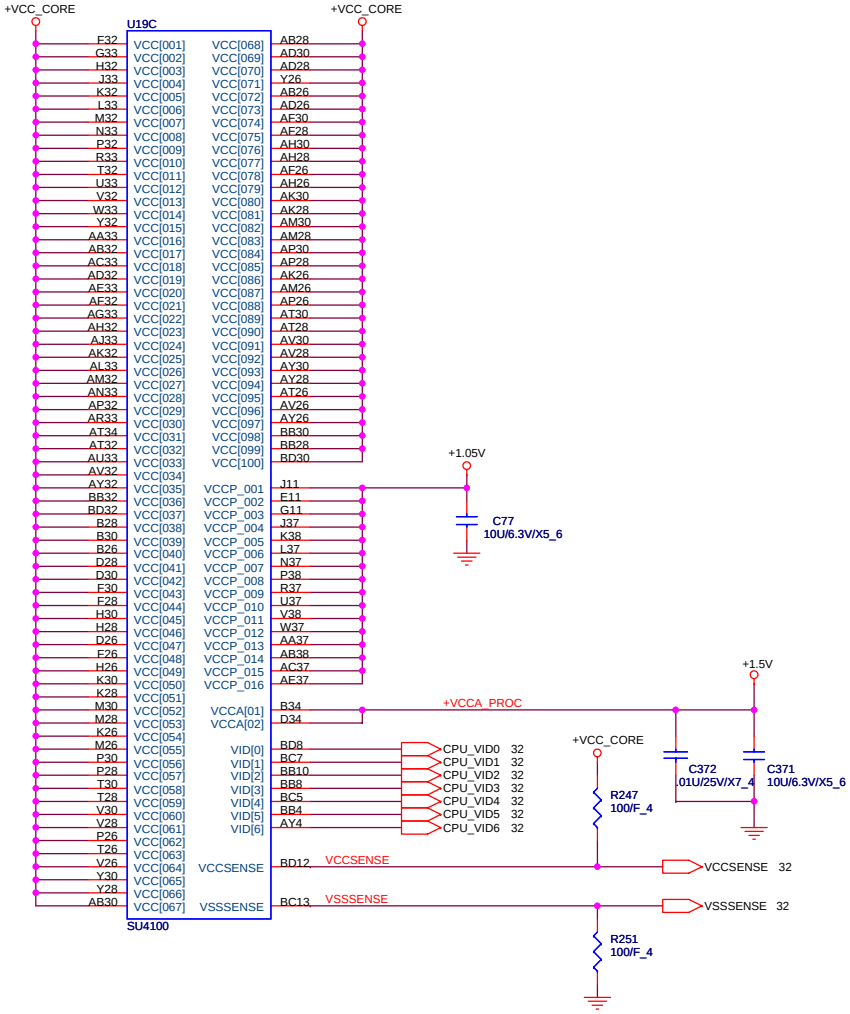
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

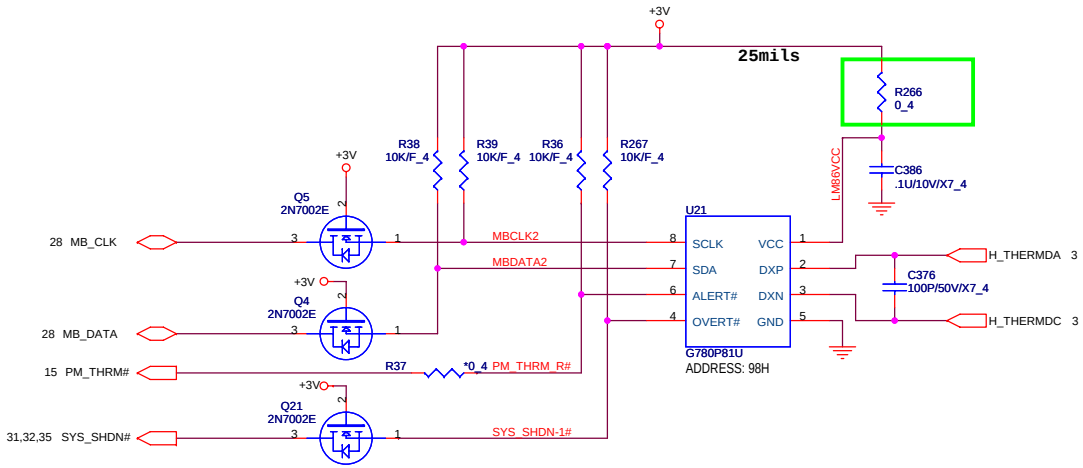
Signal	ITP disable guidelines		
TDI	Resistor Value		
TMS	150 ohm +/- 5%	Connect To	Resistor Placement
TRST#	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	680 ohm +/- 5%	VTT	Within 2.0" of the ITP
TDO	27 ohm +/- 5%	Open GND	Within 2.0" of the ITP
ITP_EN		GND	Within 2.0" of the ITP
	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Penryn (HOST BUS) 1/3	1A
Date: Saturday, October 31, 2009	Sheet 3 of 41	

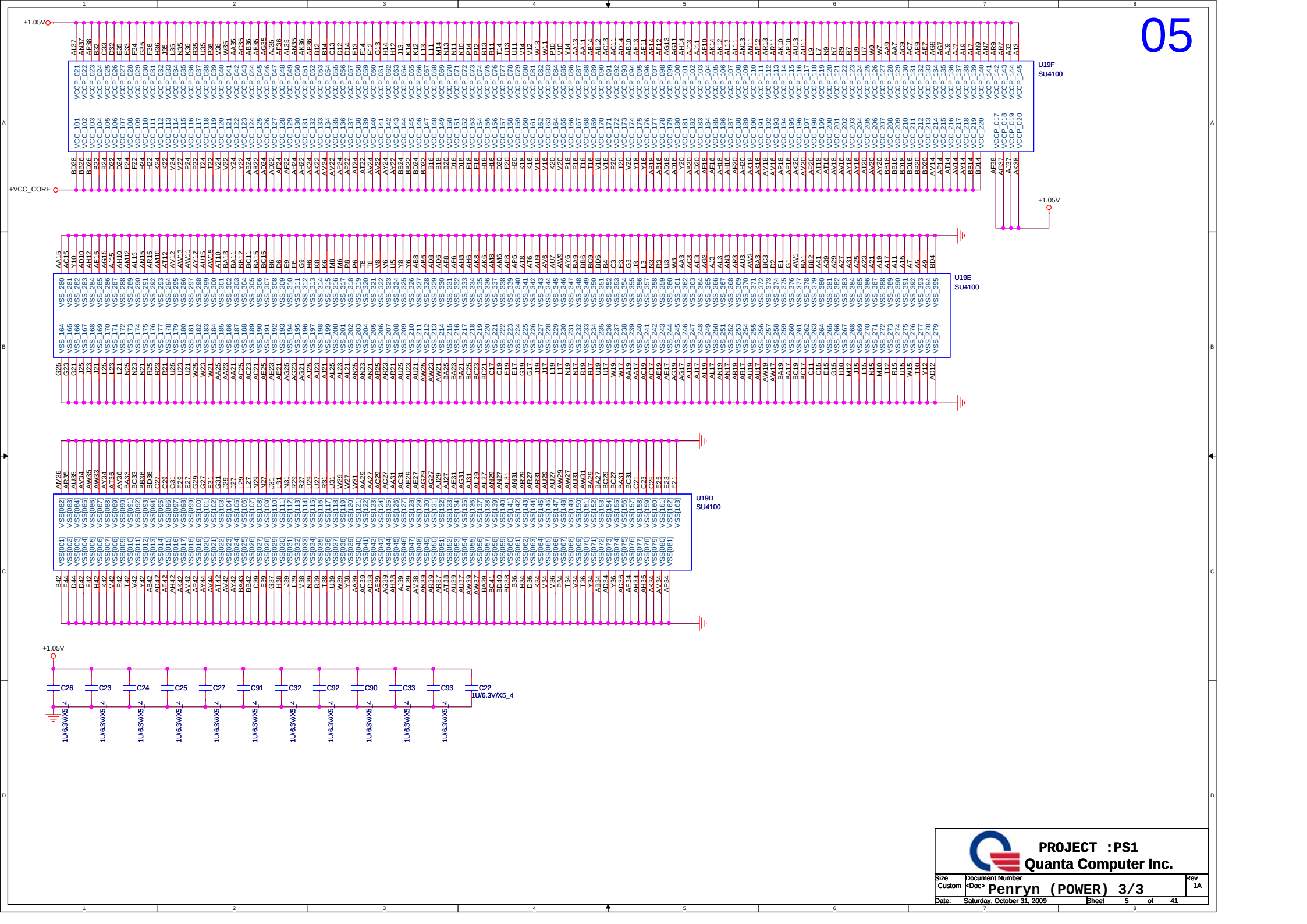






PROJECT :PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Penryn (TH Monitor) 2/3	1A
Date: Saturday, October 31, 2009	Sheet 4 of 41	


05
+1.05V
+VCC_CORE
U19F
SU4100
U19E
SU4100
U19D
SU4100
C26
C23
C24
C25
C27
C91
C32
C92
C90
C33
C93
C22
1U/6.3V/X5_4
PROJECT : PS1
Quanta Computer Inc.
Size
Custom
Document Number
<Doc>
Penryn (POWER) 3/3
Rev
1A
Date:
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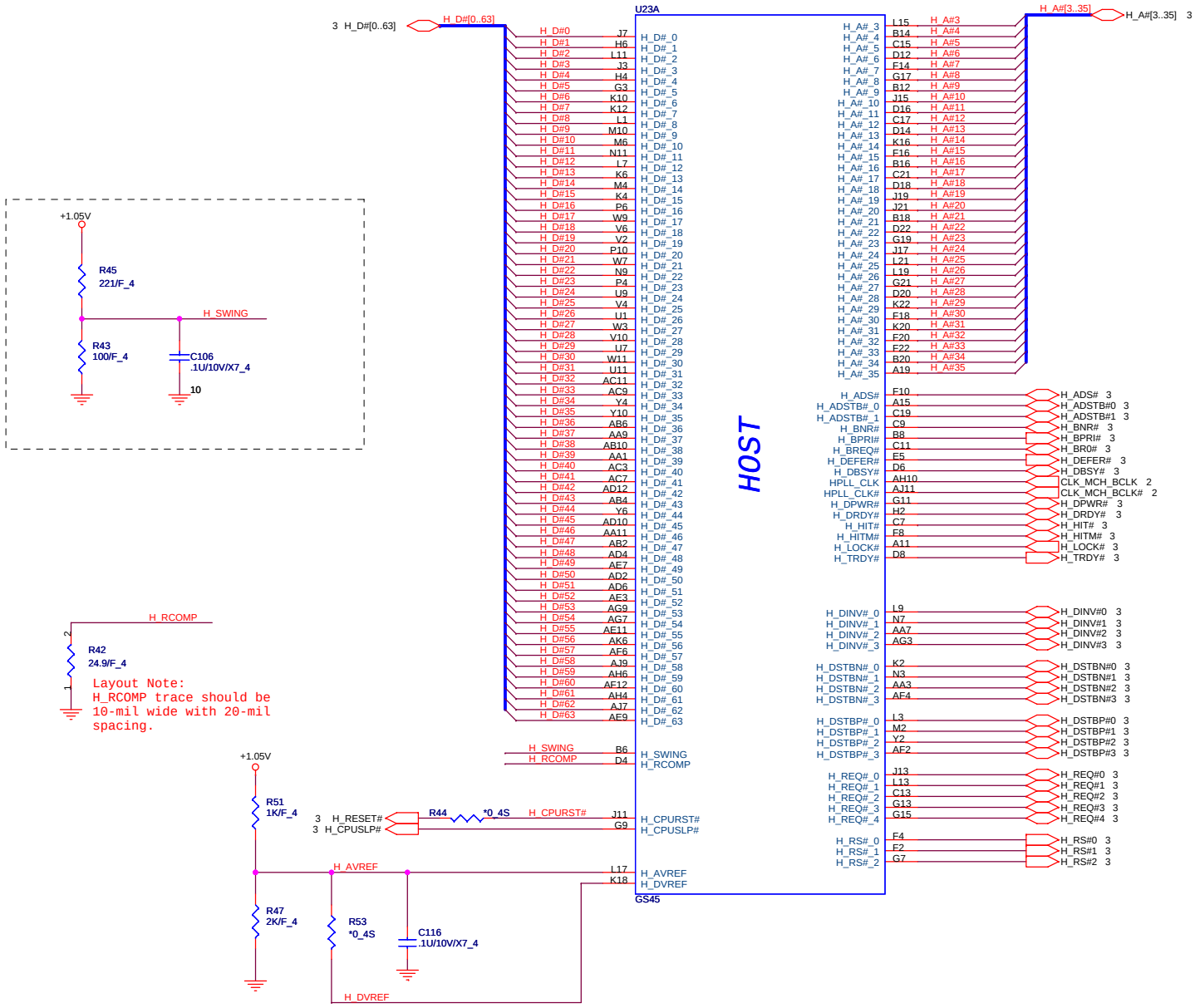
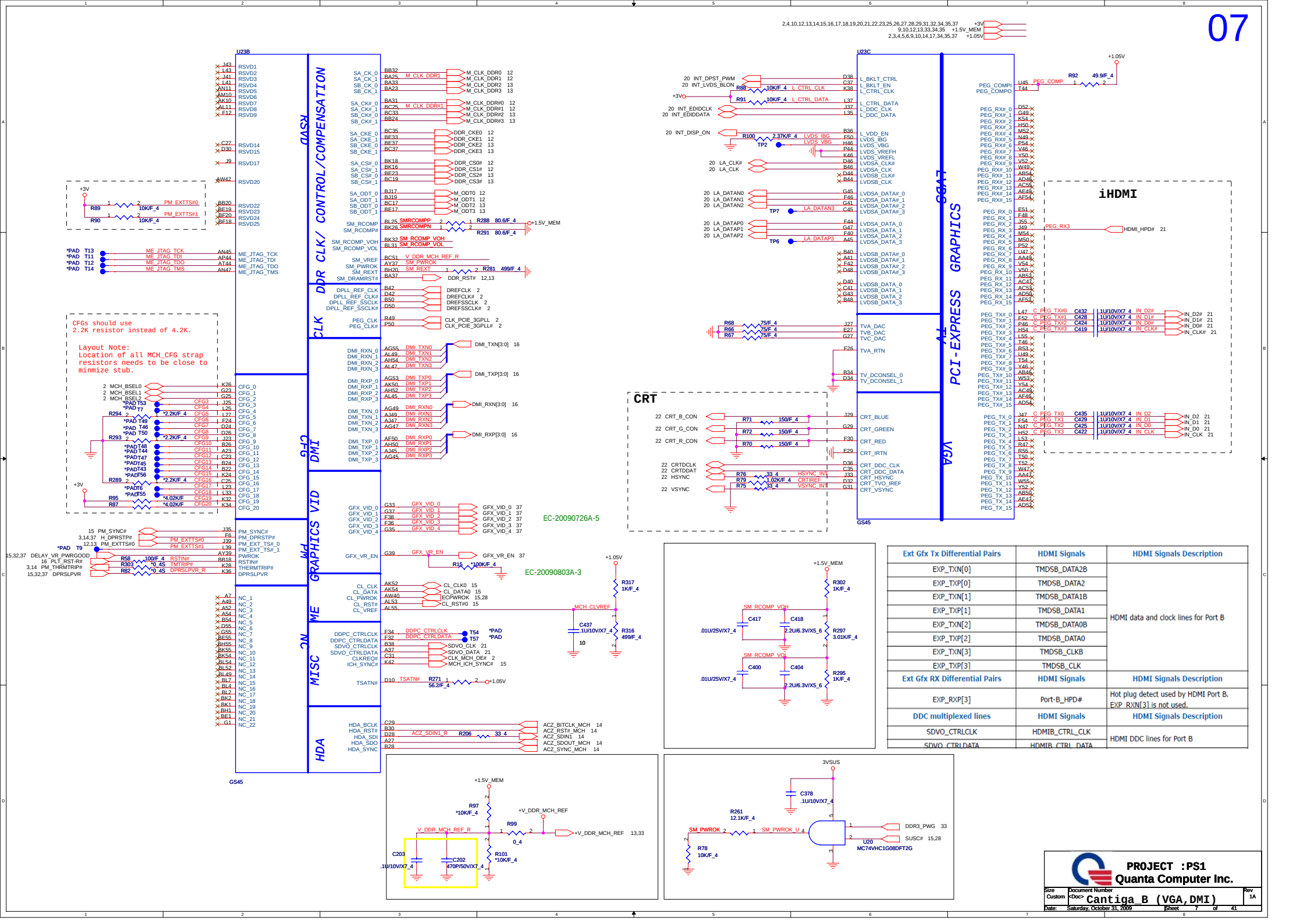
41

EC-20091002C-2



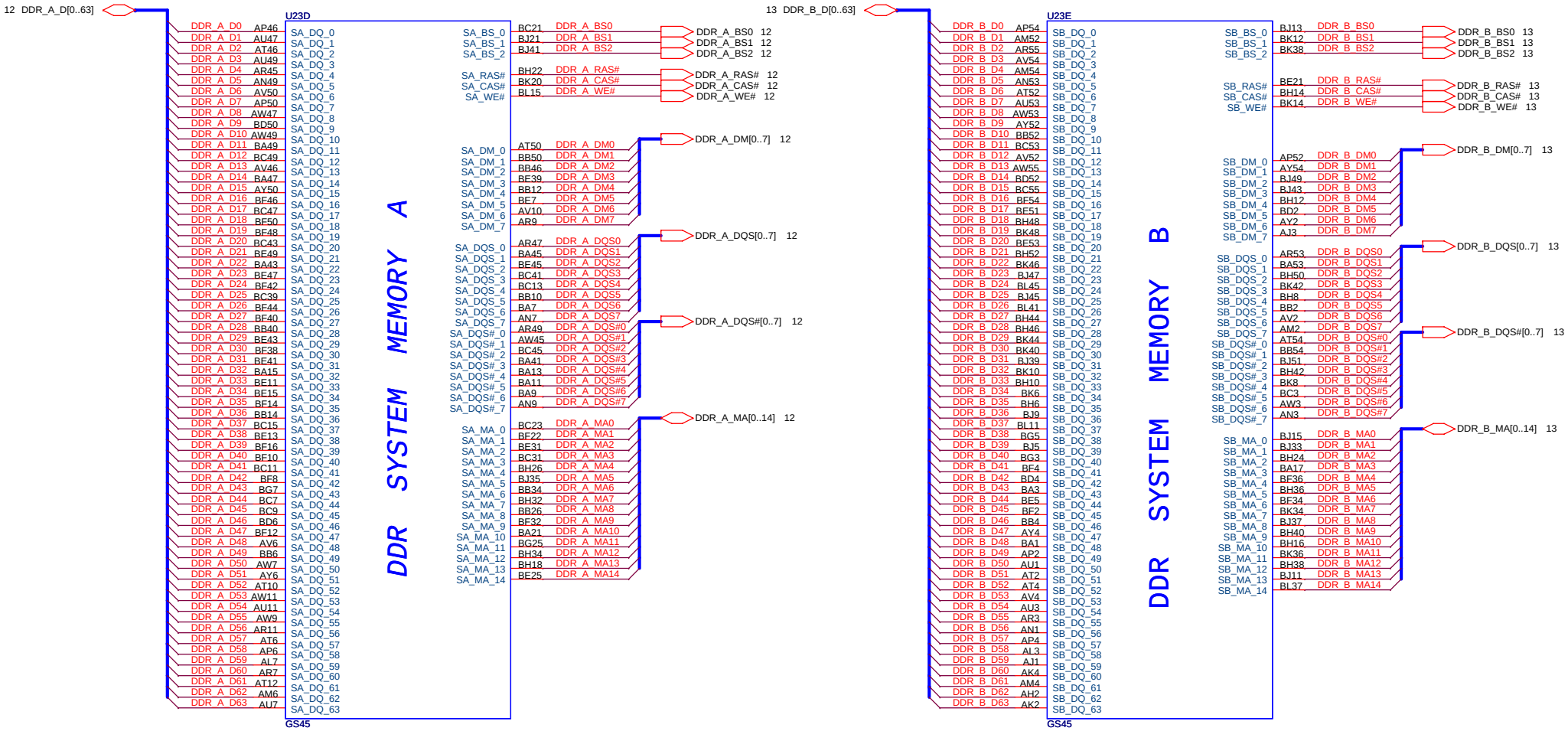
PROJECT : PS1			
Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> Cantiga_A (HOST)		Rev: 1A
Date: Saturday, October 31, 2009	Sheet 6 of 41		



Ext Gfx Tx Differential Pairs	HDMI Signals	HDMI Signals Description
EXP_TXN[0]	TMDSB_DATA2B	HDMI data and clock lines for Port B
EXP_TXP[0]	TMDSB_DATA2	
EXP_TXN[1]	TMDSB_DATA1B	
EXP_TXP[1]	TMDSB_DATA1	
EXP_TXN[2]	TMDSB_DATA0B	
EXP_TXP[2]	TMDSB_DATA0	
EXP_TXN[3]	TMDSB_CLKB	
EXP_TXP[3]	TMDSB_CLK	
Ext Gfx RX Differential Pairs	**HDMI Signals**	**HDMI Signals Description**
EXP_RXP[3]	Port-B_HPD#	Hot plug detect used by HDMI Port B. EXP_RXN[3] is not used.
DDC multiplexed lines	**HDMI Signals**	**HDMI Signals Description**
SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIB_CTRL_DATA	

PROJECT :PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Cantiga_B (VGA,DMI)	1A
Date: Saturday, October 31, 2009	Sheet 7 of 41	



PROJECT :PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Cantiga_C (DDR interface)	1A
Date: Saturday, October 31, 2009	Sheet 8 of 41	

Ivcc_sm (DDR3,1.5V,1066MTs) -->4140mA

IVCC_AXG-->7700mA(GS45)

Layout Note:
370 mils from edge.

Layout Note:
Inside GMCH cavity.

10A for each Jumper

Layout Note:
370 mils from edge.

EC-20090729A-10
EC-20090726A-5
EC-20090828B-2

EC-20090726A-5

EC-20090726A-5

U23G

U23F

GS45

GS45

VCC SM POWER

VCC GFX NCTF

VCC GFX

VCC GFX

VCC SM LF

VCC CORE POWER

VCC NCTF

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Cantiga_D (VCC,NCTF)	1A

Date: Saturday, October 31, 2009 Sheet 9 of 41

VCCA_DPLLA+VCCA_DPLLB=64.8mA

Correct as Design Guide

EC-20090811A-1

EC-20090729A-9

EC-20090819B-1

EC-20090729A-9

EC-20090729A-9

EC-20090729A-9

Correct as Design Guide

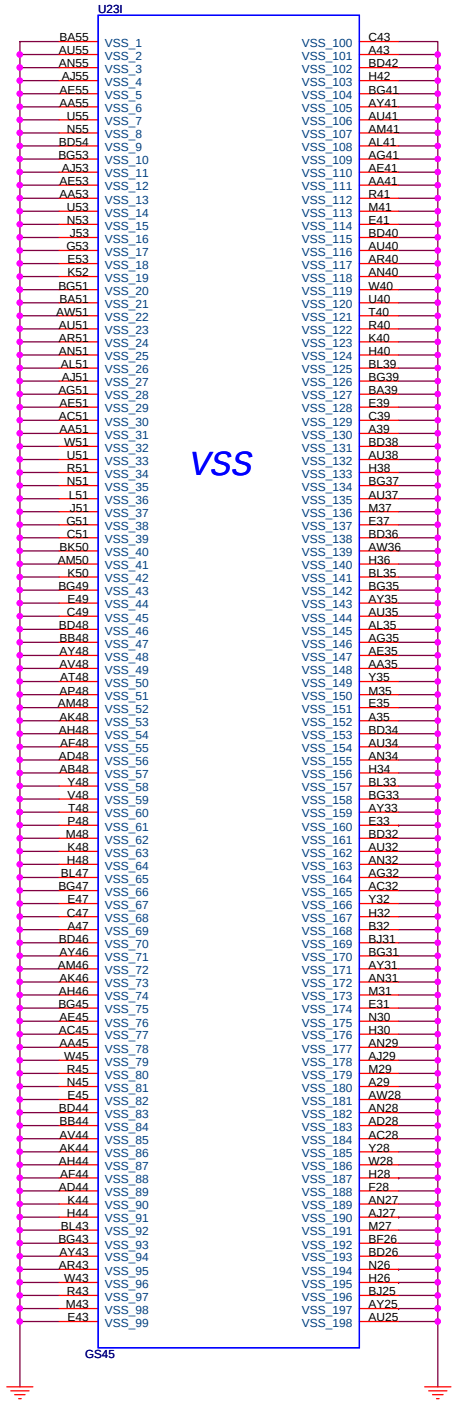
C213 and C581, one is on Top-side and another is on Bot-side

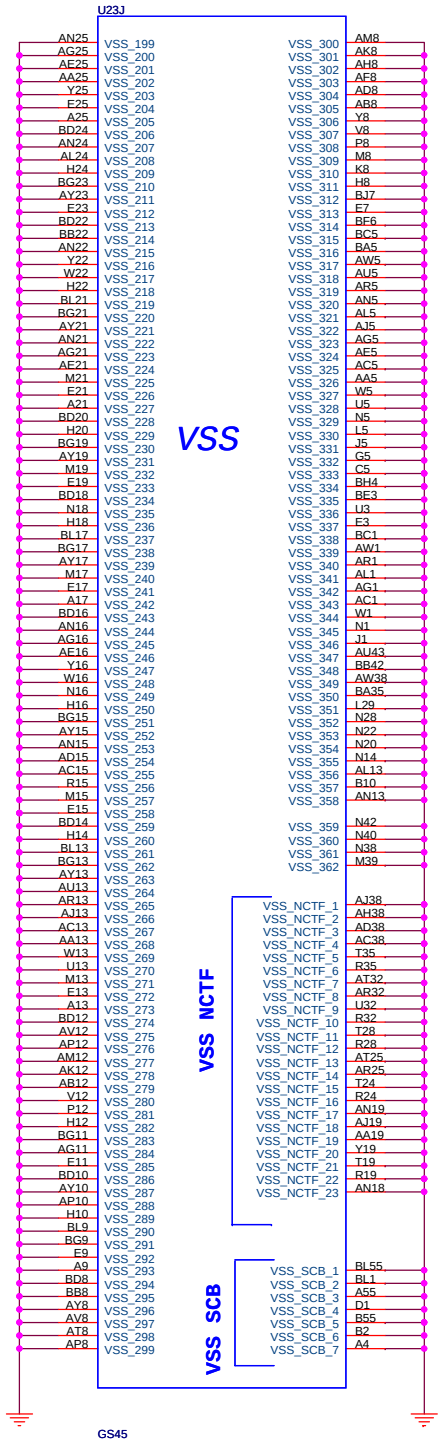
EC-20090729A-9

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Cantiga_E (POWER)	1A

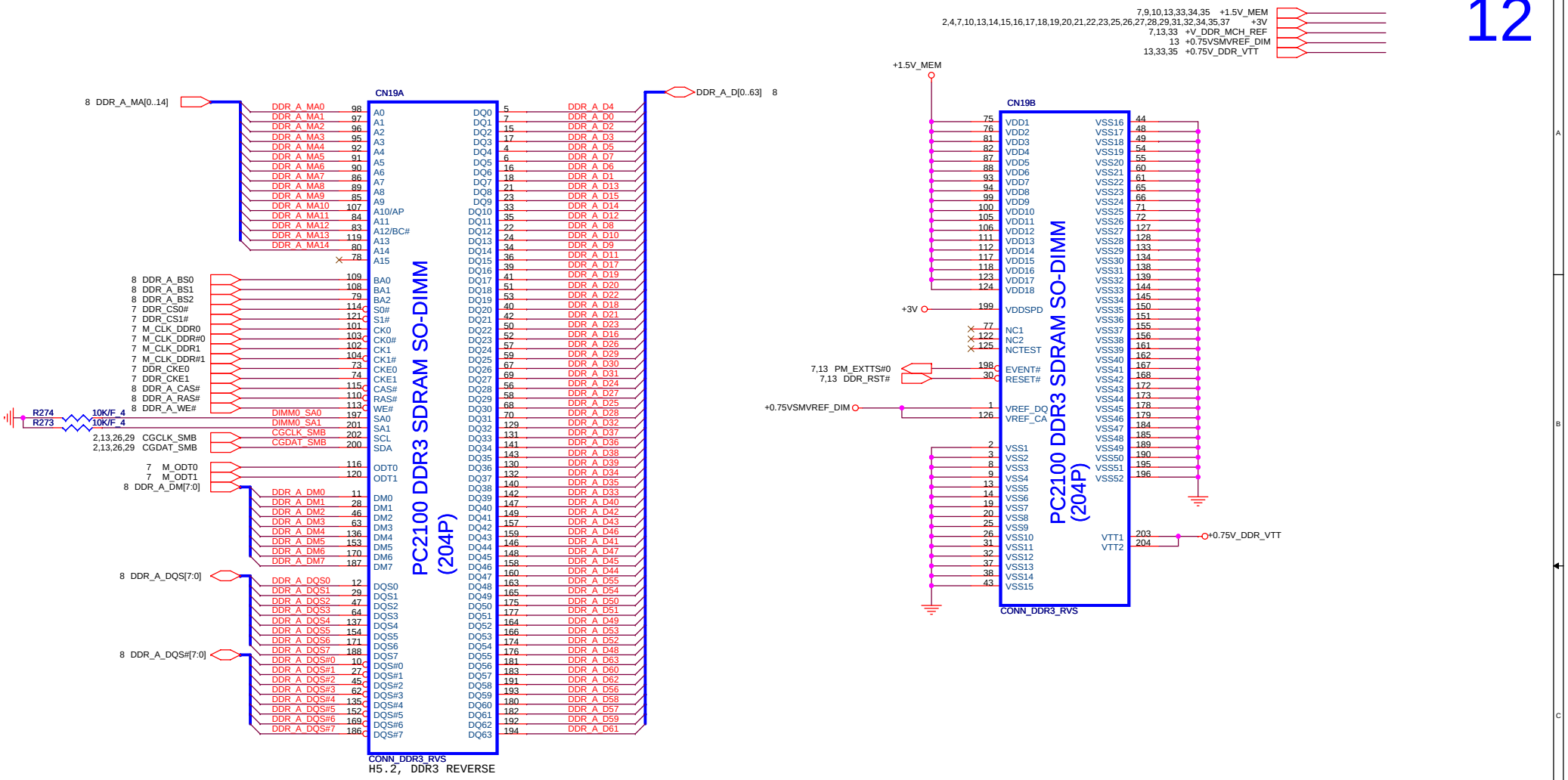
Date: Saturday, October 31, 2009 Sheet 10 of 41

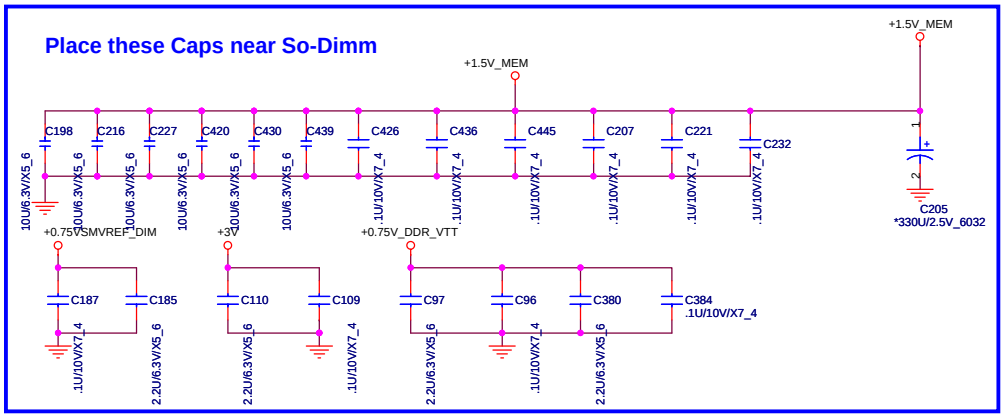




PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Cantiga_F (VSS)	1A
Date: Saturday, October 31, 2009	Sheet 11 of 41	





PROJECT : PS1			
Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> DDR3 (A) SO-DIMM RVS		Rev: 1A
Date: Saturday, October 31, 2009		Sheet 12 of 41	

7,9,10,12,33,34,35 +1.5V_MEM
2,4,7,10,12,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,31,32,34,35,37 +3V
12,33,35 +0.75V_DDR_VTT
7,33 +V_DDR_MCH_REF

CN20A

8 DDR_B_MA[0..14]

DDR_B_MA0 98 DDR_B_MA1 97 DDR_B_MA2 96 DDR_B_MA3 95 DDR_B_MA4 92 DDR_B_MA5 91 DDR_B_MA6 90 DDR_B_MA7 86 DDR_B_MA8 89 DDR_B_MA9 85 DDR_B_MA10 107 DDR_B_MA11 84 DDR_B_MA12 83 DDR_B_MA13 119 DDR_B_MA14 80

8 DDR_B_BS0 109
8 DDR_B_BS1 108
8 DDR_B_BS2 79
7 DDR_CS2# 114
7 DDR_CS3# 121
7 M_CLK_DDR2 101
7 M_CLK_DDR#2 103
7 M_CLK_DDR3 102
7 M_CLK_DDR#3 104
7 DDR_CKE2 73
7 DDR_CKE3 74
8 DDR_B_CAS# 115
8 DDR_B_RAS# 110
8 DDR_B_WE# 113

R48 10K/F_4
R49 10K/F_4
+3V
DIMM1_SA0 197
DIMM1_SA1 201
2,12,26,29 CGCLK_SMB CGCLK_SMB 202
2,12,26,29 CGDAT_SMB CGDAT_SMB 200

7 M_ODT2 116
7 M_ODT3 120
8 DDR_B_DM[7:0]

DDR_B_DM0 11 DDR_B_DM1 28 DDR_B_DM2 46 DDR_B_DM3 63 DDR_B_DM4 136 DDR_B_DM5 153 DDR_B_DM6 170 DDR_B_DM7 187

8 DDR_B_DQS[7:0]

DDR_B_DQS0 12 DDR_B_DQS1 29 DDR_B_DQS2 47 DDR_B_DQS3 64 DDR_B_DQS4 137 DDR_B_DQS5 154 DDR_B_DQS6 171 DDR_B_DQS7 188

8 DDR_B_DQS#[7:0]

DDR_B_DQS#0 10 DDR_B_DQS#1 27 DDR_B_DQS#2 45 DDR_B_DQS#3 62 DDR_B_DQS#4 135 DDR_B_DQS#5 152 DDR_B_DQS#6 169 DDR_B_DQS#7 186

PC2100 DDR3 SDRAM SO-DIMM (204P)

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15 78
BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE# SA0 SA1 SCL SDA
ODT0 ODT1
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

DQ0 5 DQ1 7 DQ2 15 DQ3 17 DQ4 4 DQ5 6 DQ6 16 DQ7 18 DQ8 21 DQ9 23 DQ10 33 DQ11 35 DQ12 22 DQ13 24 DQ14 34 DQ15 36 DQ16 39 DQ17 41 DQ18 51 DQ19 53 DQ20 40 DQ21 42 DQ22 50 DQ23 52 DQ24 57 DQ25 59 DQ26 67 DQ27 69 DQ28 56 DQ29 58 DQ30 68 DQ31 70 DQ32 129 DQ33 131 DQ34 141 DQ35 143 DQ36 130 DQ37 132 DQ38 140 DQ39 142 DQ40 147 DQ41 149 DQ42 157 DQ43 159 DQ44 146 DQ45 148 DQ46 158 DQ47 160 DQ48 163 DQ49 165 DQ50 175 DQ51 177 DQ52 164 DQ53 166 DQ54 174 DQ55 176 DQ56 181 DQ57 183 DQ58 191 DQ59 193 DQ60 180 DQ61 182 DQ62 192 DQ63 194

DDR_B_D[0..63] 8

DDR_B_D1 DDR_B_D5 DDR_B_D3 DDR_B_D7 DDR_B_D4 DDR_B_D0 DDR_B_D6 DDR_B_D2 DDR_B_D8 DDR_B_D13 DDR_B_D11 DDR_B_D15 DDR_B_D9 DDR_B_D12 DDR_B_D14 DDR_B_D10 DDR_B_D16 DDR_B_D17 DDR_B_D19 DDR_B_D23 DDR_B_D20 DDR_B_D21 DDR_B_D18 DDR_B_D22 DDR_B_D24 DDR_B_D29 DDR_B_D27 DDR_B_D26 DDR_B_D28 DDR_B_D25 DDR_B_D31 DDR_B_D30 DDR_B_D33 DDR_B_D37 DDR_B_D35 DDR_B_D34 DDR_B_D32 DDR_B_D36 DDR_B_D38 DDR_B_D39 DDR_B_D40 DDR_B_D41 DDR_B_D46 DDR_B_D43 DDR_B_D44 DDR_B_D45 DDR_B_D47 DDR_B_D42 DDR_B_D52 DDR_B_D53 DDR_B_D54 DDR_B_D49 DDR_B_D48 DDR_B_D50 DDR_B_D55 DDR_B_D51 DDR_B_D57 DDR_B_D56 DDR_B_D58 DDR_B_D61 DDR_B_D59 DDR_B_D62 DDR_B_D60 DDR_B_D63

CONN_DDR3_STD
H5.2, DDR3 STANDARD

+1.5V_MEM

CN20B

VDD1 75 VDD2 76 VDD3 81 VDD4 82 VDD5 87 VDD6 88 VDD7 93 VDD8 94 VDD9 99 VDD10 100 VDD11 105 VDD12 106 VDD13 111 VDD14 112 VDD15 117 VDD16 118 VDD17 123 VDD18 124

+3V
VDDSPD 199

NC1 77 NC2 122 NCTEST 125

7,12 PM_EXTTS#0
7,12 DDR_RST#
EVENT# 198 RESET# 30

+0.75VSMVREF_DIM
VREF_DQ 1 VREF_CA 126

VSS1 2 VSS2 3 VSS3 8 VSS4 9 VSS5 13 VSS6 14 VSS7 19 VSS8 20 VSS9 25 VSS10 26 VSS11 31 VSS12 32 VSS13 37 VSS14 38 VSS15 43

VSS16 44 VSS17 48 VSS18 49 VSS19 54 VSS20 55 VSS21 60 VSS22 61 VSS23 65 VSS24 66 VSS25 71 VSS26 72 VSS27 127 VSS28 128 VSS29 133 VSS30 134 VSS31 138 VSS32 139 VSS33 144 VSS34 145 VSS35 150 VSS36 151 VSS37 155 VSS38 156 VSS39 161 VSS40 162 VSS41 167 VSS42 168 VSS43 172 VSS44 173 VSS45 178 VSS46 179 VSS47 184 VSS48 185 VSS49 189 VSS50 190 VSS51 195 VSS52 196

VTT1 203 VTT2 204
+0.75V_DDR_VTT

PC2100 DDR3 SDRAM SO-DIMM (204P)

CONN_DDR3_STD

Place these Caps near So-Dimm

+1.5V_MEM

C224 10U/6.3V/X5_6
C204 10U/6.3V/X5_6
C234 10U/6.3V/X5_6
C193 10U/6.3V/X5_6
C214 10U/6.3V/X5_6
C229 10U/6.3V/X5_6
C228 .1U/10V/X7_4
C233 .1U/10V/X7_4
C192 .1U/10V/X7_4
C217 .1U/10V/X7_4
C208 .1U/10V/X7_4
C222 .1U/10V/X7_4

+1.5V_MEM
C215 *330U/2.5V_6032

+0.75VSMVREF_DIM
C188 .1U/10V/X7_4
C183 2.2U/6.3V/X5_6

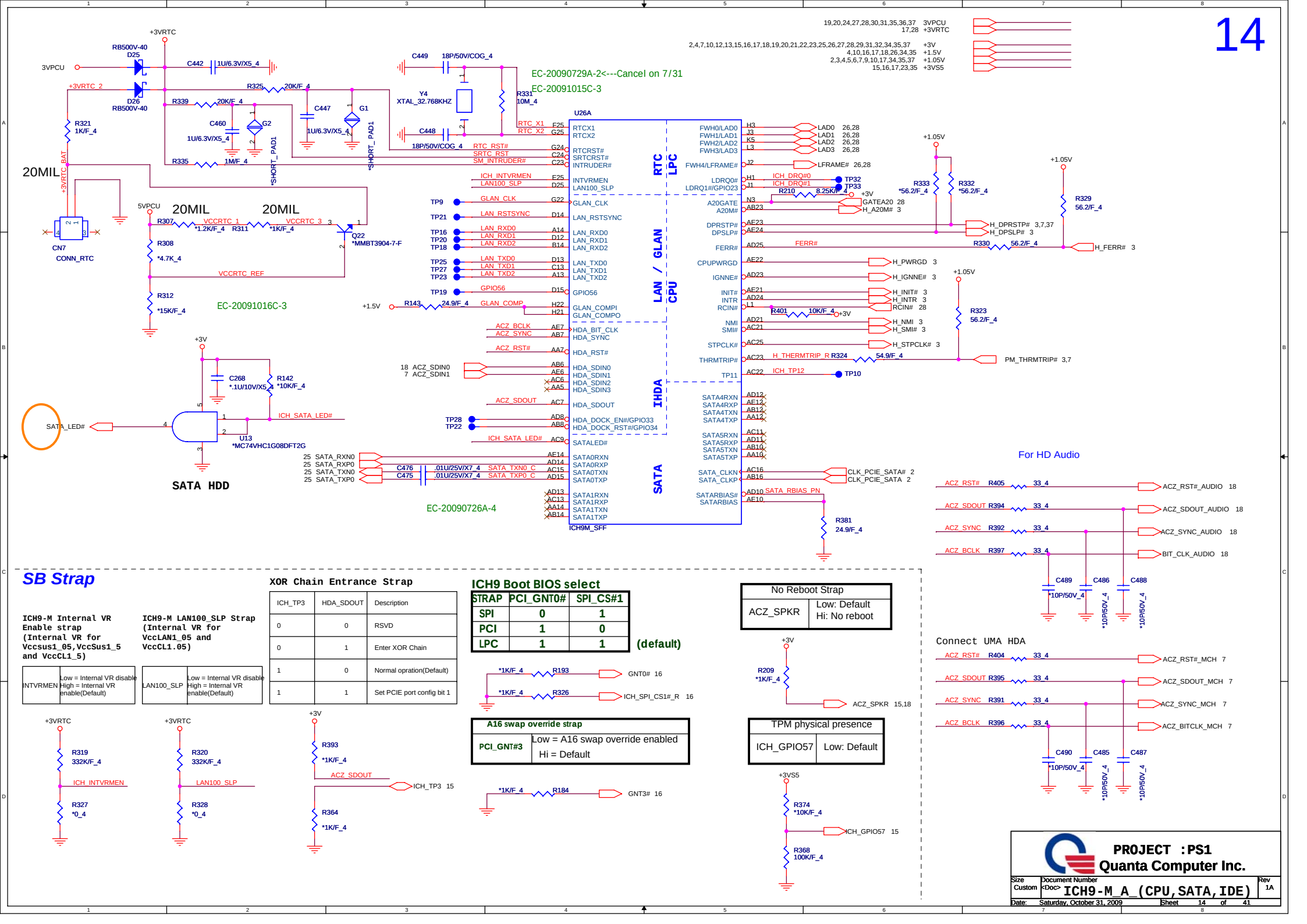
+3V
C120 2.2U/6.3V/X5_6
C118 .1U/10V/X7_4

+0.75V_DDR_VTT
C382 2.2U/6.3V/X5_6
C383 .1U/10V/X7_4
C389 2.2U/6.3V/X5_6
C385 .1U/10V/X7_4

12 +0.75VSMVREF_DIM
C174 470P/50V/X7_4
+0.75VSMVREF_DIM
R86 0_6
+V_DDR_MCH_REF 7,33
R96 *10K/F_4
+1.5V_MEM
R80 *10K/F_4

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> DDR3 (B) SO-DIMM STD	1A
Date: Saturday, October 31, 2009	Sheet 13 of 41	



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1	
SPI	0	1	
PCI	1	0	
LPC	1	1	(default)

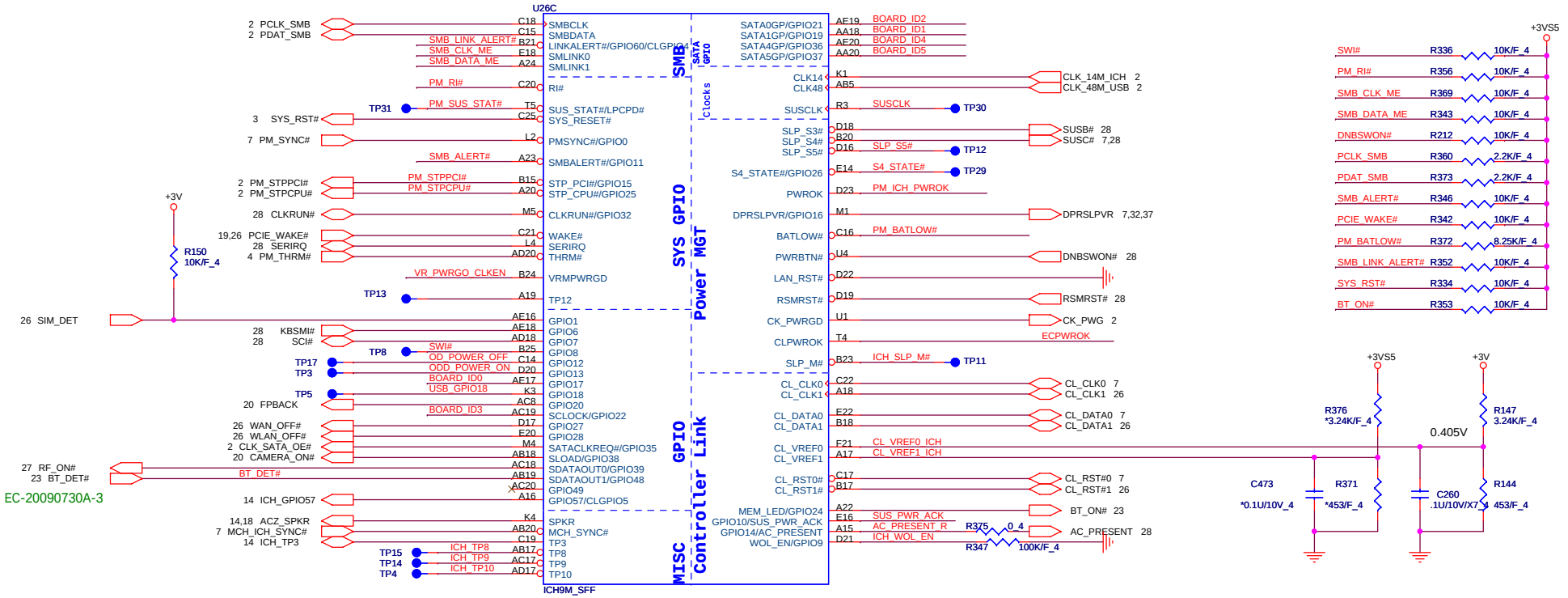
A16 swap override strap

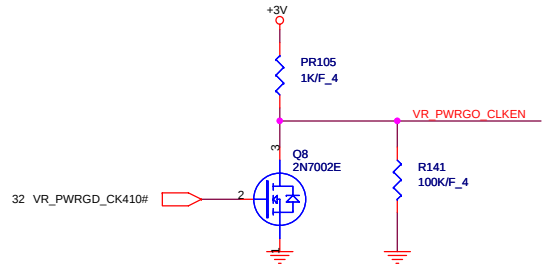
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

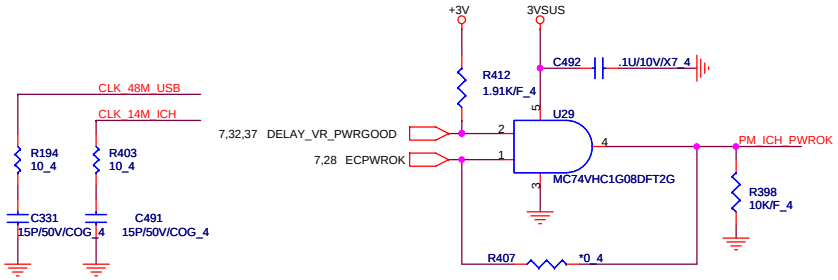
No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

TPM physical presence	
ICH_GPIO57	Low: Default

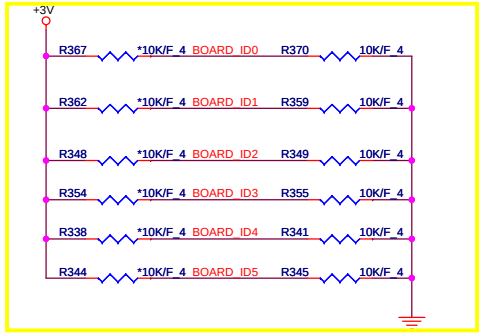
PROJECT : PS1			
Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> ICH9-M_A_(CPU,SATA,IDE)		Rev: 1A
Date: Saturday, October 31, 2009		Sheet 14 of 41	

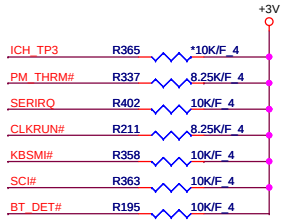


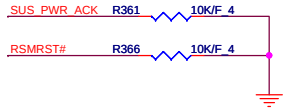




RESERVED BOARD ID







PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> ICH9-M_C_(PM,GPIO,SMB)	1A
Date: Saturday, October 31, 2009	Sheet 15 of 41	

Place TX DC blocking caps close ICH9.

EC-20090726A-4

WLAN

WWAN

LAN

EC-20090729A-3

USB port	Assignment function
USB0	USB Connector onboard
USB1	USB Connector on function board
USB2	X
USB3	X
USB4	BLUETOOTH
USB5	CCD
USB6	USB Connector on function board
USB7	X
USB8	USB Card Reader on function board
USB9	X
USB10	Mini PCI E-WWAN
USB11	Mini PCI E-WLAN

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> ICH9-M_B_(USB,PCIE,DMI)	1A
Date: Saturday, October 31, 2009	Sheet 16 of 41	

U26F

U26E

FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC

10uH+-20%_100mA

Follow LAN DG.

PROJECT	PS1
Quanta Computer Inc.	
Size	Custom
Document Number	<Doc> ICH9-M_D_(POWER,GND)
Rev	1A
Date:	Saturday, October 31, 2009
Sheet	17 of 41

EC-20090724A-1

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

HD Audio Bus

Note:

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

Cnxt review to reserve for Beep Gain.

MIC Decoupling close to Codec

HP/ MIC jack Decoupling close to Connector

EC-20090729A-11

From EC

28 VOLMUTE#

PC BEEP CONTROL

Close to codec

From EC

From SB

PC_BEEP voltage level is 3.3V--(2/3)*5V

Connect to Function Board

EC-20090729A-4

Move Jack related to daughter board

HEADPHONE Normal Open

Move Jack related to daughter board

By vendor suggestion BIAS terminator close to codec

MIC-IN JACK Normal Close

INT MIC

EC-20090729A-13

EC-20091014C-1

EC-20091006C-3

INT Speaker

EC-20090801A-1

EMI Close to Pin out

HP Sense

HP Sense

EC-20090729A-14

EC-20091006C-3

MIC Sense

EXT_MIC_PLUG=H ---- EXTERNAL MIC
EXT_MIC_PLUG=L ---- INTERNAL MIC
MIC JACK DECT PIN IS NORMAL CLOSE TYPE

EC-20091006C-3

EMI Reserve

EC-20090724A-4
EC-20090728A-2
EC-20090804A-1

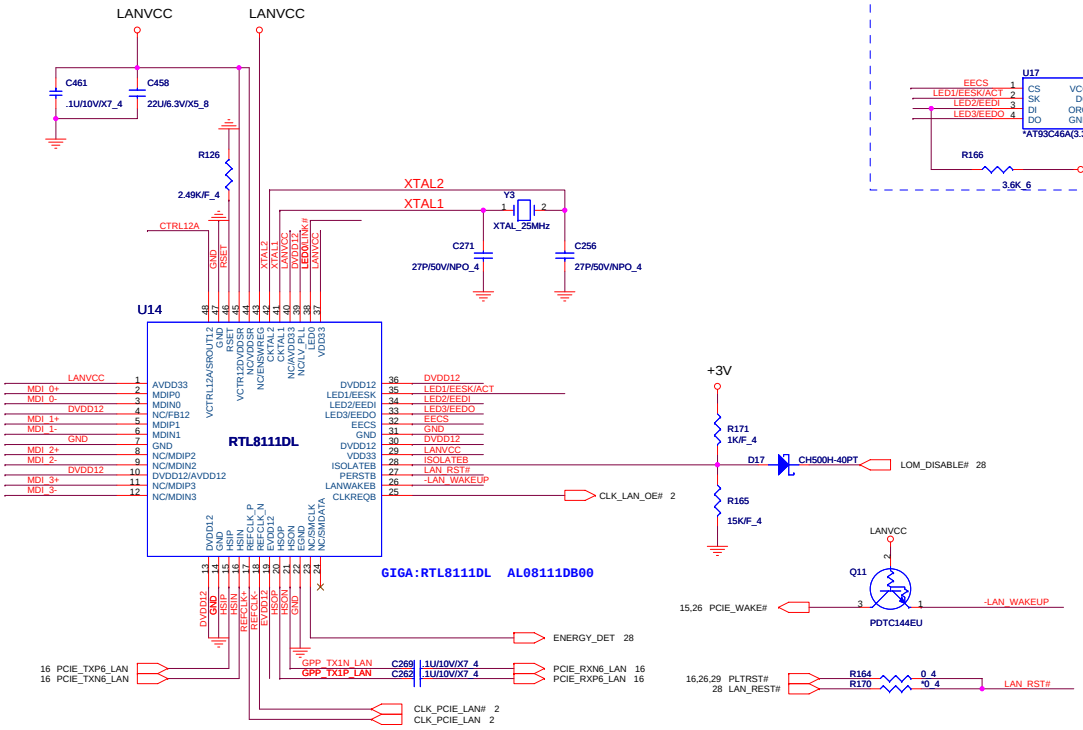
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

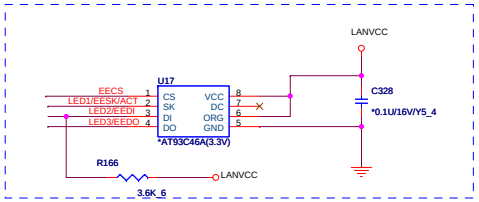
Place bypass caps very close to device.

PROJECT :PS1
Quanta Computer Inc.

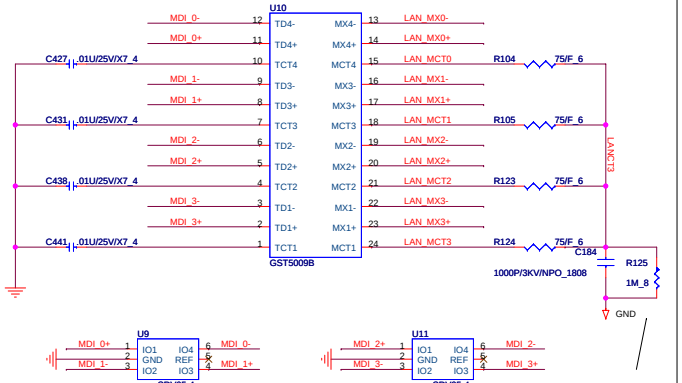
Size	Document Number	Rev
Custom	<Doc> AUDIO (CX20582, SPK)	1A
Date: Saturday, October 31, 2009	Sheet 18 of 41	

EC-20090729A-12

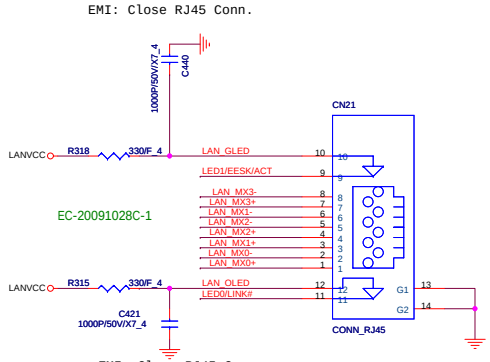


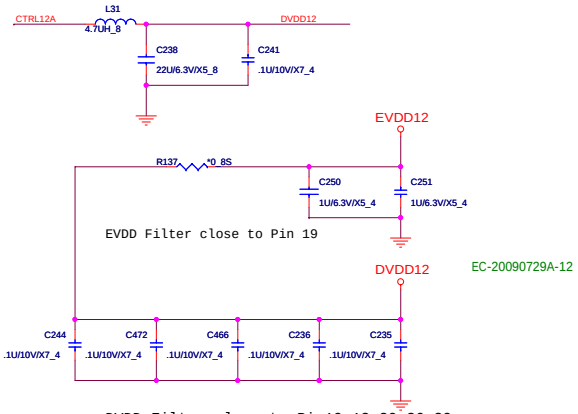


Transformer



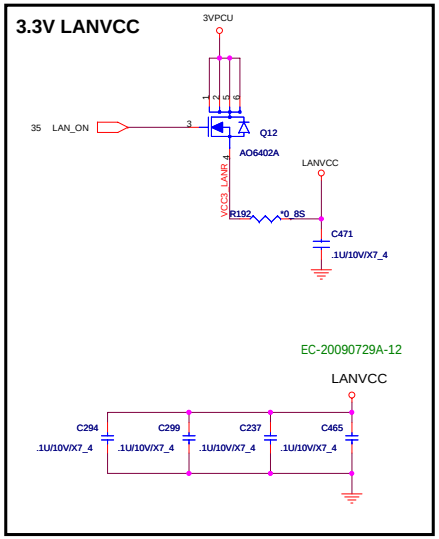
RJ45 Connector





EC-20090729A-12

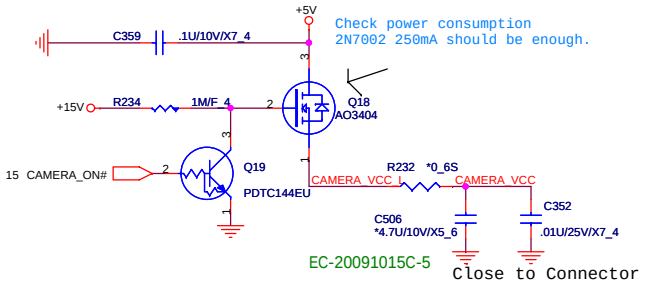
3.3V LANVCC



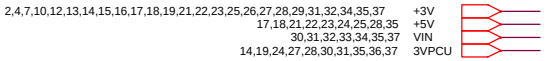
PROJECT : PS1
Quanta Computer Inc.

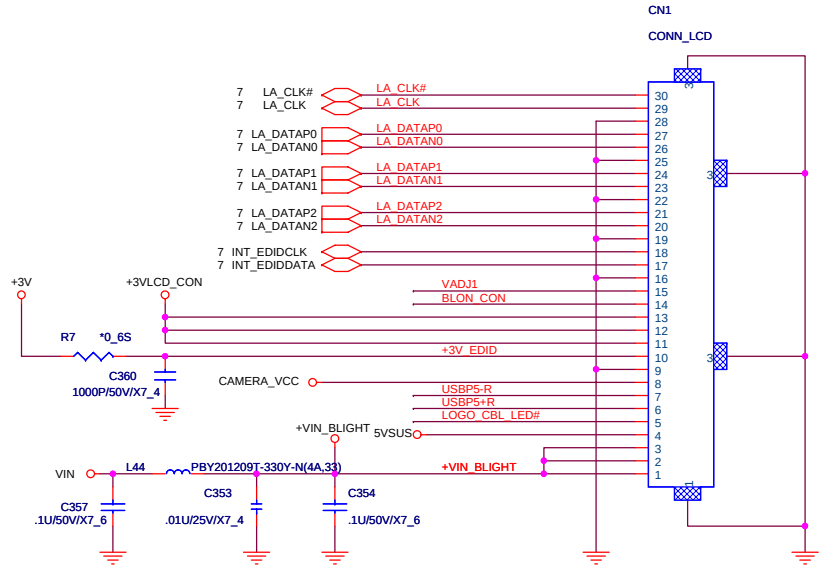
Size	Document Number	Rev
Custom	<Doc> LAN (RTL8111DL, RJ45)	1A
Date: Saturday, October 31, 2009	Sheet 19 of 41	

CCD POWER CONTROL



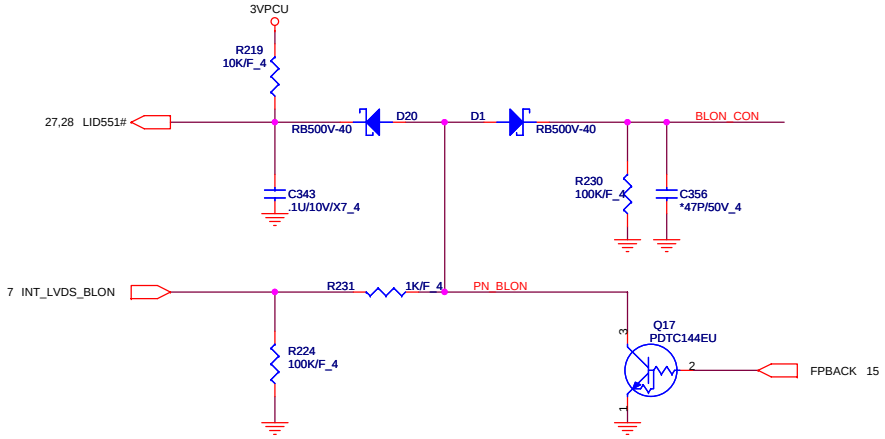
SUPPORT 13.3" LED TYPE LCD

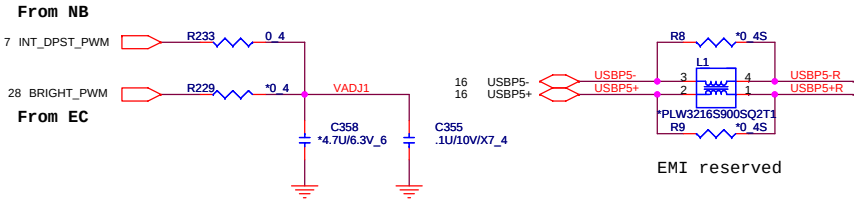




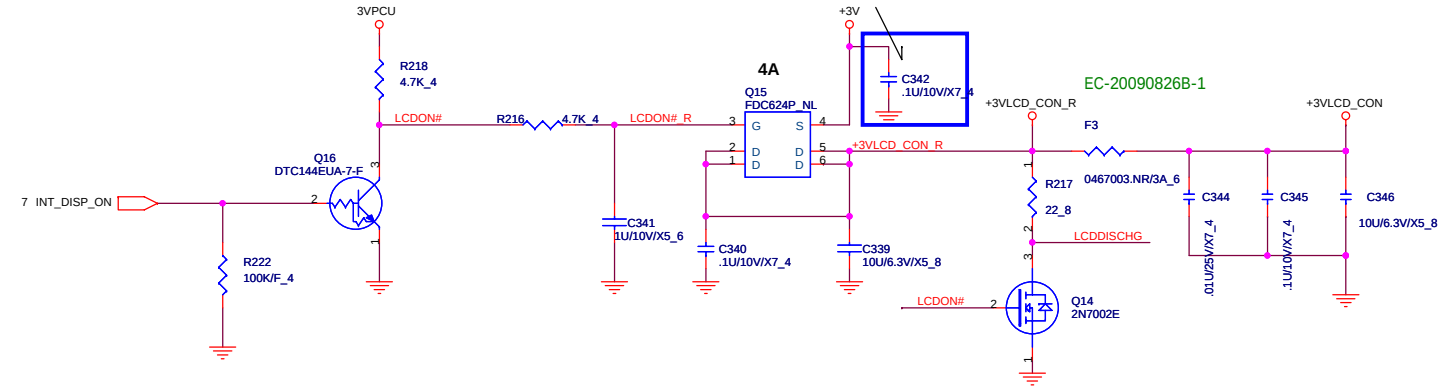
Close to LCD Connector

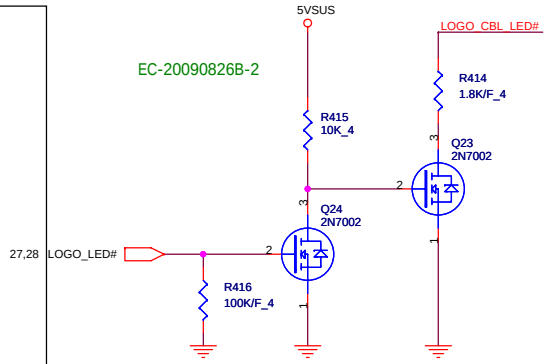
BACK LIGHT CONTROL



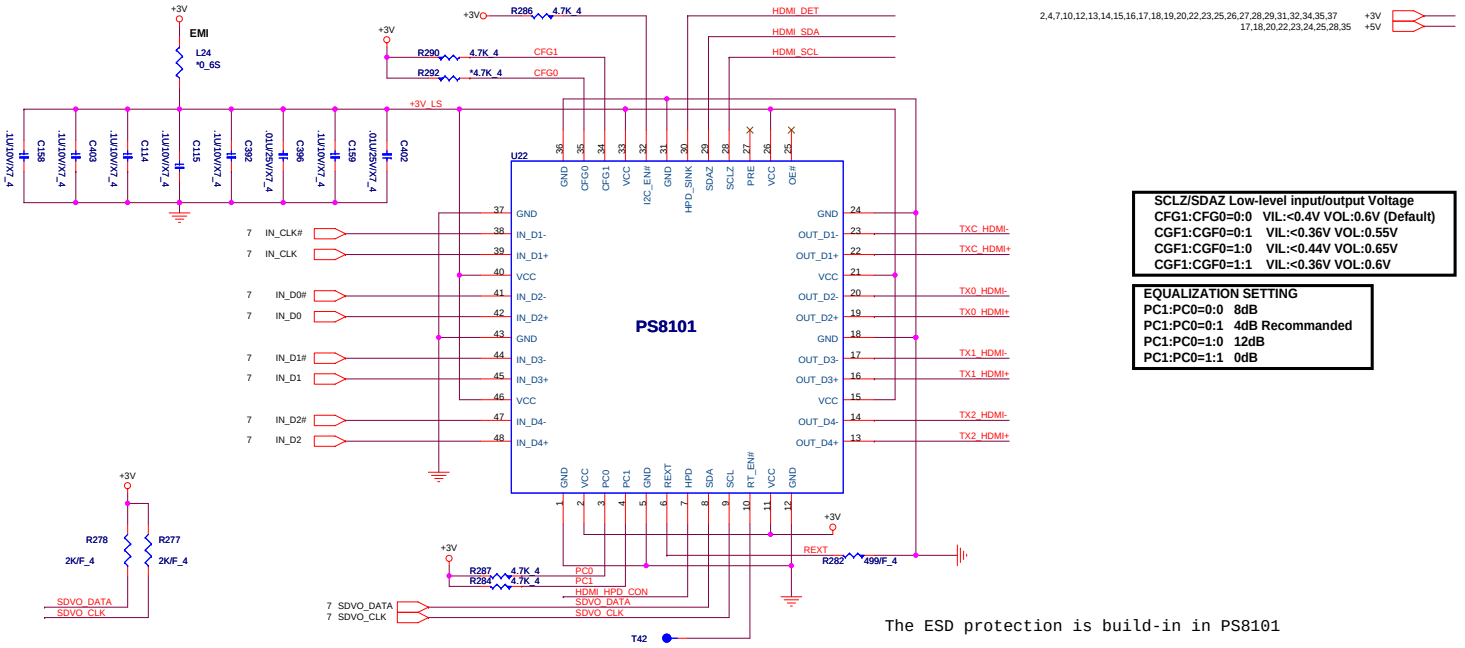


BACK LIGHT SUPPLY





Quanta Computer Inc.	PROJECT : PS1	
Size: Custom	Document Number: <Doc> CONN (LVDS, CCD)	Rev: 1A
Date: Saturday, October 31, 2009	Sheet 20 of 41	

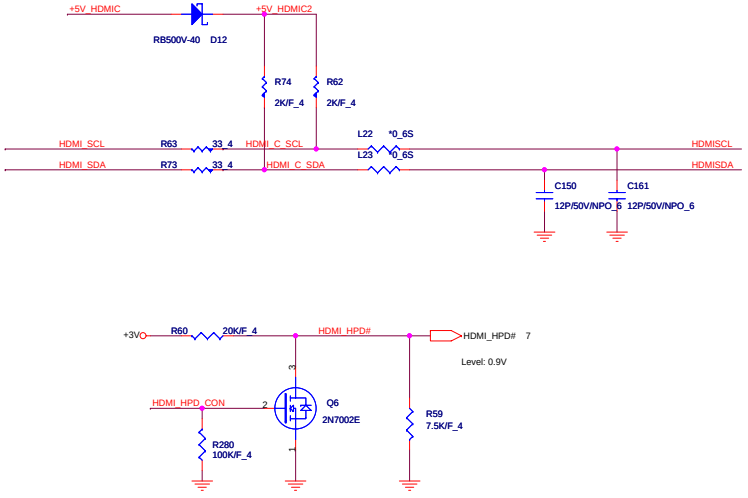


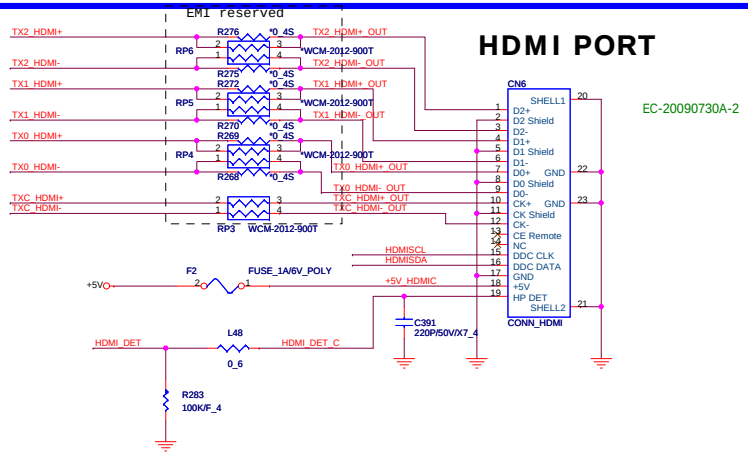
2,4,7,10,12,13,14,15,16,17,18,19,20,22,23,25,26,27,28,29,31,32,34,35,37 +3V
17,18,20,22,23,24,25,28,35 +5V

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

The ESD protection is build-in in PS8101





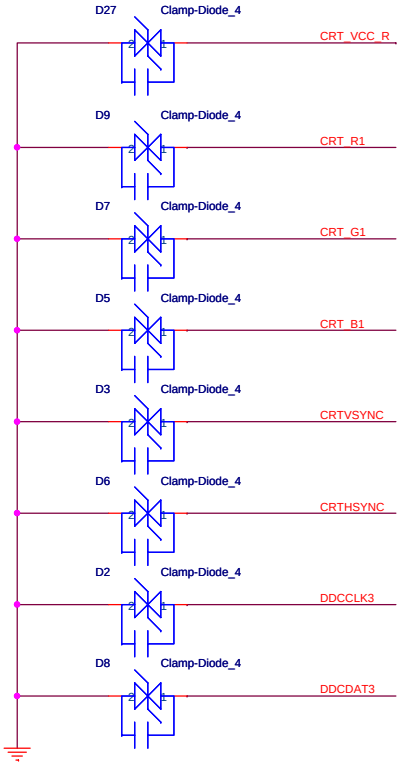
HPD# Inverting Level Shifting Circuit

PROJECT : PS1		
Quanta Computer Inc.		
Size: C	Document Number: <Doc> CONN (HDMI, level Shift)	Rev: 1A
Date: Saturday, October 31, 2009	Sheet 21 of 41	

New Tooling footpint was on-Going 0730

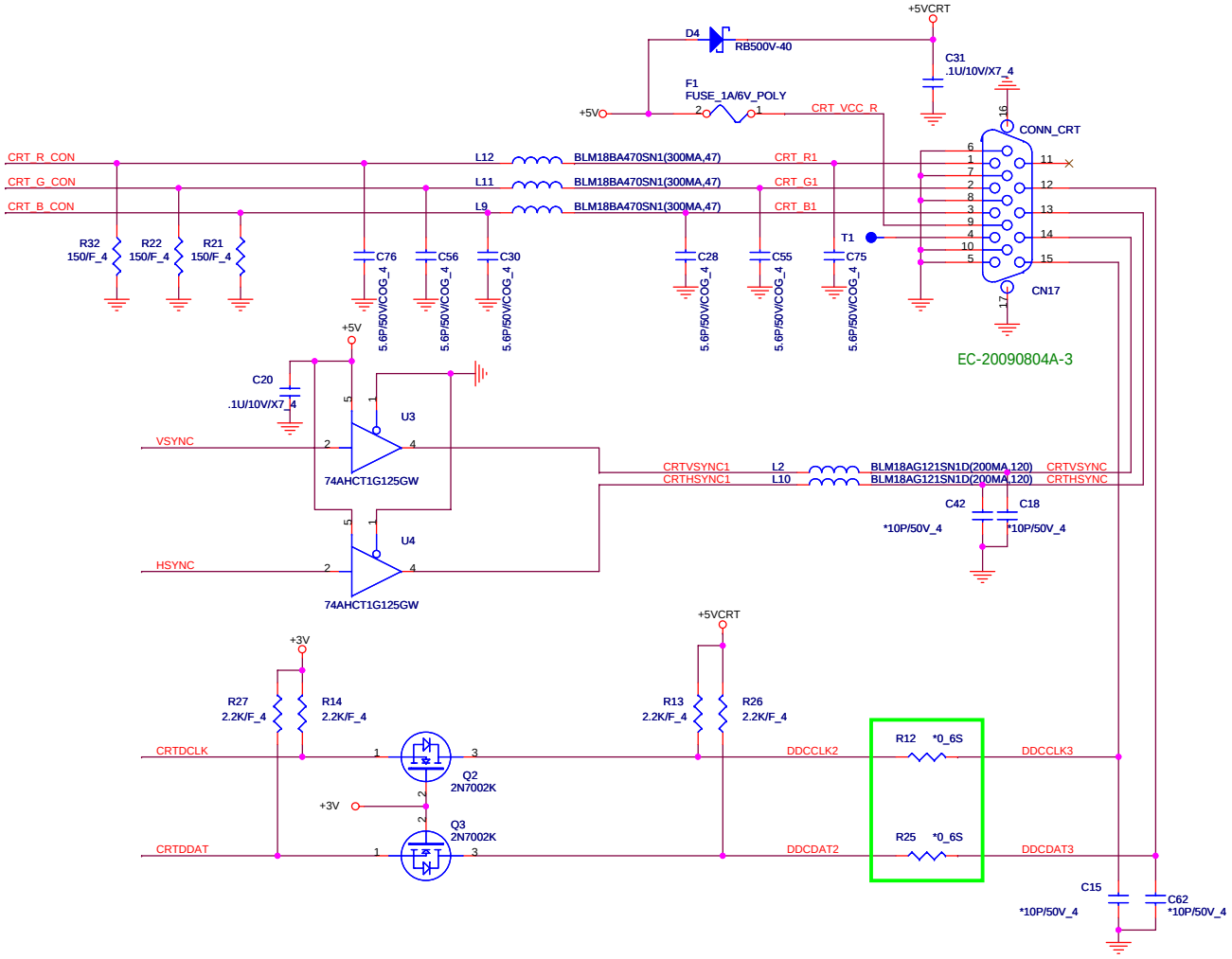
CRT PORT

7 CRT_R_CON → CRT_R_CON
7 CRT_G_CON → CRT_G_CON
7 CRT_B_CON → CRT_B_CON
7 HSYNC → HSYNC
7 VSYNC → VSYNC
7 CRTDCLK → CRTDCLK
7 CRTDDAT → CRTDDAT



EC-20090826B-3

By ESD suggestion EC-20090805A-3

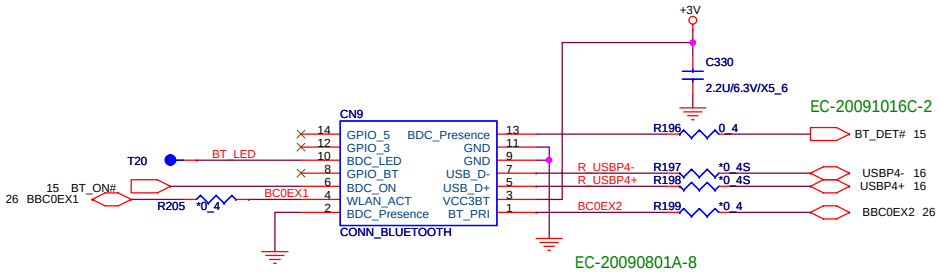


PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> CONN (CRT)	1A
Date: Saturday, October 31, 2009	Sheet 22 of 41	

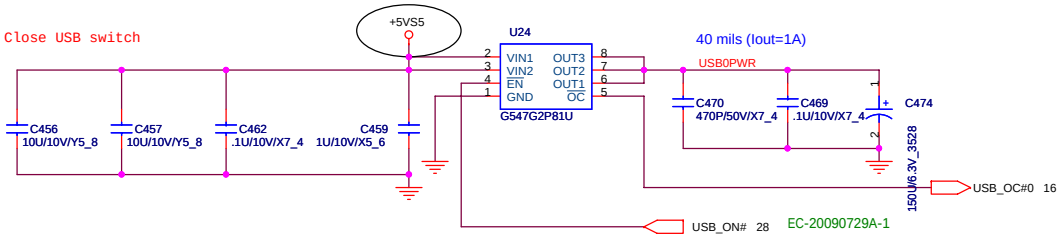
Blue Tooth control

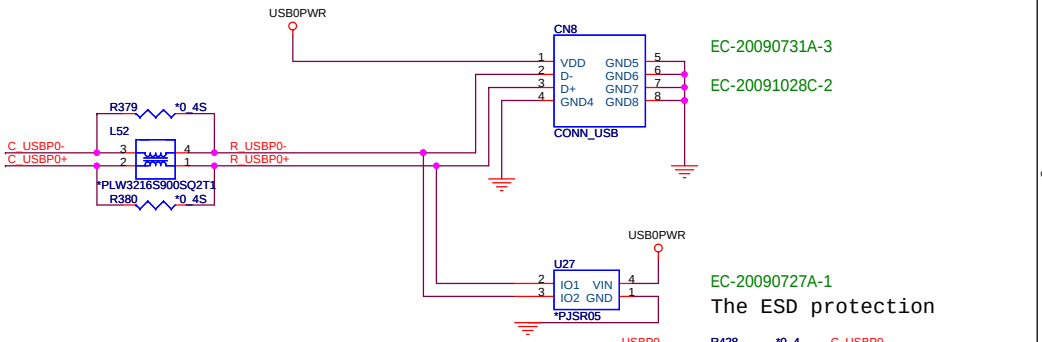
EC-20090729A-3
EC-20090730A-1



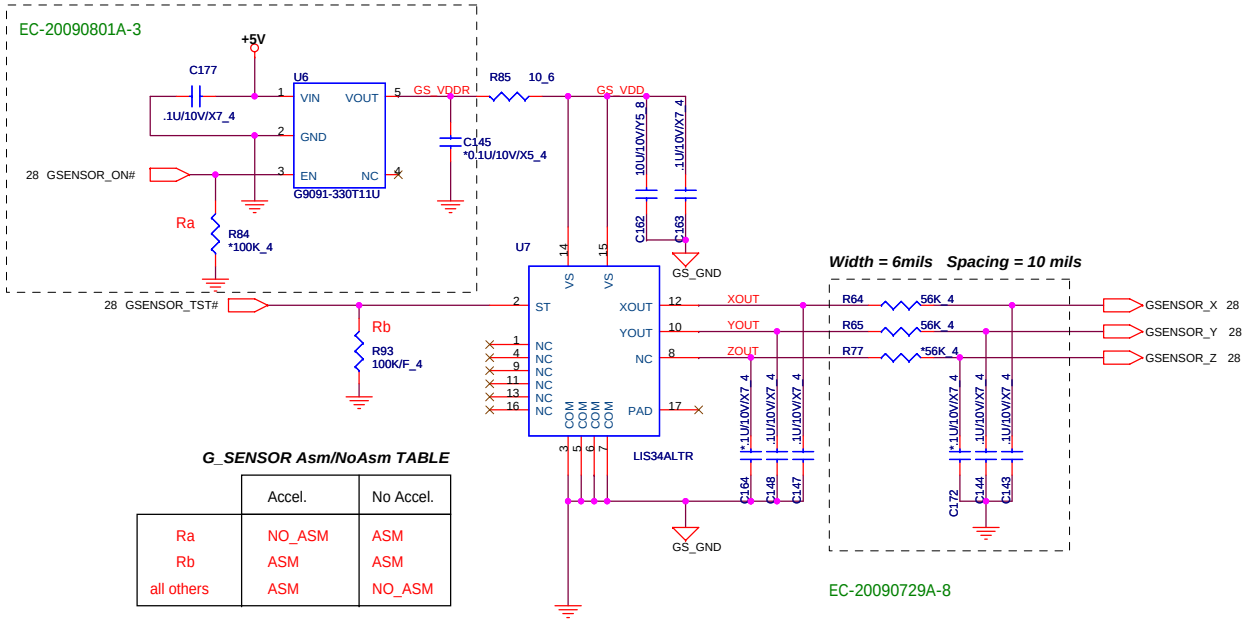
USB port X1 (Left-side)

EC-20090801A-4





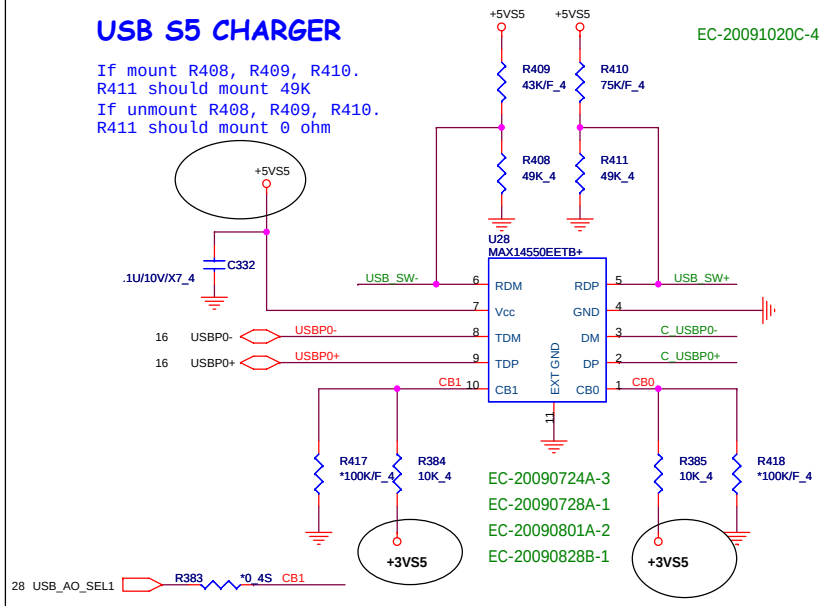
Accelerometer Sensor



USB S5 CHARGER

EC-20091020C-4

If mount R408, R409, R410.
R411 should mount 49K
If unmount R408, R409, R410.
R411 should mount 0 ohm

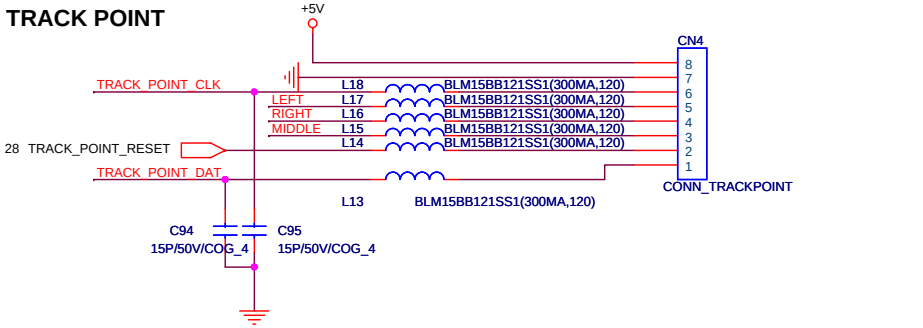


PROJECT : PS1
Quanta Computer Inc.

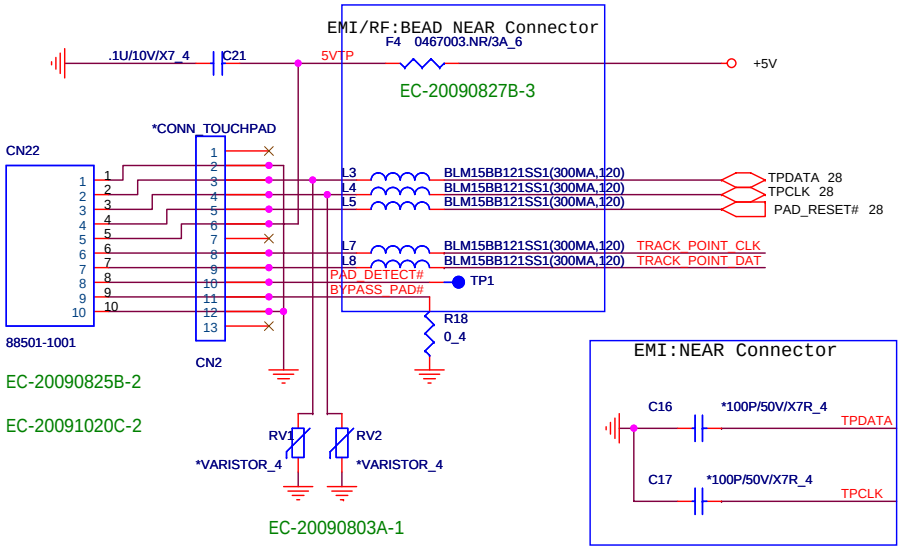
Size	Document Number	Rev
Custom	<Doc> CONN (USB, BT, G sensor)	1A
Date: Saturday, October 31, 2009	Sheet 23 of 41	

TOUCH PAD CONNECTOR

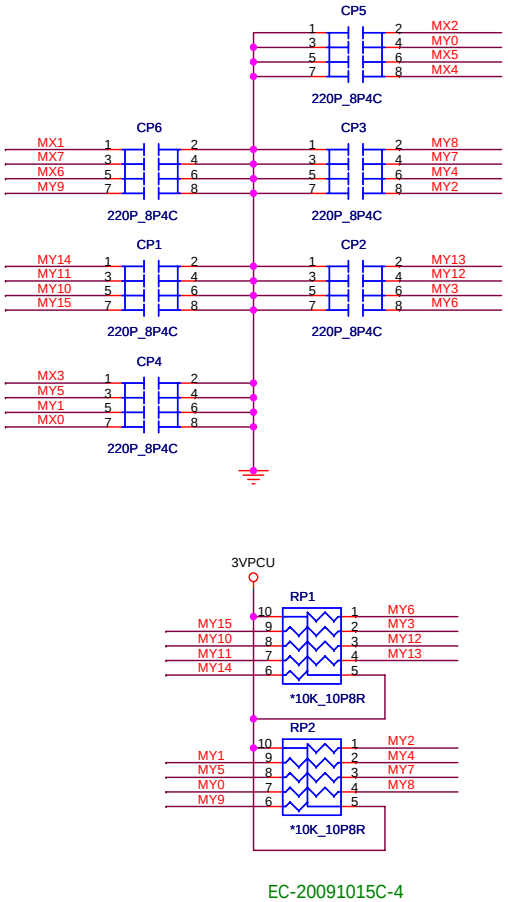
TRACK POINT



TOUCH PAD

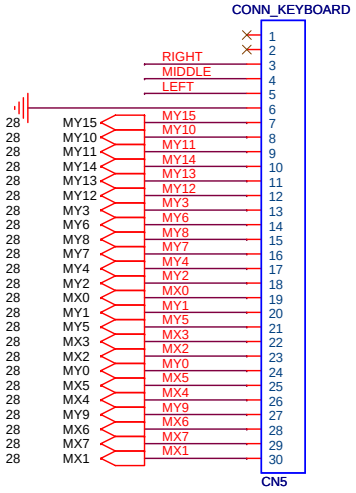


KEYBOARD CONNECTOR



EC-20091015C-4

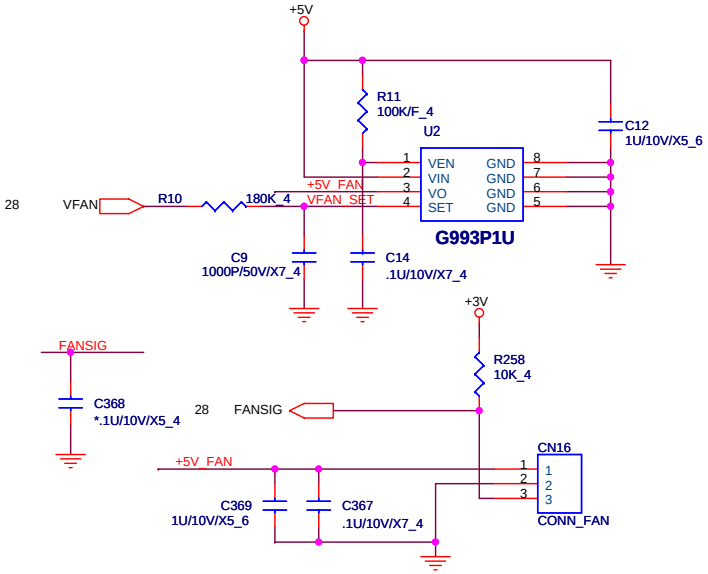
KEYBOARD connector



PROJECT :PS1
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> CONN (KB, TP, TrackPoint)	1A
Date: Saturday, October 31, 2009	Sheet 24 of 41	

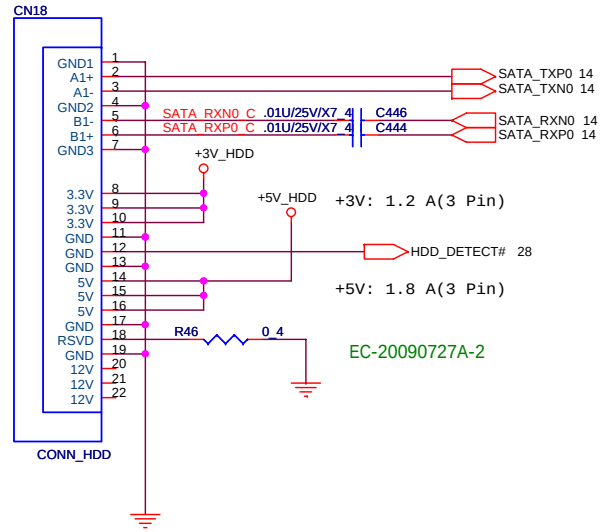
FAN CONTROL



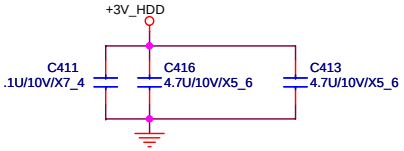
SATA-HDD CONNECTOR

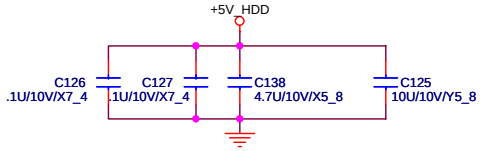
EC-20090805A-1

EC-20090804A-3



Reserved for power consumption measurement

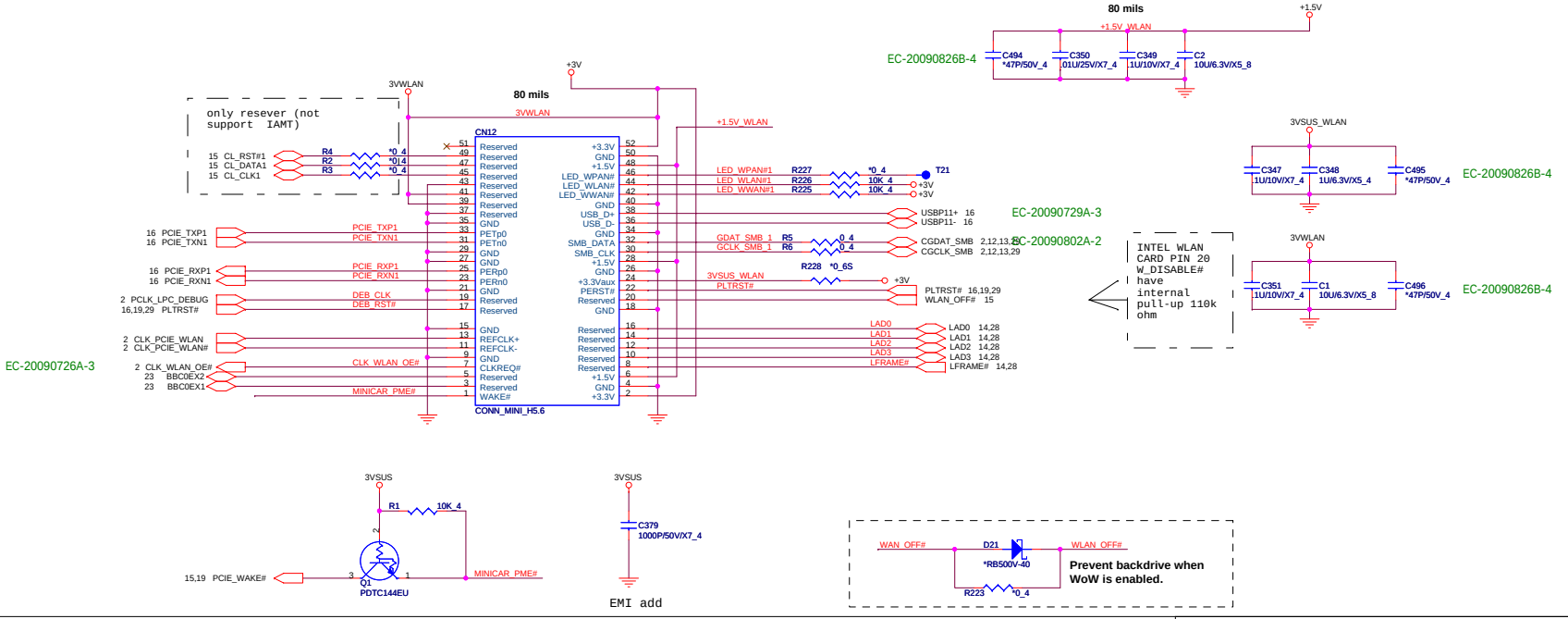




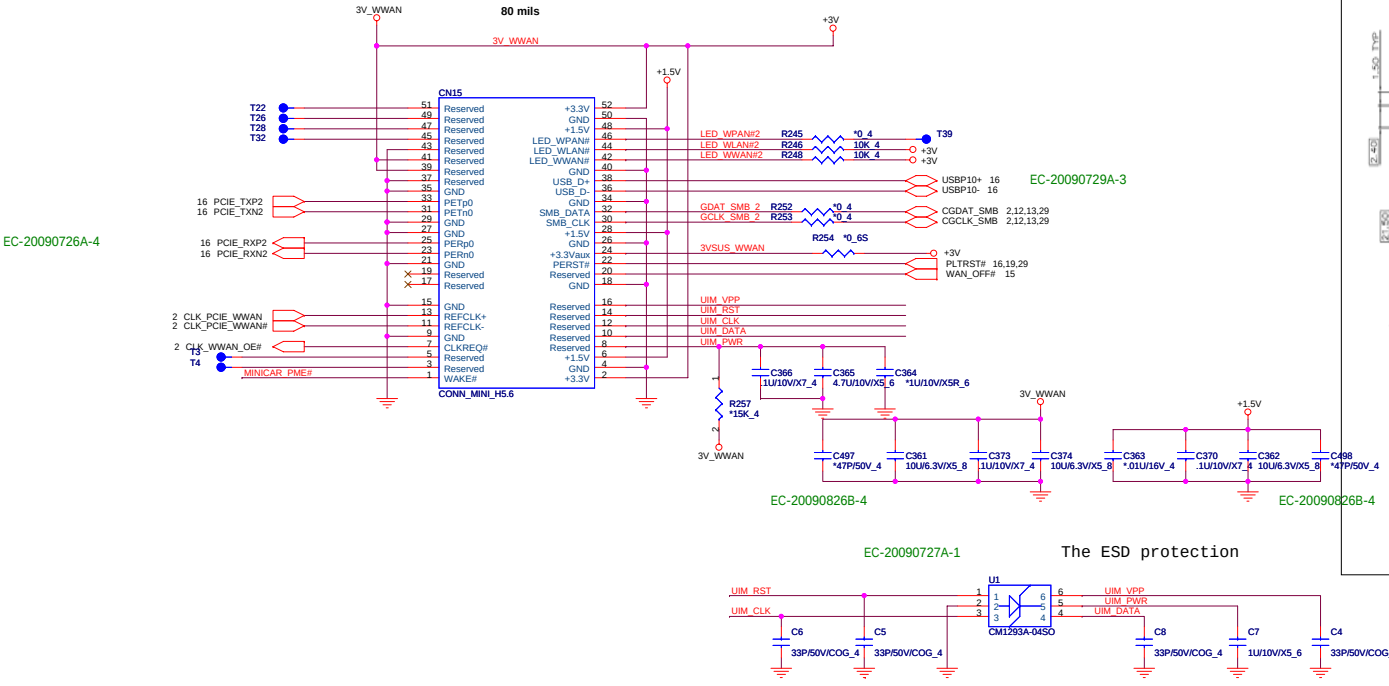
PROJECT :PS1
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> CONN (HDD,FAN)	1A
Date: Saturday, October 31, 2009	Sheet 25 of 41	

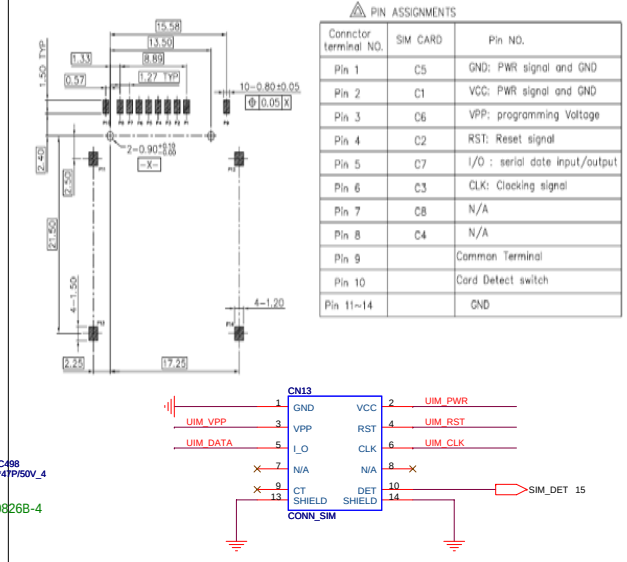
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)



SIM SOCKET



PROJECT : PS1
Quanta Computer Inc.

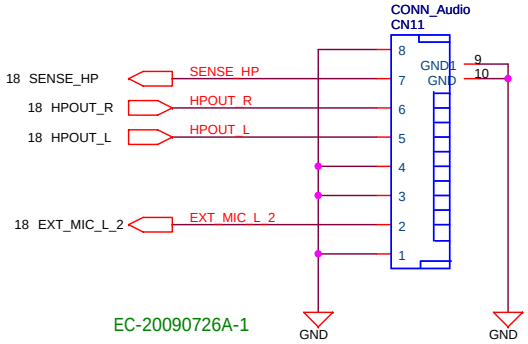
Size	Document Number	Rev
C	<Doc> CONN (MINI PCI-E, SIM)	1A

Date: Saturday, October 31, 2009 Sheet 26 of 41

EC-20090726A-1

Function Board

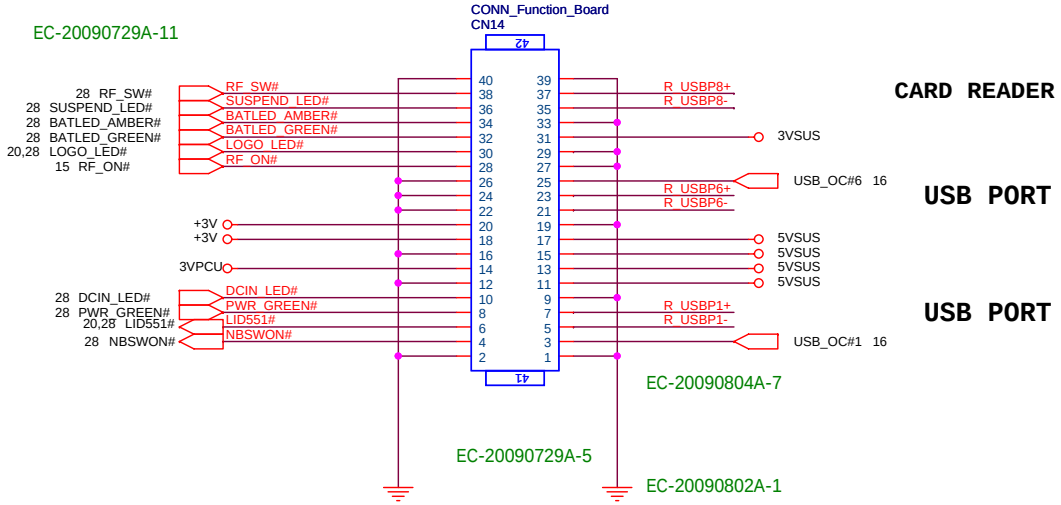
Audio connect



EC-20090726A-1
EC-20090729A-4
EC-20090729A-5
EC-20090729A-17
EC-20090730A-4

EC-20090726A-2

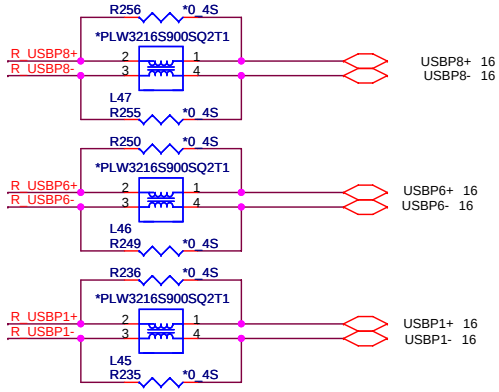
EC-20090729A-11



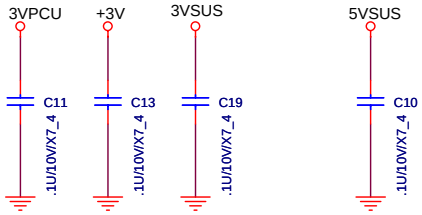
EC-20090804A-7

EC-20090729A-5

EC-20090802A-1

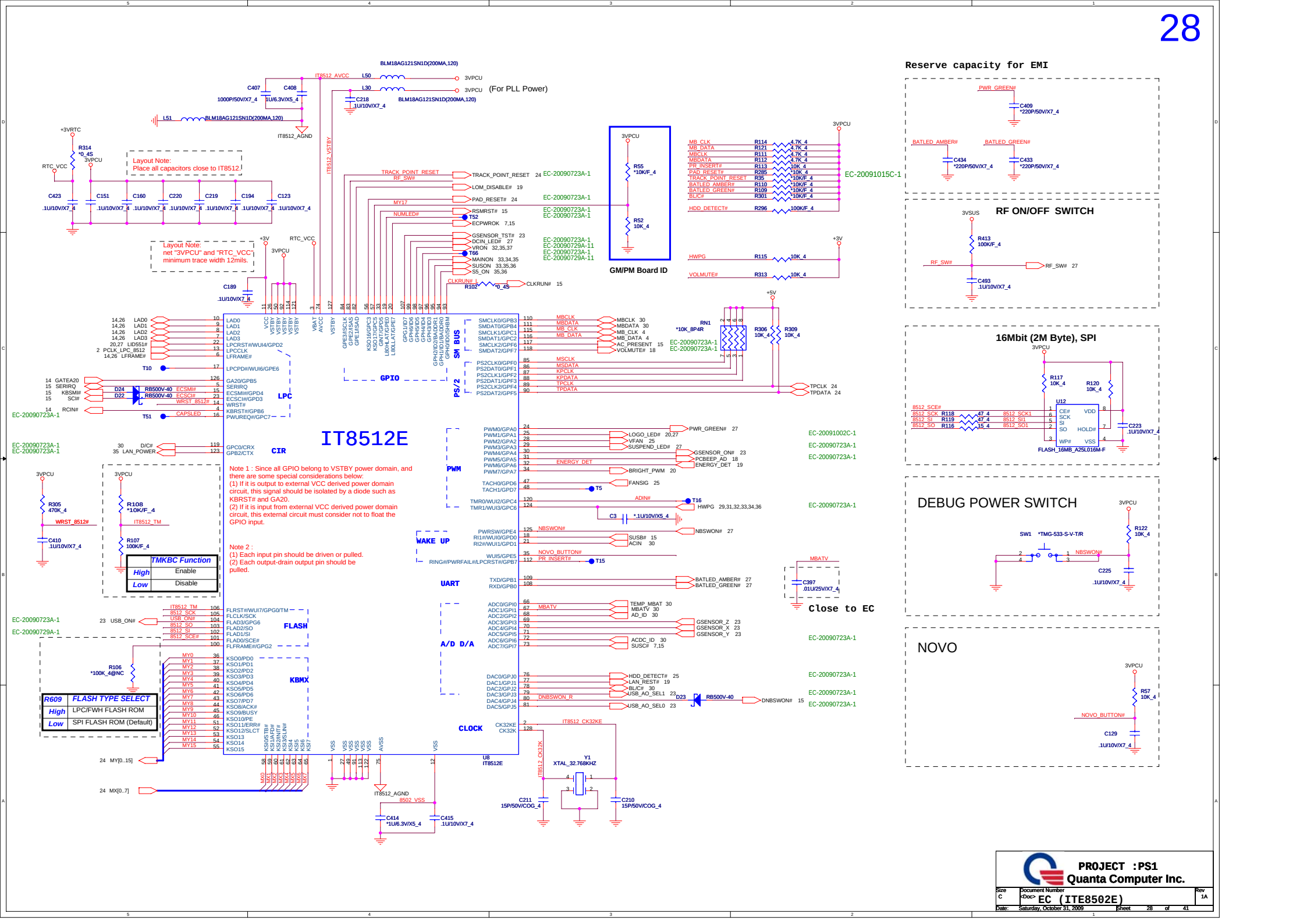


EC-20090730A-5



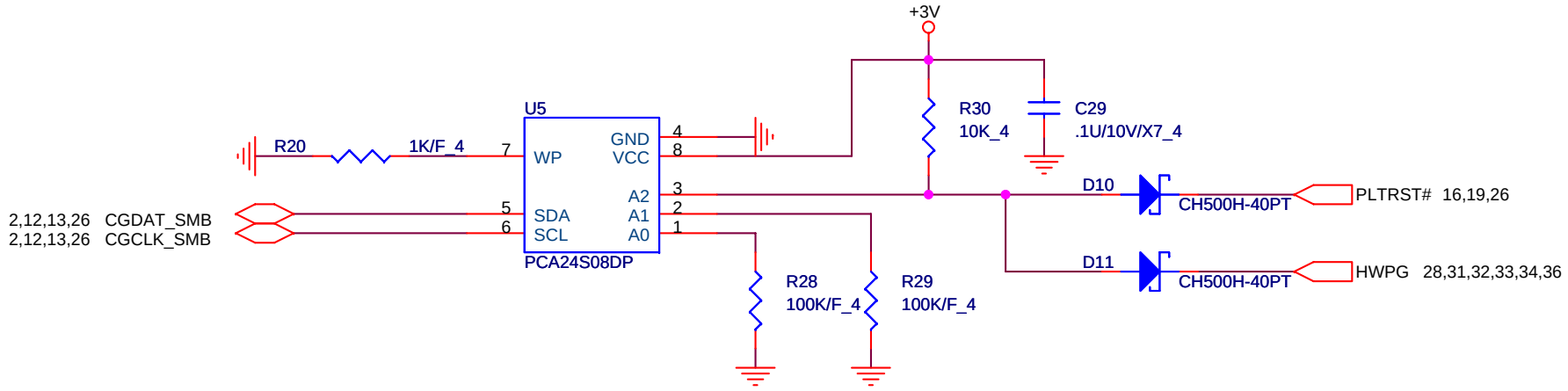
PROJECT :PS1
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> CONN (Wire to Board)	1A
Date: Saturday, October 31, 2009	Sheet 27 of 41	


IT8512E
Reserve capacity for EMI
PWR_GREEN#
C409 *220P/50V/X7_4
BATLED_AMBER#
BATLED_GREEN#
C434 *220P/50V/X7_4
C433 *220P/50V/X7_4
RF ON/OFF SWITCH
3VSUS
R413 100K/F_4
RF_SW#
RF_SW# 27
C493 .1U/10V/X7_4
16Mbit (2M Byte), SPI
3VPCU
R117 10K_4
R120 10K_4
U12
8512_SCE#
8512_SCK R118 47_4 8512_SCK1
8512_SI R119 47_4 8512_SI1
8512_SO R116 15_4 8512_SO1
CE# SCK SI SO WP# VDD HOLD# VSS
C223 .1U/10V/X7_4
FLASH_16MB_A25L016M-F
DEBUG POWER SWITCH
SW1 *TMG-533-S-V-T/R
R122 10K_4
NBSWON#
C225 .1U/10V/X7_4
NOVO
R57 10K_4
NOVO_BUTTON#
C129 .1U/10V/X7_4
GM/PM Board ID
R55 *10K/F_4
R52 10K_4
EC-20091015C-1
MB_CLK R114 4.7K_4
MB_DATA R121 4.7K_4
MBCLK R111 4.7K_4
MBDATA R112 4.7K_4
PR_INSERT# R113 10K_4
PAD_RESET# R285 *10K_4
TRACK_POINT_RESET R35 *10K/F_4
BATLED_AMBER# R110 *10K/F_4
BATLED_GREEN# R109 *10K/F_4
BLC# R301 *10K/F_4
HDD_DETECT# R296 100K/F_4
HWPG R115 10K_4
VOLMUTE# R313 10K_4
BLM18AG121SN1D(200MA,120)
IT8512_AVCC
L50 3VPCU
L30 3VPCU (For PLL Power)
C407 1000P/50V/X7_4
C408 1U/6.3V/X5_4
C218 .1U/10V/X7_4
L51 BLM18AG121SN1D(200MA,120)
IT8512_AGND
IT8512_VSTBY
+3VRTC
R314 *0_4S
RTC_VCC
Layout Note: Place all capacitors close to IT8512
C423 .1U/10V/X7_4
C151 .1U/10V/X7_4
C160 .1U/10V/X7_4
C220 .1U/10V/X7_4
C219 .1U/10V/X7_4
C194 .1U/10V/X7_4
C123 .1U/10V/X7_4
Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.
C189 .1U/10V/X7_4
+3V
TRACK_POINT_RESET
RF_SW#
LOM_DISABLE# 19
PAD_RESET# 24
MY17
RSMRST# 15
NUMLED#
T52
ECPWROK 7,15
GSENSOR_TST# 23
DCIN_LED# 27
VRON 32,35,37
T66
MAINON 33,34,35
SUSON 33,35,36
S5_ON 35,36
CLKRUN# L
R102 *0_4S
CLKRUN# 15
EC-20090723A-1
EC-20090729A-11
LAD0 LAD1 LAD2 LAD3
LPCRST#/WUI4/GPD2
LPCCLK
LFRAME#
LPCPD#/WUI6/GPE6
GA20/GPB5
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
WRST#
KBRST#/GPB6
PWUREQ#/GPC7
LPC
GATEA20
SERIRQ
KBSMI#
SCI#
RCIN#
ECSMI# D24 RB500V-40
ECSCI# D22 RB500V-40
WRST_8512#
CAPSLED
T51
GPIO
SM BUS
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7
MBCLK
MBDATA
MB_CLK
MB_DATA
MB_DATA 4
AC_PRESENT 15
VOLMUTE# 18
RN1 *10K_8P4R
R306 10K_4
R309 10K_4
PS/2
PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5
MSCLK
MSDATA
KPCLK
KPDATA
TPCLK
TPDATA
TPCLK 24
TPDATA 24
CIR
GPC0/CRX
GPB2/CTX
D/C#
LAN_POWER
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
PWM
PWM0/GPA0 LOGO_LED# 20,27
PWM1/GPA1 VFAN 25
PWM2/GPA2 SUSPEND_LED# 27
PWM3/GPA3
PWM4/GPA4 GSENSOR_ON# 23
PWM5/GPA5 PCBEEP_AD 18
PWM6/GPA6 ENERGY_DET 19
PWM7/GPA7 BRIGHT_PWM 20
ENERGY_DET
TACH0/GPD6 FANSIG 25
TACH1/GPD7
T5
TMR0/WUI2/GPC4 ADIN#
TMR1/WUI3/GPC6 HWPG 29,31,32,33,34,36
T16
C3 *.1U/10V/X5_4
WAKE UP
PWRSW/GPE4 NBSWON#
RI1#/WUI0/GPD0 SUSB# 15
RI2#/WUI1/GPD1 ACIN 30
WUI5/GPE5 NOVO_BUTTON#
RING#/PWRFAIL#/LPCRST#/GPB7 PR_INSERT#
T15
UART
TXD/GPB1 BATLED_AMBER# 27
RXD/GPB0 BATLED_GREEN# 27
A/D D/A
ADC0/GPI0 MBATV
ADC1/GPI1 TEMP_MBAT 30
ADC2/GPI2 MBATV 30
ADC3/GPI3 AD_ID 30
ADC4/GPI4 GSENSOR_Z 23
ADC5/GPI5 GSENSOR_X 23
ADC6/GPI6 GSENSOR_Y 23
ADC7/GPI7 ACDC_ID 30
SUSC# 7,15
DAC0/GPJ0 HDD_DETECT# 25
DAC1/GPJ1 LAN_REST# 19
DAC2/GPJ2 BL/C# 30
DAC3/GPJ3 USB_AO_SEL1 23
DAC4/GPJ4 DNBSWON_R
DAC5/GPJ5 USB_AO_SEL0 23
D23 RB500V-40 DNBSWON# 15
MBATV
C397 .01U/25V/X7_4
Close to EC
CLOCK
CK32KE
CK32K
IT8512_CK32KE
IT8512_CK32K
Y1 XTAL_32.768KHZ
C211 15P/50V/COG_4
C210 15P/50V/COG_4
FLASH
FLRST#/WUI7/GPG0/TM
FLCLK/SCK
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE#
FLFRAME#/GPG2
IT8512_TM
8512_SCK
USB_ON#
8512_SO
8512_SI
8512_SCE#
USB_ON# 23
R106 *100K_4@NC
R609 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
KBMX
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
MY[0..15] 24
MX[0..7] 24
R305 470K_4
WRST_8512#
C410 .1U/10V/X7_4
R108 *10K/F_4
IT8512_TM
R107 100K/F_4
TMKBC Function
High Enable
Low Disable
U8 IT8512E
IT8512_AGND
8502_VSS
C414 *1U/6.3V/X5_4
C415 .1U/10V/X7_4

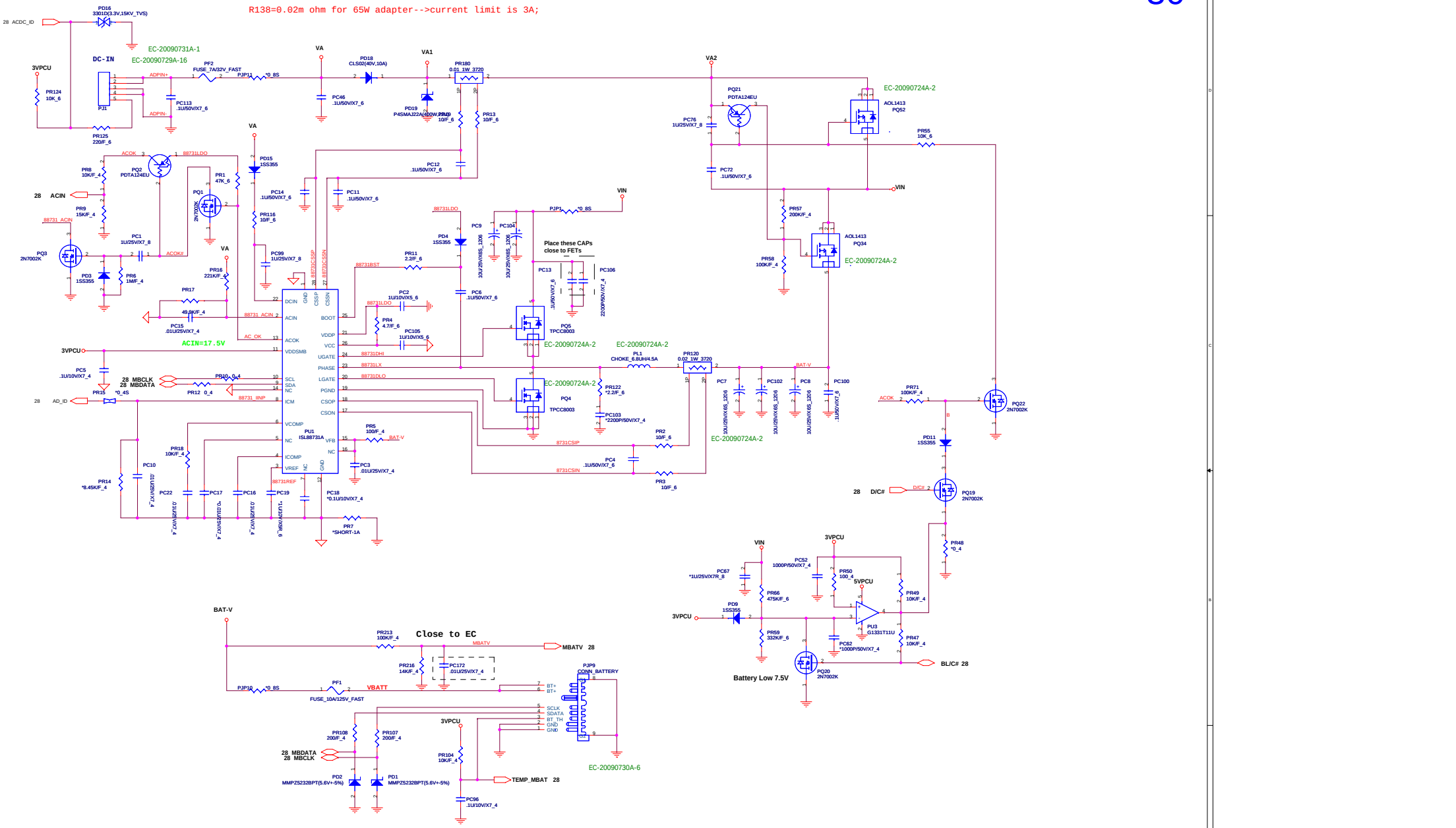
RFID EEPROM

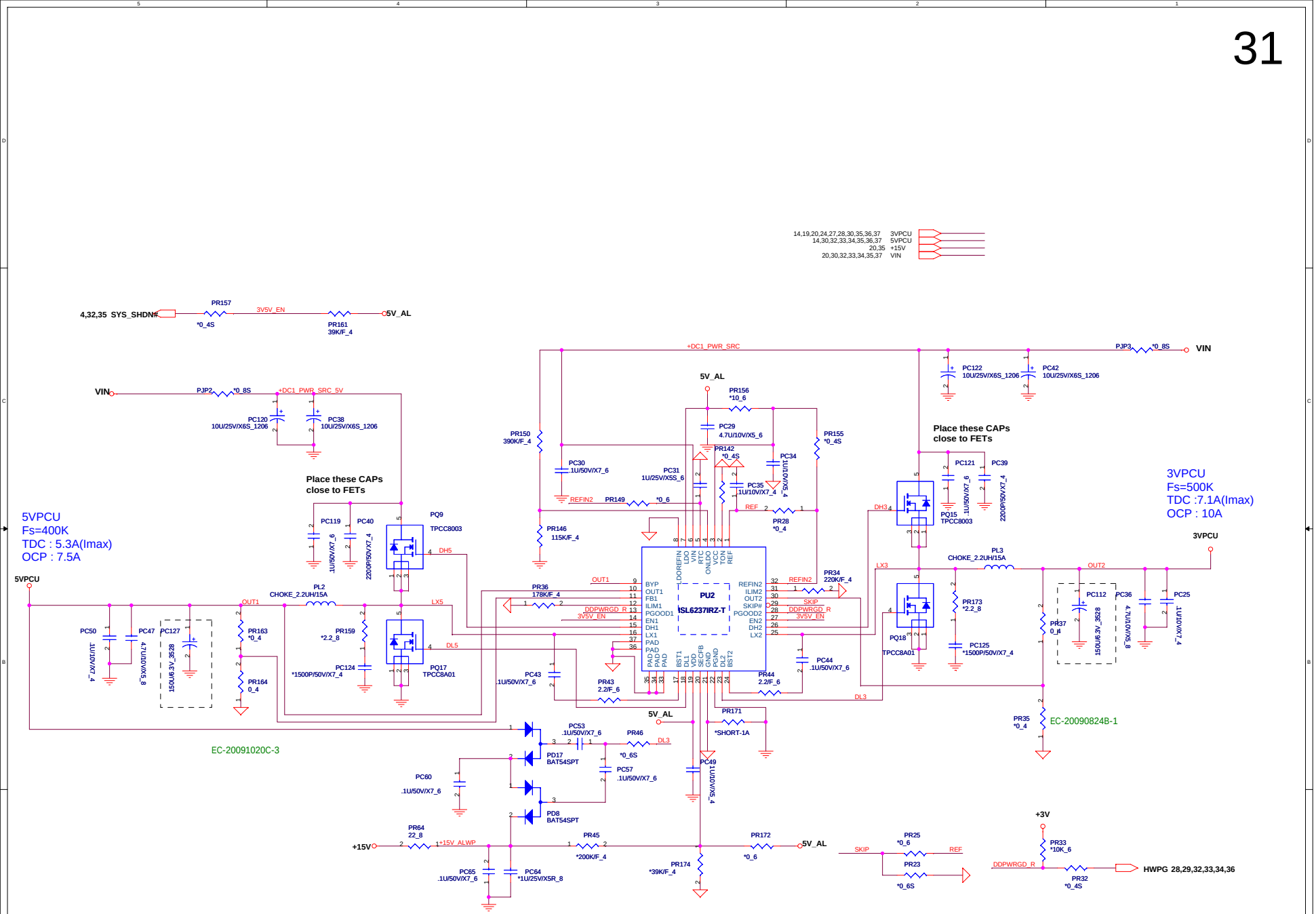
EC-20090804A-5



PROJECT : PS1 Quanta Computer Inc.		
Size: A	Document Number: <Doc> RFID EEPROM	Rev: 1A
Date: Saturday, October 31, 2009	Sheet 29 of 41	

R138=0.02m ohm for 65W adapter-->current limit is 3A;

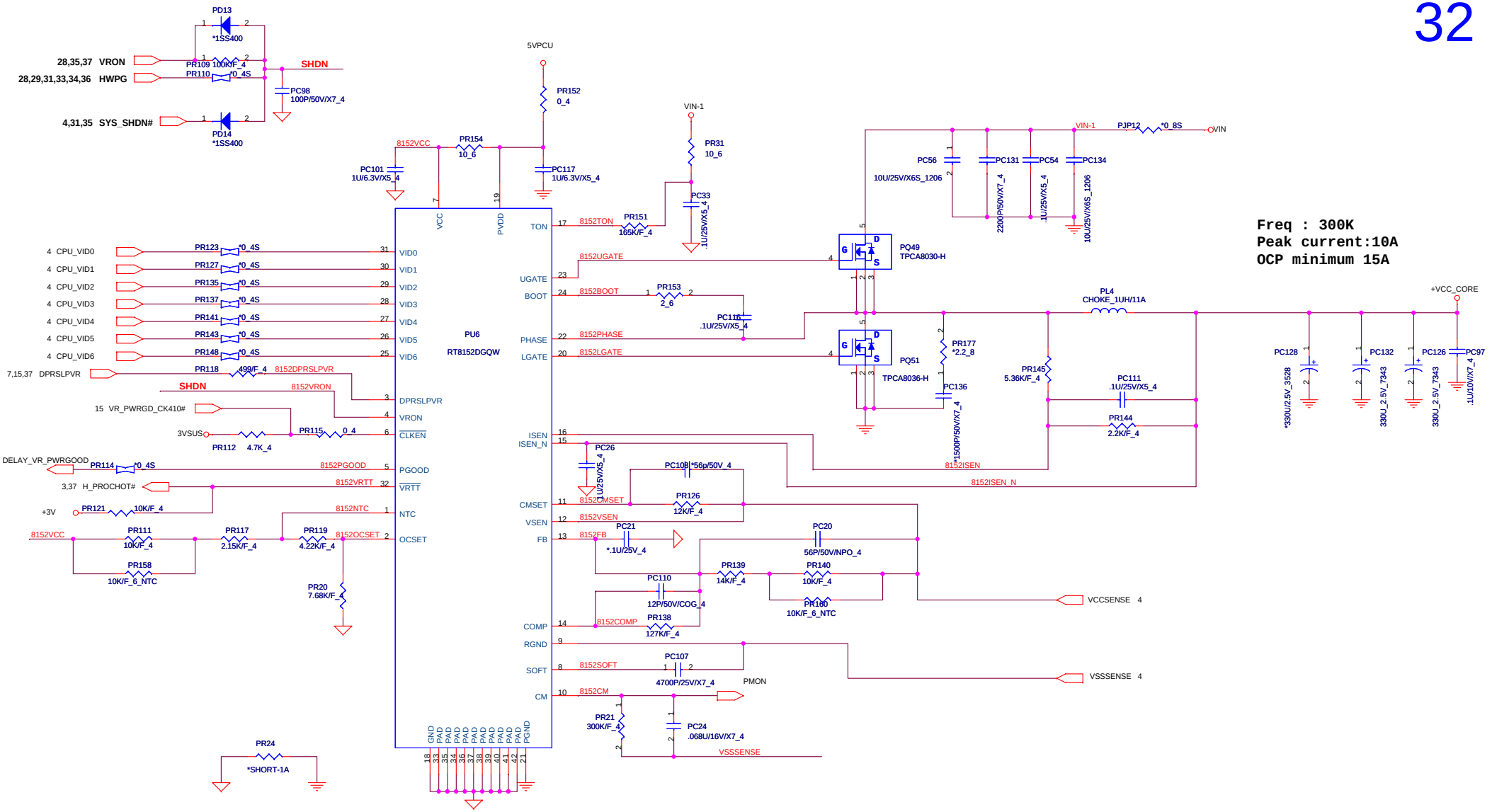




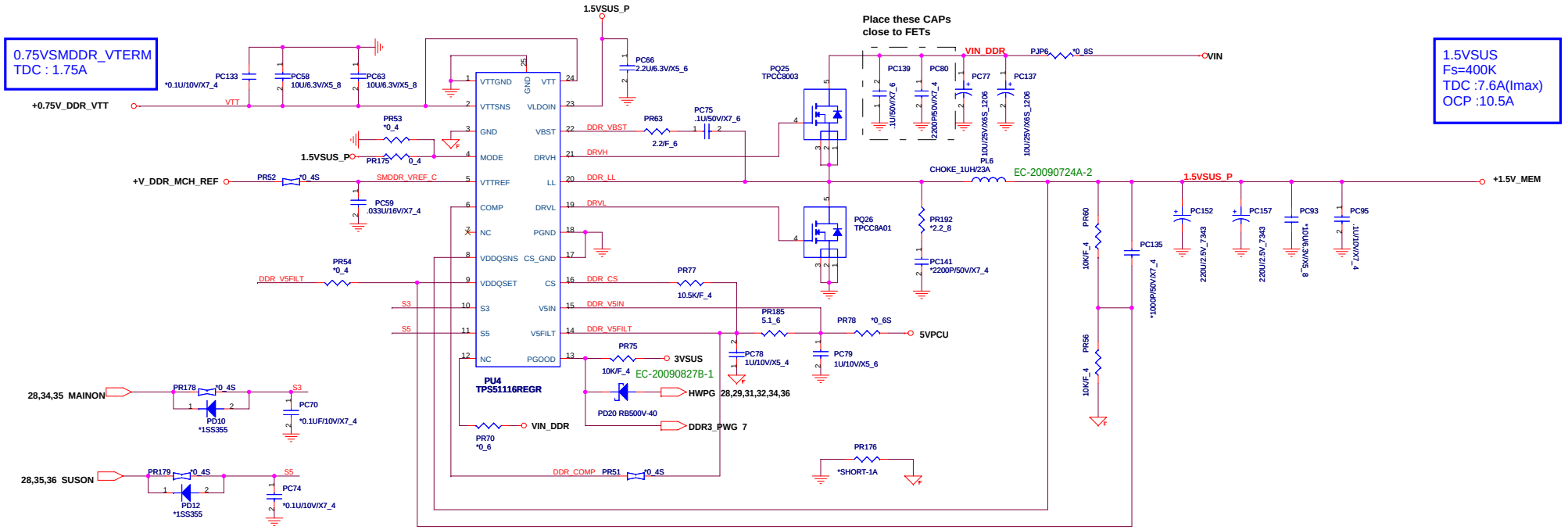
PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> POWER_3V/5V (ISL6237)	1A

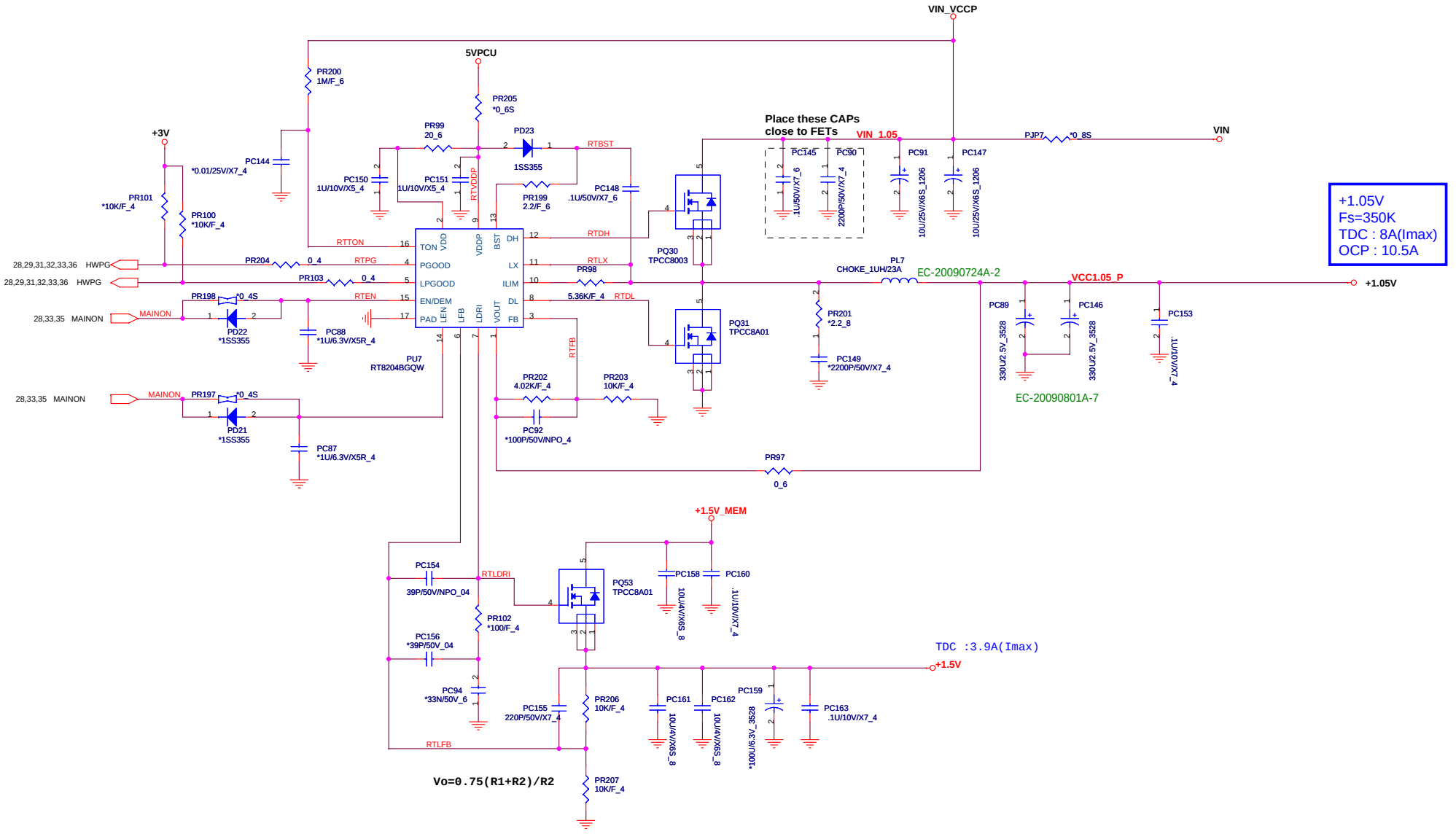
Date: Saturday, October 31, 2009 Sheet 31 of 41



Quanta Computer Inc.	PROJECT : PS1		
Size: Custom	Document Number: <Doc> POWER_CPU CORE (RT8152B)		Rev: 1A
Date: Saturday, October 31, 2009	Sheet 32 of 41		



PROJECT : PS1	
Quanta Computer Inc.	
Size: Custom	Document Number: <Doc> POWER_DDR3(TPS51116) Rev: 1A
Date: Saturday, October 31, 2009	Sheet 33 of 41



PROJECT : PS1		
Quanta Computer Inc.		
Size: Custom	Document Number: <Doc> POWER_1.05V&1.5V(RT8204C)	Rev: 1A
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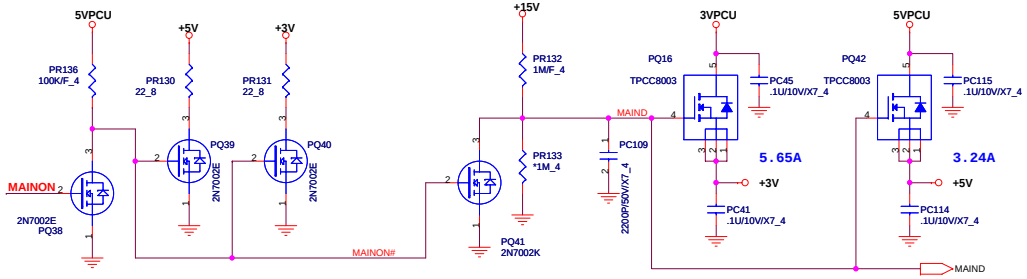
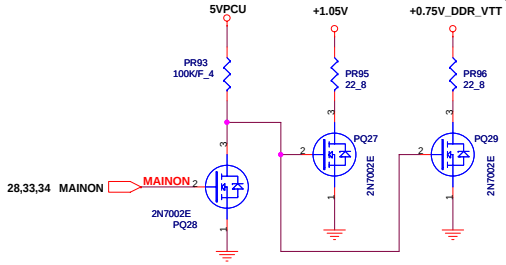
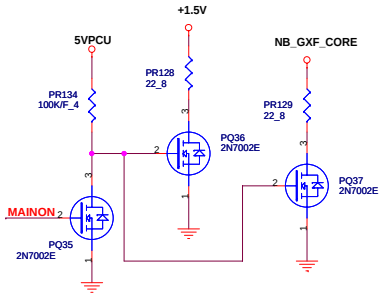
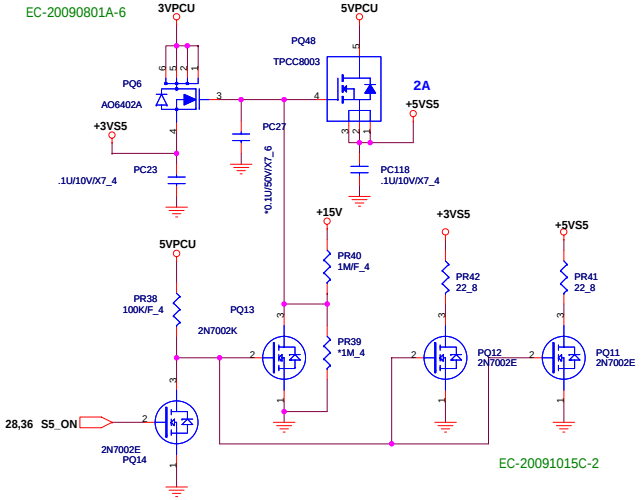
DISCHARGE



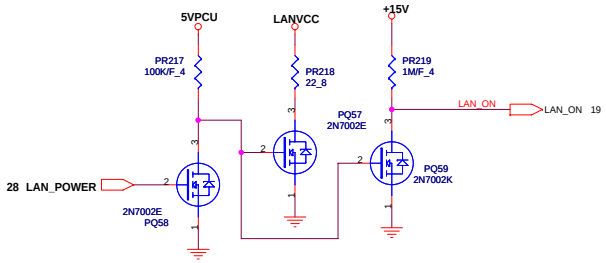




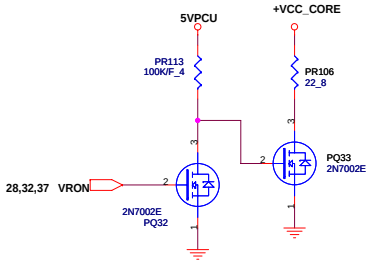
3V_S5, 5V_S5

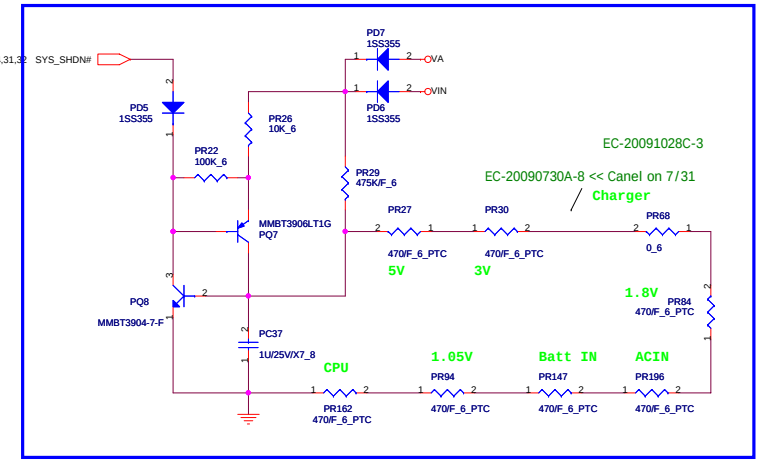


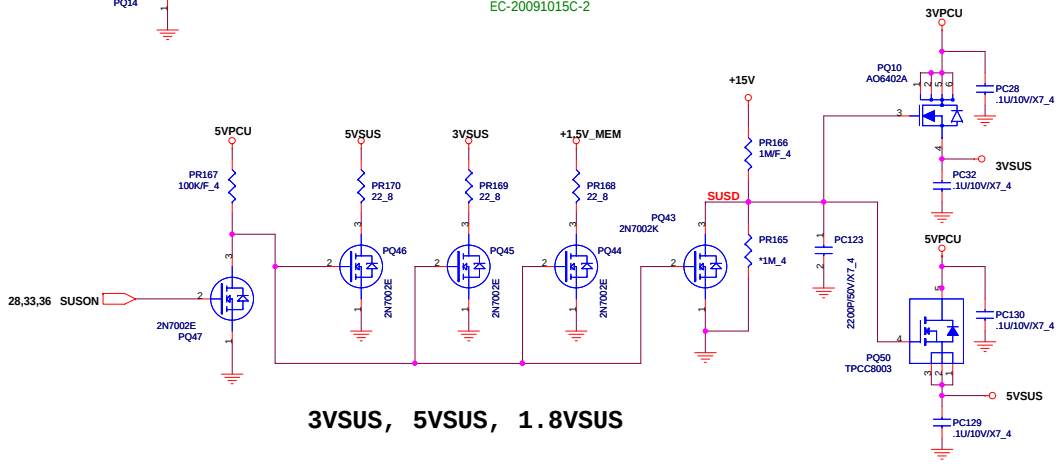
LANVCC



VCC_CORE







3VSUS, 5VSUS, 1.8VSUS

EC-20090801A-5

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	1A

POWER_Discharge

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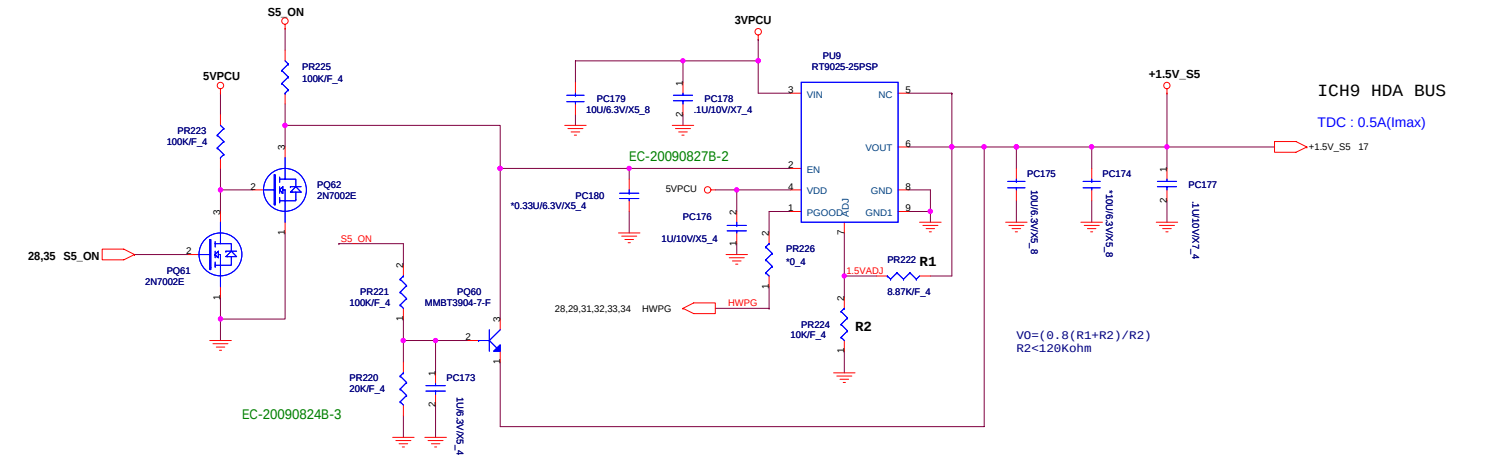

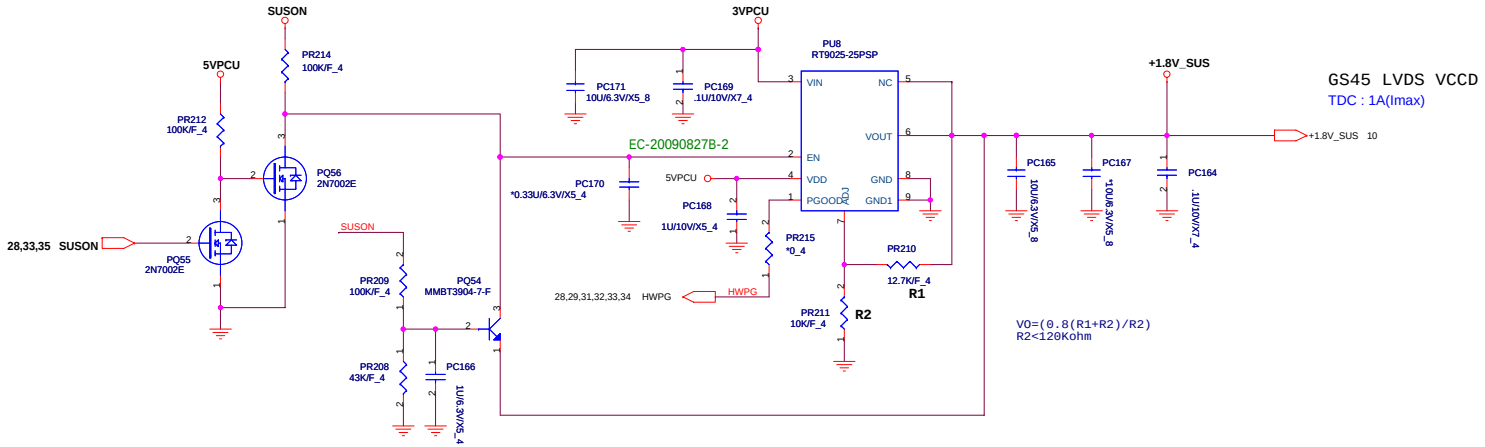

PROJECT : PS1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER_LDO	1A

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EC-20090804A-2
EC-20091020C-1

EC-20090803A-2

EC-20090726A-5

EC-20090824B-2

EC-20090813B-1

EC-20090726A-5

EC-20090730A-7

EC-20090726A-5

PU5
***MAX8796GTJ+**

tSW = 16.3pF x (RTON + 6.5K)
fsw=300KHz

Load-line=-6.9mV/A

ESR=9m

PS-Mika check with TIM about VCC_SENSE and VSS_SENSE

PS-Mika check with TIM

VID 1.0V

PROJECT	PS1
Quanta Computer Inc.	
Size: Custom	Document Number: <Doc> POWER_Render(MAX8796GTJ+) Rev: 1A
Date: Saturday, October 31, 2009	Sheet 37 of 41

HOLE6
*h-c146d146n

HOLE8
*h-c146d146n

CPU NUT

HOLE19
H-TC187BC177D146P2

VGA NUT

HOLE20
*H-TC197BC71D51P2

SB NUT
EC-20090728A-3

HOLE15
H-TC167BC75D55P2

HOLE16
H-TC167BC75D55P2

WWAN NUT

HOLE17
H-TC167BC75D55P2

HOLE18
H-TC167BC75D55P2

WLAN NUT

HOLE10
H-TC236BC154D118P2

Bluetooth NUT
EC-20090730A-10
EC-20091014C-2

HOLE1
*h-c236d91p2

HOLE3
*h-c236d91p2

HOLE7
*h-c236d91p2

HOLE5
*h-c236d91p2

HOLE12
*h-c236d91p2

HOLE14
*h-c236d98p2

HOLE11
*h-c236d91p2

HOLE9
*h-c236d91p2

MB Screw Hole
EC-20090730A-9
EC-20090804A-4

HOLE2
*h-c78d78n

HOLE13
*h-c78d78n

MB latch Hole

HOLE4
*H-TC138BC236D118P2

KB Screw Hole
EC-20090805A-2

HOLE21
*O-PS1-1

PROJECT : PS1 Quanta Computer Inc.		
Size B	Document Number <Doc> HOLES, PAD, NUT	Rev 1A
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EC-20090723A-1	P28	BIOS RECOMMAND	Pin Definition follow G-note setting
EC-20090724A-1	P18		Change audio codec circuit from ALC269 to CX20582.
EC-20090724A-2	P30	Power RECOMMAND	Update PC19, PL1, PQ2, PQ6, PQ7, PQ9 footprint
	P31		Update PL2 and PL3 footprint
	P33		Update PL5 footprint
	P34		Update PL6 footprint
EC-20090724A-3	P23		Add USB sleep charge schematic for BlackBerry
EC-20090724A-4	P18	EMI RECOMMAND	Reserve 0-ohm to separate AGND and GND
EC-20090726A-1	P27		Add Audio connector (wire to board)
	P27		Remove original U350 Power connector and Led connector (wire to board)
EC-20090726A-2	P27		Change Function connector from 30pin to 40pin (wire to board), because combine with Power and Led function
EC-20090726A-3	P2		Rename the CLK_MINI_OE# to CLK_WLAN_OE#
	P26		Rename the CLK_MINI_OE# to CLK_WLAN_OE#
EC-20090726A-4	P2		Add WWAN CLK(CLK_PCIE_WWAN) and WWAN CLKREQ#(CLK_WWAN_OE#)
	P14		Remove SATA signal
	P16		Add WWAN PCI-E signal
	P26		Mini-PCIE connector interface change from SATA-IF to WWAN-IF
EC-20090726A-5	P7		Connect VID and Enable pin between NB and MAX8796
	P9		Reserve Render standby power for NB
	P37		Connect VID and Enable pin between NB and MAX8796
EC-20090727A-1	P23		Add ESD protection at USB Port
	P26		Add ESD protection at SIM-Card
EC-20090727A-2	P25		Reserve 0ohm on SATA Pin-18 for Gen1 or Gen2
EC-20090728A-1	P23		Modify USB charge circuit, CB0 and CB1 pull high with 5VPCU
	P23		R445 and R447 change to stuff
EC-20090728A-2	P18		All AGND net-name change to GND, But keep original symbol
EC-20090728A-3	P38		Add NUT for SB Thermal module used
EC-20090729A-1	P23		Connect USB_ON# control pin, to enable USB Power switch
	P28		Connect USB_ON# control pin, to enable USB Power switch
EC-20090729A-2	P14		Change Y4 footprint for accurate component
EC-20090729A-3	P16	SW RECOMMAND	Swap USB port by SW suggestion
	P20		Swap CCD USB By SW suggestion
	P23		Swap Bluetooth USB By SW suggestion
	P26		Swap Mini-PCIE USB By SW suggestion
EC-20090729A-4	P18		Remove SPDIF Function
	P27		Remove SPDIF Function
EC-20090729A-5	P27		Swap Function-board connector pin definition
	P27		Swap Audio-connector pin definition
EC-20090729A-6	P18		Change C300 to 0.1u capacitor and Add R455 for discharge Path
EC-20090729A-7	ALL		Change the Short-pad to 0-ohm Resistor, 0402_SIZE : R99, R20, R27, R265, R58, R262, R260, R72, R101, R138, R3, R4, R281, R283, R274, R79, PR106, PR110, PR111, PR112, PR113, PR114, PR120, PR122, PR124 0603_SIZE : R45, R57, L61, L62, R193, R2, L2, L3, L38, L7, R210, R224, R222, R341 0805_SIZE : R13, R30, R158, R165, R430, R271, R60
EC-20090729A-8	P23		Reserve GSENSOR_Z signal so R376, C489, C490 no-stuff
EC-20090729A-9	P10		Change C192, C194, C213 value from 330U to 220U and add C581 Capacitor
			Change C78, C214 value from 10U to 22U
			Change R14 value from 1-ohm to 0.5-ohm
EC-20090729A-10	P9		For power rating concern, so change 0-ohm Resistor to Power-Jump
EC-20090729A-11	P27		Connect DCIN_LED# and LOGO_LED# between EC and Function-board connector
	P28		Connect DCIN_LED# and LOGO_LED# between EC and Function-board connector
EC-20090729A-12	P19		Remove RTL8103 circuit note (10/100M-Lan)
EC-20090729A-13	P18	ME RECOMMAND	Change INT_MIC connector footprint
EC-20090729A-14	P18		Add headphone sense circuit.
EC-20090729A-15	P18		Change R455 Symbol from Capacitor-type to Resistor-type
EC-20090729A-16	P30		Swap the DC_IN connector for layout routing
EC-20090729A-17	P27		Swap Audio-connector pin definition, follow daughter change

EC-20090730A-1	P23	Update Bluetooth Connector	Change Connector Type to follow latest ME placement.
EC-20090730A-2	P21	Update HDMI Connector	Change Connector Type to follow latest ME placement.
EC-20090730A-3	P15	Connect BT_DET#	Connect BT_DET# from BT conn. to GPIO48.
EC-20090730A-4	P27	Update Audio 8Pin singal	Update Audio wire to board cable pin definition.
EC-20090730A-5	P27	Delet +5V EMI filter	Due to delete SPDIF feature, no +5V needed on this conn.
EC-20090730A-6	P29	Update Bluetooth Connector	Change Connector Type to follow latest ME placement.
EC-20090730A-7	P37	Change Footprint	Change PC176/PC177 to small size to fit into placment.
EC-20090730A-8	P35	Add one thermistor	Add one more thermistor in Charger block.
EC-20090730A-9	P38	Add one more MB hole	For ME structure needed.
EC-20090730A-10	P38	Add Bluetooth modeule NUT	Add NUT for BT module support.
EC-20090730A-11	P18	Add EMI solution	Add LC filter for Bitclk.
EC-20090731A-1	P30	Swap DC in signal	Per Power input routing concern.
EC-20090730A-8	P35	Canel	Cancel this change on 0731, power remove one thermistor
EC-20090729A-2	P14	Canel	Cancel this change on 0731, Change back to small size of 32.768KHz Xtal.
EC-20090731A-2	P19	Update RJ45 connector	Change Connector Type to follow latest ME placement.
EC-20090731A-3	P23	Update USB connector	Change Connector Type to follow latest ME placement.
EC-20090731A-4	P19	Change 1M resistor size	Change 1M discharge resistor size from 0603 to 0805.
EC-20090801A-1	P18	Swap Speaker Pin definition	For Better cable routing.
EC-20090801A-2	P23	Correct GPIO pull high	Pull High EC GPIO in +3VS5 sequence to support S5 charge.
EC-20090801A-3	P23	Change G-sensor power	To meet G-sensor ripple SPEC, use LDO to generare +3V.
EC-20090801A-4	P23	Correct USB charger power	Change USB power to +5VS5 source to support S5 charge.
EC-20090801A-5	P35	Change 5VSUS supply MOS	Correct 5VSUS output rating.
EC-20090801A-6	P35	Change +3VS5 supply MOS	Correct +3VS5 output rating.
EC-20090801A-7	P34	Capacitor footprint change	Change PC121 and PC122 footprint from 7343-size to 3528-size
EC-20090801A-8	P23	Change USB net name	Change USBP13-_C and USBP13+_C net name to R_USB4- and R_USB4+
EC-20090802A-1	P27	EMI RECOMMAND	Reserve 0-ohm resistor for USB signal (USB1, USB6, USB8)
EC-20090802A-2	P26	EMI RECOMMAND	Reserve 0-ohm resistor for CN12 GCLK_SMB_1 and GDAT_SMB_1 signal
EC-20090803A-1	P24	ESD RECOMMAND	Reserve VARISTOR for Touch pad signal
EC-20090803A-2	P37	Power Tim RECOMMAND	Pull high voltage change from 5VPCU to +3V for HWPG signal
EC-20090803A-3	P07	Intel Design Guide	Follow Intel Design Guide, Option A solution --> GFX_VR_EN Pull down 100K
EC-20090803A-4	P19		Change Transformer IO_GND to GND
EC-20090804A-1	P18		Remove L61 and L62, short the AGND and GND directly
EC-20090804A-2	P37	Power engineer RECOMMAND	Render standby be modified by TIM
EC-20090804A-3	P22,25	ME RECOMMAND	CRT and SATA connector, change to correct footprint
EC-20090804A-4	P38		Add one Hole for M/B
EC-20090804A-5	P29	BIOS RECOMMAND	Add RFID EEPROM
EC-20090804A-6	P19		Modify LAN connector LED color
EC-20090804A-7	P27		Change one pin from GND to 5VSUS
EC-20090805A-1	P25	For layout space concern	Change SATA connector footprint to original U350 connector footprint
EC-20090805A-2	P38		Add one Hole for KB
EC-20090805A-3	P22		Stuff the Varistor for CRT
EC-20090806A-1	P23		Add EXT_GND for Thermal pad
EC-20090811A-1	P10	CRT ripple lesson learn	Change C165 from 0.1U to 4.7U for CRT ripple concern.

EC-20090813B-1	P37		Remove PR76 and PU5.Pin12 connect to AGND directly
EC-20090819B-1	P10		C165 : Change footprint from 0402_Size to 0603_Size
EC-20090824B-1	P31		Remove PR35 to solve 3VPCU short to Gnd issue
EC-20090824B-2	P37		Remove PR81 to solve no +VCC_CORE issue, because the VRON levle is divided by 1/10
EC-20090824B-3	P36		PR220 change from 43K to 20K to solve no +1.5V_S5
EC-20090825B-1	P30~P34 and P37		PJP5, PJP13, PJP14, PJP15, PJP16 are removed and short directly
			PJP1, PJP2, PJP3, PJP4, PJP6, PJP7, PJP10, PJP11, PJP12 are changed to 0-ohm short-pad
EC-20090825B-2	P24		Add CN22 for 10-PIN Touch-Pad
EC-20090825B-3	P30, P32, P33, P34, P37		PR15, PR123, PR127, PR135, PR137, PR141, PR143, PR148, PR110, PR114, PR51, PR52, PR178, PR179, PR197, PR198 are changed to 0-ohm short-pad (0402-size)
			PR78, PR189, PR205 are changed to 0-ohm short-pad (0603-size)
	P20		R7, R232 are changed to 0-ohm short-pad (0603-size)
	P19, P25		R137, R192, R61, R310 are changed to 0-ohm short-pad (0805-size)
EC-20090826B-1	P20	Power RECOMMAND	L43 is changed to F3 for pass IBM test
EC-20090826B-2	P20		Add schematic to control Logo-Led on/off
EC-20090826B-3	P22	ESD RECOMMAND	Add TVS (D27) for ESD protection
EC-20090826B-4	P26	RF RECOMMAND	Reserve C494~C498 for WWAN & WLAN
EC-20090827B-1	P33		Change PR75 pull-high voltage from +3V to 3VSUS to solve S3 resume issue
EC-20090827B-2	P36		PU8, PU9 : PIN4 connect to 5VPCU
EC-20090827B-3	P24		L6 is changed to F4 for pass IBM test
EC-20090828B-1	P23		USB charge U28 : modify resistor value and voltage state of PIN5 and PIN6
			Reserve R417 and R418 with PIN10 and PIN1
EC-20090828B-2	P9		PJP8 and PJP17 are changed to RC7520 footprint, that is for Render standby power

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EC-20091002C-1	P28	LOGO_LED# connect to U8.PIN25 not U8.PIN97, U8.PIN25 is PWM signal.
EC-20091002C-2	P3, P6	Change CPU and NB footprint. It is according to Lenovo request to enhance BGA rework performance, lower the F/R of solder mask or pad peel off from the reworking
EC-20091006C-3	P18	The Audio Jack is changed to Combo-type, and remove original HP_SENSE and MIC_SENSE circuit
EC-20091007C-1		R383, R386, R138, R44, R53, R303, R82, R299, R304, R98, R155, R23, R8, R9, R379, R380, R235, R236, R249, R250, R255, R256, R102, R314, R197, R198 are changed to short-pad (0402-size) R69, R83, L22, L23, L24, R12, R25, R228, R254 are changed to 0-ohm short-pad (0603-size) R40, R56, R168, R188, R189, R208 are changed to 0-ohm short-pad (0805-size)
EC-20091014C-1	P18	Follow Audio vendor suggestion, change 3V_DVDD to AVDD_3.3V for External MIC bias voltage
EC-20091014C-2	P38	By QSMC F6 PE suggestion, change BT Nut material so we need to modify footprint for new Nut use
EC-20091015C-1	P28	Remove R285 to reduce leakage current, by EC control to high or low
EC-20091015C-2	P35	Stuff PQ12 for normal discharge
EC-20091015C-3	P14	Change C448 and C449 from 15p to 18p for RTC timer
EC-20091015C-4	P24	Remove RP1 and RP2 to reduce leakage current, EC can provide internal pull-high
EC-20091015C-5	P20	Reserve C506 for CCD power, it is reference PS1A
EC-20091016C-1	P23	Add R428 and R429 for USB charge circuit, the vendor suggest it for new chip application
EC-20091016C-2	P23	R196 be change from 1K-ohm to 0-ohm
EC-20091016C-3	P14	Disable RTC charge function, remove R307, R308, R311, R312, Q22
EC-20091020C-1	P37	Disable Render Standby function, remove PU5, PL5, PQ23, PQ24 PC140, PC83, PC51, PC73, PC143, PC84, PC85, PC86, PC82, PC55, PC61, PC68, PC81, PC48, PC138, PC142 PR188, PR190, PR82, PR194, PR195, PR184, PR92, PR183, PR191, PR91, PR74, PR186, PR65, PR193, PR87, PR86, PR187, PR88, PR79, PR181
EC-20091020C-2	P24	Touch pad interface be changed from 13P(CN2) to 10P(CN22)
EC-20091020C-3	P31	Add PR164 to solve boot issue
EC-20091020C-4	P23	Remove R428 and R429, add R408, R409, R410 and R411 for USB charge circuit, the vendor suggest it for new chip application
EC-20091028C-1	P19	Adjust resistor value for Lan_LED light (R315 and R318 from 150 to 330)
	P20	Adjust resistor value for Logo_LED light (R414 from 510 to 1.8K)
EC-20091028C-2	P23	Change USB connector to yellow color
EC-20091028C-3	P35	Change PR68 from thermal-resistor to 0ohm due to remove render standby