LCFC Confidential

BMWC1&C2 M/B Schematics Document

NM-A471 REV:0.4

Intel Braswell M-Processor with DDRIIIL + NV (N16V-GM) GPU

2015-03-23

REV:0.4

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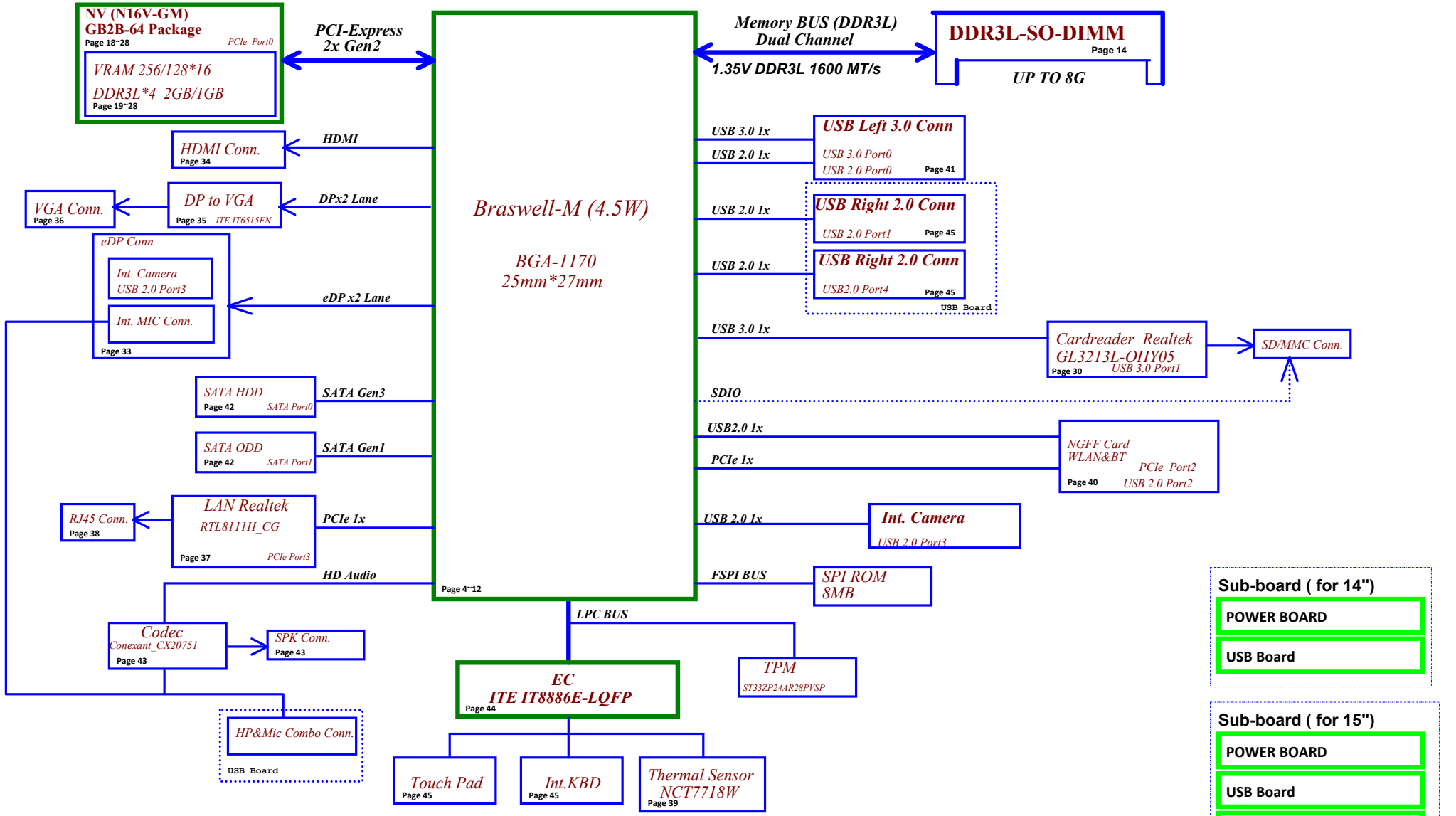

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ Power Plane	B+ +3VL	+3VALW +5VALW	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	EC +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB Port (Left Side)
	1	USB3.0 Card Reader
USB 2.0	0	USB Port (Left Side)
	1	USB Port (Right Side)
	2	BT
	3	Camera
	4	USB Port (Right Side)
USB HUB	1	
	2	
	3	
	4	

PCIE PORT LIST

Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

BOM Structure Table

BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	GPU Part
UMA@	UMA SKU ID part
14@	For 14" part
15@	For 15" part
100M@	100M LAN part
N15SGT@	N15SGT Part
N15VGM@	N15GSM Part
GIGA@	GIGA LAN Part
GC6@	GPU GC6 Part
TS@	Touch Screen part
RANKA@	GPU VRAM RANKA PART
RANKB@	GPU VRAM RANKB PART
ME@	Connector
CD@	COST DOWN
@	Not stuff
H4T@	Hynix VRAM Part
M4T@	Micron VRAM Part
S4T@@	Samsung VRAM Part

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

EC SM Bus1 address

Device	
Smart Battery	0001 011X b
Charger	need to update

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_100xb(reserve)
VGA	0x9E(base on NV default)

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
Wlan	Rsvd
TP	need to update

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Title: **Notes List**

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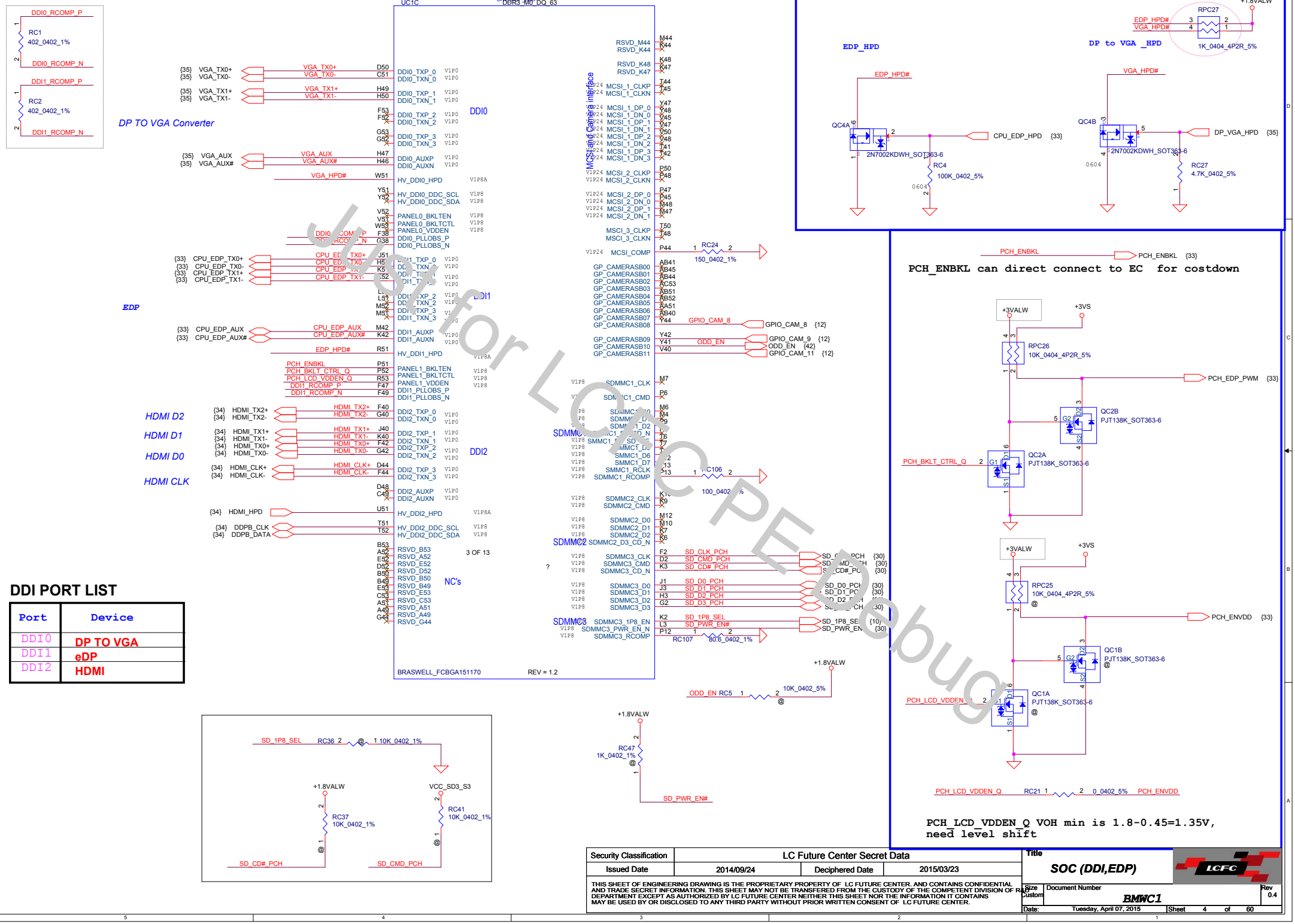

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

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DDRA_DQ[63:0] {14}
DDRA_MA[15:0] {14}
DDRA_DQS[7:0] {14}
DDRA_DQS#[7:0] {14}
DDRA_DM[7:0] {14}

UC1A — DDR0 — CHV_MC2_EDS — DDR3_M0_DQ_63 — 1 OF 13 — BRASWELL_FCBGA151170 REV = 1.2

UC1B — DDR1 — CHV_MC2_EDS — DDR3_M0_DQ_63 — 2 OF 13 — REV = 1.2

Group 6
Group 7
Group 5
Group 4
Group 3
Group 0
Group 2
Group 1

Del CS_2(chip select: 1 per Rank)
Del CKE_2(chip select: 1 per Rank)

M0_RCOMPPD — RC34 182_0402_1% — INTEL PDG 182 ohm — SD00001KG00
M1_RCOMPPD — RC35 — INTEL PDG 182 ohm — For dual rank

DDR_CORE_PWROK

VREF is not used for DDR3

+1.35V
RC6 4.7K_0402_1%
RC7 4.7K_0402_1%
DDRA_OCAVREF
CC130 .1U_0402_10V6-K
RC9 4.7K_0402_1%
RC10 4.7K_0402_1%
DDRA_ODQVREF
CC131 .1U_0402_10V6-K

+3VALW
+1.35V
RPC13 10K_0404_4P2R_5%
DDR_PWROK
QC5B 2N7002KDWH_SOT363-6
QC5A 2N7002KDWH_SOT363-6
{55} VDDQ_PGOOD
CC1 .1U_0402_10V6-K
CC3 .1U_0402_10V6-K
EMC@

+3VALW
+1.35V
RPC14 10K_0404_4P2R_5%
DDR_CORE_PWROK
QC10B 2N7002KDWH_SOT363-6
QC10A 2N7002KDWH_SOT363-6
{7,44} SYS_PWROK
CC18 .1U_0402_10V6-K
CC19 .1U_0402_10V6-K
CD@

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Title: SOC (DDI,EDP)

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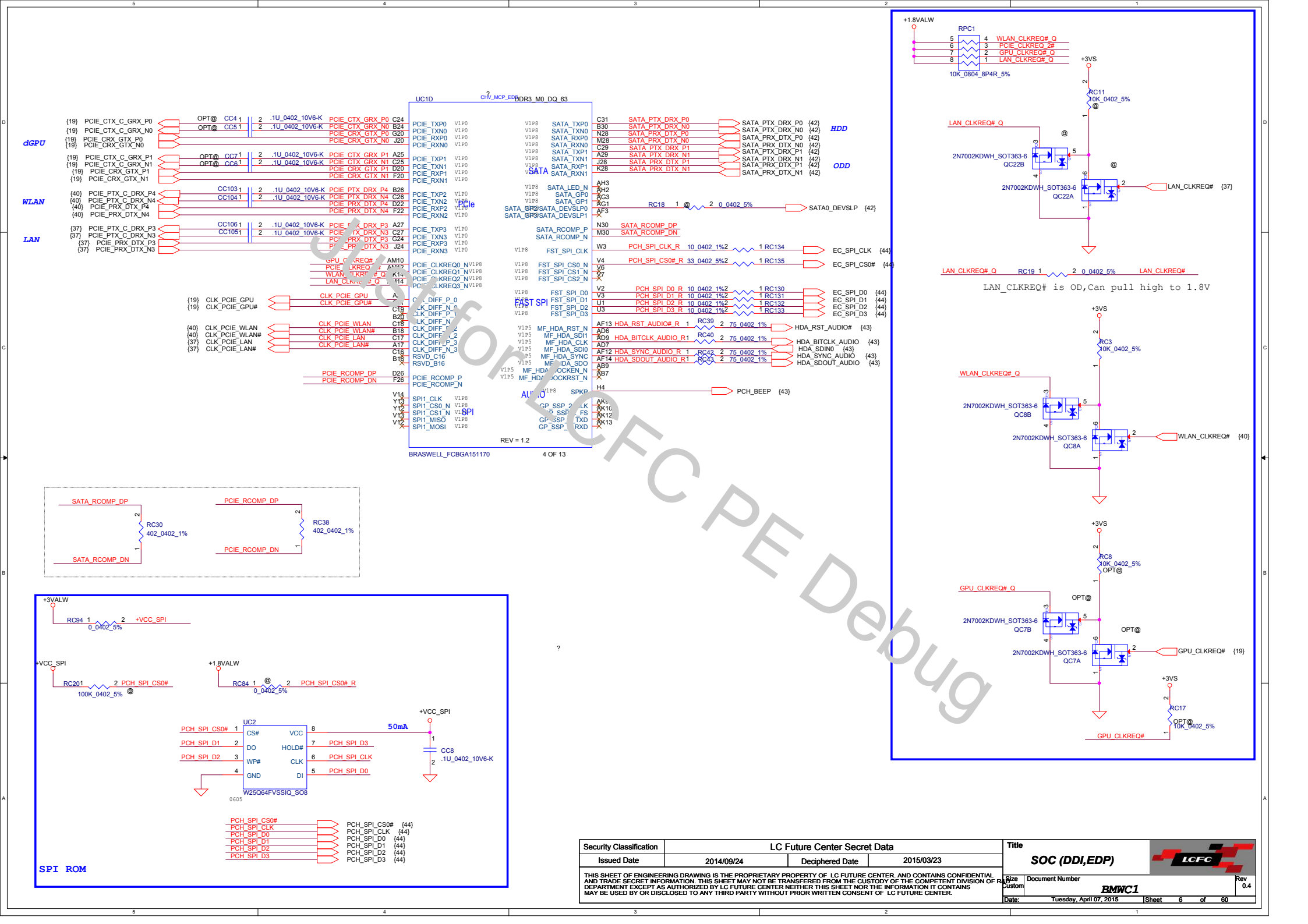

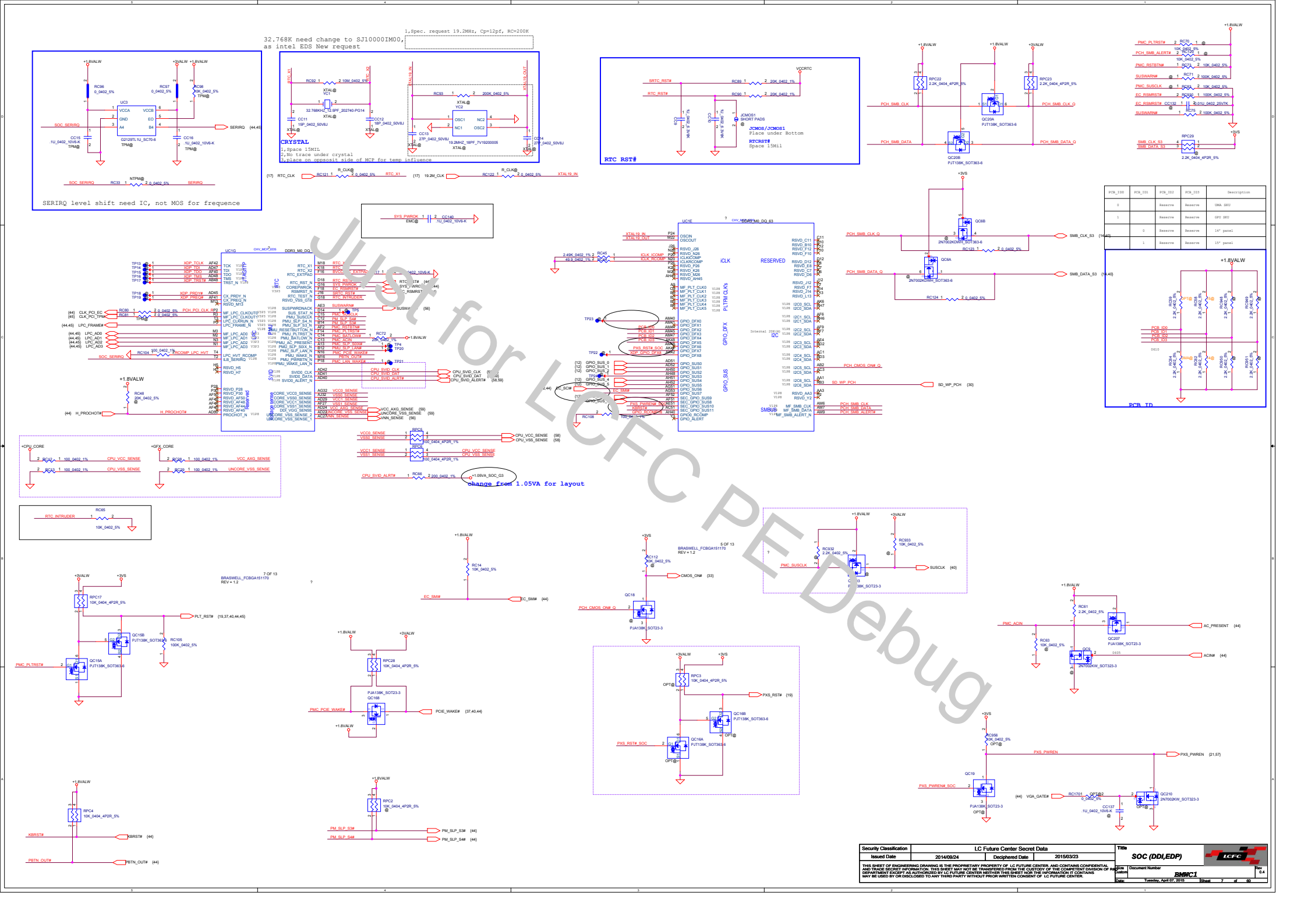
32.768K need change to SJ10000IM00,
as intel EDS New request
1,Spec. request 19.2MHz, Cp=12pf, RC=200K
SERIRQ level shift need IC, not MOS for frequence
CRYSTAL
1,Space 15MIL
2,No trace under crystal
3,place on opposit side of MCP for temp influence
RTC RST#
JCMOS/JCMOS1
Place under Bottom
RTCRST#
Space 15Mil
change from 1.05VA for layout
Just for LCFC PE Debug
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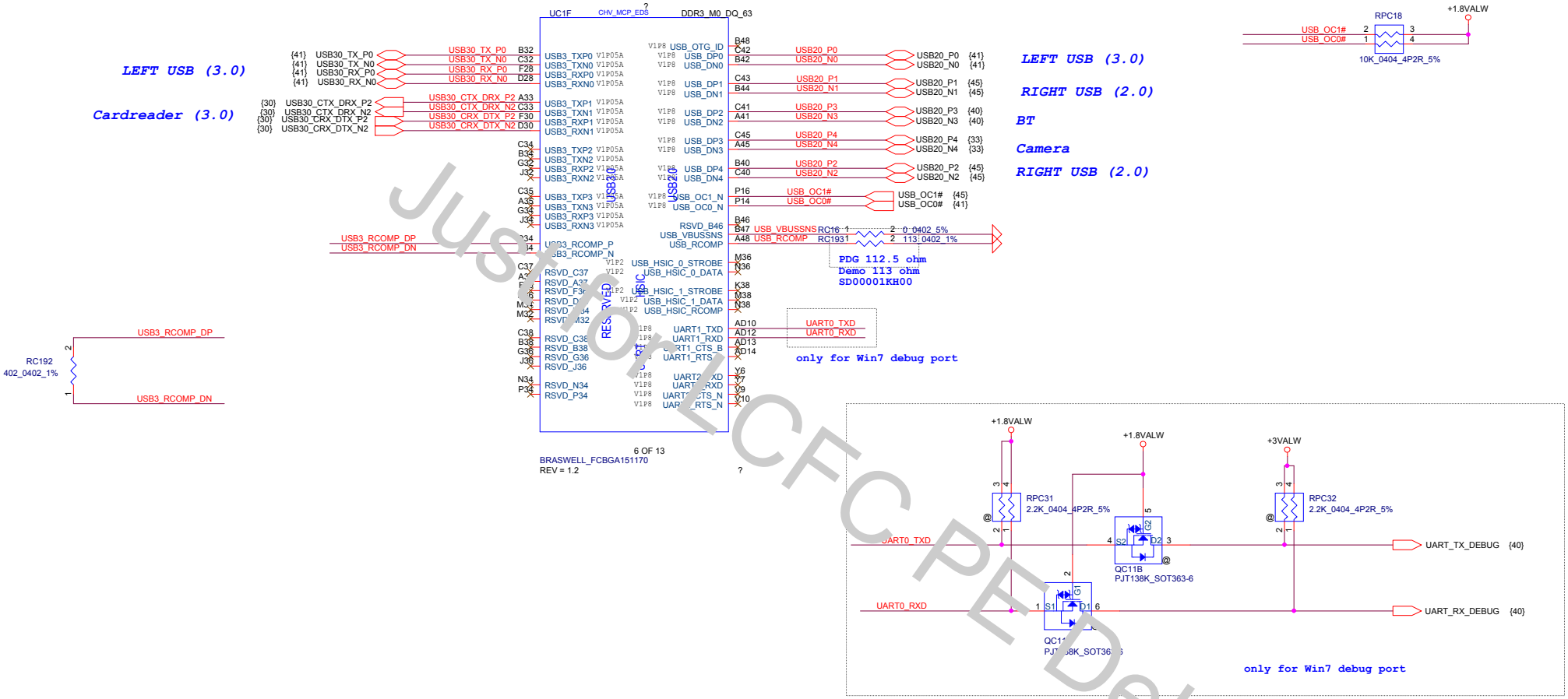

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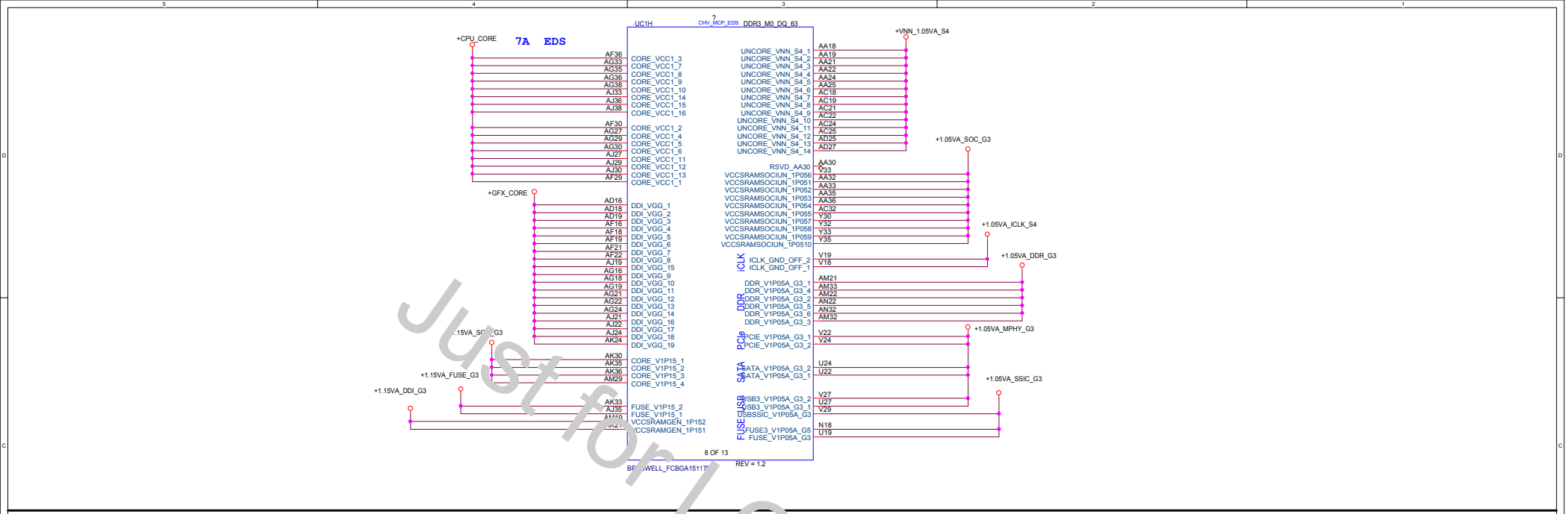

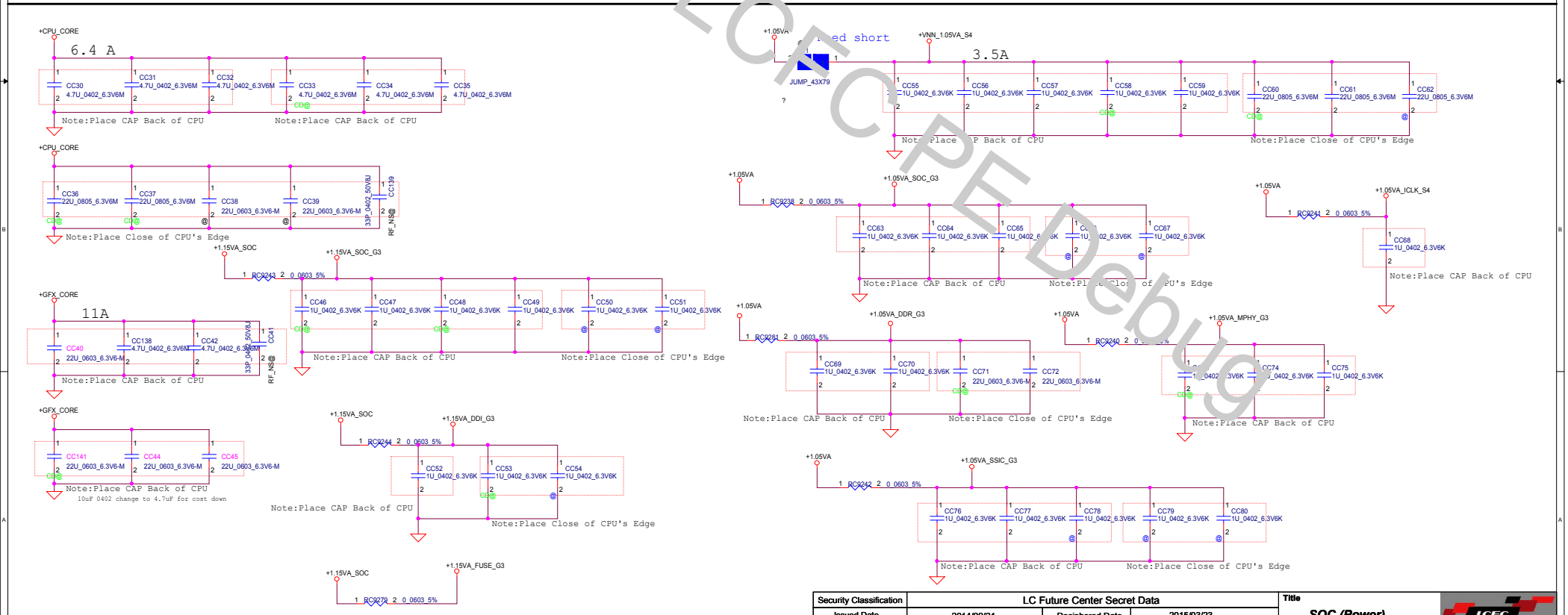

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Title: **SOC (Power)**

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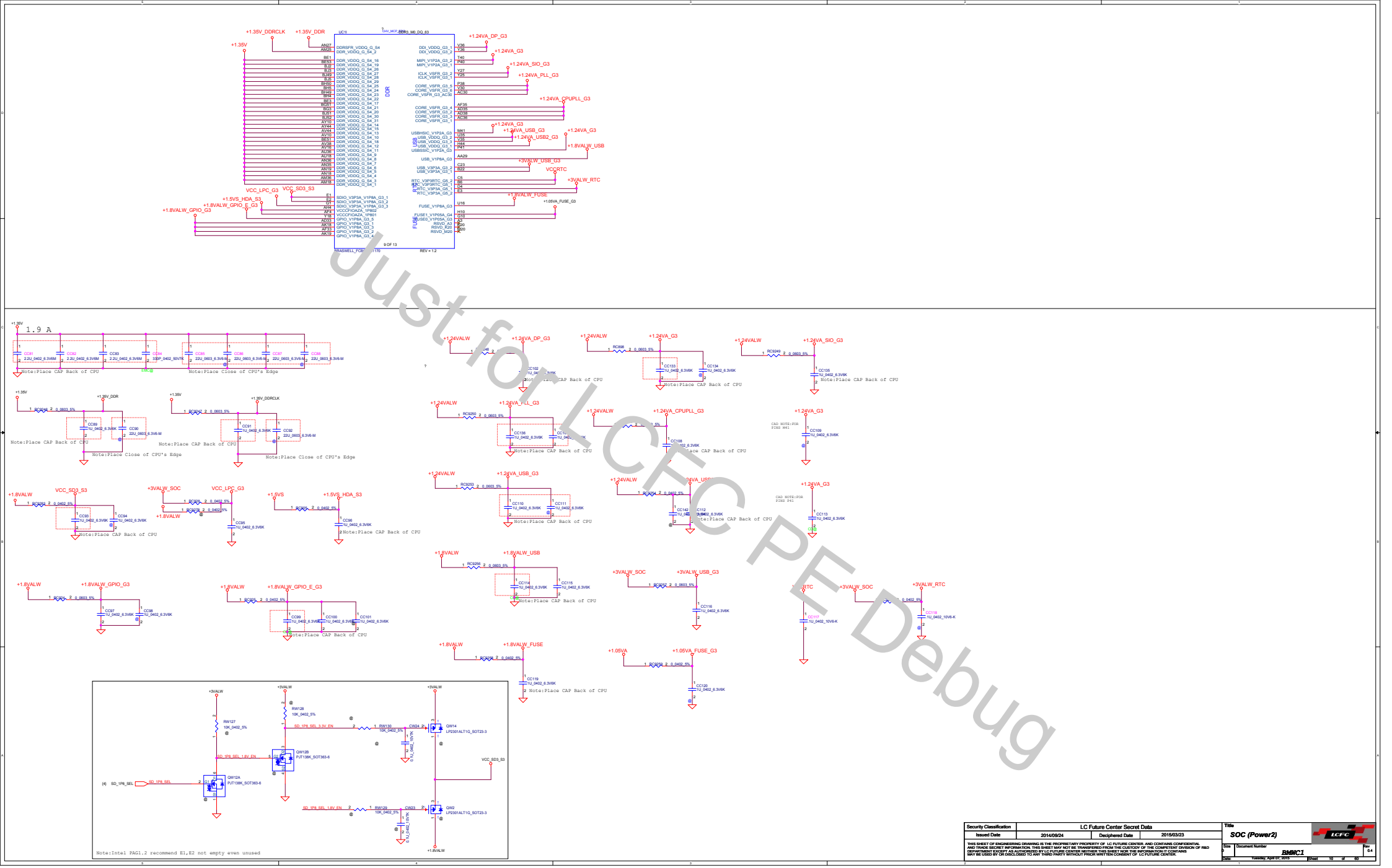

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Title: SOC (Power2)

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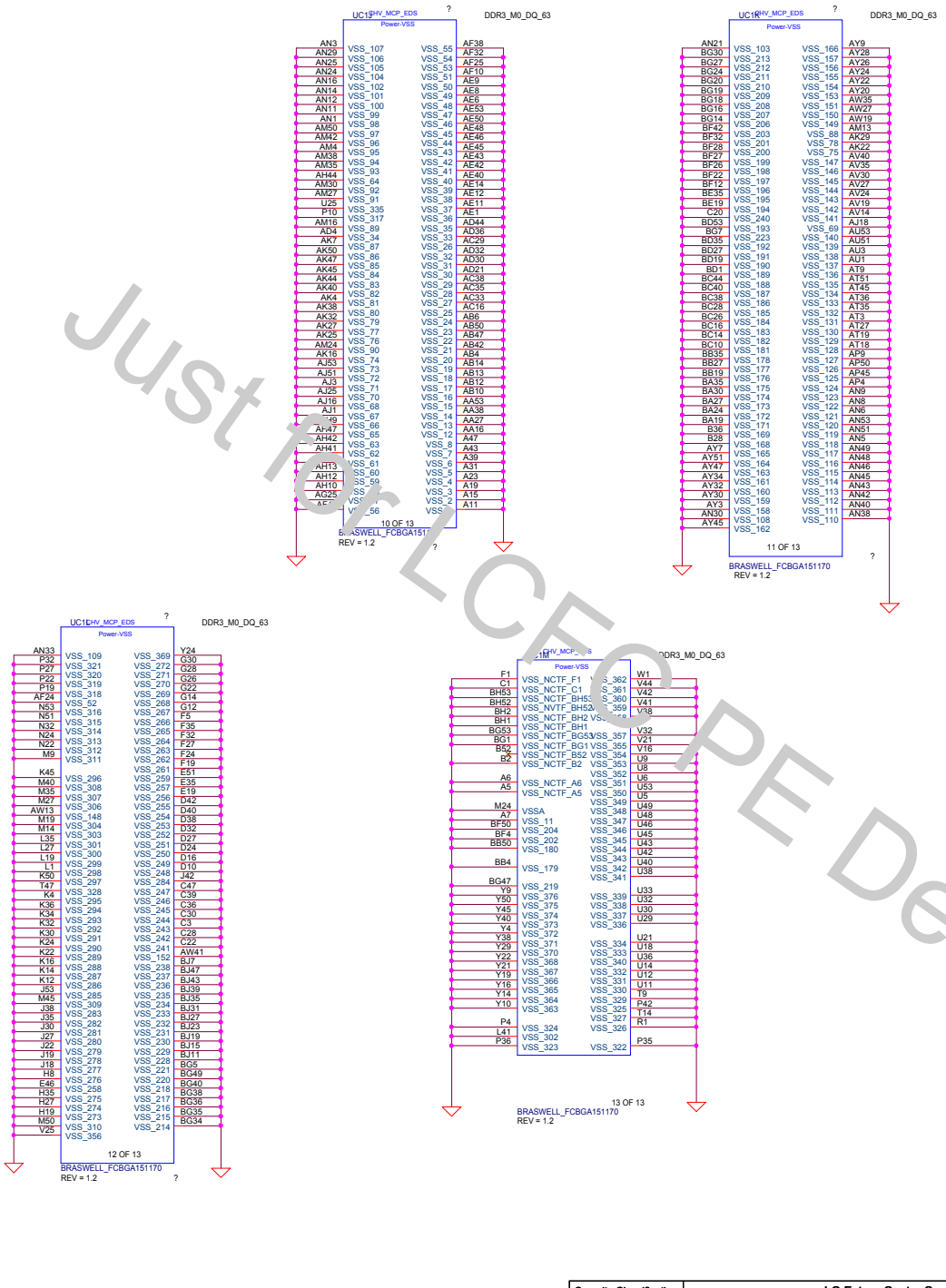

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Title: **SOC (VSS)**

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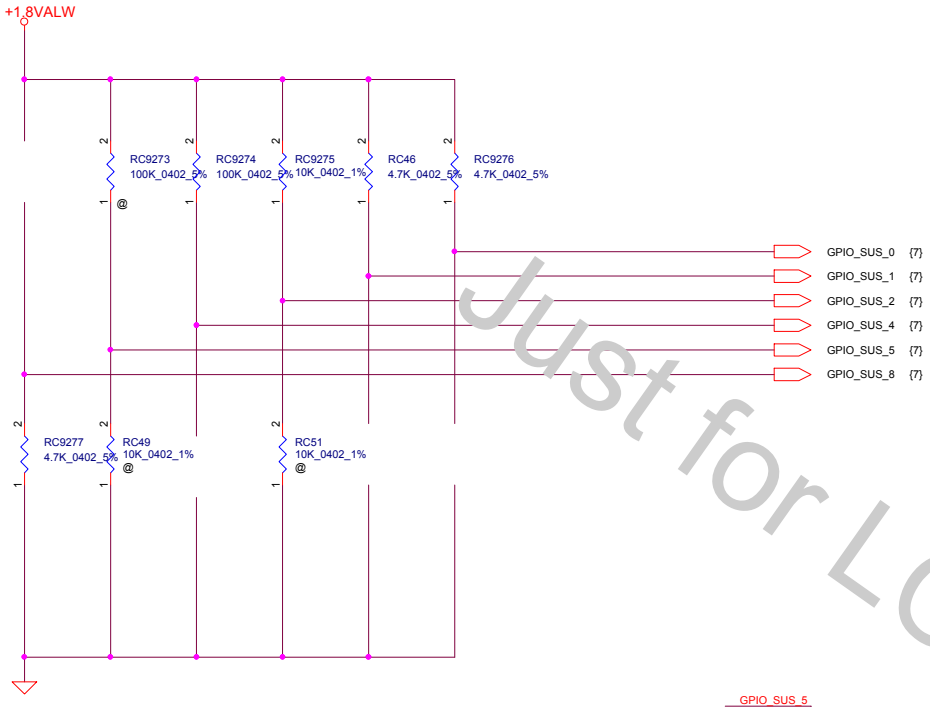
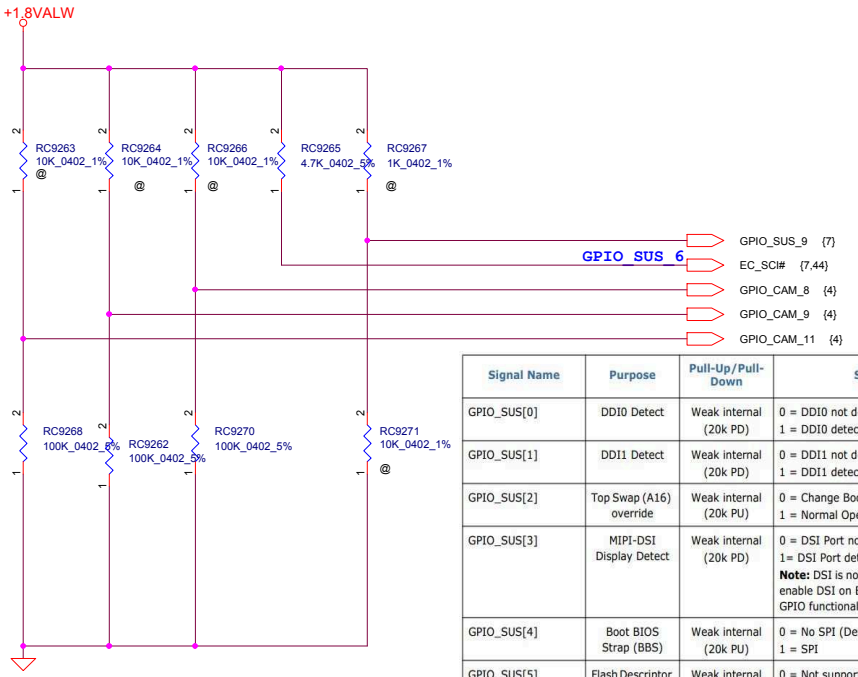
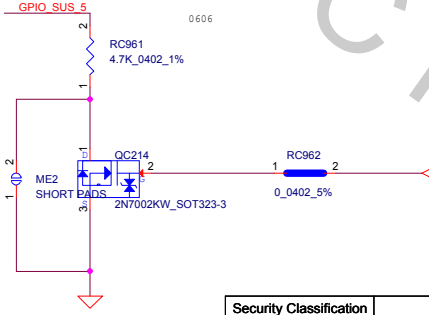
Hardware STRAPS (Follow up CRB)







Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1= DSI Port detected **Note:** DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1= Normal Operation **Note:** This strap **MUST** be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

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Title

MCP (OTHER)

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DDR3 SO-DIMM A

DDR Mapping table

DDRA_DQ6---DQ0
DDRA_DQ1---DQ1
DDRA_DQ4---DQ2
DDRA_DQ2---DQ3
DDRA_DQ3---DQ4
DDRA_DQ0---DQ5
DDRA_DQ7---DQ6
DDRA_DQ5---DQ7

DDRA_DQ9----DQ8
DDRA_DQ12---DQ9
DDRA_DQ11---DQ10
DDRA_DQ14---DQ11
DDRA_DQ8----DQ12
DDRA_DQ13---DQ13
DDRA_DQ15---DQ14
DDRA_DQ10---DQ15

DDRA_DQ20---DQ16
DDRA_DQ16---DQ17
DDRA_DQ17---DQ18
DDRA_DQ23---DQ19
DDRA_DQ19---DQ20
DDRA_DQ21---DQ21
DDRA_DQ22---DQ22
DDRA_DQ18---DQ23

DDRA_DQ28---DQ24
DDRA_DQ25---DQ25
DDRA_DQ29---DQ26
DDRA_DQ24---DQ27
DDRA_DQ27---DQ28
DDRA_DQ30---DQ29
DDRA_DQ26---DQ30
DDRA_DQ31---DQ31

DDRA_DQ32---DQ32
DDRA_DQ33---DQ33
DDRA_DQ39---DQ34
DDRA_DQ34---DQ35
DDRA_DQ37---DQ36
DDRA_DQ38---DQ38
DDRA_DQ35---DQ39

DDRA_DQ40---DQ40
DDRA_DQ45---DQ41
DDRA_DQ42---DQ42
DDRA_DQ43---DQ43
DDRA_DQ44---DQ44
DDRA_DQ41---DQ45
DDRA_DQ47---DQ46
DDRA_DQ46---DQ47

DDRA_DQ48---DQ48
DDRA_DQ51---DQ49
DDRA_DQ53---DQ50
DDRA_DQ49---DQ51
DDRA_DQ55---DQ52
DDRA_DQ50---DQ53
DDRA_DQ52---DQ54
DDRA_DQ54---DQ55

DDRA_DQ60---DQ56
DDRA_DQ61---DQ57
DDRA_DQ63---DQ58
DDRA_DQ62---DQ59
DDRA_DQ56---DQ60
DDRA_DQ57---DQ61
DDRA_DQ58---DQ62
DDRA_DQ59---DQ63

3A@1.5V

For RF request

Layout Note:
Place near DIMM

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

cost down bom to change 0.1uF

For RF request

0.65A@0.75V

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Title: DDRIII SO-DIMM A

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Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDRB_DQ17
7	DQ1	DDRB_DQ23
15	DQ2	DDRB_DQ18
17	DQ3	DDRB_DQ21
4	DQ4	DDRB_DQ16
6	DQ5	DDRB_DQ22
16	DQ6	DDRB_DQ19
18	DQ7	DDRB_DQ20
10	DQS#0	DDRB_DQS#2
12	DQS0	DDRB_DQS2
21	DQ8	DDRB_DQ3
23	DQ9	DDRB_DQ5
33	DQ10	DDRB_DQ6
35	DQ11	DDRB_DQ1
22	DQ12	DDRB_DQ2
24	DQ13	DDRB_DQ4
34	DQ14	DDRB_DQ0
36	DQ15	DDRB_DQ7
27	DQS#1	DDRB_DQS#0
29	DQS1	DDRB_DQS0
39	DQ16	DDRB_DQ8
41	DQ17	DDRB_DQ10
51	DQ18	DDRB_DQ14
53	DQ19	DDRB_DQ15
40	DQ20	DDRB_DQ13
42	DQ21	DDRB_DQ12
50	DQ22	DDRB_DQ9
52	DQ23	DDRB_DQ11
45	DQS#2	DDRB_DQS#1
47	DQS2	DDRB_DQS1
57	DQ24	DDRB_DQ27
59	DQ25	DDRB_DQ26
67	DQ26	DDRB_DQ28
69	DQ27	DDRB_DQ24
56	DQ28	DDRB_DQ31
58	DQ29	DDRB_DQ30
68	DQ30	DDRB_DQ29
70	DQ31	DDRB_DQ25
62	DQS#3	DDRB_DQS#3
64	DQS3	DDRB_DQS3
129	DQ32	DDRB_DQ33
131	DQ33	DDRB_DQ36
141	DQ34	DDRB_DQ39
143	DQ35	DDRB_DQ38
130	DQ36	DDRB_DQ37
132	DQ37	DDRB_DQ32
140	DQ38	DDRB_DQ35
142	DQ39	DDRB_DQ34
135	DQS#4	DDRB_DQS#4
137	DQS4	DDRB_DQS4
147	DQ40	DDRB_DQ40
149	DQ41	DDRB_DQ43
157	DQ42	DDRB_DQ42
159	DQ43	DDRB_DQ44
146	DQ44	DDRB_DQ45
148	DQ45	DDRB_DQ41
158	DQ46	DDRB_DQ46
160	DQ47	DDRB_DQ47
152	DQS#5	DDRB_DQS#5
154	DQS5	DDRB_DQS5
163	DQ48	DDRB_DQ52
165	DQ49	DDRB_DQ51
175	DQ50	DDRB_DQ50
177	DQ51	DDRB_DQ48
164	DQ52	DDRB_DQ49
166	DQ53	DDRB_DQ53
174	DQ54	DDRB_DQ54
176	DQ55	DDRB_DQ55
169	DQS#6	DDRB_DQS#6
171	DQS6	DDRB_DQS6
181	DQ56	DDRB_DQ62
183	DQ57	DDRB_DQ57
191	DQ58	DDRB_DQ59
193	DQ59	DDRB_DQ63
180	DQ60	DDRB_DQ56
182	DQ61	DDRB_DQ61
192	DQ62	DDRB_DQ58
194	DQ63	DDRB_DQ60
186	DQS#7	DDRB_DQS#7
188	DQS7	DDRB_DQS7

0.65A@0.75V

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Title: DDRIII SO-DIMM B

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Title: **USB Hub GL850G-OHY31**

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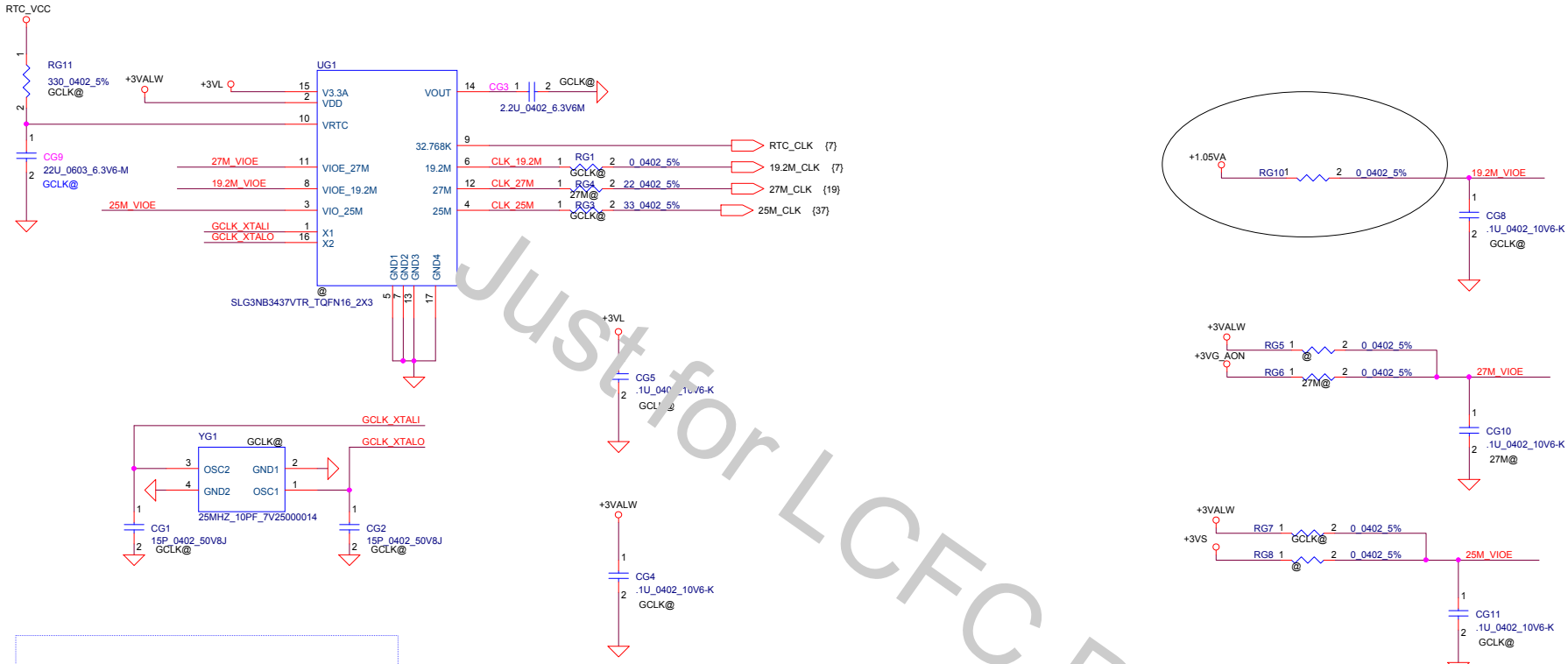
3437:SA000078V00;3436:SA000078X00



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Title: **Blank**

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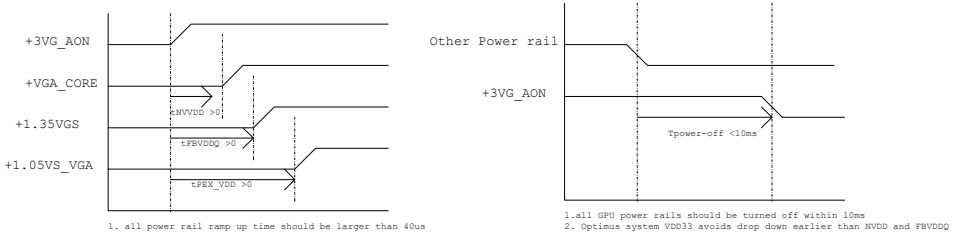
N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (1.8V Pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

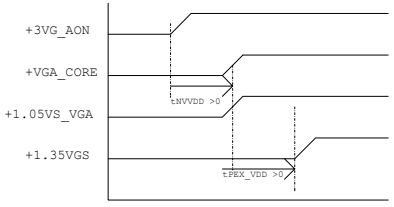
N15V-GM Power Sequence



1. all power rail ramp up time should be larger than 40us

1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence



1. all power rail ramp up time should be larger than 40us

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD		TBD	TBD	TBD	TBD

N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x4C (Multi-GPU usage)

N15x Binary Straps

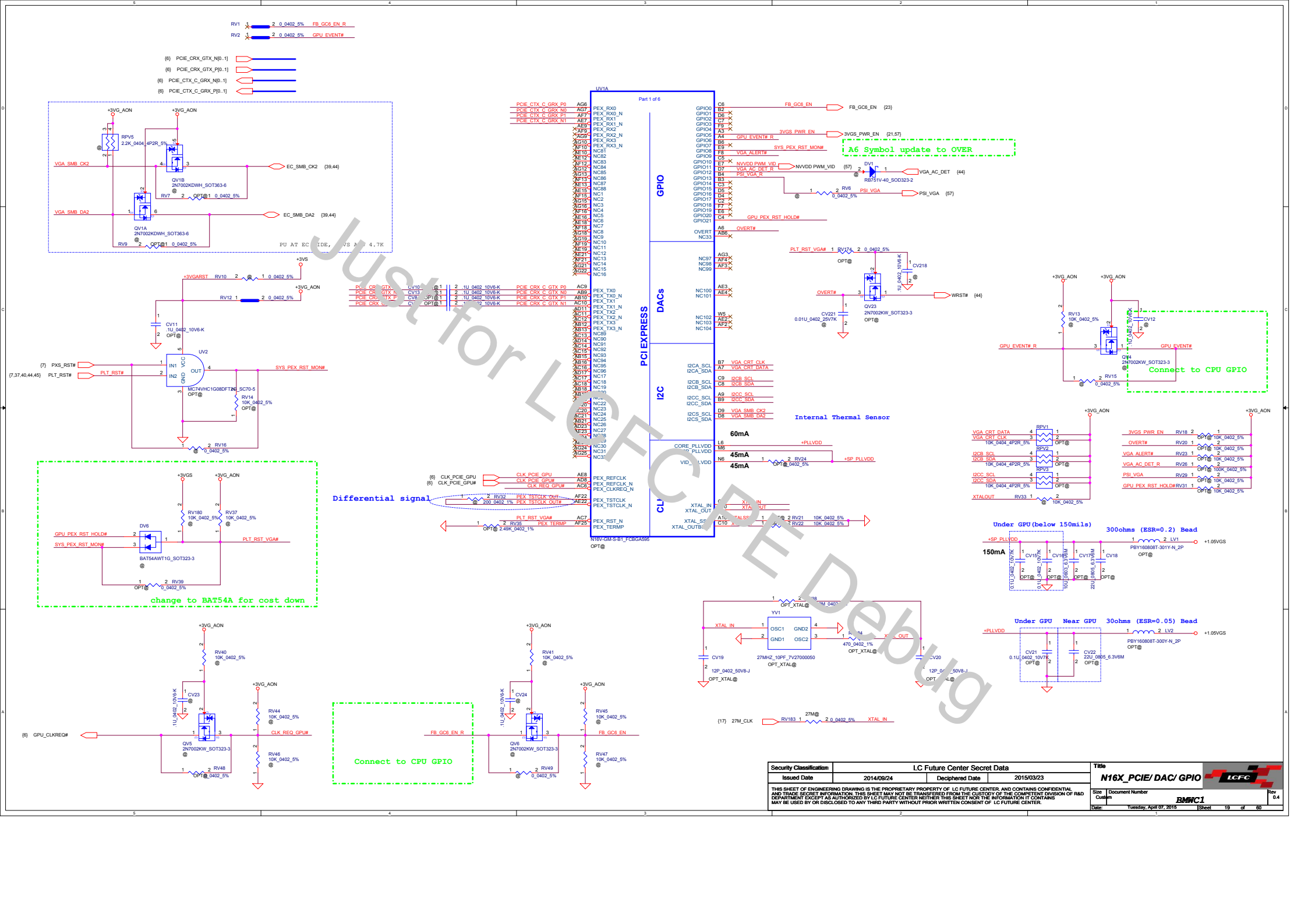
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: VGA Notes List

Size	Document Number	Rev
C	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 18 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

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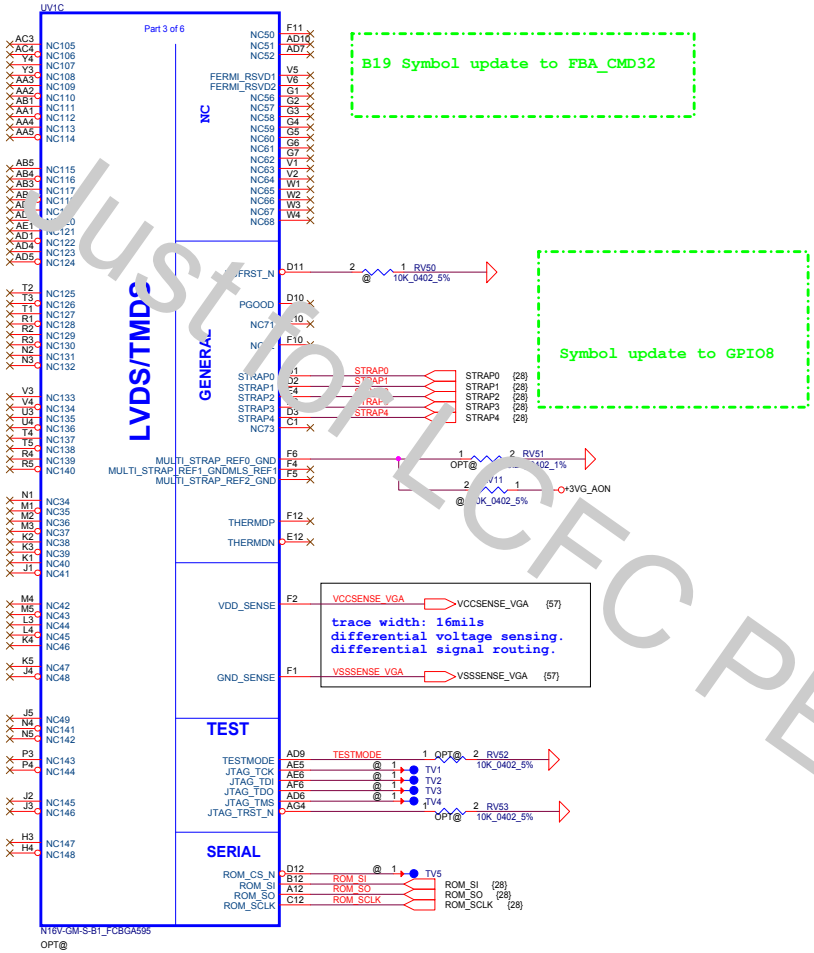
Title: N16X_PCIE/ DAC/ GPIO

Size: Custom | Document Number: BMWC1 | Rev: 0.4

Date: Tuesday, April 07, 2015 | Sheet 19 of 60

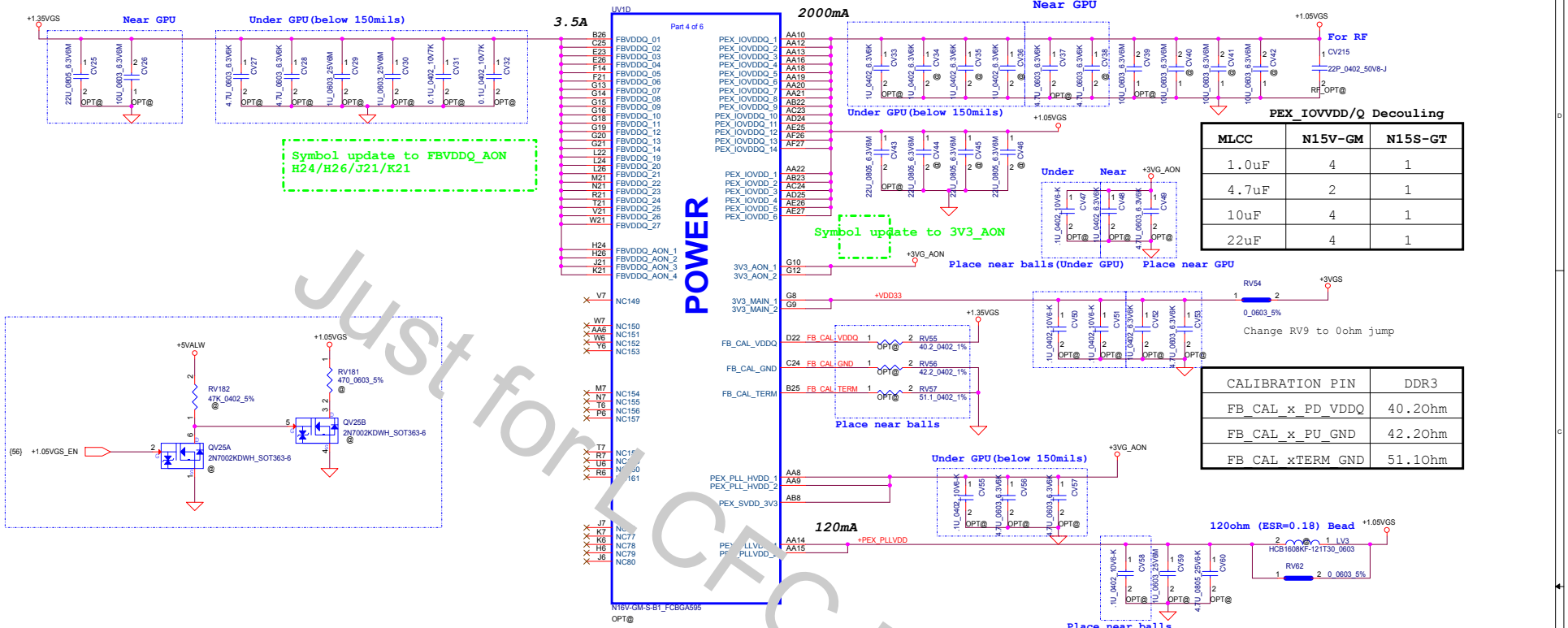


Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: *N16X_LVDS/ HDMI/ THERM*

Size	Document Number	Rev
C	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 20 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

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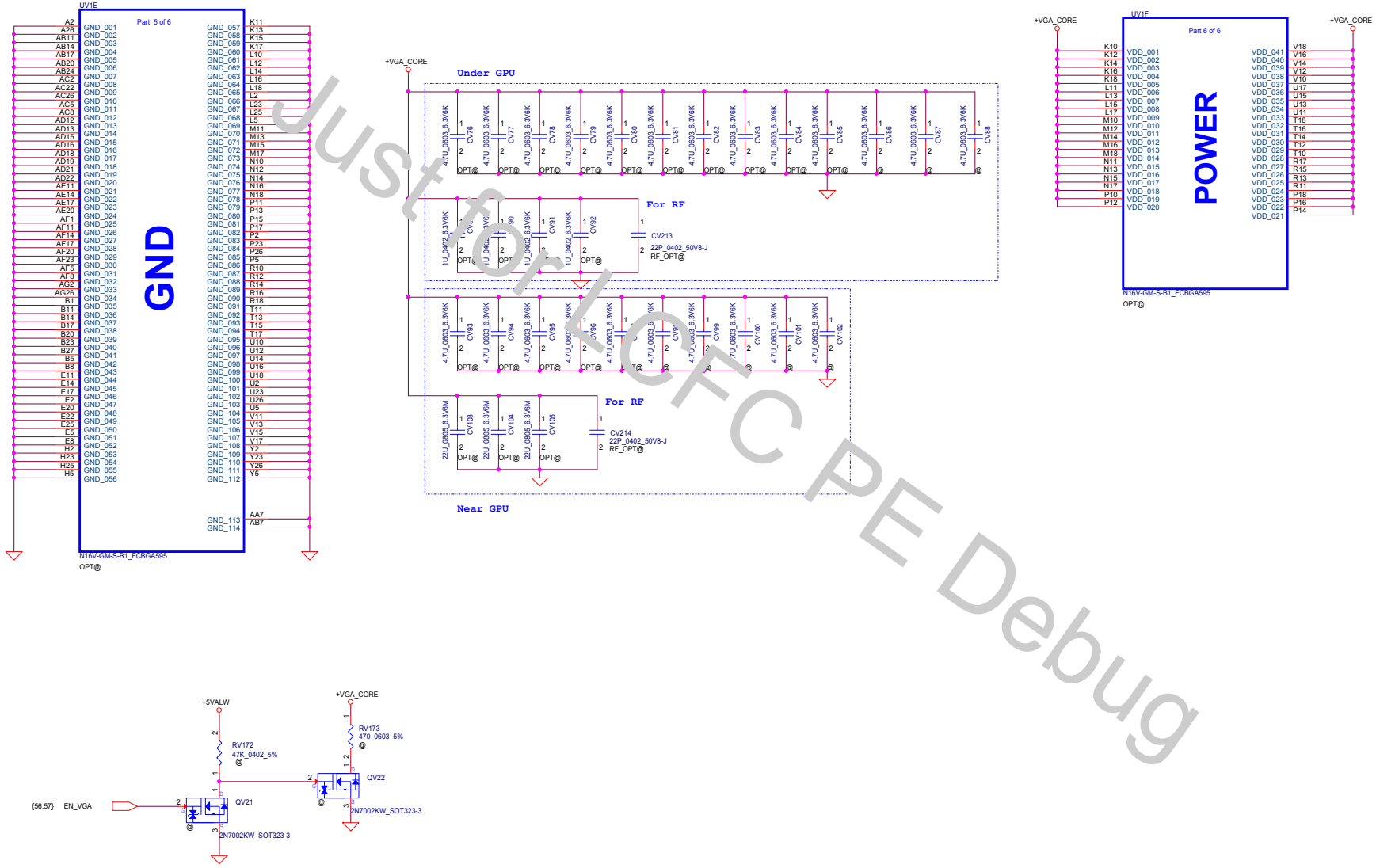
Title: N16X_Power

Size: C | Document Number: BMWC1 | Rev: 0.4

Date: Tuesday, April 07, 2015 | Sheet 21 of 60

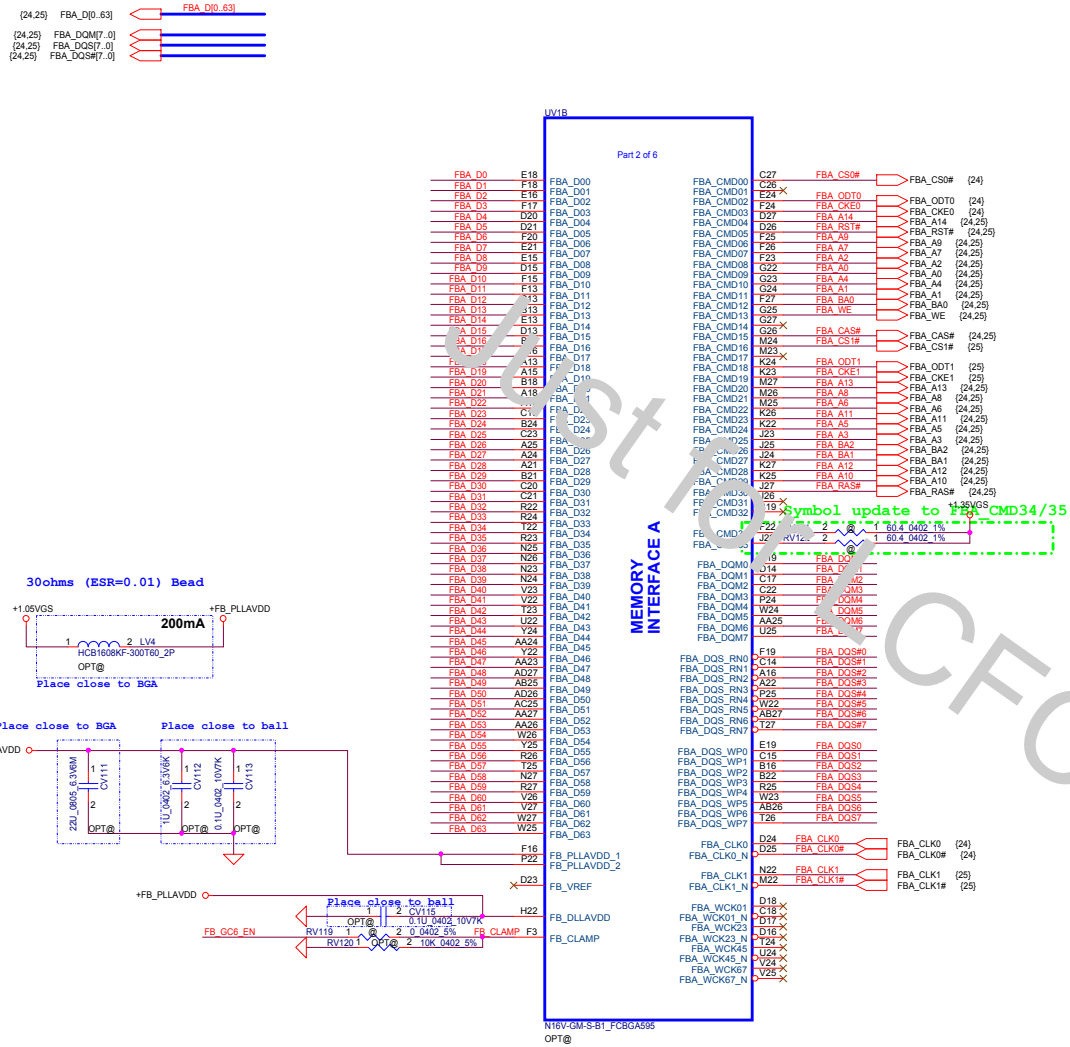


Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: *N16X_+VGA CORE, GND*

Size	Document Number	Rev
C	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 22 of 60



CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			

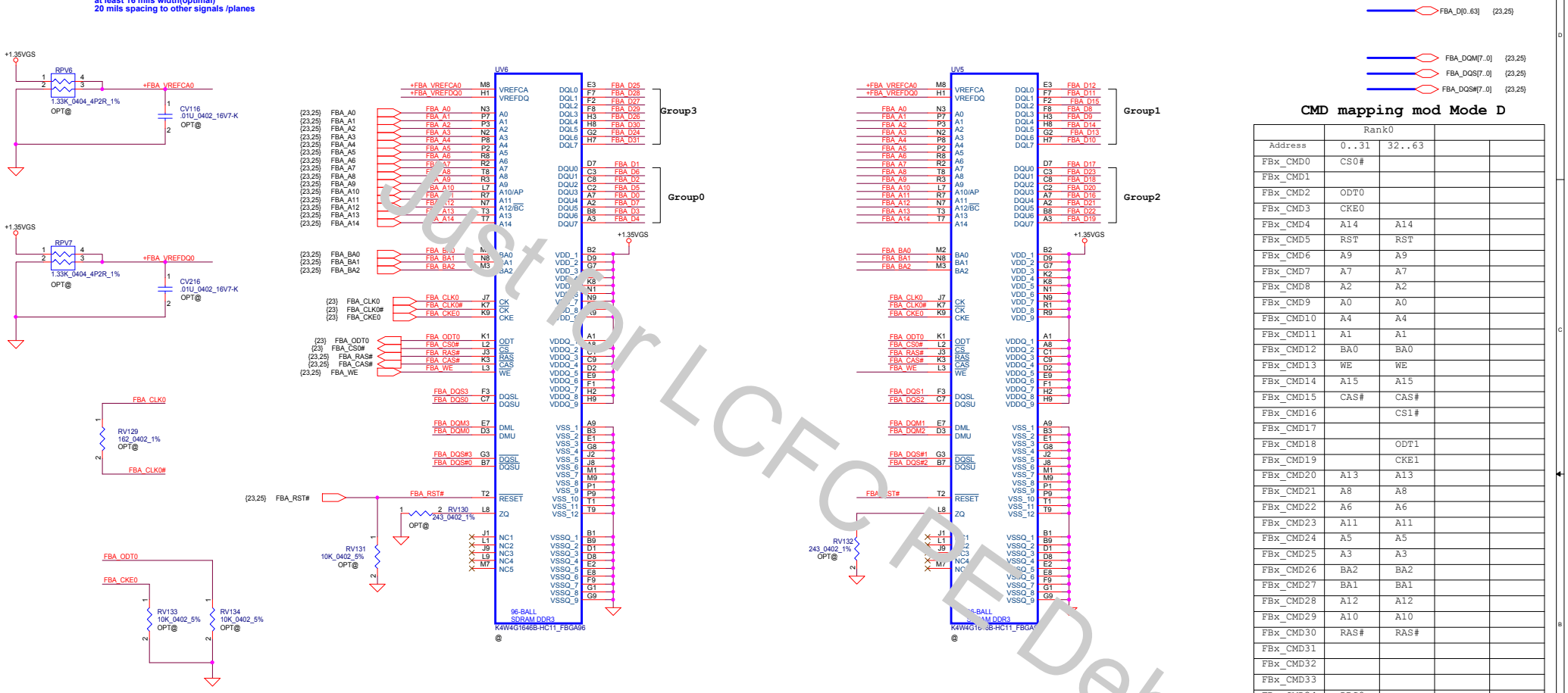
Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: N16X_MEM Interface

Size	Document Number	Rev
C	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 23 of 60

at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			

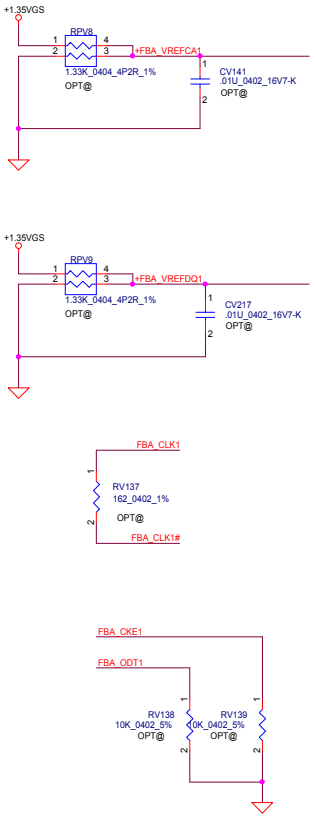
Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

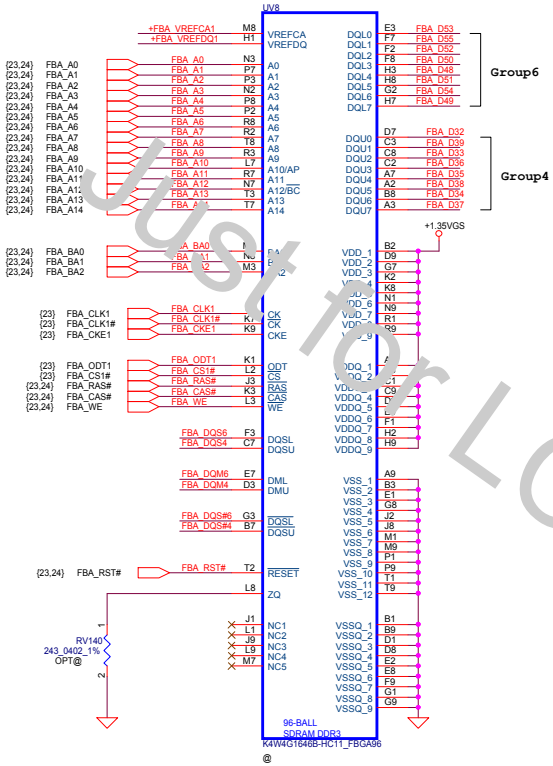
Title: DDR3 VRAM Rank0_L

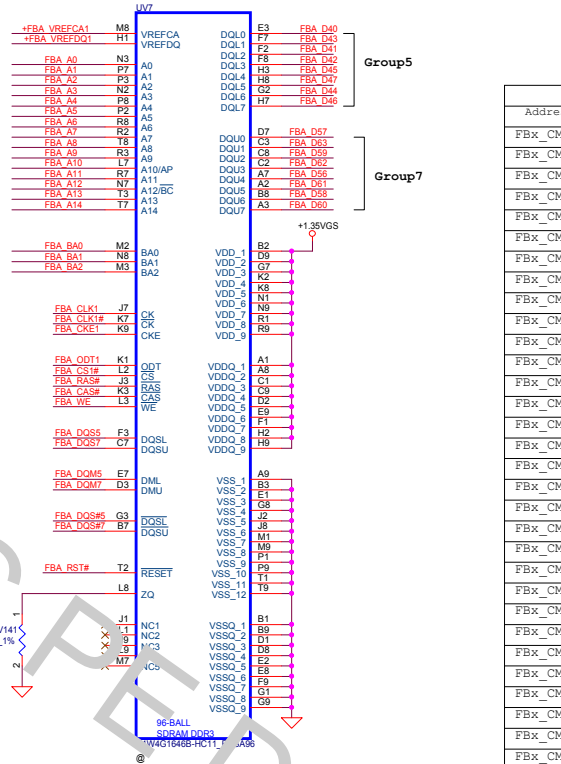
Size	Document Number	Rev
C	BMWC1	0.4

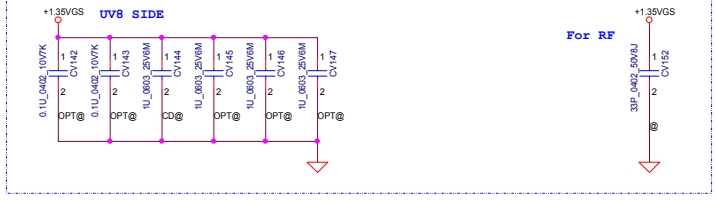
Date: Tuesday, April 07, 2015 Sheet 24 of 60

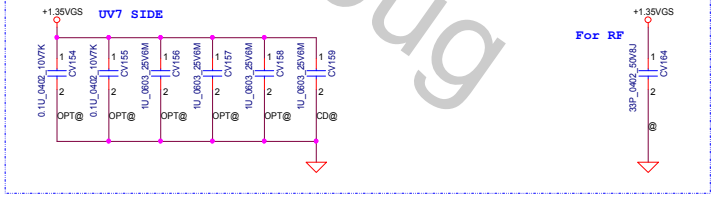
at least 16 mils width(optimal)
20 mils spacing to other signals /planes











FBA_D[0..63] {23,24}

FBA_DQM[7..0] {23,24}

FBA_DQS[7..0] {23,24}

FBA_DQS#[7..0] {23,24}

CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: DDR3 VRAM Rank0_H

Size	Document Number	Rev
C	BMWC1	0.4

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Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: ***DDR3 VRAM Rank1_L***

Size	Document Number	Rev
C	***BMWC1***	0.4

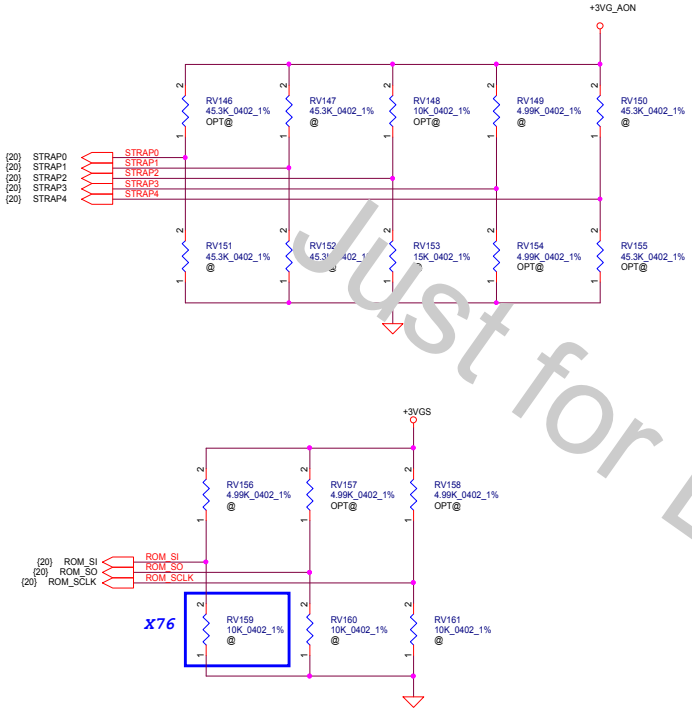
Date: Tuesday, April 07, 2015 Sheet 26 of 60

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: ***DDR3 VRAM Rank1_H***

Size	Document Number	Rev
C	***BMWC1***	0.4

Date: Tuesday, April 07, 2015 Sheet 27 of 60



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K SD03449918J	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K SD03424928J	1100	0100
30.1K SD03430128J	1101	0101
34.8K SD03434828J	1110	0110
45.3K SD03453328J	1111	0111

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (DDR3L)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16V-GM	Hynix 900MHz	H5TC4G63AFR-11C 256M x 16 0xE	0xE PU 34.8K	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K
	Micron 900MHz	MT41J256M16HA-093G:E 256M x 16 0xD	0xD PU 30.1K							
	Hynix 900MHz	H5TC2G63FFR-11C 128M x 16 0xB	0xB PU 20K							
	Micron 900MHz	MT41J128M16JT-093G 128M x 16 0x8	0x8 PU 4.99K							
	Samsung 900MHz	K4W2G1646Q-BC1A 128M x 16 0x7	0x7 PD 45.3K							

VRAM	X76	VRAM P/N
Samsung	X7606012101	SA00005SH40
Micron	X7606012001	SA00005M120
Hynix	X7606012002	SA00005VS00

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: N16X_MISC

Size	Document Number	Rev
C	BMWC1	0.4

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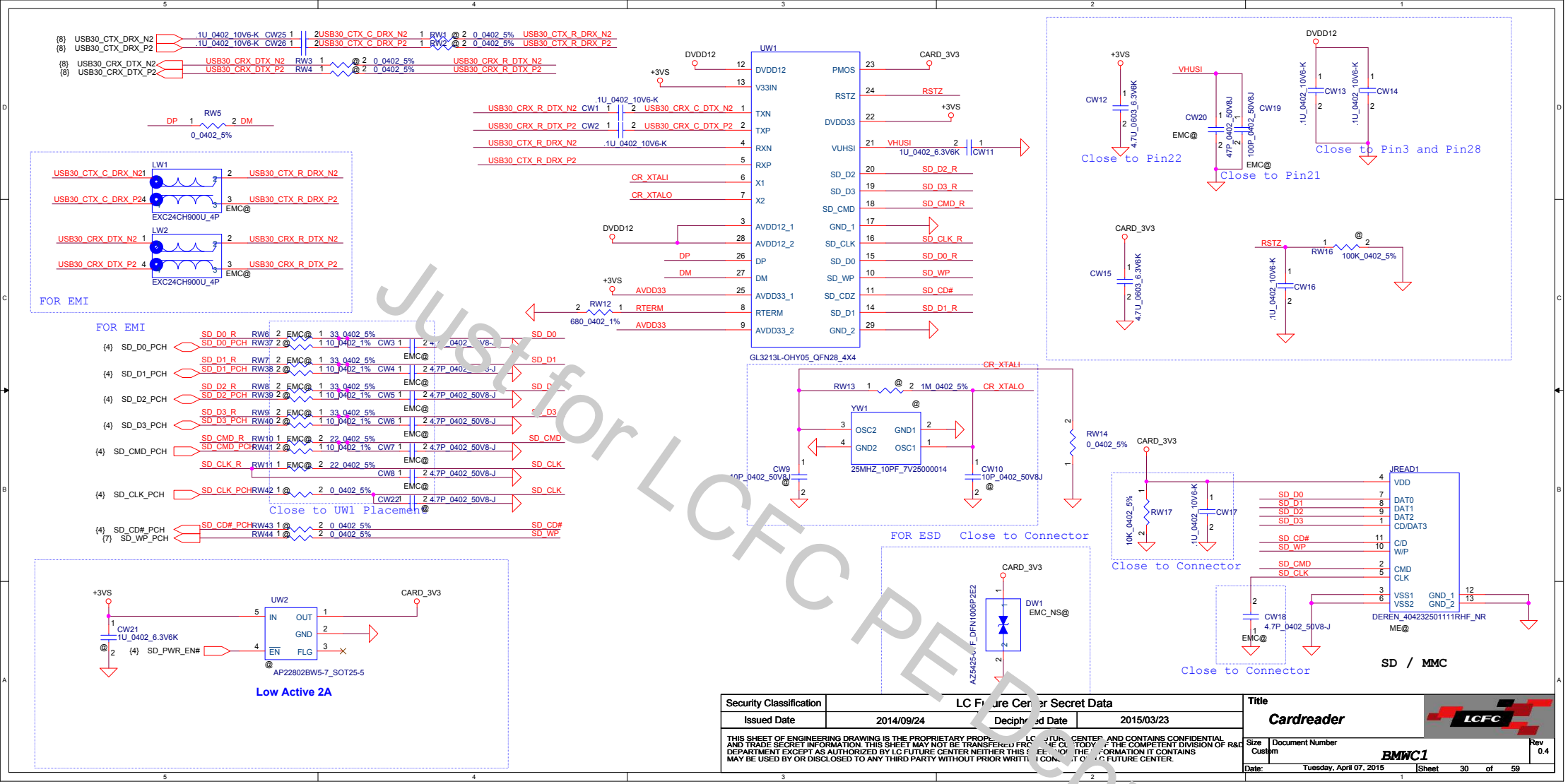
Security Classification	LC Future Center Secret Da		
Issued Date	2014/09/24	Deciphered Date	2015/0 23

Title: ***Blank***

Size	Document Number	Rev
Custom	***BMWC1***	0.4

Date: Tuesday, April 07, 2015 Sheet 29 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: **Cardreader**

Size	Document Number	Rev
Custom	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 30 of 59

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title

Blank

Size	Document Number	Rev
Custom	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 31 of 59

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: ***Blank***

Size	Document Number	Rev
Custom	***BMWC1***	0.4

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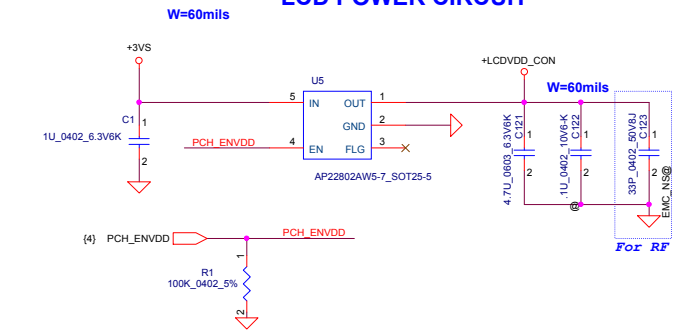
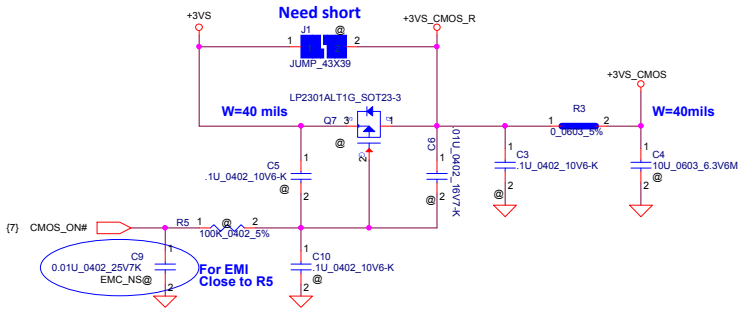
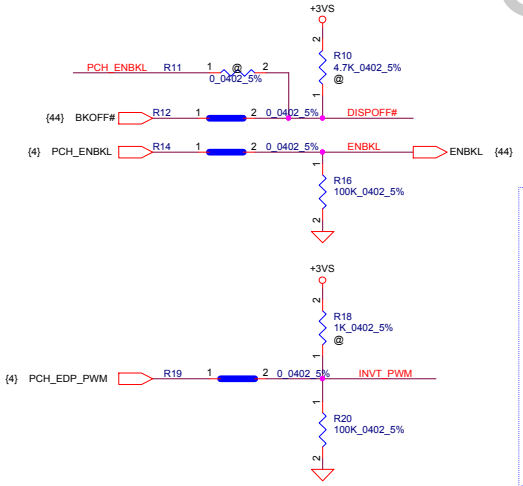
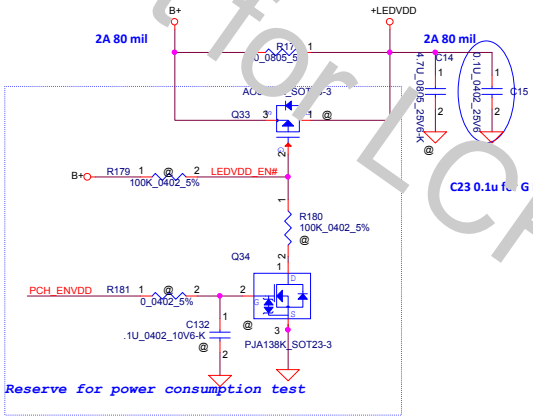
LCD POWER CIRCUIT

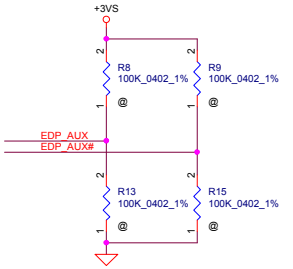


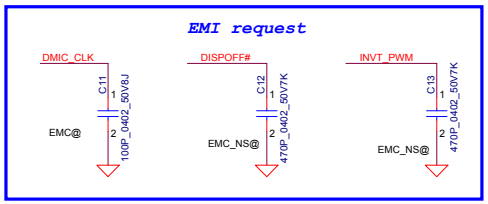
CMOS Camera

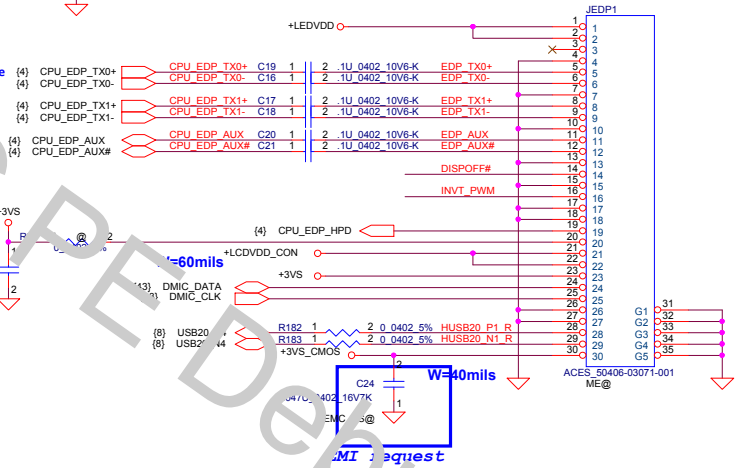


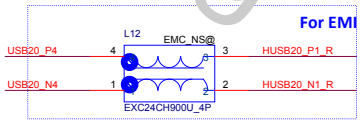












Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: eDP/ CMOS/Touch screen

Size	Document Number	Rev
Custom	BMWC1	0.4

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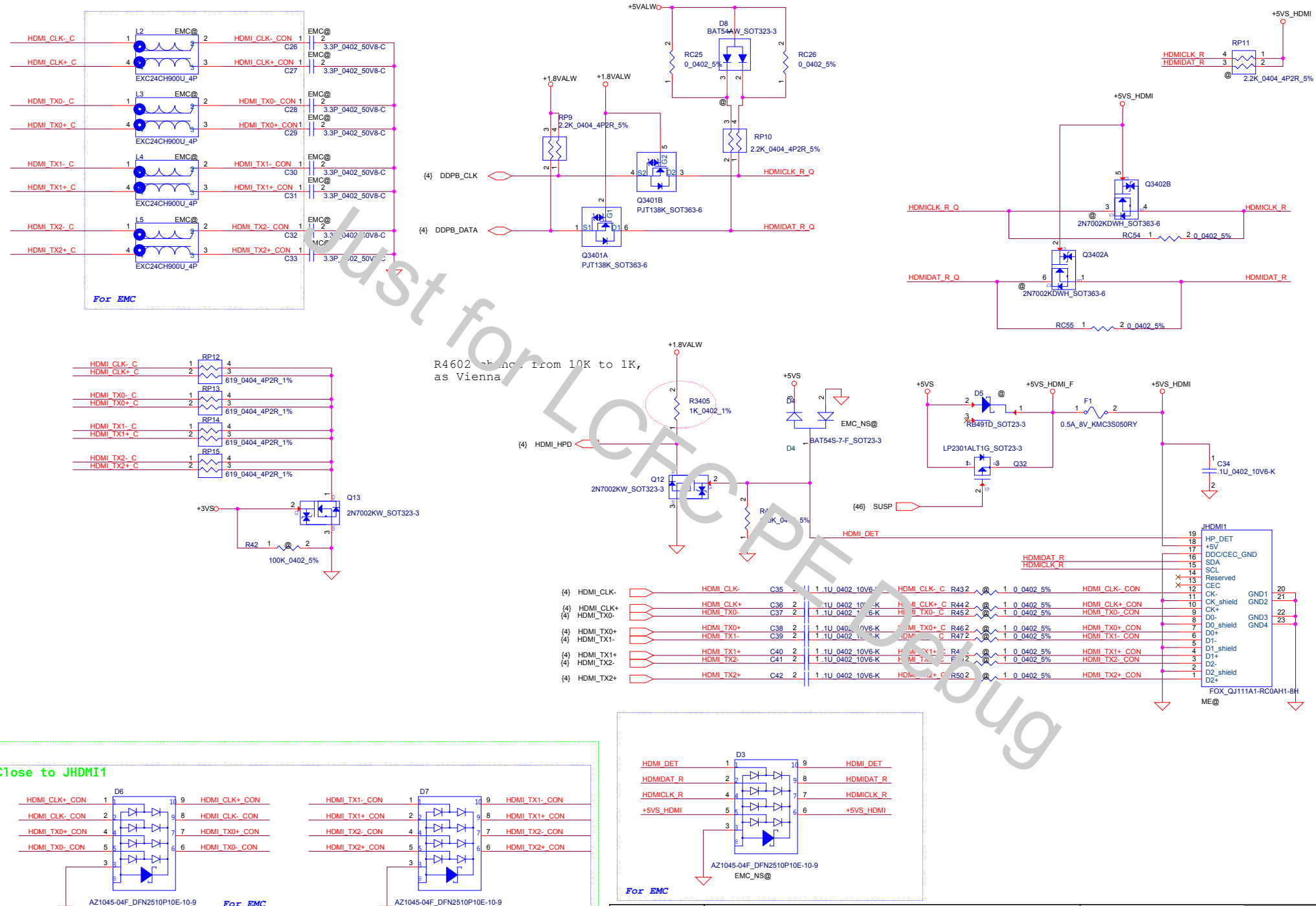

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

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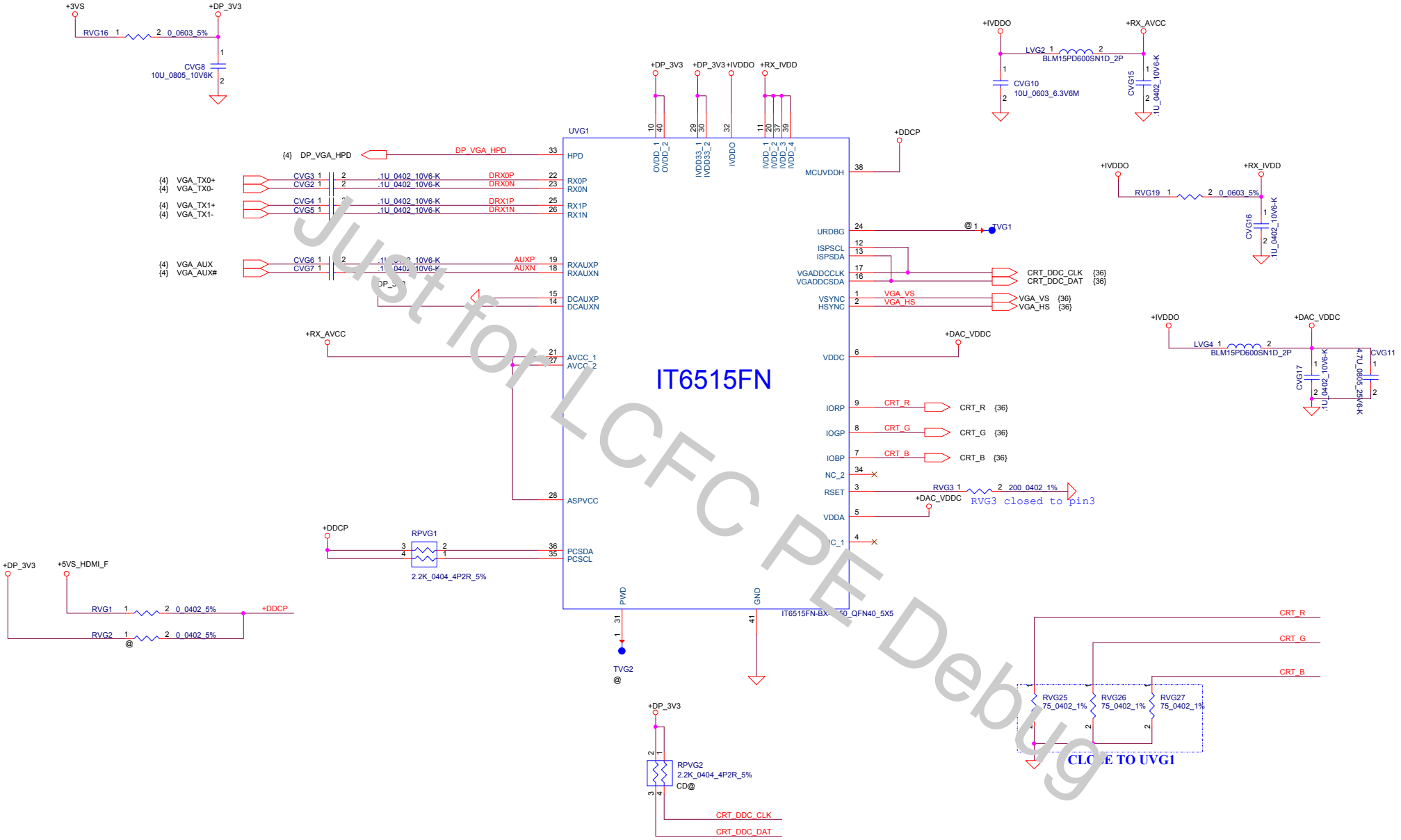
Title	HDMI_CONN		
Size	Custom	Document Number	BMWC1
Rev	0.4		
Date:	Tuesday, April 07, 2015	Sheet	34 of 60



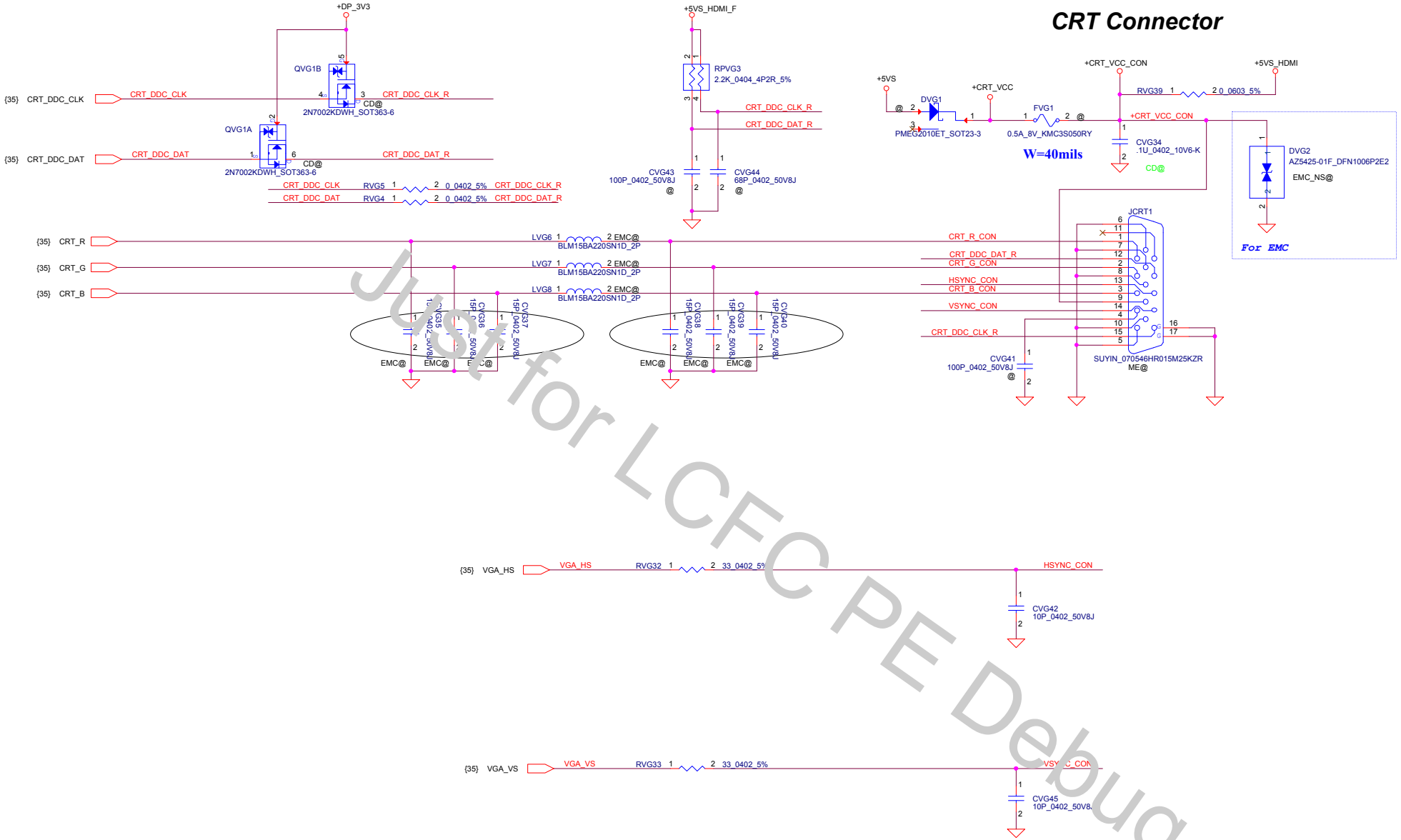
Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: DP to CRT Convert(IT6515FN)

Size	Document Number	Rev
Custom	BMWC1	0.4

Date: Tuesday, April 07, 2015 Sheet 35 of 59

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

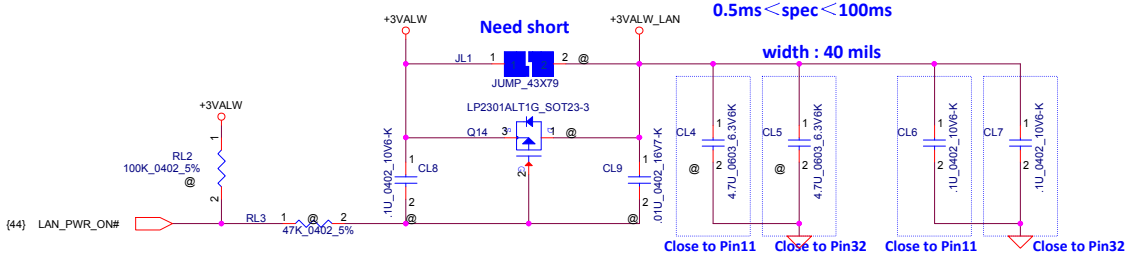
Title	CRT		
Size	Document Number		Rev
Custom	BMWC1		0.4
Date:	Tuesday, April 07, 2015	Sheet	36 of 59

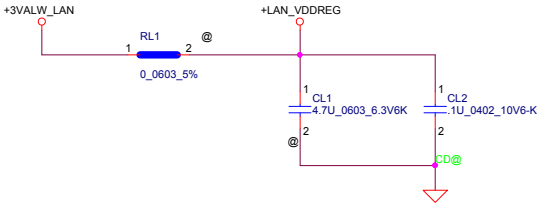
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

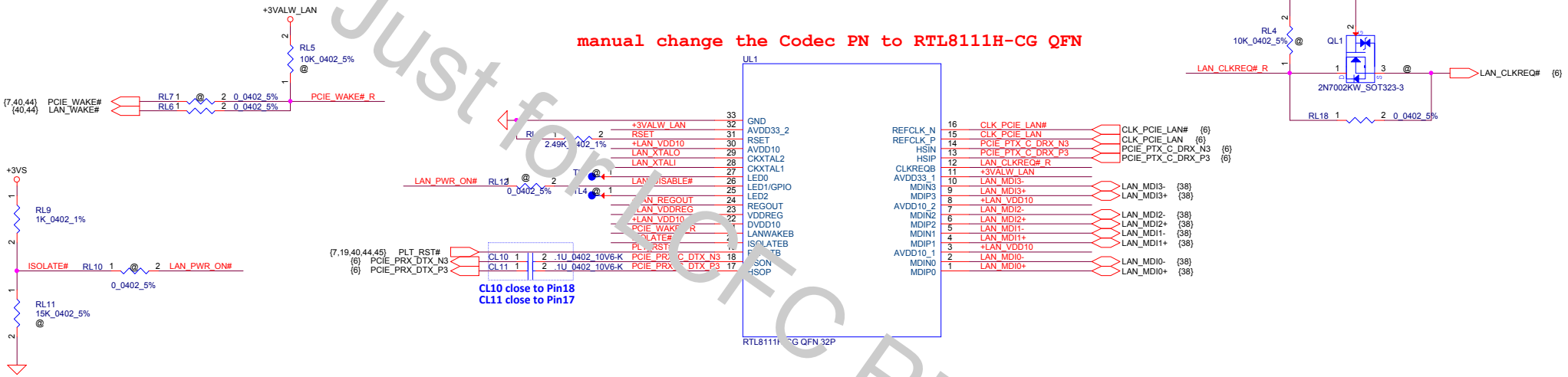
Need short

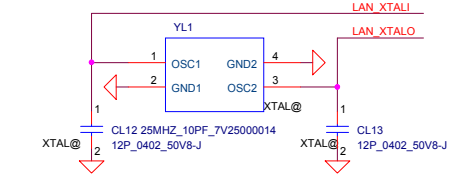
width : 40 mils

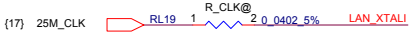


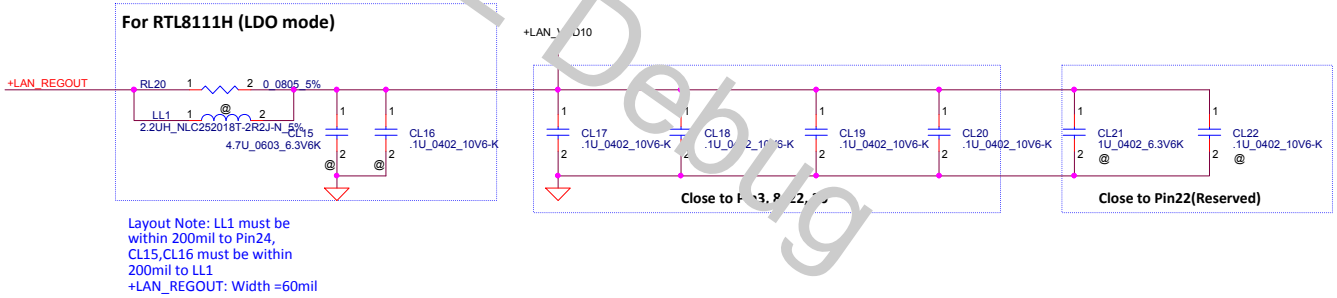


manual change the Codec PN to RTL8111H-CG QFN









Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

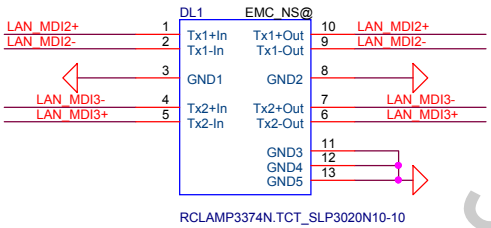
Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: LAN_RTL8111GUL/RTL8106E

Size	Document Number	Rev
Custom	BMWC1	0.4

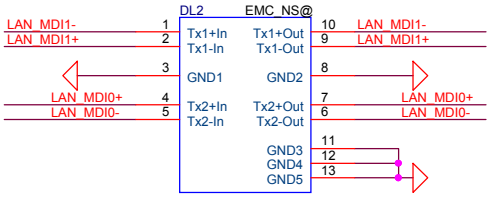
Date: Tuesday, April 07, 2015 Sheet 37 of 60

DL1/DL2
1'S PN:SC400007R00



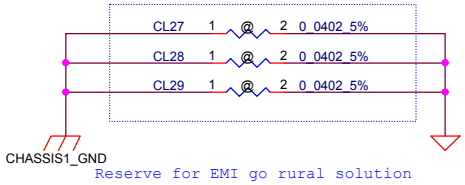
RCLAMP3374N.TCT_SLP3020N10-10

Place Close to TL1

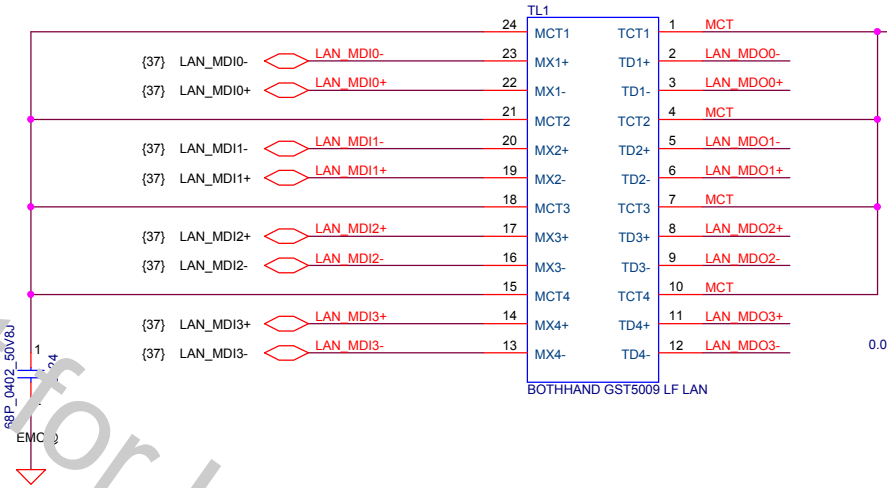


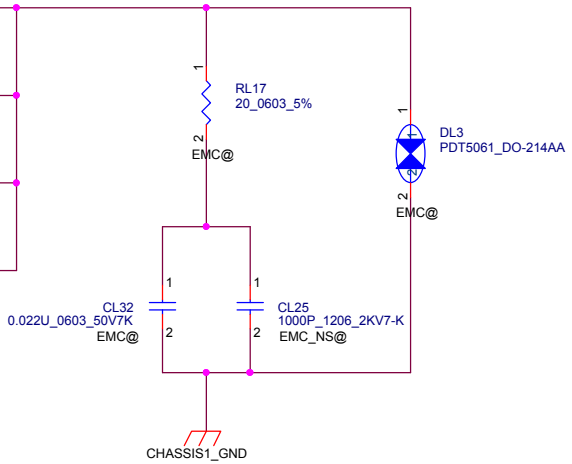
RCLAMP3374N.TCT_SLP3020N10-10

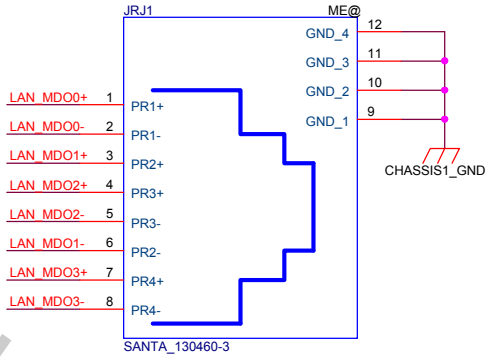
Place Close to TL2



Reserve for EMI go rural solution







Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: LAN_Transformer

Size	Document Number	Rev
B	BMWC1	0.4

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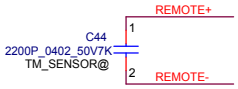
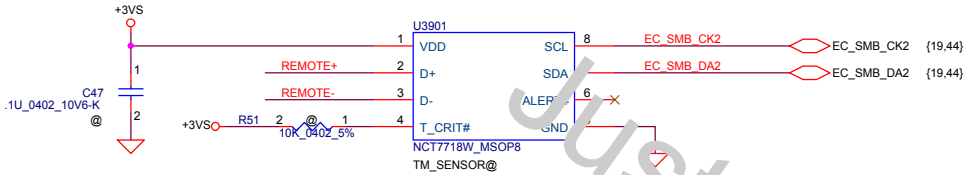
Close to U3901



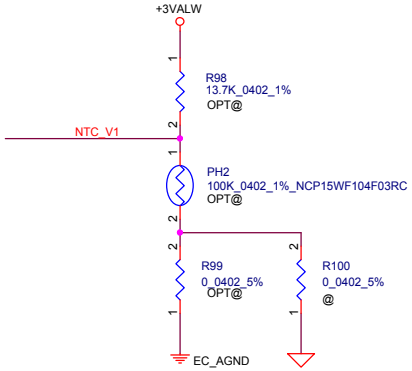
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

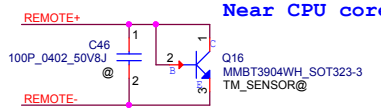


Address 1001_100xb

Near GPU&VRAM

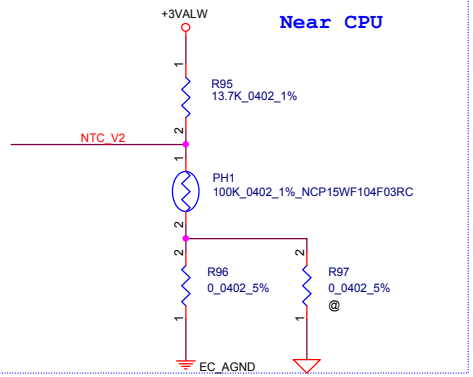


Near CPU core

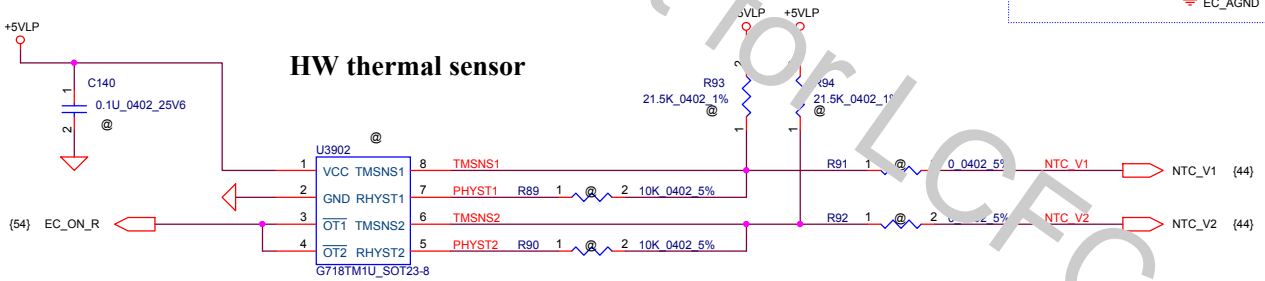


Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

Near CPU

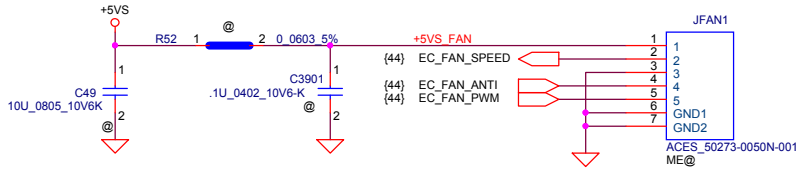


HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

FAN Conn



JFAN1 Pin defin need check other G

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: *Thermal sensor/FAN CONN*

Size	Document Number	Rev
Custom	BMWC1	0.4

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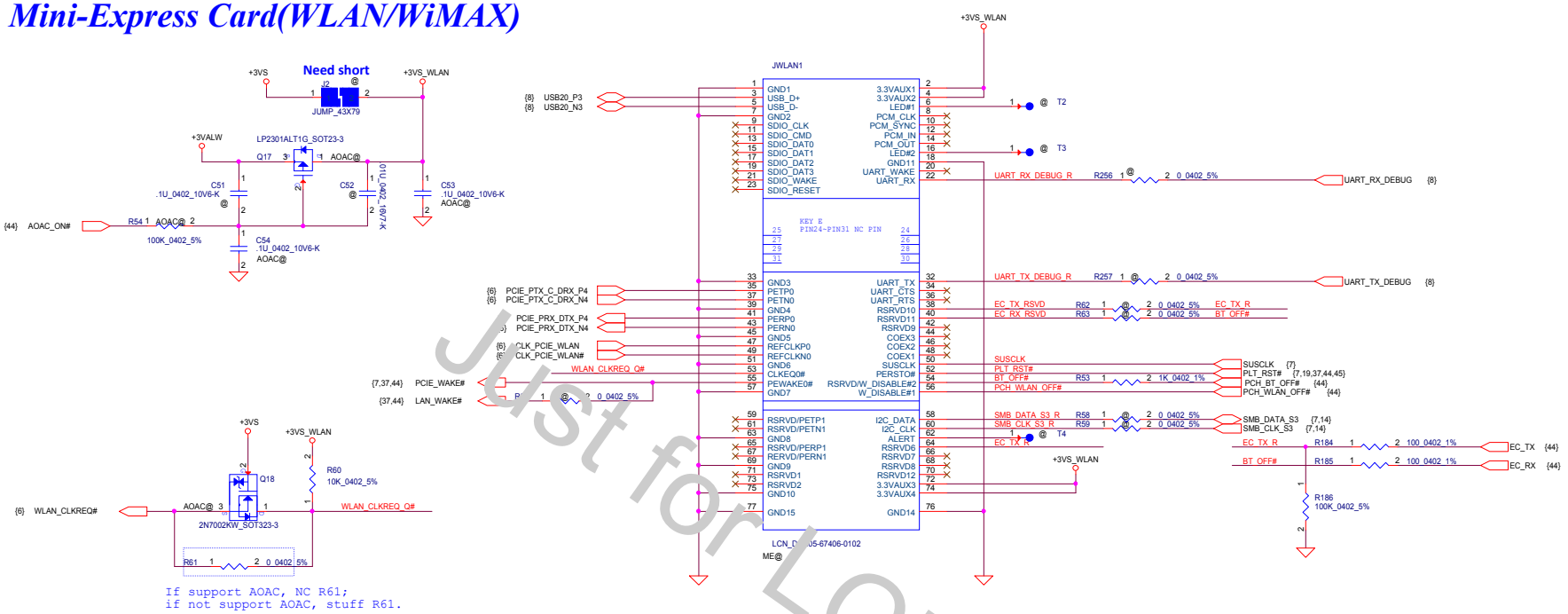
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	NGFF WLAN		
Size	Document Number		Rev
Custom	BMWC1		0.4
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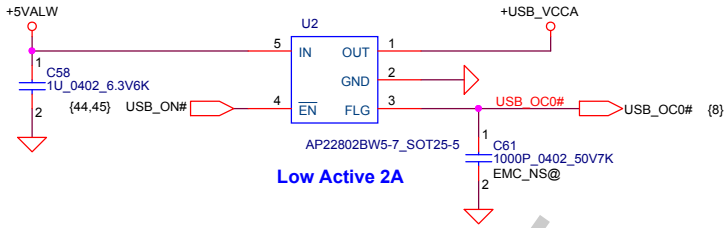
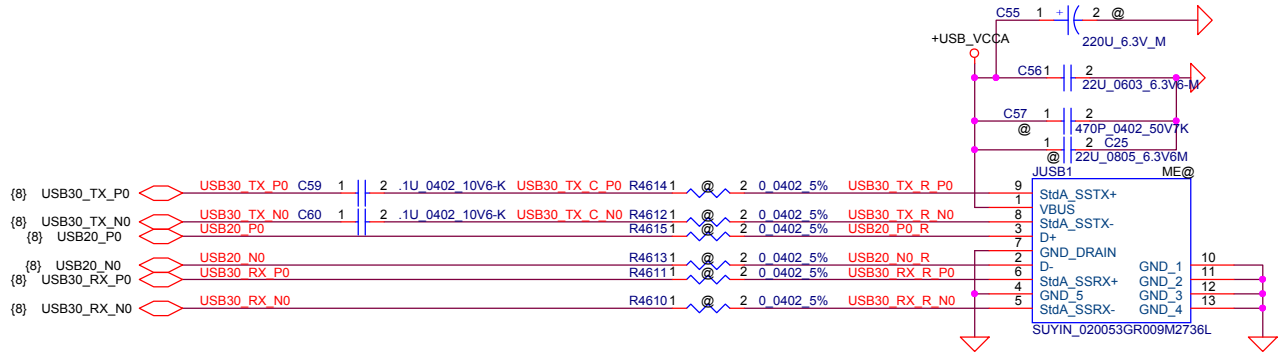
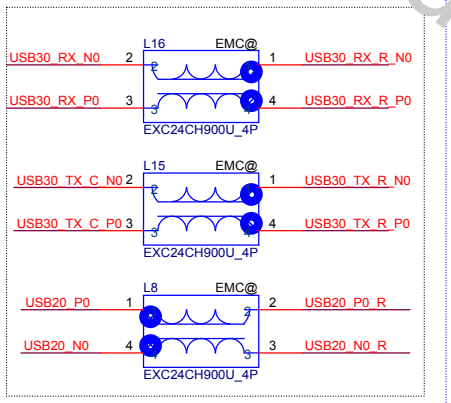
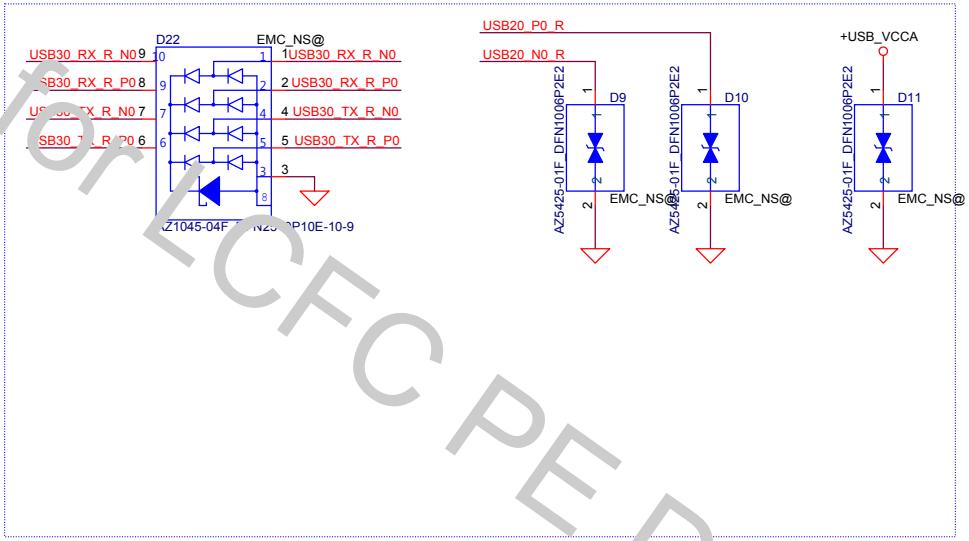
LEFT SIDE USB3.0 PORT X1







For EMC



For EMC

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: USB2.0/USB3.0 PORT (LEFT)

Size	Document Number	Rev
Custom	BMWC1	0.4

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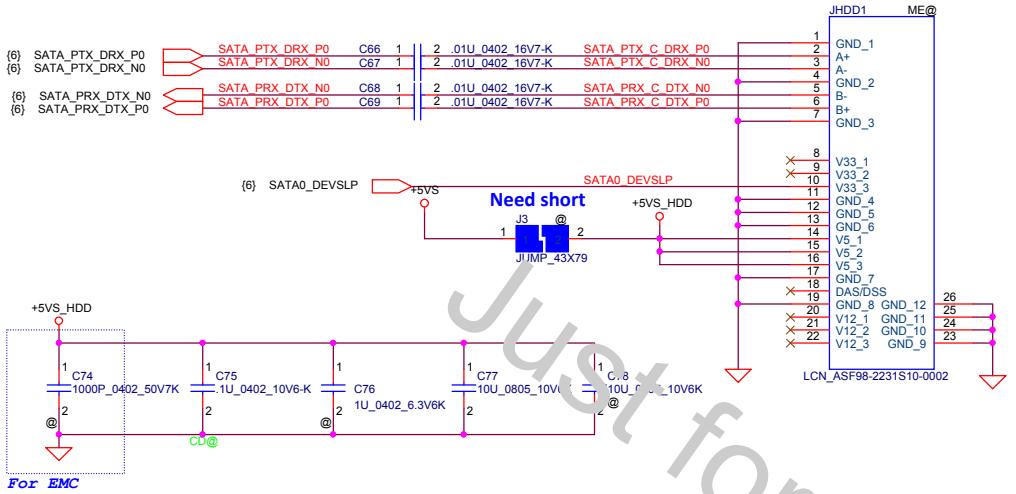
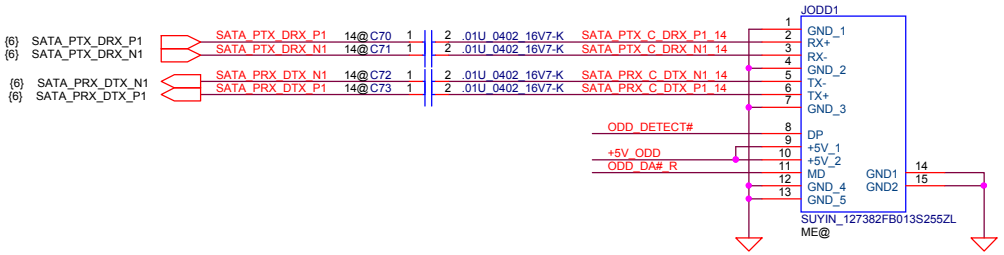
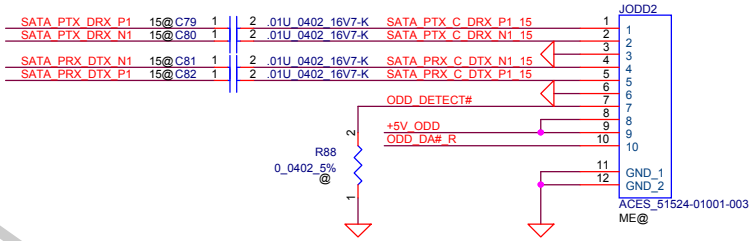
SATA HDD Conn.

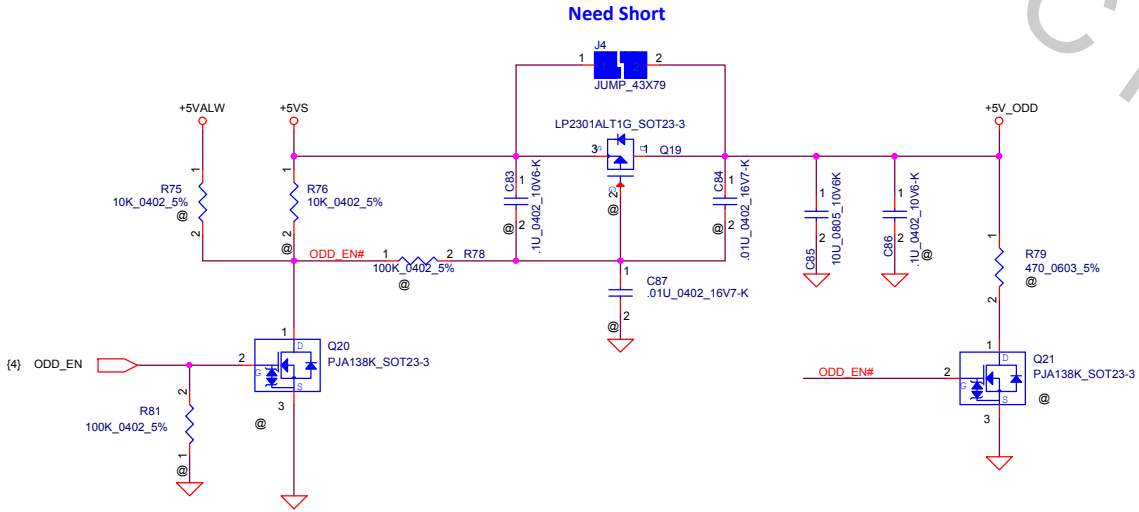


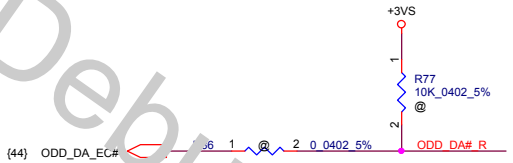
FOR 14"
SATA ODD Conn.



FOR 15"
SATA ODD FFC Conn







Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	HDD/ODD CONN		
Size	Document Number		Rev
Custom	BMWC1		0.4
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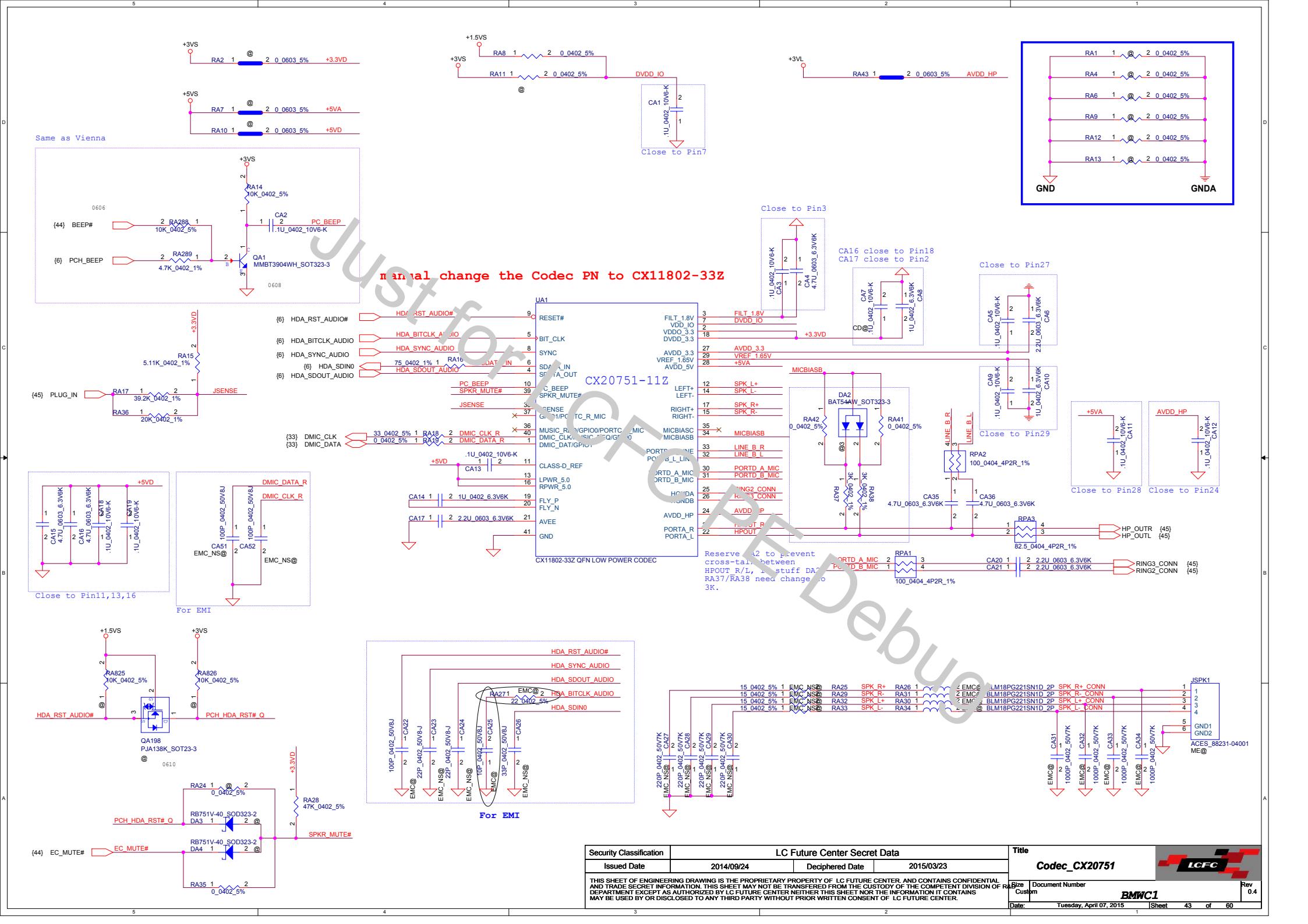
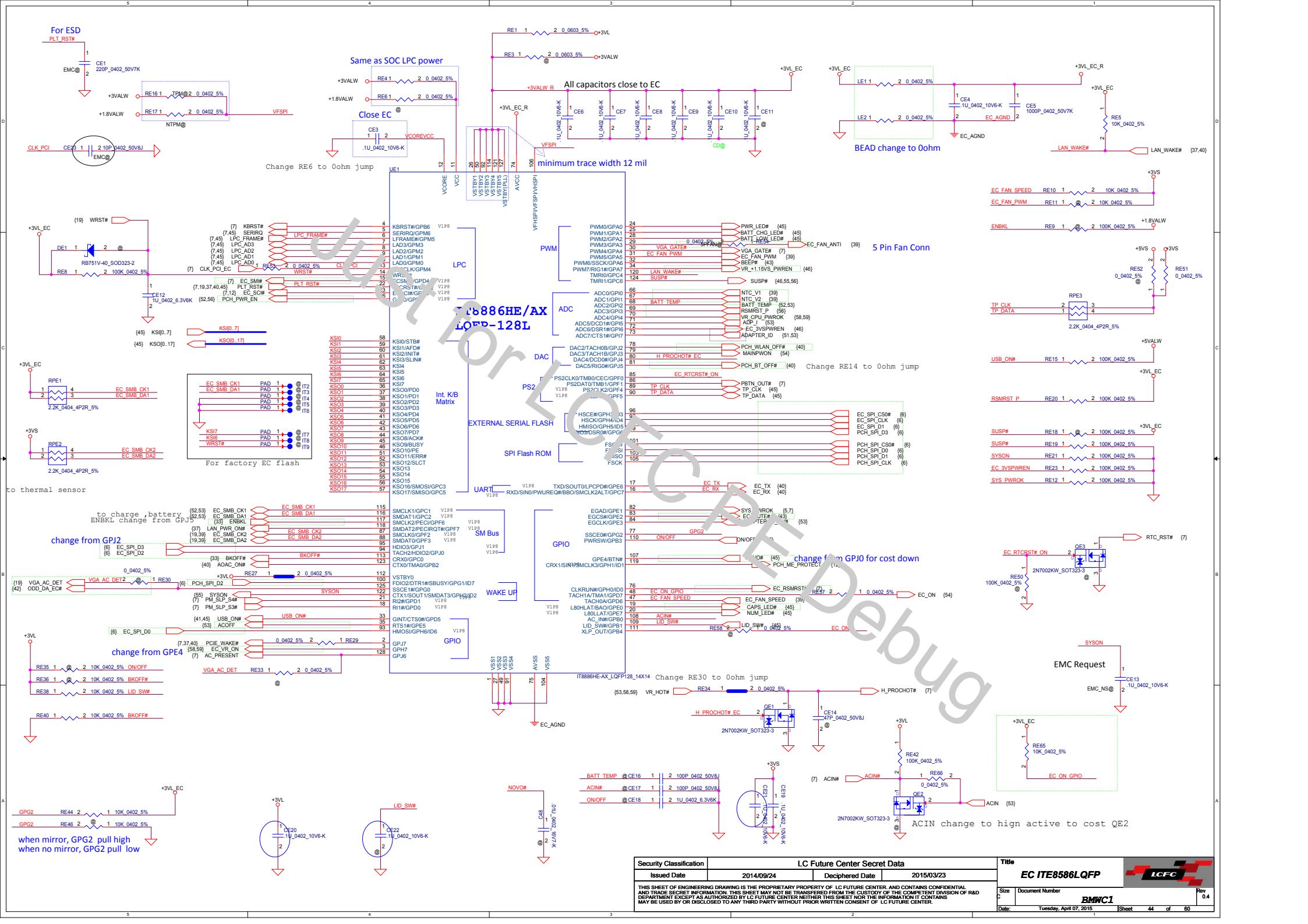


Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	Codec_CX20751		
Size	Document Number		Rev
Custom	BMWC1		0.4
Date:	Tuesday, April 07, 2015	Sheet	43 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

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Title: EC ITE8586LQFP

Size	Document Number	Rev
C	BMWC1	0.4

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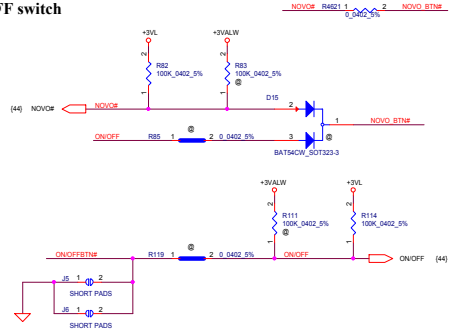
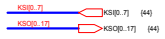
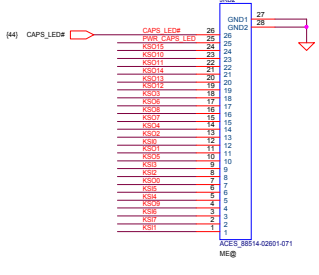
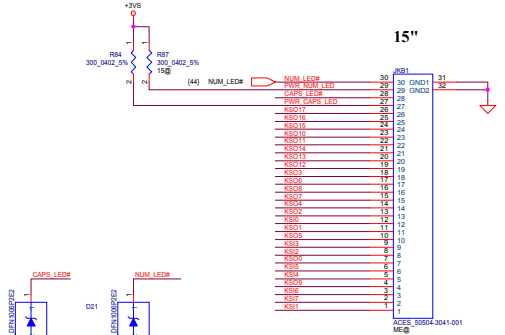
ON/OFF switch



K/B Connector

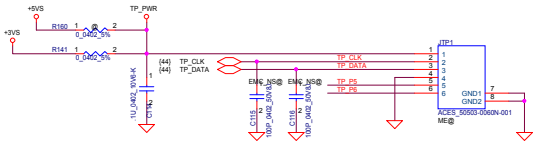


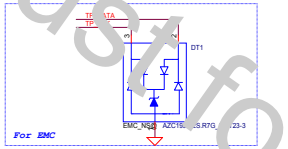


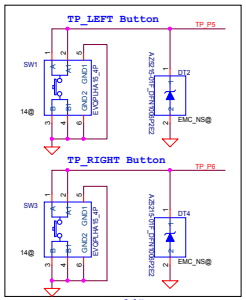


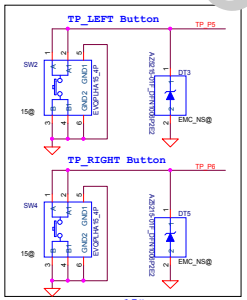
	14"	15"
KB_1	KSI1_14	KSO0_15
KB_2	KSI7_14	KSI2_15
KB_3	KSI6_14	KSI3_15
KB_4	KSO9_14	KSO5_15
KB_5	KSI4_14	KSO1_15
KB_6	KSI5_14	KSI0_15
KB_7	KSO0_14	KSO2_15
KB_8	KSI2_14	KSO4_15
KB_9	KSI3_14	KSO7_15
KB_10	KSO5_14	KSO8_15
KB_11	KSO1_14	KSO6_15
KB_12	KSI0_14	KSO3_15
KB_13	KSO2_14	KSO12_15
KB_14	KSO4_14	KSO13_15
KB_15	KSO7_14	KSO14_15
KB_16	KSO8_14	KSO11_14
KB_17	KSO6_14	KSO10_15
KB_18	KSO3_14	KSO15_15
KB_19	KSO12_14	KSO16_15
KB_20	KSO13_14	KSO17_15
KB_21	KSO14_14	KB_LED_PWR_15
KB_22	KSO11_14	CAPS_LED#_15
KB_23	KSO10_14	VDD_15
KB_24	KSO15_14	NUM_LED#_15

TP/B Connector







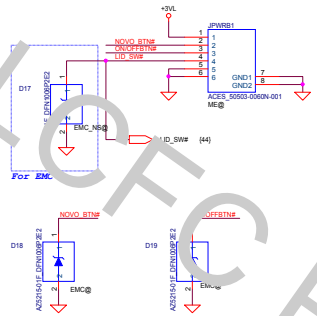


For 14"	
1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

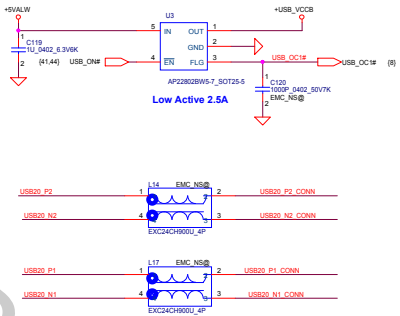
For 15"	
1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

Change to same as ACLUA

PWR/B Connector

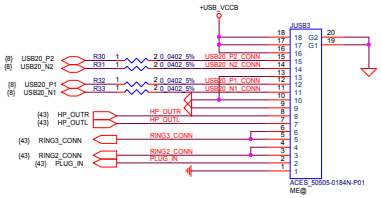


Right Side USB2.0 Port X 2 (USB/B)

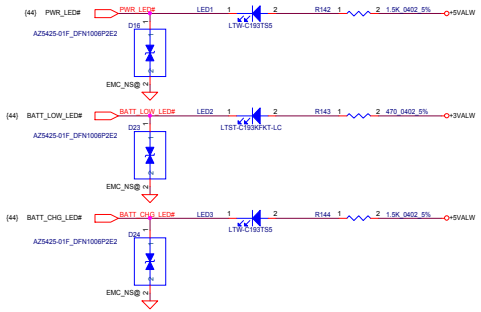


Low Active 2.5A

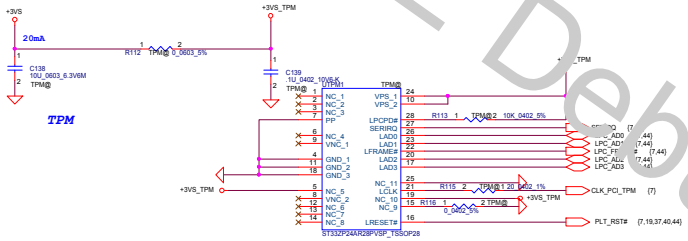
USB I/O Connector



LED



check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14"/15" 02/26



TPM

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Title: KBD/PWR/IO/LED/TP Conn.

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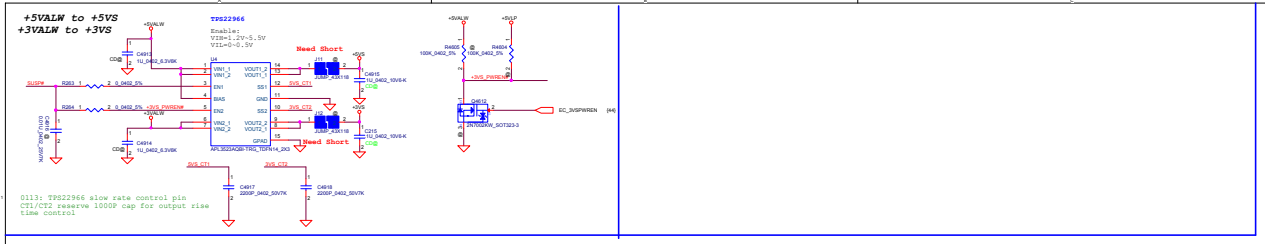

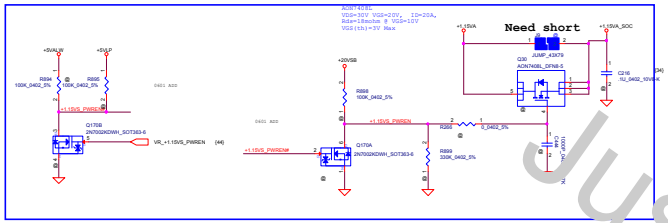

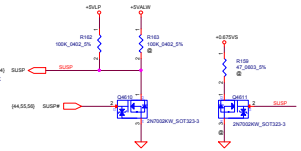

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	DC V TO VS INTERFACE		
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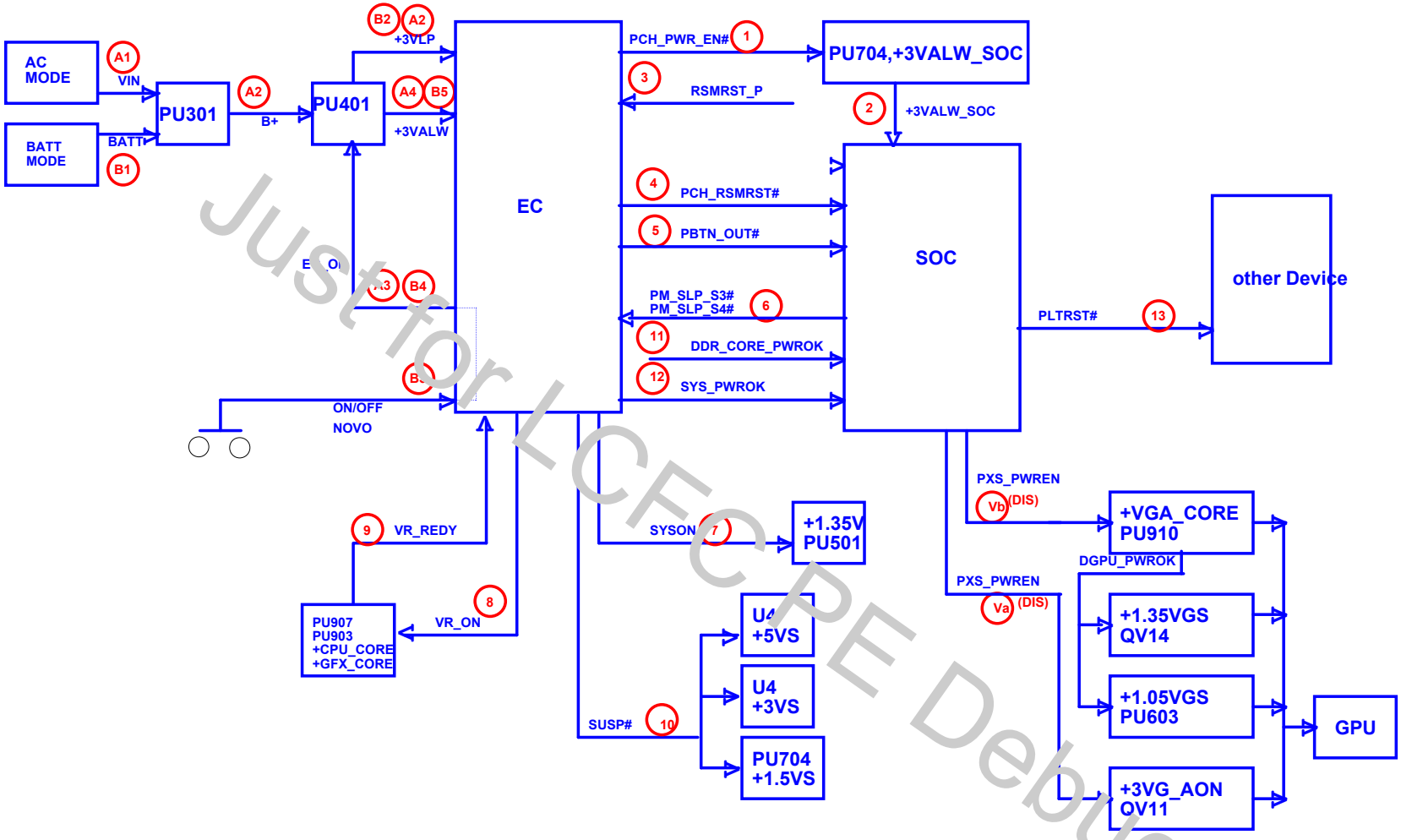

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: *Power sequence Block*

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Title: *Virtual symbol*

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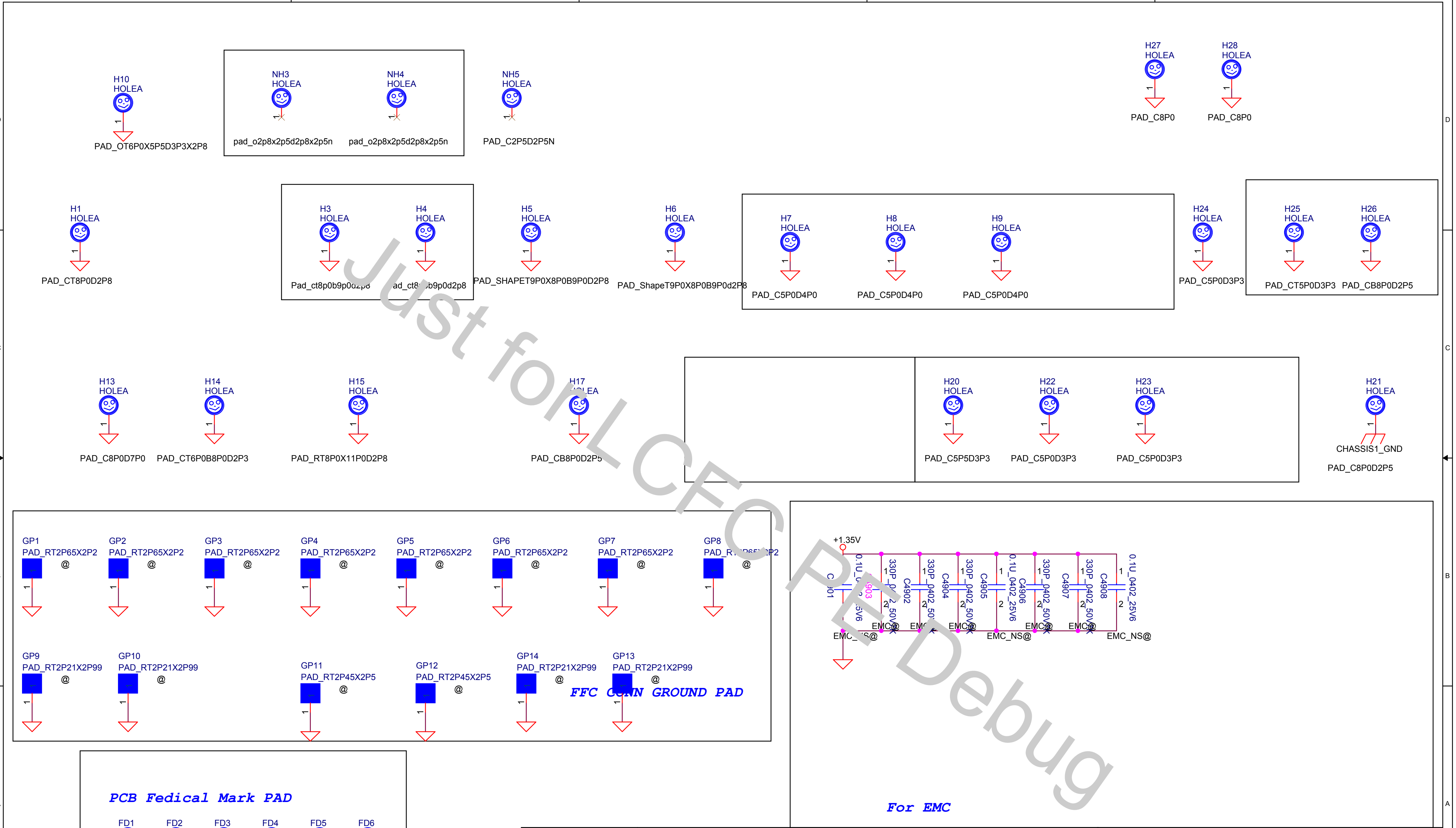

H10 HOLEA PAD_OT6P0X5P5D3P3X2P8
NH3 HOLEA pad_o2p8x2p5d2p8x2p5n
NH4 HOLEA pad_o2p8x2p5d2p8x2p5n
NH5 HOLEA PAD_C2P5D2P5N
H27 HOLEA PAD_C8P0
H28 HOLEA PAD_C8P0
H1 HOLEA PAD_CT8P0D2P8
H3 HOLEA Pad_ct8p0b9p0d2p8
H4 HOLEA Pad_ct8p0b9p0d2p8
H5 HOLEA PAD_SHAPET9P0X8P0B9P0D2P8
H6 HOLEA PAD_ShapeT9P0X8P0B9P0d2P8
H7 HOLEA PAD_C5P0D4P0
H8 HOLEA PAD_C5P0D4P0
H9 HOLEA PAD_C5P0D4P0
H24 HOLEA PAD_C5P0D3P3
H25 HOLEA PAD_CT5P0D3P3
H26 HOLEA PAD_CB8P0D2P5
H13 HOLEA PAD_C8P0D7P0
H14 HOLEA PAD_CT6P0B8P0D2P3
H15 HOLEA PAD_RT8P0X11P0D2P8
H17 HOLEA PAD_CB8P0D2P5
H20 HOLEA PAD_C5P5D3P3
H22 HOLEA PAD_C5P0D3P3
H23 HOLEA PAD_C5P0D3P3
H21 HOLEA CHASSIS1_GND PAD_C8P0D2P5
GP1 PAD_RT2P65X2P2 @
GP2 PAD_RT2P65X2P2 @
GP3 PAD_RT2P65X2P2 @
GP4 PAD_RT2P65X2P2 @
GP5 PAD_RT2P65X2P2 @
GP6 PAD_RT2P65X2P2 @
GP7 PAD_RT2P65X2P2 @
GP8 PAD_RT2P65X2P2 @
GP9 PAD_RT2P21X2P99 @
GP10 PAD_RT2P21X2P99 @
GP11 PAD_RT2P45X2P5 @
GP12 PAD_RT2P45X2P5 @
GP14 PAD_RT2P21X2P99 @
GP13 PAD_RT2P21X2P99 @
FFC CONN GROUND PAD
+1.35V
C4901 0.1U_0402_25V6 EMC_NS@
C4903 330P_0402_50V EMC@
C4902 330P_0402_50V EMC@
C4904 330P_0402_50V EMC@
C4905 0.1U_0402_25V6 EMC_NS@
C4906 330P_0402_50V EMC@
C4907 330P_0402_50V EMC@
C4908 0.1U_0402_25V6 EMC_NS@
For EMC
PCB Fedical Mark PAD
FD1 FD2 FD3 FD4 FD5 FD6

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Title: Hole

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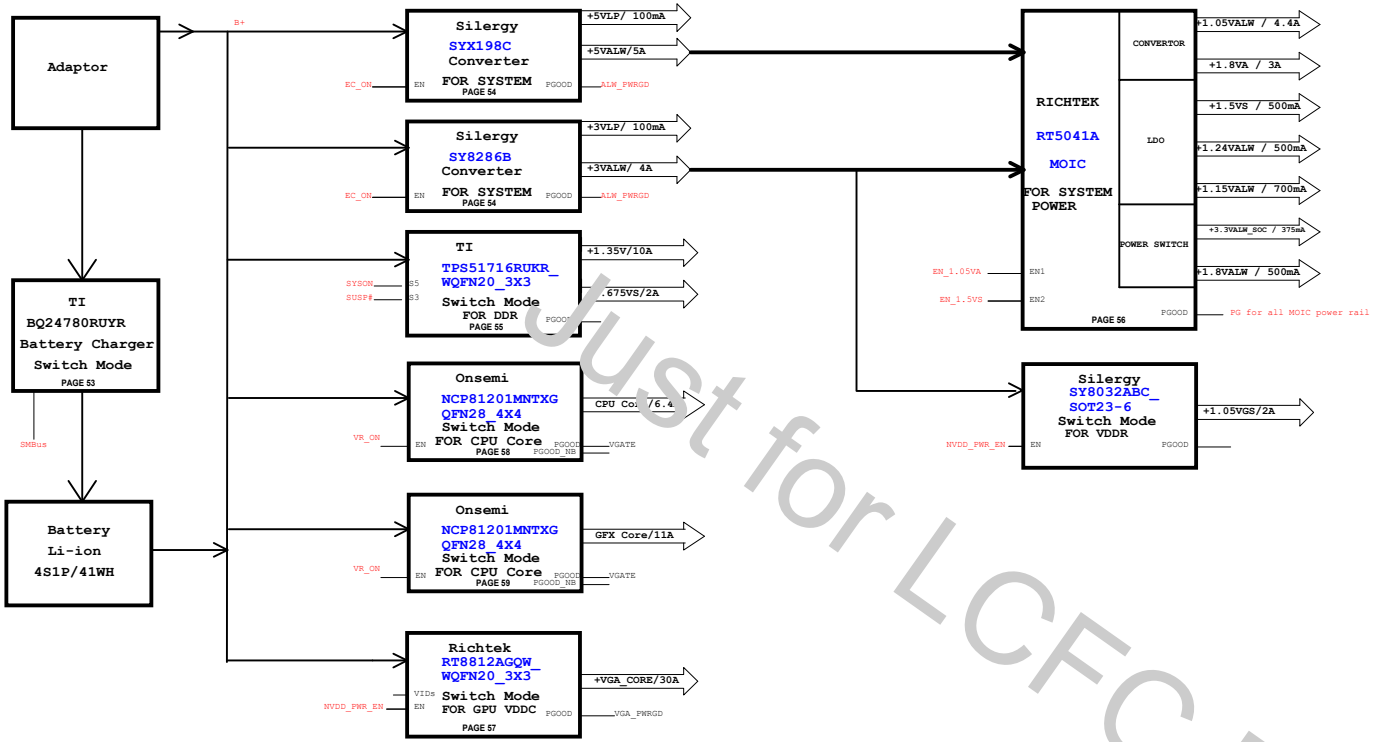

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	Power Diagram		
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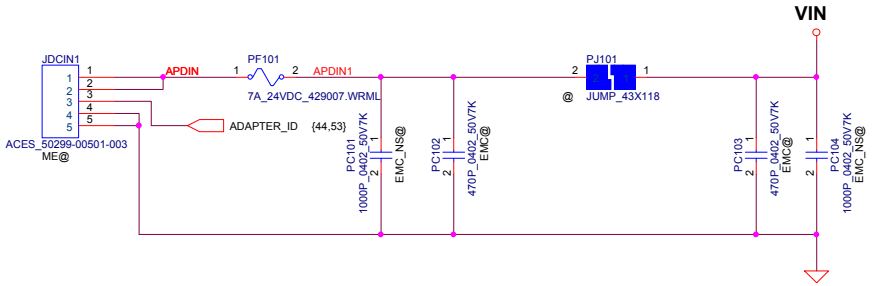

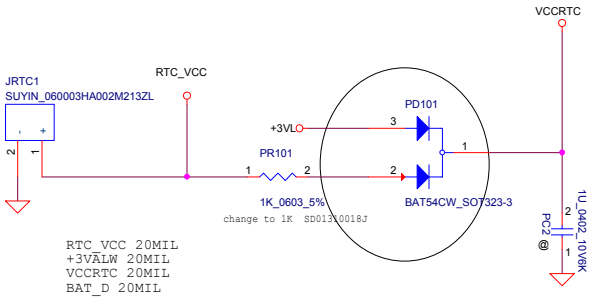

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: **DCIN / RTC**

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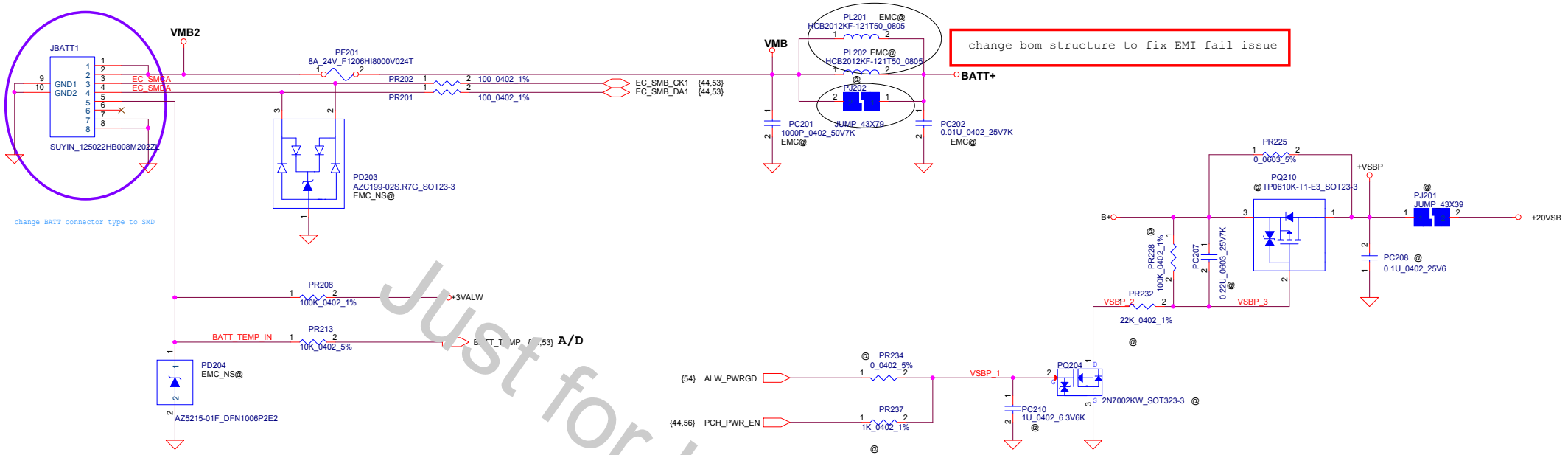

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
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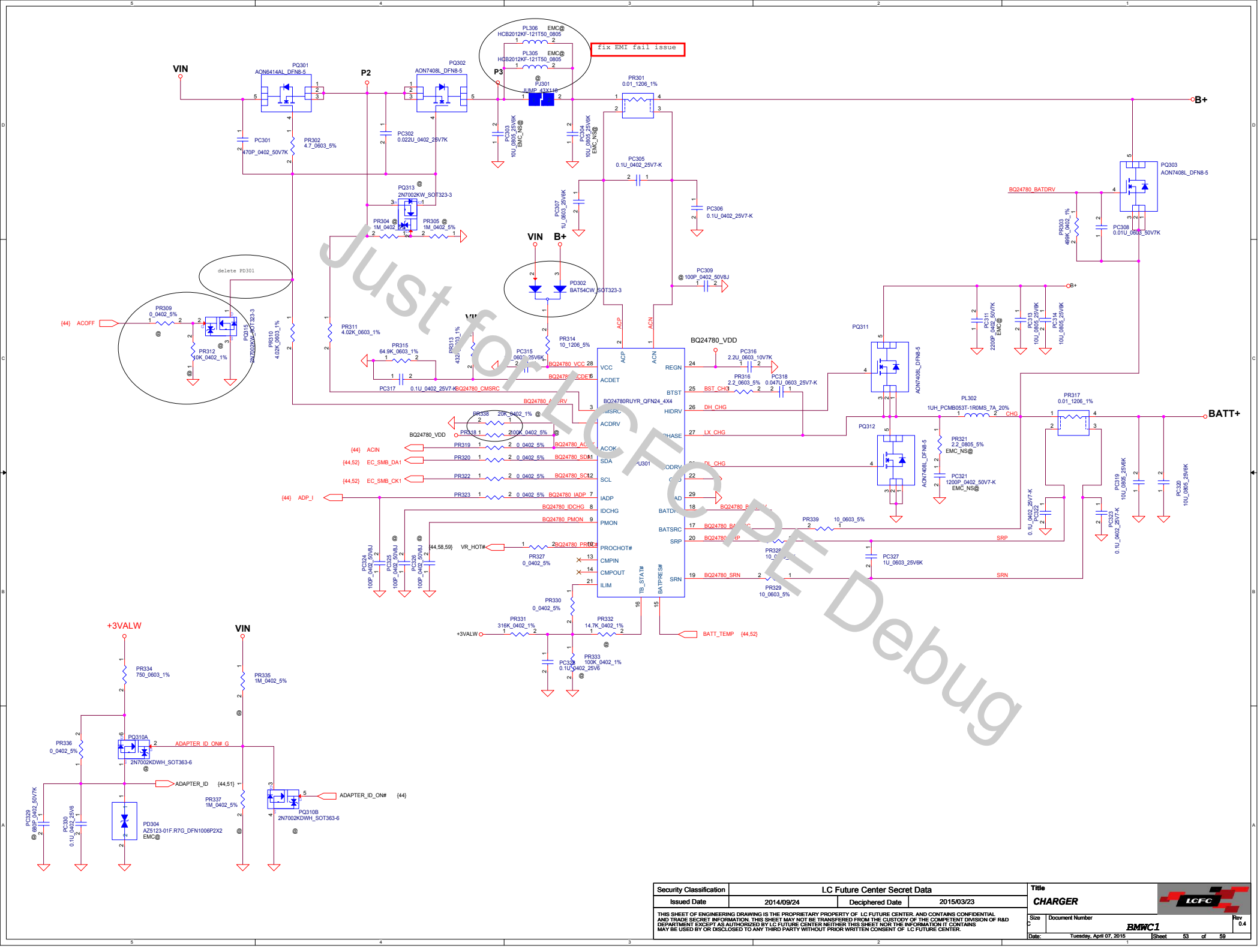

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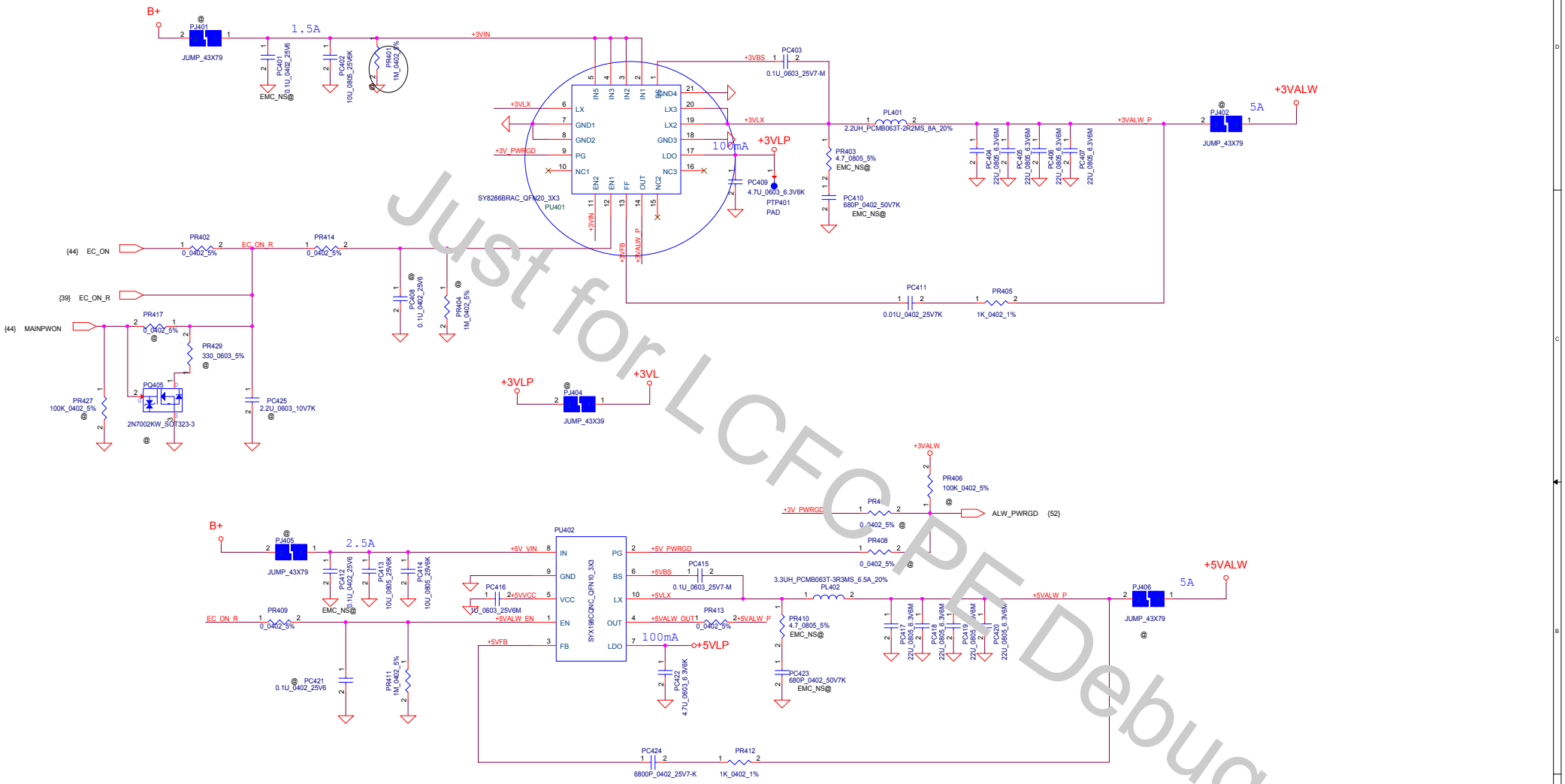

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: PWR_3VALW/5VALW

Size	Document Number	Rev
C	BMWC1	0.4

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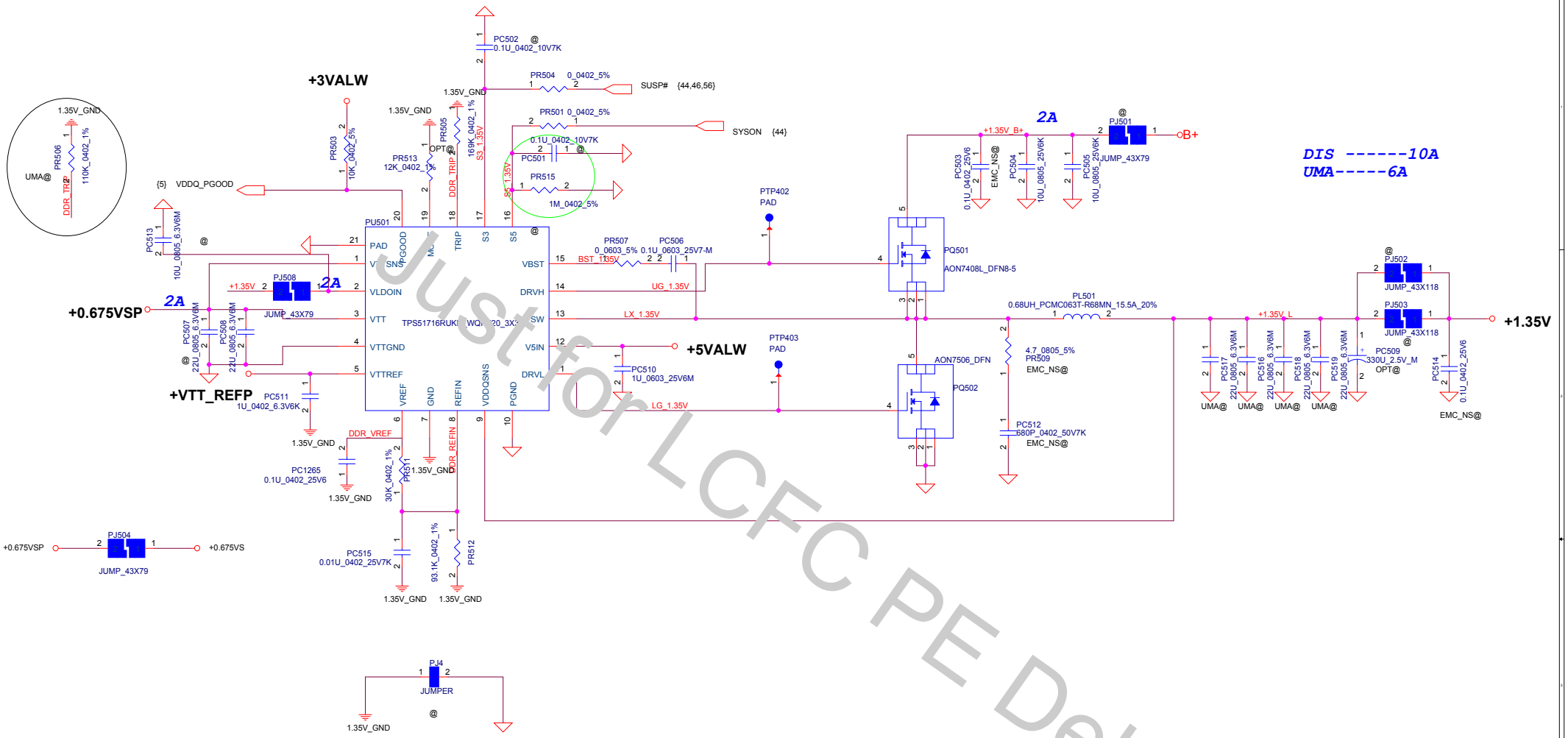

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: 1.35VS/+0.675VS

Size	Document Number	Rev
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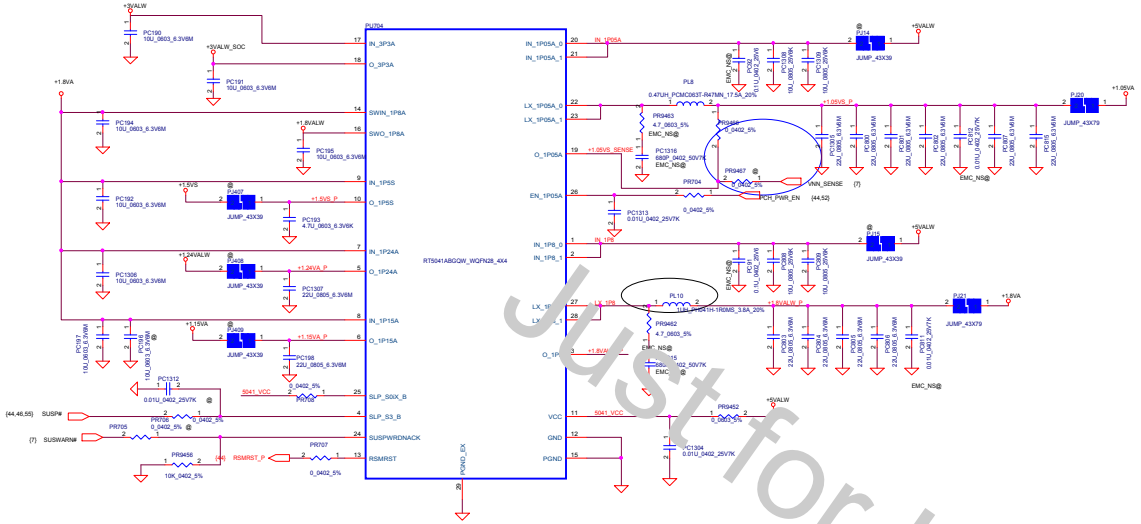

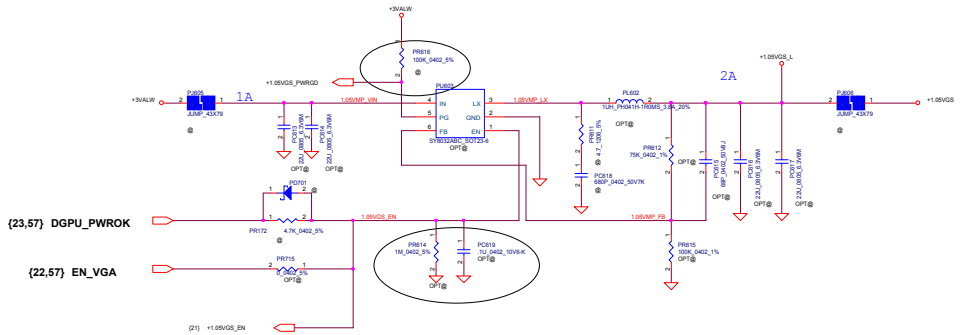

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Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	PWR-SYSTEM POWER		
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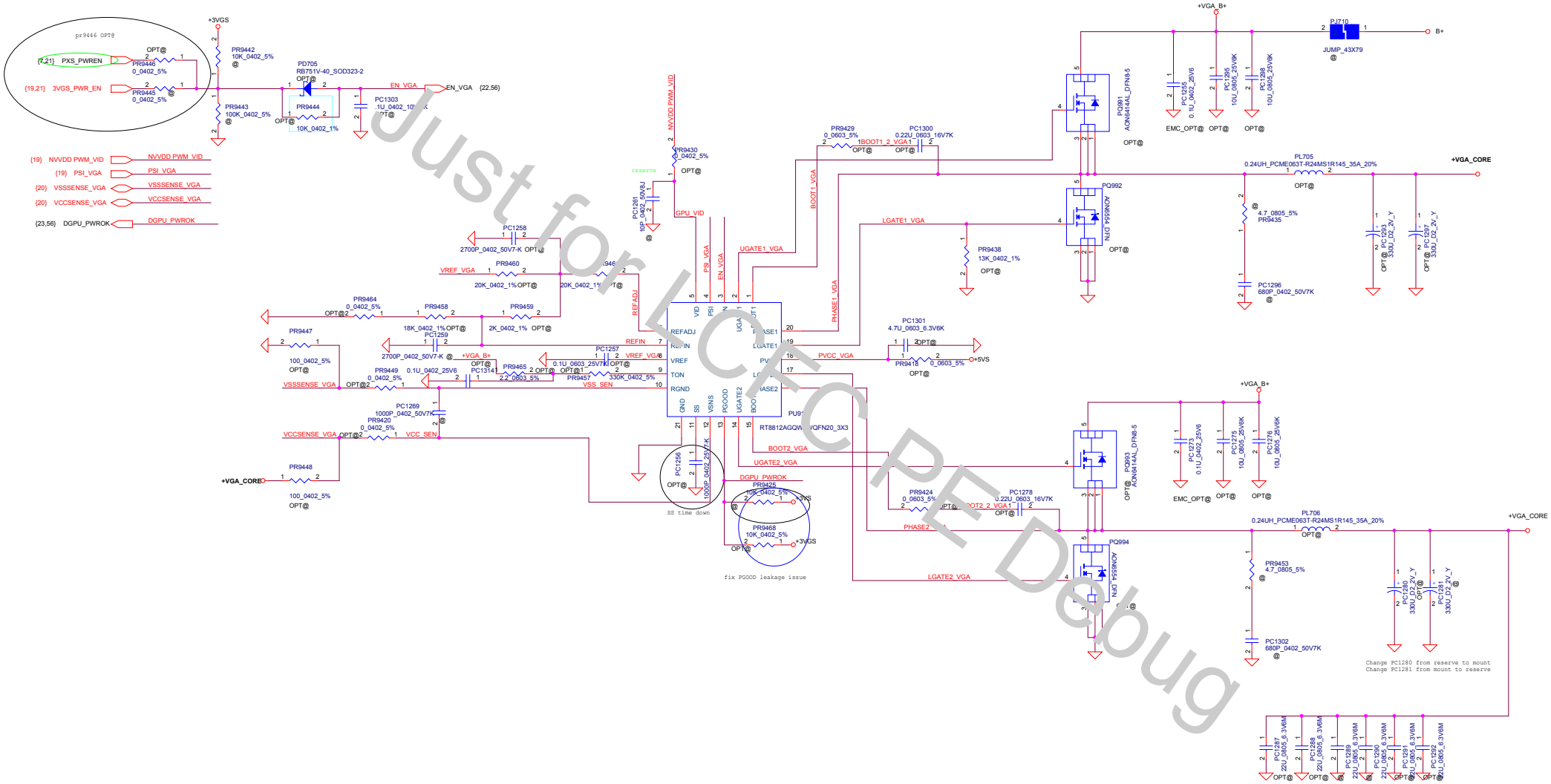

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title	PWR-VGA_CORE		
Size: Custom	Document Number: BMWC1		Rev: 0.4
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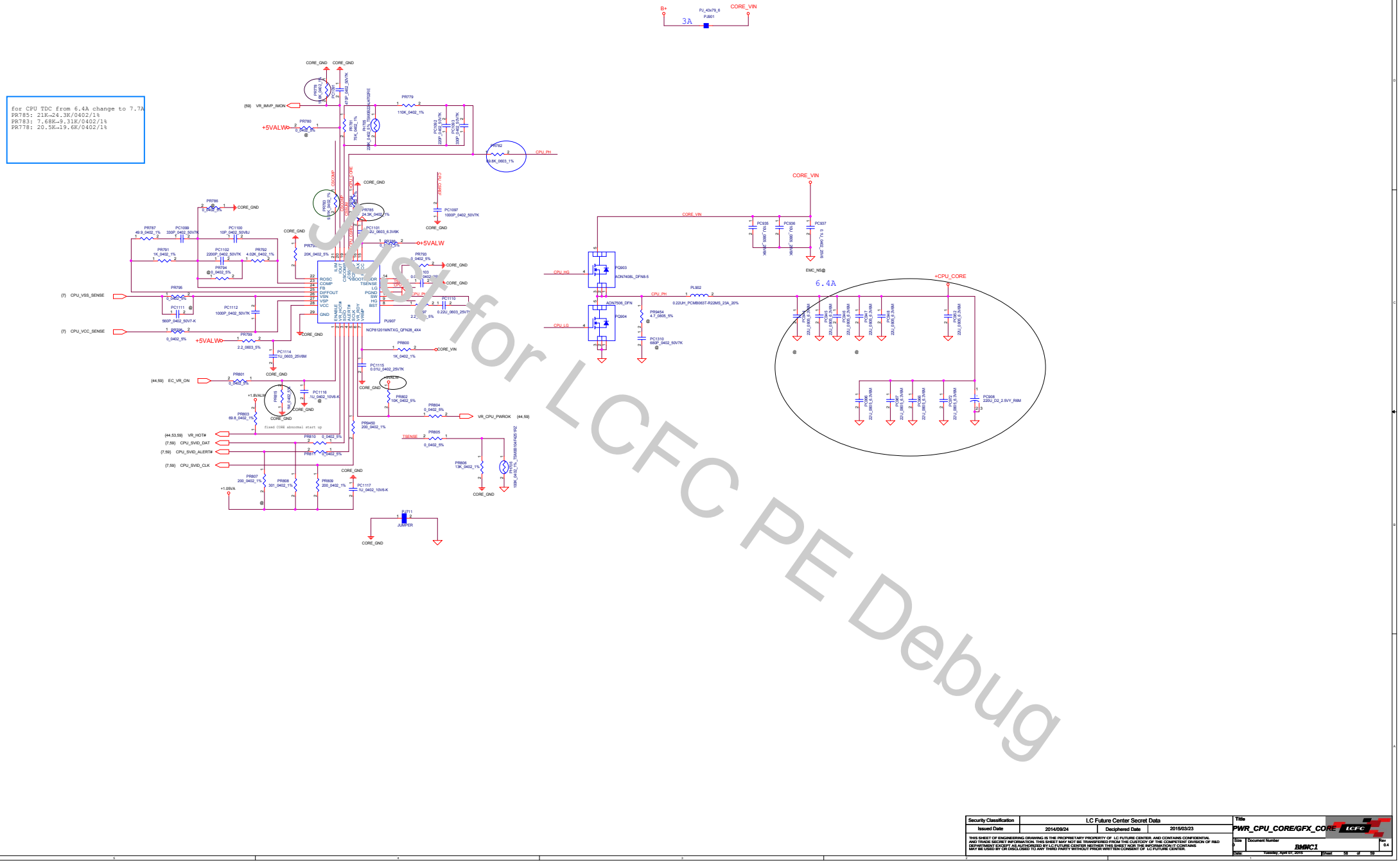

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Title: PWR_CPU_CORE/GFX_CORE

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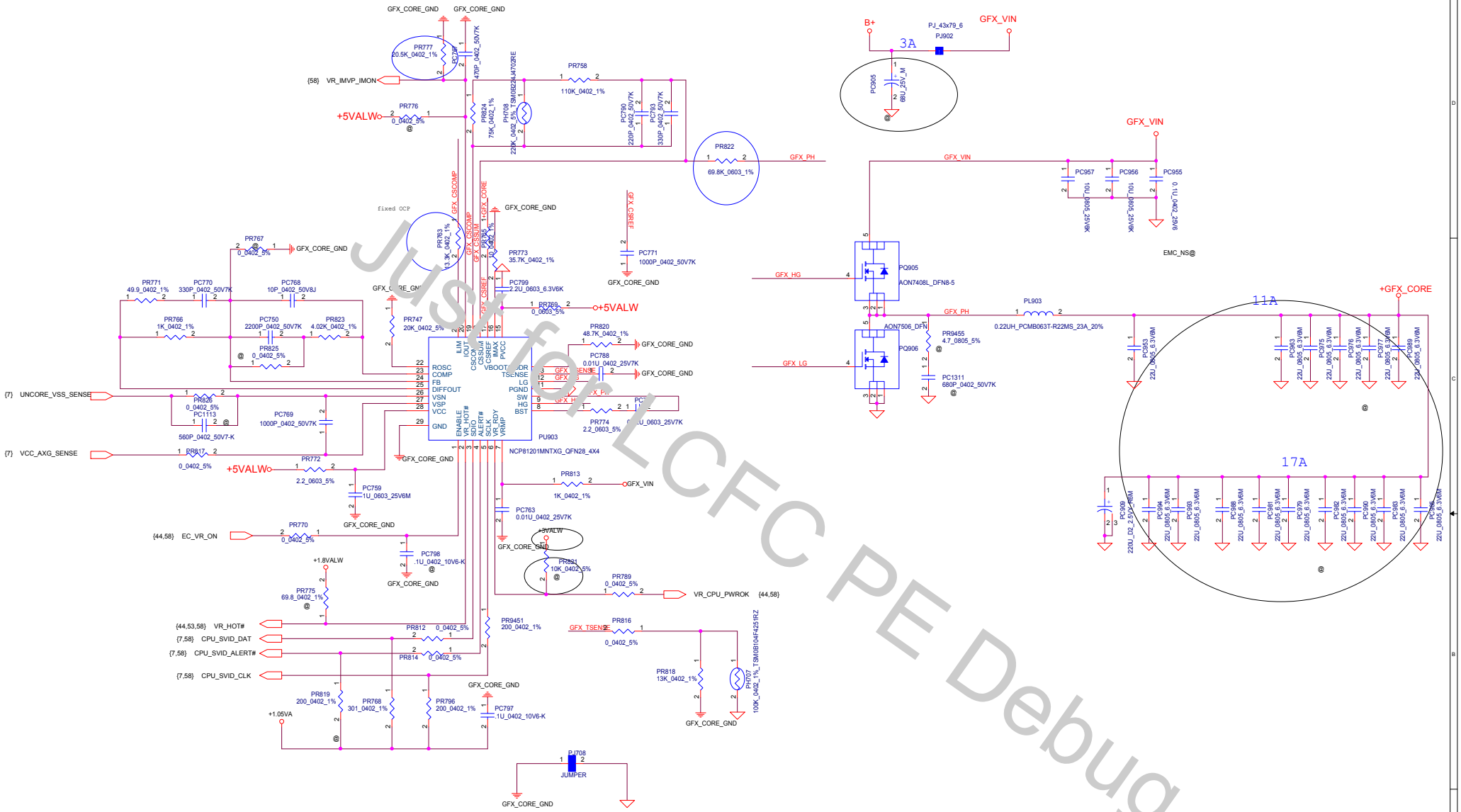

Security Classification	LC Future Center Secret Data		
Issued Date	2014/09/24	Deciphered Date	2015/03/23

Title: **PWR_GFX Core**

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