Compal Confidential

PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT

2010-11-26

REV:0.3

Security Classification	Compal Secret Data		
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Title: Cover Page		
Size: Custom	Document Number: PIQY0 LA6881P	Rev: 0.3
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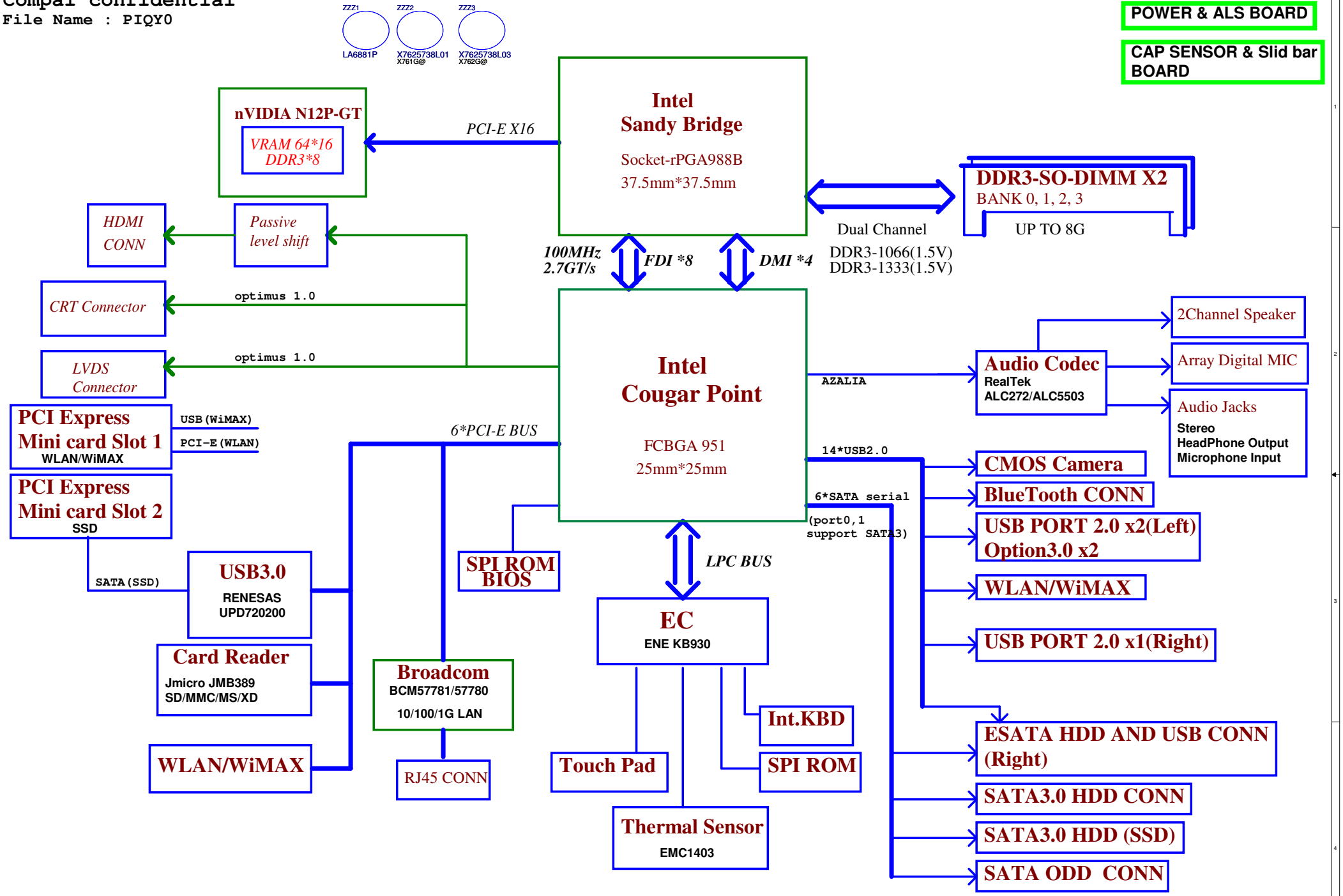
Compal confidential
File Name : PIQY0

ZZZ1 LA6881P
ZZZ2 X7625738L01 X761G@
ZZZ3 X7625738L03 X762G@

POWER & ALS BOARD

CAP SENSOR & Slid bar BOARD



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Title: MB Block Diagram

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

VRAM BOM Config

X761G@:	X7625738L01	Samsung 1GB
Sub:	X7625738L02	Hynix 1GB
X762G@:	X7625738L03	Samsung 2GB
Sub:	X7625738L04	Hynix 2GB

GPU BOM Config

N12P SKU:	OPTI@
GS SKU:	GS@
GT SKU:	GT@

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Title: Notes List

Size	Document Number	Rev
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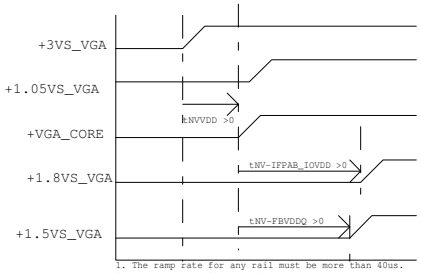

1. The ramp rate for any rail must be more than 40us.
2. +VGA_CORE <= +3VS_VGA +0.5V
3. +1.5VS_VGA <= +3VS_VGA +0.5V
4. Optimus follows power sequencing rules
   specified in discrete GPU design guide.

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Title: **VGA Notes List**

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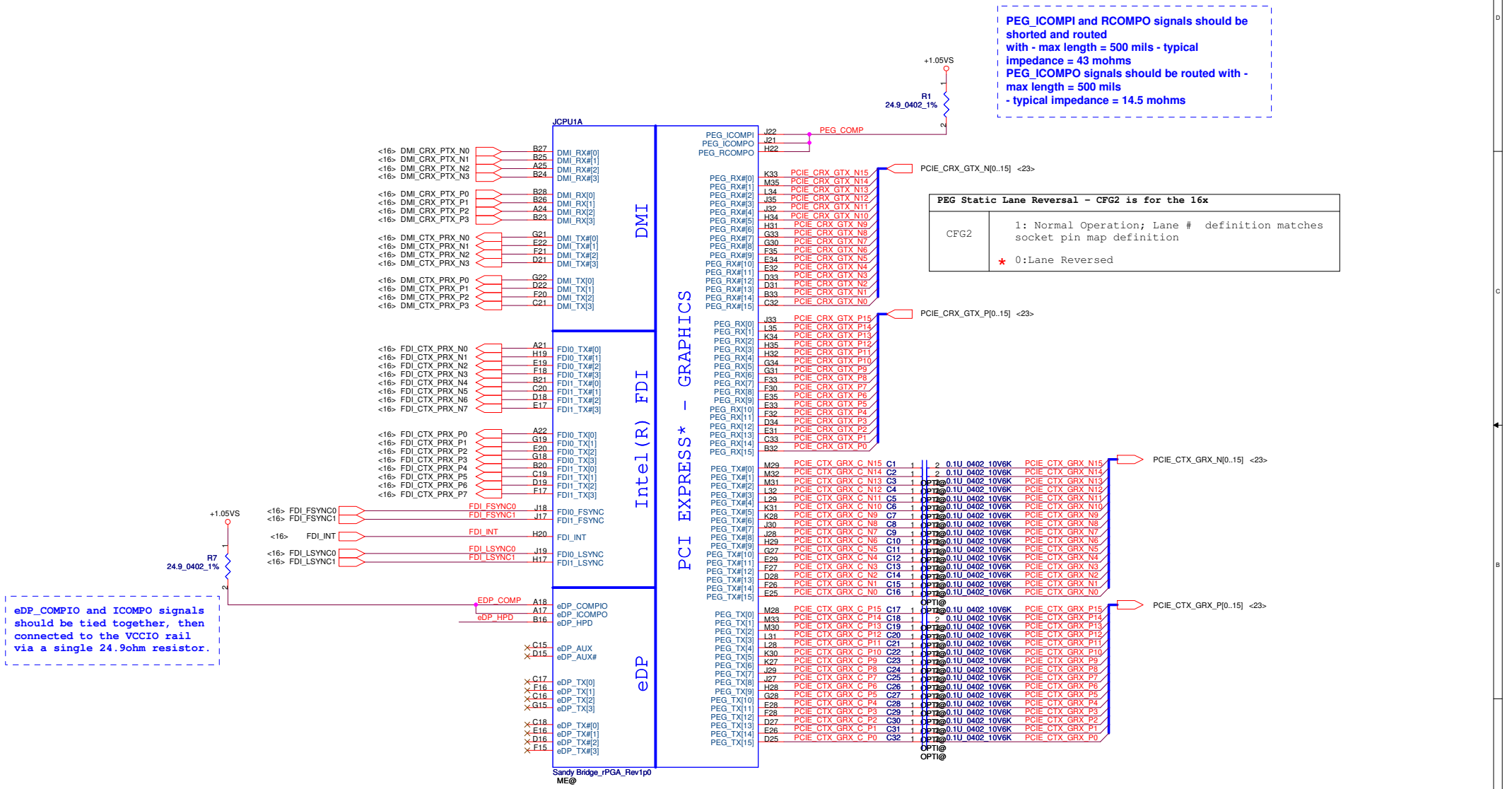

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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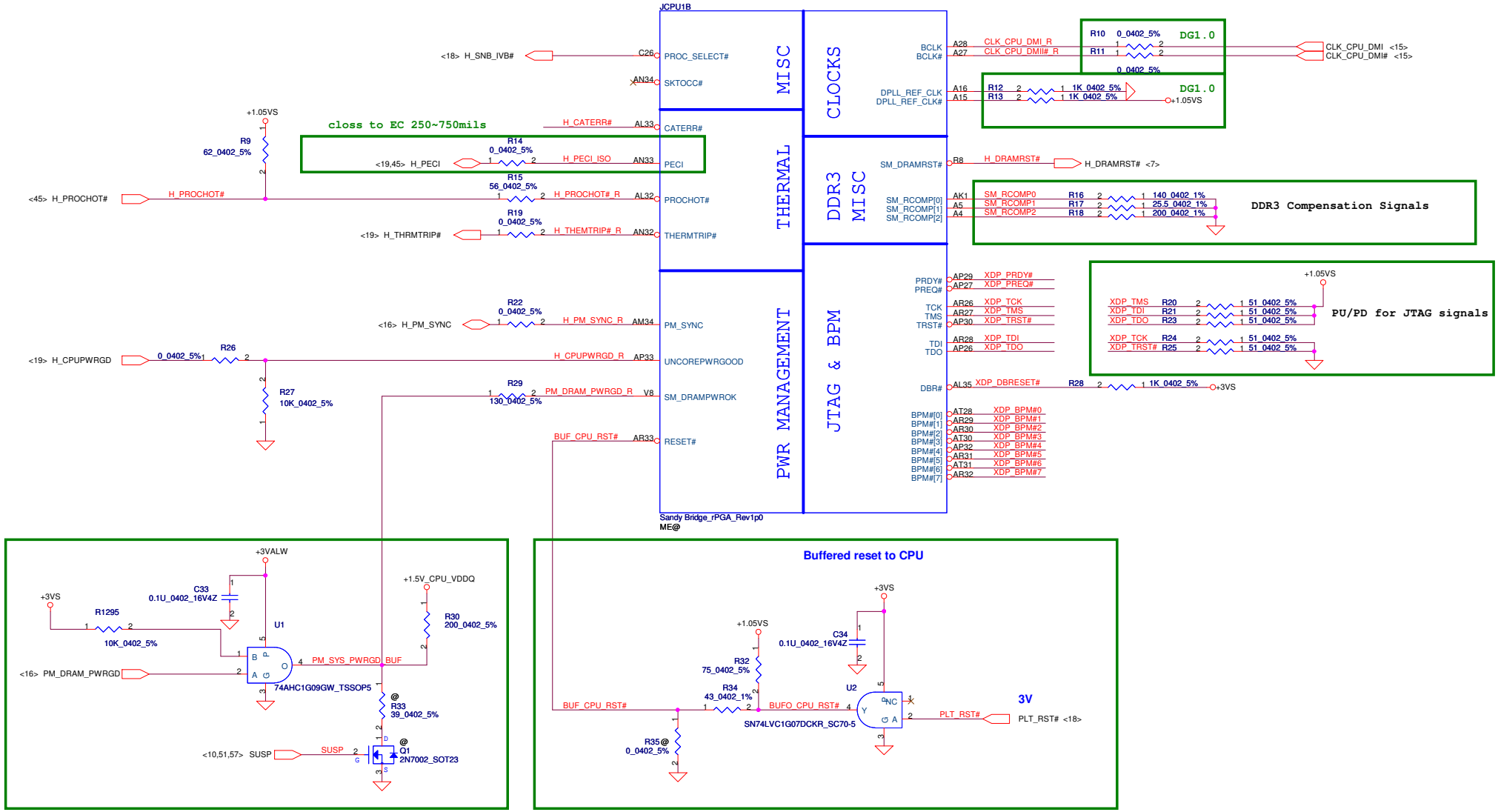

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Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: PIQY0 LA6881P		Rev: 0.3
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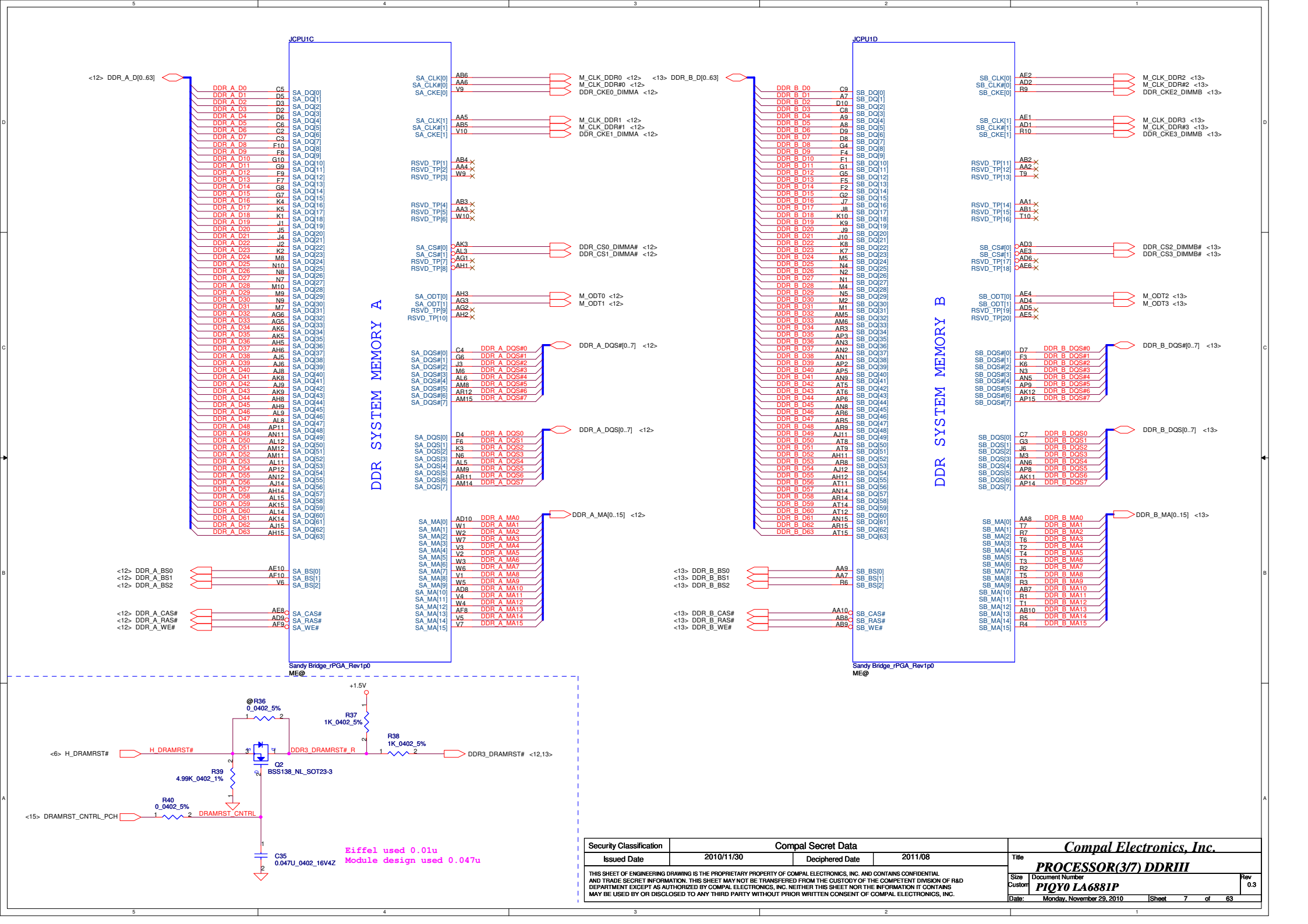

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Title: PROCESSOR(3/7) DDRIII

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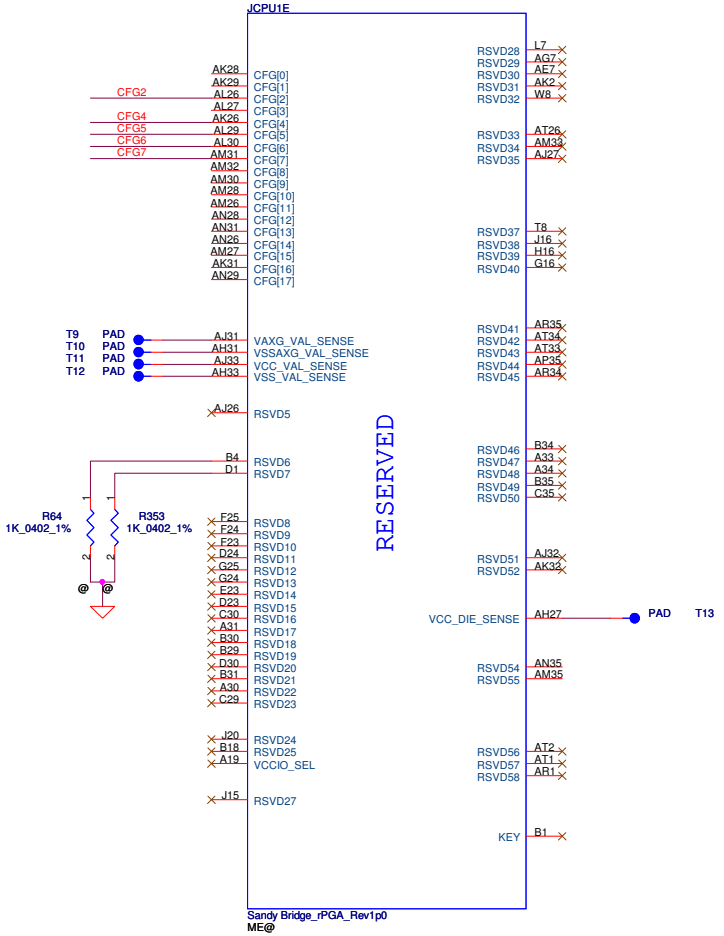
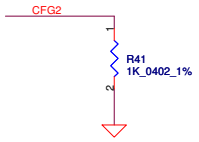
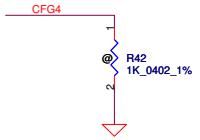
CFG Straps for Processor

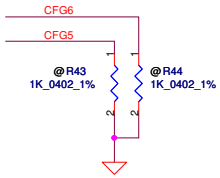




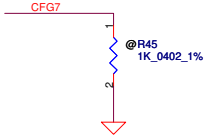
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

QC=94A
DC=53A

+CPU_CORE

(6/16 change 10uF_0603_6.3V)*5

C36 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C48 10U_0603_6.3V6M
C49 10U_0603_6.3V6M
C50 10U_0603_6.3V6M
C51 10U_0603_6.3V6M
C52 10U_0603_6.3V6M
C53 10U_0603_6.3V6M @

+CPU_CORE

(22uF_0805_6.3V)*16

C66 22U_0805_6.3V6M
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C70 22U_0805_6.3V6M
C71 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M
C81 22U_0805_6.3V6M
C82 22U_0805_6.3V6M
C83 22U_0805_6.3V6M
C84 22U_0805_6.3V6M
C85 22U_0805_6.3V6M @
C86 22U_0805_6.3V6M @
C87 22U_0805_6.3V6M @

+CPU_CORE

(330uF)*4

C88 330U_X_2VM_R6M
C89 330U_X_2VM_R6M
C90 330U_X_2VM_R6M
C91 330U_X_2VM_R6M

DUAL@ DUAL@ DUAL@ DUAL@

C88 470U_D2_2VM_R4.5M QUAD@
C89 470U_D2_2VM_R4.5M QUAD@
C90 470U_D2_2VM_R4.5M QUAD@
C91 470U_D2_2VM_R4.5M QUAD@

VCC1 AG35
VCC2 AG34
VCC3 AG33
VCC4 AG32
VCC5 AG31
VCC6 AG30
VCC7 AG29
VCC8 AG28
VCC9 AG27
VCC10 AG26
VCC11 AF35
VCC12 AF34
VCC13 AF33
VCC14 AF32
VCC15 AF31
VCC16 AF30
VCC17 AF29
VCC18 AF28
VCC19 AF27
VCC20 AF26
VCC21 AD35
VCC22 AD34
VCC23 AD33
VCC24 AD32
VCC25 AD31
VCC26 AD30
VCC27 AD29
VCC28 AD28
VCC29 AD27
VCC30 AD26
VCC31 AC35
VCC32 AC34
VCC33 AC33
VCC34 AC32
VCC35 AC31
VCC36 AC30
VCC37 AC29
VCC38 AC28
VCC39 AC27
VCC40 AC26
VCC41 AA35
VCC42 AA34
VCC43 AA33
VCC44 AA32
VCC45 AA31
VCC46 AA30
VCC47 AA29
VCC48 AA28
VCC49 AA27
VCC50 AA26
VCC51 Y35
VCC52 Y34
VCC53 Y33
VCC54 Y32
VCC55 Y31
VCC56 Y30
VCC57 Y29
VCC58 Y28
VCC59 Y27
VCC60 Y26
VCC61 V35
VCC62 V34
VCC63 V33
VCC64 V32
VCC65 V31
VCC66 V30
VCC67 V29
VCC68 V28
VCC69 V27
VCC70 V26
VCC71 U35
VCC72 U34
VCC73 U33
VCC74 U32
VCC75 U31
VCC76 U30
VCC77 U29
VCC78 U28
VCC79 U27
VCC80 U26
VCC81 R35
VCC82 R34
VCC83 R33
VCC84 R32
VCC85 R31
VCC86 R30
VCC87 R29
VCC88 R28
VCC89 R27
VCC90 R26
VCC91 P35
VCC92 P34
VCC93 P33
VCC94 P32
VCC95 P31
VCC96 P30
VCC97 P29
VCC98 P28
VCC99 P27
VCC100 P26

Sandy Bridge_rPGA_Rev1p0
ME@

PEG AND DDR

Cap quantity follow HR_PDDG_Rev07
22uF*7 NO-STUFF

18A

(22uF_0805_6.3V)*13

+1.05VS

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C41 C42 C43 C44 C54 C45 C46 C55 C56 C47 22U_0805_6.3V6M
C57 C58 C59 @ C60 @ C61 @ C62 @ C63 @ C64 @ C65 @ 22U_0805_6.3V6M

C922 330U_2.5V_M @
C69 330U_D2_2.5VY_R9M
C72 330U_D2_2.5VY_R9M @
C918 330U_2.5V_M

CORE SUPPLY

SVID

+1.05VS

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5% VR_SVID_ALRT# <60>
VIDSCLK AJ30 H_CPU_SVIDCLK R48 0_0402_5% VR_SVID_CLK <60>
VIDSOUT AJ28 H_CPU_SVIDDAT R49 0_0402_5% VR_SVID_DAT <60>

R50 130_0402_5% +1.05VS

SENSE LINES

8/11 update: Add R1309, R1310.
PDDG1.21#439028

+CPU_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R52 0_0402_5% VCCSENSE <60>
VSS_SENSE AJ34 VSSSENSE_R R53 0_0402_5% VSSSENSE <60>

+1.05VS R1313 10_0402_1%

VCCIO_SENSE B10 VCCIO_SENSE <58>
VSSIO_SENSE A10 VSSIO_SENSE

R1314 10_0402_1%

R54 100_0402_1%

@ R1309 27.4_0402_1%
R1310 27.4_0402_1%

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Title: PROCESSOR(5/7) PWR,BYPASS

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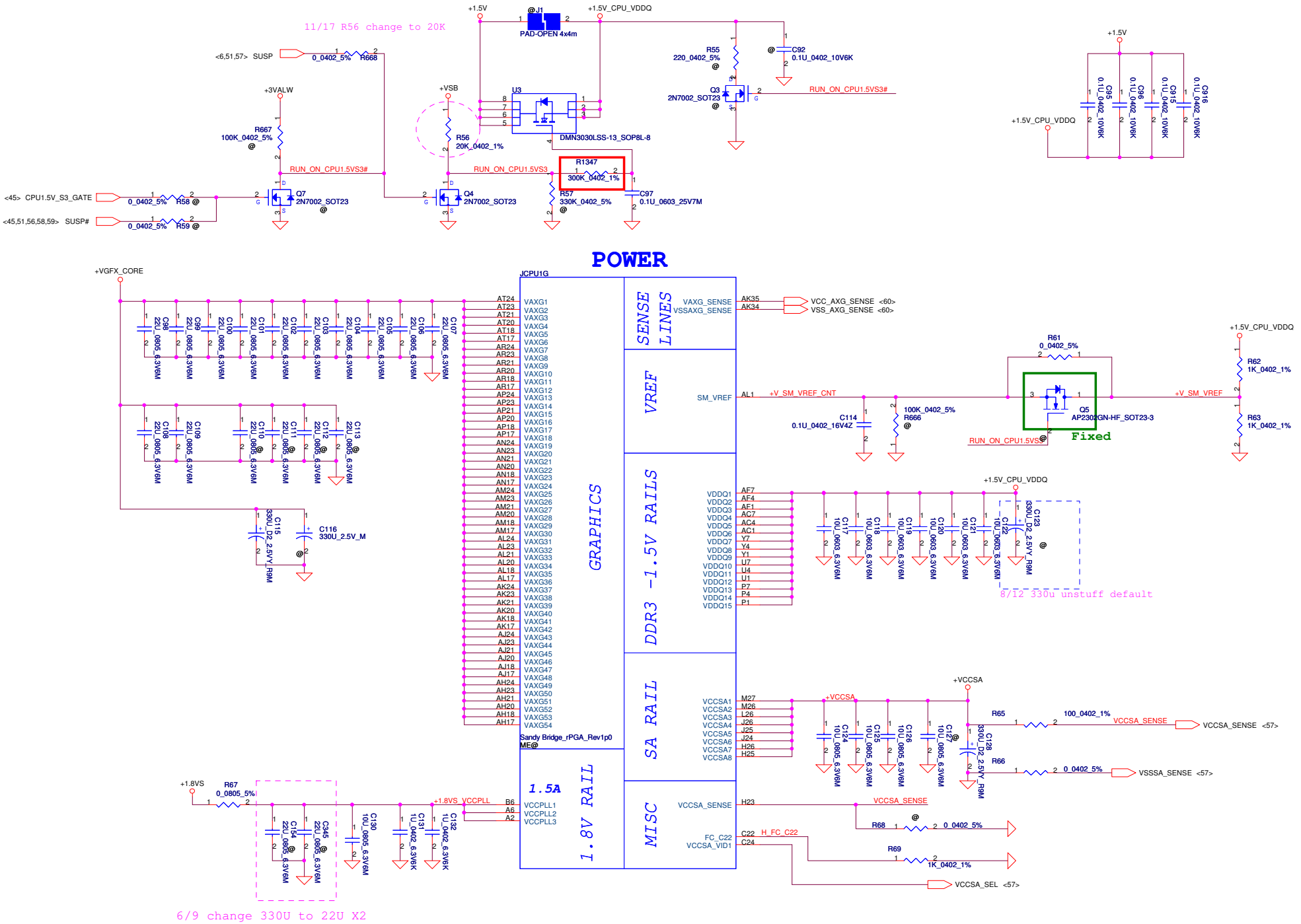

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Title: **PROCESSOR(6/7) PWR**

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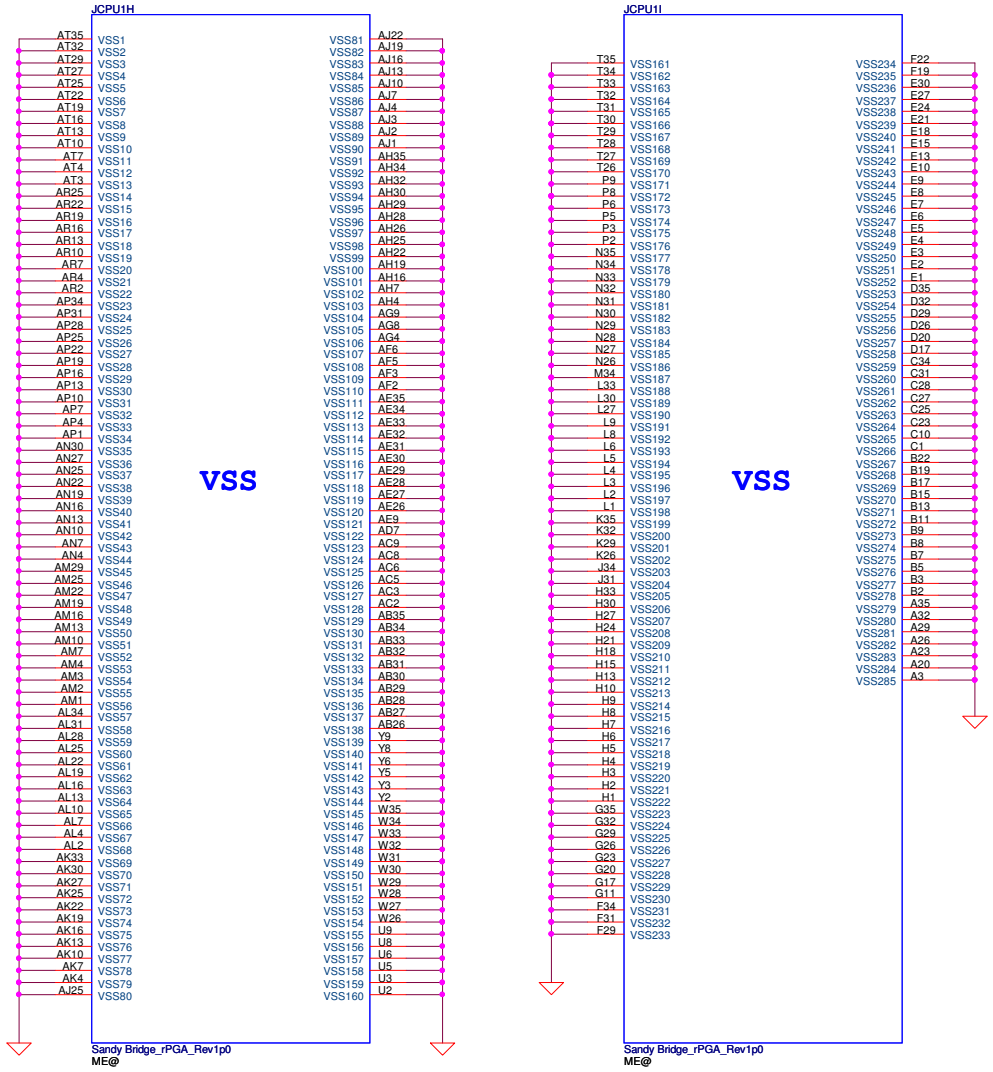

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Title: PROCESSOR(7/7) VSS

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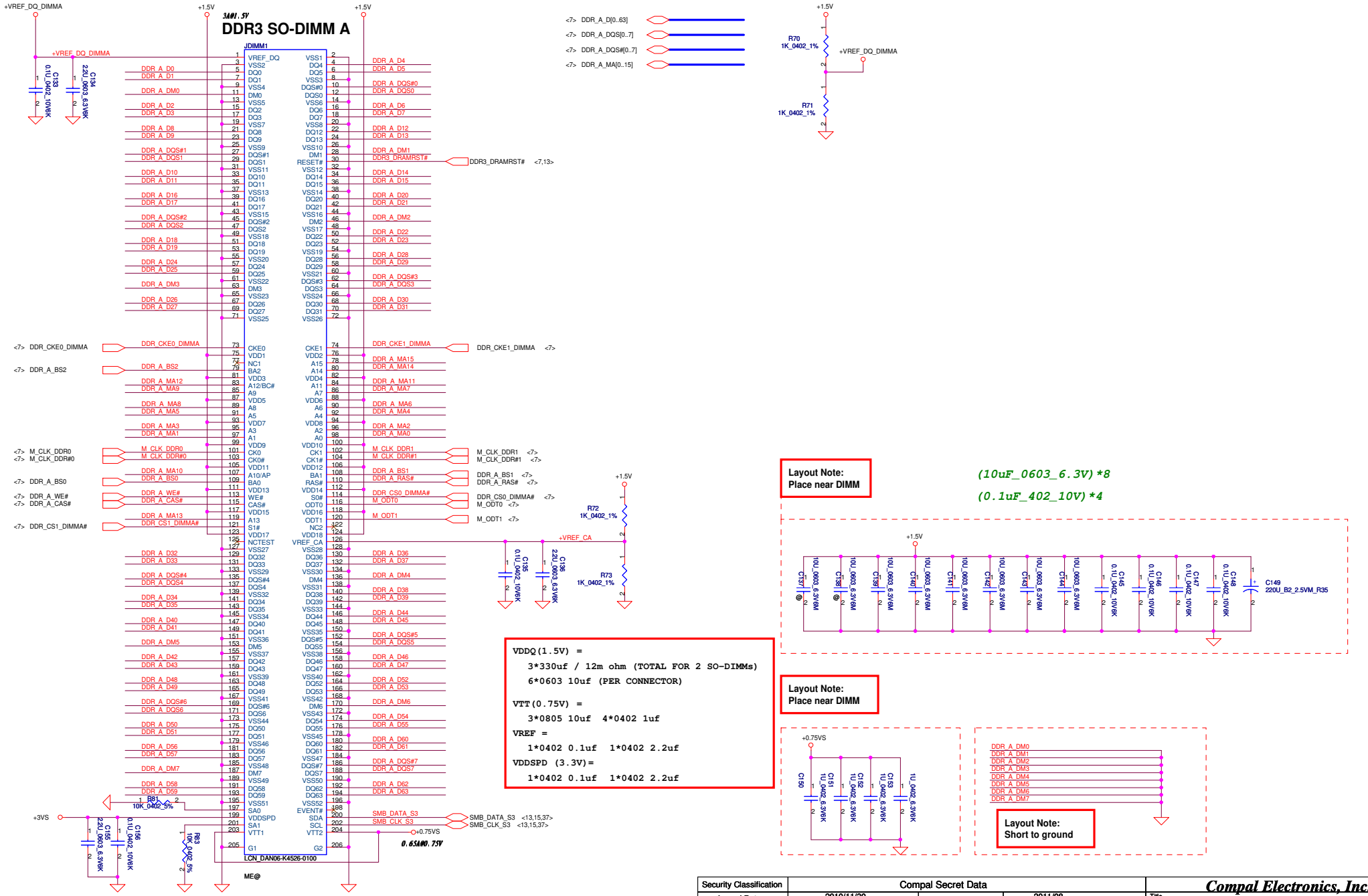

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Title: **DDRIII-SODIMM SLOT1**

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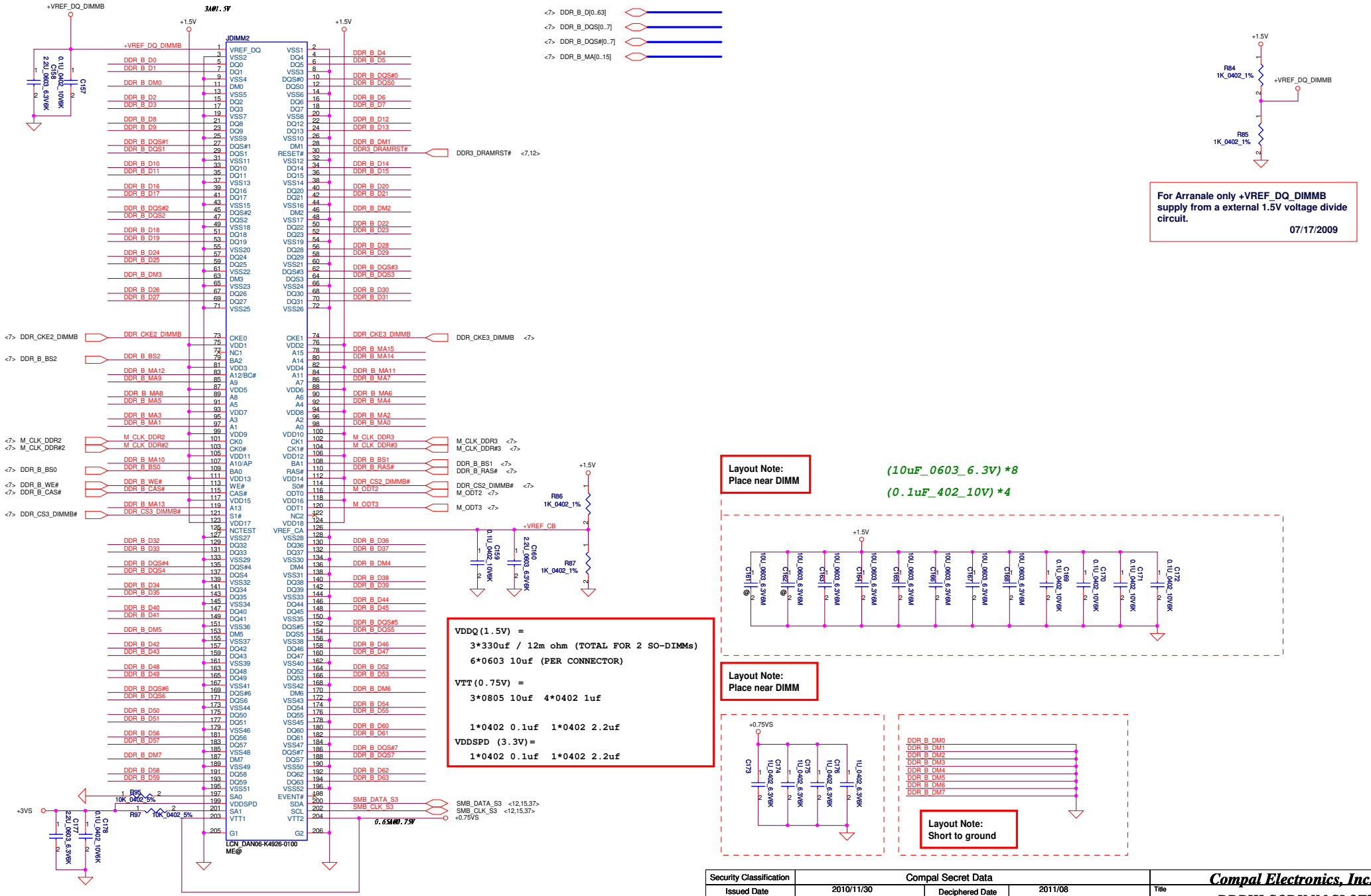

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Title: DDRIII-SODIMM SLOT2

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W=20mils
+RTCVCC
R99 1K_0402_5%
C179 1U_0603_10V4Z
W=20mils
+RTCBATT
CLRP1 SHORT PADS

+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
R1330 330K_0402_5%
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R105 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)
* LOW= Disable (Default)

+3VALW
R106 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3VALW
R108 <BOM Structure> HDA_SYNC
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
* 1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

<42> HDA_BITCLK_AUDIO R112 33_0402_5% HDA_BIT_CLK
<42> HDA_SYNC_AUDIO R114 33_0402_5% HDA_SYNC_R
<42> HDA_RST_AUDIO# R116 33_0402_5% <BOM Structure> HDA_RST#
<42> HDA_SDOUT_AUDIO R118 33_0402_5% <BOM Structure> HDA_SDOUT

+3VALW
R121 200_0402_5% PCH_JTAG_TDO
R122 200_0402_5% PCH_JTAG_TMS
R123 200_0402_5% PCH_JTAG_TDI
<BOM Structure> R125 100_0402_1%
R126 100_0402_1%
R128 100_0402_1%
DPDG1.1

6/30 update R121, R122, R123

+3VS
Q10 BSS138_NL_SOT23-3
HDA_SYNC
@R325 0_0402_5%

6/17 follow module design

PCH_RTCX1
R98 10M_0402_5%
PCH_RTCX2
Y1 32.768KHZ_12.5PF_9H03200413
C180 15P_0402_50V8J
C181 <BOM Structure> 15P_0402_50V8J
CMOS

+RTCVCC
C183 1U_0603_10V4Z
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0603_10V4Z
CLRP2 SHORT PADS
CLRP3 SHORT PADS

PCH_RTCX1 A20
PCH_RTCX2 C20
PCH_RTCRST# D20
PCH_SRTCRST# G22
SM_INTRUDER# K22
PCH_INTVRMEN C17
HDA_BIT_CLK N34
HDA_SYNC L34
<42> HDA_SPKR HDA_SPKR T10
HDA_RST# K34
<42> HDA_SDIN0 HDA_SDIN0 E34
HDA_SDIN1 G34
HDA_SDIN2 C34
HDA_SDIN3 A34
<45> ME_FLASH R109 0_0402_5% HDA_SDOUT A36
R107 1K_0402_1% PCH_GPIO33 C36
<46> Kill_SW# Kill_SW# N32
R110 51_0402_5%
PCH_JTAG_TCK J3
PCH_JTAG_TMS H7
PCH_JTAG_TDI K5
PCH_JTAG_TDO H1
SPI_CLK_PCH T3
SPI_SB_CS0# Y14
T1
SPI_SI V4
SPI_SO_R U3

U4A
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
COUGARPOINT_FCBGA989

RTC
HDA
JTAG
SPI

LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
LPC_AD0 <37,45>
LPC_AD1 <37,45>
LPC_AD2 <37,45>
LPC_AD3 <37,45>
EC and Mini card debug port
FWH4 / LFRAME# D36 LPC_FRAME#
LPC_FRAME# <37,45>
LDRQ0# E36
LDRQ1# / GPIO23 K36
R104 10K_0402_5% +3VS
SERIRQ V5 SERIRQ
SERIRQ <45>

SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7 SATA_ITX_C_DRX_N0 0.01U_0402_16V7K C184 SATA_ITX_DRX_N0
SATA0TXP AP5 SATA_ITX_C_DRX_P0 0.01U_0402_16V7K C185 SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0 <37>
SATA_DTX_C_IRX_P0 <37>
SATA_ITX_DRX_N0 <37>
SATA_ITX_DRX_P0 <37>
SSD

SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11 SATA_ITX_C_DRX_N1 0.01U_0402_16V7K C273 SATA_ITX_DRX_N1
SATA1TXP AP10 SATA_ITX_C_DRX_P1 0.01U_0402_16V7K C272 SATA_ITX_DRX_P1
SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_DTX_C_IRX_N1 <41>
SATA_DTX_C_IRX_P1 <41>
SATA_ITX_DRX_N1 <41>
SATA_ITX_DRX_P1 <41>
HDD

SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5 SATA_ITX_C_DRX_N2 0.01U_0402_16V7K C186 SATA_ITX_DRX_N2_CONN
SATA2TXP AH4 SATA_ITX_C_DRX_P2 0.01U_0402_16V7K C187 SATA_ITX_DRX_P2_CONN
SATA_DTX_C_IRX_N2
SATA_DTX_C_IRX_P2
SATA_DTX_C_IRX_N2 <41>
SATA_DTX_C_IRX_P2 <41>
SATA_ITX_DRX_N2_CONN <41>
SATA_ITX_DRX_P2_CONN <41>
ODD

SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1

SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3 SATA_ITX_C_DRX_N4 0.01U_0402_16V7K C188 SATA_ITX_DRX_N4
SATA4TXP AD1 SATA_ITX_C_DRX_P4 0.01U_0402_16V7K C189 SATA_ITX_DRX_P4
ESATA@
SATA_DTX_C_IRX_N4
SATA_DTX_C_IRX_P4
SATA_DTX_C_IRX_N4 <48>
SATA_DTX_C_IRX_P4 <48>
SATA_ITX_DRX_N4 <48>
SATA_ITX_DRX_P4 <48>
ESATA

SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11
R111 37.4_0402_1% +1.05VS_VCC_SATA
SATAICOMPI Y10 SATA_COMP
SATA3RCOMPO AB12
R113 49.9_0402_1% +1.05VS_SATA3
SATA3COMPI AB13 SATA3_COMP
SATA3RBIAS AH1 RBIAS_SATA3 R115 750_0402_1%

SATALED# P3 HDD_LED#
R117 10K_0402_5% +3VS
HDD_LED# <50>
SATA0GP / GPIO21 V14 PCH_GPIO21
R119 10K_0402_5% +3VS
SATA1GP / GPIO19 P1 SATA_DET#
SATA_DET# <37>
R316 10K_0402_5% +3VS

4MB SPI ROM FOR ME
& Non-share ROM.

+3VS
R127 3.3K_0402_5% SPI_WP#_0
R129 3.3K_0402_5% SPI_HOLD#_0
R130 0_0402_5%
SPI_SB_CS0#
SPI_SO_R
33_0402_5% R131
U5
CS# SO WP# GND
VCC HOLD# SCLK SI
SPI_SB_CS0#_R
SPI_SO_L0
SPI_WP#_0
SPI_HOLD#_0
SPI_CLK_PCH_0
SPI_SI_R0
S IC FL 32M W25Q32BVSSIG SOIC 8P
+3VS
C191 0.1U_0402_16V4Z
R1336 0_0402_5%
SPI_CLK_PCH
SPI_SI
33_0402_5% R133
SPI_CLK_PCH
R124 33_0402_5% @
C190 22P_0402_50V8J @

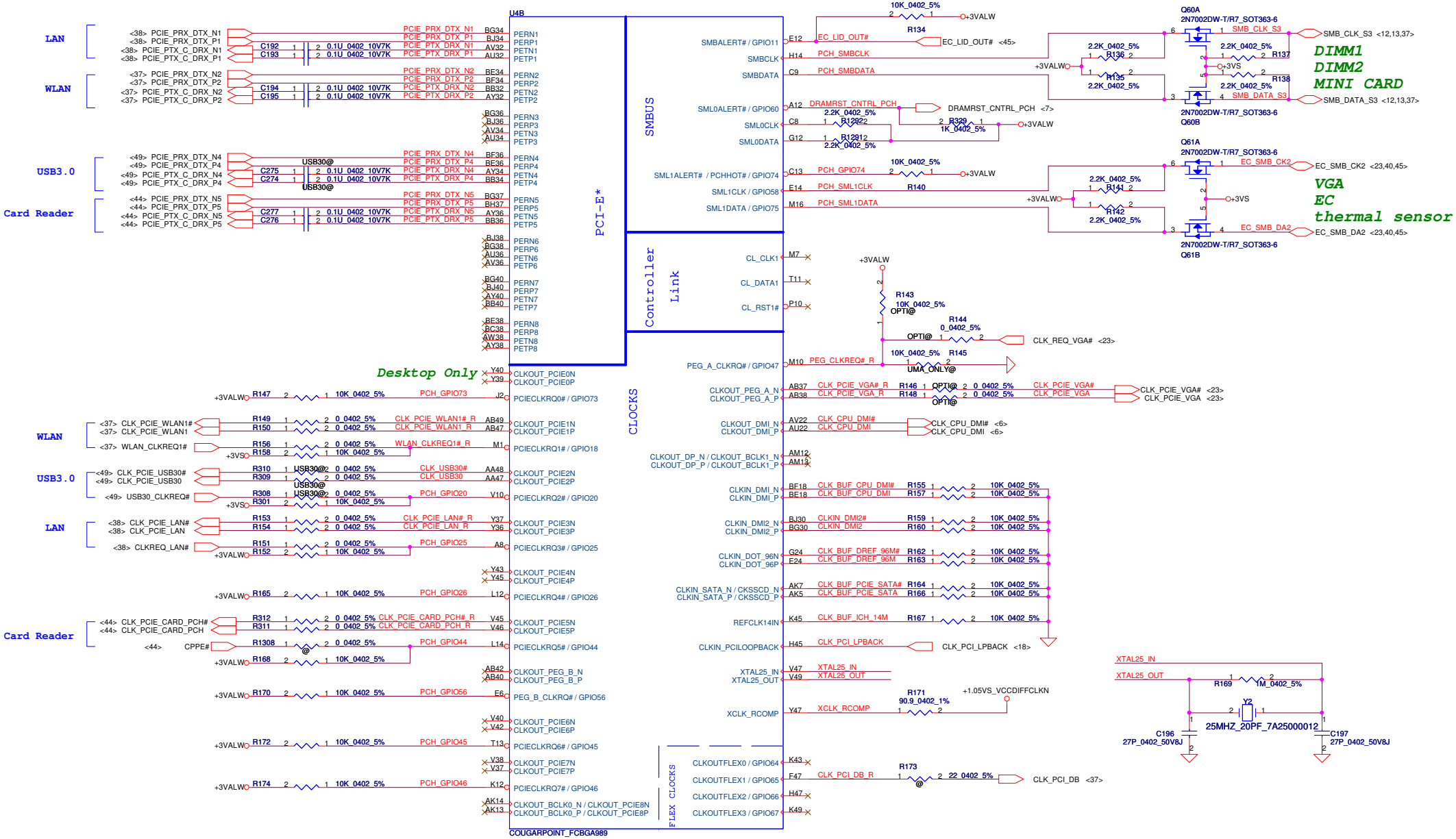
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 14 of 63



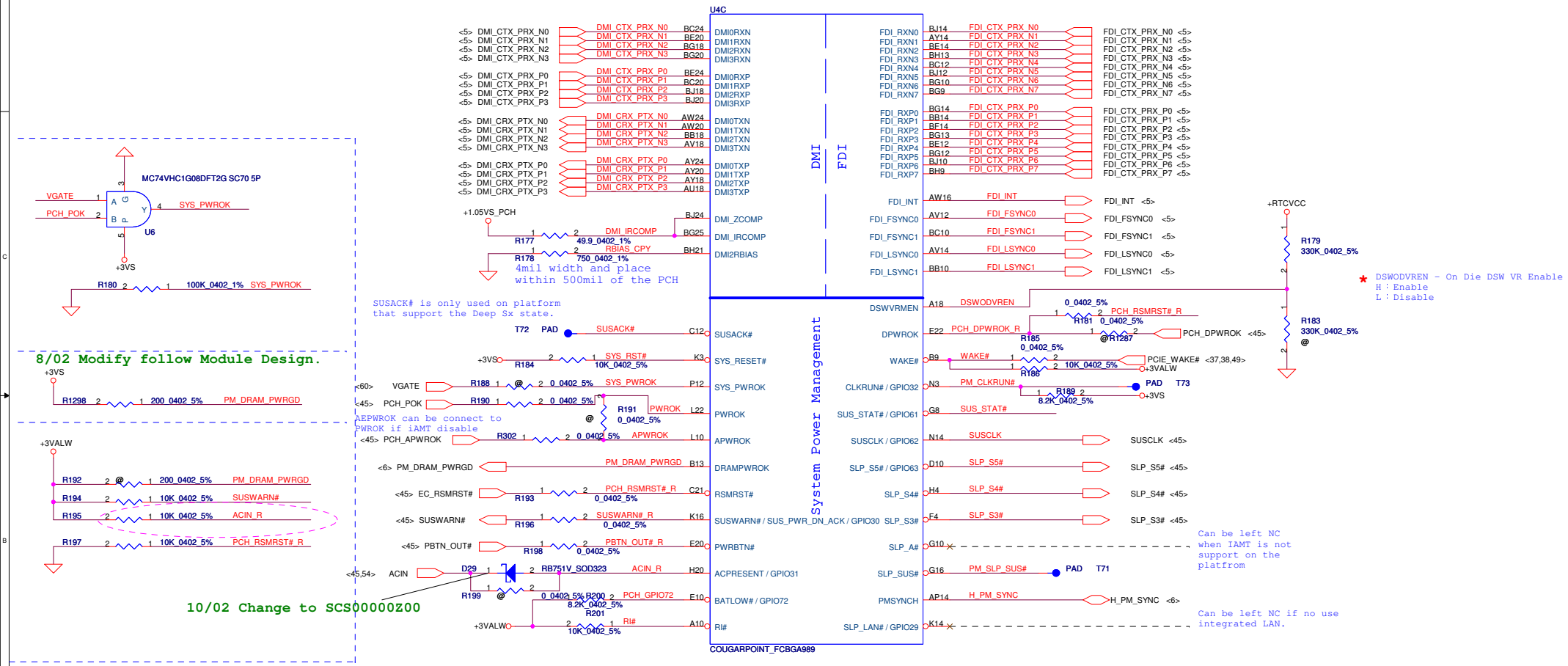
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

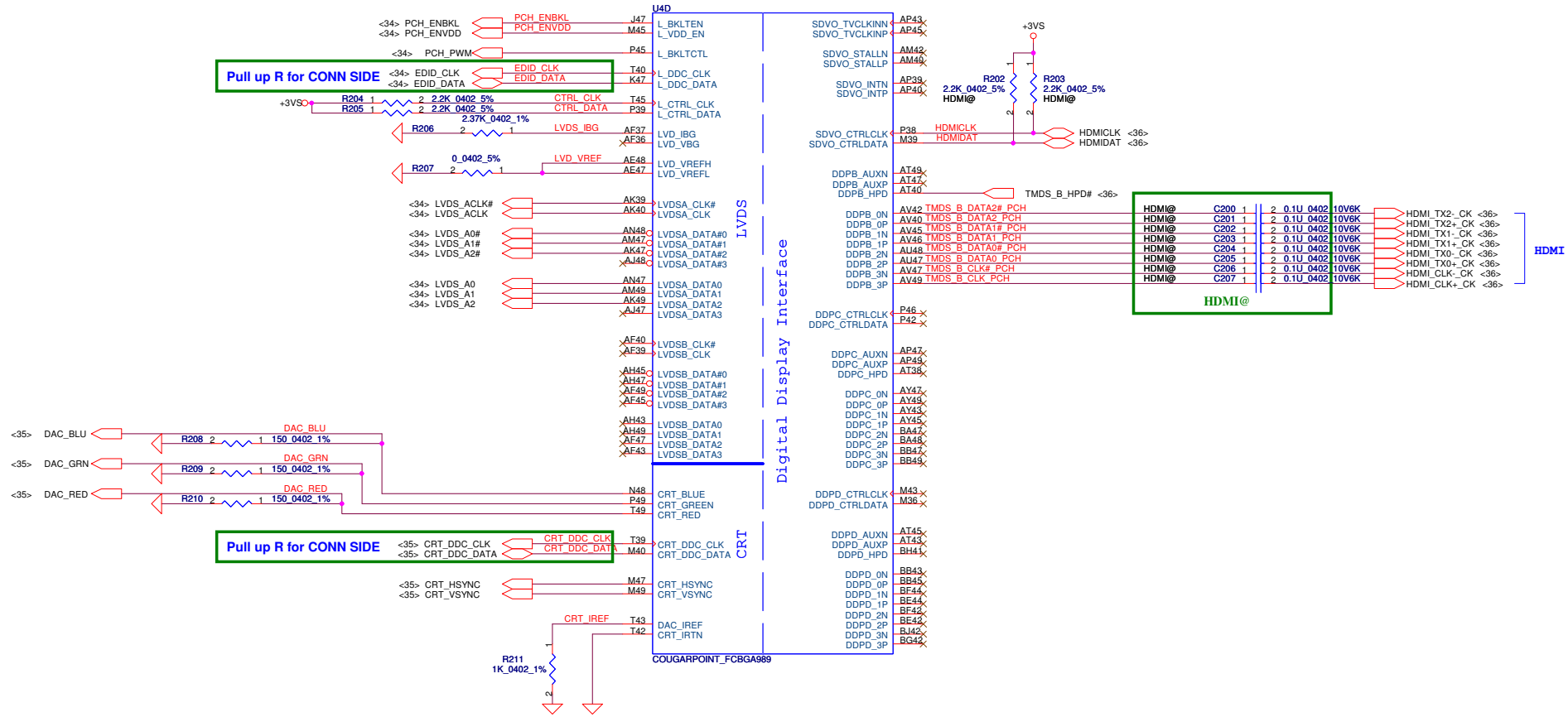
Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 15 of 63



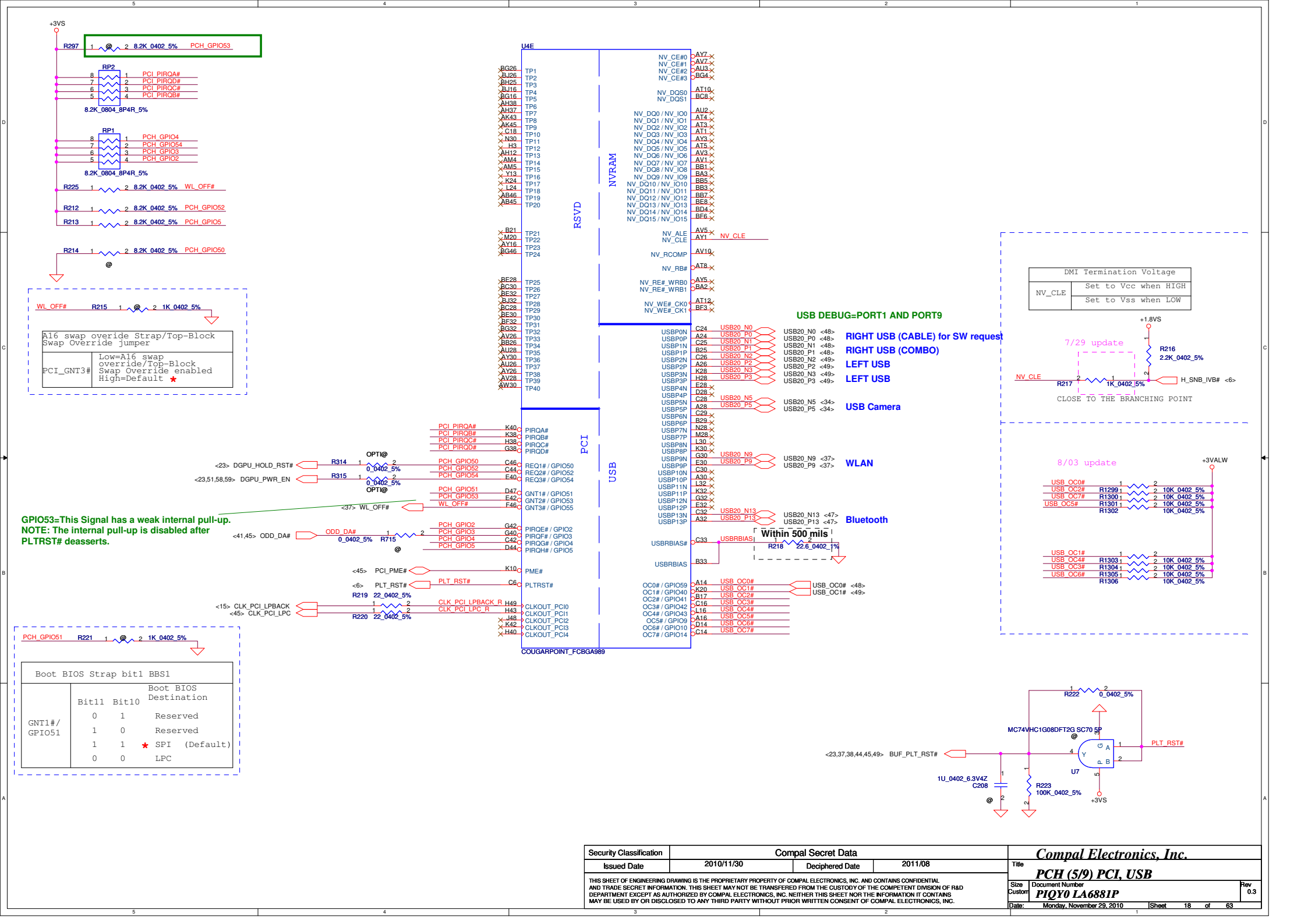
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title	PCH (3/8) DMI,FDI,PM,		
Size: Custom	Document Number: PIQY0 LA6881P		Rev: 0.3
Date: Monday, November 29, 2010	Sheet 16 of 63		



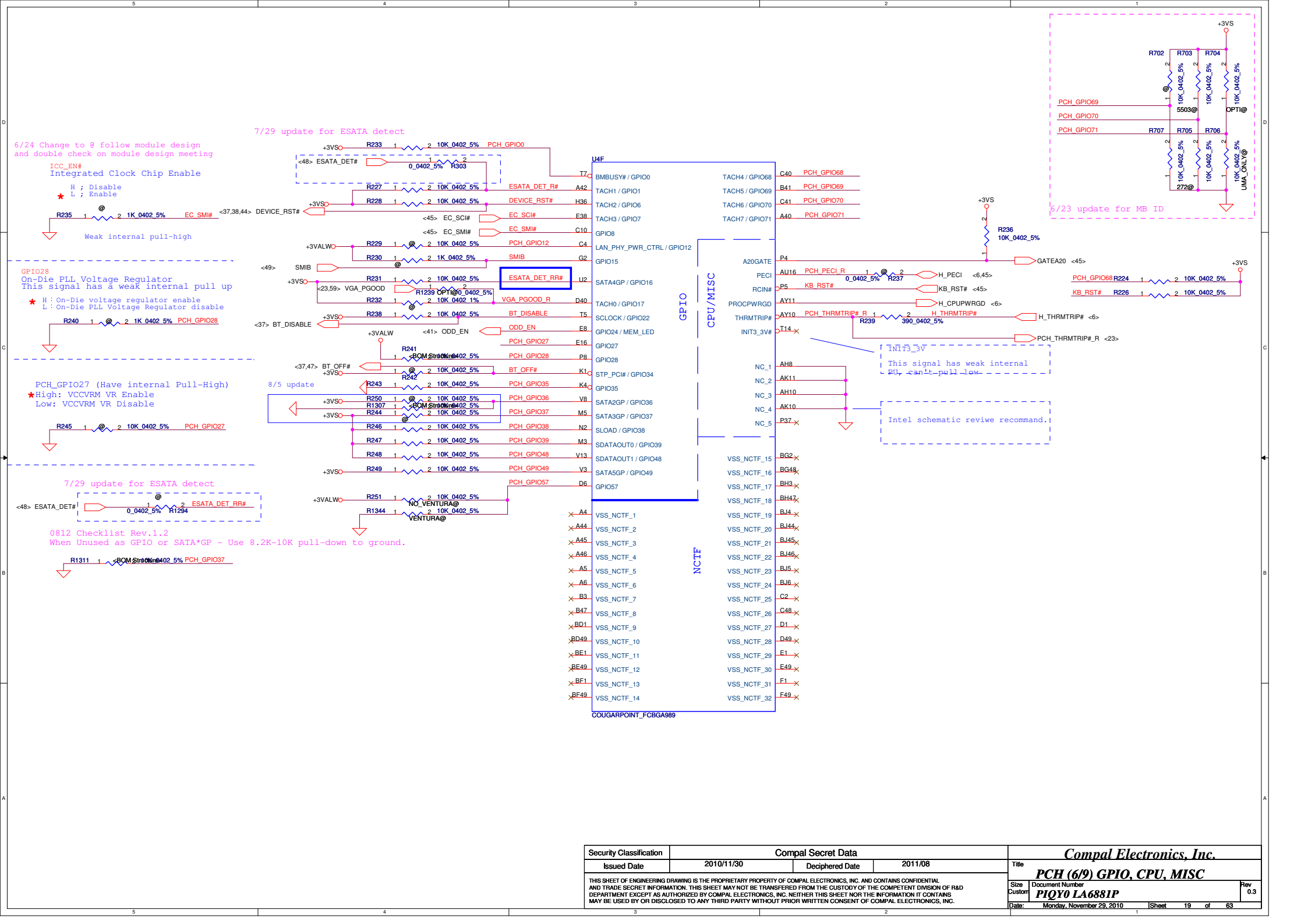
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.		
Title: PCH (4/9) LVDS,CRT,DP,HDMI		
Size: Custom	Document Number: PIQY0 LA6881P	Rev: 0.3
Date: Monday, November 29, 2010	Sheet 17 of 63	



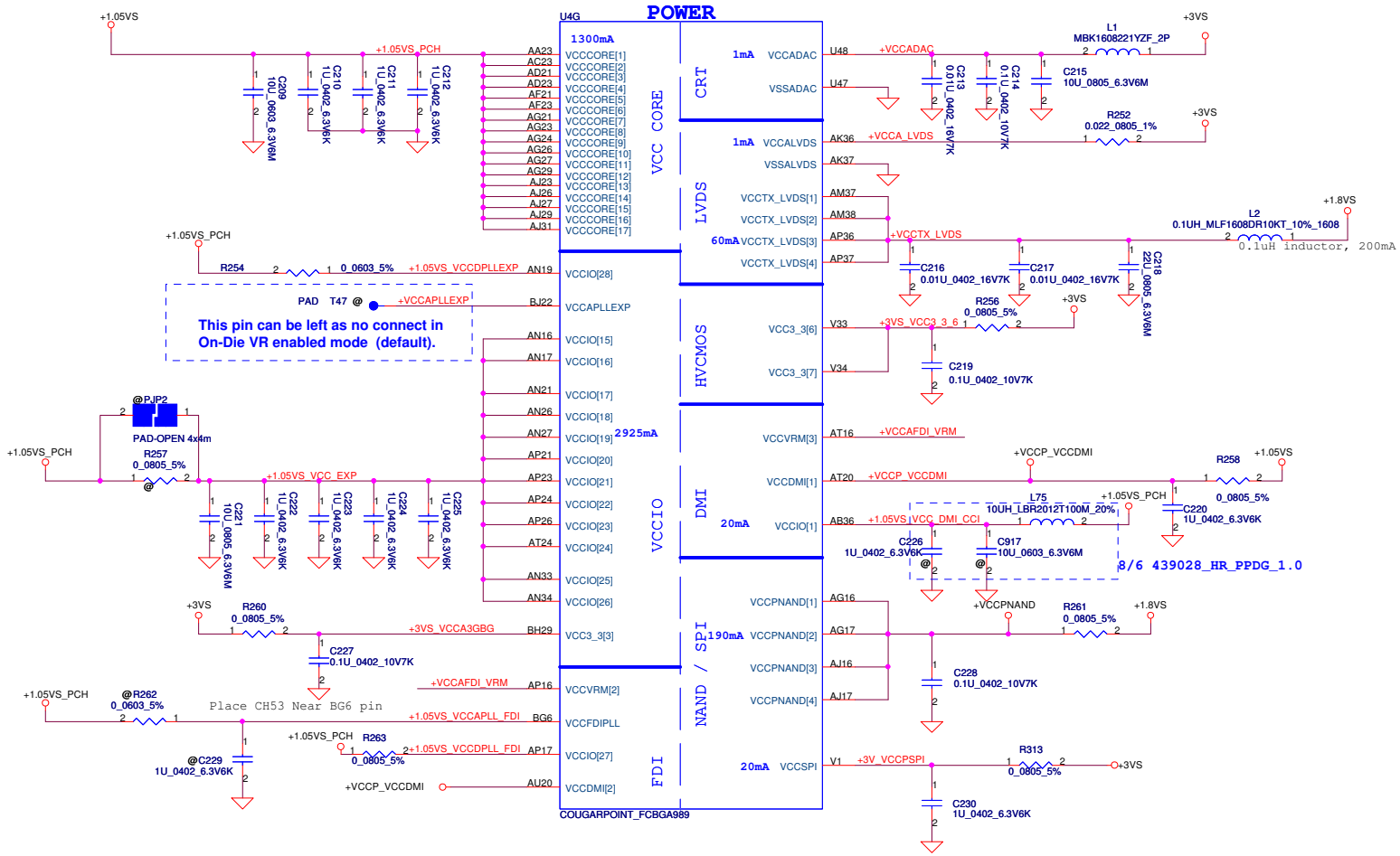
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title	PCH (5/9) PCI, USB		
Size	Document Number		Rev
Custom	PIQY0 LA6881P		0.3
Date:	Monday, November 29, 2010	Sheet	18 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title: PCH (6/9) GPIO, CPU, MISC			
Size: Custom	Document Number: PIQY0 LA6881P		Rev: 0.3
Date: Monday, November 29, 2010	Sheet 19 of 63		



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Intel HR_PDDG_1.21
1.5S rail. Default is to poppulate to enable VccVRM.

VCCVRM = 160mA detal waiting for newest spec

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 0.3

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

11/25 0ohm deleted.

10/02 Change to SCS00000Z00.

Place CH80 Near AK1 pin

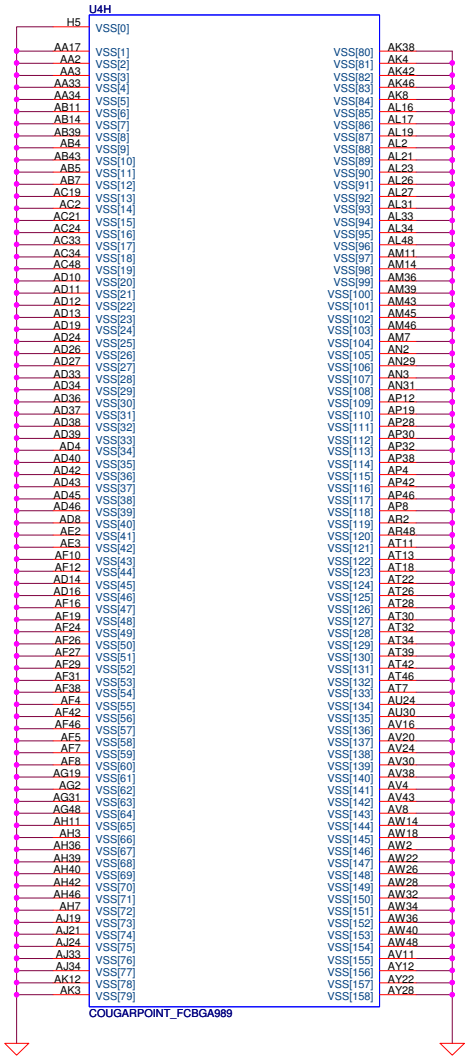
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

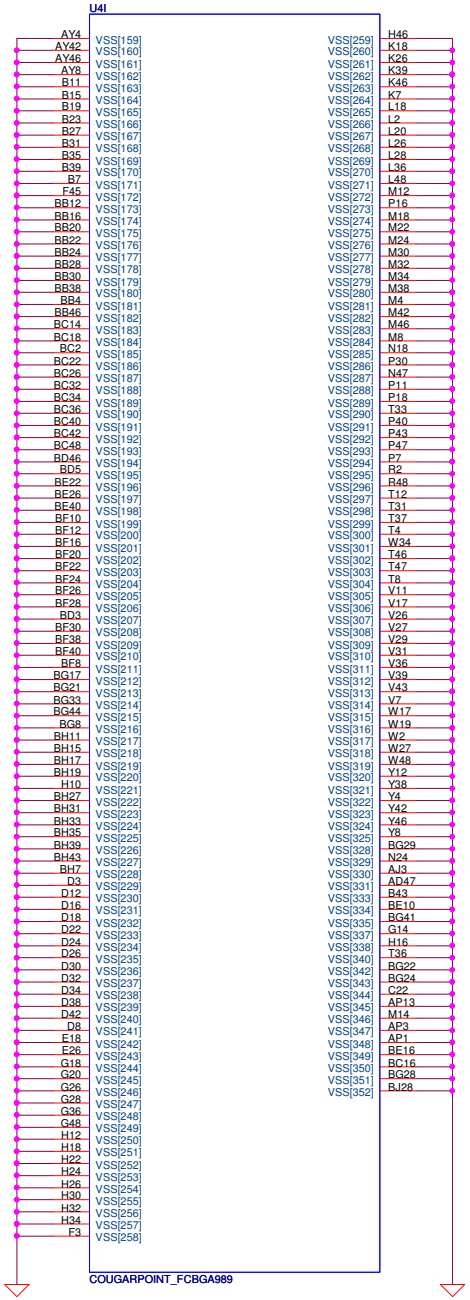
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 0.3

Date: Monday, November 29, 2010 | Sheet 21 of 63





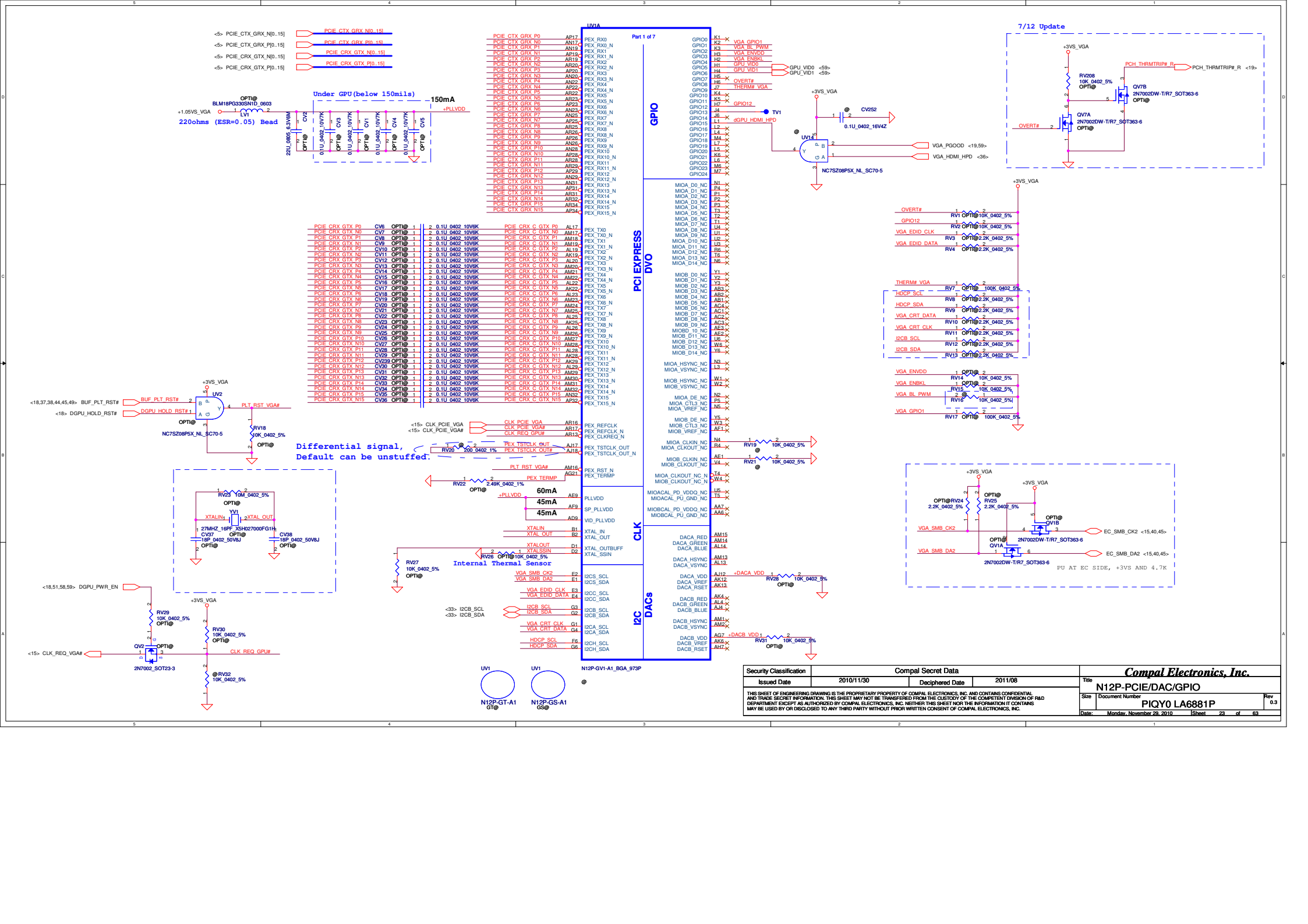
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 0.3

Date: Monday, November 29, 2010 | Sheet 22 of 63


7/12 Update
UV1A
Part 1 of 7
GPIO
PCI EXPRESS DVO
CLK
I2C DACs
N12P-GV1-A1_BGA_973P
Under GPU(below 150mils)
150mA
220ohms (ESR=0.05) Bead
Differential signal,
Default can be unstuffed.
Internal Thermal Sensor
60mA
45mA
45mA
PU AT EC SIDE, +3VS AND 4.7K
Security Classification
Compal Secret Data
Issued Date
2010/11/30
Deciphered Date
2011/08
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Compal Electronics, Inc.
Title
N12P-PCIE/DAC/GPIO
Size
Document Number
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Rev
0.3
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23
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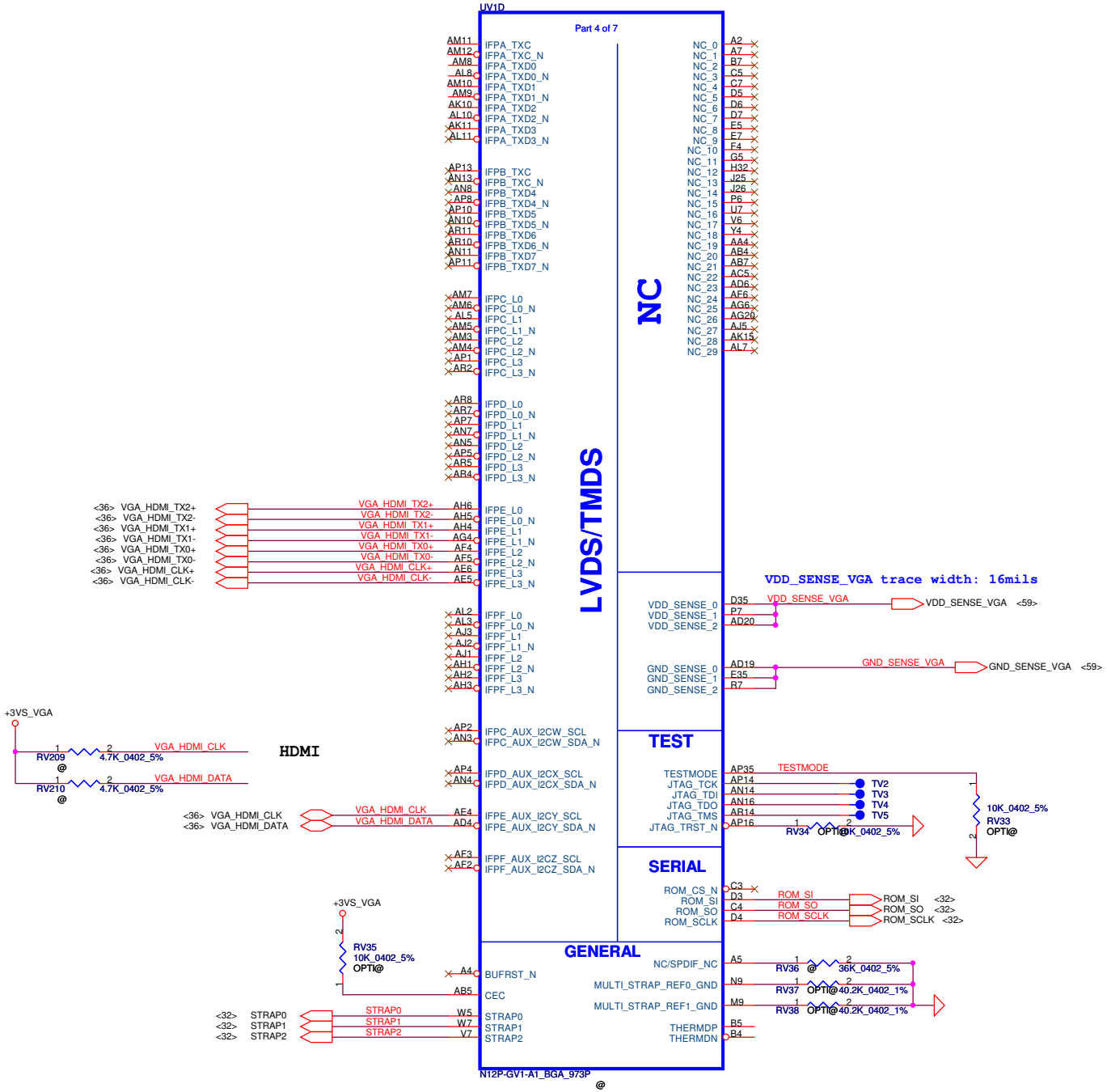
63



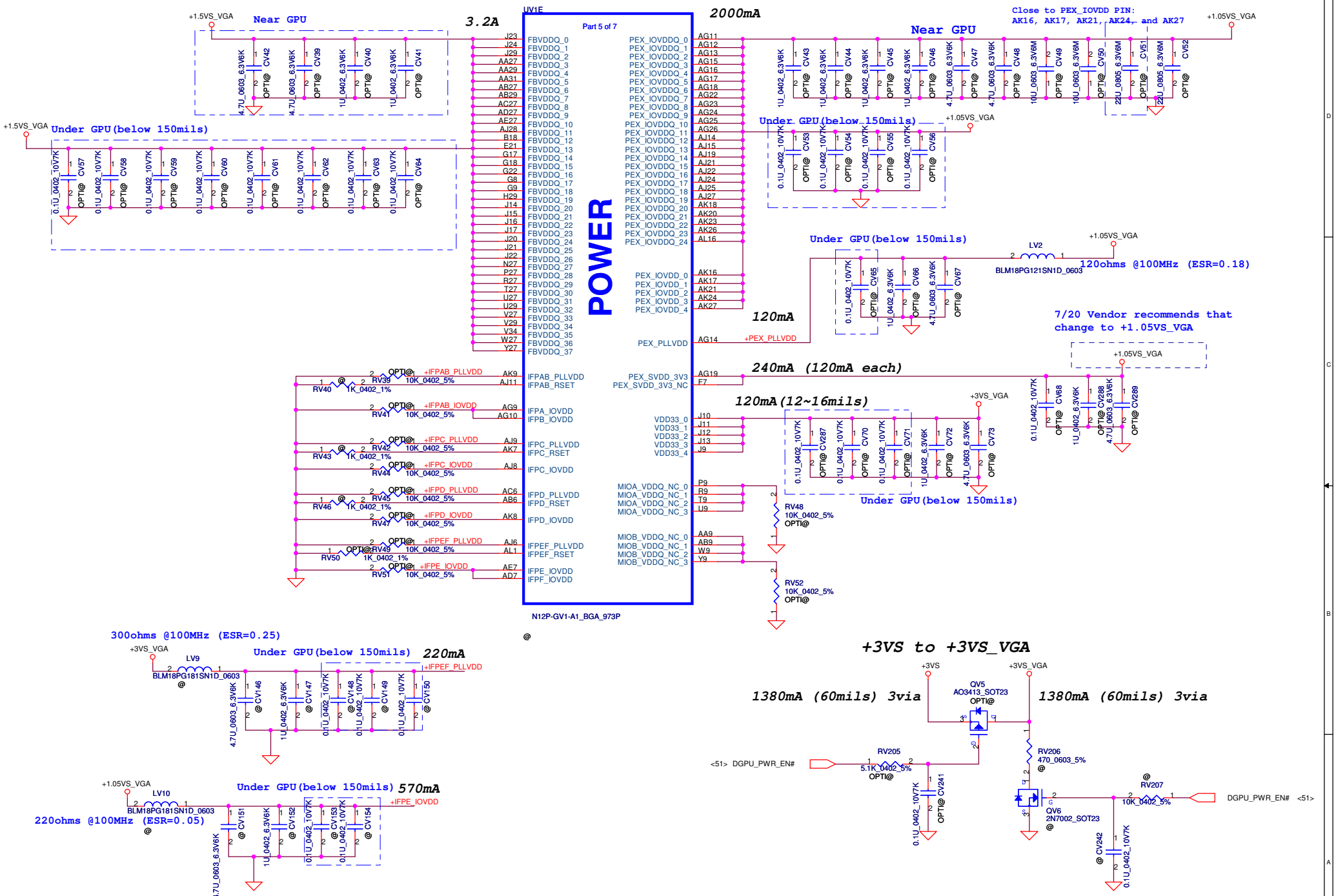
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: N12P-LVDS/HDMI/DP/THM

Size	Document Number	Rev
	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 24 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: N12P-POWER

Size: | Document Number: PIQY0 LA6881P | Rev: 0.3

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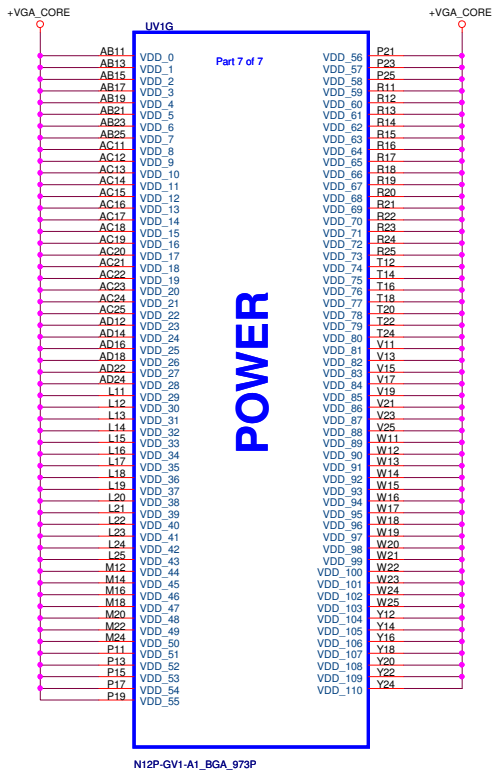
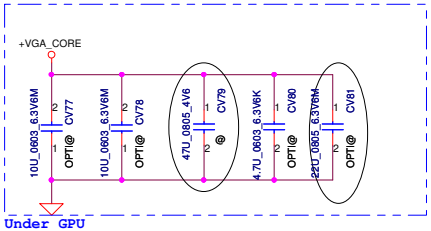
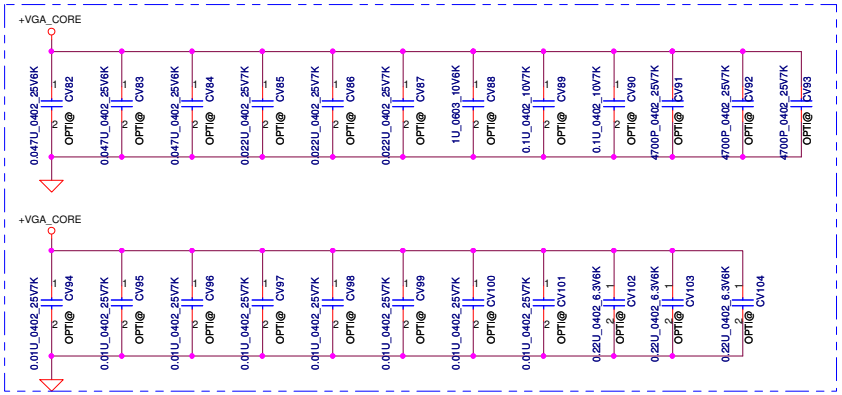
30.54A (41.02A Peak)

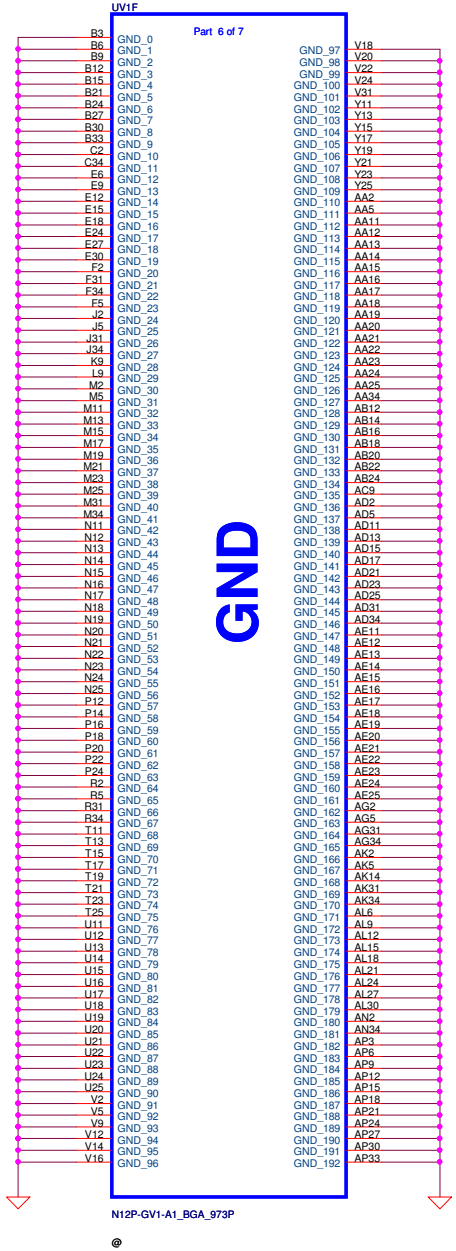


Near GPU



Under GPU





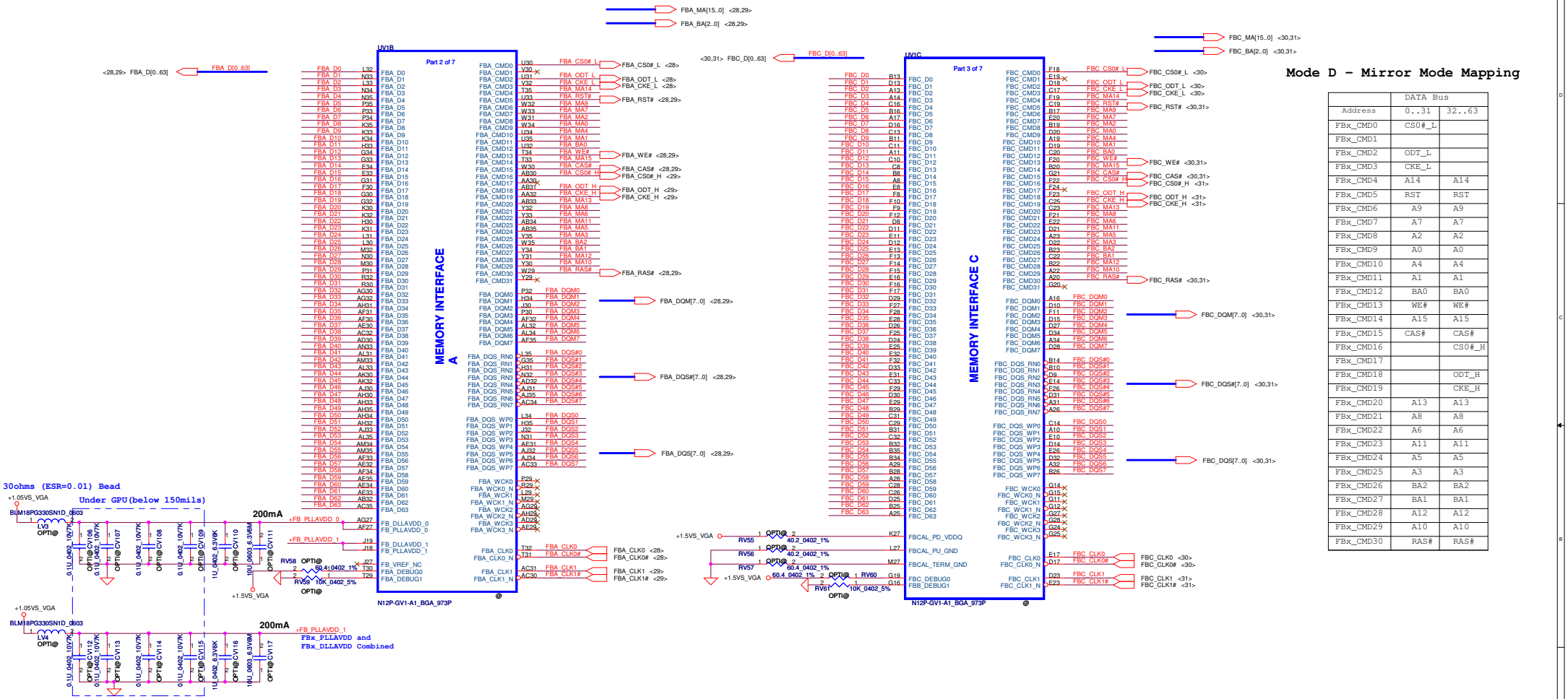
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: N12P-VGA CORE, GND

Size	Document Number	Rev
	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 | Sheet 26 of 63



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: N12P-MEM Interface

Size: | Document Number: PIQY0 LA6881P | Rev: 0.3

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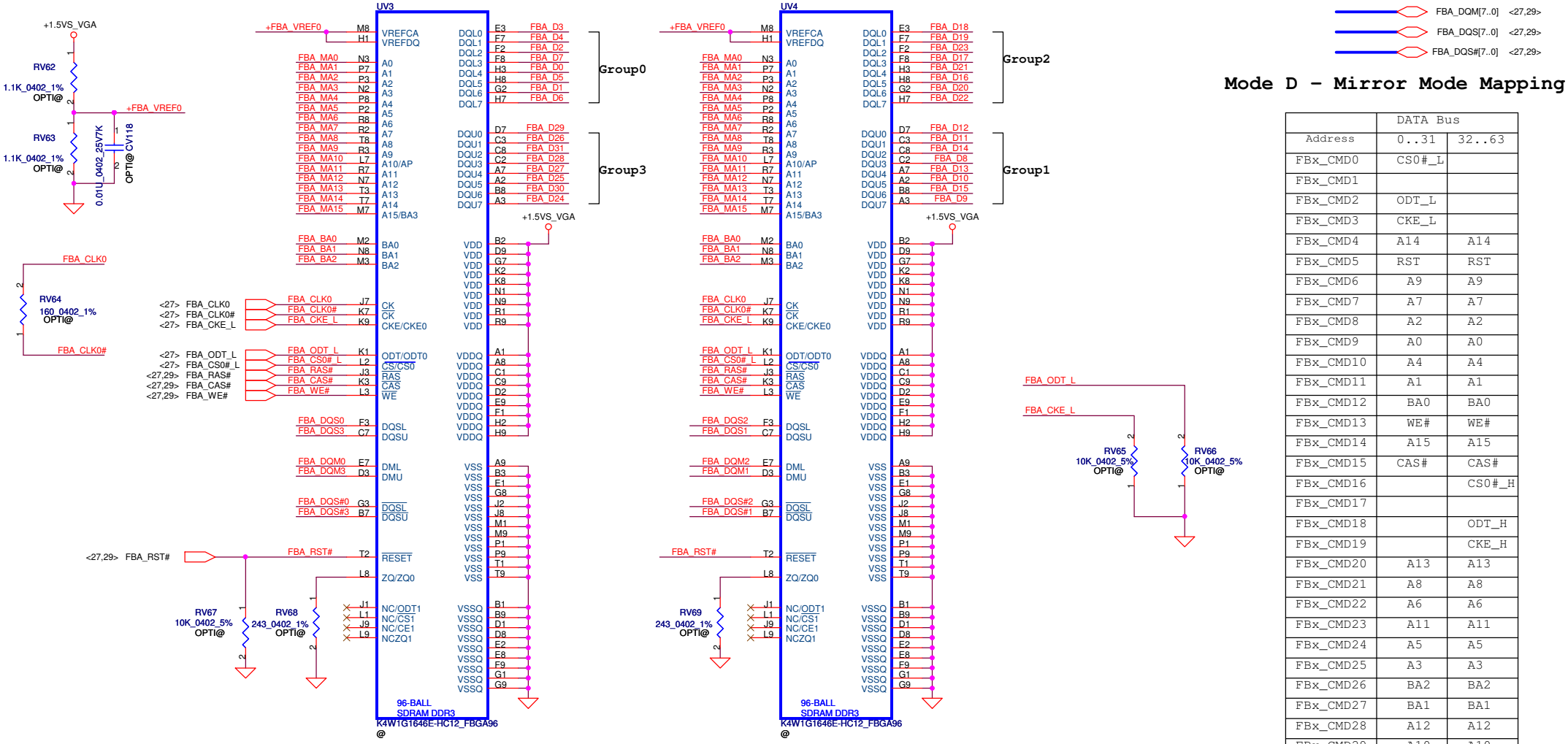
Memory Partition A - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

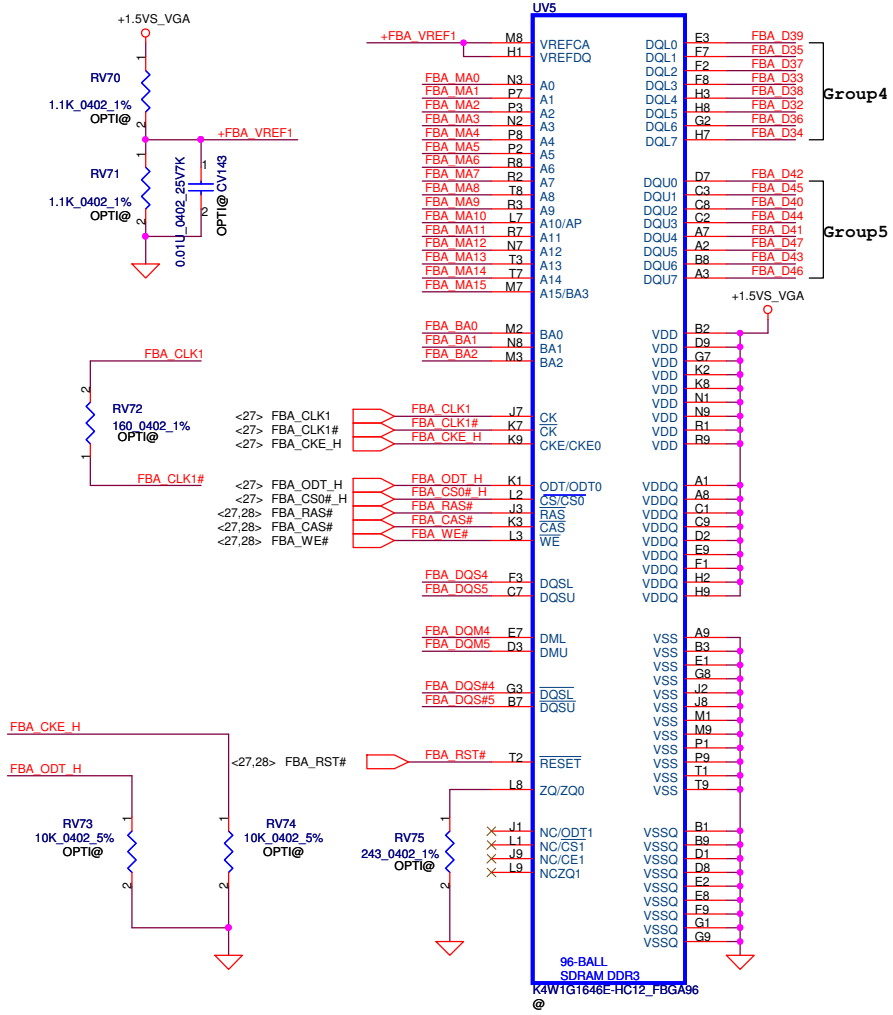
Compal Electronics, Inc.

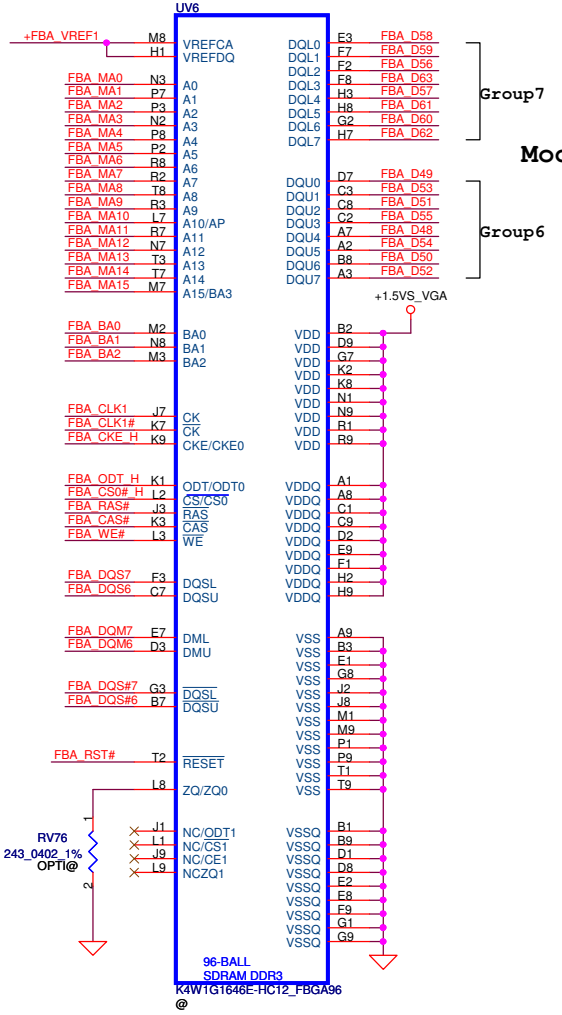
Title: N12P-VRAM A Lower

Size | Document Number: PIQY0 LA6881P | Rev: 0.3

Date: Monday, November 29, 2010 | Sheet 28 of 63

Memory Partition A - Upper 32 bits

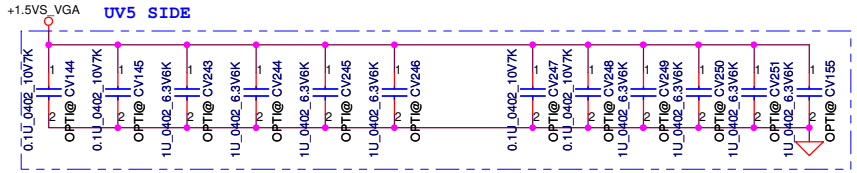


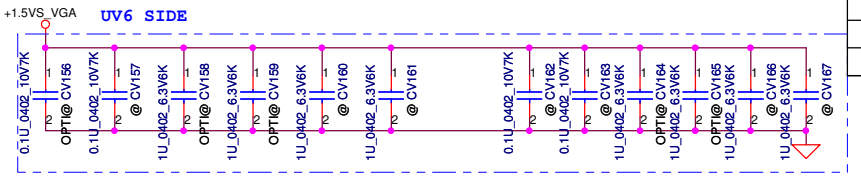


FBA_D[0..63] <27,28>
FBA_MA[15..0] <27,28>
FBA_BA[2..0] <27,28>
FBA_DQM[7..0] <27,28>
FBA_DQS[7..0] <27,28>
FBA_DQS#[7..0] <27,28>

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

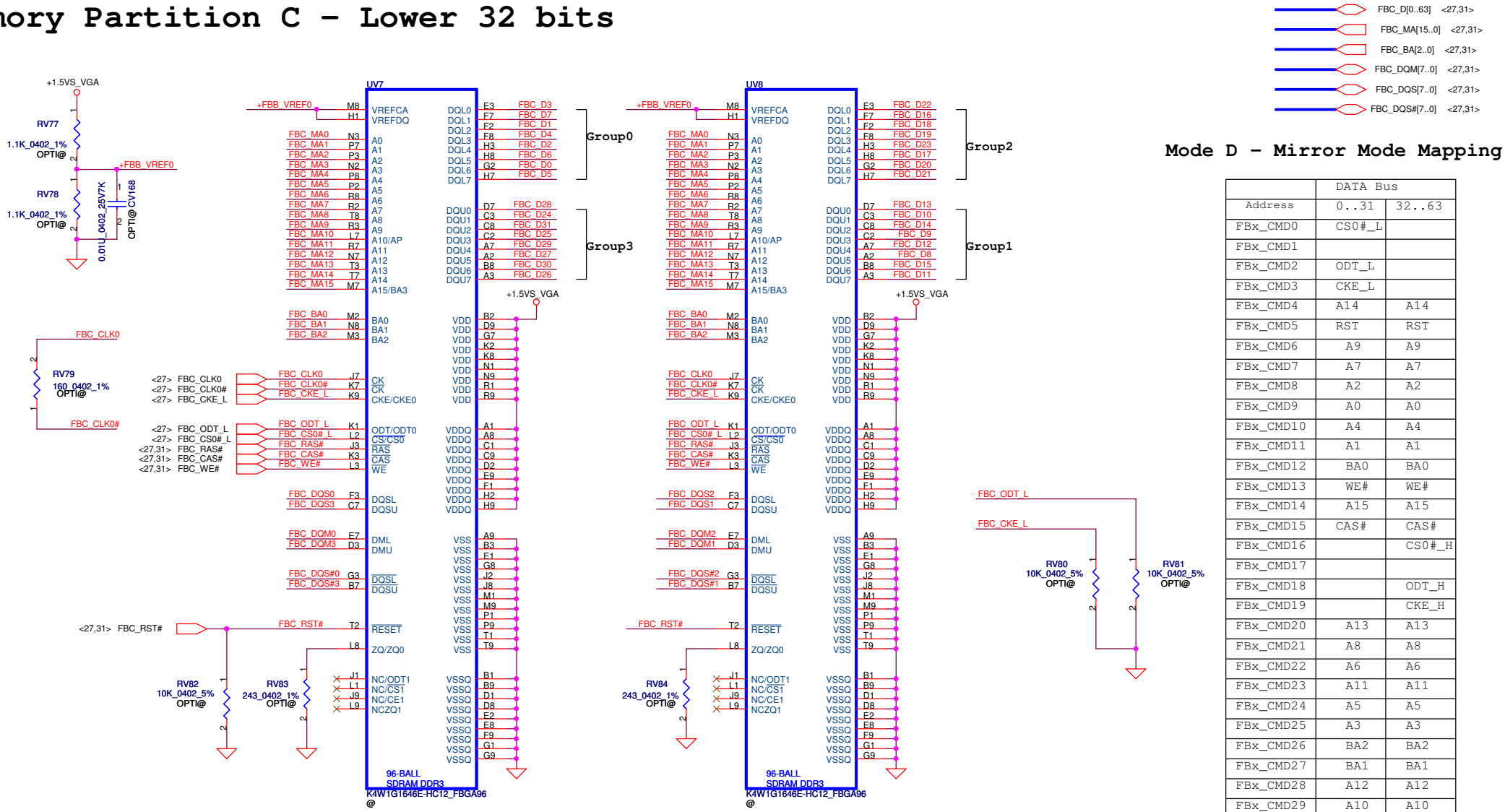
Compal Electronics, Inc.

Title: N12P-VRAM A Upper

Size | Document Number: PIQY0 LA6881P | Rev: 0.3

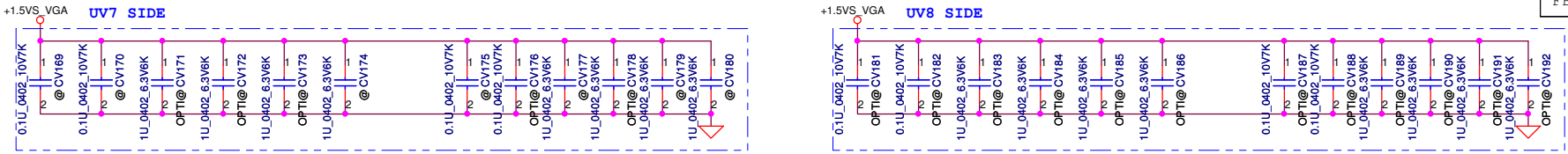
Date: Monday, November 29, 2010 | Sheet 29 of 63

Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: N12P-VRAM C Lower

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 0.3

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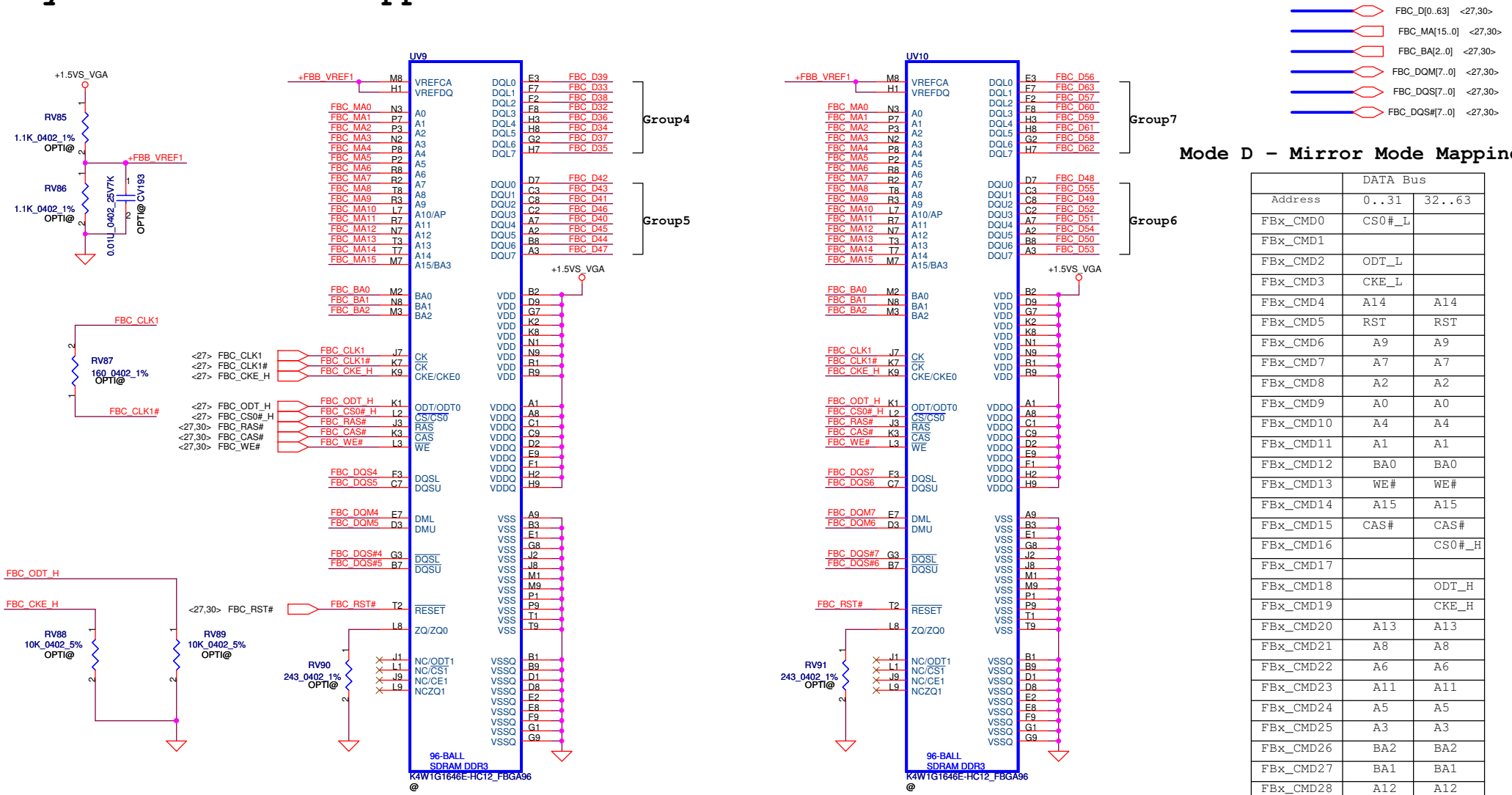
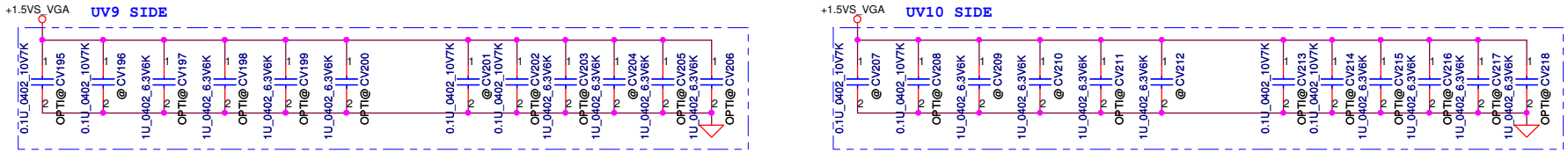
Memory Partition C – Upper 32 bits



Mode D – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.
Title: N12P-VRAM C Upper
Size: Custom
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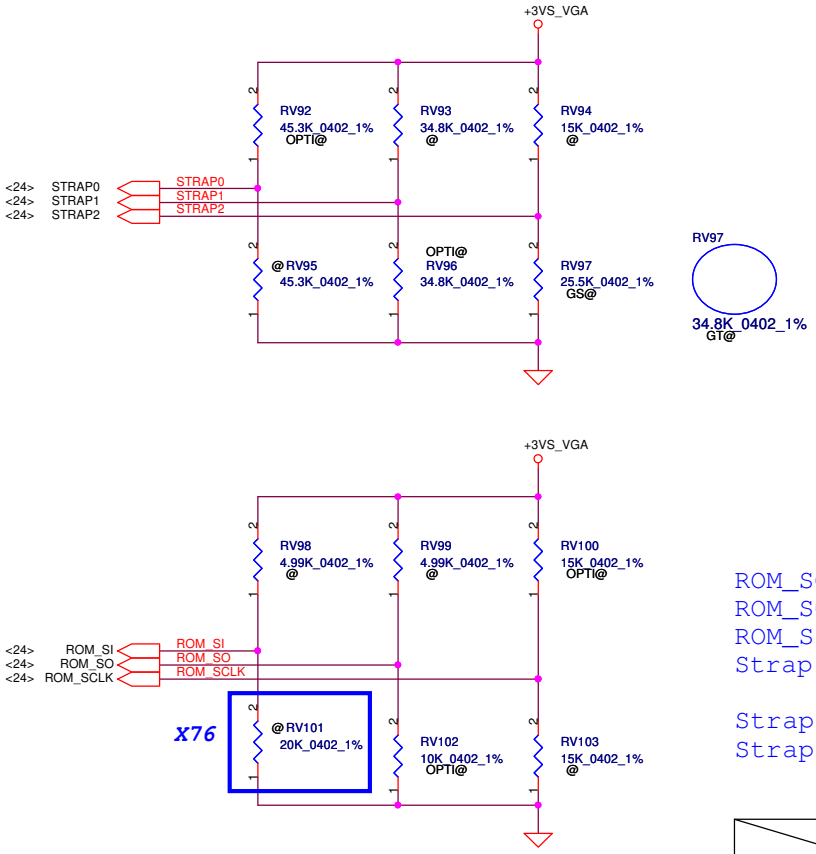

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

ROM_SO : PD-10K
ROM_SCLK : PH-15K
ROM_SI : PD20K (Samsung)
Strap 2 : N12P-GS, PD-25K,
N12P-GT, PD35K,
Strap 1 : PD-35K
Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

Hynix H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
	128Mx16	0110	PD 35K	SA00003YO10
Samsung K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
	128Mx16	0111	PD 45K	SA000047Q10

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.
Title: N12P_MISC
Size: Custom | Document Number: PIQY0 LA6881P | Rev: 0.3
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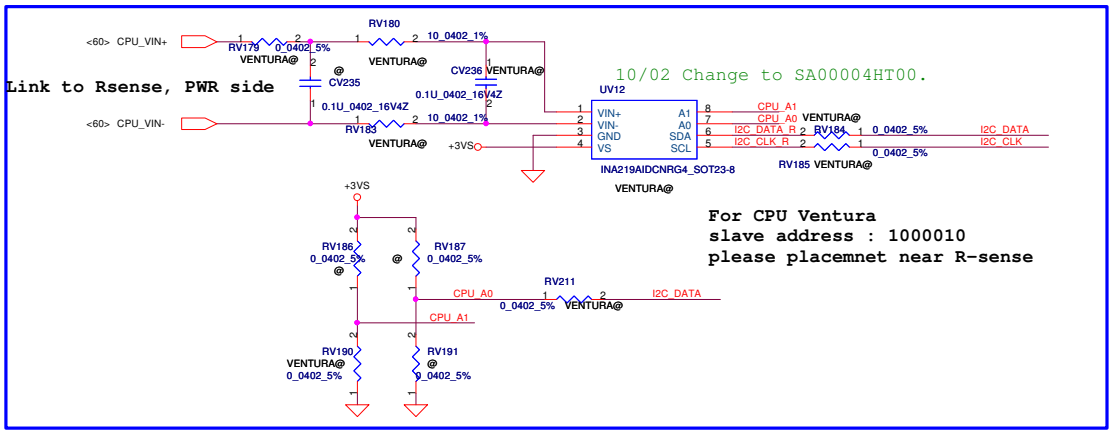
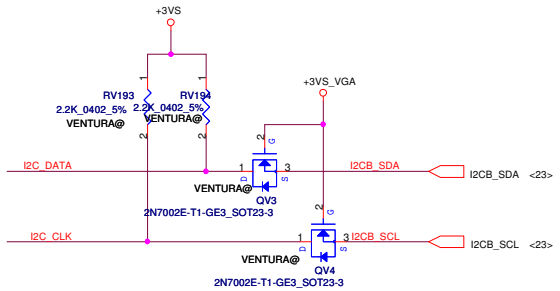
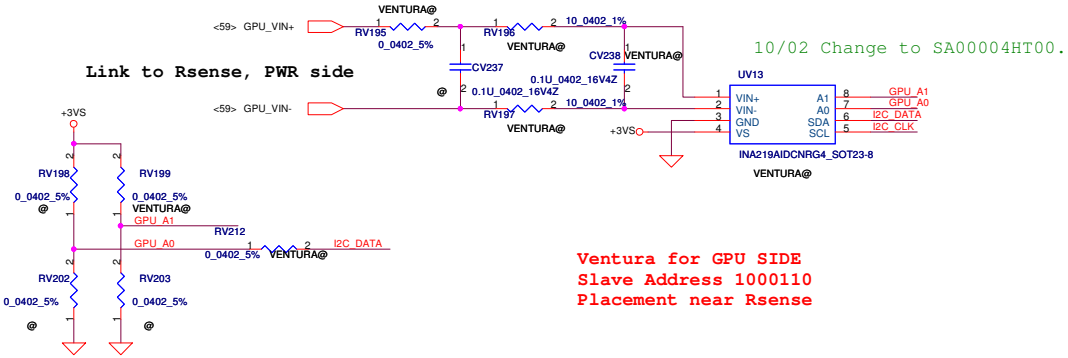
TOP side (under inductor)







Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: N12P_VENTURA

Size	Document Number	Rev
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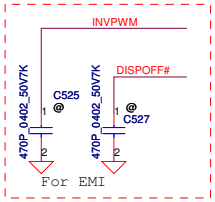
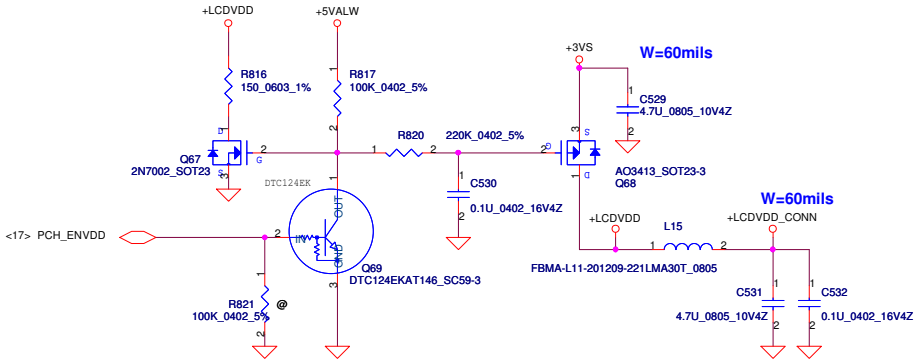
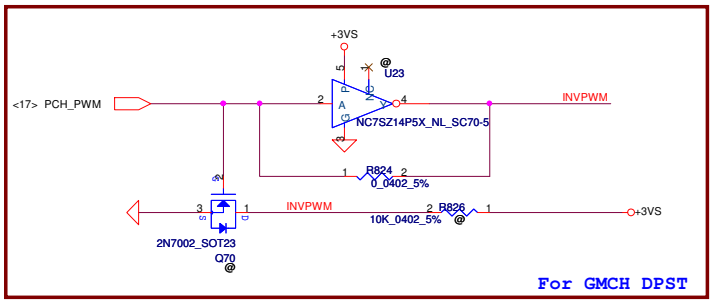
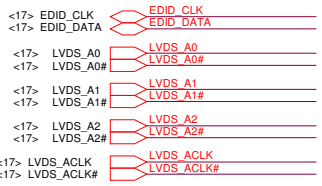
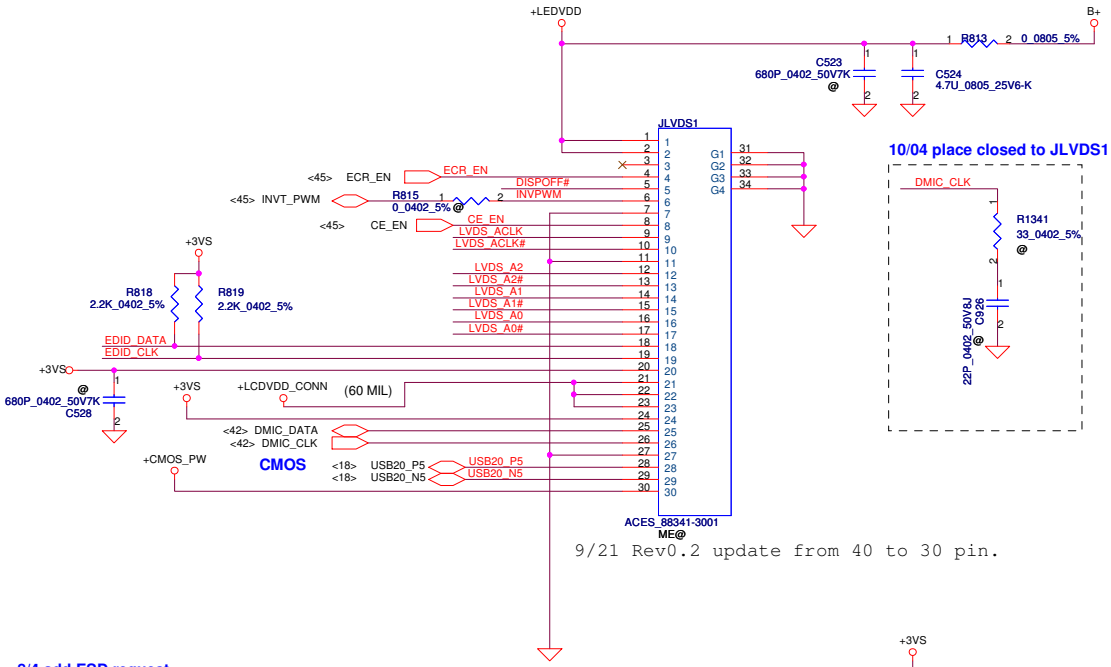


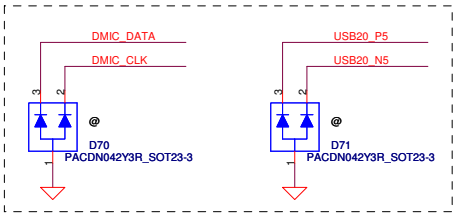
LCD POWER CIRCUIT

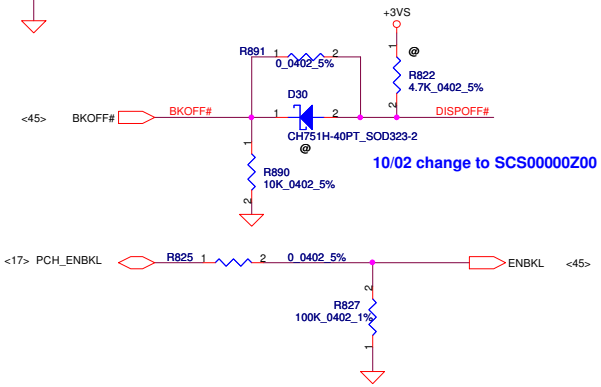


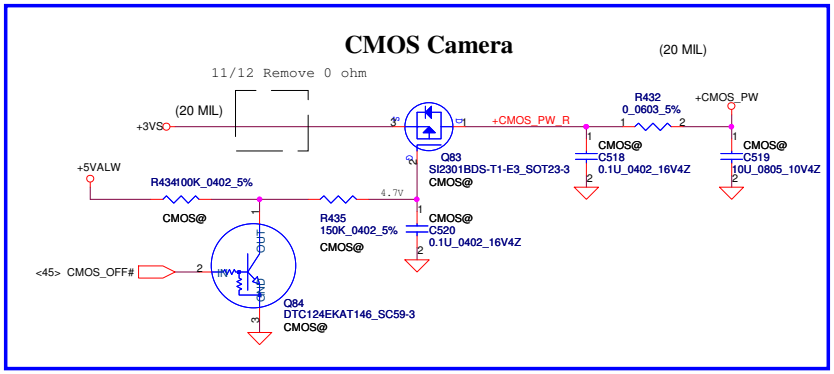












Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: B	Document Number: PIQY0 LA6881P		Rev: 0.3
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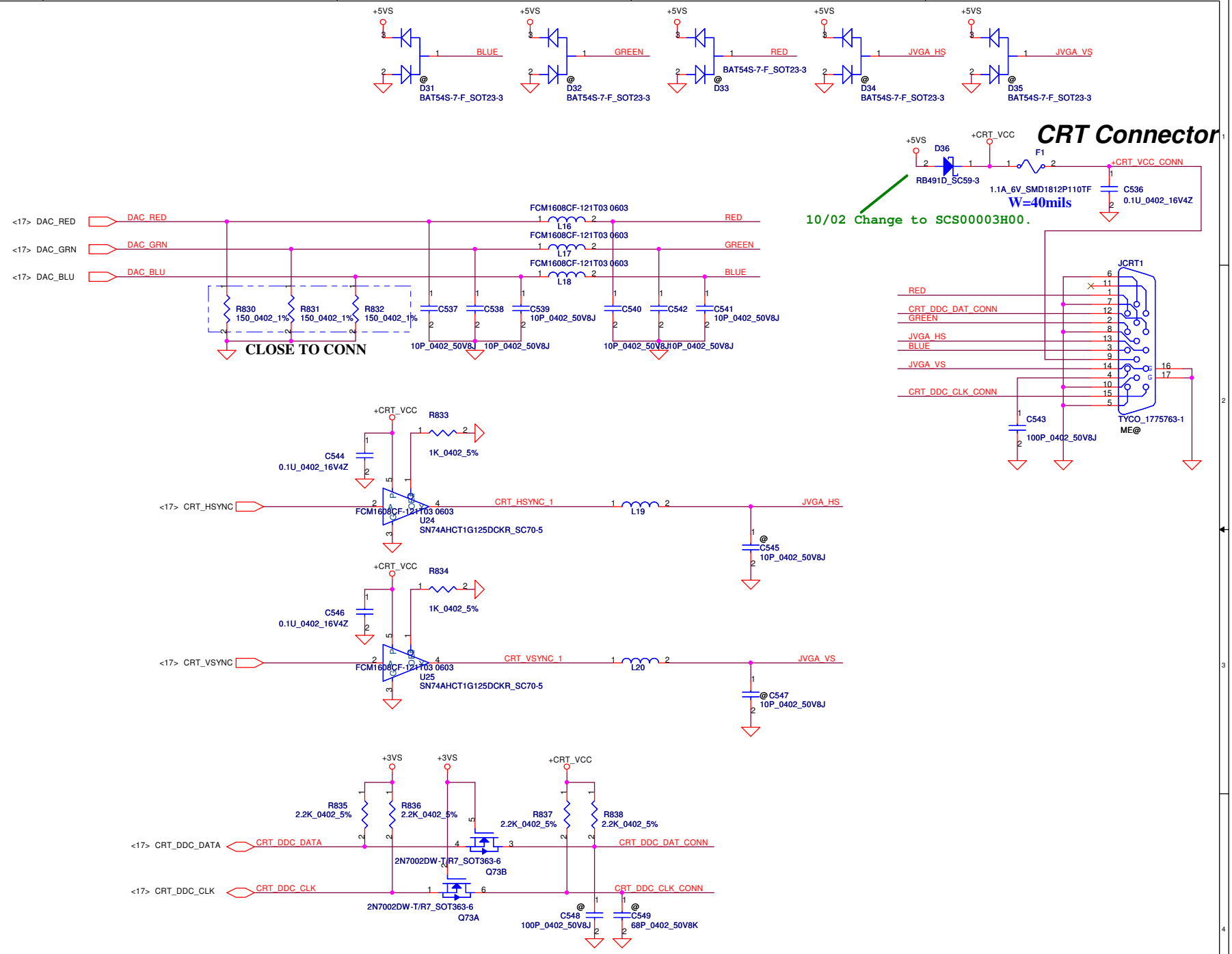

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
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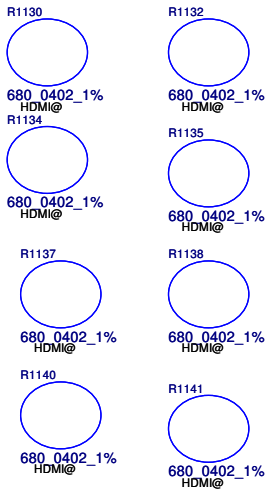
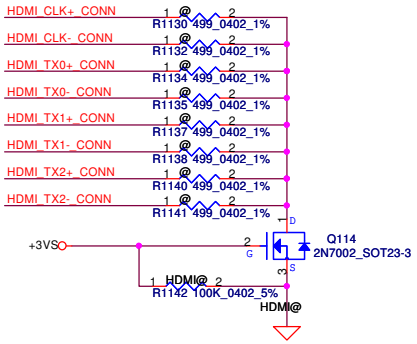
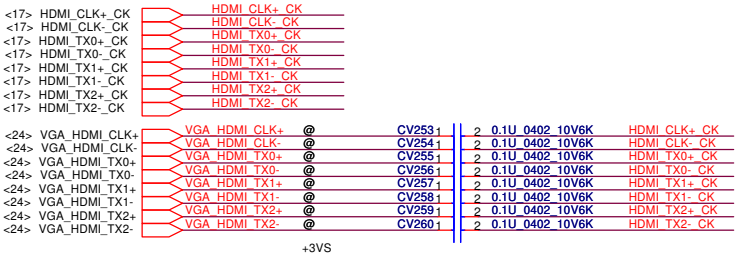
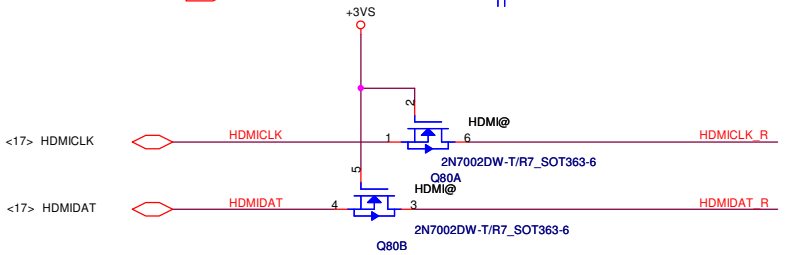
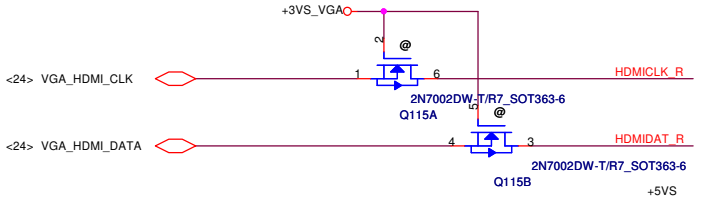


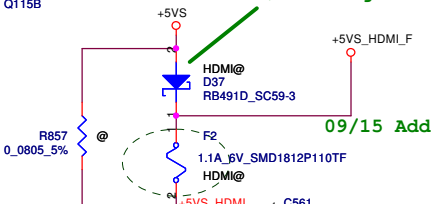




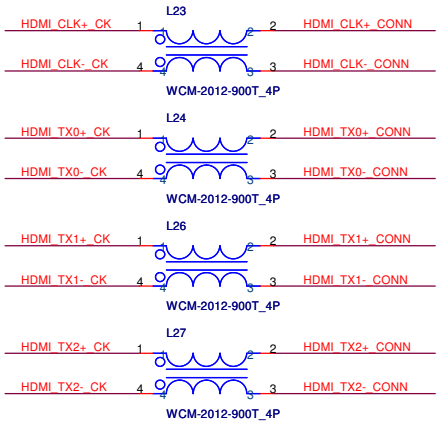


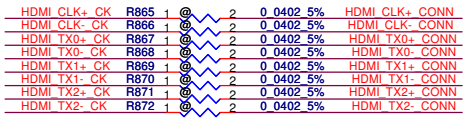


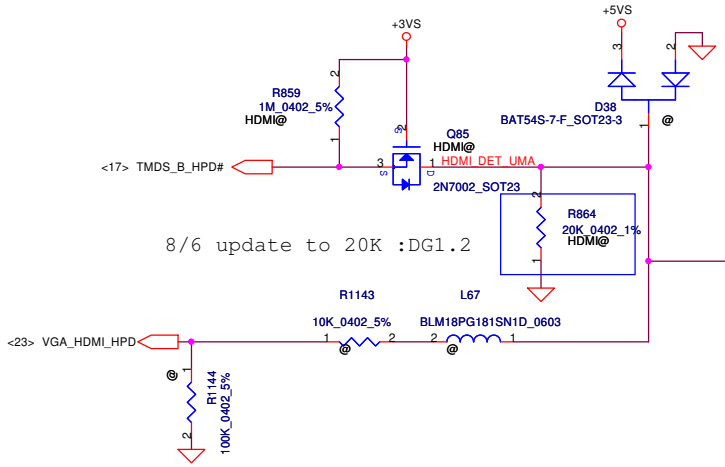
10/02 Change to SCS00003H00.

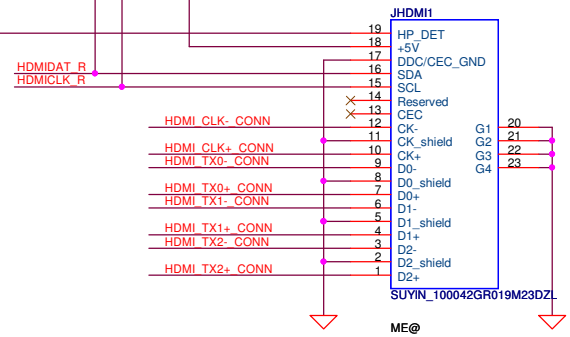


DVT, Change to SM070000I00 for EMI request.









Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics,Ltd.

Title: HDMI CONN

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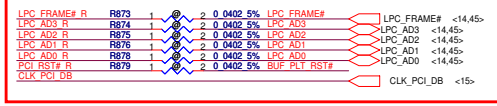
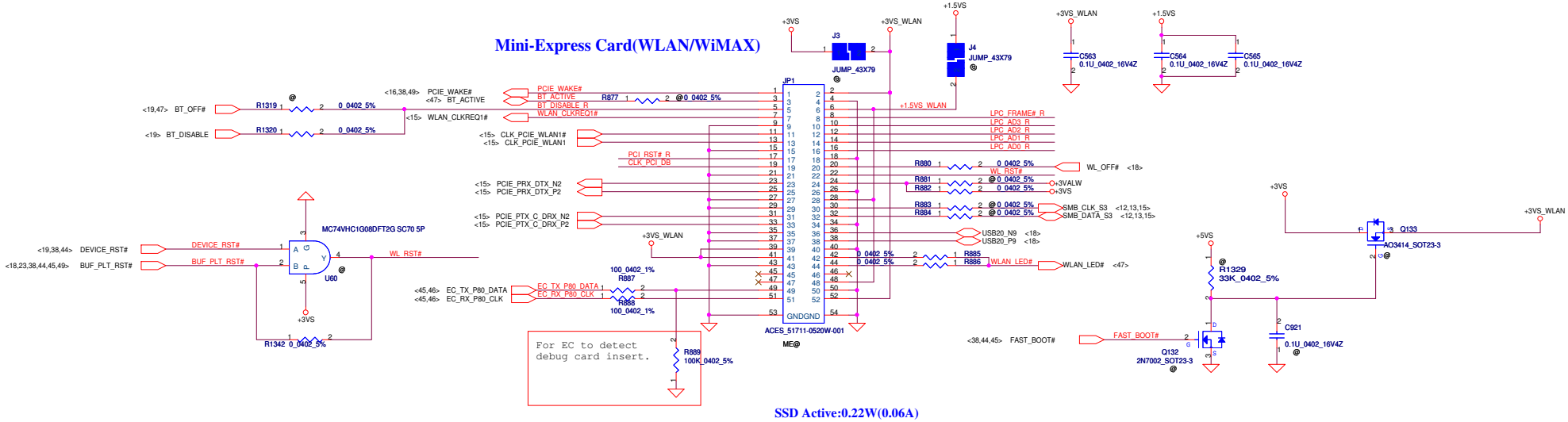
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

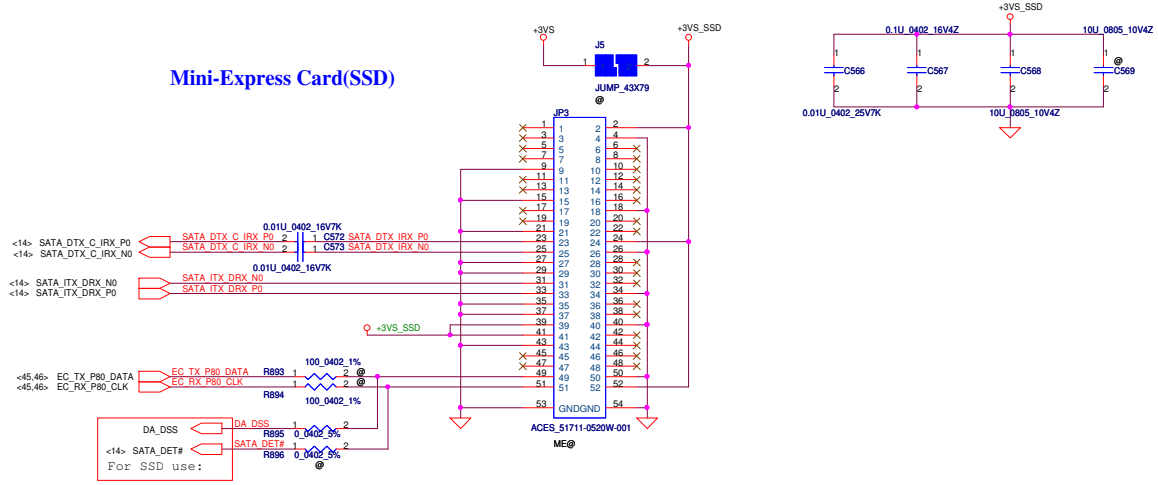


Mini-Express Card(WLAN/WiMAX)



SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: PIQY0 LA6881P		Rev: 0.3
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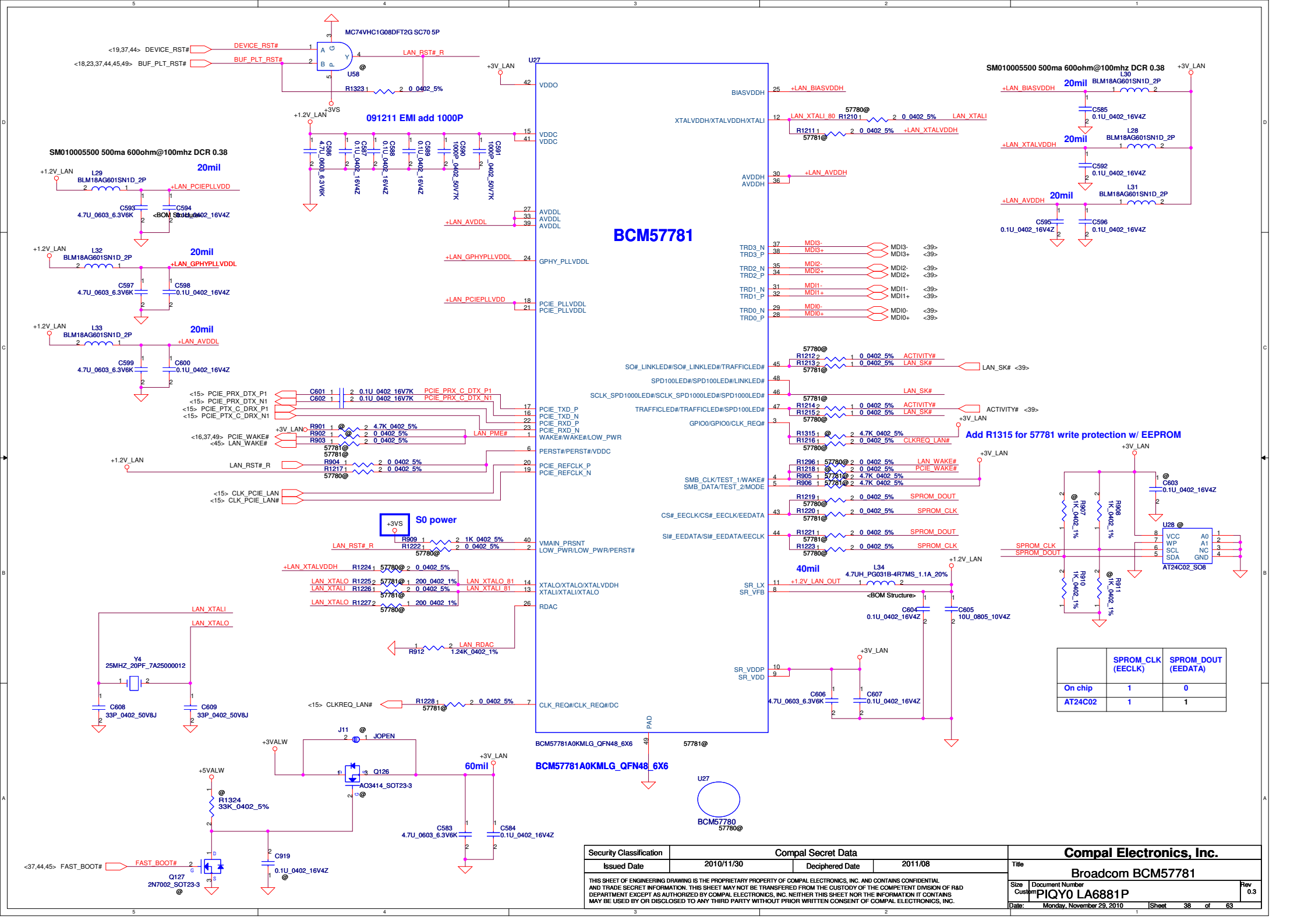

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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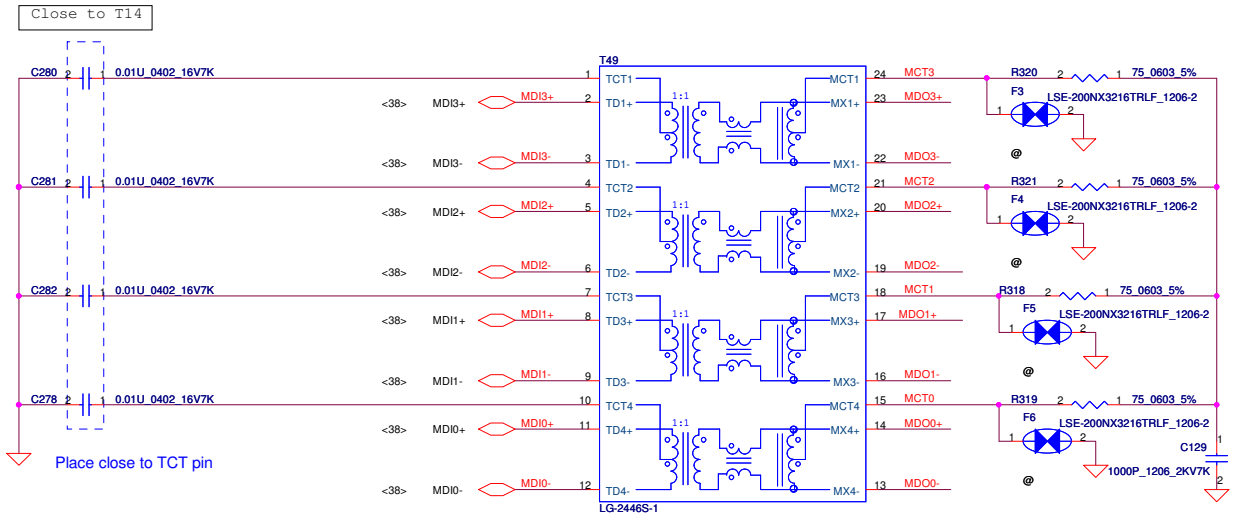
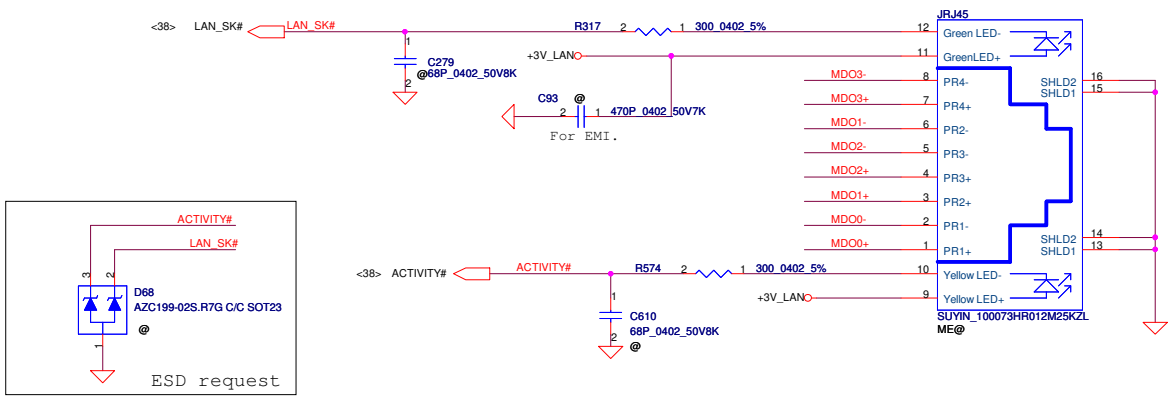


RJ45 Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 0.3

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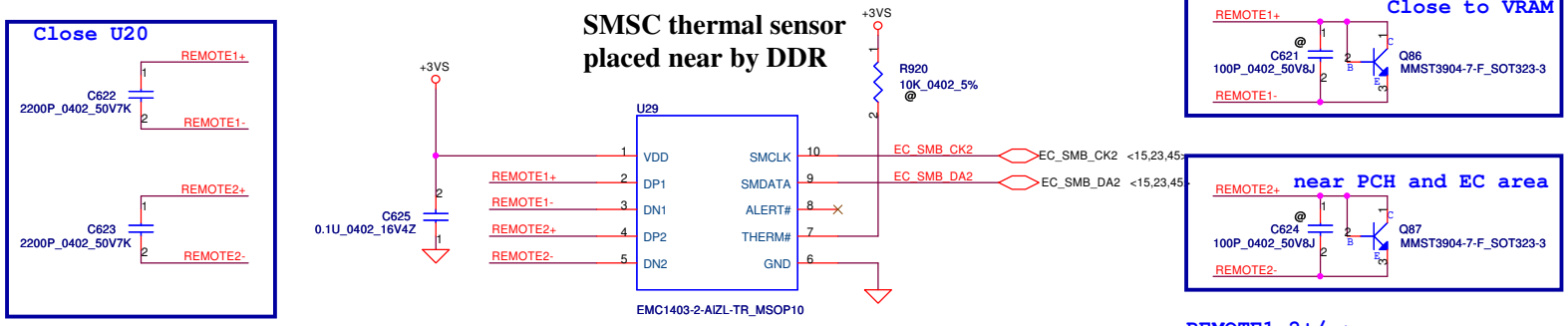
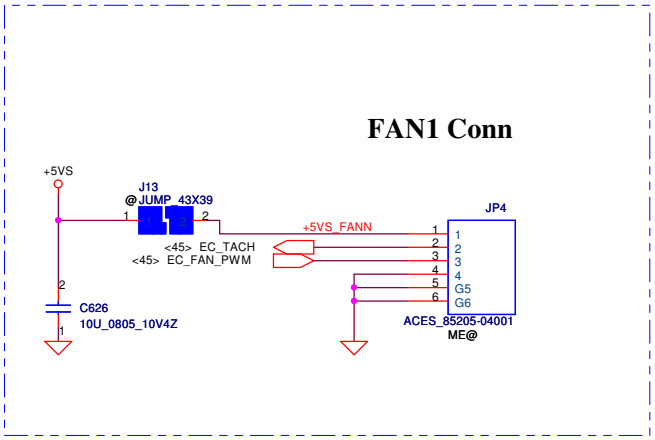


Address 1001_101xb

8/02 Change PN to SA000046C00, Fintek.

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics,Ltd.

Title: **EMC1403_Thermal sensor/FAN**

Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

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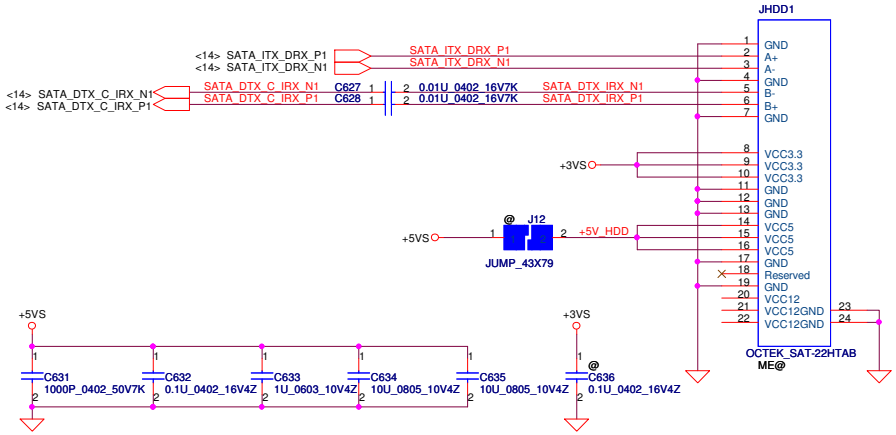
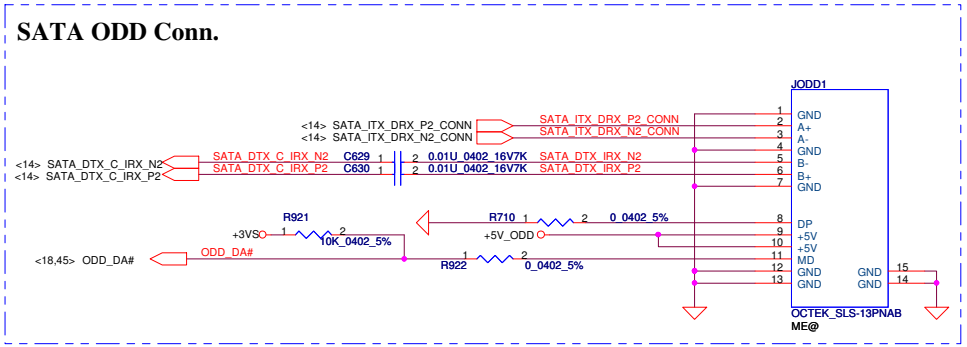
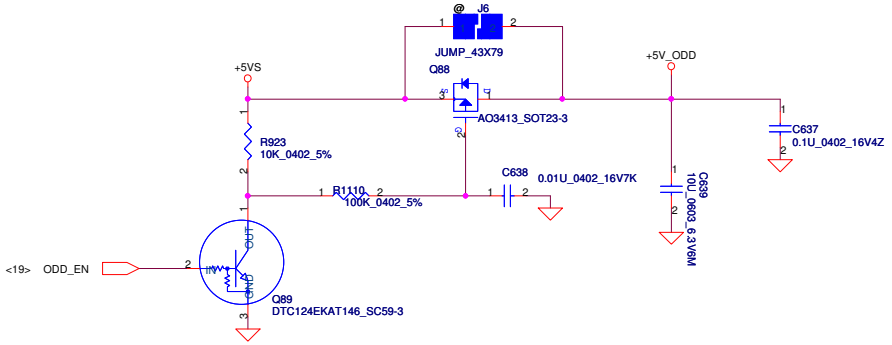
SATA HDD Conn.



SATA ODD Conn.

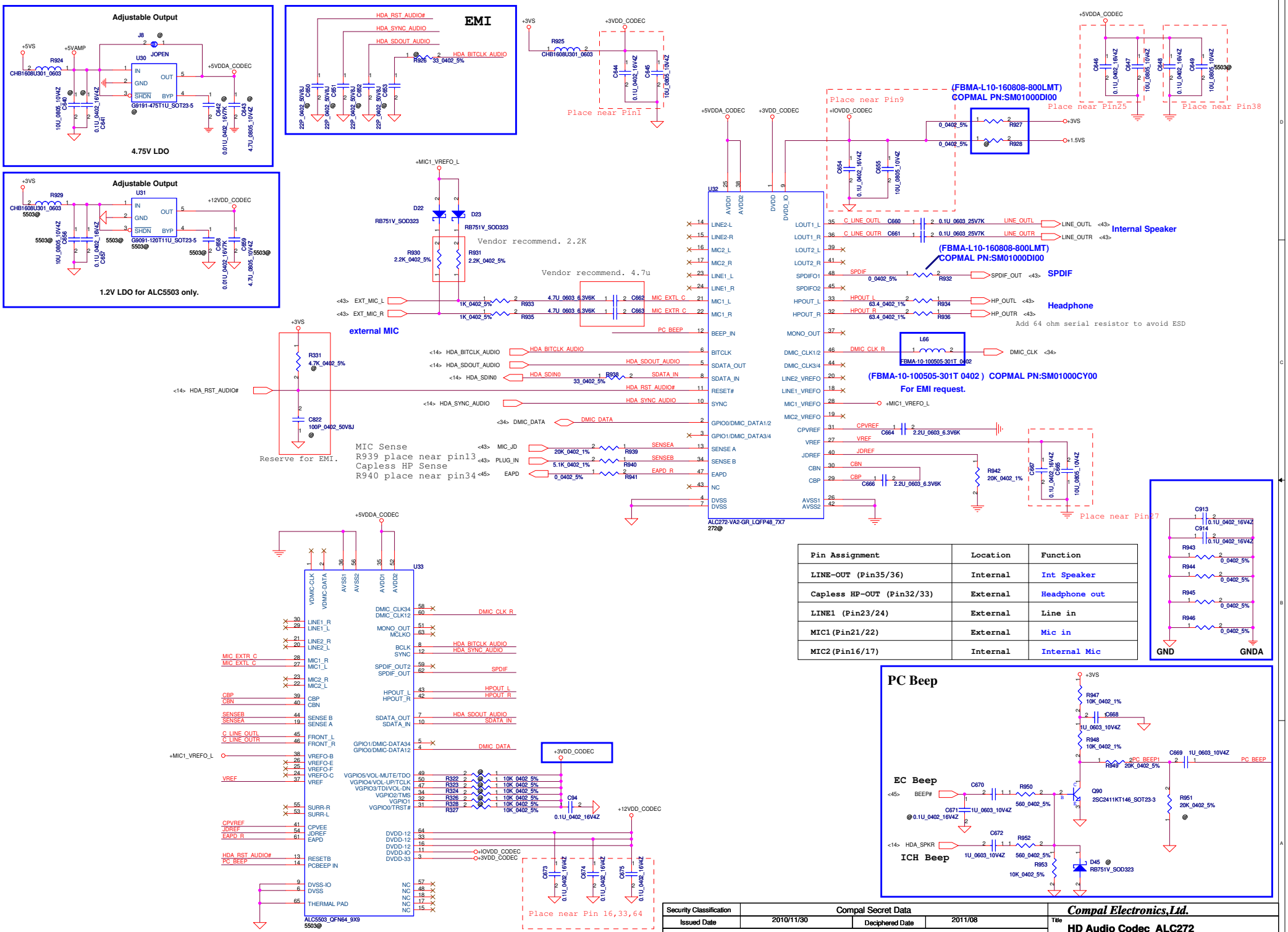


ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: B	Document Number: PIQY0 LA6881P		Rev: 0.3
Date: Monday, November 29, 2010	Sheet 41 of 63		



Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MIC2(Pin16/17)	Internal	Internal Mic

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

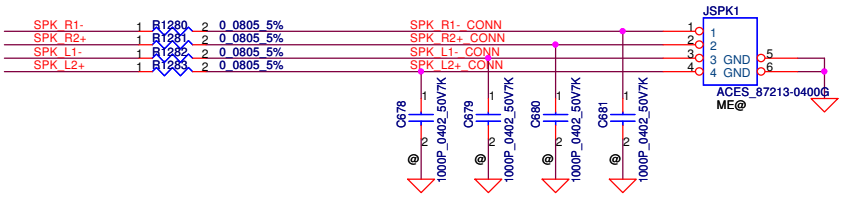
Compal Electronics,Ltd.

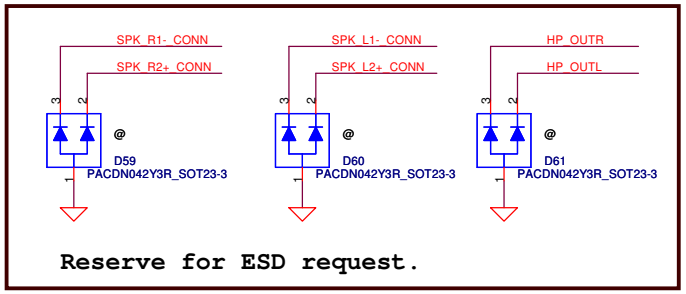
Title: HD Audio Codec_ALC272

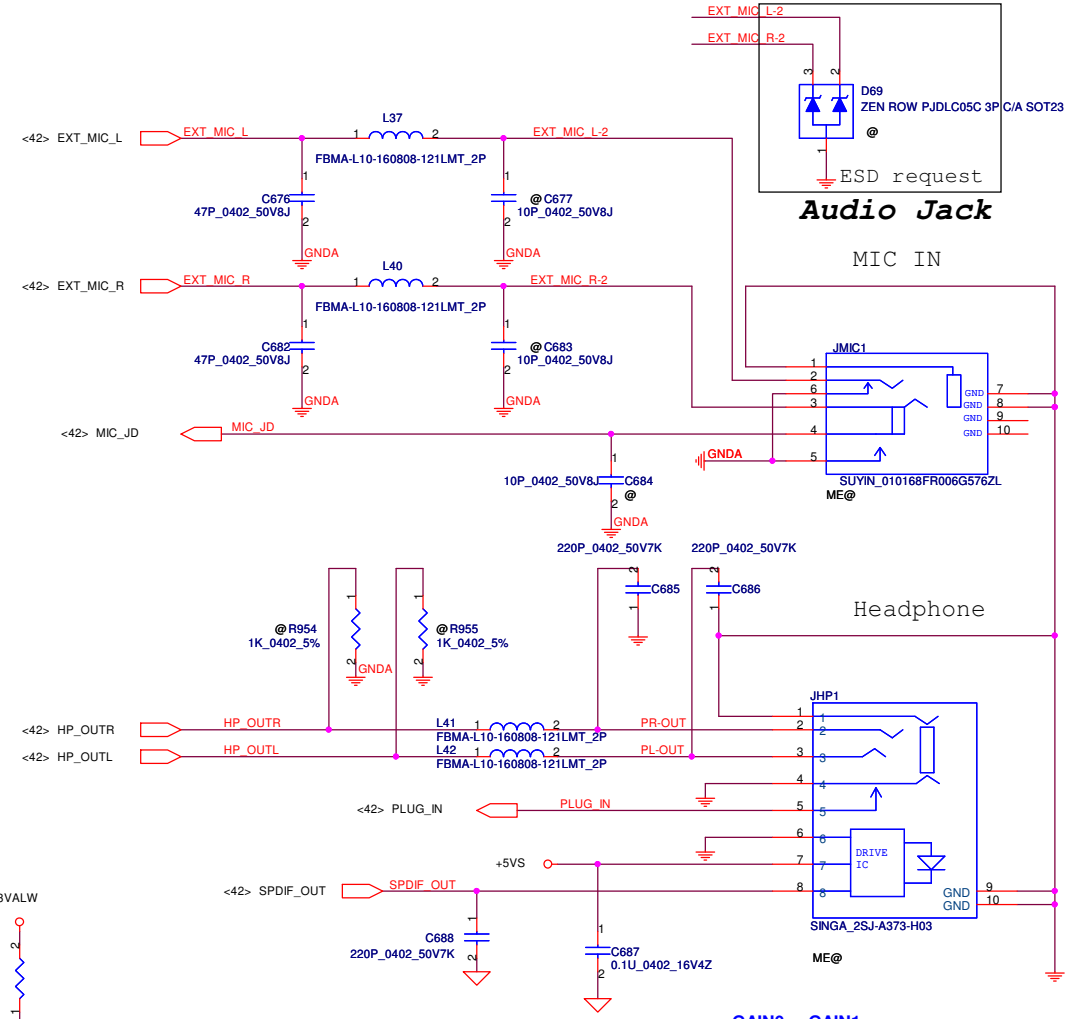
Size	Document Number	Rev
C	KIWB1/B2_LA4601P	0.3

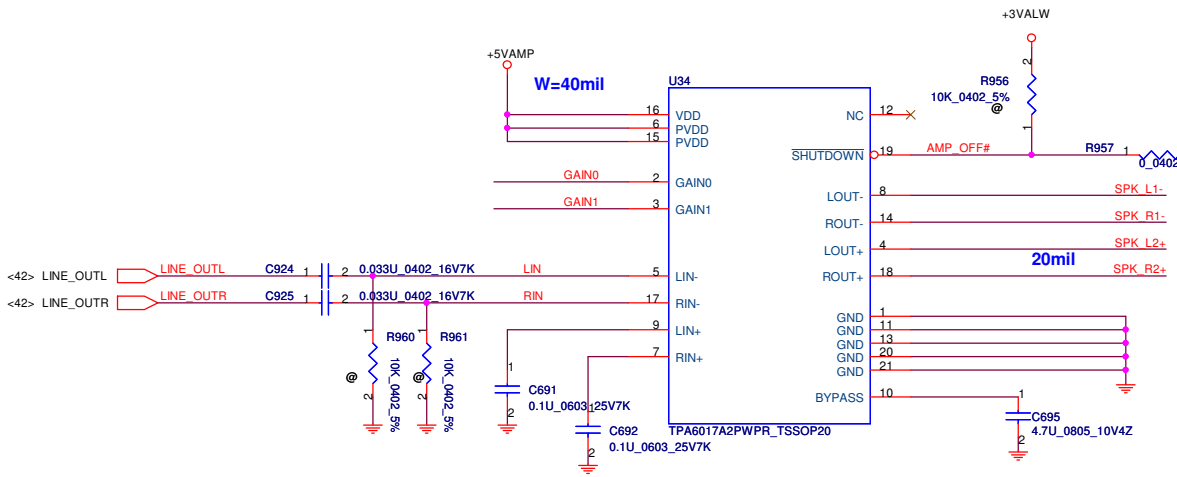
Date: Monday, November 29, 2010 Sheet 42 of 63

wide 20MIL

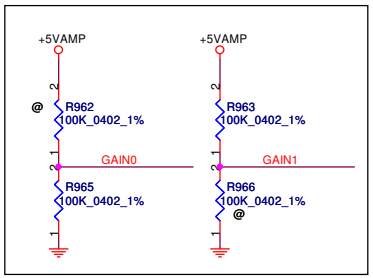








GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



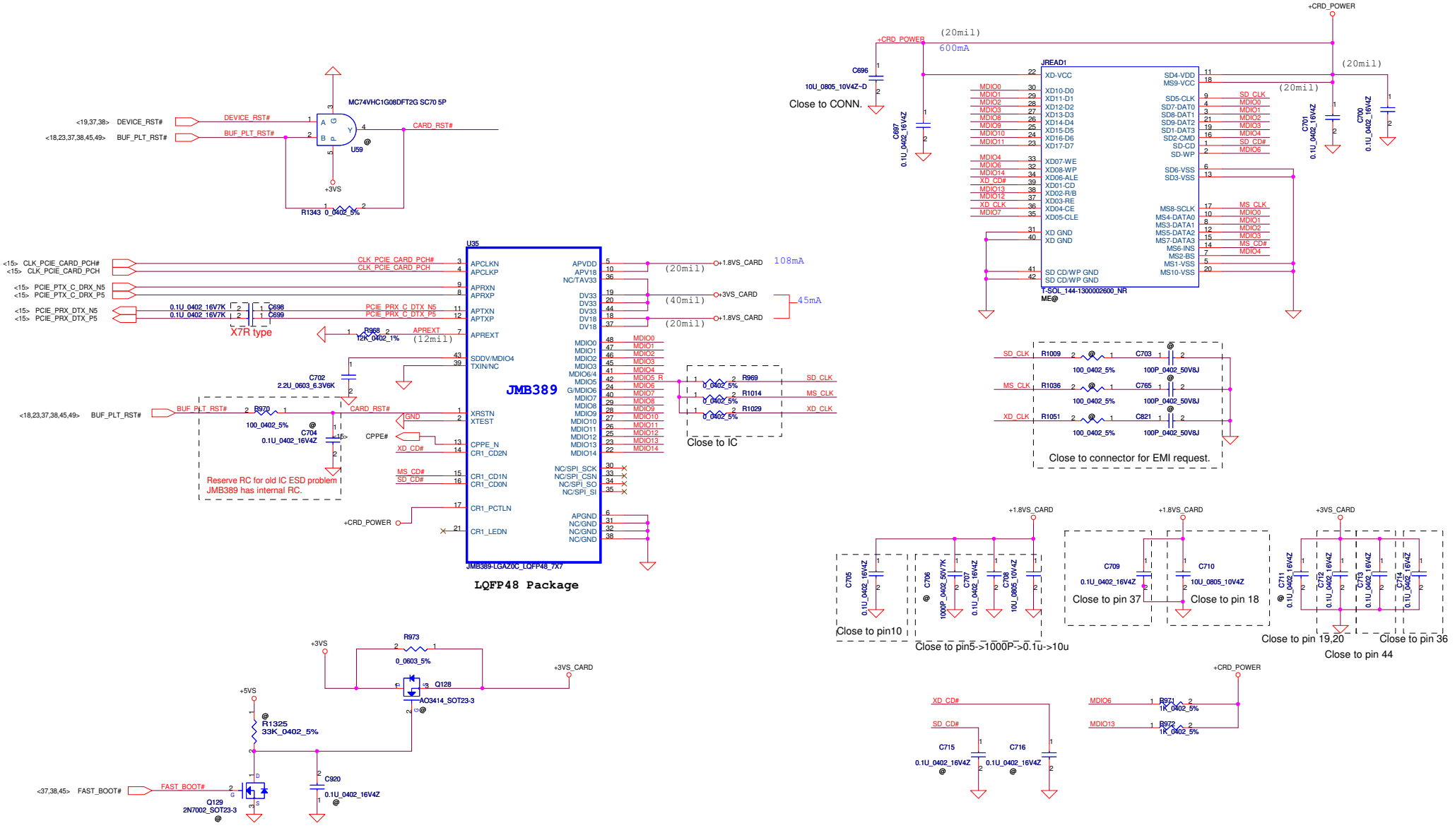
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics,Ltd.

Title: AMP,Audio speaker CONN

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.3

Date: Monday, November 29, 2010 Sheet 43 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

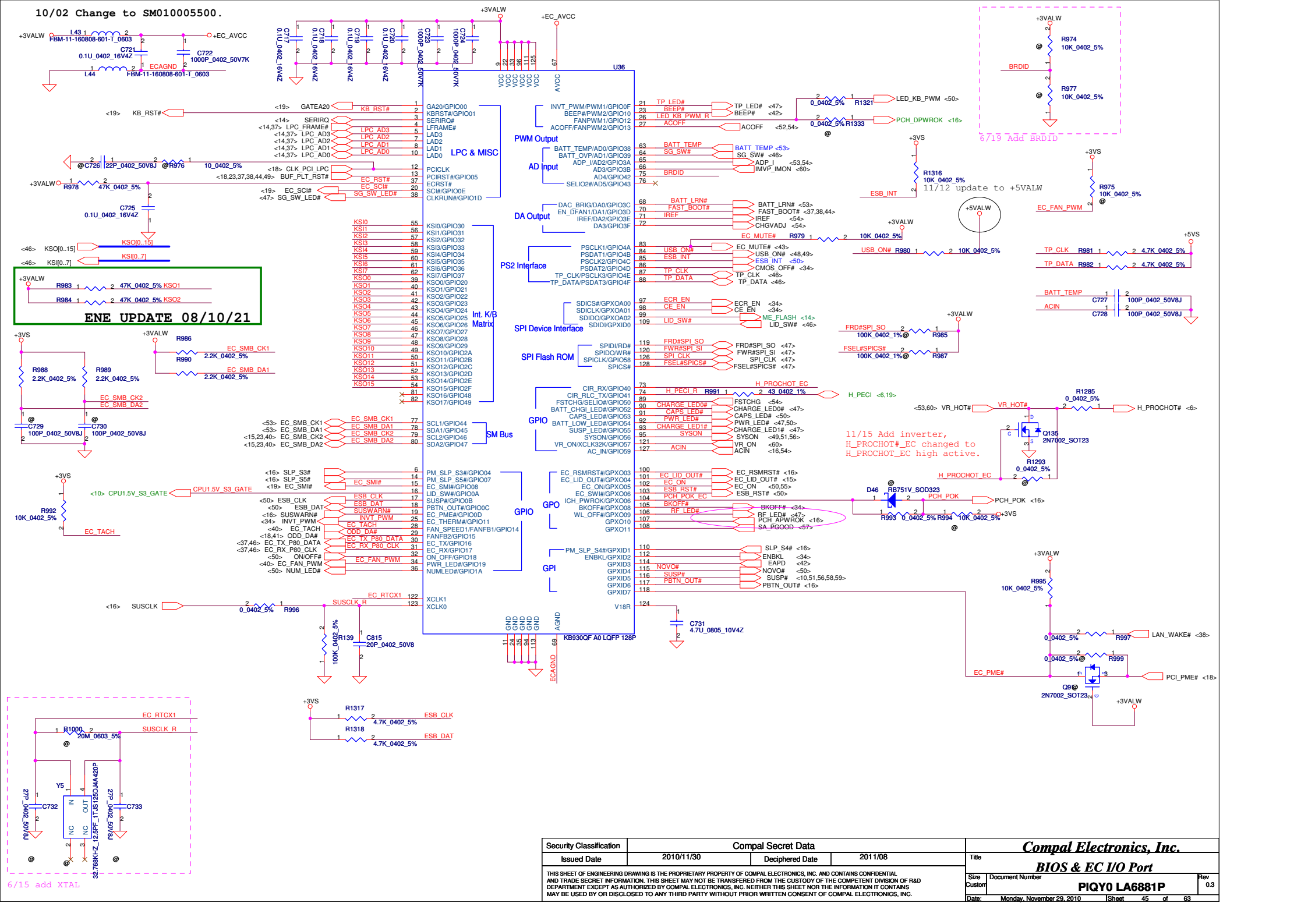
Compal Electronics, Inc.

Title: Carder JMB389

Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 44 of 63

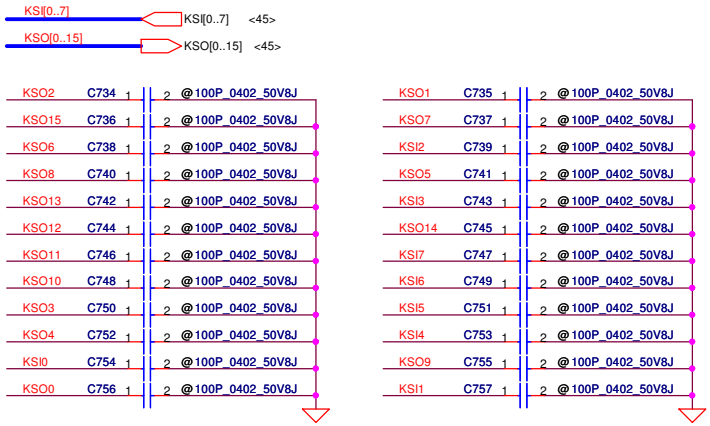
10/02 Change to SM010005500.



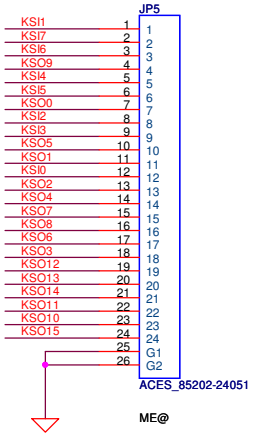
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.			
Title: BIOS & EC I/O Port			
Size: Custom	Document Number: PIQY0 LA6881P		Rev: 0.3
Date: Monday, November 29, 2010	Sheet 45 of 63		

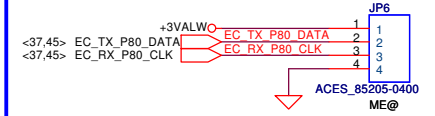
INT_KBD Conn.



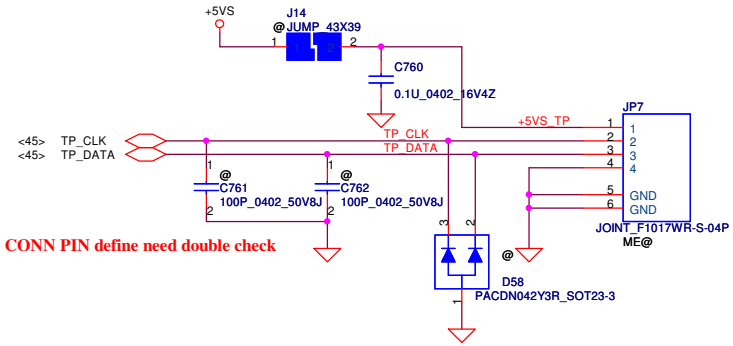
CONN PIN define need double check



EC DEBUG PORT

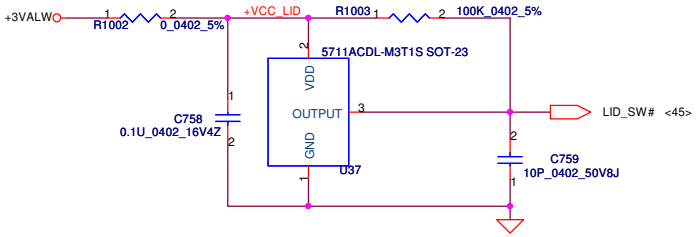


To TP/B Conn.

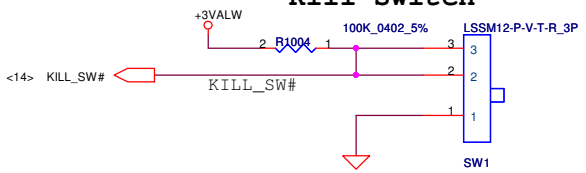


CONN PIN define need double check

Lid Switch

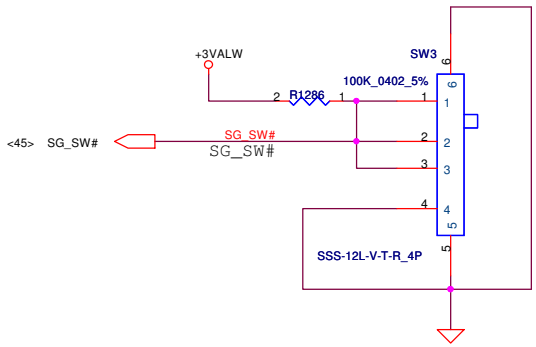


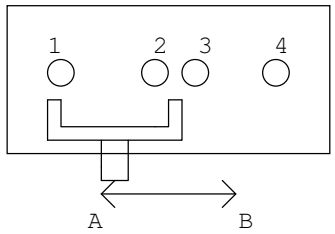
Kill Switch



Kill

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON





Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

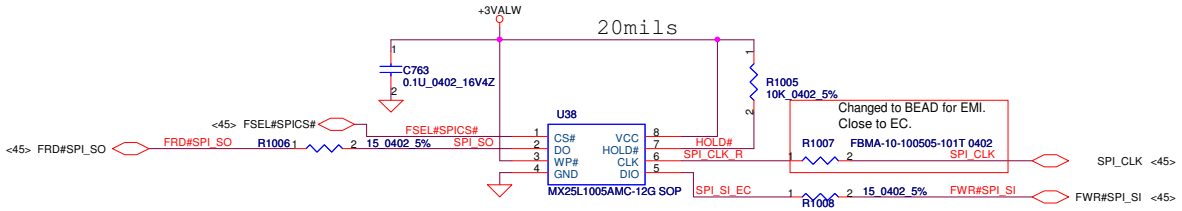
Compal Electronics, Inc.

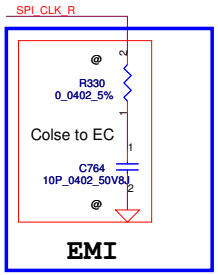
Title: KB /SW /LPC Debug Conn.

Size: B | Document Number: PIQY0 LA6881P | Rev: 0.3

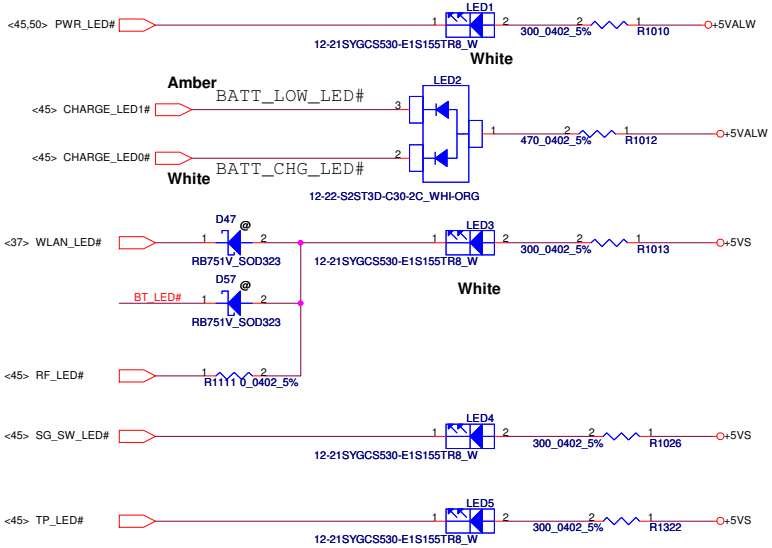
Date: Monday, November 29, 2010 | Sheet 46 of 63

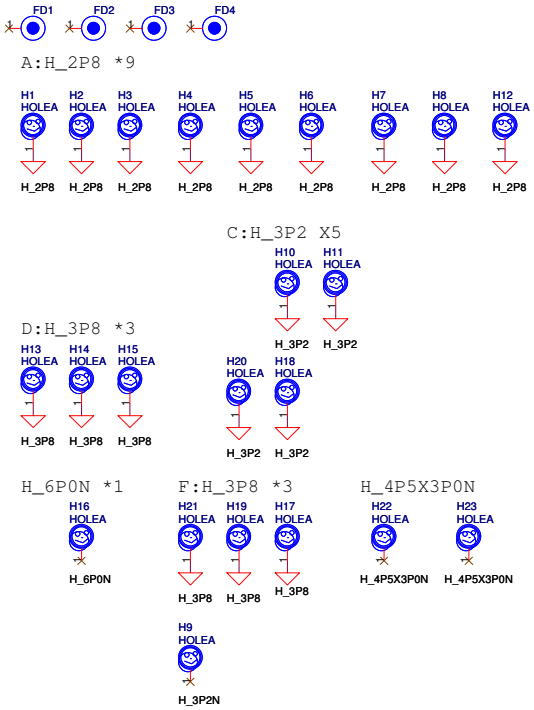
FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100



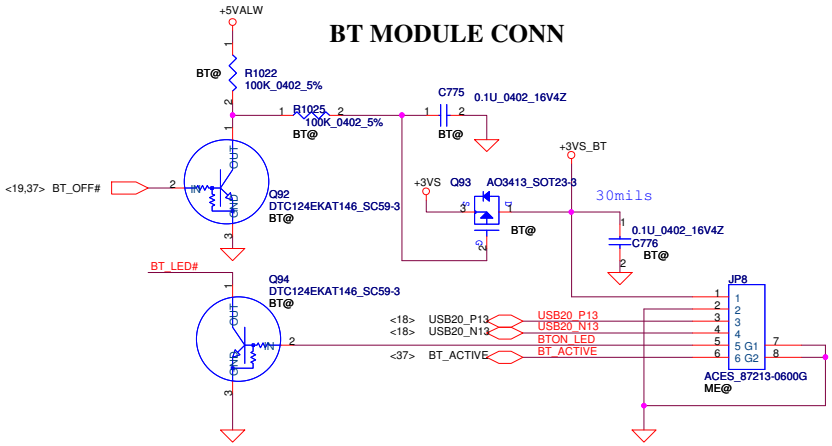


LED



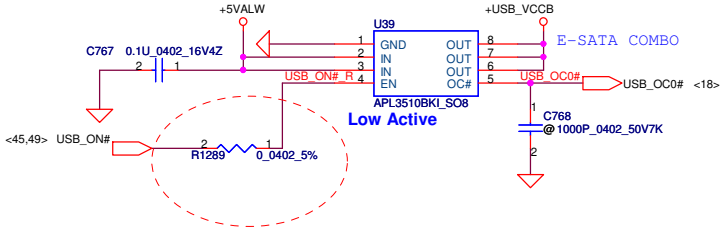


BT MODULE CONN

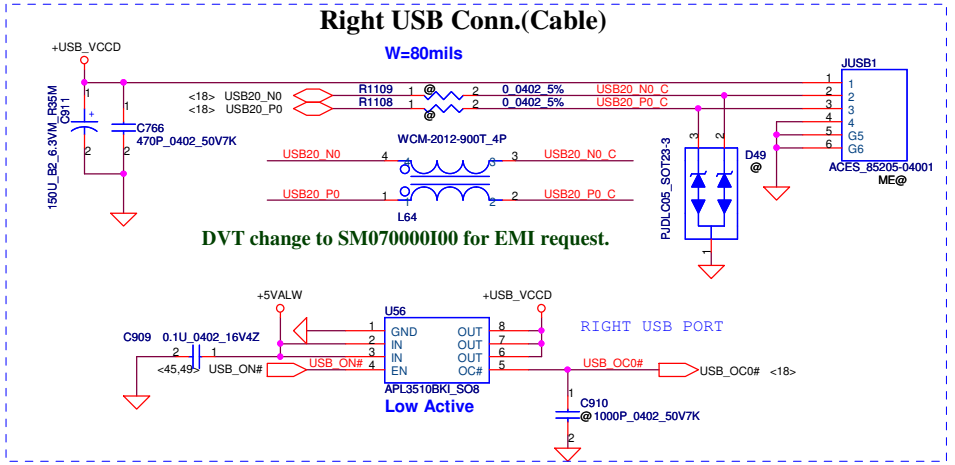


Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

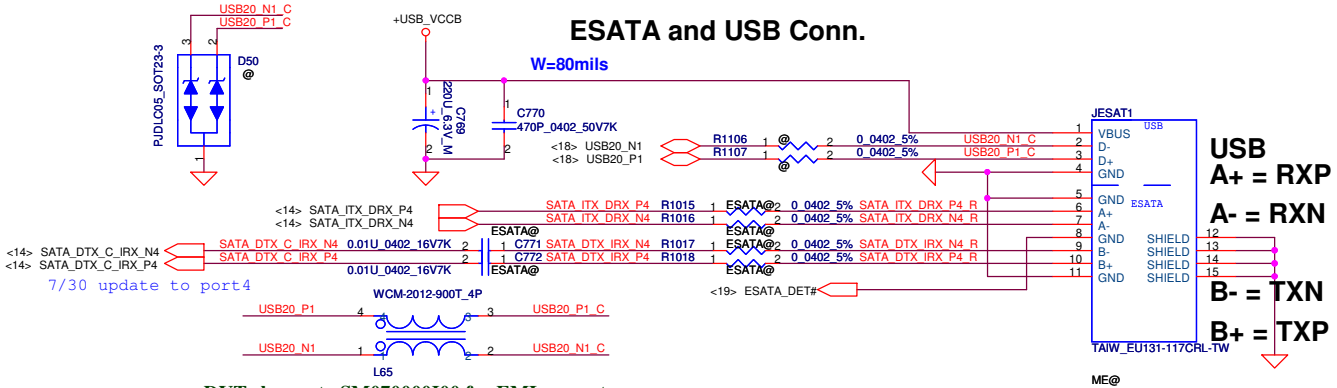
Compal Electronics, Inc.			
Title	LED/EC SPI ROM/BT		
Size B	Document Number PIQY0 LA6881P		Rev 0.3
Date: Monday, November 29, 2010	Sheet 47 of 63		

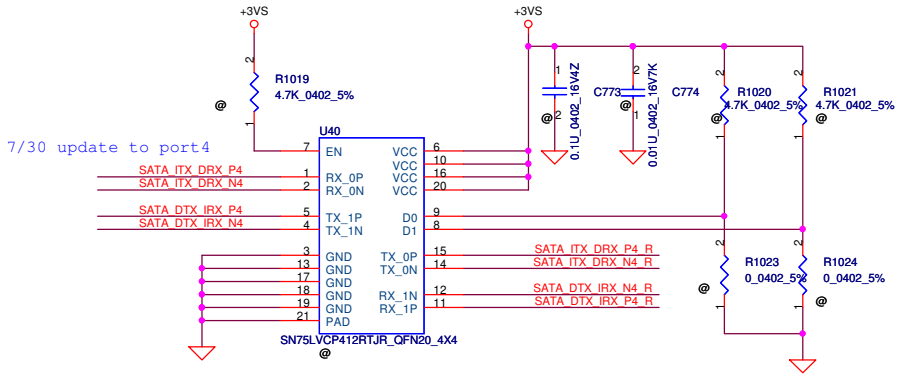


Right USB Conn.(Cable)



ESATA and USB Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

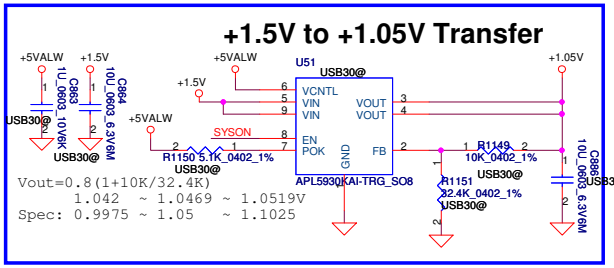
Compal Electronics, Inc.

Title: USB ports/E-SATA

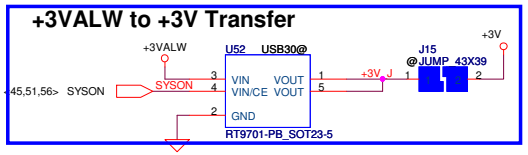
Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 48 of 63

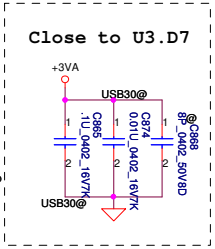
+1.5V to +1.05V Transfer



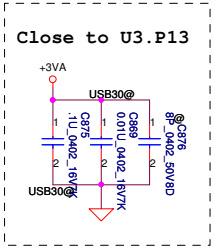
+3VALW to +3V Transfer

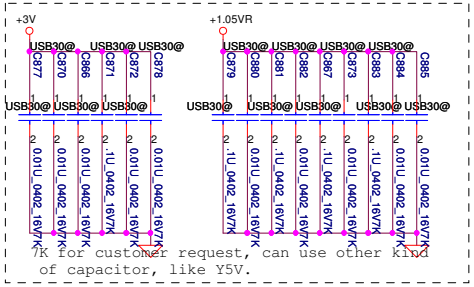


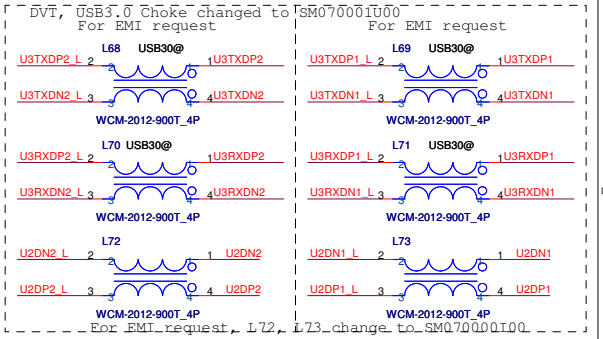
Close to U3.D7

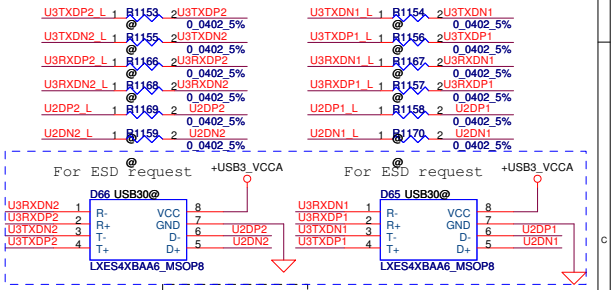


Close to U3.P13





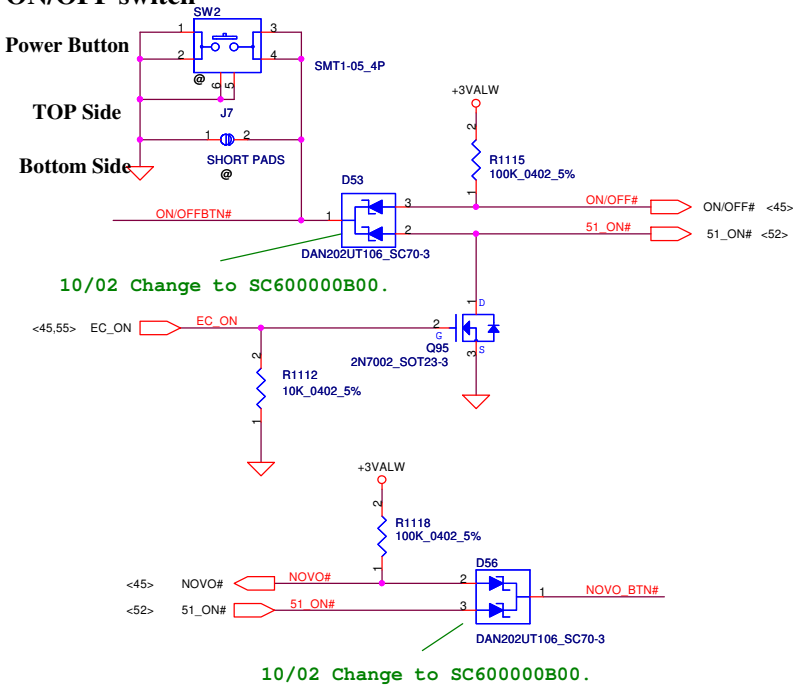




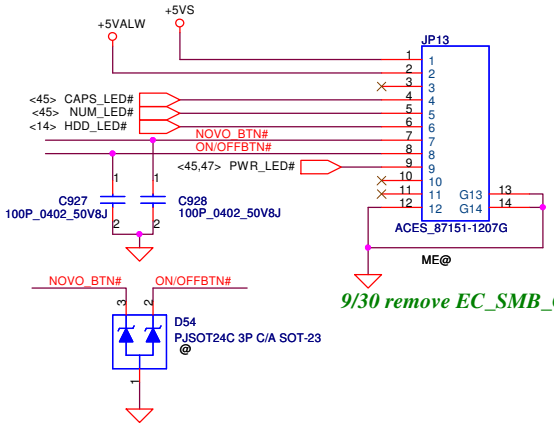
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

Title: USB3.0 PD720200
Size: Custom | Document Number | Rev: 0.3
Date: Tuesday, November 30, 2010 | Sheet 49 of 63

ON/OFF switch



Power Bottom Board Conn. 10pin

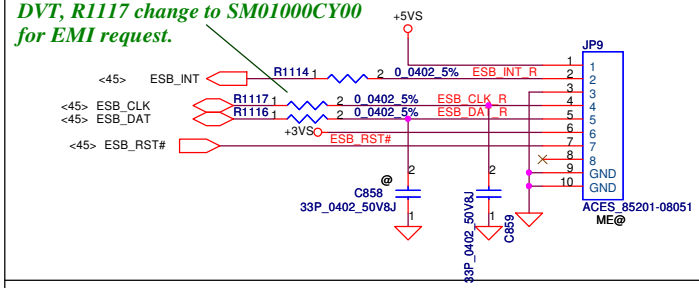


9/30 remove EC_SMB_CK2, EC_SMB_DA2

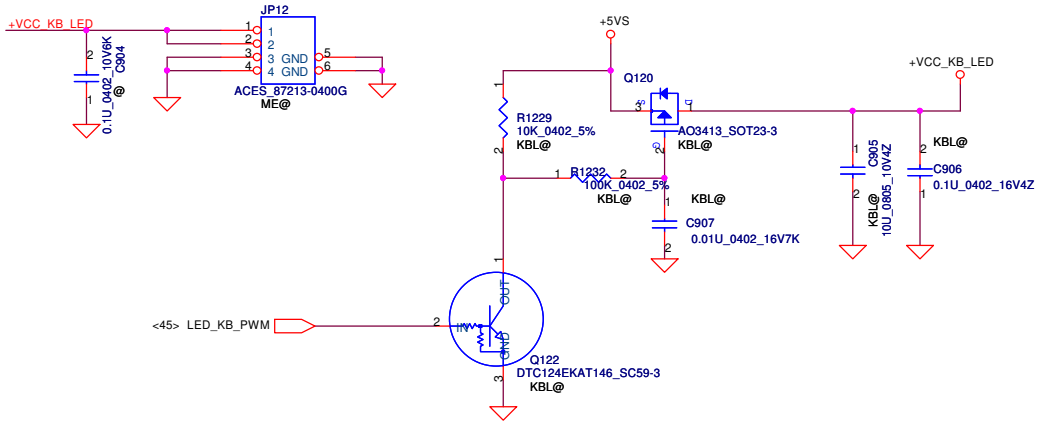
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Silder Bar Board Mdule Conn. 6pin

DVT, R1117 change to SM01000CY00 for EMI request.



KB Lighting CONN.4pin



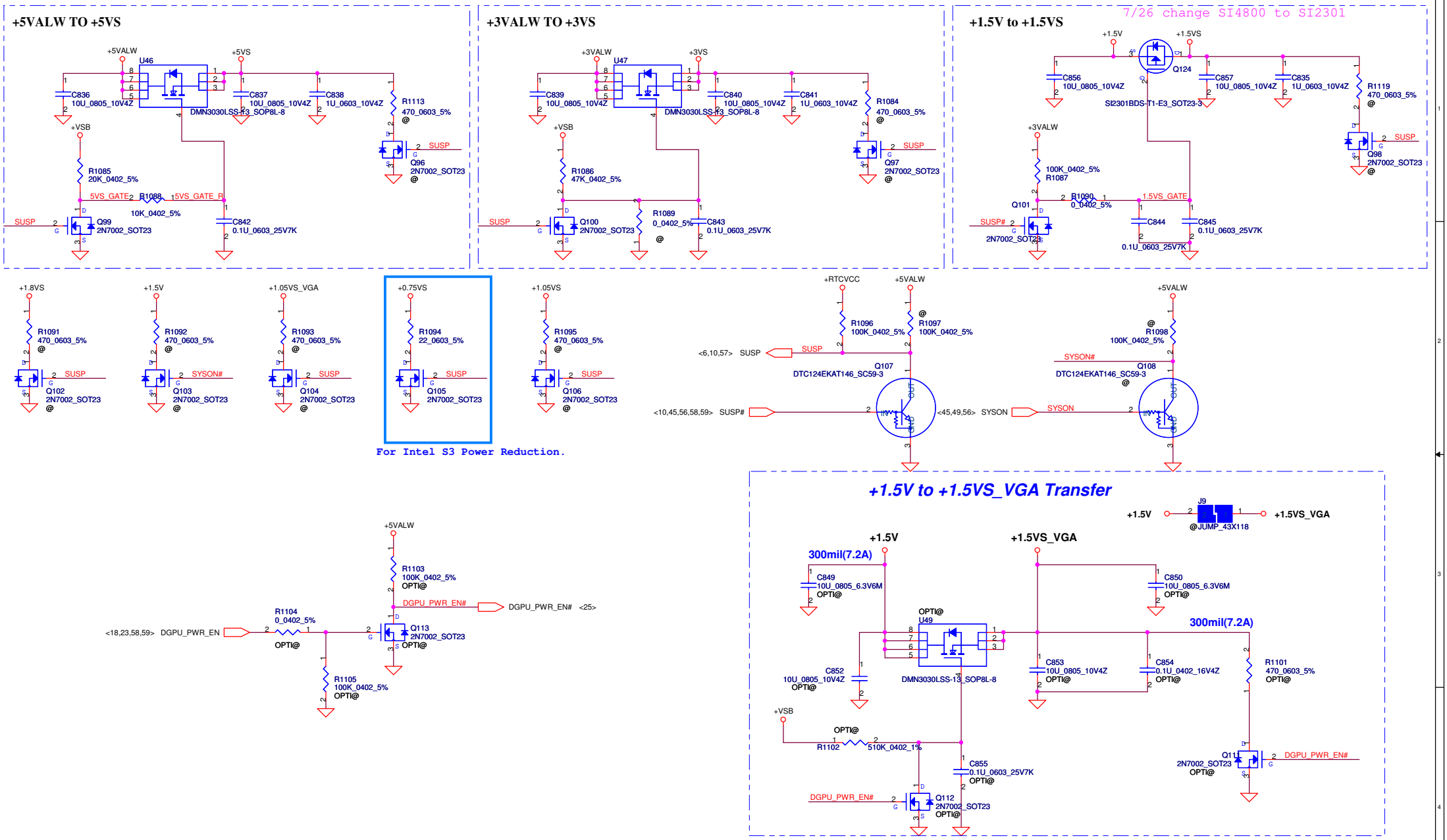
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics,Ltd.

Title: **other IO connector**

Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 50 of 63



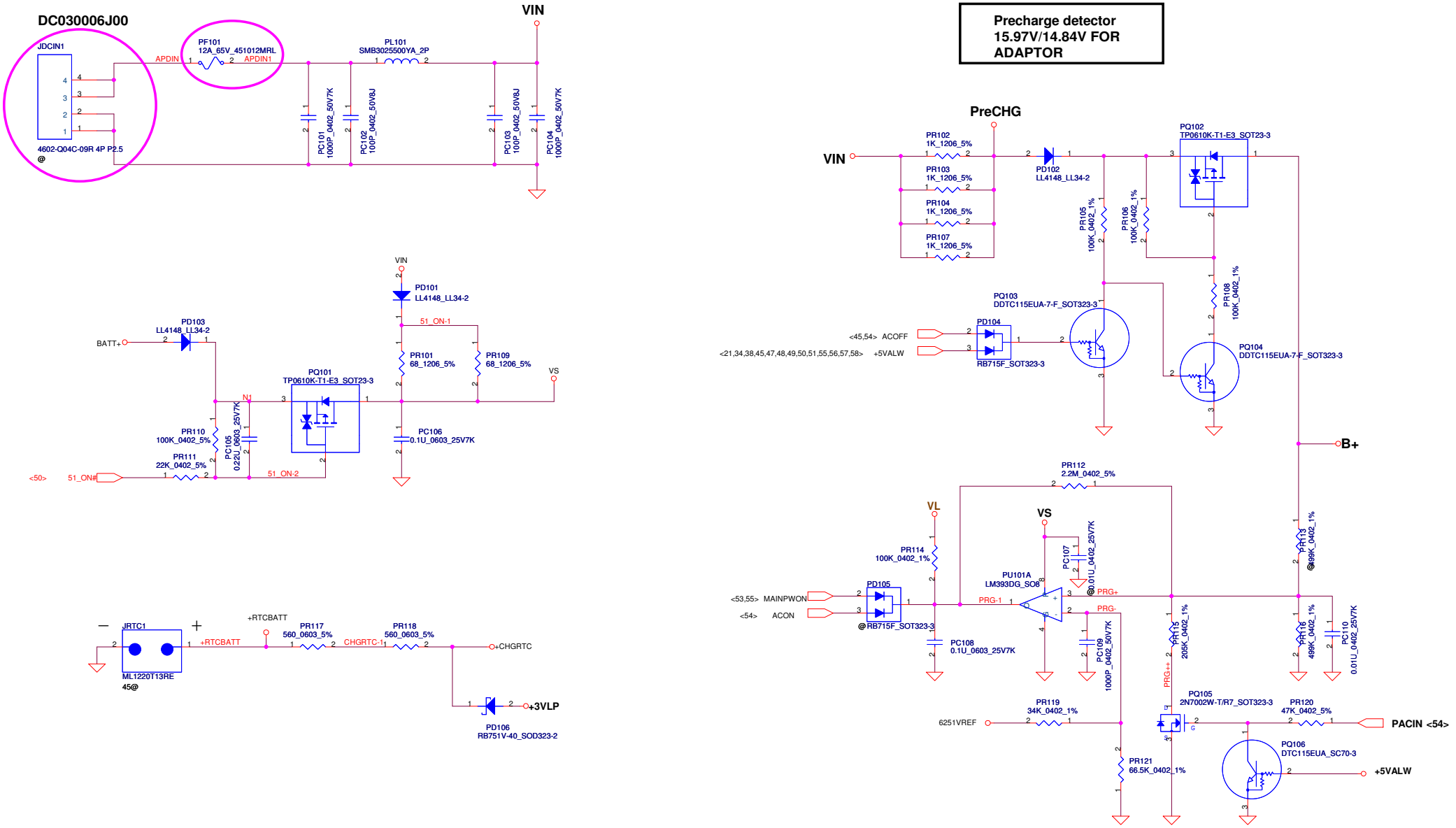
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 | Sheet 51 of 63



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

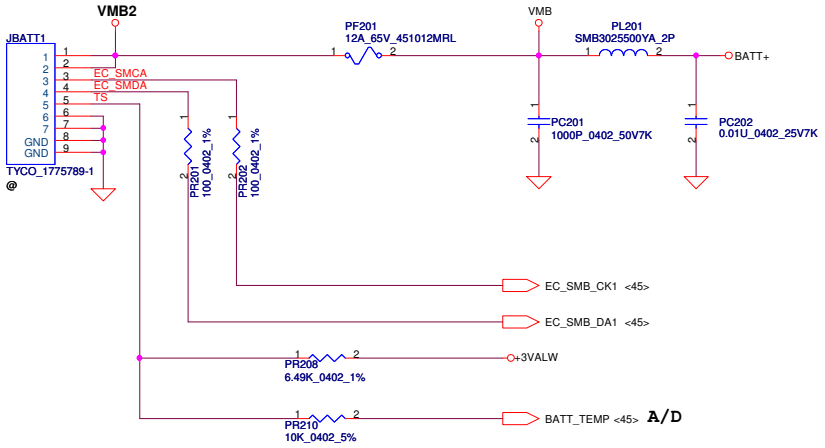
BATT ONLY

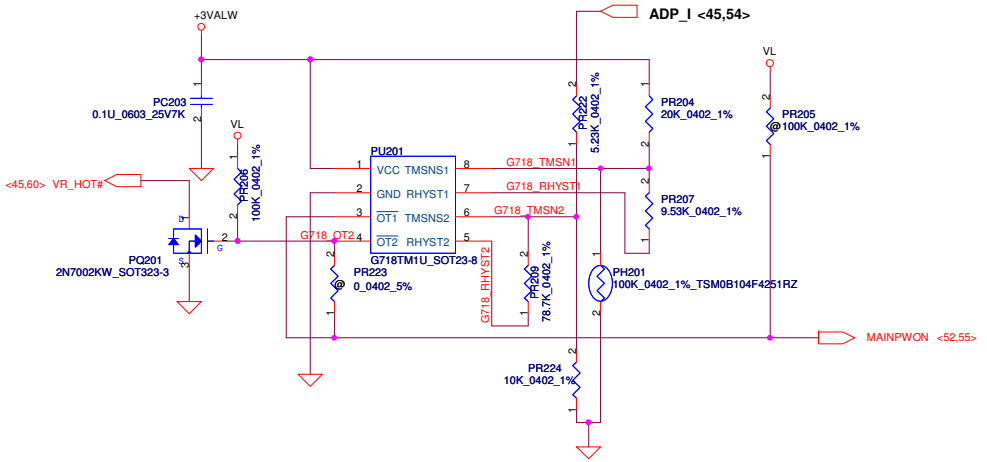
Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

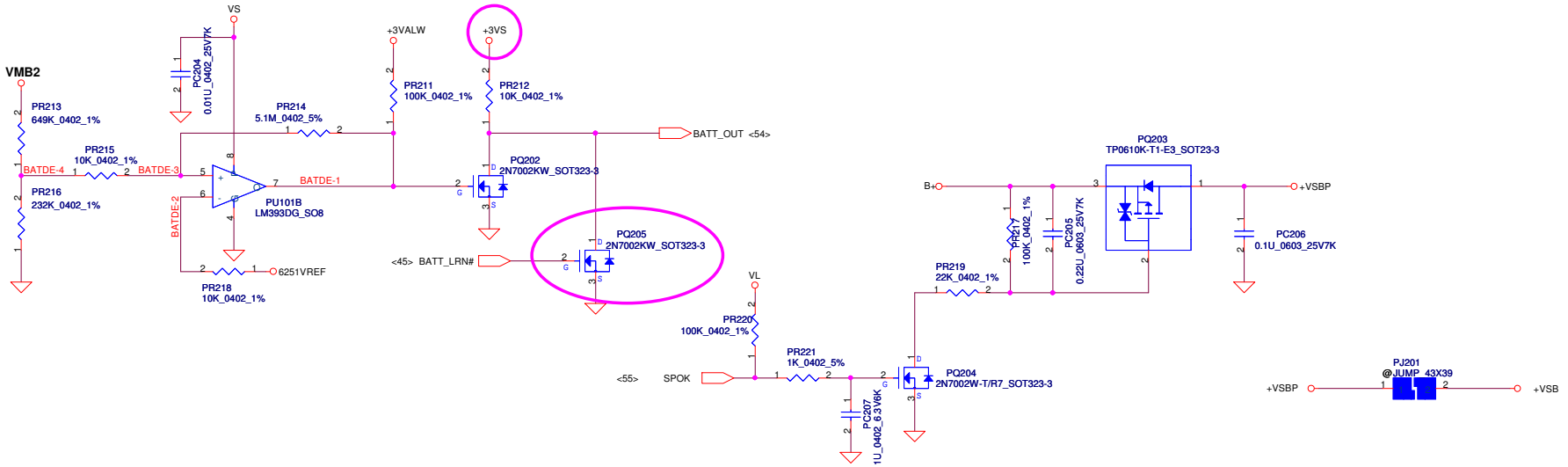
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.	
Title	PWR DCIN / Vin Detector /Pre-charge
Size: Custom	Document Number: PIQY0/Y1
Rev: 0.1	
Date: Monday, November 29, 2010	Sheet 52 of 63

PH201 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

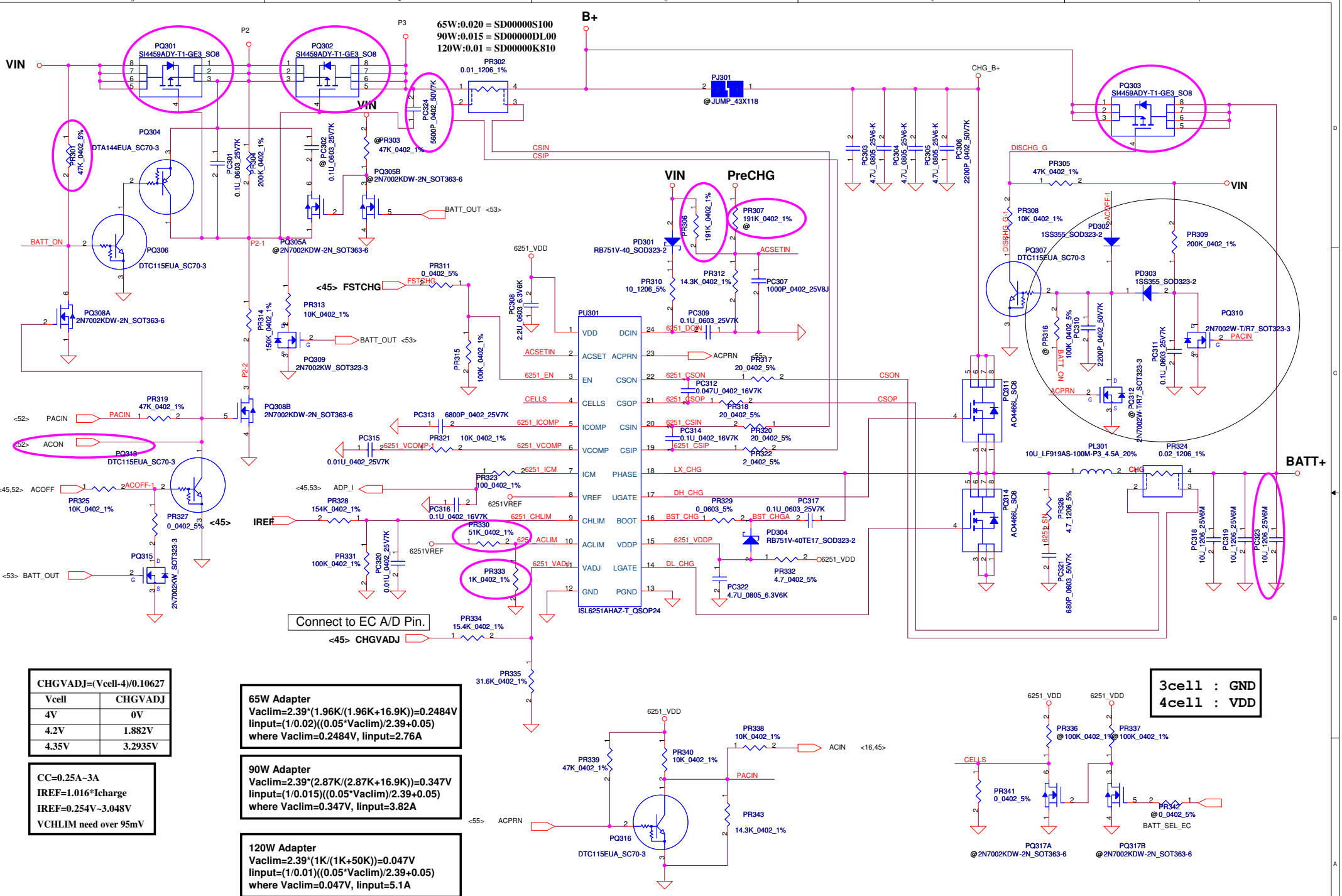






Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR-BATTERY CONN/OTP			
Size: Custom	Document Number: PIQY0/Y1		Rev: 0.1
Date: Monday, November 29, 2010	Sheet 53 of 63		



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

65W Adapter
Vaclim=2.39*(1.96K/(1.96K+16.9K))=0.2484V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2484V, Iinput=2.76A

90W Adapter
Vaclim=2.39*(2.87K/(2.87K+16.9K))=0.347V
Iinput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.347V, Iinput=3.82A

120W Adapter
Vaclim=2.39*(1K/(1K+50K))=0.047V
Iinput=(1/0.01)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.047V, Iinput=5.1A

65W : PR330=16.9K, PR333=1.96K
90W : PR330=16.9K, PR333=2.87K
120W : PR330=50K, PR333=1K

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

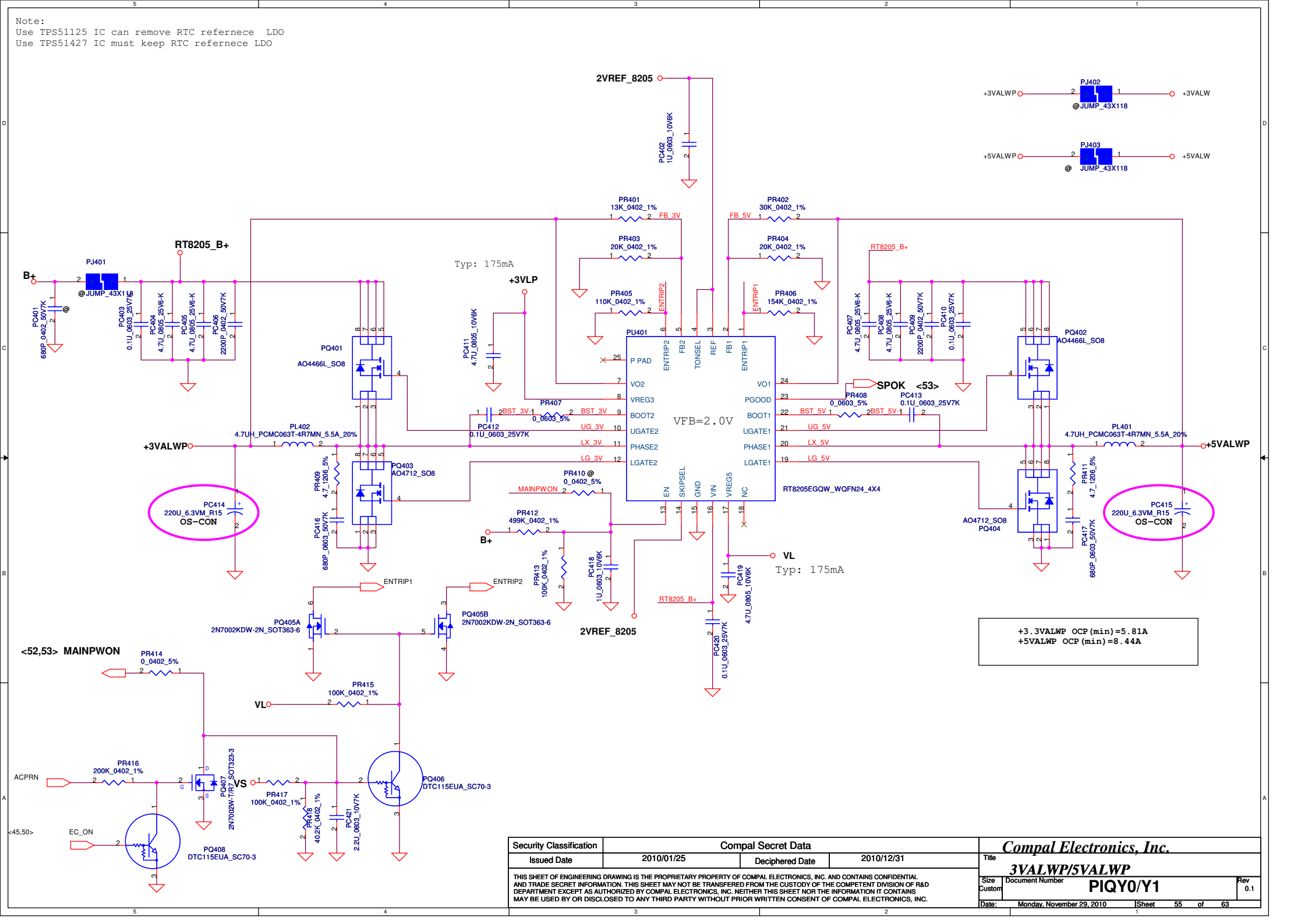
Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	PIQY0/Y1	0.2

Date: Monday, November 29, 2010 | Sheet 54 of 63

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



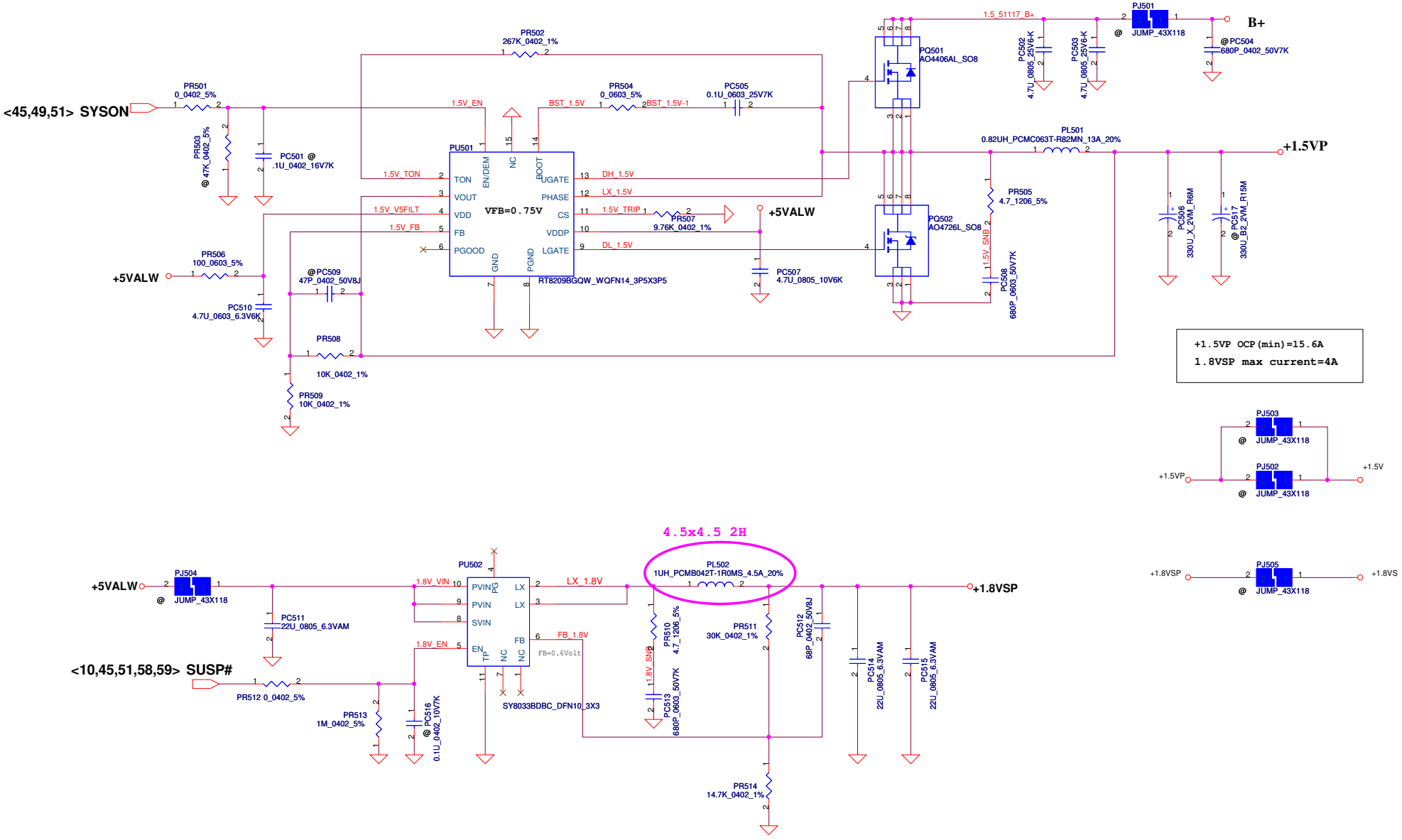
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	PIQY0/Y1	0.1

Date: Monday, November 29, 2010 Sheet 55 of 63



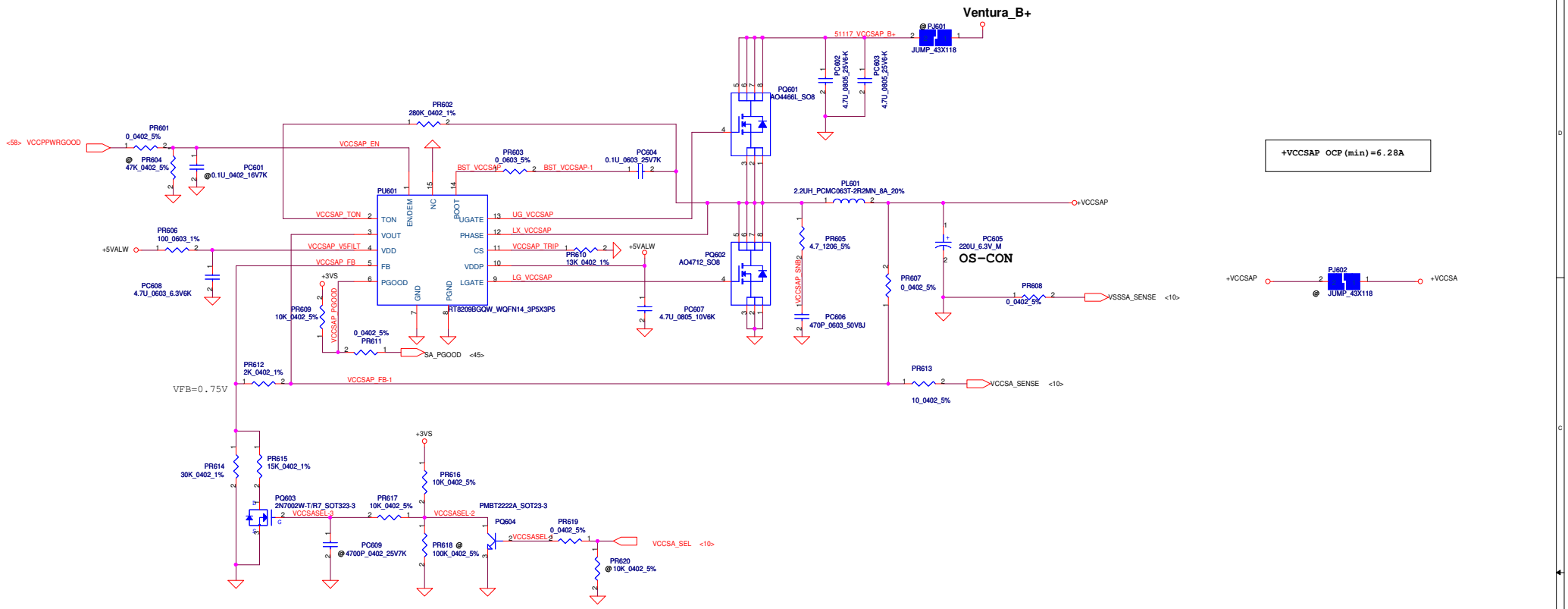
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: *PWR-+1.5VP/+1.8VSP*

Size	Document Number	Rev
Custom	PIQY0/Y1	0.1

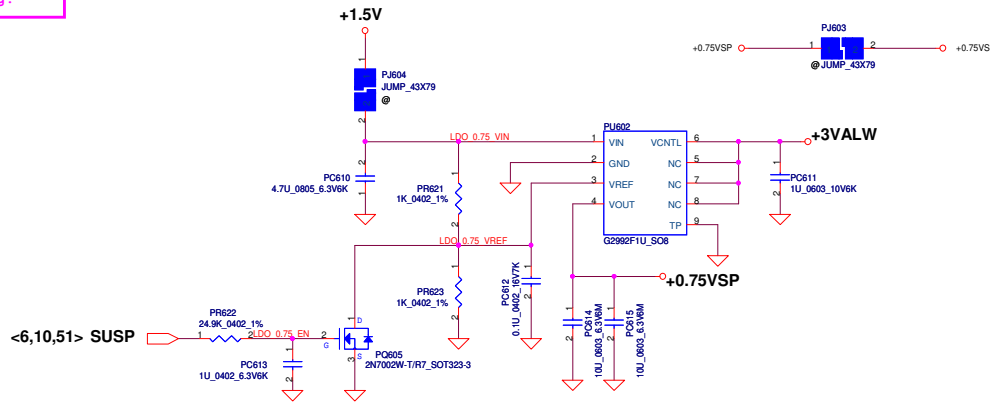
Date: Monday, November 29, 2010 | Sheet 56 of 63



+VCCSAP OCP(min)=6.28A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.



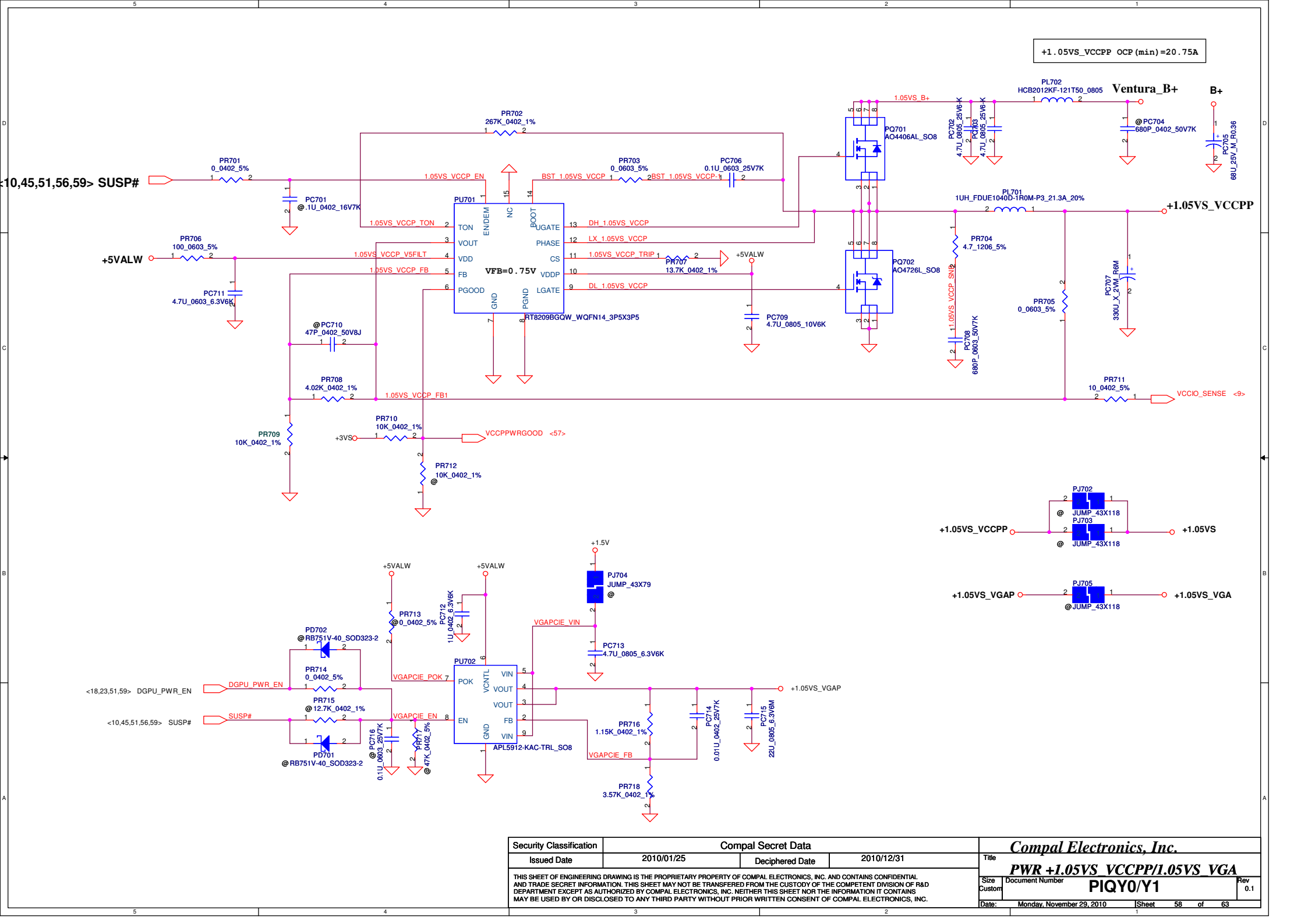
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +VCCSAP/+0.75VSP

Size	Document Number	Rev
C	PIQY0/Y1	0.1

Date: Monday, November 29, 2010 | Sheet 57 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/1.05VS_VGA

Size	Document Number	Rev
Custom	PIQY0/Y1	0.1

Date: Monday, November 29, 2010 Sheet 58 of 63

GS: PR840,PR845,PR847,PR853
GT/GT1:PR843,PR844.PR846,PR854

N12P-GS

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V

PU801 ISL6264CRZ-T_QFN40_6X6

PQ801 PQ802 PQ803 PQ804 TPCA8030-H_SOP-ADV8-5 / TPCA8028-H_SOP-ADVANCE8-5

PL801 HCB4532KF-800T90_1812

PL802 PL803 0.42UH_FDUE0640-R42M_20.2A_20%~D

7X7 4H_DCR=1.48mohm

PH801 NTCG103J4302RE B value=4300K

PQ807 PQ806 2N7002KW_SOT323-3

GPU_VID1 <23>

GPU_VID0 <23>

DGPU_PWR_EN <18,25,51,58>

SUSP# <10,45,51,56,58>

<19,23> VGA_PGOOD

<24> VDD_SENSE_VGA

<24> GND_SENSE_VGA

+VGA_CORE

Security Classification	Compal Secret Data
Issued Date	2006/12/12
Deciphered Date	2007/12/12

Compal Electronics, Inc.

Title: Power-VGA_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Monday, November 29, 2010 | Sheet 59 of 63

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

PR936
QC:19.1K
DC:19.6K

PR956
QC:3.724K
DC:2.15K

PR959
QC:1.54K=120A
DC:887=70A

QC: PC935
DC: PC933

PR943
0 ohm =>98A (Vboot=0v)
590 ohm=>91A (Vboot=0v)

B value=4700K

B value=4700K

B value=4250K

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Monday, November 29, 2010 | Sheet 60 of 63

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P18	Reserve R297	Reserve pull down for PCH GPIO53.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit Delete U55,C908,R1233,R1235,R1236,1238,R1230,R1231,Q121	Change KB light control from PWM to on/off.
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GPIO1.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swicth control inverter circuit.
~~7~~		~~P48~~	~~Add R1327~~	~~For CHG_ON# pull down.~~
8		P45	Stuff R996,R139,C815, unstuff R1000,C732,C733,Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GPIO12.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342,R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
				DVT TO PVT
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2009/01/06

Compal Electronics, Inc.

Title: PIR (HW)

Size	Document Number	Rev
Custom	LA-6882P	0.3

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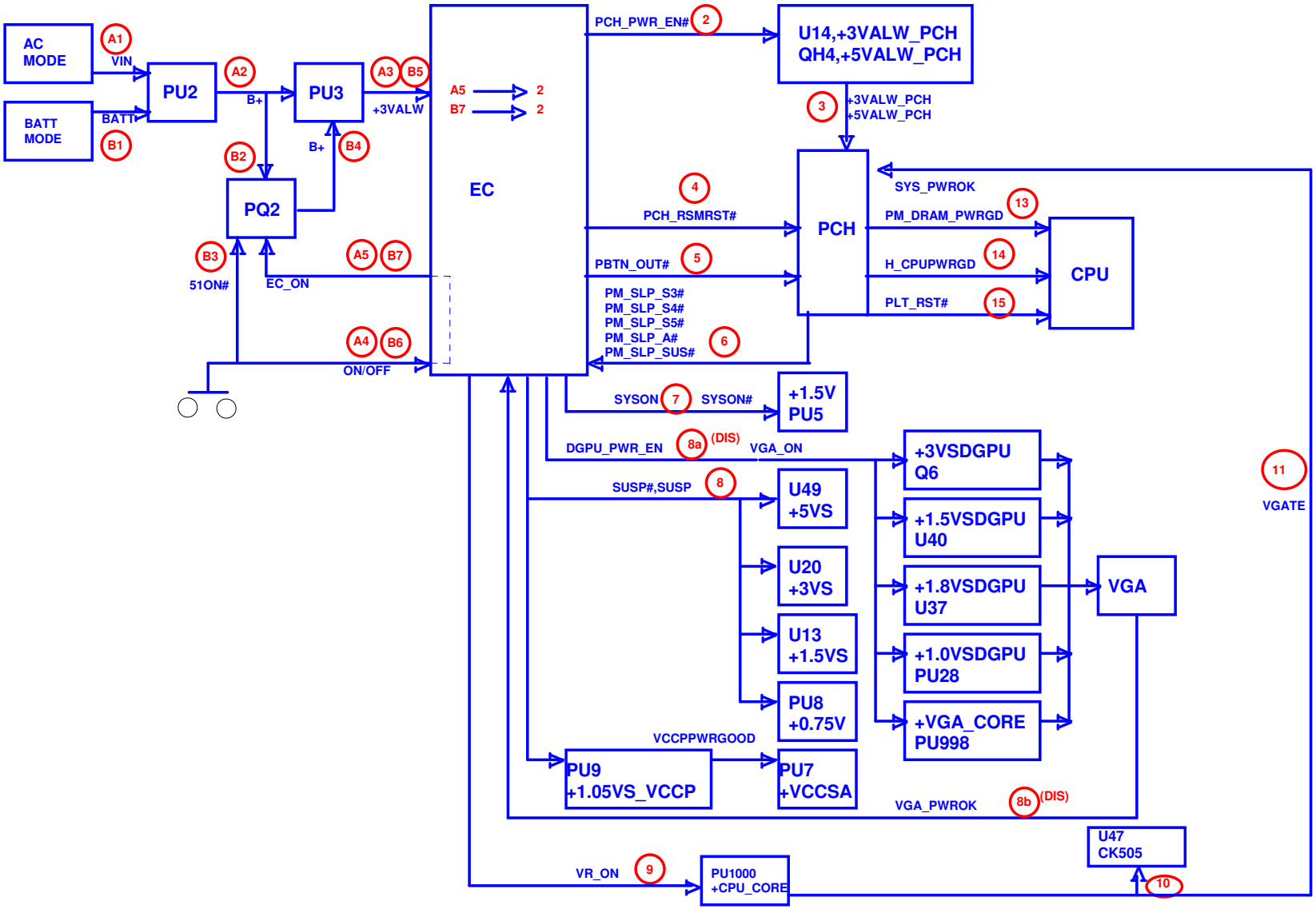

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	PIQY0 LA6881P	0.3

Date: Monday, November 29, 2010 Sheet 63 of 63